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Low-power Techniques for High-Performance Pipelined Analog to Digital Converter

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Low-power Techniques for High-Performance Pipelined Analog to Digital Converter

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Dedicated to my family.

Low-power Techniques for High-Performance Pipelined Analog to Digital Converter

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Low-power and small size analog to digital converters (ADCs) are the strategic building blocks in state of the art mobile wireless communication systems. Various techniques have been developed to reduce both power consumption and die area of the ADC. Among these, the opamp-sharing technique shows the most promise. In opamp-sharing, power and die area are saved by sharing one opamp between two successive pipeline stages. However, this technique suffers from the well-known memory effect drawback due to the absence of the reset phase that discharges the opamp's input parasitics.

In this dissertation, this drawback is solved by introducing a discharge phase before the opamp is used for the pipeline stages without compromising speed and resolution of the ADC. Further power and area reduction is achieved by using a capacitor-sharing technique. This technique reduces the effective load capacitance of the opamp by reusing the charge on the feedback

capacitor for the MDAC operation of the following stage, resulting in faster settling without increasing opamp power. The proposed low input-capacitance variable-g_m opamp also helps to reduce the memory effect and improves the settling behavior of the stage output by increasing the bandwidth of the opamp while input parasitics of the opamp are kept small.

The prototype designs of a 10-bit 50MSample/s pipelined ADC and a 14-bit 100MSample/s pipelined ADC implemented in 0.18μm CMOS technology demonstrate the effectiveness of the proposed techniques. The first ADC achieves 56.2dB SNDR and 72.7dB SFDR for a Nyquist input at full sampling rate while consuming 12 mW from a 1.8-V supply. The FOM, defined as, $\frac{power}{2^{ENOB}.Fs}$, is 0.46 pJ/step with Fin = 24.5MHz at 50MS/s. The second ADC achieves 72.4dB SNR and 88.5dB SFDR at 100MS/s with a 46MHz input and consumes 230mW from a 3V supply. The FOM of the second ADC is 0.69 pJ/step with Fin = 46MHz at 100MS/s.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

Mobile wireless communication systems are the major applications of recent analog-to-digital converters (ADCs). In these applications, the specifications of the ADC vary significantly across different receiver architectures [37], [35]. For example, IF-sampling superheterodyne receivers require high-speed and high-resolution ADCs, because intermediate frequency (IF) signals are directly converted to digital codes. On the other hand, direct conversion receivers, with more demanding front-end analog processing requirements, can significantly relax the specifications of the baseband ADC. These receiver architectures are shown in Fig. 1.1 and Fig. 1.2, respectively. IF-sampling superheterodyne receivers are mainly used in basestations and direct conversion receivers are used in mobile devices. Regardless of the receiver architectures, low-power consumption is the key specification. In addition to low-power operation, since multiple ADCs are integrated into a single-chip, a small size is also an important factor, especially for direct conversion receivers.

In this dissertation, the techniques that reduce both power consumption and die area are presented. In order to verify the effectiveness of the tech-

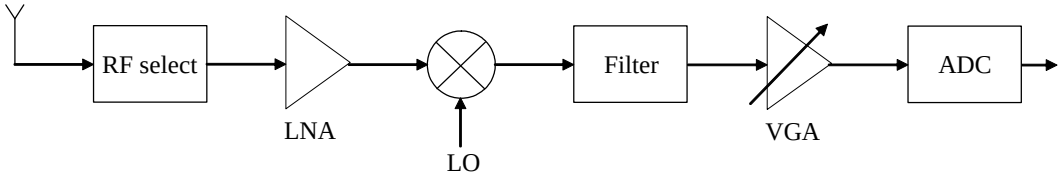


Figure 1.1: Block diagram of direct conversion receiver

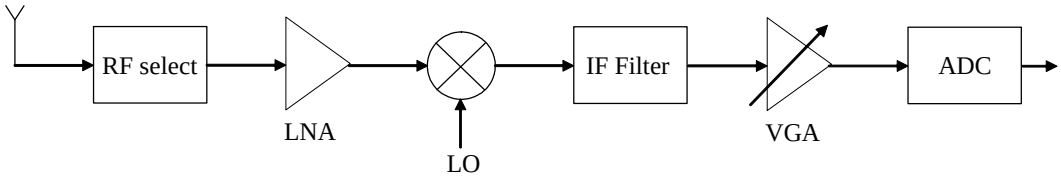


Figure 1.2: Block diagram of IF-sampling superheterodyne receiver

niques, two prototype ADCs, a 10-bit 50MSample/s and a 14-bit 100MSample/s pipelined ADCs are fabricated in 0.18μm CMOS technology.

1.2 Thesis Organization

In Chapter 2, fundamental limitations of short-channel MOSFETs are discussed. Short-channel effects such as mobility degradation, velocity saturation, V_T variation, and noise sources of MOSFET are explained. Matching of short-channel MOSFETs is also briefly discussed.

In Chapter 3, several ADC architectures are reviewed. Basic operation principles, advantages, and disadvantages of each architecture are also discussed.

In Chapter 4, power reduction techniques such as opamp-sharing and switched-opamp techniques are reviewed. Then, the proposed techniques are presented.

In Chapter 5, basic building blocks in the first prototype ADC are discussed in detail. Issues of actual implementation are also explained.

In Chapter 6, measurement results of the first ADC are presented along with a test setup.

In Chapter 7, circuit implementations of the second prototype ADC are discussed.

In Chapter 8, measurement results of the second ADC are presented.

Finally, conclusions are drawn in Chapter 9.

Chapter 2

Understanding of Short-Channel MOSFET

2.1 Short-channel Effects

As the dimensions of a metal-oxide-semiconductor field-effect transistor (MOSFET) continue to scale down, a square-law model becomes less accurate. Understanding of short-channel effects such as mobility degradation, velocity saturation, threshold voltage (V_T) variation, and drain-induced barrier lowering (DIBL) [34] becomes more and more important for analog IC designers to get a good performance out of a digital CMOS process.

2.1.1 Mobility Degradation

In scaled MOSFETs, the mobility of a carrier is severely reduced when gate-source voltage (V_{GS}) is high. With the large V_{gs}, a high vertical electric field ($E_\perp$) draws the carriers in the channel closer to the surface of the silicon, resulting in reduction of the carrier mobility. This is shown in Fig. 2.1. There are two main scattering mechanisms. One is surface roughness and the other one is coulombic interaction with fixed charges in oxide. With mobility degradation, the effective mobility (μ_{eff}) can be expressed as

$$\mu_{eff} = \frac{\mu_n}{1 + \theta(V_{GS} - V_T)} \tag{2.1}$$

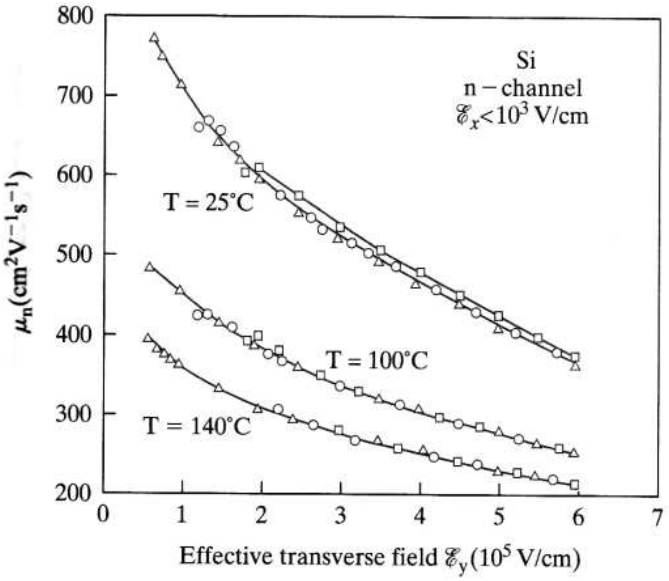


Figure 2.1: Electron mobility versus vertical electric field [34]

where μ_n is the mobility with zero $E_\perp$, θ is a technology dependent parameter, which is inversely proportional to the oxide thickness, and V_T is a threshold voltage. In the presence of the mobility degradation, the drain current (I_D) in the linear region can be written as

$$I_D = \mu_{eff} C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS} \tag{2.2}$$

where $\frac{W}{L}$ is the aspect ratio of a MOSFET, C_{OX} is the gate-oxide capacitance, and V_{DS} is the drain-source voltage of a MOSFET. By taking the derivative of I_D with respect to V_{GS} and considering the dependence of μ_{eff} on V_{GS}, the transconductance (g_m) can be expressed as

$$g_m = C_{OX} \frac{W}{L} \underbrace{\left[(V_{GS} - V_T) \frac{\partial \mu_{eff}}{\partial V_{GS}} + \mu_{eff} \right]}_{=\mu_{fe}} V_{DS} = C_{OX} \frac{W}{L} \mu_{fe} V_{DS} \tag{2.3}$$

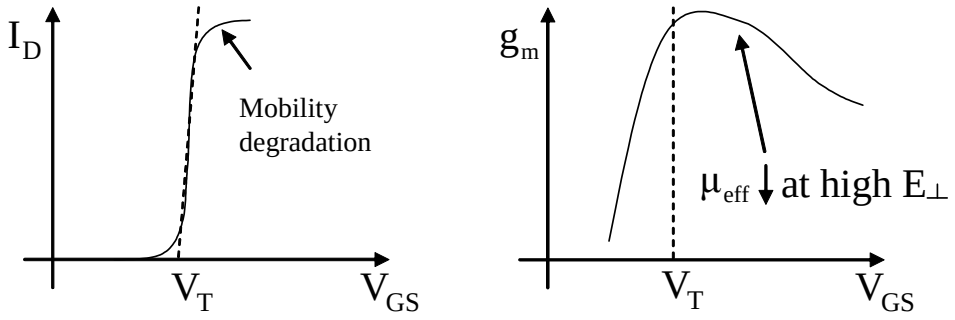


Figure 2.2: Effect of mobility degradation on I_D and g_m

where μ_{fe} is the field effect mobility and $\mu_{fe} < \mu_{eff}$. As shown in Fig. 2.2, the mobility degradation lowers the current capability and g_m of a MOSFET as V_{GS} increases.

2.1.2 Velocity Saturation

Carrier mobility is also affected by a lateral electric field (E_{lat}). As shown in Fig. 2.3, when V_{DS} is small, the carrier velocity (v_c) is proportional to E_{lat}, which can be expressed as $\frac{V_{DS}}{L}$. As V_{DS} increases, so does E_{lat} and v_c approaches a saturated value, which is known as a thermal velocity. v_c can be expressed as

$$\begin{aligned} v_c &= \frac{\mu_{eff} E_{lat}}{1 + E_{lat}/E_{sat}} \quad for \quad E_{lat} < E_{sat} \\ &= v_{sat} \qquad\qquad\qquad for \quad E_{lat} \geq E_{sat} \end{aligned} \tag{2.4}$$

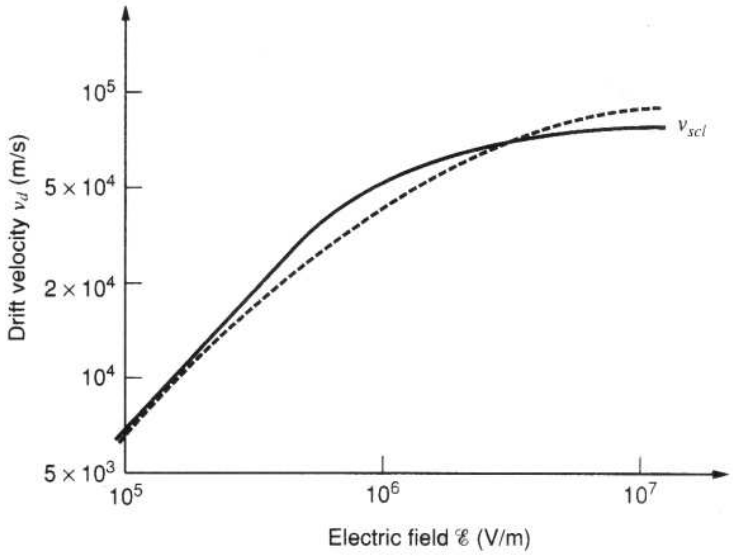


Figure 2.3: Typical electron velocity versus lateral electric field [16]

where E_{sat} is the lateral electric field when v_c=v_{sat}, and it can be written as

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}} \tag{2.5}$$

With velocity saturation, I_D in the linear region should be modified as below,

$$I_D = \mu_{eff} C_{OX} \frac{W}{L}(V_{GS} - V_T - V_{DS}/2)V_{DS}(\frac{1}{1 + \frac{V_{DS}}{E_{sat}L}}) \tag{2.6}$$

where $\frac{V_{DS}}{E_{sat}L}$ accounts for the difference between drain currents of a short-channel and a long-channel MOSFETs. For example, if $v_{sat} = 10^7 cm/s$, $\mu_{eff} = 400 cm^2/V - s$, L=100nm, and $V_{DS} = 1V$, then $\frac{V_{DS}}{E_{sat}L} = 2$ and I_D of a short-channel MOSFET is only one-third of that of a long-channel MOSFET. I_D in the saturation region should be also modified as below,

$$I_D = \mu_{eff} C_{OX} W(V_{GS} - V_T - V_{dsat})v_{sat} \tag{2.7}$$

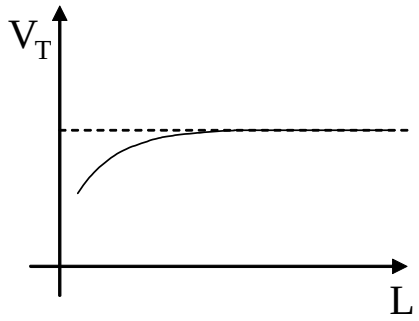


Figure 2.4: V_T versus channel length

where V_{dsat} is V_{DS} when $v_c = v_{sat}$, which can be expressed as,

$$V_{dsat} = \frac{1}{1/(E_{sat}L) + 1/(V_{GS} - V_T)} \tag{2.8}$$

In long-channel MOSFETs, since $1/(E_{sat}L)$ approaches 0, $V_{dsat} \simeq (V_{GS} - V_T)$. However, in short-channel MOSFETs, as L decreases, $1/(E_{sat}L)$ increases and $V_{dsat} < (V_{GS} - V_T)$.

2.1.3 V_T Variation

Fig 2.4 shows V_T variation with channel length (L). As L decreases, so does V_T. This can be explained by the charge-sharing effect. As shown in Fig. 2.5, the depletion regions of source and drain are extended to channel depletion region. The extended depletion regions become comparable to the channel depletion region as L decreases, resulting in reduction of channel charge (Q_D). V_T can be expressed as

$$V_T = V_{FB} + 2\Phi_F + \frac{Q_D}{C_{OX}} \tag{2.9}$$

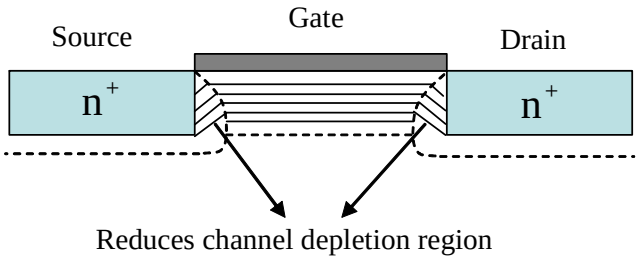


Figure 2.5: Charge-sharing model of NMOS transitor

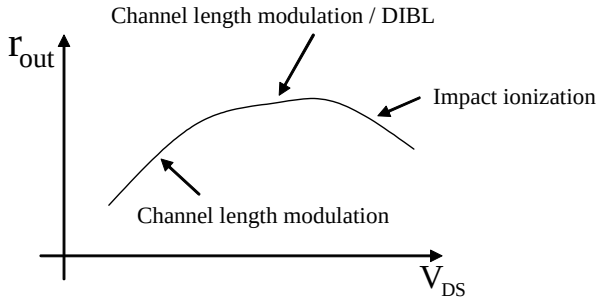


Figure 2.6: Output resistance versus V_{DS}

where V_{FB} is the flat-band voltage and $\Phi_F = \frac{kT}{q} ln \frac{N_{sub}}{n_i}$. From the equation above, since Q_D is reduced because of charge-sharing between source/drain and channel depletion regions, V_T also decreases.

2.1.4 Output Resistance Variation with V_{DS}

Output resistance (r_{out}) of a short-channel MOSFET working in the saturation region varies a lot with V_{DS}. This is depicted in Fig. 2.6. When V_{DS} is relatively small, a variation of r_{out} is mainly caused by the channel length modulation. As V_{DS} increases, the depletion region of drain extends to

the source, and potential barrier between source and channel reduces due to DIBL. This lowers V_T and increases I_D. In short-channel MOSFETs, DIBL becomes more significant and V_T of a MOSFET working in the saturation region is smaller than that of a MOSFET working in the linear region. As V_{DS} further increases, r_{out} starts to decreases rapidly because of impact ionization. In short-channel MOSFETs, when V_{DS} is large, high lateral electric field accelerates the carriers in the channel. The accelerated carriers, which are also called as hot carriers, hit the silicon atoms, creating new electron and hole pairs. These newly generated electron and hole pairs increase the drain and substrate currents and reduce r_{out}.

2.2 Noise

Noise of a MOSFET often limits the performance of many analog and mixed-signal ICs. Thus, its effect on switched-capacitor (SC) circuits needs to be discussed. There are two main noise sources, thermal and flicker noises, in a MOSFET [16], [30]. However, since the thermal noise is often dominant factor, its effect on SC circuits is discussed in this section.

2.2.1 Flicker Noise

There are many broken bonds, which are called dangling bonds, between substrate and gate oxide. These defects generate extra energy states. These energy states capture and later release the carriers in the channel in a random fashion, generating noise in the drain current. Since this capturing

and releasing process happens very slowly, the energy of the noise signal is concentrated at low frequencies. The flicker noise is often modeled as a noise voltage in series with the gate terminal of a MOSFET. The power spectral density (PSD) can be expressed as,

$$S_f(f) = \frac{K}{WLC_{OX}f}(V^2/Hz) \tag{2.10}$$

where K is a process parameter. As shown in the equation, the flicker noise is not white, its spectrum is inversely proportional to the frequency and concentrated at low frequencies. It is also inversely proportional to the area of the transistor. Thus, by increasing W or L, its effect can be reduced to an insignificant level. Techniques such as correlated double sampling (CDS) and chopper stabilization can also reduce the flicker noise [8].

2.2.2 Thermal Noise

Thermal noise is generated by a random thermal motion of the carriers in the channel. Its noise spectrum is proportional to absolute temperature (T) and is white. For a MOSFET operating in the triode region, its PSD is given by

$$S_t(f) = 4kTR_{on}(V^2/Hz) \tag{2.11}$$

where k is the Boltzmann constant, k=$1.38\times10^{-23}J/K$ and R_{on} is the on-resistance of a MOSFET in ohms. For a MOSFET operating in the saturation region, it can be modeled as a current noise source in parallel with the channel. its PSD is given by

$$S_t(f) = 4kT\gamma g_m(A^2/Hz) \tag{2.12}$$

where γ is the technology dependent constant, varying between 2/3 and 2. Since γ is close to 2 for a short-channel MOSFET, it is assumed that γ is 2 for the rest of this chapter.

2.2.3 Noise in Opamp

Thermal noise in a typical opamp can be modeled as a noise current source or a noise voltage source. This is depicted in Fig. 2.7. Noise of a transistor M_{N0} is not considered, because it appears as a common-mode noise. Noise of the cascode transistor (M_{N3}, M_{N4}, M_{P3}, and M_{P4}) is also ignored, because a voltage gain of the cascode transistor is relatively low due to a source degeneration effect. Noise of input transistor (M_{N1} or M_{N2}) can be modeled as a noise voltage source (V_{N1} or V_{N2}) and can be expressed as

$$\overline{V_N^2}\,(=\overline{V_{N1}^2}\,or\,\overline{V_{N2}^2}) = \frac{4kT\gamma}{g_{mN}} = \frac{8kT}{g_{mN}} \tag{2.13}$$

where γ is assumed to be 2 and g_{mN} is the transconductance of M_{N1} and M_{N2}. The noise of current source transistors (M_{P1} and M_{P2}) is modeled as a noise current source (I_{N1} and I_{N2}) and can be expressed by

$$\overline{I_N^2}\,(=\overline{I_{N1}^2}\,or\,\overline{I_{N2}^2}) = 4kT\gamma g_{mP} = 8kTg_{mP} \tag{2.14}$$

where g_{mP} is the transconductance of M_{P1} and M_{P2}. All these noise sources can be modeled as a equivalent noise voltage source at the gate of input transistors as shown in Fig. 2.8. The total equivalent noise V_{Neq} can be expressed as

$$\overline{V_{Neq}^2} = \overline{V_{Neq1}^2} + \overline{V_{Neq2}^2} = \frac{16kT}{g_{mN}}(1+\frac{g_{mP}}{g_{mN}}) \simeq \frac{24kT}{g_{mN}} \tag{2.15}$$

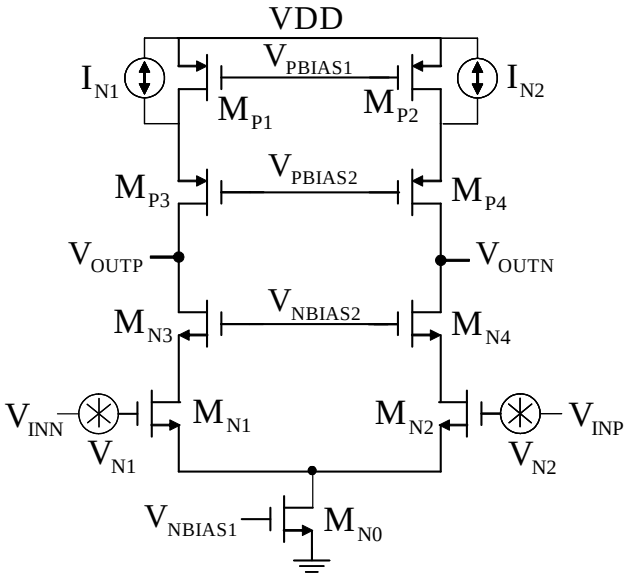


Figure 2.7: Noise sources in a telescopic opamp

It was assumed that $g_{mN} \simeq 2g_{mP}$ for simplicity. This equivalent noise will be used in the SC amplifier in the next section.

2.2.4 Noise in SC Amplifier

Fig. 2.9 shows a typical SC amplifier during the amplification phase with a equivalent opamp noise. The opamp is assumed to be a single-pole system with high DC gain. With this assumption, the transfer function of the SC amplifier, H(s), can be expressed as follows

$$H(s) = \frac{1}{\beta} \frac{1}{(1 + s/w_p)} \tag{2.16}$$

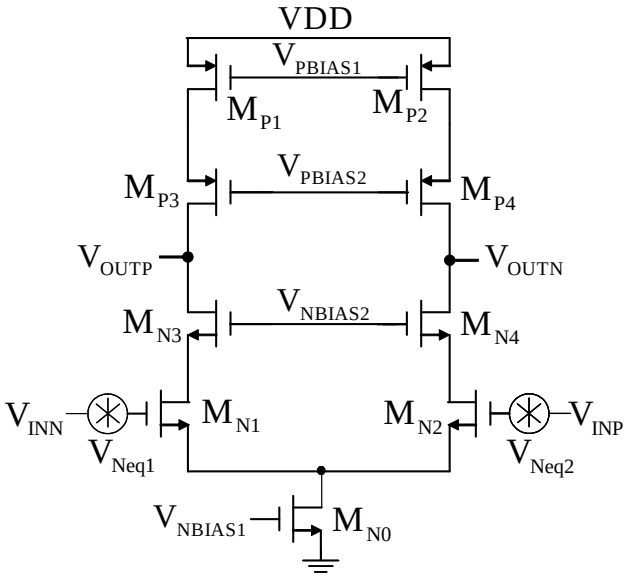


Figure 2.8: Equivalent noise source in a telescopic opamp

where the feedback factor,β=$\frac{C_2}{C_1+C_2+C_p}$ and w_p is the closed-loop pole, which is given by

$$w_p = \frac{G_m}{C_{Leff}} \tag{2.17}$$

where G_m is the transconductance of the opamp and C_{Leff} is the effective output load and C_{Leff}=C_L+(1-β)C_2 =C_L+$\frac{(C_1+C_p)C_2}{C_1+C_2+C_p}$. Since the white opamp noise is shaped by H(s), the total output noise of the SC amplifier can be calculated by integrating the shaped white noise from 0 to infinite frequency

$$\overline{v_{out}} = \int_0^\infty \overline{V_{Neq}^2}|H(j2\pi f)|^2 df = \frac{24kT}{g_{mN}}\frac{1}{\beta^2}\frac{w_p}{4} \tag{2.18}$$

Since $g_{mN} \simeq G_m$,

$$\overline{v_{out}} = 6kT\frac{1}{\beta^2 C_{Leff}} \tag{2.19}$$

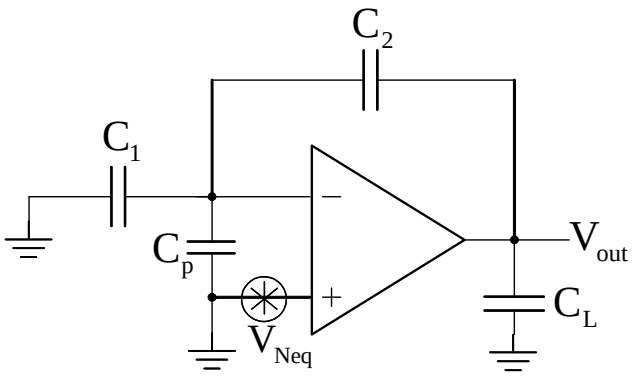


Figure 2.9: SC amplifier with a equivalent opamp noise

The equation (2.19) shows that the total output noise is a strong function of the feedback factor, that is, as the gain of SC amplifier increases, so does the output noise. It is also shown that the total output noise is independent of g_m of the opamp. This is because the opamp noise is inversely proportional to g_m, while the bandwidth of H(s) is proportional to g_m. Fig. 2.10 shows a SC amplifier with a two-phase nonoverlapping clock. The switch on-resistance (R_{ON}) also generates the output noise. To simplify the noise analysis, it is assumed that the opamp has sufficiently high-DC gain and wide bandwidth. This assumption is generally valid, because high-DC gain is required to suppress the nonlinearity of the opamp and the bandwidth of the opamp should be wide enough to meet the settling requirement (usually much wider than the sampling rate). With these assumptions, at the end of Φ_1, the noise charge sampled on the sampling capacitor (C_1) is given by

$$\overline{Q_n^2} = kTC_1 \tag{2.20}$$

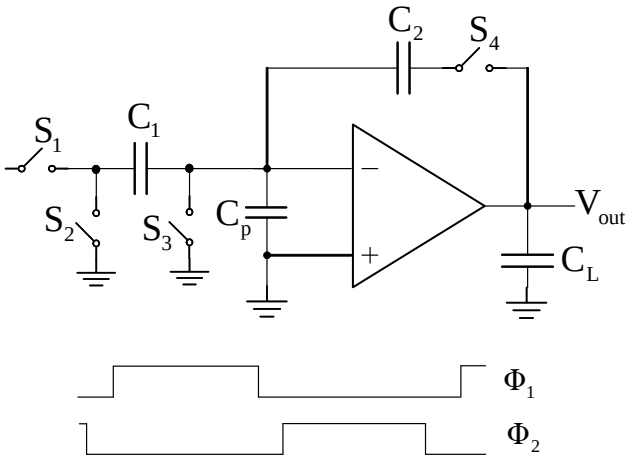


Figure 2.10: SC amplifier with timing diagram

Then, during the amplification phase (When Φ_2 is high), the charge stored on C_1 is also given by kTC_1. From the charge conservation rule, the charge stored on the feedback capacitor (C_2) during phase Φ_2 becomes $2kTC_1$. Thus, the mean squared value of the output noise can be expressed by

$$\overline{V_{o,n}^2} = 2\frac{kTC_1}{C_2^2} \tag{2.21}$$

In case of a fully differential amplifier, since the positive and negative output noise signals are uncorrelated to each other, the noise in equation (2.21) should be doubled and can be expressed by

$$\overline{V_{o,n}^2} = 4\frac{kTC_1}{C_2^2} \tag{2.22}$$

The total output noise can be found by adding the opamp noise and the noise from R_{ON} and is given by

$$\overline{V_{total,n}^2} = 6kT\frac{1}{\beta^2 C_{Leff}} + 4\frac{kTC_1}{C_2^2} = 4kT(\frac{3}{2\beta^2 C_{Leff}} + \frac{C_1}{C_2^2}) \tag{2.23}$$

For example, if gain of SC amplifier = 1 and β=0.5, that is $C_p \ll C_1 = C_2 = C_L = C$, then the total output noise becomes

$$\overline{V_{total,n}^2} = \frac{20kT}{C} \tag{2.24}$$

From the noise analysis above, it can be shown that the output noise of a SC amplifier is inversely proportional to β^2 and C_L. As a amplifier gain increases (or β decreases), the output noise also increases.

2.3 Matching

As the dimension of a MOSFET keeps decreasing, matching of MOSFETs becomes more important. The matching property of mismatch parameter ΔP of a MOSFET can be characterized by Gaussian distribution with a zero mean and variance of σ^2 [14],

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2 \tag{2.25}$$

where A_P is the area proportionality constant for parameter P, WL is the area of a MOSFET, S_P describes the variation of P with the spacing, and D is the spacing between two transistors. There are two mismatch parameters in a MOSFET. One is the $\Delta\beta$ mismatch and the other one is the ΔV_T mismatch. The current factor is given by

$$\beta = C_{ox}\mu\frac{W}{L}, \tag{2.26}$$

where μ is the carrier mobility. The variances of the ΔV_T mismatch and current factor mismatch ($\Delta\beta$) can be expressed as

$$\sigma^2(V_T) = \frac{A_{VT0}^2}{WL} + S_{VT0}^2 D^2 \tag{2.27}$$

$$\sigma^2(\beta) = \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \tag{2.28}$$

In most cases, the device mismatch is dominated by the ΔV_T mismatch. The variance of the ΔV_T mismatch and the current factor are inversely proportional to the device area.

With the understanding of fundamental limitations of short-channel MOSFETs discussed in this section, a simple square-law model can still give very meaningful insights to analog IC designers. These insights are often very useful to solve some critical problems in analog ICs without resorting to computer simulations.

Chapter 3

Fundamentals of ADC

Modern ADCs are divided into two different categories, Nyquist-rate ADCs and oversampling ADCs[4]. Nyquist-rate ADCs produce a series of output codes in which each code has a one-to-one correspondence with one sample of an analog input signal. Oversampling ADCs sample an analog input at a much higher rate than the Nyquist-rate of the input signal and, obtains the desired SNR by filtering out quantization noise that is shaped out side of the signal bandwidth. Flash, successive approximation, and pipeline ADCs are Nyquist-rate type. Sigma-delta ADCs belong to oversampling ADC category. Each ADC structure has its own merits and drawbacks. It will be discussed in the following sections.

3.1 Nyquist-Rate ADCs

3.1.1 Flash ADC

A flash ADC [22], [42] has a parallel architecture, thus it is the fastest ADC architecture. Fig. 3.1 shows a block diagram of a flash ADC. It consists of comparators, a resistor ladder and a decoder. The resistor ladder divides the reference voltage into equally spaced voltages, and the comparators com-

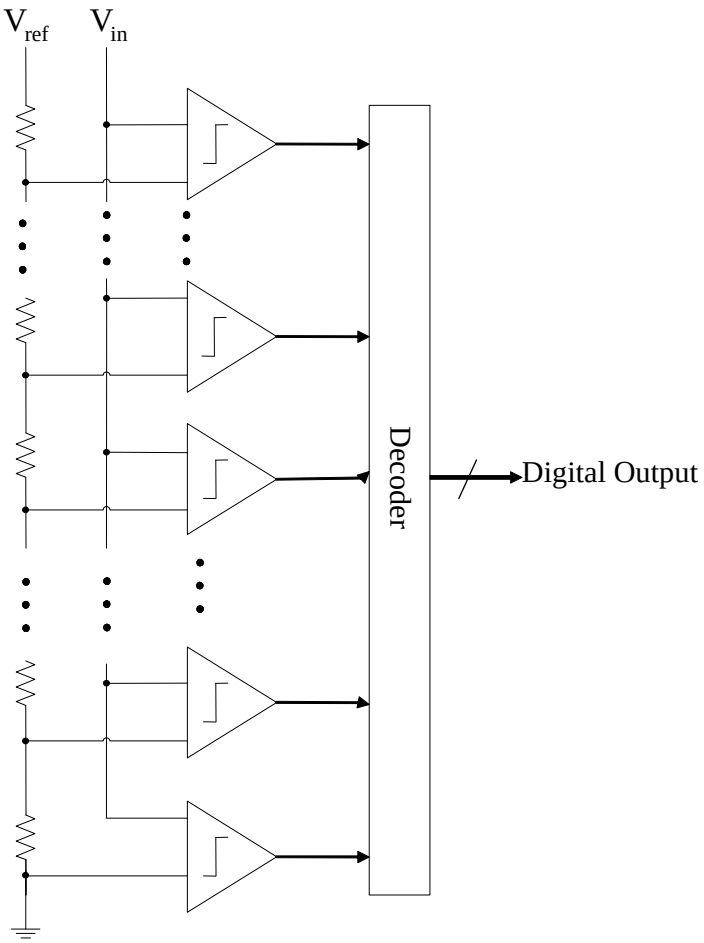


Figure 3.1: Block diagram of Flash ADC

pare the input signal with these voltages. If the input signal is larger than the certain reference voltages, the comparator produces "1", otherwise it produces "0". The comparator outputs constitute a thermometer code, which is then converted into binary code by the decoder. The disadvantage of this ADC is the hardware complexity. The required hardware increases exponentially with the number of bits.

3.1.2 Successive Approximation ADC

A successive approximation ADC employs a binary search ADC architecture [45], [28]. It uses a binary search algorithm in a feedback loop. As shown in Fig. 3.2, the ADC consists of a sample and hold circuit, a comparator, a DAC and a control logic which includes a shift register, decision logic and a decision register. The operation of the successive approximation ADC is as follows. The control logic sets the DAC input to the midscale (1000), thus the DAC produces the midscale analog output, and the DAC output is subtracted from the sampled input, then the difference is quantized by the comparator. According to the comparator output, the DAC output stays unchanged or decreases to (0000). The second MSB is set to one, (X100), the DAC output updates accordingly, the successive approximation register is decreased to (X000) or stays unchanged. The process repeats until the target accuracy is achieved. The most important advantage of the successive approximation ADC is it requires very little hardware. However, successive approximation

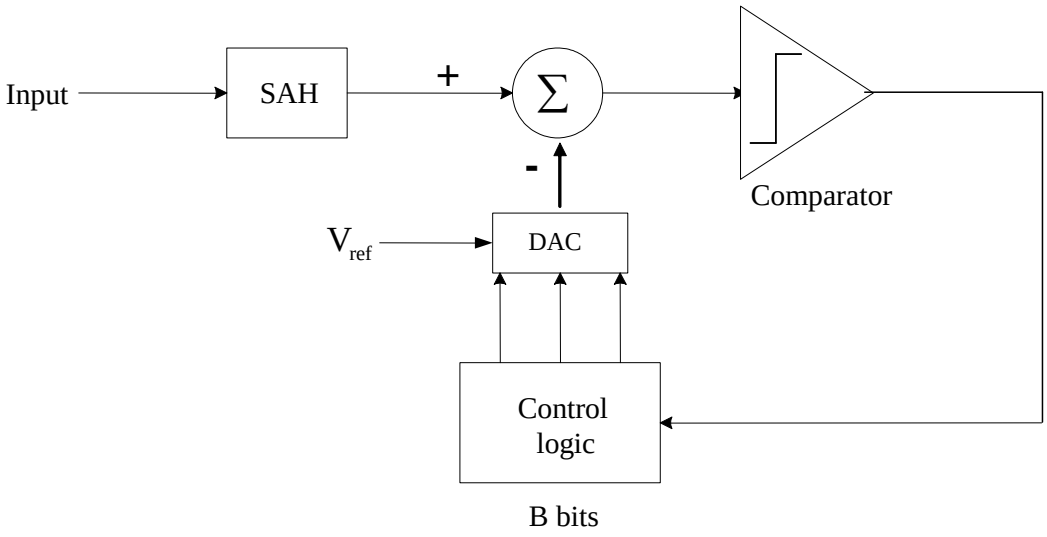


Figure 3.2: Block diagram of successive approximation ADC

ADC can only resolve one bit per cycle. Consequently, it is much slower than the flash ADC.

3.1.3 Pipelined ADC

A pipelined ADC exploits the concept of pipelined system in digital circuits [36], [41], [25]. It consists of a sample and hold circuit, sub-ADC, DAC and residue amplifier. All the stages process the samples concurrently at any given time, and each stage performs the same function with different samples. First of all, the sample and hold circuit samples the residue from the previous stage, and the sub-ADC converts the residue into a digital code. This digital code is converted to analog voltages and subtracted from the residue of

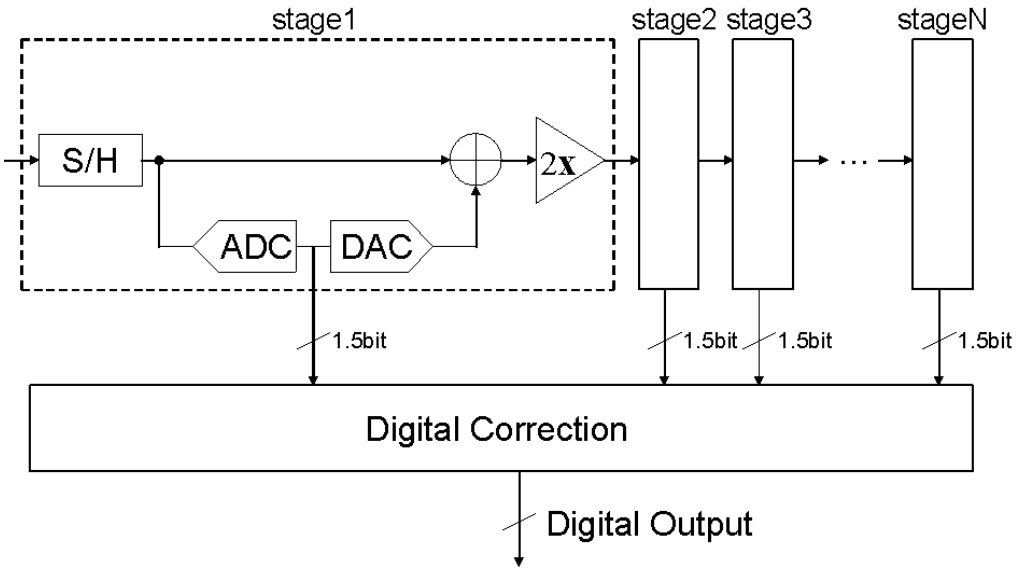


Figure 3.3: Block diagram of Pipelined ADC

previous stage, and the residue amplifier amplifies this value and generates a new residue for the next stage. Each stage operates alternately, that is, if one stage is in the sampling mode, the next stage is in the amplification mode. The most important merit of this ADC is that the throughput rate is independent of the number of pipeline stages. Thus, high resolution can be obtained at a high sampling rate. A block diagram of a typical pipelined ADC employing 1.5-bit-per-stage architecture is shown in Fig. 3.3.

3.2 Oversampling ADC

Oversampling ADCs [32], [1], [38], [23] are the most digital-friendly ADCs. They take advantage of cheap DSPs to filter out out-of-band quantiza-

tion noise and achieve high resolution at the cost of reduced signal bandwidth. Their sampling rate is much higher than Nyquist rate, typically by a factor between 8 and 512. The most popular oversampling ADC is a delta-sigma ($\Delta\Sigma$) ADC. This ADC has a $\Delta\Sigma$ modulator which passes in-band signal and pushes in-band quantization noise to out-of-band. A block diagram of a typical $\Delta\Sigma$ modulator is shown in Fig. 3.4(a). It consists of a loop filter, ADC, and DAC. Its linearized z-domain model is also shown in 3.4(b). Q(z) represents the quantization noise of the ADC. G is a linearized effective gain of the ADC, which can be expressed as follows,

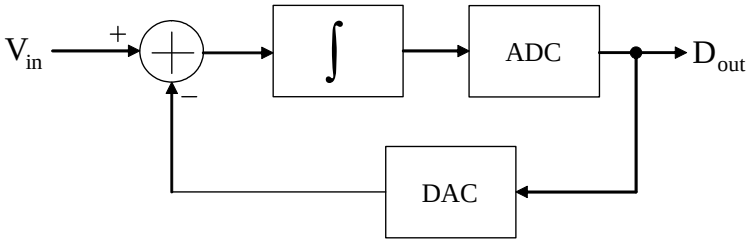
$$G = \frac{rms\,value\,of\,the\,ADC\,output}{rms\,value\,of\,the\,ADC\,input} \tag{3.1}$$

Using the linearized model, the signal transfer function (STF(z)) and noise transfer function (NTF(z)) can be expressed as follows,

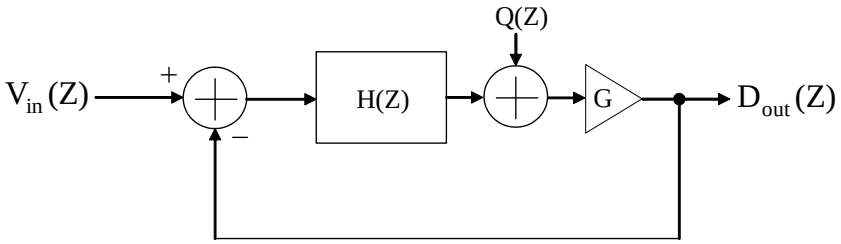
$$STF(z) = \frac{D_{out}(z)}{V_{in}(z)} = \frac{HG}{1+HG} \tag{3.2}$$

$$NTF(z) = \frac{D_{out}(z)}{Q(z)} = \frac{G}{1+HG} \tag{3.3}$$

Since H(z) has a high-gain at low frequencies, STF(z)$\simeq$1 and NTF(z)$\simeq$0. From the above equations, it is clear that while the $\Delta\Sigma$ modulator passes the input signal without any attenuation, it suppresses in-band quantization noise, resulting in high resolution. The major disadvantage of a $\Delta\Sigma$ ADC is a reduced input signal bandwidth because of oversampling.



(a) Block diagram of delta-sigma modulator



(b) Linearized model of delta-sigma modulator

Figure 3.4: Block diagram of delta-sigma modulator and its linearized model

Chapter 4

Low-Power Techniques in Pipelined ADC

Various techniques [44]-[33] have been developed to reduce power consumption. Among these, opamp-sharing [44]-[5] and switched-opamp techniques [11]-[20] show the most promise. Opamp-sharing saves power by sharing one opamp between two successive pipeline stages. Switched-opamp saves power by turning off the opamp when it is not needed. Each technique, however, suffers from its own drawbacks. These drawbacks will be discussed in the following subsections. This section is organized as follows. First of all, opamp-sharing and switched-opamp are reviewed. Then, the proposed opamp and capacitor sharing technique will be presented in greater detail.

4.1 Opamp-Sharing Technique

A conventional pipeline stage operates with a two-phase non-overlapping clock. As shown in Fig. 4.1, when Φ_1 is high, stage N samples the input and stage N+1 generates the output. Then, as Φ_2 becomes high, stage N produces the output and this is sampled by stage N+1. The basic idea behind the opamp-sharing technique is that since the opamp is not needed during the sampling phase, it can only be active during the half clock period. That is,

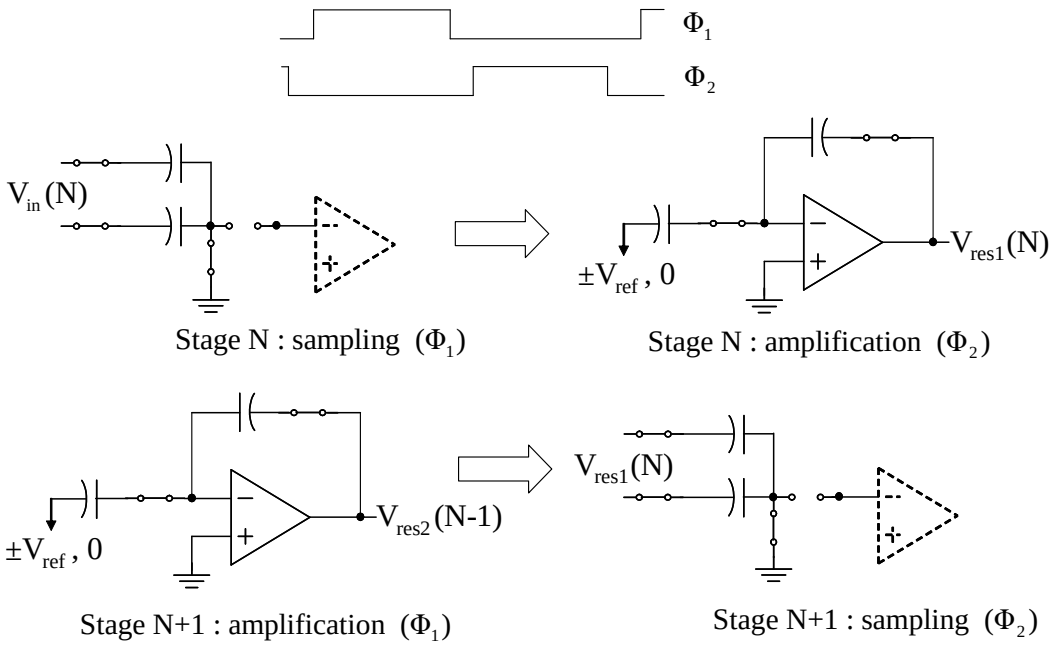


Figure 4.1: Opamp-sharing between two successive pipeline stages

the opamp can be used for stage N when Φ_1 is high, otherwise, it can be used for stage N+1. Thus, significant power and area saving can be achieved by reducing the number of opamps. However, it also has two drawbacks. First, since the opamp is always active, there is no time to reset the opamp and the previous sample stored on the opamp input capacitance affects the current output, which is called a memory effect [24], [6]. This can be relaxed by using a feedback signal polarity inverting (FSPI) technique [6], which reduces the memory effect by alternating the signal polarity. The second drawback is that it requires additional switches on the opamp input node to disconnect the opamp when it is not needed. These switches introduce series resistance and degrade the settling behavior. This series resistance can be reduced by increasing the switch size. However, as the switch size increases, so do the parasitics. Thus, there is a tradeoff between the series resistance and the parasitics. It often requires careful designs and various simulations including all the parasitics associated with the additional switches.

4.2 Switched-Opamp Technique

CMOS technology offers a good switch that plays an important role in switched-capacitor applications. However, as the supply voltage decreases, it becomes difficult to turn on the MOS switch. This is explained in Fig. 4.2. The NMOS transistor remains on for an input signal from 0 up to V_{DD}-V_{TN} (threshold voltage of NMOS). On the other hand, the PMOS transistor conducts for an input signal from $|V_{TP}|$ (threshold voltage of PMOS) to V_{DD}.

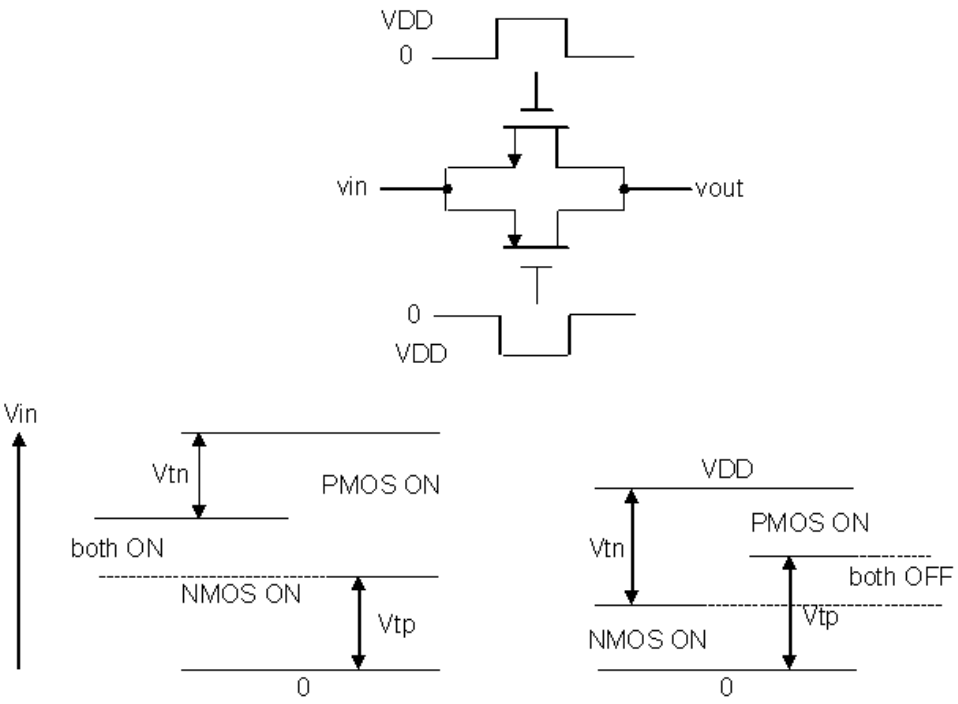


Figure 4.2: CMOS complementary switch with different gate voltage

The operation of complementary switch fails when the supply voltage is less than $V_{TN}+|V_{TP}|$. The switched-opamp was first invented for low-supply operations. The main idea is to replace the floating switch that is connected to moving signal by a switch that grounds the output terminal of the opamp. Using this method, the op-amp output is connected to ground or V_{DD} when it is off. This is explained in Fig. 4.3 and 4.4. The switches S_1 and S_2 in Fig. 4.3 are floating switches which are not connected to either supply voltage or ground. In this case, the switches can not be turned on for some range of the input signal. On the contrary, there are no floating switches in Fig. 4.4.

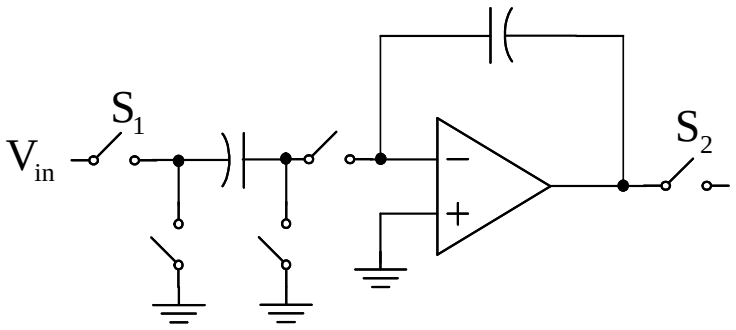


Figure 4.3: Switched-capacitor circuit with floating switches

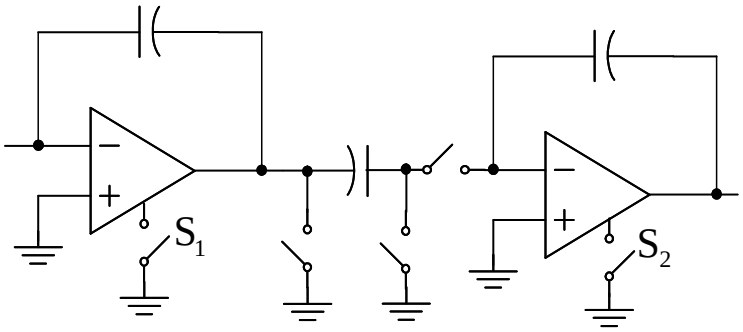


Figure 4.4: Switched-capacitor circuit without floating switches

The floating switches in Fig. 4.3 are replaced by the switched-opamp. Thus, all the switches are either connected to supply voltage or ground when they turn on. This technique can also be used for low power operation. Since the opamp does not need to be active during the sampling phase, it can be off. However, this requires the opamp to be turned on and off at each clock [11], [20]. This limits the operating speed. Recently, a partially switched-opamp technique was proposed to improve the settling behavior at the cost of power consumption. Unlike a conventional switched-opamp technique, the second

stage of the two-stage opamp is turned off during the sampling phase(when the opamp is not needed).

4.3 Proposed Opamp and Capacitor-Sharing Technique

One distinct advantage of opamp-sharing is that the number of opamps are reduced by half, resulting in area saving. However, the switch-opamp technique requires the same number of opamps as the conventional architecture does, thus it has no area saving. Further power and area saving can be achieved by sharing both the opamp and capacitor. The idea behind the opamp and capacitor-sharing technique is that after the current stage generates the output, the charge on the feedback capacitor is reused for the following stage instead of being thrown away. Fig. 4.5 shows two successive 1.5-bit-per-stage pipeline stages (stage N, stage N+1) employing the opamp/capacitor-sharing technique with the timing diagram. Even though a 1.5-bit-per-stage architecture is used in Fig. 4.5 for simplicity, this technique can be applied for any kind of pipeline stages. The stage N employs a modified 1.5-bit-per-stage architecture and the stage N+1 employs a conventional 1.5-bit-per-stage architecture. On the falling edge of Φ_1, the input signal is sampled on the sampling capacitors (C_S's) of the stage N. During the discharge phase (Φ_D), while the input sample is held on C_S, the opamp and two feedback capacitors (C_F's) are reset to common-mode voltage. Then, during the amplification phase (Φ_2), the stage N generates the output by connecting the bottom plate of the C_s's to $\pm V_{ref}$ or 0 depending on the decision from the previous phase. As Φ_1 be-

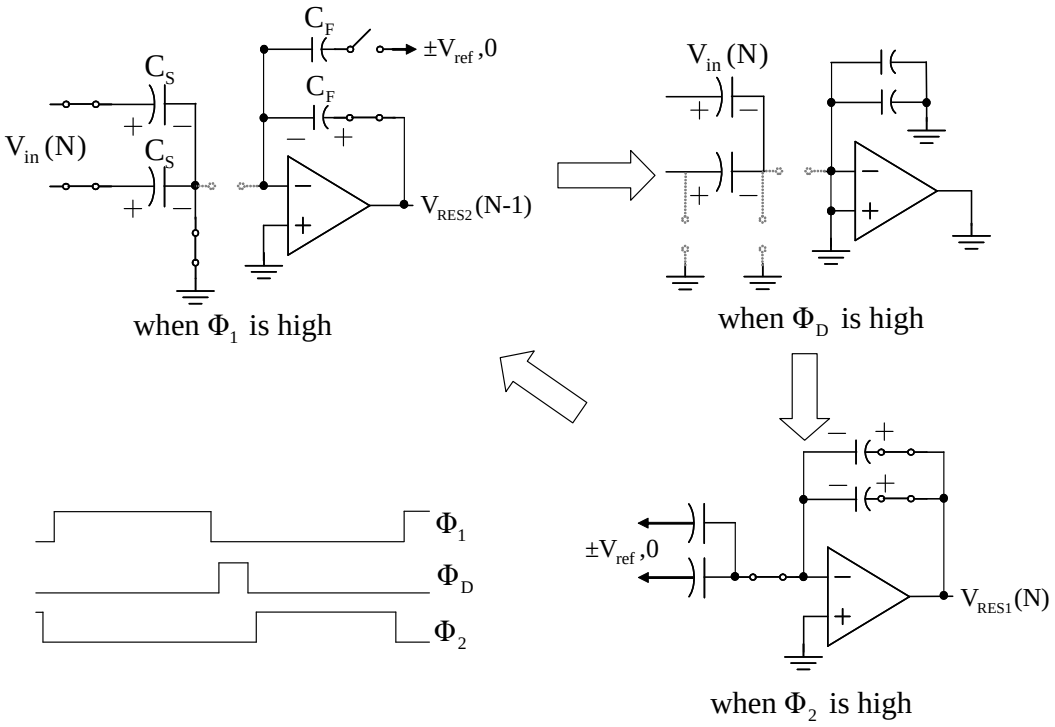
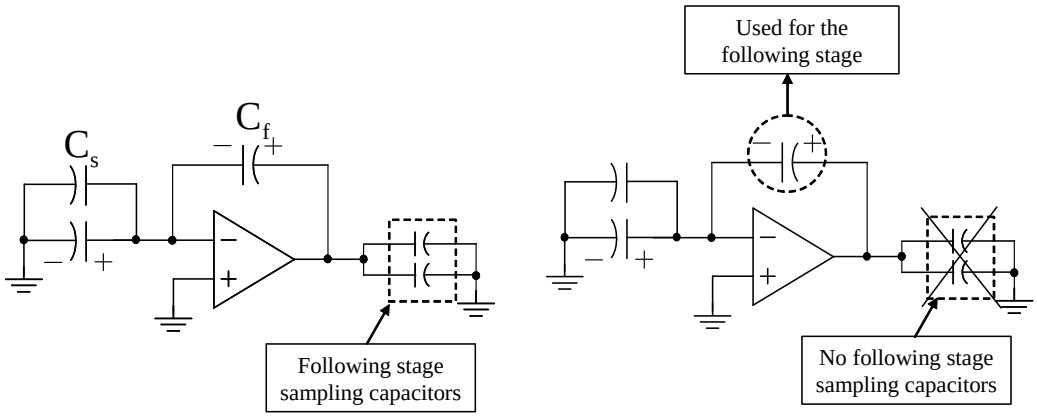


Figure 4.5: Opamp/Capacitor-sharing technique

comes high, the C_S's are charged to the next input sample, while the charge on the C_f's is directly used to generates the output of stage N+1, that is, one of the C_f's is connected to the opamp output and the other C_f is connected to $\pm V_{ref}$ or 0. Two important facts need to be noted in this technique. First, the amplification phase (Φ_2) is about $20\% \sim 30\%$ shorter than that of a conventional two-phase nonoverlapping clock due to the addition of the discharge phase (Φ_D). However, the capacitor-sharing between two successive pipeline stages reduces the considerable amount of the opamp output load during the amplification phase, because the output of the following stage (stage N+1) is



(a) Conventional pipeline stage during the amplification phase

(b) Pipeline stage with the capacitor sharing technique

Figure 4.6: Pipeline stage with and without capacitor-sharing technique

generated by redistributing the charge on the C_f's. Thus, the opamp does not have to drive sampling capacitors of the following stage in the amplification phase. This is depicted in Fig. 4.6. Using this technique, the total opamp load in amplification phase is reduced by about $40\% \sim 60\%$ depending on the architecture of the stage compared to that of a conventional pipeline stage. The reduced output load allows the stage output to settle faster to the required accuracy without increasing power. The second important fact is the memory effect. Stage N does not have the memory effect, because the opamp is reset to common-mode voltage before Φ_2 goes high (when Φ_D is high). However, since there is no reset phase between Φ_2 and Φ_1, the stage N+1 has the memory effect. Thus, it is important to keep the error voltage caused by the memory effect small such that it does not degrade the ADC performance. This was

done by using the several techniques in the prototype ADCs that will explained in the next chapter.

Chapter 5

Prototype Implementation I

In order to demonstrate the opamp and capacitor-sharing technique, a 10-bit 50MS/s pipelined ADC was implemented in 0.18μm CMOS technology. This chapter describes several practical issues of circuit implementations. The measurement results will be presented in the next chapter.

5.1 The ADC Architecture

The ADC architecture is shown in Fig. 5.1. The first opamp is shared between the first and second stages, and the second opamp between the third and fourth stages. The first stage employs a modified 1.5-bit-per-stage pipeline architecture [13], followed by three 2.5-bit-per-stage pipeline stages and a 3-b Flash ADC. The main advantage of implementing the first stage with the modified 1.5-bit-per-stage architecture is that it halves the output swing of the opamp and relaxes its settling requirement. This is done so at the expense of additional comparators and a smaller feedback factor. However, reducing the output swing is important here because the capacitor-sharing technique, as we shall see in Section 5.3, requires the charge on the feedback capacitor to be quickly discharged after the first MDAC operation. A smaller opamp

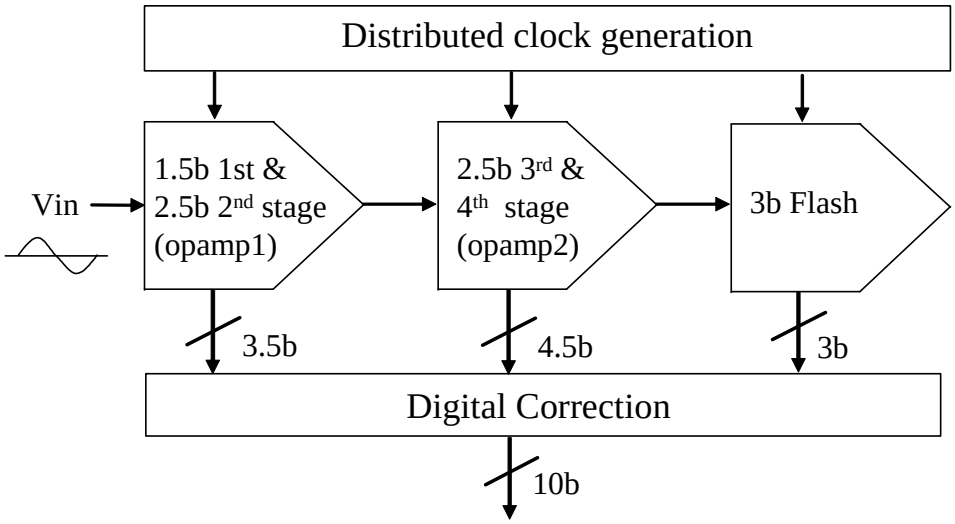


Figure 5.1: The ADC architecture

output swing translates to less charge on the feedback capacitor, and thus quicker discharge times. In addition to halving the output swing, the modified 1.5-bit-per-stage architecture has the widest digital correction range ($\pm\frac{V_{ref}}{4}$) [25], which is $\pm 200mV$ for a $1.6V_{pp}$ (peak-to-peak) input signal. With this wide correction range, a fair amount of aperture error and comparator offset can be tolerated. Fig. 5.2 shows the combined first and second stage of the ADC. It consists of one opamp, two sampling capacitors (C_s), four feedback capacitors (C_f) and two sub-ADCs for the first and second stages. Capacitor sizes are chosen to meet noise and matching requirements, and C_f is set to $\frac{1}{4}C_s$ for an interstage gain of 4. The opamp is the proposed low input-capacitance variable-g_m opamp that helps reduce power consumption and improve performance, and will be explained in Section 5.4. Capacitors ($C_f's$) are

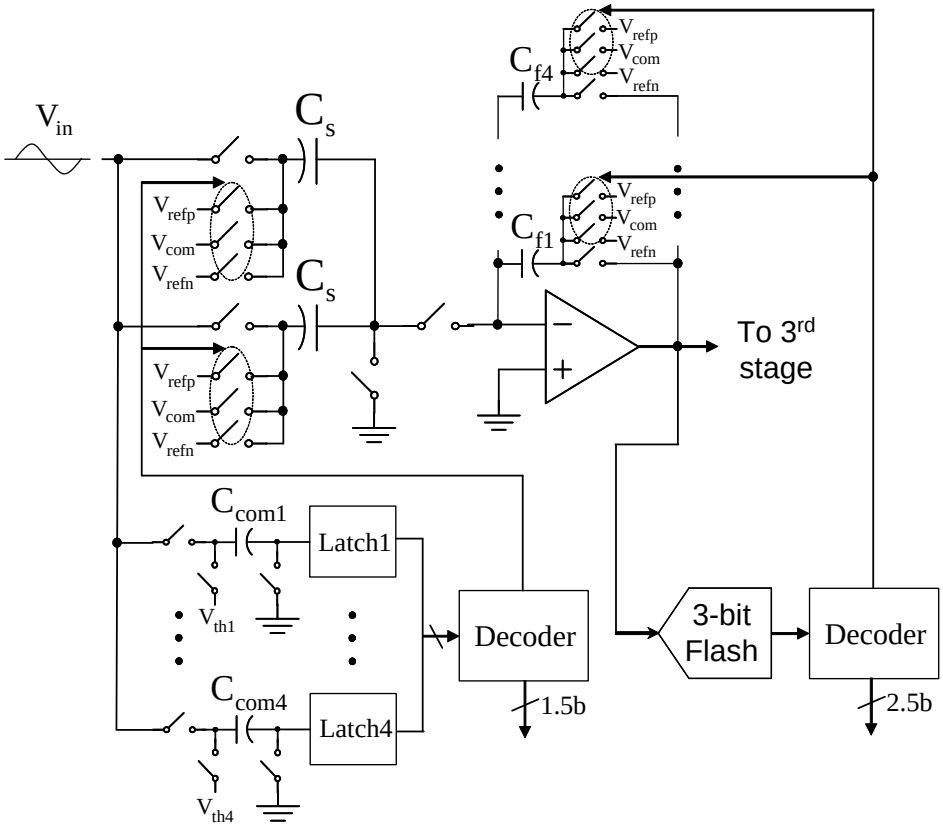


Figure 5.2: The first and second stages with opamp/capacitor-sharing

shared between the two stages to minimize power consumption and will be discussed in Section 5.4. The first *sub*_ADC has its own sampling capacitors ($C_{com1}...C_{com4}$) and four dynamic comparators. The additional two comparators are used to reduce the output signal swing. The second *sub*_ADC is a 3-bit flash ADC with a decoder logic.

5.2 Input Sampling Networks

In a conventional pipelined ADC, the front-end SHA freezes the input signal so that the first stage can operate on a unique copy of the input for quantization and MDAC operation. However, the SHA consumes a considerable amount of power and its inclusion in the ADC must be justified in power-sensitive applications. Furthermore, the SHA adds noise to the signal and can itself be nonlinear. An alternative is to completely remove the SHA and instead, have different sampling networks simultaneously sample the input. This reduces power consumption and saves valuable die space. However, doing so can limit the ADC's maximum input frequency, which often is important in subsampling applications with input frequencies multiple times above the Nyquist frequency. This input frequency ceiling is largely caused by aperture error resulting from RC-delay mismatch between the different input sampling networks [26]. In this paper, the aperture error was relaxed by matching the input sampling networks through careful layout. Assuming a square-law model, the switch on resistance (R_{on}) can be expressed as $u_n C_{ox}(\frac{W}{L})(V_{gs} - V_t)$. If all switch transistors have the same V_{gs}, and assuming the same $u_n C_{ox}(\frac{W}{L})$ for all switches, then R_{on} is determined by the $(\frac{W}{L})$ ratio, a well controlled parameter, and V_t. Since the variation of V_t can be bounded statistically, the worst case aperture error can be determined. To ensure all the bootstapped switches have the same V_{gs}, they share the same bootstapped capacitor (C_{boot}) as shown in Fig. 5.3. Other switches connected to the top plate of the sampling capacitors (C_s, $C_{com1}...C_{com4}$) also have the same V_{gs} because they all connect to the

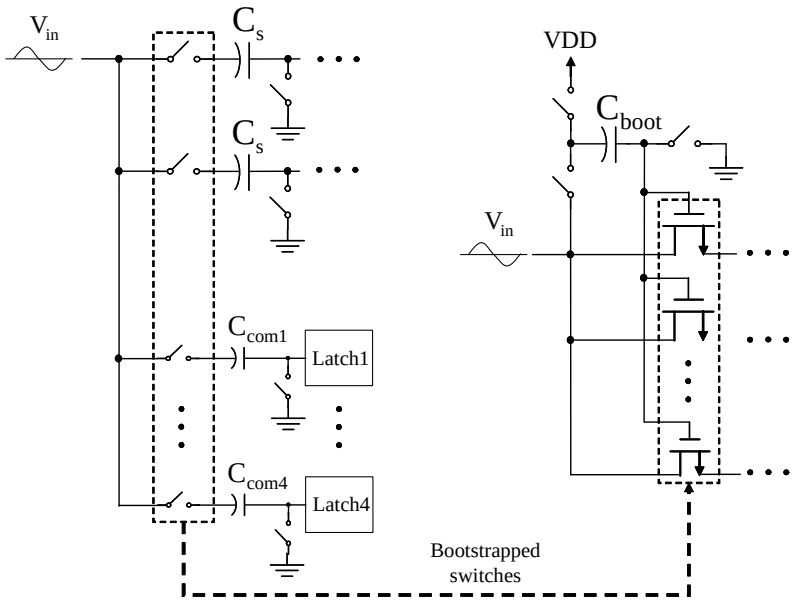


Figure 5.3: Input sampling networks for the first stage

same common-mode voltage. Setting the size of the sampling capacitors and the $(\frac{W}{L})$ ratio of the switch transistors to obtain the same RC-delay, aperture error can be minimized. Second-order non-idealities such as the short-channel effects and parasitics on the signal path are small compared to V_t mismatch and can be absorbed and corrected by digital error correction. In the ADC, the correction range is maximized by employing a 1.5-bit-per-stage pipeline architecture for the first stage. From simulations with parasitics extracted, aperture error was within the correction range for input frequency up to the edge of the fourth Nyquist zone.

5.3 Capacitor-Sharing Technique

In previous works that remove the SHA [26], [15], the first MDAC operation is seen as a speed bottleneck because it must be shortened to accommodate the extra comparison phase for the comparators to make a decision. The capacitor-sharing technique, however, eases this bottleneck by minimizing the opamp's effective load capacitance. Additionally, to take full advantage of the comparison phases, the first stage feedback capacitors and the opamp's output are discharged simultaneously, canceling any memory effects in the first MDAC operation. The idea behind the capacitor-sharing technique is that after the first MDAC generates the output, the charge on the feedback capacitor is reused for the second MDAC instead of being thrown away. Fig. 5.4 shows the detailed first and second stages with their corresponding timing diagrams. It operates as follows. The input signal is sampled on the sampling capacitors (C_s, C_{com1}...C_{com4}) at the end of the sampling phase (Φ_1). Though it is not shown in Fig. 5.4 for simplicity, Φ_{1e} is used for bottom plate sampling in the actual implementation. While the input sample is held on C_s, the opamp and feedback capacitors are reset to AC ground during the discharge phase (Φ_{Dis}). During this phase, a decision is also made by the comparators in the first sub-ADC. That is, after a short delay from the falling edge of Φ_1, which allows the input sample of the comparator to settle, the latch clock (Φ_{Lat}) goes high and the latches make a decision for the first MDAC operation at the end of Φ_{Dis}. Then, in the amplification phase (Φ_2), the output of the first MDAC is generated by connecting the bottom plate of the C_s to $\pm V_{ref}$ or V_{com} depending on

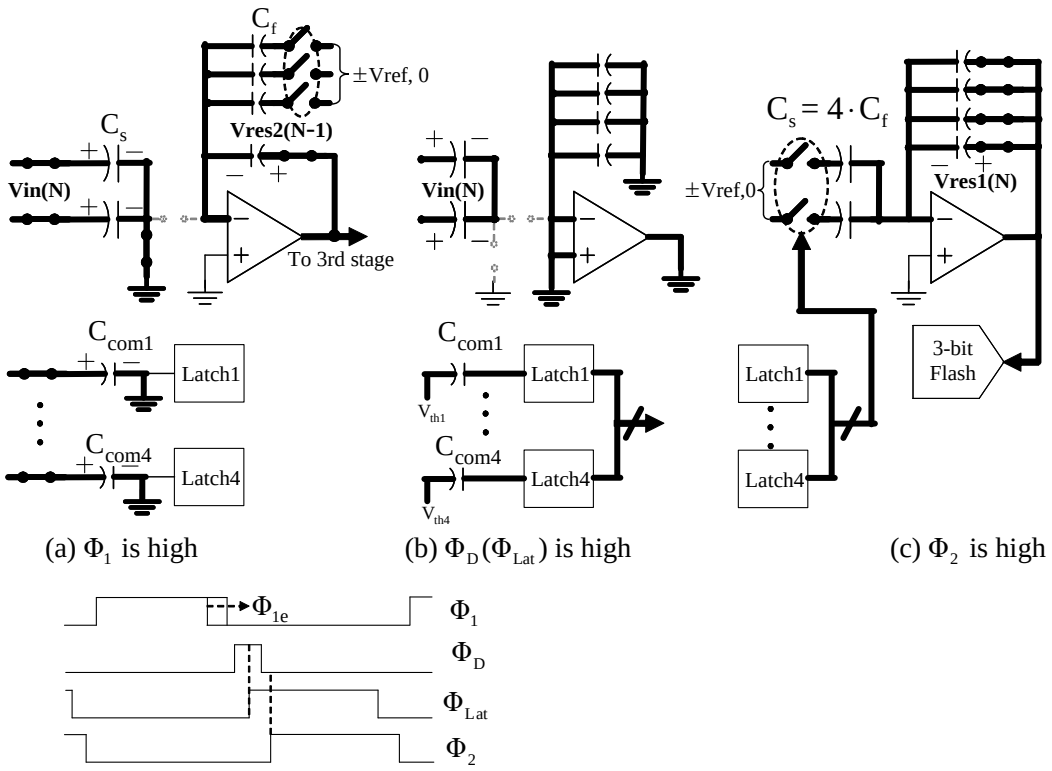


Figure 5.4: Timing diagram and the first and second stage configurations at each phase

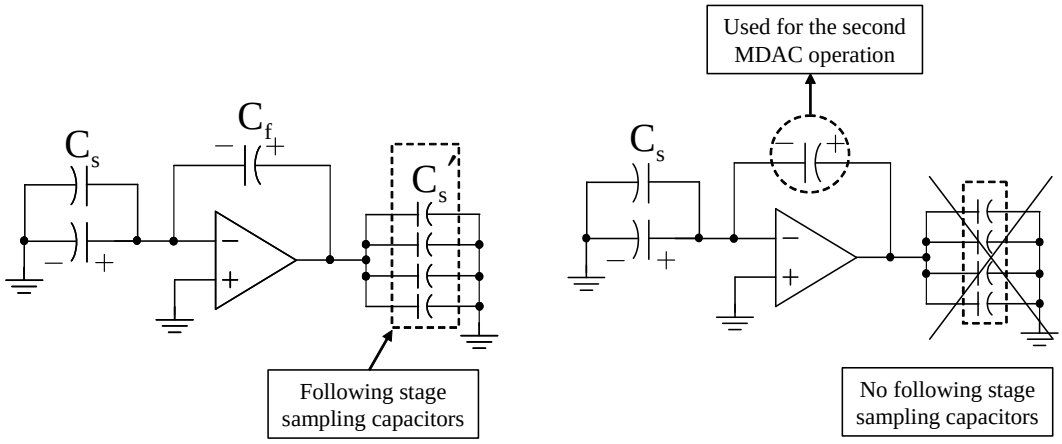


Figure 5.5: Pipeline stages with and without capacitor-sharing

the decision from the previous phase (Φ_{Lat}). The comparators of the second stage then make a decision after the opamp enters the linear-settling region [6] towards the end of Φ_2. In the next sampling phase (Φ_1), C_s is charged to the next input sample, while the charge on the C_f's is directly used for the second MDAC operation, that is, one of the 4 C_f is connected to the opamp output and the others are connected to $\pm V_{ref}$ or V_{com} depending on the output of the second sub-ADC. The rest of the pipeline stages operate with a two-phase non-overlapping clock just like a conventional pipelined ADC. As shown in Fig. 5.5, capacitor-sharing between the first and second MDACs reduces the amount of the opamp output load considerably when Φ_2 is high (amplification phase of the first MDAC). Assuming C_s=C_f=4·$C_s\prime$=C and ignoring parasitics, the total output load (C_L) of the conventional MDAC,

$$C_L = (1-\beta)\cdot C_f + 4\cdot C_s\prime = \frac{5}{3}\cdot C \tag{5.1}$$

Where the feedback factor, $\beta = \frac{C_f}{2C_s+C_f} = \frac{1}{3}$. On the other hand, the total output load ($C_L\prime$)with capacitor-sharing,

$$C_L\prime = (1-\beta)\cdot C_f = \frac{2}{3}\cdot C \tag{5.2}$$

As shown in equations (5.1) and (5.2), capacitor-sharing reduces the opamp load by about 60% compared to the conventional one. The reduced load allows the first MDAC output to settle to the required accuracy without increasing power even with a 20% shorter amplification phase (Φ_2) due to the addition of Φ_{Dis}. The parasitic capacitance at the opamp input node was not considered in the feedback factor calculation because the input transistor of the preamplifier is small and the parasitic is about ten times smaller than C_s. Considering memory effects of the 1st and 2nd MDAC operations, we see that the 1st MDAC is free of memory effects because the opamp is always reset during Φ_{Dis}. However, since there is no reset phase between Φ_2 and Φ_1, the second MDAC will have some memory effect. Nonetheless, this does not degrade the ADC performance because the opamp has high DC-gain and small input parasitics, and the second MDAC output requires only 7-bit linearity. Simulations show that the second stage memory effect is negligible, which is also verified by direct measurements.

5.4 Variable-g_m Opamp

The low input-capacitance variable-g_m opamp is shown in Fig. 5.6. The opamp is based on pre-amplification and has the desirable property of having

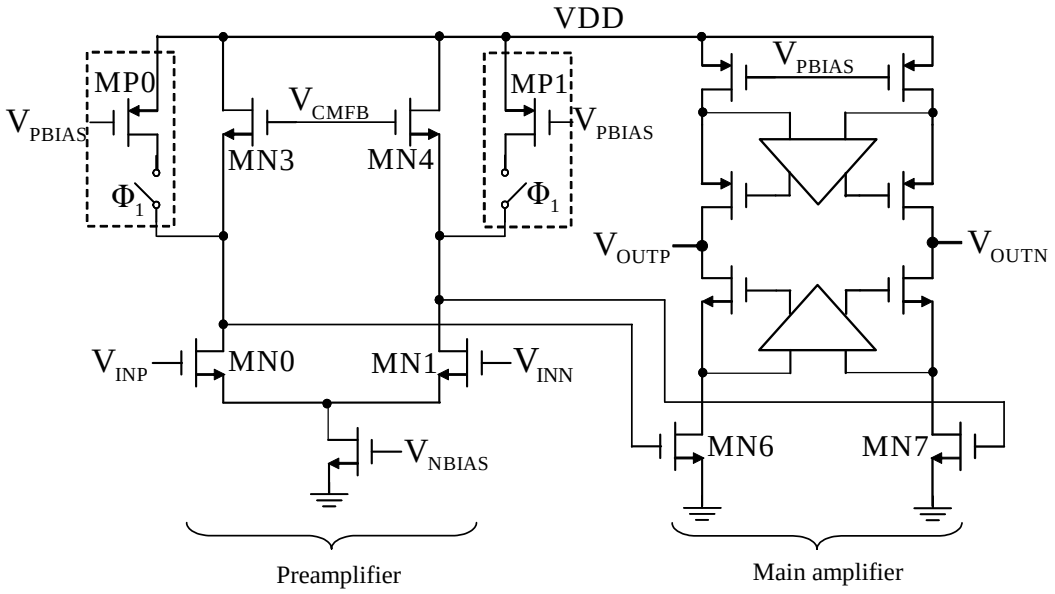


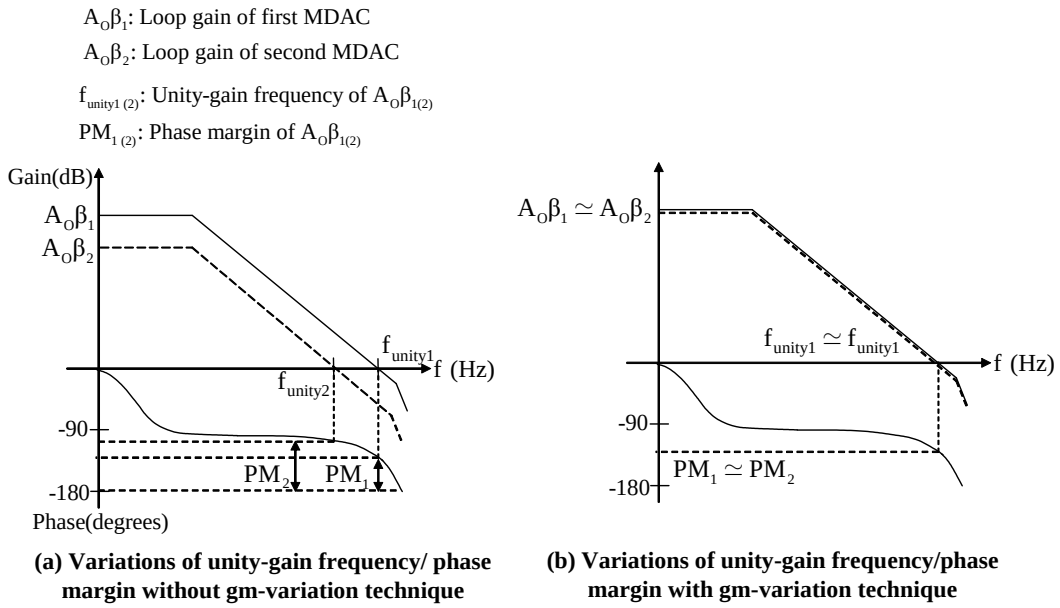
Figure 5.6: Schematic of the variable-g_m Opamp

a low input-capacitance [36]. The two PMOS transistors (MP0 and MP1) and two switches are added to control the effective transconductance (g_m) of the opamp. Without the added transistors and switches, the opamp operates exact like the original one. The low-gain wideband preamplifier boosts the transconductance of the main amplifier by its gain (A_p). That is,

$$g_m = A_p \cdot g_{m6} = \frac{g_{m0}}{g_{m3}} \cdot g_{m6} \tag{5.3}$$

Where g_{m0}, g_{m3} and g_{m6} are the transconductances of the transistor MN0, MN3 and MN6, respectively. The preamplifier can be small and low power because it only needs to drive the input transistors of the main amplifier. The size of MN0 (MN1) is about one-third of MN6 (MN7) in this design. An

advantage of adding the preamplifier is that wide bandwidth can be achieved simply by increasing A_p while keeping the parasitics of the opamp input node small. Lower input capacitance helps to increase the feedback factor and reduce memory effects. A_p can be increased by reducing g_{m3} without burning more power. However, a non-dominant pole associated with the preamplifier output node, which can be expressed as $\frac{g_{m3}}{C_L}$, (C_L is the output load of the preamplifier) will be brought down closer to a dominant pole and this reduces the phase margin (PM). The main amplifier with a gain-boosting [7] offers high DC gain and wide output swing. The main design issue of the opamp for the first and second stages is that the opamp is placed in different feedback configurations and has different output loads in each phase (Φ_1 and Φ_2). For example, when Φ_2 is high, the opamp is used for the first MDAC which has an interstage gain of 2 and feedback factor of 1/3. On the other hand, when Φ_1 is high, the opamp is used for the second MDAC which has an interstage gain of 4 and feedback factor of 1/4. The parasitic capacitance at the opamp input node was ignored again in the feedback factor calculation for the same reason as mentioned above. In addition to the feedback factor variation, because of capacitor sharing, the opamp has a smaller output load during the first MDAC than during the second MDAC as oppose to the conventional pipeline stages. For these reasons, the bandwidth of $A_O \cdot \beta_2$ decreases and the phase margin (PM) increases compared to those of $A_O \cdot \beta_1$ as shown in Fig. 5.7(a), where $A_O \cdot \beta_1$ and $A_O \cdot \beta_2$ are the loop gain of the first and second MDAC, respectively. If the opamp is optimized only for the first MDAC, then the poor



(a) Variations of unity-gain frequency/ phase margin without gm-variation technique

(b) Variations of unity-gain frequency/phase margin with gm-variation technique

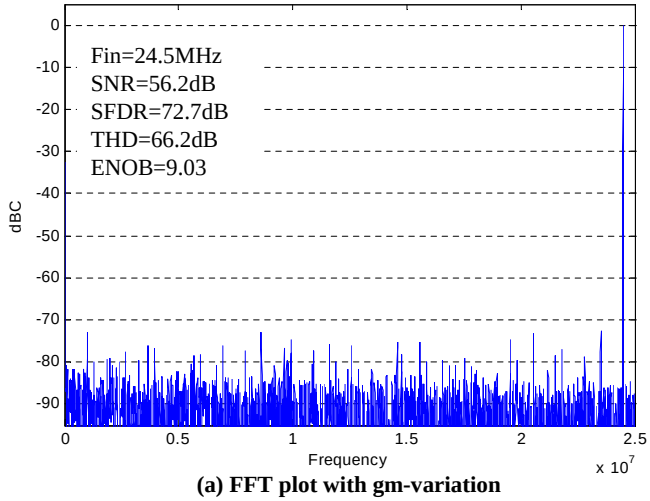
Figure 5.7: Loop gain variations with and without gm-variation

settling behavior of the second MDAC can degrade the ADC performance even with the relaxed settling requirement of the second MDAC output. In order to improve the settling behavior of the second MDAC, the opamp has to be moved back to the optimum operation region by increasing the bandwidth and decreasing PM as shown in Fig. 5.7(b). This can be done by reducing g_{m3} as explained before. Assuming the opamp is working in the optimum operation region, that is, the bandwidth and PM of $A_O \cdot \beta_1$ are set to have good settling behavior when Φ_1 is low (during the first MDAC operation). As Φ_1 goes high and the opamp is placed in the second MDAC, the loop gain starts to deviate from $A_O \cdot \beta_1$. However, at the same time, MP0 and MP1 are turned on and take some current from the MN3 and MN4. This

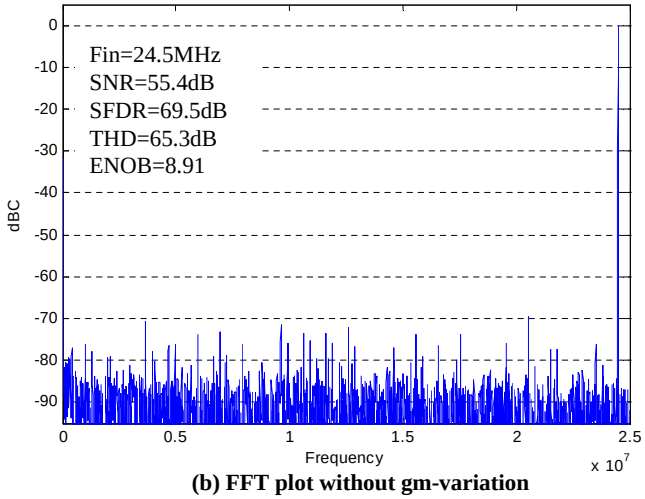
reduces g_{m3} (g_{m4}) and increases A_p. Thus, the bandwidth and PM of $A_O \cdot \beta_2$ stays close to the optimum values, resulting in improvement of the settling behavior. In the ADC, the effect of the g_m-variation was tested by controlling the switches. Fig. 5.8 shows the measurement results with and without g_m-variation. The ADC was tested with a input frequency close to the Nyquist frequency (F_{in}=24.5MHz), and sampling frequency, F_s=50MHz. With g_m-variation, the measured SNDR and SFDR were improved by 1dB and 3dB , respectively.

5.5 Dynamic Comparator

The dynamic comparator used in the ADC is shown in Fig. 5.9. The latch circuit for the comparator is the same as the one in [6]. It works with a two phase non-overlapping clock. The Φ_{1e} is used for bottom-plate sampling of the input signal. In case of the first stage comparators, the clocking scheme is different from the one in the Fig. 5.9 (and are shown in Fig. 5.4) because the comparators sample the input signal. However, the basic working principles are the same. The sizes of the input transistors (MN0 and MN1) and MN3 in the latch are chosen to be larger than other transistors to increase gm and reduce the input-referred offset voltage. By comparing the actual transition points with the theoretical ones in the measured INL curve, the measured maximum offset of the comparator was about 21mV out of 20 test samples.



(a) FFT plot with gm-variation



(b) FFT plot without gm-variation

Figure 5.8: Measured FFT plots with and without g_m-variation

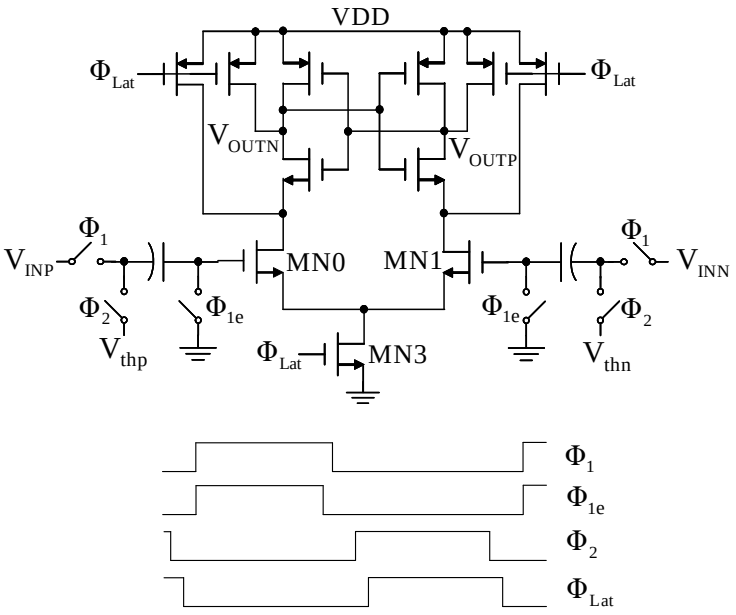


Figure 5.9: Dynamic Comparator

Chapter 6

Experimental Results I

The ADC is implemented in 0.18μm CMOS technology with metal-insulator-metal (MIM) capacitor and occupies die area of 0.86mm^2. The die micrograph is shown in Fig.6.1. It has a merged first and second stage, third and fourth stage with a opamp-sharing, 3-bit flash ADC, reference buffers, clock generation, digital correction logic and current bias circuits.

6.1 Test Setup

A test setup for the ADC is shown in Fig. 6.2. A single-ended input signal is generated by a signal generator and applied to a bandpass filter to reduce the harmonics and noise introduced by the signal generator. Then, the filtered signal is converted to a fully differential signal using a transformer (ADT1-1WT) and applied to the ADC. A clock signal is also generated by a signal generator and bandpass filtered before going into the ADC. The reference voltages are generated off-chip and buffered on-chip. The references are bypassed to the ground using a 0.1μF capacitor. A bypass capacitor is also placed between V_{refp} and V_{refn} to improve the reference settling. The master bias current is generated by the current source (LM334) and mirrored using

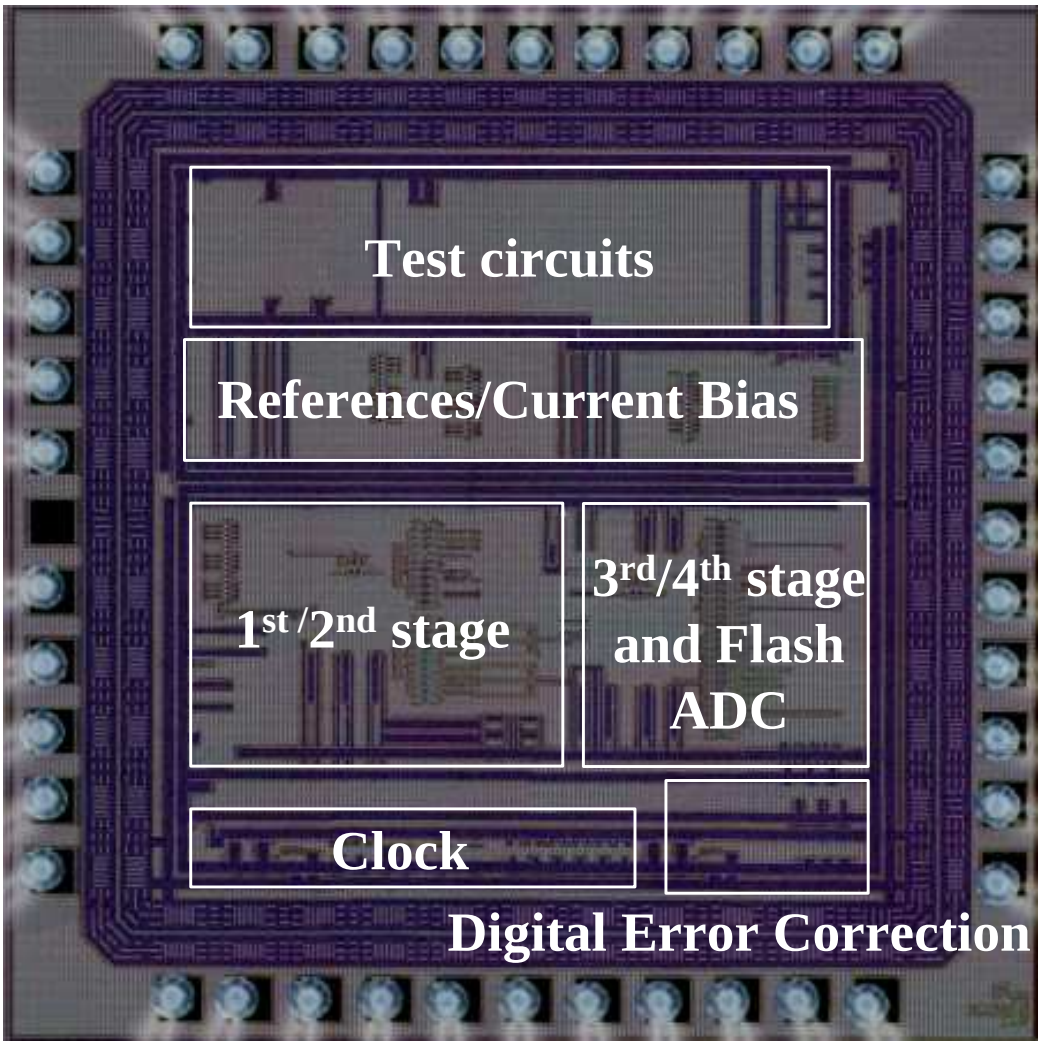


Figure 6.1: Die micrograph

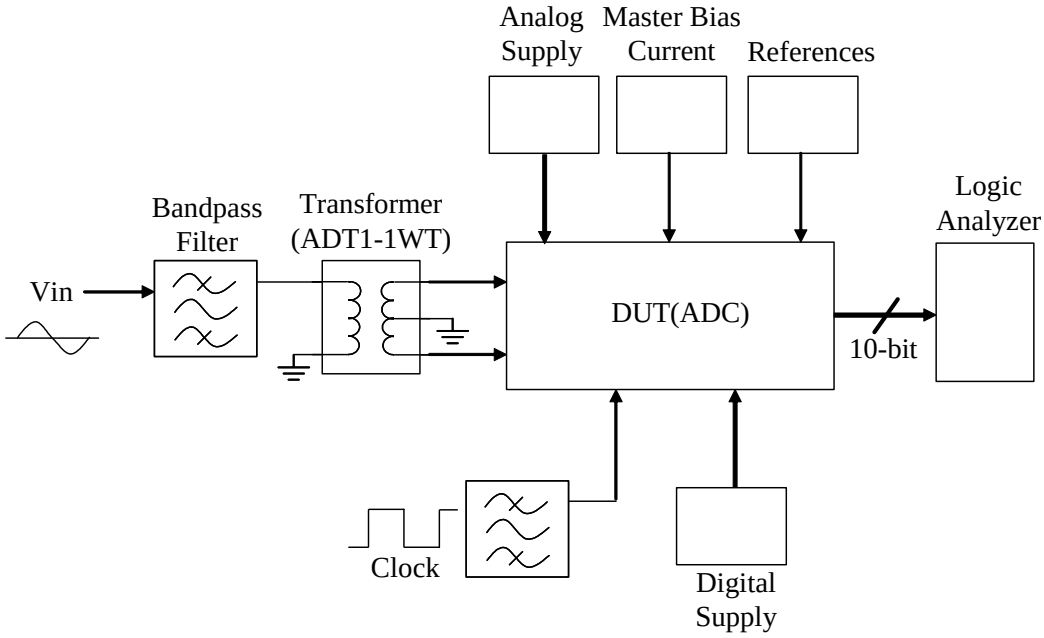


Figure 6.2: Test setup

on-chip current mirror. Analog and digital power are generated from the separate power supplies. The 10-bit digital outputs are collected using a logic analyzer and transferred to a computer. The test board has four layers. The second layer is used as a ground. The third layer is divided into two parts, one is used as a analog power plane and the other is used as a digital power plane.

6.2 Dynamic Performance

Dynamic performance includes dynamic linearity, noise and distortion. The following measures are used to characterize the dynamic performance of ADC.

1. Signal-to-noise ratio (SNR) is the ratio of the signal power to the total noise power at the output of ADC with full-scale sinusoidal input. As shown in Fig. 6.3, it can be calculated by the following equation with an N-point FFT of a signal

$$SNR = signalpeak(dB) - noisefloor(dB) - 10logN \tag{6.1}$$

2. Signal-to-noise plus distortion ratio (SNDR) is the ratio of the signal power to the total noise and harmonic power at the output of ADC with full-scale sinusoidal input.

3. Dynamic range (DR) is the range of input signal amplitudes within which the desired output can be obtained, that is, it is the input power range for which the SNR is greater than 0 dB.

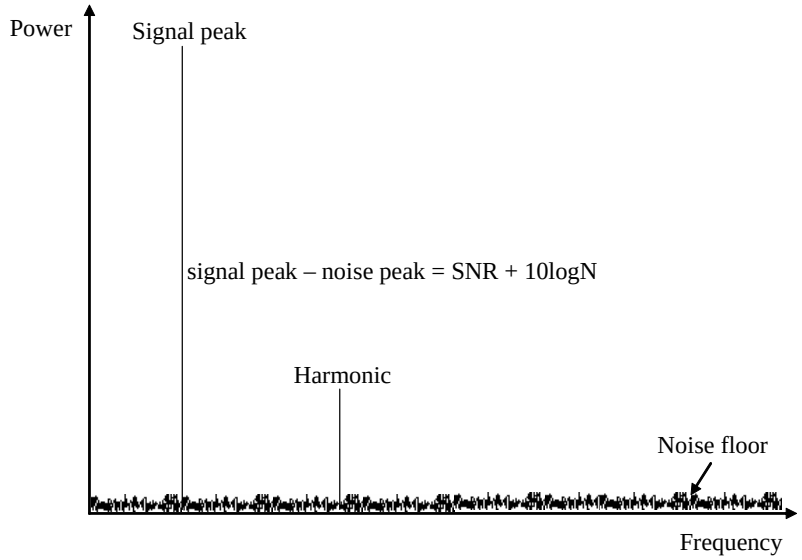


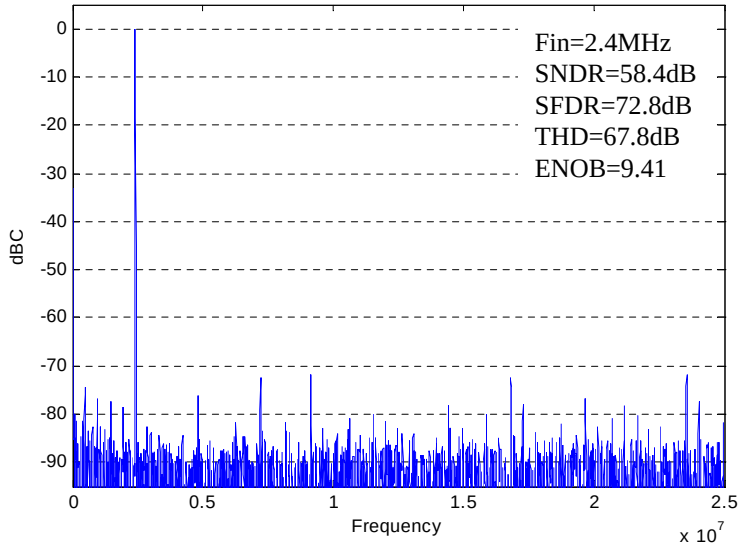
Figure 6.3: Procedure for computing SNR from an N point FFT

4. Spurious free dynamic range (SFDR) is the ratio of the signal power to the largest spurious component within a certain frequency band. It is important for telecommunication applications

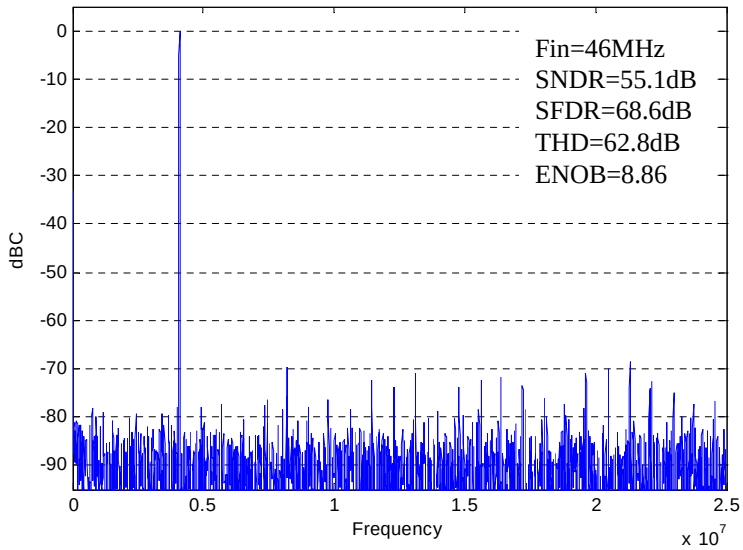
5. Effective number of bits (ENOB) is derived by the following equation,

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{6.2}$$

A 65536 point Fast Fourier transform (FFT) was used to characterize the ADC dynamic performances with various input frequencies. The measured FFT spectrums for input frequencies of 2.4 MHz and 46 MHz, are shown in Fig. 6.4. With the high frequency input (46 MHz), SNDR , SFDR, and THD are reduced by 3dB, 4dB, and 5dB, respectively. The effect of the variable-g_m



(a) FFT plot for Fin=2.4MHz @ Fs=50MS/s



(b) FFT plot for Fin=46MHz @ Fs=50MS/s

Figure 6.4: Measured FFT plots for input frequencies of 2.4 MHz and 46 MHz at 50 MS/s

opamp was tested by controlling the switches in Fig. 5.6. Fig. 6.5 shows the measurement results with and without g_m-variation. The ADC was tested with a input frequency close to the Nyquist frequency (F_{in} = 24.5 MHz), and sampling frequency, F_s = 50 MHz. With g_m-variation, the measured SNR and SFDR were improved by 1dB and 3dB , respectively. Fig. 6.6 shows the measured dynamic performances versus the input frequency. The measured SNDR, SFDR, and THD vary from 56.2dB to 58.4dB, 71.3dB to 72.8dB, and 64.6dB to 67.8dB for input frequencies up to the Nyquist and start to degrade beyond the Nyquist frequency.

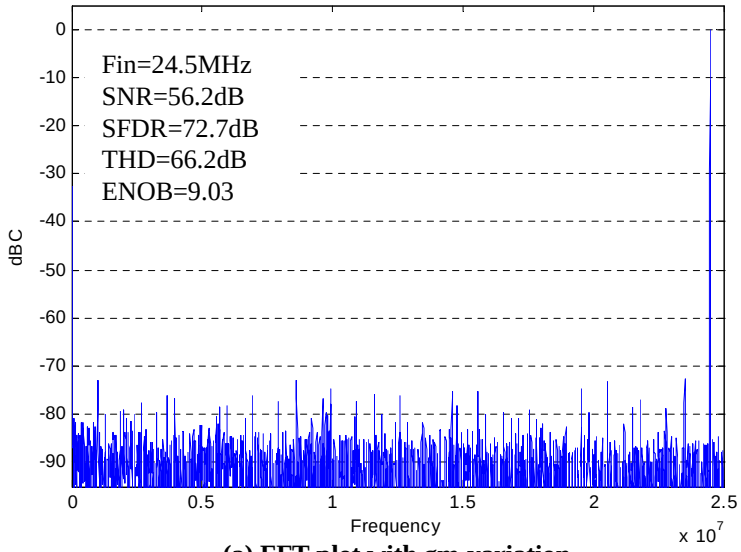
6.3 Static Performances

The most important measures of static linearity of ADC are differential nonlinearity (DNL) and integral nonlinearity (INL).

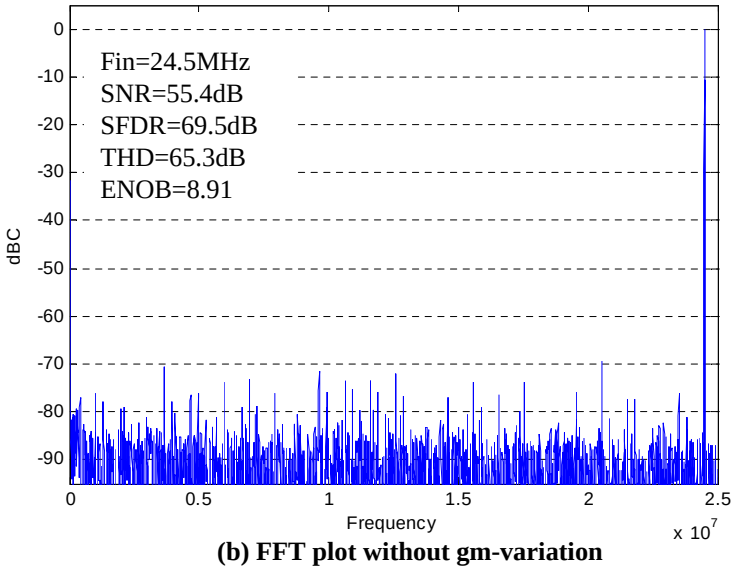
1. DNL is the deviation in the difference between two adjacent code transitions from 1 LSB.

2. INL is the deviation of the output code from a straight line passed through zero and full-scale points.

This is explained in Fig. 6.7. A 2.4 MHz sinusoidal input was applied to the ADC and two million samples were collected to perform a code-density test at 50 MS/s. The measured DNL and INL are shown in Fig. 6.8. The measured DNL and INL are less than ±0.39 LSB and ±0.81 LSB, respectively.



(a) FFT plot with gm-variation



(b) FFT plot without gm-variation

Figure 6.5: Measured FFT plots with and without g_m-variation

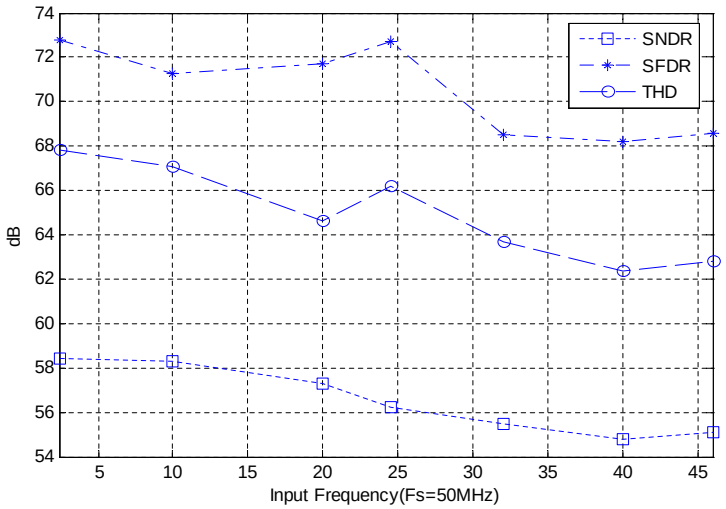


Figure 6.6: Dynamic performances versus input frequency

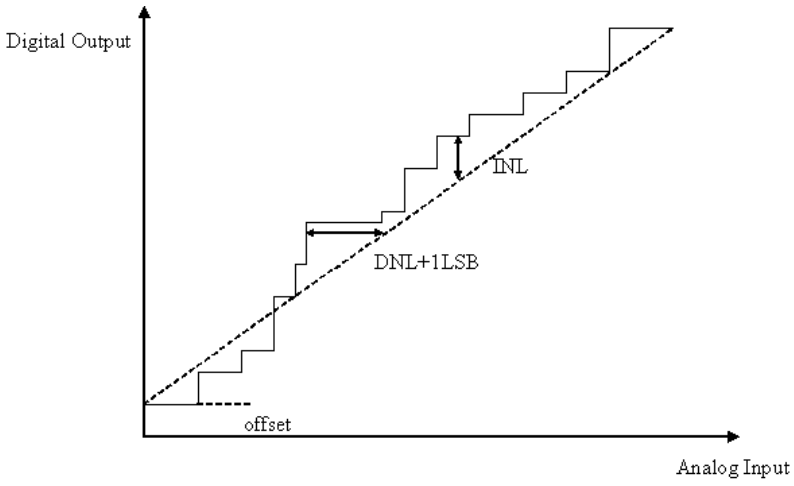


Figure 6.7: Static ADC metrics

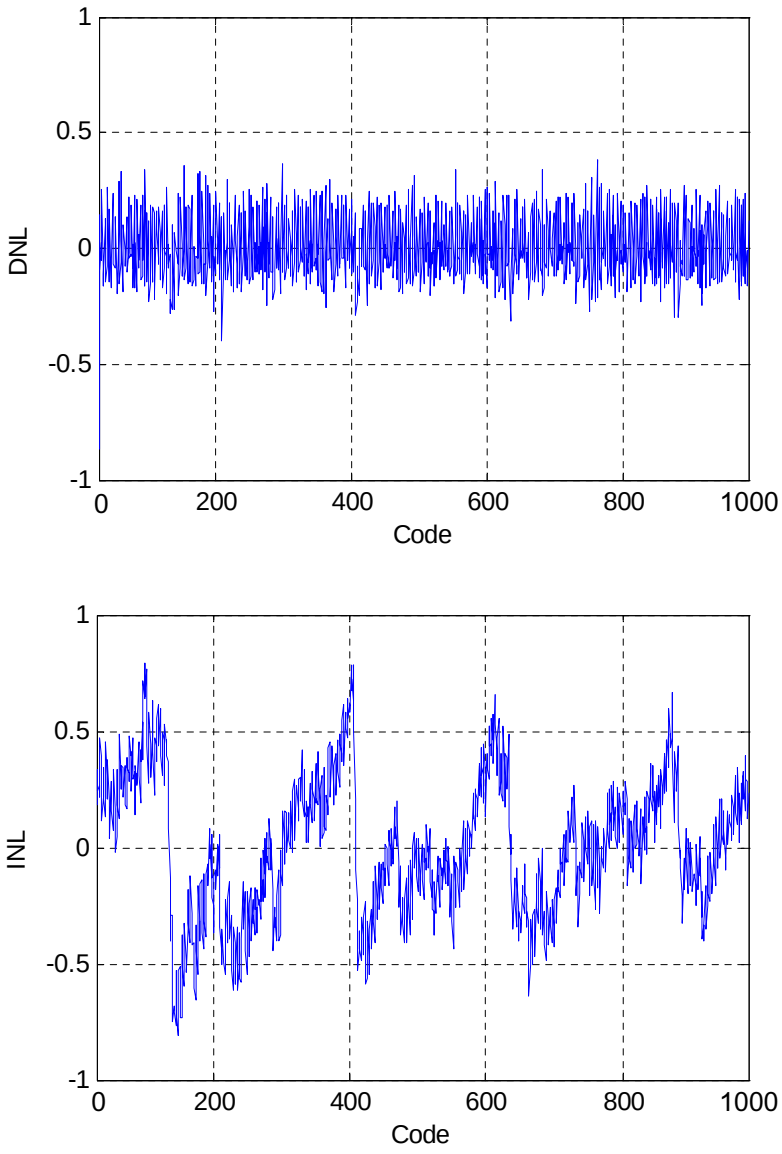


Figure 6.8: Measured DNL and INL

Technology	0.18μm CMOS process
Resolution	10 bits
Conversion rate	50MS/s
Input Range	$1.6V_{pp}$
SNDR	58.4dB (F_{in}=2.4MHz) 56.2dB (F_{in}=24.5MHz)
SFDR	72.8dB (F_{in}=2.4MHz) 72.7dB (F_{in}=24.5MHz)
THD	67.8dB (F_{in}=2.4MHz) 66.2dB (F_{in}=24.5MHz)
ENOB	9.41 (F_{in}=2.4MHz) 9.03 (F_{in}=24.5MHz)
DNL, INL	$\pm$0.39LSB, $\pm$0.81LSB
Total Power	12mW @ 1.8V Supply
Active Area	$0.86mm^2$

Table 6.1: Performance Summary

6.4 Performance Summary

The performance of the ADC is summarized in Table 6.1. The maximum input swing is $1.6V_{pp}$. The peak SNDR, SFDR, and THD are 58.4dB, 72.8dB, and 67.8dB, respectively, when the input frequency is 2.4MHz. The performances are well maintained up to the Nyquist limit. The ADC consumes 12mW at 50MS/s from a 1.8V supply. The FOM, defined as $\frac{power}{2^{ENOB}F_s}$, is 0.46 pJ/step with Fin=24.5MHz at 50MS/s. Table 6.2 shows the FOM of other ADCs recently published at the International Solid-State Circuits Conference (ISSCC). The ADC was originally targeted for higher speed operation, however, the bondwire inductance limits the ADC performance at high sampling rates. The FOM of this work is higher than [21], but is better than the other recent ADCs.

	FOM (pJ/step)
This work	0.46
[21]	0.23
[33]	0.47
[15]	0.51
[47]	0.52
[48]	0.72
[17]	0.73
[49]	0.80
[46]	0.89

Table 6.2: Comparison of FOMs

Chapter 7

Prototype Implementation II

While the ADC without a SHA successfully reduces power consumption and die area as in the first prototype design, it is difficult to achieve high-speed high-resolution operation when high-frequency signals are applied to the ADC because of aperture errors [2], [31], [40]. In the second prototype design, instead of removing the SHA, the SHA is merged with the first MDAC (SMDAC). Thus, the ADC achieves low-power operation without sacrificing speed or accuracy.

7.1 The ADC Architecture

Fig. 7.1 shows the ADC architecture including the SMDAC. The first stage consists of a SMDAC and a 3b flash ADC. The SMDAC adopts a 2.5b architecture to meet power, speed and linearity requirements. The rest of the pipeline stages consist of five 1.5b opamp-sharing stages. A feedback signal polarity inverting (FSPI) technique [6] is employed in these stages to reduce memory effects by alternating the signal polarity. The final stage is a 2b flash ADC. The ADC also has a bandgap, distributed clock generation, and reference buffers.

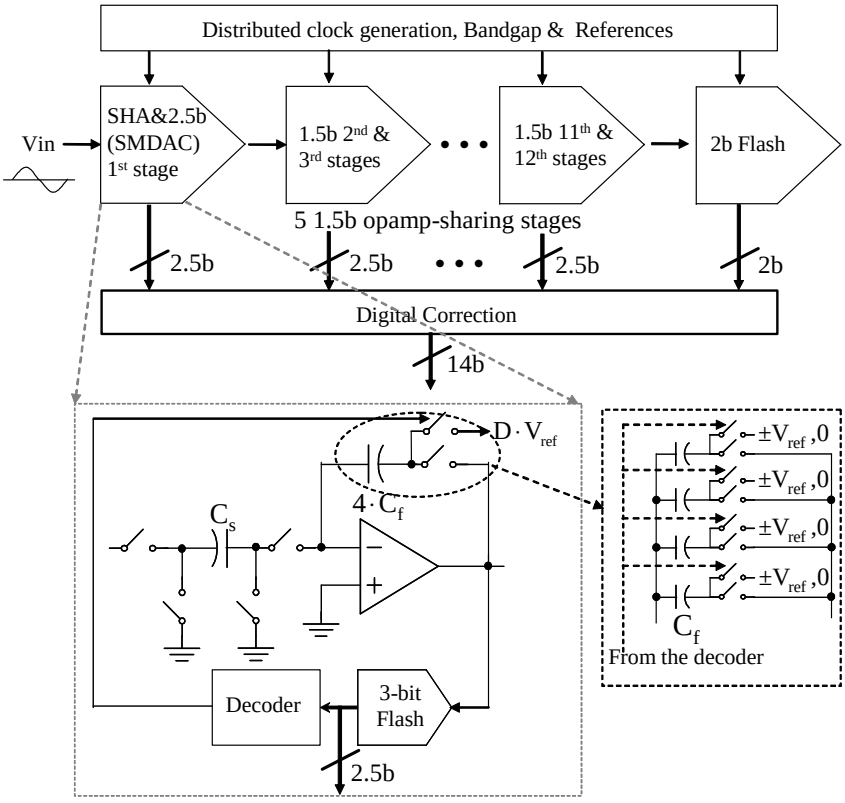


Figure 7.1: Block diagram of the ADC with SMDAC stage

7.2 Merged Active SHA and First MDAC (SMDAC)

As shown in Fig. 7.2, SMDAC works with three clock phases: sample/amplification (S/A), discharge and hold phases. During the S/A phase, the input is sampled on the sampling capacitor (C_s). While the input sample is held on C_s, the opamp and feedback capacitors (C_f) are reset to AC ground during the discharge phase. Then, in the hold phase, the charge on C_s is transferred to the C_f's and the comparators make a decision after the opamp enters the linear-settling region [6]. Capacitor sizes are carefully chosen to meet noise and matching requirements, and C_s is set to $4C_f$ for a gain of 4. In the next S/A phase, C_s is charged to the next input sample, while the charge on the C_f's is directly used for the MDAC operation, that is, one of the $4C_f$ is connected to the opamp output and the others are connected to $\pm V_{ref}$ or 0 depending on the decision from the previous phase. The rest of the pipeline stages work with a two-phase non-overlapping clock. Two important facts need to be noted in the SMDAC operation. First, the hold phase is about 30% shorter than that of a conventional SHA due to the addition of the discharge phase. However, because the MDAC operation is performed by redistributing the charge on the C_f's, the SMDAC opamp does not have to drive sampling capacitors of the following stage in the hold phase. Using this technique, the total opamp load in the hold phase is cut by about 50% compared to the conventional SHA. The reduced output load allows the SMDAC to settle fast to the required accuracy without increasing power. The second important fact is the memory effect. Since the opamp is reset during the discharge phase, there is no memory effect

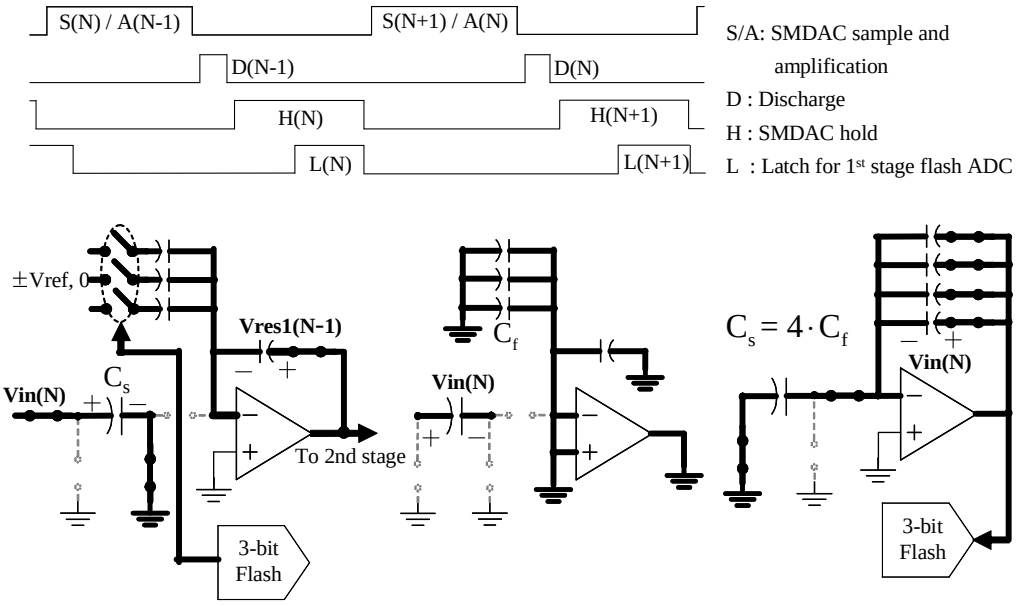


Figure 7.2: Timing diagram and SMDAC configurations at each phase

for the hold operation. However, since there is no reset phase between the hold and S/A phases, the error voltage stored on the opamp input capacitor during the hold phase can affect the SMDAC output during the S/A phase. This effect can be analyzed using the charge conservation rule. As shown in Fig. 7.3, at the end of hold phase, the total charge can be expressed as

$$Q_{total} = 4C_f \cdot [V_{in}(N) - \frac{V_{in}(N)}{A_o}] + C_p \cdot \frac{V_{in}(N)}{A_o} = 4C_f \cdot V_{in}(N) \cdot (1 + \varepsilon) \tag{7.1}$$

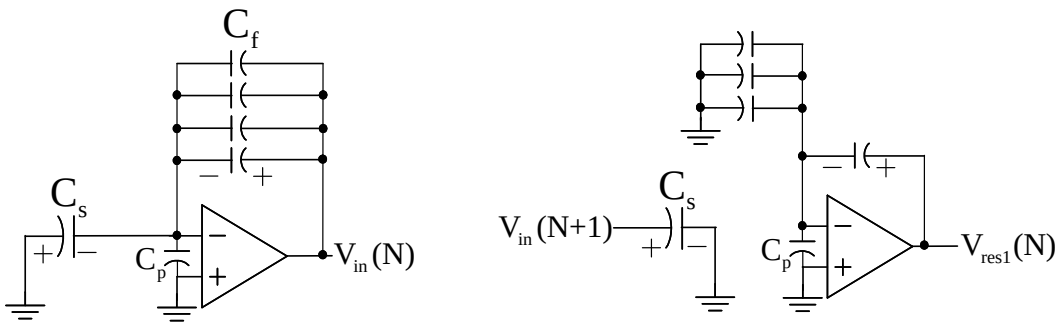
Where A_o is the opamp DC gain and . The error term (ε) caused by the opamp finite-gain (A_o) and input capacitance (C_p) is $\varepsilon = \frac{1}{A_0}[1 + \frac{C_p}{4C_f}]$. $V_{in}(N)$ is both the input sample and the output of SMDAC during the hold phase because the gain of SMDAC is 1. The charge on C_s is not considered here because it is disconnected from the opamp and the C_f's during the S/A phase. In the next phase (S/A phase), the total charge ($Q_{total}\prime$) can be expressed as

$$Q_{total}\prime = C_f \cdot V_{res1}(N) \cdot [1 + \frac{1}{A_o} \cdot (4 + \frac{C_p}{C_f})] + D \cdot C_f \cdot V_{ref} \tag{7.2}$$

where $V_{res1}(N)$ is the output of the SMDAC. D is 0, ± 1, ± 2 or ± 3 depending on the flash ADC output and assumed here to be 0 for simplicity. Since the total charge should be conserved at both phases, $Q_{total} = Q_{total}\prime$ and by ignoring the second-order error term,

$$V_{res1}(N) = \frac{4V_{in}(N) \cdot (1 + \varepsilon)}{1 + \frac{1}{A_o} \cdot (4 + \frac{C_p}{C_f})} \simeq 4V_{in}(N) \cdot [1 - \frac{1}{A_o} \cdot \frac{3}{4} \cdot (4 + \frac{C_p}{C_f})] \tag{7.3}$$

The second term in the square bracket results from the memory effect. Comparing this to the finite-gain error of a conventional switched-capacitor (SC)



(a) Hold phase **(b) Sample/Amplification phase**

Figure 7.3: Total chartge at each clock phase

amplifier with a gain of 4, i.e., $\frac{1}{\beta \cdot A_o} = \frac{1}{A_o} \cdot (4 + \frac{C_p}{C_f})$, where feedback factor, $\beta = \frac{C_f}{4C_f + C_p}$. The error is 25% smaller than that of a conventional SC amplifier. Thus, the SMDAC does not suffer from the memory effect.

7.3 High-gain Opamp

The telescopic amplifier with gain boosting is used for high DC again and power efficiency, and is shown in Fig. 7.4. The bandwidth of the opamp is carefully chosen to achieve fast-settling in each (S/A and hold) phase with a given power budget, while taking into account the variation of the feedback factor between phases. Input sampling switches for the first stage are bootstrapped. The switches in the feedback path are also bootstrapped to reduce settling-time and increase linearity.

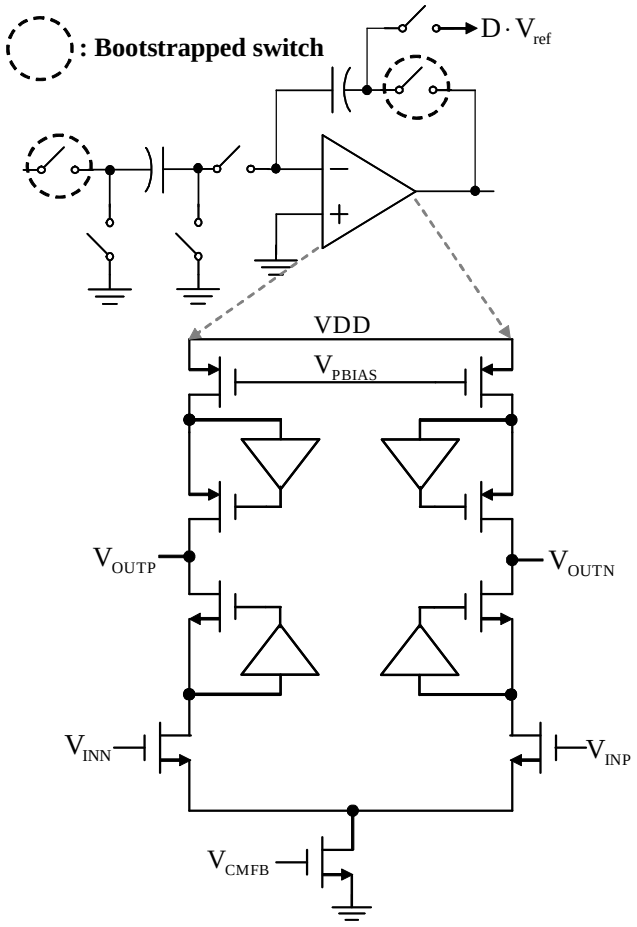


Figure 7.4: Schematic of opamp

Chapter 8

Experimental Results II

The second prototype ADC is implemented in 0.18μm dual gate-oxide (DGO) CMOS technology and occupies die area of 7.28mm^2. The die micrograph is shown in Fig. 8.1. It has a merged SHA and first MDAC stage (SMDAC) followed by five 1.5b opamp-sharing stages and a 2b flash ADC. The ADC also has a bandgap, distributed clock generation, and reference buffers. The test setup is similar to that of the first ADC. The measured FFT plots for the input frequencies 46 MHz and 135 MHz are shown in Fig. 8.2. In this design, the discharge pulse was not wide enough, which causes the high-order harmonics in the FFT plots as shown in Fig. 8.2. Thus, the measured SNR and THD are lower than the design targets of 73.5dB and 86dB, respectively. The measured SNR and ENOB vary from 70.5dB to 72.4dB and 11.4 to 11.7 for input frequencies up to 135 MHz. Fig. 8.3 shows the measured dynamic performance versus input and sampling frequencies. The measured DNL is +0.6/-0.8LSB and the INL is +2.0/-2.1LSB. As a reference, the comparison of this work and other ADCs recently published in ISSCC is shown in Table 8.2. Since power consumption grows more rapidly than the factor 2^{ENOB}, for high-resolution ADCs, a more appropriate FOM can be defined as $\frac{power}{SNR^2 \cdot Fs}$. As shown in Table 8.2, the 14-bit ADC achieves the lowest FOM.

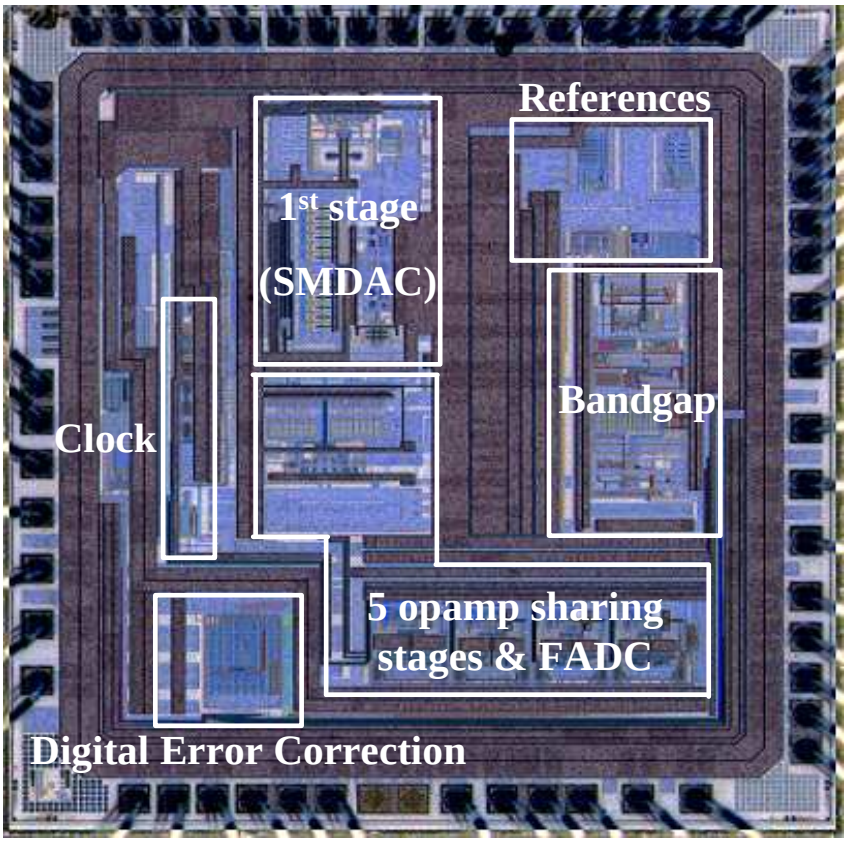
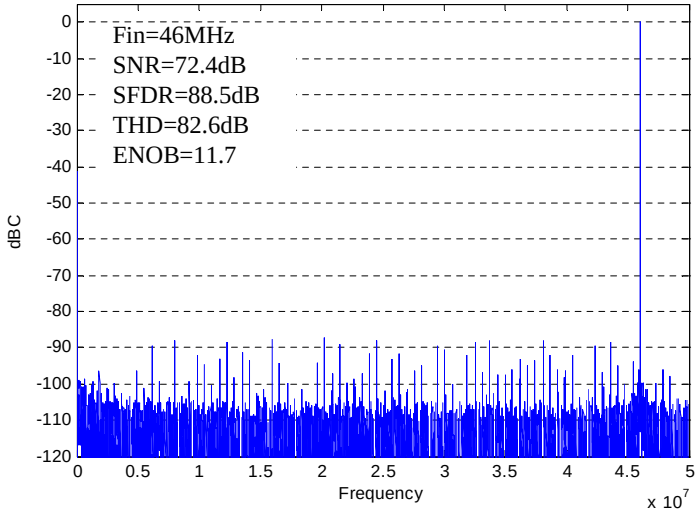
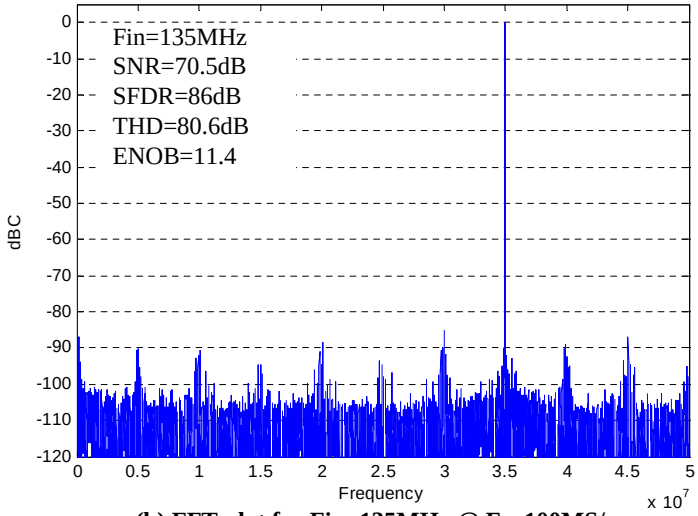


Figure 8.1: Die micrograph



(a) FFT plot for Fin=46MHz @ Fs=100MS/s



(b) FFT plot for Fin=135MHz @ Fs=100MS/s

Figure 8.2: Measured FFT plots

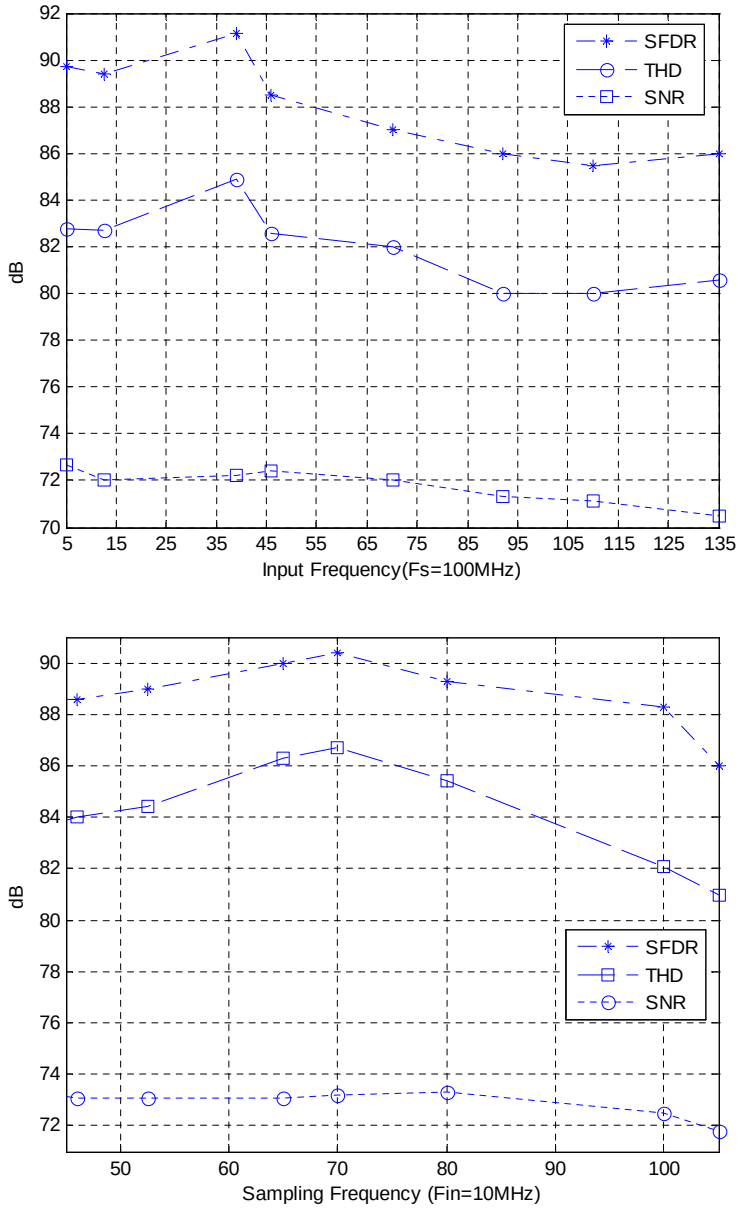


Figure 8.3: Measured dynamic performance versus input and sampling frequency

Technology	0.18μm DGO CMOS process
Resolution	14 bits
Conversion rate	100MS/s
Input Range	$2V_{pp}$
SNDR	72.2dB (F_{in}=39MHz) 70.5dB (F_{in}=135MHz)
SFDR	91.1dB (F_{in}=39MHz) 86.0dB (F_{in}=135MHz)
THD	84.9dB (F_{in}=39MHz) 80.6dB (F_{in}=135MHz)
ENOB	11.7 (F_{in}=39MHz) 11.4 (F_{in}=135MHz)
DNL, INL	+0.6/-0.8LSB, +2.0/-2.1LSB
Total Power	230mW @ 3V Supply
Active Area	$7.28mm^2$

Table 8.1: Performance Summary

	FOM [10^{-3}]
This work	0.53
[47]	2.29
[46]	4.19
[33]	4.45
[48]	4.52
[15]	5.46
[21]	5.46
[49]	6.04

Table 8.2: Comparison of FOMs

Chapter 9

Conclusion

Recent mobile SoC applications including data communication and image processing systems require multiple ADCs to be integrated into a single-chip. In these applications, a low-power and small-footprint ADC is an important building block. The main goal of this research was achieving low-power operation in a small die area without compromising speed and resolution of the ADC. Several techniques that reduce power and die size have been described. The opamp and capacitor sharing techniques achieved this goal by sharing one opamp between two successive pipeline stages, and by reusing the charge on the feedback capacitor for the MDAC operation of the following stage. The low input-capacitance variable-g_m opamp helped to further reduce power consumption by varying the bandwidth of the opamp.

Using the proposed ADC architectures and techniques, two ADCs were implemented for different applications. The first can be used for direct conversion receivers which require low-speed and moderate-resolution ADCs. The second can be used for IF-sampling superheterodyne receivers which require high-speed and high-resolution ADCs. The first ADC achieves 10-bit resolution with only two opamps by removing a front-end SHA and sharing the

opamps between two successive pipeline stages. Errors from the absence of the SHA and the memory effects of opamp-sharing are greatly reduced by the proposed techniques, namely the capacitor-sharing technique and the variable-g_m opamp. Both techniques contributed significantly to reduce power consumption and die area. The first ADC was implemented in 0.18μm CMOS technology and occupies die area of 0.86mm^2. The differential and integral nonlinearity of the ADC were less than 0.39 LSB and 0.81 LSB, respectively, at full sampling rate. The ADC achieved 56.2dB SNDR, 72.7dB SFDR, 66.2dB THD, 9.03 ENOB for a Nyquist input at full sampling rate, and consumes 12 mW from a 1.8-V supply. The second ADC achieved 72.4dB SNR and 88.5dB SFDR at 100MS/s with a 46MHz input while consuming 230mW from a 3V supply. From the simulation and measurement results, incomplete discharge of the residue introduces high-order harmonics and it is difficult to optimize the discharge time with process and temperature variations. Further study is required to implement a robust clock generation circuit for a proper discharge time.

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Index

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