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VLSI Design and Implementation of Non-Linear Decoder combined with Linear Decompressor to Achieve Greater Test Vector Compression

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VLSI Design and Implementation of Non-Linear Decoder combined with Linear Decompressor to Achieve Greater Test Vector Compression

by

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Dedication

In loving memory of my mother, Kiran Doddi, who always had confidence in my potential and gave her full support to my education. Also, I dedicate this to my father, Swamy Doddi, who guided me through my academics throughout my school years.

May 2010

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Abstract

VLSI Design and Implementation of Non-Linear Decoder combined with Linear Decompressor to Achieve Greater Test Vector Compression

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This paper investigates the cost-tradeoffs of implementing a test data compression technique previously presented in [Lee 06] which uses a small non-linear decoder combined with a linear decompressor to achieve greater test data compressions. The non-linear decoder is a sequential non-linear decompressor that exploits bit-wise and pattern-wise correlations in test vectors. This paper further emphasizes the design and implementation side of the proposed test data compressor. The linear decompressor used in this design is a Linear Feedback Shift Register (LFSR) which after choosing the right seed has the ability to produce the correct care bit values while filling the don't care value bits with pseudo-random values. Experimental results show that using the presented compression scheme here significantly improves the overall compression. Area and power results are presented for the experiments carried out on the given design.

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Chapter 1: Introduction

As the usage of digital integrated circuits is increasing in everyday life, the emphasis on placing larger and more complex designs in smaller areas using advanced process technologies is becoming more prominent. More complex designs are making testing a critical part of the design process. To tell whether a system is good or bad in Very Large Scale Integration (VLSI) circuit design testing is needed. A well designed testing strategy will be an invaluable tool in later stages of a product life, especially at system level, with enormous cost benefits.

The testing of devices after fabrication is becoming the most pressing problem for both designers and test engineers and creating a major obstacle for gaining full advantage of using very complex systems as VLSI circuits [Alleyne 94]. As the designs are becoming more complex, testing has become more expensive and time consuming. One of the problems encountered in VLSI testing is the enormous volume of test data that is required to test the circuits. Testing a digital circuit requires a set of values as its input or the *input vector* and as a result, produces a set of values on its output or the *output vector*. The result on the output side depends on the input vector and on the state of the circuit. To find a unique fault within the circuit, a specific input vector might be needed. To indentify all the faults in the circuit and to obtain a required confidence in the design, many test vectors might be needed. The number of test vectors needed depends on the complexity and the size of the circuit.

Test data compression techniques provide a way to reduce the increasing test data storage required thereby allowing usage of cost affective testers. A simple on-chip decoder has a significant role in reducing test data volume. There are various test compression schemes

already available in the field. The majority of existing test compression schemes take advantage of relatively low density of care bit values in a test cube. Test cubes are basically test vectors with don't care bit values that can be used for finding faults in a circuit. A linear decompressor, which uses only linear operations to decompress the test vectors, are good at exploiting don't care bit values across test cubes [Lee 06]. However, they are not efficient in exploiting correlations within the test cubes. A non-linear decompressor on the other hand, is efficient in exploiting correlations in the test cubes [Lee 06].

This paper investigates the technique for improving the compression achieved using a linear decompressor combined with a non-linear decompressor. It discusses the method of clustering test cubes used to form rectangles with small number of care bit values that are easy to decode using a rectangular decoder. The architecture of the rectangular decoder and the hardware design is also presented here. Finally, the paper discusses the area and power results of the implemented design in two different technologies. Considerable improvements over compression are demonstrated by presenting the experimental results obtained using the proposed technique.

Chapter 2: Proposed Design

The rectangular decoder is a sequential non-linear decompressor that is efficient in exploiting correlations in the test cubes. The proposed design here takes a linear decompressor and combines it with a non-linear rectangular decoder. The linear decompressor has a greater role in the compression since the majority of the test data is filled with don't care bit values and as previously mentioned, the linear decompressors are known to be efficient in exploiting the don't care bit values. However, the non-linear decoder can reduce the number of care bit values which in turn requires the linear decompressor to output far fewer care bit values [Lee 06]. Hence, greater compression is achieved.

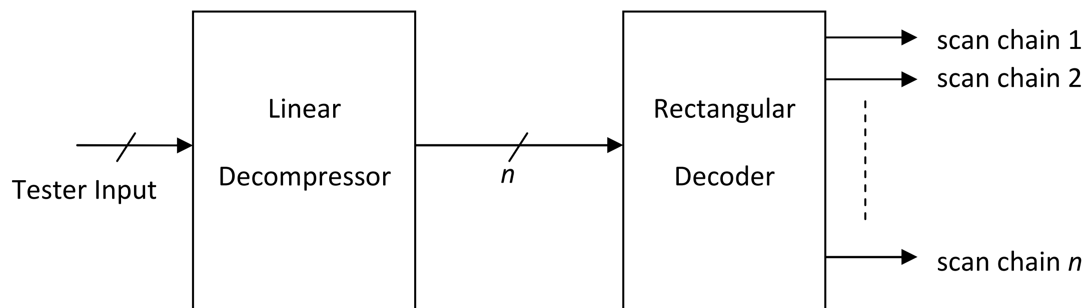

Figure 1: Linear Decompressor combined with non-linear decoder [Lee 06]

The Figure 1 above shows the block diagram of the proposed scheme. The rectangular decoder is placed between the linear decompressor and the scan chain outputs. As can be seen, the output of the linear decompressor feeds into the rectangular decoder. Because of this setup, the number of the bits required to be stored on the tester and then transferred to the linear decompressor is reduced. This drop in the tester data is linearly proportional to the fewer number of care bit values that is needed to be produced because of the decoder [Lee 06].

There are various algorithms for designing a linear decompressor and one of the commonly used techniques is the Linear Feedback Shift Register (LFSR). The LFSR algorithm can be used to exploit don't care bit values and generate a seed that will produce the correct care bit values while filling the don't care bits with pseudo-random values as a by-product [Koenemann 03]. There are many intelligent seeding algorithms to generate the right seed for the design and those algorithms are not covered in this paper. Here, we simply present a four-bit LFSR design and its function.

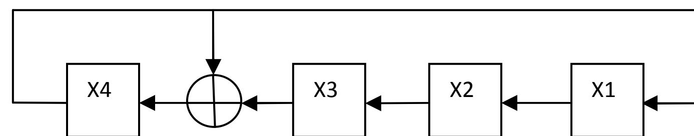

Figure 2: Linear Feedback Shift Register

The Figure 2 above shows the LFSR design used in this paper. It is a shift register with an XOR of most two significant bits. The operation of a LFSR is deterministic and the order of the values produced is fixed and is determined by the current state. The initial value loaded into the LFSR is called the seed. The following table gives results of the LFSR with the seed 0101:

X4	0	1	1	1	1	0	0	0	1	0	0	1	1	0	1
X3	1	0	1	1	1	1	0	0	0	1	0	0	1	1	0
X2	0	1	0	1	1	1	1	0	0	0	1	0	0	1	1
X1	1	0	1	0	1	1	1	1	0	0	0	1	0	0	1

Table 1: Example LFSR Sequence

Certain bit positions in test cubes tend to be correlated across many patterns and it is related to the fact that faults do not occur randomly but tend to form in clusters [Alleyne 94]. So many faults in the circuit require similar input vectors. Test cubes with similar patterns can be clustered together and form rectangles that are easy to decode. If in a test set each row

represents a test cube and each column represents a bit position, then correlations can exist across rows and columns within a test set [Lee 06].

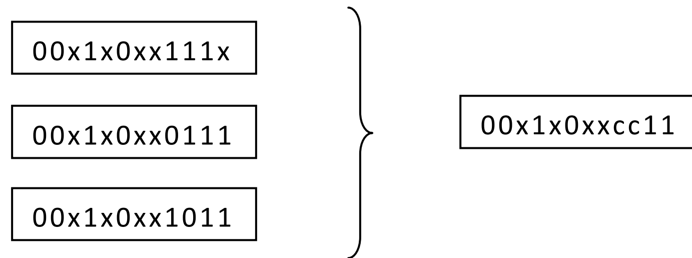

Figure 3: The Process of Clustering

Figure 3 shows an example of how test cubes of similar patterns can be clustered together. In the resulting test cluster, a value of C indicates a conflict where both 1 and 0 are present in that bit position. Once all the test cubes in the design are clustered in groups of similar patterns, each cluster is divided into rectangles [Lee 06]. The size of each rectangle is not fixed. The proper way of dividing a cluster into rectangles is by starting at the first scan slice and considering all possible rectangle widths with similar patterns until a matching point is found [Lee 06]. Once the best rectangle is identified, it is marked as selected. The process continues until all the scan slices are included as part of a rectangle. At the end the test cluster is divided into various size rectangles. The height of each rectangle is defined by the number of test cubes present in the cluster and the width is determined by the number of scan slices [Lee 06]. In this design each test cube represents a scan chain.

sc1	0	X	1	1	X	X	X	X	0	X
sc2	X	1	X	X	0	X	0	X	X	0
sc3	X	0	X	1	0	X	X	0	X	X
sc4	X	X	1	1	X	X	X	0	X	0
sc5	X	X	X	X	0	X	0	X	0	0
sc6	X	X	0	X	0	X	0	X	X	X
sc7	X	X	X	1	X	0	1	X	0	X
sc8	0	X	1	X	0	X	0	X	X	X
sc9	X	X	1	X	X	X	1	0	0	X
sc10	X	1	1	X	X	0	X	X	X	0
sc11	0	X	X	X	0	X	X	X	0	0

Table 2: Example of Rectangles

In the table above, there are eleven test cubes with similar patterns that are clustered together and added to a rectangle. This test set is then divided into multiple rectangles. This cluster can be encoded into a rectangular control data with the following parameters:

width	chain select mask bits	fill value

Figure 4: Rectangular Control Data Format

The *width* represents the size of the rectangle and the test designer can initially define the number of bits allocated for this field based on the width of the largest rectangle defined in the cluster. The second field, the *chain select mask bits,* represents how the data on to the scan chains should be loaded. Each bit in this field represents a scan chain, and the value on to the scan chain is either driven by the LFSR or loaded from the *fill value*. Fill value can either be 1 or 0, depending on the rectangle pattern.

Rect1	001	X X X X X X X X X X X	X
Rect2	011	1 1 0 1 1 0 1 1 1 1 1	1
Rect3	100	1 1 1 1 1 1 0 1 0 1 1	0
Rect4	010	1 1 1 1 1 1 1 1 1 1 1	0

Table 3: Control Data for four rectangles

The rectangular control data for the cluster in Table 2 is show in Table 3 above. In this cluster, the maximum width for a rectangle is seven, which represents the number of scan slices. There is a minimum requirement on the width for each rectangle, and it is a user-defined value [Lee 06]. For any rectangle that is smaller than this size, it is more efficient to load the bit values from the linear decompressor than by the fill value [Lee 06]. In this case, the bits in the chain select mask and the fill value can be left as don't cares. For instance, Rect1 above is only one bit wide and is directly loaded from the LFSR.

Chapter 3: Design Implementation

The sequential non-linear decoder is composed of a RAM that stores the rectangular control data, a rectangular control data register that stores the parameters for the current rectangle, a controller, a RAM address pointer, a counter for the number of scan cells and muxes for the scan chain outputs. A block diagram of the decoder with LFSR is shown below:

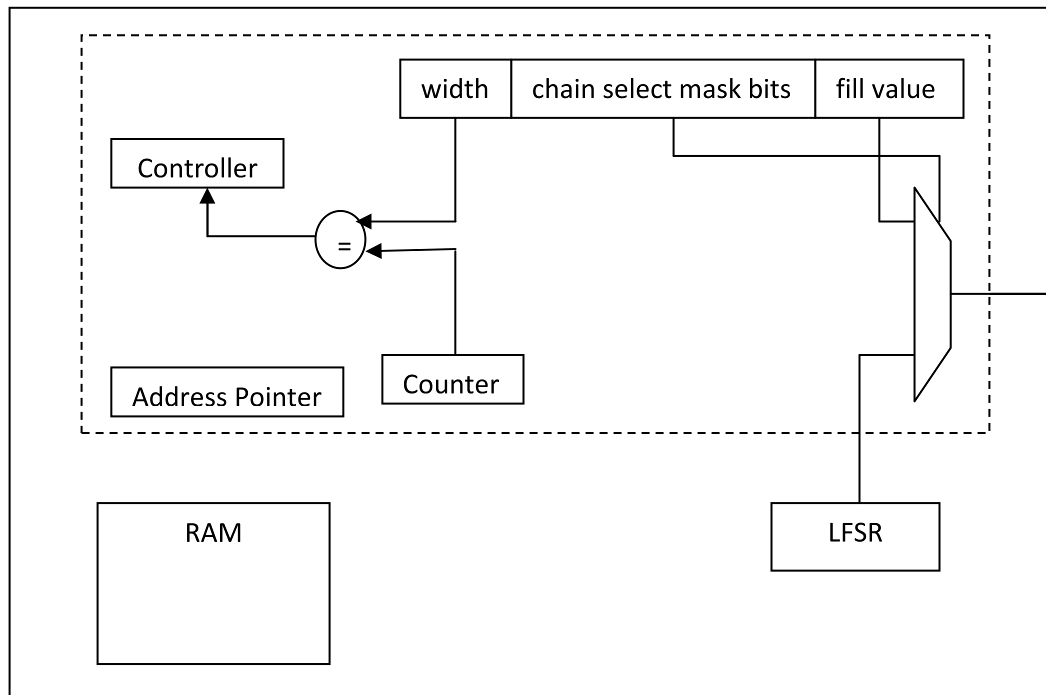

Figure 5: Rectangular Decoder with LFSR [Lee 06]

The RAM holding the rectangular control data is loaded at the beginning from the tester. It includes all the rectangles in a cluster. At the beginning of a new test session, the address pointer is reset back to the first address location and a new cluster test set is loaded into the RAM. In the hardware, the logic for the overall design has been divided into three sub-blocks: the decoder, the memory, and the LFSR. A tester is implemented to test the hardware.

The decoder includes most of the logic including the controller, address pointer, counter, rectangular control data register and the scan outputs muxing logic. The input/output (I/O) top-level diagram for the decoder is shown in Figure 6. The rectangular control data bus width is based on number of bits allocated for the width and the chain select mask bits. In the given logic, the width has been fixed to three bits and the chain select mask bits to eleven bits. The design can be modularized such that these bus widths can be easily changed depending on the design specifications.

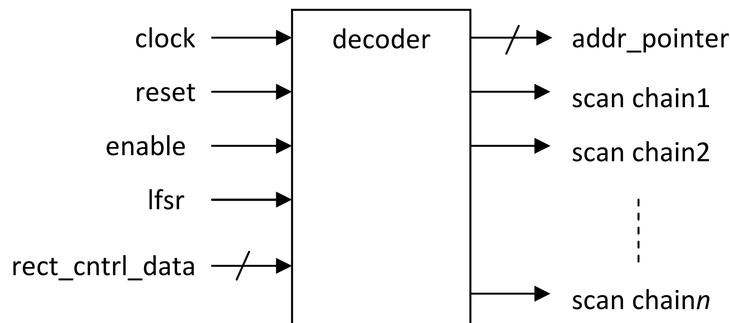

Figure 6: I/O Diagram of the Decoder

A finite state machine (FSM) is used inside the controller to implement the logic for the address pointer and the counter. There are mainly three states in the controller RSM. They are the "Reset," the "New," and the "Next." Once the clocks are running and the RAM is fully loaded from the tester at the beginning of the test session, the enable signal is asserted and the controller FSM moves from the "Reset" to the "New" state. The counter is incremented to the logical value one and compared against the width of the rectangle. If the width of the rectangle is only one, then the internal chain select mask bits are all set to zero instead of loading the bits from the rectangular control data register. A zero value on the chain select mask will mux out data from the LFSR on to the scan chain outputs instead of coming from the fill value of the

rectangular control data register. If the width is greater than one, then the counter gets incremented and the FSM remains in the “New” state till the counter is no longer smaller than the width. Then the FSM moves to the “Next” state and the address pointer of the RAM is incremented and the counter is resets to zero. The FSM stays in the “Next” state for one clock cycle to then move back to the “New” state. Again, the process continues. The state diagram for the controller RSM is shown in Figure 7.

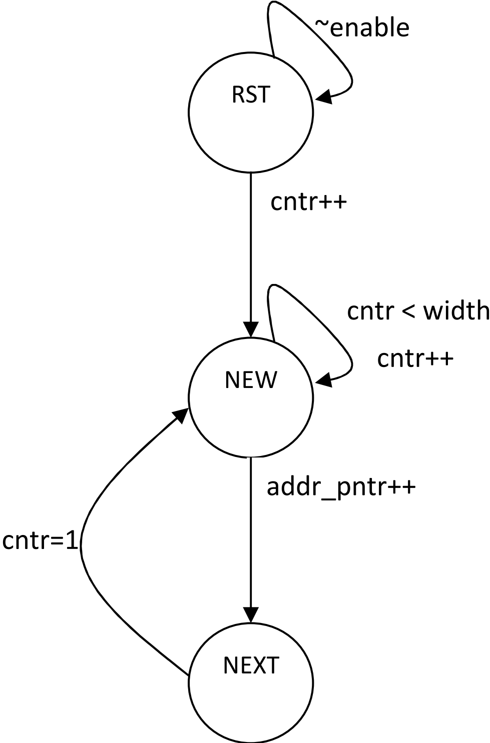

Figure 7: Controller Finite State Machine

This process repeats until the entire test cube has been shifted in. The logic has been implemented in Verilog. The Verilog design for the LFSR, the controller, and the memory is shown in the Appendix. Since the decoder has a simple, organized structure, it can be easily re-defined for any size of test data [Lee 06].

Chapter 4: Experimental Results

In the design here, experiments were performed with different number of scan chains. Changing the number of scan chains in the design affects the size of the rectangular control data register. As a result, the area and power consumption are influenced. Data are provided to show the change in area and power in two different technologies. The table below shows the area overhead in CMOS 90-nm Technology:

Type of model	Number of scan chains = 11		Number of scan chains = 20	
	Instances	Area (sq units)	Instances	Area (sq units)
Timing_model	1	45.16	1	45.16
Sequential	11,587	114,588.03	18,526	185,744.26
Inverter	439	2,796.29	706	4,496.08
Buffer	8	36.69	5	19.05
Logic	1,958	17,913.77	2,770	27,499.35
Total	13,993	135,379.94	22,008	217,803.90

Table 4: Area Report in CMOS 90-nm Technology

The timing_model in Table 4 is a simple clock structure which stays constant in both designs. It is the sequential and the combinational logic that has the greatest impact on the area. The size increased as the number of scan chains in the design increased. However, the number of buffers decreased since a design with more cells can be optimized to have fewer buffers. Similar results are provided in CMOS 45-nm Technology:

Type of model	Number of scan chains = 11		Number of scan chains = 20	
	Instances	Area (sq units)	Instances	Area (sq units)
Timing_model	1	3.99	1	3.99
Sequential	11,587	43,196.01	18,526	69,045.35
Inverter	81	178.75	109	275.04
Buffer	2	1.60	5	5.59
Logic	2,086	4,534.24	2,944	6,822.10
Total	13,757	47,914.58	21,585	76,152.08

Table 5: Area Report in CMOS 45-nm Technology

In the past, power consideration was mostly of only secondary importance, after area and speed [Pedram 95]. However, this has begun to change and increasingly power is being given comparable weight to area considerations. There are two important factors in power consumption, leakage power and dynamic power. Leakage power has become dominant contributor to the total power consumption, up to almost fifty percent in certain fabrication technologies [Lu 08]. The charging and discharging of the node capacitances is what contributes to the dynamic power dissipation [Pedram 95]. The following tables show the power consumption of the VLSI design for the decoder in two different process technologies:

Scan chains	Cells	Leakage Power (µW)	Dynamic Power (µw)	Total Power (µW)
11	13993	4.769	0.611	5.379
20	22008	8.650	0.933	9.584

Table 6: Power Report in CMOS 90-nm Technology

Scan chains	Cells	Leakage Power (µW)	Dynamic Power (µw)	Total Power (µW)
11	13757	1.887	0.291	2.178
20	21585	3.007	0.494	3.501

Table 7: Power Report in CMOS 45-nm Technology

Both the area and the power reports show that results for the design are better in CMOS 45-nm technology compared to CMOS 90-nm technology. Reduction in chip size has numerous advantages, including area and power usage.

The following results are previous experiments that have been performed on large circuits using the non-linear decoder. Results show that the decoder significantly reduced the number of care bit values that the linear decompressor has to produce. The experimental results from the circuit s13207 are shown in Table 8.

Test cubes	Original Spec. Bits	Num. Clusters	Scan Chains	Num. Rect.	Total Rect. Control bits	Total Spec. Bits	Reduction (%)	RAM (bits)
266	9389	8	10	86	10	6900	26.5	130
			20	75	15	7056	24.8	150
			30	54	20	7563	19.5	180

Table 8: Results from circuit s13207 [Lee 06]

There are three different number of scan chains used in the experiment. As the number of scan chains increases, the number of specified bits required for the proposed scheme increases slightly which does not have much impact on the overall reduction. Also, when there are test cubes with similar patterns, the design can be modified such that each chain select mask bit represents more than one scan chain [Lee 06]. However, this might have an impact on the pattern matching between test cubes and can lower the compression. Experimental data shows that best results happen when each chain select mask bit represents two scan chains [Lee 06].

Better compressions can also be achieved by increasing the number of bits used for the rectangle width [Lee 06]. When there are more bits in a rectangle (larger rectangles) it means there is more compatibility between the test data and this gives higher compression results. However, if the total number of bits used for rectangle width increases, the scope for narrow rectangles (any rectangle that is smaller than the user-defined rectangle width) increases and that will lead to more specified bits to be produced by the linear decompressor. Experimental results show that best results for compression happen when four bits are used for representing rectangle width [Lee 06].

Chapter5: Conclusion

This paper has focused on the design of a simple non-linear decoder that can be used along with linear decompressor to reduce the number of specified bits. The linear decompressor chosen in this design is a LFSR. The design turned out to be relatively simple using one finite state machine inside the controller and few muxes. The experimental results show the possibility of tangible data volume reduction by using the decoder. Not only does the technique presented here show greater compression results than previous schemes of combining linear and non-linear compression techniques [Lee 06], the decoder design is also fairly simple and independent of the test data. The next step will be to explore better pattern-wise correlations in the test data to obtain better encoded rectangular control data that specify more care bit values. In addition, using a different kind of linear decompressor other than a LFSR might have an impact on the overall design size and data compression.

Appendix A: Decoder Logic

```
module decoder (clk,reset,enable,lfsr,addr,rect_cntrl_data,
            sc1,sc2,sc3,sc4,sc5,sc6,sc7,sc8,sc9,sc10,sc11);
   input      clk;
   input      reset;
   input      enable;
   input      lfsr;
   output [7:0] addr;
   input  [14:0] rect_cntrl_data;
   // scan chains
   output     sc1;
   output     sc2;
   output     sc3;
   output     sc4;
   output     sc5;
   output     sc6;
   output     sc7;
   output     sc8;
   output     sc9;
   output     sc10;
   output     sc11;
```

```
wire [2:0]  width_rect_cntrl;

wire [10:0] chain_select_mask;

wire        fill_value;

reg [2:0]  counter, counter_reg;

reg [1:0]  state, next;

reg [7:0]  addr;

parameter [1:0] RST = 2'b00,

               NEW = 2'b01,

               NEXT= 2'b10;

assign sc1 = chain_select_mask[10] ? fill_value : lfsr;

assign sc2 = chain_select_mask[9] ? fill_value : lfsr;

assign sc3 = chain_select_mask[8] ? fill_value : lfsr;

assign sc4 = chain_select_mask[7] ? fill_value : lfsr;

assign sc5 = chain_select_mask[6] ? fill_value : lfsr;

assign sc6 = chain_select_mask[5] ? fill_value : lfsr;

assign sc7 = chain_select_mask[4] ? fill_value : lfsr;

assign sc8 = chain_select_mask[3] ? fill_value : lfsr;

assign sc9 = chain_select_mask[2] ? fill_value : lfsr;

assign sc10 = chain_select_mask[1] ? fill_value : lfsr;

assign sc11 = chain_select_mask[0] ? fill_value : lfsr;


assign width_rect_cntrl[2:0] = (~enable) ? 3'b000: rect_cntrl_data[14:12];
```

```
assign chain_select_mask[10:0] = (~enable) ? 11'b000_0000_0000 :
                                 (rect_cntrl_data[14:12] < 3'b010) ? 11'b000_0000_0000 :
                                                                     rect_cntrl_data[11:1];
assign fill_value = (~enable) ? 1'b0 : rect_cntrl_data[0];


always @ (posedge clk) begin
 if (reset) begin
   state <= RST;
   counter_reg <= 3'b000;
 end else begin
   state <= next;
   counter_reg <= counter;
 end
end
always @ (state,enable,reset,counter_reg) begin
 case (state)
  RST: begin
       counter = 3'b000;
       addr = 8'h00;
       if (enable) begin
         next = NEW;
         counter = counter + 1;
```

```
      end else begin
        next = RST;
      end
     end
  NEW: begin
       counter = counter + 1;
       if (counter_reg < width_rect_cntrl) begin
        addr = addr;
        next = NEW;
      end else begin
        addr = addr + 1;
        next = NEXT;
      end
     end
  NEXT:begin
       addr = addr;
       counter = 3'b1;
       next = NEW;
     end
  endcase
 end
endmodule
```

Appendix B: LFSR Logic

```
module lfsr (clk,reset,enable,seed,q_out);
  input      clk;
  input      reset;
  input      enable;
  input  [3:0] seed;
  output      q_out;

  reg [3:0] q;
  wire     linear_feedback;

  assign linear_feedback = (q[3]^q[2]);
  assign q_out = q[3];

  always @ (posedge clk)
   if (reset) begin
     q <= seed;
   end else if (enable ) begin
     q <= {linear_feedback, q[1], q[0], q[3]};
   end

endmodule
```

Appendix C: RAM Logic

```
module mem (clk,r_wb,addr,d,q);
   input       clk;
   input       r_wb;
   input  [7:0] addr;
   input  [14:0] d;
   output [14:0] q;


   reg [14:0] q;
   reg [14:0] mem_bank [0:255];


   always @(r_wb)
      if (r_wb) q=mem_bank[addr];
      else mem_bank[addr]=d;
   always @(addr)
      if (r_wb) q=mem_bank[addr];
      else mem_bank[addr]=d;
   always @(d)
      if (r_wb) q=mem_bank[addr];
      else mem_bank[addr]=d;
endmodule
```

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Vita

Srujana Doddi was born in Hyderabad, India on the 15th of July 1981. She moved to United States of America in May 1995. After her schooling at James Madison High School in San Antonio, TX, she received her Bachelor of Science (B.S.) in Electrical Engineering from The University of Texas, Austin in December, 2003. She joined the University of Texas at Austin in Spring 2007, to pursue her Master of Science. She has been working with the company Freescale Semiconductors since February 2004.

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