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System Oriented Delta Sigma Analog-to-Digital Modulator Design for Ultra High Precision Data Acquisition Applications

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System Oriented Delta Sigma Analog-to-Digital Modulator Design for Ultra High Precision Data Acquisition Applications

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Dedicated to my family

System Oriented Delta Sigma Analog-to-Digital Modulator Design for Ultra High Precision Data Acquisition Applications

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As high precision data acquisition systems continue to improve their performance and power efficiency to migrate into portable devices, increasing demands are placed on the performance and power efficiency of the analog-to-digital conversion modulator. On the other hand, analog-to-digital modulator performance is largely limited by several major noise sources including thermal noise, flicker noise, quantization noise leakage and internal analog and digital coupling noise. Large power consumption and die area are normally required to suppress the above noise energies, which are the major challenges to achieve power efficiency and cost targets for modern day high precision converter design. The main goal of this work is to study various approaches and then propose and validate the most suitable topology to achieve the desired performance and power efficiency specifications, up to 100 kHz bandwidth with 16-21 bits of resolution.

This work will first study various analog-to-digital conversion architectures ranging from Nyquist converters such as flash, pipeline, to the delta sigma architecture. Advantages and limitations of each approach will be compared to develop the criteria for the optimal modulator architecture. Second, this work will study analog sub-circuit blocks such as opamp, comparator and reference voltage generator, to compare the advantages and limitations of various design approaches to develop the

criteria for the optimal analog sub circuit design. Third, this work will study noise contributions from various sources such as thermal noise, flicker noise and coupling noise, to explore alternative power and die area efficient approaches to suppress the noise. Finally, a new topology will be proposed to meet all above criteria and adopt the new noise suppression concepts, and will be demonstrated to be the optimal approach. The main difference between this work from previous ones is that current work places emphasis on the integration of the modulator architecture design and analog sub-circuit block research efforts.

A high performance stereo analog-to-digital modulator is designed based on the new approach and manufactured in silicon. The chip is measured in the lab and the measurement results reported in the dissertation.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

The proliferation and advance of digital signal processing algorithms and circuits have generated increasingly stringent requirements for data acquisition circuits used in various systems ranging from industrial and medical high precision measurement applications to professional audio recording. Figure 1.1 shows multiple major applications.

Wide dynamic range and low distortion are needed to capture an analog input signal in its most original form, which, in most cases, is the most crucial step to achieve the performance target. High precision applications such as industrial measurement, medical diagnostics, and professional audio have continued to improve their performance and efficiency due to the rapid advance and availability of high-precision data acquisition technology as well as digital signal processing (DSP) technologies to improve precision in the digital domain. These applications are also rapidly migrating into USB-powered and portable devices, placing increasing stringent demands on the power efficiency and performance of high precision analog to

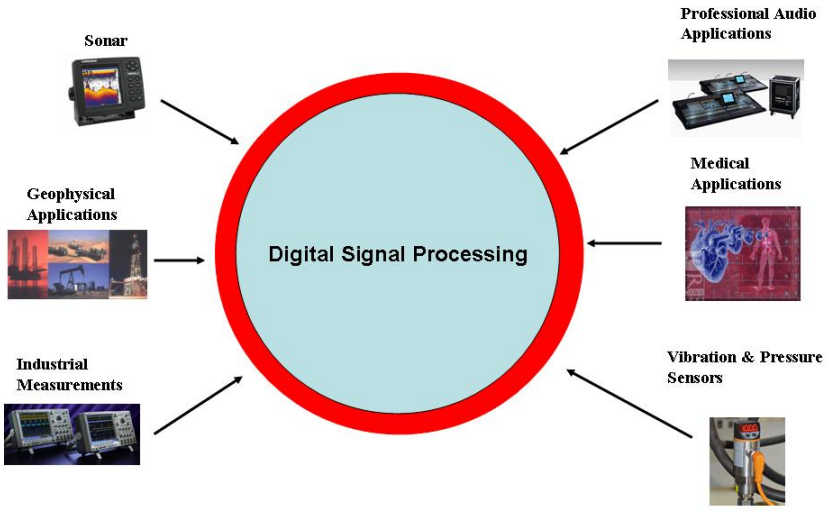


Figure 1.1: "Egg" model [1] for high precision analog to digital data conversion

digital conversion design. Following is a summary of several key application areas.

1. In audio applications, noise floor needs to be exceptionally stable, free from tones as the input level is varied, and ideally be flat throughout the audio signal band which is from 20Hz to 20 kHz. This requirement arises mainly because human hearing is very sensitive to the audibility of noise floor modulation and spurious tones. Normally, 128 sound channels are needed for professional audio applications such as recoding studios. Low cost and low power consumption are also important to this market.

2. Sonar applications require high performance over wider bandwidth, ranging from 40kHz to 100kHz. Power consumption has to be reduced for portable sonar devices.

3. Industrial, Agriculture and Medical measurement applications have various performance requirements. Geophysical application requires high performance over narrow bandwidth from DC to 1 kHz across a wide temperature range. Offset and offset drift also have to be kept low for these applications. On the other hand, vibration detection sensors need high performance over a 100 kHz bandwidth. In order to process multiple input signals in different signal bands simultaneously, the converter also has to maintain high linearity to avoid interference between signal channels.

Several designs [10] [11] [12] [13] have been developed throughout the years to address various applications. Single bit, single loop delta sigma topology was first applied to achieve 120dB dynamic range over the audio band [12]. However, as high precision measurement applications such as professional audio and industrial measurement etc., enter the consumer market, there is increased demand for higher levels of linearity and dynamic range with lower cost. However, high power consumption not only makes it difficult to achieve expected performance on the circuit board, but also increases system level cost due to package, heat sink, etc., especially for multi-channel applications.

Achieving high performance with high levels of analog and digital circuit integration, while maintaining low power consumption and small die area, are the major challenges for future high precision analog to digital converter design. Multi-bit delta sigma topology becomes popular nowadays for high performance converter design mainly due to its ability to reduce integrator output swings, which relaxes analog circuit design requirements and reduces power consumption. Such a benefit becomes more critical for high performance A/D converter design. A multibit delta-sigma topology with a large number of quantization levels also significantly lowers

the out-of-band quantization noise energy, which greatly relaxes the decimation filter design requirements. Since the quantizer is inside the delta-sigma loop, it can only tolerate minimum latency. A flash type A/D converter is normally adopted for the quantizer due to its low latency. However, each additional bit of resolution for the quantizer doubles its power consumption and die area. The power consumption increase of the quantizer quickly outweighs the benefit and power saving from low integrator output voltage swings. A large number of comparators also inject a substantial amount of signal dependant noise energy into the substrate, which causes degradation of converter performance and interference between channels in the case of multi-channel converter design. Clock jitter sensitivity [14] [15] is another major concern for high performance converter design. It is important to ensure that the converter clock jitter requirement is reasonable to achieve in a real world environment. A switched capacitor topology is widely used for analog circuit implementation due to its better immunity to clock jitter. However, charge injection from the switched capacitor input sampling network tends to degrade the performance of the input anti-alias filter, which limits the achievable performance of the converter. Although increasing the oversampling ratio decreases the sampling capacitor size, this translates to less settling time for integrator opamp and digital switching noise, which makes the converter sensitive to digital coupling noise.

1.2 Research Goals

Besides the performance targets, this work will also focus on die area and power efficiency of the analog-to-digital conversion system. The main goal of this work is to develop a system-oriented design approach to achieve the desired performance and power dissipation specifications up to 100kHz bandwidth with 16-21 bits of

resolution.

The goal of this work can be further summarized as follows:

1. To develop a system-oriented power and die area efficient modulator architecture which maximally relax the design requirements for analog sub blocks.

2. Study existing design trade offs for analog sub circuit blocks to take advantage of the new power efficient architecture.

3. Study noise contributions from various sources such as thermal noise, flicker noise and digital coupling noise to explore the power and die area efficient approaches to suppress above noises.

4. Design a stereo converter based on the newly proposed design approach to validate the approaches.

1.3 Thesis organization

Chapter 2 covers basic background information of analog to digital converters, which includes key converter performance specifications, major design challenges and system level overview of major analog to digital topologies.

Chapter 3 introduces the fundamentals of various oversampling delta sigma design approaches. Major design trade offs and impacts of different non-idealities will also be discussed.

Chapter 4 provides system level analysis of delta sigma modulator architecture, sub circuit design trade offs and challenges for high precision data acquisition applications. An optimal modulator architecture design criteria for base band high precision analog to digital converters will be developed. The study will also cover the circuit board and chip layout challenges.

Chapter 5 proposes an optimal modulator architecture for high precision applications. Detailed analysis of the new modulator will be presented.

Chapter 6 studies design trade offs for analog sub blocks. The study will be focused on approaches which take advantage of the newly proposed modulator architecture to further improve the converter power and die area efficiency.

Chapter 7 studies circuit board and chip layout approaches.

Chapter 8 presents chip measurement results.

Chapter 9 summarizes and concludes the study. This chapter also discuss possible future directions for this area.

Chapter 2

Analog to Digital Conversion Fundamentals

Analog to digital conversion operation captures real world signals into the digital domain to be further processed by digital signal processing circuits. The proliferation of digital signal processing circuits and advance in semiconductor process technologies make the analog to digital converter becoming the major bottleneck to further advance the performance and power efficiency of data acquisition system to the next level.

2.1 Nyquist's criterion

The Nyquist's criterion forms the foundation for analog to digital conversion. Nyquist's criterion [2] defines the conditions to reconstruct a uniformly sampled bandlimited signal.

$$f_s > 2f_{sig} \tag{2.1}$$

where f_s refers to the sampling frequency and f_{sig} refers to the upper input signal frequency limit. Periodic sampling process introduces spectral replications, which is periodically spaced by f_s. The Equation 2.1 is necessary to prevent overlap of such spectral replications. The distortion caused by the overlapping of these periodic spectral replications is commonly referred to as aliasing. An analog anti-aliasing filter is normally placed in front of the analog to digital converter to attenuate signal energy above f_s. Converter sampling rate is the number of times the input signal is sampled per second.

2.2 Quantization error

Quantization error is the difference between input signal and the quantized output. As illustrated in Figure 2.1, if we assume the input changes randomly, the input has equal possibility of lying anywhere within the quantization step. This statistical property suggests the quantization error is independent of input signal and can be represented as a noise, which is also referred as quantization noise.

If we further assume the quantization step is δ, then the quantization error has equal probability of lying anywhere in the range of $+/-\frac{\Delta}{2}$. The mean square value for quantization error is

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} \tag{2.2}$$

The signal to noise ratio (SNR) is the ratio between power of sine wave input and integrated noise power across the band of interest. SNR is widely used to evaluate the performance of a analog to digital converter.

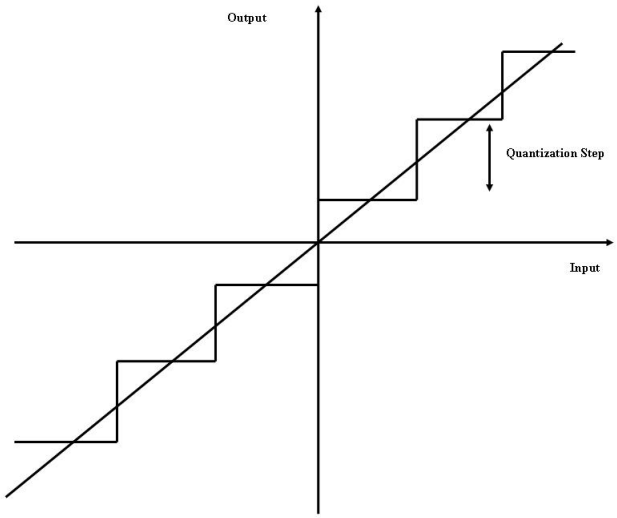


Figure 2.1: Analog to digital conversion

$$SNR = 10\log(\frac{P_{sig}}{P_{noise}}) \tag{2.3}$$

For sine wave input with signal peak amplitude is defined as A, the quantization step for N bit analog to digital converter is:

$$\Delta = \frac{2 \cdot A}{2^N - 1} \tag{2.4}$$

Insert Equation 2.4 to Equation 2.2

$$e_{rms}^2 = \frac{(\frac{2 \cdot A}{2^N - 1})^2}{12} \approx \frac{(\frac{2 \cdot A}{2^N})^2}{12} \tag{2.5}$$

The signal root mean square value is:

$$A_{rms}^2 = \frac{A^2}{2} \tag{2.6}$$

Inserting Equation 2.5 and Equation 2.6 to Equation 2.3

$$SNR[dB] = 10 \cdot \log_{10}(\frac{A_{rms}^2}{e_r ms^2}) = 10 \cdot \log_{10}(\frac{3}{2} \cdot 2^{2 \cdot N}) \tag{2.7}$$

$$SNR[dB] = 1.76 + N \cdot 6.02 \tag{2.8}$$

Equation 2.8 indicates 6dB SNR improvement per 1 bit resolution increase.

Dynamic range measurement is widely used to evaluate the range of input signal amplitudes for which the analog to digital converter can obtain meaningful output. If the converter noise power is independent of the input signal magnitude, then the dynamic range is equal to the SNR measurement. However, in most cases, converter noise power increases with the input signal level. For most high precision applications such as audio devices, dynamic range is normally obtained by measuring the SNR with -60dB input signal and then adding 60dB to the measurement results. Basically, such dynamic range measurement indicates the maximum dynamic range that can be obtained from this device before distortion component become non negligible.

2.3 Major Design Challenges for Analog to Digital Conversion

2.3.1 Input sampling network design

Input sampling network normally convert a continuous time signal into a discrete time signal at a fixed sampling rate. Ideal input sampling network samples the input signal without adding noise or distortion. The precision of the input sampling stage

sets up the upper limit of the achievable performance of the converter.

PMOS, NMOS or T-gate configuration is widely used as switches in the actual circuit design. Several issues are associated with MOS switches. One problem is for NMOS transistor, when the transistor is turned off the gate voltage reaches $V_{dd} - V_t$, where V_{dd} is the circuit supply voltage and V_t is the NMOS threshold voltage. PMOS encounters similar issues during discharging operation. Using T-gate configuration can mitigate this issue. Another issue happens in the switches' turning on and off period. In this period, the transistor goes through different operational region. For NMOS, when $V_{ds} > V_{ds} - Vt$, the transistor is in the saturation region, or the transistor enters the linear region. On the other hand, for a switched capacitor circuit, the capacitor size is normally determined by thermal noise target while the switch resistance is determined by the network's speed requirement to sample the signal without distortion. As MOS switch is fully turned on, the resistance is defined as

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{gate} - V_{in} - V_{TH})} \tag{2.9}$$

where μ is the transistor mobility, C_{ox} is the unity gate capacitance, W is the channel width, L is the channel length, V_{TH} is the threshold voltage which is different between NMOS and PMOS switches. Large channel width or high gate voltage is needed to lower the MOS switch resistance. The time constant of a switched capacitor sampling network is defined as

$$\tau = C \cdot R_{ON} = \frac{CL}{\mu C_{ox} W(V_{gate} - V_{in} - V_{TH})} \tag{2.10}$$

On the other hand, when a MOS switch is turned on, there is a conducting

channel formed under the gate. Total charge within this channel is

$$Q = WLC_{ox}(V_{gate} - V_{in} - V_{TH}) \tag{2.11}$$

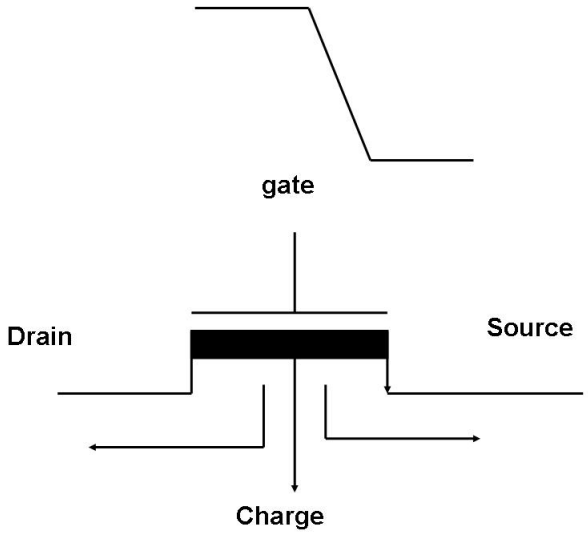


Figure 2.2: MOS switch charge injection when the switch turns off

When the switch is turned off, the charge is released from the channel and dumped to either source and drain capacitor. The exact charge dumped on either node depends on impedance difference between source and drain and the clock falling time. This error is commonly referred as charge injection error [16], [19]. It is easy to conclude from equation 2.11 that the charge injection error degrades sampling network performance since the charge itself is input signal dependant. Second order effect such as body effect further complicates this issue. For example, the threshold voltage for NMOS transistor is defined as

$$V_{th} = V_{th0} + \gamma(\sqrt{2\phi_b + V_{bs}} - \sqrt{2\phi_b}) \tag{2.12}$$

Insert equation 2.12 into equation 2.11

$$Q = WLC_{ox}(V_{gate} - V_{in} - V_{th0} - \gamma(\sqrt{2\phi_b + V_{bs}} - \sqrt{2\phi_b})) \tag{2.13}$$

As the input signal varies, different amount of charge is formed under the gate. The amount of charge dumped to source and drain nodes varies after MOS switch are turned off.

MOS switches also couple gate clock control signal to the sampling capacitor through gate to drain or gate to source parasitic capacitors. As shown in Figure 2.3, this error is commonly referred as clock feedthrough. The error voltage can be expressed as

$$\Delta V = V_{clk}\frac{C_{gs}}{C_{gs} + C_s} \tag{2.14}$$

where V_{clk} is the clock voltage, V_{gs} is parasitic capacitance between gate and source and V_s is the sample capacitor.

2.3.2 Major noise sources

As shown in Figure 2.4, MOS switches can be modeled as resistors when they are turned on. Resistor thermal noise spectral density is 4kTR, where k is the Boltzmann constant. The thermal noise of the MOS switch resistance can be modeled as a serial voltage source,V_R.

Total thermal noise power of switched capacitor circuits is the low passed result of the switch resistor thermal noise.

$$\frac{V_{out}}{V_R} = \frac{1}{RC + 1} \tag{2.15}$$

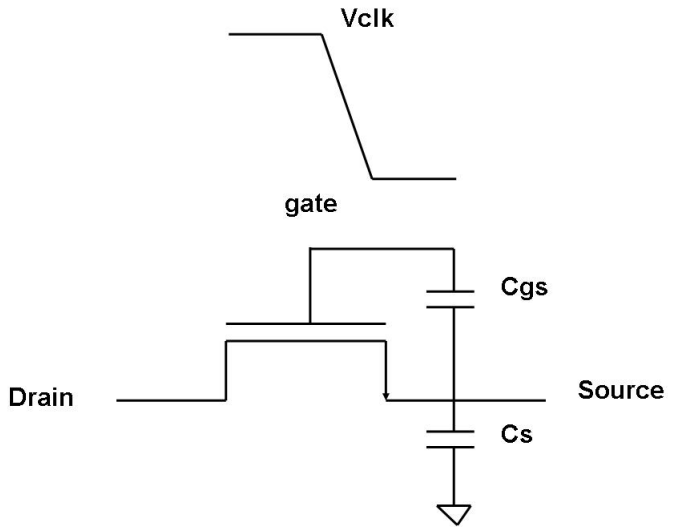


Figure 2.3: Clock feedthrough in switched capacitor circuit

Output spectral density is

$$S_{out} = \frac{4kTR}{4\pi^2 R^2 C^2 f^2 + 1} \tag{2.16}$$

where f is frequency. Equation 2.16 indicates the resistor thermal noise is low pass filtered.

$$P_{total} = \int_0^\infty \frac{4kTR}{4\pi^2 R^2 C^2 f^2 + 1} df \tag{2.17}$$

where P_{total} is the total integrated noise power. after apply

$$\int \frac{dx}{x^2 + 1} = tan^{-1} x \tag{2.18}$$

Equation 2.19 becomes

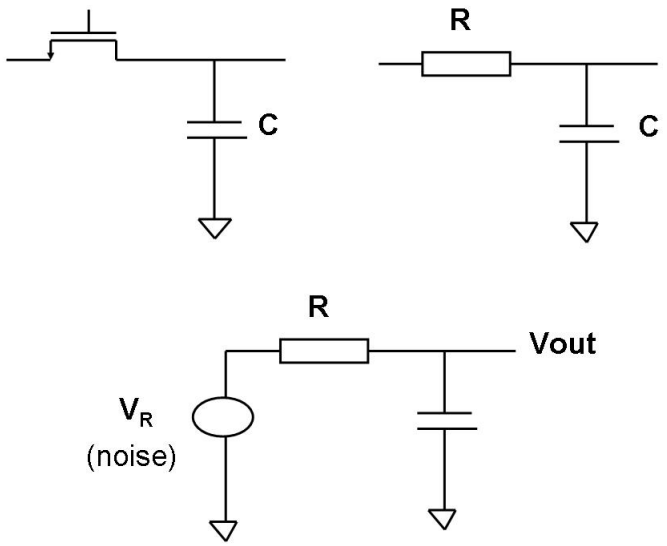


Figure 2.4: Switched capacitor thermal noise calculation

$$P_{total} = \frac{kT}{C} \tag{2.19}$$

The total integrated noise is independent of switch resistance. The total integrated noise can only be reduced by increasing capacitor size, which create multiple design challenges for high precision converter design.

A MOS transistor also generates thermal noise. It can be modeled by a current source between drain and source terminals.

$$I^2 = 4kT\gamma g_m \tag{2.20}$$

where γ varies for different process.

Another major noise source for baseband converter design is flicker noise. Flicker noise varies on multiple factors such as doping profile, voltage over gate and source [21], which makes it very difficult to model the flicker noise accurately. The

noise voltage can be roughly expressed as

$$V^2 = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.21}$$

where K is the process dependent constant. Equation 2.21 suggests device area has to be increased to reduce the noise, which results in substantial die area penalty for high precision design.

Substrate digital noise coupling is another major noise source for single die mixed signal design, especially for high precision design. Substrate noise generators include switching devices, digital ground bouncing, substrate contacts bouncing etc. They pump signal dependant current pulse into the common substrate. On the victim side, the substrate noise current affects sensitive analog node and ground through body effect and parasitic capacitance. Effects of switching noise on digital circuits range from false switching to delay variations. It affects the analog circuit through direct coupling into signal path or degrading sensitive analog signals such as reference voltage or critical analog clock edge. [23] [24] We can observe from Figure 2.5 that digital switching noises couples to analog sensitive nodes through substrate. Modern day mixed signal design commonly has tens of thousands digital gates switch simultaneity to generate a large amount of noise energy into the substrate. Three general approaches are applied to minimize the substrate noise.

1. Reduce the amount of noise injected into the substrate

2. Design circuits so that it is less sensitive to substrate coupling

3. Divert the substrate noise current away from the sensitive nodes. Guard ring and Nwell trench Guard ring and Nwell trench are commonly utilized to protect the sensitive nodes. [25] The ring is a surface region heavily doped with

the majority-carrier dopant and is intended to form a Faraday shield around any sensitive devices, which need to be protected from the substrate noise. A well thought layout floor plan diverts coupling noise current away from the most sensitive nodes. An on/off chip bypass capacitance can also be added to minimize the supply and ground fluctuation. Normally these methods result in substantial die area penalty, especially for high precision design. On the other hand, various design decisions such as circuit's structure for reference block in analog section or different filter algorithm for digital filters etc. have to be decided at early stage of the design phase.

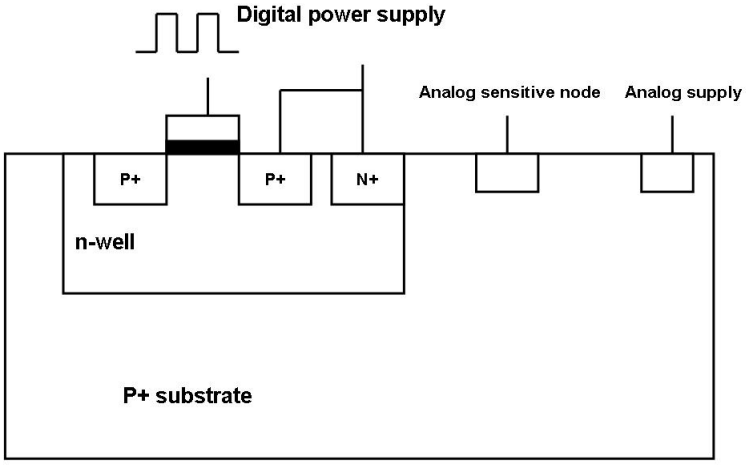


Figure 2.5: Substrate noise coupling

Several substrate noise modeling methods have been developed during the past decade such as the finite difference mesh method and the boundary element method. [26] [27] Although these approaches generate accurate results in theory, it requires detailed process and layout information such as sheet resistivity and

doping density across substrate. In most cases, such information is only available after the circuit design method has been established and the layout is completed. Long computation time is needed to set up substrate coupling models to achieve the accuracy needed for high precision design. Several critical decisions we have to make for the design.

1. Digital algorithm/structure selection based on trade off between die area, power consumption, reusability etc.

2. Analog topology selection based on trade off between performance, power consumption, die area etc.

3. Package pin layout selection based on on-chip noise coupling, ESD, circuit board noise immunity etc.

4. Floor plan based on noise immunity, reusability, layout time etc.

A new simple substrate noise estimation method is needed to guide the design and layout of the high precision mixed signal design design.

2.3.3 Major Nyquist analog to digital converter topology overview

Flash ADC

Flash ADC is one of the most widely used analog to digital converters [3] [4] [5]. Its main advantage is low latency since flash ADC is able to generate digital output with one operation clock cycle. Low latency makes the converter suitable for high speed applications. A typical flash ADC block diagram is shown in Figure 2.6. Comparators are used to compare the input with various reference levels.However, each additional bit of resolution doubles the power consumption and die area and

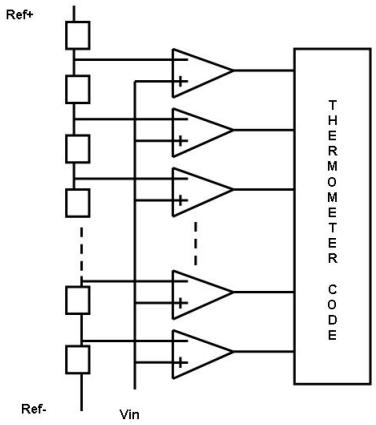


Figure 2.6: Flash ADC architecture

the topology is also very sensitive to comparator offset. The comparator offset has to be less than half LSB for high precision design. Flash ADC is normally employed for applications which requires 8 to 10 bit resolutions.

Pipeline ADC

In pipeline topology [3] [6] [7], each downstream ADC only needs to processes the "residual" voltage from the previous stage. This approach significantly reduces the overall power consumptions. The major advantage of pipeline topology is the comparators in its downstream stages are much less sensitive to offset. The major resolution limitation of the pipeline topology is the gain mismatch between each sub-ADC. Special process is normally required to achieve high resolution by this topology. Since the input signal has to go through multiple stages, the latency is much larger than flash ADC. A typical pipeline ADC is shown in Figure 2.7.

Pipeline ADC is able to achieve 8 to 16 bit resolution over a 125MHz to 1GHz bandwidth.

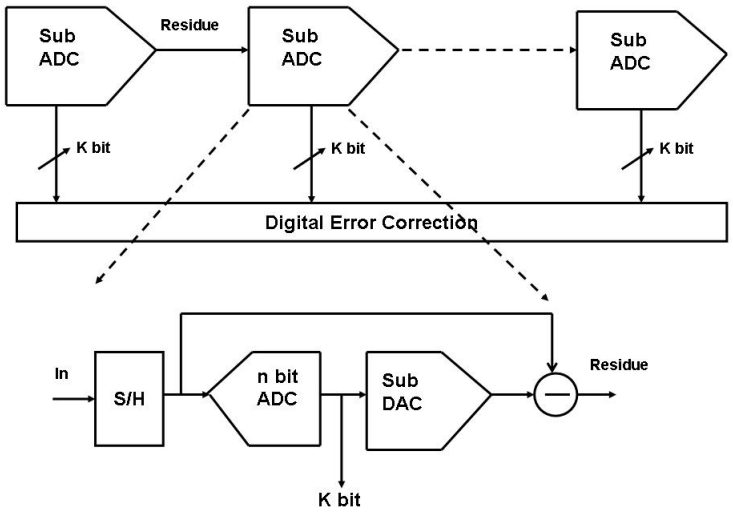


Figure 2.7: Pipeline ADC architecture

Successive approximate ADC (SAR ADC)

A successive approximate ADC [8] [9] is composed of only one stage, which offers significant power consumption and die area advantages over other topologies. A typical successive approximate ADC architecture is shown in Figure 2.8. A digital to analog converter (DAC) is introduced to generate analog signal from its output. This internal analog signal is subtracted from input signal to produce the "residual" voltage for the next operation, which is similar to that of a typical pipeline ADC. Therefore, at least clock cycle is required for each bit of resolution, which limits successive approximate ADC to relatively low speed applications. Since SAR ADC avoids stage to stage mismatch, this converter can achieve over 18 bit resolution in high quality analog process.

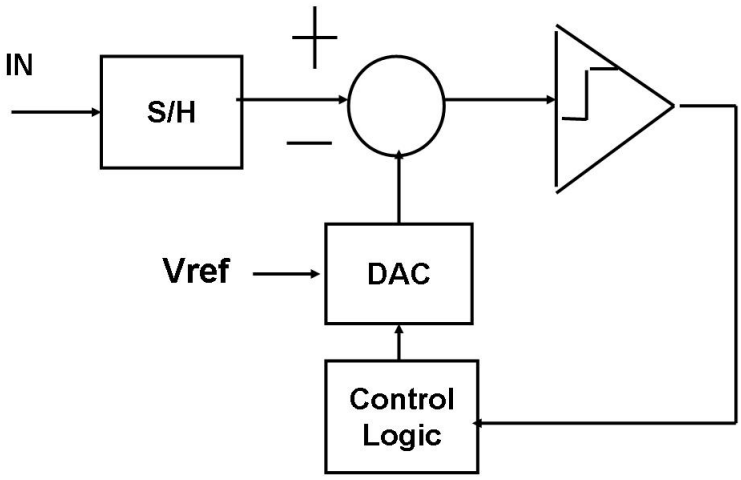


Figure 2.8: SAR ADC architecture

Chapter 3

Delta Sigma Converter Topology Overview

As shown in the previous chapter, total quantization energy is $\frac{\Delta^2}{12}$. One common approach to relax design requirements for high precision design is to increase the sampling frequency to much higher frequency than the Nyquist criterion, which is twice the input signal frequency. For simplicity, we continue to assume quantization noise is white noise.

As shown in Figure 3.1, we only have to deal with the quantization noise left inside the signal bandwidth, which is the portion of $\frac{f_{sig}}{\frac{f_s}{2}}$, where f_{sig} is the signal frequency and f_s is the sampling frequency. Normally, each doubling of sampling frequency improves signal to noise ratio by 3dB. Oversampling ratio (OSR) is normally referred to as the ratio between the oversampling frequency and the Nyquist frequency.

The oversampling delta sigma topology is introduced to further suppress the quantization noise within the signal band. As shown in Figure 3.2, the delta sigma

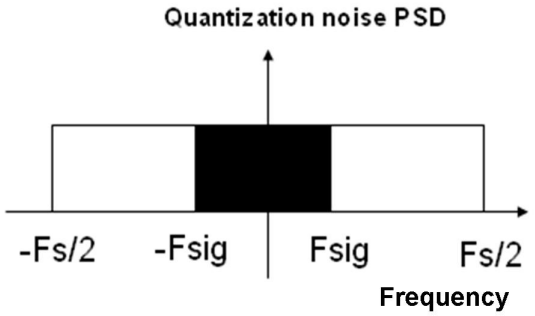


Figure 3.1: Oversampling concept

modulator is consisted of an integrator, a quantizer and a negative feedback path formed by a Digital-to-Analog (DAC) converter. For simplicity, the quantization noise is assumed to be white noise and the DAC is assumed to be ideal. The modulator can be considered as a linear system under above assumptions. The signal transfer function STF(z) and the noise transfer function NTF(z) can be derived as

$$NTF(z) = \frac{H(z)}{1 + H(z)} \tag{3.1}$$

$$STF(z) = \frac{1}{1 + H(z)} \tag{3.2}$$

The delta sigma modulator output is the summation of Equation 3.1 and Equation 3.2.

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot Q(z) \tag{3.3}$$

By selecting a loop filter as $H(z) = \frac{1}{1-z^{-1}}$ and insert it to Equation 3.1 and 3.2, the signal transfer function and noise transfer function for L-th order modulator is

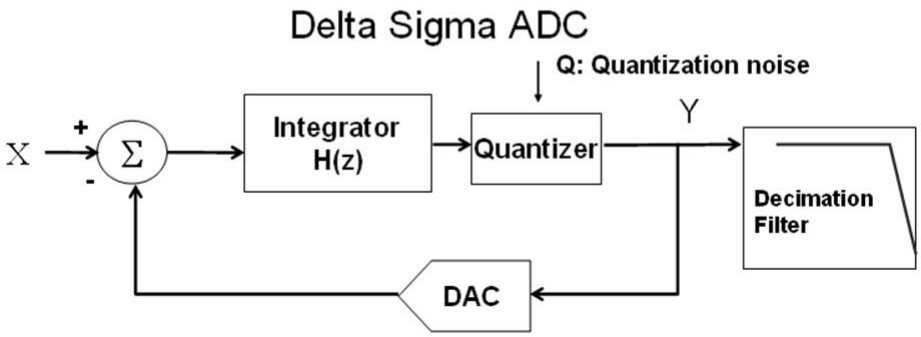


Figure 3.2: Delta sigma modulator architecture

shown as:

$$NTF(z) = \frac{H(z)}{1 + H(z)} = z^{-L} \tag{3.4}$$

$$STF(z) = \frac{1}{1 + H(z)} = (1 - z^{-1})^{L} \tag{3.5}$$

The L-th delta sigma modulator output is

$$Y(z) = X(z) \cdot z^{-L} + Q(z) \cdot (1 - z^{-1})^{L} \tag{3.6}$$

The output includes the delayed version of the input signal. The delta sigma modulator suppresses quantization noise within signal band and moves the noise energy to

higher frequency, which will be filtered out by the following digital decimation filter. Such operation is also referred as noise shaping. Using z domain transformation $z = e^{j2\pi f}$, the integrated quantization energy over signal band can be calculated as

$$P_{noise} = \int_{f_{-sig}}^{f_{sig}} \frac{\Delta^2}{12} NTF^2 df \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \tag{3.7}$$

The converter dynamic range when only the quantization noise is taken into consideration can be shown as:

$$DR_(Q) \approx \frac{3}{2} \frac{2L+1}{\pi^{2L}} OSR^{2L+1} (2^{N_{quan}} - 1)^2 \tag{3.8}$$

where N_{quan} is the internal quantizer resolution.

It is easy to observer from Equation 3.8 that the noise shaping of quantization bases on multiple factors which include order of the modulator, oversampling ratio(OSR) and the internal quantizer resolution. Even for first order modulator, each doubling of the oversampling frequency improves the dynamic range by 9dB, while non noise shaped oversampling topologies improve the dynamic range by only 3dB. Multiple disadvantages are associated with increasing the oversampling ratio. First, increasing the oversampling ratio moves the quantization noise to higher frequency which degrades modulator stability. Second, higher oversampling ratio also increases power consumptions as well. On the other hand, each additional bit of resolution for the internal quantizer also improves the dynamic range by 6dB. This is one of the major reason multibit delta sigma topology is widely adopted recently to achieve high performance and power efficient at the same time.

3.1 Delta sigma loop filter topologies

Loop topology is another important factor for modulator design. Normally, a loop filter has high gain within the band of interest to attenuate quantization noise. Figure 3.3 shows a fifth order distributed feedback filter architecture. It places negative feedback around each integrator. The quantization noise transfer function is:

$$NTF(z) = \frac{(z-1)^5}{(z-1)^5 + a5(z-1)^4 + a4(z-1)^3 + a3(z-1)^2 + a2(z-1) + a1} \tag{3.9}$$

All zeros are placed in DC. A high pass filter such as butterworth filter can be used to implement the poles. As shown in Equation 3.1 and 3.2, noise transfer function and signal transfer function normally share the same poles. The signal transfer function is a low pass filter with butterworth poles for distributed feedback architecture, which helps to filter out out-of-band energy to improve modulator stability.

An alternative feedforward filter topology is shown in Figure 3.4. The output of each integrator is weighted and then summed together to feed to the input of the internal quantizer. The noise transfer function is the same as Equation 3.9

By adding additional negative feedback around integrators, the zeros in the noise transfer function can be moved away from DC to add additional attenuation to in-band quantization noise. The feedforward modulator with local resonator is shown in Figure 3.5.

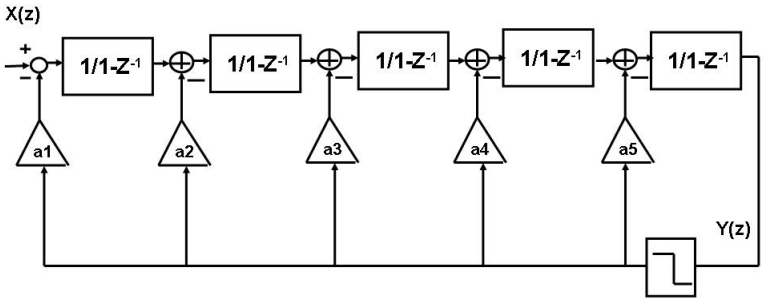


Figure 3.3: 5th order distributed feedback delta sigma modulator

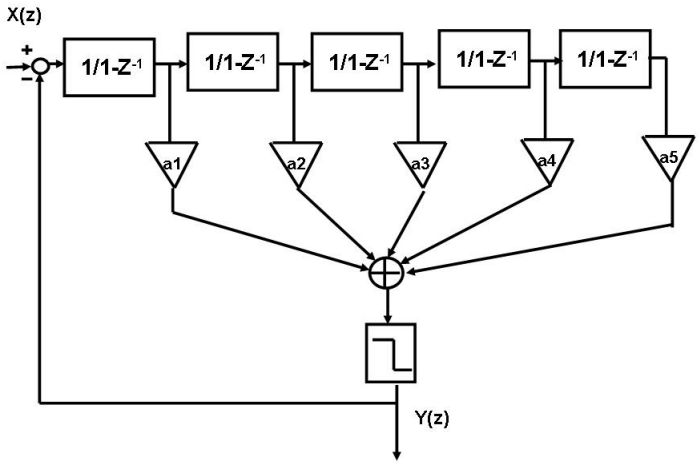


Figure 3.4: Feedforward summation topology

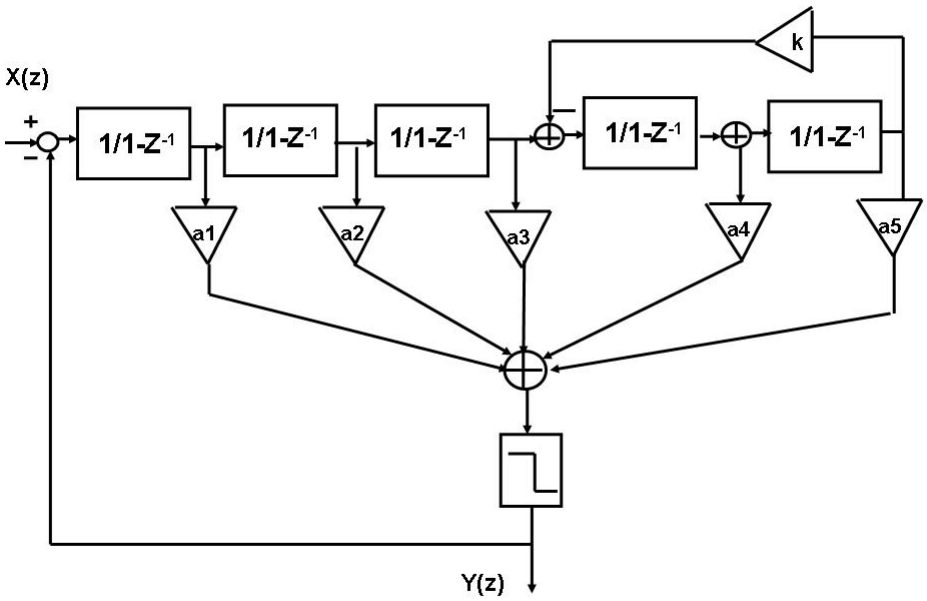


Figure 3.5: Feedforward modulator with local resonate

3.2 Cascaded delta sigma modulator

Cascaded delta sigma architecture is another approach to improve stability for high order modulator design. As shown in Figure 3.6, quantization noise generated in the first stage is further processed in the second stage. Outputs from each stages are further weighted by the noise cancellation logic circuit based on the prediction of integrator gain of previous stages. All outputs are summed in the digital domain to cancel most quantization noises. Ideally, only the quantization noise of the last stage is left in the final output. As an example, we consider a second order modulator to illustrate the operation. Now, we assume first order integrator filter, $H(z) = \frac{1}{1-z^{-1}}$.

$$Y_1 = X(z) + (1 - z^{-1})Q_1 \tag{3.10}$$

$$Y_2 = -Q_1 + (1 - z^{-1})Q_2 \tag{3.11}$$

Y_2 is further processed by noise cancellation logic, $1 - z^{-1}$. The final output is

$$Y = Y_1+(1-z^{-1})Y(2) = X(z)+(1-z^{-1})Q_1-Q_1(1-z^{-1})+(1-z^{-1})^2Q_2 = X+(1-z^{-1})^2Q_2 \tag{3.12}$$

The quantization noise from the first modulator is completely suppressed and this architecture achieves second order noise shaping with first order modulator in each stage. This topology can be further extended to achieve high order noise shaping while using low order modulator in each stage to achieve excellent stability. For multibit cascade scheme,the feedback digital to analog converter (DAC) non-

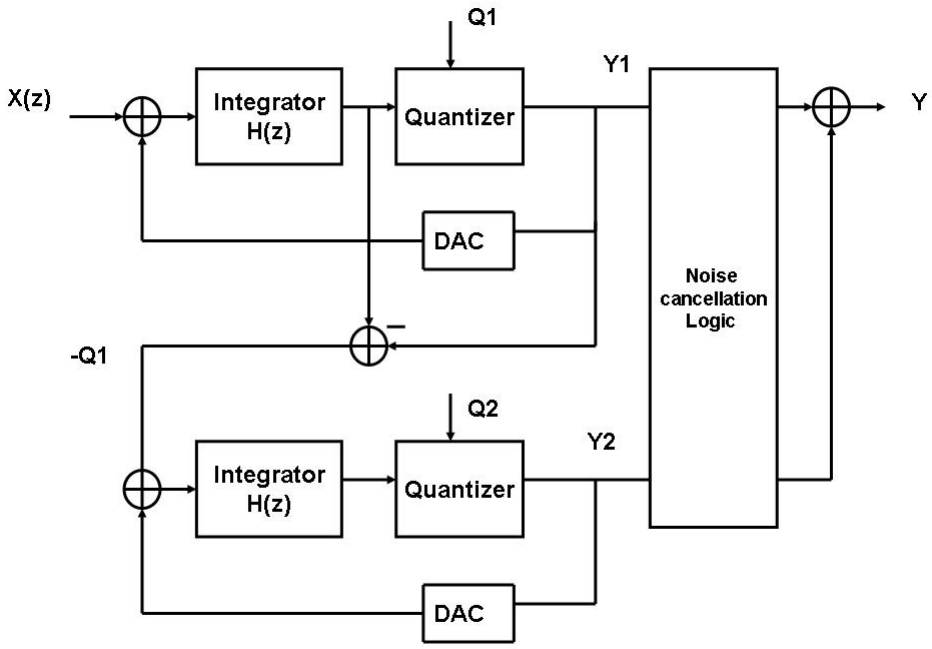


Figure 3.6: Cascade delta sigma architecture

linearity is suppressed by the noise cancellation logic that processes the outputs of multiple quantizer in the cascade. Also, the feedback DAC of downstream stages doesn't contribute thermal noise directly to the input sampling capacitors. These facts greatly reduce the dynamic element matching (DEM) logic complexities and overall die area required for the feedback DAC. The major shortcoming of this approach can be easily observed from this example as well. The noise cancellation is not perfect in the actual circuit design. Part of the quantization noise from the first stage can leak to the final output due to this effect,which may create performance limitations for high precision design.

3.3 Discrete and continuous time delta sigma modulator design

The delta sigma modulator can be designed as a discrete time data sampling system or as a continuous time circuit. As shown in Figure 3.7, the discrete time sigma delta normally adopts switched capacitor integrators and the continuous time systems use RC integrator. Since the coefficient of a switched capacitor integrator depends the ratio of two capacitors, the integrator operation is not only more accurate but also more insensitive to process variations. For a continuous time integrator, its coefficient is associated with the resistor and capacitors. Its accuracy depends on the absolute value of resistor and capacitors, which makes it very difficult to improve the converter performance. On the other hand, the speed of a switched capacitor integrator is limited by the bandwidth of its opamp while the opamp inside continuous time delta sigma modulator doesn't have to settle to full accuracy during each clock period. Therefore, a continuous time delta sigma modulator is widely used in low to medium performance, high speed applications.

3.4 Stability

For simplicity, the internal quantizer gain is normally assumed to be constant. However, the quantizer gain varies during operation since the output is a step function for both the signal bit and multibit architecture. Conventional transfer function pole analysis is not sufficient to guarantee the modulator stability. Normally, extensive time domain simulation is also needed. [20] For high precision design, a high order modulator is often used to suppress the quantization noise within the signal band. It is difficult to achieve excellent stability for single loop high order architecture due

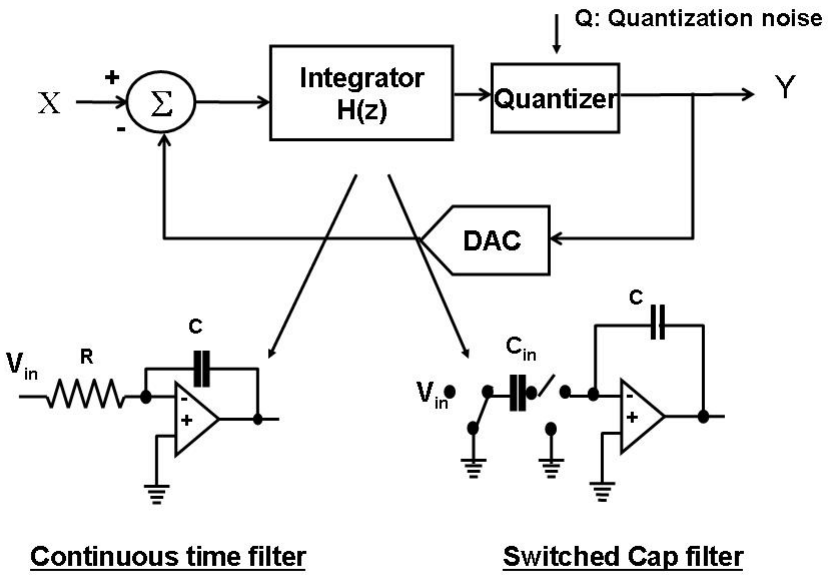


Figure 3.7: Continuous time and discrete time delta sigma modulator

to high level of out of band high frequency quantization noise energy. In real world applications, a high frequency signal can leak to the converter input directly and cause the modulator to become unstable. In general, the whole modulator has to be reset to get out of the unstable condition. The converter is unable to process the input signal during this reset process, which results in data loss. The new generation converter not only has to achieve excellent stability but also has to be able to recover from unstable condition quickly to minimize the data loss.

3.5 Tones and dithers

For simplicity, we assume quantization noise as white noise so far. However, in reality, the delta sigma quantization noise spectrum contains signal like components which are commonly referred to as tones. Tones exist even for low level input signals, which is problematic for applications such as audio or high precision measurement applications. Tones are normally caused by the correlation between the input signal and the quantization noise. Therefore, tones vary with the input signal magnitude and frequency in most cases. One method to break such correlation is to add a random signal directly to the input of the internal quantizer. Such random signal is commonly referred as dither signal. Although the dither signal can break tones, it also adds noise to the converter. The magnitude of the dither signal has to be kept as minimum. Beside the dither signal, adopting a high order modulator or multibit internal quantizer also significantly weakens the correlation between the input signal and the quantization noise.

3.6 Sub circuit design parameter analysis

3.6.1 Finite opamp DC gain

Finite opamp dc gain allows internal quantization noise leaks back to the input, which introduces additional noise into the converter.

$$H(z) = \frac{z^{-1}}{1-(1-\varepsilon)z^{-1}} \tag{3.13}$$

where ε represents the error introduced by the opamp finite DC gain. For first order delta sigma modulator, the noise transfer function becomes

$$NTF = \frac{1-(1-\varepsilon)z^{-1}}{1+\varepsilon z^{-1}} \approx (1-z^{-1}) + \varepsilon z^{-1} \tag{3.14}$$

The first term on the right side of Equation 3.14 is the first order noise shaping function. The second term is the error introduced by the finite opamp DC gain. The integrated noise over signal band is

$$P_{noise} = \int_{f_{-sig}}^{f_{sig}} \frac{\Delta^2}{12} NTF^2 df \approx \frac{\Delta^2}{12}\left(\frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} + \frac{\varepsilon^2}{OSR}\right) \tag{3.15}$$

Compared with Equation 3.7, the second term on the right side of Equation 3.15 is the error introduced by the opamp finite DC gain. The additional noise power is proportional to the quantization noise energy inside the loop. [17] [18] For single loop architecture, the quantization noise leakages from down stream integrators are suppressed by the gain of first integrator, while each stage contributes quantization noise leakages in a cascade delta sigma modulator due to stage to stage mismatch. For a high precision converter design, the integrator normally has to adopt high DC

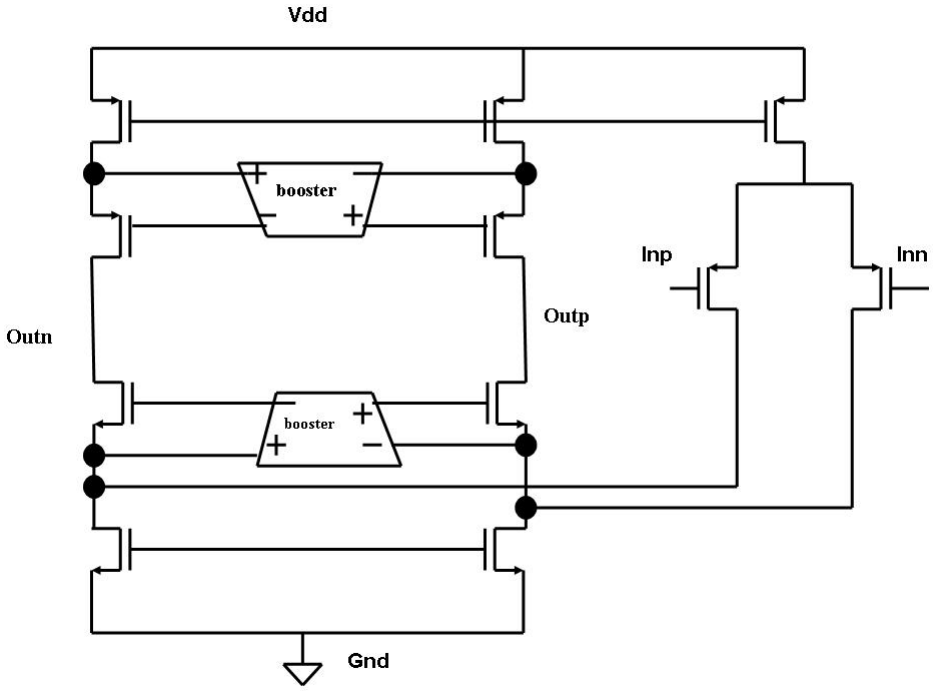


Figure 3.8: Opamp with gain boosting stages

gain opamp with gain boosting scheme, which becomes a bottleneck to lower the die cost and power consumption of the design. A typical folded cascode opamp with gain boosting is shown in Figure 3.8.

3.6.2 Opamp settling & Slew analysis

A typical switched capacitor first integrator is shown in Figure 3.9. Phase one and phase two are two non overlapping clocks. C_{in} is the sampling capacitor and C_{int} is the integration capacitor.

Phase two is normally referred to as the integration phase when the charge from the sampling capacitor is transferred to the integration capacitor. The phase one is normally referred as the holding phase when the integrator output voltage

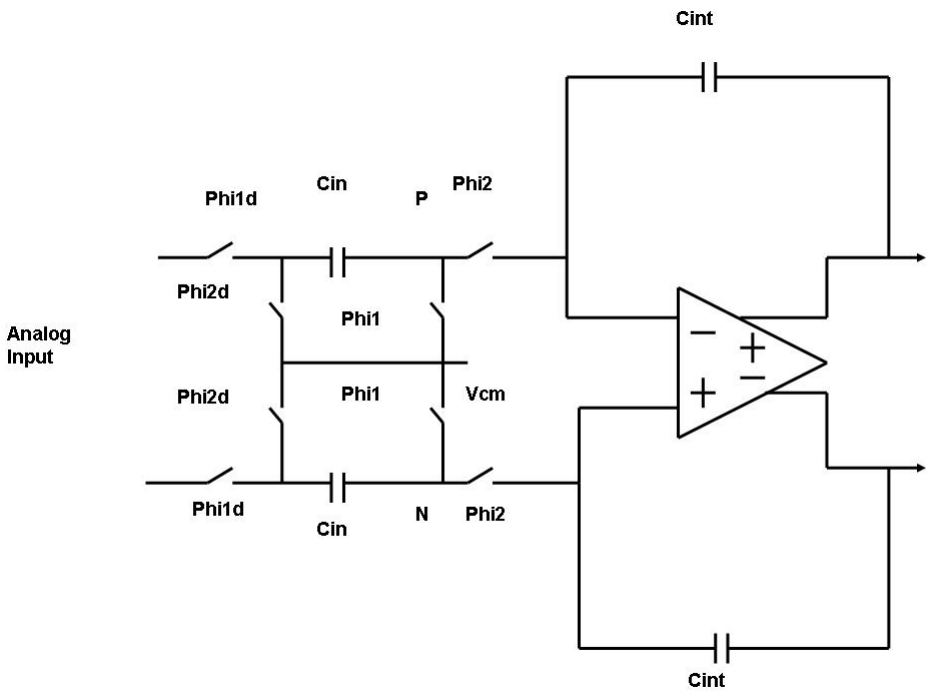


Figure 3.9: Switched capacitor first integrator

is hold from previous clock phase. As integrator switches between these two clock phases, the opamp has to be able to settle the glitches in both phases. The settling requirement of the opamp is determine by the more stringent value between these two cases. The integrator settling error can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{C_{in}}{C_{int}} \frac{z^{-1}}{1 - z^{-1}} (1 - \varepsilon_s) \tag{3.16}$$

where ε_s is the settling error. In order to achieve N bit accuracy, the settling error has to satisfy the following expression.

$$\varepsilon_s < \frac{1}{2^{N+1}} \tag{3.17}$$

The switched capacitor network can also lead to gain error. The settling error of the switched capacitor network is

$$\frac{V_{out}}{V_{in}} = \frac{C_{in}}{C_{int}} \cdot \frac{z^{-1}}{1 - z^{-1}} (1 - e^{-\frac{T_s}{R_{on} \cdot C_{in}}}) \tag{3.18}$$

where T_s is the settling time period and R_{on} is the MOS switch resistance when the switch is turned on.

The slew requirement is defined by the maximum integrator output voltage step and the slew time period.

$$SR = \frac{\Delta V_{step}}{\Delta t} = \frac{I}{C_{load}} \tag{3.19}$$

where ΔV_{step} is the maximum integrator output step, $Deltat$ is the time period, I is the bias current and C_{load} is the load capacitor, which is mostly the bottom plate parasitic capacitor of the integration capacitor. In summary, opamp bias current and sampling switch sizes have to be increased to improve converter performance,

which makes it very difficult to design a high performance converter with low power consumption and small die area.

3.6.3 Opamp noise

Opamp inside internal integrator and reference buffer etc. introduces noise into converter. The noise sources generally consist of thermal noise and flicker noise. For MOS transistor in strong inversion region, the input referred thermal noise density is modeled as

$$v^2_{noise,thermal} = \frac{8kT}{3g_m}\Delta f \tag{3.20}$$

The flicker noise can modeled as

$$v^2_{noise,flicker} = \frac{k}{C_{ox}WL \cdot f}\Delta f \tag{3.21}$$

where k and C_{ox} are process dependant parameters. The flicker noise becomes the dominate noise source as the signal band approaches DC. In general,modulator quantization noise and opamp noise are independent of each other. Each noise source can be studied separately and summed together to calculate the total noise power.

3.6.4 Switched capacitor input sampling network design

Charge injection from the switched capacitor input sampling network tends to degrade the performance of the input anti-alias filter, which limits the achievable performance of the converter. A two-phase, rough and fine topology has been reported, [39]which is able to suppress the charge injection error. The circuit diagram

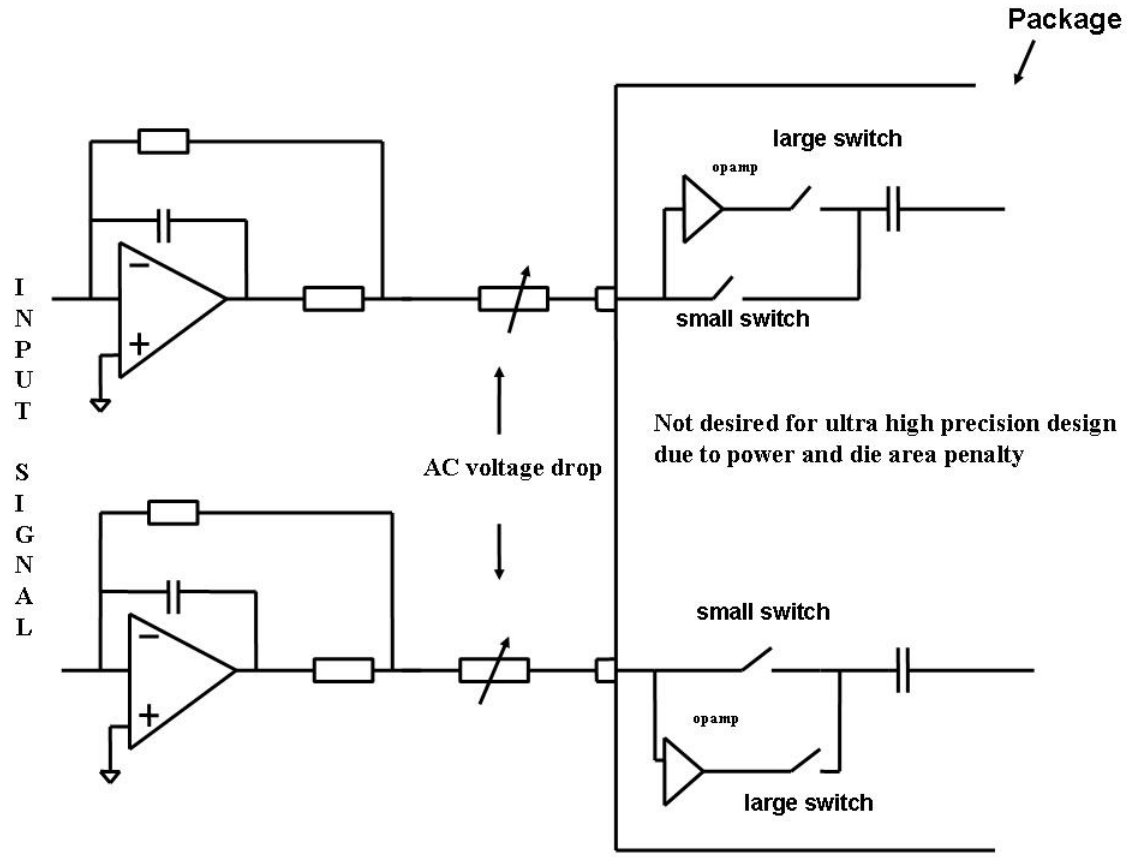


Figure 3.10: Rough and fine input sampling stage

is shown in Figure 3.10.

A pre-charge opamp is introduced for each input to bring the node closely to its final value during the rough phase. The front buffer only needs to provide remaining charges to bring the sampling capacitor to its final value. This scheme relaxes the requirement for the front buffer. However, since the topology requires an additional rough phase opamp to pre-charge the sampling capacitor, the power consumption and die area penalty increases substantially for higher performance designs.

3.6.5 Comparator design

Since the delta sigma modulator is a feedback system, the internal quantizer and comparators have to generate their outputs and feedback them to the first integrator within one clock cycle, or the delta sigma modulator stability will begin to degrade. Therefore, the internal quantization and comparators must have very low latency. Therefore, a high speed comparator is normally adopted for signal bit topology, while flash ADC type quantizer is used for multibit topology. For continuous normal operation, the internal ADC and comparators have to be memoryless from previous clock cycles. Comparators are normally reset after each operation.

3.6.6 State of art converter topology comparison

The current analog to digital converter performance versus signal bandwidth plot is shown in Figure 3.11.

Different converter topologies are selected for different resolution and input signal bandwidth. Delta sigma topology is widely used for baseband high precision applications due to its ability to relax design requirements for sub analog circuits and fabrication process.

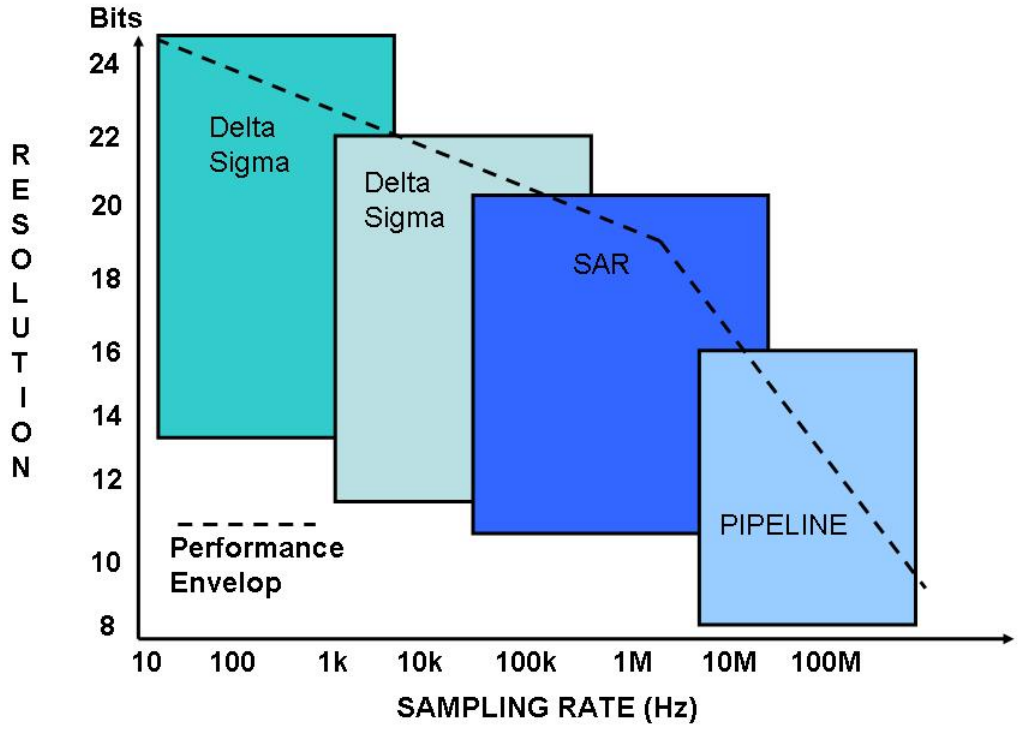


Figure 3.11: Analog to Digital Converter Comparison

Chapter 4

System Aspects of High Precision Analog to Digital Converter Design

High precision applications have continued to improve their performance and efficiency due to the rapid advance and availability of high-precision data acquisition technology as well as digital signal processing (DSP) technologies. These applications are also rapidly migrating into USB-powered devices and portable device, placing increasing stringent demands on the power efficiency and performance of high precision analog to digital conversion design. Furthermore, as the new generations of high end systems enter the consumer market, there are also increasing demands to reduce the overall system level cost.

4.1 System level view of switched capacitor input sampling stage design

On typical modern day multi channel high precision data acquisition circuit board, all on chip components are placed closely to each other to save circuit board space. Adding either heat sink or fan will substantially increase the system level cost. This trend places more stringent requirements on high precision converters to realize their performance in such environment. A switched capacitor ADC input is measured in this environment to further illustrate the challenges.

As discussed in the previous chapter, charge injections from the switched capacitor input stage rattles the front opamp and introduces nonlinearity to the signals being sampled by the converter. For lower level input signals, the front opamp can settle the charge injection "kick" well and introduce less nonlinearity. As shown in Figure 4.1 (a) to (c), most nonlinearity harmonics disappears as input signal magnitude reduces from -60dBFs to -100dBFs with on board digital signal processing(DSP) circuits are in operational mode. However, one large harmonic still remains in the signal band with -80dBFs input signal. The magnitude of this harmonic remains almost the same as as input signal level decreases. As shown in (e), this harmonic continues to exit even the converter is stopped. The harmonic only disappears after the on board DSP is shut down. These measurement plots indicate harmonics shown in (a) & (b) are generated from multiple sources. One first source is from the charge injections from the switched capacitor input stage, the second source is from the noise coupling from on board DSP circuits, the third source is the intermodulation components of previous two sources. For multichannel design, noise coupling also occurs on the circuit board. A commonly used anti aliasing buffer is shown in Figure 4.2. The capacitor C_{cm} is added to be used as charge

reserve to mitigate the charge injection issue. This capacitor also form a single pole anti aliasing filter. During each sampling phase, the internal sampling capacitor is connected to the front buffer to be charged up. The sampling capacitor and its switches can be viewed as an equivalent resistor.

$$R_{eq} = \frac{1}{f \cdot C_s} \tag{4.1}$$

where R_{eq} is the equivalent resistance of the input sampling network, C_s is the sampling capacitor and f is converter sampling frequency. As the oversampling ratio and frequency are increased to suppress more quantization noise, the sampling capacitor size is increase to lower thermal noise for high precision converter design. On the other hand, the sampling switch size also increases to achieve targeted RC time constant, which generates more charge injections during the sampling operation. This requires the front buffer to settle large transient current at high frequency. Unfortunately, most existing amplifiers are unable to provide such current, which introduces excessive nonlinearity into the converter sampling stages. Specially designed high performance amplifiers not only increase overall system level cost but also normally consumes much more power. A converter input sampling stage design which relaxes the performance requirements of the front anti alias buffer is an important step to achieve the performance, cost and power consumption target. Although the front anti alias filter filtered out high frequency energy in theory, high frequency energy leaks to converter input during real world applications, especially when all discrete components are placed closely to each other. The converter modulator has to have excellent stability to recover from the high frequency input and to return to normal operation.

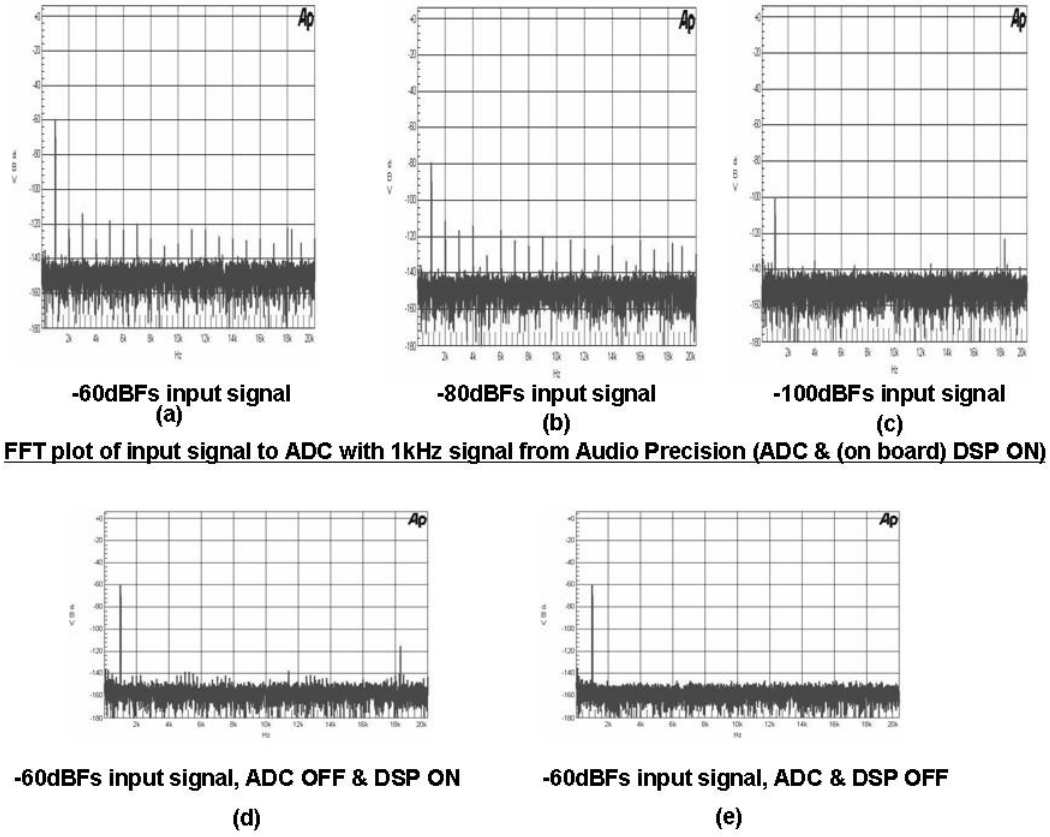


Figure 4.1: Switched capacitor ADC input measurement plots

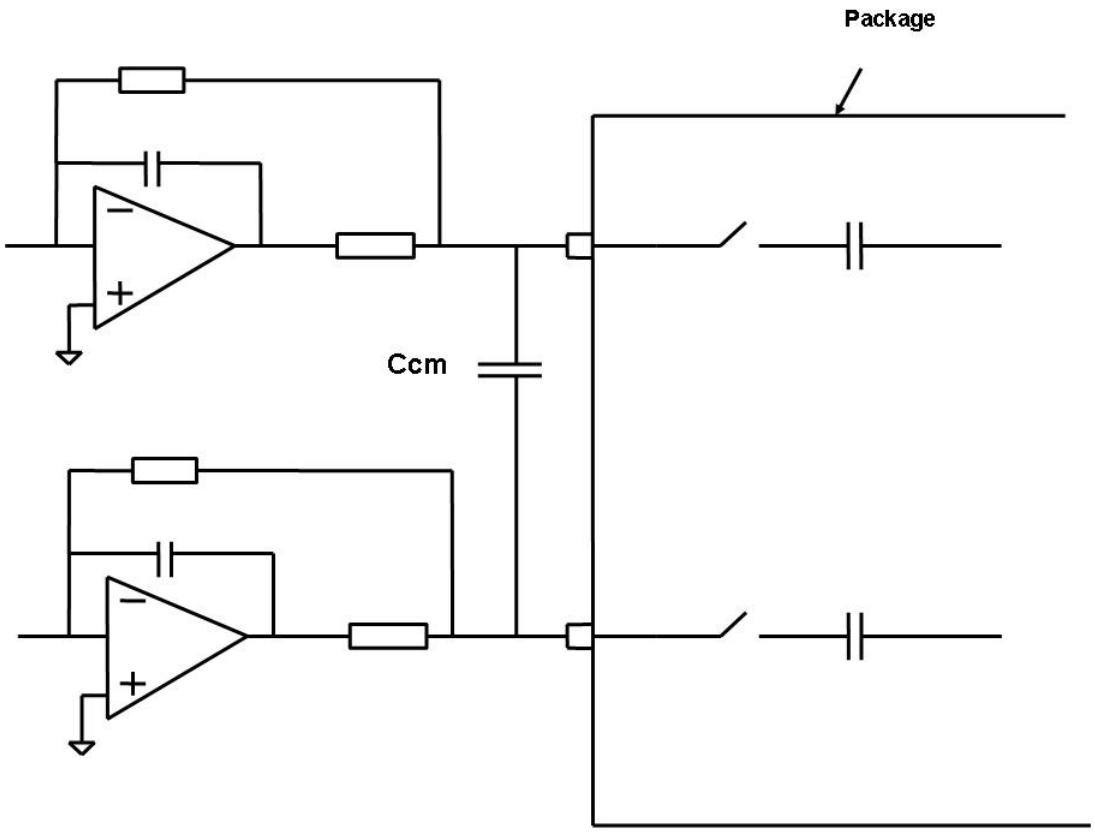


Figure 4.2: Delta sigma analog-to-digital converter anti aliasing buffer

4.2 System level view of converter design parameters

Although it is possible to design digital filters and converter reference circuits on a separate die to suppress internal noise coupling and to reach performance target, it is important to design a single die high precision converter with a high degree of integration to reduce the die and circuit board cost.

It is easy to observe from Equation 2.3 that adopting a larger input signal magnitude improves the converter signal-to-noise ratio. However, large input signal normally increases internal integrator output swings, which degrades modulator stability and increases power consumptions. A single ended, single sampled switched capacitor integrator with feedback reference path is shown in Figure 4.3.

The converter kT/C noise is defined as

$$\frac{kT}{C} = \frac{kT}{C_{in}} \cdot (1 + \frac{C_{fb}}{C_{in}}) \cdot \frac{f_{sig}}{\frac{f_s}{2}} \tag{4.2}$$

C_{in}: input sampling capacitor, C_{fb}: feedback DAC capacitor, f_s: sampling frequency.

The ratio of C_{fb} and C_{in} is limited by the modulation index, MI.

$$MI = \frac{V_{in} \cdot C_{in}}{V_{ref} \cdot C_{fb}} \tag{4.3}$$

V_{in}: input signal magnitude, V_{ref}: reference voltage magnitude

Insert Equation 4.3 into Equation 4.2

$$\frac{kT}{C} = \frac{kT}{C_{in}} \cdot (1 + \frac{V_{in}}{MI * V_{ref}}) \cdot \frac{f_{sig}}{\frac{f_s}{2}} \tag{4.4}$$

Equation 4.4 indicates that, for a given input signal, a high modulation index and large reference voltage minimizes the kT/C noise contribution from the feedback

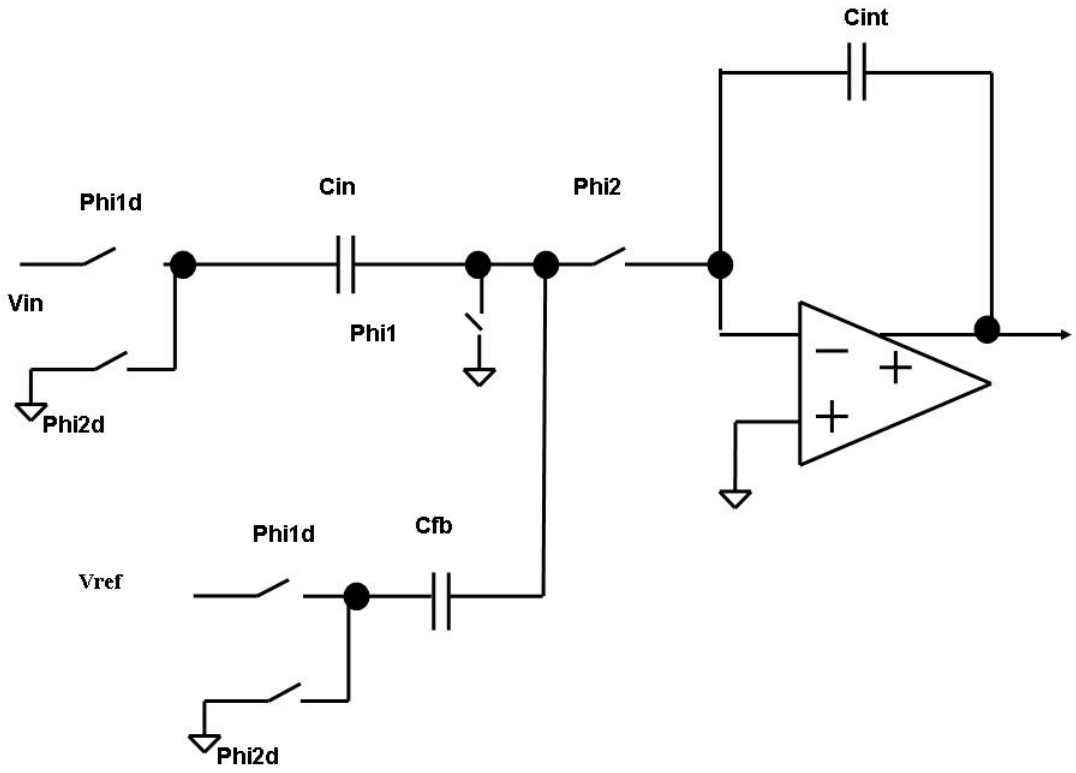


Figure 4.3: A single ended switched capacitor Integrator 1 and feedback path circuit diagram

DAC capacitors, thus reducing the input sampling capacitor size for a given design target.

Opamp is another major contributor. The input referred opamp noise is sampled by both the input and integration capacitor. The converter input referred opamp noise is

$$N_{op_{in}}^2 \cdot (C_{int} + C_{in})^2 = C_{in}^2 \cdot N_{nop}^2 \tag{4.5}$$

$$N_{nop}^2 = N_{op_{in}}^2 \frac{(C_{in} + C_{int})^2}{C_{in}^2} \tag{4.6}$$

where $N_{op_{in}}$ is the input referred opamp noise which includes both the thermal and flicker noise. The N_{nop} is the converter input referred opamp noise.

The opamp noise is also limited by the switched capacitor network. Assume the unity gain bandwidth of the switched capacitor network is f_o. Bandlimited converter input referred noise is

$$N_{nop_{bi}}^2 = N_{op_{in}}^2 \frac{(C_{in} + C_{int})^2}{C_{in}^2} \cdot \int_0^\infty \frac{1}{(1 + \frac{f}{f_0})^2} df \tag{4.7}$$

By using

$$\tan^2 \theta + 1 = \frac{1}{\cos^2 \theta} \tag{4.8}$$

$$N_{nop_{bi}}^2 \approx N_{nop}^2 f_o \frac{\pi}{2} \tag{4.9}$$

where $N_{nop_{bi}}$ is the bandlimited converter input referred opamp noise.

$$N_{nop_{bi}}^2 \approx N_{op_{in}}^2 \frac{(C_{in}+C_{int})^2}{C_{in}^2} f_o \frac{\pi}{2} \tag{4.10}$$

This noise is aliased back to signal band.

$$N_{nop_{bi}}^2 \approx N_{op_{in}}^2 \frac{(C_{in}+C_{int})^2}{C_{in}^2} f_o \frac{\pi}{2} \frac{f_{sig}}{\frac{f_s}{2}} \tag{4.11}$$

$$N_{nop_{bi}}^2 \approx N_{op_{in}}^2 (1+\frac{1}{\frac{C_{in}}{C_{int}}})^2 \frac{\pi f_o f_{sig}}{f_s} \tag{4.12}$$

Equation 4.12 indicates that converter input referred opamp noise is attenuated by the integrator 1 coefficient, $\frac{C_{in}}{C_{int}}$. However, large integrator coefficient generally results in large output swings, which introduce distortion and increase power consumption. Down stream integrators and their internal opamps also contribute noise to the converter. The converter referred noise energy is attenuated by the total gain of previous stages. Normally, noise contrition after the third integrator is negligible.

The reference circuit also contribute thermal and flicker noise. Its converter input referred noise can be expressed as

$$N_{ref_{in}}^2 = N_{ref}^2 (\frac{C_{fb}}{C_{in}})^2 \tag{4.13}$$

where $N_{ref_{in}}$ is the converter input referred noise from reference circuit, N_{ref} is reference circuit noise.

Insert equation 4.3 into equation 4.13

$$N_{ref_{in}}^2 = N_{ref}^2 (\frac{V_{in}}{MI \cdot V_{ref}})^2 \tag{4.14}$$

Equation 4.14 again indicates a large reference voltage and stable modulator with large modulation index can reduce the noise contribution from the reference path. Similar calculation can be calculated for the input referred noise from down stream integrators to demonstrate that the down stream integrator noise energies are attenuated by the front integrator gain. [37] For the second integrator, its noise energy is attenuated by first integrator transfer function $\frac{C_{in}}{C_{int}}\frac{z^{-1}}{1-z^{-1}}$.

The input referred noise from down stream integrators are expressed as:

$$N_{dsin}^2 = \frac{\pi^2}{3a_1^2(OSR)^3}N_{ds2}^2 + \frac{\pi^4}{5a_1^2a_2^2(OSR)^5}N_{ds3}^2 + \cdot\cdot \tag{4.15}$$

where N_{dsin} is the input referred down stream integrator noise, N_{ds2} is the second integrator noise , N_{ds3} is the third integrator noise, $a_1\&a_2$ is the first and second integrator gain and OSR is the oversampling ratio. As shown in equation 4.15, down stream integrator noise are suppressed by the oversampling topology. Normally, only the noise contribution from the second and third integrator is considered. Beside the oversampling ratio, increasing first and second integrator gain will also help to attenuate the noise contribution from down stream integrators.

On the other hand, the chip is placed in package and signals and power lines are connected to package pins, front buffer and supplies through bond wires and on board metal traces. As shown in Figure 4.4, signal dependant currents generate signal dependant voltages which further degrade sampled input signal and converter power supplies. For multichannel systems, since all converters share common power supply and analog ground, signal dependent supply and ground current will cause very serious inter-channel interference. Also shown in Figure 4.4, the layout of a conventional single die high performance switched capacitor converter is dominated by the large capacitor inside the first integrator and feedback digital to analog con-

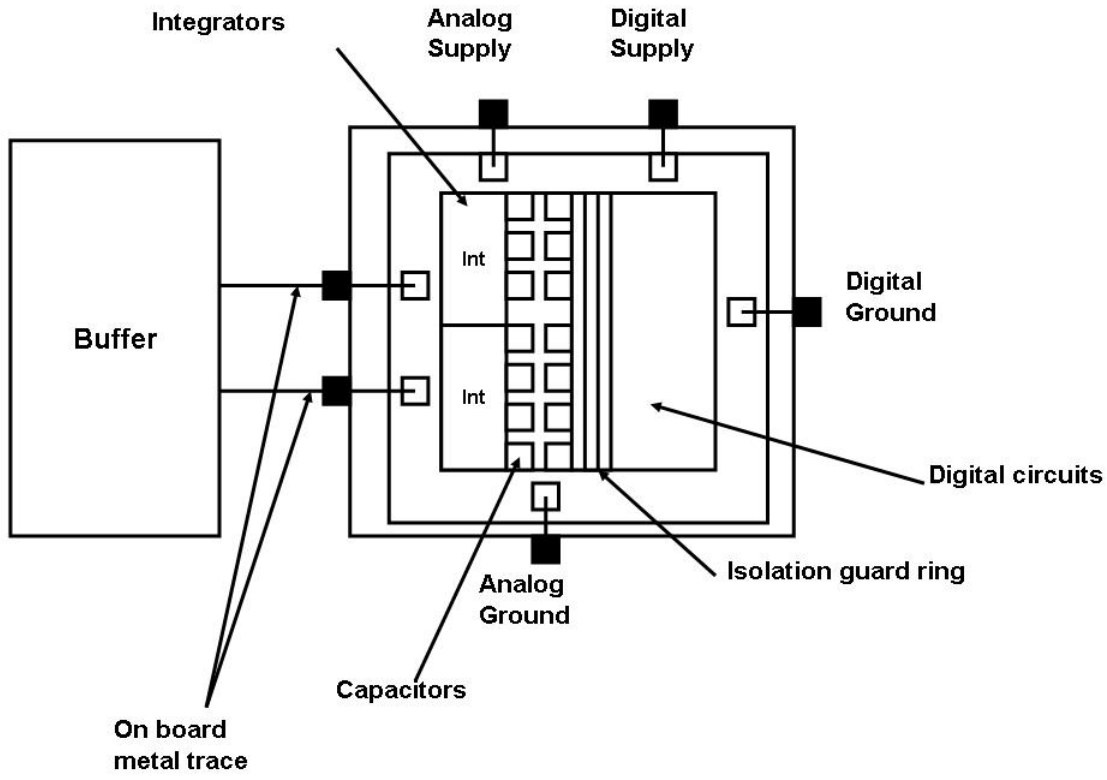


Figure 4.4: Package & layout aspect of high precision converter design

verter(DAC). Large isolation guard ring is needed to minimize the effect of digital coupling noise. These factors become the major bottlenecks to suppress the converter die cost.

Thermal effects such as transistor self heating are also able to seriously affect the high performance converter design. Self heat generated inside the transistors not only degrades the DC, AC performance of transistors themselves but also the performance of nearby devices. Such a effect is illustrated in Figure 4.5.

As shown in Figure 4.5 (a), when the tail current is switched between input pair transistors, self heat generated inside transistors introduces large threshold

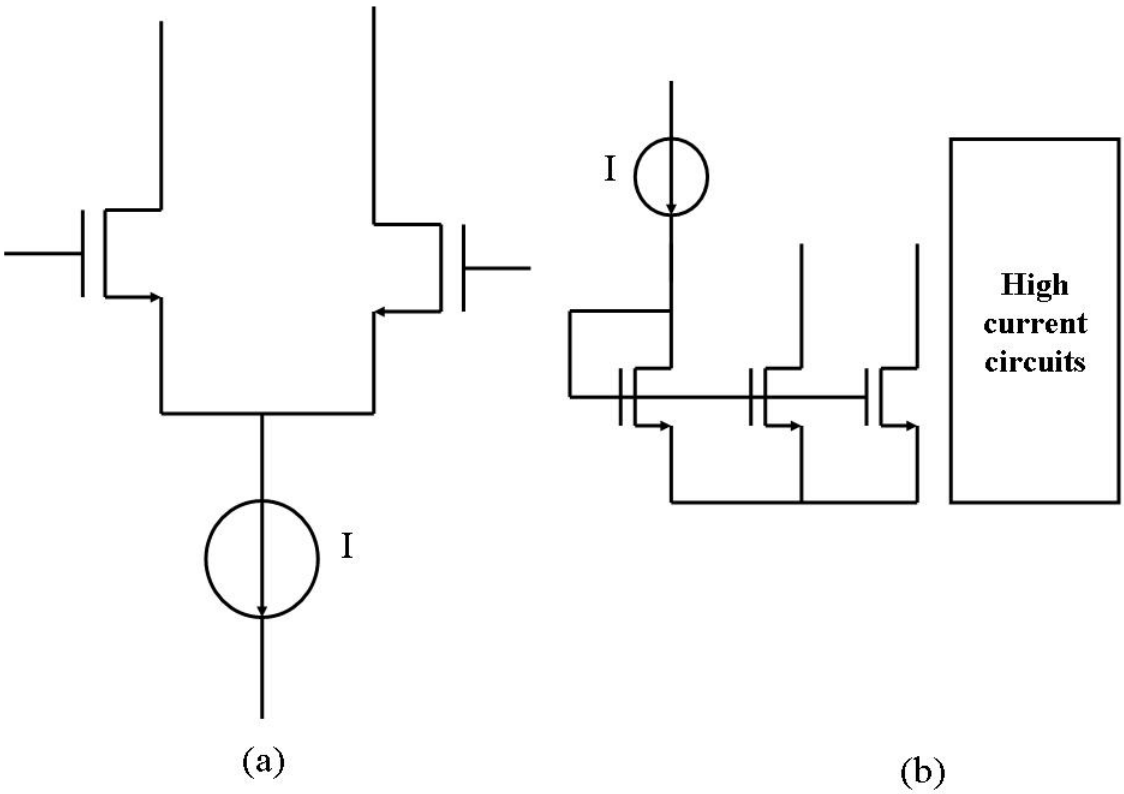


Figure 4.5: Illustration of self heating

voltage and mobility difference between transistors. This difference introduces large dc offset and ac performance degradation for the opamp. For converter design, this error is strongly signal dependant, which degrades conversion linearity. Self heat also degrades circuits performance nearby. As shown in Figure 4.5 (b), even the current mirror doesn't suffer from the self heating directly, self heating generated by near by devices still introduces additional errors. Another challenge with self heating is that it is very difficult to model the phenomena accurately since it is both process and layout structure dependant.

In summary, from system level analysis, in order to achieve the targeted performance with efficiency in real world applications, next generation high precision modulators have to be able to handle large input signal, adopt large first and second integrator coefficient without increasing internal integrator output swings while still maintaining excellent stability. For the circuit level design, the converter needs to limit the settling requirements of the front buffer and the internal opamps, generate minimum signal dependant current, reduce the size of internal opamp, capacitors, the isolation guard rings and limit the overall power consumption to improve performance and overcome thermal effects such as self heating.

Chapter 5

High Precision Delta Sigma Modulator Design

5.1 High precision delta sigma topology analysis

Single bit, single loop delta sigma topology was first applied to achieve 120dB dynamic range over the audio band [22]. The first drawback of single-bit delta sigma is that its modulator is prone to generate tones over the signal band for cases of low input signals. For professional audio applications, the signal band should also be free from tones for low level inputs. The second drawback is that it is difficult for high order analog modulators to achieve good stability. The modulation index is normally under 0.6 for fifth-order single loop, single bit modulators. In real world applications, if the modulator becomes unstable during cases such as high frequency signal energy leaks to the ADC input network, it is also hard for the analog modulator to recover from such unstable conditions. In most cases, the modulator has to be stopped and reset to recover from the unstable condition. This normally results

data loss in real time applications. Finally, high power consumption, which is close to one watt for a stereo audio ADC [22], becomes the bottleneck to further improve the ADC performance and lower the system level cost. An alternative approach is to use cascaded delta sigma modulation topology. Since the modulator is composed of multiple low order modulators, this topology is able to achieve excellent stability. The main limitation for this approach is that the quantization noise and tones from the first stage, low order delta sigma loop of a multistage converter tends to leak to the converter output due to stage-to-stage mismatch [30] [31], which makes it difficult to avoid idle tones in the signal band. Based on analysis from previous chapters, it is easy to conclude that achieving high performance with high levels of analog and digital circuit integration, while maintaining low power consumption, reducing front buffer settling requirements and small die area are the major challenges for future high precision analog to digital converter design. A multibit delta sigma topology has been demonstrated to be suitable for modern day high-precision analog to digital conversion design.A conventional first order multibit delta sigma modulator is shown in Figure 5.1. The main advantage over a single-bit design is its ability to reduce integrator output swings, which relaxes the analog circuit design requirements and reduces power consumption. Such a benefit becomes more critical for high performance A/D converter design. A multibit delta sigma topology with a large number of quantization levels also significantly lowers the out-of-band quantization noise energy, which greatly relaxes the decimation filter design requirements. Compared with continuous time topology, a switched capacitor topology is widely used for high precision ADC design due to its relatively less sensitivity to process variations.

The integrator transfer function of the conventional first order multibit delta

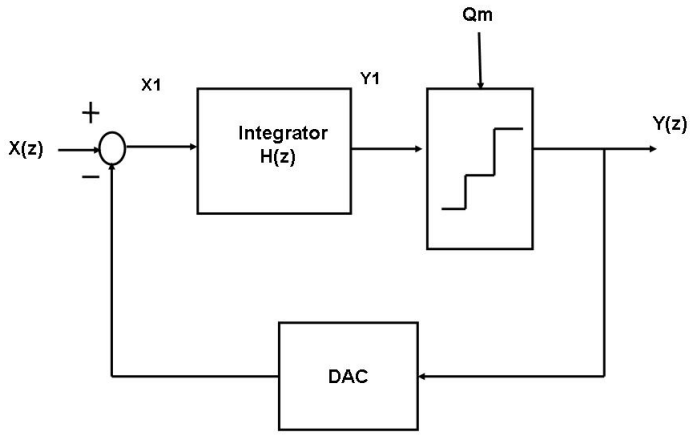


Figure 5.1: Multibit delta sigma architecture

sigma modulator, which is shown in Figure 5.1 is $\frac{z^{-1}}{1-z^{-1}}$. As shown in the second chapter, its output can be expressed as

$$Y(z) = X(z) \cdot z^{-1} + Q_m(z) \cdot (1 - z^{-1}) \tag{5.1}$$

The internal signal X_1 and Y_1 can be expressed as:

$$X_1 = (1 - z^{-1}) \cdot X - (1 - z^{-1}) \cdot Q_m(z) \tag{5.2}$$

$$Y_1 = z^{-1} \cdot X - z^{-1} \cdot Q_m(z) \tag{5.3}$$

where Q_m is the quantization noise of the multibit quantizer and X is the input signal. Both the internal signal X_1 and Y_1 shows strong dependence on the input signal. Contrary to common impression about multibit topology, integrator

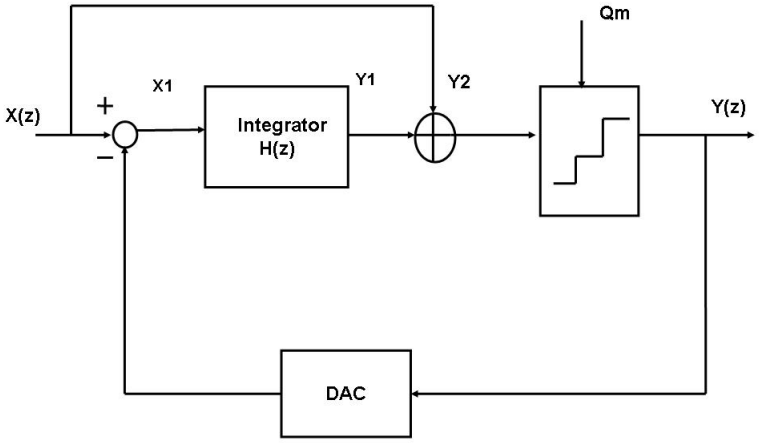


Figure 5.2: Feedforward multibit delta sigma architecture

output swing doesn't scale down proportionally with the increase of quantization level, which seriously diminishes the benefit of the multibit modulator structure. As input signal energy appears in the internal nodes, it substantially increases the settling requirements of internal opamp and introduce additional nonlinearity. Furthermore, high frequency energy leaks to input node can also quickly degrade the stability of the internal opamp and modulator.

A first order feedforward modulator architecture is shown in Figure 5.2. In this topology, the input signal is directly fed into the quantizer, which force the internal quantizer to track the input signal to first order throughout the operation.

The output and internal signals can be expressed as:

$$Y(z) = X(z) + Q_m(z) \cdot (1 - z^{-1}) \tag{5.4}$$

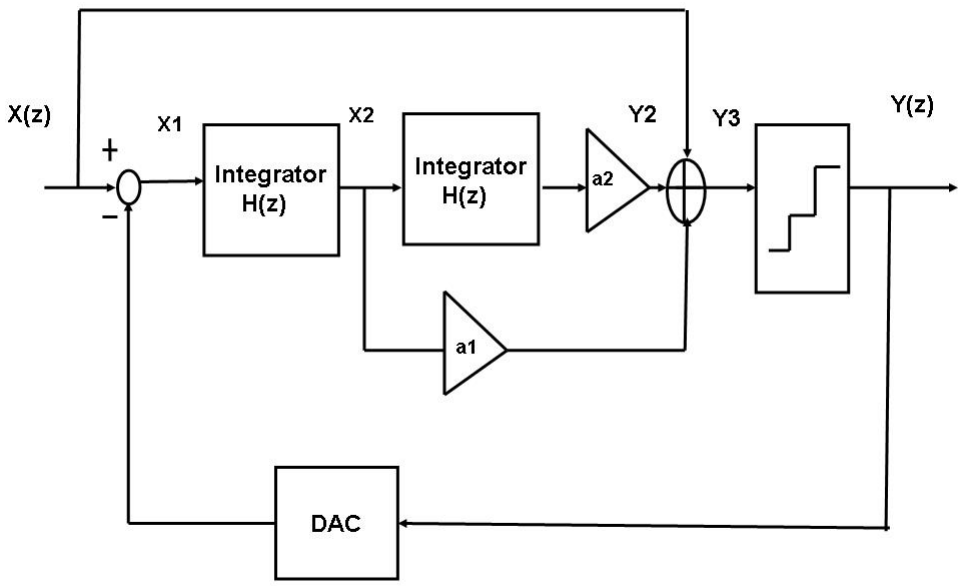


Figure 5.3: Second order feedforward multibit delta sigma architecture

$$X_1 = -(1 - z^{-1}) \cdot Q_m \tag{5.5}$$

$$Y_1 = -z^{-1} \cdot Q_m \tag{5.6}$$

$$Y_2 = X(z) - z^{-1} \cdot Q_m \tag{5.7}$$

In this structure, there is no input signal component in the input and output nodes of the internal opamp. This topology can be extended further to second order architecture. A second order feedforward delta sigma modulator is shown in Figure 5.3.

$$Y(z) = X(z) + Q(z) \cdot (1 - z^{-1})^2 \tag{5.8}$$

$$X_1 = -(1 - z^{-1})^2 \cdot Q_m \tag{5.9}$$

$$X_2 = -z^{-1}(1 - z^{-1})^2 \cdot Q_m \tag{5.10}$$

$$Y_2 = -a_2 \cdot z^{-2} \cdot Q_m \tag{5.11}$$

$$Y_3 = X + a_2 z^{-1} \cdot (z^{-1} - a_1) \cdot Q_m \tag{5.12}$$

Since integrator output swing depends mostly on quantization noise, instead of input signal level in this approach, it not only reduces opamp settling requirements and power consumption, but also reduces signal dependent energy generated inside the loop, which helps to reduce inter channel interference. Another implication for this architecture is larger input signal can be used since the internal opamp swing depends only on quantization noise. In conventional modulator design, large input signal appears in the internal opamp output is more likely to saturate the circuits. So far, we assume linear model for above calculations. For actual multibit quantizer, the signal energy cancellation at X_1 is not perfect due to the variation of the multibit quantizer gain. The signal energy leaks into the loop normally propagates and accumulates at the last down stream integrator output which results in the largest output swing among all integrators. Therefore, the integrator output swings are based on both the internal quantizer resolution and the order of loop filter.

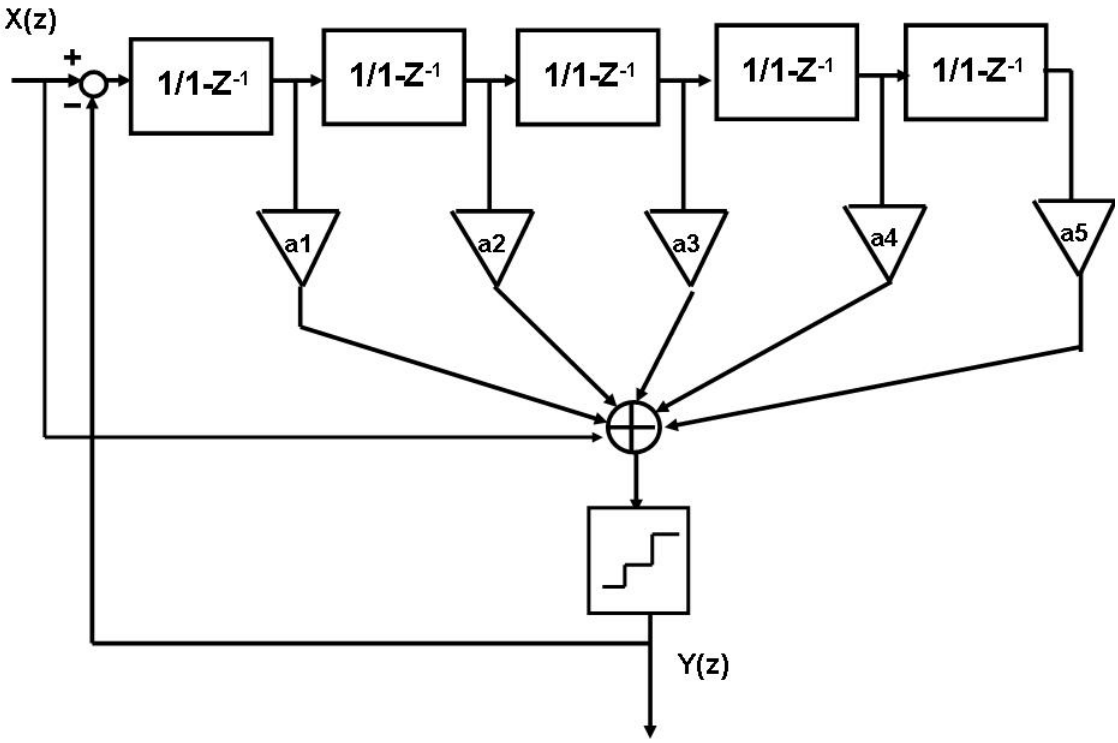


Figure 5.4: High order feedforward delta sigma architecture

Increasing quantizer resolution decreases quantization noise energy, which reduces integrator output swings,while increasing the order of loop filter accumulates more signal energy to integrator output in real design due to the variation of quantizer gain. A fifth order feedforward architecture is shown in Figure 5.4

For L-th order feedforward summation delta sigma modulator, the output can be expressed as:

$$Y(z) = (X(z) - Y(z)) \cdot (\frac{a_1}{1 - z^{-1}} + \frac{a_1 a_2}{(1 - z^{-1})^2} + \frac{a_1 a_2 a_3}{(1 - z^{-1})^3} + \cdots + \frac{a_1 a_2 \cdot \cdot a_L}{(1 - z^{-1})^L}) + X(z) + Q_m \tag{5.13}$$

$$Y = X + \frac{(1 - z^{-1})^L}{1 + a_1 a_2 \cdot \cdot a_L + a_1 (1 - z^{-1})^{L-1} + a_1 a_2 (1 - z^{-1})^{L-2} + \cdot \cdot + a_1 a_2 \cdot \cdot a_{L-1} (1 - z^{-1})} Q_m \tag{5.14}$$

Therefore, the noise transfer function is:

$$NTF = \frac{(1 - z^{-1})^L}{1 + a_1 a_2 \cdot \cdot a_L + a_1 (1 - z^{-1})^{L-1} + a_1 a_2 (1 - z^{-1})^{L-2} + \cdot \cdot + a_1 a_2 \cdot \cdot a_{L-1} (1 - z^{-1})} \tag{5.15}$$

The last down stream integrator output swing S_L is:

$$S_L = \frac{a_1 a_2 \cdot \cdot a_L}{1 + a_1 a_2 \cdot \cdot a_L + a_1 (1 - z^{-1})^{L-1} + a_1 a_2 (1 - z^{-1})^{L-2} + \cdot \cdot a_1 a_2 \cdot \cdot a_{L-1} (1 - z^{-1})} Q_m \tag{5.16}$$

As opposed to the multistage case, all feedback DAC capacitors contribute thermal noise to the sampling capacitor and the dynamic element matching (DEM) circuit must suppress the static nonlinearity caused by capacitor mismatch. Since the DEM circuit is placed inside the modulator feedback loop, it is crucial to minimize its latency otherwise stability will be compromised.

A single loop multibit delta-sigma architecture is selected for this design. However, traditional single loop multibit design results in large integrator output swings due to input signal energy leakage into the delta sigma loop. A feedforward

architecture is adopted in this work [10] [33] [34].A conventional second order single loop multi-path feedforward delta-sigma modulator is shown in Figure 5.5. The signal feedforward path 1 prevents most signal energy from leaking into the delta sigma loop, which limits output swings of all integrators. Since the quantizer gain is not constant across input range, there are residual signal energy leaks into the delta sigma modulator, which diminish the advantage of adopting multilevel topology. A second input feedforward path is added to cancel the residual input signal energy remaining inside the delta-sigma loop. However, for a high order, many-level delta-sigma modulator, input feedforward paths for downstream integrators increases die area, layout complexity and power consumption.

5.2 Proposed high precision delta sigma modulator architecture

The delta-sigma analog modulator adopted in this design to meet various challenges is shown in Figure 5.8 . It is a modified 5th order feedforward modulator with thirty-three quantization levels. A large number of quantization levels are selected to reduce the out-of-band quantization noise energy, which relaxes the on-chip decimation filter design requirements, and to eliminate tones for low level inputs. The signal feedforward path 1 prevents most signal energy from leaking into the delta-sigma loop, which limits the output swings of all integrators. Residual signal energy leaks into the modulator are mostly accumulated at the last downstream integrator output. This suggest that there are input signal energy remains at the output of the last integrator. The input signal is added negatively to the input of the last integrator, which is easy to implement in a fully differential structure, to cancel the remaining signal energy. Equation (5.13) now becomes

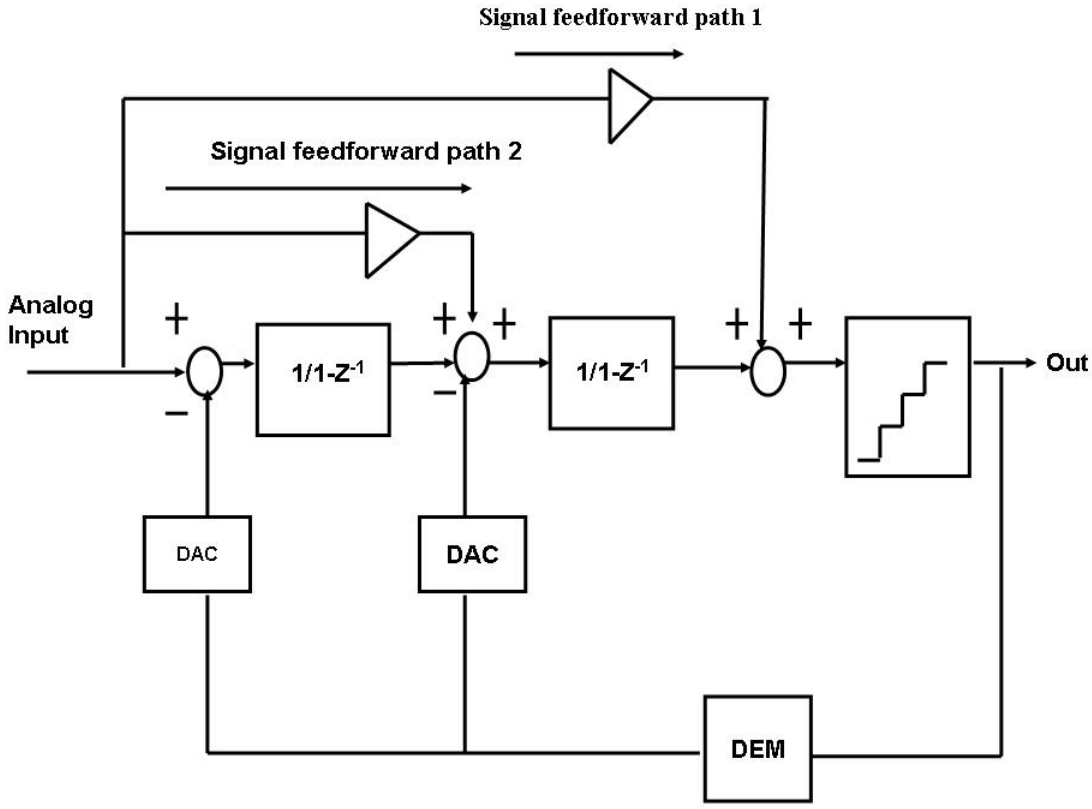


Figure 5.5: Conventional feedforward delta sigma modulator

$$Y = (X-Y)\cdot(\frac{a_1}{1-z^{-1}}+\frac{a_1a_2}{(1-z^{-1})^2}+\frac{a_1a_2a_3}{(1-z^{-1})^3}+\cdot\cdot+\frac{a_1a_2\cdot\cdot a_L}{(1-z^{-1})^L})+X-\frac{bX}{1-z^{-1}}+Q_m \tag{5.17}$$

The signal swing at the last integrator output is:

$$\begin{aligned} S_L &= -\frac{(1-z^{-1})^L\cdot bX}{(1+a_1a_2\cdot\cdot a_L+a_1(1-z^{-1})^{L-1}+\cdot\cdot+a_1a_2\cdot\cdot a_{L-1}(1-z^{-1}))\cdot(1-z^{-1})} \\ &\quad +\frac{(1-z^{-1})^L\cdot Q_m}{1+a_1a_2\cdot\cdot a_L+a_1(1-z^{-1})^{L-1}+\cdot\cdot+a_1a_2\cdot\cdot a_{L-1}(1-z^{-1})} \end{aligned}$$

This approach limits the output swings of all integrators with minimum increase of system and circuit level complexity. All integrator output swings and maximum steps are shown in Table 5.1 Additional negative feedforward paths can be added to the inputs of integrator 2 to integrator 4 to further reduce their output swings at the expense of increasing analog circuit complexities. As this modulator structure suppresses all integrator output swings, it helps to reduce signal dependant energy injected into substrate and noise coupling between the analog modulator, which improves the inter-channel isolation for this stereo converter. Finally, for over range input signal, the modulator returns to normal operation after the over range condition is gone without resetting the loop. This minimizes possible data loss in real applications. Outputs of the first and last integrator during recovering from over range input signal are shown in Figure 5.6 and Figure 5.7 The integrator outputs are able to return to normal range after the over range signal condition is removed.

Although increasing the oversampling ratio decreases the sampling capacitor size, this translates to less settling time for integrator opamp and digital switching

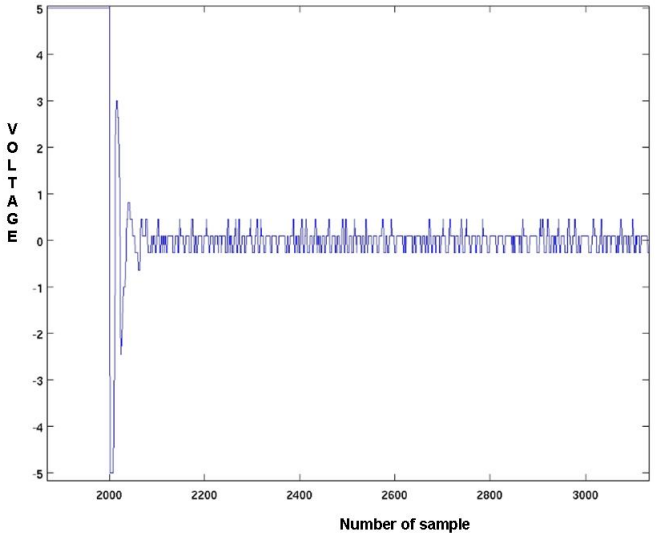


Figure 5.6: First integrator output during over range signal recovering process

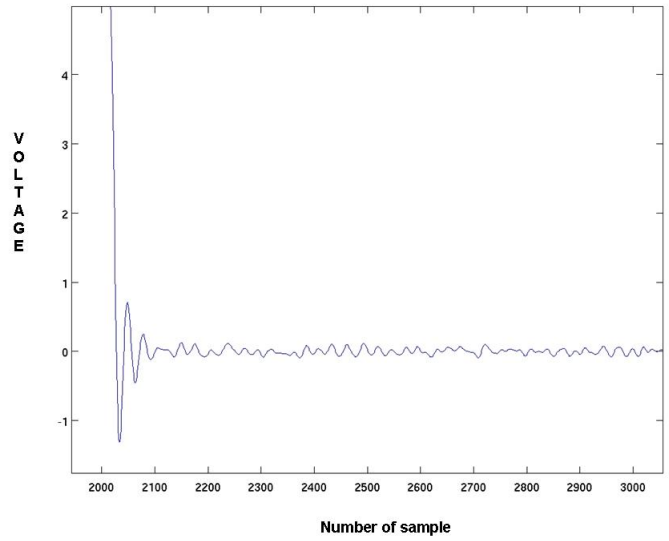


Figure 5.7: Last integrator output during over range signal recovering process

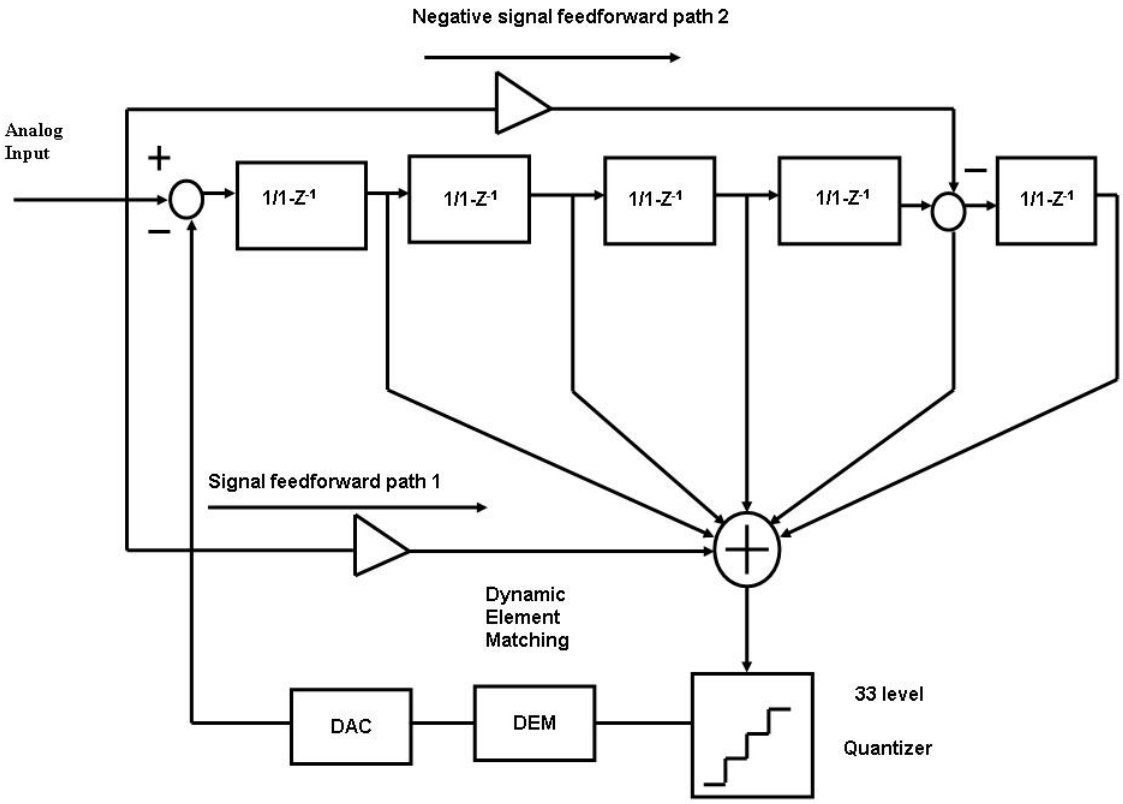


Figure 5.8: High precision feedforward delta sigma modulator

noise, which makes the converter sensitive to digital coupling noise. An oversampling ratio of 128 is chosen for this design, which is a trade off between digital switching noise immunity, die area and power consumption. This architecture also helps to improve modulator stability and prevent overload for full scale input signals. Clocked at 6.144MHz, the theoretical SNR of this this analog modulator is 145dB over a 20 kHz bandwidth. The maximum modulation index exceeds 0.95 for this design.

The fft plot of the modulator output is shown in Figure 5.9

The poles and zeros of the signal transfer function is shown in Figure 5.10

Integrator Output	Int1	Int2	Int3	Int4	Int5
Maximum Swing	0.52	0.65	0.78	0.95	0.89
Maximum step	0.32	0.25	0.19	0.15	0.11

Table 5.1: Integrator output maximum swings and steps

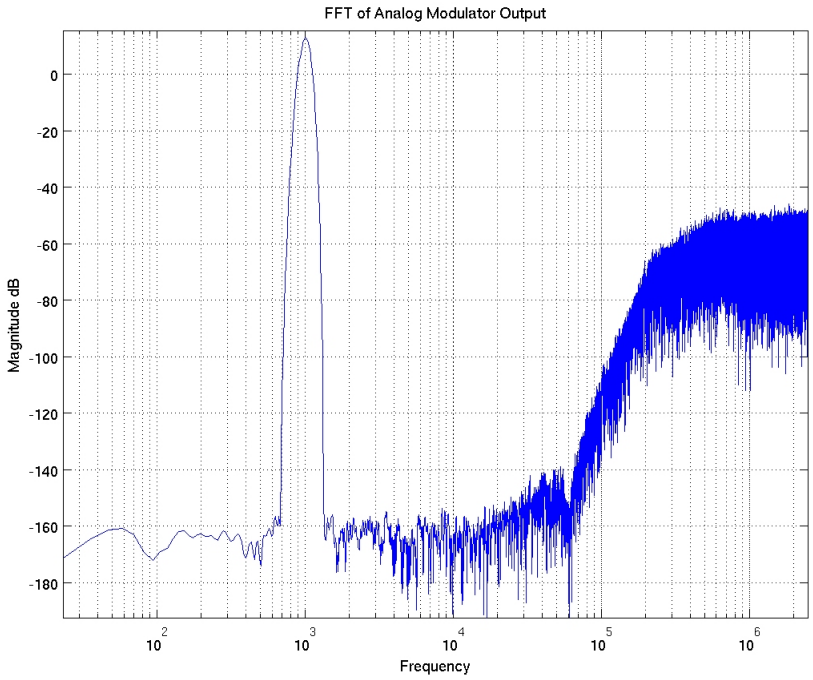


Figure 5.9: FFT plot of the modified feedforward delta sigma modulator

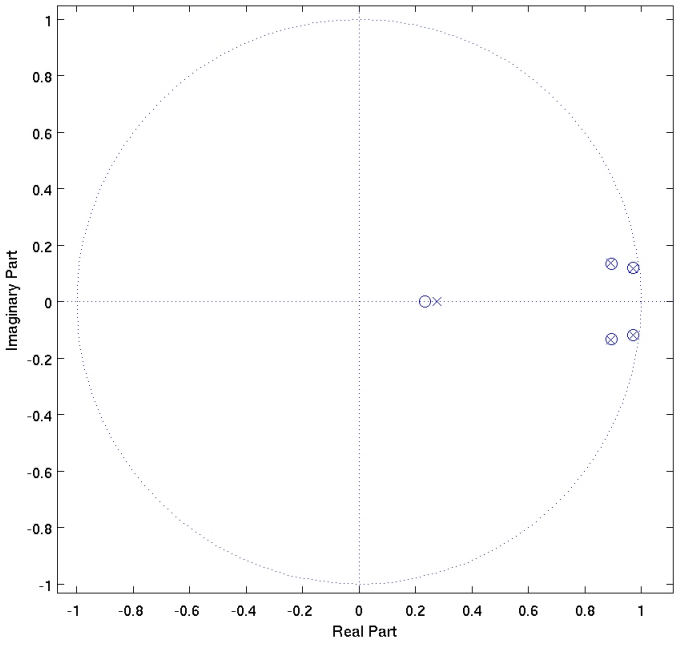


Figure 5.10: Poles and zeros of the signal transfer function

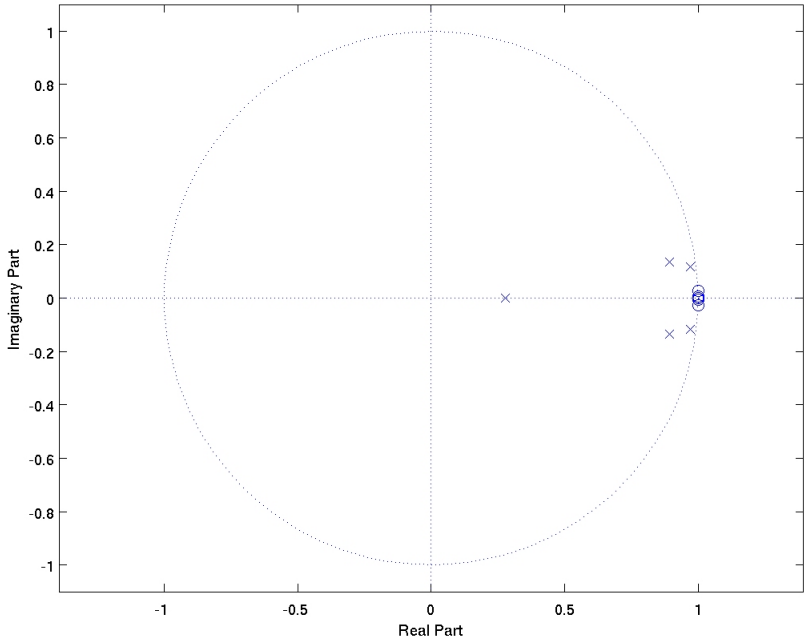


Figure 5.11: Poles and zeros of the noise transfer function

The poles and zeros of the noise transfer function is shown in Figure 5.11

Chapter 6

Analog Sub-circuit Design

For single loop delta sigma modulator design, since the quantizer is inside the delta-sigma loop, it can only tolerate minimum latency. A flash type A/D converter is normally adopted for the quantizer due to its low latency. A conventional flash type quantizer doubles in size for each additional bit of resolution. A large number of comparators also inject a substantial amount of signal dependant noise energy into the substrate, which causes degradation of converter performance and severe interference between channels in the case of multi-channel converter design. Furthermore, having many quantization levels decreases the reference voltage step substantially, which increases design and layout requirements of individual comparators. A large number of comparators also create large "kick-back" on the quantizer reference line, which potentially introduces excessive errors. Tracking quantizers [35], which is shown in Figure 6.1 , have been reported to deal with the issue. This topology employs additional digital to analog (DAC) circuits to generate input signal tracking reference voltages to reduce the total number of comparators. However, this approach suffers from several major shortcomings such as requiring a separate circuit

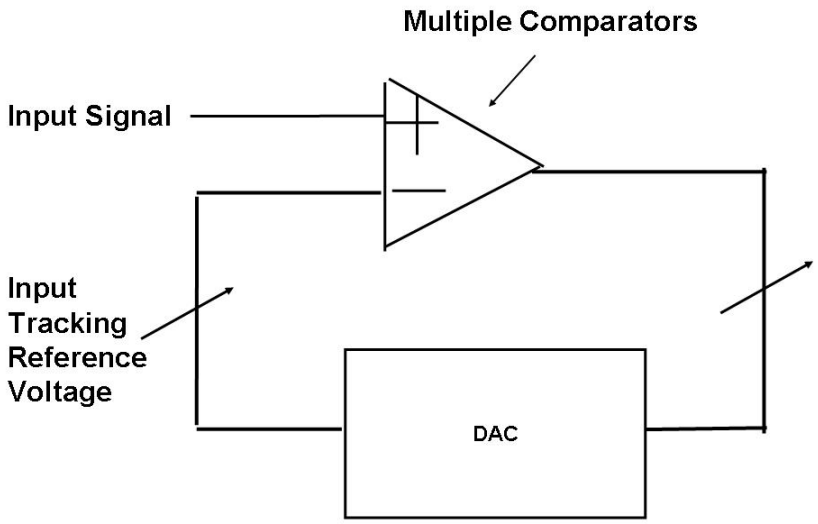


Figure 6.1: Input tracking multilevel quantizer scheme

to set up the initial loop operating point, DAC circuits, and potential modulator instability due to high frequency input signal leakage, which makes it risky to apply the design to real world applications.

The multilevel quantizer topology applied in this design is shown in Figure 6.2. The quantization levels are divided into two sections, which are coarse and fine. The quantizer changes one quantization level in the fine section, while it changes two quantization levels in the coarse section. In order to utilize existing dynamic element matching (DEM) logic circuits [38], the middle quantization output bit is interpolated by ANDing two adjacent comparator outputs in the coarse quantization section. The multilevel quantizer output waveform is shown in Figure 6.3.

Since the multilevel quantizer is inside the loop, nonlinearity introduced by this approach is suppressed by the delta sigma modulator. The fine quantization

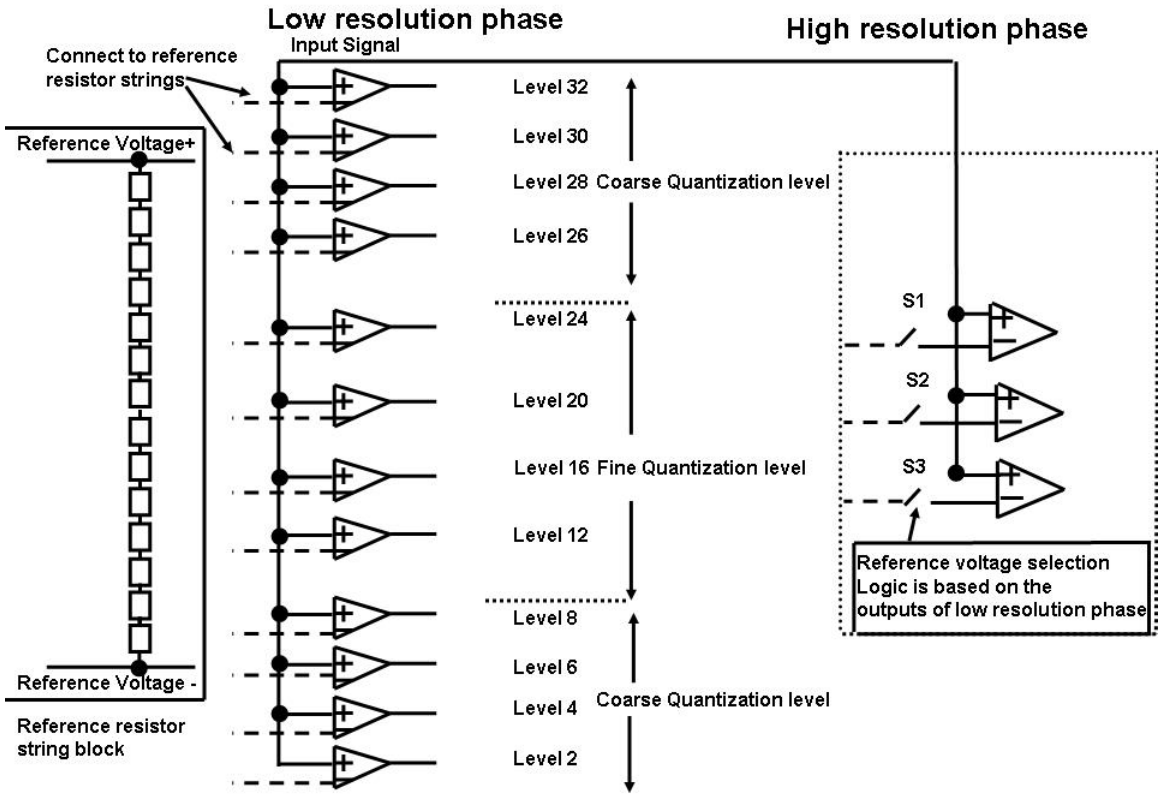


Figure 6.2: Dual phase multilevel quantizer

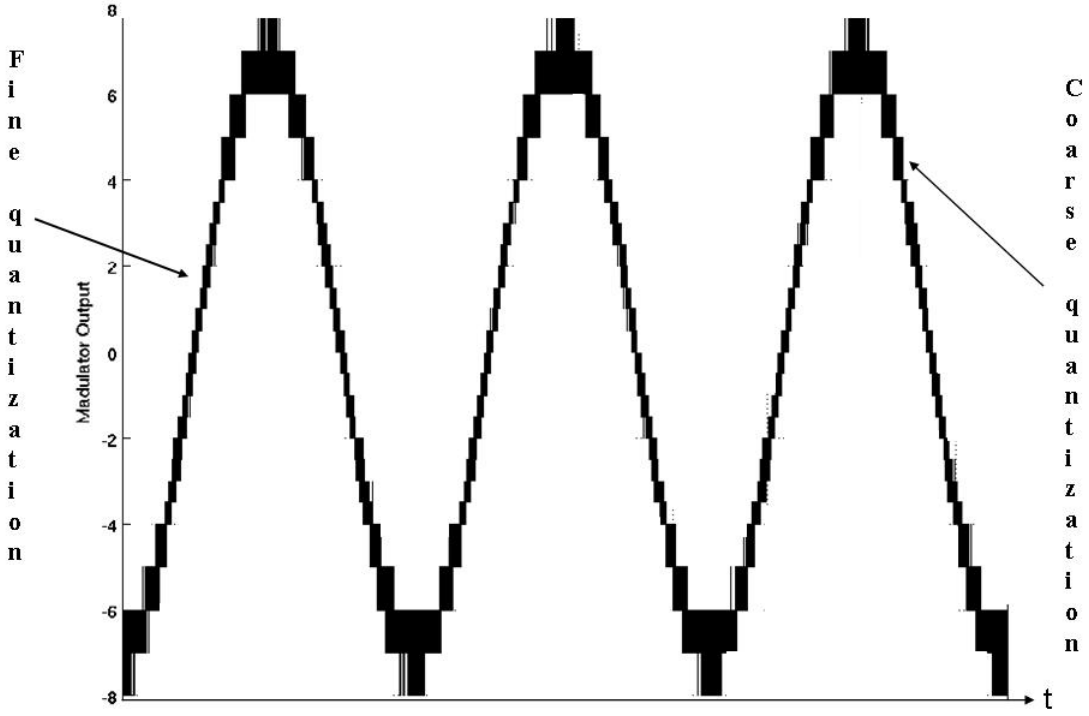


Figure 6.3: Dual phase multilevel quantizer output waveform

section, which is from level 8 to level 24, is further divided into two phases, a low resolution phase and high resolution phase. There are four comparators in the low resolution phase, and three reference voltage levels interleave between two adjacent comparators. The high resolution phase consists of three comparators. During the low resolution phase, if adjacent comparators outputs are the same, then comparison operations between these bits are skipped and the outputs are "interpolated" by simple digital logic circuits. Switches S1, S2 and S3 are controlled by an XOR of adjacent low resolution comparator outputs. For example, if the level 20 output is low and level 16 output is high, the XOR of these two outputs is high. This operation turns on the switches S1, S2 and S3, which steers the high resolution comparators to detect level 17 to level 19. On the other hand, if both level 20 and level 16 are high or low, this suggests that the input level is either higher than level 20 or lower than level 16, and quantization operations between level 17 to level 19 can be skipped.

For large input signals, the ADC output performance is dominated by nonlinearity components such as even and odd harmonics. This new scheme, which increases quantization noise slightly for large input signals, virtually has no impact on large input signal ADC performance. For small input signals, when nonlinearity components such as even and odd harmonics are negligible, the fine quantization level is applied to achieve the lowest noise floor. Although adding a large number of coarse quantization levels reduces die area and power consumption of the new multilevel quantizer, this introduces excessive quantization noise and degrades dynamic range for small input signal when nonlinearity harmonics are still negligible.

The low resolution phase comparators also set up the initial DC operational points for the delta-sigma loop. Ideally, an anti-alias analog filter in front of this

modulator filters out all high frequency signals. However, in real world applications, there are cases where high frequency energy is leaked to the A/D converter input that forces the quantizer to change multiple levels during one operation. The low resolution phase comparators are always able to track the input changes and maintain the stability of the delta-sigma loop. This new multilevel quantizer design reduces the number of comparators from thirty two to twelve in the low resolution phase and three in the high resolution phase, which significantly lowers the "kick back" on the quantizer reference line especially for the critical high resolution quantization phase. Furthermore, comparators in the low resolution phase only need to distinguish every two or four quantization levels, which relax the design requirements for individual comparators.

6.1 First Integrator and Feedback DAC Design

Flicker noise is one of the major noise source for baseband applications. Chopper stabilization technique is able to remove 1/f noise [10] [46]. A chopper stabilized opamp is shown in Figure 6.4.

The op-amp flicker noise is modulated once and moved up to the chopping frequency, away from the baseband. The input signal, however, is modulated up to the chopping frequency and then demodulated back down to baseband. Therefore, there exists a possibility that the high frequency shaped quantization noise could be demodulated down thus coupling additional noise into the converter signal band. Digital switching noise can also be coupled into the opamp input nodes and mismatch among chopper switches introduce additional noise as well. Chopper stabilization is purposely avoided for this single die, high precision design.

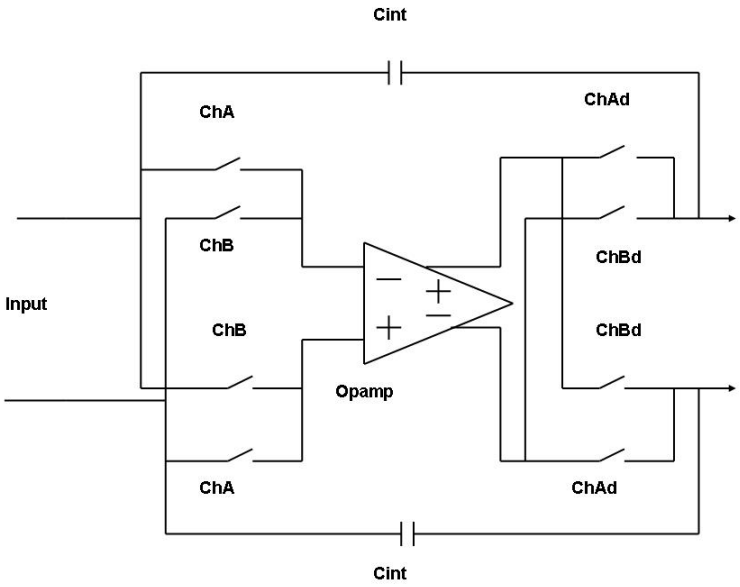


Figure 6.4: Chopper stabilized opamp

6.1.1 Reference scheme design

Noise form reference path is one of the major noise source in high precision design. One common approach is to use off chip reference circuits, which will allow the reference chip to use high end, low noise process to achieve the performance target. However, such scheme tends to substantially increase system level cost.

As shown in Equation 4.4, a high modulation index and large reference voltage minimizes the kT/C noise contribution from the feedback DAC capacitors, thus reducing the input sampling capacitor size for a given design target. On the other hand, passive rough and fine switched capacitor references are used to eliminate the noise from the reference path. [10] The passive reference scheme is shown in Figure 6.5. The feedback DAC samples either the analog power supply or analog power ground, depending on the code output from the DEM coupling logic, during the

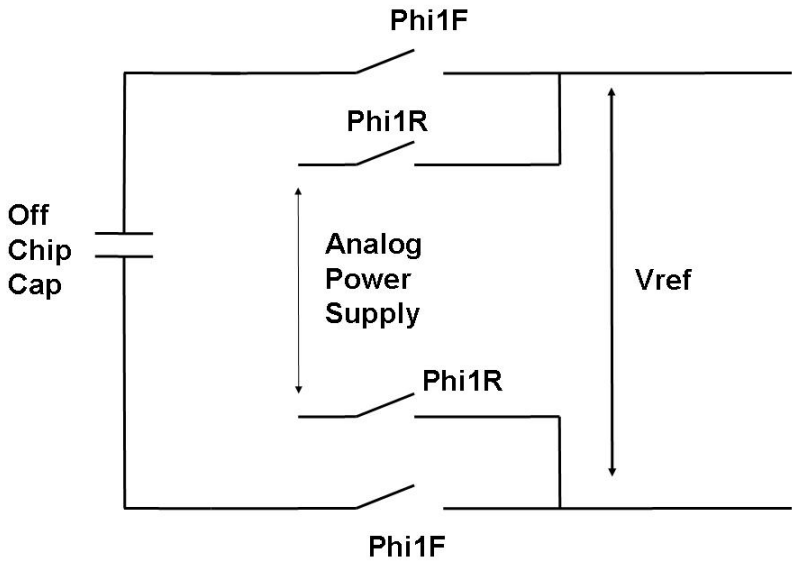


Figure 6.5: Passive rough and fine reference sampling scheme

rough phase. During the fine phase, the DAC is connected to an off-chip capacitor that effectively filters out high frequency noise components. The low pass corner frequency is set around 3 to 4Hz, and this configuration is able to achieve reasonably good power supply rejection (in the range of 60dB at 1kHz). However, better power supply rejection ratio is needed for the ultra high precision converter design.

An on-chip reference circuit is included in this design and a double sampled scheme [45] is used for both the input and the reference feedback network while single sampled scheme is used for all downstream integrators. For the input signal path, the double sampling scheme increases the signal charge, which lead to smaller sampling capacitor size and sampling switch size. For reference path, as shown in equation 4.4, the double sampling scheme minimizes the kT/C noise contribution from the feedback path, thus reducing the input sampling capacitor size for a given design

target. An on-chip reference circuit also provides better power supply rejection ratio than sampling the power supply [10]. An off chip capacitor is used to filter out the excessive noise in this case. A folded cascode architecture, which is similar to first integrator opamp, is used in the reference opamp design.

A conventional double sampled scheme [36] is shown in Figure 6.6 and Figure 6.7. For 5V power supply and 2.5V common mode voltage, if the V_{ref+} is 4V, then the V_{ref-} is 1V. Total equivalent feedback voltage is 6V. Normally, reference voltages are generated through gain stages from bandgap voltages. A conventional reference stage is shown in Figure 6.7. The noise from the bandgap is amplified through the gain stage to the reference signal V_{ref+} and V_{ref-}. In such a scheme, two off chip capacitors are required for each channel, which occupies large circuit board area for multichannel applications.

In order to further increase the reference voltage range, the V_{ref-} is connected to analog ground in our design. The equivalent reference voltage increases to 8V. The modified reference double sampled scheme is shown in Figure 6.8. The corresponding reference scheme is shown in Figure 6.9. Only one buffer and one off chip capacitor is used in this approach, which reduces the noise contribution from the reference path and the circuit board area required for this stereo design. The off capacitor also acts to absorb voltage glitches caused by the switching operation.

Also discussed in equation 4.4, a high modulation index helps to limit the noise contribution from the reference path as well. A modulation index of 0.9 is used in this design. Combined with the double sampling scheme for both the input and reference path, a fully differential configuration is used for the design to further suppress nonlinear errors such as clock injection, clock feed-through and digital coupling noise.

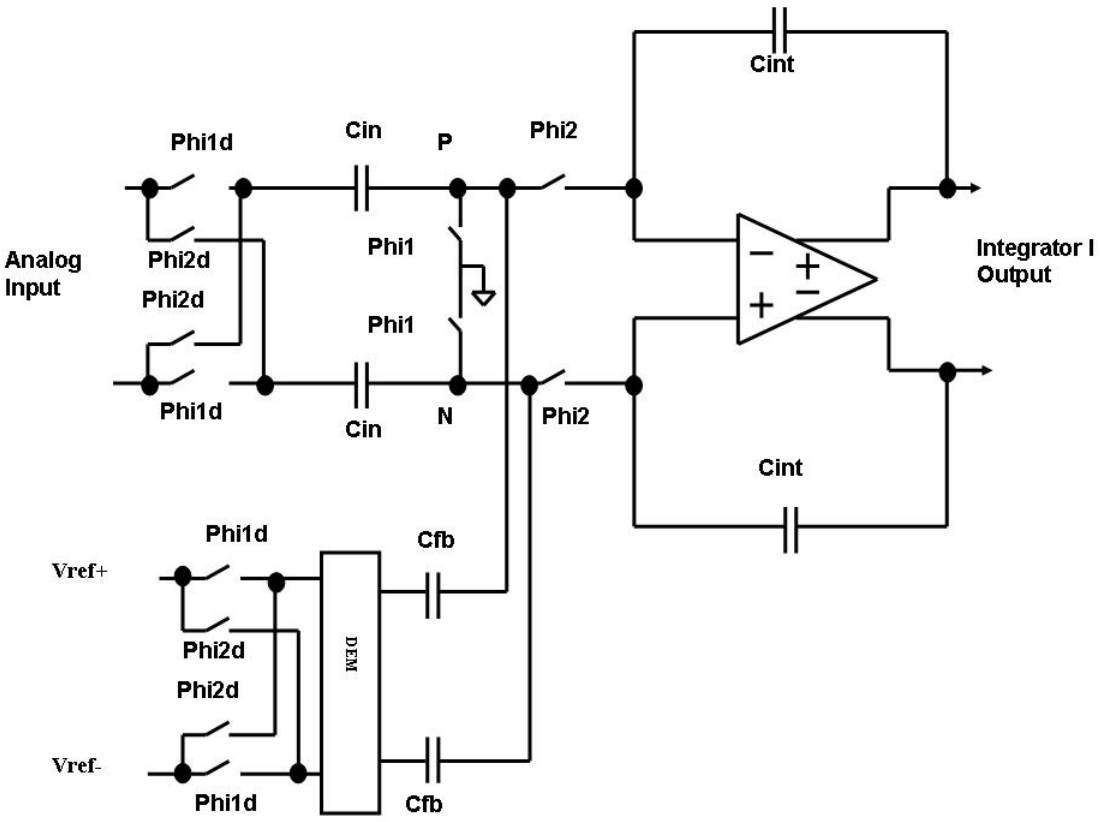


Figure 6.6: Switched capacitor first integrator and conventional feedback DAC circuit diagram

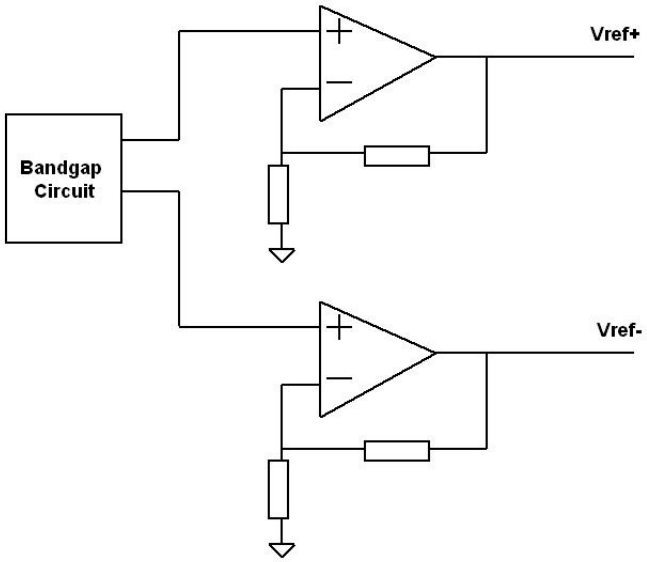


Figure 6.7: Conventional dual reference voltage generation circuit diagram

6.1.2 Input sampling switch design

Combined with the double sampling scheme for both the input and reference path, a fully differential configuration is used for the design to further suppress nonlinear errors such as clock injection, clock feed-through and digital coupling noise. Reducing the input sampling capacitor size leads to smaller sampling switches and less charge injection. The T-gate switch configuration is applied for this design to minimize design complexity and reduce die area. In order to maintain constant impedance through the input signal range, PMOS needs to be larger than NMOS since PMOS' mobility is normally smaller.

$$\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = \frac{\mu_N}{\mu_P} \tag{6.1}$$

where μ_N is the mobility for NOMS and μ_P is the mobility for PMOS.

On the other hand, NMOS and PMOS is chosen to have equal size to cancel

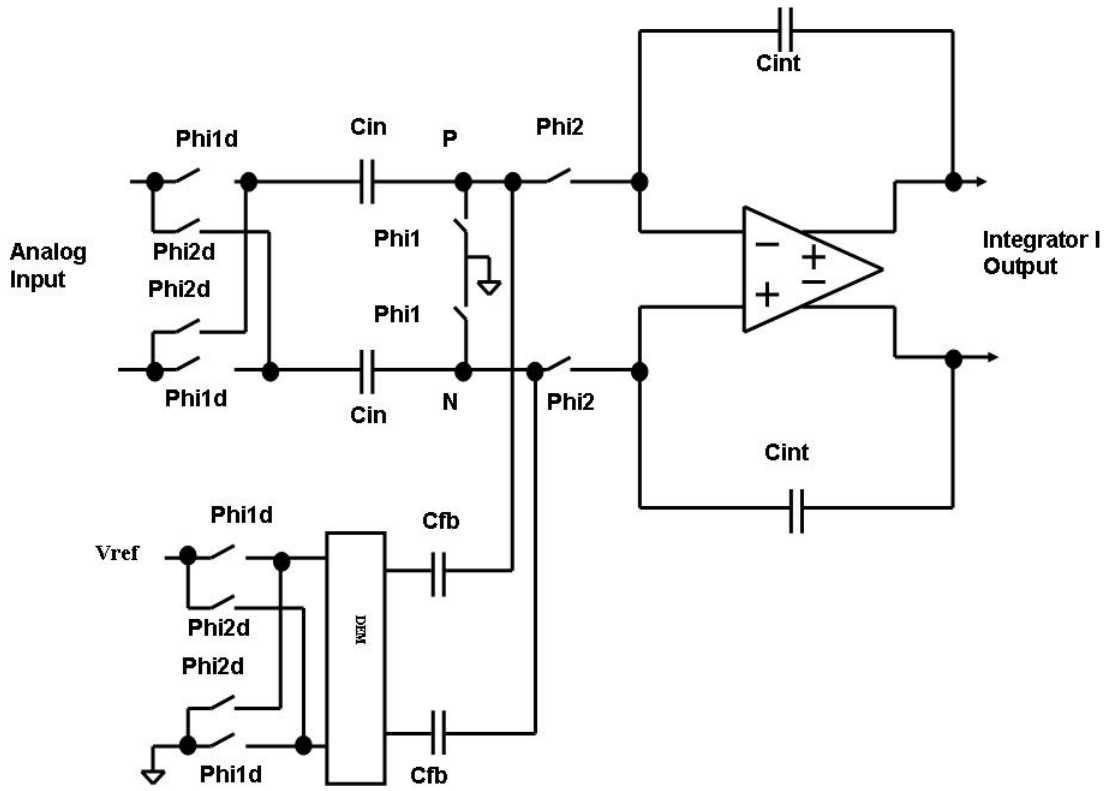


Figure 6.8: Switched capacitor first integrator and modified feedback DAC circuit diagram

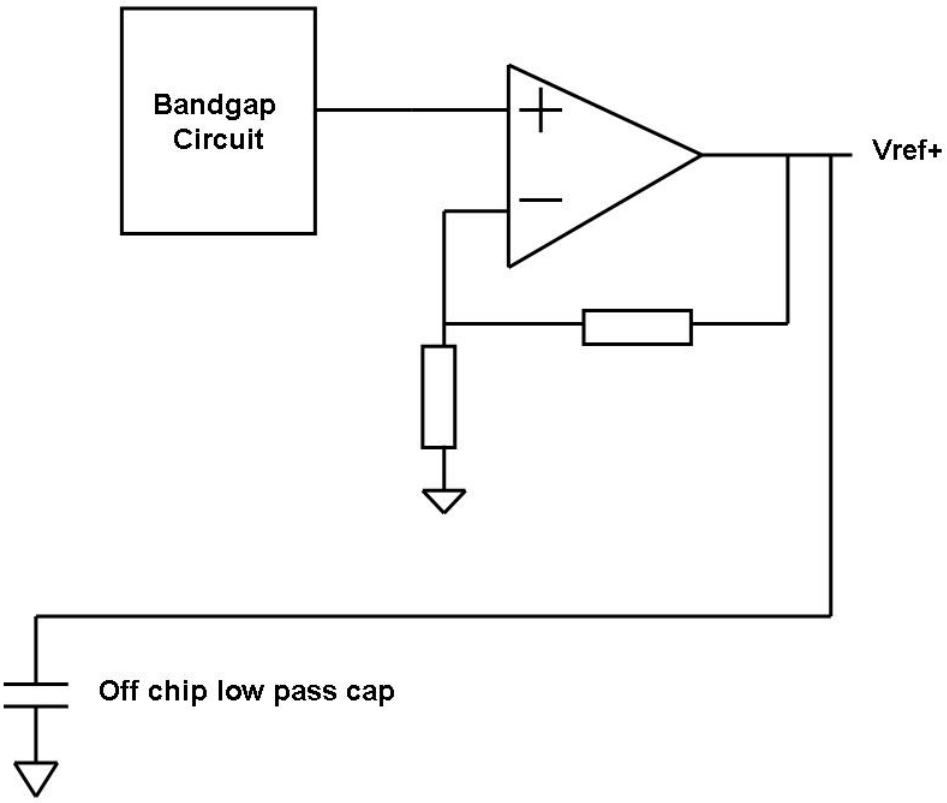


Figure 6.9: Single ended reference voltage generation circuit diagram

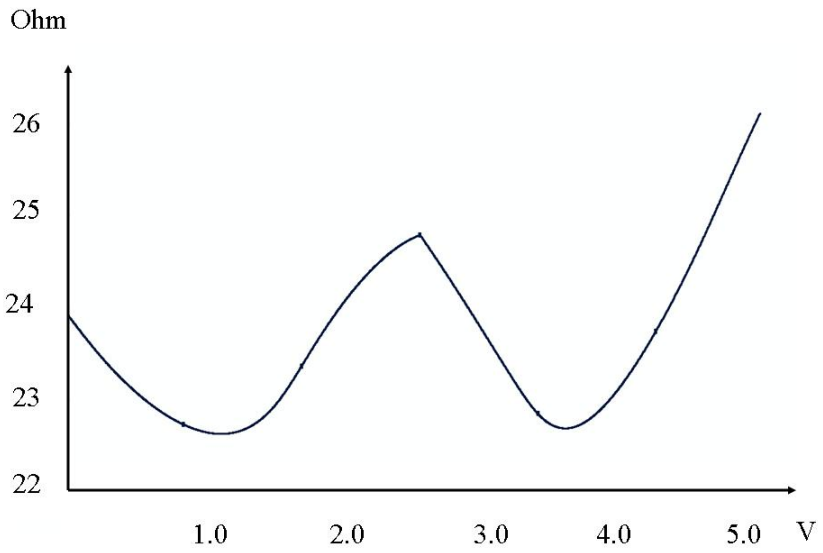


Figure 6.10: Sampling switch resistance across the voltage range

charge injection.

$$W_N \cdot L_N = W_P \cdot L_P \tag{6.2}$$

where W is the transistor width and L is transistor channel length.

A poly resistor is connected in serial with the T-gate in this design to further improve its linearity across signal range. Equation 6.1 and 6.2 are combined with the switched capacitor network time constant to choose the size of the switch transistor sizes. The sampling switch resistance across the supply range is shown in Figure 6.10. Although other alternative approaches such as front slew boosting unity gain opamp or switching opamp are also able to further minimize the switch charge injection, the decision is based on trade-offs between circuit performance, complexity, die area and power consumption.

6.1.3 Opamp analysis and design

Since the modified feedforward modulator eliminates most signal energy leakage into the delta sigma loop and reduces integrator output swing, a class A type opamp is adopted for Integrator I and the design still achieves the power consumption target. The quantization noise leakage due to finite integrator opamp DC gain has potential to seriously degrade the converter performance. On the other hand, the opamp also has to provide large slew rate. The integrator opamp is the major contributor to the overall converter power consumption and die area. Therefore, it is important to accurately model the finite opamp DC gain effects. The block diagram of the first integrator with feedback reference is shown in Figure 6.11

For ideal case when the opamp gain is infinity, the integrator output can be expressed as

$$V_{out} = \frac{z^{-1}}{1 - z^{-1}}(\frac{C_{in}}{C_{int}}V_{in} + \frac{C_{fb}}{C_{int}}V_{ref}) \tag{6.3}$$

For cases when the opamp gain is finite,

At t=n-1:

$$Q_1[n-1] = C_{in}(V_{in}[n-1] - V_x[n-1]) \tag{6.4}$$

$$Q_2[n-1] = C_{fb}(V_{ref}[n-1] - V_x[n-1]) \tag{6.5}$$

$$Q_3[n-1] = C_{int}(V_{out}[n-1] - V_x[n-1]) \tag{6.6}$$

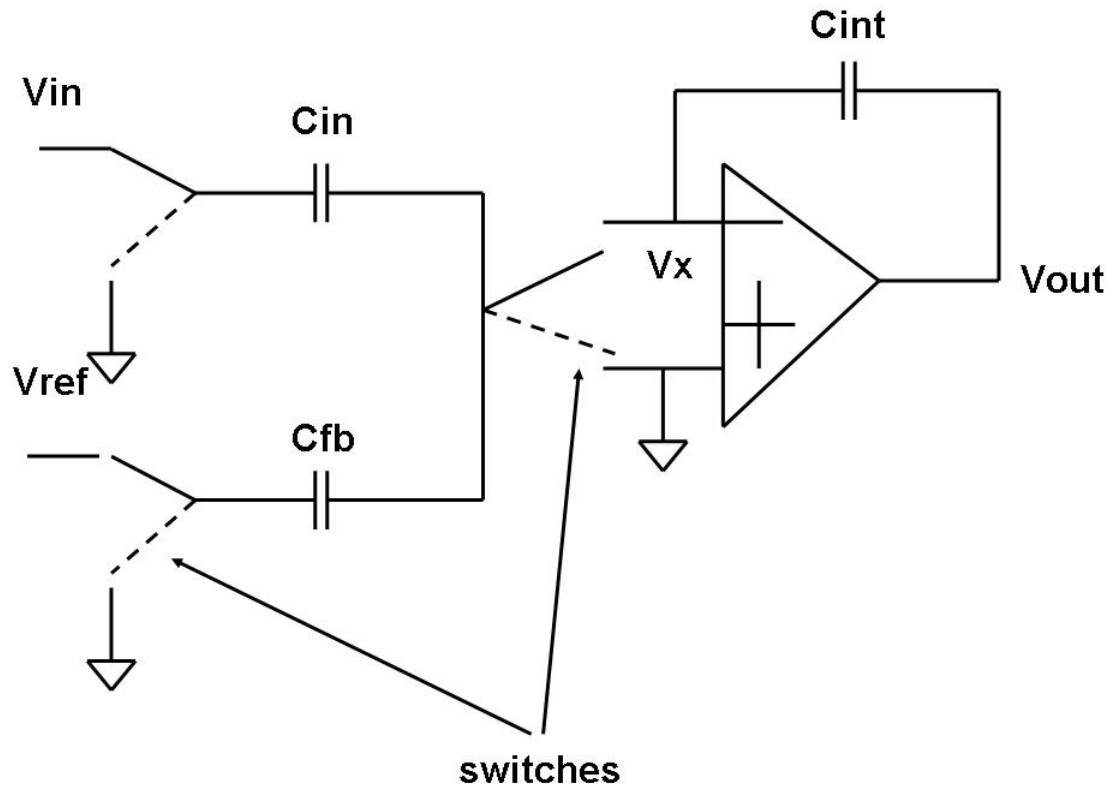


Figure 6.11: First integrator with feedback reference capacitor block diagram for opamp finite DC gain analysis

$$V_{out}[n-1] = -V_x[n-1] \cdot A \tag{6.7}$$

At t=n:

$$Q_1[n] = -V_x[n] \cdot C_{in} \tag{6.8}$$

$$Q_2[n] = -V_x[n] \cdot C_{fb} \tag{6.9}$$

$$Q_3[n] = C_{int}(V_{out}[n] - V_x[n]) \tag{6.10}$$

$$V_x[n] = -\frac{V_{out}[n]}{A} \tag{6.11}$$

$$((V_{out}[n]-V_x[n])-(V_{out}[n-1]-V_x[n-1]))\cdot C_{int} = C_{in}V_{in}[n-1]+V_x[n]C_{in}+C_{fb}V_{ref}[n-1]+V_x[n]C_{fb} \tag{6.12}$$

Insert Equation 6.8, 6.9, 6.10 and 6.11 into Equation 6.12, assume the integrator is reset during the start up sequence and transform the equation to z domain.

$$V_{out1}(1 - z^{-1})C_{int} = -\frac{V_{out1}}{A}C_{in} - \frac{V_{out1}}{A}C_{fb} + (C_{in}V_{in} + C_{fb}V_{ref})z^{-1} \tag{6.13}$$

The Equation 6.14 can be rewritten as

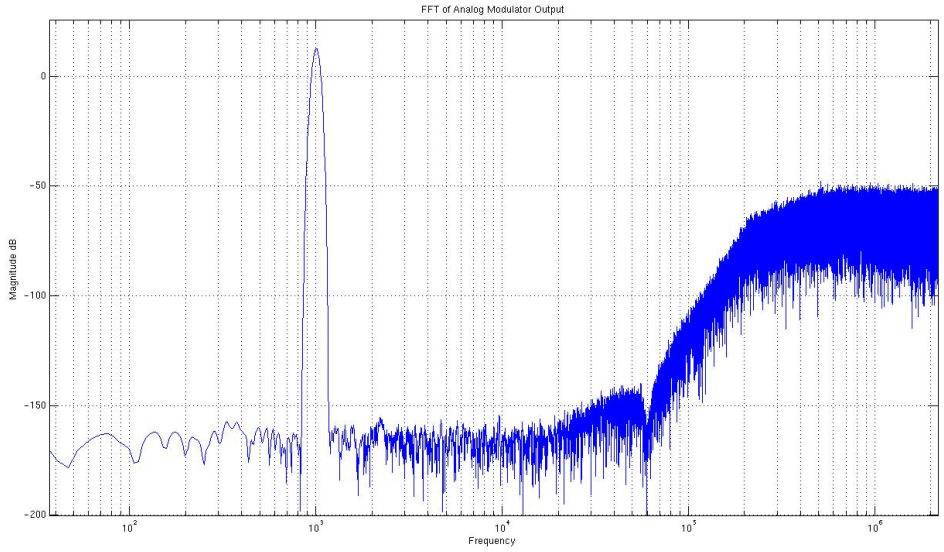


Figure 6.12: Simulated converter output FFT plot of 85dB opamp DC gain

$$V_{out1} = \frac{(C_{in}V_{in} + C_{fb}V_{ref})z^{-1}}{(1-z^{-1})C_{int} + \frac{C_{in}}{A} + \frac{C_{ref}}{A}} \tag{6.14}$$

For the next clock cycle

$$V_{out2} + \frac{V_{out2}}{A} = \frac{C_{in}}{C_{int}}(V_{x2} + V_{in}) + \frac{C_{fb}}{C_{int}}(V_{x2} + V_{ref}) + V_{out1} + \frac{V_{out1}}{A} \tag{6.15}$$

$$V_{out2} = \frac{\frac{C_{in}}{C_{int}}V_{in} + \frac{C_{fb}}{C_{int}}V_{fb} + (1+\frac{1}{A})V_{out1}}{1 + \frac{1}{A}(1 + \frac{C_{in}}{C_{int}} + \frac{C_{fb}}{C_{int}})} \tag{6.16}$$

The calculation is included in the delta sigma behavioral simulation. The converter output fft plot of 85dB opamp DC gain is shown in Figure 6.12. The signal to noise ratio is 140dB over 20kHz audio bandwidth.

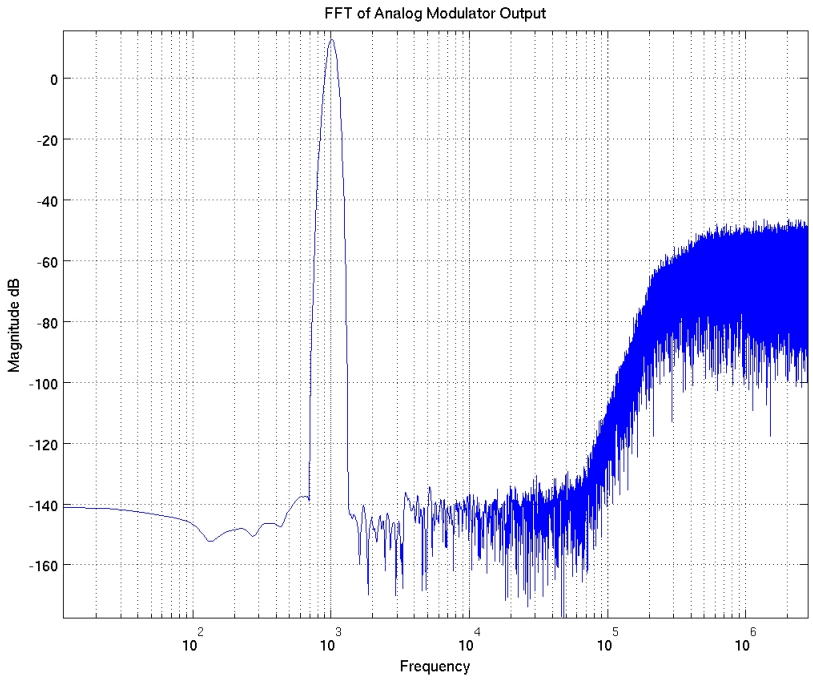


Figure 6.13: Simulated converter output FFT plot of 75dB opamp DC gain

The converter output fft plot with 75dB opamp DC gain from Matlab simulation is shown in Figure 6.13. The signal to noise ratio is 128dB over 20kHz audio bandwidth. The internal opamp DC gain is selected around 85dB for this converter.

A class A type opamp is selected mainly due to its constant tail current, instead of a class AB type opamp which generates a large amount of signal dependent current inside the chip. As shown in Figure 6.14, a folded cascode, single stage opamp with PMOS input pair is selected for the first integrator opamp. PMOS input pair is used because of its low flicker noise and the PMOS N-well provides isolation and shielding from analog and digital coupling noise. A cascode stage, which is biased by bias voltage 3, is added to the input pair to provide additional protection for the input pair. Reduced integrator output swing also relaxes design

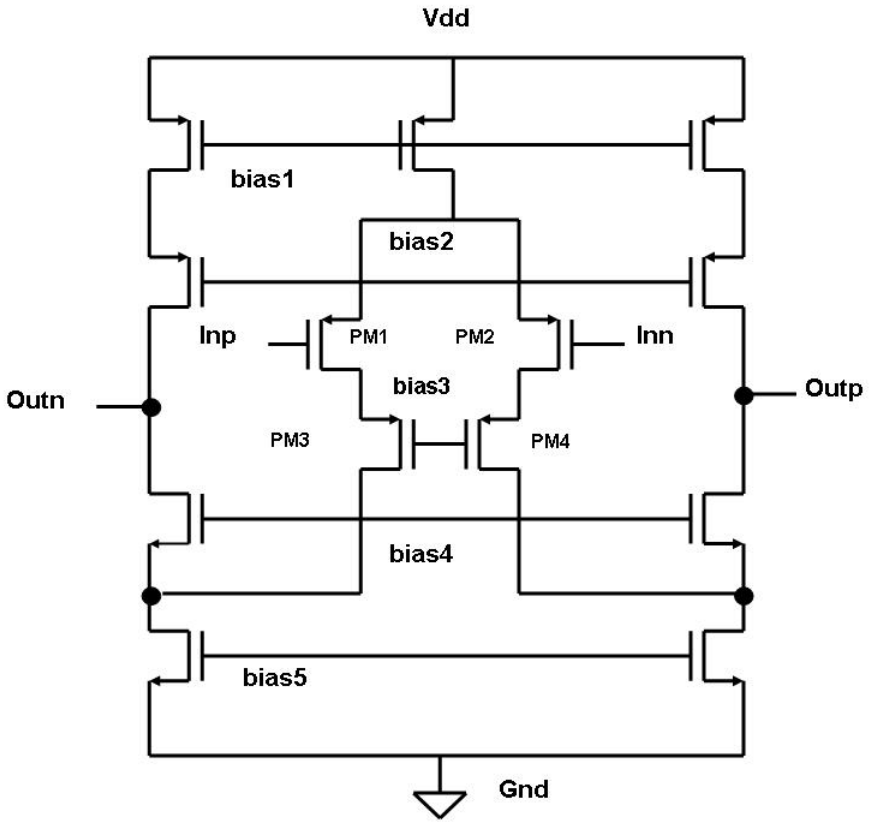


Figure 6.14: First integrator opamp circuit diagram

requirements for the opamp. Simulated opamp DC gain for the integrator opamp is 85dB and unity gain bandwidth is 90MHz. The performance summary of the first integrator opamp is shown in Table 6.1.

6.1.4 Common mode feedback circuit design

For fully differential circuit, a common mode feedback circuit is normally needed to control the common mode voltage of the integrator output. A switched capacitor common mode feedback [48] circuit is used in this design to reduce power consumption. A switched capacitor common mode feedback circuit diagram is shown in

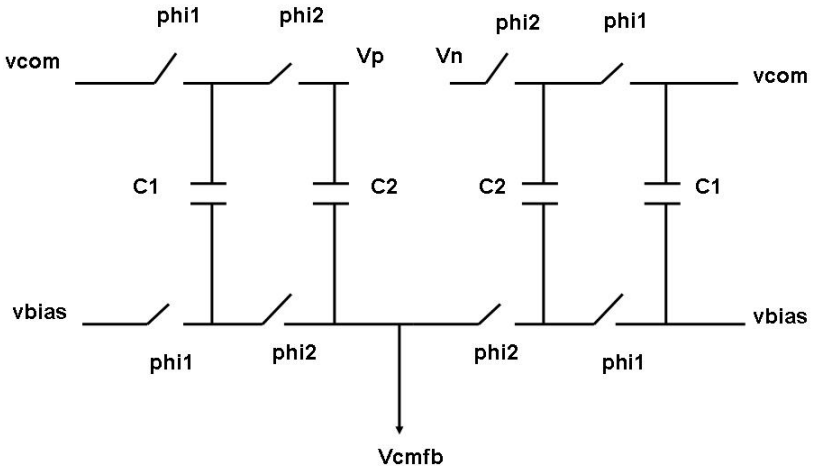


Figure 6.15: Switched capacitor common mode feedback circuit diagram

Integrator 1 opamp	DC gain	Bandwidth	Phase margin	Power consumption
	85dB	90MHz	68 degree	65mW

Table 6.1: Integrator 1 opamp performance summary

Figure 6.15. Signal V_p, Vn are the fully differential integrator output. During phase 1, capacitor C_1 samples the difference between the intended common mode voltage and bias voltage. During phase 2, electric charges from C_1 is transferred to capacitor C_2 which also samples the integrator output to produce the middle DC point of the output. V_{cmfb} is feedback to the internal opamp of the integrator to control the common mode. All switches are kept minimum to reduce charge injection during the operation.

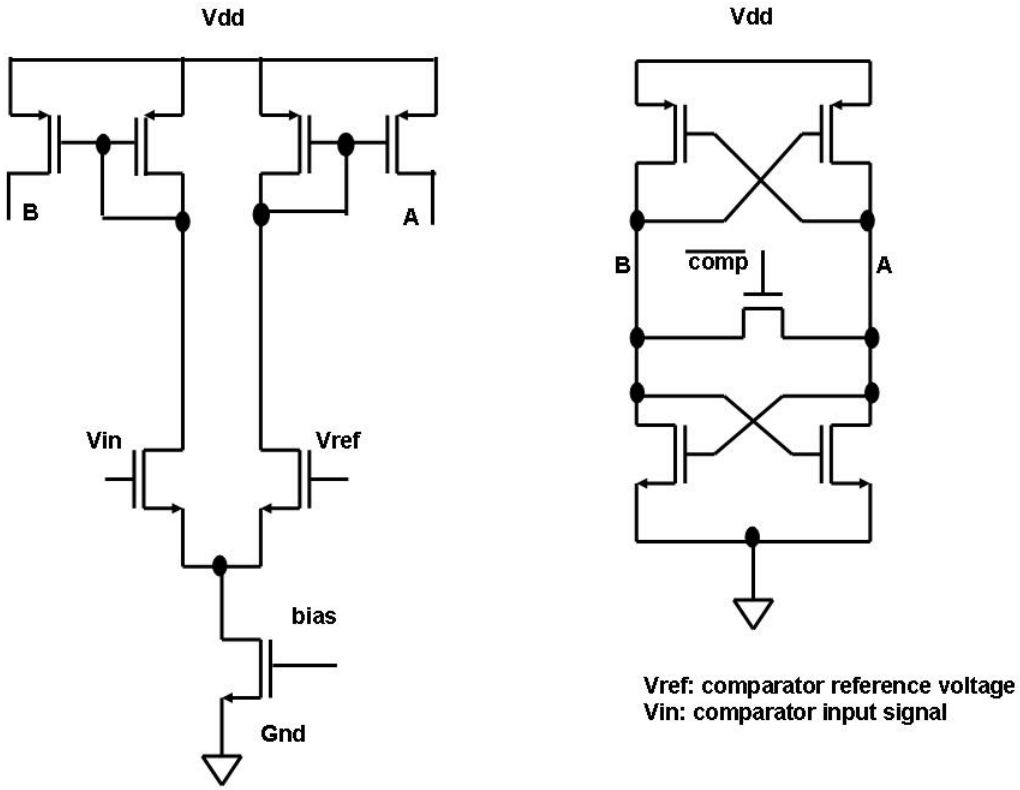


Figure 6.16: Comparator Circuit Diagram

6.2 Comparator Design

Since the quantizer is inside the delta sigma feedback loop, the comparator offsets are largely suppressed. The new dual phase quantization scheme further relaxes the requirements of individual comparator, especially for the comparators in the low resolution phase.

The comparator schematic diagram is shown in Figure 6.16. A current mirror is inserted between the input pair and the output signals to reduce "kick back" energy from the regeneration output stage [47]. Dummy transistors are added around

input pair, current mirror and the regeneration output stage for the three high resolution phase comparators, which help to limit the comparator offset to under 10mV. Simulation indicates that the increase of integrator output swing from 10mV comparator offset in this modulator is negligible. Therefore, no comparator offset cancellation techniques are used in this design to reduce design complexity.

6.3 Summation circuit

In feedforward summation delta sigma architecture, all integrator outputs are summed together at the summation circuit. This summation circuit should not have any "memory" from previous operations, which means the circuit must be reset after each summation operation. This requirement presents an unique dilemma for multi-bit topology. Even each integrator output only changes by a small amount from one clock cycle to another, the summation circuit still needs to provide large slew rate since its output has to be reset to zero after each clock cycle. This internal opamp of the summation circuit also has to drive the input of the following multibit quantizer. The loading capacitor for multibit quantizer with a large number of comparators is non-trivial. Summation circuit with holding capacitor has been proposed to deal with this issue. The circuit diagram is shown in Figure 6.17

During phase 1, capacitor C_s and C_1 are discharged. At the same time, the holding capacitor C_H are connected across the input and output of the opamp to maintain the opamp output value. The holding capacitors are connected between opamp output and common mode voltages. The new opamp output voltage is stored on the holding capacitor after phase 2. Capacitor C_s and C_1 form a switched capacitor gain stage during phase 2. Under this scheme, the summation circuit output changes only be small steps. The main drawback of this approach is the

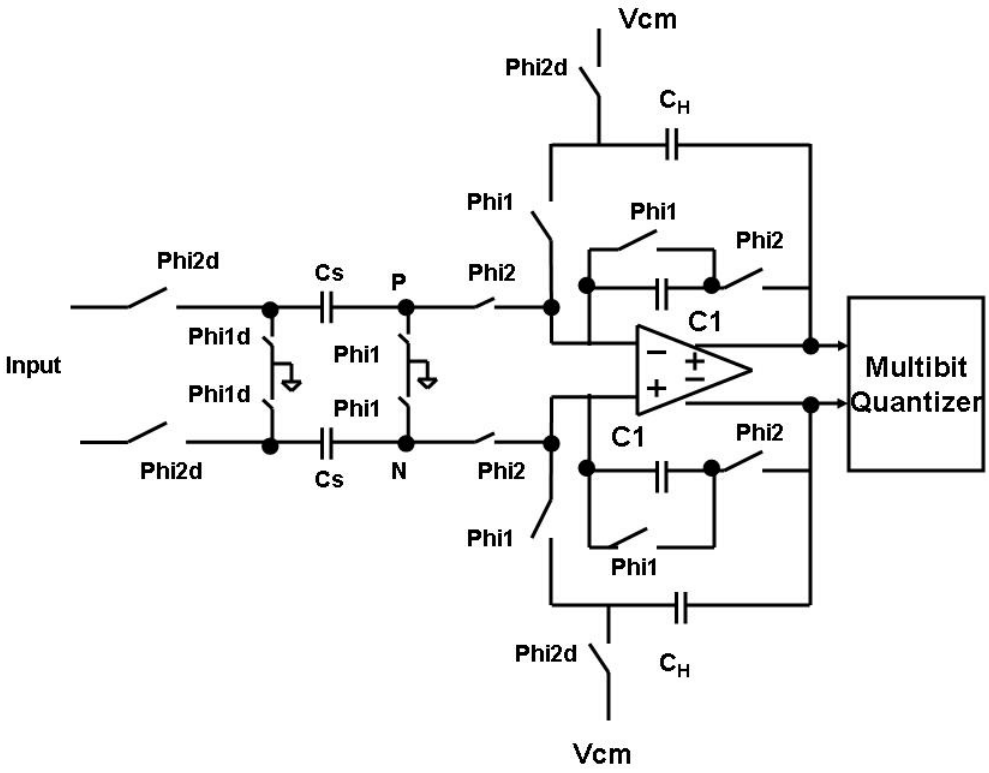


Figure 6.17: Switched capacitor summation circuit with holding capacitor

Summation opamp	DC gain	Bandwidth	Phase margin	Power consumption
	95dB	120MHz	71 degree	15mW

Table 6.2: Summation opamp performance summary

additional circuit complexity.

In our design, the dual phase multibit quantizer scheme reduces the total number of comparator to fifteen and the modified feedforward summation modulator substantially reduces the output swings of all integrators. The summation circuit can be simplified and still achieve the power consumptions target. The summation circuit is shown in Figure 6.18.

During phase 1, capacitor C_{s1} to C_{s5} and C_1 are discharged. The input of the following multibit quantizer is also reset. During phase 2, the circuit again operates as a switched capacitor gain stage.

A second stage opamp is used for the summation stage. The circuit diagram is shown in Figure 6.19. The summation opamp performance is summarized in Table 6.2.

6.4 Dynamic element matching circuit and analog clock diagram

The mismatch among capacitors of the multibit feedback DAC (digital to analog converter) introduces nonlinearity and tones into the converter. This is because such errors are directly added to the input signal and not suppressed by the delta sigma noise shaping. In this design, the capacitors are fabricated in a double poly, low cost digital CMOS process. One possible layout scheme is shown in Figure 6.20 (a). In this scheme, capacitors are placed close to each other to minimize gradient and

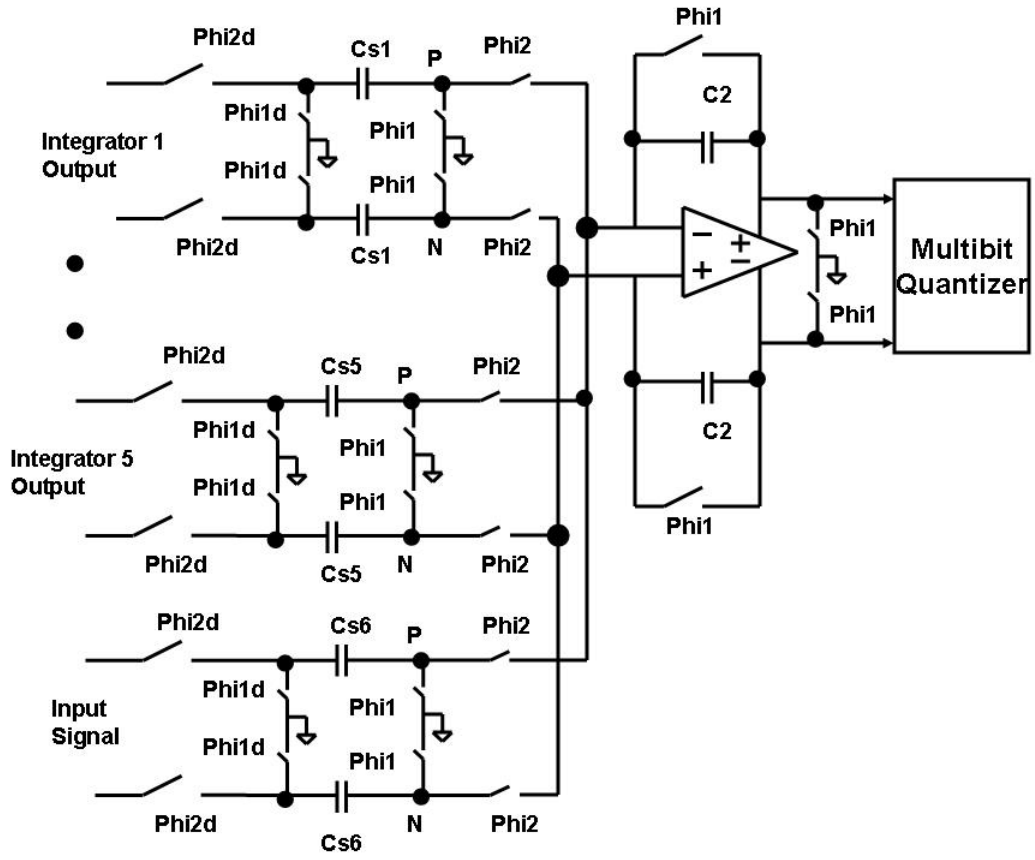


Figure 6.18: Multi-input switched capacitor summation circuit

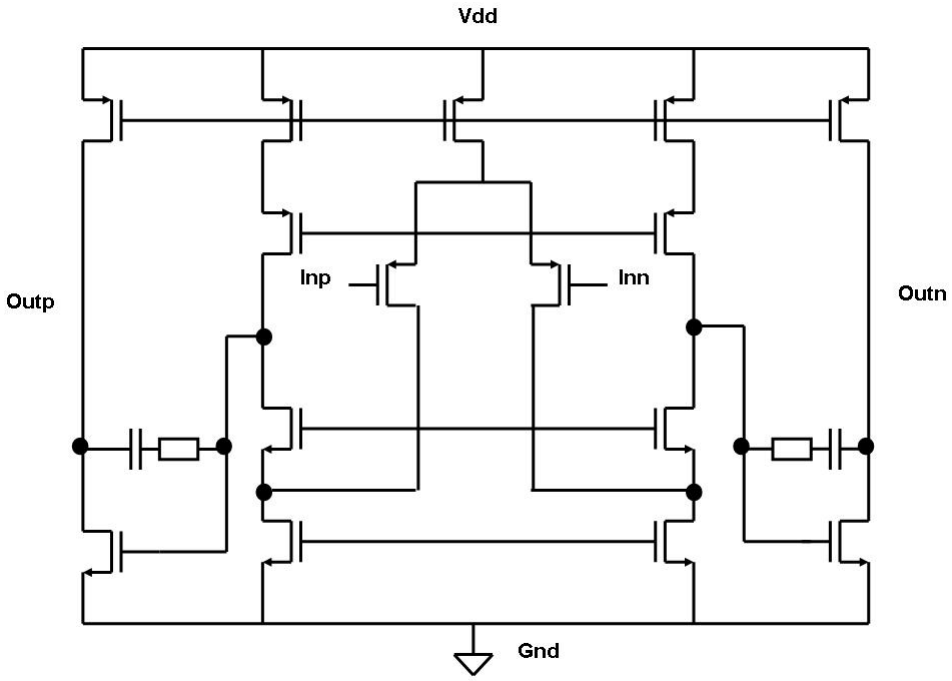


Figure 6.19: Summation circuit opamp

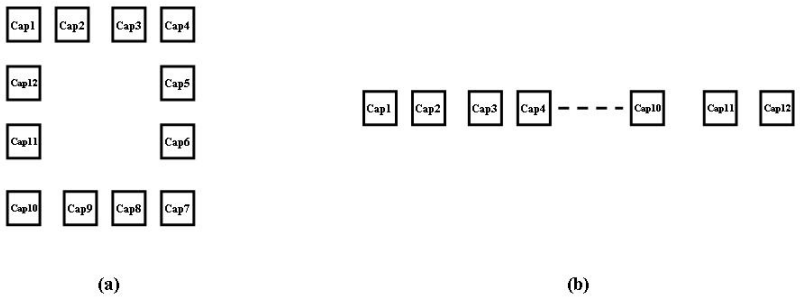


Figure 6.20: Feedback DAC capacitor layout

random process mismatch. However, since there are thirty two pairs of capacitors inside the feedback DAC, such layout scheme occupies large die area and it is very difficult to match the parasitic capacitor introduced by the signal lines to the top and bottom capacitor plates.

The layout scheme used in this design is shown in Figure 6.20 (b). The scheme makes it easier to match parasitic capacitor introduced by the top and bottom plate signal lines and occupies less die area. Furthermore, the feedback DAC itself acts as active shielding to prevent digital noise coupling into rest of the analog blocks. However, such layout scheme introduce large gradient mismatch, which has to be suppressed. For low to medium resolution converter design, using special analog process or various calibration schemes are able to remove such errors. [40] [44] However, both approaches are not sufficient to achieve the performance target of

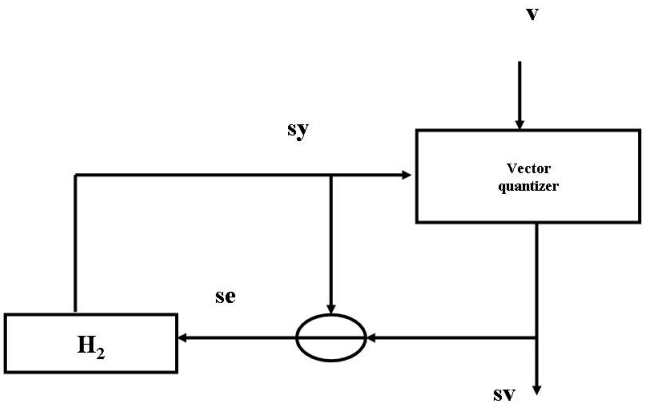


Figure 6.21: Noise shaping dynamic element matching block diagram

this design.

Dynamic element matching circuits have been implemented for high precision design. One popular topology is the data weighted averaging (DWA) [41] [42] [43]. This algorithm scrambles through the feedback capacitors to ensure each capacitor are equally used throughout the operation. Combined with the oversampling nature of the delta sigma modulator, this scheme moves the capacitor error out of the band of interest. However, such periodic scrambling of the capacitor also creates tones inside baseband.

A DEM circuit with second order noise shaping is implemented in this design [38]. The second order DEM is needed to handle the worst-case scenario, with potentially larger than fiver percent gradient mismatch. It also eliminates unwanted signal dependant tones associated with the first order DEM circuit. The noise shaping element matching block diagram is shown in Figure 6.21.

The output sv are the control bits which select individual capacitor inside

feedback DAC. Signal sy represents the ideal usage for each capacitor. The vector quantizer selects capacitor with the largest sy value to minimize the difference between sy and sv. The signal se is then filtered by noise shaping function H_2. In other word, the mismatch error is noise shaped by H_2. By selecting second order noise shaping for $H_2 = (1 - z^{-1})^2$, second order mismatch suppression circuit is implemented for this design. Simulation result of the modulator output with the second order DEM and five percent gradient mismatch among feedback DAC capacitors is shown in Figure 6.22. The signal to noise ratio in this case is 135dB over 20kHz bandwidth.

6.5 Clock generator

The analog clock diagram of the dual phase quantizer with their reset phase is shown in Figure 6.23. The low resolution quantization occurs in the middle of the integration phase. This arrangement creates a time slot to switch in the proper reference voltage and turn on comparators for the high resolution quantization phase. This operation also divides quantization into two phases, which effectively increases the settling time for comparison glitches prior to the critical sampling clock edge. The DEM starts computation after the fine quantization phase is completed.

The clock generator to produce the non-overlapping clock signals are shown in Figure 6.24.

An external fifty percent duty cycle clock is used as the input to the clock generator. The delay cell defines the period length of phase one and phase two. Each clock signal is buffered to achieve roughly equal rising and falling edge across the layout. The clock for the low resolution quantization is generated from the bottom delay cell.

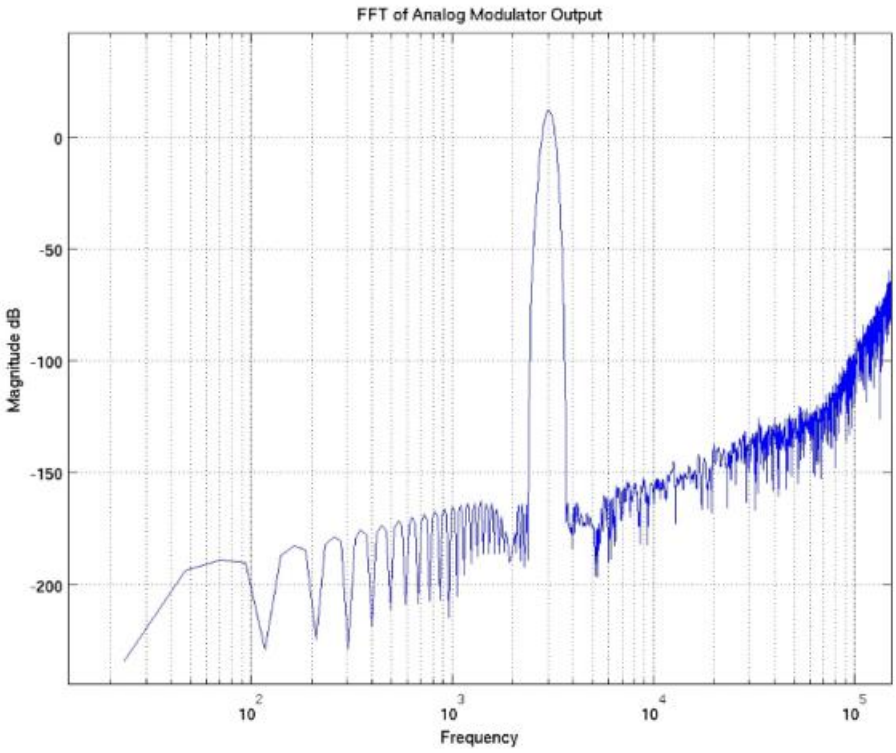


Figure 6.22: Simulated FFT plot of the modulator output with second order DEM and 5 % feedback DAC capacitor mismatch

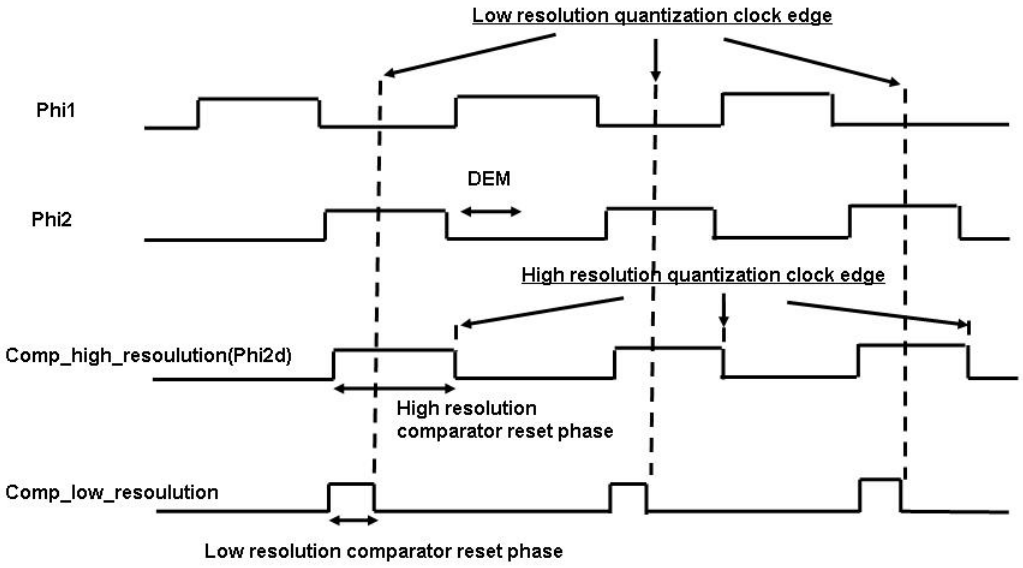


Figure 6.23: Analog clock diagram

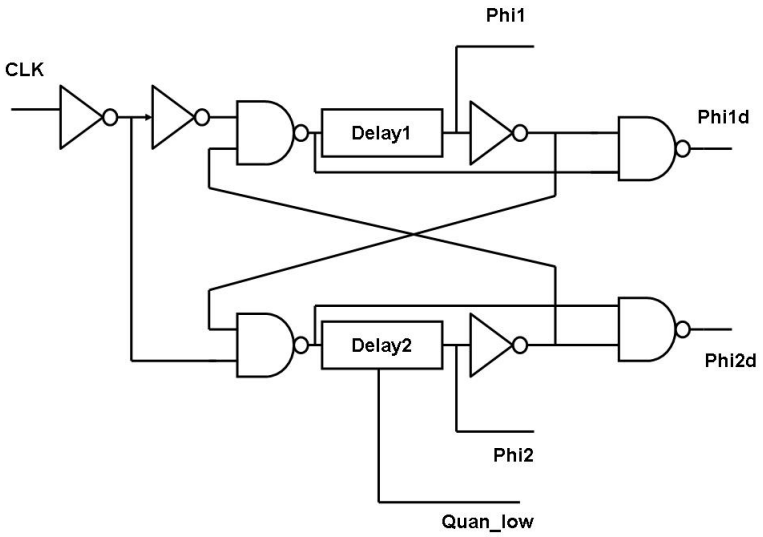


Figure 6.24: Non-overlapping clock generator

6.6 Decimation filter design

For a single die A/D converter design, it is also important to suppress the switching noise of the decimation filter to achieve the ADC performance targets. However, conventional approach requires over 120dB stopband attenuation [49] for the decimation filter which generates a large amount of digital coupling noise inside the single die chip. Such digital coupling noise can easily degrade the overall ADC performance. The adoption of thirty three quantization levels for the analog modulator reduces out-of-band quantization noise energy substantially, which helps to relax stop band attenuation requirement for the decimation filter. An on-chip high pass filter further processes the decimation filter output to remove the DC offset from the analog modulator.

In a conventional multistage comb filter design, an additional circuit is needed to compensate for the passband droop. Halfband filters are used for this design.

Since a halfband filter is flat throughout its passband, the passband droop compensation circuit is eliminated. A transposed form structure is applied to implement the half band decimation filter to reduce memory requirements. The last two stages of the decimation filtering and the high pass filtering are implemented by a fixed point MAC engine. Digital circuit synthesis is optimized to achieve optimum trade off between minimizing worst case delay and digital die area. This linear phase filter is simulated with 100dB stopband attenuation and 0.00015dB passband ripple.

6.7 Top level verification and optimization for mixed signal circuit design

Top level verification and optimization for mixed signal circuit design is normally performed with transistor level simulation after most analog circuit design is completed. However, with the increase of circuit complexities, simulation time for mixed signal circuit verification and optimization takes very long time even with the latest high speed processor. It is not unusual for top level simulations to take over one week, which becomes another bottleneck for high performance mixed signal design.

Verilog behavioral model is introduced for this design. Compared with Matlab model, the Verilog model is established to be more closely resemble the actual switched capacitor operation. On the other hand, eliminating SPICE simulation blocks greatly reduces simulation time. Since the Verilog language can not pass real values between modules, Bitstoreal and Realtobits functions are used to convert real and digital value between each function module. Multiple decisions have to be made before establishing such models. First, the behavioral models need to closely match the actual analog circuit function and performance while limit the model complexities. In other word, it is important to balance the performance of the model and

its complexities to speed up the simulation. Second, the models need to be flexible enough to track possible design changes.

The behavioral model includes the following

1. common mode voltage and offset inside the quantizer module to model the effect of common mode voltage mismatch and quantizer offset.
2. power down and reset signals to model the analog start up sequence.
3. delays to model the analog sub circuit behaviors.
4. mismatch in feedback DAC elements to model the capacitor mismatch.
5. delays introduced by the analog & digital interface operation.

The Verilog behavioral model is also used to verify and optimize the digital filter performance before and after the synthesis. The Verilog behavioral model codes are shown in the attached appendix.

Chapter 7

Circuit Board Design and Chip Layout

Based on the understanding of current flow paths, a resistive macro model [28] [29], which is shown in Figure 7.1, has been established to simulate the effectiveness of substrate coupling noise.

Although the resistive macro model requires much less computation time, it still models nodes across substrate. Information regarding G2, which depends on layout and design, is also only available after the layout is completed. Since larger substrate impedance associated with longer distance in non-epi process provides better isolation between sensitive analog section and digital circuits, non-epi process is selected for this design. We can also make several observations from typical modern mixed signal circuits.

1. Transistors are located on the top layer of the substrate.

2. The resistance of this transistor layer increases with transistor density.

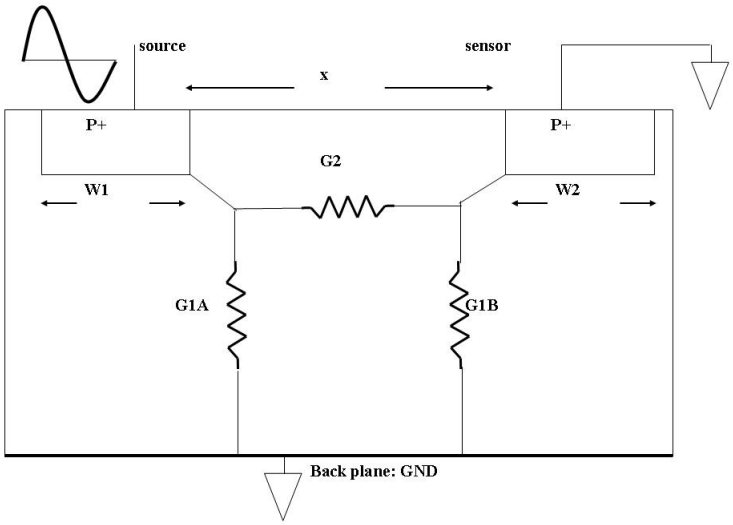


Figure 7.1: Substrate modeling

3. Transistor density is substantiallly different between various blocks such as between analog section, memory cells and common digital blocks.

4. Digital blocks are normally to be the main contributor of signal dependant substrate coupling noise.

5. Digital switching activities/power consumptions differ substantially between each digital circuit block, normally due to operation frequency or function difference.

A 3-D resistive macro model, which is shown in Figure 7.2, is used to study the substrate coupling noise profile in the analog section of baseband applications. R_t represents the top layer and R_b represents the bottom layer substrate resistor. The resistive macro model is composed of top layer resistors, bottom layer resistors and vertical resistors. Bottom and vertical resistors are process dependent. Digital section is composed of three blocks, highly noisy, medium noisy and low

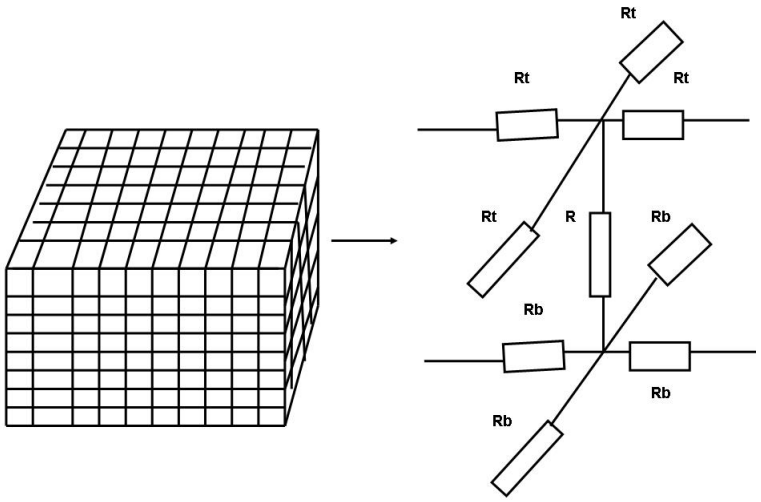


Figure 7.2: 3D resistor macro model

noisy section. These three sections represent typical digital functions seen inside modern digital circuits such as digital filter, memory, digital signal processing etc. Low noisy digital section, which represents memory, is assumed highest transistor density while analog section is assumed lowest transistor density in the simulation. Current pulses are applied to resistor nodes to represent digital activities. Package pin macro model is used in the simulation as well. The search flow is shown in Figure 7.3. The first step is to establish the substrate noise model with information available in the early design stage such as major function blocks, estimated die area and power consumption, clock rate etc. The second step is to compare the coupling noise profile for all possible chip and circuit board layout floor plans. The key motivation of this approach is to compare possible layout floor plans, instead of trying to calculate and model the digital coupling noise energy itself.

The first issue is how to connect the substrate.The conventional wisdom is to connect the substrate to digital ground. The assumption here is noise current

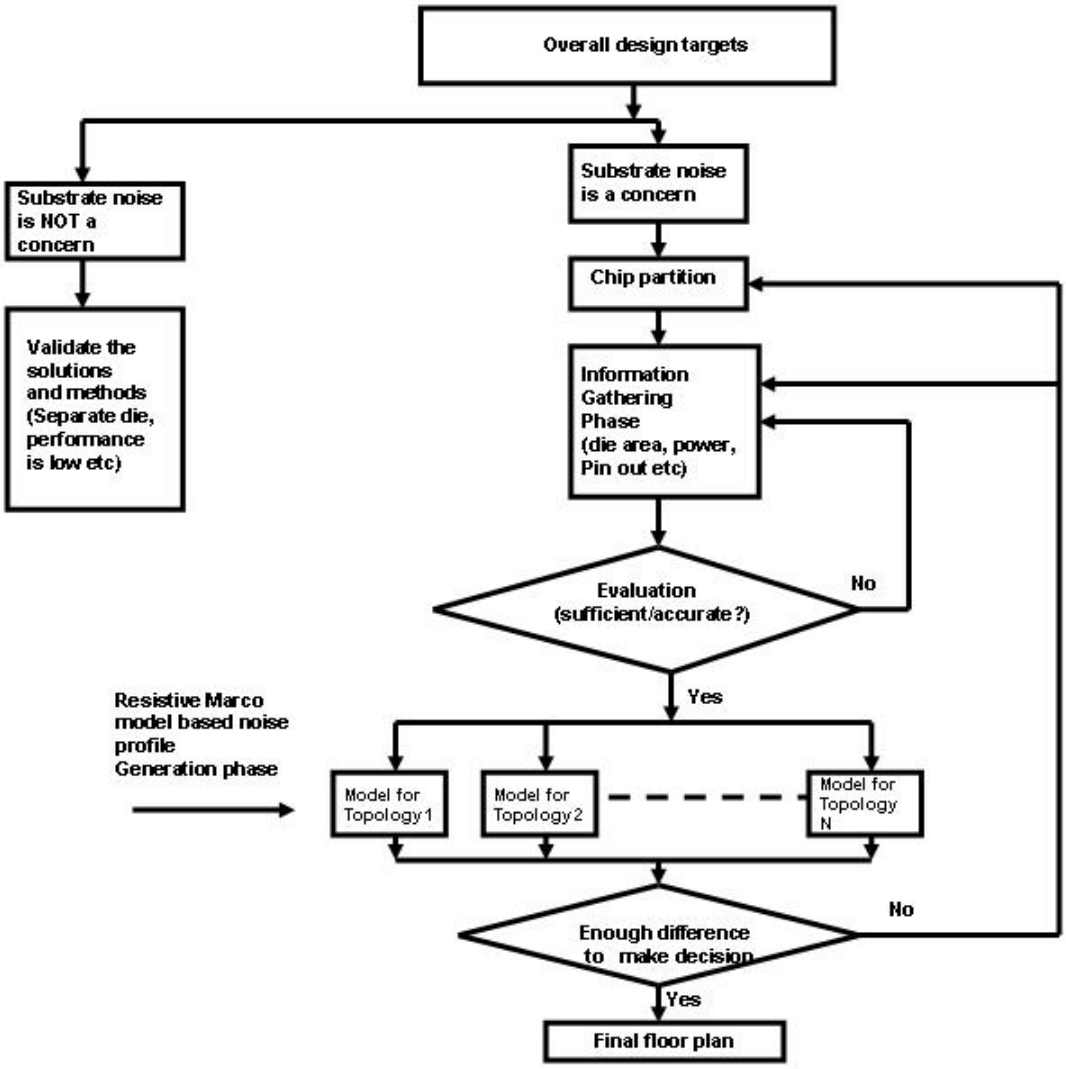


Figure 7.3: Layout floor plan search flow

should always flow to the lowest voltage potential and low impedance points which is the digital ground nearby. The noise current should not flow into analog section. However, analog section continues to experience sever digital coupling noise in such arrangement which indicates the original assumption is not accurate.

By connecting the substrate to digital ground, analog section substrate coupling current profile is shown in Figure 7.4, where section A represents the digital block running on highest clock rate, section B represents the digital block running on medium speed bloc and section C represents the low speed digital block such as memory. Again, only the difference between these two plots is important. The absolute value of coupling current is not irrelevant to the discussion.

Instead of steering the digital coupling current to digital ground, the digital current penetrates deeply into the analog section. The coupling current profile also varies substantially for different digital layout. This matches what people normally observed from silicon measurement.

The original assumption overlooks the transistor density between analog and digital section and among various digital blocks. As shown in Figure 7.5, due to transistor density difference among various circuit blocks, digital coupling currents follow low impedance path into analog section instead of flow to the digital ground directly.

A similar plot with substrate tied to analog ground is shown in Figure 7.6 . The substrate to analog ground connection behaves like a "current collector". Therefore, a current peak can be observed around the connection pin.

Compared with the case in which the substrate is tied to digital group, the coupling current profile variation between different digital floor plan is much smaller. The comparison yield sufficient difference between these two different substrate con-

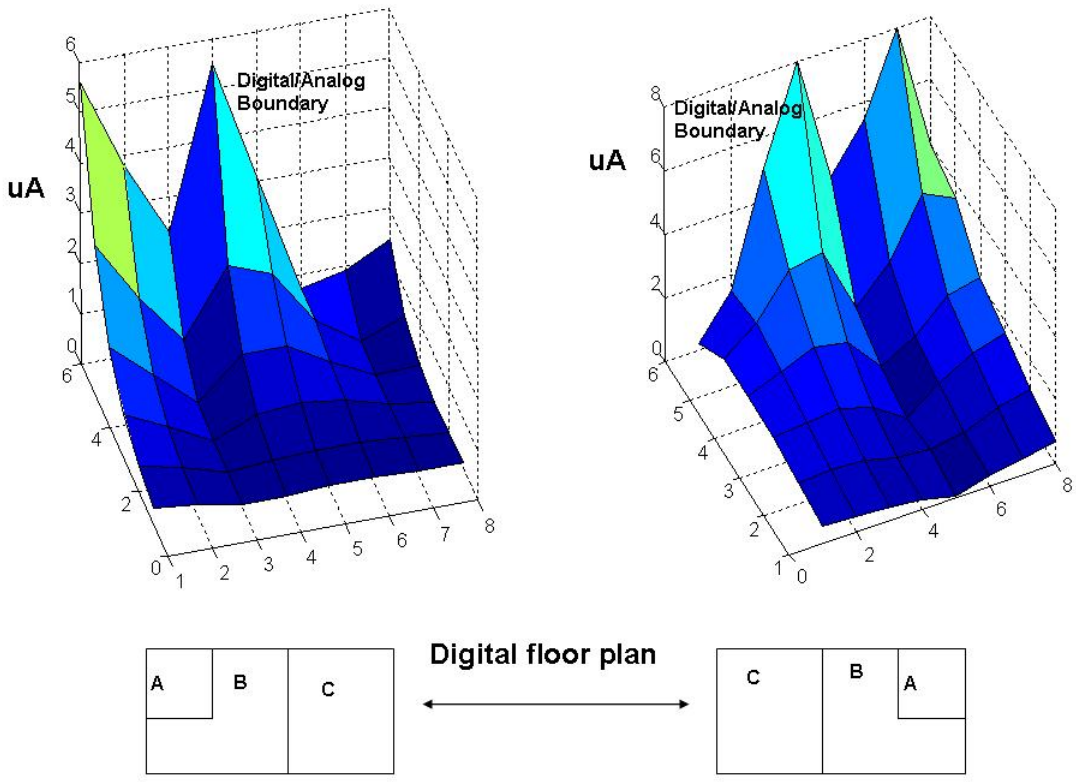


Figure 7.4: Analog coupling noise current profile with substrate tied to digital ground

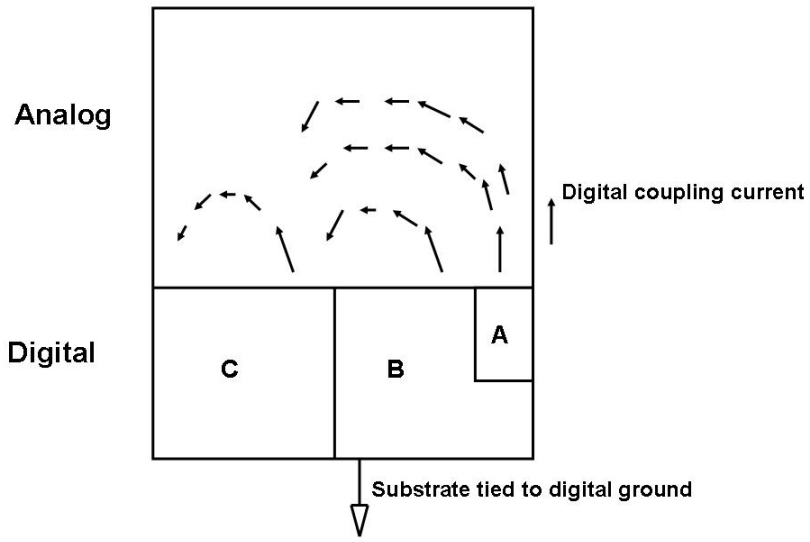


Figure 7.5: Analog coupling current flow for cases of substrate tied to digital ground

nections. This approach is further apply to identify the best digital floor plan for the high precision converter. The result is shown in Figure 7.7.

Contrary to conventional wisdom, highly noisy section A is placed closest to analog section, which is a direct result from the proposed modeling flow. The model also suggests tying analog ground to substrate to minimize substrate noise coupling. Transistor density of the analog section is also normally lower than the digital section since it usually includes redundant metal lines or empty area to protect critical analog blocks. Placing a high energy digital block close to the analog section and tying substrate to analog ground suppresses digital coupling noise by reducing its settling time.Three substrate tie options are pre-arranged in the layout to validate the new model. Option one is tying the substrate to one analog ground. Option two is tying the substrate to two analog grounds on different locations. Option three

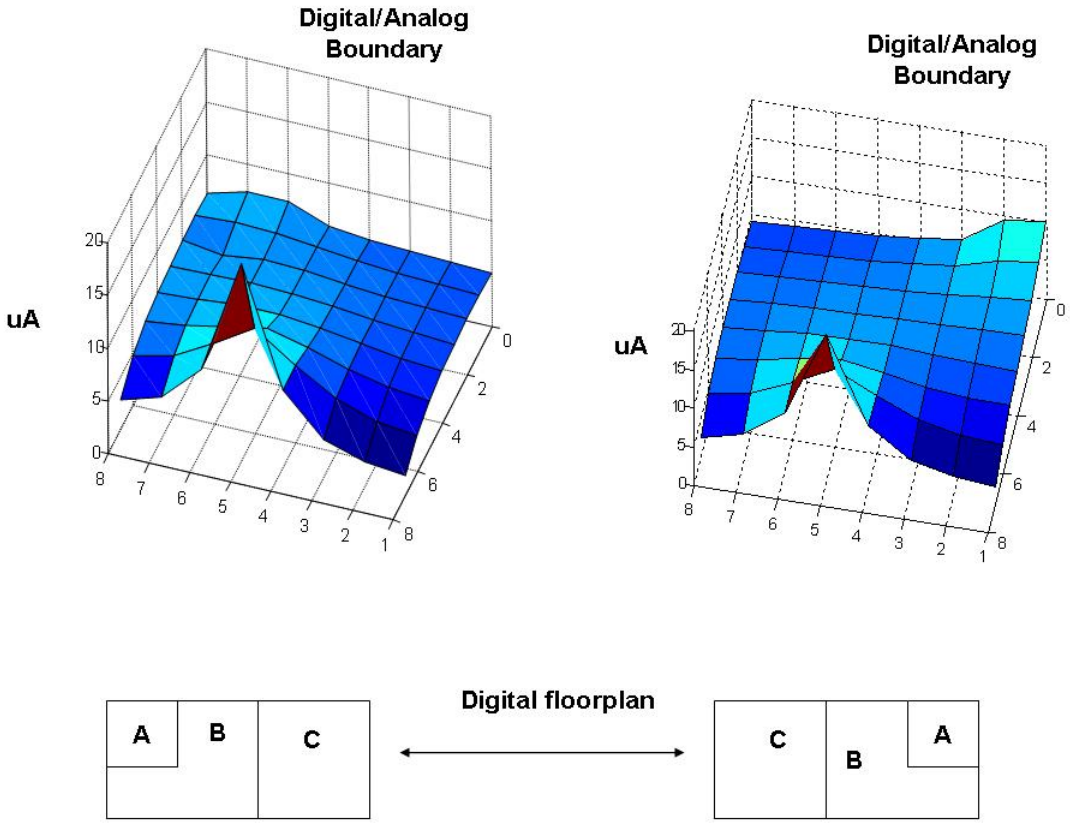


Figure 7.6: Substrate coupling current flow for cases of substrate tied to analog ground

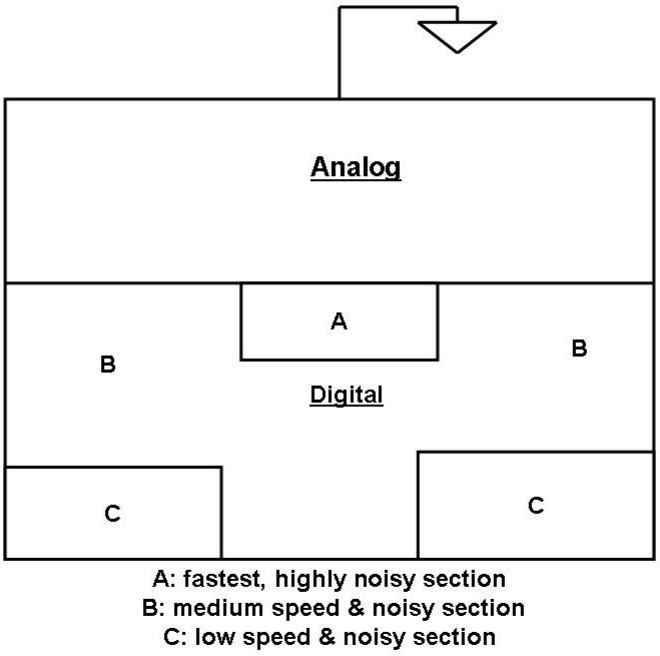


Figure 7.7: Converter digital floor plan and substrate connections

is tying the substrate to digital ground. The measurement results from different substrate connections will be shown in the next chapter.

Since the capacitor size is substantially reduced by techniques shown in previous chapters, this gives more flexility for the analog layout floor planning. The stereo ADC is implemented in a 0.35 μm, double poly, three metal CMOS process. A great deal of attention was given to analog floor planning, which is shown in Figure 8, to achieve compact modulator layout and adequate shielding between sensitive analog nodes and clock lines. The clock generator and digital control circuits for analog section are placed between two analog modulators to minimize clock skew between the channels. The multibit quantizer and digital control circuits for the feedback DAC are placed between the critical first integrator and digital filter circuits to act as "active" shielding for the digital coupling noise. The layout of the first integrator and feedback DAC are fully symmetric, and node parasitic capacitors were carefully minimized through optimal placement of the switches and capacitors adjacent to each integrator's op-amp. The critical reference circuits are placed far away from the analog clock generator and digital circuits. Sensitive nodes such as loop summing junctions and the reference-sampling path were very carefully routed, and shielded from interfering signal. The analog floor plan is shown in Figure 7.8.

Following are several additional descriptions of the floor plan.

1. First integrator and the input sampling network are placed close to the signal pads to minimize the length of bond wire.

2. Reference voltage generation circuits are placed far away from the analog input signals and the digital circuit to minimize coupling noise from the analog and digital section.

3. Clock generation circuit is placed in the middle of the layout and next to the

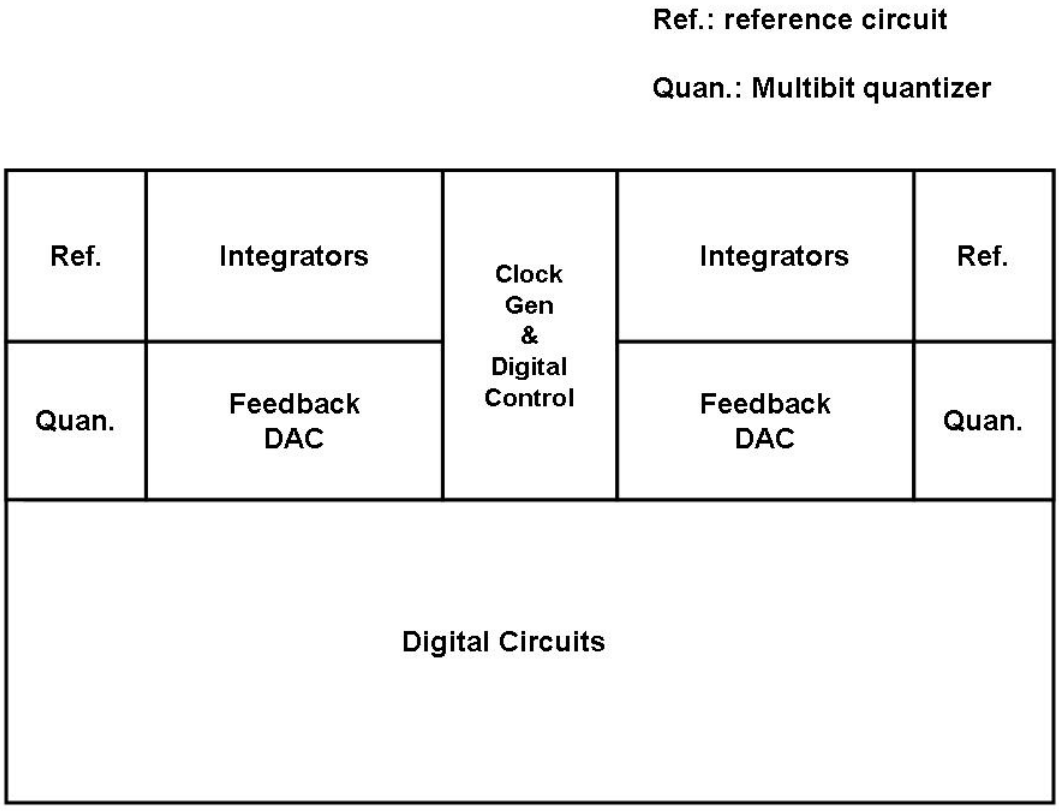


Figure 7.8: Analog section floor plan

critical first integrator to minimize the effect from clock skew.

4. Feedback DAC is placed close to the dynamic element matching circuit(DEM) to minimize delay.

5. Analog ground pads are inserted between the input signal and the reference signals to minimize noise coupling.

Since fully differential structure is used in the design, the layout is carefully matched to to suppress circuit mismatch and coupling noise. Following techniques are used in this design.

1. Dummy devices such as dummy transistor and dummy capacitors are placed around opamp and feedback capacitors to minimize edge effects.

2. Common centroid layout is adopted for opamp input pairs to minimize doping and oxide gradient effects.

3. Input signal lines are shielded to minimize signal coupling to nearby analog blocks. The shielding scheme is shown in Figure 7.9

4. Reference circuit and signal lines are shielded to minimize noise coupling from analog and digital sections.

5. Static digital signals are placed close to analog section to shield again digital coupling noise from pad ring and circuit board

6. The multibit quantizer is shielded to minimize its noise coupling to nearby analog circuits

7. Wider power and ground lines are used for internal circuits to minimize the voltage drop

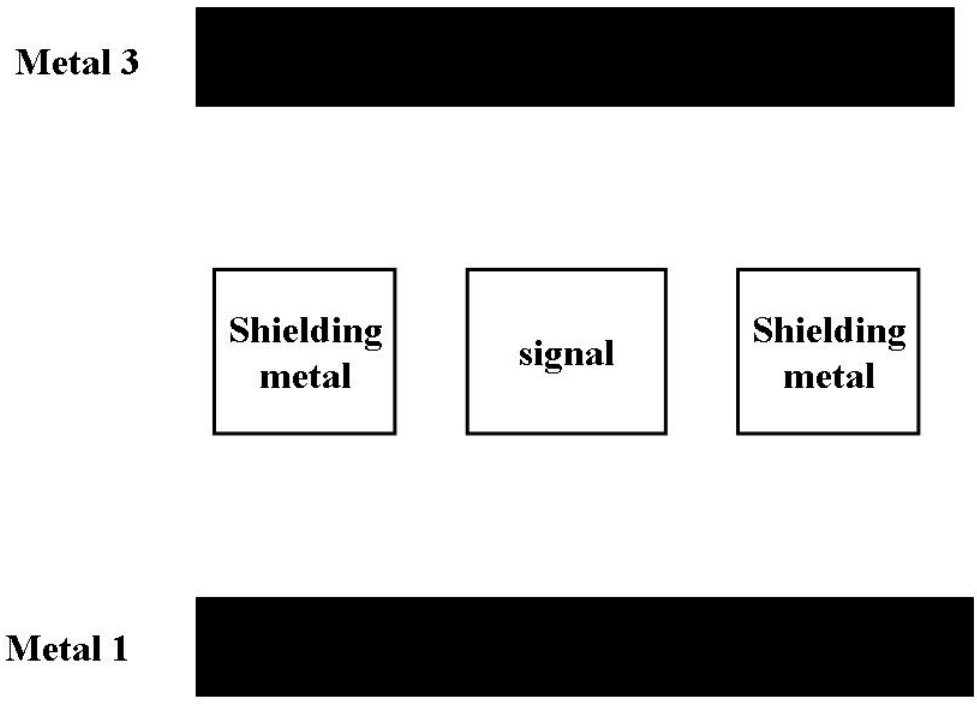


Figure 7.9: Illustration of signal shielding

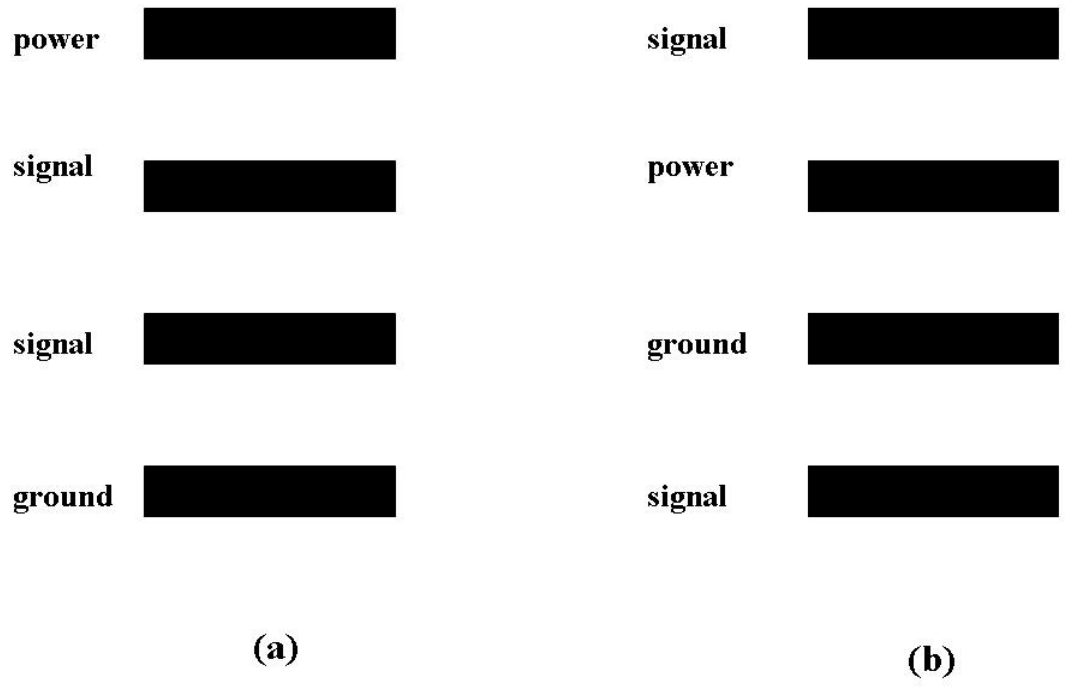


Figure 7.10: Illustration of circuit board layer allocation

8. Instead of connecting substrate contacts to local ground, substrate connections are summed at the dedicated substrate pad

Noise coupling can seriously degrade performance on the circuit board as well. Although it is important to prevent noise coupling on circuit board, it is also important to design the circuit board so that it is practical for real world applications. A four layer board is selected for this design. Two possible circuit board layer allocation schemes are shown in Figure 7.10.

In theory, the scheme shown in Figure 7.10 (a) can best protect the design

again noise coupling. However, it is hard to debug and requires a large number of vias betweens layers. The allocation scheme used in this design is shown in Figure Figure 7.10 (b). Analog signals are placed on the top layer while digital signals are placed on both the top and bottom layer. The same power and ground layer is used for both the analog and digital sections. The scheme is selected as a compromise between performance, debugging process and manufacture cost.

Chapter 8

Chip Fabrication and Measurement Results

The chip was fabricated in a double-poly three metal $0.35\mu m$ digital CMOS process. Transistor matching degrades for small geometry process, which introduces additional errors into conventional flicker noise suppression approaches such as chopper stabilization. Error energy caused by the mismatches among chopping switches can easily affect the performance of high precision converters. On the other hand, low digital library density of a long channel, low 1/f noise analog process substantially raises overall die area and manufacture cost.

Process selection was based on a trade off between design target, design risk and manufacture cost. The die photo is shown in Figure 8.1. Extra analog ground pins are placed around the input and reference signals to provide additional channel isolation. The bandgap and clock generator are placed in the middle to minimize performance differences between stereo channels. Static digital signals are placed next to the analog section while dynamic digital signals are placed far away from

analog signals. No deep N-well and small guard ring is used in this design to further reduce cost and layout complexity. The core die area, which includes the reference voltage circuit and decimation filter is 14.8 mm^2. Total power consumption is less than 330mW.

The total noise contribution from various analog block is shown in Figure 8.2. The total simulated noise voltage is around $3.0047\mu V$ over 20kHz bandwidth.

All measurement results were taken with a 5V analog and 2.5V digital power supply. The test setup is shown in Figure 8.3. Audio precision generates the analog input signal and read back the digital output signal for analysis. A single power supply provides the supply for both the analog and digital section.

The A/D converter achieves 124dB dynamic range (A-weighted), -111dB THD over 20kHz bandwidth. 16384-point FFT plots of -60dB and -1dBFs input signals are shown in Figure 8.4 and Figure 8.5. As shown in Figure 8.4, no tones are observed for -60dBFS input signal. High order harmonics shown in Figure 8.5 are believed to be caused by charge injection from the input sampling network.

1. The A-weighted dynamic range measurement of Figure 8.4 is 124dB over 20kHz bandwidth

2. The THD+N measurement of Figure 8.5 is -110dB over 20kHz bandwidth.

3. The dynamic range measurement of Figure 8.6 is 128dB over 1kHz bandwidth.

4. The Total harmonic distortion(THD) of Figure 8.7 is -114dB over 1kHz bandwidth.

5. The dynamic range measurement of Figure 8.8 is 112dB over 80kHz bandwidth.

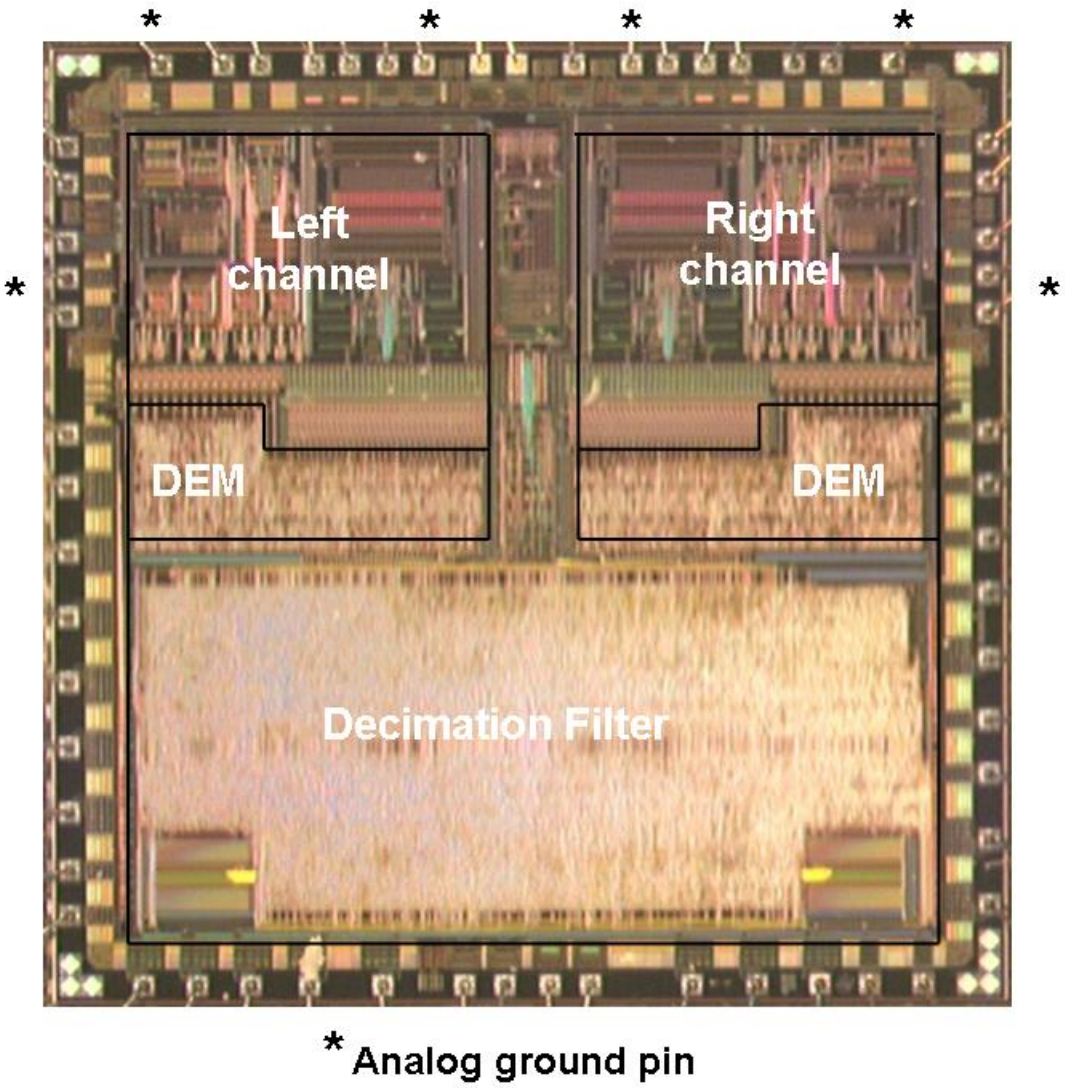


Figure 8.1: Die photo

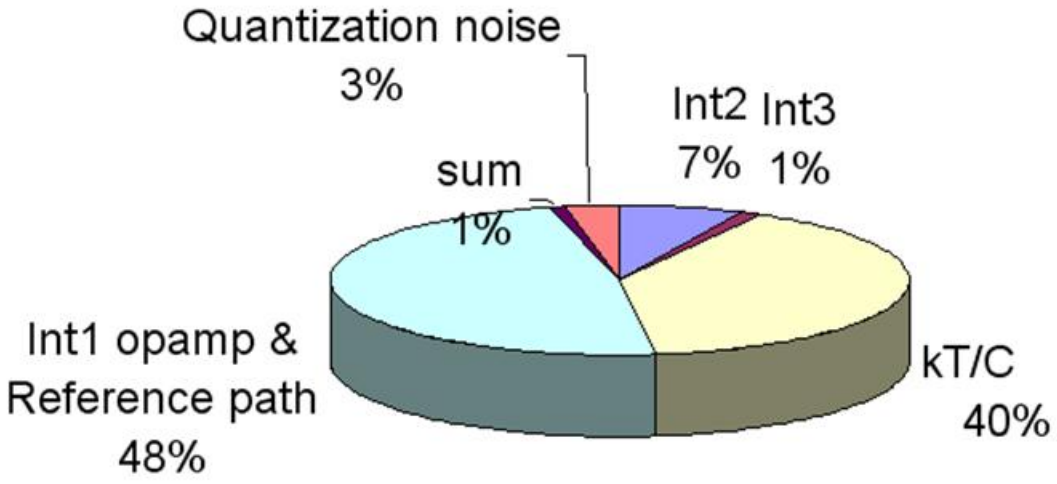


Figure 8.2: Major analog noise sources

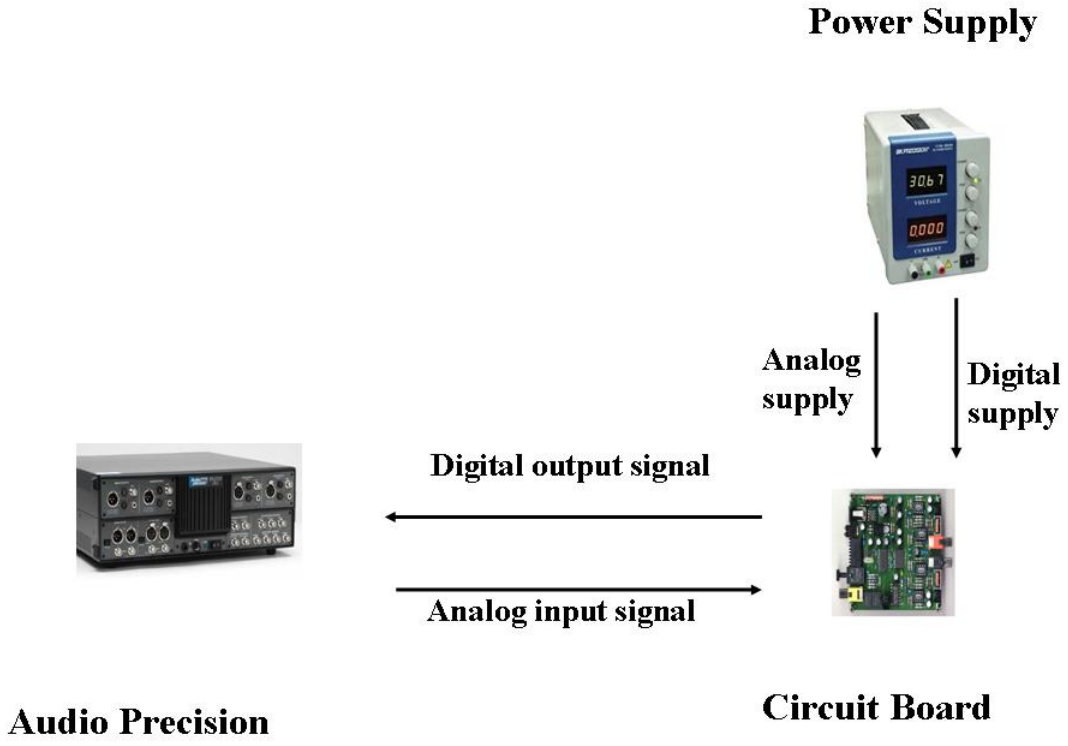


Figure 8.3: Test set up

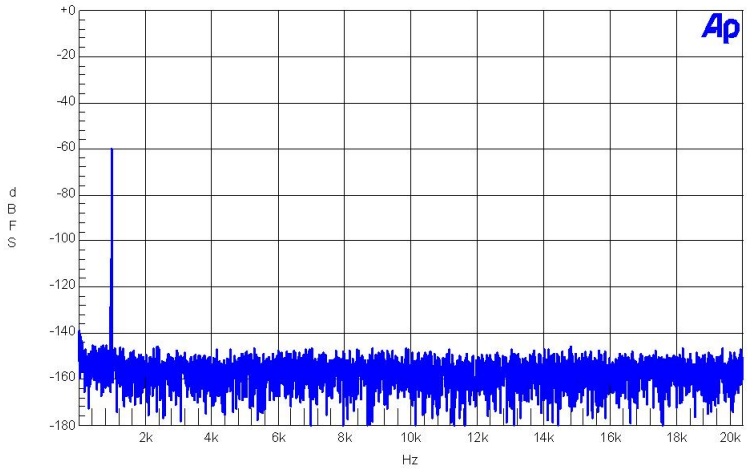


Figure 8.4: FFT plot for -60dBFs 1kHz input signals over 20kHz bandwidth

Signal Bandwidth	20kHz	1kHz	80kHz
Dynamic range	124dB((A-weighted)	128dB	112dB
Distortion	-110dB(THD+N)	-114dB(THD)	-108dB(THD+N)

Table 8.1: Performance measurement summary

6. The THD+N measurement of Figure 8.8 is -108dB over 80kHz bandwidth.

Breakdown of major power consumption sources are shown in Figure 8.11.

The performance measurement summary is shown in Table 8.1.

As shown in Figure 8.10, the worst harmonic when the substrate is connected to digital ground is -102dB, the worst harmonic when the substrate is connected to multiple analog ground is -108dB, and the worst harmonic when the substrate is connected to analog ground is -117dB. The measurement results validate the substrate noise model and analysis shown in previous chapter. Inter-channel isolation for a 1kHz full scale input signal is shown in Figure 8.12 while the inter-channel isolation across the audio signal band is shown in Figure 8.13. This stereo ADC

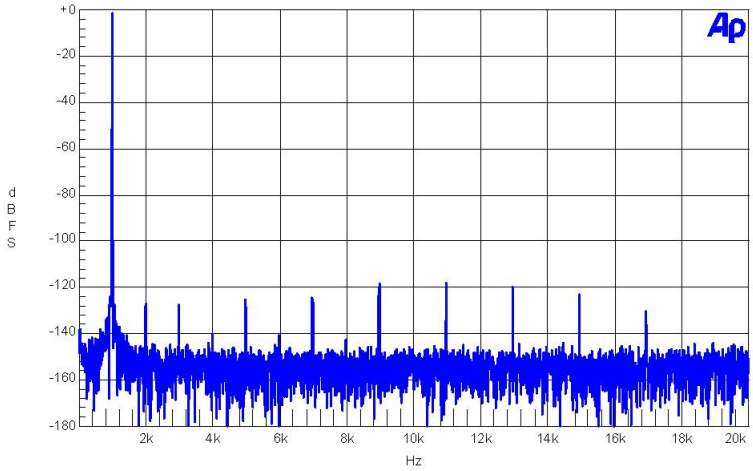


Figure 8.5: FFT plot for -1dBFs 1kHz input signals over 20kHz bandwidth

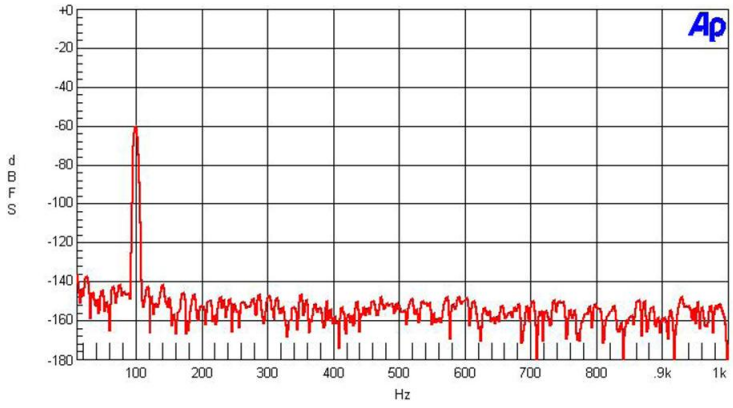


Figure 8.6: FFT plot for -1dBFs 100Hz input signals over 1kHz bandwidth

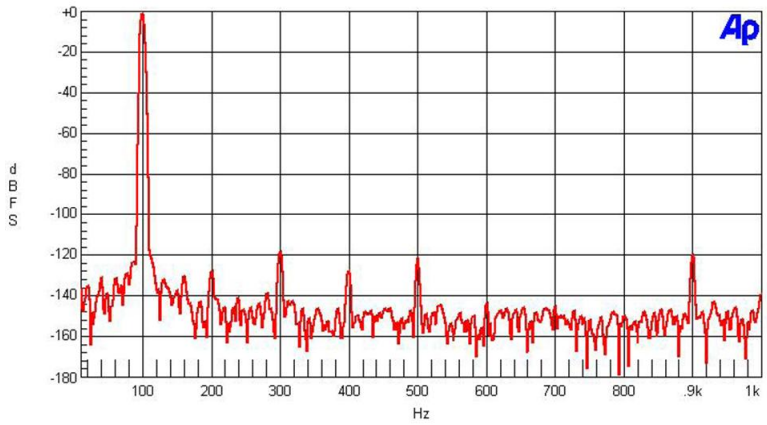


Figure 8.7: FFT plot for -1dBFs 100Hz input signals over 1kHz bandwidth

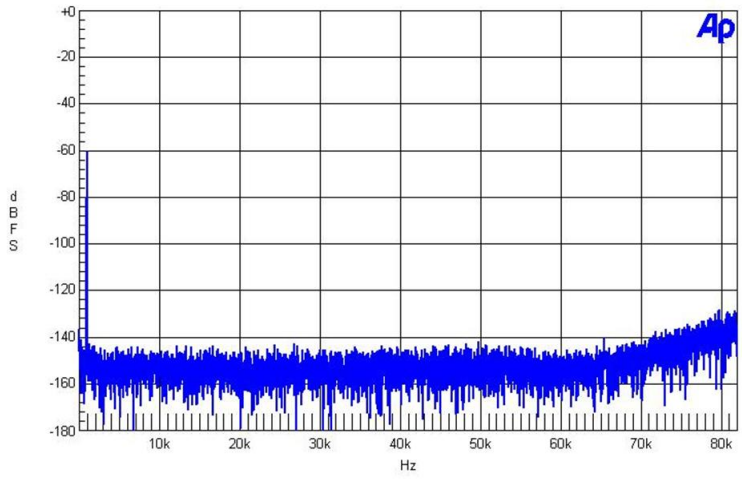


Figure 8.8: FFT plot for -60dBFs 1kHz input signals over 80kHz bandwidth

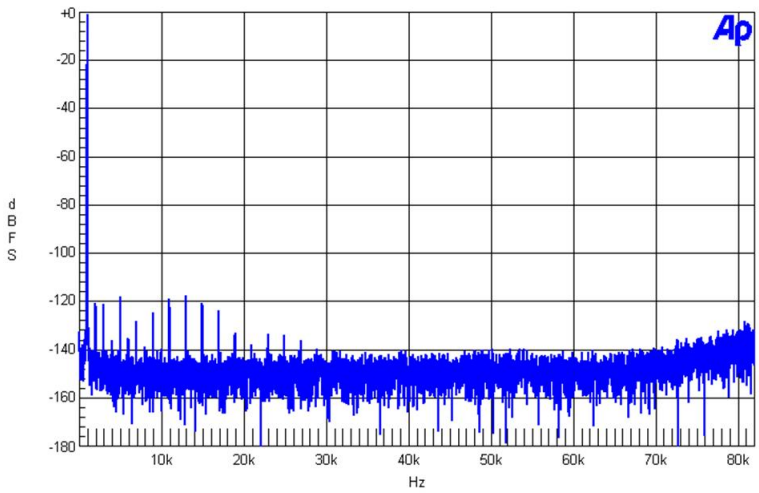
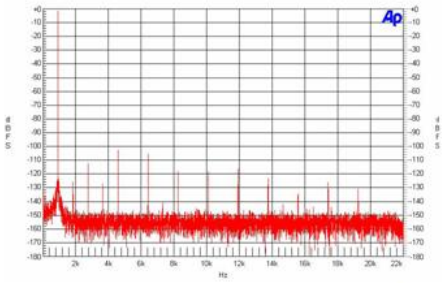


Figure 8.9: FFT plot for -1dBFs 1kHz input signals over 80kHz bandwidth

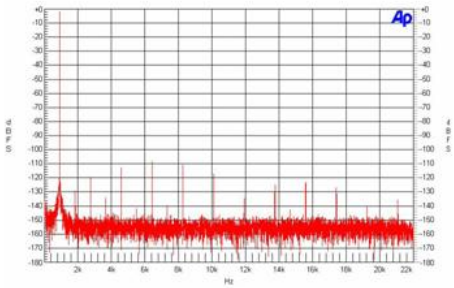
achieves better than 130dB inter-channel across the signal band and over 140dB channel isolation for 1kHz full scale input signal. This result indicates that, contrary to the common design practice which places emphasis on layout techniques such as using large guard ring or deep N-well etc. to handle coupling noise, the more effective and die area efficient approach is to focus on reducing signal depend energy generated inside the chip.

Major specifications of this high precision stereo analog to digital converter is shown in Table 8.2.

Substrate tied to digital ground



Substrate tied to multiple analog grounds



Substrate tied to analog ground

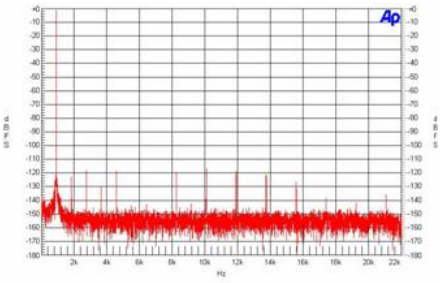


Figure 8.10: FFT plot for -1dBFs 1kHz input signals with various substrate connections

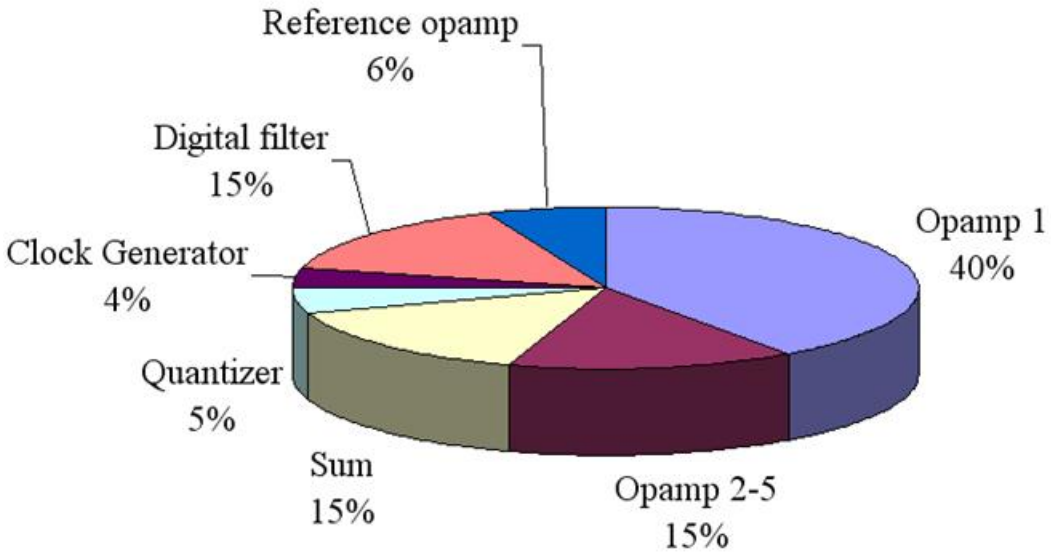


Figure 8.11: Breakdown of major power consumption sources

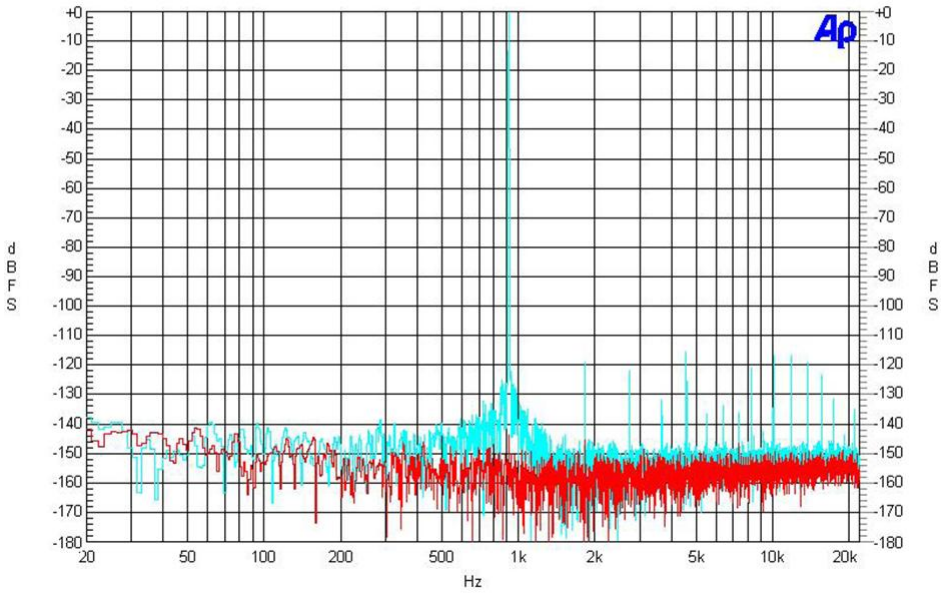


Figure 8.12: Interchannel isolation measurement for 1kHz full scale input signal

Technology	$0.35\mu m$ double poly, triple metal
Core die area	$14.8mm^2$
Analog power supply	5V
Digital power supply	2.5V
Full scale input range	$2V_{rms}$(fully differential)
Dynamic range	124dB((A-weighted) over 20kHz bandwidth
Dynamic range	128dB over 1kHz bandwidth
Dynamic range	112dB over 80kHz bandwidth
Dynamic rang	108dB over 100kHz bandwidth
Distortion	-110dB(THD+N) over 20kHz bandwidth
Distortion	-114dB(THD) over 1kHz bandwidth
Distortion	-108dB(THD+N) over 80kHz bandwidth
Distortion	-107dB(THD+N) over 100kHz bandwidth
Total Power Consumption	330mW

Table 8.2: Stereo A/D converter summary

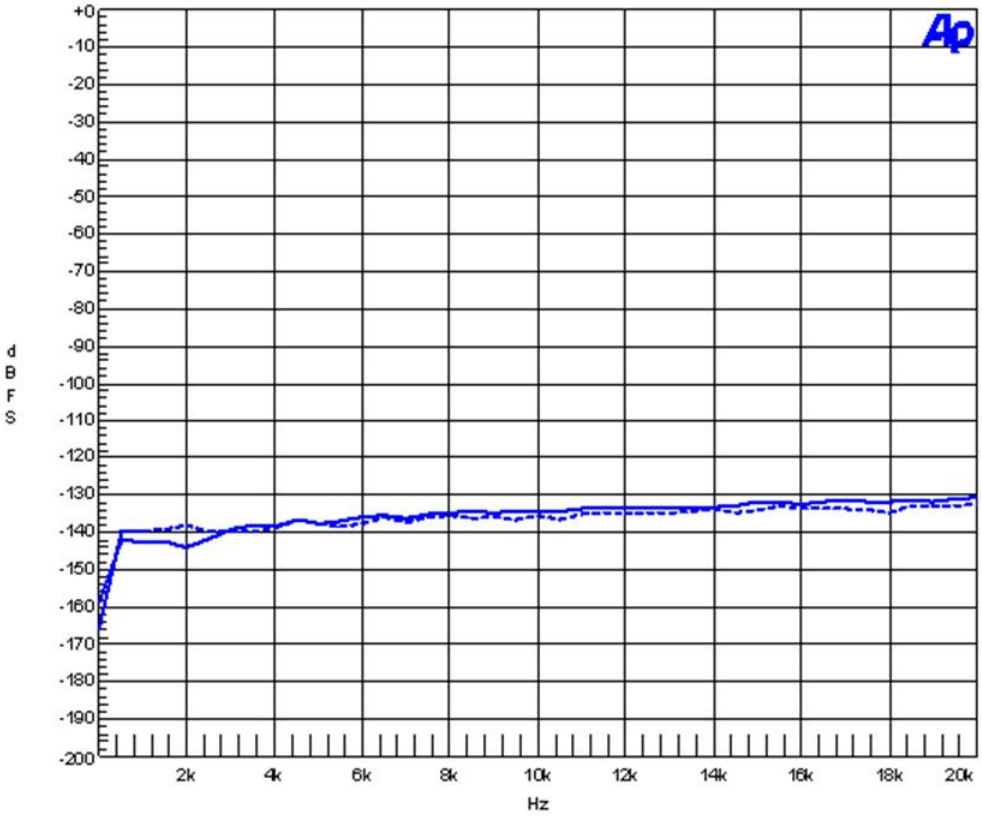


Figure 8.13: Interchannel isolation measurement across audio signal band

Chapter 9

Conclusions and future work

9.1 Conclusions

This work studied single die, high preformance, high power, die area and circuit board area efficient multi channel analog to digital sigma delta converter design for high precision measurement and professional audio applications. Beside achieving targeted performance, the work also studied challenges which are critical for modern day mixed signal design, such as reducing inter channel interference and overall system level cost. Our research is mainly focused on system level approaches, instead of circuit level methods, to relax requirements for the fabrication process, sub-circuit and circuit board design etc., to improve the efficiency of the overall data acquisition system.

The research results can be summarized as follows.

1. Our research analyzed the system level requirements for modern day high precision multi channel data acquisition systems to develop the criteria for the high precision data converters.

2. Our research studied the impact of circuit nonideality to delta sigma modulator performance, die area and power consumption. The criteria for optimal high precision delta sigma modulator is developed.

3. Our research studied various data conversion approaches and delta sigma topologies to design an optimal delta sigma modulator.

4. Our research studied circuit and board layout techniques for mixed signal, high precision design.

5. Our research designed a single die, high performance, high power efficient stereo delta sigma ADC is designed. Multiple techniques are applied in the analog and digital circuits to suppress noise coupling within the analog modulator and from digital switching activities, and to optimize performance, limit die area and power consumption. A single loop, fifth-order, thirty-three level delta-sigma analog modulator with positive and negative feedforward paths is implemented. An interpolated multilevel quantizer with unevenly weighted quantization levels replaces a conventional 5-bit flash type quantizer in this design. Integrated with an on-chip bandgap reference circuit and decimation filter, the ADC achieves 124dB dynamic range (A-weighted), -111dB THD over 20kHz bandwidth, 128dB and 108dB dynamic range over 1kHz and 80kHz bandwidth. Inter-channel isolation is 130dB across the audio signal band, and over 140dB for a 1KHz full scale input signal. Total power consumption is less than 330mW.

9.2 Possible Future Work

Improving performance and robustness, increasing system level integration while suppressing power consumption is a common challenge for modern day mixed signal circuit design. Our research demonstrated a system level approach to the multibit delta sigma topology and the switched capacitor circuit design. This research can be further extended to the following areas.

1. Apply the new approach to low voltage design.

   Since the modified modulator design lower the maximum integrator output swings to under 1V, current design can be extend to low voltage supply to further improve power efficiency.

2. Apply the new approach to advanced digital process.

   Circuit noise is suppressed in this design through various architecture level approaches. This scheme can be apply to advanced digital process, which normally has degraded noise performance, to improve analog performance while maintaining the high digital circuit routing density.

3. Apply the new approach to Digital to Analog converter (DAC) design

   The theory can be applied to improve the performance and power efficiency of high precision Digital to Analog (DAC) converter.

4. Improve analog performance in the mixed signal design environment

   Various design and layout approaches are applied in this design to suppress analog and digital coupling noise. Similar approaches can be applied to Digital to Analog converter (DAC) and Codec designs.

APPENDIX

1. Bias signal, power down and reset signals are introduced to model the circuit start up and power down sequence. The signal p and n are used to model the signal from the feedback DAC. Double sampled scheme is also included in the model

2. Verilog behavioral model for the down stream integrator with and without zero are attached

3. Verilog behavioral model for the summation which includes the feedforward path and dither signal

4. Verilog behavioral model for the feedback DAC which includes capacitor mismatch model

```
module int1 (outn1, outp1, ibias, inn1, inp1, pdn, phi1, phi1d, phi2, phi2d , rst,
vcm, p, n, outd_ideal,a);

    output [63:0] outn1, outp1, inn1, inp1
    input ibias, pdn, rst
    input phi1, phi1d, phi2, phi2d

    input [63:0] vcm, p, n,a

    input [63:0] outd_ideal;

    reg [63:0] outn1, outp1;

real vind,vindx,voutd,outp1_real,outn1_real, vinfb_sc; integer
infile; real input_real; integer outfile; real output_real;

initial
 begin
   vind=0.0; vindx=0.0;voutd=0.0;outp1_real=0.0;outn1_real=0.0;vinfb_sc=0.0;
 end

always @(pdn or ibias) begin
 if (pdn || ~ibias)
  begin
   assign outp1=64'bz, outn1=64'bz;
  end
 else
  begin
   assign outp1=$bitstoreal(vcm), outn1=$bitstoreal(vcm);
  end
end

always @(rst)
 begin
  if ((pdn || ~ibias))
   begin
    assign outp1=64'bz, outn1=64'bz;
   end
  else
   begin
    $display(" int1 amp powered up \n");
    assign outp1=$bitstoreal(vcm), outn1=$bitstoreal(vcm);
   end
 end
```

Figure 9.1: Verilog behavioral model of first integrator, section 1: initial conditions and start up

```
always @(posedge phi1)

 #10
 begin
  if (~rst && ibias && ~pdn)
   begin
    vindx =$bitstoreal(inp1)-$bitstoreal(inn1);
    input_real=vind;
    zdx_real=$bitstoreal(zp)-$bitstoreal(zn);
   end
 end


always @(posedge phi2 ) begin
   #5
   Begin
   vinfb_sc=$bitstoreal(p)-$bitstoreal(n);
   output_real = vinfb_sc;

   if (~rst && ibias && ~pdn)
    begin
      //double sample input
      vind=$bitstoreal(inp1)-$bitstoreal(inn1)+vindx;
      input_real=vind;

       voutd=(vind-vinfb_sc)*($bitstoreal(a))+voutd;

      outp1_real=voutd*0.5+$bitstoreal(vcm);
      outn1_real=voutd*-0.5+$bitstoreal(vcm);
      assign outp1=$realtobits(outp1_real);
      assign outn1=$realtobits(outn1_real);
    end

   end

end

endmodule
```

Figure 9.2: Verilog behavioral model of first integrator, section 2: Phase 1 and Phase 2 operations

```
module int( inn, inp, ibias, pdn, phi1, phi1d, phi2, phi2d, rst, outn, outp,vcm,a);

input ibias, pdn,rst, phi1, phi1d, phi2, phi2d;
input [63:0] inn, inp, vcm, a;
output [63:0] outp, outn;

real inn_real, inp_real, ind_real, outd_real,outp_real, outn_real;

reg [63:0] outp, outn;

initial
 begin
  inn_real = 0.0; inp_real = 0.0; outp_real=0.0; outn_real=0.0; ind_real=0.0;
  outp = 64'h0; outn = 64'h0;
 end

always @ (posedge phi1)
        #15
          begin
         inn_real = $bitstoreal(inn); inp_real = $bitstoreal(inp);
        end

always @ ( posedge phi2 )
 begin
  if(!pdn & ibias)
   begin
    if (!rst)
     begin
      ind_real=inp_real-inn_real;
      outd_real=outd_real + $bitstoreal(a)*ind_real;

      outp_real = 0.5*outd_real + $bitstoreal(vcm);
      outn_real = -0.5*outd_real + $bitstoreal(vcm);
      assign outp=$realtobits(outp_real);
      assign outn=$realtobits(outn_real);
     end
    else
     begin
      outp_real = 0.0; outn_real = 0.0;
     end
    outp=$realtobits(outp_real); outn=$realtobits(outn_real);
   end
 end

endmodule
```

Figure 9.3: Verilog behavioral model of down stream integrator without zero feedback path

```
module int( inn, inp, ibias, pdn, phi1, phi1d, phi2, phi2d, rst, zn,
                zp, outn, outp, vcm, a, az);

input ibias, pdn, rst, phi1, phi1d, phi2, phi2d;
input [63:0] inn, inp;
input [63:0] zp, zn, vcm, a, az;
output [63:0] outp, outn;     reg [63:0] outp, outn;

real inn_real, inp_real; zp_real, zn_real; outp_real, outn_real; ind_real, zd_real, outd_real;

initial
 begin
  outp_real=0.0; outn_real=0.0;
  zp_real=0.0; zn_real=0.0; inn_real=0.0; inp_real=0.0; ind_real=0.0; zd_real=0.0;
outd_real=0.0; outp = 64'h0; outn = 64'h0;
 end

always @ (posedge phi1)
     begin
          inn_real = $bitstoreal(inn);
        inp_real = $bitstoreal(inp);
     end

always @ ( posedge phi2 )
 begin
  if(!pdn & ibias)
   begin
    if (!rst)
     begin
      #5
      ind_real = inp_real - inn_real;
      zn_real  = $bitstoreal(zn); zp_real  = $bitstoreal(zp); zd_real = zp_real -zn_real;
      outd_real = outd_real+$bitstoreal(a)*ind_real-$bitstoreal(az)*zd_real;
      outp_real = 0.5*outd_real + $bitstoreal(vcm);
      outn_real = -0.5*outd_real + $bitstoreal(vcm);
      assign outp=$realtobits(outp_real); assign outn=$realtobits(outn_real);
     end
    else
     begin
      outp_real = 0.0; outn_real = 0.0;
     end
    outp=$realtobits(outp_real); outn=$realtobits(outn_real);
   end
 end

endmodule
```

Figure 9.4: Verilog behavioral model of down stream integrator with zero feedback path

```
module summation (dith, dithmag buff_op, buff_on, on1, op1, on2, op2, on3, op3, on4,
op4, on5, op5, rst, ibias, pdn, vcm, phi1d, phi2, phi2d, inp1, inn1, k1, k2, k3, k4, k5,k6);

input dith; ibias; rst, pdn; phi1d, phi2, phi2d;
input [63:0] vcm,k1,k2,k3,k4,k5,k6,dithmag; inp1,inn1; op1,op2,op3,op4,op5;
input [63:0] on1,on2,on3,on4,on5;
output [63:0] buff_op, buff_on;
real op1_real, op2_real, op3_real, op4_real, op5_real; on1_real, on2_real, on3_real,
on4_real, on5_real; inp1_real, inn1_real; buff_op_real, buff_on_real;
real dith; sum, dithmag,k1,k2,k3,k4,k5,k6;
reg [63:0] buff_op, buff_on; wire rst_all = rst | phi1d;
initial
  begin
    inp1_real=0.0; inn1_real=0.0; op1_real=0.0; op2_real=0.0; op3_real=0.0;
    op4_real=0.0; op4_real=0.0; on1_real=0.0; on2_real=0.0; on3_real=0.0;
    on4_real=0.0; on4_real=0.0; sum=0.0; buff_op_real=0.0; buff_on_real=0.0;
    buff_op=64'b0; buff_on=64'b0;
  end
always @ (posedge phi2)
begin
      #25
      inp1_real = $bitstoreal(inp1); inn1_real = $bitstoreal(inn1);
        op1_real = $bitstoreal(op1); op2_real = $bitstoreal(op2);
        op3_real = $bitstoreal(op3); op4_real = $bitstoreal(op4);
        op5_real = $bitstoreal(op5); on1_real = $bitstoreal(on1);
    on2_real = $bitstoreal(on2); on3_real = $bitstoreal(on3);
    on4_real = $bitstoreal(on4); on5_real = $bitstoreal(on5);
        sum= 0.5*((op1_real - on1_real)*$bitstoreal(k1) +
          (op2_real - on2_real)*$bitstoreal(k2) +
          (op3_real - on3_real)*$bitstoreal(k3) +
          (op4_real - on4_real)*$bitstoreal(k4) +
          (op5_real - on5_real)*$bitstoreal(k5) +
          (inp1_real - inn1_real)*$bitstoreal(k6) + dith*$bitstoreal(dithmag));
    buff_op=$realtobits(0.5*sum+$bitstoreal(vcm));
    buff_on=$realtobits(-0.5*sum+$bitstoreal(vcm));
end
always @ (rst_all)
begin
        if(rst_all == 1'b1)
          begin
           buff_op=(vcm); buff_on=(vcm);
      end
end

endmodule
```

Figure 9.5: Verilog behavioral model of summation circuit

```
module quan_mbit(b, phi1d, phi2d, comp, vip, vin, ibias_comp, pdn);

input phi1d, phi2d, comp, pdn; ibias_comp;  input [63:0] vip; vin;
output [31:0] b; real vip_real, vin_real, vind; reg [31:0] b;

initial
   begin
         vip_real=0.0; vin_real=0.0; vind=0.0;
   end
always @ (posedge comp)
begin
if(comp == 1'b1)
  begin
  vip_real = $bitstoreal(vip); vin_real = $bitstoreal(vin); b=32'b0; vind=vip_real-vin_real;
   #30
    if (vind >= 2.79)
          b[31]=1'b1;
    if (vind >= 2.43)
          b[29]=1'b1;
    if (vind >= 2.07)
          b[27]=1'b1;
    if (vind >= 1.71)
          b[25]=1'b1;
    if (vind >= 1.35)
          b[23]=1'b1;

    if (vind >= 0.63)
          b[19]=1'b1;

    if (vind  >= -0.09)
          b[15]=1'b1;

    if (vind  >= -0.81)
          b[11]=1'b1;

    if (vind >= -1.53)
          b[7]=1'b1;
    if (vind >= -1.89)
          b[5]=1'b1;
    if (vind >= -2.25)
          b[3]=1'b1;
    if (vind >= -2.61)
          b[1]=1'b1;
   end
```

Figure 9.6: Verilog behavioral model of multibit quantizer, section 1: low resolution phase quantization

```
#70

    if (vind >= 1.17)
        b[22]=1'b1;
    if (vind >= 0.99)
        b[21]=1'b1;
    if (vind >= 0.81)
        b[20]=1'b1;

    if (vind >= 0.45)
        b[18]=1'b1;
    if (vind >= 0.27)
        b[17]=1'b1;
    if (vind >= 0.09)
        b[16]=1'b1;

    if (vind  >= -0.27)
        b[14]=1'b1;
    if (vind  >= -0.45)
        b[13]=1'b1;
    if (vind  >= -0.63)
        b[12]=1'b1;

    if (vind >= -0.99)
        b[10]=1'b1;
    if (vind >= -1.17)
        b[9]=1'b1;
    if (vind >= -1.35)
        b[8]=1'b1;

         end
endmodule
```

Figure 9.7: Verilog behavioral model of multibit quantizer, section 2: high resolution phase quantization

```
module dac_mbit(p, n,  D, vcm, phi2d, phi2, phi1d,  outd_ideal);


input phi2, phi2d, phi1d; input [63:0] vcm; input [31:0] D;
output [63:0] p, n; outd_ideal;

real mismag;
real mis32, mis31, mis30, mis29, mis28, mis27, mis26, mis25;
real mis24, mis23, mis22, mis21, mis20, mis19, mis18, mis17;
real mis16, mis15, mis14, mis13, mis12, mis11, mis10, mis9;
real mis8, mis7, mis6, mis5, mis4, mis3, mis2, mis1;
real D32_real, D31_real, D30_real, D29_real;
real D28_real, D27_real, D26_real, D25_real;
real D24_real, D23_real, D22_real, D21_real;
real D20_real, D19_real, D18_real, D17_real;
real D16_real, D15_real, D14_real, D13_real;
real D12_real, D11_real, D10_real, D9_real;
real D8_real, D7_real, D6_real, D5_real;
real D4_real, D3_real, D2_real, D1_real, D0_real;
real outd, p_real, n_real,vcm_real;
real level_vol;

reg [63:0] p, n, outd_ideal;
initial
  begin
  D31_real=0.0; D30_real=0.0; D29_real=0.0; D28_real=0.0;D27_real=0.0;D26_real=0.0;
  D25_real=0.0; D24_real=0.0; D23_real=0.0; D22_real=0.0;D21_real=0.0; D20_real=0.0;
  D19_real=0.0; D18_real=0.0; D17_real=0.0; D16_real=0.0;D15_real=0.0; D14_real=0.0;
  D13_real=0.0; D12_real=0.0; D11_real=0.0; D10_real=0.0;D9_real=0.0; D8_real=0.0;
  D7_real=0.0; D6_real=0.0; D5_real=0.0; D4_real=0.0; D3_real=0.0; D2_real=0.0;
  D1_real=0.0; D0_real=0.0; outd=0.0; p_real=0.0; n_real=0.0;p=64'b0; n=64'b0;
        level_vol=0.0; mismag=0.025; //mismatch in percentage
      mis32=-1;  mis31=-1; mis30=-1;  mis29=1; mis28=1;   mis27=-1; mis26=1;  mis25=-1;
      mis24=-1;  mis23=-1; mis22=1;  mis21=1; mis20=-1;  mis19=1; mis18=-1;  mis17=-1;
      mis16=1;  mis15=-1; mis14=1;  mis13=1; mis12=-1;  mis11=1; mis10=-1;  mis9=1;
      mis8=-1;    mis7=-1;  mis6=1;   mis5=1; mis4=-1;   mis3=1;  mis2=1;   mis1=-1
end
```

Figure 9.8: Verilog behavioral model of the feedback DAC, section 1: initial conditions

```
always @ (D[31] or D[30] or D[29] or D[28] or D[27] or D[26] or D[25] or D[24] or D[23] or
D[22] or D[21] or D[20] or D[19] or D[18] or D[17] or D[16] or D[15] or D[14] or D[13] or
D[12] or D[11] or D[10] or D[9] or D[8] or D[7] or D[6] or D[5] or D[4] or D[3] or D[2] or D[1]
or D[0])
begin
  D31_real = D[31]? 1.0 : -1.0;D30_real = D[30]? 1.0 : -1.0; D29_real = D[29]? 1.0 : -1.0;
  D28_real = D[28]? 1.0 : -1.0; D27_real = D[27]? 1.0 : -1.0; D26_real = D[26]? 1.0 : -1.0;
  D25_real = D[25]? 1.0 : -1.0; D24_real = D[24]? 1.0 : -1.0; D23_real = D[23]? 1.0 : -1.0;
D22_real = D[22]? 1.0 : -1.0; D21_real = D[21]? 1.0 : -1.0; D20_real = D[20]? 1.0 : -1.0;
D19_real = D[19]? 1.0 : -1.0; D18_real = D[18]? 1.0 : -1.0; D17_real = D[17]? 1.0 : -1.0;
D16_real = D[16]? 1.0 : -1.0; D15_real = D[15]? 1.0 : -1.0; D14_real = D[14]? 1.0 : -1.0;
D13_real = D[13]? 1.0 : -1.0; D12_real = D[12]? 1.0 : -1.0; D11_real = D[11]? 1.0 : -1.0;
D10_real = D[10]? 1.0 : -1.0; D9_real =  D[9]? 1.0 : -1.0; D8_real =  D[8]? 1.0 : -1.0;
D7_real =  D[7]? 1.0 : -1.0; D6_real =  D[6]? 1.0 : -1.0; D5_real =  D[5]? 1.0 : -1.0;
D4_real =  D[4]? 1.0 : -1.0; D3_real =  D[3]? 1.0 : -1.0;  D2_real =  D[2]? 1.0 : -1.0;
D1_real =  D[1]? 1.0 : -1.0;  D0_real =  D[0]? 1.0 : -1.0;  end
always @(phi1d)
 if ( phi1d == 1)
        begin
          level_vol=0.25;  #2
        begin
outd=level_vol*(1+mis32*mismag)*D31_real+level_vol*(1+mis31*mismag)*D30_real+level
_vol*(1+mis30*mismag)*D29_real+level_vol*(1+mis29*mismag)*D28_real+level_vol*(1+m
is28*mismag)*D27_real+level_vol*(1+mis27*mismag)*D26_real+level_vol*(1+mis26*mism
ag)*D25_real+level_vol*(1+mis25*mismag)*D24_real+level_vol*(1+mis24*mismag)*D23_r
eal+level_vol*(1+mis23*mismag)*D22_real+level_vol*(1+mis22*mismag)*D21_real+level_
vol*(1+mis21*mismag)*D20_real+level_vol*(1+mis20*mismag)*D19_real+level_vol*(1+mi
s19*mismag)*D18_real+level_vol*(1+mis18*mismag)*D17_real+level_vol*(1+mis17*mism
ag)*D16_real+level_vol*(1+mis16*mismag)*D15_real+level_vol*(1+mis15*mismag)*D14_r
eal+level_vol*(1+mis14*mismag)*D13_real+level_vol*(1+mis13*mismag)*D12_real+level_
vol*(1+mis12*mismag)*D11_real+level_vol*(1+mis11*mismag)*D10_real+level_vol*(1+mi
s10*mismag)*D9_real+level_vol*(1+mis9*mismag)*D8_real+level_vol*(1+mis8*mismag)*
D7_real+level_vol*(1+mis7*mismag)*D6_real+level_vol*(1+mis6*mismag)*D5_real+
level_vol*(1+mis5*mismag)*D4_real+level_vol*(1+mis4*mismag)*D3_real+level_vol*(1+mi
s3*mismag)*D2_real+level_vol*(1+mis2*mismag)*D1_real+level_vol*(1+mis1*mismag)*D
0_real;

p_real= 0.5*outd+$bitstoreal(vcm); n_real=-0.5*outd+$bitstoreal(vcm);

p=$realtobits(p_real); n=$realtobits(n_real)
        end
      end
endmodule
```

Figure 9.9: Verilog behavioral model of the feedback DAC, section 1: feedback operation

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