Experimental Investigation of the Performance of Two New Types of Soft-Switching Power Converters for Electric Ships

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Abstract—**Power electronic converters are significant contributors to system mass, system loss, and system cost in the all-electric ship, and are, therefore, a significant area of interest. This paper investigates the reduction of switching losses in high power (MW level) converters. These losses remain a major obstacle to the development of converters capable of operating at higher frequencies and higher power densities using silicon power electronics.**

The Auxiliary Resonant Commutated Pole (ARCP) soft-switching converter topology offers the potential for minimization of switching losses, but has some inherent limitations. This paper examines two new converter designs based on the ARCP soft-switching topology that allow for more compact converter units by reducing the semiconductor switching losses generated within them. These concepts have been proven with simulation and laboratory testing of a sub-scale 20 kW test converter configurable in four distinct modes of operation. Efficiency has been measured for the two new ARCP topologies, as well as the original ARCP and standard hard-switching (conventional) technology using an induction motor as a load. New control algorithms to drive the ARCPs switches have also been developed, which improve the performance and reduce the amount of sensors that are required. The new proposed topologies are described and experimental waveforms and efficiency measurements are given.

Keywords—Converter topology, ARCP, Auxiliary Resonant Commutated Pole, Switching losses.

I. Introduction

Advanced electric sensors and weapons are increasing the demand for electric power on naval platforms. As part of the Electric Ship Research and Development Consortium (ESRDC), the University of Texas (UT) has been conducting research into integrated electric power systems with support from the Office of Naval Research (ONR) and the Naval Surface Warfare Center, Carderock Division (NSWCCD). Much of the research has centered on the system-level evaluations of power system architectures and identification of high payoff technology development activities. Ship hotel, weapon, and propulsion loads require power with different voltage and frequency characteristics, so power electronic conversion equipment will be a critical element of the power distribution system. ESRDC architecture evaluations show that power conversion equipment can represent 25-30% of the total volume and weight of the electric power distribution system [1] and the number of conversion stages has a significant impact on overall efficiency of the system. Enhanced power conversion efficiency has broader implications on ship design, as the reduced losses reduce the size of the associated thermal management system. Increasing the capability, power density and efficiency of power conversion equipment will have a major impact on the performance of the power system. Consequently, UT developed new power converter concepts that improve the performance and efficiency of these critical elements of naval electric power systems. This paper reports on two novel topologies for improved power conversion, improved control strategies for these converters, and the results of laboratory testing.

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II. The New Topologies

Power converters are an ever-increasing need on the electric ship, but transistor (typically of the Insulated Gate Bipolar Transistor, IGBT, type) switching losses limit the maximum operating frequency of large power converters. While silicon carbide devices promise to be a long term solution, there are significant improvements possible in silicon-based converters in the interim.

Switching losses are caused by the finite switching time of the devices and by the simultaneous presence of non-zero values of voltage and current during the transition. While IGBT switching times depend on the underlying physics of the devices, the converter designer can explore ways to achieve the switching transition at reduced values of either voltage or current in order to minimize switching losses. In fact, if the commutation can be accomplished when the current through the IGBT is zero or when the voltage across it is zero, the switching losses would be zero. The attainment of either condition, namely zero voltage or zero current during switching, resulting in zero switching loss, is known as “soft switching” of the device.

The Auxiliary Resonant Commutated Pole (ARCP) is an existing soft-switching inverter topology, but it has several significant drawbacks. Two alternative topologies that address these limitations are examined here (Figure 1).

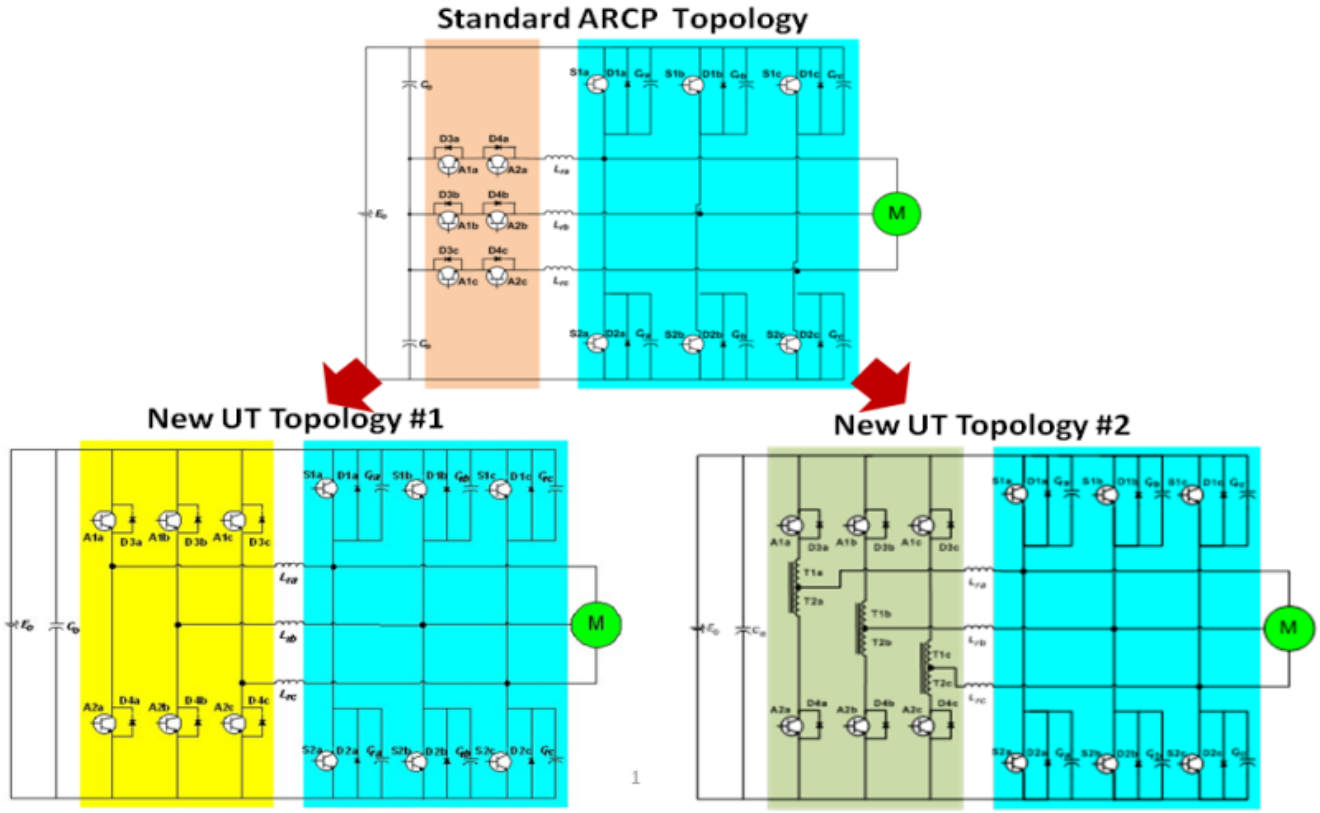

Figure 1: Derivation of the two new ARCP topologies developed and tested.

Referring to Figure 1, the standard ARCP is essentially a customary inverter (bracketed in blue in all three topologies shown) with an auxiliary circuit (brown section for the standard ARCP) that helps to soft-switch the main inverter. The auxiliary switches are activated before the main output switches are triggered, and generate a current in the auxiliary inductor that is used to induce the condition for a soft-switching transition for the main inverter switches. The auxiliary switches are turned on and off at zero current while the main switches are switched at zero voltage. The ARCP operating principle and commutation sequence is described in more detail in [2]. Unfortunately, the standard ARCP has some drawbacks such as requiring a center tapped dc bus, and has issues with diode reverse recovery currents leading to damaging voltage spikes [3].

The new UT (University of Texas) topology #1 replaces the standard ARCP's auxiliary circuit with a second smaller auxiliary inverter (yellow section). This topology eliminates the diode reverse recovery and the DC bus center-tap requirement of the standard ARCP, while still soft-switching the main devices. This topology is simpler to implement than the standard ARCP and can be made more compact, but it is slightly less efficient due to only partially soft-switching the auxiliary circuit.

The new UT topology #2 uses a small pulse transformer (see green section in Figure 1), which is used to create a virtual neutral point for the auxiliary inductor. This topology, just like the first alternative topology, solves both of the issues with the standard ARCP. Furthermore, this topology achieves an efficiency equivalent to the standard ARCP due to fully soft-switching the main and auxiliary circuits. Additionally, the auxiliary switches can be downsized since they only need to carry half of the auxiliary current, while the other two topologies have the auxiliary switches carrying the entire auxiliary current. The only additional complexity for this approach is that some method is required to reset the magnetic core of the transformer. Figure 2 shows simulated and measured waveforms for this converter. The last set of traces shows that the two auxiliary switches share the auxiliary current load.

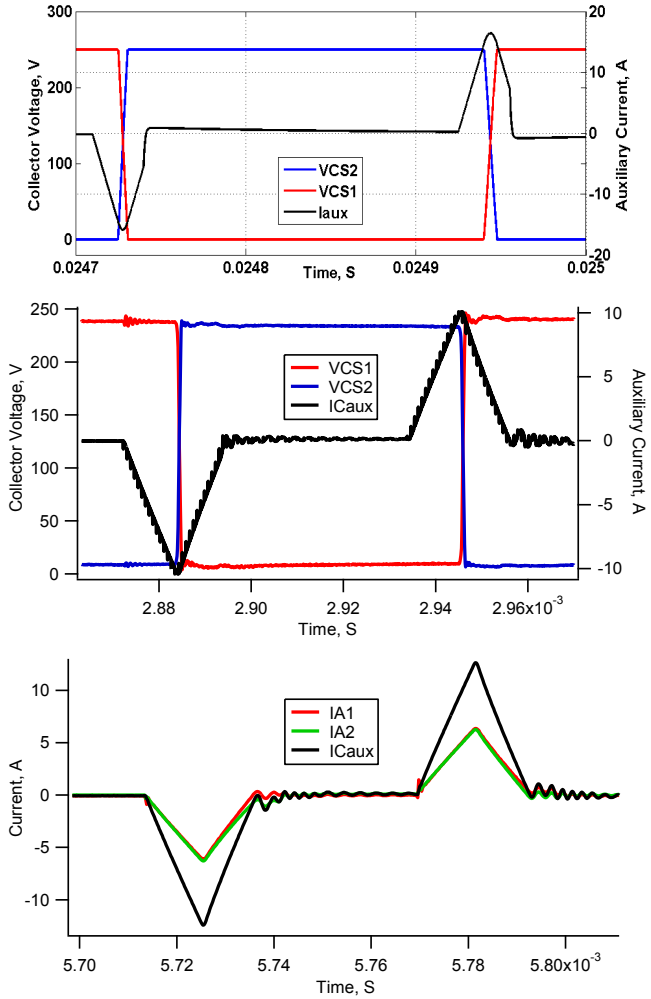

Figure 2: Simulated (upper) and measured waveforms (lower two) for the new concept no. 2 ARCP. Black is the current in the auxiliary inductor, red is the collector to emitter voltage for main switch S1 and blue is the collector to emitter voltage for main switch S2. The final plot shows the current through auxiliary switches A1(red) and A2(green) summing to the auxiliary current (black).

The attributes of the two new topologies, and the standard ARCP, are compared in Table 1. Further details on the operation and commutation of the two new UT inverters are given in [4].

III. Experimental Prototypes

MATLAB/Simulink with the simpowersystems package was the software tool used to support the simulations. A three phase 20 kw experimental inverter that can be configured in any of the three discussed topologies was constructed using powerex CM100DY-24NF IGBT modules driven by powerex VLA504 gate driver modules. Zero-current and zero-voltage detection was provided by discrete circuitry. Xilinx Complex Programmable Logic Devices(cplds) were used to generate the soft-switching gating signals and implement the control strategies. 130 µH air core inductors were used for the standard ARCP and the new ARCP concept #2. 260 µH air core inductors were used for the ARCP new concept #1 to keep the timing and operating conditions identical. A 10 µs boost time was used, and the resonant capacitors were 10 nf film-type capacitors rated for "snubber" duty. The experimental 20 kw prototype is shown in Figure 3.

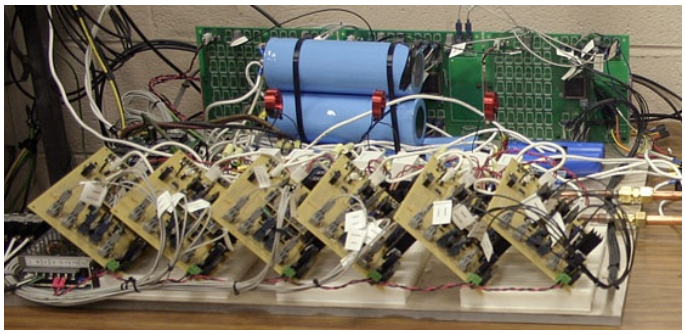

Figure 3: 20 kW experimental inverter.

A 2 MW ARCP converter was also available for laboratory testing and is shown in Figure 4. This converter was built using the standard ARCP topology [5]. A Baldor S15 drive was used to generate the pulse-width-modulated (PWM) waveforms for the converters and the switching frequency was set to 4 kHz.

Table 1: Summary comparison of the three topologies.

	Standard ARCP	New concept #1	New Concept #2
Main devices soft-switched	yes	yes	yes
Auxiliary devices soft-switched	yes	partially	yes
Split DC bus required	yes	no	no
Power handling	normal	higher	normal
Transformer required	no	no	yes
Voltage spike issue	On auxiliary switches	no	Transformer reset
Auxiliary device current (total device: IGBT and freewheel diode)	full	Full (for half the time)	Half (since split between A1 and A2)

9501.02

Figure 4: The 2MW ARCP converter.

IV. Control Strategy Developments

Any ARCP-type converter requires precisely timed gate signals to operate at maximum performance. Programmable logic devices have been used to implement the required gating strategies and the same algorithms are also implemented in the simulations. A simplified block diagram of the control logic is shown in Figure 5. In essence, the logic takes in signals from the PWM generator and generates properly timed auxiliary trigger and main switch enable signals. These signals then flow into interlock logic that enforces the zero-voltage switching behavior of the main switches and the zero-current switching of the auxiliary switches.

One of the most important control parameters in an ARCP inverter is the "boost time", which is the time that is spent charging the resonant inductor. A higher boost time allows the inverter to handle a higher load, but increases resistive losses in the auxiliary circuit. While a standard hard-switching inverter applies the PWM signal directly to the gates of the power switches, an ARCP requires additional logic to provide the following essential functions:

- activation of the correct auxiliary switch before commutating the main switches.
- controlling the boost time of the inverter
- ensuring that the main switches are switched at zero-voltage
- ensuring that the auxiliary switches are switched at zero-current.

Since the timing of the switches is critical for proper ARCP operation, the control strategy is a key candidate for optimization. The following improvements over standard ARCP controller operation have been developed:

- The current-sensing circuit on the auxiliary switches has been eliminated by using the zero-voltage transition times of the main switches as well as a simplification of the gate drive hardware. The traditional approach to controlling the ARCP's auxiliary switches is to use a zero-current sensor to make them function as a virtual thyristor. The simplest solution would be to activate the auxiliary switch for double the length of the boost time, but this does not take into account the slightly variable time that the output takes to slew from one power rail to the other, first from negative to positive and then from positive to negative. The improved control strategy is to activate the auxiliary switch for one boost time period before the old main switch is turned off, and then delaying the start of the second boost time (ramp down) period until the new main switch has achieved zero-voltage. This algorithm has shown a superior auxiliary switch turn-off behavior with respect to the one based on a current sensor.

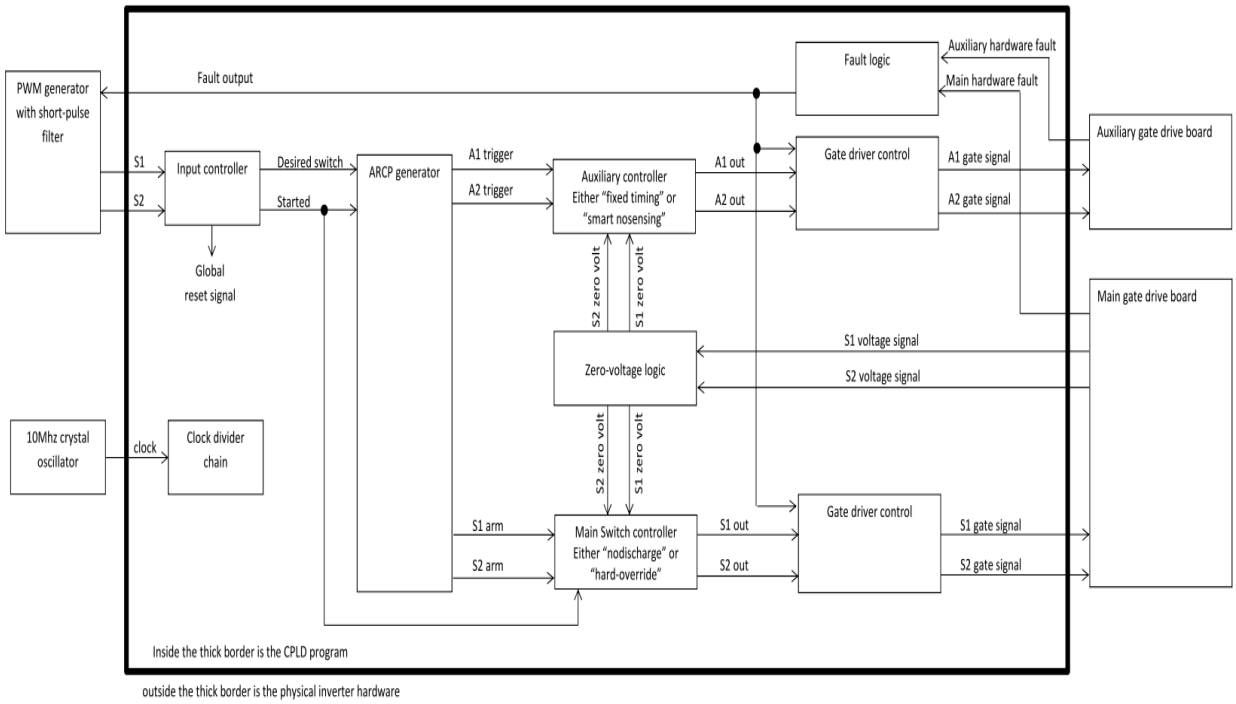

Figure 5: block diagram overview of the CPLD control system.

- New software has also eliminated some dedicated auxiliary circuitry originally used to provide an initial zero-voltage condition across a pre-established set of IGBTs to start the ARCP switching sequence. In the new algorithm, when the first PWM edge is received by the inverter, the corresponding main switch is activated in a hard-switching manner and then the standard soft-switching sequence begins.

- The original control strategy would enforce an inverter shutdown every time the inverter is overloaded and the main switches cannot achieve zero-voltage. A new control strategy has been implemented, which allows for the inverter to operate as a hard-switched inverter during transient overload conditions to improve system reliability. This is achieved by using a timer that forces the next main switch to turn on when no zero-voltage state has been reached after a timeout. While this hard-switched event incurs additional losses during the transient, the inverter can continue to operate eliminating nuisance shutdowns. Since the boost time needs to be set to ensure that sufficient auxiliary current is available to commutate the inverter, and additional auxiliary current incurs additional resistive losses, it may be possible to improve the overall system efficiency by decreasing the boost time to reduce the resistive losses in the auxiliary circuit, while still supporting larger transient higher loads.

The following additional control enhancements are currently under consideration:

- An "auto-tuning" variable boost time is under investigation. Since the boost time setting has a significant impact on the inverter's efficiency, an ARCP, which can dynamically adjust its boost time in relation to the output load, can show a significant reduction in losses [6]. Usually, the variable boost time control strategy needs to monitor the inverter load with a current sensor. The above mentioned hard-override capability, which ideally should correspond to zero boost time, can be expanded up to provide variable boost time without need for any current sensors. When a hard-override switching event occurs, it is an indication that the boost time is too short. Frequent hard-override events would signal the control system to increase the boost time. Conversely, absence of hard-override events would cause the control system to reduce the boost time. It must be noted that this control strategy does not depend on the use of any high bandwidth, high accuracy current transducer, as is required for the traditional variable boost time schemes that have been previously reported [6][7].

- An additional control strategy could be implemented to skip the auxiliary current pulses when the inverter load current is in the correct direction and of a magnitude that is sufficient to soft-switch the main inverter without assistance from the auxiliary circuit. In fact, an inverter can operate in a soft-switching mode without intervention of the auxiliary circuit under these favorable conditions [2][7]. This would require a current sensor on the inverter output, but only the current direction and whether its magnitude is above

or below a threshold need to be sensed (again, there is no need for high bandwidth, high accuracy transducers).

V. RESULTS

In theory, minimization of switching losses results in an improvement of the efficiency in the main switches; however, it must be considered that the added hardware needed to accomplish this task introduces additional losses of its own that tend to negate some of the gains due to soft-switching. In our case, particularly losses, both conduction and switching, in the auxiliary switches *A1* and *A2* are not negligible. The question, then, is whether a net gain in loss reduction is still accomplished with the ARCP topology.

In principle, the task of measuring the losses in a converter is straightforward: measurements must be made of the power input to the converter and its power output as a function of load in order to get a plot of its losses, or equivalently its efficiency, versus load. The practical difficulties of carrying out these measurements, however, can make them quite demanding. It would be helpful if one could rely on published standards for the measurement of converter losses, but the fact that, to this date, no standards have been promulgated dealing with this issue highlights the depth of the problem. The main obstacle is the difficulty of making accurate power measurements with the heavily distorted waveforms found in converters. It is sobering to realize that, nearly all efficiencies advertised or quoted by converter manufacturers are estimated efficiencies with little or no direct experimental validation. Against this backdrop of limited guidelines and information, UT researchers set out to experimentally establish the validity of the expected efficiency gains to be accrued by soft-switching converters of the ARCP type.

The efficiencies of the traditional hard-switching inverter, the standard ARCP, and the two new topologies have been measured experimentally as a function of load. The largest load with which the 20 kW converter could be loaded in a controllable and reliable way was 6.5 kW with a combination of resistive and motoring load for a combined power factor of 0.76. Tests, however, were performed up to a total load of 10 kW. These measurements were performed using the same power transistors in the same reconfigurable sub-scale test-bed inverter. This approach was selected to provide a topology comparison, without the additional complexity of potential different switch properties, which could occur if different switches were used in the different topologies.

A Voltech PM6000 digital power analyzer was used to measure the efficiencies while a custom-built induction motor dynamometer was used as a load for the inverter under test. Although this instrument is capable of handling arbitrary waveforms, it was found that special care had to be exercised in the definition of its integrating interval, in the use of appropriate shunts, and in the interface with other elements of the data acquisition system. The difficulty of achieving high-quality, repeatable measurements of electrical variables and the derivation of efficiency values from them in the presence of large amounts of high-frequency PWM noise cannot be overstated.

Typical results obtained using the UT 20 kW prototype are shown in Figure 6. Of particular importance are the following observations:

1. The loss reduction achieved by the ARCP at the largest test load (6.5 kW) is about 22% of the hard-switched losses. This number is significant.
2. It is expected that the trend will continue for larger loads, thus achieving larger loss reduction percentages at higher loads (the inverter is rated at 20 kW).
3. The standard ARCP and the second new topology (which alleviates some of the implementation issues with the standard ARCP) both achieve higher efficiency than the traditional hard-switching inverter.
4. The first alternative topology achieves a higher efficiency than the hard-switched inverter at higher loading, although it is not as efficient as the other ARCP configurations (due to the one remaining hard switched transition per cycle in the auxiliary circuit), but can achieve a higher power density and is simpler to implement.

VI. CONCLUSIONS

The proposed new configurations for a soft switching ARCP converter have been shown to be viable alternatives and achieve the following goals:

- The first alternative topology maximizes the achievable power density with better efficiency than the conventional hard-switched inverter when the load exceeds a minimum threshold.
- The second alternative topology maximizes the converter efficiency achieving full soft-switching with the same power density as the standard ARCP topology.

The results prove that the soft switching topology generally known as ARCP can be an effective way to reduce switching losses in high power converters. The ARCP technology holds the best promise for improving the performance of converters based on present day semiconductor switches. Should the availability of wide band-gap switches be delayed for whatever reason, the ARCP technology applied with Si switches is a good fall-back option for loss reduction.

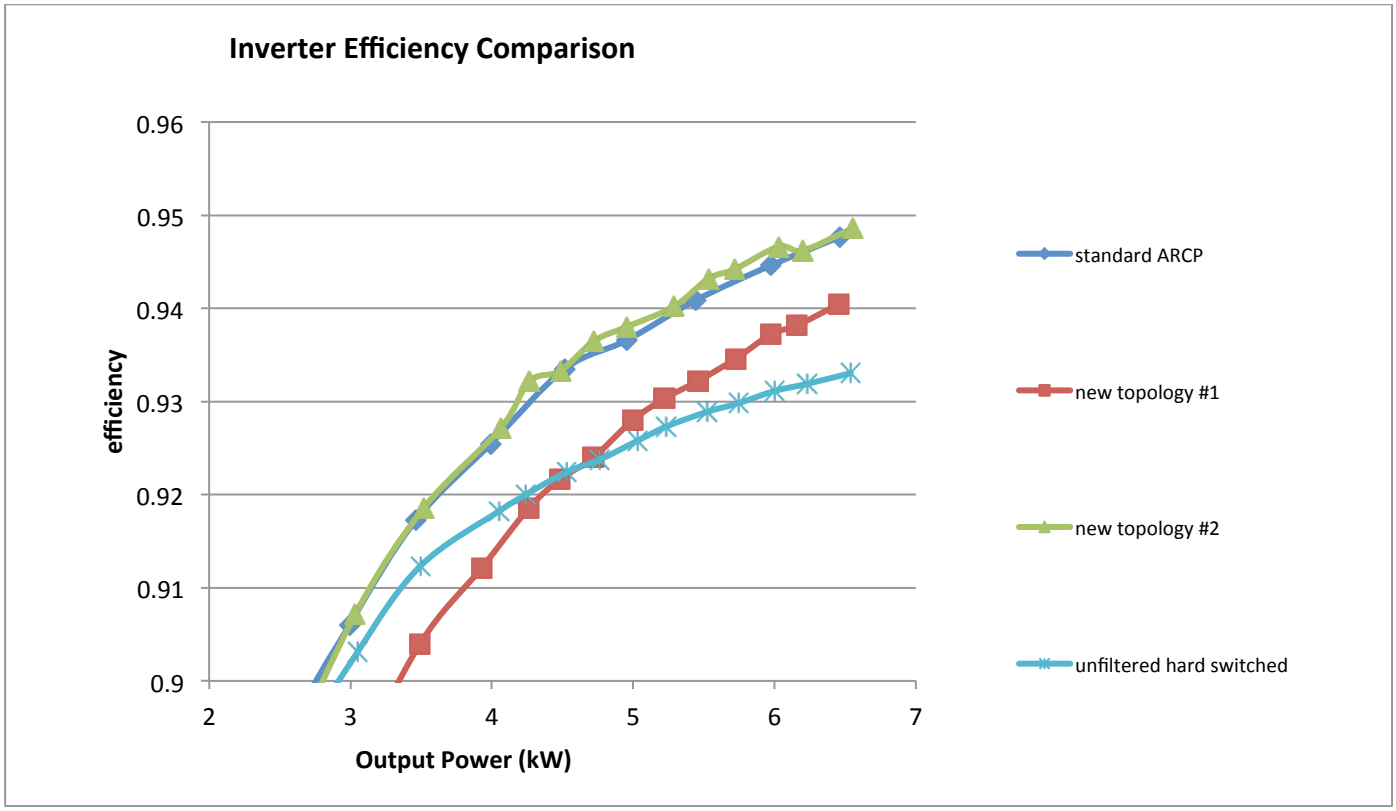

Figure 6: Efficiency results for hard-switched inverter, standard ARCP inverter, and the two new ARCP topologies

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