Power Electronics and Controls for Air Core Compulsator

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Abstract -- **The Center for Electromechanics at the University of Texas (CEM-UT) has been engaged in a large scale effort to develop the power electronics and control systems required to demonstrate a multi-megawatt, full control, SCR based rectifier/inverter and high power SCR closing switch. The ultimate objective of this development effort is to provide high efficiency switching for self-excitation of air core single phase rotating machines and to control the delivery of energy to the final loads. The self-excitation process is initiated by a seed current capacitor followed by active rectification of the compulsator ac output into the field coil. Upon reaching full open circuit voltage, the main closing switch is used to initiate current into the rail gun load. After termination of the gun current pulse, stored field coil energy is returned to the rotor via source commutated, full wave inversion.**

This paper will present theory of operation for the complete rectification and inversion cycle, SCR selection criteria, overall design strategy and all available test data. The test results will include the testing of individual devices, multiple series/parallel modules, and full system testing if available. Funding for this effort has been provided jointly by Task C (contract no. DAAA21-86-C-0281) and CCEML (contract no. DAAA21-92-R-0002).

Introduction

The Center for Electromechanics at the University of Texas at Austin (CEM-UT) has been engaged in a research effort to design and fabricate a lightweight, air-core compulsator to be used in conjunction with a cannon caliber electromagnetic launcher (CCEML). Mechanical aspects of the system design and the associated tradeoff analyses are presented in reference [1]. This paper will present specifics of the of the detailed design efforts required to select, package and control the high power SCR arrays which will be used to accomplish the electrical goals of the CCEML contract.

As a result of the initial tradeoff studies, a four-pole, air-core compulsator was selected to power a 2.25 m, augmented railgun. This system will be capable of launching fifteen 185 g projectiles at a velocity of 1,850 m/s. This mission will be arranged as three, one second, five-shot salvos with a salvo rate of one every 2.5 s. The over all electrical design is summarized in figure 1.

This system will require the use of five distinct switch designs, each with unique operating requirements. Initiation of main gun current will require a repetitive, pulse duty switch with a surge current of 825 kA and a symmetrical voltage rating of 3.8 kV. This switch will be composed of 40 parallel, 75 mm thyristors arranged in a five layer, interleaved, toroidal geometry. Muzzle arc suppression will be require a similar closing switch with identical voltage ratings and a forward surge rating of only 250 kA.

Field coil current generation is achieved using a 95 MW thyristor bridge. Each bridge leg will operate at a maximum forward current of 25 kA with a 50% duty and must have a symmetrical voltage stand-off of 3.8 kV. Compulsator (CPA) source voltage will be used to drive leg-to-leg commutation during inverter operation thus achieving effective reclamation of stored field coil energy. Field coil seed current will be provided from a 4 kV capacitive energy store switched by dual 4.5 kV thyristors. Recharging of this store is provided by anti-parallel high voltage diodes with current limiting integral to the diode bus.

Overcurrent and thermal protection of the CPA and all solid state subsystems is accomplished using an explosively operated opening switch which must carry the combined currents and action demands of both the gun and field coil circuits. During opening, this switch must be capable of dissipating all inductively stored energy. Normally, switch initiation is via a standard exploding bridgewire initiator. Fail-safe operation is provided by designing the replaceable switch elements for passive thermal failure beyond normal mission actions.

All interconnecting buswork will be designed to allow the use of flexible, hexapolar cable. Both the flex-bus and terminations have been previously built and tested at CEM-UT. Existing flex-bus designs feature "kickless," self-supporting operation with EM compensation and bipolar terminations. Cable impedances of 218 μΩ/m and 123 nH/m have been demonstrated. Thus, interconnection of the CPA and all switching elements can be completed within the present impedance budget [2].

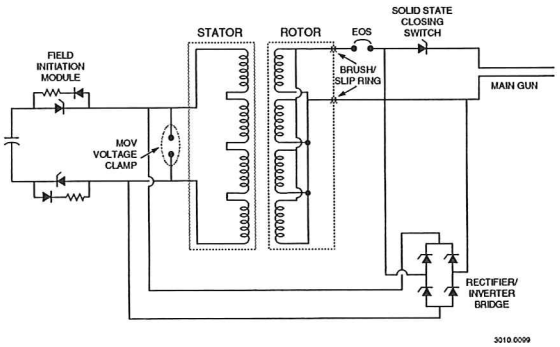

Figure 1. Overall system design

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Gate Drive

One of the first areas to receive attention was the gating requirements of the 70 to 100 mm SCRs which would be used to switch the gun and field coil circuits. Conventional gate drive circuits used with amplifying gate SCRs can categorized into two gate drive levels (hard and soft) and two gate drive strategies (picket fence and back porch.).

Soft drive is generally characterized by a gate current of one or two times the minimum gate current needed to provide SCR latching, while hard drive is considered to be a current of five to six times minimum latching current. A soft drive system results in the lowest power demands while a hard drive system provides assurance that the full turn-on di/dt and surge ratings of the SCR can be obtained. If a small number of SCRs are to be used, then a hard gate pulse is usually selected in order to guarantee the rated turn-on characteristics of the device. In the case of the CCEML system, a soft gate pulse was initially considered in order to reduce the peak power demands of the gate drive system. In order to make a final selection it was also necessary to consider the impact of picket fence vs. back porch gating.

Due to the high common-mode voltages normal for the gate and cathodes of this type of high voltage SCRs, a pulse transformer is frequently used to provide isolation of the control and drive electronics from the SCR gates. The term "back porch" is used to describe the normal output characteristics of the secondary winding in this configuration. If the primary winding of the transformer is driven with a square wave then magnetic saturation of the core will produce an output pulse with a sharply rising front edge followed by an exponential decay of the output voltage and ending with a low level but reasonably flat tail. This tail has come to be known as the back porch, and helps provide follow-on current to establish stable turn-on in the main channel.

If an extremely low dv/dt is seen across parallel SCRs then it is difficult to know sufficient voltage exists at the time of gating to provide positive turn-on of all parallel paths. In this case, it may be useful to extend the gating interval beyond the saturation limits of the pulse transformers. This can be done by driving the transformer input with a square wave having a voltage swing of +Vcc to -Vcc and then using a full wave rectifier on the output to produce a poor quality dc gate drive. While this does allow extended gating intervals, the resulting complexity of the gate drive circuit has increased dramatically over the case of the simpler, single pulse, back porch.

After examining the possibilities presented above, it was clear that two of the possible configurations were only usable for specific special conditions. Soft drive is only usable for low di/dt, non-surge turn-on and picket fence is only required for very low dv/dt turn-on. A hard drive gate pulse with a 50 ms back porch was selected as the best general solution for the moderate to high di/dt and dv/dt requirements of the CCEML system (fig. 2). The prototyping and testing of this drive will be covered in detail later in this paper.

Controls / CPE

After satisfying the general gating requirements of the SCRs to be used in the CCEML switches, the next area to receive detailed attention was the design and prototyping of

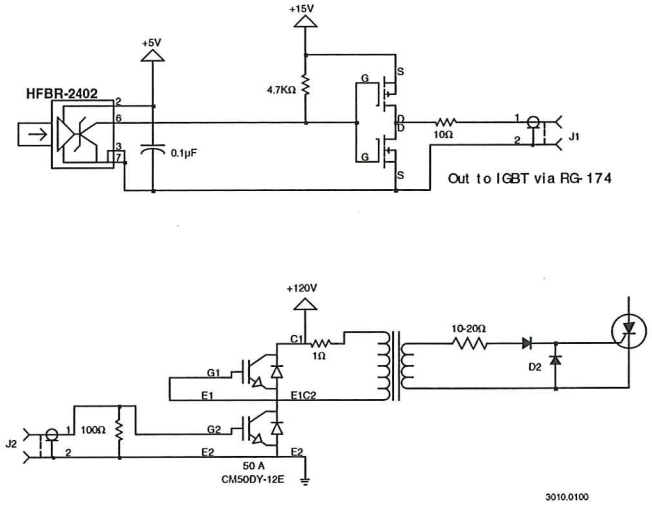

Figure 2. Final gate drive configuration

the control circuits required to generate the gate firing angles. CEM-UT has developed and patented [3,4] a highly specialized circuit design for the computation of firing angles within repetitive ac cycles, referred to as a cycle portion encoder (CPE). All of the CPE designs developed at CEM-UT have several common operating characteristics. The primary input is a TTL square wave with the rising and falling edges synchronized to the positive and negative going zero crossings of the compulsator output voltage. Internal to the CPE, the period of this waveform is measured using an integer count of clock cycles and the output of a CPE is an integer count proportional to the programmed cycle fraction. This output count is loaded into a countdown timer which is clocked at the same rate as the input counter such that the zero count of the output counter coincides with the firing angle output time.

The first generation CPE was designed for use with the iron core compulsator (ICC) and was tested during the commissioning of that machine. The block diagram for this system is shown in figure 3. After deriving the input period, this CPE placed the resulting binary count into a buffered digital to analog (D/A) converter. This voltage was passed across a simple resistive voltage divider and the new voltage converted back to digital using an analog to digital (A/D) converter. Proper operation of this unit required that the divider network be preset to the required cycle fraction. While this first design did suffer from analog conversion errors, its primary strength was the ease with which an arbitrary number of one-per-shot gun firing angles could be preset. For the multiple shot case, an analog mux was placed at the input to the A/D and individual dividers were used to represent each gun shot firing angle.

A second generation CPE was designed and tested for use with the small caliber compulsator (SCC). The block diagram for this system is shown in figure 4. This unit featured several important improvements over the first CPE design. The analog stage was eliminated from this design and the cycle length division performed using a EEPROM memory configured as a fast lookup table. This EEPROM was preprogrammed with the appropriate lookup tables prior to a gun

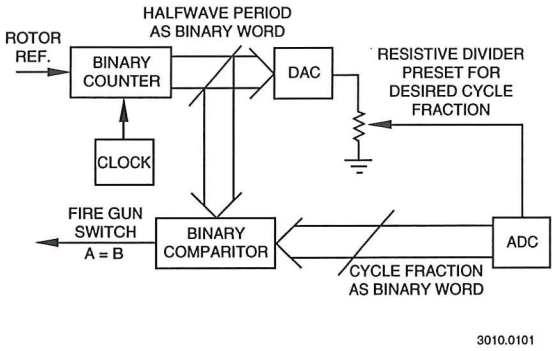

Figure 3. Figure generation CPE

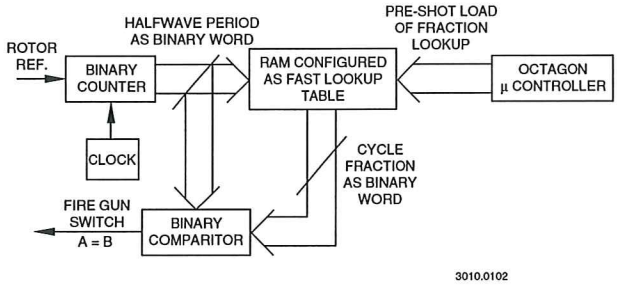

Figure 4. Second generation CPE

shot by a stand-alone microcontroller. The resulting system measured the input period, placed this binary word on the address lines of the EEPROM and the cycle fraction count was available on the EEPROM data lines.

A second major revision to the SCC CPE was the use of automatic master clock selection. The first CPE required the operator to select a master clock rate which was appropriate the machine frequency of the upcoming shot. This function was replace by a single master clock with a bank of divide-by-2 counters. A pair of binary magnitude comparitors checked for the minimum and maximum period count values and generated automatic doubling or halving of the clock rate to correct the out of range condition.

After a review of the operating history of these two units, the design of the next generation CPE for use with the CCEML system started with several clear goals. First, both of the previous systems were built to generate gun firing pulses which are always single pulse in nature. The requirements of the new gun CPE were identical to previous systems, but during inverter mode the bridge CPE must produce stable timing pulses during each half of the voltage waveform to gate the two bridge halves. This required a design which was able to function as a full-cycle CPE. Second, an alternative to the EEPROM lookup was needed. Since the contract required a full mission the 15 shots, the memory required quickly becomes quite large. Additionally, use of the lookup solution eliminates any type of dynamic control on the bridge firing angle. For these reasons, a fast integer multiplying chip was explored as an alternate method of generating cycle fractions.

Since the gate drivers were also a new design, it was decided to prototype a demonstration system which could be used to debug a first pass full-wave CPE in operation with the new gate drive circuitry. In order to limit the complexity of the first test the CPE built for this evaluation used an EEPROM lookup, but included all of the revisions to allow full-wave operation. The main change required for full-wave operation is the use of a master-slave clock select to allow clock updates on the output counter to occur one machine half-cycle later than on the input counters. Thus, the output fraction width is always clocked at the same rate as the input period from which it is generated (fig. 5). A change was also required to the manner in which the input period was counted. On all previous designs, the input period was counted from rising edge to rising edge. This system required that each half cycle be counted as the input period. This was done by passing the input square wave through a digital delay and then XORing the original signal with the delayed version of itself. The output of the XOR is a positive pulse with a width equal to the initial delay time and occurring at any input edge, rising or falling. Several such timing "strobes" were generated for all timing control through use of multiple XOR gates and a single multi-tap digital delay chip produced by Dallas Semiconductor.

Once the evaluation CPE design was fabricated and tested on the bench top, a simple timing control circuit was designed and built. This controller allowed independent control of the rectify and inverter intervals for the test fixture which was to be built. The final test setup consisted of the full wave CPE, RI controller, three channels of the prototype gate drive, and a clamping fixture for five SCRs. These SCRs were one per leg of a full wave bridge and a single freewheel SCR. Input power to the test rig came from a 300 A ac welder. This welder was chosen for the fact that it provided internal current limiting while still producing an output with usable symmetry. The dc output of the bridge was used to charge a 4 mH inductor which was available from the CEM-UT lab equipment pool.

Initial testing of the R/I setup was performed using a resistive load in the place of the inductor. This was done to limit the amount of stored energy in first shake down tests. Early

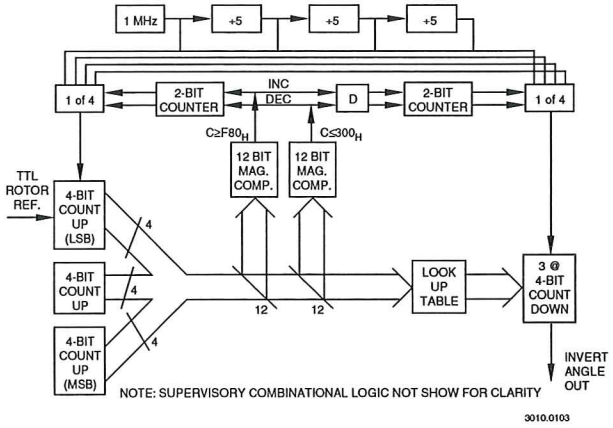

Figure 5. Third generation CPE

results of this testing showed that an instability existed within the gate drive circuit. In order to deal with what appeared to be multiple retriggering of the IGBT, the 74HC123 timing circuit which controlled gate pulse width was moved out of the final drive box and reinstalled at the fiber optic drive point. It was also found at this time the switching characteristics of the IGBT were very sensitive to the resistor values used in the series/parallel IGBT gate lead termination. The final values selected are shown in figure 2. One final problem continued which was the intermittent failure of the IGBT itself. After talking with the Powerex technical staff, this was chased to the fact that magnetic saturation of the isolation transformers caused the final primary current to approach 200 A, which exceeded the surge limit of the device. The addition of a 1 Ω, low inductance, series resistance to the primary circuit solved this problem and resulted in very reliable operation.

With all of the SCR gating problems resolved, the inductor was installed as the new test load. The rectification of current into the inductor proved to be quite easy and so the freewheel circuit was defeated and inversion was attempted. This attempt produced less happy results. During all attempts to operate in the inverter mode the first inverter cycle was successful but all following gate angles were wrong which resulted in very erratic operation. This was due to the internal current limiting of the welder which was used. During inversion, the output waveform symmetry was severely distorted which resulted in false period data being input to the CPE. After this dysfunction was understood, it was concluded that the R/I test fixture could not produce a usable test without the use of a very stiff ac source. Since this implies that a compulsator must be used, the testing of the evaluation system ended here. Final verification of the inverter mode will await fabrication of the CCEML compulsator and the normal electrical testing of the field coil system.

Main Closing Switch

Design Goals

The main closing switch is required to repetitively switch a 2.5 ms half-sinusoidal pulse with a peak current of 825 kA and an open circuit voltage of 3.8 kV. The required rep rate for the closing switch is three consecutive 5 shot salvos with a shot rate of 5 Hz and time between salvos of 2.5 s.

The primary design goal for the SCR closing switch was to minimize the system mass and volume. The classical approach to an SCR closing switch is to include an RC snubber network parallel with the SCR in order to address the voltage overshoot at turn off. Since the mass and volume for a conventional RC snubber is nearly equivalent to that of the SCR in the switch, elimination of the snubber would result in large mass and volume savings. In addition, SCR packaging is another area which greatly impacts the switch mass and volume. Over 90% of the total mass and volume goes into the commercially available capsule SCR case. While custom packaging the wafers into a "thin pak" [5] would have advantages the aggressive schedule of this design effort disallowed a complete investigation into all of the potential liabilities for such an aggressive reduction in packaging. Therefore device selection was limited to the readily available capsule package.

Electrical Testing/Design

Early in the solid state switch development at CEM-UT a snubberless gun closing switch was designed and successfully implemented on the small caliber program [6]. The small caliber closing switch used 8 parallel Westcode N540CH18 devices, which operated snubberless with no device mortality. Parallel testing of SCR closing switches at CEM-UT revealed that snubbers were only required in some cases to keep the voltage overshoot below acceptable levels. To answer this question about the necessity of snubbers for closing switch protection, an extensive test program was undertaken to evaluate SCRs of different manufacture to determine if snubber requirements were device specific. These tests were conducted on a 360 kJ capacitor bank, configured to allow high di/dt rates at device turn-off in order to evaluate reverse recovery characteristics of the device under test. The results of these tests suggested that the Westcode family of devices exhibit a soft turn-off resulting in a voltage overshoot significantly less than the applied voltage. Armed with this data, we examined the Westcode family of SCRs for devices with sufficient surge current ratings and voltages to adhere to the accepted factors of safety for closing switch design. Ultimately, the Westcode N750CH45 phase control thyristor was selected and tested to verify successful snubberless operation. Using 40 parallel Westcode N750CH45 for the closing switch, yields factors of safety of 1.33 and 1.20 for surge current, voltage respectively. These factors of safety are consistent with those as recommended by an independent review board, which reviewed the Task C power electronics [7].

Mechanical Packaging

For reliable switching using parallel SCRs it is paramount in insure that the devices share the current evenly. To induce current sharing, the current path to and from each device must be equal length and enclose the same area yielding equivalent resistance and inductance for each parallel path. To meet these criteria a coaxial approach was taken for packaging the main closing switch (fig. 6). In order to maximize power density for the switch, the SCRs are arrayed in five layers of eight for a total of 40 parallel devices.

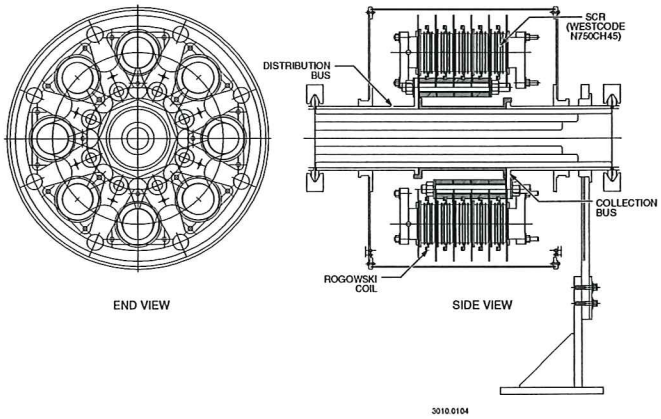

Figure 6. Main closing switch package

In order to minimize the mass and volume, a coaxial bus was chosen for the explosive opening switch (EOS) and main gun closing switch. The inner conductor of the coaxial bus is the current return path and the outer conductor is the switched leg. The current flows in the outer conductor from the EOS to a four petal distribution bus which extends the length of the SCR array. The four petal collection bus also extends the length of the SCR array but is indexed 45° with respect to the distribution bus. This results in the distribution and collection buses alternating radially around the coaxial tube at the same radial distance from coax center. Following the current path for one SCR, current flows from the distribution bus into two adjacent SCRs and is switched into the collection bus and then flows to the launcher via a hexapolar cable array. Note that since the distribution and collection buses are at the same radial distance and are of equal length the current path through any SCR has an equivalent impedance.

The final design parameters for the main closing switch are as follows:

- peak current(surge): 1120 kA
- peak voltage: 4.5 kV
- peak action*: 9.0×10^9 A^2s
- total volume: 126×10^{-3} m^3
- total mass: 102 kg
- peak power: 5.04 GW

* Assumes an adiabatic system.

Current flow through each SCR is monitored using a dedicated Rogowski coil, which is hard mounted in a holder in order to reduce shot to shot variations in the instrumentation.

The gating strategy for the switch is to gate each layer of eight devices with a common pulse transformer. So in the event of gate drive failure a complete layer of eight devices wont turn on and the remaining current carrying SCRs still maintain radial symmetry to insure an even current distribution between parallel devices.

Rectifier/Inverter Bridge

Design Goals

Field coil excitation and regenerative field coil dump for the CPA is accomplished using a full control, single phase rectifier/inverter. For an air core compulsator the initial magnetic field is provided by a seed current from a charged 50 kJ capacitor. As the CPA terminal voltage reaches the threshold for self-excitation, ac current from the main armature is rectified to charge the field coil. Between discharges residual field coil energy is then reclaimed by the bridge operating in the inverter mode and returned to the rotor where it is stored as kinetic energy. As a result, the bridge is required to operate in a quasi-steady state mode with a peak instantaneous power of 95 MW. For each gun shot the bridge rectifies to a peak current of 25 kA at 3.8 kV for between 50 to 100 ms (rotor speed dependent) which is then directly followed by an inversion cycle (approximately 50 to 100 ms) to reclaim field coil energy. The reclamation of field coil energy is extremely important in that it greatly reduces the thermal demands on the R/I bridge and associated buswork and also increases overall system efficiency.

As with the main closing switch, mass, volume and efficiency are key design concerns. The efficiency of the rectification/inversion cycle is very highly dependent on the SCR turn-off time. In designing the bridge SCRs with a fast turn off time and high action capacity were pursued as candidate devices. These devices were then evaluated in the laboratory. The apparatus and results of the testing are discussed in the following section.

Electrical Design/Testing

RI Electrical Testing

Since the electrical design and device testing for the GSM had preceded the design effort for the R/I bridge module all of the electrical testing fixtures existed to test the bridge devices once selected. However, upon review of the commercially available devices, a rather startling fact presented itself. Standard inverter grade devices are available only up to the 52 mm families, while all 70 mm and larger device families have been optimized for phase control operation due to the inherently slow operation within the larger SCRs. Using only off-the-shelf devices, it was not possible to design a bridge without sacrificing either inverter efficiency or packaging volume/mass.

The primary difference between SCRs intended for inverter operation and those intended for rectifier systems is the forward turn-off characteristics. This difference is best seen by the values of turn off time (T_q) for the two device grades. Simply stated, T_q is the minimum amount of time during which a reverse bias must be maintained across the device prior to reapplying forward voltage. If a forward voltage is applied to the device prior to satisfying the T_q "rest" time, then destructive retriggering of the device may occur. Typical values of T_q for inverter grade SCRs range from 100 µs to as little as 20 µs while phase control grades may have T_q's as high as 400 to 600 µs.

Prior to starting a search for the ideal SCR it was necessary to determine the maximum value of T_q which would result in a usable bridge design. A closed form interactive solution was used to evaluate the impact of T_q on inverter mode bridge operation. It was found that for $T_q \leq 100$ µs an inverter design was possible which would provide 92% of the theoretical maximum power levels, and that further decreases in T_q did not cause a significant increase in available power levels.

During preliminary discussions with several SCR manufactures, we were informed that large geometry SCRs could be processed for shorter T_q's, but the trade-off would be an increase in forward drop and a corresponding reduction in the forward surge current and action ratings. The fact that it would be necessary to de-rate the forward characteristics made it difficult to produce a device with all of the desired parameter values simultaneously. Ultimately, two manufacturers were able to provide us with samples of candidate devices for destructive testing. Westcode produced a modified 77 mm device which is a 3600 V SCR with surge ratings of 32 kA and an action rating of 7.6×10^6 A^2s which was based on the N880CH36. Powerex produced a modified 100 mm device which is a 3800 V SCR with surge ratings of 56 kA and an action rating of 1.3 x 107 A2s which was based on the TD-20, a new device.

Both of these devices were tested under identical conditions in order to verify the surge and turn-off ratings of the devices. This was required because the modified SCRs no longer operated according to the base line data sheets. The Powerex TD-20 prototype failed during turn-off at a di/dt of 570 A/μs after a peak current of 53.4 kA. The N880CH36 failed similarly at a di/dt of 400 A/μs after a peak current of 38.3 kA. Since this test fixture produced a symmetrical half-sin pulse, turn-on and turn-off di/dt's were equal for all tests. For the CCEML bridge, the worst simulated di/dt is 150 A/μs per device. Thus, either of these devices could be used in the final system. Ultimately, the Powerex device was selected for the simple reason that the higher voltage, current, and action ratings would produce the largest overall safety factors.

Mechanical Packaging

The full R/I bridge is composed of four identical legs, each containing 6 SCRs, 3 parallel-2 series (fig. 7). AC power is brought from the main coax into the center nodes of the bridge assembly via a single hexapolar cable . The ac input is rectified and the dc output is delivered to the field coil from the top of the bridge assembly and returns to the bottom of the bridge all via a single hexapolar cable bus. The RC snubber components are packaged in a compartment on the top of the SCR assemblies. The final layout is show in figure 8.

The Powerex TC2038UT device was selected not only for the above electrical characteristics but Powerex offered a reduced volume capsule SCR package. The capsule features a standard ceramic case with a 30% reduced thickness over a standard press pak. The preload requirement of 20,000 lb per device is achieved using a gang clamping system. The clamp uses a single alloy steel tie-rod in conjunction with two titanium flanges each of which has three self aligning tilt pads. The tilt pads are required so that an even pressure distribution is maintained across the SCR stack. Preload is initially applied using a hydraulic press and then maintained using spring washers.

The final design parameters for the rectifier/inverter bridge are as follows:

- peak current(surge): 138 kA
- peak voltage: 7.6 kV
- peak action*: 460 x 10^6 A^2s
- total volume: 112 x 10^{-3} m^3
- total mass: 125 kg
- peak power: 95 MW

* Assumes an adiabatic system.

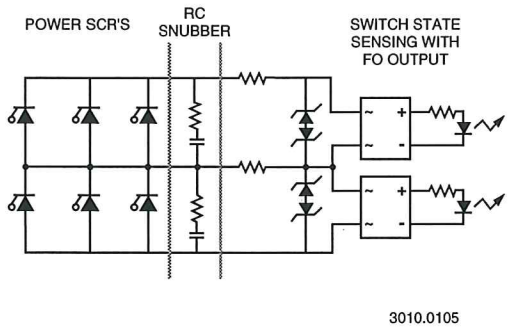

Figure 7. CCEML bridge leg

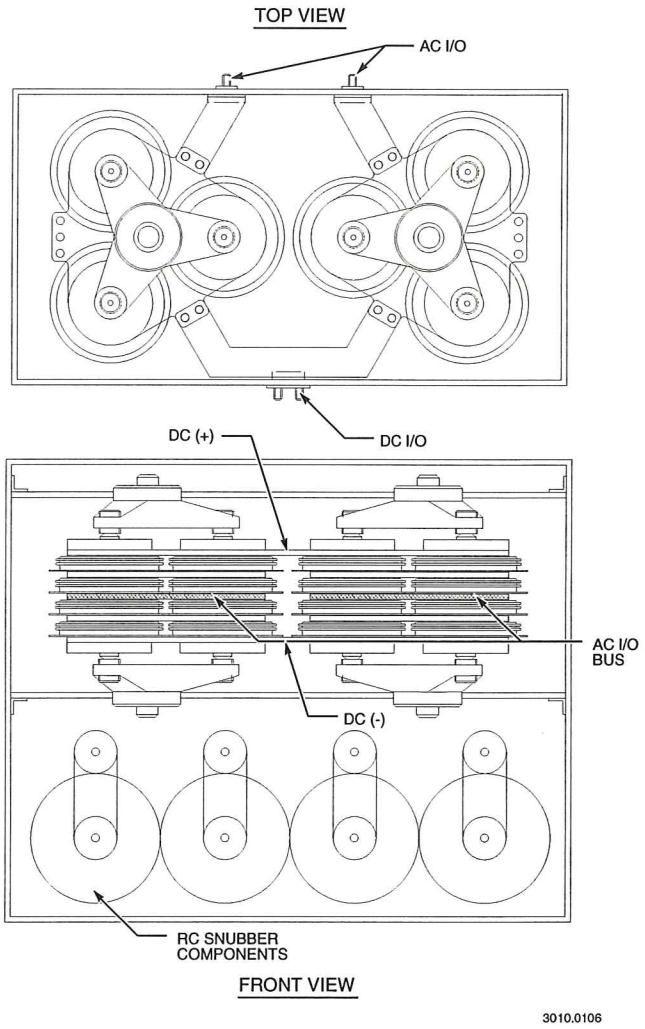

Figure 8. Rectifier/inverter bridge

Like the main closing switch current flow through each SCR is monitored using a dedicated Rogowski coil which is hard mounted in a holder.

References

1. J.R. Kitzmiller, et al "Optimization and Critical Design Issues of the Air Core Compulsator for the Cannon Caliber Electromagnetic Launcher System (CCEML)" to be presented at the 7th EML Symposium, San Diego, CA, April 29-24, 1994
2. J.H. Price, et al, "Design and Testing of High Current, High Voltage Hexapolar Flexible Cables for Pulsed Power Applications," 8th IEEE Pulsed Power Conference, San Diego, CA 1991.
3. R.F. Thelen, "Pulse Discharge Control and Machine Protection for a Multi-Discharge Compulsator," *IEEE Transactions on Magnetics*, Vol. 25, No. 1, Jan 1989.
4. Patent #4,905,004
5 R.F. Thelen, J.H. Price, "Power Electronics in the 9 MJ EM Range Gun System," 8th Pulsed Power Conference, San Diego, CA, June 17 to 19, 1991.
6. R.F. Thelen, et al, "Solid-State Switch Development for High Power Pulse Discharge Control," 1990 Nineteenth Power Modulator Symposium, June 26-28, 1990.
7. Task C Electrical Independent Design Review, U.S. Army ARDEC, May 1993.