The Dissertation Committee for Tae Ho Jung Certifies that this is the approved version of the following dissertation:

SUBMICRON AND NANOSCALE ORGANIC FIELD-EFFECT TRANSISTORS AND CIRCUITS

Committee:

Ananth Dodabalapur, Supervisor

Leonard F. Register,

Dean P. Neikirk,

Dim-Lee Kwong,

Yueh Lin Loo

Submicron and nanoscale organic field-effect transistors and circuits

by

Tae Ho Jung, B.S.; M.S.

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

August, 2006

Dedication

To my lovely wife, Hoyeon Kim

Acknowledgements

First I would like to sincerely thank my advisor, Dr. Ananth Dodabalapur, for his guidance, encouragement, and patience throughout my graduate studies. Without his technical and editorial advice, I could not have completed this dissertation. I also like to thank Dr. Leonard F. Register, Dr. Dean P. Neikirk, Dr. Dim-Lee Kwong, Dr. Yueh Lin Loo, and Dr. Joe C. Campbell for giving me valuable inputs and advice.

My thanks go to Liang Wang, Daniel Fine, Debarshi Basu, Suvid Nadkarni, Yeon Taek Jeong, Byungwook Yoo, Deepak Sharma, Chris Lombardo, and Lawrence Dunn. They were my colleagues and they are now my friends. Without them my research and life in Austin would have been incomplete, boring and dry.

Lastly, as always she waited for me, my lovely wife, Ho Yeon Kim, receives my deepest gratitude. She totally devoted herself to me, which I cannot compensate by any means. I'd like to thank our parents for their dedication and support during my study.

Submicron and nanoscale organic field-effect transistors and circuits

Publication No._____

Tae Ho Jung, Ph.D.

The University of Texas at Austin, 2006

Supervisor: Ananth Dodabalapur

The first part of this work is the electrical characterization and numerical analysis of the performance of an organic field-effect transistor (OFET) with novel components such as dielectrics, semiconductors, surface treatment, and electrode material. Since the electrode contact affects the device performance in most cases, a new transistor structure with a number of floating electrodes inserted in a channel was devised to decouple the resistance of the contact and channel. It was shown that the contact was an active component not a passive resistor, as is the case in inorganic transistor. This method can be used to develop accurate analytical models based on experimental data. In addition, a new simulation tool for an OFET has been developed using MATLAB and C language, which provides considerable freedom in order to include charge transport models and application environments that are often necessary for an accurate description of OFETs.

Fabricating submicron and nanoscale OFETs and their use in an inverter circuit and rectifier are the second part of the work because decreasing the channel length is

expected to enhance device performance by increasing the switching frequency. A nanoscale ambipolar FET consisting of thin layers of p- and n-type semiconductors has been studied which will simplify the fabrication of circuits in ease by removing a masking step for semiconductor. Submicron complementary inverters were studied because complementary circuits possess low power consumption and high noise margins. The characteristics of poly(4-vinyl phenol) (PVP) dielectric were also studied since all organic/polymer submicron circuits are the desired goal. It was found that the PVP and other polymer dielectrics are convenient to use but can be charged depending on the environmental condition and produce unstable output.

Table of Contents

CHAPTER 1 INTRODUCTION

1.1 Organic field-effect transistors in action

Since the discovery of the metallic properties of doped polyacetylene in 1977 [1], remarkable progress has been made in synthesizing pi-conjugated polymers as well as other lower-molecular-weight organic molecules, in understanding their properties, and in fabricating electronic and optical devices. Organic field effect transistors (OFETs) are of great interest because of their potential use in low-cost, large-area circuits on flexible substrates. As new materials with higher charge carrier mobilities and other favorable properties (such as easy processibility) are synthesized, the range of applications for which OFETs can be employed gets broader. Such applications include chemical sensors [2], display devices [3], and photodetectors [4]. One commercial application that has attracted the consumer electronics industry is an active matrix display, in which OFETs are integrated with organic light-emitting diodes (OLEDs) into smart pixels [5]. Organic transistors also used in non-LED based display applications such as the electronic paper based on pixels comprising either electrophoretic ink-containing microcapsules or twisting balls [6].

1.2 Organic/polymer submicron and nanoscale field-effect transistor

1.2.1 ORGANIC MATERIALS FOR DIELECTRICS AND SEMICONDUCTORS

In general organic and polymer semiconductors have ability to transport both types of charges when synthesized, but are in most case determined to transport only one type of charge when implemented in an electrical device due to the dielectric surface [7]. This is the opposite of inorganic semiconductors whose type is determined during device fabrication process. When an oligomer or polymer is formed, a carbon atom bonds to surrounding atoms and forms either sp^2 or sp^3 hybridization. When sp^3 hybridization occurs, all of the four valence electrons equally participate in four σ bonds and these bonds are equally distributed in three-dimensional space. The resulting structure is a tetrahedral shape as shown in Fig. 1.1. Since all four unpaired electrons are now engaged in the bonding, there is no free electron to contribute to any electrical conduction. In sp^2 hybridization three electrons from s and p orbitals hybridize to form sp^2 orbital and three σ bonds are equally distributed in two-dimensional space as shown in Fig. 1.1. The fourth valence electron is in the p_z orbital and forms the π bond, which is perpendicular to the plane of sp^2 orbital. This π electron is delocalized and makes an oligomer or polymer with conjugated bond (alternating single and double bonds) semiconducting. When this oligomer or polymer is deposited by thermal evaporation or solution processing to make an OFET, they are pulled to each other by Van der Waals forces and form a thin film. The electron transfer between the oligomers and polymers

is less facile than transfer between covalently bonded atoms such as silicon since the interaction between the molecules is much weaker than a covalent bond. The charge transport between molecules could be hopping [8, 9], band-like transport [10], or tunneling [11].

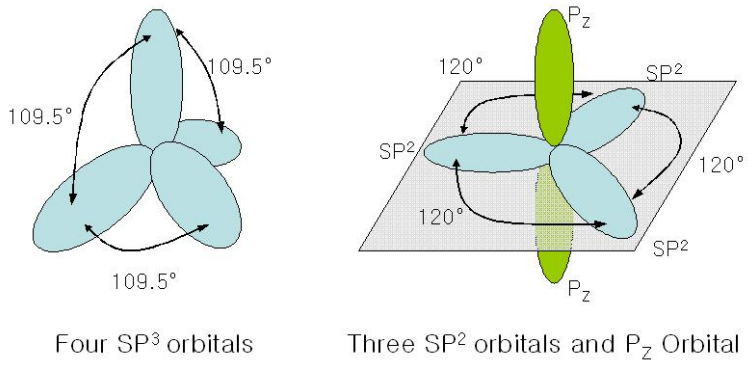

Fig. 1.1 Hybridizations of a carbon atom

Since it is relatively difficult to synthesize stable and well performing n-type organic semiconductors, most research has been conducted on devices with high performance p-type semiconductors such as pentacene, copper phthalocyanine (CuPc), and regioregular poly(3-hexylthiophene) (P3HT) (Fig. 1.2). Examples of widely used electron transporting materials are fluorinated copper phthalocyanine (F_{16}CuPc) and C_{60} (Fig. 1.2). The n-type materials are necessary to fabricate organic light emitting diodes and complementary circuits, which are regarded as a promising circuit technology for organic semiconductors due to their low power consumption and high noise margins. A

perylene derivative, N,N'-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboxiimide) (PDI-8CN_2), is synthesized and shows air stable performance when used in a transistor [12].

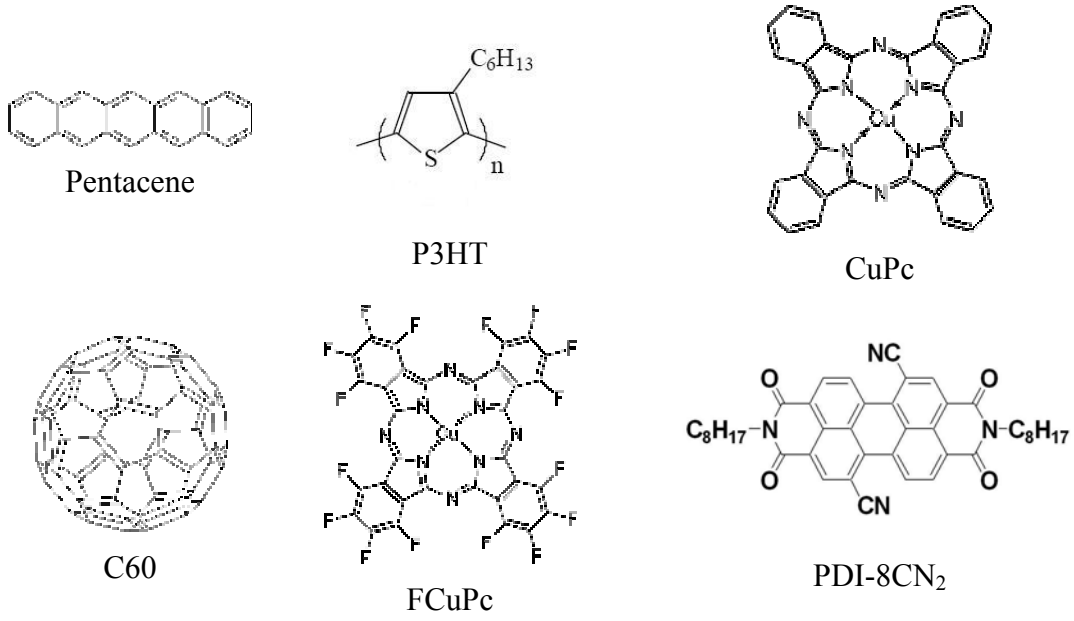

Fig. 1.2 organic and polymer semiconductors.

In the case of dielectrics, SiO_2 is a conventional gate dielectric in inorganic semiconductor FETs. It is also used in OFETs since it is chemically stable and is virtually leakage free. Although SiO_2 dielectric can be used in flexible circuit application implementing silicon and silane precursors, polymeric dielectrics are getting attention because they can be synthesized according to the demands such as surface characteristics and processibility. After these materials are implemented as a thin film dielectric, usually by the spin process, the solvents are removed and polymers are

designed to cross-link with each other to thermoset. Once they thermoset it is generally difficult to reverse the status, i.e. dissolve the thin film into the aqueous state. One of most used polymeric dielectrics is poly(4-vinylphenol) (PVP) [13, 14] because it forms a thin film with poly(melamine-co-formaldehyde) as a cross-linker and can be easily etched with oxygen plasma for further process (Fig. 1.3). Although a thin film of PVP with cross-linker forms a cross-linked film, it has pores inside the film. The pores may nest external molecules, which can behave as impurities. The amount and size of these pores depends on the degree of linking process.

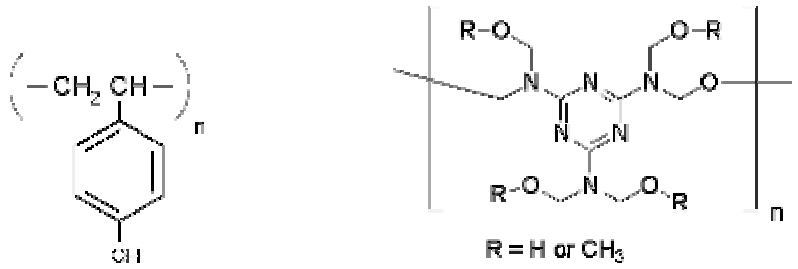

Fig. 1.2 Poly(4-vinylphenol) (left) and poly(melamine-co-formaldehyde) (right)

1.2.2 STRUCTURE OF AN ORGANIC FIELD-EFFECT TRANSISTOR

There are two typical structures for an OFET, which are known as a top contact structure and bottom contact structure. The schematics of these structures are shown in Fig. 1.3. In a top contact structure, an organic semiconductor is deposited on top of the gate dielectric layer. Source and drain electrodes are then defined on top of organic semiconductor. Prior to semiconductor deposition, the dielectric surface can be treated

with surface modifiers which, in general, form a self-assembled monolayer (SAM). SAMs usually provide a hydrophobic surface to organic semiconductors so that they can easily form ordered thin films. Hexamethyldisilazane (HMDS) [15] and octadecyltrichlorosilane (OTS) [16] are some of the SAMs used for the dielectric treatment. In order to coat metal electrodes, molecules such as nitrobenzenethiol (NBT) with the thiol functional group (-SH) are used [17, 18, 19]. Depending on the fabrication method, the gate electrode may be defined last so that the transistor structure is not upside-down. In this configuration the source/drain electrodes are not directly accessing the dielectric interface at which the field induced charge carriers are accumulated. These charge carriers are injected vertically from an electrode to the accumulation layer, move parallel to the dielectric surface, and are collected into the other electrode. Even though this structure has inherent demerit, the top contact structure is still favored because of the ease of fabrication with a shadow mask.

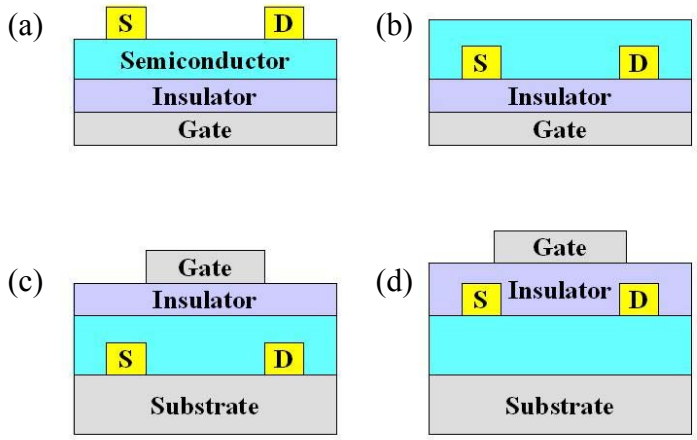

Fig. 1.3 Device structure for organic field-effect transistor. (a) and (c) are top contact structures; (b) and (d) are bottom contact structure.

In the bottom contact structure source/drain electrodes are directly connected to the charge accumulation layer like the conventional inorganic MOSFET. It could be upside-down structure depending on the gate electrode like the one shown in Fig.1.3(b). This structure is better than the top contact structure in terms of the route along which the charge carriers travel but, the contact between source/drain electrodes and semiconductor is not a passive resistor which is the case in an inorganic MOSFET. The resistance of the contacts varys depending on operation environment such as bias, temperature, and time. SAM treatments become crucial in this configuration because they screen out the influence of a metal electrode on a semiconductor or provide intermediate energy states for charges to be injected into a semiconductor [17, 18, 19]. In order to understand the performance of a newly synthesized transistor component, the performance of an OFET

should be studied carefully. The conventional device characterization utilizing the source-drain currents from various samples is not enough to give clear picture of the device behavior. This is because the electrode contact is inherent in a FET structure and hard to decouple the resistance of the contact and channel. Researches are actively being performed on contact characterization [20, 21] because it becomes dominant when a device channel length shrinks below submicron.

1.2.3 ISUSSUES IN SUBMICRON AND NANOSCALE OFETS

Along with technology development, the demands for high performance OFET applications have increased. Some of these demands are high-speed operation at low voltages, environmental stability, and device integration. The current limitation on the operation speed of OFET based circuits is due to the low field-effect mobility of organic semiconductors, which is below 10 cm^2/Vs. It was believed that circuits based on OFETs would not suitable for applications operating at high speed. The communication frequencies used in radio-frequency identification (RFID) tags range from 125 kHz to 2.45 GHz. Among them the operation speed of 13.56 MHz was chosen by Federal Communications Commission (FCC) to transmit data effectively over longer distance. This speed was believed to be out of range that OFET could operate but recently it has been reported an OFET based full wave rectifier successfully operated at the speed [22].

It has been shown that the operation speed of a ring oscillator increased with decreasing channel length [23] but the research has been conducted on OFETs whose channel length was longer than 2 μm. Ideally the switching frequency of a transistor increases with decreasing channel length [24] if the properties of a transistor don't change. This will increase the operation speed of a circuit with submicron OFETs if designed properly.

1.2.4 NUMERICAL ANALYSIS OF ORGANIC FIELD-EFFECT TRANSISTORS

Although analytical models based on extracted device characteristics are useful and physically accurate, the extension to include multiple effects such as many transport mechanisms, field-dependent mobility, carrier-density dependence of transport, contact injection details, etc. make them very cumbersome and inconvenient to use. It is therefore desirable to develop a numerical model that includes all of the physics of analytical models. Simulation has proven vital in the development of inorganic transistors and there are many commercially available simulation tools for these devices such as MEDICI and PADRE. Unfortunately, model development for OFETs is still in the early stages so organic transistor models were either based on inorganic modeling packages [25] or were incomplete analytical approaches that captured one or two physical aspects of the problem [26]. The use of inorganic packages can never capture the complexity of the transport and injection phenomena that dominate organic transistor operation. There have been some reports on simulation characteristics of OFETs [25,

27] but transport related issues have not been described well in the bottom contact structure [28, 29]. In order to implement these requirements, it is necessary to create a simulation tool with a programming language or tool such as C or MATLAB.

References

[1] H. Shirakawa, E. Louis, A. G. MacDiarmid, C. K. Chiang, A. J. Heeger, J. Chem. Soc. Chem. Commun., 16, 578 (1977)

[2] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger, and Z. Bao, Appl. Phys. Lett., 78, 2229 (2001)

[3] C.W. Tang and S. A. VanSlyke, Appl. Phys. Lett., 51, 913 (1987)

[4] P. Peumans, V. Bulovic, and S. R. Forrest, Appl. Phys. Lett., 76, 3855 (2000)

[5] K. Tsukagoshi, J. Tanabe, I. Yagi, K. Shigeto, K. Yanagisawa, Y. Aoyagi, J. Appl. Phys., 99, 064506 (2006)

[6] Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates, and M. McCreary, Nature, 423, 136 (2003)

[7] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, Nature, 434, 194 (2005)

[8] T. Holstein, Ann. Phys. (N.Y.), 8, 325 (1959)

[9] D. Emin, Phys. Rev. Lett., 25, 1751 (1970)

[10] N. Karl, J. Marktanner, R. Stehle, and W. Warta, Synth. Met., 42, 2473 (1991)

[11] R. M. Glaser and R. S. Berry, J. Chem. Phys., 44, 3797 (1966)

[12] B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks, Appl. Phys. Lett., 88, 082104 (2006)

[13] H. S. Byun, Y.-X. Xu, and C. K. Song, Thin Solid Films, 493, 278 (2005)

[14] J. Lee, D. K. Hwang, J.-M. Choi, K. Lee, J. H. Kim, S. Im, J. H. Park, and E. Kim, Appl. Phys. Lett., 87, 023504 (2005)

[15] H. Y. Choi, S. H. Kim, and J. Jang, Adv. Mater., 16, 732 (2004)

[16] Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, IEEE Elect. Dev. Lett., 18, 606 (1997)

[17] D. J. Gundlach, L. Jia, and T. N. Jackson, IEEE Elect. Dev. Lett., 22, 571 (2001)

[18] I. Kymissis, C. D. Dimitrakopoulos, and S. Prurushothaman, IEEE Trans. on Elect. Dev., 48, 1060 (2001)

[19] A. Salleo, M. L. Chabinyc, M. S. Yang, and R. A. Street, Appl. Phys. Lett., 81, 4383 (2002)

[20] K. Seshadri, and D. Frisbie, Appl. Phys. Lett., 78, 993 (2001)

[21] L. Burgi, H. Sirringhaus, and R. H. Friend, Appl. Phys. Lett., 80, 2913 (2002)

[22] R. Rotzoll, S.h Mohapatra, V. Olariu, R. Wenz, M. Grigas, O. Shchekin, K. Dimmler, and A. Dodabalapur, Mater. Res. Soc. Symp. Proc. 871E, I11.6 (2005)

[23] W. Clemens, W. Fix, J. Ficker, A. Knobloch, and A. Ullmann, J. Mater. Res., 19, 1963 (2004)

[24] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York, 1982)

[25] M. A. Alam, A. Dodabalapur, and M. Pinto, IEEE Trans. on Elect. Dev., 44, 1332 (1996)

[26] G. Horowitz and P. Delannoy, J. Appl. Phys. 70, 469 (1991)

[27] N. Tessler and Y. Roichman, Appl. Phys. Lett., 79, 2987 (2002)

[28] M. J. Deen, O. Marinov, S. Holdcroft, W. Woods, IEEE Trans. on Elect. Dev., 48, 1688 (2001)

[29] S. Martin, J.-Y. Nahm, and J. Kanicki, J. Elect. Mater., 31, 512 (2002)

CHAPTER 2 NUMERICAL ANALYSIS OF AN ORGANIC FIELD-EFFECT TRANSISTOR

2.1 Introduction

The development of a numerical model for OFETs is still in the early stages and not much attention has been paid to this aspect due to the lack of analytical models describing the behavior of an OFET, that are yet to be well developed. Since a tool performing numerical analysis on inorganic devices cannot simulate an OFET correctly with the physical models developed for inorganic materials, a new tool needs to be developed with physical models for organic devices. There were reports on simulation of OFETs [1-3] but transport related issues have not been described well. In order to incorporate the physics in such a tool, it is best to create this tool with a programming language such as C or MATLAB, which provides considerable freedom to include physical models as per requirement.

We developed a simulation tool, OSim, which was written in MATLAB script and the programming language C. The user interface and report parts were implemented using MATLAB script because MATLAB has well developed graph modules such as the one shown in Fig. 2.1. Two main sections involving calculations, the current continuity and Poisson's equation solvers, were written in C and compiled in order to speed up the calculations (refer to the Appendix A for the code). Our model

aimed at including physical models and application environments that are often necessary for an accurate description of OFETs, on demand. For comparison and reference purposes, OFETs were modeled in MEDICI, which provided a reasonable description of the basic behavior of a transistor.

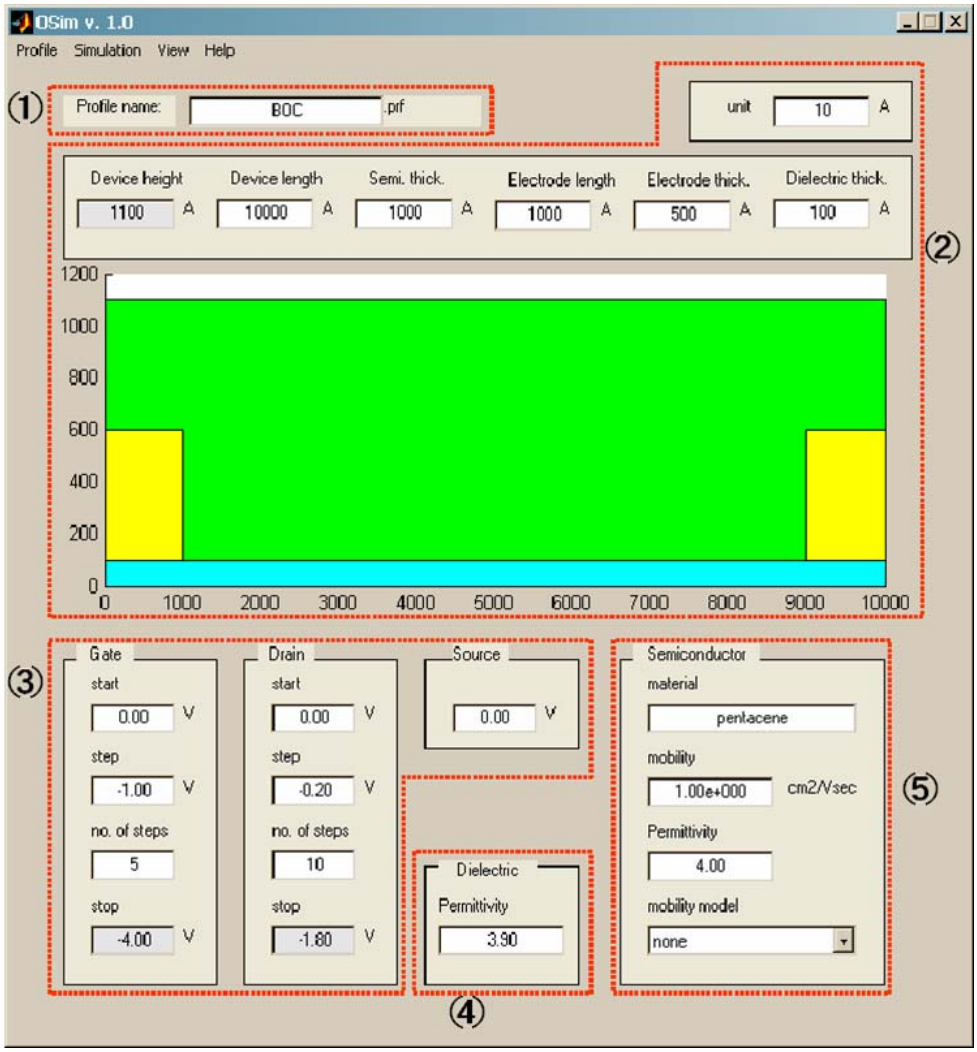

Fig. 2.1 The user interface of OSim written in MATLAB script. The section (1) is for a simulation profile in which the simulation parameters are saved. The device dimensions are defined in section (2). The sections (3), (4), and (5) are the bias conditions, permittivity, and semiconductor types, respectively.

2.2 Numerical modeling of an OFET with a bottom contact structure

In a simulation tool, a device structure is represented as a mesh network, in which every node has values describing the region around it. In MEDICI, a mesh network is represented by the finite element method, which uses arbitrary triangles. Since arbitrary triangles can make any shape easily, nodes can be placed close in a region that requires precise calculation. This region can be a dielectric interface or source/drain electrode contacts, since the state of the region changes significantly within a short range. For example, the induced or inversion charges accumulate at the dielectric interface to form a channel and the thickness of the channel is very small compared to the rest of the device. Likewise, less calculation points can be assigned for a region, the state of which does not change much in the course of operation. Such a region is, for instance, the bulk of a substrate. However, the ease of designing an arbitrary device structure comes at the price of intensive computational complexity.

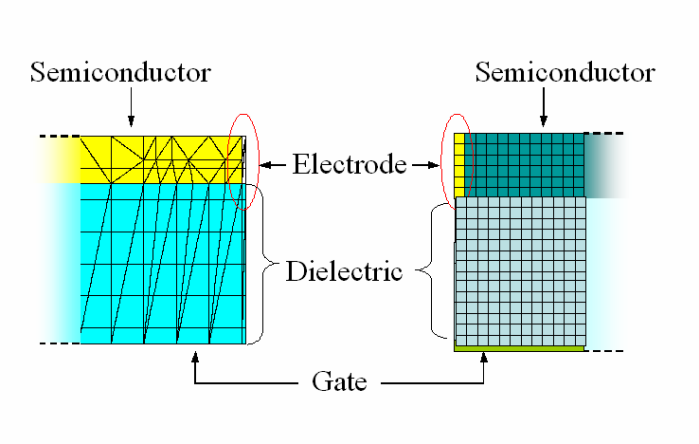

Fig. 2.2 Device structures in MEDICI (left) and OSIM (right)

In OSim, a mesh structure is defined by the finite difference method, which uses rectangles of the same size. Since the size of the rectangles is constant, unnecessary calculation points may be defined in some areas. However, sub-regions can be easily defined and different properties can be assigned with this structure as shown in Fig. 2.3. Since in a typical OFET, the semiconductor forms a polycrystalline thin film, the channel can be conveniently split up into three regions: injection at the electrode contact, intra-grain and inter-grain carrier transport. Charge motion in each of these regions, for example, possessed different dependences on operating environments such as electric fields and temperature.

In OFETs, mobility is influenced by several factors such as parallel and perpendicular electric fields, carrier density, trap within the grain, at the interface with the insulator, and grain boundaries trapping [4-6]. In many cases, a high contact resistance

at the electrode and semiconductor interface is a feature in the bottom contact structure [7-10]. Part of the high resistance is due to the disordered region caused by a metal electrode as shown in Fig. 2.4. The size of the grains becomes smaller as they are formed close to the metal electrode. This justified the fact that the effective mobility in the vicinity of the metal electrode was lower than the mobility in other regions in the channel.

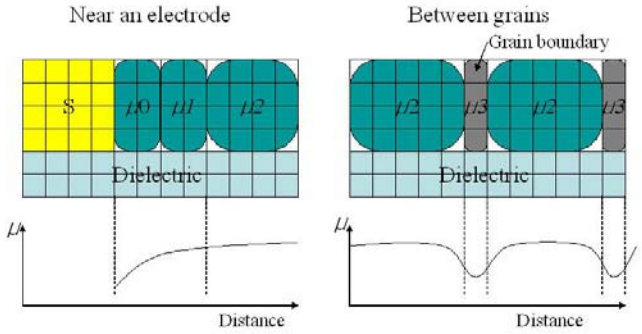

Fig. 2.3 Sub regions for the electrode contact, grain, and grain boundary

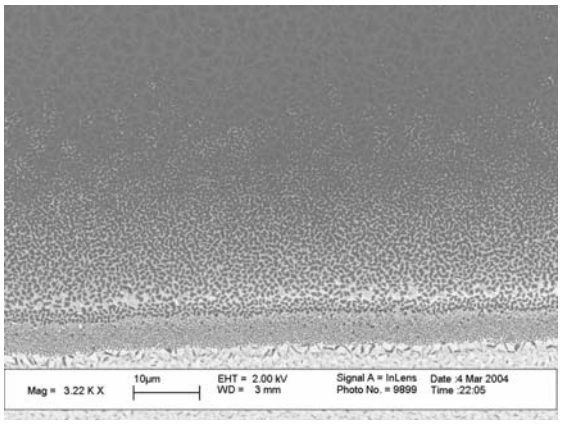

Fig. 2.4 Disordered morphology near a metal electrode (bottom of the picture) taken by SEM

All charges in the channel induced by the gate were assumed to be free charges that could contribute to source-drain current [4] and is given by

$$Q_{total} = Q_f = CV_y$$

where Q_f is the free charge, V_y is the voltage of a channel at the distance y from the source electrode, and C is the capacitance of the gate dielectric. To calculate the charge distribution in a device, the current continuity equation and Poisson's equation were solved [11]. Since only one charge carrier was considered in an OFET, the current continuity equation for a hole is

$$\frac{\partial p}{\partial t} = -\frac{1}{\varepsilon}\nabla \cdot J_p + (G - R)$$

where J_p is the hole current density, and G and R are the generation and recombination rates, respectively. Since the induced charges were accumulated in less than one or two monolayer(s) [12, 13], the channel was modeled using a single layer of rectangles in the mesh network. Assuming the device was in steady state the equation became

$$\nabla \cdot J = \nabla \cdot (Q_f \mu \mathrm{E}) = \frac{d}{dy}(Q_f \mu \mathrm{E}) = 0.$$

When the hole mobility was assumed to be constant and the truncated Taylor series was used to apply the equation into the discrete mesh network [14], we obtained

$$\frac{d^2 V_y}{dy^2}(V_G - V_y) - \left(\frac{dV_y}{dy}\right)^2 = 0$$

$$\frac{V_y(y+\Delta y)-2V_y(y)+V_y(y-\Delta y)}{\Delta y^2}\left(V_G - V_y(y)\right)-\left(\frac{V_y(y+\Delta y)-V_y(y-\Delta y)}{2\Delta y}\right)^2 = 0$$

where V_G was the gate voltage and Δy was the distance between the neighboring nodes.

The two-dimensional Poisson's equation is

$$\frac{\partial^2\phi}{\partial x^2} + \frac{\partial^2\phi}{\partial y^2} = -\frac{\rho(x)}{\varepsilon}$$

where the symbols have their usual meanings. Two dimensional truncated Taylor series was also used to apply the equation to the mesh network. For the boundary condition, the Dirichlet boundary condition was used to define the electrodes [3, 14]. A point with the Dirichlet attribute has a fixed voltage value and this voltage is not changed or updated by the Poisson solver. The edge of the semiconductor however, assumed the Von Neumann boundary condition which defined the normal component of the electric field at the edge to be constant [3, 14].

In order to calculate the source-drain current it was assumed that all induced charges contributed to the source-drain current, which is expressed by [4]

$$G = \left|Q_f\right|\mu$$

where G is the conductivity of the channel. The drain-source current was calculated by

$$I_d = \frac{W}{L}\int_0^{V_d} G(V_y)dV_y .$$

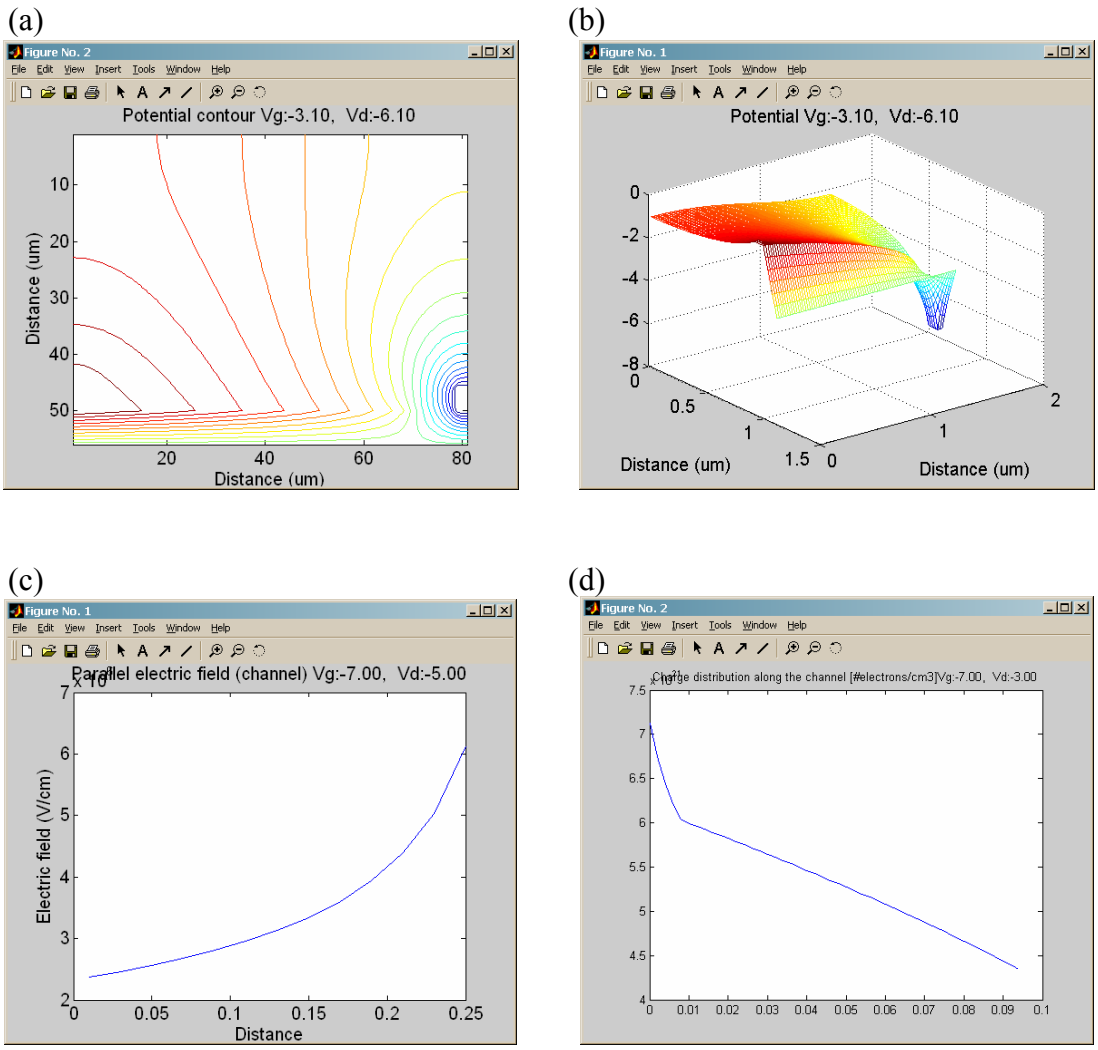

Fig. 2.5 Electrostatic potential distribution in (a) two and (b) three dimensional representation. (c) Electric field parallel to the dielectric surface. (d) Charge distribution along the channel.

The electrostatic potential, electric field, and charge distributions inside the device are shown in Fig. 2.5 using MATLAB's built-in graph functions. The transfer characteristics from the model done in MEDICI for a bottom contact pentacene FET is shown in Fig.2.6 (refer to the Appendix B for the code). A 1000 Å thick layer of SiO_2 served as the gate dielectric. The metal electrode formed a Schottky contact with pentacene. A hole mobility of 0.1 cm^2/Vs characterized from an OFET was used. The channel length was scaled down to 21 *μm* for quicker simulation and the result was scaled up to 840 *μm*. The measurement data was from a pentacene FET, the channel width and channel length of which, were 10,000 *μm* and 840 *μm* respectively. Though the simulation result agreed well with the measurement data, the parameters used in this modeling scheme did not bear a meaningful relation to the physics taking place in the OFET.

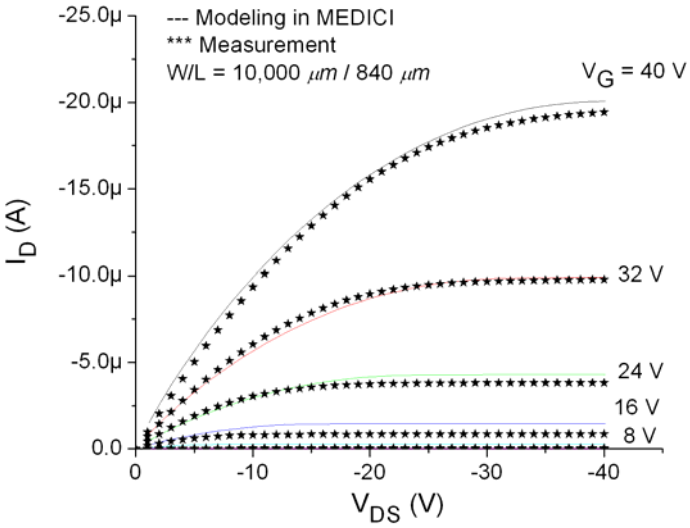

Fig. 2.6 Transfer characteristics from modeling done in MEDICI and a pentacene FET.

The same pentacene FET was modeled in OSim and the resulting transfer characteristics are shown in Fig 2.7(a). The channel length was scaled down to 1 μm in the simulation for quicker calculation. The carrier density dependent mobility model was implemented [4], which was given by

$$\mu = \alpha(V_G - V_T)^{\beta}$$

where both α and β were to be defined by the electrical characterization. In this modeling scheme, the hole mobility was 0.1 cm^2/Vs and a non-uniform mobility profile was assigned to describe the disorder region in the vicinity of the source electrode. The mobility profile is shown in Fig. 2.7(b). The mobility near the source was lower than the mobility in the rest of the channel. The mobility near the drain electrode was not degraded. This was due to the charge carriers having high kinetic energy as they reached the drain electrode. Consequently, the effect of the electrode contact could be neglected. In order to see the effect of the non-uniform mobility profile, two device models were simulated and the results are shown in Fig. 2.8. The transfer characteristics in Fig.2.8(a) was from an OFET with uniform mobility profile (0.1 cm^2/Vs). Fig. 2.8(b) shows the transfer characteristics of a device with the non-uniform mobility profile shown in Fig. 2.7(b). As a result of the contact region being simulated, the performance of the device degraded, which is always the case in the real OFETs.

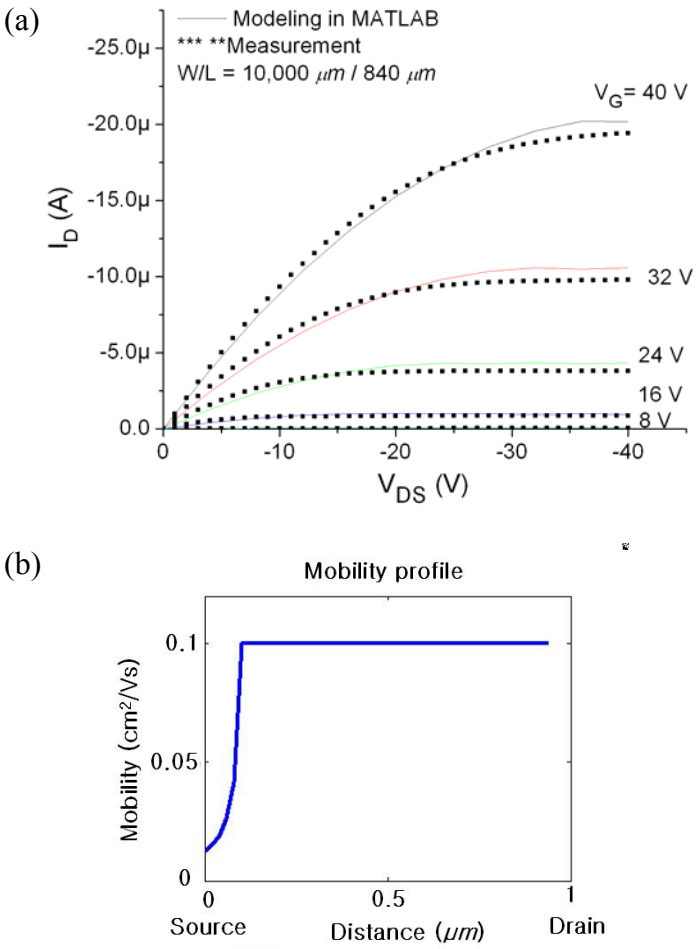

Fig. 2.7 (a) Transfer characteristics from a modeling done in OSim and a pentacene FET. (b) The mobility profile along the channel. The lower mobility profile near the source electrode simulated the contact effect.

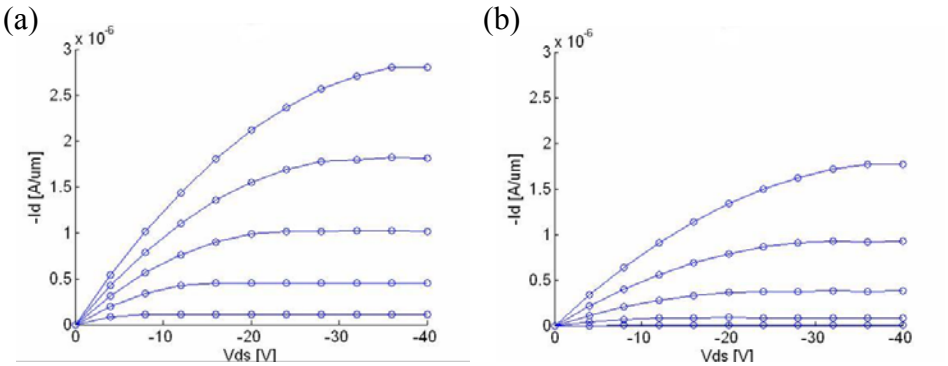

Fig. 2.8 The transfer characteristics from (a) a device with uniform mobility (0.1 cm^2/Vs) along the channel and (b) a device with the mobility profile shown in Fig. 2.7(b).

2.3 Conclusion

Simulations with OSim depicted the electric field, carrier density along the channel and the effect of contact resistance/contact disorder. The resulting transistor characteristics agreed well with experimental data. Carrier-density dependent mobility, grain/grain boundary, and electrode contact issues were implemented in this work. Our model allows us to include new analytical models and modify transport equations as more becomes known about charge transport in an OFET. A multi-grid finite difference method can be implemented to reduce the burden of calculations.

References

[1] N. Tessler and Y. Roichman, Appl. Phys. Lett., 79, 2987 (2002)

[2] Y. Roichman and N. Tessler, Appl. Phys. Lett., 80, 151 (2002)

[3] T. Li, J. W. Balk, P. P. Ruden, I. H. Campbell, and D. L. Smith, J. Appl. Phys., 91, 4312 (2002)

[4] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, J. Appl. Phys., 87, 4456 (2000)

[5] G. Horowitz, R. Hajlaoui, D. Fichou, and A. E. Kassmi, J. Appl. Phys., 85, 3202 (1999)

[6] J. H. Schon and B. Batlogg, J. Appl. Phys., 89, 336 (2001)

[7] I. Kymissis, C. D. Dimitrakopoulos, and S. Prurushothaman, IEEE Trans. on Elect. Dev., 48, 1060 (2001)

[8] D. J. Gundlach, L. Jia, and T. N. Jackson, IEEE Electron Device Lett., 22, 571 (2001)

[9] N. J. Watkins, L. Yan, and Y. Gao, Appl. Phys. Lett., 80, 4384 (2002)

[10] N. Koch, A. Kahn, J. Ghijsen, J.-J. Pireaux, J. Schwartz, R. L. Johnson, and A. Elschner, Appl. Phys. Lett., 82, 70 (2003)

[11] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York, 1982)

[12] M. A. Alam, A. Dodabalapur, and M. Pinto, IEEE Trans. on Elect. Dev., 44, 1332 (1996)

[13] G. Horowitz, R. Hajlaoui, R. Bourguiga, and M. Hajlaoui, Synth. Met., 101, 401 (1999)

[14] E. Kreyszig, Advanced Engineering Mathmatics, 7th ed. (John Wiley & Sons, 1993)

CHAPTER 3 DECOUPLING THE RESISTANCE OF THE CHANNEL AND ELECTRODE CONTACT

3.1 Introduction

In the bottom contact structure, the source and drain electrodes are defined prior to organic semiconductor deposition. Since devices and interconnects can be defined with the conventional photolithography process before organic semiconductor deposition, the bottom contact structure is more favorable than the top contact structure for circuits. However, there are electronic and morphological problems at the metal-to-semiconductor contact in the bottom contact structure. Metal electrodes can affect the growth of organic semiconductor films in close proximity [1]. As a result, near the contact electrodes, organic molecules are not ordered well and this area degrades device's performance. This effect has been noted by several groups [1, 2]. In addition, dipoles may be generated at the interface creating additional barriers to charge injection [3, 4]. The influence of the contact becomes considerable as the channel length of an OTFT becomes smaller and it plays critical role in a transistor's performance in the case of a nanoscale device. In order to minimize the interface problems, metal electrodes are sometimes coated with a SAM to lower their surface energy and/or dope semiconductor near electrodes [2].

Although the metal-to-semiconductor contact can be improved by the surface treatments, the effect of the contact on the performance of an OTFT should be

characterized in detail in order to characterize the device completely. Since the injection characteristics of the contact are not electrically constant as in a passive resistor, it is not easy to decouple the contact and the organic film characteristics. Previous research on contact resistance in OTFTs can be classified into three approaches. The first approach uses the relationship between the total resistance and the channel length [5]. This simple method provides useful information about the channel and contact resistances. In the second approach, the surface potential of a device is measured with AFM-based potentiometry or scanning Kelvin probe microscopy [6, 7]. This method measures the whole potential distribution along the channel but is not applicable to the low temperature measurement and a material which has severe bias-stress effect. The third approach employs a four point probe measurement technique [8, 9] to measures potentials of two points within a channel. This method works well when the contact resistance effect is large but is not accurate for smaller contact resistances. Additionally, the potential distribution in the linear region of an OTFT is not really linear [7]. We developed a method to separate the channel resistance from the metal-to-semiconductor contact resistance in a bottom contact structured OTFT. This method is especially accurate when the contact resistance is small relative to the channel resistance, but also works well when the contact resistance is large.

3.2 A new device structure to decouple contact and channel resistance

In the new approach we describe, we keep the effective channel length constant and place a varying number of floating (unbiased) electrodes between a source electrode and a drain electrode in order to controllably increase the relative effect of contact voltage drop in the channel. Fig. 3.1(a) shows the schematic of a device with two floating electrode. The width of these floating electrodes is the channel width (W) of a device. Charge carriers injected at the source have to be collected and reinjected into the semiconductor at each of these floating electrodes. The channel resistance is extrapolated from the data and used to calculate the source and drain contact resistances.

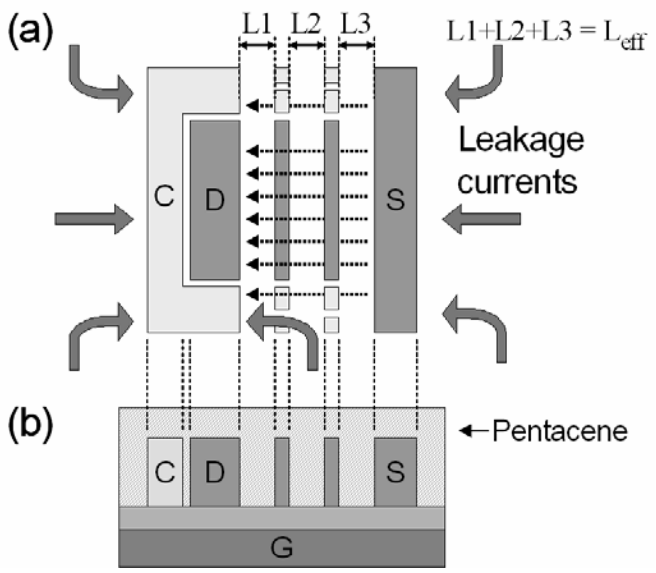

Fig. 3.1 Schematics of device geometry with two floating electrodes (D: drain, S: source, C: collector). The effective channel length, L_{eff}, was kept constant while varying number of floating electrodes.

3.3 Fabrication of OFETs with floating electrodes

Electrodes composed of 30 Å of titanium and 350 Å of gold were defined by an e-beam lithography on top of 1000 Å of thermally grown silicon dioxide/Si. E-beam patterning was used to control the channel lengths precisely. Since this experiment involves comparing several devices, the results are very susceptible to leakage currents, which are mainly gate leakage current flowing through dielectric and fringing current flowing along the marginal space [10]. These currents can be collected by a drain electrode and add to the measurement error. In order to minimize those errors, the active semiconductor region was confined to reduce the leakage and side current. In addition to the confinement we placed an additional electrode, named as collector, right next to the drain of FET of concern to collect those undesirable currents as shown in Fig. 3.1(b). The drain electrode of the inner FET is enveloped by the collector to protect the inner FET further. Additional structures close to the floating electrodes (see Fig. 3.1) ensure that the potential profile at the edges of the device do not have any unusual boundary conditions. The leakage currents coming from outside the channel of concern are collected at the source electrode and the collector. The device dimensions are 48 μm for channel length and 600 μm for channel width. The number of a floating electrode is varies from 0 to 7 and the number of the contact interfaces is 2 to 16 increasing by 2 for each floating electrode. One sample was cleaned with oxygen plasma and coated with HMDS by spin casting. 350 Å thickness of purified pentacene was thermally evaporated in vacuum of 1×10^{-6} Torr. The deposition rate was gradually increased from 0.3 Å/s to 2 Å/s at room temperature. The devices were characterized by an

Agilent 4155C semiconductor analyzer in a Desert Cryogenics vacuum probe station at a pressure of less than 1×10^{-3} Torr. The sample was held in darkness during the measurement. In all the experiments, devices were biased to operate in the linear regime so that charge density along the channel did not change appreciably.

3.4 Experiment and discussion

The effective channel length, L_{eff}, (Fig. 3.1) is kept constant and only the number of contact interfaces is changed. The floating electrodes were evenly distributed along the channel and each added 10 μm to the total channel length. Since floating electrodes, the source electrode, and the drain electrode are identical except their location in a channel, they behave identically if electrical conditions and surrounding materials are same. Since the conductivity of the metal electrode is many orders of magnitude higher than that of the semiconductor, all the carriers flowing through a channel will not overpass a floating electrode but flow through an electrode and are ejected/injected at the electrode edge. The potentials at both end of the floating electrode are virtually same and thus floating electrodes does not add anything to a channel except additional metal-to-semiconductor contact interfaces. All the samples were fabricated together except for the surface treatment in order to rule out the process dependent variations.

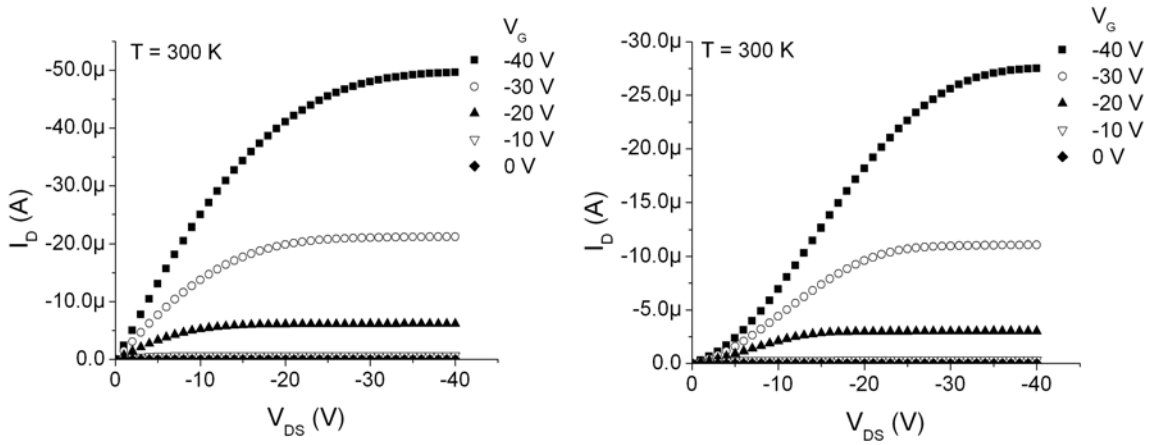

Fig. 3.2 (a) Output characteristics of a FET with pentacene on top of HMDS treated SiO_2. The calculated mobilities at the linear regime and the saturation regime were 0.2 cm^2/Vs. The on/off ratio was about 10^6. (b) The output characteristics of a FET with 7 floating electrodes giving 18 metal-to-semiconductor contact interfaces.

Fig. 3.2(a) shows the drain currents measured from devices having only a source and a drain and no floating electrodes. Fig. 3.2(b) shows the effect of the contact when the number of floating electrodes is 7 introducing 16 metal-to-semiconductor interfaces including a source and a drain. The large number of metal-to-semiconductor contacts caused superlinear increase in the drain current in the linear regime and impede the formation of the saturation region. In addition to the onset of superlinear current-voltage characteristics, the magnitude of the drain current was decreased for the same biasing condition as the number of contact interfaces is increased. This is due to additional voltage drop at the metal-to-semiconductor interfaces (Fig. 3.3). As a result the lateral electric field becomes weaker and is unable to drive enough charges to across

the contacts and throughout the channel in order to get the same magnitude of drain current as in a device without the additional floating electrodes.

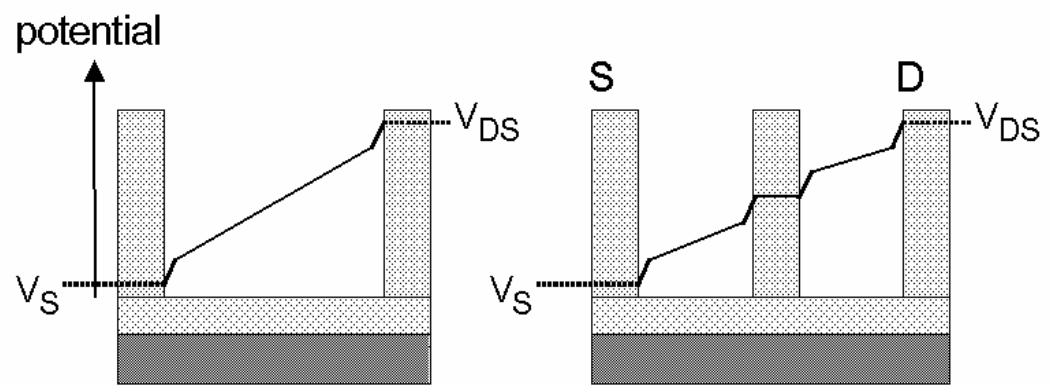

Fig. 3.3 Schematic potential distribution and potential drop at metal-to-semiconductor interface.

It should be noted that we assumed the semiconductor channel characteristics (especially the charge density) are uniform, since devices were operated in the linear regime with high gate voltage. The decrease in the drain current became larger as the number of contact interfaces increased. In order to get the relationship between the voltage drop and the number of contact interfaces, the drain voltages needed to apply to get the same magnitude of drain current from devices were interpolated in the linear regime (Fig. 3.4).

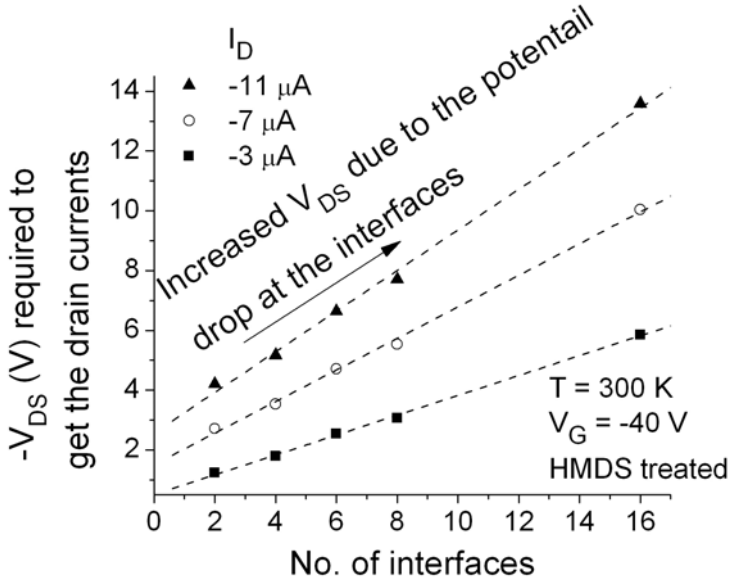

Fig. 3.4 Interpolated V_{DS} and extrapolation of V_{DS0} for the given drain currents

Given the constant gate voltage and the assumption that a channel is nearly uniform across a channel in the linear regime, devices produce the same magnitude of drain current only when lateral electric fields along channels are same. Thus the increase in the drain voltage in Fig. 3.4 as the number of contact interfaces increases is due to the voltage drops at the contact interfaces of the floating electrodes, which is expressed by

$$V_{DS}(n) = V_{channel} + V_{contact}(n) \quad (1)$$

where n is the number of contact interfaces. These additional voltage drops at the contact interfaces are exactly same as those occur at the source/drain contact interfaces.

The dashed lines in Fig. 3.4 are the linear least square regressions to the interpolated drain voltages.

As the magnitude of the drain current increased, the correlation between the interpolated drain voltages became weak. This was attributed to the variation in the induced charge density along the channel. In order to get the given magnitude of drain current from a device with many contact interfaces the drain voltage was raised more to compensate the voltage drop at the contact interfaces. As a result the channel segment at the drain side approached the saturation regime and made the channel carrier distribution uneven. The degree of the correlation was expressed by coefficient of determination (COD). The COD approaches 1 with increasing correlation and becomes 1 when all the data of concern lie on a straight line. We considered drain voltages when the correlations were high enough, i.e., when the COD was larger than 0.92 was used. When the number of contact interfaces becomes zero in Fig. 3.4 along the dashed lines, the extrapolated value, V_{DS0}, is a drain voltage which will be applied only to a channel to get the given magnitude of drain current. This helps determine the intrinsic device characteristics free of all contact effects.

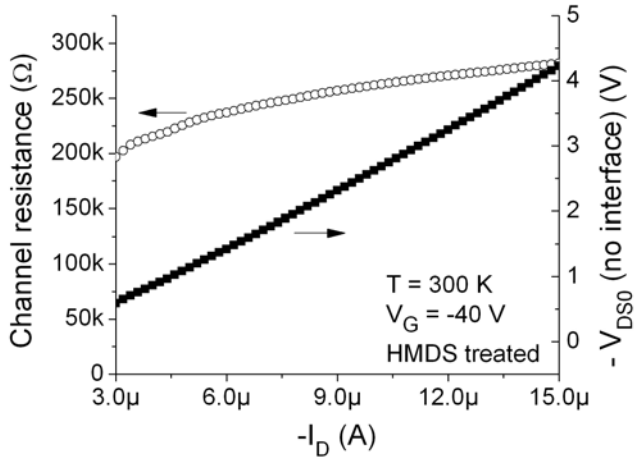

Fig. 3.5 Extrapolated drain voltage, V_{DS0}, applied only to the channel and the channel resistance.

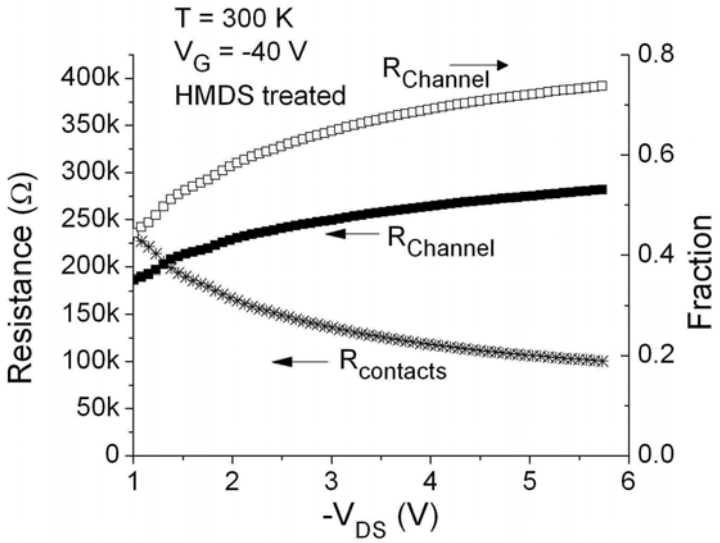

Fig. 3.6 The channel resistance and the source and drain contact resistances for a sample with HMDS treatment.

The resistance of a channel can be calculated by dividing the extrapolated drain voltage by the given drain current. The extrapolated drain voltage and the resistance of a channel versus the drain current are shown in Fig. 3.5. The increase in the channel resistance with increasing drain voltage is attributed to the fact that there are fewer carriers. The channel resistance is used to separate the source and drain contact resistance from the total resistance in a device with a source and a drain (Fig. 3.6). The approximated channel resistance is 290 kΩ with the mobility of 0.2 cm^2/Vs calculated by the first order expressed as

$$R = \rho \times \frac{L}{Wh} \approx \frac{1}{\mu Q} \times \frac{L}{Wh} \quad (2)$$

where the h is the channel thickness. The approximated channel resistance is a bit higher than the extrapolated resistance which is around 230 kΩ but it decreases to 193 kΩ with the mobility of 0.2 cm^2/Vs when source and drain contact correction is done. The metal-to-semiconductor contacts at the source and the drain are forming forward and reverse Schottky diodes respectively [11] and the total resistance decreases as the applied drain voltage increased. The fraction of the channel resistance showed that the channel resistance was the major contribution to the device performance.

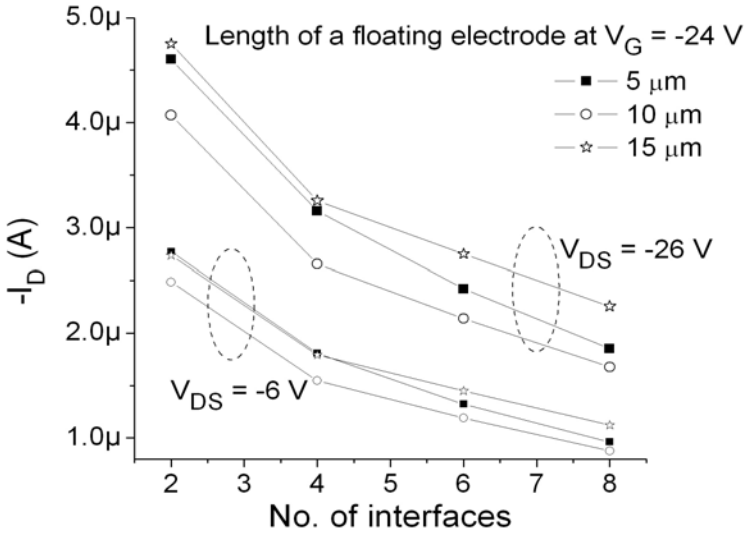

Fig. 3.7 Effect of the size of a floating electrode on device performance in the linear (left) and saturation (right) regimes.

The effect of the size of the floating electrode on the device performance was examined by changing the size of it with fixed width. We used 5 μm, 10 μm, and 15 μm lengths for floating electrodes. Fig. 3.7 shows the drain currents from devices with different floating electrodes in the linear regime and the saturation regime. There are differences in the drain currents but there is no relationship between the size of the floating electrode and the drain current. The differences are rather caused by intrinsic variation existing in each device such as dielectric surface and the structure of the channel.

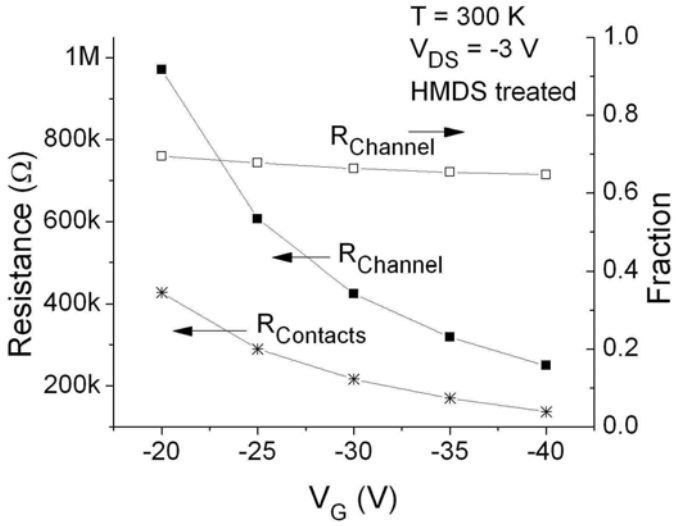

Fig. 3.8 Gate voltage dependency of the channel and the source and drain resistances.

The resistances as a function of the gate voltage are shown in Fig. 3.8. The channel resistance is decreased with increasing gate voltage due to the increase in the field induced charges of which filled up traps and increased channel conductance [12]. The contact resistance was also decreased because the barrier between a metal and a semiconductor was reduced by the increased gate bias [11]. The fraction of the channel resistance was nearly maintained throughout the gate voltage change. This shows clearly that higher induced carrier densities in the channel lower contact resistance. Fig. 3.9 shows the temperature dependence of the channel and the contact resistances. Both resistances decreased with the increasing temperature. The channel resistance decreases due to temperature-assisted hopping [13]. The contact resistance was also decreased, possibly due to more efficient thermionic emission at the interface. The changes in

semiconductor mobility with temperature are consistent with thermally-activated hopping transport [14].

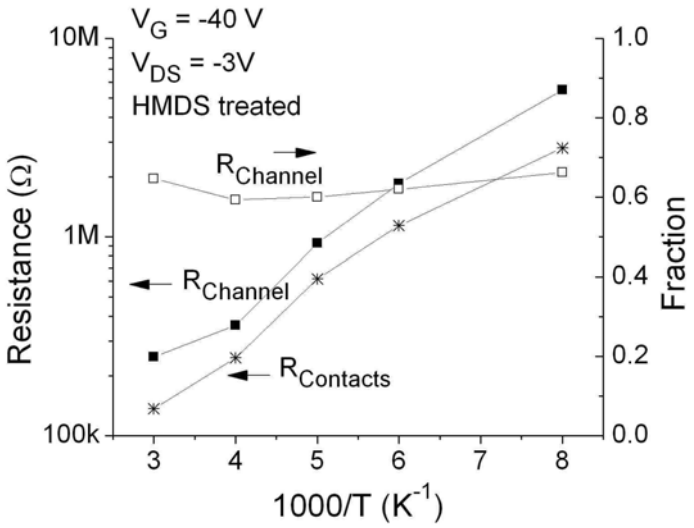

Fig. 3.9 Temperature dependency of the channel and the source and drain resistances.

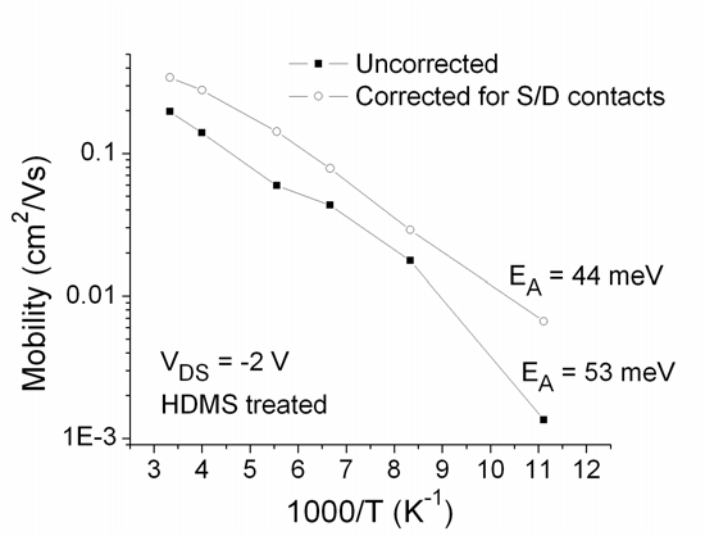

Fig. 3.10 Temperature dependency of linear mobilities from the raw data and the corrected data for the source and drain contacts.

Fig. 3.10 shows the mobility calculated from the raw drain current as a function temperature. The source and drain contact resistance was removed from the raw drain current and corrected mobility was calculated and was also plotted in the figure. The activation energy of the corrected mobility (44 meV) is about 10 meV higher than that of the raw mobility. The corrected mobility at room temperature (300 K) is about 0.32 cm^2/Vs.

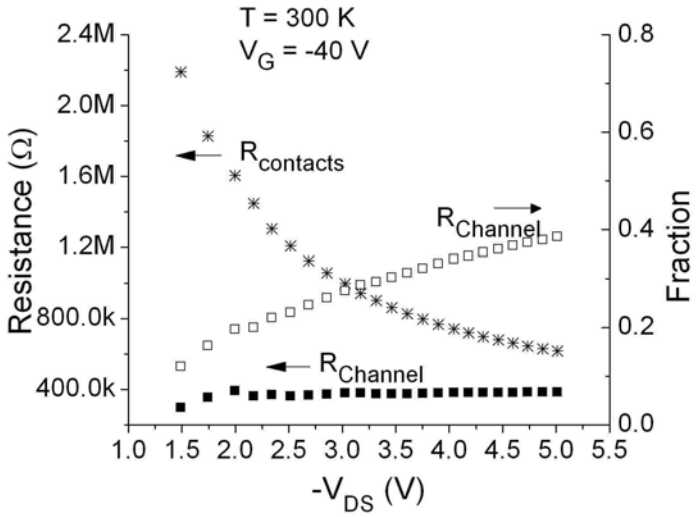

Fig. 3.11 The channel resistance and the source and drain contact resistances for a sample without any treatment.

A sample without any surface or electrode treatment was prepared and characterized for the resistances (Fig. 3.11). Fig. 3.12 and 3.13 show comparison of the channel resistances and the metal-to-semiconductor resistances as a function of gate voltage, respectively. The channel resistance with the HMDS treatment is approximately half of the raw channel resistance. This is because HMDS bonds with SiO_2 and provides a nonpolar trimethylsilyl terminated surface, which is hydrophobic and helps pentacene form ordered grains. However, based on the resistance comparisons in Fig. 3.12 and 3.13 the HMDS treatment influences the metal-to-semiconductor contact interface more than the film ordering. Since HMDS has neither inherent adhesive property to gold surface nor charge carrier modification property such as nitrobenzenethiol [2], the effect was from well-ordered pentacene molecules at the

contact interface. Fig. 3.14 showed the phase of the samples scanned by atomic force microscopy (AFM). The left part of each picture is the gold electrode and right part is the semiconductor channel. The contact interfaces were shown as black lines due to the abrupt change in the height and should be noted because the widths of them were not same. The HMDS treated sample had the narrow contact region and this is possibly responsible for the improved performance.

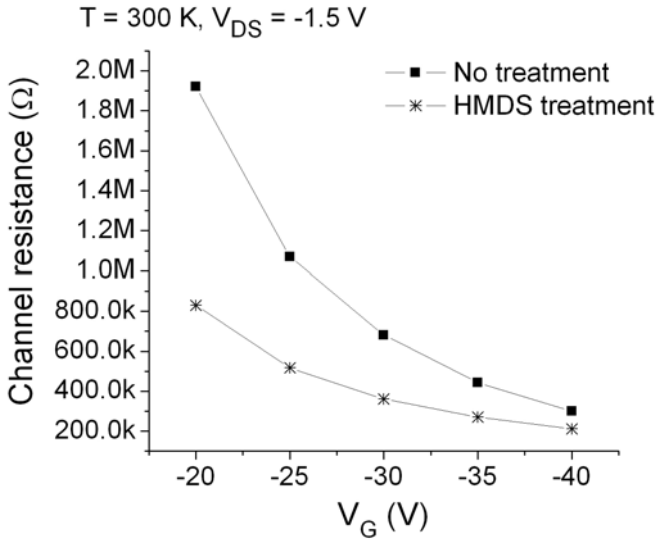

Fig. 3.12. Comparison of the channel resistances for samples with and without HMDS treatment as a function of gate voltage.

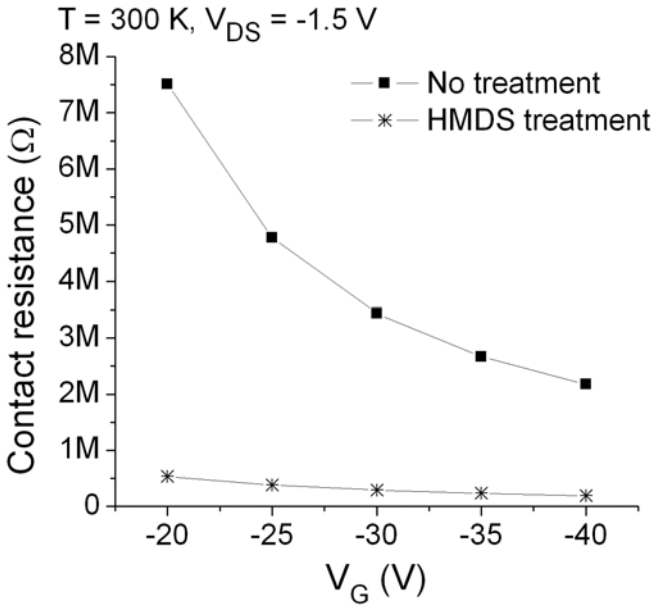

Fig. 3.13. Comparison of the source and drain contact resistances for samples with and without HMDS treatment as a function of gate voltage.

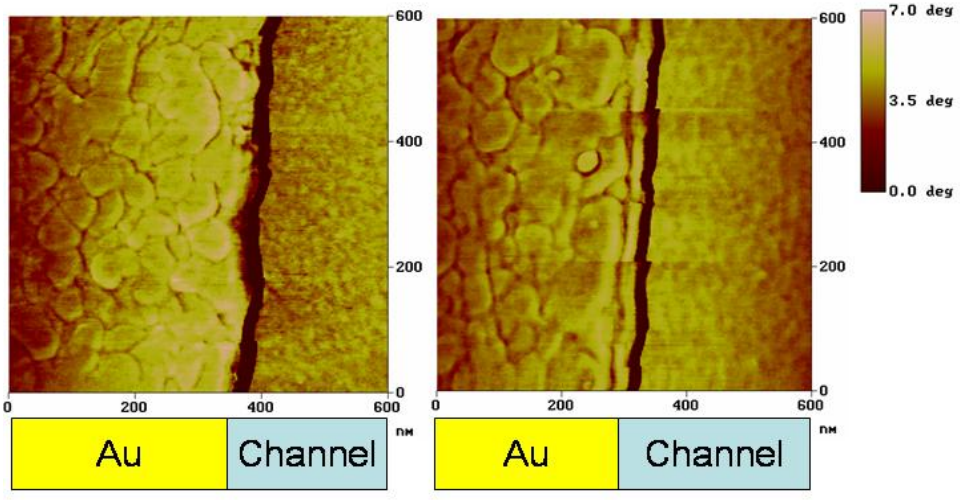

Fig. 3.14. AFM image of samples with (right) and without (left) HMDS treatment at the gold electrode edge.

3.5 Conclusion

We have described an experimental approach to accurately determine the metal-semiconductor contact resistance in organic thin-film transistors in the linear region. To facilitate this measurement, we designed new transistor structures with floating electrodes between source and drain electrodes to separate the film resistance from the source and drain contact resistances. The floating electrodes provide additional metal-to-semiconductor interfaces and consume part of the applied drain-to-source voltage exactly like source and drain electrodes. By changing the number of floating electrodes the relationship between the number of contact interfaces and drain voltage was found and the film resistance was calculated. This design is suitable for inclusion in organic semiconductor test circuits as a way to obtain quantitative information about the contacts as a function of temperature. The effect of gate dielectric surface treatment with HMDS is also examined. The dielectric surface treatment has a beneficial effect on both the contact resistance and the channel mobility. This method is easily applicable to other materials systems. This method of determining the contact resistance is very accurate even when the contact resistance is small relative to the channel resistance.

References

[1] I. Kymissis, C. D. Dimitrakopoulos, and S. Prurushothaman, IEEE Trans. on Elect. Dev., 48, 1060 (2001)

[2] D. J. Gundlach, L. Jia, and T. N. Jackson, IEEE Electron Device Lett., 22, 571 (2001)

[3] N. J. Watkins, L. Yan, and Y. Gao, Appl. Phys. Lett., 80, 4384 (2002)

[4] N. Koch, A. Kahn, J. Ghijsen, J.-J. Pireaux, J. Schwartz, R. L. Johnson, and A. Elschner, Appl. Phys. Lett., 82, 70 (2003)

[5] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, T. N. Jackson, Solid-State Electronics, 47, 297 (2003)

[6] K. Seshadri, and D. Frisbie, Appl. Phys. Lett., 78, 993 (2001).

[7] L. Burgi, H. Sirringhaus, and R. H. Friend, Appl. Phys. Lett., 80, 2913 (2002)

[8] R. J. Chesterfield, J. C. McKeen, C. R. Newman, and C. D. Frisbie, J. Appl. Phys., 95, 6396 (2004)

[9] C. R. Newman, R. J. Chesterfield, J. A. Merlo, and C. D. Frisbie, Appl. Phys. Lett., 85, 422 (2004)

[10] L. Wang, D. Fine, T. Jung, D. Basu, H. V. Seggern, and A. Dodabalapur, Appl. Phys. Lett., 85, 1772 (2004)

[11] R. Brederlow, S. Briole, H. Klauk, M. Halik, U. Zschieschang, G. Schmid, J.-M. Gorriz-Saez, C. Pacha, R. Thewes, and W. Weber, IEEE ISSCC (2003)

[12] C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, J. M. Shaw, Science, 283, 822 (1999)

[13] L. Torsi, A. Dodabalapur, L. J. Rothberg, A. W. P. Fung, and H. E. Katz, Phys. Review. B, 57, 2271 (1998)

[14] R. A. Street, D. Knipp, and A. R. Völkel, Appl. Phys. Lett., 80, 1658 (2002)

CHAPTER 4 AN ORGANIC FIELD-EFFECT TRANSISTOR WITH POLYMER DIELECTRIC

4.1 Introduction

Organic and polymeric materials have received great interest due to the fact that they can be solution processed conveniently for various applications such as printed circuits and flexible displays [1-3]. Since all organic/polymer submicron circuits are the desired goal eventually, organic/polymer materials for electrodes and dielectrics are equally important as are organic/polymer semiconducting materials. Solution processible dielectric materials such as poly(4-vinyl phenol) (PVP) and glass resins are some of the polymeric dielectric materials for low-cost processing on flexible substrates [13-15]. However, the polymeric dielectrics are distinct from inorganic dielectrics in some properties such as surface energy and reactivity to organic solvents. This is due to the fact that SiO_2 is a chemically stable material with ideally no impurity. Since the surface energies of dielectrics have an effect on both formation of a thin film of semiconducting material and the performance of a device, OFETs with the polymer dielectrics may behave differently under certain conditions. Pentacene thin-film transistors with PVP as the gate dielectric were fabricated to investigate the effect of the surface of a dielectric on device performance. Identical pentacene transistors were fabricated with SiO_2 as the dielectric were fabricated for comparison.

4.2 Effect of moisture on OFETs with polymer dielectric

4.2.1 Fabrication of an OFET with PVP dielectrics

PVP and methylated poly(melamine-co-formaldehyde) as a cross-linker were mixed in propylene glycol methyl ether acetate (PGMEA) at two different concentrations. The cross-linker is generally mixed in the solution to increase the chemical resistivity of the dielectric to organic solvents by connecting PVP molecules via covalent bonds. It also reduces the free volume of the dielectric and consequently the dielectric shrinks after cross-linking. The first type of solution (type A) was prepared with cross-linker concentration of ~26.5 wt. %. A recipe type B had less cross-linker (~ 11.5 wt. %) and was prepared to examine the effect of cross-linker on the property of PVP dielectric. All the materials were used as received from Sigma-Aldrich and the solutions were prepared in a nitrogen flow hood and stirred overnight before use. PVP solution was spun on top of bare silicon samples under the normal ambient air. The samples were then cured on top of a hot plate at a temperature of ~180°C in nitrogen ambient for 8 min. Both PVP and SiO_2 dielectric samples were cleaned with oxygen plasma. Hexamethyldisilazane (HMDS) was spun cast onto both types of dielectrics to lower the surface free energies [17]. As will be shown later, the HMDS layer does not screen out the properties of the underlying dielectric layers but still provides a hydrophobic surface to pentacene. A 350 Å thick pentacene film without any purification was deposited onto

a substrate at room temperature at a growth rate of 0.2-0.5 Å/s with a base pressure of 2×10^{-6} Torr. Gold was vacuum deposited through a shadow mask to define source and drain electrodes. All the devices have a channel width to length ratio of 10. Measurements were conducted with an Agilent 4155C semiconductor parameter analyzer and Keithley 6430 sourcemeters. Humidity of the ambient air was between 42-48 % at ~22°C. Between measurements, the devices were reverse biased and then left unbiased for several minutes to recover from the stressed state.

4.2.2 EXPERIMENTS AND DISCUSSION

Fig. 4.1 shows the drain-source current versus drain-source voltage of devices with SiO_2 and PVP dielectrics characterized in the normal air. The devices with SiO_2 dielectrics showed normal responses as field-effect transistors. However, transfer characteristics from devices with PVP dielectrics showed high off currents and no plateaus in the drain currents when operated in the saturation regime. In addition, PVP type B dielectric showed higher breakdown voltage than that of type A.

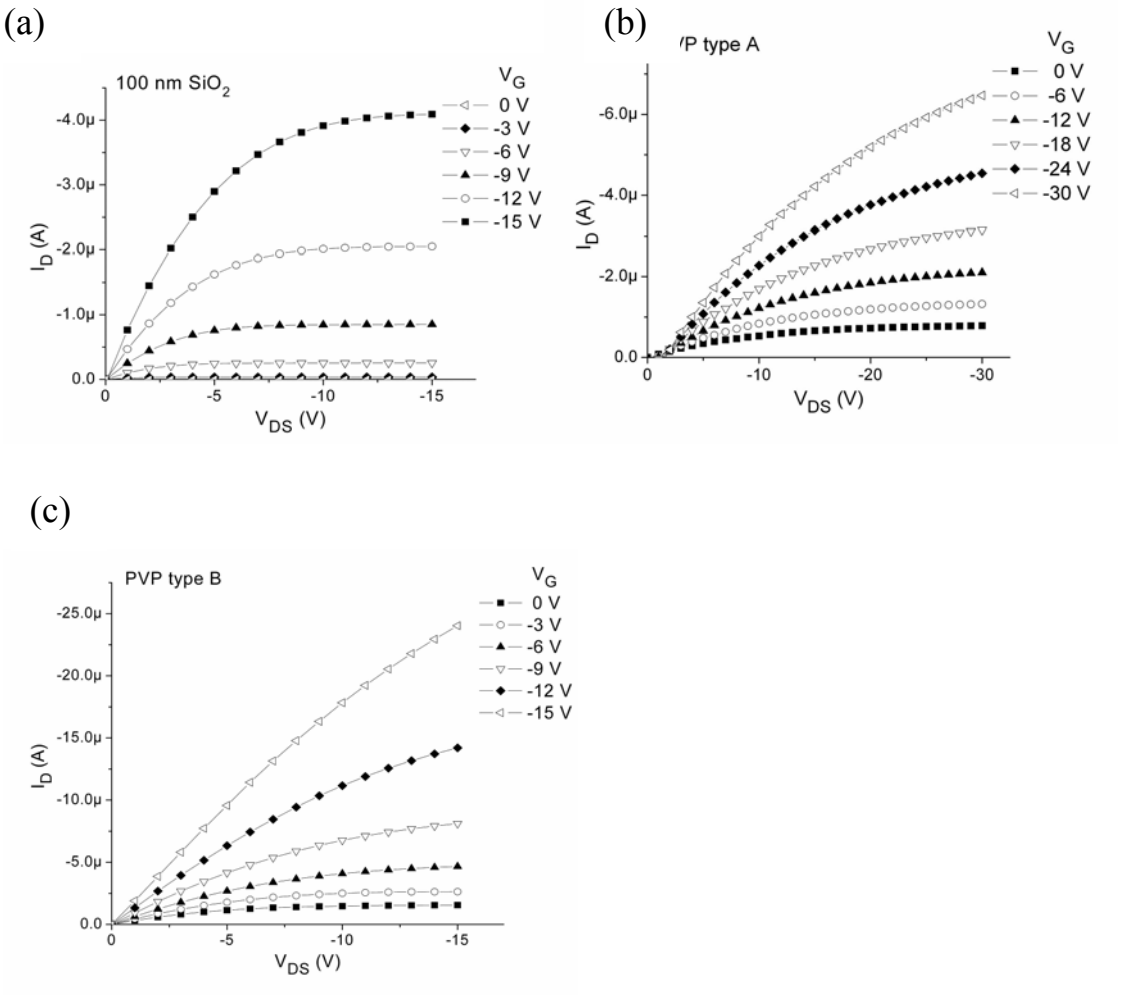

Fig. 4.1 Transfer characteristics of OTFTs with (a) SiO_2, (b) PVP type A, (c) PVP type B. Characterized under the normal ambient. Reprinted with permission from Taeho Jung; Ananth Dodabalapur; Robert Wenz; Siddharth Mohapatra, Appl. Phys. Lett. 87, 182109 (2005). Copyright 2005, American Institute of Physics.

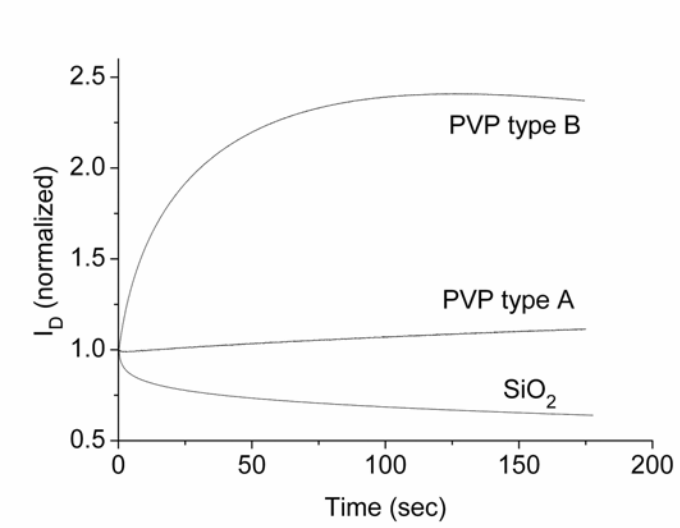

Fig. 4.2 Time dependent drain currents in the saturation regime ($V_G = V_{DS} = -30$ V). The decrease in the drain current with SiO_2 dielectric is due to the bias stress effect. Initial decreases in the current were observed in some responses with PVP dielectric of the recipe type A. Reprinted with permission from Taeho Jung; Ananth Dodabalapur; Robert Wenz; Siddharth Mohapatra, Appl. Phys. Lett. 87, 182109 (2005). Copyright 2005, American Institute of Physics.

In order to examine the different responses of the saturation currents, the devices were biased with constant voltages to operate in the saturation regime. The drain-source current versus time of the devices are showed in Fig. 4.2. The magnitude of drain current decreases with time in devices with SiO_2 dielectric due to the bias stress effect. Some of the possible causes for the bias stress are trapping inside the pentacene or at the dielectric interface [16]. This trapping could be enhanced by the presence of molecules such as H_2O. The opposite responses were observed for devices with PVP dielectrics of

both recipe types. The opposite direction of change in the drain currents indicates that the cause of change occurs not inside the pentacene film but at the dielectric surface. We attribute the difference in the responses to the surface polarization generated by water molecules in the air, which induces extra charge carriers and thus increases the channel conductance. The devices of the recipe type A showed initial decrease followed by continuous increase in the drain current. Whereas the recipe type B devices showed a peak in the current. Considering the initial decrease and slow change in the drain current from the recipe type A devices, which are more highly cross-linked than the type B devices, it appears that the degree of the surface polarization depends on the free volume of the dielectric surface. The onset of decrease in the drain current for type B devices indicates the degree of polarization becomes slowed and is overwhelmed by the bias stress effect. It should be noted that all the samples had an HMDS layer between the pentacene and the dielectric layer but showed different behavior. Based on these results, the properties of the dielectrics beneath the HMDS layer were not screened out totally even though the HMDS layer had changed the surface free energy.

In order to examine the effect of moisture on the drain current, the devices were exposed either nitrogen gas or clean air both with and without moisture. The experimental set up is shown in Fig 4.3. The end of the gas delivery tube was placed close to samples so that when gas was turned on the samples were exposed to the local ambient created by the flow. In the case of devices with SiO_2 dielectric the magnitude of drain current decreased when subject to both nitrogen gas and dry air flowing through the water reservoir [Fig. 4.4(a)], which made the device environment more humid than

the normal air. The decrease of the drain current is partly attributed to trapping at the grain boundaries caused by the water molecules [18]. After stopping delivery of humid gases, the drain current showed rapid increase followed by the plateau, when the bias stress effect was balanced with the recovery by means of releasing of charge carriers from water induced traps. Nitrogen gas and dry air were injected again after the decrease of the drain current was observed. This ensured the devices operated in the normal operation because the effect of trapping caused by moisture was less than the bias stress effect. The drain current increased with the dry gases. The initial small peaks before the changes in the responses were due to the remaining gases inside the gas delivery tube at the sample side.

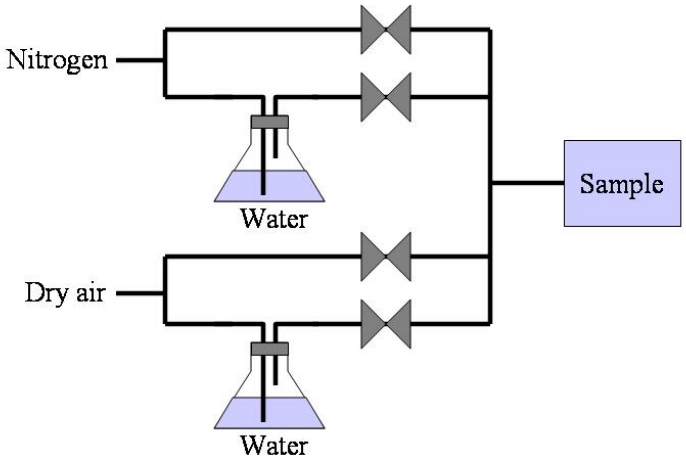

Fig. 4.3 Experimental set up. Both nitrogen gas and dry air were delivered to the sample with/without moisture.

The opposite patterns were obtained from devices with PVP dielectrics of both recipe types. A typical response from the recipe type B devices is shown in Fig. 4.4(b). The increasing drain current increased even more after being exposed to the humid nitrogen gas and dry air indicating the dielectric surface was polarized more by excess water molecules. The drain current decreased after stopping delivery of the moist gases and exposing the devices once again to the ambient air. Then, upon delivery of dry nitrogen, the decrease in drain current is more strongly marked. This clearly shows that moisture is very influential in determining device characteristics of PVP devices.

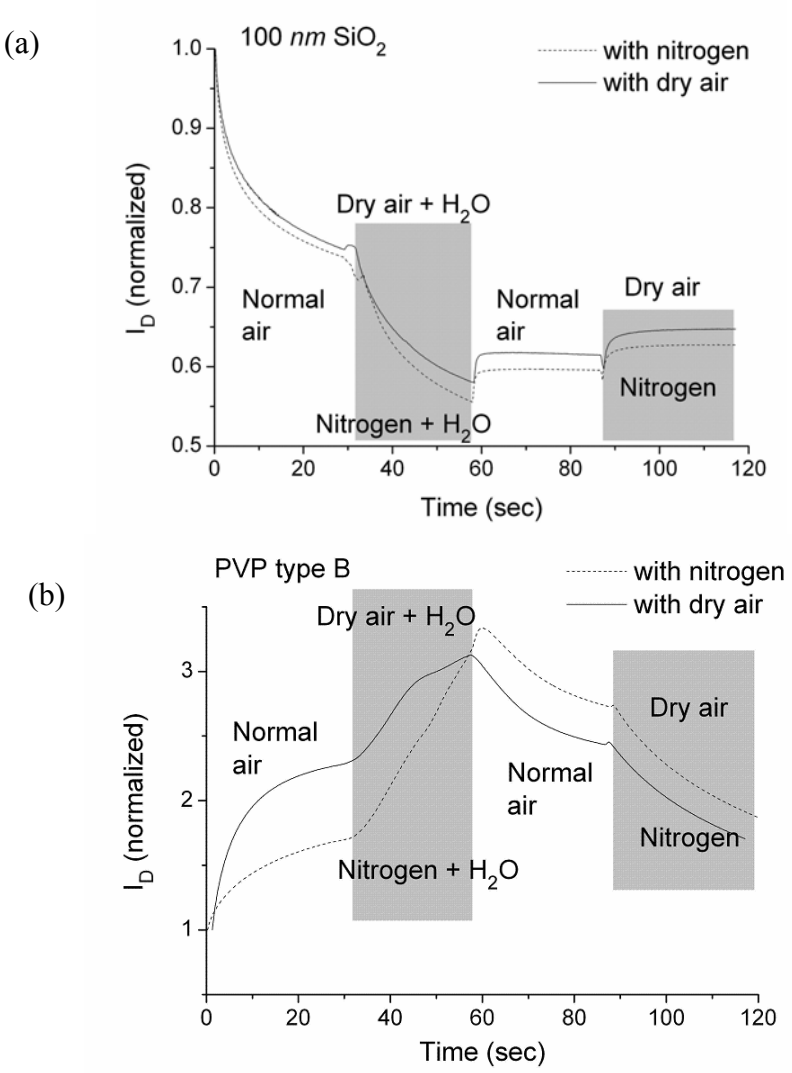

Fig. 4.4 Responses from a device with (a) SiO_2 and (b) PVP dielectrics in the saturation regime (V_G = V_{DS} = -20 V). Dry air and nitrogen gas with/without moisture were delivered to samples during the periods indicated by shades. Samples were exposed to the normal air (42-48 % humidity) otherwise. Reprinted with permission from Taeho Jung; Ananth Dodabalapur; Robert Wenz; Siddharth Mohapatra, Appl. Phys. Lett. 87, 182109 (2005). Copyright 2005, American Institute of Physics.

The effect and response time of dry nitrogen gas and dry air were compared qualitatively by periodically turning the devices on and off [Fig. 4.5]. The devices were turned off long enough to recover to their original state. By so doing, the bias stress can be excluded from the device response to some degree and thus the effect of humidity can be observed more clearly. The duty cycles were determined based on the device responses. The experiment started under the normal humid ambient. After the drain currents from on-states stabilized, the nitrogen gas was delivered to the devices. The magnitudes of the drain currents changed in accordance with the results shown in Fig. 4.4. When this trend was clear, the nitrogen gas was turned off and the devices were once again exposed to the moist air. They were then turned off and then turned on under dry air. Comparing the time scale and the shape of the normalized drain currents shows that the decrease in the response from the devices with SiO_2 dielectrics when nitrogen was turned off was the fastest [Fig. 4.5(a)]. This reaction is due to the water induced charge trapping in the pentacene layer which in turn is attributed to the grain boundaries which were exposed to the environment. The devices with the recipe type A showed the slower and smaller responses to moisture and this was attributed to the lower free volume of the PVP dielectric.

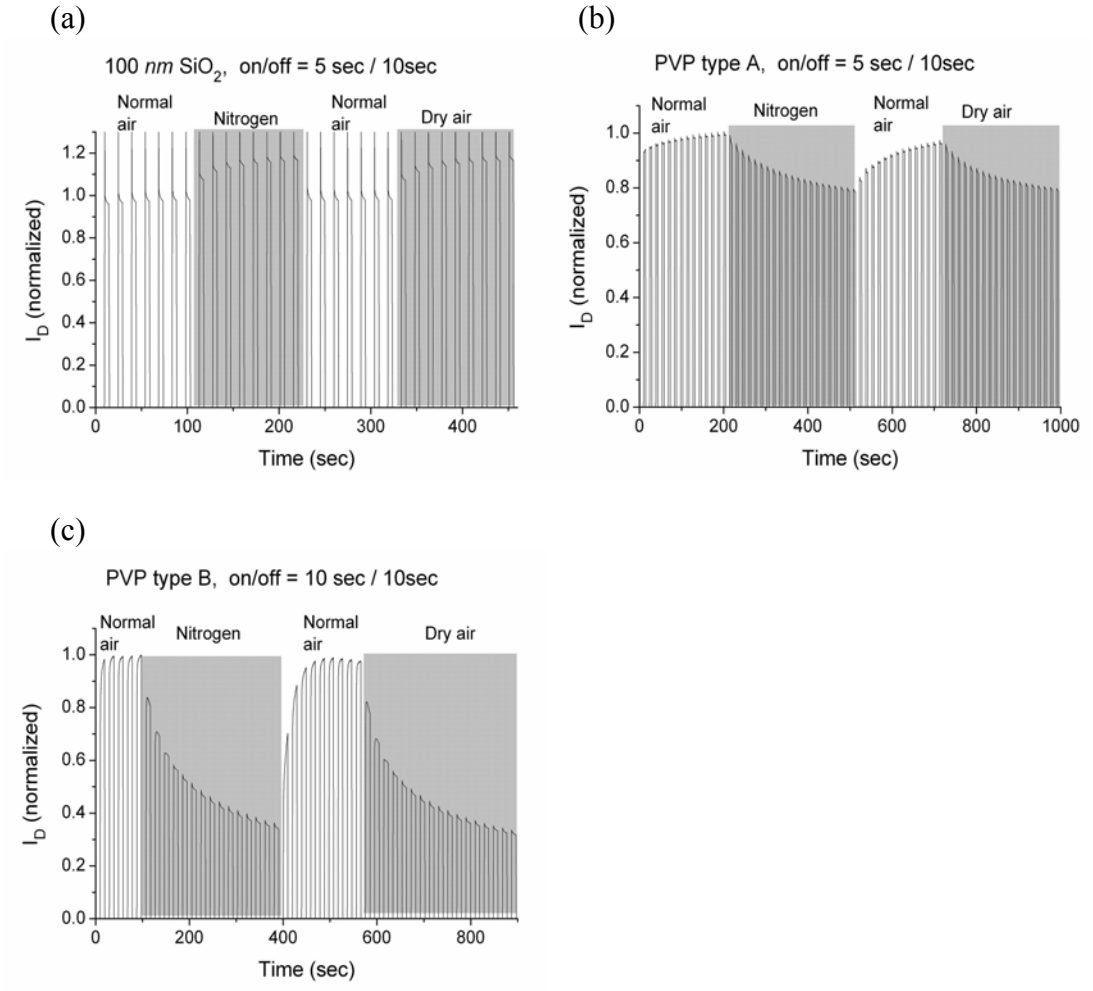

Fig. 4.5 The drain currents with on/off biasing. The devices were in the saturation regime (V_G = V_{DS} = -30 V) when turned on. The bias stress effect was excluded from the observation by changing the duty cycle and the effects of moisture were clearly evident. Reprinted with permission from Taeho Jung; Ananth Dodabalapur; Robert Wenz; Siddharth Mohapatra, Appl. Phys. Lett. 87, 182109 (2005). Copyright 2005, American Institute of Physics.

The clear and marked effects of moisture on the performance characteristics of pentacene transistors with PVP gate insulators were illustrated. The bias stress effect is observed as a decrease in the drain current. When the dielectric is porous water molecules can be absorbed in the dielectric layer causing a greater amount of polarization in the dielectric. This effect can vastly overwhelm the bias stress and cause an increase in the drain current. Based on this experiment the time scale of the polarization depends on the free volume of the dielectric. The effects of moisture or polar molecules on other materials systems can also be significant and must be included in the analysis of mobility. If not, there may be errors as large as an order of magnitude or more in determining mobility from the current-voltage characteristics. The use of surface treatments and self-assembled monolayers also crucially influence the effect of water molecules on device performance, apart from influencing self-assembly of the semiconductor. We have illustrated this effect in PVP gate insulators; however, the effect is more general and is likely to be present in some degree when slightly porous materials are used in TFT fabrication, which is often the case.

4.3 A capacitor with polymer insulator

It was shown that the PVP dielectric caused the polarization. However, it was not enough to prove that surface polarization was the only phenomenon in the course of transistor operation. In order to confirm the behavior of the bulk PVP dielectric with moisture, a device with only PVP needs to be examined. A capacitor having a PVP

dielectric between two metallic electrodes gives a qualitative idea of the contribution of bulk dielectric to the moisture response.

4.3.1 FABRICATION OF A CAPACITOR

Capacitors were made with different ratios of cross-linker to PVP. The component ratios of the dielectrics and devices made with them were same as before. The solutions were spun on heavily doped n-type silicon substrates at the speed of 3000 RPM. The samples were cured for 20 minutes at 180 °C under the ambient. Titanium and gold were deposited using a shadow mask to pattern electrodes. The characterization was conducted at room temperature and pressure and in vacuum at the base pressure of about 5 mTorr at room temperature.

4.3.2 EXPERIMENTS AND DISCUSSION

A HP 4284A precision LCR meter was used to apply 5 mV AC signal oscillating at 1 MHz superimposed on the DC bias signal and measure the capacitance of the devices. Fig. 4.6 shows capacitance-voltage hysteresis of the capacitors with different solution types characterized under the vacuum (~ 5 mTorr). Hysteresis from all the devices was observed under the ambient and it showed no noticeable change after the samples were put in vacuum more than 12 hours. The characterization started from the origin point at which both electrodes were biased to the same ground voltage to prevent

any displacement current. The hysteresis was independent of the direction of the sweep. When the n-type silicon substrate that acted as the gate electrode for the transistors was biased positive with respect to the metal electrodes, the capacitances decreased. The decrease was attributed to the depletion region induced in the n-type silicon electrode, which was connected in cascade to the dielectric layer [19]. As the bias voltage increased the depletion layer became thicker and the capacitance continued to decrease. When the bias voltage was decreased, capacitance of a type A capacitor increased by a small amount. However, a large amount of the hysteresis was observed from the type B capacitor. It should be noted that the hysteresis was not observed when the silicon substrates were biased negative with respect to the metal electrode, which was the biasing condition for operating the OFETs in the previous section.

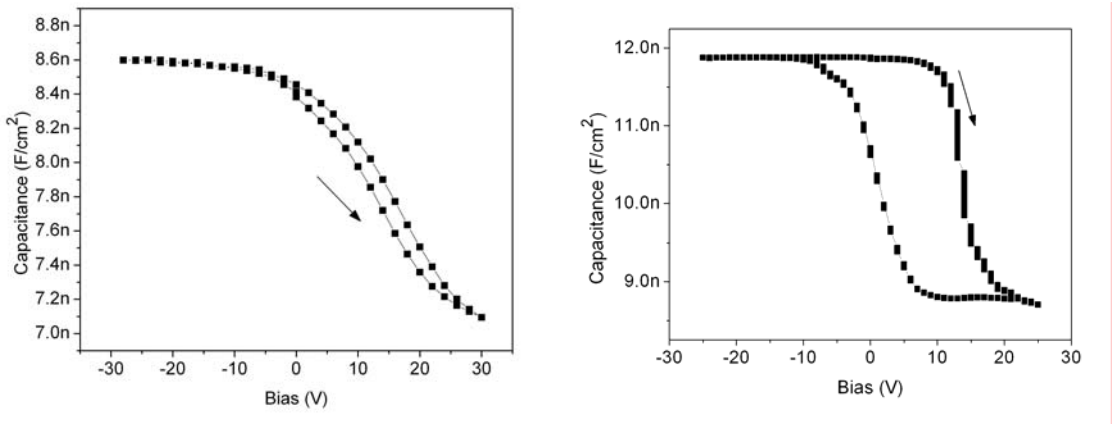

Fig. 4.6 Capacitance-voltage hysteresis of devices measured under the ambient. (a) type A and (b) type B. The silicon substrate was biased positive with respect to the metal electrode when the bias was positive.

As has been reported previously, the observed hysteresis is attributed to the defect in the dielectric [20]. As was the case with the OFETs with PVP dielectric, it was observed that the PVP dielectric with less cross-linker was more susceptible to the external impurity.

Fig. 4.7 shows the change in the capacitance with time and bias. Each bias condition was maintained for around 10 seconds. The lower-left inset in Fig 4.7 shows capacitance characterized over a 20 second period. The capacitance decreased when the bias was kept constant. This trend continued until the capacitance reached the minimum value. The capacitance didn't change once the depletion region in the substrate was completely formed. The capacitance increased slightly when the bias was swept in the reverse direction as shown in lower-right inset of Fig. 4.7. The capacitance became constant again after reaching the maximum value.

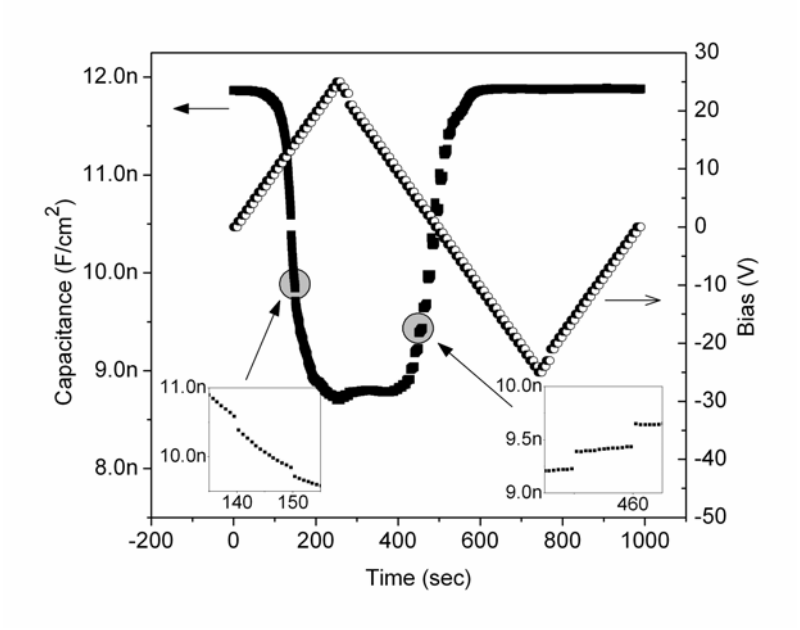

Fig. 4.7 Capacitance and bias versus time measured from type B.

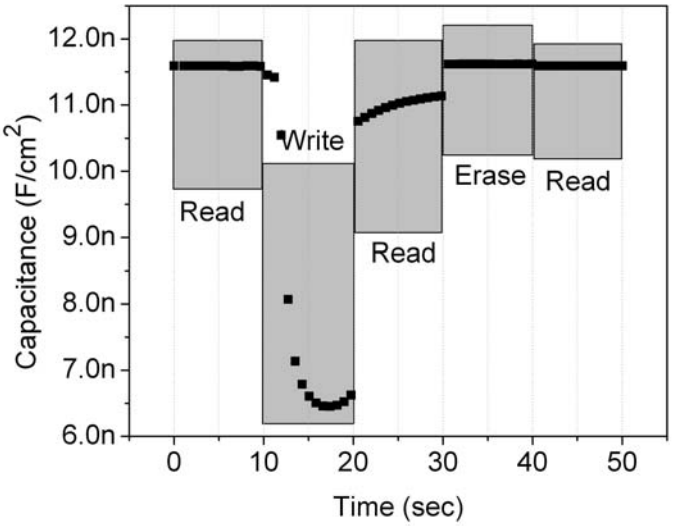

Fig. 4.8 Capacitance measurement with memory-like bias.

In order to examine the possibility of using PVP dielectric in a memory device, memory-like bias was applied to the capacitor device type B. The capacitance was recorded with time and the result is shown in Fig. 4.8. The first bias state was the reading at which both electrodes had the same voltage in order to prevent any charging. A 23-volt DC voltage with 5 mV AC signal was applied to silicon substrate to discharge the dielectric and the effective dielectric constant decreased with time. The altered status was measured by applying 0 V and was maintained over a few tens of seconds. In order to remove charged electrets, a negative 23-volt DC voltage was applied. After discharging, the capacitor returned to the original status.

4.4 Conclusion

We investigated the effect of surface polarization on pentacene thin-film transistors with PVP dielectric. The degree of the surface polarization as a function of time can be controlled by changing the degree of cross-linking of PVP molecules. The effect of surface polarization is superimposed on the drain current along with the bias stress. As a result, the drain current either increases with time or decreases slower than it does in the case with no surface polarization. This could lead to inaccurate estimation of device performance if the device characterization is conducted in an ambient with considerable humidity. Our data shows that this error can be as much as a factor of 30. Polarization effects should also be taken into account when devices are designed for sensing applications since water molecules in the air polarize the dielectric surface and can screen out the response from analytes that are of concern.

Capacitors with PVP dielectric were studied to confirm the effect of moisture on the dielectric. Large amount of hysteresis was observed from the less cross-linked dielectric. Based on the time scale of the hysteresis response and the bias condition, the observed increase in the drain current from the OFETs with PVP dielectric was not attributed to what caused the hysteresis. It appears that the hysteresis can be attributed to impurities in the pores in the dielectric layer. The pores were abundant in the less cross-link one.

References

[1] Z. Bao, Adv. Mater., 12, 227 (2000)

[2] A. Facchetti, M. Mushrush, M. H. Yoon, G. R. Hutchison, M. A. Ratner, and T. J. Marks, J. A.C.S., 126, 13859 (2004)

[3] R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. S. Filho, J. L. Brédas, L. L. Miller, K. R. Mann, and C. D. Frisbie, J. Phys. Chem. B, 108, 19281 (2004)

[4] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger, and Z. Bao, Appl. Phys. Lett., 78, 2229 (2001)

[5] L. Wang, D. Fine, and A. Dodabalapur, Appl. Phys. Lett., 85, 6386 (2004)

[6] C.W. Tang and S. A. VanSlyke, Appl. Phys. Lett., 51, 913 (1987)

[7] A. Dodabalapur, Z. Bao, A. Makhija, J. G. Laquindanum, V. R. Raju, Y. Feng, H. E. Katz, and J. Rogers, Appl. Phys. Lett., 73, 142 (1998)

[8] H. Sirringhaus, N. Tessler, and R. H. Friend, Science, 280, 1741 (1998)

[9] C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, Appl. Phys. Lett., 80, 1088 (2002)

[10] G. H. Gelinck, H. E. A. Huitema, E. V. Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. Putten, T. C. Geuns, M. Beenhakkers, J. B. Giesbers, B. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. Rens, and D. M. Leeuw, Nature Mater., 3, 106 (2004)

[11] H. Klauk, M. Halik, U. Zschieschang, F. Eder, G. Schmid, and C. Dehm, Appl. Phys. Lett., 82, 4175 (2003)

[12] P. Peumans, V. Bulovic, and S. R. Forrest, Appl. Phys. Lett., 76, 3855 (2000)

[13] U. Zschieschang, H. Klauk, M. Halik, G. Schmid, and C. Dehm, Adv. Mater., 15, 1147 (2003)

[14] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, Adv. Mater., 14, 1717 (2002)

[15] H. Klauk, M., U. Zschieschang, F. Eder, G. Schmid, and C. Dehm, Appl. Pyhs. Lett. 82, 4175 (2003)

[16] R. A. Street, A. Salleo, and M. L. Chabinyc, Phys. review B, 68, 085316 (2003)

[17] H. Y. Choi, S. H. Kim, and J. Jang, Adv. Mater., 16, 732 (2004)

[18] D. Li, E. J. Borkent, R. Nortrup, H. Moon, H. Katz, and Z. Bao, Appl. Phys. Lett., 86, 042105 (2005)

[19] S. M. Sze, Physics of Semiconductor Devices (Wiley, New York, 1982)

[20] C. Huang, J. E. West, and H. E. Katz, Mater. Res. Soc. Symp. Proc., 889, 0889, W08-07.1 (2006)

CHAPTER 5 NANOSACALE N-CHANNEL AND AMBIPOLAR ORGANIC FIELD-EFFECT TRANSISTORS

5.1 Introduction

Complementary circuits have emerged as a promising circuit technology for organic semiconductors due to low power consumption and high noise margins. There are three strategies to realize complementary circuits: i) using different semiconductor materials to fabricate separate n-channel and p-channel transistors; ii) employing ambipolar materials; iii) using materials combinations to mimic ambipolar behavior. While a large number of p-channel organic semiconductors are known, n-channel materials with suitable properties are more rare and their properties far less investigated. In recent years there have been promising reports on n-channel organic transistors with air-stable materials [1-3]. There have been reports of ambipolar devices including single component materials [4], blends [5] and heterostructures [6, 7]. However, scaling down circuit feature size to enhance performance is difficult in the first approach, where transistors with different semiconductors must be located spatially apart, requiring additional patterning.

In inorganic semiconductor state terminology, the term “ambipolar” is used to describe a semiconductor that has no distinctive conductivity type (n- or p-type) or has approximately the same amount of excess electrons and holes under certain conditions.

The latter is known as the quasi-neutrality condition and charge transport is described by the ambipolar transport equation in which ambipolar diffusion constants and ambipolar mobilities are used. However, in organics, the term is often used to describe a semiconductor which has the ability to transport both type of charge carriers, electrons and holes. When an OFET is fabricated with an ambipolar organic semiconductor, an electron or a hole current is observed depending on bias condition. Under some conditions both currents are observed in a field-effect transistor. In reality all organic semiconductors are fundamentally ambipolar and thus they make ambipolar OFETs in principle. However, organic semiconductors in contact with certain insulators possess interface traps that permit only one type of charge carrier to move. Therefore, in order to realize ambipolar behavior with these semiconductors, two different materials are blended together or stacked in layers. The mechanism of transport in bilayered structure will be explained in the following section. In some cases, by careful choice of insulator, ambipolar behavior is observed in a single semiconductor.

While much of the research effort to improve OFET performance involves new materials and device structures, decreasing the channel length is expected to greatly enhance device performance by increasing the switching frequency, which is inversely proportional to the square of the channel length [8]. There have been concurrent developments in low-cost techniques to pattern devices with channel lengths below a micron, making the investigation of the electrical properties of n-channel and ambipolar transistors with such channel lengths necessary and important. Most n-channel organic transistors employ the top-contact configuration, in which the contacts are made after the

semiconductor is deposited [9, 10]. With the top-contact approach, patterning channel lengths less than 25 μm becomes problematic due to limitations in the available lithographic techniques. Recent work by Yoo *et al.*, demonstrated that the robust, n-channel organic semiconductor, N,N'-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2), exhibits unprecedented n-type electrical performance in the bottom-contact configuration with transistor channel lengths ranging from 4-8 μm [11].

When the field-effect mobility is extracted using the conventional analytical model, the effects of the geometry of an OFET, whose channel length is of the order of tens of nanometers, should be carefully taken into account. This is because the roughness of the electrode edge is not negligible and the variation of the channel edge is of the order of the channel length. In addition, the semiconductor region outside of the channel area, defined by source and drain electrodes, can flow significant amount of spreading current and thus this region becomes a part of the channel. As a result the effective channel width becomes larger than the designed and fabricated width. Therefore, the device geometry should be designed carefully to give reasonable approximation on the channel length and width in this scale. Otherwise extracted parameters such as the field-effect mobility will not be reasonably estimated. In order to minimize the variation in the channel length, the channel width was kept small, of the order of the channel length. Furthermore additional electrodes, next to the channel area, were inserted to collect the spreading current and to confine the active area between the

source and drain electrodes. It is also noted that even in Si FETs, extraction of mobility in very small geometry devices becomes problematic.

5.2 fabrication of n-type and ambipolar field-effect transistors

The present transistors are based on the air-stable electron transporting molecular semiconductor PDI-8CN_2 and hole transporting pentacene [Fig 5.1(a)]. The experimentally determined energies of the highest occupied and lowest unoccupied molecular orbitals (HOMOs and LUMOs) for both pentacene and PDI-8CN_2 are shown in Fig. 5.1(b). The device structures (Figs. 5.1(c) and 5.1(d)) employ 100 *nm* of a thermally grown SiO_2 dielectric on top of a conducting p-type Si gate/substrate. The source and drain electrodes were patterned by e-beam lithography on a JEOL JBX-5DII instrument and metals (2.5 *nm* Ti/ 35 *nm* Au) were deposited by e-beam evaporation for both nano- and micro-scale devices. Electrically guarding electrodes, which are biased at the same voltage as the drain during operation, are placed near the drain electrode to collect fringe and leakage currents. The behavior and advantages of these guarding electrodes has been described previously [12]. After lift-off, the patterned samples are cleaned with an oxygen plasma, then coated with hexamethyldisilazane (HMDS) from the vapor phase to improve substrate wettability by the semiconductor. The HMDS layer lowers the surface free energy of the SiO_2 [13]. In order to examine the effect of the gold electrode/semiconductor interface, some devices were immersed in a 10 mM solution of nitrobenzenethiol (NBT) in acetonitrile or a 10 mM solution of octadecanthiol

(ODT) in ethanol with/without HMDS treatment for ~1 h prior to semiconductor deposition. PDI-8CN_2 was synthesized and purified as described previously [3, 14] and pentacene was purchased from Sigma-Aldrich and purified by sublimation. A 30-40 *nm* thick PDI-8CN_2 film is first deposited at a substrate temperature of 100-110 °C, with a base pressure ~4×10^{-7} Torr and at a growth rate of 0.2-0.5 Å/s. For ambipolar operation, a 40 *nm* thick pentacene layer is then sublimed onto the PDI-8CN_2 at a substrate temperature of 60 °C at a rate of 0.5 Å/s with a base pressure ~4×10^{-7} Torr. Electrical characterization was conducted in a Desert Cryogenics vacuum probe station with a base pressure ~1 mTorr at 300 K with an Agilent 4155C semiconductor parameter analyzer. A field-emission SEM (FE-SEM, LEO 1530) was used to characterize the electrodes.

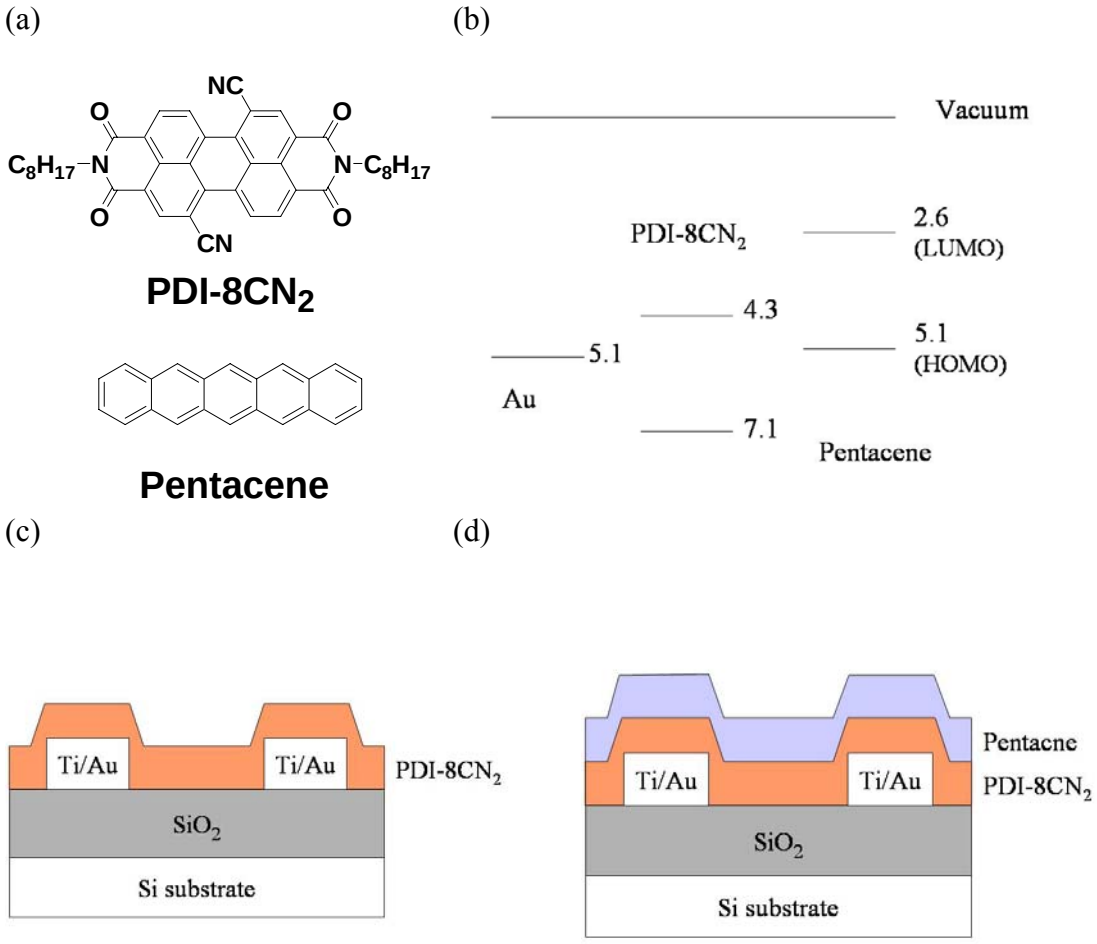

Fig. 5.1 (a) Molecular structure of the PDI-8CN_2 (1,7-isomer), (b) energy level (in eV) diagram of PDI-8CN_2, pentacene, and gold. Schematic diagrams of (c) an n-channel organic field-effect transistor (OFET) and (d) an ambipolar OFET. Reprinted with permission from Taeho Jung, Byungwook Yoo, Liang Wang, Ananth Dodabalapur, Brooks A. Jones, Antonio Facchetti, Michael R. Wasielewski, and Tobin J. Marks Appl. Phys. Lett., 88, 183102 (2006). Copyright 2006, American Institute of Physics.

5.3 Results and discussion

Linear regime electron mobilities of 2.3×10^{-3} cm^2/Vs and 9.2×10^{-3} cm^2/Vs with V_G ranges from 0 V to 40 V are extracted from PDI-$8CN_2$ devices having channel lengths ranging from 15 *nm* to 68 *nm* [Fig. 5.2(a)]. When the thickness of the gate dielectric (100 *nm*) is greater than the lengths of channels, the applied drain voltages are always lower than that of gate voltages, and the devices operate in the linear regime. Most devices exhibit field-dependent mobilities and short channel effects in which drain current does not saturate and the off current increases. The application of self-assembled monolayers to metal electrodes with thiol-based nitro and aliphatic groups has been shown to improve device performance by altering surface energies [12, 15]; however, enhancement in the performance of the present PDI-$8CN_2$ thin film transistors with submicron channel lengths is not noticeable after these treatments [Fig. 5.2(a)]. Furthermore, experiments using very thin self-assembled dielectrics developed by Marks and co-workers [16] in which improved electrical characteristics should be observed are promising for future work.

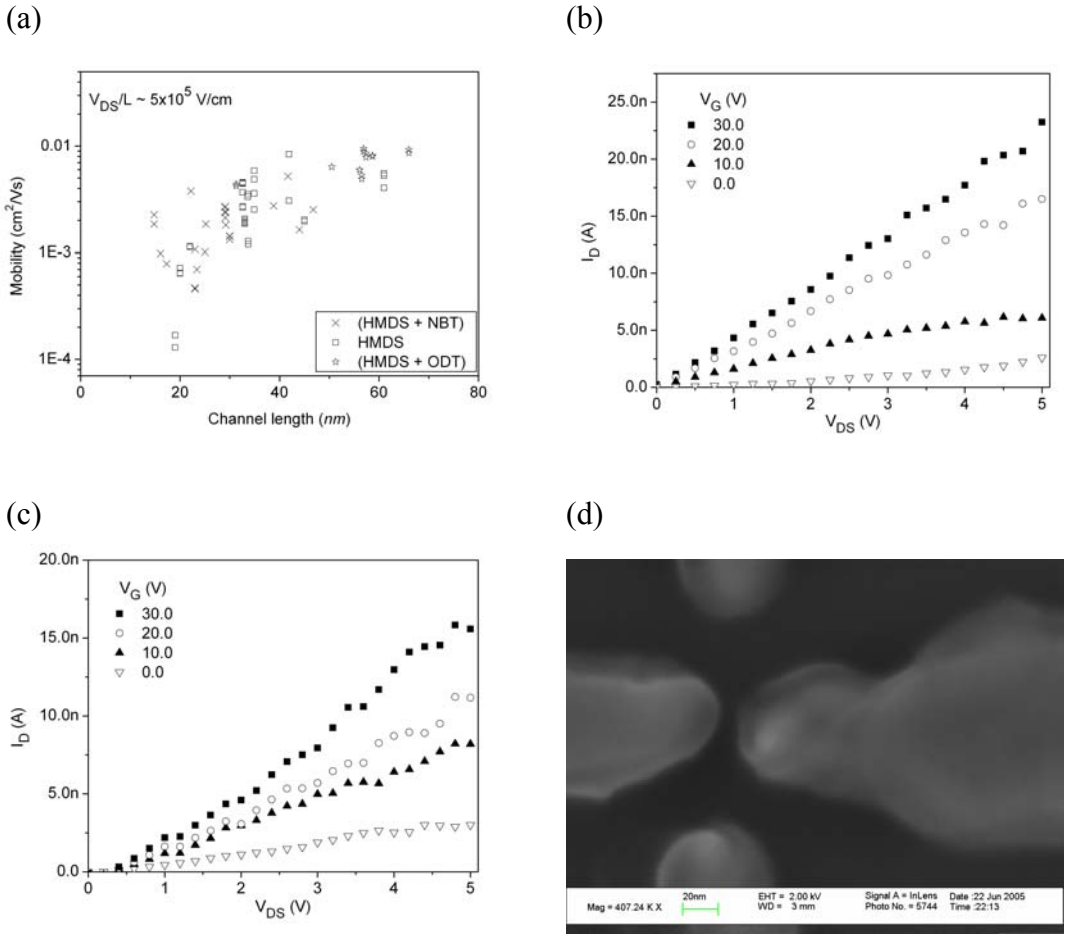

Fig. 5.2 (a) Field-effect mobilities in the linear regime from n-channel OFETs with channel lengths ranging from 15 *nm* to 68 *nm*. Samples are treated with hexamethyldisilazane (HMDS) for dielectric surface with/without nitrobenzenethiol (NBT) or octadecanthiol (ODT) for electrode surface. Applied lateral electric fields are about 5×10^5 V/cm in all devices. I_D vs. V_{DS} plots of an OFET with 15 *nm* channel characterized (b) in vacuum and (c) under the ambient condition. (d) SEM image of the OFET taken after electrical characterization. Reprinted with permission from Taeho Jung, Byungwook Yoo, Liang Wang, Ananth Dodabalapur, Brooks A. Jones, Antonio Facchetti, Michael R. Wasielewski, and Tobin J. Marks Appl. Phys. Lett., 88, 183102 (2006). Copyright 2006, American Institute of Physics.

As a general trend, the electron mobility in the present devices increases with channel length. Some devices exhibit injection-limited behavior consistent with Fowler-Nordheim tunneling [17]. The transfer characteristics of a device with 15 *nm* channel length are shown in Fig. 5.2(b). When V_{DS} is biased to 0.75 V, the calculated field-effect mobility in the linear regime is ~2.3×10^{-3} cm^2/Vs by conventional I_{DS} vs. V_G transistor relationships [17]. The I_{on}/I_{off} ratio (V_G=30 V/0 V) is 9. Importantly, since PDI-8CN2 is one of the very few air-stable n-channel semiconductors, these devices exhibit stable performance when characterized under ambient conditions [Fig. 5.2(c)]. Figure 2(d) shows a SEM image of the device with the semiconductor, taken after electrical characterization. The left and right electrodes are the drain and source, respectively. The other two electrodes are used as guarding electrodes, which are necessary for the proper characterization of nanoscale transistors with unpatterned gates.

Ambipolar PDI-$8CN_2$/pentacene bilayer transistors were next fabricated by first depositing PDI-$8CN_2$ onto the gate dielectric, since the electron mobility of PDI-$8CN_2$ thin films on SiO_2 is generally lower than pentacene thin film hole mobility on SiO_2 (see Refs.3 and 12). Although electrodes located between the two semiconductor layers are ideal for heterostructure FETs [6], a bottom contact structure is necessary for the realization of submicron and nanoscale devices. To investigate ambipolar transport in these devices, PDI-$8CN_2$ layer thickness was varied within the range 30-45 *nm* [15]. In the case of hole transport, carriers are injected from the source/drain electrodes into pentacene through the PDI-$8CN_2$ layer which acts as a charge injection barrier.

Therefore, the thickness of the PDI-8CN_2 thin film must be carefully controlled. Note that even though the field-induced 2D charge channel is independent of the PDI-8CN_2 film thickness [18] experimentally efficient n-channel operation requires films of ~ 30 *nm* thick or greater.

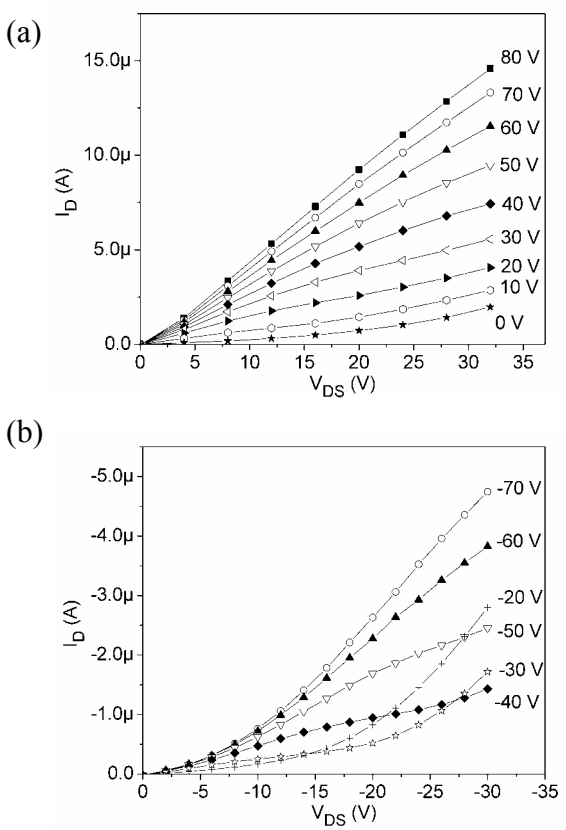

Fig. 5.3 ID vs. VDS plots for an ambipolar OFET with 16 μm channel length. The sample is treated with HMDS before the semiconductor deposition. (a) n-channel mode of operation. (b) p-channel mode of operation. Reprinted with permission from Taeho Jung, Byungwook Yoo, Liang Wang, Ananth Dodabalapur, Brooks A. Jones, Antonio Facchetti, Michael R. Wasielewski, and Tobin J. Marks Appl. Phys. Lett., 88, 183102 (2006). Copyright 2006, American Institute of Physics.

The ambipolar operation of a heterostructure transistor with 16 μm channel length is shown in Fig. 5.3. When the gate substrate is biased positively with respect to the source electrode, the devices operate as n-channel FETs and the transfer characteristics are shown in Fig. 5.3(a). A saturation regime electron mobility of 6.3×10^{-3} cm^2/Vs is extracted when V_{DS} = 32 V, and V_G ranges from 0 V to 80 V. The on-off current ratio = 7.4 between V_G = 80 V and 0 V. The electron mobility is lowered by more than a factor of 10 compared to single component transistors [11]. A possible reason for this is because the grain boundaries in PDI-$8CN_2$ layer is filled with pentacene molecules deposited on top disturbing energy states for electron charge to move through. For p-channel operation, the gate electrode is biased negatively with respect to the source electrode [Fig. 5.3(b)]. Unlike n-channel mode operation, the drain current decreases with gate voltage until reaching a minimum value, followed by increasing drain current with gate voltage. The initial high current is due to the electron injection from the drain electrode at a low gate voltage and high drain voltage biasing condition. The magnitude of the electron current is reduced with increasing gate voltage, which in turn suppresses electron injection and causes holes to accumulate in the pentacene thin film. This behavior has been previously observed in ambipolar OFETs [6, 7, 19, 20]. In the present case, crossover between electron current and hole current injection occurs at gate voltage values between -30 V and -40 V. The hole mobility in a saturation regime is 6.4×10^{-3} cm^2/Vs with V_{DS} = -30 V and V_G ranging from -40 V and -70 V. The on-off current ratio = 3.4 between V_G = -80 V and -40 V. The measured hole mobilities are lower than those in pentacene-only devices. This decrease is ascribed to the injection barrier and the rough

surface topography of the PDI-8CN_2 layer between the electrodes and pentacene, which is expected to affect the organization of the pentacene film.

The SEM micrograph and current-voltage characteristics of one of the heterostructure ambipolar devices with a channel length of 22 *nm* are shown in Fig. 5.4. A linear regime electron mobility of 4.0×10^{-3} cm^2/Vs is extracted when V_{DS} = 1 V (lateral electric field ~ 5×10^{-3} V/cm), and V_G ranges from 0 V to 50 V. The on-off current ratio = 3.4 between V_G = 50 V and 0 V. For p-channel operation, the electron injection is also observed with the low gate voltage. The hole mobility is 9.2×10^{-3} cm^2/Vs in the linear regime with V_{DS} = -1 V and V_G ranging from -50 V and -20 V. All the currents show injection-limited behavior because of the PDI-8CN_2 thin film. However, the decrease in the hole mobility is not severe compared to nanoscale pentacene transistors [12], possibly because of the high lateral electric field.

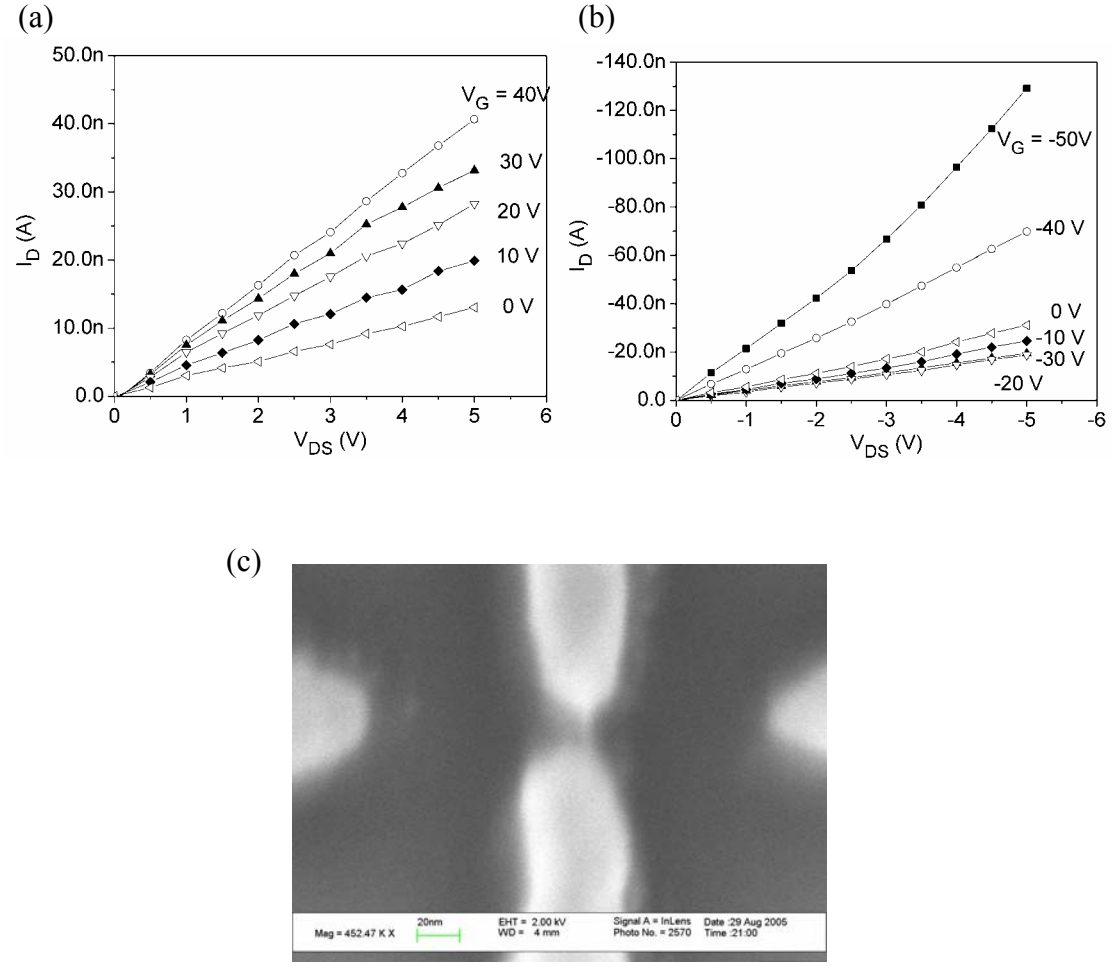

Fig. 5.4 I_D vs. V_{DS} plots for an ambipolar OFET with 23 *nm* channel length. (a) n-channel mode of operation. (b) p-channel mode of operation; (c) FE-SEM image taken after the semiconducting materials were removed. Reprinted with permission from Taeho Jung, Byungwook Yoo, Liang Wang, Ananth Dodabalapur, Brooks A. Jones, Antonio Facchetti, Michael R. Wasielewski, and Tobin J. Marks Appl. Phys. Lett., 88, 183102 (2006). Copyright 2006, American Institute of Physics.

5.4 Conclusion

The response characteristics of the first nanoscale n-channel organic transistors based on PDI-8CN_2 with channel lengths scaled down to 15 *nm* are described. We also fabricated ambipolar OFETs utilizing a heterostructure of pentacene and PDI-8CN_2. Both devices exhibit stable behavior when operated under the ambient conditions. Despite the additional injection barrier and disordered interface, the hole mobility through the pentacene thin film deposited on top of the n-type material does not undergo severe degradation due to the strong lateral electrical field. These transistors represent by far the smallest featured organic n-channel and ambipolar transistors that have been fabricated to date.

References

[1] C. R. Newman, C. D. Frisbie, D. A. da Silva, J. L. Bredas, P. C. Ewbank, and K. R. Mann, Chem. Mater., 16, 4436 (2004)

[2] H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y.-Y. Lin, and A. Dodabalapur, Nature, 404, 478 (2000)

[3] B. A. Jones, M. J. Ahrens, M.-H. Yoon, A. Facchetti, T.J. Marks, and M. R. Wasielewski, Angew. Chem. Int. Ed., 43, 6363 (2004)

[4] E. J. Meijer, D. M. de Leeuw, S. Setayesh, E. van Veenendaal, B.-H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, and T. M. Klapwijk, Nature Mater., 2, 678 (2003)

[5] Y. Hayashi, H. Kanamori, I. Yamada, A. Takasu, S. Takagi, and K. Kaneko, Appl. Phys. Lett., 86, 052104 (2005)

[6] E. Kuwahara, Y. Kubozono, T. Hosokawa, T. Nagano, K. Masunari, and A. Fujiwara, Appl. Phys. Lett., 85, 4765 (2004)

[7] A. Dodabalapur, H. E. Katz, L. Torsi, and R. C. Haddon, Appl. Phys. Lett., 68, 1108 (1996)

[8] M. Leufgen, U. Bass, T. Muck, T. Borzenko, G. Schmidt, J. Geurts, V. Wagner, and L.W. Molenkamp, Synth. Met., 146, 341 (2004)

[9] R.J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. da Silva Filho, J.-L. Bredas, L. L. Miller, K. R. Mann, and C. D. Frisbie, J. Phys. Chem. B, 108, 19281 (2004)

[10] Y. Takahashi, T. Hasegawa, Y. Abe, Y. Tokura, K. Nishimura, and G. Saito, Appl. Phys. Lett., 86, 063504 (2005)

[11] B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks, Appl. Phys. Lett., 88, 082104 (2006)

[12] L. Wang, D. Fine, T. Jung, D. Basu, H. V. Seggern, and A. Dodabalapur, Appl. Phys. Lett., 85, 1772 (2004)

[13] H. Y. Choi, S. H. Kim, and J. Jang, Adv. Mater., 16, 732 (2004)

[14] M.J. Ahrens, M. J. Fuller, and M. R. Wasielewski. Chem. Mater., 15, 2684 (2003)

[15] I. Kymissis, C. D. Dimitrakopoulos, and S. Prurushothaman, IEEE Trans. on Elect. Dev., 48, 1060 (2001)

[16] M.-H. Yoon, A. Facchetti, and T. J. Marks PNAS, 102, 4678 (2005)

[17] S. M. Sze, Physics of Semiconductor Devices (Wiley, New York, 1982)

[18] A. Dodabalapur, L. Torsi, and H. E. Katz, Science, 268, 270 (1995)

[19] A. Dodabalapur, H.E. Katz, L. Torsi, and R. C. Haddon, Science, 269, 1560 (1995)

[20] J. Wang, H. Wang, X. Yan, H. Huang, and D. Yan, Appl. Phys. Lett., 87, 093507 (2005)

CHAPTER 6 ORGANIC SUBMICRON CIRCUITS

6.1 Introduction

6.1.1 SUBMICRON ORGANIC CIRCUITS

Until recently it was thought that circuits implemented with OFETs can not operate fast enough for radio-frequency applications because of their slow field-effect mobilities (less than 10 cm^2/Vs). This view was a result of quasi-static analysis in which the channel is fully developed by the applied electric field and the macroscopic field-effect mobility is characterized by the stabilized, steady-state current. In reality, a significant amount of fast charge carriers crosses the channel before the channel is fully formed [1, 2]. These charges are indeed able to act as an input signal to the next stage before the conventionally characterized charges in a fully formed channel can contribute. In this type of operation mode a circuit is in a non-quasi-static (NQS) regime which has allowed for the fabrication and demonstration of a full wave rectifier operating at 13.56 MHz [2]. The schematic diagram of a full wave rectifier is shown in Fig. 6.1(a) [2] and the ideal outputs of half and full wave rectifiers are shown in Fig. 6.1(b).

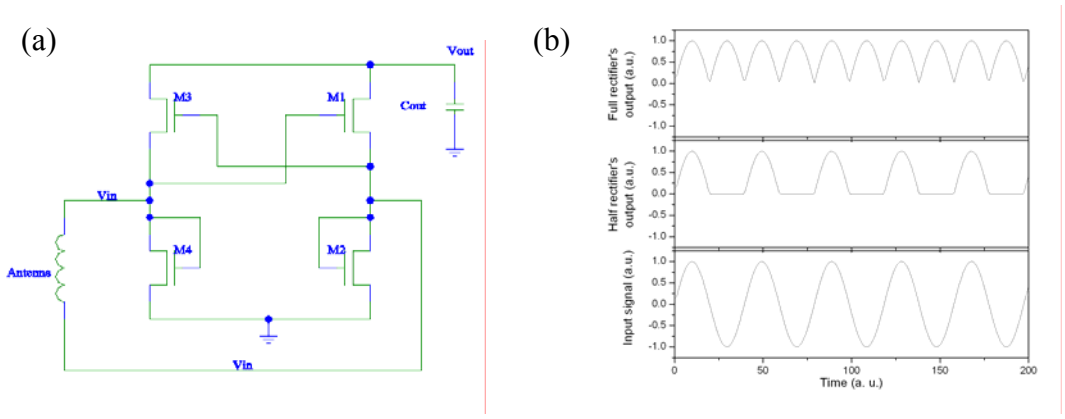

Fig. 6.1 (a) Circuit schematic of a full wave rectifier and (b) the responses from a half wave rectifier and a full wave rectifier.

It was predicted in the previous chapter that the maximum switching speed of a discrete transistor increases with decreasing channel length. Although it has been proven to be valid in the case of an inorganic device, it is not applicable to an OFET until some requirements are satisfied. The major issue is that an OFET should not have a significant decrease in the field-effective mobility with decreasing channel length, which happens in submicron OFETs as shown in the previous chapter. The other issue is short channel effects, which can be mitigated with thin gate dielectrics. Fig. 6.2 shows the linear regime mobility of FETs with PDI-8CN_2 and MCS-2 (tetrabenzoporphyrin derivative from Mitsubishi chemical corp.) versus channel length from 16 *μm* down to around 30 *nm*. All the semiconductors formed polycrystalline thin films. Overall the linear regime mobility decreased with decreasing channel length and was due to the injection or contact limited operation at short channel length. Fig. 6.3 shows the

transfer characteristics of pentacene FETs with various channel lengths. A 1000 Å SiO_2 layer on top of a n-type silicon substrate was used as the gate dielectric. The source/drain electrodes were patterned with a JEOL 6000 e-beam lithography tool and titanium/gold was used for metallization as described in the previous chapter.

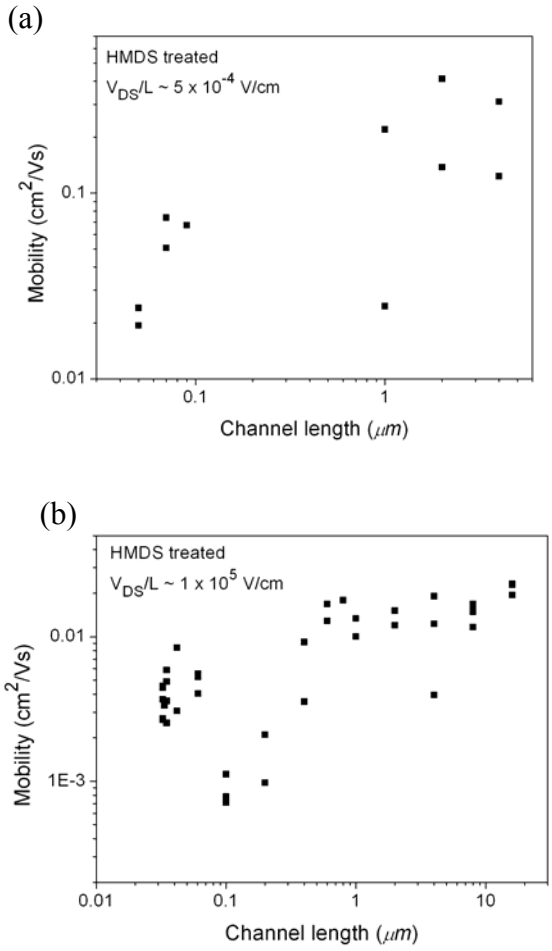

Fig 6.2 Saturation regime mobility versus channel length of FETs with (a) MCS-2 (Mitsubishi chemical corp.) and (b) PDI-8CN_2. All devices were treated with HMDS after oxygen plasma cleaning.

As the channel length decreased toward 1 *μm*, the plateau in the drain current in the saturation regime gradually disappeared and a super-linear increase in the drain current in the linear regime became noticeable. The super-linear increase became dominant even in saturation when the channel length was shorter than 800 *nm*. The off-

current also increased and, as a result, the on/off ratio decreased. In order for the gate to control the channel of a device with such a short channel length, the thickness of the gate dielectric layer should be reduced. A 100 *nm* channel length pentacene FET with a dry oxidized thin oxide layer (t_{ox} ~ 200 Å) was fabricated and the transfer characteristics shown in Fig. 6.4. The field-effect mobility was increased about one order of magnitude compared to the OFET with a 1000 Å SiO_2 gate dielectric layer. The off current was suppressed and the on/off characteristic was improved. However, the field-effect mobility and on/off characteristic of the submicron OFET were still lower than that of the devices with micron channel lengths.

Although short channel effects and mobility degradation are disadvantages for submicron and nano-scale OFETs, there have been concurrent developments in low-cost techniques to pattern devices with channel lengths below a micron and ring oscillator performance showing increasing operating speeds with decreasing channel length in the micro-scale [3]. Because of these factors, submicron full wave rectifiers were fabricated and their electrical properties were studied.

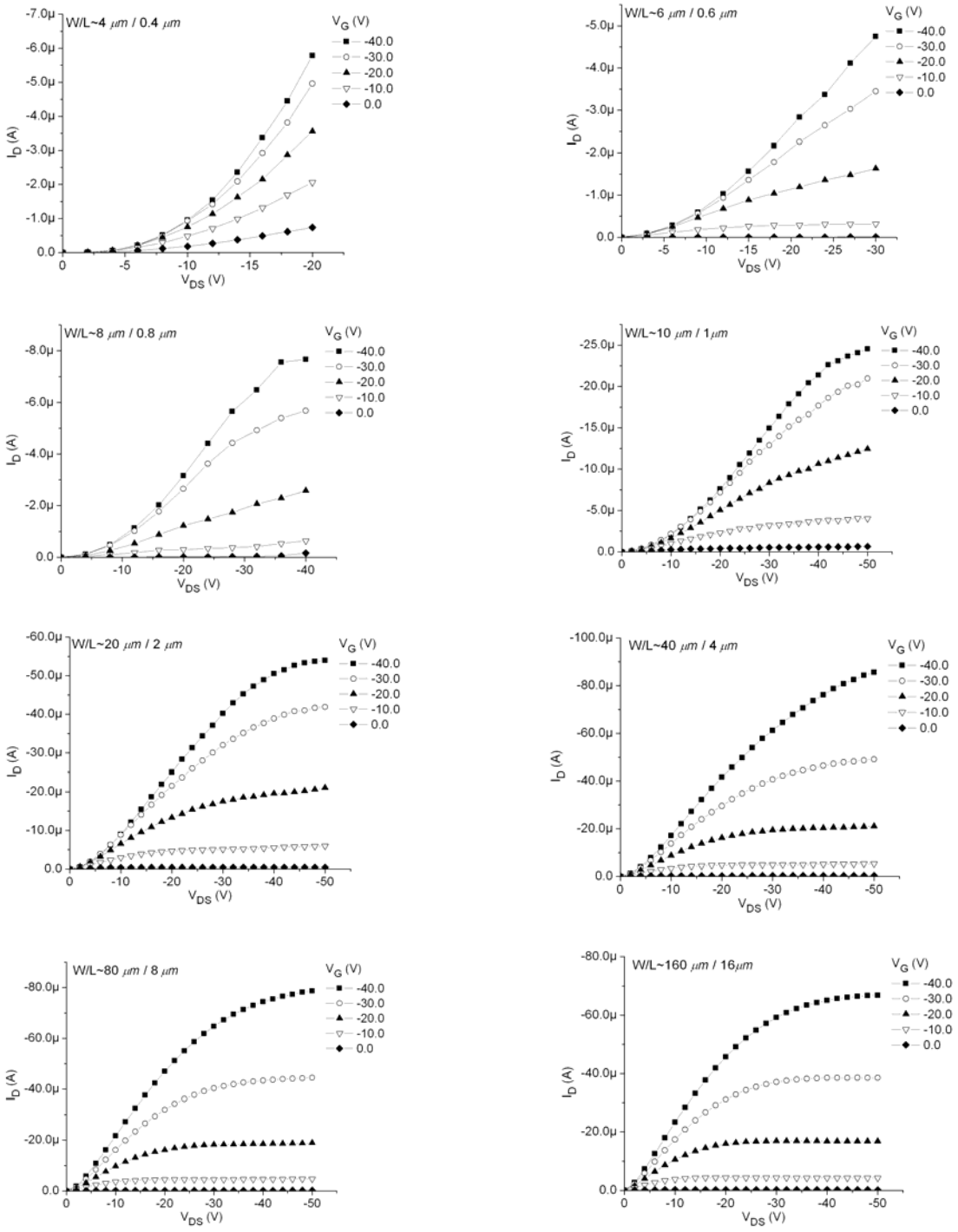

Fig. 6.3 Transfer characteristics for pentacene FETs with 1000 Å SiO_2 gate dielectric layer. The channel length are changing from 0.4 *μm* to 8 *μm*.

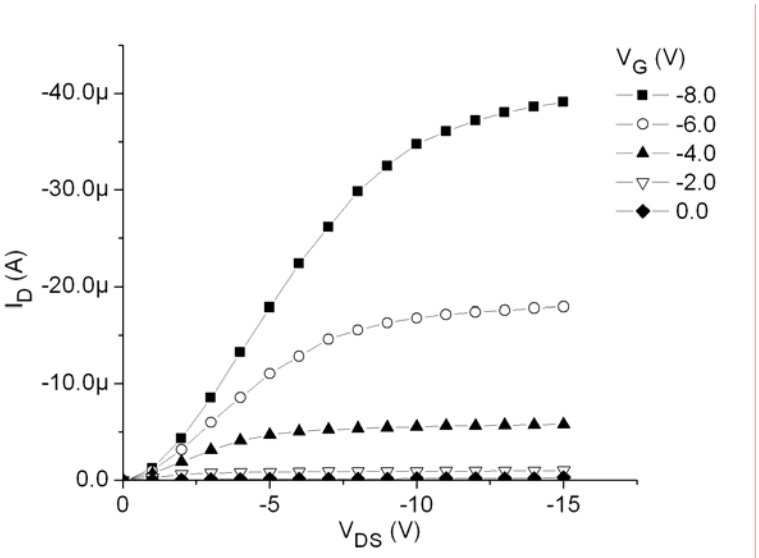

Fig. 6.4 The transfer characteristics of a pentacene FET. t_{ox} ~ 200 Å, L ~ 100 *nm*, W/L ~ 200, V_T ~ 1.1 V, on/off ~ 1.3×10^2, saturation regime mobility ~ 0.04 cm^2/Vs

6.1.2 COMPLEMENTARY CIRCUITS WITH OFETS

Complementary circuits have emerged as a promising circuit technology for organic semiconductors due to low power consumption and high noise margins [4]. Since p-type materials have shown better performance than n-type materials, however, inverters implemented with only p-type materials have been demonstrated [3, 5-7]. Inverters with a single semiconductor component have a load resister which is a transistor whose gate and drain are connected as shown in Fig. 6.5(a). The operation of this type of an inverter was simulated by T-SPICE and the output of the inverter shown in Fig.

6.5(b). V_{OH} and V_{OL} are minimum and maximum output voltages for valid logic 1 and 0, respectively. Likewise, V_{IH} and V_{IL} are minimum and maximum input voltages for valid logic 0 and 1, respectively [4].

Ring oscillators implemented with the single component inverters have been demonstrated [3, 5, 8] and the schematic diagram is shown in Fig. 6.5(c). In some cases transistors had positive turn on voltages and thus a level shift was inserted between the inverters [5]. Even though circuits with a single component have been demonstrated with stable performance, the power consumption is still a problem with this type of circuit since the current continually flows through the saturated load resistor.

This necessitates the use of complementary circuits in which both electron and hole transporting transistors are implemented. An inverter consisting of both p- and n-type transistors is shown in Fig. 6.6 which consumes power only when the output is altered [4]. A complementary 5-stage ring oscillator consisting of pentacene and PDI-$8CN_2$ FETs, with micron channel lengths, was fabricated which operated at 34 kHz [9]. In this study, inverters consisting of submicron pentacene and PDI-$8CN_2$ FETs were fabricated due to the nearly ubiquitous use of inverters as one of the basic components in logic gates and ring oscillators. The channel length of OFETs was varied from 150 *nm* to 950 *nm*.

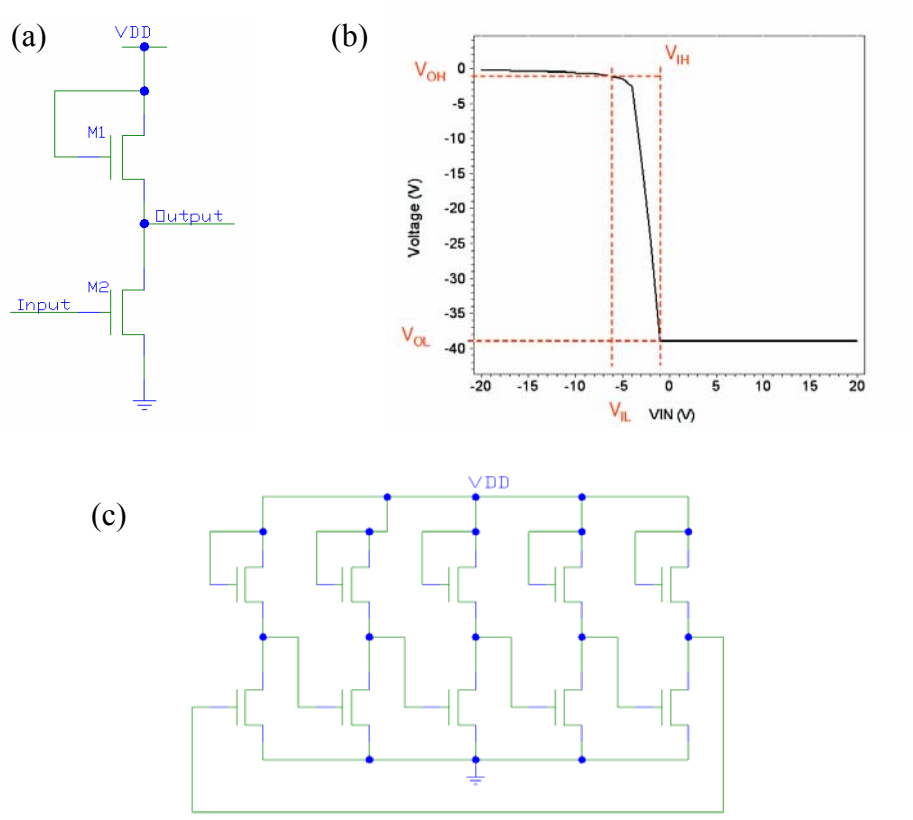

Fig. 6.5 (a) Circuit schematic of an inverter implemented with p-type FETs. (b) The electrical characteristics simulated by SPICE. (c) 5-stage ring oscillator.

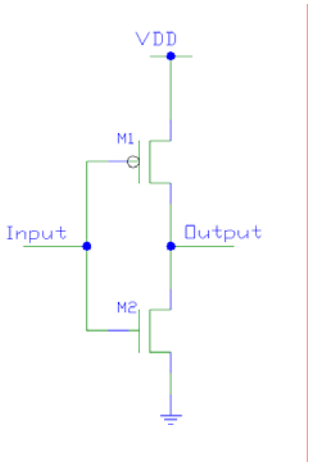

Fig. 6.6 An inverter with p- and n-type FETs.

6.2 The fabrication of organic submicron circuits

Ideally an insulating substrate is needed to isolate devices and minimize capacitive coupling between the devices and the surrounding environment. This substrate must also have an easily patternable conducting layer on top which can be used to create individually addressable gates for the OFETs. However, the choice of substrate should be compatible with conventional silicon processing, in this case growing silicon dioxide insulating layers. A candidate which satisfies these requirements is silicon-on-insulator (SOI) substrates. The thicker the buried insulator, the less critical the capacitive coupling between the OFETs and substrate becomes. Therefore P-type doped SOI substrates with 1904 Å of silicon on top of 3400 Å of buried oxide were used for full wave rectifiers and inverters. A second candidate, in addition to SOI substrates, is polysilicon grown on top of a thick silicon dioxide layer which can achieve the same device isolation and allow for control of the thickness of the buried insulator. The situation will be better with polymer based materials since polymers provide a broader range of choices. The schematic flow chart to make devices using SOI or polysilicon on insulator substrates is shown in Fig. 6.7. In the case of a polysilicon gate, amorphous silicon was first deposited by a low pressure chemical vapor deposition (LPCVD) method at 600 °C. The amorphous silicon film was then doped with phosphorous by POCL diffusion at 900 °C. The POCL diffusion was better than the ion-implantation to heavily dope the silicon films but the surface of the silicon became rough. The amorphous silicon film transformed into a polysilicon film during the diffusion process. Since the mobility of charges in polysilicon is larger than that in amorphous silicon,

polysilicon is desirable when used as a gate electrode and as interconnect wires. The oxide layer formed during the diffusion process was removed by HF. The polysilicon surface was smoothed by chemical mechanical polishing (CMP) for 10 to 20 seconds.

Gate electrodes and wires were defined by conventional lithography. The silicon was etched either by Cl/Br plasma or by polysilicon etchant. 3000 Å to 4000 Å of a SiO_2 layer was deposited by PECVD for isolating the channel from the gate and various individual devices from each other. The channel area and gate via were lithographically patterned and opened by buffered oxide etch (BOE). A thin SiO_2 film used for the gate dielectric layer was grown by dry oxidation at 900 °C. The thin dielectric blocking the gate via was removed again by BOE. Aluminum, used for the via plug, was immediately sputtered onto the samples to prevent the silicon surface from being covered with contaminants. Unnecessary aluminum was removed by a lift-off method in acetone. The samples were annealed in a nitrogen and hydrogen ambient at 450 °C for 30 minutes in order to remove any native oxide formed between the aluminum and the silicon gate or silicon wires. The source and drain electrodes were patterned by a JEOL electron beam lithography tool. 30 Å of titanium and 350 Å of gold were deposited by an e-beam evaporator in high vacuum (less than 1×10^{-5} Torr) followed by another lift-off process. The micron wires were defined by conventional lithography and the same metals were deposited and removed by lift-off. Prior to semiconductor deposition the samples were cleaned by oxygen plasma and treated with hexamethyldisilazane (HMDS) to improve the quality of the semiconductor film [10]. Pentacene layer was deposited first with a shadow mask since the pentacene devices outperformed the PDI-8CN_2

devices by at least one order of magnitude in terms of field-effect mobility. PDI-8CN_2 was deposited second with a shadow mask. After the electrical characterization, the semiconductors were removed and the physical dimensions of the devices were characterized by a Hitachi S-4500 field emission scanning electron microscope (SEM).

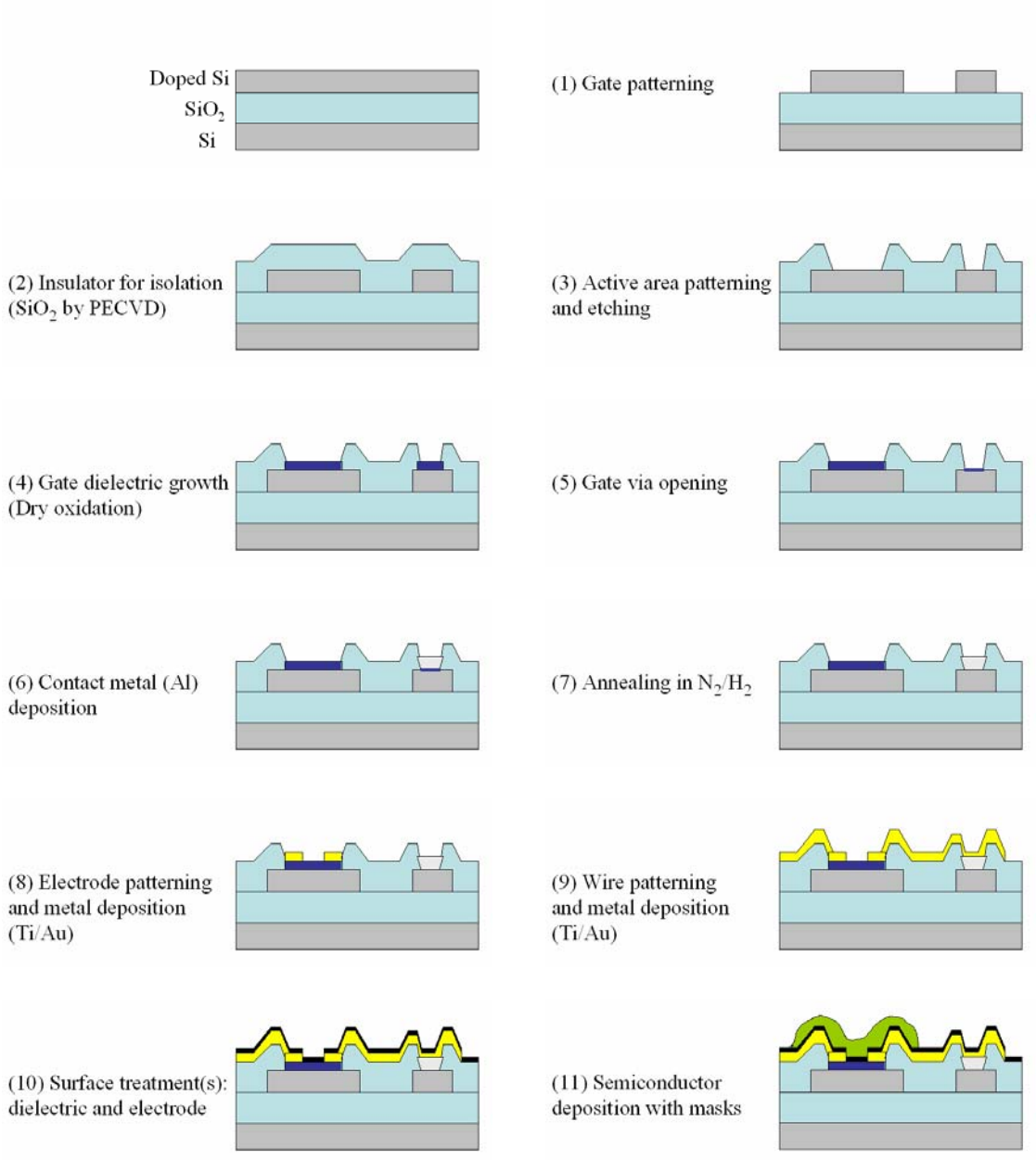

Fig. 6.7 The fabrication process for circuits on top of an insulator layer.

6.3 Experiments and discussion

6.3.1 THE DISCRETE ORGANIC TRANSISTORS

The transfer characteristics for a pentacene and PDI-8CN_2 FETs with 150 *nm* channel length are shown in Fig. 6.8(a) and Fig. 6.8(b). The characterization was conducted in vacuum (~1 mTorr) at 300 K in the dark with an Agilent 4155C semiconductor parameter analyzer. The characterized hole and electron mobilities were 3.9×10^{-2} cm^2/Vs and 3.2×10^{-4} cm^2/Vs, respectively.

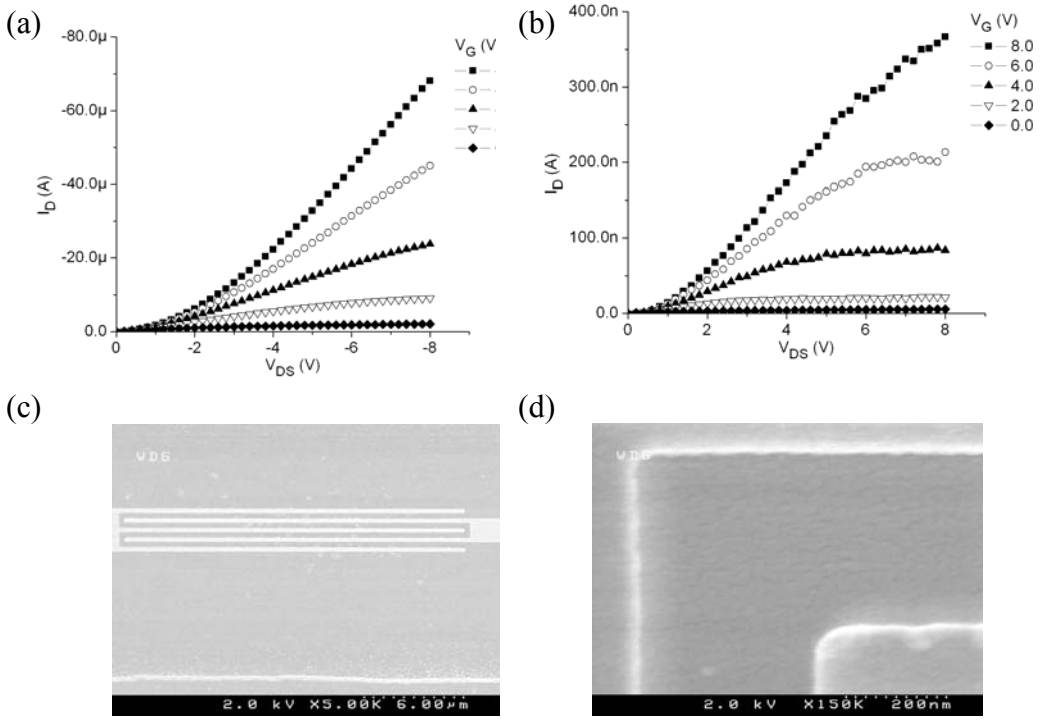

Fig. 6.8 I_D vs. V_{DS} plots of an OFET with 150 *nm* channel with (a) pentacene and (b) PDI-8CN_2. (c) SEM picture of the pentacene FET and (d) upper left corner of the channel region.

6.3.2 THE INVERTERS

The inverters were measured in a Desert Cryogenics vacuum probe station with a base pressure of ~1 mTorr at 300 K in the dark. An Agilent 4155C semiconductor parameter analyzer was used to apply input signals and record output voltages. Fig. 6.10 shows the voltage transfer characteristics of the inverters. W/L ratios for n- and p-type OFETs are around 220 and 220, respectively, for the inverters in the left column. They are 510 and 220 for the inverters in the right column since the performance of the pentacene FET was higher than the n-type FETs in the previous chapter. The V_{DD} was set to 8 V and the input was swept from 0 V to 8 V and back to 0 V to examine any hysteresis.

When the input signal was low, the pentacene FET was on and the PDI-8CN_2 FET was off so that the output port was connected to V_{DD} through the p-channel FET. Because the n-channel FET drew a certain amount of off-current, the outputs were less than V_{DD}. When the input signal was high, the pentacene and PDI-8CN_2 FETs were off and on respectively. This output was much higher than the ideal output of 0 V. The deviation from the ideal output was larger when the input was high. This was because the on-current of the PDI-8CN_2 FET was not much larger than the off-current of the pentacene FET and, as a result, around three quarters of V_{DD} dropped across the pentacene FET, which is more than that in a well functioning inverter. This explained

the reason that the transition region was shifted to the right side when the W/L ratio was 220 for both p- and n-type FETs.

After electrical characterization, the semiconductors were removed and SEM images were taken. The channel lengths varied from 150 *nm*, as shown in Fig. 6.9, down to 950 *nm*.

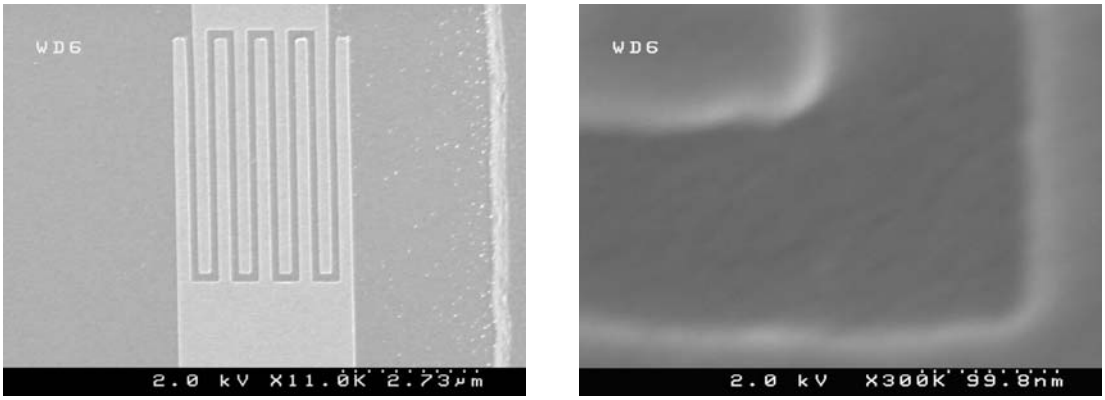

Fig. 6.9 (left) The SEM image of the transistor (L = 150 *nm*). (right) lower-right corner of the channel.

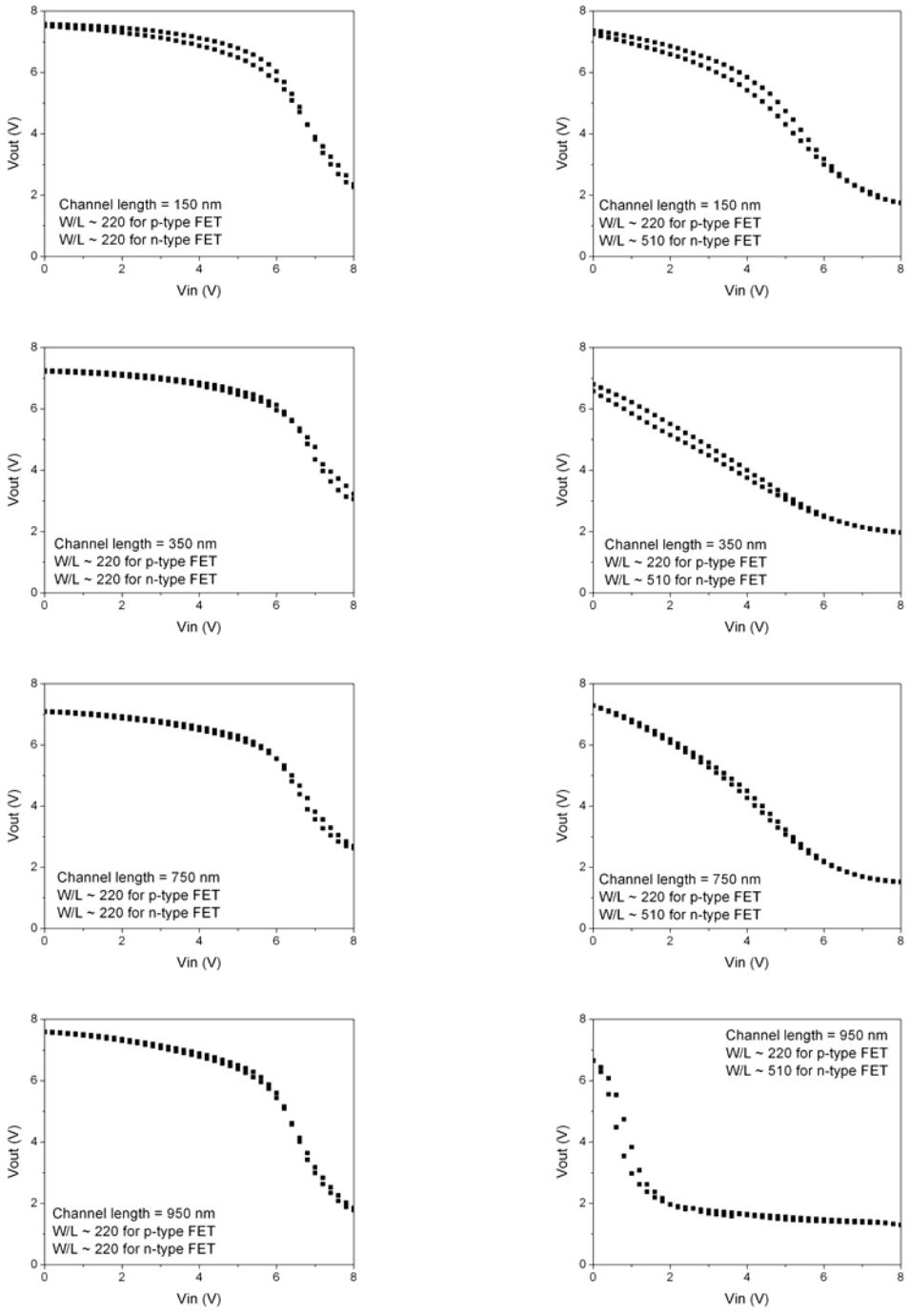

Fig. 6.10 Voltage transfer characteristics of inverters with channel lengths from 150 *nm* to 950 *nm*. The input was swept from 0 V to 8 V and back to 0 V.

When an OFET is turned on, the induced charge carriers start to fall into less mobile states and can screen out some of the charges induced in the gate [11]. These less mobile states can be considered as traps and they are located either in the semiconductor, in the dielectric, or at the dielectric-semiconductor interface. As a result the gate bias must be increased to compensate for the loss caused by the trapped charges. This phenomenon is characterized as a threshold shift and is called the bias stress effect. The trapped charges can be released from the trap states over time and thus the OFET returns to its original status. The bias stress effect becomes problematic when OFETs are operated in a circuit for prolonged periods of time if they are not refreshed regularly. The effect of the bias stress effect on an inverter implemented with a p-type semiconductor was studied [12] but not on complementary or submicron inverters. In order to induce the bias stress effect, the inverters were subject to continuous sweeps between 0 and 8 V. The initial sweeps are marked with the voided circles in Fig. 6.11. The voltage transfer characteristics changed with time and were recorded until they did not show noticeable change. The filled circles in Fig. 6.11 show the transfer characteristics under bias stress. The decreases in the output voltage for logic 0 were observed from all the inverters but were not significant except for the 150 *nm* channel length. In the case of an inverter with a p-type semiconductor, the voltage transfer characteristics became worse because of the bias stress effect on the load transistor which was always on [12]. When both p- and n-type semiconductors were used in an inverter, the bias stress effect didn't degrade the performance because both transistors were subjected to the bias stress effect.

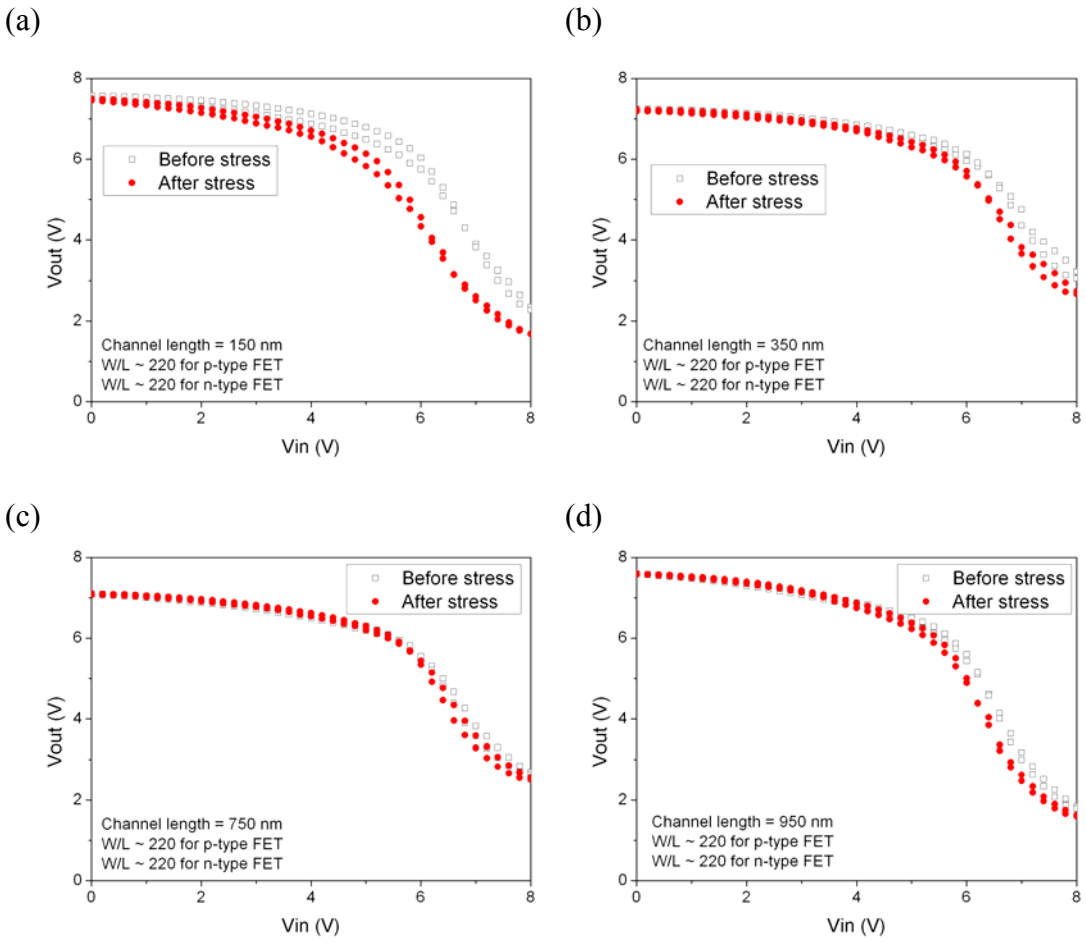

Fig. 6.11 The voltage transfer characteristics of several inverters. The voided circles indicate the output voltage during the first measurement. The input continued to be swept until the change in the output voltage became negligible. The filled circles indicate the transfer characteristics under the bias stress effect.

6.3.3 FULL WAVE RECTIFIERS

The schematic of the experimental setup is shown in Fig. 6.12. A Sony AWG2021 arbitrary waveform generator was used to generate 16 V peak-to-peak sinusoidal input signals. The full wave form rectifiers were placed in a Desert Cryogenics vacuum probe station with a base pressure of ~1 mTorr at 300 K in the dark. A Tektronics oscilloscope was connected to the output of the rectifiers with a 1 MΩ resister coupled to ground. A 10 μF capacitor was connected to the output of the rectifiers via a switch in order to observe the rippled output as well as the DC output.

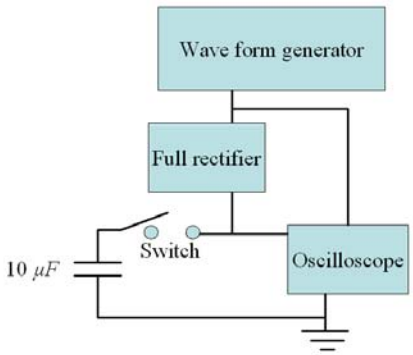

Fig. 6.12 The measurement setup for full wave rectifiers.

Fig. 6.13 shows the full wave rectifier designed with L-Edit. S1 and S2 transistors are switches and D1 and D2 are diodes [2]. The operation of a full wave rectifier consisting of pentacene FETs is as follows: during the operation, an AC signal is applied to Input1 and the opposite AC signal is applied to Input2. At a certain time Input1 and Input2 have positive and negative voltages, respectively, with respect to the

ground. The high voltage at input1 turns off D1 and S2. Whereas D2 and S1 are on and current flows from the output terminal to ground via S1 and D2. When a capacitor is connected to the output terminal, the output voltage decreases slowly and as a result, the current flows only when the output voltage is lower than Input1. Fig. 6.14 shows the output waveforms for the full wave rectifiers consisting of pentacene FETs with the channel lengths of 150 *nm*. Fig. 6.14(a) is the output of the rectifier when the input frequency was 1 kHz. Two positive peaks were observed for every input peak but the magnitudes were not the same. Because the input1 signal had to be fed to S2 via the silicon wire shown at the center of Fig. 6.13, that part of the input signal was lost at the metal-to-silicon wire contacts. Fig. 6.14(b) shows the output waveform with a 10 μF capacitor connected at the output. As the input frequency increased, the peak to valley difference became small due to the capacitance of the measurement setup. When the operating frequency was over 100 kHz, the output without the capacitor didn't differ from that with the capacitor.

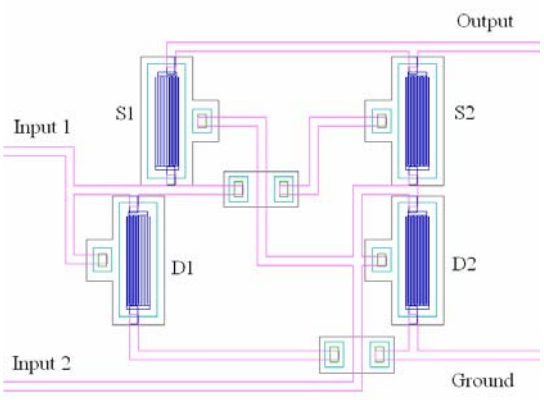

Fig. 6.13 The full wave rectifier layout designed with L-Edit.

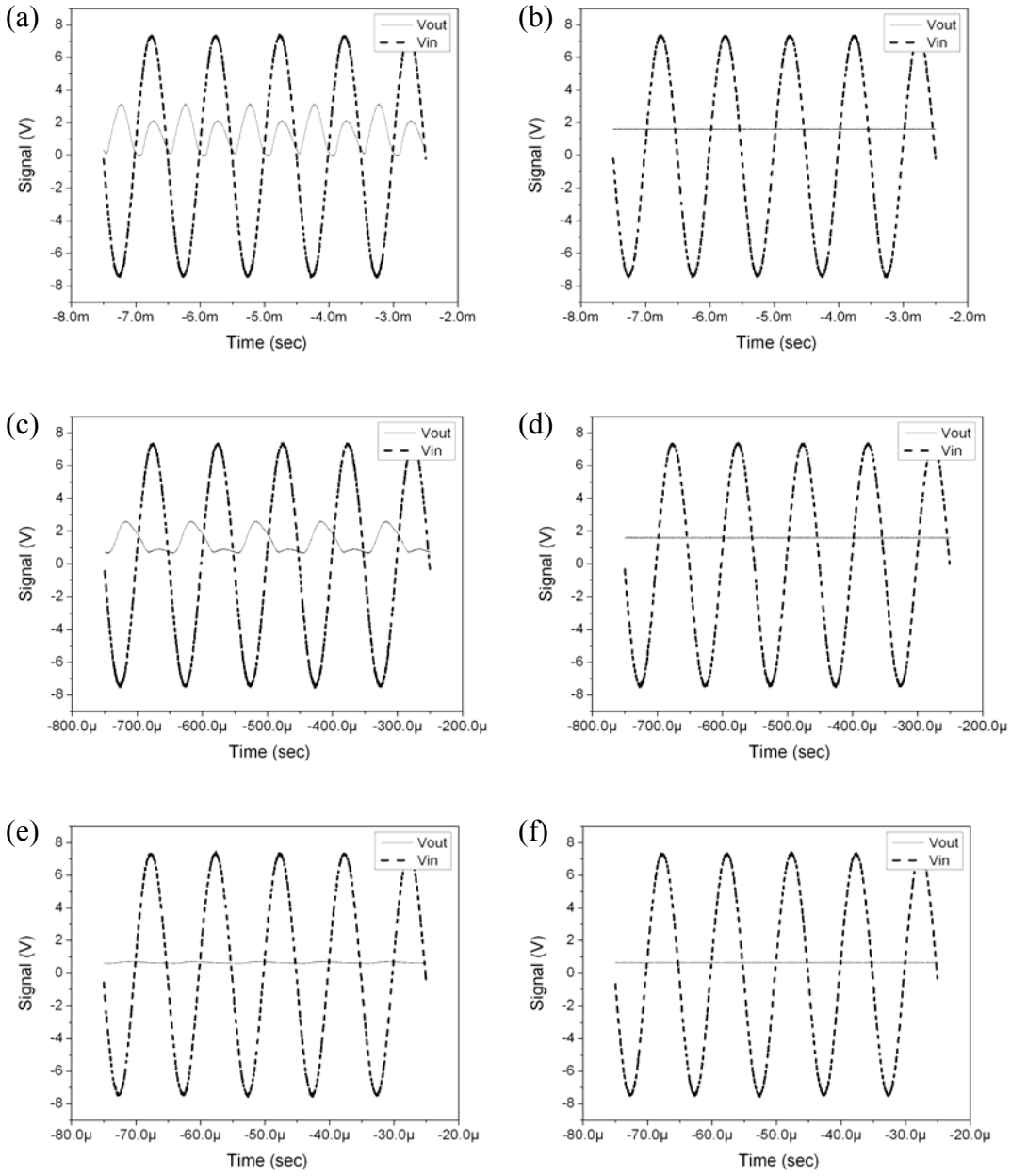

Fig. 6.14 The output wave forms for the full wave rectifiers consisting of pentacene FETs with channel lengths of 150 *nm*. The input frequencies were 1 kHz for (a) and (b); 10 kHz for (c) and (d); 100 kHz for (e) and (f). The waveforms in the right column show the measurements with a 10 *µF* capacitor connected at the output of the rectifier. The left column shows the measurements without a capacitor.

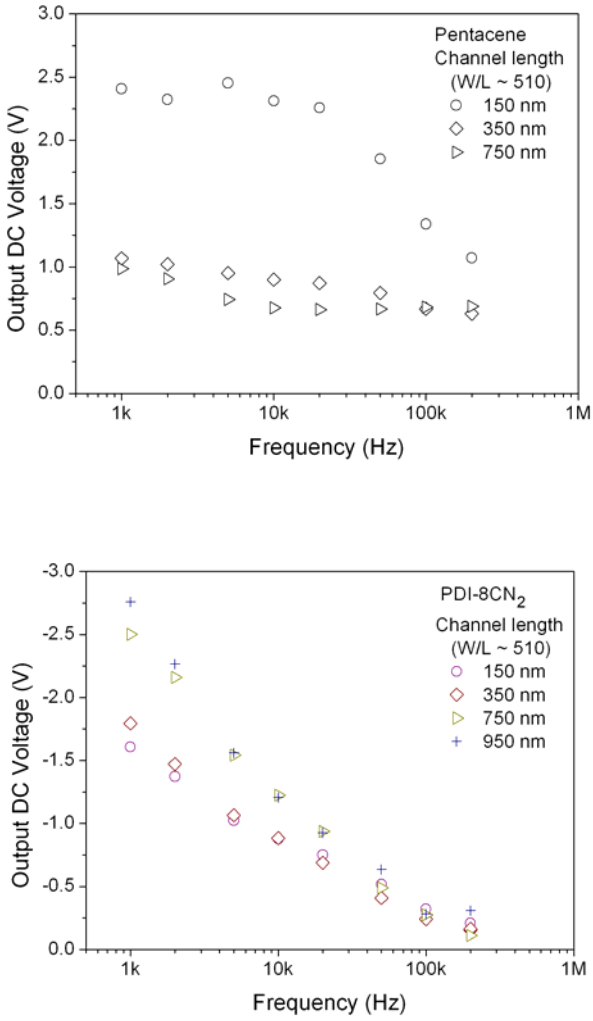

Fig. 6.15 The output DC voltages of the full wave rectifiers with a 10 μF capacitor connected at the output terminal. The rectifiers with pentacene (upper) and PDI-$8CN_2$ (lower) FETs.

Fig. 6.15 shows the overall performance of the full wave rectifiers with pentacene and PDI-8CN_2 FETs of various channel lengths. The output DC voltages were measured with the capacitor. The output of the rectifiers consisting of the PDI-8CN_2 FETs degraded much faster than that of the pentacene rectifiers.

6.4 Conclusion

Full wave rectifiers consisting of submicron OFETs were fabricated with pentacene and PDI-8CN_2. Although they produced rectified signals at a certain input frequency range, their performance was not sufficient for use in practical applications such as radio-frequency identification (RFID) tags, which require 13.56 MHz for operation. In order to achieve high frequency operation, the metal electrode to semiconductor contact must be improved further.

The complementary inverters with submicron channel lengths were fabricated and studied. The effect of bias stress on the complementary inverter was studied. It turned out that the degradation was not noticeable in the case of the complementary inverter whereas the output for logic 0 was degraded from an inverter created using only a p-type semiconductor [12].

References

[1] L. Dunn, D. Basu, L. Wang, and A. Dodabalapur, Appl. Phys. Lett., 88, 063507 (2006)

[2] R. Rotzoll, S.h Mohapatra, V. Olariu, R. Wenz, M. Grigas, O. Shchekin, K. Dimmler, and A. Dodabalapur, Mater. Res. Soc. Symp. Proc., 871E, I11.6 (2005)

[3] W. Clemens, W. Fix, J. Ficker, A. Knobloch, and A. Ullmann, J. Mater. Res., 19, 1963 (2004)

[4] A. S. Sedra and K. C. Smith, Microelectronic Circuits, 4th ed. (Oxford university press, New York, 2002)

[5] U. Zschieschang, H. Klauk, M. Halik, G. Schmid, and C. Dehm, Adv. Mater., 15, 1147 (2003)

[6] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, Adv. Mater., 14, 1717 (2002)

[7] H. Klauk, M., U. Zschieschang, F. Eder, G. Schmid, and C. Dehm, Appl. Pyhs. Lett. 82, 4175 (2003)

[8] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, T. N. Jackson, Solid-State Electronics, 47, 297 (2003)

[9] B. Yoo, T. Jung, D. Basu, A. Dodabalapura, B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks, Appl. Phys. Lett., 88, 082104 (2006)

[10] H. Y. Choi, S. H. Kim, and J. Jang, Adv. Mater., 16, 732 (2004)

[11] R. A. Street, A. Salleo, and M. L. Chabinyc, Phys. review B, 68, 085316 (2003)

[12] S. J. Zilker, C. Detcheverry, E. Cantatore, and D. M. de Leeuw, Appl. Phys. Lett., 79, 1124 (2001).

7 CONCLUSION

The solution processible polymer dielectric, poly(4-vinylphenol), used as the gate insulator in an organic field-effect transistor, was characterized under various environments since the polymer dielectric is not chemically inert during the fabrication process and afterwards. It was shown that the degree of cross-linking played important role in device performance with respect to the operation time. When the dielectric was less cross-linked the device was unstable in the presence of water molecules due to dielectric polarization. However, the dielectric polarization can be used effectively to compensate for the effects of the bias stress. Since the changes in source-drain currents due to the polarization and the bias stress effect are opposite, they can be canceled out by each other. This will enable us to do away with the requirement of an additional circuit to compensate the loss of control of the gate electrode due to the bias stress effect.

The scaling behavior of n-type and ambipolar OFETs was studied when the channel length was shrunk down to 15-25 *nm*. The field-effect mobility was decreased with decreasing channel lengths due to the contact effect and short channel effects. However, relatively high electron field-effect mobilities were observed from PDI-8CN2 FETs, the channel lengths of which were ranging from 15 *nm* to 100 *nm*. Amongst these FETs, a high electron mobility of 0.8×10^{-2} cm^2/Vs was observed from an OFET with 42 *nm* channel length, which was comparable to one observed in OFETs having

channel lengths in microns. Even though the field-effect mobilities from discrete OFETs are degraded, the operation speed of a circuit implemented with these OFETs will be faster than one with micron OFETs since the maximum switching frequency of a discrete transistor is inversely proportional to the square of the channel length. This shed light on the advantages of submicron circuits.

Submicron full wave rectifiers and complementary inverters, with channel lengths ranging from 150 *nm* to 950 *nm*, were first fabricated and their performances were studied. The full wave rectifiers operated in the non-quasi static mode in which the operation speed of the circuit was faster than the usual expectation based on the conventional characterization in steady state. The submicron complementary inverters showed stable outputs with time whereas a micron inverter with a single semiconductor component showed a change in output signal with time, due to the bias stress effect.

In conclusion, submicron and nanoscale OFETs were studied and it has been shown that even though the field-effect mobility decreased with decreasing channel lengths the operation speed of a circuit implemented with these submicron and nanoscale OFETs will increase.

Appendices

APPENDIX A

This appendix contains Solver.c program written in C language. This file was compiled into a dynamic-link library (DLL) file to be used with MATLAB script file. Functions contained in Solver.c are:

1) mexFunction - an interface function between MATLAB and the Solver.c

2) Poisson - a function to solve the Poisson equation

3) SolveChannelVer1 - a function to solve the current continuity equation

```
#include "mex.h"
#include <math.h>
#include <malloc.h>

#define DEBUG
#define DEBUG1

#ifdef DEBUG
#include <stdio.h>
char szTemp[256];
#endif

#define DIRICHLET      2
#define CHANNEL      32

#define e0    (8.854e-14)
```

```
#define q    (1.602e-19)

double Poisson(mxArray* mxDevice);
double SolveChannelVer1(mxArray* mxDevice, double tolerance);

void mexFunction( int nlhs, mxArray *plhs[], int nrhs, const mxArray *prhs[] )
{
    int iFunction;
    mxArray *mxDevice;
    double* pMaxChange;

    iFunction = (int)(double)*mxGetPr(prhs[0]);
    mxDevice = prhs[1];
    switch(iFunction) {
        case 0:
            plhs[0] = mxCreateDoubleMatrix(1, 1, mxREAL);
            pMaxChange = mxGetPr(plhs[0]);
            *pMaxChange = Poisson(mxDevice);
            break;
        case 1:
            plhs[0] = mxCreateDoubleMatrix(1, 1, mxREAL);
            pMaxChange = mxGetPr(plhs[0]);
            *pMaxChange = SolveChannelVer1(mxDevice, (double)*mxGetPr(prhs[2]));
            break;
    }
}

double Poisson(mxArray* mxDevice)
{
    double *pPcenter, *pPup, *pPright, *pPleft, *pPdown;
    double *pCharge, *pAttr;
    int row, col, offset2NextStart, rowOffset, isRowOdd;
    double tempPotential, prevPotential, change, maxChange;
    mxArray* mxPotential = mxGetField(mxDevice, 0, "mPotential");
    int nRow = mxGetM(mxPotential);
    int nCol = mxGetN(mxPotential);
```

```
mxArray* mxAttribute = mxGetField(mxDevice, 0, "mAttr");
mxArray* mxCharge = mxGetField(mxDevice, 0, "mCharge");
double w = (double)*mxGetPr(mxGetField(mxDevice, 0, "w"));
double w_bar = 1.0 - w;
double tolerance = (double)*mxGetPr(mxGetField(mxDevice, 0, "tol_poisson"));

while (1) {
    if (nRow & 1) /* odd number */
        isRowOdd = 1;
    else
        isRowOdd = 0;
    /* for black balls */
    maxChange = 0.0;
    pPcenter = (double*)mxGetPr(mxPotential) + 1 + nRow;
    pPright    = pPcenter + nRow;
    pPleft     = pPcenter - nRow;
    pPdown     = pPcenter + 1;
    pPup       = pPcenter - 1;
    pAttr      = (double*)mxGetPr(mxAttribute) + 1 + nRow;
    pCharge    = (double*)mxGetPr(mxCharge) + 1 + nRow;
    rowOffset = 0;
    offset2NextStart = isRowOdd ? 2 : 3;
    for (col = 2; col<nCol; col++) {
        for (row = rowOffset+2; row<nRow; row +=2) {
            if (*pAttr != DIRICHLET) {
                tempPotential = (*pPup + *pPdown + *pPright + *pPleft + *pCharge) / 4.0;
                prevPotential = *pPcenter;
                *pPcenter = w_bar * prevPotential + w * tempPotential;
                change = (*pPcenter>prevPotential) ? *pPcenter-prevPotential: prevPotential-
*pPcenter;
                maxChange = change > maxChange ? change : maxChange;
            }
            pPcenter += 2; pPup += 2; pPdown += 2; pPright += 2; pPleft += 2;
            pAttr += 2; pCharge += 2;
        }
```

```
                pPcenter += offset2NextStart; pPup += offset2NextStart; pPdown +=
offset2NextStart;
                pPright += offset2NextStart; pPleft += offset2NextStart;
                pAttr += offset2NextStart; pCharge += offset2NextStart;
                rowOffset = 1 - rowOffset;
                offset2NextStart = 4 - offset2NextStart;
            }

            /* for red balls */
            pPcenter = (double*)mxGetPr(mxPotential) + 2 + nRow;
            pPup = pPcenter + nRow;
            pPdown = pPcenter - nRow;
            pPright = pPcenter + 1;
            pPleft = pPcenter - 1;
            pAttr = (double*)mxGetPr(mxAttribute) + 2 + nRow;
            pCharge = (double*)mxGetPr(mxCharge) + 2 + nRow;
            rowOffset = 1;
            offset2NextStart = isRowOdd ? 2 : 1;
            for (col = 2; col<nCol; col++) {
                for (row = rowOffset+2; row<nRow; row +=2) {
                    if (*pAttr != DIRICHLET) {
                        tempPotential = (*pPup + *pPdown + *pPright + *pPleft + *pCharge) / 4.0;
                        prevPotential = *pPcenter;
                        *pPcenter = w_bar * prevPotential + w * tempPotential;
                        change = (*pPcenter>prevPotential) ? *pPcenter-prevPotential : prevPotential-
*pPcenter;
                        maxChange = change > maxChange ? change : maxChange;
                    }
                    pPcenter += 2; pPup += 2; pPdown += 2; pPright += 2; pPleft += 2;
                    pAttr += 2; pCharge += 2;
                }
                pPcenter += offset2NextStart; pPup += offset2NextStart; pPdown +=
offset2NextStart;
                pPright += offset2NextStart; pPleft += offset2NextStart;
                pAttr += offset2NextStart; pCharge += offset2NextStart;
                rowOffset = 1 - rowOffset;
```

```
                offset2NextStart = 4 - offset2NextStart;
            }
            if (maxChange < tolerance)
                break;
        }//end of while
        return maxChange;
    }

    double SolveChannelVer1(mxArray* mxDevice, double tolerance)
    {
        mxArray* mxPotential = mxGetField(mxDevice, 0, "mPotential");
        mxArray* mxCharge = mxGetField(mxDevice, 0, "mCharge");
        mxArray* mxMobility = mxGetField(mxDevice, 0, "mMobility");
        int nRow = mxGetM(mxPotential);
        int nCol = mxGetN(mxPotential);
        double es = e0 * (double)*mxGetPr(mxGetField(mxDevice, 0, "es"));
        double ei = e0 * (double)*mxGetPr(mxGetField(mxDevice, 0, "ei"));
        mxArray* mxSrChannel = mxGetField(mxDevice, 0, "srChannel");
        int left = (int)(double)*mxGetPr(mxGetField(mxSrChannel, 0, "left"));
        int right = (int)(double)*mxGetPr(mxGetField(mxSrChannel, 0, "right"));
        int top = (int)(double)*mxGetPr(mxGetField(mxSrChannel, 0, "top"));
        int bottom = (int)(double)*mxGetPr(mxGetField(mxSrChannel, 0, "bottom"));
        int nDepletionWidth = (int)(double)*mxGetPr(mxGetField(mxDevice, 0,
"nDepletionWidth"));
        double d = (double)*mxGetPr(mxGetField(mxDevice, 0, "unit"));
        double h = (double)*mxGetPr(mxGetField(mxDevice, 0, "unit"));
        double vVg = (double)*mxGetPr(mxGetField(mxDevice, 0, "vVg"));
        double tins = (double)*mxGetPr(mxGetField(mxDevice, 0, "hDielect")) * 1e-8; // cm
        double channel_height = (double)*mxGetPr(mxGetField(mxDevice, 0,"hChannel")) * 1e-8;
//cm
        double C = e0 * ei / tins; // F/cm2
        double change = 1;
        double maxChange = 1;
        int i;

        double P, Q, u, uVar, a, b, c;
```

```
        double *pPotential, *pMobility, *pCharge;
        double newPotential;

        while (maxChange > tolerance) {
            maxChange = 0;
            pPotential = (double*)mxGetPr(mxPotential)+ top-1 + nRow*(left-1); // left-top of the
channel
            pMobility = (double*)mxGetPr(mxMobility) + top-1 + nRow*(left-1);
            for (i=left; i<=right-nDepletionWidth; i++, pPotential+=nRow, pMobility+=nRow) {
                P = *(pPotential+nRow) + *(pPotential-nRow);
                Q = *(pPotential+nRow) - *(pPotential-nRow);
                u = *(pMobility);
                uVar = (*(pMobility+nRow)-*(pMobility-nRow))/(2*d);
                a = -8 * u;
                b = 2*d*uVar*Q + 4*u*P + 8*u*vVg;
                c = u*Q*Q - 2*d*uVar*vVg*Q - 4*u*P*vVg;
                newPotential = (-b - sqrt(b*b - 4*a*c))/(2*a);
                change = fabs(*pPotential - newPotential);
                if (change > maxChange)
                    maxChange = change;
                *pPotential = newPotential;
            }
        }
        pPotential = (double*)mxGetPr(mxPotential) + top-1 + nRow*(left-1); // left-top of the
channel
        pCharge = (double*)mxGetPr(mxCharge) + top-1 + nRow*(left-1);
        for (i=left; i<=right-nDepletionWidth; i++, pPotential+=nRow, pCharge+=nRow) {
            *pCharge = C * fabs(vVg-*pPotential) /    q / channel_height;
        }
        return maxChange;
    }
```

APPENDIX B

This appendix contains MEDICI scripts that calculate the transfer characteristic for a pentacene field-effect transistor.

1mak_init_mesh defines an initial mesh network

```
title This file generate initial grid

$ Include device profile
call       file=./include_device
$ Include parameters for organic semiconducting material.
$ Pentacene
call       file=./include_material

mesh       smooth=1 out.file=./data/OFET_init_mesh
x.mesh     width=@WElect h1=@WElect
x.mesh     width=@LChannel h1=@LChannel
x.mesh     width=@WElect h1=@WElect

y.mesh     depth=@HOrgSemi h1=@GridOrg
y.mesh     depth=@HDielect h1=@GridDiel

region     name=OrgSemi semicond y.max=@HOrgSemi
region     name=Dielec oxide y.min=@HOrgSemi y.max=@HOrgSemi+@HDielect
region     name=rSource semicond y.min=@HOrgSemi-@HElect y.max=@HOrgSemi
+            x.max=@WElect
region     name=rDrain semicond y.min=@HOrgSemi-@HElect y.max=@HOrgSemi
+          x.min=@WElect+@LChannel

electr     name=Gate bottom
electr     name=Source region=rSource
electr     name=Drain region=rDrain

Plot.2d    grid title="Initial Grid" fill scale
```

2refine_mesh refines the mesh network created by 1make_init_mesh

```
title This file reads the initial mesh and regrids it.

$ Include device profile
call        file=./include_device
$ Include parameters for organic semiconducting material.
$ Pentacene
call        file=./include_material

mesh in.file=./data/OFET_init_mesh ABC
+           JUNC.ABC      out.file=./data/OFET_mesh
+           ^GRIDTOP RFN.CRNR

abc.mesh            boundary region1=OrgSemi region2=Dielec
+           x.min=@WElect x.max=@WElect+@LChannel
+           grdcntr h1=0.01 h2=0.02

$abc.mesh           region=OrgSemi neighbor=dielec
$+          normal1=0.001 normal2=0.001 GRDLEFT
$abc.mesh           region=OrgSemi neighbor=source
$+          y.min=0 y.max=0.5 normal1=0.001 normal2=0.001 GRDDOWN
Plot.2d     grid title="Initial Grid" fill scale
```

3make_init_solution calculate an initial solution

```
TITLE   Device profile for BOC-type OFET

$$$ Include device profile
call        file=./include_device
$$$ Include parameters for organic semiconducting material.
$ Pentacene
call        file=./include_material
```

```
mesh      in.file=./data/OFET_mesh

$$$ Doping
profile   region=OrgSemi p-type n.peak=@OrgDope    uniform
+         out.file=./data/OFET_init_doping

$Plot.2d grid title="Initial Grid" fill scale

regrid    doping log max=1 ratio=2 smooth=1
+         in.file=./data/OFET_init_doping
plot.2d   grid title="Doping Regrid" fill scale

contact   name=gate n.poly
contact   name=source workfunc=@SWork
contact name=drain workfun=@DWork

materi    region=OrgSemi PERMITTI=@Permi AFFINITY=@Affinity
+         EG300=@EG300 NC300=@NC300 NV300=@NV300
mobil     region=OrgSemi mup0=@Mobility

$models ^conmob ^fldmob ^srfmob2
symb      carriers=0
method    iccg damped
solve
regrid    poten ignore=dielec ratio=.1 max=1 smooth=1
+         in.file=./data/OFET_init_doping out.file=./data/OFET_mesh_potential
plot.2d   grid title="Potential Regrid" fill scale

comment Initial solution using the refined grid.
symb carriers=0
solve out.file=./data/OFET_init_solution
```

4gate_ramp_up applies voltage to a gate electrode

```
title BOC type OFET - gate ramp up

$ This file produces solution for various gate voltages
$ for later IV curve calculation.

$--- Read mesh file
mesh      in.file=./data/OFET_mesh_potential
$--- Read zero bias solution
load      in.file=./data/OFET_init_solution
$--- Include predefined voltages
call      file=./include_voltage

$--- Newtons method and solve for holes
symb      newton carriers=1 hole
$mobil    region=silicon mup0=1.00

solve     v(gate)=-0.0 v(drain)=-0.0
$--- Ramp up VdSub
loop      steps=@nVdSub
call      file=./include_voltage
solve     v(gate)=-0.0 v(drain)=@vVdSub
l.end
load      out.file="./data/solution-Vg-0.0-Vd"@vVdSub
$--- Ramp up VgSub
loop      steps=@nVgSub
call      file=./include_voltage
solve     v(gate)=@vVgSub
l.end
load      out.file="./data/solution-Vg"@vVgSub"-Vd"@vVdEnd

$--- Threshold Region
assign    name=vVgPrev n.value=@vVgEnd
loop      steps=@nVg
call      file=./include_voltage
assign    name=nVgStep n.value=(@vVg-@vVgPrev)/@vVgStep
```

```
solve     elec=gate vstep=@vVgStep nstep=@nVgStep
load      out.file="./data/solution-Vg"@vVg"-Vd"@vVdEnd
assign    name=vVgPrev n.value=@vVg
l.end
```

5drain_ramp_up applies voltage to a drain electrode

```
title BOC type OFET - drain current

$--- Read mesh file
mesh      in.file=./data/OFET_mesh_potential

$--- Newtons method and solve for holes
symb      newton carriers=1 hole
$mobil    region=silicon mup0=1.00
$--- Read predefined voltages
call      file=./include_voltage

loop      steps=@nVg
call      file=./include_voltage
log       out.file="./data/IV-Vg"@vVg
load      in.file="./data/solution-Vg"@vVg"-Vd"@vVdEnd
assign    name=nVdStep n.value=(@vVd-@vVdEnd)/@vVdStep
solve     elec=drain vstep=@vVdStep nstep=@nVdStep
load      out.file="./data/solution-Vg"@vVg"-Vd"@vVd
l.end
```

include_device contains parameters for device structure

```
$ include this file to define device profile.

assign name=LDevice n.value=7.620
```

```
assign name=LChannel n.value=7.5
assign name=HChannel n.value=0.001

assign name=HElect n.value=0.1
assign name=WElect n.value=0.06

assign name=HDielect n.value=0.1
assign name=GridDiel n.value=0.01

assign name=HOrgSemi n.value=0.5
assign name=GridOrg n.value=@HElect
assign name=OrgDope n.value=1e16

$ Source/Drain workfunctions
assign    name=SWork n.value=5.1
assign    name=Dwork n.value=5.1

$ Variable for voltage contour
assign    name=vConGrid n.value=1

$ Variable for charge distribtion graph
assign    name=nCDgraph n.value=5
assign    name=xPoints n.value=(0.2, 0.4, 0.8, 1.2, 1.4)
assign    name=ystart n.value=@HOrgSemi
```

include_material contains parameters for materials

```
$ Parameters for organic semiconducting material.
$ Pentacene
assign    name=Permi n.value=(4.0)
assign    name=Affinity n.value=(2.6)
assign    name=EG300 n.value=(2.5)
assign    name=NC300 n.value=(5.8e21)
```

```
assign    name=NV300 n.value=(5.8e21)
assign    name=Mobility n.value=(8e-3)
```

include_voltage contains a bias condition

```
$ This file defines gate voltages and drain voltages.

$ Skip subthreshold region by increasing voltages roughly.
assign    name=nVdSub n.value=5
assign    name=vVdSub n.value=(-0.001, -0.005, -0.01, -0.02, -0.1)
assign    name=vVdEnd n.value=-0.1

assign    name=nVgSub n.value=5
assign    name=vVgSub n.value=(-0.005, -0.01, -0.02, -0.05, -0.1)
assign    name=vVgEnd n.value=-0.1

$ Threshold region
assign    name=nVg n.value=4
assign    name=vVg
+n.value=(-3+@vVgEnd, -6+@vVgEnd, -9+@vVgEnd, -12+@vVgEnd)
assign    name=vVgStep n.value=-0.5

assign    name=vVd n.value=-10+@vVdEnd
assign    name=vVdStep n.value=-0.5

$ Transient time analysis
assign    name=vVgTran n.value=-40
assign    name=vVdTran n.value=-40
assign    name=tStep n.value=1e-14
assign    name=tStop n.value=1e-4
```

Bibliography

H. Shirakawa, E. Louis, A. G. MacDiarmid, C. K. Chiang, A. J. Heeger, J. Chem. Soc. Chem. Commun., 16, 578 (1977)

B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger, and Z. Bao, Appl. Phys. Lett., 78, 2229 (2001)

C.W. Tang and S. A. VanSlyke, Appl. Phys. Lett., 51, 913 (1987)

P. Peumans, V. Bulovic, and S. R. Forrest, Appl. Phys. Lett., 76, 3855 (2000)

K. Tsukagoshi, J. Tanabe, I. Yagi, K. Shigeto, K. Yanagisawa, Y. Aoyagi, J. Appl. Phys., 99, 064506 (2006)

Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates, and M. McCreary, Nature, 423, 136 (2003)

L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, Nature, 434, 194 (2005)

T. Holstein, Ann. Phys. (N.Y.), 8, 325 (1959)

D. Emin, Phys. Rev. Lett., 25, 1751 (1970)

N. Karl, J. Marktanner, R. Stehle, and W. Warta, Synth. Met., 42, 2473 (1991)

R. M. Glaser and R. S. Berry, J. Chem. Phys., 44, 3797 (1966)

B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks, Appl. Phys. Lett., 88, 082104 (2006)

H. S. Byun, Y.-X. Xu, and C. K. Song, Thin Solid Films, 493, 278 (2005)

J. Lee, D. K. Hwang, J.-M. Choi, K. Lee, J. H. Kim, S. Im, J. H. Park, and E. Kim, Appl. Phys. Lett., 87, 023504 (2005)

H. Y. Choi, S. H. Kim, and J. Jang, Adv. Mater., 16, 732 (2004)

Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, IEEE Elect. Dev. Lett., 18, 606 (1997)

D. J. Gundlach, L. Jia, and T. N. Jackson, IEEE Elect. Dev. Lett., 22, 571 (2001)

I. Kymissis, C. D. Dimitrakopoulos, and S. Prurushothaman, IEEE Trans. on Elect. Dev., 48, 1060 (2001)

A. Salleo, M. L. Chabinyc, M. S. Yang, and R. A. Street, Appl. Phys. Lett., 81, 4383 (2002)

K. Seshadri, and D. Frisbie, Appl. Phys. Lett., 78, 993 (2001)

L. Burgi, H. Sirringhaus, and R. H. Friend, Appl. Phys. Lett., 80, 2913 (2002)

R. Rotzoll, S.h Mohapatra, V. Olariu, R. Wenz, M. Grigas, O. Shchekin, K. Dimmler, and A. Dodabalapur, Mater. Res. Soc. Symp. Proc. 871E, I11.6 (2005)

W. Clemens, W. Fix, J. Ficker, A. Knobloch, and A. Ullmann, J. Mater. Res., 19, 1963 (2004)

S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York, 1982)

M.A. Alam, A. Dodabalapur, and M. Pinto, IEEE Trans. on Elect. Dev., 44, 1332 (1996)

G. Horowitz and P. Delannoy, J. Appl. Phys. 70, 469 (1991)

N. Tessler and Y. Roichman, Appl. Phys. Lett., 79, 2987 (2002)

M. J. Deen, O. Marinov, S. Holdcroft, W. Woods, IEEE Trans. on Elect. Dev., 48, 1688 (2001)

S. Martin, J.-Y. Nahm, and J. Kanicki, J. Elect. Mater., 31, 512 (2002)

Y. Roichman and N. Tessler, Appl. Phys. Lett., 80, 151 (2002)

T. Li, J. W. Balk, P. P. Ruden, I. H. Campbell, and D. L. Smith, J. Appl. Phys., 91, 4312 (2002)

G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, J. Appl. Phys., 87, 4456 (2000)

G. Horowitz, R. Hajlaoui, D. Fichou, and A. E. Kassmi, J. Appl. Phys., 85, 3202 (1999)

J. H. Schon and B. Batlogg, J. Appl. Phys., 89, 336 (2001)

N. J. Watkins, L. Yan, and Y. Gao, Appl. Phys. Lett., 80, 4384 (2002)

N. Koch, A. Kahn, J. Ghijsen, J.-J. Pireaux, J. Schwartz, R. L. Johnson, and A. Elschner, Appl. Phys. Lett., 82, 70 (2003)

G. Horowitz, R. Hajlaoui, R. Bourguiga, and M. Hajlaoui, Synth. Met., 101, 401 (1999)

E. Kreyszig, Advanced Engineering Mathmatics, 7th ed. (John Wiley & Sons, 1993)

H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, T. N. Jackson, Solid-State Electronics, 47, 297 (2003)

R. J. Chesterfield, J. C. McKeen, C. R. Newman, and C. D. Frisbie, J. Appl. Phys., 95, 6396 (2004)

C. R. Newman, R. J. Chesterfield, J. A. Merlo, and C. D. Frisbie, Appl. Phys. Lett., 85, 422 (2004)

L. Wang, D. Fine, T. Jung, D. Basu, H. V. Seggern, and A. Dodabalapur, Appl. Phys. Lett., 85, 1772 (2004)

R. Brederlow, S. Briole, H. Klauk, M. Halik, U. Zschieschang, G. Schmid, J.-M. Gorriz-Saez, C. Pacha, R. Thewes, and W. Weber, IEEE ISSCC (2003)

C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, J. M. Shaw, Science, 283, 822 (1999)

L. Torsi, A. Dodabalapur, L. J. Rothberg, A. W. P. Fung, and H. E. Katz, Phys. Review. B, 57, 2271 (1998)

R. A. Street, D. Knipp, and A. R. Völkel, Appl. Phys. Lett., 80, 1658 (2002)

Z. Bao, Adv. Mater., 12, 227 (2000)

A. Facchetti, M. Mushrush, M. H. Yoon, G. R. Hutchison, M. A. Ratner, and T. J. Marks, J. A.C.S., 126, 13859 (2004)

R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. S. Filho, J. L. Brédas, L. L. Miller, K. R. Mann, and C. D. Frisbie, J. Phys. Chem. B, 108, 19281 (2004)

L. Wang, D. Fine, and A. Dodabalapur, Appl. Phys. Lett., 85, 6386 (2004)

A. Dodabalapur, Z. Bao, A. Makhija, J. G. Laquindanum, V. R. Raju, Y. Feng, H. E. Katz, and J. Rogers, Appl. Phys. Lett., 73, 142 (1998)

H. Sirringhaus, N. Tessler, and R. H. Friend, Science, 280, 1741 (1998)

C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, Appl. Phys. Lett., 80, 1088 (2002)

G. H. Gelinck, H. E. A. Huitema, E. V. Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. Putten, T. C. Geuns, M. Beenhakkers, J. B. Giesbers, B. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. Rens, and D. M. Leeuw, Nature Mater., 3, 106 (2004)

H. Klauk, M. Halik, U. Zschieschang, F. Eder, G. Schmid, and C. Dehm, Appl. Phys. Lett., 82, 4175 (2003)

U. Zschieschang, H. Klauk, M. Halik, G. Schmid, and C. Dehm, Adv. Mater., 15, 1147 (2003)

M. Halik, H. Klauk, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, Adv. Mater., 14, 1717 (2002)

R. A. Street, A. Salleo, and M. L. Chabinyc, Phys. review B, 68, 085316 (2003)

D. Li, E. J. Borkent, R. Nortrup, H. Moon, H. Katz, and Z. Bao, Appl. Phys. Lett., 86, 042105 (2005)

C. Huang, J. E. West, and H. E. Katz, Mater. Res. Soc. Symp. Proc., 889, 0889-W08-07.1 (2006)

C. R. Newman, C. D. Frisbie, D. A. da Silva, J. L. Bredas, P. C. Ewbank, and K. R. Mann, Chem. Mater., 16, 4436 (2004)

H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y.-Y. Lin, and A. Dodabalapur, Nature 404, 478 (2000)

B. A. Jones, M. J. Ahrens, M.-H. Yoon, A. Facchetti, T.J. Marks, and M. R. Wasielewski, Angew. Chem. Int. Ed., 43, 6363 (2004)

E. J. Meijer, D. M. de Leeuw, S. Setayesh, E. van Veenendaal, B.-H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, and T. M. Klapwijk, Nat. Mater., 2, 678 (2003)

Y. Hayashi, H. Kanamori, I. Yamada, A. Takasu, S. Takagi, and K. Kaneko, Appl. Phys. Lett., 86, 052104 (2005)

E. Kuwahara, Y. Kubozono, T. Hosokawa, T. Nagano, K. Masunari, and A. Fujiwara, Appl. Phys. Lett., 85, 4765 (2004)

A. Dodabalapur, H. E. Katz, L. Torsi, and R. C. Haddon, Appl. Phys. Lett., 68, 1108 (1996)

M. Leufgen, U. Bass, T. Muck, T. Borzenko, G. Schmidt, J. Geurts, V. Wagner, and L.W. Molenkamp, Synth. Met.,146, 341 (2004)

Y. Takahashi, T. Hasegawa, Y. Abe, Y. Tokura, K. Nishimura, and G. Saito, Appl. Phys. Lett., 86, 063504 (2005)

M.J. Ahrens, M. J. Fuller, and M. R. Wasielewski. Chem. Mater., 15, 2684 (2003)

M.-H. Yoon, A. Facchetti, and T. J. Marks PNAS, 102, 4678 (2005)

A. Dodabalapur, L. Torsi, and H. E. Katz, Science, 268, 270 (1995)

A. Dodabalapur, H.E. Katz, L. Torsi, and R. C. Haddon, Science, 269, 1560 (1995)

J. Wang, H. Wang, X. Yan, H. Huang, and D. Yan, Appl. Phys. Lett., 87, 093507 (2005)

L. Dunn, D. Basu, L. Wang, and A. Dodabalapur, Appl. Phys. Lett., 88, 063507 (2006)

A. S. Sedra and K. C. Smith, Microelectronic Circuits, 4th ed. (Oxford university press, New York, 2002)

S. J. Zilker, C. Detcheverry, E. Cantatore, and D. M. de Leeuw, Appl. Phys. Lett., 79, 1124 (2001)

Vita

Tae Ho Jung was born in Seoul, Korea on November 20th 1973, the son of Kihyun Jung and Jungja Choi. He graduated Karak high school, Seoul. He received the B.S. and M.S. degrees in electronics engineering from Korea University, Korea in 1998 and 2000, respectively. During college, he served in the military one and half year. He joined Prof. Ananth Dodabalapur's group for Doctor of Philosophy in the Microelectronics Research Center at the University of Texas at Austin in 2001.

Permanent address: 11215 Research Blvd., Apt 1162, Austin, TX 78759

This dissertation was typed by the author.