The Dissertation Committee for Siddarth A. Krishnan certifies that

this is the approved version of the following dissertation:

CHARACTERIZATION AND RELIABILITY OF HFO_2 AND HFSION GATE DIELECTRICS WITH TIN METAL GATE

Committee

_____

Jack C. Lee, Supervisor

_____

Leonard F. Register

_____

Dean P. Neikirk

_____

Paul S. Ho

_____

Jeff J. Peterson

CHARACTERIZATION AND RELIABILITY OF HFO_2 AND HFSION GATE DIELECTRICS WITH TIN METAL GATE

by

Siddarth A. Krishnan, B.Tech., M.S.

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

December 2005

Dedicated to

Jack Lee, whose faith in me surpassed my own

My parents, whose values they passed on to me in strength

and

Shobha, whose boundless encouragement inspired and motivated me

Acknowledgements

"For knowest thou what argument
Thy like to thy neighbor's creed has lent,
All are needed by each one;
Nothing is fair or good alone"

– Ralph Waldo Emerson.

Several people have been enablers in the successful completion of this work. I would like to first acknowledge the contribution of my parents and sister, whose faith in me was unflinching, and encouragement, unending. For providing me every possible resource affordable to them, for educating me, for encouraging me at the successes along the way and standing by me at the failures, I stand indebted to them. At every faltering step, I drew inspiration from their completely selfless support.

I would also like to thank Professor Jack Lee, for his guidance and encouragement. He helped me identify my strengths and weaknesses and supported me through all the roadblocks that I had to overcome. His enthusiastic approach to not just research, but to also teaching undergraduate and graduate classes has stemmed a desire to teach in me. I cannot thank him enough for his decision to aid me through periods of uncertainty in my research.

A constant source of support, during my time in Austin has been my friend, Shobha Vasudevan, a doctoral student at UT. Without her, I can safely assert, I would not have been successful in my pursuit of this dream. A formidable intellectual with an indomitable will, her encouragement and wise guidance at various

junctures helped me immeasurably. Her ever-cheerful and positive disposition has inspired in me the desire to cultivate that spirit in myself. She, along with Vinod provided the support framework for my tenure in Austin, making this professional endeavor a thoroughly enjoyable experience. I would like thank her for her invaluable counsel and her selfless support.

Another significant influence on my life has been my friend and erstwhile roommate, Vinod Viswanath, another doctoral student at UT. His determination and moral rectitude cannot help but inspire his acquaintances to emulate him, and I am no different. A selfless leader, he helped me formulate my goals in both my personal and professional bearings. I have learnt much from his expansive technical expertise at topics that varied from digital electronics to health and nutrition. I would also like to thank Kunal Punera, another erstwhile roommate of mine for being a great friend and for providing innumerable fun outings, along with some very insightful guidance on various technical issues.

I would like to thank Dr. Paul Kirsch, my manager at Sematech, for the technical guidance and support through my sojourn as an intern there. He has what I perceive to be great managerial qualities, combined with a very deep understanding of device and material physics and I am thankful that he let me draw upon his technical expertise. I would also like to thank Dr. Manuel Quevedo-Lopez, whose industry has contributed heavily to many of Sematech's deliverables. He helped fabricate many of the samples I utilized for my reliability measurements, without which this research would never have been completed. He has also been a great friend and mentor. Dr. Jeff Peterson, with

whom I collaborated on various projects, while at Sematech is another person I would like to offer thanks to. He helped me by providing samples and also in setting up experiments and analyzing the data. He mentored me through several projects, during which time I learnt much of what I was to apply to the bulk of my research.

I thank my committee members, Prof. Dean Neikirk, Prof. Frank Register and Prof. Paul Ho, for mentoring this dissertation.

I would also like to thank Dr. Rino Choi, Dr. Rusty Harris, Dr. Byoung Hun Lee, Dr. Gennadi Bersuker, Dr. Hong-Jyh Li, Dr. Chadwin Young and Dr. Sundar Gopalan for some very fruitful technical debates and insightful advice.

Kenneth Matthews, of ATDF, helped steepen my learning curve with various test equipment in the lab and continues to help set up experiments and I would like to express my gratitude to him. Several graduate students have helped in various capacities and I would like to acknowledge their contribution to this work: Changyoung, Sejong, Changwan, Injo, Hyoungsub, Feng are some of the current students. Amongst former graduate students in the group, I would like to thank Katsu, Young-Hee, Renee, Changseok and Hag-Ju.

I would also like to thank Prof. Bob Wallace and Gaurang Pant for providing assistance with XRD measurements.

CHARACTERIZATION AND RELIABILITY OF HFO_2 AND HFSION GATE DIELECTRICS WITH TIN METAL GATE

Publication No. _____

Siddarth A. Krishnan, Ph.D.

The University of Texas at Austin

Supervisor: Jack C. Lee

"*Give me a place to stand, and I will move the Earth*" – Archimedes (235 B.C.)

Since the invention of the integrated circuit in 1958, the semiconductor industry has progressed at a fiery pace, through aggressive shrinking of the transistor channel length and associated device dimensions. The problems associated with such aggressive scaling are many-fold and have been dealt with by clever modifications or additions to existing process technology. However, as the 65 nm technology node nears production, the semiconductor industry hits a fundamental physical limitation: The thickness of the gate dielectric, Silicon Dioxide (SiO_2) has been reduced to such an extent that the tunneling leakage current through the gate stack is reaching untenable levels. High permittivity dielectrics or high-κ dielectrics are being investigated to replace SiO_2 in order to preserve the capacitance while maintaining larger physical thickness to keep the leakage

current down. However, the introduction of high-κ materials into the conventional process flow is rendered difficult by various issues. It has been shown that gate stacks with high-κ materials have severely degraded mobility, while possessing large densities of charge traps. Additional concerns include the pinning of Fermi level at the midgap of the silicon bandgap, yielding undesirable threshold voltages, dielectric phase separation in ternary high-κ materials, high interface state density, low crystallization temperature and growth of a low-κ interfacial layer. We present a systematic study of the reliability aspects of hafnium based dielectrics with TiN gate electrode, and propose a robust and reliabile dielectric for introduction into CMOS product flow. Stress induced leakage current or SILC is studied in thick HfO_2 dielectrics with TiN gate electrode and it has been observed that significant low voltage SILC-like behavior is exhibited when nMOSFETs and pMOSFETs are stressed under positive biased stress. Such SILC behavior is also shown to be reversible when a negative voltage is applied after the stress, or if the devices are relaxed with a 0V bias. This reversible low-voltage SILC is attributed to electrons being trapped during the stress, which subsequently detrap during the I-V sweeps, leading to the appearance of SILC-like behavior. Mobility degradation in high-κ gate stacks is studied and it is proposed that the mobility degradation is a combination of remote coulomb scattering, due to fixed charges in the dielectric and phonon scattering. Thinning the high-κ dielectric down is offered as a solution to reduce the mobility degradation. Positive bias temperature instability is studied, and it is shown that the threshold voltage instability can be reduced to insignificant levels by reducing the thickness of the dielectric. However, the threshold voltage instability of thick high-κ

dielectrics remains problematic and will need to be solved before high-κ gate stacks can be incorporated into low power applications. It is shown that incorporating nitrogen into the dielectric through plasma nitridation or thermal nitridation could be used to reduce charge trapping in thick dielectrics. Negative bias temperature instability is shown to be a combination of electron detrapping from the high-κ layer and interface state creation due to hole injection into the interfacial layer. Although the interface state creation is made slightly worse by thinning the dielectric down, the threshold voltage shift is still less significant in thin dielectrics.

While the introduction of high-κ dielectrics can now be considered viable, caution needs to applied while integrating metal gates into the product flow, for the problem of fermi-level pinning still remains unsolved. An outline of all the remaining issues with such high-κ / metal gate gate stacks is presented at the end of this report.

Table of Contents

Chapter 1

Introduction

1.1 Motivation for High-κ Dielectrics

The performance of integrated circuits has been improving continuously primarily due to the shrinkage of Metal-Oxide-Semiconductor (MOS) transistors[1]. The reduction of channel length, called scaling, is accompanied by reduction in size of most of the other features, consequent to which, the entire circuit scales in size. Figure 1.1 shows the increase in performance due to scaling, over the years. This performance increase over the years occurs at a rate predicted by Intel co-founder Gordon Moore and is called Moore's law in his honour.

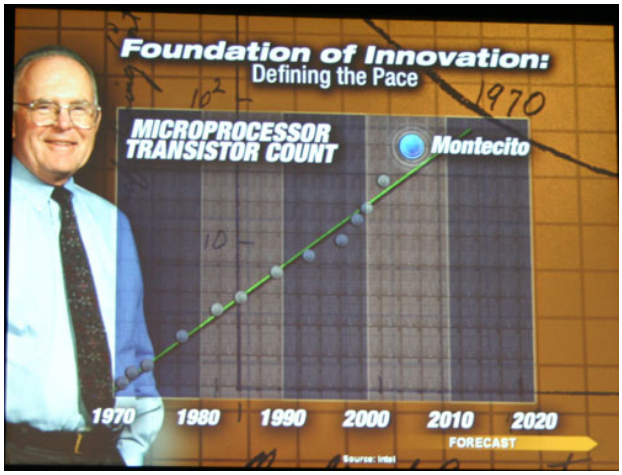


Figure 1.1: Moore's law – Increase in performance due to scaling [2].

Minimum feature size has shrunk more than ten-fold and the number of transistors has increased by more than three orders of magnitude in the last 20 years. There have been

many fundamental problems that have been posed over the technology generations, like hot carrier reliability and drain induced barrier lowering. It was possible to overcome these barriers with innovative technology solutions like halo-doping and LDDs [3]. For the first time, however, technological evolution in the near-future nodes is facing a fundamental roadblock. The thickness of the gate dielectric, Silicon dioxide has been scaled to the extent that only a few atomic layers remain. Silicon dioxide (SiO_2) has many qualities that has made it the dielectric of choice for decades in MOS processing, namely[4]:

a) Excellent thermal stability, on contact with silicon substrate.
b) Good interface with silicon substrate, with low interface trap density.
c) Low bulk fixed charges.
d) Good lattice match with Silicon.
e) Easy to grow or deposit in a wide variety of techniques.

Indeed, SiO_2 has been one of the primary reasons for the industry to sustain silicon technology over decades. The electrical thickness or equivalent oxide thickness (EOT) of the gate dielectric needs to be scaled along with channel length for the scaling rules to apply[5]. Figure 1.2 shows Equivalent Oxide Thickness scaling with technology node[6].

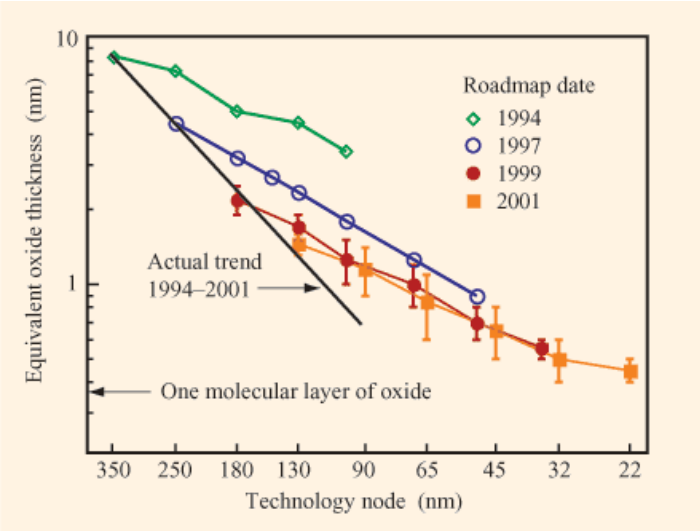


Figure 1.2: EOT scaling with technology – Current technologies[6].

The tunneling leakage current, increases exponentially with decreasing T_{ox} [7], as shown in equation 1.1.

$$I_{ox} = K_2 W \left(\frac{V}{T_{ox}}\right)^2 e^{-\alpha T_{ox}/V}$$ ……..Equation 1.1[8].

The gate leakage current, along with subtreshold leakage current, leads to off state static power consumption in the circuits [8]. Figure 1.3 illustrates the increase of power consumption over the years[8].

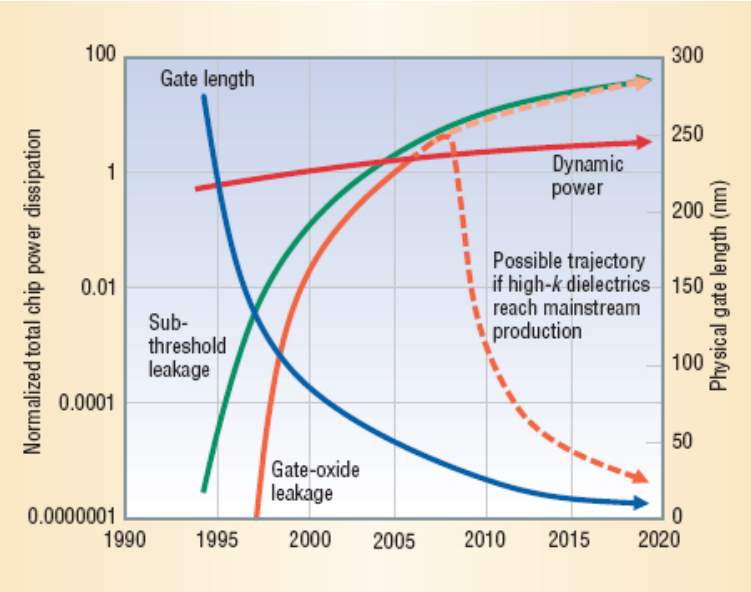


Figure 1.3: Normalized total chip power consumption over the years – large increase in the near future [8].

The leakage current density as a function of gate voltage for different SiO_2 thicknesses is shown in figure 1.4 [9]. The reliability of SiO_2 dielectrics of such low thicknesses is another concern [10].

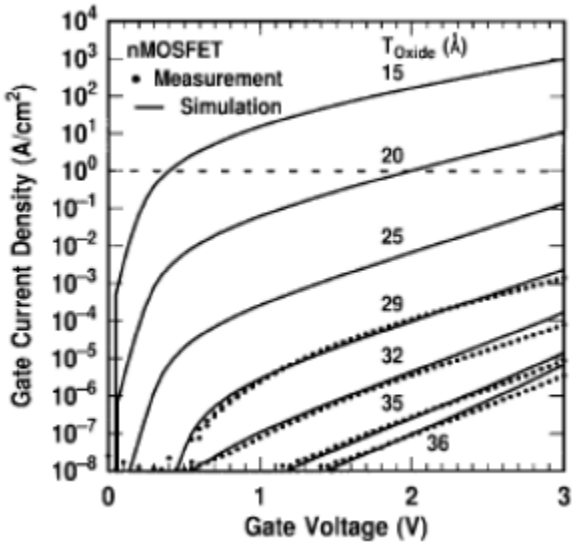


Figure 1.4: Leakage current density vs. gate voltage – for different thicknesses of SiO_2

Thinner gate dielectrics are required in order to facilitate the achievement of higher capacitance [5]. As the channel length is reduced, higher capacitance is needed to attain better control over the channel, thereby suppressing short channel effects and achieving higher drive current. The gate capacitance is given by equation 1.2.

$C_{ox} = (\varepsilon_0 \kappa) / T_{phys}$ ……..Equation 1.2

Where ε_0 is the vacuum permittivity, κ is the relative dielectric constant or dielectric constant (also referred to as ε_R). It can be seen that the capacitance can be increased decreasing the thickness *or* increasing κ. The materials for which the dielectric constant is higher than that of SiO_2 (κ_{SiO2} = 3.9) are called "high-κ" materials. The equivalent thickness of SiO_2 needed to achieve the same capacitance as the capacitance of a high-κ material of a given physical thickness t_{phy} is called Capacitance Equivalent thickness (CET). CET can be defined as:

$CET = (\varepsilon_{SiO2}/\kappa_{high\text{-}k})*T_{phys.}$

Various high-κ materials have been studied over the last decade and this dissertation deals with reliability issues associated with hafnium based high-κ materials.

1.2 High-κ Dielectrics: The Road So Far

1.2.1 "Higher-κ" Materials

There has been frenetic activity in the research community in the last decade in the area of high permittivity dielectrics. Dielectric materials with κ values between 7-30 are defined as high-κ dielectrics, while materials with κ values between 30-100 are termed "higher-κ" dielectrics. Indeed, higher-κ dielectrics like Barium Strontium Titanate (BST) and Lead Zirconium Titanate (PbZrTiO) were amongst the first to be investigated. However, the capacitance values offered by these dielectrics are too high for the near-future technology [11] besides which, the bandgap of these materials is too small for electrical viability [12, 13]. Due to the availability of materials with more desirable qualities, the consideration of higher-κ materials was abandoned (at least temporarily). Figure 1.5 shows electrical properties of various dielectric materials that have been investigated [12].

	Gap (eV)	CNL (eV)	ϵ_∞	S calculated	EA (eV)	Calculated CB offset (eV)
Si	1.1	0.2	12		4.0	
SiO_2	9		2.25	0.86	0.9	3.5 (exp)
Si_3N_4	5.3		3.8	0.51	2.1	2.4 (exp)
$SrTiO_3$	3.3	2.60	6.1	0.28	3.9	−0.1
$PbTiO_3$	3.4	1.90	6.25	0.31	3.5	0.6
$BaZrO_3$	5.3	3.7	4	0.53	2.5	0.8
$PbZrO_3$	3.7	2.6	4.8	0.4	3.2	0.2
Ta_2O_5	4.4	3.3	4.84	0.40	3.2	0.36
$SrBi_2Ta_2O_9$	4.1	3.3	5.3	0.35	3.3	0.15
TiO_2	3.05	2.2	7.8	0.18	3.9*	0
ZrO_2	5.8	3.6	4.8	0.41	2.5*	1.4
HfO_2	6	3.7	4	0.53	2.5*	1.5
Al_2O_3	8.8	5.5	3.4	0.63	1*	2.8
Y_2O_3	6	2.4	4.4	0.46	2*	2.3
La_2O_3	6*	2.4	4	0.53	2*	2.3
$ZrSiO_4$	6*	3.6	3.8	0.56	2.5*	1.5
$HfSiO_4$	6*	3.6	3.8	0.56	2.5*	1.5

Table 1.1: Electrical properties of various materials [12].

1.2.2 Other high-κ materials

As focus settled on high-κ materials with κ values ~ 10-30, tantulum pentoxide (Ta_2O_5) was studied extensively [14-16]. Although MOS capacitors and short channel transistors with excellent electrical properties and CETs below 10Å were reported [14], it was generally agreed that Ta_2O_5 is thermally unstable in contact with silicon and forms tantulum silicide pockets in the gate stack. Titanium oxide was another material [17] that was investigated because of the high κ value that it offers. Similar to Ta_2O_5, TiO_2 was also found to be thermally unstable in contact with silicon. Moreover, both Ta_2O_5 and TiO_2 have low barrier heights for electron conduction, leading to high leakage currents [17].

Indeed, these drawbacks formed the basis for further investigation into high-κ dielectrics for MOS applications. The rules formulated for high-κ dielectrics were as follows [18]:

a) High dielectric constant ~ 10-30.

b) Bandgap > 5eV.

c) Good thermal stability in contact with silicon.

d) Amorphous after high temperature processing – Defect density in poly-crystalline materials is generally high.

e) Good interface with top electrode (Poly-si or metal gate).

f) Scalable to EOT < 10Å.

g) Form good interface with silicon – Low interface trap density.

h) Good mechanical properties.

Two lanthanide materials emerged from a careful consideration of the above specified rules – hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) (and subsequently, their silicates) [18, 19]. Both of these oxides exhibited excellent thermal and electrical properties and capacitors and transistors with sub-nm EOTs were demonstrated. While HfO_2 was found to have good electrical qualities with both poly-silicon (poly-Si) gate electrode [20]and metal gates [21], ZrO_2 was found to be unstable with poly-Si gate electrode, due to silicide formation during the poly-Si deposition [22]. Zirconium Oxide was therefore abandoned in favor of HfO_2 and hafnium silicate. Subsequently, however,

owing to many of poly-silicon's drawbacks as the gate electrode (see next section), metals like titanium Nitride and tantalum Nitride have become strong contenders for the gate electrode, in conjunction with hafnium based dielectrics, thereby rendering the reason to avoid ZrO_2 irrelevant.

1.3 Hafnium Based Dielectrics with Metal Gates

Poly-silicon, the gate electrode which has been used with SiO_2 dielectrics, is also running into roadblocks. As the scaling heads towards sub-nm EOTs, poly-depletion becomes a significant deterrent to the use of this gate electrode [23]. Poly-depletion occurs due to the formation of a thin depletion layer in the poly-electrode, despite the high dopant densities. This causes an increase in EOT (loss in capacitance) due to an increase in physical thickness, and consequently, causes drain current loss. This additional EOT is in the order of a few Å and cannot be ignored as the EOT targets are scaled down to below 10Å.

As the technologies scale down, the dopant densities in poly-Si need to be increased in order to avoid the poly depletion effect. In the case of pMOS transistors, this is achieved by increasing the dose of Boron dopant (p-type). Boron, however, has high diffusivity in SiO_2 [23] (and even higher diffusivity in HfO_2 [24]) and diffuses down to the substrate, causing faulty devices. Metal gate electrodes have therefore attracted a lot of attention over the years. Several metals like titanium [25], tungsten (W) [26], titanium nitride (TiN) [27], tantalum nitride (TaN)[27], titanium silicon nitride (TiSiN), molybdenum [28], molybdenum nitride [28], molybdenum silicon nitride (MoSiN), hafnium nitride (HfN) [29] and hafnium silicide (HfSi) [30] have been investigated. Like

in the case of SiO_2, attempts are underway to identify metal gates with work functions which can provide nMOS and pMOS transistors with appropriate threshold voltages [31]. Attempts have also been made to integrate two different metals with nMOS and pMOS type work function into the standard cMOS flow [32]. Schaeffer et al investigated a variety of metals and reported that most metals on hafnium based dielectrics have work functions close to the mid-gap of silicon [31]. Figure 1.5 shows all the works functions of various metal gates that investigated by schaeffer et al.

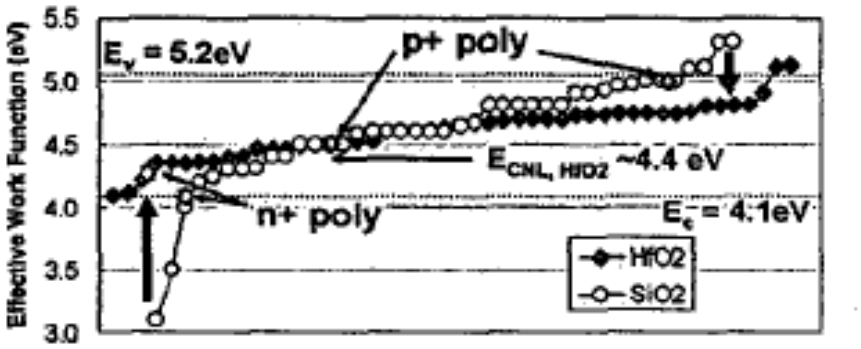


Figure 1.5: Effective work function of various metals on HfO_2 and SiO_2 [31].

This phenomenon is due to the pinning of the fermi level to the mid-gap of silicon, due to dipoles formed at the interface between the metal and the hafnium based dielectric. The effect of fermi-level pinning is also seen in poly-silicon gate electrodes on hafnium based dielectrics (figure 1.5). There have been attempts to modify the top interface with a different dielectric, with both metal gates and poly-silicon gates in order to achieve the correct effective work function. Aluminum oxide has been studied as the top interface dielectric, for pMOS work function metals on hafnium based dielectrics

[33]. The search for the appropriate metals and integration techniques still continues as we get closer to the 65nm and 45nm technology nodes.

1.4 High-κ dielectrics: Primary concerns

1.4.1 Mobility Degradation

The timing delay through VLSI circuits is scaled down by increasing the drain current in successive generations. The drain current is given by:

$I_D = \mu C_{ox}(W/2L)\,(2(V_G-V_{TH})\,V_{DS} - V_{DS}^2)$ for $V_{DS} < V_G - V_T$ …..Equation 1.3 (a)

$I_D = \mu C_{ox}(W/2L)\,(V_G-V_{TH})^2$ for $V_{DS} > V_G - V_T$ …….Equation 1.3 (b)

The intrinsic mobility of the carrier needs to be preserved as the drain current is increased by scaling L (channel length) and oxide capacitance (C_{ox}). In hafnium based dielectrics, however, the mobility has been reported to be severely degraded, as compared to SiO_2 dielectrics, which follows a universal curve. There are many fundamental phenomena responsible for carrier mobility degradation in hafnium based dielectrics:

a) Remote coulomb scattering from fixed charges in the bulk high-κ dielectric [34, 35].
b) Soft optical phonons that couple with phonons in the silicon substrate to provide addition scattering [35-37].
c) Remote roughness scattering: Due to roughness in the top interface layer [34].
d) Loss of inversion charge in the channel due to “trapping” in trap sites in the high-κ layer – this leads to the appearance of mobility degradation[38, 39].

Zhu et al [35] proposed that the mobility degradation in HfO_2 is due to a combination of phonon scattering, coulomb scattering and remote phonon scattering, especially at high fields. Figure 1.6 illustrates the different degradation mechanisms and the fields at which they dominate.

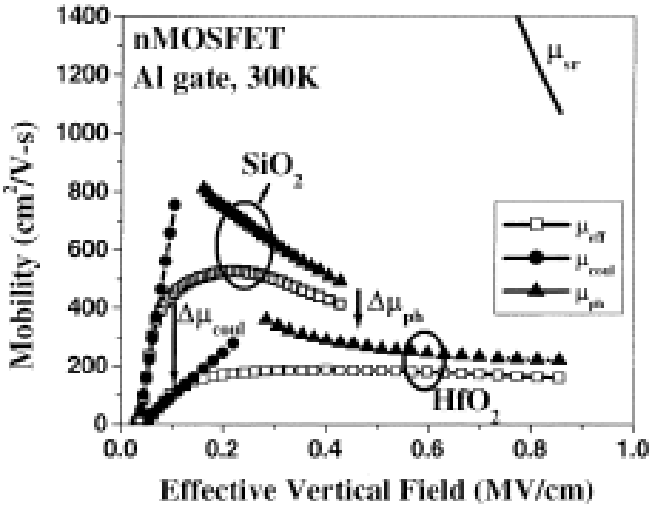


Figure 1.6: Scattering in mechanisms with HfO_2 – Mechanisms dominant at different fields [35].

Scattering mechanisms and their mitigation are some of the issues addressed in the following chapters. Andy kerber et al [38] and Chadwin young [39] showed that the effect of charge trapping on "apparent" mobility degradation could be eliminated by performing fast I_d-V_g measurement in the microsecond regime, thereby eliminating the trapping of electrons, which trap on the order of a 100 μsec. Figure 1.7 shows the fast I_d-V_g curves that Young et al [39] performed.

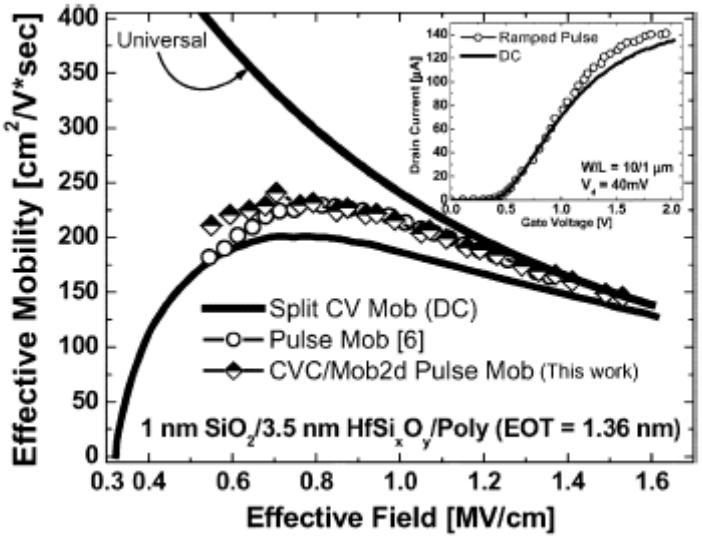


Figure 1.7: Pulsed Id-Vg vs. DC Id-Vg – Increased drain current in fast Id-Vg [39].

1.4.2 Charge Trapping in high-κ gate stacks

In the previous section, we briefly touched upon the effect of charge traps on mobility. The high trap density in high-κ dielectrics has the effect of significant threshold voltage instability as well. The trapping of electrons into charge traps at low voltages (<2V) has the consequence of shifting the threshold voltage in nMOSFETs. This shift in threshold voltage is unique to high-κ dielectric gate stacks and has been reported to be > 50mV [40-42]. Figure 1.8 shows the V_{TH} shift with time reported by Shanware et al [42].

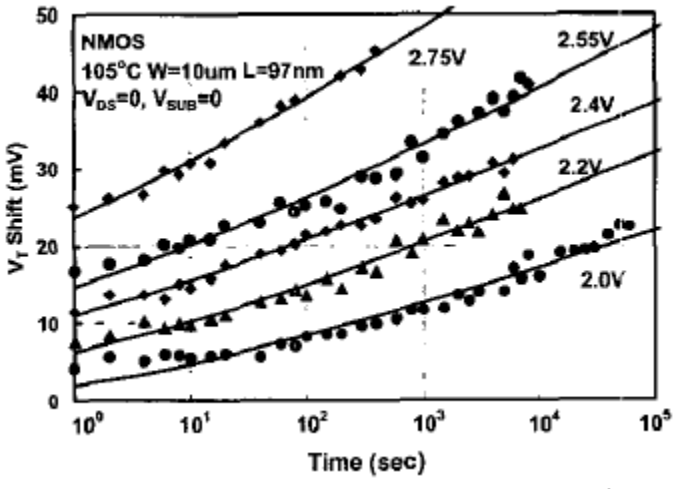


Figure 1.8: V_{TH} in HfSiON gate stacks [42]

There have been various reports speculating that the high-κ charge traps are neutral or positively charged oxygen vacancies and are intrinsic to the high-κ dielectrics [43, 44]. It was also reported that it is possible to "passivate" such oxygen vacancies by introducing nitrogen into the gate stacks, by various techniques [43].

The metal gate electrode also has a profound effect the charge trapping dynamics of the gate stack [45]. Solving the problem of threshold voltage instability in high-κ gate stacks is of paramount importance, as circuits are designed with threshold voltage error specifications < 10mV.

1.4.3 Negative Bias Temperature Instability

Negative Bias Temperature Instability or NBTI in pMOSFETs is a controversial topic in SiO_2/Poly-Si, spawning a decade of research and many viable, yet unprovable theories. Hydrogen-Reaction-Diffusion or H°-R-D is the most popular theory offered in the literature. In H°-R-D, negative threshold voltage shift is reported to be due to the

creation of interface traps by the breakage of hydrogen bonds, caused by hole trapping during negative biased stress and the subsequent diffusion of hydrogen through the dielectric [46].

NBTI in hafnium based high-κ gate stacks is complicated by the presence of various types of charge traps, which trap and detrap under electrical stress. R. Harris et al [47] reported that the presence of the charge traps renders the effect of H°-R-D negligible in these gate stacks and the threshold voltage shift is largely due to electron detrapping from existing trap sites.

1.4.4 Breakdown and Stress Induced Leakage Current

Time Dependent Dielectric Breakdown (TDDB) and its indicative precursor Stress Induced Leakage Current (SILC) have been reported to be mechanisms of failure in SiO_2 gate stacks. The catastrophic failure of the dielectric leads to large increases in leakage current through the dielectric, reducing the inversion charge significantly [5]. This reduction in inversion charge leads to drain current loss, which causes the circuit to fail. The operating voltage for ten years of device operation in HfO_2 has been reported by several groups to be within the voltage scaling limits [48, 49] . However, the TDDB studies are complicated by

a) Charge trapping – Electron trapping reduces the leakage current in the initial stages of stress.
b) Soft Breakdown or Progressive Breakdown [50, 51]: Progressive breakdown is the wearout of the dielectric during stress, resulting in slow increase in current – This is typically seen in thin dielectrics (EOT <10Å).

c) Polarity dependence: The breakdown in high-κ dielectrics is heavily polarity dependent and is not easily modeled and no consensus has been reached on the exact mechanism of breakdown in the dielectric.

Stress induced leakage current increase or SILC is another important phenomenon that is often considered a pre-cursor to breakdown. SILC is conventionally thought to occur due to stress-generated traps that increase the leakage current [4]. The high trap density in high-κ gate stacks also complicates the issues associated with stress induced leakage current.

1.5 Outline

This dissertation deals primarily with the said reliability issues, the mechanism, physical modeling and possible resolutions.

Chapter 2 deals with Stress Induced Leakage Current (SILC) in HfO_2 with TiN gate electrode. After a brief description of the sample fabrication and stress methodology, the influence of high trap density in the dielectric on SILC and threshold voltage instability is discussed, with particular emphasis on pre-existing defects and stress generated defects.

Chapter 3 discusses the mobility degradation mechanisms in high-κ gate stacks. Mobility dependence on the thickness of the interfacial layer is investigated, after an introduction to previous methodologies employed in discussion of mobility degradation. The effect of coulombic, phonon and remote phonon scattering are investigated in detail.

The thickness dependence of the high-k layer on carrier mobility and threshold voltage instability is reported in chapter 4. It is shown that threshold voltage instability

can be mitigated by reducing the thickness of the high-κ layer to < 2.0 nm. A possible correlation between the morphology of the dielectric and threshold voltage instability is also discussed. A new mathematical model is proposed for threshold voltage instability in high-κ gate stacks.

Negative Bias Temperature Instability in ultra-thin high-κ gate stacks is investigated in chapter 5. From an examination of the evolution of the power law exponent "n" with the thickness of the dielectric layer, NBTI is concluded to be a combination of charge trapping and Hydorgen-Reaction-Diffusion model. The activation energy for trap creation and the degradation of peak transconductance are also examined.

Chapter 6 discusses the influence of the presence of nitrogen in high-κ dielectrics on threshold voltage instability in nMOSFETs and pMOSFETs. Nitrogen incorporated through plasma nitridation technique is shown to reduce charge trapping in thick dielectrics, while thin dielectrics are insensitive to the presence of nitrogen in the film. A comparison of different nitridation techniques with respect to threshold voltage instability, EOT and mobility is presented.

In chapter 7, all the reliability characteristics and dielectric properties in high-κ gate stacks reported in this dissertation are summarized. Some relevant outstanding issues and suggestions for future research are also presented.

1.6 References

1. **Internation Technology Roadmap for Semiconductors**
2. Intel: **Craig Barret's Keynote speech on IDF**. In: *wwwanandtechcom.* 2005.
3. Wolf S: **Silicon Processing for the VLSI era**, vol. 2: Lattice Press; 1990.
4. Hori T: **Gate Dielectrics and MOS ULSIs**. Berlin: Springer-Verlag 1997.
5. B. Streetman SB: **Solid State Electronic Devices**: Prentice Hall; 2001.
6. **Technology Scaling**
7. A. Chandrakasan WB, and F. Fox: **Design of High-Performance Microprocessor Circuits**: IEEE press; 2001.
8. N.S. Kim TA, D. Blaauw, T. Mudge, K. Flautner, J.S. Hu, M.J. Irwin, M. Kandemir, and V. Narayanan: **Leakage Current: Moore's law meets static power**. *computer* 2003, **36**(12).
9. S.-H. Lo DAB, Y. Taur, and W. Wang: **Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thinoxide nMOSFET's**. *IEEE Trans Electron Devices* 1997, **18**:209-211.
10. DiMaria JHSaDJ: **Reliability projection for ultra-thin oxides at low voltage**. *IEDM Tech Dig* 1998:167-170.
11. T.-S. Chen DH, V. Valu, V. Jiang, S.-H. Kuah, P. C. McIntyre, S. R., Summerfelt JMA, and J. C. Lee: **Ir-electroded BST thin film capacitors for 1 giga-bit DRAM application**. *IEDM Tech Dig* 1996:797-800.

12. Robertson J: **Band offsets of wide-band-gap oxides and implications for future electronic devices**. *Journal of Vaccuum Society B* 2000, **18**:1785.

13. Scott JF: **High-Dielectric Constant Thin Films for Dynamic Random Access Memories**. *Annual Review of Materials Science* 1998.

14. D. Park Y-CK, Q. Lu, T.-J. King, C. Hu, A. Kalnitsky, S.-P. Tay, and, Cheng C-C: **Transistor characteristics with Ta2O5 gate dielectric**. *IEEE Electron Device Lett* 1998, **19**:441-443.

15. M. Saito MY, K. Asaka, H. Goto, N. Fukuda, M. Kawano, M. Kojima, M. Suzuki, K. Ogaya, H. Enomoto, K. Hotta, S. Sakai, H. Asakura,, T. Fukuda TS, T. Takakura, and N. Kobayashi: **Advanced thermally stable silicide S/D electrodes for high-speed logic circuits with large-scale embedded Ta2O5-capacitor DRAMs**. *IEDM Tech Dig* 1999:805-808.

16. P. K. Roy and I. C. Kizilyalli: **Stacked high-ε gate dielectric for gigascale integration of metal–oxide–semiconductor technologies**. *Appl Phys Lett* 1998, **72**:2835-2837.

17. Campbell SA, Gilmer DC, Xiao-Chuan W, Ming-Ta H, Hyeon-Seag K, Gladfelter WL, Jinhua Y: **MOSFET transistors fabricated with high permitivity TiO₂ dielectrics**. *Electron Devices, IEEE Transactions on* 1997, **44**(1):104-109.

18. Lee BH: **Technology Development and process integration of alternative gate dielectric material; Hafnium Oxide**. *Dissertation.* Austin: The University of Texas; 2001.

19. Qi W-J: **Study on high-k dielectrics as alternative gate insulators for 0.1 micron and beyond ULSI applications**. Austin: The University of Texas; 2000.
20. Onishi K, Chang Seok K, Rino C, Hag-Ju C, Gopalan S, Nieh R, Krishnan S, Lee JC: **Effects of high-temperature forming gas anneal on HfO/sub 2/ MOSFET performance**. In: *VLSI Symposium: 2002*; 2002: 22-23.
21. Rino C, Onishi K, Chang Scok K, Renee N, Gopalan S, Hag-Ju C, Krishnan S, Lee JC: **High quality MOSFETs fabrication with HfO/sub 2/ gate dielectric and tan gate electrode**. In: *Device Research Conference, 2002 60th DRC Conference Digest: 2002*: IEEE; 2002: 193-194.
22. Nieh R, Krishnan S, Hag-Ju C, Chang Seok K, Gopalan S, Onishi K, Choi R, Lee JC: **Comparison between ultra-thin ZrO/sub 2/ and ZrO/sub x/N/sub y/ gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices**. In: *VLSI Symposium: 2002*; 2002: 186-187.
23. Wong CY, Sun JY, Taur Y, Oh CS, Angelucci R, Davari B: **Doping of n⁺ and p⁺ polysilicon in a dual-gate CMOS process**. In: *Electron Devices Meeting, 1988 Technical Digest, International 1988*; 1988: 238-241.
24. Onishi K, Kang L, Choi R, Dharmarajan E, Gopalan S, Yongjoo J, Chang Seok K, Byoung Hun L, Nieh R, Lee JC: **Dopant penetration effects on polysilicon gate HfO₂ MOSFET's**. In: *VLSI Technology, 2001 Digest of Technical Papers 2001 Symposium on 2001*; 2001: 131-132.
25. Ching-Huang L, Wong GMT, Deal MD, Tsai W, Majhi P, Chi On C, Visokay MR, Chambers JJ, Colombo L, Clemens BM *et al*: **Characteristics and mechanism of**

tunable work function gate electrodes using a bilayer metal structure on SiO/sub 2/ and HfO/sub 2. *Electron Device Letters, IEEE* 2005, **26**(7):445-447.

26. Narayanan V, Callegari A, McFeely FR, Nakamura K, Jamison P, Zafar S, Cartier E, Steegen A, Ku V, Nguyen P *et al*: **Dual work function metal gate CMOS using CVD metal electrodes**. In: *VLSI Technology, 2004 Digest of Technical Papers 2004 Symposium on 2004*: IEEE; 2004: 192-193.
27. Majhi P, Young C, Bersuker G, Wen HC, Brown GA, Foran B, Choi R, Zeitzoff PM, Huff HR: **Influence of metal gate materials and processing on planar CMOS device characteristics with high-k gate dielectrics**. In: *Solid-State Device Research conference, 2004 ESSDERC 2004 Proceeding of the 34th European: 2004*; 2004: 185-188.
28. Qiang L, Lin R, Ranade P, Tsu-Jae K, Chenming H: **Metal gate work function adjustment for future CMOS technology**. In: *VLSI Technology, 2001 Digest of Technical Papers 2001 Symposium on 2001*; 2001: 45-46.
29. Kang JF, Yu HY, Ren C, Wang XP, Li MF, Chan DSH, Liu XY, Han RQ, Wang YY, Kwong DL: **Characteristics of sub-1 nm CVD HfO/sub 2/ gate dielectrics with HfN electrodes for advanced CMOS applications**. In: *Solid-State and Integrated Circuits Technology, 2004 Proceedings 7th International Conference on 2004*; 2004: 393-398 vol.391.
30. Chang Seo P, Byung Jin C, Dim-Lee K: **Thermally stable fully silicided Hf-silicide metal-gate electrode**. *Electron Device Letters, IEEE* 2004, **25**(6):372-374.

31. Schaeffer JK, Capasso C, Fonseca LRC, Samavedam S, Gilmer DC, Liang Y, Kalpat S, Adetutu B, Tseng HH, Shiho Y *et al*: **Challenges for the integration of metal gate electrodes**. In: *Electron Devices Meeting, 2004 IEDM Technical Digest IEEE International 2004*; 2004: 287-290.
32. Samavedam SB, La LB, Smith J, Dakshina-Murthy S, Luckowski E, Schaeffer J, Zavala M, Martin R, Dhandapani V, Triyoso D *et al*: **Dual-metal gate CMOS with HfO/sub 2/ gate dielectric**. In: *Electron Devices Meeting, 2002 IEDM '02 Digest International 2002*; 2002: 433-436.
33. Hong-Jyh L, Gardner MI: **Dual high-/spl kappa/ gate dielectric with poly gate electrode: HfSiON on nMOS and Al/sub 2/O/sub 3/ capping layer on pMOS**. *Electron Device Letters, IEEE* 2005, **26**(7):441-444.
34. Weber O, Andrieu F, Casse M, Ernst T, Mitard J, Ducroquet F, Damlencourt JF, Hartmann JM, Lafond D, Papon AM *et al*: **Experimental determination of mobility scattering mechanisms in Si/HfO/sub 2//TiN and SiGe:C/HfO/sub 2//TiN surface channel n- and p-MOSFETs**. In: *Electron Devices Meeting, 2004 IEDM Technical Digest IEEE International 2004*; 2004: 867-870.
35. Zhu WJ, Ma TP: **Temperature dependence of channel mobility in HfO/sub 2/-gated NMOSFETs**. *Electron Device Letters, IEEE* 2004, **25**(2):89-91.
36. Chau R, Datta S, Doczy M, Doyle B, Kavalieros J, Metz M: **High-/spl kappa//metal-gate stack and its MOSFET characteristics**. *Electron Device Letters, IEEE* 2004, **25**(6):408-410.

37. Ren Z, Fischetti MV, Gusev EP, Cartier EA, Chudzik M: **Inversion channel mobility in high-/spl kappa/ high performance MOSFETs**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International 2003*; 2003: 33.32.31-33.32.34.

38. Kerber A, Cartier E, Ragnarsson LA, Rosmeulen M, Pantisano L, Degraeve R, Kim Y, Groeseneken G: **Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics**. In: *VLSI Technology, 2003 Digest of Technical Papers 2003 Symposium on 2003*; 2003: 159-160.

39. Young CD, Bersuker G, Brown GA, Lysaght P, Zeitzoff P, Murto RW, Huff HR: **Charge trapping and device performance degradation in MOCVD hafnium-based gate dielectric stack structures**. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 597-598.

40. Onishi K, Rino C, Chang Seok K, Hag-Ju C, Young Hee K, Nieh RE, Jeong H, Krishnan SA, Akbar MS, Lee JC: **Bias-temperature instabilities of polysilicon gate HfO/sub 2/ MOSFETs**. *Electron Devices, IEEE Transactions on* 2003, **50**(6):1517-1524.

41. Sa N, Kang JF, Yang H, Liu XY, He YD, Han RQ, Ren C, Yu HY, Chan DSH, Kwong DL: **Mechanism of positive-bias temperature instability in sub-1-nm TaN/HfN/HfO/sub 2/ gate stack with low preexisting traps**. *Electron Device Letters, IEEE* 2005, **26**(9):610-612.

42. Shanware A, Visokay MR, Chambers JJ, Rotondaro ALP, Bu H, Bevan MJ, Khamankar R, Aur S, Nicollian PE, McPherson J *et al*: **Evaluation of the positive**

biased temperature stress stability in HfSiON gate dielectrics. In: *Physics Symposium Proceedings, 2003 41st Annual 2003 IEEE International 2003*; 2003: 208-213.

43. J. L. Gavartin ALS, A. S. Foster and G. I. Bersuker: **The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies**. *JOURNAL OF APPLIED PHYSICS* 2005, **97**:13.
44. Nobuyuki Ikarashi MM, Koji Masuzaki, and Toru Tatsumi: **Electron energy-loss spectroscopy analysis of the electronic structureof nitrided Hf silicate films**. *APPLIED PHYSICS LETTERS* 2004, **84**(18).
45. Xuguang W, Peterson J, Majhi P, Gardner MI, Dim-Lee K: **Impacts of gate electrode materials on threshold voltage (V/sub th/) instability in nMOS HfO/sub 2/ gate stacks under DC and AC stressing**. *Electron Device Letters, IEEE* 2005, **26**(8):553-556.
46. Alam MA: **A critical examination of the mechanics of dynamic NBTI for PMOSFETs**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International 2003*; 2003: 14.14.11-14.14.14.
47. Harris HR, Choi R, Lee BH, Young CD, Sim JH, Mathews K, Zeitzoff P, Majhi P, Bersuker G: **Comparison of NMOS and PMOS stress for determining the source of NBTI TiN/HfSiON devices**. In: *Reliability Physics Symposium, 2005 Proceedings 43rd Annual 2005 IEEE International: 2005*; 2005: 80-83.

48. Sungjoo L, Kwong DL: **TDDB and polarity-dependent reliability of high-quality, ultrathin CVD HfO/sub 2/ gate stack with TaN gate electrode**. *Electron Device Letters, IEEE* 2004, **25**(1):13-15.

49. Young Hee K, Onishi K, Chang Seok K, Hag-Ju C, Rino C, Krishnan S, Akbar MS, Lee JC: **Thickness dependence of Weibull slopes of HfO/sub 2/ gate dielectrics**. *Electron Device Letters, IEEE* 2003, **24**(1):40-42.

50. Kauerauf T, Degraeve R, Zahid MB, Cho M, Kaczer B, Roussel P, Groeseneken G, Maes H, De Gendt S: **Abrupt breakdown in dielectric/metal gate stacks: a potential reliability limitation?** *Electron Device Letters, IEEE* 2005, **26**(10):773-775.

51. Young Hee K, Onishi K, Chang Seok K, Hag-Ju C, Nieh R, Gopalan S, Choi R, Jeong H, Krishnan S, Lee JC: **Area dependence of TDDB characteristics for HfO/sub 2/ gate dielectrics**. *Electron Device Letters, IEEE* 2002, **23**(10):594-596.

Chapter 2

Stress Induced Leakage current

2.1 Introduction

Stress Induced Leakage current (SILC) is a precursor to hard breakdown in SiO_2 dielectrics. The leakage current increases due to the gradual creation of new defect centers, which provide leakage paths for the electrons. Breakdown occurs when a set of newly created defect centers line up, leading to catastrophic leakage increase (Percolation Path theory). Although several studies have focused on this issue [1, 2], the extent of stress-induced degradation in Hi-K dielectrics is still not clear. In traditional SiO_2/Poly-Si gate stacks, almost all oxide degradation is attributed to trap generation leading to percolation model type failure, while pre-existing defects are believed to contribute to extrinsic mode failure [3]. For the HfO_2/TiN gate stack, it has been reported that a similar mechanism was at work[1]. In this study, we have investigated SILC characteristics of HfO_2 / TiN gate nMOS and pMOS transistors in conjunction with the trapping/de-trapping processes in the high-k dielectric.

2.2 Experiment

2.2.1 Device Fabrication

The process flow of 70nm TiN gate MOSFET devices fabrication is shown in Table 2.1. The experimental devices consist of T_{phy}=3.0nm HfO_2. On the HF cleaned 200 mm wafer, a thin high quality SiO_2 layer of 10Å is grown using an O_3 (Ozone)

oxidant [8]. The ALD HfO_2 is then deposited using $HfCl_4$ precursor and O_3 oxidant. In this flow, HfO_2 layer is removed after gate patterning with minimal damage in the extension region. A thin nitride layer is then deposited to protect the HfO_2 layer. LDD and Halo implants were implanted through this thin nitride layer. LDD and halo are optimized to ensure a proper overlap of LDD and control of short channel behavior. TiN/HfO_2 showed an EOT of 14.4Å (without quantum mechanical effect deduction) excellent wafer uniformity, both in threshold voltage and leakage current.

- HF cleaning
- O_3 SiO_2 Interface (10Å)
- ALD HfO_2 30Å deposition
- PDA (700ºC, 1min in NH3 ambient)
- TiN / Polysilicon 1500 Å deposition
- Gate predoping
- N LDD/halo
- Nitride spacer (90nm)
- N SD (Source and Drain)
- SD RTA (1000ºC, 5sec)
- Metallization
- Forming Gas anneal (480ºC, 30min)

Table 2.1: Process Flow of 70nm O3/HfO2/TiN gate stack [8].

2.2.2 Stress Set-up

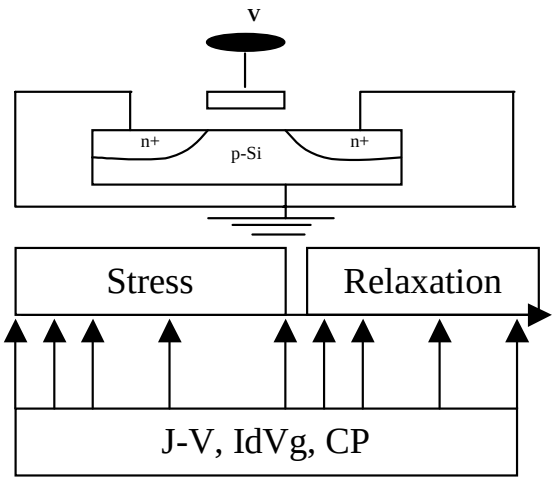


Figure 2.1: SILC Stress setup

The devices used in this setup were 10x1 μm (10^{-7} cm^2) and 10x0.5 μm ($5x10^{-8}$ cm^2) nMOS and pMOS transistors. The EOT of the fabricated gate stack was 14.4 Å, with excellent across-the-wafer uniformity. The measurement setup is shown in fig. 2.1. For inversion SILC (positive gate bias in NMOS) study, the leakage current characteristics (J-V) were measured on fresh devices (Vg sweep from 0 to 1.75V), with the source, drain and substrate grounded. On the same device, the I_d-V_g characteristics were then measured, with V_d = 50 mV. Then the gate was stressed at various voltages (2.0 V, 2.4V, 2.6V and 2.8V) for 1000 sec (with source, drain and substrate grounded) and the stress was interrupted at various intervals for J-V and Id-Vg measurements. Once the stress cycle was complete, a gate stress of the opposite polarity and various magnitudes (0V, -1V, -2V and -2.6V) was applied for 1000 sec, interrupted for J-V and Id-Vg

measurements. A similar methodology was used for negative gate stress on nMOS, and negative and positive gate stress on pMOS, as well.

2.3 Results and Discussion

2.3.1 nMOS:

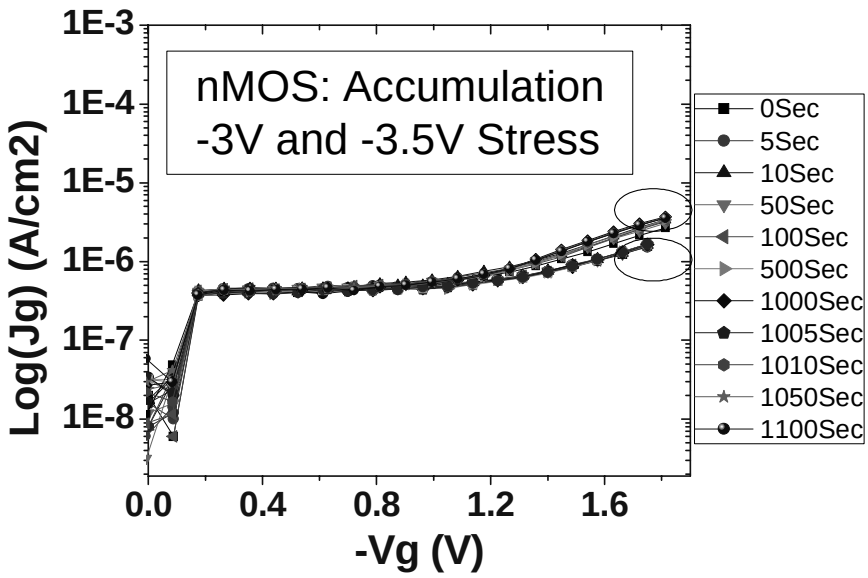


Figure 2.2: SILC under accumulation stress in nMOS - Accumulation Stress of -3V and –3.5V show no increase in leakage current till 1100 seconds

Accumulation and Inversion SILC was investigated in nMOS transistors For this study, 10x1um transistors (1e-7 cm^2) and 10x0.5um (5e-8 cm^2) transistors were used. In all devices tested under negative gate bias conditions (Accumulation), there was almost no detectable SILC observed (fig. 2.2): therefore, this study focussed on the effects of substrate injection stress.

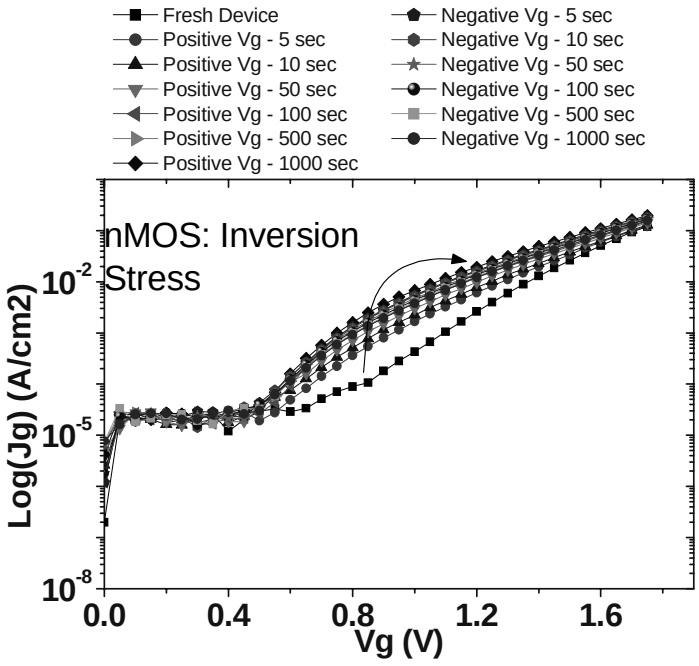


Figure 2.3 (a): SILC in nMOS under Inversion Stress – For a 2.6V stress voltage and 0V relaxation bias, SILC is reversible.

The nMOSFETs were then stressed under substrate bias condition, in order to quantify the SILC under inversion stress of various magnitudes. During the substrate injection stress, both leakage current and threshold voltage increased, while the subthreshold swing remained constant. During the negative bias portion of the stress cycle, however, the leakage current decreased significantly (even for 0V relaxation stress – fig. 2.3 (a)), indicating that SILC increase is not exclusively due to irreversible trap generation.

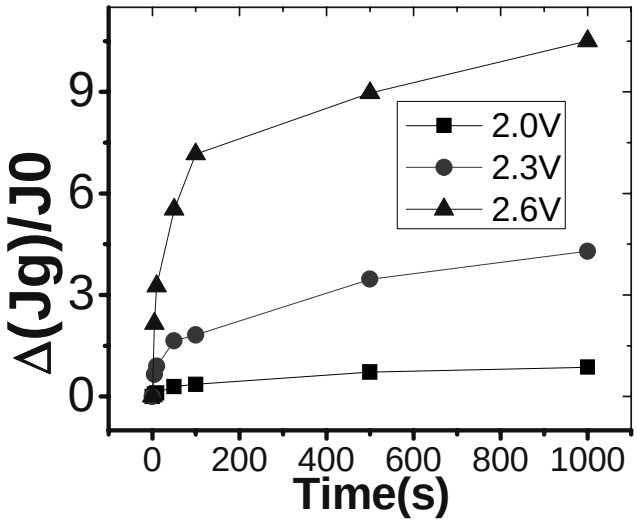


Figure 2.3 (b): SILC at different stress voltages

The magnitude of the increase in leakage current increases with increase in stress voltage, as we would expect (Figure 2.3 (b)). As the negative or recovery bias is increased, the amount of leakage current recovered increased significantly. Indeed, at a recovery bias of -1.5V, nearly all of the leakage current is recovered (figure 2.4).

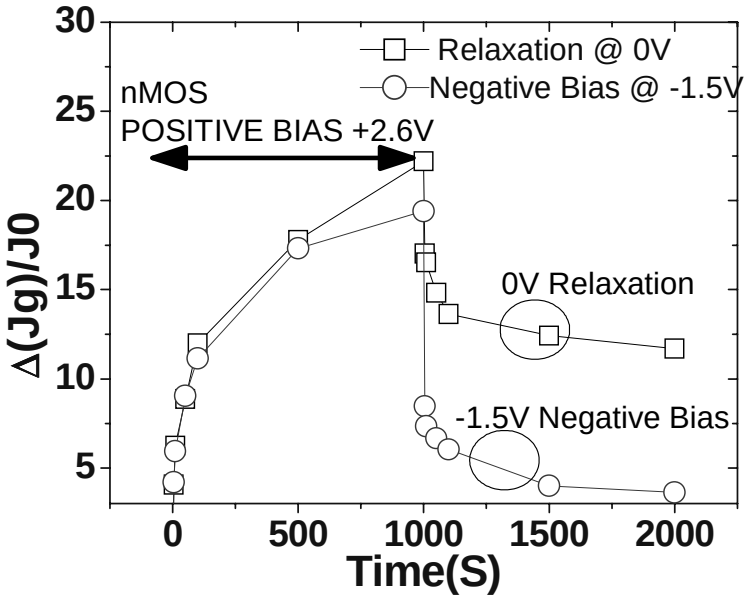


Figure 2.4: nMOS: The amount of recovered leakage current increased with magnitude of negative bias.

Such SILC reduction was accompanied by the almost complete recovery of the transistor threshold voltage. This recovery in SILC in conjunction with threshold voltage recovery indicates that the mechanism for the two phenomena might be similar. The subthreshold swing remained constant during the stressing cycle (fig. 2.5). The subthreshold swing is an indicator of interface trap density.

$S \cong kT/q\ (\ln 10)(1+C_D/C_i)$ …….Equation 2.1

where C_D is the depletion capacitance and can be expressed as $C_{D,\ ideal} + qD_{it}$, where $C_{D,\ ideal}$ is the depletion capacitance with no interface traps and D_{it} is the interface trap density[4]. As expressed earlier, during inversion stress, the subthreshold swing does not

change, indicating that the interface trap density remains constant, which we would expect in the case of electron trapping. We therefore rule out hole trapping and the corresponding interface bond breakage as possible mechanisms under inversion stress conditions.

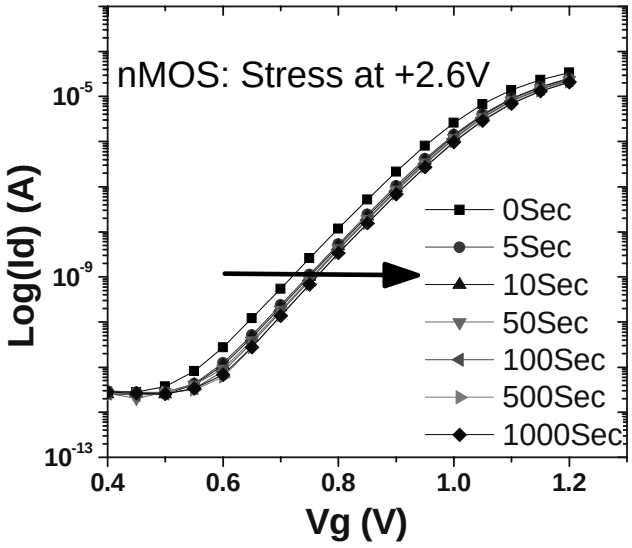


Figure 2.5: No Subthreshold Swing degradation is seen for a stress of 2.6V done for 1000 Sec.

That the subthreshold swing remains constant is not indicative of trap generation free stress. Trap generation could occur in other parts of the dielectric. In order to quantify the trap generation, charge pumping measurements were done before and after the stress at three frequencies (10KHz, 100KHz and 1MHz). Stress-induced N_{it} increase is greater at 10 KHz than at 1MHz (fig. 2.6), indicating significant trap generation away

from the gate stack interface with the substrate, which is consistent with the unchanged sub-threshold swing [5]. Charge trapping has been described to be a transient process in high-κ gate stacks, wherein, electrons from the inversion layer are trapped into charge centers in the bulk of the high-κ dielectric, in the μsec time range [6]. This leads to a loss in the drain current. In addition, the carrier mobility in the channel, which is generally extracted from the DC drain current – gate voltage measurement (I_d-V_g) appears to diminish due to this charge trapping phenomenon, because of the drain current loss. In order to address this issue, kerber et al [6] suggested that the Id-Vg characteristics be collected during the rise time (~5 μsec) of a fast single pulse (100 μsec). The rise time is fast enough that the Id-Vg characteristics are devoid of any inversion charge loss and the drain current loss during the 100 μsec pulse width is indicative of the bulk trap density in the high-κ dielectric. Single pulse Id-Vg measurements in the μsec range, in the gate stacks under study, do not show any trap generation (fig. 2.7). This suggests that the generated defects affecting CP measurements may be located near the high-k/SiO2 interface and not in the bulk high-K film.

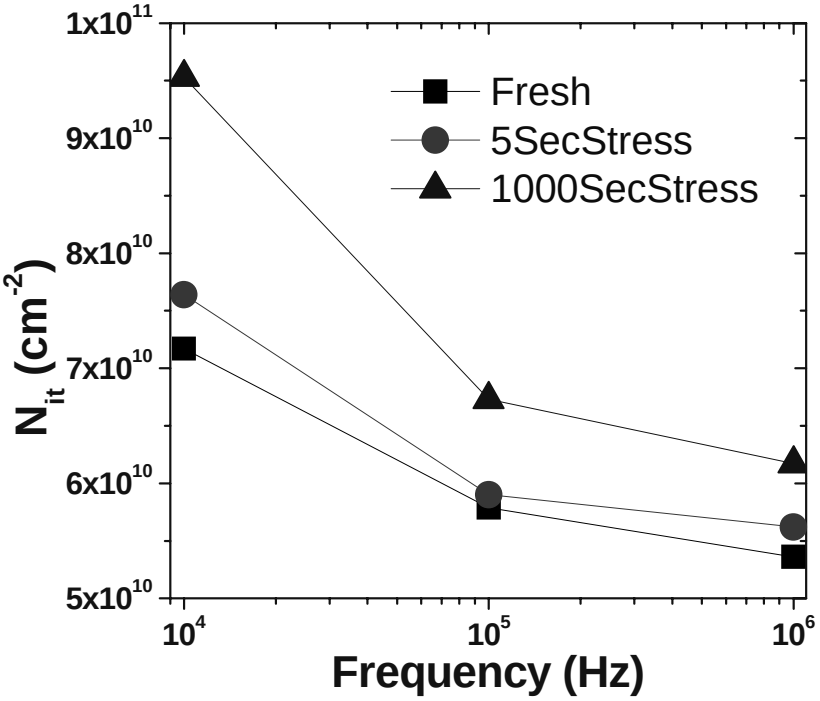


Figure 2.6: Charge pumping vs. frequency: Lower frequencies show higher increase in N_{it} after stress indicating trap generation away from the interface, but within the interface layer (~10 Å from interface)

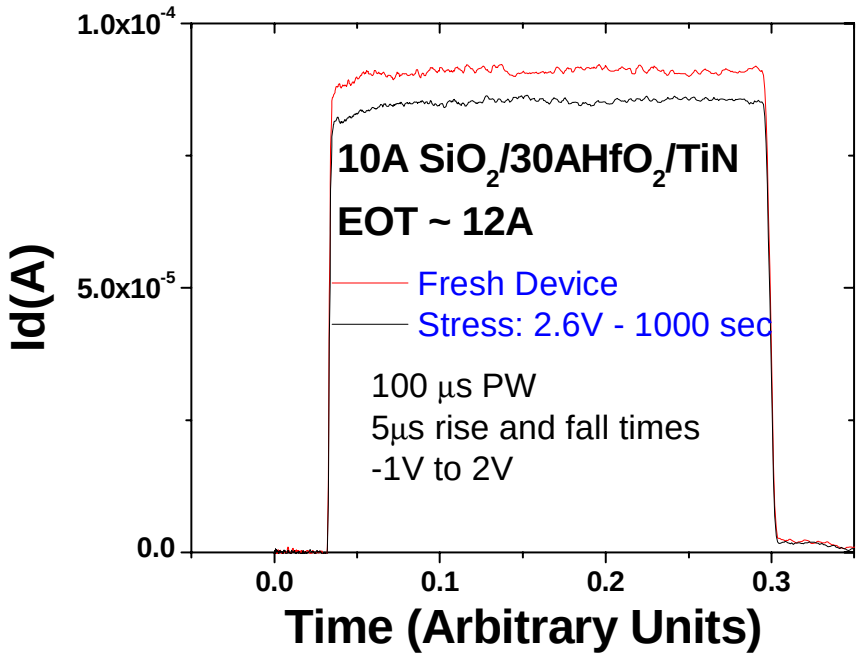


Figure 2.7: Single Pulse Id-Vg shows no change after a 1000sec stress, indicating minimal bulk trap creation.

The band diagrams for nMOSFET transistors are drawn to scale in fig. 2.8 (using an estimated dielectric constant of 18 for HfO_2). Since there is no interface degradation, we ruled out contribution from hole injection and assume that the observed parameter changes occur primarily due to electron injection. For a +2.6V stress (fig. 2.8), electron injection occurs near the high-k conduction band edge; electron trapping near the high K/ SiO_2 interface causes the threshold voltage to increase while causing non-uniformity of the electric field across the HfO_2 layer and corresponding distortion of the conduction band bending. However, when the stress is removed, the trapped electrons start to de-trap

under the built-in electric field, under no external bias. The SILC characteristics are measured from 0 to 1.5V, during which time, de-trapping continues to occur, leading to increase in leakage current. The increase is more evident in the lower voltages when the current due to the de-trapping is comparable to the leakage current from the inversion layer. In summary, the leakage current measured during the J-V measurement is due to two sources:

a) The inversion charge leakage through the oxide due to tunneling from the substrate [7].

b) The trapped charge de-trapping – At low voltages this is comparable to the leakage current from the inversion charge, as the inversion layer has not yet formed. At high voltages, the inversion layer leakage is much higher and therefore the effect is not evident.

At higher voltages (~1.5V), the leakage current from the inversion layer dominates and the increase due to the detrapping is not so evident. During the negative bias portion of the stress cycle, the electrons are de-trapped quickly and the J-V characteristics are reduced to their original levels.

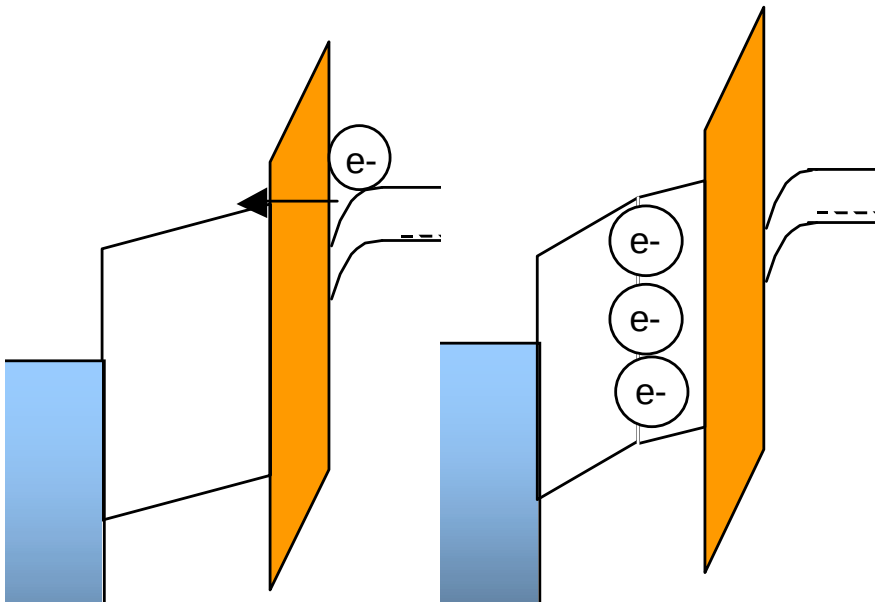


Figure 2.8: a) Schematic of the energy band diagram (in scale) for 2.6V stress before and b) After electron trapping.

Alternatively stressing the sample with positive and negative biases for several cycles shows that the threshold voltage is entirely recovered at the end of every relaxation cycle (with no interface degradation), pointing to complete electron de-trapping while the leakage current shows “permanent” degradation after the first stress cycle, which probably indicates defect generation in or near the interfacial sub-oxide layer (fig. 2.9 & 2.10). This degradation, however, seems to saturate after the first stress cycle, indicating that permanent trap generation happens in the initial stages of the stress and gradually reduces.

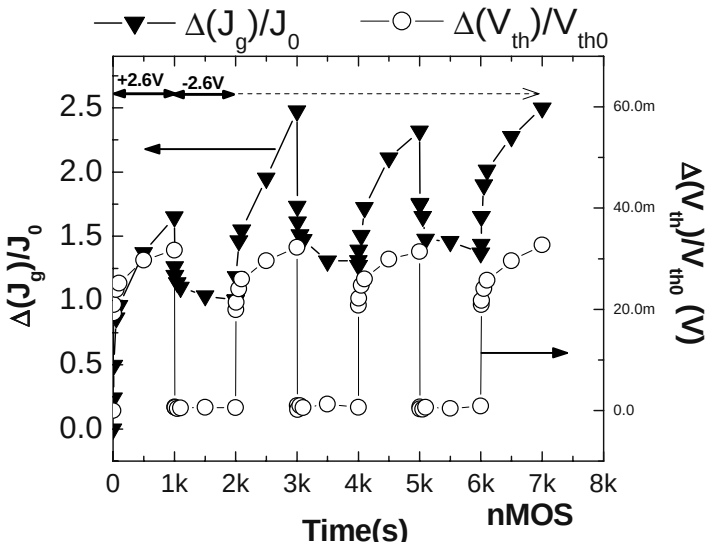


Figure 2.9: When alternatively stressed between positive and negative biases, leakage current seems to saturate

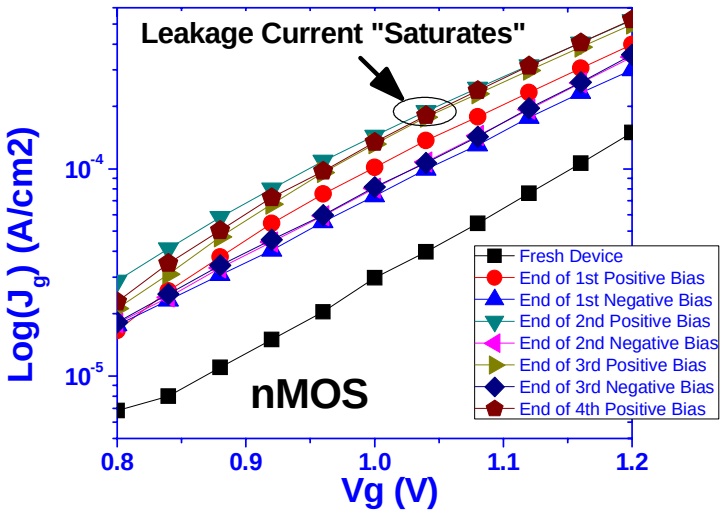


Figure 2.10: Saturation of Leakage Current after the first cycle of stress, indicating damage in the first cycle.

2.3.2 pMOS:

The SILC behavior during the negative bias stress is similar to negative bias stress in nMOS transistors. There is no detectable SILC until breakdown (fig. 2.11). This indicates that SILC in nMOS or pMOS is due to the same phenomenon, electron trapping and detrapping.

Effects of the positive bias stress are similar to the nMOS transistor - partially recoverable "low voltage" SILC is observed (fig. 2.12). Fig. 2.13 shows the band diagrams for pMOS.

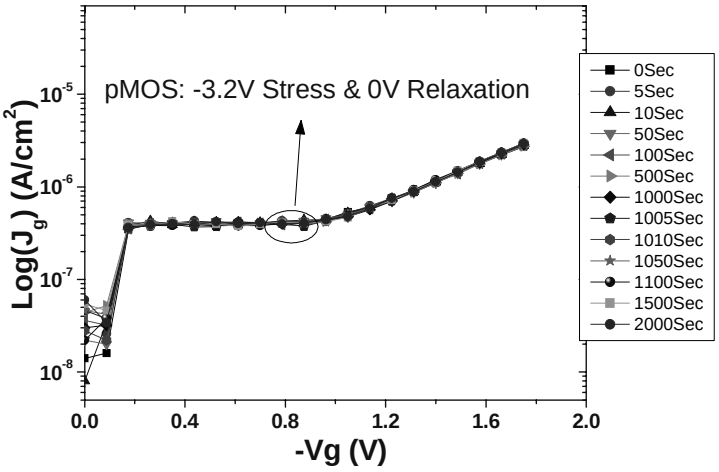


Figure 2.11: pMOS in Inversion (Negative Bias).

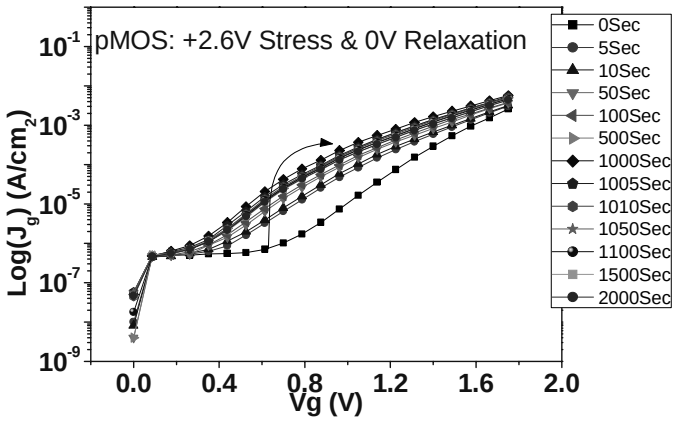


Figure 2.12: pMOS in Accumulation (Positive Bias).

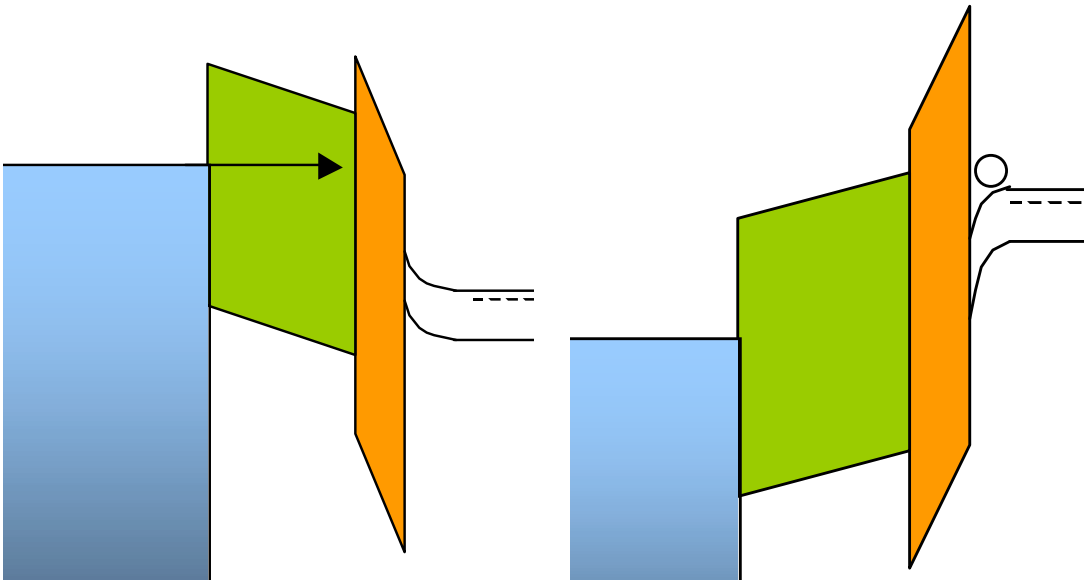


Figure 2.13: Band diagram for a) pMOS in accumulation at 2.6V b) pMOS in Inversion (-2.6V)

2.4 Conclusions

SILC behavior in 1.0 nm SiO_2/3.0 nm HfO_2/TiN nMOS and pMOS transistors was investigated. SILC dependence on stress time and polarity was found to closely correlate to the one of the threshold voltage in both nMOS and pMOS transistors. This suggests that the stress-induced reversible changes in both parameters are mostly determined by the same mechanism - reversible electron trapping in pre-existing defects. Small amount of traps are believed to be generated within or near the interfacial sub-oxide layer during the initial stages of stressing. Since electron trapping is much more efficient under the substrate injection stress, NMOS devices are expected to exhibit greater SILC degradation at normal operating conditions. However, most of this leakage current increase is due to trapping in charge traps in the bulk of the dielectric and as such, cannot be taken to indicate degradation of the film.

2.5 References:

1. Crupi F, Degraeve R, Kerber A, Kwak DH, Groeseneken G: **Correlation between Stress-Induced Leakage Current (SILC) and the HfO/sub 2/ bulk trap density in a SiO/sub 2//HfO/sub 2/ stack**. In: *Reliability Physics Symposium, 2004 Proceedings 42nd Annual 2004 IEEE International 2004*; 2004: 181-187.
2. Garros X, Leroux C, Reinibold G, Mitard J, Guillaumot B, Martin F, Autran JL: **Reliability assessment of ultra-thin HfO/sub 2/ oxides with TiN gate and polysilicon-n/sup +/ gate**. In*: 2004*; 2004: 176-180.
3. Ernest W. Yu JS: **Ultra-Thin Oxide Reliability**. In: *Reliability Physics Symposium, 2005 Proceedings 43rd Annual 2005 IEEE International* San Jose, Ca: IEEE; 2005.
4. Sze SM: **physics of semiconductor devices**, 2 edn. New Jersey: John Wiley and sonds; 1999.
5. Young CD, Bersuker G, Brown GA, Lysaght P, Zeitzoff P, Murto RW, Huff HR: **Charge trapping and device performance degradation in MOCVD hafnium-based gate dielectric stack structures**. In*: 2004*; 2004: 597-598.
6. Kerber A, Cartier E, Ragnarsson LA, Rosmeulen M, Pantisano L, Degraeve R, Kim Y, Groeseneken G: **Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics**. In*: 2003*; 2003: 159-160.
7. Mizubayashi W, Yasuda N, Ota H, Hisamatsu H, Tominaga K, Iwamoto K, Yamamoto K, Horikawa T, Nabatame T, Toriumi A: **Carrier separation analysis for clarifying leakage mechanism in unstressed and stressed HfAlO/sub x//SiO/sub 2/**

stack dielectric layers. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 188-193.

8. Jeff J. Peterson et al, **The Role of Interfacial Oxides in Mobility Improvement in HfO_2 Gate Stacks**. In: *Semiconductor Interface Specialists Conference, 2004, 35th Annual 2004 IEEE International: 2004.*

Chapter 3

Mobility Issues in High-κ Dielectrics

3.1 Introduction

Mobility degradation in high κ gate stacks is a major concern. As the required EOT reaches sub-nm levels, the mobility is severely degraded to 50-60% of the universal mobility at room temperature. The presence of fixed charge in high-k dielectrics is known to have a negative effect on the mobility of high-k gate stacks through carrier scattering [1] . Additionally, charge trapping in the high-k dielectric has been shown to contribute to inversion charge loss in the channel, giving the appearance of mobility degradation[2]. Soft optical phonons were also suggested to contribute to mobility reduction in high-k gate stacks [3]. These mechanisms may be mitigated through the introduction of a bottom interfacial screening oxide between the high-k gate dielectric and the transistor channel[4]. In relation to the fixed high-k charge, the screening oxide increases the distance between the fixed charge in the high-k dielectric and the carriers, thereby reducing the scattering effect of the fixed charge [4]. In the case of soft optical phonons, the screening oxide acts as a barrier to dampen the phonon penetration and likewise reduce their scattering effect. On the other hand, it was shown that the properties of the interfacial oxide layer, in particular its oxygen content, might have significant impact on carrier mobility. Although high-k deposition on top of the oxide layer results in increase of its k-value, the screening oxide still constitutes a significant portion of the high-k gate stack equivalent oxide thickness (EOT). It is, therefore, critical to optimize thickness and quality of the screening oxide to achieve the required mobility.

3.2 Experiment and Results

3.2.1 Screening effect of Interfacial Oxides

This study used 30Å ALD-HfO_2 gate dielectric transistors and capacitor structures on 200 mm Si <100> wafers, fabricated using a standard CMOS process with 1000°C/10s dopant activation and TiN gate electrode (Table 1 shows the complete transistor process) [11]. In order to evaluate the oxide thickness screening effect on transistor mobility, several bottom interface oxides are compared: a 1 nm ozonated oxide, a 1.2 nm thermal oxide, and a 1.6 nm rapid thermal nitrided oxide. After completion of CMOS processing, standard C-V and I-V analysis was done to evaluate EOT, CET, Vfb, Jg, and Vt. Mobility was extracted using the mob2d methodology. The data demonstrates that both the peak and high-field mobilities are increased through the incorporation of thicker screening oxides (fig. 3.1). Fig 3.1 (right) shows the high field mobility improvement.

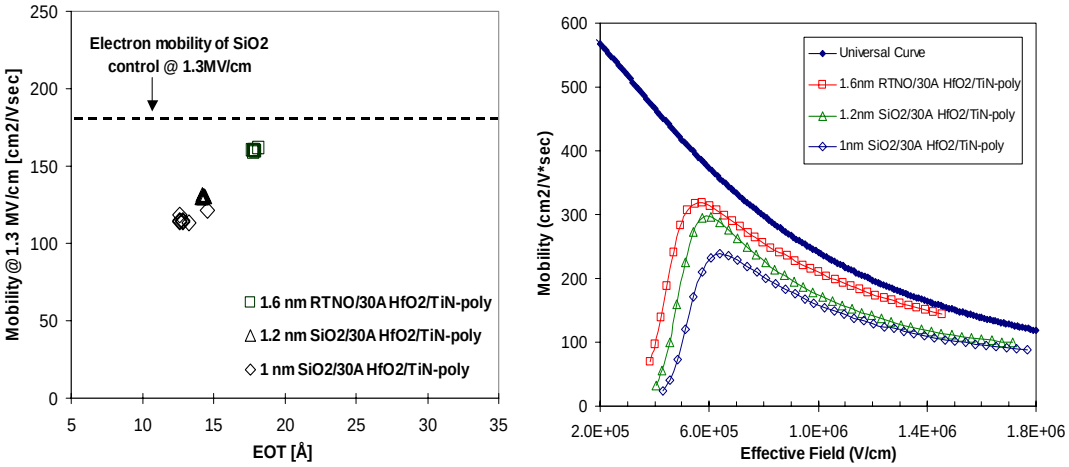


Figure 3.1: The Effective Mobility of electrons in nMOS transistors increase with thinner interfacial layers.

Fast transient single pulse Id-Vg measurements [5] were performed using a short voltage pulse at 2.5 V (from a minimum of –1 V), with a pulse width of 100 μs. The single pulse Id-Vg plots show absolutely no discrepancy from the DC Id-Vg plots, for all the three samples. This indicates that the screening effect of the oxide interfaces (1.0 nm, 1.2 nm and 1.6 nm) is sufficient to bring trapping down to a minimum (fig. 3.2). Charge pumping measurements, done at both 1 MHz and 100 KHz, show that N_{it} values decreased monotonically with the thickness of the interfacial oxide (fig. 3.3). This indicates that part of the mobility degradation comes from fixed charge in the interface layer. The fixed charge increase could be due to hafnium incorporation inside the interface layer. The hafnium incorporation inside a thin interface layer would be more than that in thick interface layers.

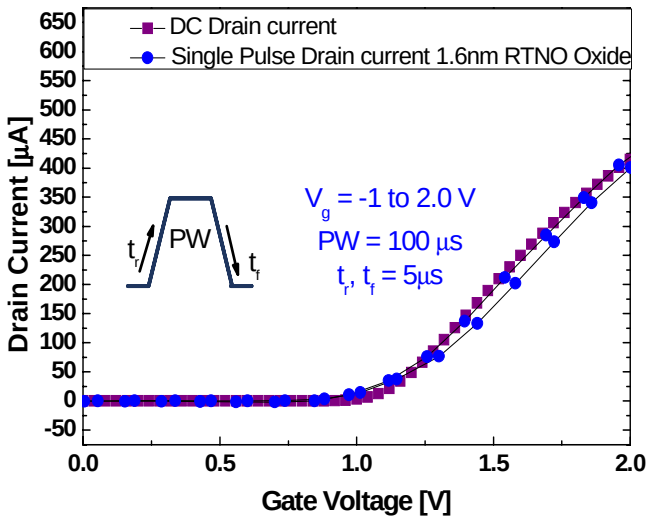


Figure 3.2: Single Pulse Drain current for the 1.6nm RTNO oxide lies exactly on top of DC Id-Vg

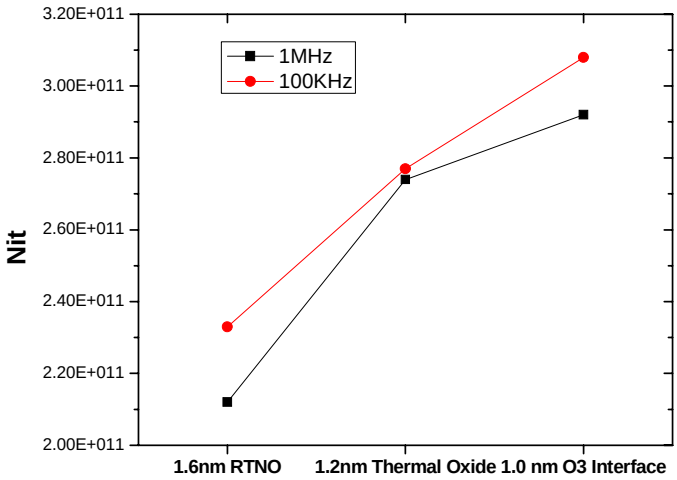


Figure 3.3: The Interface State density increases as the interface thickness grows thinner.

3.3 Interface Effect on Mobility

The screening effect of the interface thickness on mobility was investigated. It was shown that both high field and peak mobility progressively increase as we increase the thickness of the interface from 1.0nm to 1.6nm. Interface thickness of 1.6nm is enough to make the interface sufficiently like SiO_2, so that the high field mobility is the same as that of SiO_2 with TiN. The N_{it} values increase as the thickness of the interface is decreased. Charge trapping properties were investigated and it was found that DC Id-Vg curves coincide with the single-pulse Id-Vg curves, indicating that the charge trapping effect was minimized due to the presence of even a 10Å Interface.

3.4 Mobility Degradation Study

3.4.1 Mobility Vs Temperature: Effect of phonon Scattering

To qualitatively and quantitatively assess the degradation effects of the high K on the electron intrinsic mobility, electron mobility in nMOSFETs was measured as a function of temperature. There is no significant apparent mobility degradation in the samples due to charge trapping. Therefore, the DC mobility curves are used for the calculations (fig 3.2). Both peak mobility and high-field mobility (at 1MV/cm) decreased with temperature (fig 3.4). However, there were subtle differences in the high-field mobility-temperature relationships between the different interfaces.

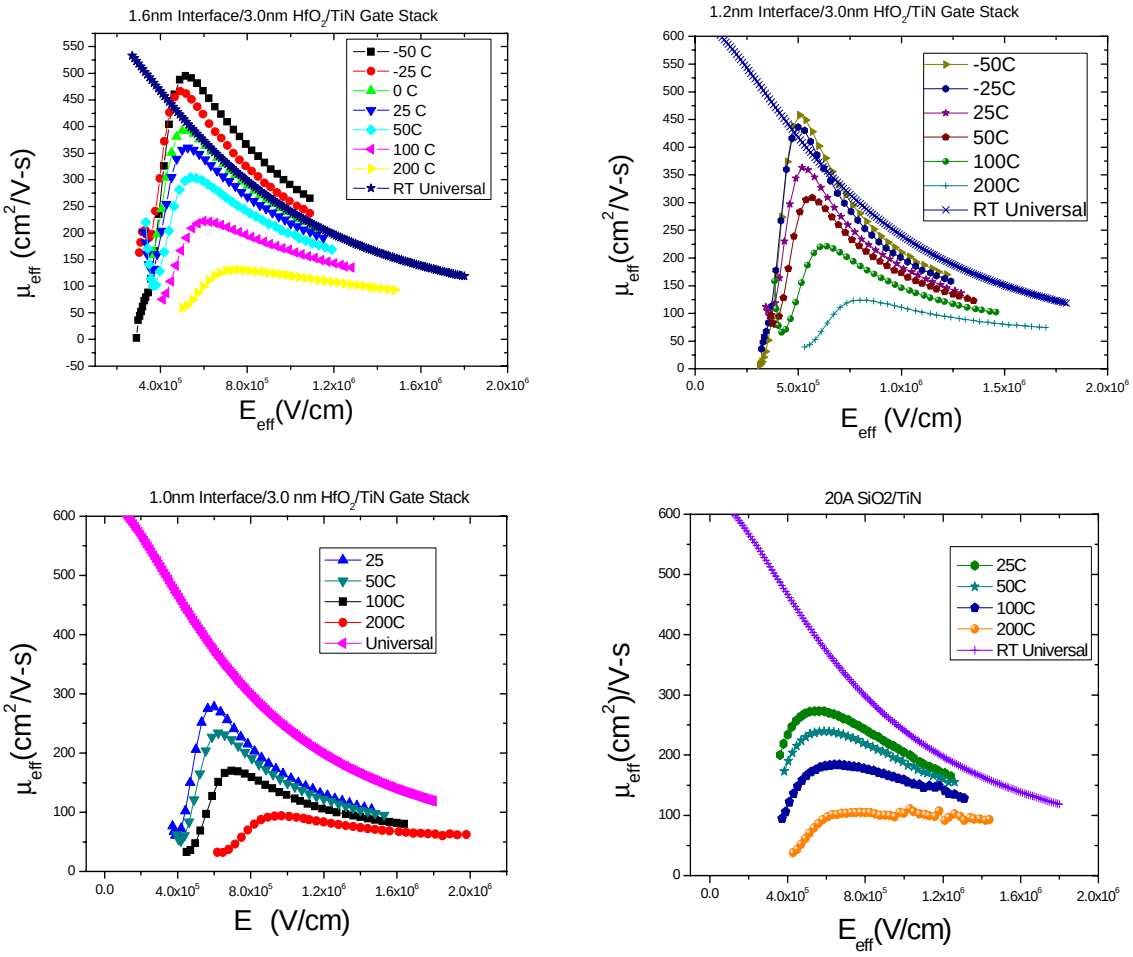


Figure 3.4: Mobility vs. temperature measurements for the different interfaces

Fig. 3.5 shows I_d vs. V_g and capacitance vs. V_g for different temperatures for the 1.2nm Interface. As can be seen, the interface state effects on CV and IdVg measurements are lower at lower temperatures (the curve "slewouts" are lesser at lower temperatures)

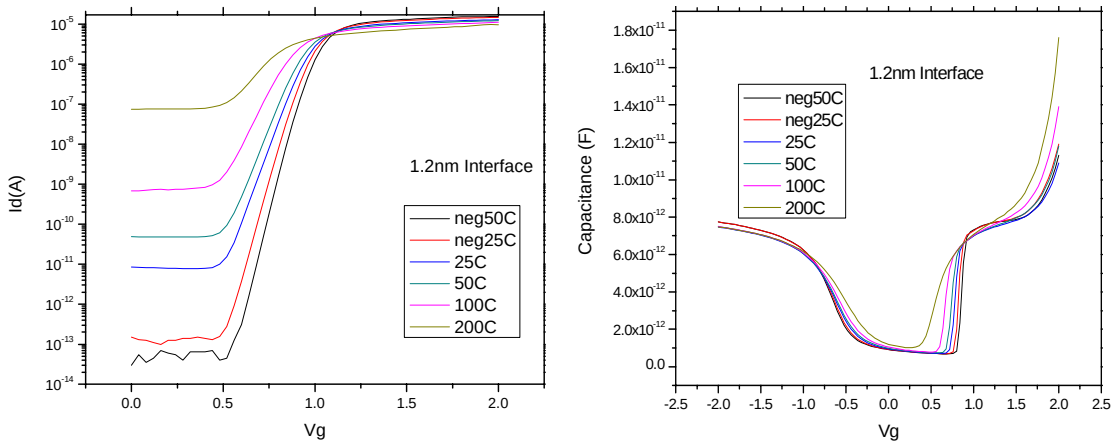


Figure 3.5: (a) Subthreshold swing improvement with temperature (b) CV "slewout" with temperature

In the high-field region (1MV/cm), the mobility dependence on temperature is maximum for the 1.6nm Interface, which lies exactly on top of the SiO_2/TiN mobilities (fig 3.6). This indicates that the degradation mechanisms for both are identical and a 1.6nm interfacial layer is enough to make the gate stack sufficiently SiO_2-like, as far as mobility is concerned.

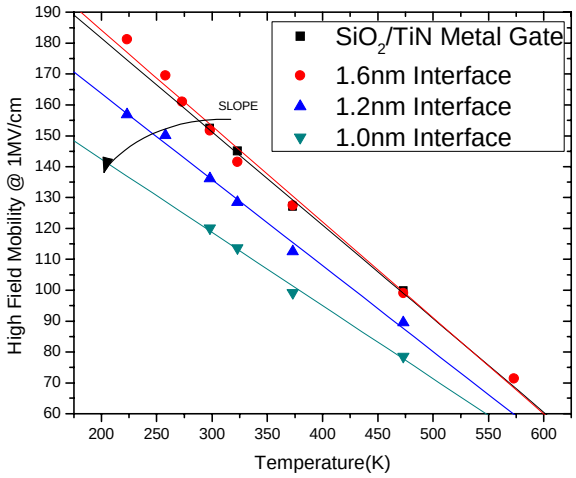


Figure 3.6: High field mobility dependence on temperature reduces steadily with thinner interface.

Quantitative assessment of the mobility is proposed to be investigated. Zhu *et al* [6] used Matthiesen's rule to approximately estimate the effect of coulombic, phonon and surface roughness scattering on HfO_2 samples with metal gates. According to Matthiesen's rule:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{coulomb}} + \frac{1}{\mu_{SurfaceRoughness}} \text{.....} \qquad \text{Equation 3.1}$$

: Matthiesen's rule

The surface roughness term can assumed to be constant with temperature and furthermore,

it can be assumed that the surface roughness is approximately the same as it is with a SiO_2/Poly-Si gate stack [7]

Numerical calculation of μ_{SR} can be done using the equation for SiO_2:

$$\mu_{SR} = B.E_{eff}^{-2.6} \qquad \text{Equation 3.2}$$

:Surface Roughness

B = 4.5 x 10^{19}: all the parameters are in S.I units.

This different scattering mechanisms are dominant at different field regimes in tradition SiO_2 gate stacks and are illustrated in fig. 3.7 [6].

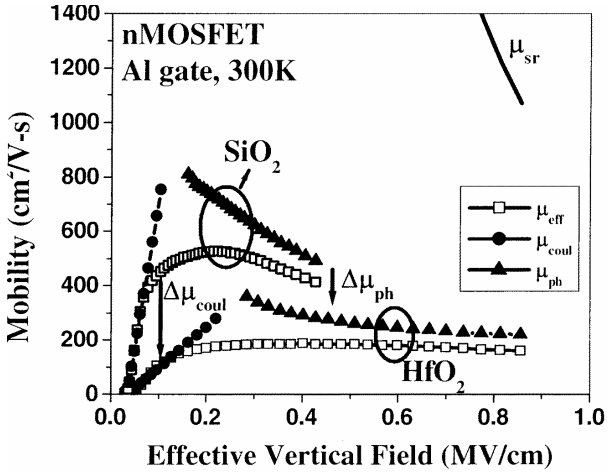


Figure 3.7: Figure illustrating different scattering modes [6]

The coulomb scattering component is illustrated in Fig. 3.7. The coulomb scattering component is extracted, as explained by extrapolating the low field mobility to 1MV/cm, by the fitting the mobility curve in that region to a straight line. This assumes that coulomb

scattering is the dominant scattering mechanism in the low field region and depends linearly on the field. As can be seen, the coulomb scattering term is not insignificant at room temperature and higher temperatures, especially in the thin films. Using matthiesen's rule and substituting for the coulomb scattering term and the surface roughness term, we can extract the phonon scattering term at 1MV/cm [3, 8]. This has been plotted in fig. 3.8 and fig. 3.9. As can be seen the phonon mobility is lower than the coulombic mobility and therefore is more dominant than coulomb scattering. The phonon mobility is independent on temperature in the high temperature regime and for all three interface thicknesses. This leads to the lower temperature dependence of effective mobility in the thinner interfaces.

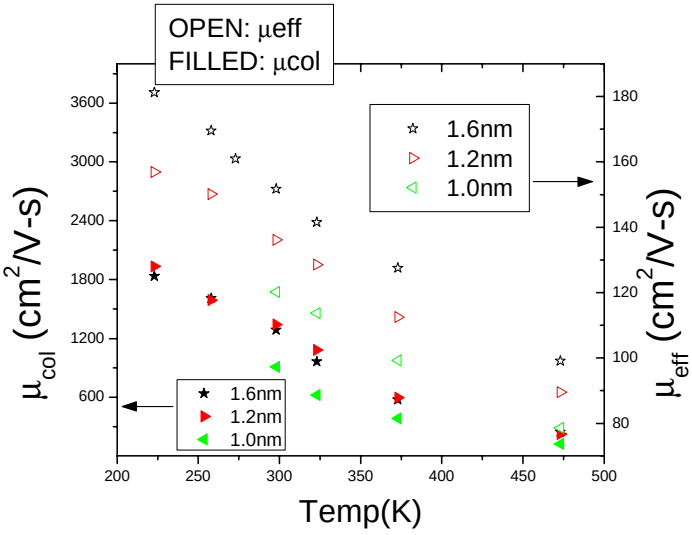


Figure 3.8: $\mu_{coulomb}$ reduces with temperature and is a significant portion of the scattering in HfO_2 gate stacks.

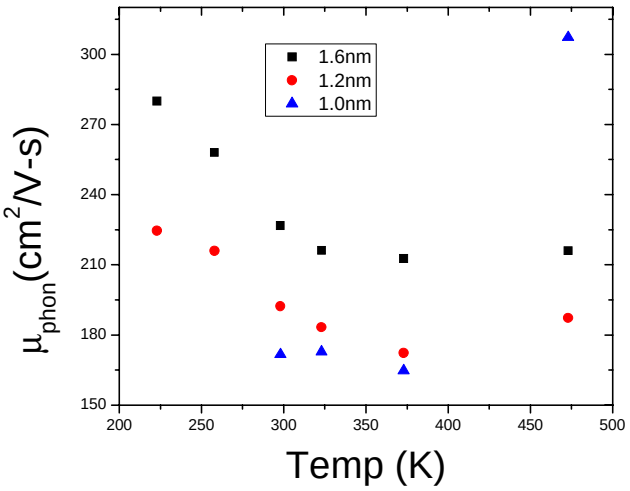


Figure 3.9: Phonon scattering reduces with temperature in the low temperature regime and flattens out in the high temperature regime

In order to estimate the soft optical phonon contribution in the high-κ devices, the phonon mobility of the thinner interface devices is subtracted from the 1.6 nm interface devices, assuming that the soft optical phonon mode is insignificant in the thick interface device (the mobility response to temperature is similar to that of SiO_2). We see in fig. 3.10 that there is a substantial soft optical phonon scattering in high-k devices and as expected, this scattering is independent of the temperature [9].

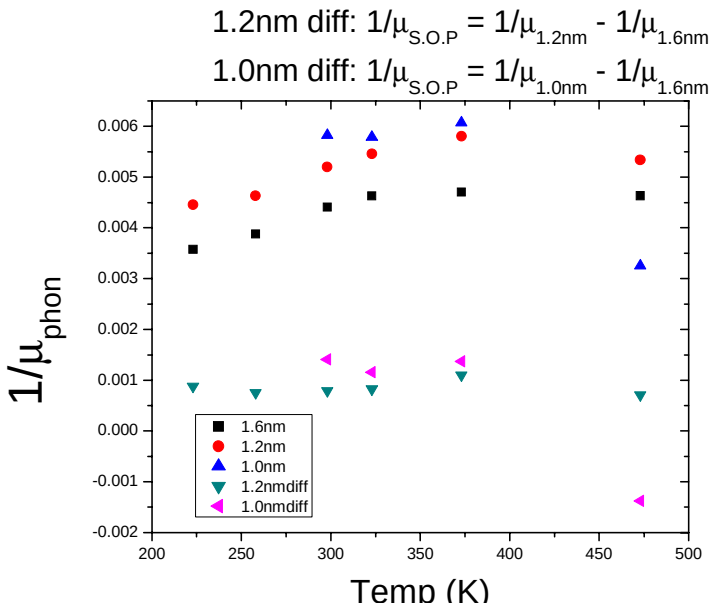


Figure 3.10: The soft optical mode is small in the 1.2nm and 1.0nm interface devices and is not comparable to the regular phonon mode.

3.5 Mobility Improvement Techniques

So far, we have discussed the various degradation mechanisms that beset HfO_2 dielectric that is 3.0 nm thick and is grown on interfaces that are 1.0 nm, 1.2 nm and 1.6 nm thick. It was discussed that the 1.6 nm interface layer yields high field mobility that is comparable to that of SiO_2 / TiN devices. However, for high performance applications, the required EOT is much lesser than the EOT that can be achieved with an interface layer of 1.6 nm. In order to achieve EOTs of 1.0 nm we need to reduce the interfacial layer thickness down to less than 1.0 nm. To recover the mobility degradation that occurs due to the high-κ layer, we could reduce the thickness of the high-κ layer. Although the study of reduced oxide thickness is discussed in much more detail in chapter 4, it is

relevant to present the mobility improvement with decreased high-κ layer thickness here. Samples with different high-κ layer thicknesses, ranging from 1.2nm to 3.0nm are made on an interfacial layer of 1.0 nm SiO_2, grown using ozone oxidant. Titanium nitride grown using ALD is used as the gate electrode. Figure 3.11 shows the mobility improvement as we decrease the thickness of the HfO_2 layer down to less than 2.0 nm. In chapter 4, reduced crystallization will be offered as a possible mobility improvement mechanism. EOT of 1.0 nm can be achieved by such reduction of physical thickness below 2.0 nm [10].

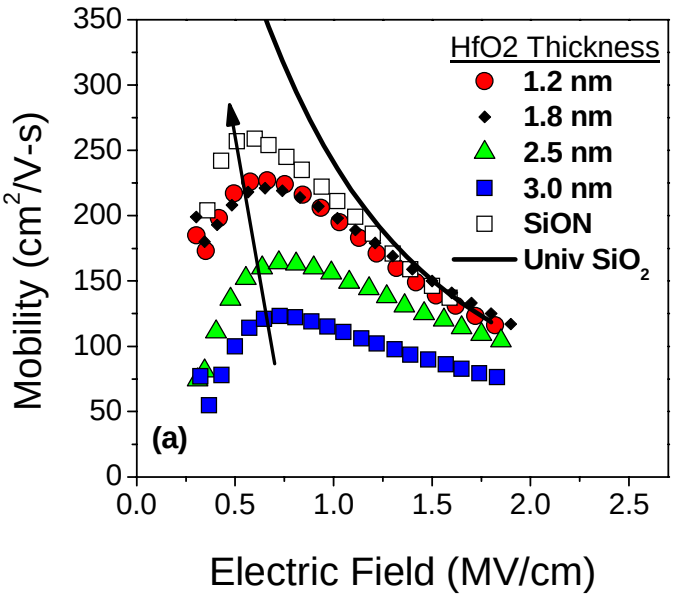


Figure 3.11: Electron mobility improvement with decrease in physical thickness [10].

3.6 Summary and Conclusions:

The effect of SiO_2 interface thickness on mobility was studied and it was found that mobility in both the peak and the high field region increased significantly. This is in part

due to reduction of interface trap density in thicker interfaces, leading to reduced coulombic scattering. An interface thickness of about 1.6 nm, with 30Å HfO_2 layer has high field and peak mobility that is comparable to SiO_2/TiN control devices. Therefore 1.6 nm of interface is enough to screen out the degradation mechanisms associated with the HfO_2 layer. The mobility degradation due to the high-κ layer is found to be dominated by phonon scattering in the high field region, with additional degradation due to coulombic scattering and soft optical phonon scattering as well. Further reduction in thickness of the high-κ layer could lead to better mobility.

3.7 References

1. Lime F, Ghibaudo G, Guillaumot B: **Investigation of electron and hole mobilities in MOSFETs with TiN/HfO/sub 2//SiO/sub 2/ gate stack**. In: *European Solid-State Device Research, 2003 ESSDERC '03 33rd Conference on: 2003*; 2003: 247-250.
2. Kerber A, Cartier E, Ragnarsson LA, Rosmeulen M, Pantisano L, Degraeve R, Kim Y, Groeseneken G: **Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics**. In: *VLSI Technology, 2003 Digest of Technical Papers 2003 Symposium on 2003*; 2003: 159-160.
3. Chau R, Datta S, Doczy M, Doyle B, Kavalieros J, Metz M: **High-/spl kappa//metal-gate stack and its MOSFET characteristics**. *Electron Device Letters, IEEE* 2004, **25**(6):408-410.
4. Wu WH, Chen MC, Wang MF, Hou TH, Yao LG, Jin Y, Chen SC, Liang MS: **Effects of base oxide in HfSiO/SiO/sub 2/ high-k gate stacks**. In: *Physical and Failure Analysis of Integrated Circuits, 2004 IPFA 2004 Proceedings of the 11th International Symposium on the 2004*; 2004: 25-28.
5. Young CD, Bersuker G, Brown GA, Lysaght P, Zeitzoff P, Murto RW, Huff HR: **Charge trapping and device performance degradation in MOCVD hafnium-based gate dielectric stack structures**. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 597-598.

6. Zhu WJ, Ma TP: **Temperature dependence of channel mobility in HfO/sub 2/-gated NMOSFETs**. *Electron Device Letters, IEEE* 2004, **25**(2):89-91.

7. Takagi S, Toriumi A, Iwase M, Tango H: **On the universality of inversion layer mobility in Si MOSFET's: Part II-effects of surface orientation**. *Electron Devices, IEEE Transactions on* 1994, **41**(12):2363-2368.

8. Massimo V. Fischetti DAN, and Eduard A. Cartier **Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high- insulator: The role of remote phonon scattering** *Journal of Applied Physics* 2001, **90**(9):4587.

9. Watling JR, Lianfeng Y, Asenov A, Barker JR, Roy S: **Impact of high-/spl kappa/ dielectric HfO/sub 2/ on the mobility and device performance of sub-100-nm nMOSFETs**. *Device and Materials Reliability, IEEE Transactions on* 2005, **5**(1):103-108.

10. Kirsch PD, J.H.Sim, S.C.Song, Krishnan S, Peterson J, Li H-J, Quevedo-Lopez M, Young CD, R.Choi, N.Moumen *et al*: **Mobility Enhancement of High-k Gate Stacks Through Reduced Transient Charging**. In: *EESDERC: 2005; Grenoble*: IEEE; 2005.

11. Jeff J. Peterson et al, **The Role of Interfacial Oxides in Mobility Improvement in HfO_2 Gate Stacks**. In: *Semiconductor Interface Specialists Conference, 2004, 35th Annual 2004 IEEE International: 2004.*

Chapter 4

Thickness Dependence of PBTI

4.1 Introduction

Among the primary issues deterring the introduction of high-κ dielectrics into the 45nm CMOS product flow, mobility, charge trapping in nMOSFETs and fermi-level pinning remain the most problematic and need to be addressed urgently. Positive Bias Temperature Instability or PBTI has been reported to be a severe problem in high-κ nMOSFETs and is reported to be due to electron trapping in neutral or positively charged trapping centers [1-4]. This electron trapping leads to a significant increase in the threshold voltage (V_{TH}) with positive bias stress. For reliable operation over time, this threshold voltage instability needs to be reduced to less 10mV, after 10 years [5]. The charge trap density in the dielectric, which is responsible for the reported high V_{TH} shifts, needs to be reduced to suppress the V_{TH} instability to acceptable values. There have been several techniques that have been reported to reduce the charge trap density. Eliminating the crystallinity of the dielectric, which might in turn reduce the intrinsic charge traps at the grain boundaries, is one of them [6]. Incorporating nitrogen in the dielectric through various techniques is another often reported technique[6-8]. In this chapter, the effect of the physical structure of the film (i.e. amorphous or crystalline) is examined.

4.2 Sample Fabrication and Experiment

On HF-cleaned wafers, two different interfaces are grown: a) 10Å of chemically grown SiO_2 or b) SiON. This is followed by atomic layer deposition (ALD) of Hafnium Silicon Oxy-Nitride (HfSiON - 30% SiO_2) or Hafnium Oxide (HfO_2). ALD Titatnium Nitride (TiN) is used as the gate electrode. The thickness of the HfSiON is increased from 1.8 nm to 3.0 nm in regular steps [9]. The HfO_2 is similar varied. The standard CMOS transistor flow yielded wafers with excellent across-wafer-uniformity, equivalent oxide thicknesses (EOTs) of 1.0–1.5 nm, and electron mobility approaching universal channel mobility (~90%). Figure 4.1 shows the Leakage current characteristics as a function of EOT and mobility as a function of EOT [9].

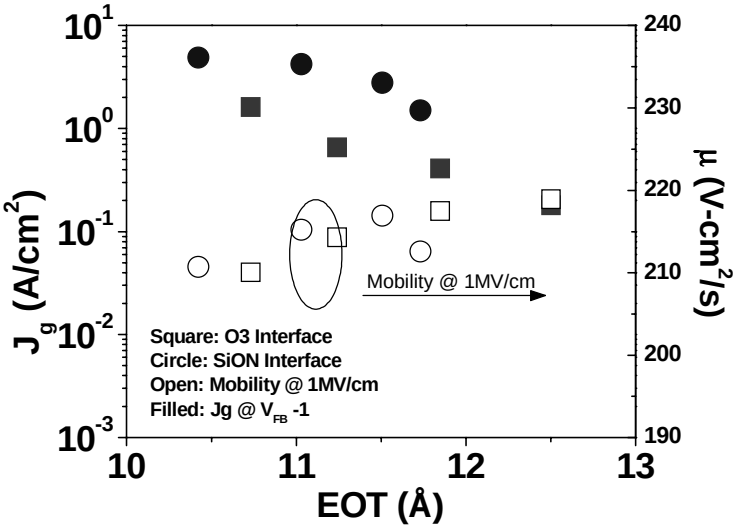


Figure 4.1: As physical thickness is increased, Jg decreases, while mobility increases mildly in HfSiON.

The mobility of the HfSiON in this very thin regime between 1.8 nm and 3.0 nm increases with increasing thickness. The mobility degradation mechanisms that were discussed in the previous chapter indicated that the coulombic scattering might be one of the mechanisms responsible for mobility degradation. FTIR results showed that the thickness of the interfacial SiO_x increased with increase in the thickness of the HfSiON layer (Fig. 4.2).

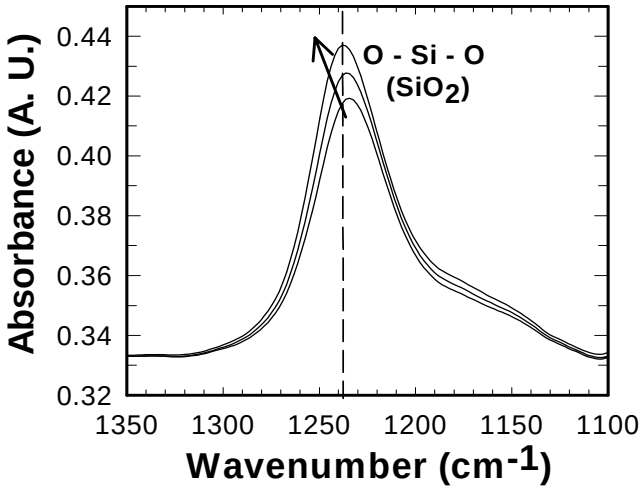


Figure 4.2: FTIR – shows increase in peak and shift to the left, indicating increase in O-Si-O bonds

Figure 4.2 indicates also that the quality of the SiO_x layer improved (to more SiO_2 like bonding states) with increase in thickness of the HfSiON layer, leading to better interface state density. The combined effect of better screening due to increased interfacial layer thickness and improved interface state density leads to improved mobility with increase in the thickness of the dielectric. In the case of HfO_2, however,

while EOT-J_g characteristics were similar to the HfSiON case, the mobility decreased with increase in thickness (Fig. 4.3 and 4.4) [10].

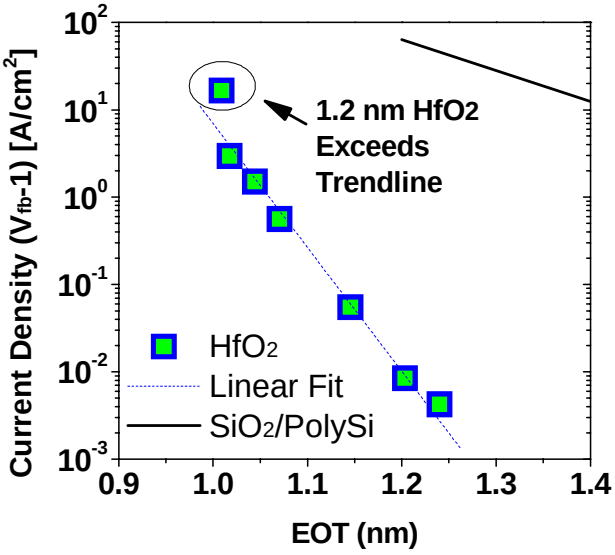


Figure 4.3: Jg – EOT shows leakage current ~100x lower than SiO_2/Poly-Si.

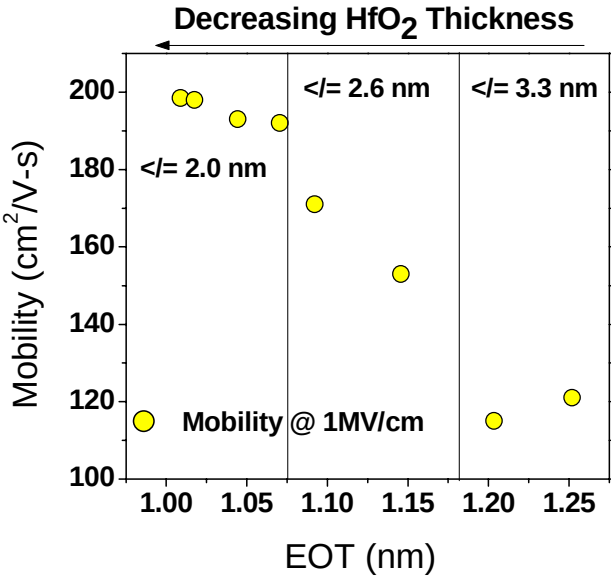


Figure 4.4: Mobility at 1MV/cm decreases with increasing EOT.

The PBTI tests are performed on 10x1 μm nMOS devices, with source, drain, and substrate grounded during the stress. To fairly compare the characteristics of the different samples, the vertical field across the MOSFET is matched by applying (V_g-V_{TH})/EOT = Constant MV/cm. The threshold voltage is extracted from I_d-V_g sweeps that are performed during periodic interruptions of the stress. The I_d-V_g sweeps are performed from 0 to 1.5V.

4.3 PBTI in HfSiON

The vertical electrical field is set at 10.9 MV/cm ((V_g-V_{TH})/EOT = 10.9 MV/cm). The measured V_{TH} instability as a function of time at room temperature is shown in Fig. 4.5 for thicknesses for samples with SiO_2 interface.

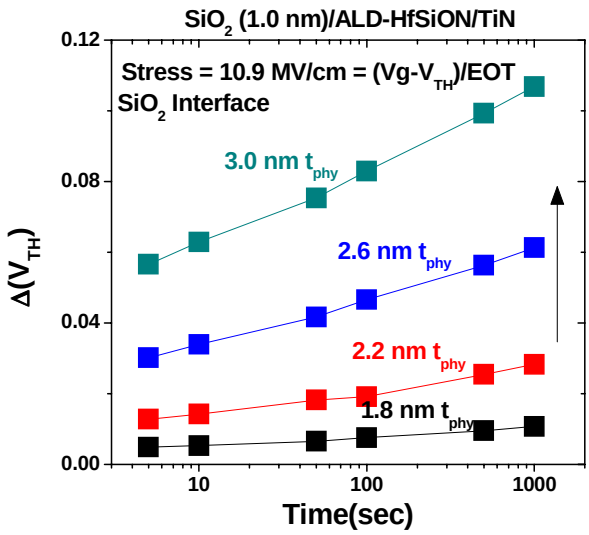


Figure 4.5: V_{TH} instability as a function of dielectric thickness (SiO_2 Interface): Significant increase in V_{TH} instability thickness increases.

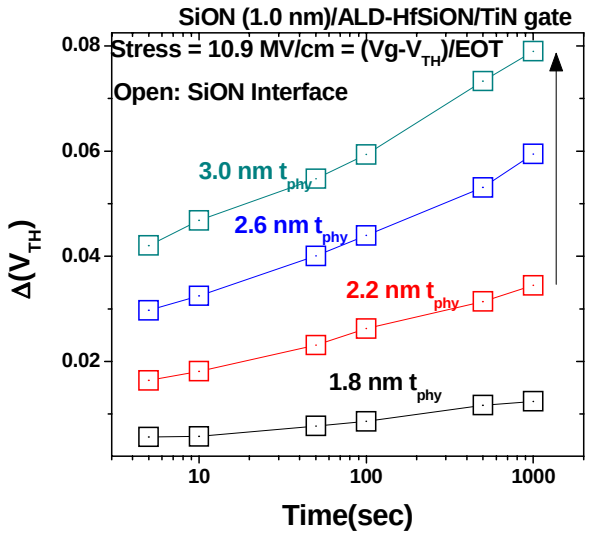


Figure 4.6: V_{TH} Instability as a function of thickness in SiON/HfSiON/TiN gate stacks.

As can be seen, there is a very significant thickness dependence of V_{TH} shift on the thickness of the film. The same thickness dependence is seen in samples with SiON interface, as well (Fig. 4.6). A notable result from these measurements is that the V_{TH} shift at this high stress field (~1.87 V) can be reduced to *less* than 10 mV after 1000 sec of stress by reducing the thickness of the dielectric to 1.8 nm. This is amongst the lowest reported V_{TH} shift values for comparable fields [1-3]. The increased V_{TH} instability with dielectric thickness is to be expected, as the number of charge traps that can trap electrons (that tunnel through the dielectric) increases with increasing thickness. Similar measurements were performed at 85C as well (Fig. 4.7 & 4.8)

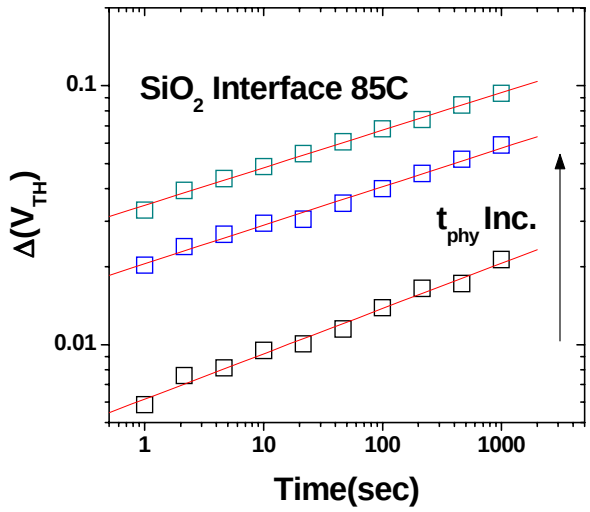


Figure 4.7: Elevated temperature measurements show the same trends as the measurements at room temperature.

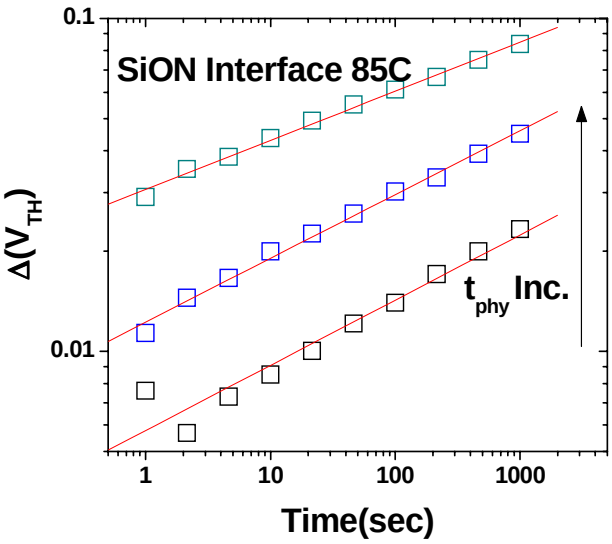


Figure 4.8: V_{TH} Instability at 85C for SiON interface: Significant dependence on thickness

The effect of temperature on the thin dielectric (18Å) is more pronounced than on the thicker dielectric. This is because the leakage current mechanism is more temperature-dependent in the thinner oxide (more electron supply at higher temperature).

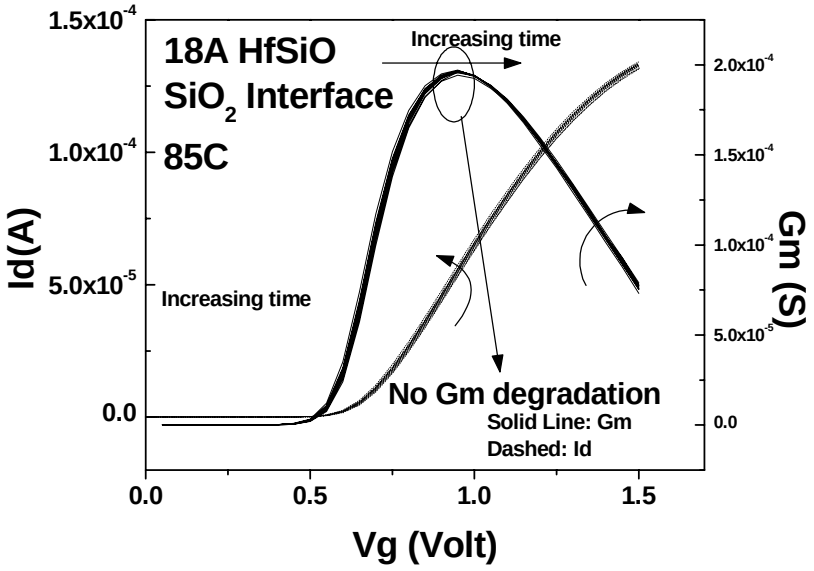


Figure 4.9: No Gm degradation during stress. Only V_{TH} shift.

While the V_{TH} increase is accompanied by no degradation of transconductance (at both temperatures) (Fig. 4.9), the instability in threshold voltage is slightly worse for the SiON than for the SiO_2 interface. This appears to be due to the lower bandgap of SiON [11], due to which the supply of electrons is larger across the interfacial layer, as can be ascertained from the Jg-EOT plot (Fig. 4.1). The V_{TH} increase after 1000 sec of stress is plotted as a function of EOT for both the SiO_2 and the SiON interfaces in Fig. 4.10.

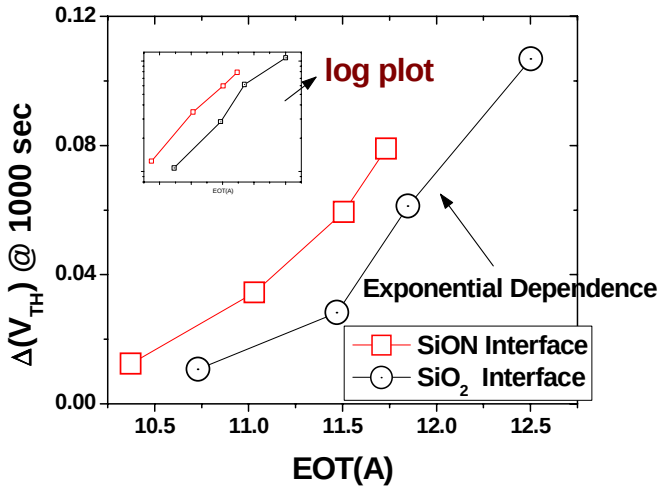


Figure 4.10: EOT Dependence of V_{TH} shift is exponential in the thickness range investigated.

The ΔV_{TH} is *exponentially dependent* on EOT for both the interfaces (inset shows log-linear plot) in the thickness range investigated. The expected trend would be linear, as the number of charge traps should increase linearly with a linear increase in thickness.

4.3.1 Theoretical Analysis:

Figure 4.11 shows the schematic of the electron trapping that is used for this analysis.

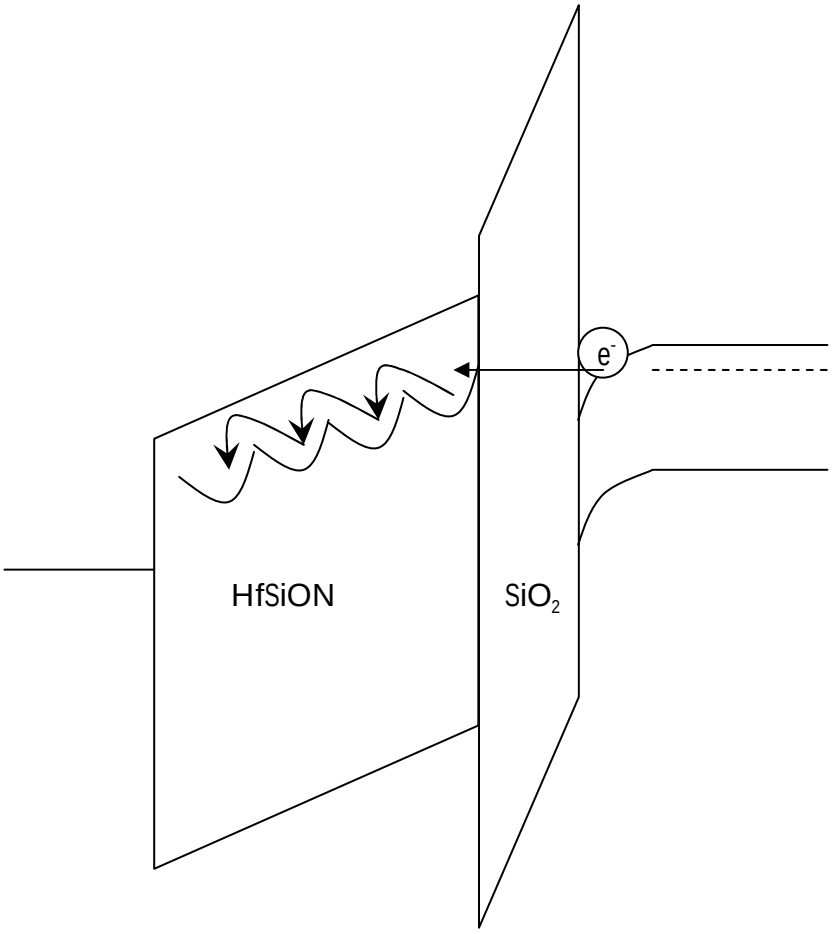


Figure 4.11: During the stress, electron gets trapped in a transient manner and is redistributed.

G. Bersuker et al [12] suggested that during electrical stress, electrons get trapped within 100 μsec in traps located close to the interface between the SiO_x interface layer and HfO_2 layer. This accounts for the rather large V_{TH} shift seen in the initial stages of the stress. The slower shift that happens during the stress is due to slow migration along the conduction band, under the influence of stress field and temperature. If N_t is the

total number of charge traps into which electrons have been trapped, the change dN_t is proportional to remaining empty traps (that electrons from inversion layer can tunnel into) and is proportional to the total number of currently trapped electrons (N_t, from which electrons can migrate into neighbouring traps). Therefore,

$$dN_t = k_1(N - N_t)dt + K_2 N_t dt \quad \text{.....Equation 4.1}$$

$$dQt = k_1(Q_0 - Q_t)dt + K_2 Qtdt \quad \text{.....Equation 4.2}$$

Equation 4.2 is the same as equation 4.1, with trapped charge in coulombs, than electron numbers.

$$\int_0^{Qt} \frac{dQ_t}{k_1 Q_0 + (k_2 - k_1)Q_t} = \int_o^t dt \quad \text{.....Equation 4.3}$$

Where Q_t is the trapped charge at any point in time t: The solution for this equation is:

$$Qt = A(1 - e^{-t/\tau 1}) \quad \text{.....Equation 4.4}$$

Now, as we stress the device for a long time, the charge migration through the dielectric moves the charge centroid in the direction of the electric field.

The change in threshold voltage when there is charge Q_t at distance x_t is:

$\Delta(V_{TH}) = Q_t (x/d)/(\varepsilon/d) = Q_t x/\varepsilon$ ……..Equation 4.5 [13]

Differentiating w.r.t time:

$$dV_t = x_t dQ_t + Q_t dx_t$$ .....Equation 4.6

Now, the charge centroid x_t is going to move along the direction of the electric field according to the grove model [14], because for charge migration, there is almost a constant charge supply, like in the case of constant source diffusion. Therefore, a not-insignificant assumption needs to be made about the rate at which the centroid moves as a function of time:

$x/t_{phy} = e^{-t/\tau 2}$ …….. Equation 4.7

This assumption is not strictly accurate, since the tunneling electrons get trapped at least 10Å away from the interface (thickness of the interface layer). For a first approximation, it is a good assumption, though.

Substituting for x_t in equation 4-6, we get:

$$\Delta V_{TH} = A + Be^{-t(\frac{1}{\tau 1}+\frac{1}{\tau 2})} + Ce^{-\frac{t}{\tau 1}}$$ .....Equation 4.8

When the data from the 18Å film is fitted to this equation, we get a fit with R^2> 99.4% (Fig. 4.12)

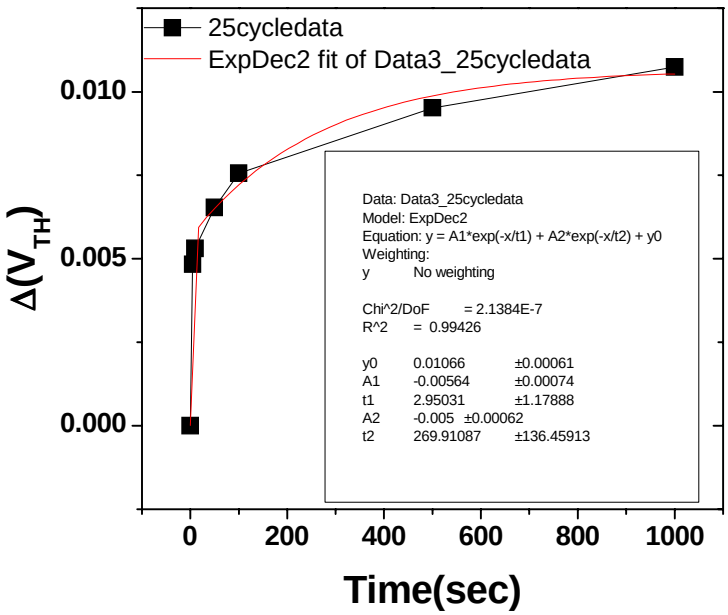


Figure 4.12: Fit of the equation to the data: R^2 =0.994.

Note that τ_1 ~ 2.9 sec, while τ_2 is the in the order of 269 seconds. The first time constant is the time constant for tunneling electrons to get trapped, while the second is the time constant for migrating electrons to move along the conduction band. Since the second time constant is the rate limiting step, the data is fitted to equation 4.8 assuming τ_1 ~ 0:

i.e. $V_{TH} = V_{TH0}(1+e^{-(\frac{t}{\tau 2})})$

The time constants are derived for the data from the SiO_2 interface samples and plotted in figure 4.13.

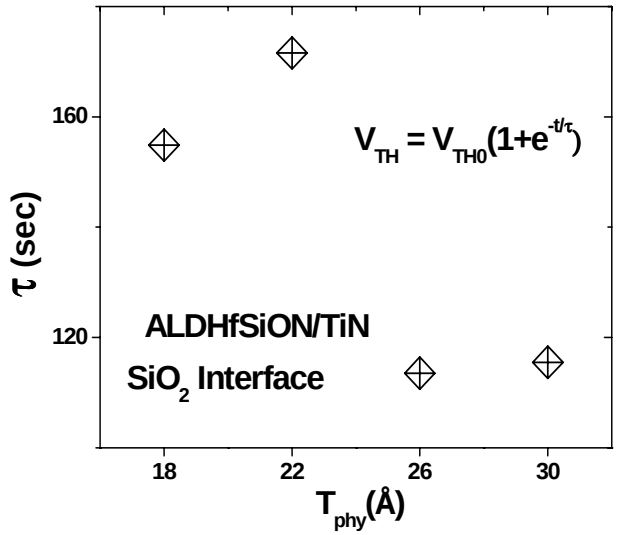


Figure 4.13: Extracted time constant as a function of physical thickness.

The time constant changes significantly when physical thickness is increased from 2.2 nm to 2.6 nm, indicating a change in the physical structure. Figure 4.10 showed that that the dependence of V_{TH} shift on EOT is exponential in this thickness range and we can see that charge trapping increases significantly when we go from 2.2 nm to 2.6 nm. It is proposed that the sudden change in the trapping behavior happens due to a transition in the physical structure. The extent of crystallization increases significantly when the film becomes more than ~2.0 nm thick.

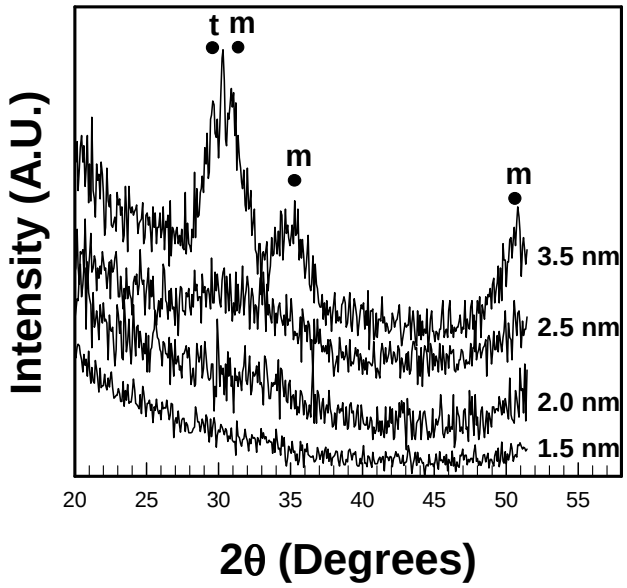


Figure 4.14: XRD peaks corresponding to the monoclinic and triclinic phases begin to appear as the thickness is increased beyond 2.5 nm, which corresponds to the charge trapping behavior.

To further investigate this proposal, XRD was performed on the HfSiON films to study the extent of crystallinity as a function of HfSiON thickness. A special XRD technique using grazing angles (<5°) on a Rigaku Ultima III thin film diffractometer, was used because the films were too thin for conventional diffractometers. Figure 4.14 shows the XRD characteristics as a function of the HfSiON thicknesses. For the thin HfSiON films (<2.0 nm), there is no detectable peak, but as the film becomes thicker, distinct peaks corresponding to monoclinic and tetragonal phases of HfO_2 phase develop. This is an indication of increased crystallinity in the thicker films. From Avrami's equation [15],

in equation 4.9, the fraction of the dielectric that is crystallized increases with increasing deposition time (Figure 4.15).

$f=1-\exp(-k.t^n)$ ……Equation 4.9

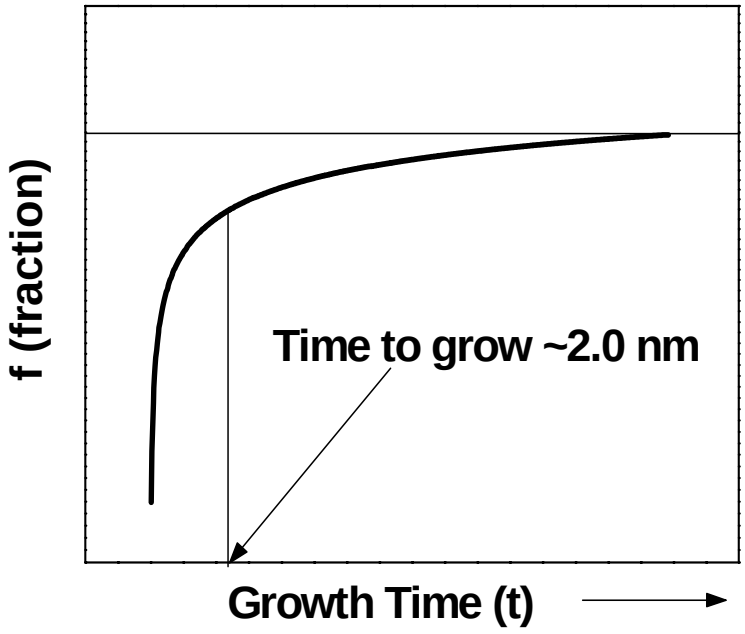


Figure 4.15: Graphical representation of Avrami's equation.

It is concluded that for HfSiON thinner than ~2.0 nm, crystallization is significantly suppressed, leading to reduced charge trap density. This reduced charge trap density is responsible for significantly reduced V_{TH} instability. The reduction in charge trap density could be due to a number of reasons. Reduction in crystallization would reduce the grain boundary area in the dielectric, leading to reduced trapping from defect sites in the grain boundaries. It has been proposed that the oxygen vacancies in the bulk or in the grain boundaries are responsible for increased trapping in high-κ gate stacks [16, 17].

Reduction in crystallization might also reduce the density of oxygen vacancy related traps, that might be present in the grain boundary.

4.4 Stress Induced Leakage Current (SILC) in HfSiON

As discussed in chapter 2, Stress Induced Leakage Current or SILC is an important issue in conventional dielectrics and has been thought of as a wear-out mechanism before breakdown occurs. As the high-κ dielectrics are made thinner, the trap density in the dielectrics becomes lesser, leading to lesser threshold voltage shift as discussed in the earlier sections in this chapter. As discussed in chapter 2, we would expect the reversible SILC phenomenon to get less as the trap density is reduced. This could happen by increasing the percentage of silicon in HfSiON or by decreasing the thickness. The evolution of SILC as a function of dielectric thickness in HfSiON is investigated, when the samples are stressed at $(V_G-V_{TH})/EOT = 10.9$ MV/cm. Figure 4.16 shows just the addition of silicon is enough to reduce the trap density down to the point where the SILC phenomenon almost completely disappears. Trap generation at this field is, therefore, minimal.

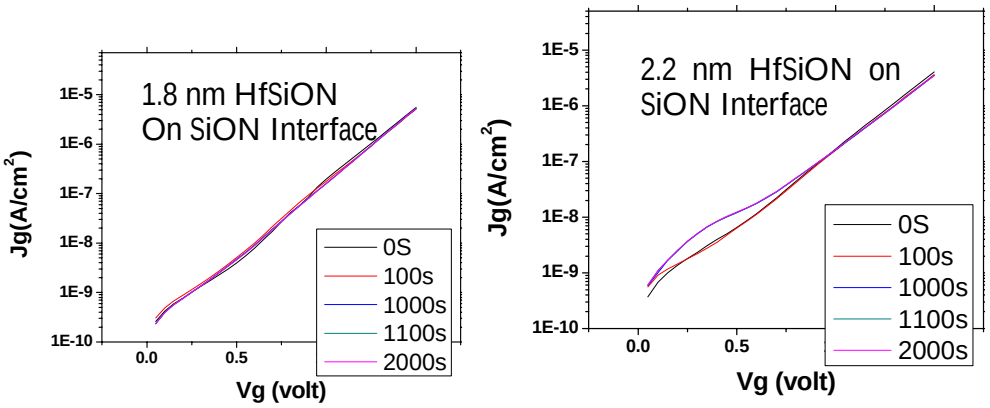


Figure 4.16: SILC is insignificant in both thickness – No leakage current increase can be seen.

4.5 Time Dependent Dielectric Breakdown (TDDB) dependence on thickness

Time dependent dielectric breakdown or TDDB has been a premier tool in assessing the lifetime of transistors under accelerated testing conditions[18-20]. Breakdown in SiO_2 dielectrics has been attributed to creation of defects under electrical stress leading to the creation of a "percolation path", i.e., a path of defects that line up and form a direct path of leaking carriers to flow from the substrate to the gate, leading to catastrophic increase in leakage current and loss of drain current [21]. This is illustrated in the figure.

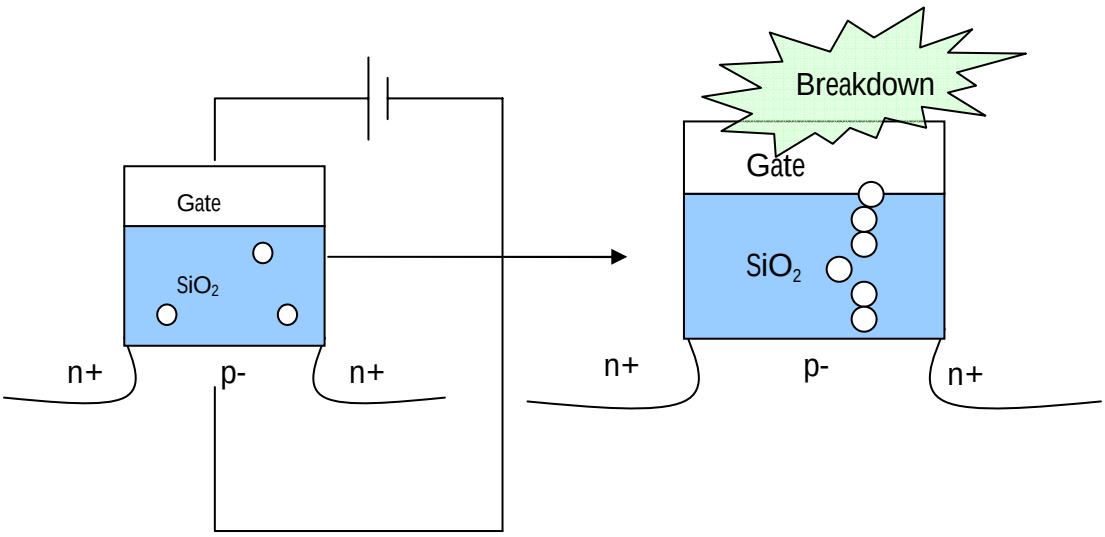


Figure 4.17: Illustration of the formation of a percolation in the example of an nMOSFET with SiO_2 and gate under positive bias stress.

In order to assess the breakdown characteristics of HfSiON with ALD-TiN as a function of dielectric thickness, two of the samples discussed in the earlier sections, 1.8 nm HfSiON and 3.0 nm HfSiON are taken stressed at various stress voltages, in order to extract stress weibull slopes [22] and time to failure. From the weibull plots, the times to 63% sample failure rate are extracted and are plotted with stress voltage in order to obtain 10 year lifetime operating voltage. The devices used were nMOS-capacitors with source/drain "rings" around the perimeter, with n+ doping levels equal to that seen in

source/drain areas in transistors. The active area is used because an active inversion layer can be formed when the capacitor is stressed with a positive bias.

Figure 4.18 shows the extracted time to failure curves for the 1.8 nm devices.

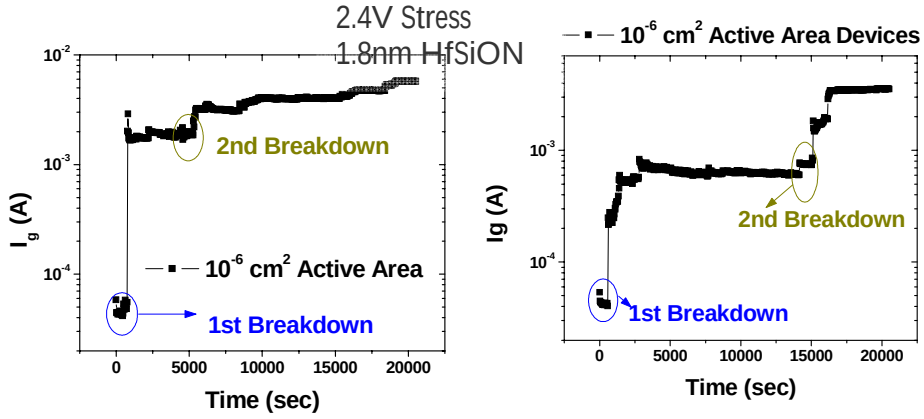


Figure 4.18: Sample Ig-time curves in a 10^{-6} cm^2 in 18Å HfSiON devices, when stressed at 2.4V Stress

The typical curve in 1.8 nm devices looks like figure 4.18. There are two breakdowns, the first of which is the interface layer breakdown. This speculation is backed up by our report (chapter 2) that most of the trap generation in the in interface layer, during constant voltage stress. The second breakdown is that of the high-k breaking down. Figure 4.19 shows the typical breakdown characteristics in the thicker HfSiON. As can be seen, the two breakdowns still exist, but the breakdowns are much closer to each other.

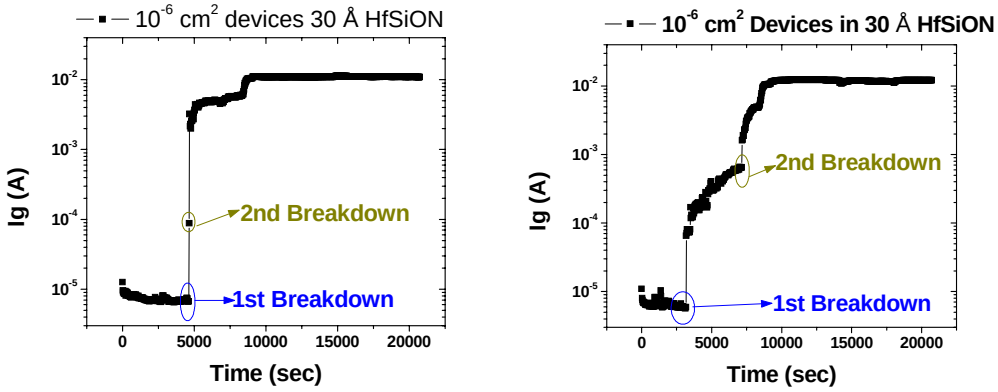
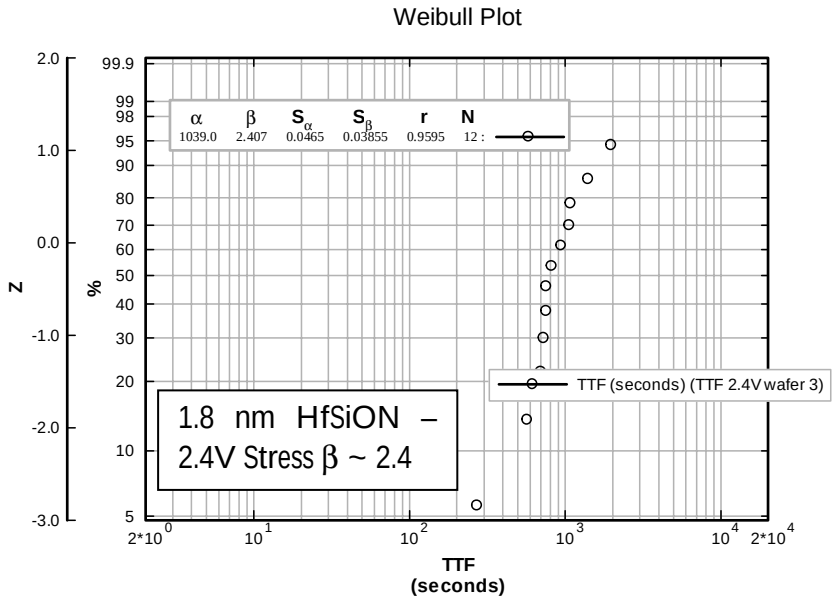


Figure 4.19: The gate current (Ig)-time characetistics when the active area devices are stressed under a 2.45V stress. The two breakdowns happen close together.

This essentially means that breakdown is catalysed much more easily in the high-κ layer due to the interface layer in the thicker HfSiON device. This might be due to a more defective high-κ layer, as indicated by the charge trapping results, in the earlier sections. The high-κ layer, being much more robust in the thin dielectric due to lesser trap density, is not affected by the breakdown of the interface layer significantly. This is also reflected in the weibull plots drawn from over 16 devices from each thickness (1.8 nm and 3.0 nm).



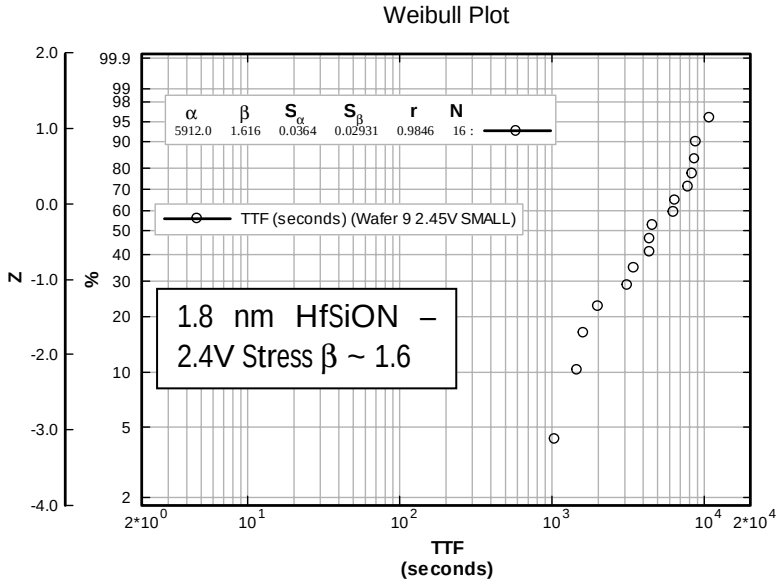


Figure 4.20: a) Weibull plot of 1.8 nm HfSiON under 2.4V stress - β ~ 2.407.

b) Weibull plot of 3.0 nm HfSiON under 2.45V Stress - β~ 1.6.

The increase in "beta" values of the weibull distribution as we increase the thickness from 1.8 nm to 3.0 nm is reflective of increase in randomization of the breakdown, which in turn is indicative of increased defect density, which is also consistent with the earlier theories. The extracted 10 year lifetime operating voltage is shown in figure 4.21, and it can be seen that both the thickness have operating voltages which are well above the specifications that are laid down by the ITRS.

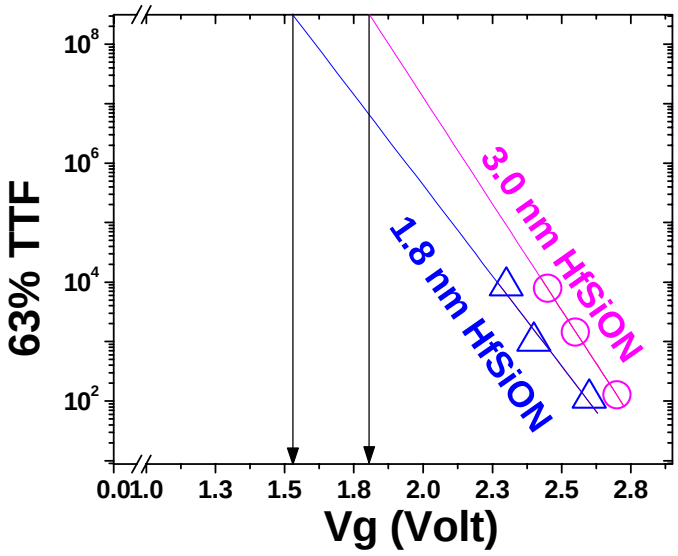


Figure 4.21: The extracted 10 year lifetime operative voltages are above 1.5V for both thickness.

4.6 PBTI in HfO_2

Samples for this study used various thicknesses of HfO_2 starting from 1.2 nm and going on till 3.0 nm. SiON reference [23] is used to compare mobility. Figure 4.16

shows the mobility of the devices as a function of EOT [2]. As can be seen, there is a dramatic improvement in mobility in the as the HfO_2 is made thinner than 1.8 nm.

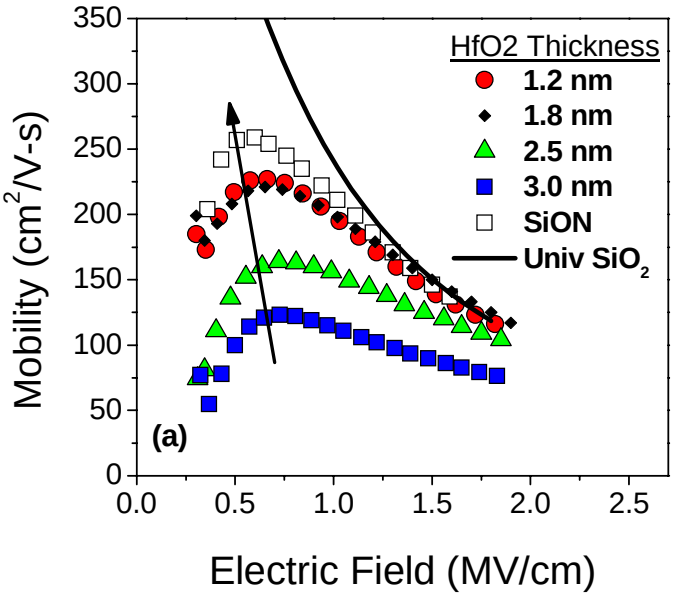


Figure 4.22: Dramatic improvement in HfO_2 mobility below t_{phy} ~ 2.0 nm.

This improvement in mobility is attributed to two factors:

a) Reduction in charge trapping, which reduces the reduction in inversion charge loss.

b) Reduction in fixed charges in the high-κ leading to reduced coulombic scattering.

These samples are stressed at ~10.9 MV/cm to compare the charge trapping characteristics. Figure 4.17 shows the V_{TH} instability plots as a function of thickness. As before, when the thickness of the dielectric is below 2.0 nm, V_{TH} instability is reduced to very low values.

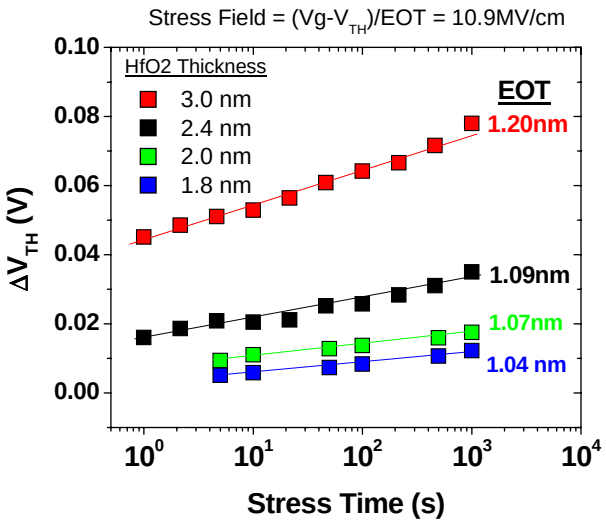


Figure 4.23: As before, HfO_2 also exhibits reduced charge trapping at thicknesses below 2.0 nm.

For these samples P. Kirsch et al [2] also reported reduced crystallinity at t_{phy} = 1.2 nm.

Device Wafers: 1000C-5s S/D anneal

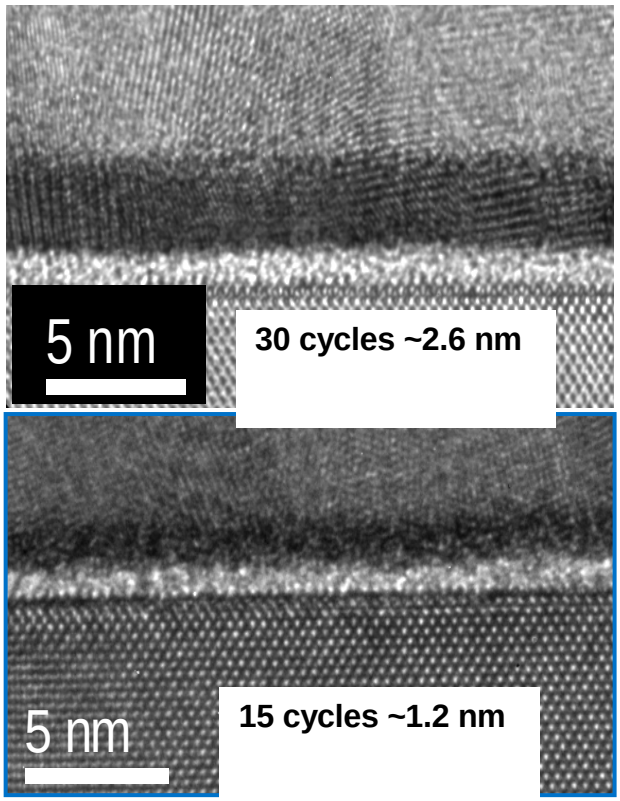


Figure 4.24: Reduced crystallization in thin HfO_2.

4.7 SILC in HfO_2

Like in the case of HfSiON, there is nearly no SILC in HfO_2 when the thickness of the film is reduced to below 2.0 nm (Fig. 4.20). It is evident that the most important factor in the reduction of SILC is the trapping density in the films.

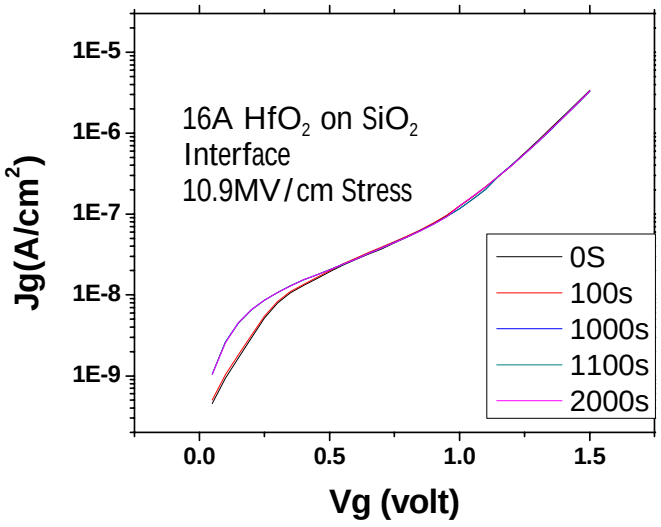


Figure 4.25: No increase detected in leakage current during 10.9 MV/cm in 16A HfO_2 film on SiO_2 Interface.

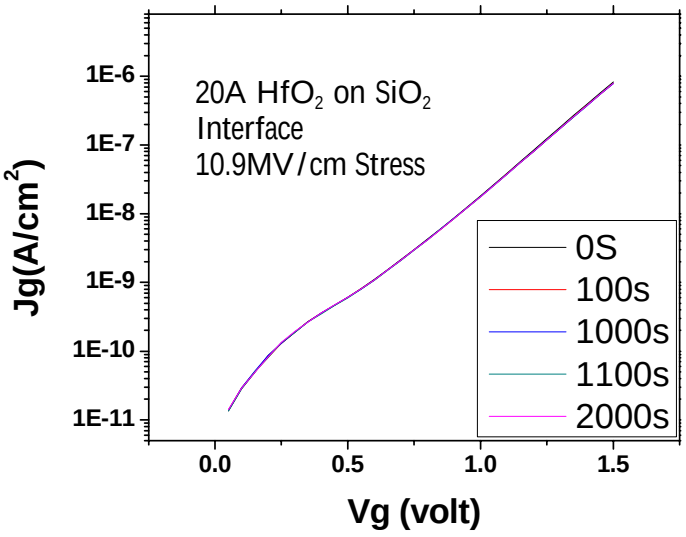


Figure 4.26: 20A HfO_2 does not have any increase in leakage current after 2000 seconds of stressing, either.

4.8 Conclusions

Positive bias temperature instability as a function of dielectric thickness was investigated in HfSiON/ALD TiN gate, with SiO_2 and SiON interfaces. PBTI is also investigated as a function of thickness in HfO_2 dielectric with SiO_2 interface and ALD TiN. An exponential dependence of charge trapping on the EOT of the gate stack in the thickness range investigated in HfSiON, is observed. V_{TH} instability also was significantly reduced (<10mV) as the physical thickness of the dielectric was reduced to 18Å. This dramatic change in trapping behavior is attributed to a transition in the physical structure from crystalline to amorphous phase, reducing the trap density in the films dramatically. The SiON interface films have greater V_{TH} instability than the SiO_2 interface films due to higher leakage leakage. A comprehensive mathematical model for the evolution of threshold voltage shift was proposed, showing the change in threshold voltage follows a 2^{nd} order exponential decay dependence on time. Stress induced leakage current (SILC) is shown to be negligible in both HfSiON and HfO_2 when the physical thickness is reduced to lower than 2.0 nm.

TDDB is investigated with active area capacitors in inversion. In each 10^{-6} cm^2 device tested, two distinct breakdowns are seen. The two breakdowns are far apart in the thin dielectric, suggesting independent mechanisms for breakdown of the interface and the bulk HfSiON, while they are much closer to each other in the thick HfSiON, suggested catalysis of the bulk HfSiON breakdown, by the interface layer breakdown.

This confirms the reduced trap density in thin HfSiON that was proposed in the earlier paragraph. The weibull slope values increase from 1.6 to 2.4 as we decrease the thickness of the dielectric from 3.0 nm to 1.8 nm. This also is indicative of reduced defect density (which is proportional to the randomization of the breakdown) in the thinner dielectrics. The reduction in trap density at thickness below 2.0 nm is also observed in HfO_2.

4.9 References

1. Byoung Hun L, Rino C, Sim JH, Krishnan SA, Peterson JJ, Brown GA, Bersuker G: **Validity of constant voltage stress based reliability assessment of high-/spl kappa/ devices**. *Device and Materials Reliability, IEEE Transactions on* 2005, **5**(1):20-25.
2. Kirsch PD, J.H.Sim, S.C.Song, Krishnan S, Peterson J, Li H-J, Quevedo-Lopez M, Young CD, R.Choi, N.Moumen *et al*: **Mobility Enhancement of High-k Gate Stacks Through Reduced Transient Charging**. In: *EESDERC: 2005; Grenoble*: IEEE; 2005: 367.
3. Kerber A, Cartier E, Ragnarsson LA, Rosmeulen M, Pantisano L, Degraeve R, Kim Y, Groeseneken G: **Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics**. In*: 2003*; 2003: 159-160.
4. Ribes G, Muller M, Bruyere S, Roy D, Denais M, Huard V, Skotnicki T, Ghibaudo G: **Characterization of Vt instability in hafnium based dielectrics by pulse gate voltage techniques [CMOS device applications]**. In: *Solid-State Device Research conference, 2004 ESSDERC 2004 Proceeding of the 34th European: 2004*; 2004: 89-92.
5. **Internation Technology Roadmap for Semiconductors**
6. Koyama M, Satake H, Koike M, Ino T, Suzuki M, Iijima R, Kamimuta Y, Takashima A, Hongo C, Nishiyama A: **Degradation mechanism of HfSiON gate insulator and effect of nitrogen composition on the statistical distribution of the breakdown**. In: *VLSI Symp: 2003*; 2003: 38.34.31-38.34.34.

7. Koike M, Ino T, Kamimuta Y, Koyama M, Kamata Y, Suzuki M, Mitani Y, Nishiyama A, Tsunashima Y: **Effect of Hf-N bond on properties of thermally stable amorphous HfSiON and applicability of this material to sub-50nm technology node LSIs**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International: 2003*; 2003: 4.7.1-4.7.4.
8. Koyama M, Kaneko A, Ino T, Koike M, Kamata Y, Iijima R, Kamimuta Y, Takashima A, Suzuki M, Hongo C *et al*: **Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics**. In: *IEDM Tech Dig: 2002*; 2002: 849-852.
9. M.Quevedo-Lopez: **High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements**. In: *International Electron Devices Meeting: 2005; Ca*: IEEE; 2005.
10. Kirsch PD, J.H.Sim, S.C.Song, Krishnan S, Peterson J, Li H-J, Quevedo-Lopez M, Young CD, R.Choi, N.Moumen *et al*: **Mobility Enhancement of High-k Gate Stacks Through Reduced Transient Charging**. In: *EESDERC: 2005; Grenoble*: IEEE; 2005.
11. Hori T: **Gate Dielectrics and MOS ULSIs**. Berlin: Springer-Verlag; 1997.
12. Bersuker G: **Novel dielectric materials for future transistor generations**. In*: 2005*; 2005: 10-10.
13. B. Streetman SB: **Solid State Electronic Devices**: Prentice Hall; 2001.
14. Wolf S: **Silicon Processing for the VLSI era**, vol. 2: Lattice Press; 1990.
15. M.Avrami: *Journal of chemistry and physics* 1939, **7**:1103.

16. J. L. Gavartin ALS, A. S. Foster and G. I. Bersuker: **The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies**. *JOURNAL OF APPLIED PHYSICS* 2005, **97**:13.

17. Robertson J, Ka X, Falabretti B: **Point defects in ZrO/sub 2/ high-/spl kappa/ gate oxide**. *Device and Materials Reliability, IEEE Transactions on* 2005, **5**(1):84-89.

18. Chaparala P, Suehle JS, Messick C, Roush M: **Electric field dependent dielectric breakdown of intrinsic SiO₂ films under dynamic stress**. In: *Reliability Physics Symposium, 1996 34th Annual Proceedings, IEEE International: 1996*; 1996: 61-66.

19. Hokari Y, Baba T, Kawamura N: **Reliability of 6-10 nm thermal SiO<inf>2</inf>films showing intrinsic dielectric integrity**. *Electron Devices, IEEE Transactions on* 1985, **32**(11):2485-2491.

20. Suehle JS, Chaparala P, Messick C, Miller WM, Boyko KC: **Field and temperature acceleration of time-dependent dielectric breakdown in intrinsic thin SiO₂**. In: *Reliability Physics Symposium, 1994 32nd Annual Proceedings, IEEE International 1994*; 1994: 120-125.

21. Cheung KP: **The last trap that form the percolation path - the stress voltage effect**. In: *Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 599-600.

22. **The Weibull Distribution**

23. Datta S, Dewey G, Doczy M, Doyle BS, Jin B, Kavalieros J, Kotlyar R, Metz M, Zelick N: **High Mobility Si/SiGe Strained Channel MOS Transistors with HfO2/TiN Gate Stack**. *IEDM Tech Dig* 2003:653.

Chapter 5

NBTI in HfSiON

5.1 Introduction

Negative Bias Temperature instability (NBTI) has been reported to be a primary reliability problem in SiO_2/Poly-Si gate stacks, leading to increase in interface trap density [1-3]. This increase in interface trap density is due to the breakage of Si-H and Si-OH bonds at the interface (Hydrogen-Reaction-Diffusion model or H^0-R-D), due to hole injection from the inversion layer in the n- substrates. A direct result of this bond breakage is the increase of threshold voltage, which leads to increase in circuit timing delay, because of a reduction in drain current. Alam [4] showed that this increase in threshold voltage in the SiO_2 gate stacks could be mathematically shown to follow a power law relationship with time (Equation 1 [4]). This increase in threshold voltage is due to the creation of interface charge due to the breakage of hydrogen bonds and the subsequent diffusion of hydrogen through the dielectric to the gate electrode.

$$N_{IT} = \sqrt{\frac{k_F N_0}{k_R}}(D_H t)^n = \sqrt{\frac{k_{F0} N_0}{k_{R0}}} D_{H0}{}^n \left[\sqrt{p e^{-E_{ox}/E_0}}\right]\left[e^{-\left\{\frac{\Delta E_F - \Delta E_R}{2} + n\Delta E_H\right\}/kT}\right]\left[t^n\right]$$

Field-dependence Temp-dependence Time-dependence

…….Equation 5.1 [4].

Equation 5.1 shows that the shift in threshold voltage follows a power law relationship with exponent “n”. This exponent “n” has been theoretically and experimentally shown to be approximately 0.26 [1-4] in SiO_2/Poly-si.

The threshold voltage shift also has temperature dependence, as the breakage of H-bonds and the subsequent diffusion of neutral or charged H atoms is a temperature dependent process. Prof. Alam reported the activation energy of this process to be ~ 0.5 eV [4] (figure 5.1)

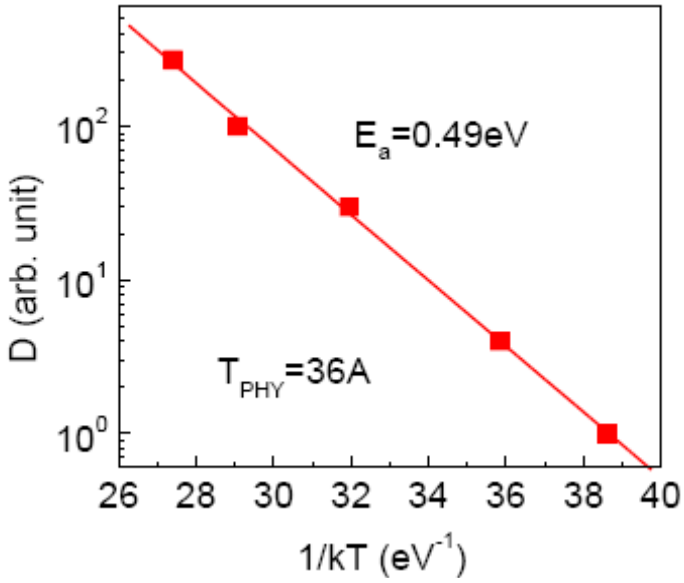


Figure 5.1: Activation energy for H°-R-D – Prof. Alam report E_a ~ 0.5 eV.

In high-κ dielectrics, the presence of traps complicates the mechanism of NBTI further. R. Harris et al [5] showed reported that the increase of threshold voltage in 40 Å high-κ HfSiON is dominated by detrapping of negative charges from traps that are deep in the bandgap of HfSiON [5]

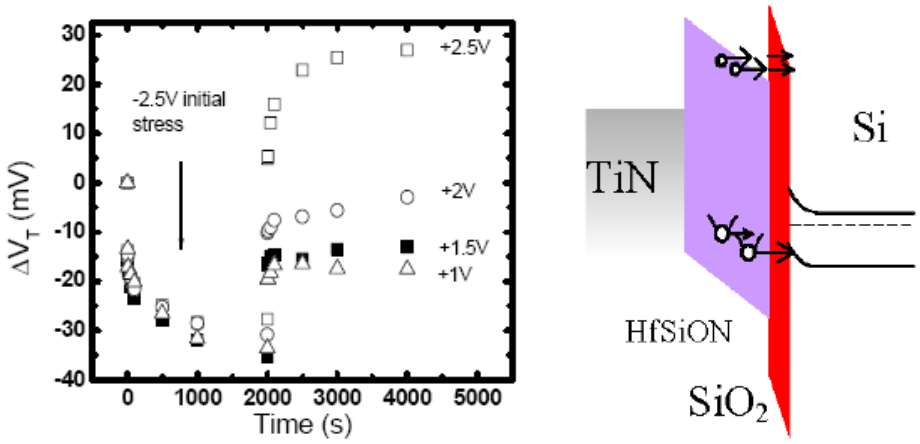


Figure 5.2: R. Harris[5] showed that Charge trapping dominates V_{TH} shift.

The charge trapping is dominant in the thick films and dominates the effect interface traps that are formed during the stress. As trap density is reduced, it is expected that the Hydrogen Reaction Diffusion, if it is present in these dielectrics, will become increasingly evident.

5.2 Sample Fabrication and Experimental Details

On HF cleaned wafers, 10Å of interfacial oxide is grown, followed by atomic layer deposition (ALD) $HfSiO_x$ (30% SiO_2 – 18Å, 22Å, 26Å and 30Å) using $Hf[N(CH_3)C_2H_5]_4$ (TEMAHf) and $Si[N(CH_3)C_2H_5]_4$ (TEMASi) precursors with ozone oxidant (Post Deposition Anneal - 700C for 30s). The ALD TiN gate electrode is then deposited [8]. The remaining transistor flow is standard and yielded wafers with excellent across-wafer-uniformity, EOT of 1.0-1.5 nm and electron mobility approaching universal channel mobility (already shown in fig. 4.2). In order to qualitatively assess the HfSiON dielectric and the sub-oxide interface with the silicon substrate, Fourier Transform

Infrared Spectroscopy [6, 7] is done on blanket films with the same thickness as the device films. The absorbance peak of the O-Si-O cluster increases in magnitude and shifts to the left. This indicates an increase in SiO_2 bonding, which might be due to mild increase in thickness of the sub-oxide layer or an improvement in the quality of the interface layer or a combination of the two. Table 5.1 shows the CMOS product flow used to make the pMOS transistors.

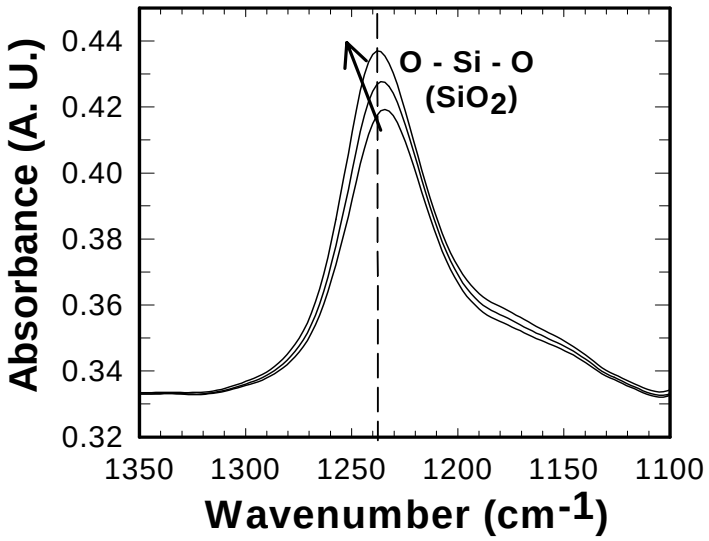


Figure 5.3: FTIR results show an increase in the peak of O-Si-O bonding and a shift to the left, indicating improvement in quality if interface.

HF cleaning
SiO_2 Interface (10Å)
ALD 30% $HfSiO_x$ (18Å, 22Å, 26Å and 30Å)
PDA (700ºC, 30sec)
TiN / Polysilicon 1500 Å deposition
Gate predoping
N LDD/halo
Nitride spacer
N SD (Source and Drain)
SD RTA (1000ºC, 5sec)
Metallization
Forming Gas anneal (480ºC, 30min)

Table 5.1: CMOS product flow used to make transistors.

The NBTI tests are performed on 10×1 μm pMOS devices, with source, drain, and substrate grounded during the stress. The samples are stressed using a constant voltage for 1000s. The transconductance (gm) and threshold voltage (V_{TH}) are extracted using Id-Vg sweeps performed during periodic interruptions of the stress. Measurements are performed at various stress voltages and 3 different temperatures - Room Temperature (RT), 75°C and 125°C.

5.3 Results and Discussion

As discussed in the earlier sections, NBTI in SiO_2/Poly-Si devices has been described to be due to breakage of H-bonds and subsequent diffusion of neutral or charge H-atoms or molecules, causing an increase in threshold voltage ("negative shift"). Measurements are done at three different voltages 2V, 2.2V and 2.4V on the thinnest and the thickest dielectric (1.8 nm and 3.0 nm). According to equation 5.1, the V_{TH} shift

plotted with time on a log-linear scale should be parallel. Figure 5.4 shows the V_{TH} shift with time at the three different voltages for the 1.8nm dielectric. The lines are all parallel and the power law exponent (slope "n") is extracted to be ~ 0.22-0.23 for the 1.8 nm dielectric. The V_{TH} shift lines are also parallel at three different measurement temperatures: room temperature, 75°C and 125°C. This is shown in figure 5.5.

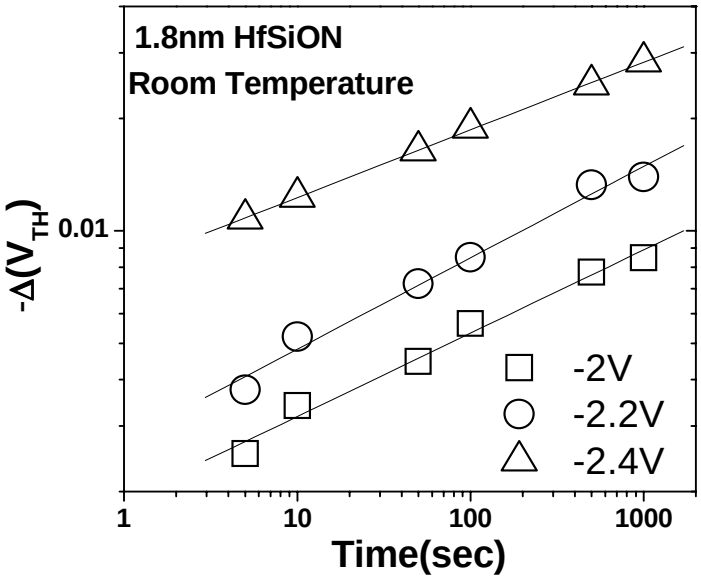


Figure 5.4: V_{TH} shift is shown as a function of time for the 1.8nm HfSiON dielectric – The lines are nearly parallel and the slope is seen to be 0.22.

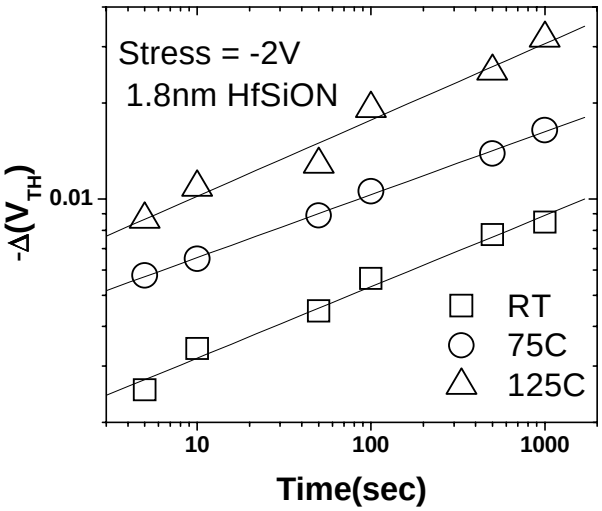


Figure 5.5: V_{Th} shift as a function of time at different temperatures in 1.8 nm HfSiON. Slope "n" ~ 0.22-0.23.

For the thick HfSiON (3.0 nm), however, the slope is ~ 0.14-0.15. Figure 5.6 shows the V_{TH} shift lines at different stress voltages for the thick HfSiON.

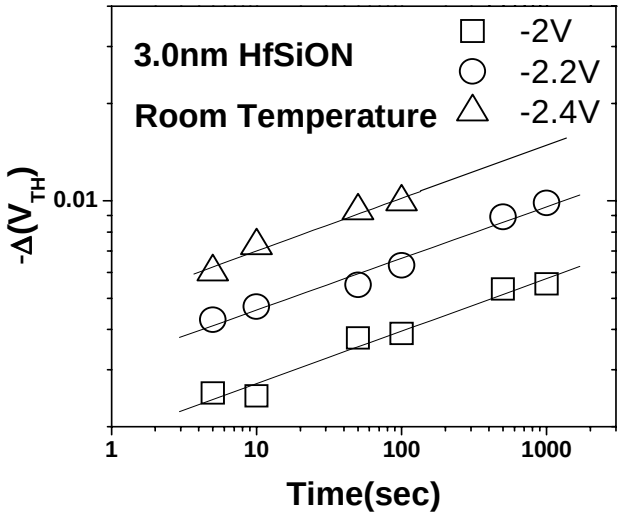


Figure 5.6: V_{TH} shift as a function of time in the thick HfSiON – Slope "n" ~ 0.14-0.16.

The slope is also independent of the measurement temperature and is shown for two temperatures in figure 5.7.

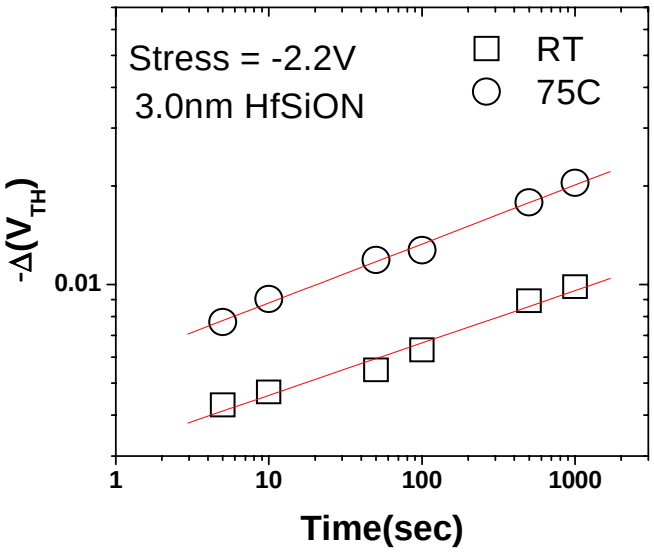


Figure 5.7: V_{TH} shift as a function of time in the 3.0nm HfSiON – Slope is independent of temperature.

Now, it is not just sufficient to look at the threshold voltage shift alone in these dielectrics, because the threshold voltage is accompanied by (and is due, in part to) a downward shift in the peak transconductance ($g_{m,max}$) (Figure 5.8). The downward shift in the transconductance peak is related directly to the creation of interface traps (gm α μ). The shift in threshold voltage is more than what could occur due to creation of interface traps, due to concurrent charge trapping / detrapping in the bulk HfSiON layer.

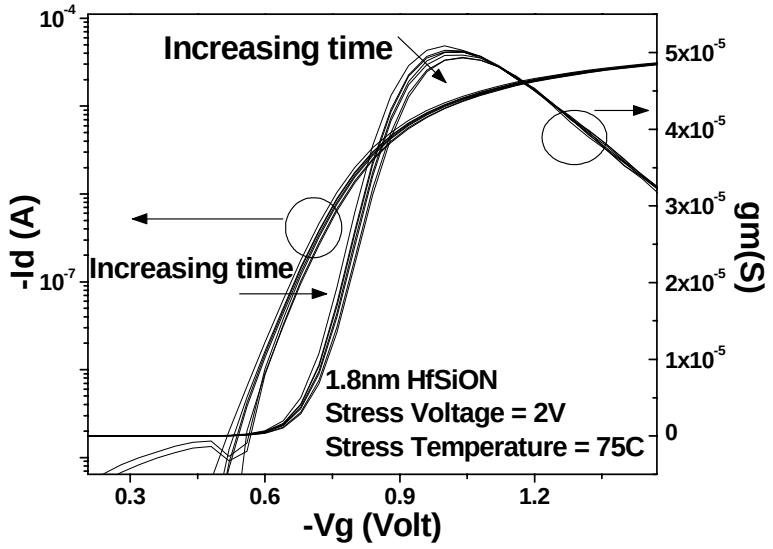


Figure 5.8: The V_{TH} shift is accompanied by a concurrent decrease in peak transconductance, indicative of creation of interface traps.

The said results can be explained as follows. NBTI in high-κ dielectrics can be said to be from two sources:

a) Electron detrapping from bulk HfSiON.

b) Interface trap creation due to hole trapping from the inversion layer in the substrate. The trap creation might be due to breakage of weak Si-H bonds at the interface.

The power law exponent in the thin dielectric is ~0.22, much closer to the SiO_2 power law exponent of 0.26. The contribution of (a) is minimal is SiO_2 and the threshold voltage shift is almost entirely due to creation of interface traps due to Hydrogen reaction and diffusion.

However, the larger bulk contribution controls the power law exponent in the case of thick HfSiON (3.0 nm). The low value "n" implies slow charge detrapping in the thick dielectric. In the thin dielectric, however, the "n" value is much closer to that in SiO_2, implying that the H°-R-D is significant, although the charge detrapping is still prevalent. This theory is further bolstered if we consider the entire range of thickness from 1.8 nm to 3.0 nm and plot the slope "n" as a function of physical thickness (figure 5.9)

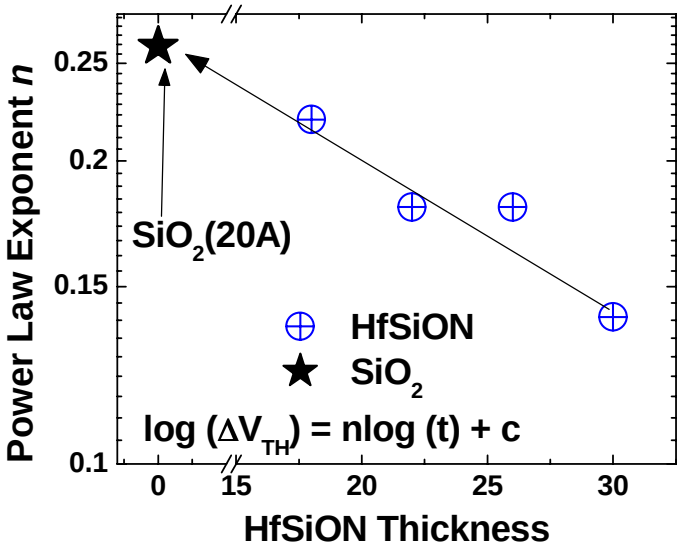
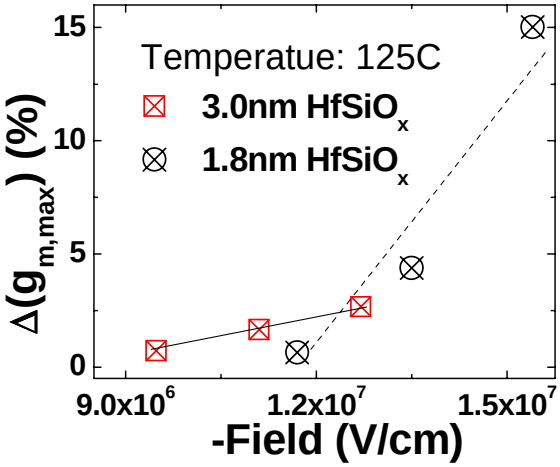
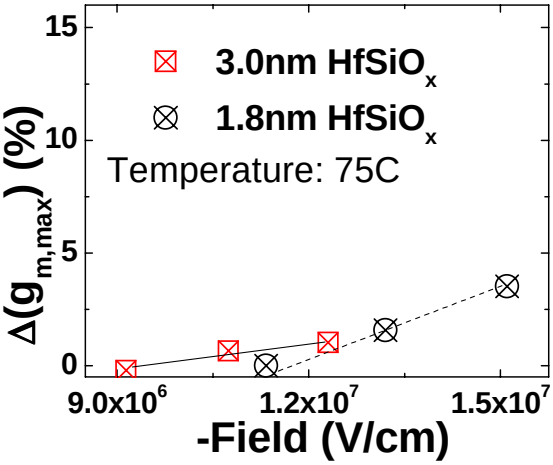


Figure 5.9: Power law exponent "n" collapses towards that of SiO_2 as we reduce the thickness of the high-κ layer.

As can be seen in figure 5.9, the power law exponent “n” collapses towards that of SiO_2/Poly-Si (0.26), showing the increasing prominence of Hydrogen-Reaction-diffusion in thinner dielectrics.

The interface therefore starts playing a more significant role in the NBTI processes in the thin dielectrics. The peak transconductance degradation (at 10 sec of stress) is shown as a percentage value of the unstressed film in figure 5.10 (next page). The peak transconductance degradation is plotted as a function of the stress field at three different temperature. The increase in slope of the line is much more severe for the thin dielectric (1.8 nm) than for the thick dielectric (3.0 nm) as we increase the temperature from room temperature to 75°C to 125°C. The dependence on temperature and field in the thin film is indicative of the bond breakage mechanism becoming more significant. Figure 5.11 shows the same set of curves for the threshold voltage, where the same trends are evident.





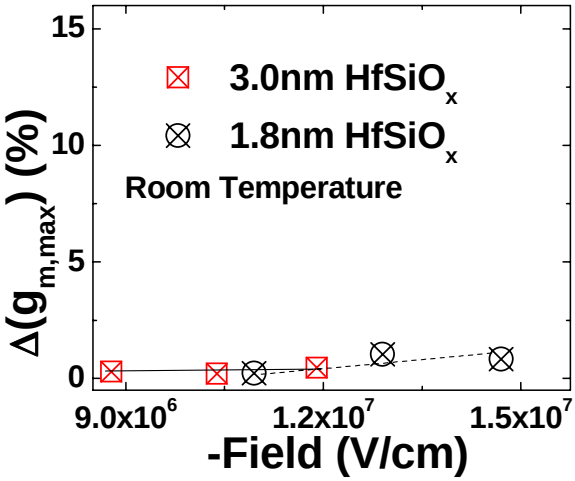


Figure 5.10 Transconductance degradation at 10sec as a function of stress field - Slope of the thinner dielectric increases much more than the thick dielectric as the temperature is increased from room temperature (a) to 125C (c)

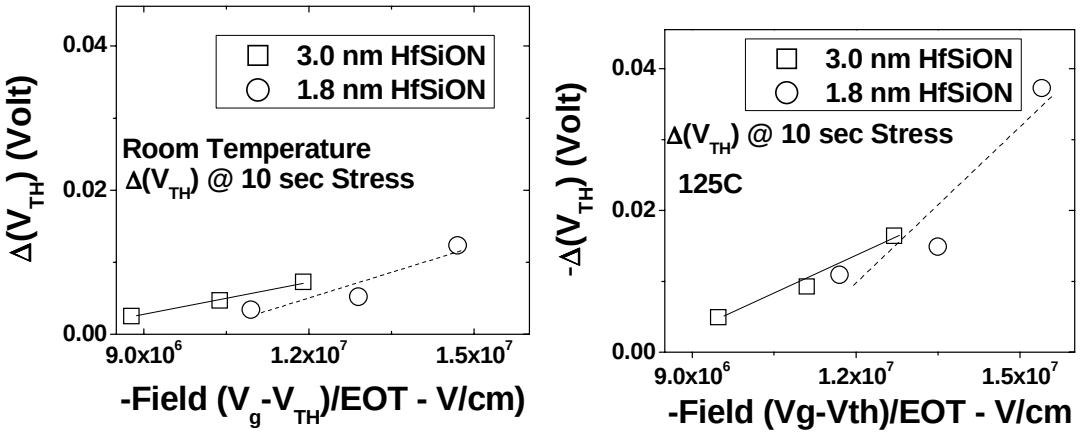


Figure 5.11: Shows the ΔV_{TH} at 10 sec stress, as a function of stress field at room temperature and 125C. The slope increase is much more severe for the 1.8nm HfSiON.

In SiO_2/Poly-Si gate stacks, the activation energy is indicative of the energy to break the bonds at the interface and the activation energy of the diffusion of the H atoms through the dielectric. The change in threshold voltage is plotted as a function of 1/kT in figure 5.12 for all four dielectric thicknesses, at a field of 12MV/cm (Figure 5.13). The extracted activation energies is about 0.15eV and is found to be independent of film thickness. This indicates that even though H°-R-D is becomes more significant as the physical thickness of the high-κ layer is reduced, the dominating mechanism is still charge detrapping, whose

activation energy is on the order of activation energies reported for charge hopping from trap to trap or diffusion [5].

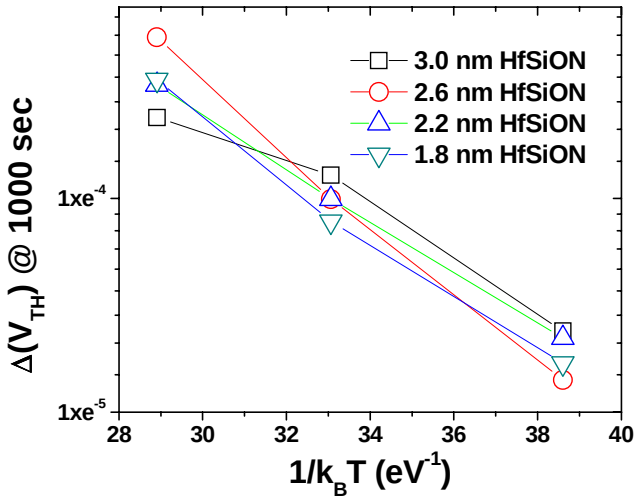


Figure 5.12: The activation energy of ΔV_{TH} is not dependent on the dielectric thickness.

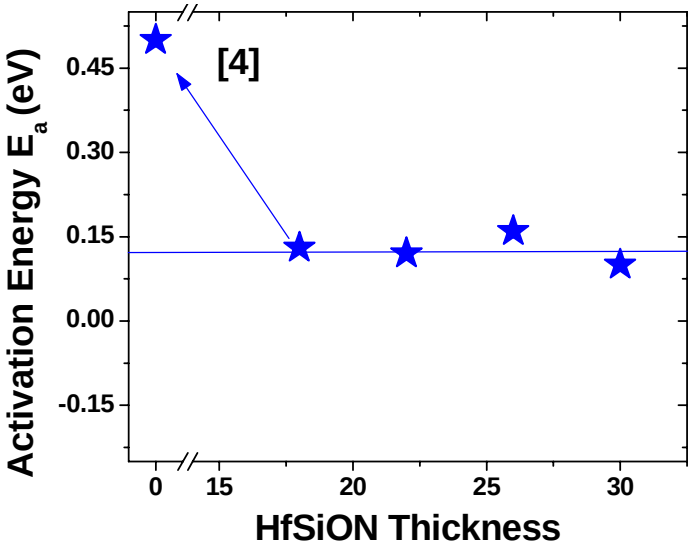


Figure 5.13: The activation energy of threshold voltage shift can is independent of HfSiON thickness and is about 0.15eV.

5.4 Conclusions

NBTI is investigated in gate stacks with HfSiON dielectric of varying thickness. In the preceding chapter, it was reported that the trap density in high-κ gate stacks could be reduced significantly by decreasing the thickness. NBTI in the high-κ dielectrics is found to be a combination of charge detrapping from the bulk and interface trap creation due to Si-H bond breakage due to hole-trapping. The magnitude of threshold voltage is reduced as the physical thickness is reduced, because of reduced charge detrapping from the bulk. However, the creation of interface traps in much more significant in the 1.8 nm film than in the 3.0 nm film, indicating that H°-R-D is more significant in the 1.8 nm film. The power law exponent n is found to collapse towards that of SiO_2 as the thickness of the HfSiON layer is reduced to 1.8 nm. The activation energy of threshold voltage shift is found to be close 0.15eV, indicating that the temperature dependence of V_{TH} shift is dominated by trapping /diffusion mechanism.

5.5 References

1. Chakravarthi S, Krishnan A, Reddy V, Machala CF, Krishnan S: **A comprehensive framework for predictive modeling of negative bias temperature instability**. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual* 273-282.
2. Tsujikawa S, Akamatsu Y, Umeda H, Yugami J: **Two concerns about NBTI issue: gate dielectric scaling and increasing gate current**. In: *Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 28-34.
3. Tsujikawa S, Watanabe K, Tsuchiya R, Ohnishi K, Yugami J: **Experimental evidence for the generation of bulk traps by negative bias temperature stress and their impact on the integrity of direct-tunneling gate dielectrics**. In: *VLSI Technology, 2003 Digest of Technical Papers 2003 Symposium on 2003*; 2003: 139-140.
4. Alam: **Tutorial on NBTI basic modeling**. In: *IRPS: 2005; San Jose, Ca*; 2005.
5. Harris HR, Choi R, Lee BH, Young CD, Sim JH, Mathews K, Zeitzoff P, Majhi P, Bersuker G: **Comparison of NMOS and PMOS stress for determining the source of NBTI TiN/HfSiON devices**. In: *IRPS: 2005; San Jose Ca*; 2005: 80-83.
6. M.A.Quevedo-Lopez: **Thermal stability of hafnium–silicate and plasma-nitrided hafnium silicate films studied by Fourier transform infrared spectroscopy**. *Applied Physics Letters* 2005, **87**(012902):1-3.
7. Smith BC: **Fundamentals of Fourier Transform Infrared Spectroscopy** CRC press; 2000.

8. M.Quevedo-Lopez: **High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements**. In: *International Electron Devices Meeting: 2005; Ca*: IEEE; 2005.

Chapter 6

Effect of Nitrogen Incorporation on PBTI and NBTI in Hafnium Silicate

6.1 Introduction

PBTI and NBTI in high-κ /metal gate gatestacks [1-5] have been shown to be dominated by trapping /detrapping from neutral or charged trap centers. Several reports in the literature have focused on techniques to mitigate the issues associated with charge trapping, like reducing the thickness of the dielectric [6-9] or incorporating nitrogen in the bulk of the dielectric [10-12]. Koyoma et al [11] reported that incorporating nitrogen reduced the increased the crystallization temperature of Hafnium Silicate to temperatures higher than those encountered during the standard CMOS product flow (i.e. Source/Drain Anneal). Gavartin et al [10] and others [13-15] reported that nitrogen passivates oxygen vacancies in the Hafnium based dielectric films. These oxygen vacancies are reported to be the source for charge trapping in the dielectric. A systematic study of the said techniques with particular emphasis on the physical model behind the reduction in charge trapping, however, has not performed. The thickness and nitrogen content dependence of PBTI in ALD HfSiON / TiN gate stacks is investigated. The merits and demerits of nitrogen incorporated through plasma nitridation and thermal nitridation is also explored.

6.2 Sample Fabrication and Experimental Details

6.2.1 Plasma Nitridation:

On HF cleaned wafers, SiON interface is thermally grown. This is followed by deposition of ALD (Atomic Layer Deposition) - Hafnium Silicate (30% SiO_2) of

thickness of 1.8 nm and 2.7 nm. Nitridation is performed in a commercially available plasma nitridation chamber (No post-nitridation Anneal). The N content in the films is controlled by changing the plasma nitridation processing time, while maintaining all the other plasma process conditions constant (pressure, gas composition and power etc.). Nitrogen content in the films are estimated by X-ray Photo-electron Spectroscopy (XPS) [16] to be 4 at%, 8 at%, 12 at% and 16 at% in films of either thickness (1.8 nm or 2.7 nm). The gate electrode, ALD TiN is then deposited and the rest of the CMOS processing is standard, yielding wafers with excellent uniformity across the wafer and good $I_{on} - I_{off}$ characteristics.

6.2.1.1 Electrical Parameters

As expected, increased N content in the film monotonically decreased the Equivalent Oxide Thickness (EOT) of the resulting HfSiON films (Fig. 6.1), while the mobility is only mildly affected (85-98% of universal electron □obility). The mobility of thinner film is higher than that in thicker films, due to higher nitrogen content in the interface layer. In order to assess the percentage of nitrogen in the interface layer, charge pumping measurements are done as a function of frequency. As explained in previous chapters, charge pumping at low frequencies can probe traps up to 1.0 nm (~thickness of interface layer) away from the Si-SiO_x interface [17]. As can be seen in figure 6.2, the thicker dielectric with plasma nitrogen has more trap density than the thinner dielectric with plasma N.

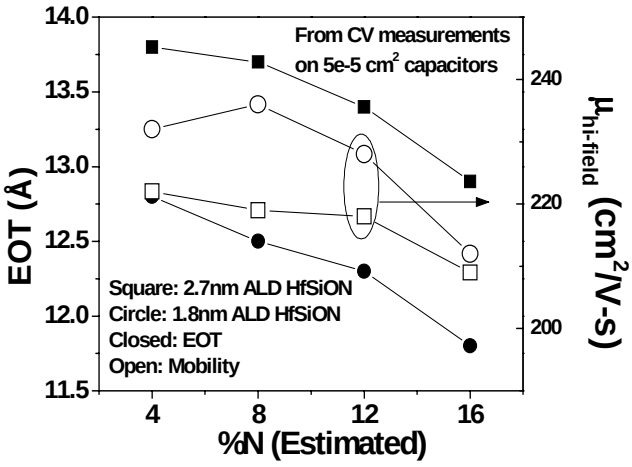


Figure 6.1: EOT and high field mobility at 1MV/cm decrease with N incorporation. 2.7 nm HfSiON has higher EOT and lower mobility.

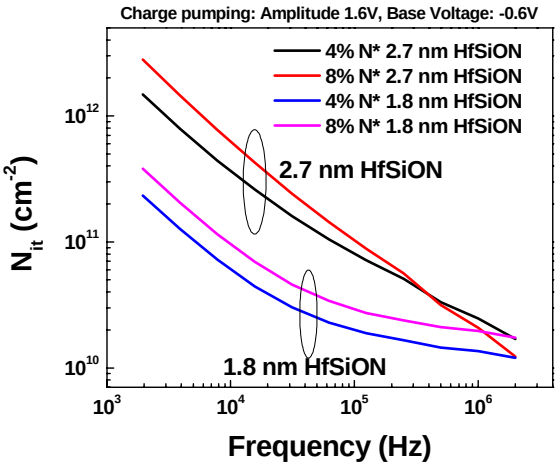


Figure 6.2: N_{it} as a function of charge pumping frequency – 2.7 nm HfSiON has higher trap density than 1.8 nm HfSiON inside the interface layer.

The incorporation of nitrogen in the bulk of the HfSiON films is confirmed by Dynamic Secondary Mass Ion Spectroscopy (DSIMS) [18]. Figure 6.3 shows the

DSIMS profiles showing an increase in Hf-N^+ ion cluster with increase in nitrogen content, in the thick film (same trend is seen in the 1.8 nm HfSiON films, too). The DSIMS measurements are on the device films, by etching through the metal layers and the metal gate. A 0% N reference sample was used, which is annealed in N_2 gas, in order ensure no incorporation of nitrogen, whatsoever.

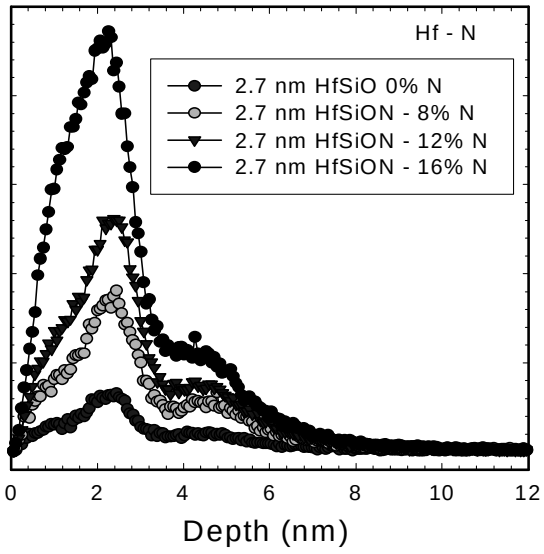


Figure 6.3: DSIMS profile – shows increase in Hf-N^+ clusters with increased nitrogen incorporation, indicating bulk incorporation.

6.2.2 Thermal Nitridation vs. Plasma Nitridation:

For this experiment, similar nitrogen concentrations are incorporated in ALD deposited 1.8 nm HfSiO by plasma nitridation and thermal nitridation in NH_3 ambient. As before, in the plasma nitrided films the N content is increased by increasing the nitridation times, while the N content in the thermally nitrided films is increased by increasing the temperature of the NH_3 anneal (600C, 700C, 800C and 900C). XPS (at

takeoff angle 45°) was performed on blanket films, which go through the exact same thermal budget with as the device wafers to extract the resulting N content in the films.

6.3 Results and Discussion

6.3.1 Plasma Nitridation in ALD HfSiON

In order to determine trap (N_{it}) density in the interface layer, charge pumping measurements are performed as a function of frequency in the different films. As discussed before, at low frequencies, charge pumping measurements can probe up to 1.0 nm away from the interface. The amplitude of the charge pumping measurements is 1.6V and the base voltage is -0.6V. Fig. 6.4 shows the N_{it} variation with frequency for the four nitrogen-bearing films with thickness 1.8 nm and 2.7 nm. The trap density increases monotonically with increase in N content (plasma nitridation times) in both the thicknesses, indicating significant N incorporation in the interface layer.

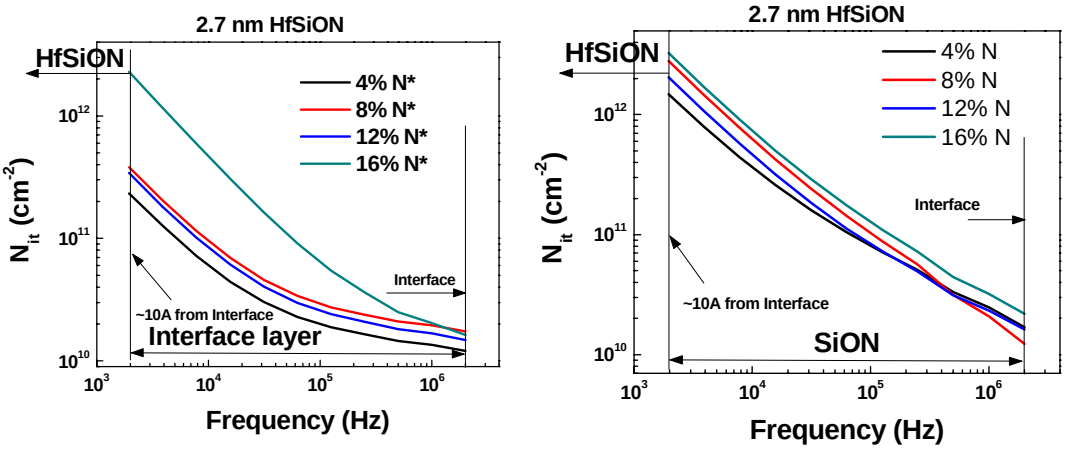


Figure 6.4: Charge pumping as a function of frequency: shows increase nitrogen content in the interface layer with increase in plasma nitridation time in both films.

In order to assess the charge trapping characteristics of the films, PBTI measurements are carried out under Constant Voltage Stress (CVS). The vertical electric field (E_{eff} = (V_g-V_{TH})/EOT) was fixed at 10 MV/cm to fairly compare the samples. The stress is interrupted at various times to measure I_d-V_g characteristics, from which the threshold voltage (V_{TH}) is extracted. There was no peak transconductance (g_m) degradation in any of the samples. Figure 6.5 shows representative g_m curves at different stress times – only shift in threshold is seen, accompanied by no peak transconductance degradation.

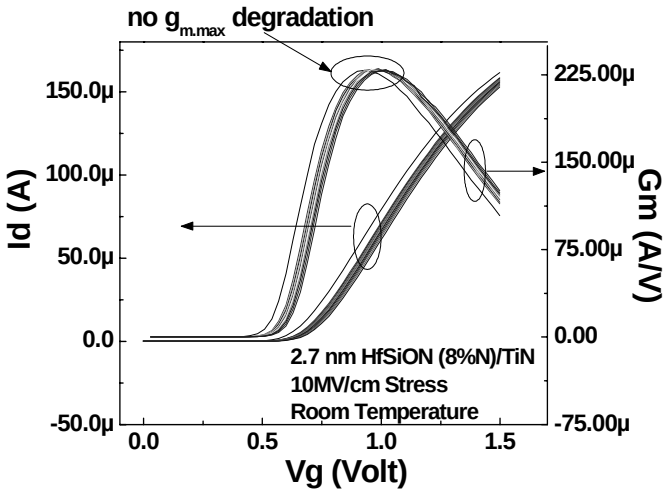


Figure 6.5: I_d-V_g and g_m-V_g curves as shown at different stress times – Only V_{TH} shift seen – No transconductance degradation (representative curve -8% N).

We therefore rule out the possibility that V_{TH} shift during the PBTI measurement could be due to fixed charge creation at the interface. In Fig. 6.6, the V_{TH} shift (ΔV_{TH}) is plotted as a function of time in the 1.8 nm HfSiON films, for different N content. As can be seen,

there is very little V_{TH} shift during the stress (10-15 mV) and there is no dependence on N content in the film.

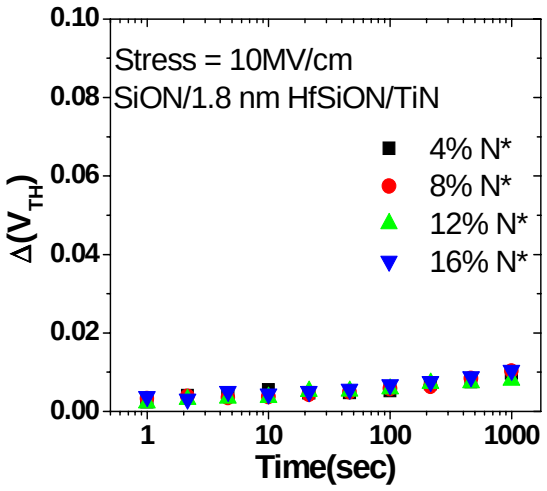


Figure 6.6: ΔV_{TH} vs. time in 1.8nm HfSiON: There is no dependence on nitrogen percentage and the V_{TH} shift is very low (<15mV).

In the thick HfSiON (2.7 nm), however, the V_{TH} shift is much higher than in the thin HfSiON and there is a significant dependence on N content in the film (Fig. 6.7). The ΔV_{TH} seems to reduce monotonically with increasing nitrogen content.

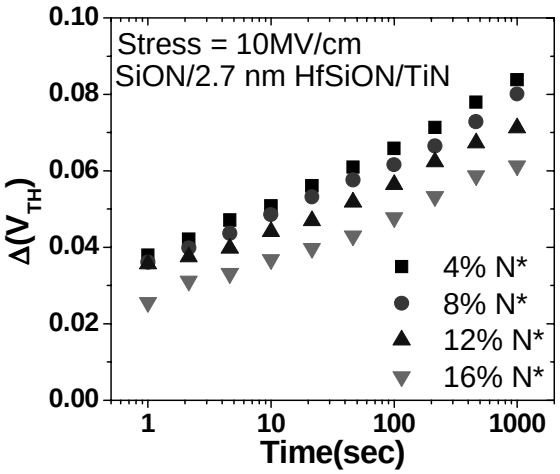


Figure 6.7: ΔV_{TH} vs. time in 2.7nm HfSiON: ΔV_{TH} reduces monotonically with increasing nitrogen content.

The V_{TH} shift at 1,000 sec of stress is plotted as a function of N content for both the 1.8nm films and the 2.7 nm films in Fig. 6.8.

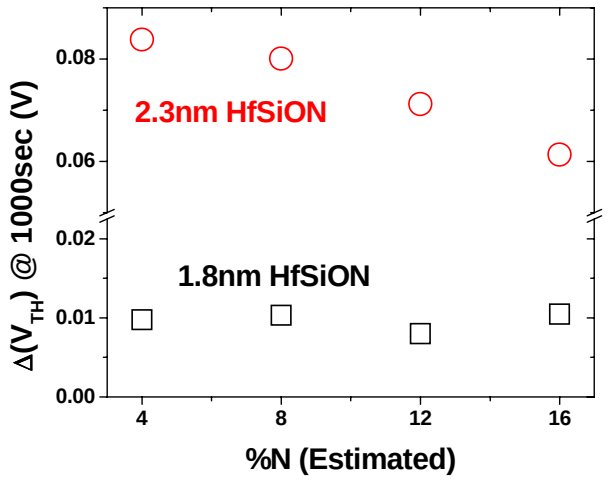


Figure 6.8: ΔV_{TH} at 1000 sec stress vs. %N – Reduces monotonically with N content in thick films, while it is much lower in thin films and independent of N content.

The dependence of threshold voltage shift in thick films agrees well with reported data [10, 13].The primary knob to reduce charge trapping is the film's physical thickness; this dependence may be explained by the reduction in trap density as films are made more amorphous (<2.0 nm). In the thick (2.7 nm) films, N content is a secondary knob to reduce V_{TH} shift. In thin films, the charge trapping is minimal and insensitive to N content. In chapter 4, it was reported that there is a distinct correlation between crystallization and charge trapping in HfSiON films [8, 19]. The degree of crystallinity decreases significantly below physical thickness of 2.0 nm HfSiON, accompanied by significant reduction in charge trap density. The reduction of charge trapping with increase in N content in the thick (2.7 nm) films might be due to passivation of oxygen vacancies (which have suggested as a possible source of charge traps by nitrogen, as discussed earlier. Additionally, nitrogen may also reduce the degree of crystallinity [11], which in turn would reduce the charge trap density. The thin films, which are already amorphous (to the limit of the XRD detection technique) [20, 21], are insensitive to further addition of nitrogen. To further investigate the effect of nitrogen on charge trapping characteristics, PBTI measurements were done at 75°C and 110°C. The V_{TH} shift at 1,000 sec is shown as a function of 1/kT in Fig. 6.9 for the 2.7 nm films.

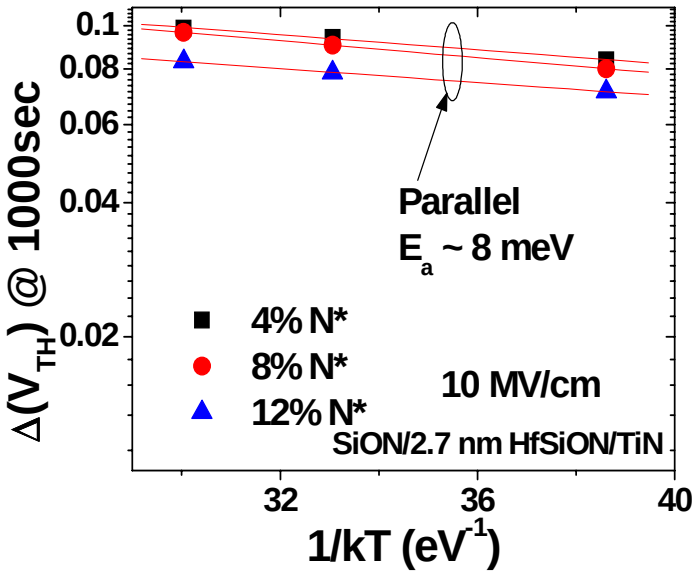


Figure 6.9: ΔV_{TH} at 1000 sec as a function of 1/kT – The temperature dependence is very mild and is independent of the N content, yielding activation energies ~ 8meV.

As explained in chapter 4, the slope of the log-linear plots is indicative of the activation energy for trapped electrons to slowly migrate to other traps along the conduction band over time [22]. Temperature dependence is seen to be mild in the thick films (of the kind seen for diffusion type processes) and the slopes are independent of N content and the activation energy is found to be nearly negligible (8 meV). This suggests that while nitrogen reduces the trap density, it does not change the energy of the trap levels very much. Conversely, for the 1.8 nm films, there is no distinct temperature dependence, due to insufficient number of traps for the electron to migrate to, in the direction of the electric field (Fig. 6.10).

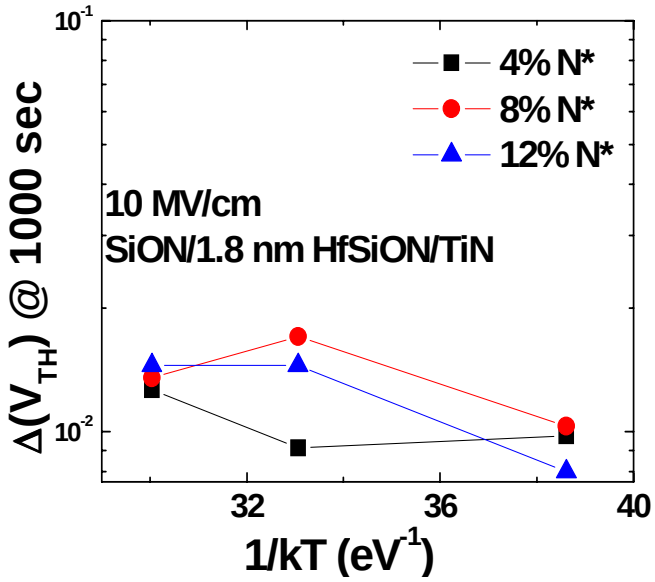


Figure 6.10: ΔV_{TH} @ 1000 sec vs. 1/kT in 1.8 nm films - the ΔV_{TH} in thin films does not have temperature dependence as there is nearly no migration occurring.

6.3.2 Thermal Nitridation and Plasma Nitridation:

For similar N contents, thermal nitridation decreases the EOT of the films more than plasma nitridation does (Fig. 6.11).

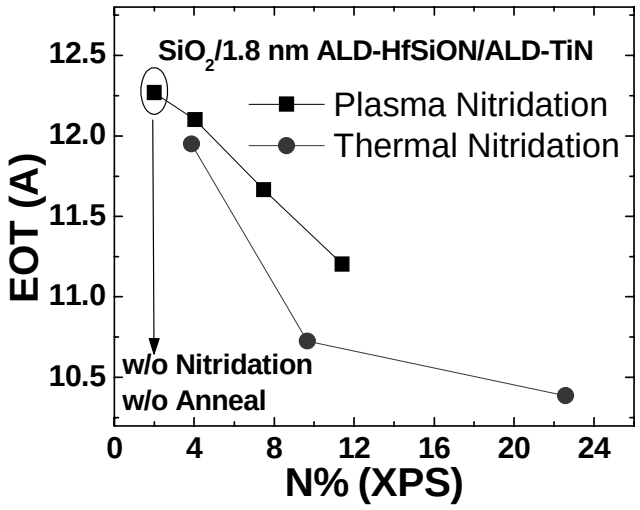


Figure 6.11: EOT vs. %N – The EOTs of Thermally nitrided samples are lower than that of Plasma Nitrided samples, for similar Nitrogen content.

The EOT reduction may be attributed to higher nitrogen content in the interface layer in the thermally nitrided sample than in the plasma nitrided sample, as indicated by the charge pumping measurements (Figure 6.12), in which the N_{it} values at low frequencies are higher for the thermally nitrided samples, compared to the plasma nitrided samples (for 8% nitrogen – the trend is similar for the other nitrogen contents). This indicates that the nitrogen is driven deeper into the interface layer, with aggressive high temperature thermal nitridation process. The nitrogen content in the bulk HfSiON is roughly the same for the two techniques of nitridation.

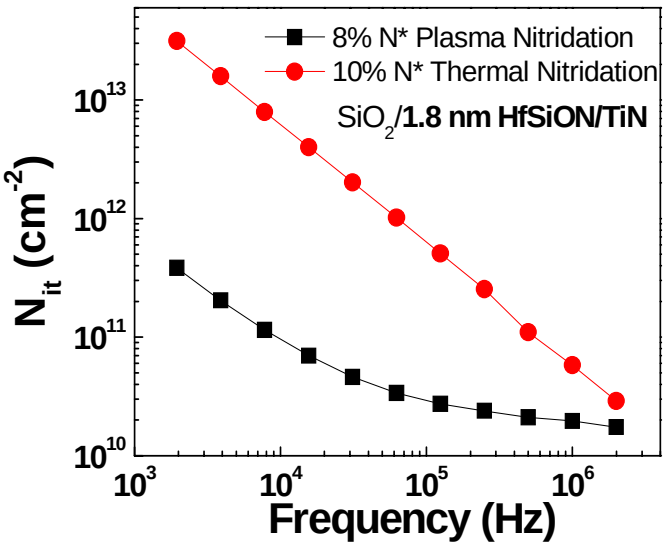


Figure 6.12: N_{it} vs. frequency – Thermally nitrided samples have higher N_{it} at low frequencies.

However, when stressed at 12.3 MV/cm, thermally nitrided samples show higher V_{TH} shift than the plasma nitrided samples (Fig. 6.13). This may be attributed to higher tunneling current through the interface layer in the thermally nitrided samples, due to the lower barrier height for tunneling through the interface layer, which has higher nitrogen content in the thermally nitrided samples. Plasma nitridation allows better control of nitrogen profile across the bulk and the interface layer, while thermal nitridation, due to its intrinsic higher thermal budget drives more nitrogen to the interface layer. These results are contrary to published work that report lower EOTs and better lower leakage current [23]. The caveat associated with the investigation of process techniques is that they need to be optimized minutely before they can be compared for merits and demerits.

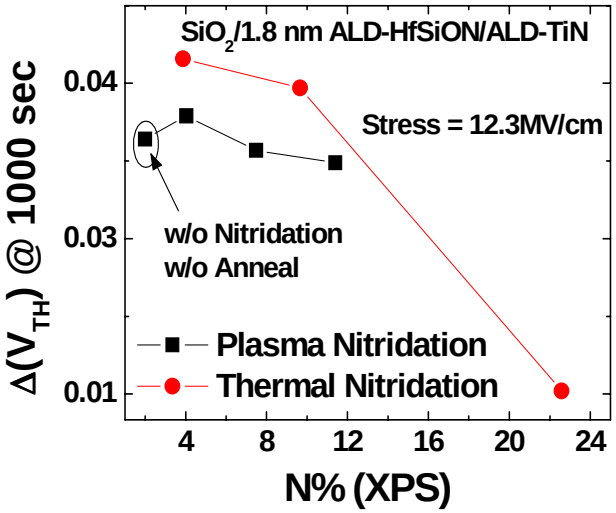


Figure 6.13: ΔV_{TH} vs. %N - ΔV_{TH} at 1000 sec is higher for the thermal nitrided samples than for plasma nitrided samples at similar nitrogen contents.

6.4 NBTI in Plasma Nitrided HfSiON

NBTI in nitrided SiO_2 dielectrics has been reported [24]to be worse than that in non-nitrided SiO_2 dielectrics, due to the presence of nitrogen bonds that can be easily broken by hole injection, apart from the conventional weak hydrogen bonds that contribute to NBTI. NBTI in high-κ dielectrics, however, has been shown to have a dominant trapping component (chapter 5). NBTI measurements are done on 10x1 μm pMOSFETs on devices with 2.7 nm plasma mitrided HfSiON described in the previous sections. Figure 6.14 shows the ΔV_{TH} plots for 4%, 8% and 12% nitrided films. It is evident that NBTI is dominated by the bulk trapping mechanism, because V_{TH} reduces significantly with

addition of nitrogen. Indeed, a similar trend was observed in the PBTI tests, as well, where it was established that nitrogen reduces charge trapping in the bulk.

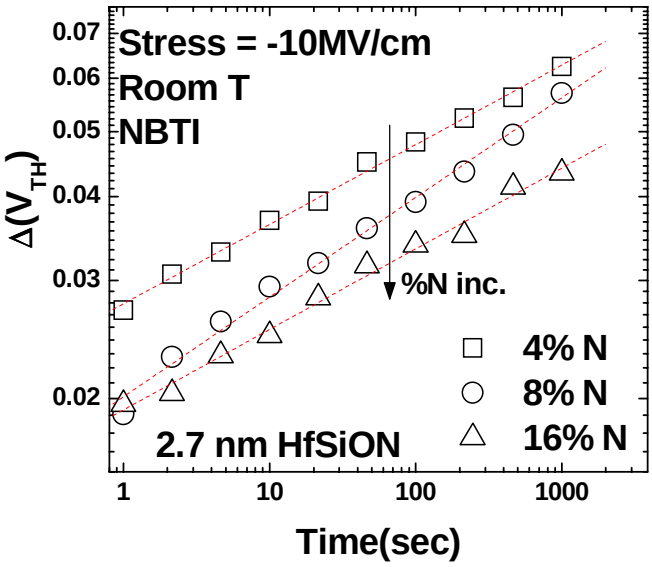


Figure 6.14: ΔV_{TH} vs. Time: At a stress of -10MV/cm, nitrogen incorporation reduces the threshold voltage shift in pMOSFETs.

Measurements were done at room temperature and 100C on the 4% and 16% nitrogen samples. Peak transconductance degradation during the 1000 sec stress is also observed to be less for the nitrogen incorporated samples. However, the rate at which the threshold voltage shifts is more with increased nitrogen. The effect of nitrogen on the bond breakage is not entirely certain.

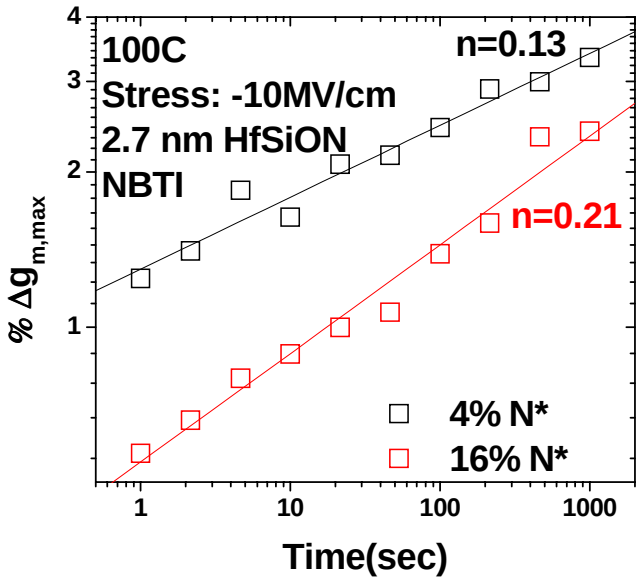


Figure 6.15: Normalized peak transconductance degradation percentage vs. time at different N content – N incorporation reduces the transconductance degradation, also.

6.5 Conclusions

The effect of nitrogen incorporation on PBTI and NBTI in ALD-HfSiON/TiN gate stacks is studied. While thickness of the dielectric is found to be the primary knob to reduce PBTI effects, nitridation further reduces PBTI in thicker films (2.7 nm). The effect of nitridation on PBTI effects on thin films (1.8 nm films) is minimal. The 1.8 nm HfSiON films trap exhibit minimal charge trapping and are therefore insensitive to the presence of nitrogen. Nitrogen could reduce charge trapping in thick films due to:

a) Passivation of oxygen vacancies [10], which are reported to act as charge traps.

b) Disruption of crystallization network in the high-κ layer.

c) A combination of (a) and (b).

The thin films exhibit significantly reduced trapping characteristics due to reduced crystallization (chapter 4).

Thermal nitridation, while reducing the EOTs of the gate stacks more than plasma nitridation (due to more nitrogen incorporation in interface layer), leads to more charge trapping, due to reduction in barrier height for electrons tunneling through the interface layer.

6.6 References

1. Garros X, Leroux C, Reinibold G, Mitard J, Guillaumot B, Martin F, Autran JL: **Reliability assessment of ultra-thin HfO/sub 2/ oxides with TiN gate and polysilicon-n/sup +/ gate**. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International 2004*; 2004: 176-180.
2. Onishi K, Rino C, Chang Seok K, Hag-Ju C, Young Hee K, Nieh RE, Jeong H, Krishnan SA, Akbar MS, Lee JC: **Bias-temperature instabilities of polysilicon gate HfO/sub 2/ MOSFETs**. *Electron Devices, IEEE Transactions on* 2003, **50**(6):1517-1524.
3. Sa N, Kang JF, Yang H, Liu XY, He YD, Han RQ, Ren C, Yu HY, Chan DSH, Kwong DL: **Mechanism of positive-bias temperature instability in sub-1-nm TaN/HfN/HfO/sub 2/ gate stack with low preexisting traps**. *Electron Device Letters, IEEE* 2005, **26**(9):610-612.
4. Shanware A, Visokay MR, Chambers JJ, Rotondaro ALP, Bu H, Bevan MJ, Khamankar R, Aur S, Nicollian PE, McPherson J *et al*: **Evaluation of the positive biased temperature stress stability in HfSiON gate dielectrics**. In: *Physics Symposium Proceedings, 2003 41st Annual 2003 IEEE International 2003*; 2003: 208-213.
5. Xuguang W, Peterson J, Majhi P, Gardner MI, Dim-Lee K: **Impacts of gate electrode materials on threshold voltage (V/sub th/) instability in nMOS HfO/sub 2/ gate stacks under DC and AC stressing**. *Electron Device Letters, IEEE* 2005, **26**(8):553-556.

6. Kirsch PD, J.H.Sim, S.C.Song, Krishnan S, Peterson J, Li H-J, Quevedo-Lopez M, Young CD, R.Choi, N.Moumen *et al*: **Mobility Enhancement of High-k Gate Stacks Through Reduced Transient Charging**. In: *EESDERC: 2005; Grenoble*: IEEE; 2005: 367.
7. Krishnan SA, Peterson JJ, Young CD, Brown G, Choi R, Harris R, Sim JH, Zeitzoff P, Kirsch P, Gutt J *et al*: **Dominant SILC mechanisms in HFO/sub 2/TiN gate nMOS and pMOS transistors**. In: *International Reliability Physics Symposium: 2005; Ca*; 2005: 642-643.
8. Quevedo-Lopez MA, Krishnan SA, Kirsch PD, Li HJ, Sim JH, Huffman C, Peterson JJ, Lee BH, Pant G, Gnade BE *et al*: **High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements**. *accepted IEDM Tech Dig* 2005.
9. Sim JH, Song SC, Kirsch PD, Young CD, Choi R, Kwong DL, Lee BH, Bersuker G: **Effects of ALD HfO2 Thickness on Charge Trapping and Mobility**. In: *INFOS: 2005*; 2005.
10. J. L. Gavartin ALS, A. S. Foster and G. I. Bersuker: **The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies**. *Journal of Applied Physics* 2005, **97**:13.
11. Koyama M, Kaneko A, Ino T, Koike M, Kamata Y, Iijima R, Kamimuta Y, Takashima A, Suzuki M, Hongo C *et al*: **Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics**. In: *IEDM Tech Dig: 2002*; 2002: 849-852.

12. Koyama M, Satake H, Koike M, Ino T, Suzuki M, Iijima R, Kamimuta Y, Takashima A, Hongo C, Nishiyama A: **Degradation mechanism of HfSiON gate insulator and effect of nitrogen composition on the statistical distribution of the breakdown**. In: *VLSI Symp: 2003*; 2003: 38.34.31-38.34.34.
13. Naoto Umezawa KS, Kazuyoshi Torii, Mauro Boero, Toyohiro Chikyow, Heiji Watanabe, Kikuo Yamabe, Takahisa Ohno, Keisaku Yamada, and Yasuo Nara: **The Role of Nitrogen Incorporation in Hf-based High-k Dielectrics: Reduction in Electron Charge Traps**. In: *ESSDERC: 2005; Grenoble, France*; 2005: 201.
14. Nobuyuki Ikarashi MM, Koji Masuzaki, and Toru Tatsumi: **Electron energy-loss spectroscopy analysis of the electronic structure of nitrided Hf silicate films**. *APPLIED PHYSICS LETTERS* 2004, **84**(18).
15. Robertson J, Ka X, Falabretti B: **Point defects in ZrO/sub 2/ high-/spl kappa/ gate oxide**. *Device and Materials Reliability, IEEE Transactions on* 2005, **5**(1):84-89.
16. Carlson TA: **X-Ray Photoelectron Spectroscopy** Academic Press 1978.
17. Bauza D: **Extraction of Si-SiO2 Interface Trap Densities in MOSFET's with Oxides Down to 1.3 nm Thick**. In: *Solid-State Device Research Conference, 2002 Proceeding of the 32nd European: 24-26 September 2002 2002*; 2002: 231-234.
18. Quevedo-Lopez M: **Material Properties of Hafnium and Zirconium Silicate**. Denton: University of North Texas; 2003.
19. Siddarth Krishnan MQ-L, Rino Choi, Paul Kirsch, Chadwin Young, Rusty Harris,, Jeff Peterson H-JL, Byoung Hun Lee and Jack Lee: **Charge Trapping Dependence on the Physical Structure of Ultra-thin ALDHfSiON/TiN Gate Stacks**. In:

International Integrated Reliability Workshop (IIRW): 2005; Lake Tahoe, Ca: IEEE; 2005.

20. Frank Chung DS: **Industrial Applications of X-Ray Diffraction** Marcel Dekker 1999.
21. Rigarku **Ultima III XRD**
22. Bersuker G: **Novel dielectric materials for future transistor generations**. In*: 2005*; 2005: 10-10.
23. Sekine K, Inumiya S, Sato M, Kaneko A, Eguchi K, Tsunashima Y: **Nitrogen profile control by plasma nitridation technique for poly-Si gate HfSiON CMOSFET with excellent interface property and ultra-low leakage current**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International Dec., 2003 2003*: IEEE; 2003: 4.6.1-4.6.4.
24. Kimizuka N, Yamaguchi K, Imai K, Iizuka T, Liu CT, Keller RC, Horiuchi T: **NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10-μm gate CMOS generation**. In: *VLSI Technology, 2000 Digest of Technical Papers 2000 Symposium on 13-15 June 2000 2000*; 2000: 92-93.

Chapter 7

Conclusion

7.1 Summary and Conclusions

This dissertation has largely dealt with issues thought to be intrinsic to high-κ dielectric materials for gate oxide applications. We have demonstrated a hafnium silicon oxynitride / titanium nitride solution that is nearly trap-free and exhibits intrinsic carrier (electron and hole) mobility that is over 90% of the universal channel mobility, at an Equivalent Oxide Thickness of 10.7Å. The threshold voltage instability has been shown to have an exponential dependence on physical thickness of HfSiON (with approximately 30% SiO_2). The physical thickness at which the threshold voltage instability starts increasing significantly is shown to be very close to the thickness at which the crystallization of the dielectric starts to occur. The dependence of the crystallization of the material is speculated to follow avrami's equation, which avrami published in 1939. An equation was derived (after making simplifying but not far-fetched assumptions) expressing the threshold voltage instability as a function of time, where it was shown that threshold voltage instability (ΔV_{TH}) followed a 2^{nd} order exponential dependence on time. The data fit with $R^2 > 99.4\%$ with the theoretical curve predicted by this equation.

Mobility degradation studies were undertaken on samples with varying interface thickness and a constant high-κ thickness. It was shown that the electron mobility of 3.0 nm HfO_2 devices could be improved significantly to over 80% of the universal channel mobility, with an interface thickness of 1.6 nm. This mobility improvement comes at the

cost of EOT, though. The mobility degradation in these thick HfO_2 layers was shown to have components of coulomb scattering, remote phonon scattering and soft optical phonon scattering, with the phonon scattering component dominating at high fields. The electron mobility of HfO_2 based gate stacks could be increased to over 85% universal channel mobility without compromising the EOTs by decreasing the thickness of the HfO_2 layer down to less than 2.0 nm.

Nitrogen incorporation was also investigated with respect to charge trapping in HfSiON dielectrics. In relatively thick HfSiON (2.7 nm), charge-trapping-induced positive bias temperature instability was shown to reduce with increase in nitrogen content in the film. In thin HfSiON, however, PBTI was shown to be independent of nitrogen content. It was postulated that the thin dielectrics were amorphous, due to which the trap density was already significantly low and nitrogen, therefore, has little effect, if any. In thick HfSiON, the nitrogen might decrease the degree of crystallization and/or passivate possible trap centers, like neutral or charged oxygen vacancies. V_{TH} instability in thick HfSiON increased with temperature with a mild activation energy of 8 meV, from which it can be conjectured that temperature dependent process is electron hopping from trap to trap in the direction of the electric field. The dependence on temperature is not changed in any significant way by the presence of nitrogen in the film. In the thin films, however, there is no discernable temperature dependence of V_{TH} instability, indicating the lacking of hopping like processes. It is likely that the trap density in the direction of the electric field is not inadequate for efficient hopping mechanisms to occur. Negative bias temperature instability was also investigated in these gate stacks and it was

shown that the threshold voltage shift after 1000 seconds of stress during NBTI decreased with increase in nitrogen content, while the rate of the threshold voltage shift seemed to increase. Ammonia nitridation was shown to be less efficient at reducing charge trapping than plasma nitridation, where, it was shown that better control of the nitrogen profile is possible (nitrogen distributed between dielectric and interface).

Negative Bias Temperature Instability in HfSiON was shown to be a combination of charge trapping/detrapping and interface Si-H bond breakage processes. In thick films (T_{phy} > 3.0 nm), the trapping/detrapping is dominant and leads to negative threshold voltage shifts in excess of 45mV, while in thin films (T_{phy} < 2.0 nm), both the processes exist and the interface degradation is shown to be distinctly electric field and temperature dependent. The activation energy of NBTI was observed to be independent of dielectric thickness and close to 0.15 eV.

7.2 Suggestions for Future Work

7.2.1 Metal Gates

Despite the intense investigation of metal gates on high-κ dielectrics, a clear solution eludes the semiconductor industry. Metal gates with appropriate nMOS and pMOS effective work functions have not been identified, yet. A "barrier" dielectric, that could modify the dipoles at the top interface with the metal gate, could be used to modify the effective work function.

7.2.2 "Higher-κ" Dielectrics

As the various issues associated with hafnium based dielectric continue to be resolved, the 45 nm and 22nm technology nodes need to looked at more intensively. As the EOT

requirements in these nodes are more stringent, in order to maintain high capacitance values of the gate dielectrics, higher-κ dielectrics may need to be introduced. To this end, various new materials are being investigated. A systematic study of the of the oxides of lanthanide materials like La, Pr, Ce, Gd, Dy, Er, Yb etc. could yield a material with appropriate properties. The traditionally investigated metal oxides of Titanium, Tantalum, Zirconium and Scandium also need to be investigated thoroughly.

7.2.3 High-κ and Higher-κ materials on high mobility substrates

High mobility substrates, like Silicon-Germanium, Germanium and Gallium-Arsenide offer yet another way to increase the drain current in MOSFETs. There is no consensus on the choice of a dielectric that is chemically and mechanically compatible with such high-mobility substrates. Hafnium based dielectrics, which are on the verge of introduction into the convetional silicon product flow, need to be investigated for compatibility with such high mobility substrates. Various surface preparation techniques, barrier materials and dielectric deposition techniques need to be investigated with high mobility substrates.

Bibiography

International Technology Roadmap for Semiconductors

Intel: **Craig Barret's Keynote speech on IDF**. In: *www.anandtech.com.* 2005.

Wolf S: **Silicon Processing for the VLSI era**, vol. 2: Lattice Press; 1990.

Hori T: **Gate Dielectrics and MOS ULSIs**. Berlin: Springer-Verlag 1997.

B. Streetman SB: **Solid State Electronic Devices**: Prentice Hall; 2001.

Technology Scaling

A. Chandrakasan WB, and F. Fox: **Design of High-Performance Microprocessor Circuits**: IEEE press; 2001.

N.S. Kim TA, D. Blaauw, T. Mudge, K. Flautner, J.S. Hu, M.J. Irwin, M. Kandemir, and V. Narayanan: **Leakage Current: Moore's law meets static power**. *computer* 2003, **36**(12).

S.-H. Lo DAB, Y. Taur, and W. Wang: **Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thinoxide nMOSFET's**. *IEEE Trans Electron Devices* 1997, **18**:209-211.

DiMaria: **Reliability projection for ultra-thin oxides at low voltage**. *IEDM Tech Dig* 1998:167-170.

T.-S. Chen DH, V. Valu, V. Jiang, S.-H. Kuah, P. C. McIntyre, S. R., Summerfelt JMA, and J. C. Lee: **Ir-electroded BST thin film capacitors for 1 giga-bit DRAM application**. *IEDM Tech Dig* 1996:797-800.

Robertson J: **Band offsets of wide-band-gap oxides and implications for future electronic devices**. *Journal of Vaccuum Society B* 2000, **18**:1785.

Scott JF: **High-Dielectric Constant Thin Films for Dynamic Random Access Memories**. *Annual Review of Materials Science* 1998.

D. Park Y-CK, Q. Lu, T.-J. King, C. Hu, A. Kalnitsky, S.-P. Tay, and, Cheng C-C: **Transistor characteristics with Ta2O5 gate dielectric**. *IEEE*

Electron Device Lett 1998, **19**:441-443.

M. Saito MY, K. Asaka, H. Goto, N. Fukuda, M. Kawano, M. Kojima, M. Suzuki, K. Ogaya, H. Enomoto, K. Hotta, S. Sakai, H. Asakura,, T. Fukuda TS, T. Takakura, and N. Kobayashi: **Advanced thermally stable silicide S/D electrodes for high-speed logic circuits with large-scale embedded Ta2O5-capacitor DRAMs**. *IEDM Tech Dig* 1999:805-808.

P. K. Roy and I. C. Kizilyalli: **Stacked high-ε gate dielectric for gigascale integration of metal–oxide–semiconductor technologies**. *Appl Phys Lett* 1998, **72**:2835-2837.

Campbell SA, Gilmer DC, Xiao-Chuan W, Ming-Ta H, Hyeon-Seag K, Gladfelter WL, Jinhua Y: **MOSFET transistors fabricated with high permitivity TiO₂ dielectrics**. *Electron Devices, IEEE Transactions on* 1997, **44**(1):104-109.

Lee BH: **Technology Development and process integration of alternative gate dielectric material; Hafnium Oxide**. *Dissertation.* Austin: The University of Texas; 2001.

Qi W-J: **Study on high-k dielectrics as alternative gate insulators for 0.1 micron and beyond ULSI applications**. Austin: The University of Texas; 2000.

Onishi K, Chang Seok K, Rino C, Hag-Ju C, Gopalan S, Nieh R, Krishnan S, Lee JC: **Effects of high-temperature forming gas anneal on HfO/sub 2/ MOSFET performance**. In: *VLSI Symposium: 2002*; 2002: 22-23.

Rino C, Onishi K, Chang Scok K, Renee N, Gopalan S, Hag-Ju C, Krishnan S, Lee JC: **High quality MOSFETs fabrication with HfO/sub 2/ gate dielectric and tan gate electrode**. In: *Device Research Conference, 2002 60th DRC Conference Digest: 2002*: IEEE; 2002: 193-194.

Nieh R, Krishnan S, Hag-Ju C, Chang Seok K, Gopalan S, Onishi K, Choi R, Lee JC: **Comparison between ultra-thin ZrO/sub 2/ and ZrO/sub x/N/sub y/ gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices**. In: *VLSI Symposium: 2002*; 2002: 186-187.

Wong CY, Sun JY, Taur Y, Oh CS, Angelucci R, Davari B: **Doping of n⁺ and p⁺ polysilicon in a dual-gate CMOS process**. In: *Electron Devices Meeting, 1988 Technical Digest, International 1988*; 1988: 238-241.

Onishi K, Kang L, Choi R, Dharmarajan E, Gopalan S, Yongjoo J, Chang Seok K, Byoung Hun L, Nieh R, Lee JC: **Dopant penetration effects on polysilicon gate HfO₂ MOSFET's**. In: *VLSI Technology, 2001 Digest of Technical Papers 2001 Symposium on 2001*; 2001: 131-132.

Ching-Huang L, Wong GMT, Deal MD, Tsai W, Majhi P, Chi On C, Visokay MR, Chambers JJ, Colombo L, Clemens BM *et al*: **Characteristics and mechanism of tunable work function gate electrodes using a bilayer metal structure on SiO/sub 2/ and HfO/sub 2**. *Electron Device Letters, IEEE* 2005, **26**(7):445-447.

Narayanan V, Callegari A, McFeely FR, Nakamura K, Jamison P, Zafar S, Cartier E, Steegen A, Ku V, Nguyen P *et al*: **Dual work function metal gate CMOS using CVD metal electrodes**. In: *VLSI Technology, 2004 Digest of Technical Papers 2004 Symposium on 2004*: IEEE; 2004: 192-193.

Majhi P, Young C, Bersuker G, Wen HC, Brown GA, Foran B, Choi R, Zeitzoff PM, Huff HR: **Influence of metal gate materials and processing on planar CMOS device characteristics with high-k gate dielectrics**. In: *Solid-State Device Research conference, 2004 ESSDERC 2004 Proceeding of the 34th European: 2004*; 2004: 185-188.

Qiang L, Lin R, Ranade P, Tsu-Jae K, Chenming H: **Metal gate work function adjustment for future CMOS technology**. In: *VLSI Technology, 2001 Digest of Technical Papers 2001 Symposium on 2001*; 2001: 45-46.

Kang JF, Yu HY, Ren C, Wang XP, Li MF, Chan DSH, Liu XY, Han RQ, Wang YY, Kwong DL: **Characteristics of sub-1 nm CVD HfO/sub 2/ gate dielectrics with HfN electrodes for advanced CMOS applications**. In: *Solid-State and Integrated Circuits Technology, 2004 Proceedings 7th International Conference on 2004*; 2004: 393-398 vol.391.

Chang Seo P, Byung Jin C, Dim-Lee K: **Thermally stable fully silicided Hf-silicide metal-gate electrode**. *Electron Device Letters, IEEE* 2004, **25**(6):372-374.

Schaeffer JK, Capasso C, Fonseca LRC, Samavedam S, Gilmer DC, Liang Y, Kalpat S, Adetutu B, Tseng HH, Shiho Y *et al*: **Challenges for the integration of metal gate electrodes**. In: *Electron Devices Meeting, 2004 IEDM Technical Digest IEEE International 2004*; 2004: 287-290.

Samavedam SB, La LB, Smith J, Dakshina-Murthy S, Luckowski E, Schaeffer J, Zavala M, Martin R, Dhandapani V, Triyoso D *et al*: **Dual-metal gate CMOS with HfO/sub 2/ gate dielectric**. In: *Electron Devices Meeting, 2002 IEDM '02 Digest International 2002*; 2002: 433-436.

Hong-Jyh Li, Gardner MI: **Dual high-/spl kappa/ gate dielectric with poly gate electrode: HfSiON on nMOS and Al/sub 2/O/sub 3/ capping layer on pMOS**. *Electron Device Letters, IEEE* 2005, **26**(7):441-444.

Weber O, Andrieu F, Casse M, Ernst T, Mitard J, Ducroquet F, Damlencourt JF, Hartmann JM, Lafond D, Papon AM *et al*: **Experimental determination of mobility scattering mechanisms in Si/HfO/sub 2//TiN and SiGe:C/HfO/sub 2//TiN surface channel n- and p-MOSFETs**. In: *Electron Devices Meeting, 2004 IEDM Technical Digest IEEE International 2004*; 2004: 867-870.

Zhu WJ, Ma TP: **Temperature dependence of channel mobility in HfO/sub 2/-gated NMOSFETs**. *Electron Device Letters, IEEE* 2004, **25**(2):89-91.

Chau R, Datta S, Doczy M, Doyle B, Kavalieros J, Metz M: **High-/spl kappa//metal-gate stack and its MOSFET characteristics**. *Electron Device Letters, IEEE* 2004, **25**(6):408-410.

Ren Z, Fischetti MV, Gusev EP, Cartier EA, Chudzik M: **Inversion channel mobility in high-/spl kappa/ high performance MOSFETs**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International 2003*; 2003: 33.32.31-33.32.34.

Kerber A, Cartier E, Ragnarsson LA, Rosmeulen M, Pantisano L, Degraeve R, Kim Y, Groeseneken G: **Direct measurement of the inversion charge in MOSFETs:**

application to mobility extraction in alternative gate dielectrics. In: *VLSI Technology, 2003 Digest of Technical Papers 2003 Symposium on 2003*; 2003: 159-160.

Young CD, Bersuker G, Brown GA, Lysaght P, Zeitzoff P, Murto RW, Huff HR: **Charge trapping and device performance degradation in MOCVD hafnium-based gate dielectric stack structures**. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 597-598.

Onishi K, Rino C, Chang Seok K, Hag-Ju C, Young Hee K, Nieh RE, Jeong H, Krishnan SA, Akbar MS, Lee JC: **Bias-temperature instabilities of polysilicon gate HfO/sub 2/ MOSFETs**. *Electron Devices, IEEE Transactions on* 2003, **50**(6):1517-1524.

Sa N, Kang JF, Yang H, Liu XY, He YD, Han RQ, Ren C, Yu HY, Chan DSH, Kwong DL: **Mechanism of positive-bias temperature instability in sub-1-nm TaN/HfN/HfO/sub 2/ gate stack with low preexisting traps**. *Electron Device Letters, IEEE* 2005, **26**(9):610-612.

Shanware A, Visokay MR, Chambers JJ, Rotondaro ALP, Bu H, Bevan MJ, Khamankar R, Aur S, Nicollian PE, McPherson J *et al*: **Evaluation of the positive biased temperature stress stability in HfSiON gate dielectrics**. In: *Physics Symposium Proceedings, 2003 41st Annual 2003 IEEE International 2003*; 2003: 208-213.

J. L. Gavartin ALS, A. S. Foster and G. I. Bersuker: **The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies**. *JOURNAL OF APPLIED PHYSICS* 2005, **97**:13.

Nobuyuki Ikarashi MM, Koji Masuzaki, and Toru Tatsumi: **Electron energy-loss spectroscopy analysis of the electronic structureof nitrided Hf silicate films**. *APPLIED PHYSICS LETTERS* 2004, **84**(18).

Xuguang W, Peterson J, Majhi P, Gardner MI, Dim-Lee K: **Impacts of gate electrode materials on threshold voltage (V/sub th/) instability in nMOS HfO/sub 2/ gate stacks under DC and AC stressing**. *Electron Device Letters, IEEE* 2005, **26**(8):553-556.

46.

Alam MA: **A critical examination of the mechanics of dynamic NBTI for PMOSFETs**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International 2003*; 2003: 14.14.11-14.14.14.

Harris HR, Choi R, Lee BH, Young CD, Sim JH, Mathews K, Zeitzoff P, Majhi P, Bersuker G: **Comparison of NMOS and PMOS stress for determining the source of NBTI TiN/HfSiON devices**. In: *Reliability Physics Symposium, 2005 Proceedings 43rd Annual 2005 IEEE International: 2005*; 2005: 80-83.

Sungjoo L, Kwong DL: **TDDB and polarity-dependent reliability of high-quality, ultrathin CVD HfO/sub 2/ gate stack with TaN gate electrode**. *Electron Device Letters, IEEE* 2004, **25**(1):13-15.

Young Hee K, Onishi K, Chang Seok K, Hag-Ju C, Rino C, Krishnan S, Akbar MS, Lee JC: **Thickness dependence of Weibull slopes of HfO/sub 2/ gate dielectrics**. *Electron Device Letters, IEEE* 2003, **24**(1):40-42.

Kauerauf T, Degraeve R, Zahid MB, Cho M, Kaczer B, Roussel P, Groeseneken G, Maes H, De Gendt S: **Abrupt breakdown in dielectric/metal gate stacks: a potential reliability limitation?** *Electron Device Letters, IEEE* 2005, **26**(10):773-775.

Young Hee K, Onishi K, Chang Seok K, Hag-Ju C, Nieh R, Gopalan S, Choi R, Jeong H, Krishnan S, Lee JC: **Area dependence of TDDB characteristics for HfO/sub 2/ gate dielectrics**. *Electron Device Letters, IEEE* 2002, **23**(10):594-596.

Crupi F, Degraeve R, Kerber A, Kwak DH, Groeseneken G: **Correlation between Stress-Induced Leakage Current (SILC) and the HfO/sub 2/ bulk trap density in a SiO/sub 2//HfO/sub 2/ stack**. In: *Reliability Physics Symposium, 2004 Proceedings 42nd Annual 2004 IEEE International 2004*; 2004: 181-187.

Garros X, Leroux C, Reinibold G, Mitard J, Guillaumot B, Martin F, Autran JL: **Reliability assessment of ultra-thin HfO/sub 2/ oxides with TiN gate and polysilicon-n/sup +/ gate**. In*: 2004*; 2004: 176-180.

Ernest W. Yu JS: **Ultra-Thin Oxide Reliability**. In: *Reliability Physics Symposium, 2005 Proceedings 43rd Annual 2005 IEEE International* San Jose, Ca: IEEE; 2005.

Sze SM: **physics of semiconductor devices**, 2 edn. New Jersey: John Wiley and sonds; 1999.

Young CD, Bersuker G, Brown GA, Lysaght P, Zeitzoff P, Murto RW, Huff HR: **Charge trapping and device performance degradation in MOCVD hafnium-based gate dielectric stack structures**. In*: 2004*; 2004: 597-598.

Kerber A, Cartier E, Ragnarsson LA, Rosmeulen M, Pantisano L, Degraeve R, Kim Y, Groeseneken G: **Direct measurement of the inversion charge in MOSFETs:**

application to mobility extraction in alternative gate dielectrics. In*: 2003*; 2003: 159-160.

Mizubayashi W, Yasuda N, Ota H, Hisamatsu H, Tominaga K, Iwamoto K, Yamamoto K, Horikawa T, Nabatame T, Toriumi A: **Carrier separation analysis for clarifying leakage mechanism in unstressed and stressed HfAlO/sub x//SiO/sub 2/ stack dielectric layers**. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 188-193.

Lime F, Ghibaudo G, Guillaumot B: **Investigation of electron and hole mobilities in MOSFETs with TiN/HfO/sub 2//SiO/sub 2/ gate stack**. In: *European Solid-State Device Research, 2003 ESSDERC '03 33rd Conference on: 2003*; 2003: 247-250.

Kerber A, Cartier E, Ragnarsson LA, Rosmeulen M, Pantisano L, Degraeve R, Kim Y, Groeseneken G: **Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics**. In: *VLSI Technology, 2003 Digest of Technical Papers 2003 Symposium on 2003*; 2003: 159-160.

Chau R, Datta S, Doczy M, Doyle B, Kavalieros J, Metz M: **High-/spl kappa//metal-gate stack and its MOSFET characteristics**. *Electron Device Letters, IEEE* 2004, **25**(6):408-410.

Wu WH, Chen MC, Wang MF, Hou TH, Yao LG, Jin Y, Chen SC, Liang MS: **Effects of base oxide in HfSiO/SiO/sub 2/ high-k gate stacks**. In: *Physical and Failure Analysis of Integrated Circuits, 2004 IPFA 2004 Proceedings of the 11th International Symposium on the 2004*; 2004: 25-28.

Takagi S, Toriumi A, Iwase M, Tango H: **On the universality of inversion layer mobility in Si MOSFET's: Part II-effects of surface orientation**. *Electron Devices, IEEE Transactions on* 1994, **41**(12):2363-2368.

Massimo V. Fischetti DAN, and Eduard A. Cartier **Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high- insulator: The role of remote phonon scattering** *Journal of Applied Physics* 2001, **90**(9):4587.

9.

Watling JR, Lianfeng Y, Asenov A, Barker JR, Roy S: **Impact of high-/spl kappa/ dielectric HfO/sub 2/ on the mobility and device performance of sub-100-nm nMOSFETs**. *Device and Materials Reliability, IEEE Transactions on* 2005, **5**(1):103-108.

10.

Kirsch PD, J.H.Sim, S.C.Song, Krishnan S, Peterson J, Li H-J, Quevedo-Lopez M, Young CD, R.Choi, N.Moumen *et al*: **Mobility Enhancement of High-k Gate Stacks Through Reduced Transient Charging**. In: *EESDERC: 2005; Grenoble*: IEEE; 2005.

Byoung Hun L, Rino C, Sim JH, Krishnan SA, Peterson JJ, Brown GA, Bersuker G: **Validity of constant voltage stress based reliability assessment of high-/spl kappa/ devices**. *Device and Materials Reliability, IEEE Transactions on* 2005, **5**(1):20-25.

2.

Ribes G, Muller M, Bruyere S, Roy D, Denais M, Huard V, Skotnicki T, Ghibaudo G: **Characterization of Vt instability in hafnium based dielectrics by pulse gate voltage techniques [CMOS device applications]**. In: *Solid-State Device Research conference, 2004 ESSDERC 2004 Proceeding of the 34th European: 2004*; 2004: 89-92.

Koyama M, Satake H, Koike M, Ino T, Suzuki M, Iijima R, Kamimuta Y, Takashima A, Hongo C, Nishiyama A: **Degradation mechanism of HfSiON gate insulator and effect of nitrogen composition on the statistical distribution of the breakdown**. In: *VLSI Symp: 2003*; 2003: 38.34.31-38.34.34.

Koike M, Ino T, Kamimuta Y, Koyama M, Kamata Y, Suzuki M, Mitani Y, Nishiyama A, Tsunashima Y: **Effect of Hf-N bond on properties of thermally stable amorphous HfSiON and applicability of this material to sub-50nm technology node LSIs**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International: 2003*; 2003: 4.7.1-4.7.4.

Koyama M, Kaneko A, Ino T, Koike M, Kamata Y, Iijima R, Kamimuta Y, Takashima A, Suzuki M, Hongo C *et al*: **Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics**. In: *IEDM Tech Dig: 2002*; 2002: 849-852.

M.Quevedo-Lopez: **High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements**. In: *International Electron Devices Meeting: 2005; Ca*: IEEE; 2005.

Hori T: **Gate Dielectrics and MOS ULSIs**. Berlin: Springer-Verlag; 1997.

Bersuker G: **Novel dielectric materials for future transistor generations**. In*: 2005*; 2005: 10-10.

Wolf S: **Silicon Processing for the VLSI era**, vol. 2: Lattice Press; 1990.

M.Avrami: *Journal of chemistry and physics* 1939, **7**:1103.

Robertson J, Ka X, Falabretti B: **Point defects in ZrO/sub 2/ high-/spl kappa/ gate oxide**. *Device and Materials Reliability, IEEE Transactions on* 2005, **5**(1):84-89.

Chaparala P, Suehle JS, Messick C, Roush M: **Electric field dependent dielectric breakdown of intrinsic SiO₂ films under dynamic stress**. In: *Reliability Physics Symposium, 1996 34th Annual Proceedings, IEEE International: 1996*; 1996: 61-66.

Hokari Y, Baba T, Kawamura N: **Reliability of 6-10 nm thermal SiO<inf>2</inf>films showing intrinsic dielectric integrity**. *Electron Devices, IEEE Transactions on* 1985, **32**(11):2485-2491.

Suehle JS, Chaparala P, Messick C, Miller WM, Boyko KC: **Field and temperature acceleration of time-dependent dielectric breakdown in intrinsic thin SiO₂**. In: *Reliability Physics Symposium, 1994 32nd Annual Proceedings, IEEE International 1994*; 1994: 120-125.

Cheung KP: **The last trap that form the percolation path - the stress voltage effect**. In: *Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 599-600.

The Weibull Distribution

Datta S, Dewey G, Doczy M, Doyle BS, Jin B, Kavalieros J, Kotlyar R, Metz M, Zelick N: **High Mobility Si/SiGe Strained Channel MOS Transistors with HfO2/TiN Gate Stack**. *IEDM Tech Dig* 2003:653.

Chakravarthi S, Krishnan A, Reddy V, Machala CF, Krishnan S: **A comprehensive framework for predictive modeling of negative bias temperature instability**. In: *Reliability Physics Symposium Proceedings, 2004 42nd Annual* 273-282.

Tsujikawa S, Akamatsu Y, Umeda H, Yugami J: **Two concerns about NBTI issue: gate dielectric scaling and increasing gate current**. In: *Physics Symposium Proceedings, 2004 42nd Annual 2004 IEEE International: 2004*; 2004: 28-34.

Tsujikawa S, Watanabe K, Tsuchiya R, Ohnishi K, Yugami J: **Experimental evidence for the generation of bulk traps by negative bias temperature stress and their impact on the integrity of direct-tunneling gate dielectrics**. In: *VLSI Technology, 2003 Digest of Technical Papers 2003 Symposium on 2003*; 2003: 139-140.

Harris HR, Choi R, Lee BH, Young CD, Sim JH, Mathews K, Zeitzoff P, Majhi P, Bersuker G: **Comparison of NMOS and PMOS stress for determining the source of NBTI TiN/HfSiON devices**. In: *IRPS: 2005; San Jose Ca*; 2005: 80-83.

M.A.Quevedo-Lopez: **Thermal stability of hafnium–silicate and plasma-nitrided hafnium silicate films studied by Fourier transform infrared spectroscopy**. *Applied Physics Letters* 2005, **87**(012902):1-3.

Smith BC: **Fundamentals of Fourier Transform Infrared Spectroscopy** CRC press; 2000.

Onishi K, Rino C, Chang Seok K, Hag-Ju C, Young Hee K, Nieh RE, Jeong H, Krishnan SA, Akbar MS, Lee JC: **Bias-temperature instabilities of polysilicon gate HfO/sub 2/ MOSFETs**. *Electron Devices, IEEE Transactions on* 2003, **50**(6):1517-1524.

Sa N, Kang JF, Yang H, Liu XY, He YD, Han RQ, Ren C, Yu HY, Chan DSH, Kwong DL: **Mechanism of positive-bias temperature instability in sub-1-nm TaN/HfN/HfO/sub 2/ gate stack with low preexisting traps**. *Electron Device Letters, IEEE* 2005, **26**(9):610-612.

Shanware A, Visokay MR, Chambers JJ, Rotondaro ALP, Bu H, Bevan MJ, Khamankar R, Aur S, Nicollian PE, McPherson J *et al*: **Evaluation of the positive biased temperature stress stability in HfSiON gate dielectrics**. In: *Physics Symposium Proceedings, 2003 41st Annual 2003 IEEE International 2003*; 2003: 208-213.

Krishnan SA, Peterson JJ, Young CD, Brown G, Choi R, Harris R, Sim JH, Zeitzoff P, Kirsch P, Gutt J *et al*: **Dominant SILC mechanisms in HFO/sub 2/TiN gate nMOS and pMOS transistors**. In: *International Reliability Physics Symposium: 2005; Ca*; 2005: 642-643.

Quevedo-Lopez MA, Krishnan SA, Kirsch PD, Li HJ, Sim JH, Huffman C, Peterson JJ, Lee BH, Pant G, Gnade BE *et al*: **High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements**. *accepted IEDM Tech Dig* 2005.

Sim JH, Song SC, Kirsch PD, Young CD, Choi R, Kwong DL, Lee BH, Bersuker G: **Effects of ALD HfO2 Thickness on Charge Trapping and Mobility**. In: *INFOS: 2005*; 2005.

Naoto Umezawa KS, Kazuyoshi Torii, Mauro Boero, Toyohiro Chikyow, Heiji Watanabe, Kikuo Yamabe, Takahisa Ohno, Keisaku Yamada, and Yasuo Nara: **The Role of Nitrogen Incorporation in Hf-based High-k Dielectrics: Reduction in Electron Charge Traps**. In: *ESSDERC: 2005; Grenoble, France*; 2005: 201.

Carlson TA: **X-Ray Photoelectron Spectroscopy** Academic Press 1978.

Bauza D: **Extraction of Si-SiO2 Interface Trap Densities in MOSFET's with Oxides Down to 1.3 nm Thick**. In: *Solid-State Device Research Conference, 2002 Proceeding of the 32nd European: 24-26 September 2002 2002*; 2002: 231-234.

Quevedo-Lopez M: **Material Properties of Hafnium and Zirconium Silicate**. Denton: University of North Texas; 2003.

Siddarth Krishnan MQ-L, Rino Choi, Paul Kirsch, Chadwin Young, Rusty Harris,, Jeff Peterson H-JL, Byoung Hun Lee and Jack Lee: **Charge Trapping Dependence on the Physical Structure of Ultra-thin ALDHfSiON/TiN Gate Stacks**. In: *International Integrated Reliability Workshop (IIRW): 2005; Lake Tahoe, Ca*: IEEE; 2005.

Frank Chung DS: **Industrial Applications of X-Ray Diffraction** Marcel Dekker 1999.

Rigarku **Ultima III XRD**

Sekine K, Inumiya S, Sato M, Kaneko A, Eguchi K, Tsunashima Y: **Nitrogen profile control by plasma nitridation technique for poly-Si gate HfSiON CMOSFET with excellent interface property and ultra-low leakage current**. In: *Electron Devices Meeting, 2003 IEDM '03 Technical Digest IEEE International Dec., 2003 2003*: IEEE; 2003: 4.6.1-4.6.4.

Kimizuka N, Yamaguchi K, Imai K, Iizuka T, Liu CT, Keller RC, Horiuchi T: **NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10-μm gate CMOS generation**. In: *VLSI Technology, 2000 Digest of Technical Papers 2000 Symposium on 13-15 June 2000 2000*; 2000: 92-93.

Vita

Siddarth A. Krishnan was born in Tamil Nadu, India on the 20th of August, 1978 to Mr. A.R. Krishnan (C.A.I.I.B) and Mrs. Sumathi Krishnan (General Manager, BSNL, Madras circle). After 16 years of primary and higher schooling at Sri Sankara Senior Secondary School, he enrolled in the Department of Metallurgical Sciences in the Indian Institute of Technology in Madras in 1995. After receiving a B.Tech degree in 1999, he went on to receive an M.S degree from the Department of Materials Sciences in December 2001. Since December 2001, he has been researching high-κ dielectrics with Professor Jack Lee, as part of his Ph.D. dissertation. During this tenure, he has interned with Visionflow Inc. (2003), in digital image processing, and interned with SEMATECH (2004-present). As part of the performed research, he authored or co-authored the following publications:

1. **Siddarth A. Krishnan**, M.A. Quevedo-Lopez, Rino Choi, Paul D.Kirsch, Chadwin Young, Rusty Harris, Jeff J. Peterson, Hong-Jyh Li, Byoung Hun Lee and Jack C. Lee, "Charge Trapping Dependence on the Physical Structure of Ultra-thin ALD-HfSiON/TiN Gate Stacks", **International Integradted Reliability Workshop**, October 20th, California.
2. M. A. Quevedo-Lopez, **S. A. Krishnan**, P. D. Kirsch, H. J. Li, J. H. Sim, C. Huffman, J. J. Peterson, B .H. Lee, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, D. Guo, H. Bu, and T.P. Ma, "High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements", to be presented at IEDM, December 2006.

3. **Siddarth A. Krishnan**, Manuel Quevedo, Hong-Jyh Li, Paul Kirsch, Rino Choi, Byoung Hun Lee, Jack C. Lee and Gennadi Bersuker, "Impact of nitrogen on PBTI characteristics of HfSiON/TiN Gate Stacks", accepted to **International Reliability Physics Symposium,** 2006.
4. **Siddarth A. Krishnan**, Manuel Quevedo, Rusty Harris, Paul D. Kirsch, Rino Choi, Byoung Hun Lee, Gennadi Bersuker, Jeff Peterson, Hong-Jyh Li, Chadwin Young and Jack C. Lee, "NBTI Dependence on Dielectric Thickness in Ultra-scaled HfSiO Dielectric/ALD-TiN Gate Stacks", **SSDM** 2005, Kobe, Japan.
5. **Siddarth A. Krishnan**, Jeff Peterson, Rino Choi, Paul D. Kirsch, Kenneth Matthews, Byoung Hun Lee, Gennadi Bersuker and Jack C. Lee, "Effect of Dynamic Stress on Threshold Voltage Instability in High-κ/TiN nMOSFETs", submitted to **EDL** in October 2005.
6. **Siddarth A. Krishnan**, Manuel Quevedo, Rusty Harris, Paul D. Kirsch, Rino Choi, Byoung Hun Lee, Gennadi Bersuker and Jack C. Lee, "NBTI Dependence on Dielectric Thickness and Nitrogen concentration in Ultra-scaled HfSiON Dielectric/ ALD-TiN Gate Stacks", submitted to **JJAP**, 2005.
7. "Comparison of ALD and MOCVD deposition processes for deposition of Hafnium Silicate" , **Siddarth A. Krishnan**, Paul D. Kirsch, Byoung Hun Lee, Jeff Peterson, Hong Jyh Li, Jim Gutt, Texas, Joint Fall Meeting of the Texas Sections of the APS, AAPT, and Society of Physics Students - Zone 13, Baylor University, Waco, Texas October 7-9, 2004.

8. “Dominant SILC mechanisms in HfO_2/TiN Gate nMOS and pMOS transistors”, **Siddarth A. Krishnan**, Jeff J. Peterson, Chadwin D. Young, George Brown, Rino Choi, Rusty Harris, Jang Hoan Sim, Peter Zeitzoff, Paul Kirsch, Jim Gutt, Hong Jyh Li, Ken Matthews, Jack C. Lee, Byoung Hun Lee, and Gennadi Bersuker, **Reliability Physics Symposium**, 2005. Proceedings. 43rd Annual. 2005 IEEE International, April 17-21, 2005 Page(s):642 – 643.
9. "Comparison between ultra-thin ZrO2 and ZrOxNy gate dielectrics in TaN or Poly-Gated NMOSCAP and NMOSFET devices", Renee Nieh, **Siddarth Krishnan** et al, in **VLSI Tech**, 2002.

Permanent Address:

5200 N Lamar Blvd, Apt# L202, Austin Texas 78751.

This dissertation was type-written by Siddarth A. Krishnan.