The Dissertation Committee for Robin Matthew Tsang
certifies that this is the approved version of the following dissertation:

High-Performance $\Delta\Sigma$ Analog-to-Digital Conversion

Committee:

Jonathan W. Valvano, Supervisor

Pio Balmelli

Francis Bostick

Robert Flake

Douglas Holberg

Earl Swartzlander

High-Performance $\Delta\Sigma$ Analog-to-Digital Conversion

by

Robin Matthew Tsang, B.S.E.E.; M.S.E.E.

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

May 2008

Dedicated to Mom and Dad for their hard work in raising the three of us.

Acknowledgments

The person I owe all of this to is my supervisor, Professor Jonathan W. Valvano, who believed in me and encouraged me through the ups and downs of my pursuit for the doctoral degree. His teachings are nothing short of the most excellent. I learned a great deal from him both as an engineer and as a person. He always taught us to 'do the right thing', something I will never forget. Since the very first day, never once was he impatient with me, and never did I feel pressured at work. For the four years I have been Professor Valvano's student, I always felt happy and privileged to work for him. He gave me freedom to allocate my time as I like, which allowed me to do exercise and stay healthy and positive. This I believe was the key to the success of this work, and I thank him for that.

I thank Mom and Dad for being so supportive of me for all these years. There are no words that can describe how much I love them and how much they mean to me. Without their unconditional love, none of this would have been possible. There were times when things were difficult because Suzanne, Jason, and I all studied abroad, and money was scarce. But each and every time, with God's grace, we were able to get by just fine. Mom always believed that God will provide for us as long as we truly believed in Him and did the best we could with the talents given to us. I believe my work at this university is a testament to Him being by my side because there were so many obstacles I had to overcome to complete the project. Without anything short of a miracle, this would not have happened. Since a young age, Mom explained to me that everything can be taken away from you e.g., your car, your house, and your money, but no one can ever take away your education. This is at least partially why I continued on to the doctorate degree, and is true for Suzanne and Jason as well. Dad, with his infinite passion for sports, instilled the passion in me at a very young age. He taught me to use my time wisely and to play sports as much as I can. This really helped keep me healthy and happy throughout my life and I am so grateful for that.

I thank Professor Robert Flake for seeing the potential in me and accepting my application to the graduate program. He advised me to take the right classes and introduced me to the world of control systems. Professor Flake made an effort to form my Ph.D. committee, and much is appreciated. Professor Francis Bostick and Professor Earl Swartzlander posed excellent questions and motivated me to do better in every way. I especially thank Professor Swartzlander for editing my dissertation with care. His effort has helped improve this dissertation beyond my capability.

I thank Dr. Pio Balmelli for serving on my committee and for giving me such high quality feedback that ultimately led to much of my dissertation material. His enthusiasm and intelligent questions during my Ph.D. proposal and defense made it a fun and enjoyable experience for everyone. I thank Dr. Doug Holberg for offering to tape-out my chip. Although I was not able to take advantage of his offer, the process of trying to meet his deadline and then failing, led to my discovery of the new modulator topology which I proposed in this dissertation.

Besides my committee members, I thank Dr. Michael D. Cave for teaching me circuit design techniques with an industry perspective. We had stimulating discussions on how to improve yield, clock jitter, floor planning, and ADC characterization. Much of the things he taught me can only be gained through years of experience and I thank him for that. Dr. Byung-Geun Lee, my former research colleague, also contributed to the success of this work. His discipline has indirectly affected me in a very positive way. Him coming to the office at seven in the morning and not leaving until past dinner time, kept my own schedule and progress in check. His methodical circuit analysis techniques made me a better circuit designer. We had fruitful discussions on simulation, amplifier design, layout, and packaging, all of which led to critical circuit design decisions in this project. His help with setting up my simulation and layout tools is also greatly appreciated.

I thank Professor Eric Swanson for introducing me to the world of mixed-signal circuit design and for his teaching efforts at the University. Without his Mixed-Signal and Systems Design and Analysis course, I would have never stumbled onto such a fascinating topic. His help with debugging silicon and finding the root cause of the excess noise source is much appreciated. I also thank him for offering his time to meet with me once a week during the last semester to improve this dissertation. He helped me understand the intricacies and tradeoffs in data converter design like nobody else has.

I thank my research colleague, Nachiket Kharalkar, for his enthusiasm and encouragement. Over the years Nachiket has become a good friend. There were many semesters where we held the same teaching assistant (TA) position and organized laboratory assignments together for large undergraduate classes. His knowledge and hard work helped make my life as a TA enjoyable. Without him, things could have been much more difficult. Nachiket also worked the same hours as I did in the lab, often until the last scheduled shuttle-bus departure. His company during late nights in the lab helped keep me motivated from the circuit-design stage all the way to silicon characterization. I also thank him for his help with photographing my chip using his medical research equipment.

Daryl Goodnight and Paul Landers, two very friendly and knowledgable technicians at the University, offered sound advise for solder rework and reflow.

Without their help, my make-shift PCB assembly process would not have operated as smoothly as it did. Robert Chua, the very best analog/mixed-signal test engineer I know, pointed me in the right direction by suggesting the prototype be placed in the smallest package possible, for the highest performance. He also suggested an asymmetrical die placement to reduce the inductance of sensitive pins. Without Robert, the prototype's performance would have been limited by the package, and therefore I am grateful for his help.

Some of my long-time EE friends from my undergraduate days, Khachatur Papanyan, Jon Perry, David Magness, Orson Lo, and Alvaro Garcia, were all supportive of my work. I especially thank Jon Perry for offering to lend me his own money to tape-out my chip. Although I declined his offer, I am sincerely grateful for his most unselfish heartfelt gesture. I thank Michel Azarian for his friendship and for his help with board-level circuit design. I thank Frank Raffaeli for letting me use his RACAL-DANA 9087 RF signal generator. Finally, I thank Professor Archie Holmes and Professor Jack Lipovski for writing my graduate school letter-of-recommendation, which was the beginning to all of this.

Robin Matthew Tsang

The University of Texas at Austin
May 2008

High-Performance ΔΣ Analog-to-Digital Conversion

Publication No. ____________________

Robin Matthew Tsang, Ph.D.
The University of Texas at Austin, 2008

Supervisor: Jonathan W. Valvano

This dissertation is about a new ΔΣ analog-to-digital converter that offers enhanced quantization noise suppression at low oversampling ratios. This feature makes the converter attractive in applications where speed and resolution are simultaneously demanded. The converter exploits double-sampling for speed, and takes advantage of a new loop-filter to pin down passband quantization noise. A prototype is fabricated in 0.18-μm CMOS and tested. Results show that at 200-MS/s, the converter achieves an effective number of bits (ENOB) of 12.2-b in a 12.5-MHz signal band while consuming 89-mW from a 1.8-V supply. Using a common performance metric that takes into account of ENOB and signal bandwidth, the prototype outperforms all previously-reported IEEE switched-capacitor ΔΣ modulators.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Overview

Discrete-time (DT) switched-capacitor (SC) $\Delta\Sigma$ analog-to-digital converters (ADCs) have long been a workhorse in high-performance analog-to-digital conversion. These converters are popular because they can achieve high-resolution under a limited power-supply voltage and are tolerant against process and temperature variations. Unfortunately, due to its oversampling nature, achieving a wide bandwidth while maintaining high-resolution and linearity is difficult. To the best knowledge of the author, no DT $\Delta\Sigma$ modulator with an effective number of bits (ENOB) $>$ 12-b and a signal bandwidth $>$ 10-MHz has been reported to date. This work demonstrates with a novel feedforward DT loop-filter and a time-interleaved offset-canceled comparator, that such performance (12.2-b ENOB, 12.5-MHz) can be achieved in a 0.18-μm CMOS process with relatively low power (89-mW), relatively small silicon area (0.8-mm^2), and no calibration.

To maximize signal bandwidth for a given process technology, a low oversampling ratio (OSR) is desired. However, quantization noise, which normally can be reduced down to negligible levels in mid to high OSR modulators, can become a significant source of error in low OSR modulators. For example, at 8× OSR, the popular cascade-of-integrators-feedforward form (CIFF) $\Delta\Sigma$ modulator [20] has a peak signal-to-quantization-noise ratio (SQNR) of only 81.5-dB with 4-b quantization and an out-of-band noise gain of 6. In practice, a 10-dB margin between the target SNR and the SQNR is often added on to ensure a robust design. This suggests a modulator with an SQNR of 81.5-dB has a final SNR of 71.5-dB, which is less than 12-b ENOB performance. This leads to the main contribution of this work, which is the introduction of a new loop-filter topology that uses strictly delaying (z^{-1}) integrators similar to CIFF, but provides 86.5-dB of SQNR (5-dB advantage over CIFF). Unlike Balmelli's loop-filter [4] which also provides better SQNR than CIFF, this loop-filter can be *double-sampled* in a straightforward manner so that the bandwidth of the operational transconductance amplifier (OTA) is fully exploited. In addition to the loop-filter, a time-interleaved comparator suitable for accurate high-speed signal quantization in a double-sampled converter is introduced. This comparator plays a key role in the successful implementation of the prototype $\Delta\Sigma$ modulator in this research work.

The rest of this dissertation is organized as follows. In the remaining parts of this chapter, state-of-the-art DT and continuous-time (CT) $\Delta\Sigma$ modulators reported in IEEE literature will be compared to the prototype herein in terms of performance and silicon area. The basic operation of feedforward DT $\Delta\Sigma$ modulators will be discussed, followed by an outline of the differences between feedforward and feedback modulators, and DT and CT modulators. Chapter 2 discusses the bottlenecks that limit performance in conventional and recently-published feedforward $\Delta\Sigma$ loop-filters. Chapter 3 introduces the new loop-filter topology suitable for high-speed double-sampled low OSR $\Delta\Sigma$ modulation and explains why this topology advances the state-of-the-art. Chapter 4 goes over the basic concept of double-sampling and the bilinear feedback network [5] vital to combating capacitor mismatch in the global feedback path of a double-sampled $\Delta\Sigma$ modulator. Chapter 5 introduces the new double-sampled $\Delta\Sigma$ modulator that exploits the proposed loop-filter for efficient high-speed low OSR analog-to-digital conversion. Chapter 6 details the prototype implementation and introduces the new time-interleaved comparator for accurate high-speed signal quantization in a double-sampled converter. Chapter 7 elaborates on the peripheral circuits used to complete the prototype, including a Low-Voltage Differential Signalling (LVDS) clock amplifier, LVDS transmitters, electro static discharge (ESD) circuitry, and biasing circuits. Chapter 8 describes the test setup, measurement results, and PCB construction. Chapter 9 discusses some of the difficulties faced by the author during design, prototyping, and testing. Finally, a summary of this research and suggestions for future work follows in Chapter 10.

1.2 A quick comparison with the state-of-the-art

A common figure-of-merit (FOM) used to compare $\Delta\Sigma$ modulators is defined as total power consumption divided by performance, where performance is defined as the product of the effective number of bits (2^{ENOB}) and the decimated sampling-rate (2·Bandwidth):

$$FOM = \frac{Power}{2 \cdot 2^{ENOB} \cdot Bandwidth} \ . \tag{1.1}$$

Here, ENOB = $\frac{SNDR-1.76}{6.02}$ and SNDR, in units of decibels (dB), represents the signal-to-noise-and-distortion ratio of the modulator [27]. The rationale behind the FOM is that it provides a measure of how much power is needed to achieve a certain performance. In ADCs, performance is generally accepted as the resolution and linearity it provides i.e., ENOB, and the speed at which it operates (Nyquist frequency). Naturally, the lower the FOM, the more efficient the modulator. This FOM has units of *Joules per conversion* and is often scaled by a factor of 10^{-12} and annotated as *pJ/conversion*. To compare the measured prototype performance of this work with the state-of-the-art, a list of IEEE-reported $\Delta\Sigma$ modulators[1], both DT and CT, is complied and plotted on a log-log scale in Figure 1.1. A trend is visible in the graph between performance and power consumption, which indicates that higher performance generally requires more power. Here, performance is defined as the denominator term of the FOM. Comparing all DT modulators, this work not only bucks the trend, but is also the highest-performing DT $\Delta\Sigma$ modulator. As will be discussed in Chapter 9, the prototype's SNDR is still 3-dB short of the original target. However, the discrepancy is likely due to a now-known error made during OTA noise simulation and can be corrected in a future revision of the circuit.

Besides efficiency, ADCs can be compared in terms of its physical size with respect to performance. Plotted on a log-log scale in Figure 1.2 are the silicon areas of the same modulators in the previous figure. A weaker but still visible trend suggests higher performance usually demands larger silicon areas. Comparing this work to others, this modulator is physically small for the performance it delivers. Smaller silicon area can translate to lower cost and eases integration into larger chips. For a list of the data-points used here, please refer to Table 1.1.

1.3 Basic operation of feedforward $\Delta\Sigma$ modulators

At a high-level, the feedforward $\Delta\Sigma$ modulator consists of a loop-filter and a quantizer placed in feedback configuration. The modulator is operated at a rate much higher than the maximum input signal frequency of interest. A block-level diagram of a 4-b $\Delta\Sigma$ modulator is shown in Figure 1.3. A 4-b digital-to-analog converter (DAC) in the feedback path converts the quantized output back to the analog domain so proper feedback can be applied. The loop-filter, *L(z)*, provides the necessary

---

[1] Not an exhaustive list, but to the best knowledge of the author, the highest-performing $\Delta\Sigma$ modulators reported in IEEE literature up until Apr. 2008 have been included.

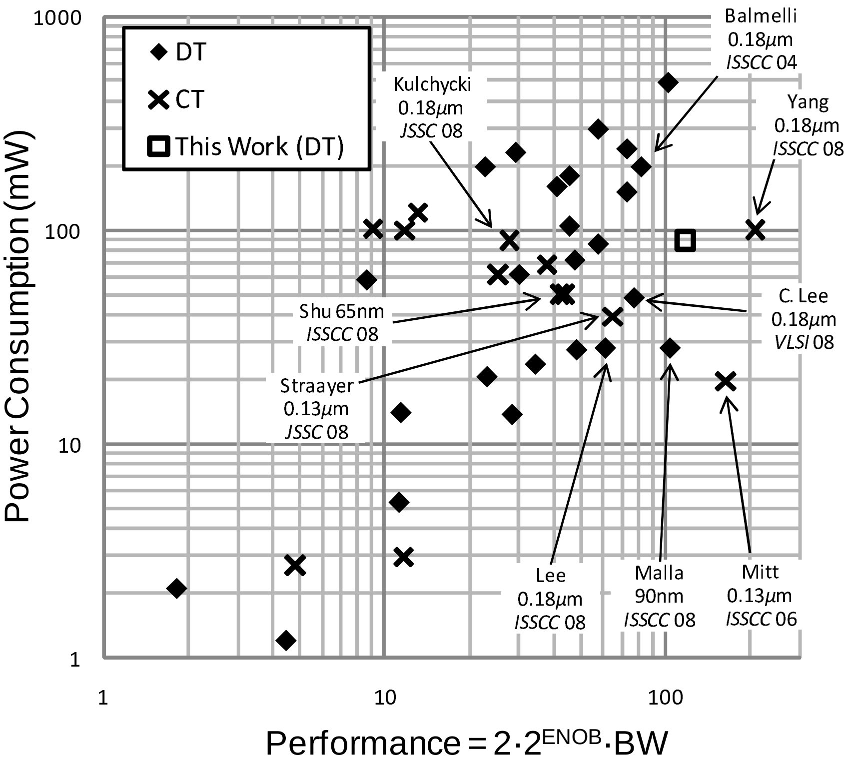

Figure 1.1: Performance comparison with IEEE-published DT and CT $\Delta\Sigma$ modulators.

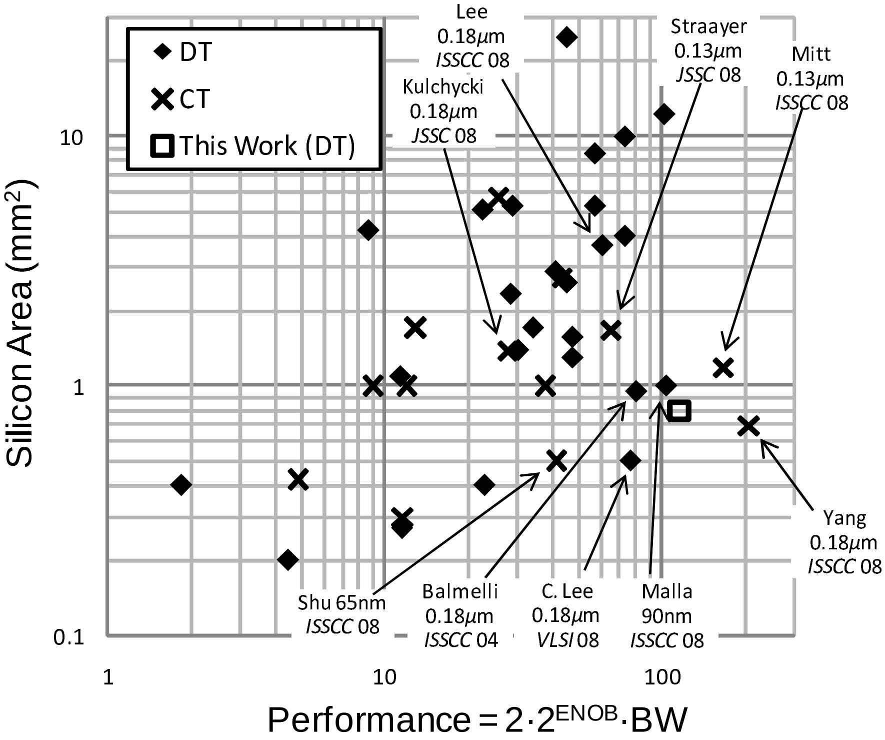

Figure 1.2: Silicon area comparison with IEEE-published DT and CT $\Delta\Sigma$ modulators.

Table 1.1: IEEE-published $\Delta\Sigma$ modulators

Author	Year	Type	OSR	Tech.	MHz	SNDR	mW	mm^2
Paton [54]	2004	CT	10	0.13-μm	15	63.7	70	1
Breems [55]	2004	CT	8	0.18-μm	10	58	122.4	1.7
Yan [15]	2004	CT	16	0.5-μm	1.1	83	62	5.76
Dörrer [56]	2005	CT	26	0.13-μm	2	71	3	0.3
Mitteregger [1]	2006	CT	16	0.13-μm	20	74	20	1.2
Caldwell [16]	2006	CT	5	0.18-μm	10	57.2	101	1
Caldwell [16]	2006	CT	5	0.18-μm	20	48.8	103	1
Li [14]	2007	CT	12	0.25-μm	2.5	80.5	50	2.73
Song [58]	2008	CT	37.5	0.25-μm	2	63.4	2.7	0.42
Shu [59]	2008	CT	16	65-nm	8	70	50	0.5
Yang [2]	2008	CT	32	0.18-μm	10	82	100	0.7
Marques [60]	1998	SC	24	1-μm	1	85	230	5.25
Geerts [61]	1999	SC	24	0.5-μm	1.1	82	200	5.06
Fujimori [62]	2000	SC	8	0.5-μm	1.25	87	105	24.8
Geerts [63]	2000	SC	24	0.65-μm	1.25	89	295	5.3
Vleugels [6]	2001	SC	16	0.5-μm	2	87	150	10
Gupta [64]	2002	SC	29	0.18-μm	1.1	88	180	2.6
Hamoui [65]	2003	SC	16	0.18-μm	1.5	71	59	4.2
Park [66]	2003	SC	8	0.35-μm	2.5	88	495	12.25
Jiang [10]	2004	SC	8	0.18-μm	2	82	159	2.9
Balmelli [4]	2004	SC	8	0.18-μm	12.5	72	200	0.95
Bosi [57]	2005	SC	4	0.18-μm	10	73	240	4
Koh [67]	2005	SC	20	90-nm	1.94	63	1.2	0.2
Jiang [68]	2005	SC	20	90-nm	1	61	2.1	0.4
Nam [34]	2005	SC	16	0.25-μm	1.25	89	87	8.6
Paramesh [69]	2006	SC	8	90-nm	20.48	63	73	1.3
Lee [71]	2006	SC	60	0.18-μm	1.1	76	5.4	1.1
Kwon [70]	2006	SC	33	0.18-μm	2.2	78	13.8	2.32
Cao [72]	2007	SC	50	0.25-μm	1.25	75	14	0.27
Kanazawa [73]	2006	SC	12.5	0.18-μm	4	77.3	27.54	1.57
Fujimoto [74]	2006	SC	12	0.18-μm	3.2	76.3	23.76	1.7
This work	2008	SC	8	0.18-μm	12.5	75.1	89	0.8
Christen [75]	2007	SC	12	0.13-μm	10	63	20.5	0.4
C. Lee [76]	2008	SC	23.8	0.18-μm	4.2	79	28	3.67
Malla [3]	2008	SC	10.5	90-nm	20	70	28	1
Chang [77]	2007	SC	16	0.25-μm	2.2	78.5	62.5	1.4

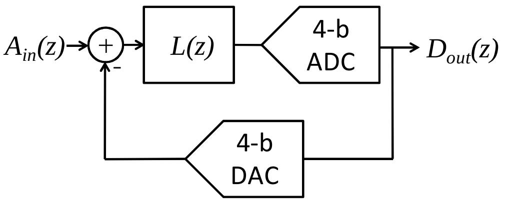

Figure 1.3: A 4-b ADC put in a feedback configuration together with a loop-filter and 4-b DAC can achieve >4-b resolution if oversampled.

filtering to "shape" the quantization noise of the 4-b ADC to push it outside the band-of-interest. Figure 1.4 shows the concept of noise-shaping at work. The lighter color spectrum is the standalone 4-b ADC output with no feedback and zero input. The flat response across the entire Nyquist band suggests that no noise-shaping is present. Now assuming the user is only interested in a small range of input frequencies from dc to $\frac{F_s}{2} \div 8 = \frac{F_s}{16}$, then negative feedback and filtering can be applied to the 4-b ADC such that the quantization noise from dc to $\frac{F_s}{16}$ is "pushed" to higher frequencies, as exemplified by the darker color spectrum in Figure 1.4. In this example, because the highest frequency of interest is $\frac{F_s}{2} \div 8$, the OSR equals 8. To complete the analog-to-digital conversion process, the noise beyond $\frac{F_s}{16}$ is filtered out with a sharp digital filter and decimated to reduce the sampling-rate to twice the Nyquist frequency, i.e. $\frac{F_s}{8}$.

To model the noise-shaping phenomenon, a linearized model of the $\Delta\Sigma$ modulator is needed. Figure 1.5 shows how the 4-b ADC can be modeled as a quantization noise source, *Q(z)*, that sums with the output of the loop-filter. The 4-b DAC is assumed perfectly linear in the feedback path and can be done so because different DAC linearization algorithms exists to partially or completely remove the DAC's nonlinearity in a $\Delta\Sigma$ modulator. Chapter 6 studies the Data Weighted Averaging (DWA) algorithm [22] used in this work.

Using superposition, it is possible to separate the output, $D_{out}(z)$, into its respective signal ($A_{in}(z)$) and quantization noise (*Q(z)*) components. Setting *Q(z)*

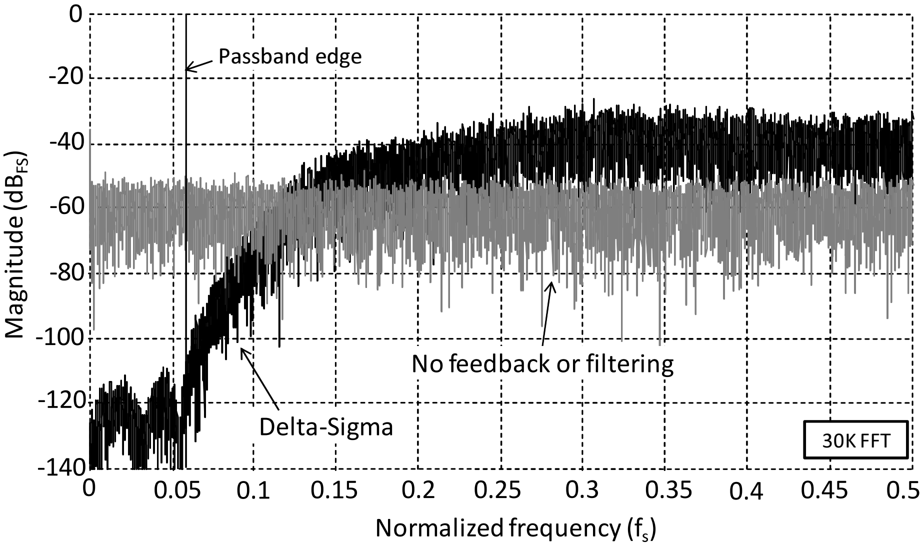

Figure 1.4: Noise-shaping can push quantization noise out-of-band. Shows how a 4-b ADC can achieve 15-b performance (87.5-dB SQNR) through feedback, filtering, and oversampling. As shown, the OSR is 8×.

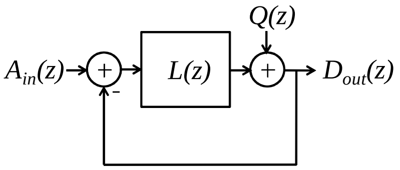

Figure 1.5: Assuming the DAC does not introduce any errors, the modulator's quantization error is solely due to the ADC and is modeled by *Q(z)*.

to zero, the contribution of $V_{in}(z)$ at $D_{out}(z)$ can be found:

$$STF = \left.\frac{D_{out}(z)}{A_{in}(z)}\right|_{Q(z)=0} = \frac{L(z)}{1+L(z)}. \tag{1.2}$$

This result is termed the signal transfer function (STF) and tends to unity if $|L(z)| \gg 1$. Since the STF describes the conversion process from the analog domain to the digital domain, a unity gain response across the passband is desirable. Now setting $A_{in}(z)$ to zero, the contribution of *Q(z)* at $D_{out}(z)$ can be found, which equals

$$NTF = \left.\frac{D_{out}(z)}{Q(z)}\right|_{A_{in}(z)=0} = \frac{1}{1+L(z)}. \tag{1.3}$$

This result is termed the noise transfer function (NTF) and tends to zero if $|L(z)| \gg 1$. Again, this is a desirable result because the goal is to suppress quantization noise, *Q(z)*, at the output. By giving *L(z)* a large magnitude response within the band-of-interest, quantization noise is suppressed while the input signal is faithfully converted to the digital domain. The aggregate output that combines the contributions of $A_{in}(z)$ and *Q(z)* equals to

$$D_{out}(z) = A_{in}(z) \cdot STF + Q(z) \cdot NTF. \tag{1.4}$$

To gain a better understanding of the relationship between *L(z)*, NTF and STF, a set of pole-zero plots that generated the noise-shaping response in Figure 1.4 is shown in Figure 1.6. Poles of *L(z)*, due to feedback, become zeros of the NTF. STF and NTF share the same set of poles, and is a distinct characteristic of feedforward $\Delta\Sigma$ modulators. Figure 1.7 plots the magnitude response of *L(z)*, NTF and STF. It is easy to see that *L(z)* and NTF mirror each other in the modulator's passband because poles of *L(z)* are zeros of NTF as mentioned earlier. The zeros of NTF are spread across the passband to achieve better quantization noise suppression. Spreading these zeros is not always an option and depends on the loop-filter's

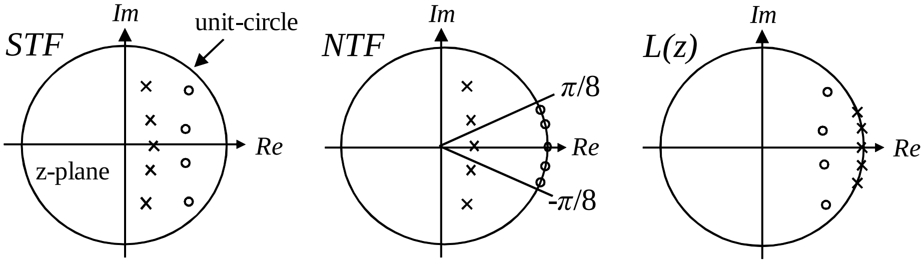

Figure 1.6: Pole-zero plots of the STF, NTF, and *L(z)* of a feedforward $\Delta\Sigma$ modulator. STF and NTF share the same set of poles. Poles of *L(z)* mirror and become the zeros of the NTF.

topology. In some topologies, NTF zeros must be located at dc, and subsequently their SQNR will be worse for a given set of pole locations.

Also worth noting is the coupling between STF and NTF beyond the passband. In a feedforward $\Delta\Sigma$ modulator, higher out-of-band NTF gain results in higher out-of-band STF gain. This phenomena is seen as a drawback because excessive out-of-band STF gain increases the modulator's sensitivity towards high-frequency inputs. In a communication system where adjacent or nearby channels cannot be attenuated sufficiently, the modulator can saturate and become unstable. There exists, however, a tradeoff that justifies higher out-of-band STF gain, and that is, by increasing the NTF's out-of-band gain, passband quantization noise can be reduced. A term often used to describe the aggressiveness of the noise-shape is quantization noise gain. It is a vaguely defined term that conveys how much out-of-band gain is in the NTF's frequency response. Usually, the more quantization noise gain a modulator can handle, the higher the SQNR. However, higher quantization noise gain threatens stability because accumulated quantization noise in the modulator can take up precious dynamic range, which in turn can saturate the quantizer and drive the modulator unstable [21, 10]. From here on, quantization noise gain is defined to be the magnitude of the NTF at $\frac{F_s}{2}$.

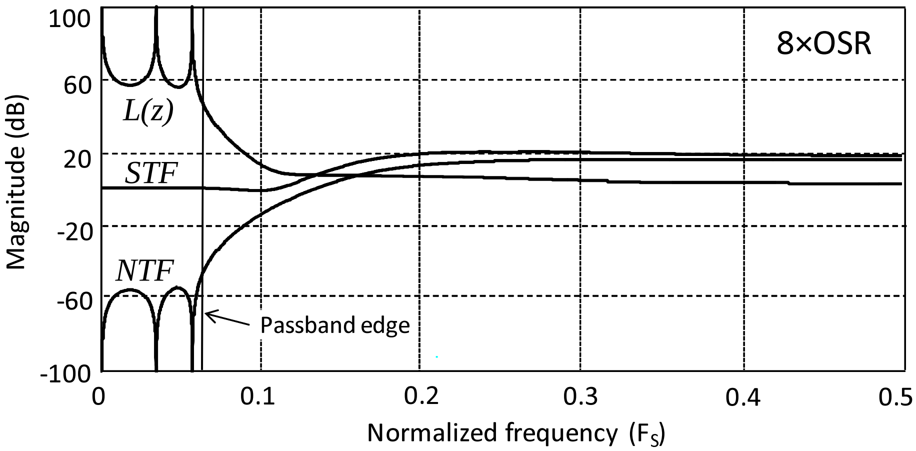

Figure 1.7: Frequency response of the STF, NTF, and *L(z)* of a feedforward $\Delta\Sigma$ modulator. Peaks in *L(z)* mirror to become zeros in the NTF.

1.4 Feedforward vs. feedback $\Delta\Sigma$ modulators

DT $\Delta\Sigma$ modulators can be separated into two main categories, feedforward and feedback, as shown in Figure 1.8 and Figure 1.9, respectively. In a feedforward modulator, outputs of all integrators are fed forward and summed at the input of the quantizer. Only one global negative feedback path exists, which goes from the output of the modulator back to the input of the 1^{st} integrator. In a feedback modulator, there are no feedforward paths to the quantizer (except for the last integrator), but multiple feedback paths exist that go from the output of the modulator back to the input of each integrator. From a complexity standpoint, it can be argued that both are similarly complex because on one hand, the feedforward modulator requires an extra summing node, but on the other hand, the feedback modulator requires multiple feedback DACs. From the perspective of relaxing the modulator's out-of-band signal sensitivity, the feedback modulator wins because its STF usually exhibit a low-pass characteristic, which act to prevent out-of-band input signals from saturating the modulator. This is possible because its STF and NTF do not

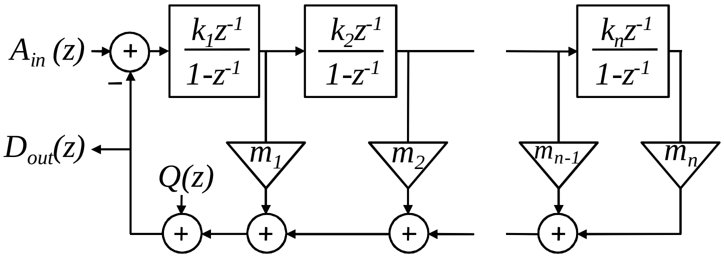

Figure 1.8: A feedforward ΔΣ modulator.

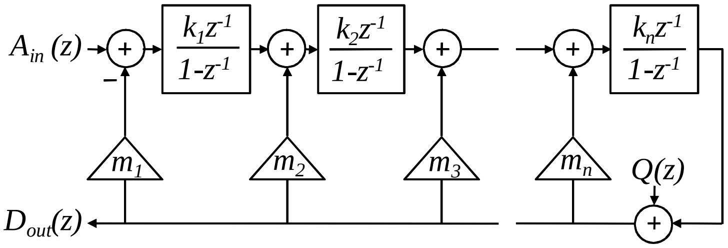

Figure 1.9: A feedback ΔΣ modulator.

share the same set of poles [20]. From the perspective of performance at low OSRs, however, the feedforward modulator has an advantage. Balmelli showed that the input-referred error and noise contributions beyond the 1^{st} integrator depends on the gain coefficient, k_1, of the 1^{st} integrator, and the OSR [4]. Errors and noise beyond the 1^{st} integrator are suppressed when

$$k_1 > \frac{\pi}{OSR}. \tag{1.5}$$

As the OSR is reduced, it becomes more difficult to satisfy (1.5) for both feedforward and feedback modulators. However, because the values of the coefficients, k_1 to k_n, usually appear in descending order for feedforward modulators and ascending order for feedback, the feedforward modulator has a better chance at reducing the effects of errors and noise beyond the 1^{st} integrator. It is for this reason, that a feedforward topology is chosen for this research work.

1.5 Discrete-time vs. continuous-time $\Delta\Sigma$ modulators

In recent years, a significant number of publications have appeared in the literature regarding advances in CT $\Delta\Sigma$ modulators [55, 54, 56, 14, 15, 16]. These modulators are attractive to the designer for two main reasons. First, they provide inherent anti-alias filtering with its continuous-time loop-filter at no additional cost in power or silicon area. Second, the internal sampling-rate of CT modulators can be several times higher than DT modulators implemented in the same process because its integrators are not required to settle at the end of every cycle. As long as a CT integrator does not slew and its phase-shift induced excess loop-delay is under a certain limit, its speed requirements are met. Two of the best CT $\Delta\Sigma$ modulators reported to date operate at an impressive 640-MS/s [1, 2], which is very fast compared to the 200-MS/s prototype of this work. However, there are at least four reasons for choosing a DT implementation over CT, and the rest of this section explains what they are.

First, in terms of clock jitter sensitivity, the DT modulator has an edge because its sensitivity is proportional to the input signal frequency rather than the sampling-frequency. In an 8× OSR 1-b 90-dB SNR-targeted design, the jitter sensitivity of a DT modulator is roughly an order of magnitude less sensitive than a CT modulator [4]. However, it must be noted that a multi-bit non-return-to-zero (NRZ) feedback DAC in a CT modulator can significantly relax jitter sensitivity. Nonetheless, the CT modulator with 12-b ENOB and 20-MHz of bandwidth reported by Mitteregger [1], features a 4-b NRZ feedback DAC, but due to its still-critical jitter specification, a dedicated 300-fs RMS jitter phase-locked loop (PLL) was invested to accompany the modulator. As a comparison, the RMS jitter specification for the prototype herein is 3.2-ps (an order of magnitude less sensitive) for an ENOB of 12.2-b in a 12.5-MHz band (comparable performance).

Second, in terms of manufacturability and robustness, the DT modulator has an edge because its filter coefficients can be defined precisely with excellent predictability. Coefficients of a DT modulator are defined by capacitor ratios, which can be matched to roughly 0.1% (3-σ) accuracy in modern CMOS processes. The absolute value of the capacitors are unimportant as it does not alter the ratio between them. With such initial coefficient accuracy, it is possible for a DT modulator to implement an NTF with a higher Q-factor than a CT modulator, yet suffer less performance variability due to manufacturing process variations. Loop-filter coefficients of CT modulators, at least for the case of active-RC $\Delta\Sigma$ modulators, are dependent upon the absolute values of resistors and capacitors. In modern CMOS processes, the absolute value of resistors can vary by as much as ±75% depending on the type of resistor element used. If salicide-blocked polysilicon resistors are available, the tolerance level can improve to roughly ±25%. Nonetheless, calibration is still necessary to tune the CT modulator's coefficients to within a ±10% range for stable operation [14]. Additional circuitry needed to calibrate the CT modulator also increases the complexity of the converter.

Third, in terms of flexibility, the DT modulator wins because it can be clocked at virtually any rate below the maximum sampling-frequency. In communication systems, this can be beneficial if the channel bandwidth varies over time and the converter is able to dynamically adjust its sampling-rate to reduce power consumption. This is possible with DT modulators because poles and zeros of the NTF automatically scale with the clock frequency. However, CT modulators do not enjoy this flexibility because their filter coefficients are determined by time-constants rather than capacitor ratios. Changing the clock frequency of a CT modulator without properly adjusting the time constants can destabilize the modulator.

Fourth, in a DT modulator, sampling of critical signals can be time-isolated such that the sampling instant occurs during a window where other circuits are quiet [17]. For large system-on-chip (SoC) designs fabricated on heavily-doped epitaxial wafers, noise can couple from distant locations regardless of physical separation or guard rings [47]. In these situations, time-isolation may be the answer. However, signals in a CT modulator are continuous by nature, so time-isolation is not an option.

In addition to the four reasons stated above, DT modulators can be *double-sampled* to gain, ideally, a factor-of-two increase in bandwidth without increasing power consumption, assuming a 50% duty cycle [5, 6]. Equally so, double-sampling a modulator can ideally halve its power consumption while maintaining the same signal bandwidth. However, double-sampling brings with it sensitivities that do not exist for single-sampled $\Delta\Sigma$ modulators. Chapter 4 studies the non-idealities that must be overcome in order to fully take advantage of the speed benefits offered by double-sampling.

1.6 Basic design methodology for DT feedforward $\Delta\Sigma$ modulators

The design of a DT modulator usually begins by specifying a target NTF. A classical filter function such as inverse Chebyshev or an automated filter design algorithm such as CLANS [21, 9] can be used to design the NTF. Once it is obtained, the coefficients in the denominator of the NTF are used to solve for the coefficients in *L(z)*. As shown in Figure 1.8, the feedforward modulator has $2n$ coefficients, k_1 to k_n and m_1 to m_n. The denominator of the NTF, on the other hand, has only n coefficients (a_{1-n}) for an n^{th}-order modulator. To reduce the number of coefficients in *L(z)* to n, k_{1-n} or m_{1-n} can be set to unity. As an example, k_{1-n} is set to unity and the equation is used to solved for m_{1-n} with respect to the target NTF, which may be in the following form:

$$NTF_{target} = \frac{(1-z^{-1})^n}{1 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_n z^{-n}} \ . \tag{1.6}$$

Here, the target NTF that has all n NTF zeros located at dc because the feedforward modulator in Figure 1.8 does not allow zeros to be located elsewhere. Chapter 2 looks at topologies that can move the zeros away from dc for better passband quantization noise suppression. The closed-loop NTF of the feedforward modulator in Figure 1.8 can be shown to be equal to

$$NTF = \left.\frac{D_{out}(z)}{Q(z)}\right|_{A_{in}(z)=0} = \frac{(1-z^{-1})^n}{(1-z^{-1})^n + \sum_{i=1}^{n} z^{-1} \cdot (1-z^{-1})^{(n-i)} \cdot m_i}. \tag{1.7}$$

Equating the coefficients in the denominator of (1.6) to the coefficients in the denominator of (1.7) for the same powers of z^{-1}, permits solving for m_{1-n} (n equations and n unknowns). Thereafter, the gains m_{1-n} can be redistributed throughout the modulator so that the signal-swing at each integrator's output stays within practical limits for circuit implementation [18]. Finally, to ease layout and to improve the predictability of capacitor ratios, all coefficients are quantized into rational numbers. Slight changes in the NTF pole locations are expected after quantization, but if done properly, the changes should affect the NTF minimally. A step-by-step example of matching an NTF to a modulator topology is available in Chapter 3.

Chapter 2

Existing $\Delta\Sigma$ Loop-Filter Topologies

2.1 Conventional feedforward topologies

The previous chapter looked at the differences between feedforward and feedback modulators. In particular, it explained why the feedforward modulator has a better chance at achieving high-performance in a low OSR design than the feedback modulator. In this section, two conventional feedforward topologies are studied that enable the implementation of NTFs with zeros spread across the passband. Both modulators are similar to the feedforward modulator in Figure 1.8, but they utilize local feedback to move the NTF zeros away from dc. The first topology is the cascade-of-integrators-feedforward form (CIFF) which offers extra speed, but confines zeros to the vertical line that intersects z=1 in the z-plane. The second topology is the cascade-of-resonators-feedforward form (CRFF) which is slower than CIFF but allows zeros to be pinned to the unit-circle for maximum quantization noise suppression. Both topologies have their merits and will be studied here.

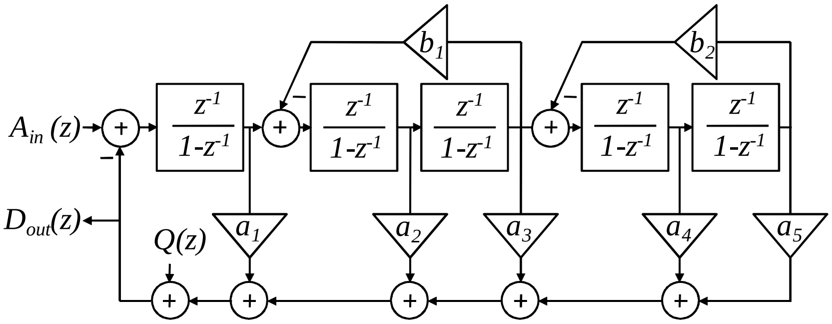

Figure 2.1: 5^{th}-order cascade-of-integrators feedforward form (CIFF).

2.1.1 CIFF

Shown in Figure 2.1 is a 5^{th}-order CIFF $\Delta\Sigma$ modulator. It consists of five delaying (z^{-1}) integrators with two local feedback loops. Since all integrators are delaying, this topology offers the highest speed because the signal does not need to propagate through two or more amplifiers before it is sampled as is the case for CRFF (discussed shortly). Between the basic feedforward modulator shown earlier in Figure 1.8 and CIFF, the only difference is the addition of local feedback. This topology allows NTF zeros to be spread across the passband for enhanced quantization noise suppression similar to the example shown in Figure 1.6. By introducing local feedback around every two consecutive integrators, the zeros originally at dc will migrate to higher frequencies in the z-plane as complex conjugate pairs. The location of the zeros in the z-plane cannot be arbitrarily set, but depend on the topology of the loop-filter. For CIFF, the zeros are restricted to the vertical line that intersects z=1 as depicted in Figure 2.2. The feedback coefficient b_i controls the movement of its associated complex conjugate pair along this vertical line. Each feedback coefficient is responsible for exactly one complex conjugate pair.

Now consider how the NTF zeros move with respect to b_i. One feedback loop of the modulator is isolated as shown in Figure 2.3. The transfer function $\frac{Y(z)}{X(z)}$

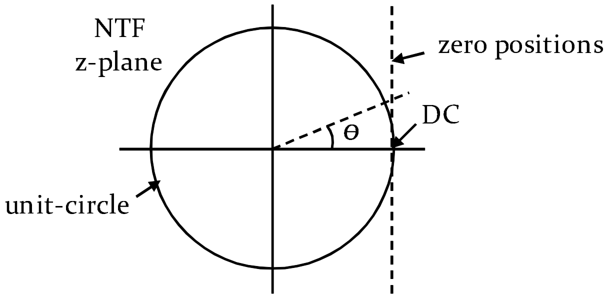

Figure 2.2: Possible NTF zero positions in the z-plane for a CIFF $\Delta\Sigma$ modulator.

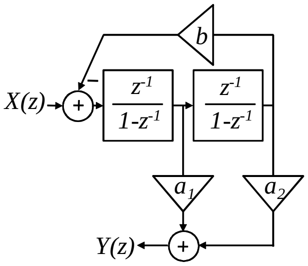

Figure 2.3: Local feedback loop of CIFF.

can be found and is equal to

$$\frac{Y(z)}{X(z)} = \frac{a_1 z^{-1} + (a_2 - a_1)z^{-2}}{1 + 2z^{-1} + (1+b)z^{-2}} \ . \tag{2.1}$$

Since poles of the loop-filter become zeros of the NTF for feedforward modulators (Chapter 1), the poles of $\frac{Y(z)}{X(z)}$ will be the zeros of the NTF. Using the quadratic formula, the pole locations of $\frac{Y(z)}{X(z)}$ (zeros of the NTF) can be determined as a function of b:

$$z = 1 + j\sqrt{b} \tag{2.2}$$

These NTF zeros are confined to the vertical line z=1, and because of this, the zeros are not as effective in pinning down the NTF as they would be if they were on the unit-circle. To see why, recall that the magnitude response for a system with a given set of pole-zero locations can be determined by the dividing the multiplication of the distance to all zeros by the multiplication of the distance to all poles:

$$|H(z)| = \frac{\prod distance\ to\ zeros}{\prod distance\ to\ poles}\ . \tag{2.3}$$

If the zeros are not on the unit-circle, the numerator in (2.3) never becomes zero, therefore the zeros are not as effective. To make matters worse, as the frequency of the zeros on the vertical z=1 line increases, they move further away from the unit-circle, and the notch becomes shallower. This will be studied in detail later in this chapter. The angle θ in Figure 2.2 determines the frequency of the zero-pair. To a good degree, and especially when $\theta \ll 1$, the frequency can be approximated with the following equation:

$$\theta \approx \sqrt{b}\ . \tag{2.4}$$

Later in this section, the effectiveness the zeros of CIFF for different OSRs are examined. When trying to match an NTF equation to a CIFF modulator, the feedback coefficients b_i should be assigned first, then the denominator of the NTF of n^{th} power can be used to solve for the remaining n coefficients (a_i) of the modulator.

2.1.2 CRFF

Shown in Figure 2.4 is a 5^{th}-order CRFF $\Delta\Sigma$ modulator. It is essentially the same as the CIFF modulator except two of the five delaying integrators are replaced by non-delaying integrators. These non-delaying integrators do not sample the input but rely on the previous stage to sample the signal. By cascading one non-delaying integrator with one delaying integrator, the signal is forced to propagate through two integrators in one clock period. This configuration limits speed and is the main drawback of CRFF. On the positive side, because of the non-delaying integrator, the delay around each local feedback loop is reduced to one cycle from two. This

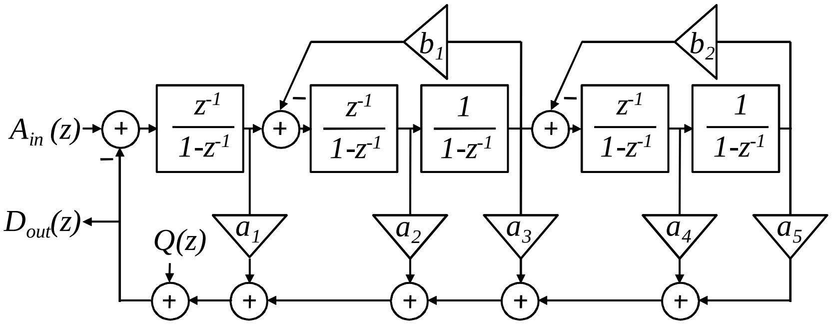

Figure 2.4: 5^{th}-order cascade-of-resonators feedforward form (CRFF).

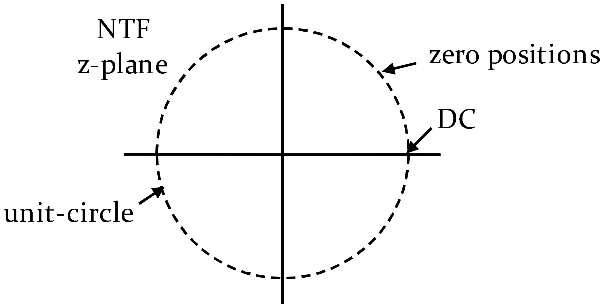

Figure 2.5: Possible NTF zero positions in the z-plane for a CRFF $\Delta\Sigma$ modulator.

speedup around the loop causes the NTF zeros to move around the unit-circle as opposed to moving along the vertical z=1 line as shown in Figure 2.5. Again, the zeros move in complex conjugate pairs, and each pair is controlled by exactly one feedback coefficient b_i similar to CIFF.

To study how the NTF zeros move with respect to b_i, one feedback loop is isolated as shown in Figure 2.6. Its transfer function $\frac{Y(z)}{X(z)}$ can be found and is equal to

$$\frac{Y(z)}{X(z)} = \frac{(a_1 + a_2)z^{-1} - a_1 z^{-2}}{1 + z^{-1}(b-2) + z^{-2}} \ . \tag{2.5}$$

Since the poles of the loop-filter become the zeros of the NTF for feedforward modulators, the poles of $\frac{Y(z)}{X(z)}$ are expected to be the zeros of NTF. Using the quadratic

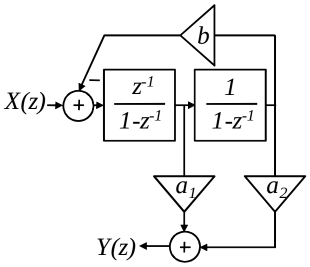

Figure 2.6: Local feedback loop of CRFF.

formula, the pole locations of $\frac{Y(z)}{X(z)}$ (zeros of the NTF) can be determined as a function of b:

$$z = 1 - \frac{b}{2} \pm \frac{\sqrt{b^2 - 4b}}{2} \tag{2.6}$$

If $0 \leq b \leq 4$, the term under the square root is negative, and the pole locations can be rewritten as

$$z = 1 - \frac{b}{2} \pm j\frac{\sqrt{4b - b^2}}{2} \ for\ 0 \leq b \leq\ 4\ . \tag{2.7}$$

These poles are on unit-circle and their angle (frequency) can be calculated using one of the following relationships:

$$\sin\theta = \frac{\sqrt{4b - b^2}}{2} \tag{2.8}$$

$$\cos\theta = 1 - \frac{b}{2} \tag{2.9}$$

The notch of this zero-pair is very deep because the zeros are on the unit-circle. Furthermore, as frequency increases, the effectiveness of the zero-pair remains the same as it will continue to move along the unit-circle. This is the main advantage CRFF has over CIFF. However, due to the speed limitation imposed by non-delaying integrators, most designers still opt for CIFF instead.

2.1.3 CIFF vs. CRFF for different OSRs

The previous two subsections looked at the differences between CIFF and CRFF. In particular, the NTF zeros of CIFF are restricted to the vertical line that intersects z=1 while the zeros of CRFF are always positioned around the unit-circle. The zeros of CIFF are less effective than the zeros of CRFF because their ability to pin down quantization noise diminish as the zeros move towards higher frequencies (lower OSRs). However, CIFF offers speed as it uses only delaying integrators. Here, the NTFs of CIFF and CRFF are compared at 8× and 16× OSR to study the impact of the zeros on the NTF.

Shown in Figure 2.7 are two overlaid NTFs of a CIFF modulator and a CRFF modulator at 16× OSR. Both NTFs are designed with 4-b quantization. Only the passband is shown because the zeros of the NTF is the primary interest here. Both NTFs share the same set of poles and both have a quantization noise gain of 4. The pole locations are designed using the Delta-Sigma Toolbox [9]. The NTFs are given here:

$$NTF_{CIFF(16\times)} = \frac{(1-z^{-1})(1-2z^{-1}+1.013z^{-2})(1-2z^{-1}+1.035z^{-2})}{(1-0.4299z^{-1})(1-0.8894z^{-1}+0.2523z^{-2})(1-1.0207z^{-1}+0.5637z^{-2})} \tag{2.10}$$

$$NTF_{CRFF(16\times)} = \frac{(1-z^{-1})(1-1.987z^{-1}+z^{-2})(1-1.965z^{-1}+z^{-2})}{(1-0.4299z^{-1})(1-0.8894z^{-1}+0.2523z^{-2})(1-1.0207z^{-1}+0.5637z^{-2})} \tag{2.11}$$

Table 2.1: 16× OSR coefficients

	CIFF	CRFF
b_1	0.013	0.013
b_2	0.035	0.035
a_1	2.6600	2.6120
a_2	3.1370	1.6731
a_3	1.9673	1.3380
a_4	0.6332	0.4590
a_5	0.0423	0.0643

A pole-zero plot of these NTFs is shown in Figure 2.8, with the passband zeros magnified to highlight the differences between CIFF and CRFF. Comparing the frequency response plot with the pole-zero plot, it is easy to see the effect of the zeros on the NTF. For CRFF, the zeros are on the unit-circle which translate into deep notches in the frequency response. These notches hold down quantization noise so higher SQNR can be achieved. On the other hand, the zeros of CIFF are not on the unit-circle so the notches are shallower. This is clearly visible by comparing the notch of CIFF with the notch of CRFF in the middle of the passband. Moving up in frequency to the edge of the passband, the CIFF zero-pair has deviated so far from the unit-circle that the intended notch now appears as a momentary plateau that only serves to slow down the rise of the NTF. Nonetheless, discrete-time simulation suggests only a 1-dB difference in SQNR between CIFF (112-dB) and CRFF (113-dB). Mostly likely than not, this mere 1-dB difference justifies choosing CIFF over CRFF for its speed advantage. Listed in Table 2.1 are the coefficients of the CIFF and CRFF modulators discussed here. As a side note, since the main purpose of this analysis is to study the effect of zero-placement on the NTF, no effort was made to gain-scale [18] or quantize the coefficients.

Now consider CIFF and CRFF at 8× OSR. Shown in Figure 2.9 and Figure

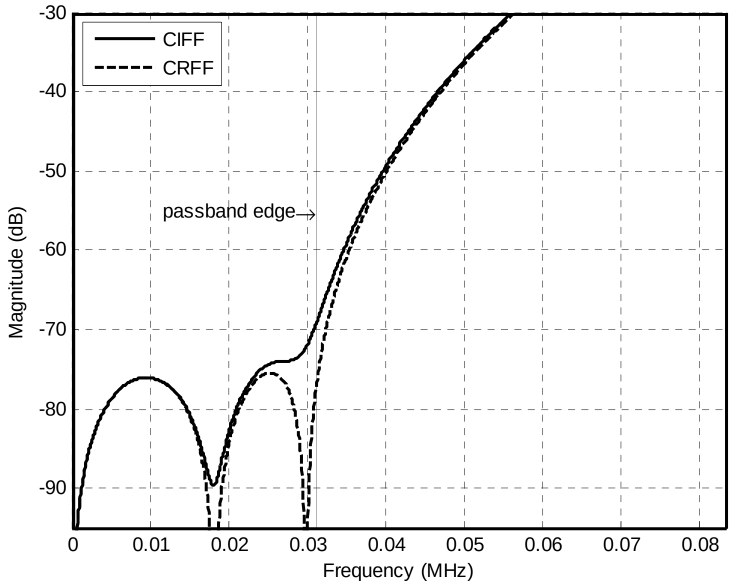

Figure 2.7: Frequency response of CIFF and CRFF at 16× OSR.

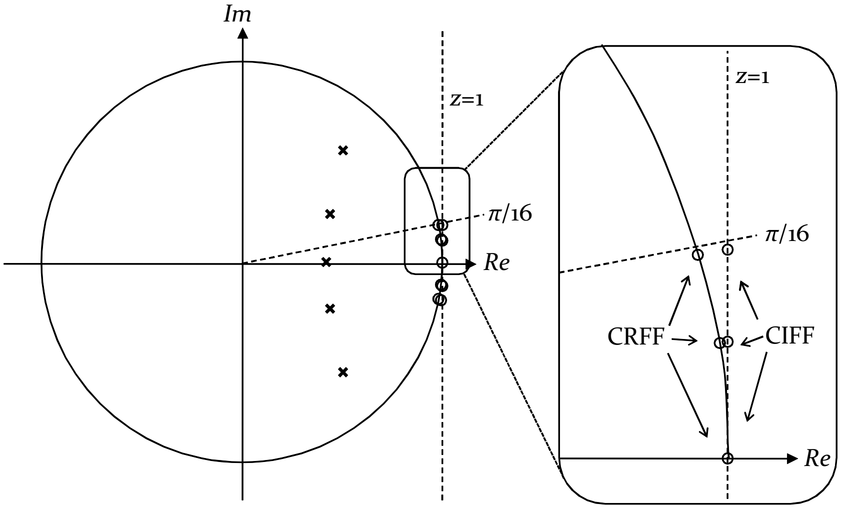

Figure 2.8: Pole-zero plot of CIFF and CRFF at 16× OSR.

2.10 are the frequency response plots and pole-zero plots of the NTFs of CIFF and CRFF, respectively. Again, both NTFs share the same set of poles and have a quantization noise gain 6. Since the OSR is now halved, the passband bandwidth doubles. The NTF of CRFF appears well defined with three deep notches spread across the passband. The NTF of CIFF, on the other hand, has two notches that struggle to pin down the NTF. Most concerning is the intended notch at the edge of the passband where it is almost invisible and seems to have no effect on the NTF in the immediate vicinity of the notch. In discrete-time simulation, a difference of 6-dB in SQNR is observed between CRFF (87.5-dB) and CIFF (81.5-dB), with 4-b quantization assumed. This 6-dB deficit is significantly worse than the 1-dB deficit at 16× OSR, and especially because the peak SQNR here is only 87.5-dB as compared to 113-dB in the 16× case. In other words, the percentage loss in SQNR is much greater here. The coefficients used to generate the plots are summarized in Table 2.2, and the NTFs are listed here:

$$NTF_{CIFF(8\times)} = \frac{(1-z^{-1})(1-2z^{-1}+1.05z^{-2})(1-2z^{-1}+1.125z^{-2})}{(1-0.3466z^{-1})(1-0.6659z^{-1}+0.1626z^{-2})(1-0.6238z^{-1}+0.451z^{-2})} \tag{2.12}$$

$$NTF_{CRFF(8\times)} = \frac{(1-z^{-1})(1-1.952z^{-1}+z^{-2})(1-1.865z^{-1}+z^{-2})}{(1-0.3466z^{-1})(1-0.6659z^{-1}+0.1626z^{-2})(1-0.6238z^{-1}+0.451z^{-2})} \tag{2.13}$$

In practice, designers usually set a margin between the target SNR of the modulator and the SQNR so that quantization noise is at least close to being negligi-

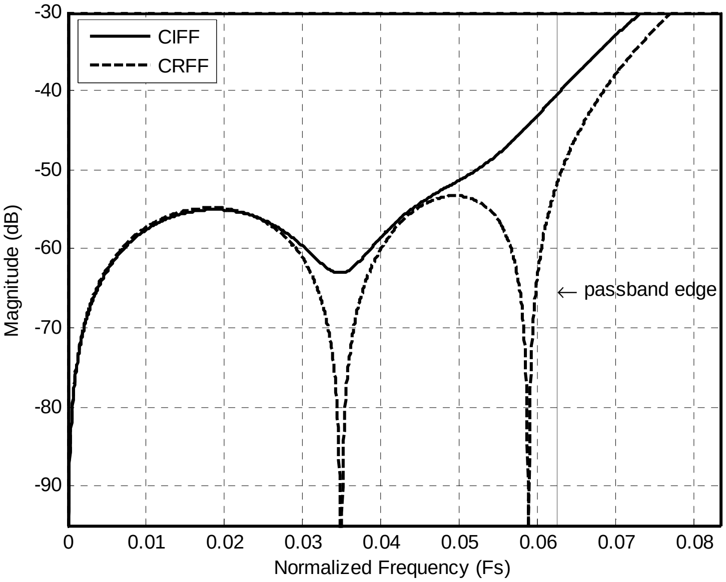

Figure 2.9: Frequency response of CIFF and CRFF at 8× OSR.

ble if not completely negligible in the final noise budget. Here, with only 81.5-dB of SQNR, even a 10-dB margin will put the target SNR at 71.5-dB, which is below 12-b ENOB performance. Therefore, even though CIFF offers speed, it may not qualify as a viable topology in certain low OSR applications due to its low SQNR. The following section looks at Balmelli's modulator, which can alleviate this drawback of CIFF while using strictly delaying integrators.

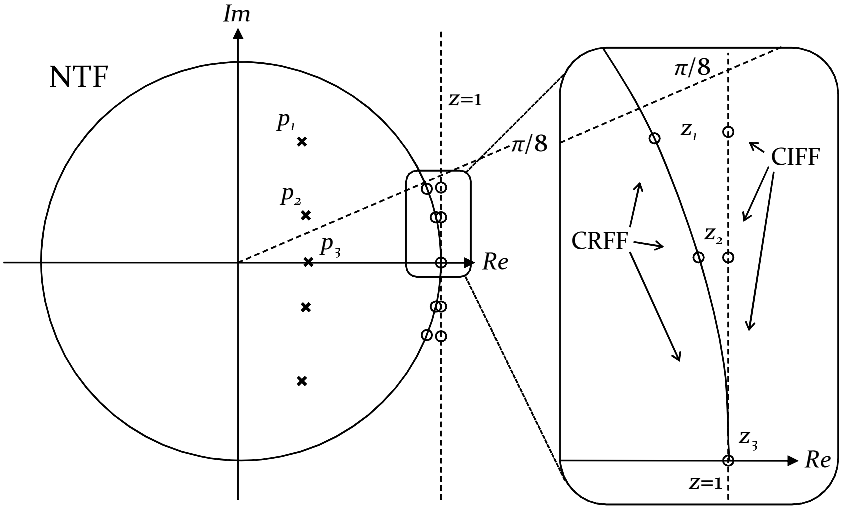

Figure 2.10: Pole-zero plot of CIFF and CRFF at 8× OSR.

Table 2.2: 8× OSR coefficients

	CIFF	CRFF	Balmelli
b_1	0.05	0.048	0.05
b_2	0.125	0.135	0.13475
a_1	3.3637	3.1807	3.2290
a_2	4.7558	2.2061	4.3109
a_3	3.2632	1.9531	2.6676
a_4	0.9779	0.7373	0.6097
a_5	-0.1605	-0.0158	-0.1128

2.2 Low OSR feedforward $\Delta\Sigma$ modulators

This section looks at two modulator topologies in the literature that are suitable for low OSR operation. Both can provide excellent attenuation of quantization noise within the passband at low OSRs, and neither resort to non-delaying integrators. The first is Balmelli's modulator [4], which is similar to CIFF in terms of speed, but has the ability to pin one pair of complex conjugate zeros to the unit-circle. The second is Jiang's modulator [10], which can pin two pairs of quantization noise zeros to the unit-circle, but has the drawback of heavier output loads and lower feedback factors.

2.2.1 Balmelli's $\Delta\Sigma$ modulator

Balmelli introduced a modulator that harnesses the speed advantage of CIFF while maintaining a level of quantization noise suppression comparable to CRFF [4]. The topology is shown in Figure 2.11. All five integrators are delaying, but the 4^{th} and 5^{th} integrators are setup in such a way that the clocking scheme can 'steal' one cycle to speedup the feedback loop around the last two integrators. By reducing the feedback loop delay around the 4^{th} and 5^{th} integrators from two cycles to one, the zero-pair associated with that feedback loop will move around the unit-circle as opposed to the vertical z=1 line. This is the behavior desired because a zero-pair on the unit-circle translates to a deep notch in the NTF frequency response. A sensible design will assign this feedback loop to control the zero-pair nearest to edge of the passband so that the deep notch can be fully exploited to hold down the most critical part of the NTF.

To understand how one clock cycle can be 'stolen', consider Figure 2.12. A cascade of three integrators is shown and are designated as integrators 3, 4, and 5, with outputs labeled as V_3, V_4, and V_5. The input to the cascade is assumed to be the output of integrator 2 (not shown), and is designated as V_2. The timing

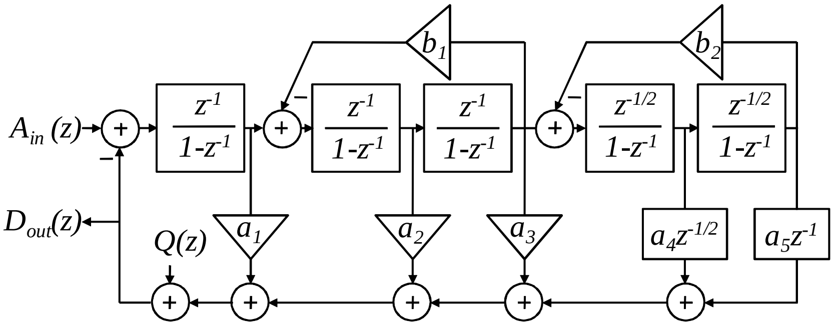

Figure 2.11: Balmelli's modulator.

diagram illustrates how one sample travels down the cascade with respect to the clock phases ϕ_1 and ϕ_2. All integrators operate similarly with one sample phase (ϕ_1) and one charge-transfer phase (ϕ_2). The patterned boxes on the outputs V_{3-5} should be understood as the time when the sample is actively changing (settling). As is, it takes two cycles for the sample at the output of integrator 3 (V_3) to reach the output of integrator 5 (V_5).

Now consider Figure 2.12. The integrators here are the same as the integrators in Figure 2.12 except for swapped sample and charge-transfer phases in integrator 4. As the output of integrator 3 changes, integrator 4 samples V_3 (ϕ_2), and as the output of integrator 4 changes, integrator 5 samples V_4 (ϕ_1). The total delay from V_3 to V_5 is now reduced down to one cycle using this clocking scheme. In Figure 2.11, this technique is depicted as half-cycle delays ($z^{-1/2}$) in the 4^{th} and 5^{th} integrators. It is important to note that this technique is possible only because the sample phase is used as a charge-transfer phase for integrator 4. If during the sample phase the integrators are busy for whatever reason, this technique cannot be applied.

Now compare Balmelli's topology to CIFF and CRFF. To ensure a fair comparison, the pole locations of Balmelli's modulator are redesigned and set equal to the pole locations of CIFF and CRFF at 8× OSR. The resulting NTF is plotted

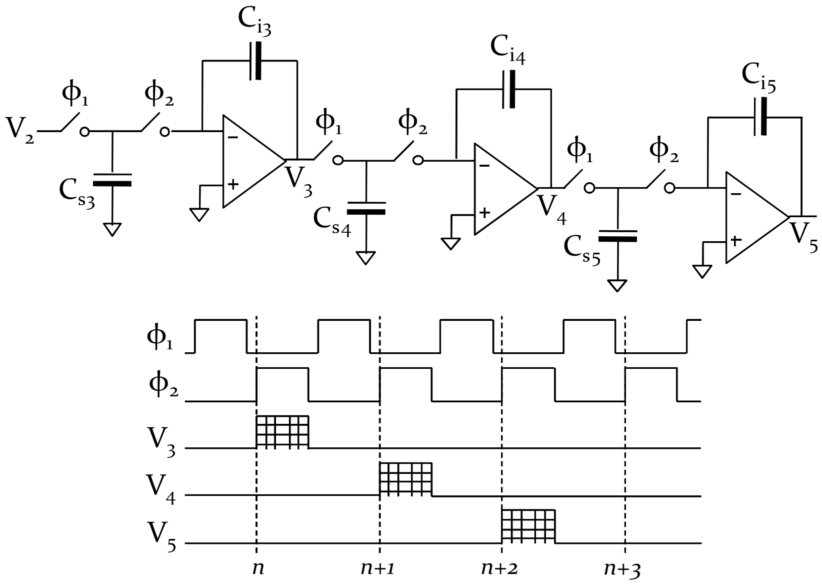

Figure 2.12: Conventional clocking scheme.

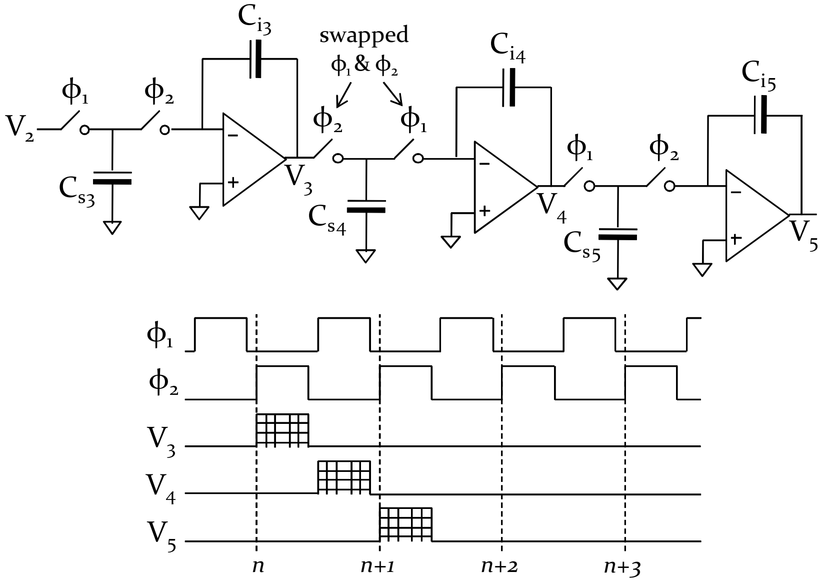

Figure 2.13: Balmelli's modulator clocking scheme for the 4^{th} and 5^{th} integrators.

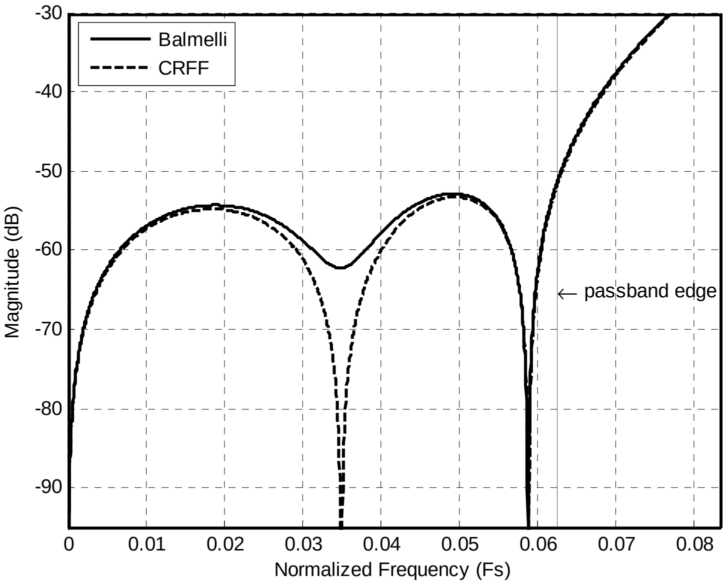

Figure 2.14: Frequency response of Balmelli's modulator at 8× OSR.

in Figure 2.14 together with the NTF of CRFF. The new coefficients for Balmelli's modulator are listed in Table 2.2, with its corresponding pole-zero plot is shown in Figure 2.15. The NTF used for this design is listed here:

$$NTF_{Balmelli} = \frac{(1-z^{-1})(1-2z^{-1}+1.05z^{-2})(1-1.8653z^{-1}+z^{-2})}{(1-0.3466z^{-1})(1-0.6659z^{-1}+0.1626z^{-2})(1-0.6238z^{-1}+0.451z^{-2})} \tag{2.14}$$

According to the frequency response plot, Balmelli's modulator is almost as effective as CRFF in pinning down the NTF. Comparing it to the pole-zero plot, the location of the notch near the edge of the passband can be matched to the complex conjugate zero-pair on the unit-circle in the z-plane. Similarly, the shallow notch in the middle of the passband can be matched to the zero-pair along the vertical

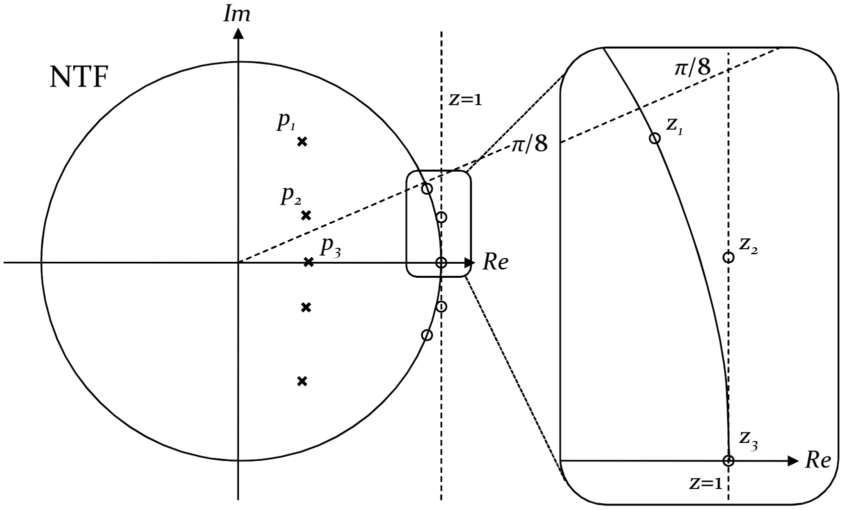

Figure 2.15: Pole-zero plot of Balmelli's modulator at 8× OSR.

z=1 line in the z-plane. Discrete-time simulation suggests that only 1-dB SQNR difference exists between Balmelli's modulator (86.5-dB) and CRFF (87.5-dB). This level of quantization noise suppression without the speed penalty of non-delaying integrators makes this topology very attractive in high-speed low OSR applications.

2.2.2 Jiang's $\Delta\Sigma$ modulator

Jiang introduced a 5^{th}-order modulator that can pin all NTF zeros to the unit-circle using strictly delaying integrators. The concept is based on replacing the cascade of integrators with 2^{nd}-order biquads to obtain the same loop-filter transfer function [10]. Since the NTF zeros are on the unit-circle, Jiang's modulator is capable of excellent passband quantization noise suppression similar to CRFF. Additionally, Jiang cites low coefficient sensitivity and low amplifier dc gain requirements as key advantages of this topology. A linearized model of Jiang's modulator is shown in Figure 2.16.

The main drawback of this topology, however, is the loading on the 1^{st} integrator and low feedback factors for the remaining stages. Since the 1^{st} integrator

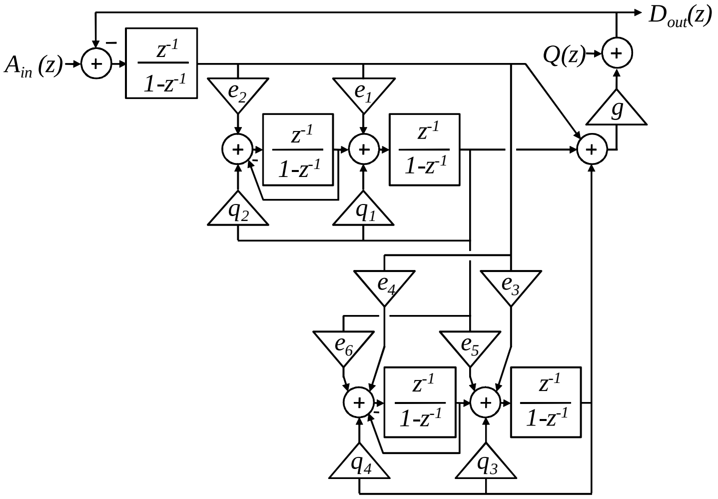

Figure 2.16: Jiang's modulator.

drives four other stages plus the quantizer, the loading is significantly higher than CIFF or CRFF where the 1^{st} integrator only has to drive the 2^{nd} integrator and the quantizer. Interconnect capacitance also play a role in loading down the 1^{st} integrator because the other stages can be far away and spread across different areas of the chip. Besides the 1^{st} integrator, the remaining stages, especially the 4^{th} and 5^{th}, suffer from low feedback factors because of multiple inputs and feedback branches. More on feedback factor will be discussed in Chapter 7. Even though Jiang's modulator offers excellent passband NTF attenuation, its speed penalty makes it difficult to implement in a high-speed design as compared to Balmelli's modulator or CIFF.

Chapter 3

A New and Improved Loop-Filter Topology

In this chapter, a new loop-filter topology especially suited for high-speed low OSR operation is introduced. The design methodology is discussed, followed by a comparison with existing topologies, namely, CIFF, CRFF and Balmelli's modulator. Results show that this new loop-filter can provide a level of quantization noise suppression comparable to CRFF and has a coefficient sensitivity in par with CIFF and Balmelli's modulator.

3.1 A new 5^{th}-order $\Delta\Sigma$ loop-filter

The previous chapter analyzed Balmelli's modulator and showed that it simultaneously offers the speed advantage of CIFF and the quantization noise suppression performance of CRFF. However, Balmelli's modulator uses both sampling and charge-transfer phases of the clock to speed up the delay around the feedback loop in the last two stages of the loop-filter. This was done so to move a pair of NTF complex conjugate zeros from the vertical z=1 line to the unit-circle to enhance

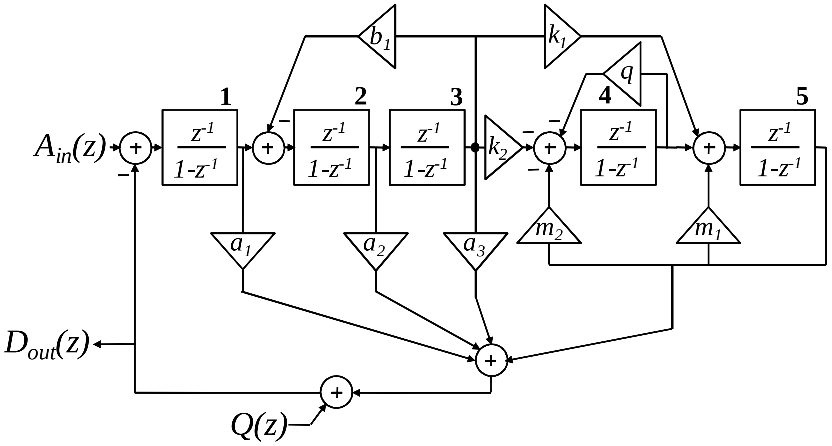

Figure 3.1: The proposed modulator.

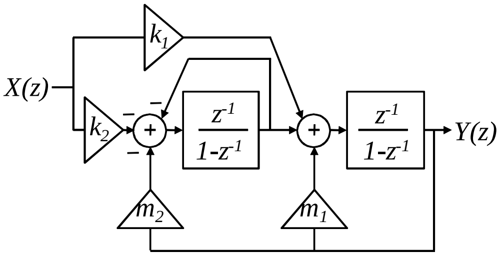

Figure 3.2: Jiang's biquad cell.

quantization noise suppression in the passband. Here, a new loop-filter is introduced that does not require the use of both phases of the clock to move the zeros to the unit-circle. The benefits of this will become clear in the next two chapters when discussion on *double-sampling* begins.

A linearized model of the proposed loop-filter is shown in Figure 3.1. The loop-filter uses five delaying integrators to realize an NTF with five poles and five zeros. Of the five zeros, one is located at dc, two are spread along the vertical line in the z-plane that intersects z=1 as a complex conjugate pair, and two are on the unit-circle, again as a complex conjugate pair. This configuration of zero-placement, as shown earlier with Balmelli's modulator, offers excellent passband quantization noise suppression comparable to CRFF.

The first three stages of the proposed loop-filter, similar to CIFF, consists of three cascaded delaying integrators and local feedback around the 2^{nd} and 3^{rd} integrators. The feedback coefficient, b_1, is responsible for positioning the zero-pair along the vertical z=1 line. Since the first three stages are similar to the first three stages of CIFF, it is expected to offer the same high-speed properties as CIFF. Beyond the 3^{rd} integrator, the last two stages essentially form an IIR biquad cell similar to the biquad cell proposed by Jiang [10]. The author noticed that Jiang's biquad cell, shown in Figure 3.2, has a transfer function that may allow it to replace the last feedback loop of a CRFF modulator. This has significant implications because if a replacement can be found for the CRFF feedback loop using strictly delaying integrators, potential speed improvement is possible without the loss of quantization noise suppression performance. The transfer function of Jiang's biquad is equal to

$$\frac{Y(z)}{X(z)} = \frac{k_1 z^{-1} + k_2 z^{-2}}{1-(1+m_1)z^{-1} + m_2 z^{-2}} \ . \tag{3.1}$$

Comparing (3.1) to CRFF's feedback loop transfer function (2.5, repeated here):

$$\frac{Y(z)}{X(z)} = \frac{(a_1+a_2)z^{-1} - a_1 z^{-2}}{1+z^{-1}(b-2)+z^{-2}} \ ,$$

it is immediately clear that the biquad and the feedback loop can be interchanged if m_2 and q are set to unity and the rest of the coefficients are matched. Taking this one step further, from the discussion of Balmelli's modulator, only one complex conjugate zero-pair is needed on the unit-circle to effectively pin down the NTF. Therefore, instead of substituting this biquad for the last two stages of a CRFF modulator, it is substituted for the last two stages of a CIFF modulator for additional speed. The result is the proposed modulator in Figure 3.1.

As an additional benefit of this loop-filter, instead of having five feedforward

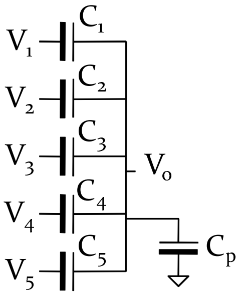

Figure 3.3: Passive summation.

paths for a 5^{th}-order loop-filter, this loop-filter only has four feedforward paths. With one less path, it offers a meaningful improvement in signal swing at the summing node that precedes the quantizer if passive summation is employed. This in turn can relax the quantizer's offset specification. An example passive summation network with five input signals is shown in Figure 3.3. The output voltage is given by

$$V_o = \frac{\displaystyle\sum_{i=1}^{5} V_i C_i}{C_p + \displaystyle\sum_{i=1}^{n} C_i} = \frac{C_1V_1 + C_2V_2 + C_3V_3 + C_4V_4 + C_5V_5}{C_p + C_1 + C_2 + C_3 + C_4 + C_5} \tag{3.2}$$

where C_p represents any parasitic capacitance at the summing node. To see how the output signal swing can be improved with one less input branch, C_p is omitted, and hypothetically it is assumed that all summing capacitors are of the same size i.e., C=C_1= ... =C_5. This leads to the following expression at the output:

$$V_o = \frac{C(V_1 + V_2 + V_3 + V_4 + V_5)}{5C} = \frac{V_1 + V_2 + V_3 + V_4 + V_5}{5}\ . \tag{3.3}$$

With one less branch, and assuming C_5V_5 is removed, the output equals

$$V_o = \frac{C(V_1 + V_2 + V_3 + V_4)}{4C} = \frac{V_1 + V_2 + V_3 + V_4}{4}\ . \tag{3.4}$$

Now the key is, since the modulator's stability is determined by when the quantizer saturates, this means the numerator of (3.3) and (3.4) will have the same maximum signal swing regardless of topology. For this reason, having one less feedforward path does indeed improve signal swing at the summing node. In the above example, the signal swing improves by 25%. In a practical modulator, the feedforward coefficients are usually not all equal to each other, so the signal swing improvement will vary from modulator to modulator.

3.2 Design methodology

The goal in this section is to show how the proposed loop-filter in Figure 3.1 can be designed to match a target NTF with five poles and five zeros. Similar to CIFF and CRFF, the first step is to determine the coefficients that position the zeros. For this topology, the zeros are controlled by b_1 and m_1. Here, m_1 is used to position the zero-pair near the edge of the passband (because this zero-pair is on the unit-circle) so that maximum attenuation can be achieved. The term b_1 is used to position the lower frequency zero-pair because it is not on the unit-circle and will have less attenuation at higher frequencies. According to Chapter 1, the zero-pair frequency associated with b_1 can be approximated if $\theta \ll 1$, where θ is the angle on the unit-circle in radians:

$$\theta \approx \sqrt{b_1} \ . \tag{3.5}$$

To find the value of m_1, the denominator of (3.1) is used. Using the quadratic formula, the solutions to z are found, assuming m_2=1:

$$z = \frac{1+m_1}{2} \pm \frac{\sqrt{(1+m_1)^2-4}}{2} \ . \tag{3.6}$$

For the term under the square root of (3.6) to generate an imaginary component, the argument must be negative, which means $0 \leq (1+m_1)^2 \leq 4$. Therefore, (3.6) can be rewritten as

$$z = \frac{1+m_1}{2} \pm j\frac{\sqrt{4-(1+m_1)^2}}{2} \quad for \ -3 \leq m_1 \leq \ 1. \tag{3.7}$$

These zeros are always on unit-circle and its angle (frequency) can be calculated using one of the following relationships:

$$\sin\theta = \frac{\sqrt{4-(1+m_1)^2}}{2} \tag{3.8}$$

$$\cos\theta = \frac{1+m_1}{2} \tag{3.9}$$

Now that b_1, m_1, and m_2 are determined, the last five coefficients, namely, a_1, a_2, a_3, k_1, and k_2 can be found. With the help of a computer, the NTF of the proposed modulator can be easily obtained:

$$NTF = \frac{N(z)}{D(z)} \tag{3.10}$$

where

$$N(z) = (1-z^{-1})(1-2z^{-1}+(1+b_1)z^{-2})(1+(-1-m_1)z^{-1}+z^{-2}) \tag{3.11}$$

and

$$\begin{aligned} D(z) = & \\ & 1+(a_1-m_1-4)z^{-1}+(7+a_2+b_1-a_1m_1-3a_1+3m_1)z^{-2} \\ & +(a_1b_1-b_1m_1-7-3m_1+2a_1m_1-2b_1+4a_1-2a_2+a_3-a_2m_1)z^{-3} \\ & +(4-a_1b_1-3a_1+2a_2-a_3-a_3m_1+a_2m_1+b_1m_1-a_1m_1+k_1+ \\ & +2b_1-a_1b_1m_1+m_1)z^{-4} \\ & +(-1+a_1b_1+a_1-a_2+a_3-k_2-b_1)z^{-5} \end{aligned} \tag{3.12}$$

Substituting in the values for b_1, m_1, and m_2, *N(z)* and *D(z)* become

$$N(z) = (1 - z^{-1})(1 - 2z^{-1} + 1.05z^{-2})(1 - 1.8653z^{-1} + z^{-2}) \ , \tag{3.13}$$

and

$$\begin{aligned} D(z) = & \\ & 1 + (a_1 - 4.865)z^{-1} + (a_2 - a_1 3.865 + 9.645)z^{-2} \\ & +(a_3 - a_2 2.865 + a_1 5.78 - 9.7383)z^{-3} \\ & +(k_1 - a_3 1.865 + a_2 2.865 - a_1 3.9583 + 5.0083)z^{-4} \\ & +(-k_2 + a_3 - a_2 + a_1 1.05 - 1.05)z^{-5} \ . \end{aligned} \tag{3.14}$$

For comparison purposes, the target NTF of this modulator is set to position the poles at the same locations as the 8× OSR CIFF, CRFF modulators in the previous chapter. Since the zero pattern is akin to Balmelli's modulator (one zero at dc, one zero-pair on the unit-circle, and one zero-pair on the vertical z=1 line), the zeros are positioned at the same locations as Balmelli's modulator:

$$NTF_{target} = \frac{(1 - z^{-1})(1 - 2z^{-1} + 1.05z^{-2})(1 - 1.8653z^{-1} + z^{-2})}{(1 - 0.3466z^{-1})(1 - 0.6659z^{-1} + 0.1626z^{-2})(1 - 0.6238z^{-1} + 0.451z^{-2})} \ . \tag{3.15}$$

Writing the denominator in terms of negative powers of z gives

$$NTF_{target} = \frac{(1 - z^{-1})(1 - 2z^{-1} + 1.05z^{-2})(1 - 1.8653z^{-1} + z^{-2})}{1 - 1.636z^{-1} + 1.476z^{-2} - 0.7584z^{-3} + 0.2126z^{-4} - 0.02542z^{-5}} \ . \tag{3.16}$$

Table 3.1: The proposed modulator

Coefficient	Value
b_1	0.05
m_1	0.865
m_2	1
a_1	3.2287
a_2	4.3099
a_3	2.6659
k_1	0.6083
k_2	0.7215
q	1

Comparing the denominator of (3.16) with (3.14), like powers of z^{-1} are matched and a_1, a_2, a_3, k_1, and k_2 are found with a simultaneous equation solver. The results are listed in Table 3.1. The NTF and STF are plotted in Figure 3.4. As expected, the NTF and STF, due to the feedforward configuration, are coupled at high frequencies. This coupling resulted in an out-of-band STF gain of 5 at $\frac{F_s}{2}$. The quantization noise gain is 6, which matches the original design objective. Taking a closer look at the passband NTF response in Figure 3.5, there are two very deep notches, one at dc and the other near the edge of the passband. Comparing the frequency response to the pole-zero plot in Figure 3.6, the location of these notches can be verified with the positions of the zeros on the unit-circle in the z-plane. The zero-pair along the vertical z=1 line falls in the middle of the passband and its notch is not as deep as the other zero-pair, but nonetheless provides meaningful quantization noise suppression due to its close proximity to the unit-circle.

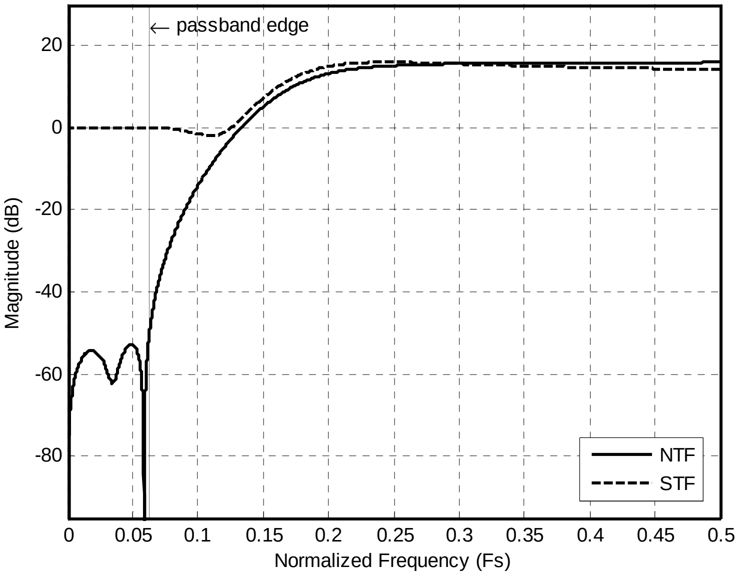

Figure 3.4: NTF and STF.

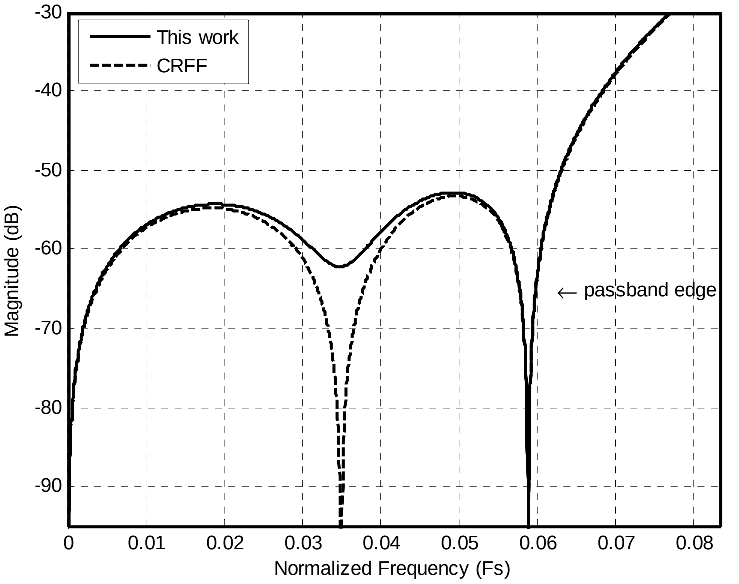

Figure 3.5: The proposed modulator.

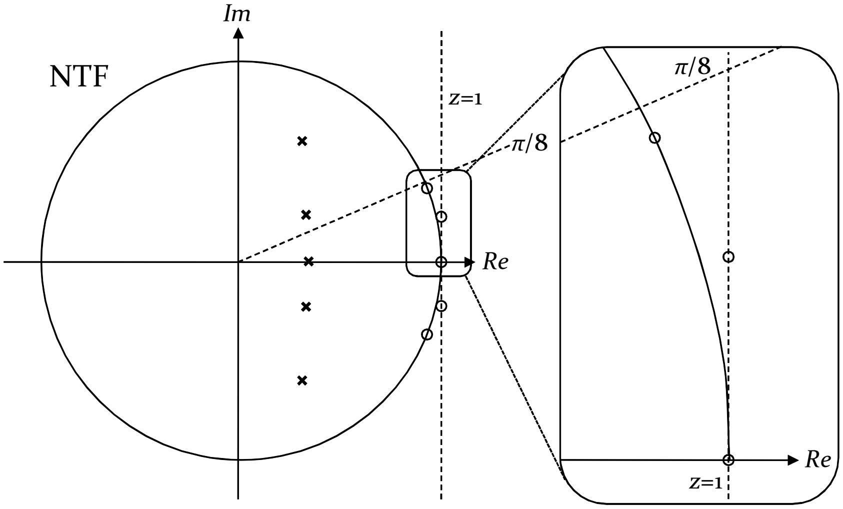

Figure 3.6: Pole-zero plot of the proposed topology.

3.3 Coefficient sensitivity

In this section, the sensitivity of poles and zeros of the proposed topology is studied with respect to changes in the loop-filter's coefficients. In a manufacturing environment, capacitor ratios can deviate from their intended value due to natural variations in the manufacturing process. The less sensitive the loop-filter is, the more tolerant it is to defects and the easier it is to quantize the coefficients into rational numbers to aid the layout process. Therefore, it is important to develop a sense of how much variation to expect and compare it to existing topologies to gauge the modulator's robustness.

Here, sensitivity is taken to mean how much a pole or zero moves with respect to a small perturbation of a particular loop-filter coefficient. The analysis here does not take into account the location of the pole or zero with respect to the unit-circle. For high-Q poles or zeros that are close to the unit-circle, the reader should understand that even slight movements can cause drastic changes in the magnitude or phase response. On the other hand, movement of lower Q poles or zeros that are far away from the unit-circle will see a much smaller impact on the magnitude or phase response. Nonetheless, since all the modulators studied here implement the same set of pole locations, and because the Q of the poles are not high, the comparison between the modulators is valid. It is true that a particular topology may have poles that move in such a way that cancels the movement of other poles. This is not analyzed here because the goal is to obtain a first-order quantitative result.

Now turn to Figure 3.7 to study the methodology used here. The plot shows five poles and five zeros that represent the z-plane of a hypothetical NTF with pole-zero locations similar to the modulators discussed earlier. One pole is depicted to move from p_1 to p_1' over a distance ΔL, presumably due to a small change in one of the coefficients (in a real modulator, the complex conjugate will move as well). Here,

Table 3.2: The proposed modulator coefficient sensitivity

	p_1	p_2	p_3	z_1	z_2	z_3
b_1	0.68	5.25	9.56	0	0.109	0
m_1	3.43	28.7	50.9	1.20	0	0
m_2	5.92	82.3	168	1.38	0	0
a_1	14.1	71.2	117	0	0	0
a_2	20.7	123	202	0	0	0
a_3	13.9	109	202	0	0	0
k_2	5.01	57.0	113	0	0	0
k_1	2.84	19.4	32.9	0	0	0
q	6.14	80.1	161	1.38	0	0

sensitivity is defined as the percentage change in the pole's location ($\frac{\Delta L}{L}$) divided by the percentage change in the value of the coefficient of interest ($\frac{\Delta x}{x}$):

$$S_x^{p_1} = \frac{\Delta L/L}{\Delta x/x} \tag{3.17}$$

Using this definition of sensitivity, the modulators discussed earlier including the proposed modulator, CIFF, CRFF, and Balmelli's modulator are analyzed. The results are listed in Tables 3.2, 3.3, 3.4, and 3.5.

Results indicate that CRFF is the least sensitive of all in terms of pole sensitivity and CIFF appears to be the most sensitive. The proposed modulator and Balmelli's modulator fall in between CRFF and CIFF and are relatively similar. Therefore, the proposed modulator offers the same type of robustness expected of conventional single-loop feedforward $\Delta\Sigma$ modulators.

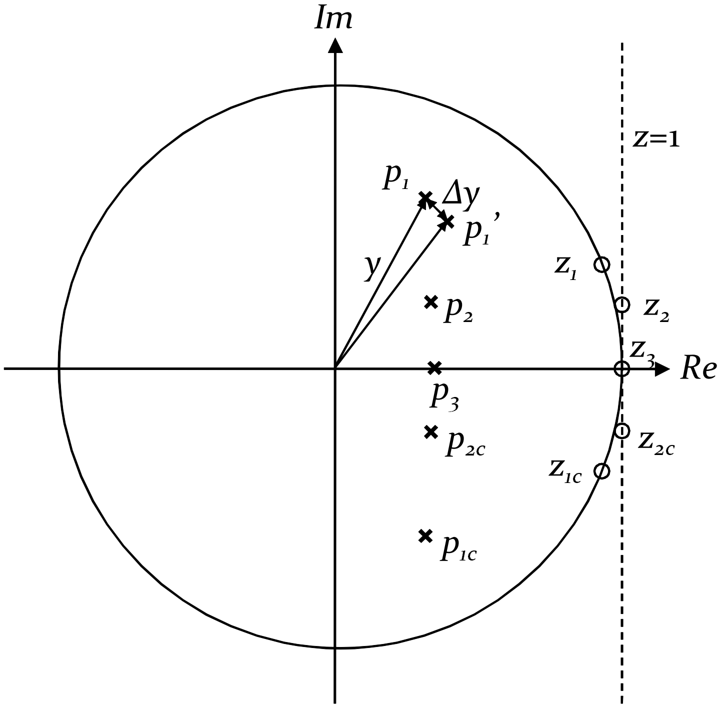

Figure 3.7: First-order coefficient sensitivity analysis.

Table 3.3: CIFF coefficient sensitivity

	p_1	p_2	p_3	z_1	z_2	z_3
b_1	0.81	6.42	11.7	0	0.109	0
b_2	1.03	13.87	28.3	0.167	0	0
a_1	16.6	86.4	143	0	0	0
a_2	25.9	158	257.1	0	0	0
a_3	19.2	156	290.1	0	0	0
a_4	6.19	54.4	99.2	0	0	0
a_5	1.11	12.7	25.1	0	0	0

Table 3.4: CRFF coefficient sensitivity

	p_1	p_2	p_3	z_1	z_2	z_3
b_1	0.29	3.28	4.91	0	0.06	0
b_2	0.37	1.76	2.61	0.19	0	0
a_1	13.3	65.7	107	0	0	0
a_2	10.6	63.2	105	0	0	0
a_3	6.88	32.1	50.2	0	0	0
a_4	3.13	16.6	26.2	0	0	0
a_5	0.05	0.20	0.30	0	0	0

Table 3.5: Balmelli's modulator coefficient sensitivity

	p_1	p_2	p_3	z_1	z_2	z_3
b_1	0.68	5.25	9.55	0	0.109	0
b_2	0.54	4.47	7.88	0.19	0	0
a_1	14.1	71.2	117	0	0	0
a_2	20.7	123	202	0	0	0
a_3	13.9	109	202	0	0	0
a_4	3.86	33.9	62.1	0	0	0
a_5	0.78	8.9	17.6	0	0	0

3.4 Integrator output swing

In the design of a practical $\Delta\Sigma$ modulator, it is important to analyze the signal swing of integrators within the loop-filter. This is because real amplifiers have a limited output range and the signal must be able to fit within this range. Gain-scaling [18] is a technique commonly used to spread the signal swing across different parts of the modulator. Here, the proposed modulator is compared with the different topologies discussed earlier. Discrete-time simulation is used to observe the peak positive and negative sample of each integrator for each topology over a range of different input amplitudes. The difference between the peak positive and negative sample of an integrator is practically the output swing of the integrator needed to process the signal without saturation. A 4-b quantizer is used for all simulations. The results are shown in Figures 3.8, 3.9, 3.10, and 3.11, for the proposed modulator, CIFF, CRFF, and Balmelli's modulator, respectively.

The horizontal axis is the input signal swing normalized to the reference voltage. The vertical axis is the output swing experienced by each integrator normalized to the reference voltage. For the proposed modulator, Figure 3.8 indicates that as the input amplitude increases, the output swing of the individual integrators remain roughly constant over the entire input signal range where the modulator is stable. At around -12dB input amplitude, the quantizer saturates and the modulator becomes unstable. Compared to the other topologies, the proposed modulator actually has an advantage because none of its integrators have an output swing that grows with the input. For CIFF, CRFF, and Balmelli's modulator, gain-scaling must performed on the 5^{th} integrator to relax its output swing for practical implementation. One may ask how much normalized output swing can be tolerated. The answer depends on the amplifier topology used to implement the integrator and the power supply voltage available. If a telescopic amplifier is used in a low supply environment, the tolerable signal swing may be very small due to cascoding and the extra tail cur-

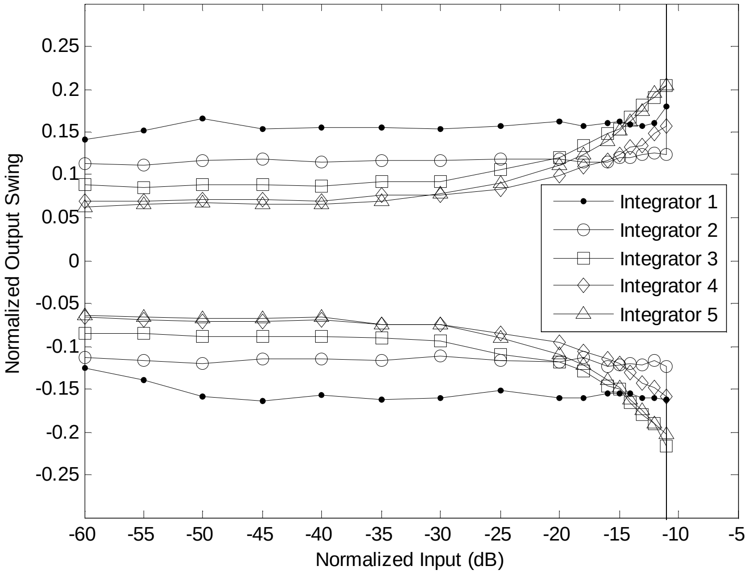

Figure 3.8: The proposed modulator's output swing for different integrators.

rent source. Substituting in a two-stage amplifier can possibly double the tolerable output swing.

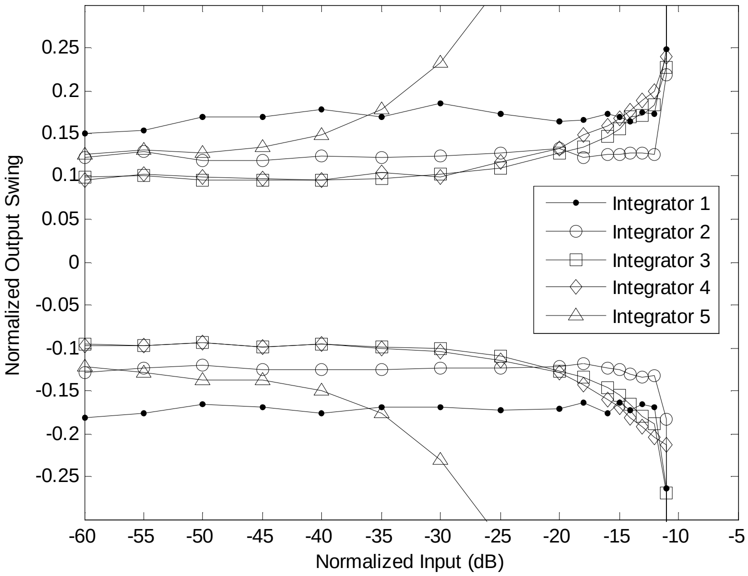

Figure 3.9: CIFF output swing for different integrators.

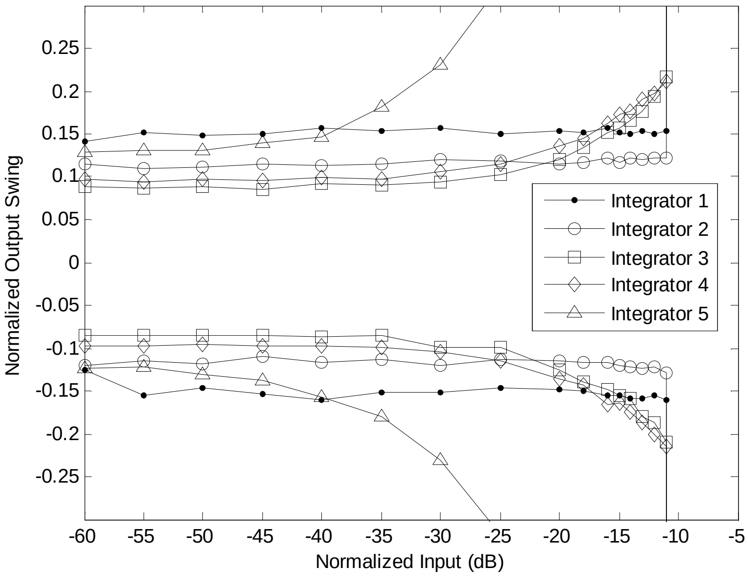

Figure 3.10: CRFF output swing for different integrators.

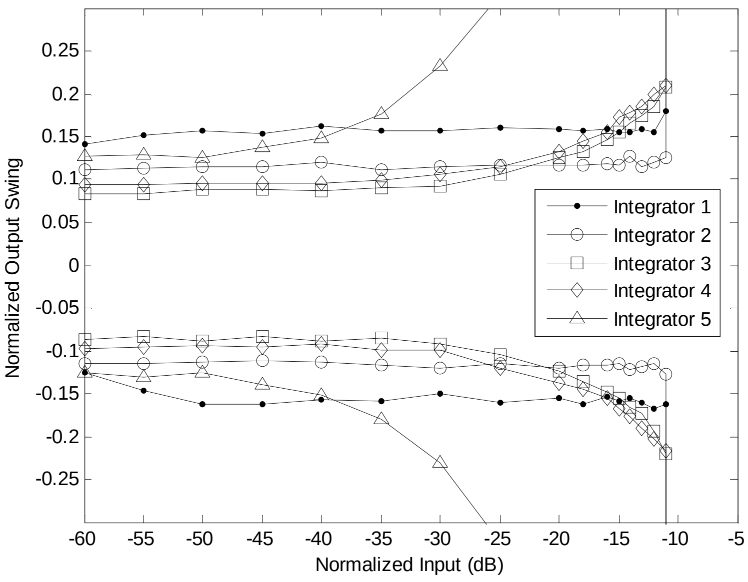

Figure 3.11: Balmelli's modulator output swing for different integrators.

Chapter 4

Double-Sampled $\Delta\Sigma$ A/D Conversion

4.1 Basic concept and advantages of double-sampling

In conventional $\Delta\Sigma$ modulators, sampling and charge-transfer are separated by two non-overlapping clock phases. To increase throughput, it is possible to use two sets of sampling capacitors in a time-interleaved manner to achieve twice the effective sampling-rate without increasing power consumption. This assumes the conventional modulator has a 50-50 duty-cycle clock.

Shown in Figure 4.1 and Figure 4.2 are two integrators with the same effective sampling-rate. The first is a conventional integrator, which is referred to as the single-sampled integrator. There is only one sampling capacitor, and the sampling and charge-transfer functions are separated in time. The second is the double-sampled integrator with two time-interleaved sampling capacitors. At any time other than the non-overlapping period, there is always one sampling capacitor transferring charge to the integrating capacitor. A setup like this, with a clock that is half the original frequency, doubles the amount of time available for the amplifier to settle,

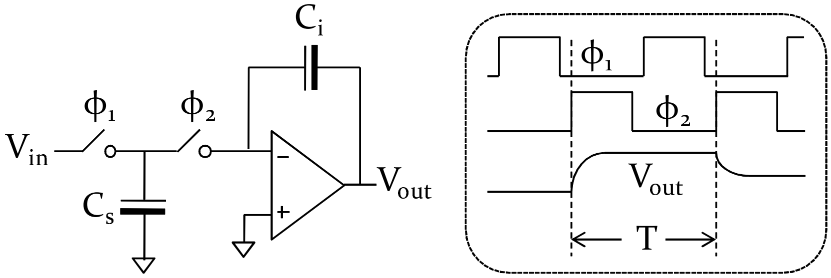

Figure 4.1: Single-sampled integrator.

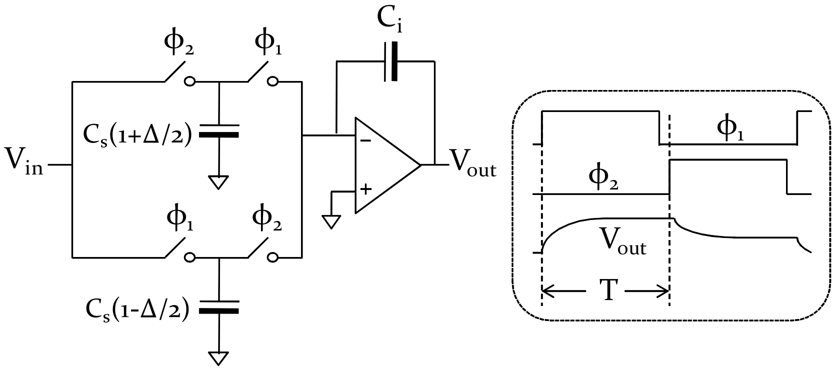

Figure 4.2: Double-sampled integrator.

significantly relaxing the speed requirements of the amplifier and leads to lower power consumption. If on the other hand a higher sampling-rate is desired, the clock can be kept the same, so the effective sampling-rate is doubled, ideally without additional power. Again, this assumes the original clock has a 50-50 duty-cycle.

In Figure 4.2, a slight mismatch of $\Delta \cdot C_s$ is purposely added to emphasize random variations in the manufacturing process that can potentially affect the modulator's performance. The following sections look at how this mismatch mechanism manifests itself at the modulator's output and what techniques can be used to circumvent this non-ideality. As a side note, the sampling networks shown in Figure 4.1 and Figure 4.2 are sensitive to parasitic capacitance of both the switches and the sampling capacitor itself. In practice, a parasitic insensitive configuration [35] should be used instead.

4.2 Limitations of double-sampling

There are two main non-idealities that limit the performance of double-sampled $\Delta\Sigma$ modulators. The first is the mismatch between two sampling capacitors (ΔC_s) as illustrated earlier in Figure 4.2. This mismatch causes any signal energy around the Nyquist frequency to be mixed down to the passband. The second is the systematic mismatch between the two double-sampled phases of the clock. If the clock's duty-cycle is not split exactly 50-50, signal energy around the Nyquist frequency can be mixed down to the passband. Here, both non-idealities are discussed separately to the extent which they limit the performance of the modulator.

4.2.1 Sampling-capacitor mismatch

In a double-sampling modulator, when a mismatch exists between two sampling capacitors such as that shown in Figure 4.2, any signal energy near the Nyquist frequency at V_{in} will be attenuated and mixed down to the passband. This can be understood by finding an expression for the output of the integrator at time instant $(n+1)T$:

$$V_{out}((n+1)T) = V_{out}(nT) + \frac{C_s}{C_i} V_{in}(nT) + (-1)^n \frac{\Delta C_s}{2C_i} V_{in}(nT) \tag{4.1}$$

The first two terms are basically the operation of the integrator. The last term is a result of alternately sampling the input through the mismatched capacitors $+\Delta C_s/2$ and $-\Delta C_s/2$. The term $(-1)^n$ can be viewed as a tone at $\frac{F_s}{2}$. If $V_{in}(nT)$ has energy near $\frac{F_s}{2}$, it will be mixed down to the passband by this tone. Therefore, it is important to make sure the input signal is properly lowpass filtered to prevent such unintended signals to appear in the passband.

To put this mismatch mechanism into perspective, assume a Δ of 0.1% exists between the pair of sampling capacitors. If the interstage gain of the integrator is 0.5 ($2C_s=C_i$), then the signal near Nyquist will appear at the passband attenuated by 72-dB according to (4.1). If a 3^{rd}-order anti-aliasing filter with a constant -60-dB/decade attenuation precedes the modulator, then assuming an 8× OSR, the intruding signal will be further knocked down by another ~45-dB, reaching a total attenuation of 117-dB. This dynamic range is well beyond the maximum performance of the modulator's target. However, in the global feedback path of a $\Delta\Sigma$ modulator, there is significant amount of quantization noise near the Nyquist frequency which do not benefit from the filtering of the external anti-aliasing filter. From the calculation above, this feedback signal (quantization noise) will see an attenuation of only 72dB. Mixed down to the passband, if the attenuation is inadequate, the total passband noise will increase, leading to a reduction in dynamic range. The amount of attenuation needed depends on the energy of the quantization noise in the feedback path and the target dynamic range of the modulator. With multi-bit quantization, the quantization noise energy can be significantly reduced which can alleviate the amount of attenuation needed. Nonetheless, Senderowicz [5] introduced a feedback topology termed the *fully-floating* feedback network, which elegantly desensitizes a double-sampled $\Delta\Sigma$ modulator from mismatch in the feedback capacitors. We will study this feedback network in the next section.

4.2.2 Systematic clock mismatch

In a double-sampled $\Delta\Sigma$ modulator, sampling of the input happens on both phases of the clock. If the clock is not split exactly 50-50, an attenuated version of the input signal near the Nyquist frequency will be mixed down to the passband, similar to sampling capacitor mismatch. This non-ideality only affects the input signal and not the global feedback path of the modulator because the feedback path is assumed to settle before the end of the clock period.

To see how the input signal is mixed down to the passband, assume the input is a pure sinusoid at frequency f_{in}. If the sinusoid is sampled by a clock with systematic error, Δ_T, such that

$$T_{\phi_1} = T + \frac{\Delta_T}{2} \tag{4.2}$$

and

$$T_{\phi_2} = T - \frac{\Delta_T}{2} \tag{4.3}$$

then, the sampled input at time instant (nT) is equal to [25]

$$\begin{aligned} V_{in}(nT) = & \\ & A\cos(2\pi f_{in} nT)\cos(2\pi f_{in}\frac{\Delta_T}{2}) \\ & -A\sin(2\pi f_{in} nT)(-1)^n \sin(2\pi f_{in}\frac{\Delta_T}{2}) \end{aligned} \tag{4.4}$$

where T is the nominal sampling period and A is the amplitude of the input signal. If $\Delta_T/T \ll 1$, the first term is approximately A$\cos(2\pi f_{in} nT)$ because $\cos(2\pi f_{in}\frac{\Delta_T}{2})$ ≈ 1. Therefore, the original signal is minimally affected by systematic mismatch in the sampling process. However, in the second term, because of the alternating multiplier (-1)^n, an attenuated and phase-shifted version of the input signal near $\frac{F_s}{2}$ is mixed down to the passband. If the the attenuation factor, $\sin(2\pi f_{in}\frac{\Delta_T}{2})$, is inadequate, the dynamic range of the modulator can be compromised. For instance, if the goal is to achieve 80dB of dynamic range, and the clock has a systematic phase mismatch of 0.5%, i.e. Δ_T/T=0.005, then the term $\sin(2\pi f_{in}\frac{\Delta_T}{2})$, assuming $f_{in} \approx \frac{F_s}{2}$, is equal to $\sin(\frac{\pi}{2}\cdot 0.005) \approx \frac{\pi}{2}\cdot 0.005$. This translates to 42-dB of attenuation, which means an additional 38-dB is needed to reach the target of 80-dB. With a preceding anti-aliasing filter, this should not pose a problem because as a point of reference, a 3^{rd}-order Butterworth filter offers ≥45-dB of attenuation for signals around $\frac{F_s}{2}$, assuming an 8× OSR. The above example assumed the intruding signals near $\frac{F_s}{2}$ are at full-scale. If the magnitude of these signals are lower or are attenuated by other filters that precede the anti-aliasing filter, then the constraints on the clock can be relaxed.

To achieve a systematic clock mismatch of 0.5%, consider some realistic numbers for a 0.18-μm CMOS process and go through an example. Assume an input clock with frequency F_s is available. This clock is divided down to generate two non-overlapping clock phases, ϕ_1 and ϕ_2, with frequency $\frac{F_s}{2}$. Since both ϕ_1 and ϕ_2 are triggered off the same edge of the original F_s clock, the error between the phases mainly arise from the V_{TH} mismatch of inverters that makeup the clock tree. If the traveling clock edge has a slope of 1.8-V/100-ps, and a 3-σ V_{TH} mismatch of 100-mV, the 3-σ error per inverter, Δ_T'', equals

$$\Delta_T'' = \frac{100mV}{\frac{1.8V}{100ps}} = 5.6ps \ . \tag{4.5}$$

Comparing this to a hypothetical clock of 200-MHz with period T=5-ns, the 3-σ error introduced by one inverter is approximately 0.1%. For a clock tree with ten similar inverters in cascade, the 3-σ error per clock tree, Δ_T', equals

$$\Delta_T' = \sqrt{10(\Delta_T'')^2} = 17.6ps \ . \tag{4.6}$$

Taking into account it is the difference between ϕ_1 and ϕ_2, the actual 3-σ error is therefore

$$\Delta_T = \frac{\Delta_T'}{\sqrt{2}} = 12.4ps \ . \tag{4.7}$$

With T=5-ns, in percentage terms, the 3-σ error is 0.25%. From this first-order analysis, a systematic clock mismatch target of 0.5% is indeed realistic and should

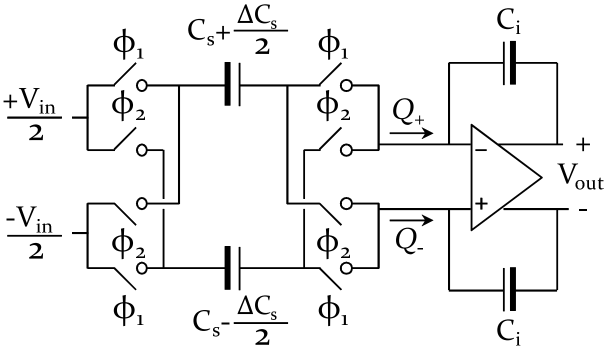

Figure 4.3: Integrator with a fully-floating input network.

be achievable in 0.18-μm CMOS process for a 200-MHz modulator.

4.3 Senderowicz's fully-floating feedback network

The previous section discussed why high-frequency quantization noise near $\frac{F_s}{2}$ feeding back to the input can be a threat to the passband signal in a double-sampled $\Delta\Sigma$ modulator. This section looks at a feedback network that can elegantly overcome the capacitor mismatch problem in the feedback path. Shown in Figure 4.3 is a double-sampled integrator that features the *fully-floating* feedback network [5]. The sampling capacitors switch between the positive and negative input terminals of the amplifier every cycle to cancel out the mismatch of the capacitors from the differential signal. However, with this switching sequence, the input experiences a *bilinear* transfer function and not the ordinary discrete-time integrator transfer function. Ignoring the mismatch capacitance ΔC_s for the moment, the expression for the output of the integrator is:

$$V_{out}(z) = z^{-1}V_{out}(z) + V_{in}(z)(1 + z^{-1})\frac{C_s}{C_i} \ . \tag{4.8}$$

The second term averages the past and the present samples of $V_{in}(z)$, and scales it by the gain ($\frac{C_s}{C_i}$) of the integrator. The transfer function from V_{in} to V_{out} follows:

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_s}{C_i}\frac{1+z^{-1}}{1-z^{-1}} \ . \tag{4.9}$$

This is the transfer function of a *bilinear integrator* [7]. Now investigate the effect of ΔC_s on the transfer function. First, assume the input terminals of the amplifier are biased at a fixed common-mode voltage. The signal charge that gets injected into the amplifier's input node is given by:

$$Q_+(z) = \left[+\frac{V_{in}(z)}{2} - \left(-\frac{V_{in}(z)z^{-1}}{2}\right)\right](C_s + \frac{1}{2}\Delta C_s) \tag{4.10}$$

and

$$Q_-(z) = \left[-\frac{V_{in}(z)}{2} - \left(+\frac{V_{in}(z)z^{-1}}{2}\right)\right](C_s - \frac{1}{2}\Delta C_s) \ . \tag{4.11}$$

Looking at the differential charge, the terms with ΔC_s cancel out, leaving

$$Q_d(z) = Q_+(z) - Q_-(z) = V_{in}(z)(1+z^{-1})C_s \ . \tag{4.12}$$

This is the desired result and is why the mismatch in (4.8) can be ignored. Looking at the common-mode, the charge injected into the amplifier's input node equals:

$$Q_{cm}(z) = \frac{1}{2}(Q_+(z) + Q_-(z)) = \frac{1}{4}V_{in}(z)(1+z^{-1})\Delta C_s \ . \tag{4.13}$$

The polarity of this common-mode charge alternates every cycle. The worst case common-mode input voltage step occurs when z=1 (V_{in} is dc), leading to

$$\Delta V_{icm} = \frac{1}{2}V_{in}\frac{\Delta C_s}{C_s + C_i}. \tag{4.14}$$

For a capacitor mismatch of 0.1%, an interstage gain of 0.5, and V_{in} of 1.8-V for 0.18-μm CMOS, ΔV_{icm} is around 300-μV, which is tolerable in most cases.

The fully-floating input network should be used whenever high-frequency signals are present at the input. The global feedback path of a $\Delta\Sigma$ modulator should take advantage of it because of the highpass characteristic of quantization noise. The input signal, on the other hand, is usually protected from high-frequency signals by the anti-aliasing filter, and therefore does not need a fully-floating input. For this reason, the input signal can use a conventional sampling network, which can also set the bias point for the amplifier's input terminal as shown in Figure 4.4. This bilinear feedback integrator with conventional (nonbilinear) input can be modeled in the z-domain as shown in Figure 4.5. The feedback path is divided by 2 so that in the passband where $z \approx 1$, the feedback gain is approximately unity.

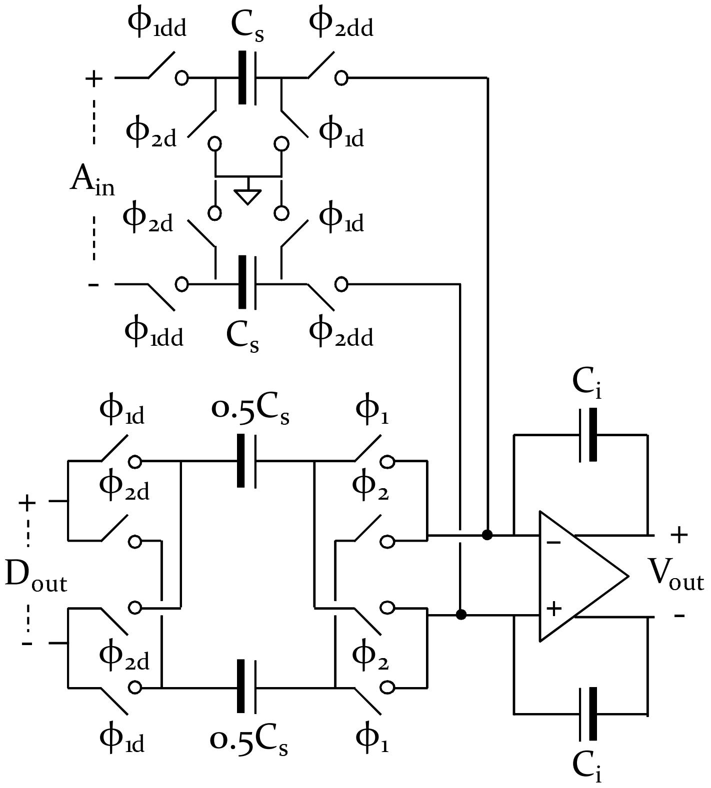

Figure 4.4: Bilinear feedback with conventional (nonbilinear) input.

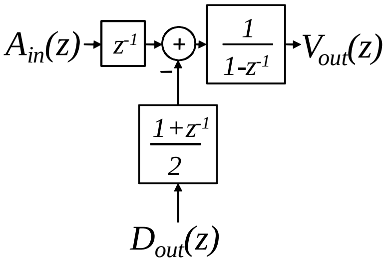

Figure 4.5: Bilinear feedback with conventional (nonbilinear) input z-domain model.

Chapter 5

A New Double-Sampled $\Delta\Sigma$ Modulator for High-Speed Low OSR A/D Conversion

In this chapter, a new double-sampled $\Delta\Sigma$ modulator is introduced. The topology of the modulator is based on the new loop-filter described in Chapter 3. The key advantages of this modulator is its ability to position a pair of complex conjugate zeros on the unit-circle of the NTF using strictly delaying integrators. This unique property allows the modulator to operate at 8× OSR while providing an SQNR of 91-dB with 4-b quantization. Compared to Balmelli's modulator that offers similar SQNR at 8× OSR [4], this topology exploits double-sampling to double the bandwidth or halve the power consumption. In the sections to follow, a linearized model of the modulator is introduced, followed by the design procedures for matching it to a target NTF. Thereafter, the differences between the double-sampled and single-sampled versions of the same modulator are analyzed. Finally, an empirical study of the double-sampled modulator's sensitivity towards capacitor mismatch beyond the 1^{st} integrator is provided.

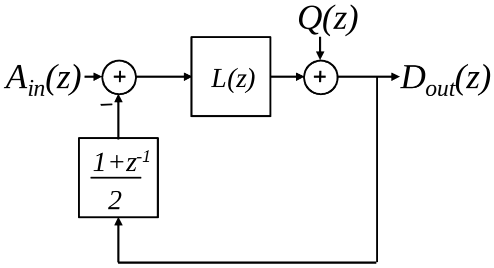

Figure 5.1: A double-sampled modulator with Senderowicz's fully-floating feedback network.

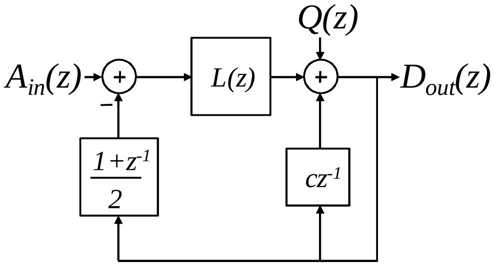

Figure 5.2: Adding a degree-of-freedom to a modulator with fully-floating feedback.

5.1 Linearized model

A high-level block-diagram of a double-sampled feedforward $\Delta\Sigma$ modulator with fully-floating feedback is shown in Figure 5.1. First pointed out by Rombouts [7], the fully-floating feedback adds an extra pole to the NTF of the modulator without introducing an extra degree-of-freedom. This is a problem because an additional pole without and additional degree-of-freedom makes it difficult, if not impossible, to assign coefficients to the loop-filter so that it matches the target NTF pole locations. For this reason, in the past, double-sampled modulators have been limited to 2^{nd}-order loops [5, 6]. Rombouts suggested three topologies that have the same number of poles as degrees-of-freedom. However, all of the topologies are for feedback modulators. Here, an extra degree-of-freedom can be added to the *feedforward* modulator by introducing a delayed feedback loop around the quantizer as shown in Figure 5.2. To realize this loop, a digital-to-analog converter with the same resolution as the quantizer is needed. The new STF and NTF can be found for this new modulator and are respectively equal to

$$
\begin{aligned}
STF &= \left.\frac{D_{out}(z)}{A_{in}(z)}\right|_{Q(z)=0} \\
&= \frac{L(z)}{1 + cz^{-1} + \frac{1+z^{-1}}{2}L(z)} \\
&= \frac{N(z)}{D(z) + cz^{-1}D(z) + \frac{(1+z^{-1})}{2}N(z)} \qquad (5.1)
\end{aligned}
$$

and

$$
\begin{aligned}
NTF &= \left.\frac{D_{out}(z)}{Q(z)}\right|_{A_{in}(z)=0} \\
&= \frac{1}{1 + cz^{-1} + \frac{1+z^{-1}}{2}L(z)} \\
&= \frac{D(z)}{D(z) + cz^{-1}D(z) + \frac{(1+z^{-1})}{2}N(z)} \qquad (5.2)
\end{aligned}
$$

where

$$L(z) = \frac{N(z)}{D(z)} \; .$$

Replacing the loop-filter, *L(z)*, with the new loop-filter described in Chapter 3, the modulator in Figure 5.3 results. This is the modulator that can position one of the NTF zero-pairs on the unit-circle using strictly delaying integrators. In the next section, this modulator is matched to a target NTF and compared to the single-sampled version from Chapter 3.

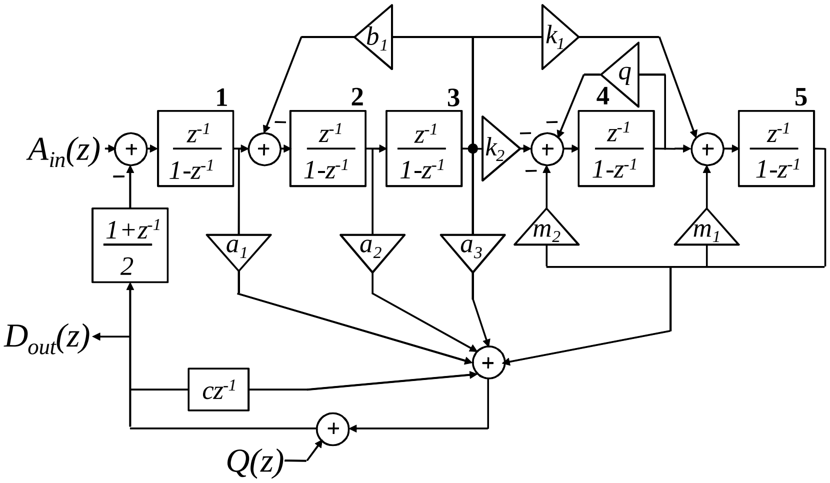

Figure 5.3: The proposed 5^{th}-order double-sampled $\Delta\Sigma$ modulator.

5.2 Design methodology

The goal in this section is to show how the proposed double-sampled modulator in Figure 5.3 can be designed to match a target NTF with five poles and five zeros. Due to the fully-floating feedback, an extra pole is introduced to the NTF, which must be positioned explicitly by the coefficients of the loop-filter and c. To start, the coefficients that determine the locations of the NTF zero-pairs, namely b_1 and m_1, are assigned, similar to the single-sampled modulator in Chapter 3. The coefficient q is set to unity to cancel out the previous cycle's charge [10] on the 4^{th} integrator. m_2 is set to unity so that the zero-pair associated with the biquad can move around the unit-circle. The coefficient b_1 positions the zero-pair along the vertical line that intersects the z-plane and can be set using the following approximation:

$$\theta \approx \sqrt{b_1} \tag{5.3}$$

Here, θ is the angle of the zero in the z-plane with respect to the real axis in radians. This zero-pair should be positioned at a lower frequency so that the penalty of not being on the unit-circle is minimized. The coefficient m_1 positions and restricts the zero-pair to the unit-circle. This zero-pair should be positioned near the edge of the passband so that the deep notch can be exploited. Either of the two following equations can be used to set the frequency of the zeros:

$$\sin\theta = \frac{\sqrt{4-(1+m_1)^2}}{2} \tag{5.4}$$

or

$$\cos\theta = \frac{1+m_1}{2} \ . \tag{5.5}$$

Now that b_1, m_1, m_2, and q are determined, the last six coefficients, namely, a_1, a_2, a_3, k_1, k_2, and c can be determined. With the help of a computer, the NTF of the modulator in Figure 5.3 is easily found. Substituting b_1, m_1, and m_2 into the NTF gives the following:

$$N(z) = (1-z^{-1})(1-2z^{-1}+1.05z^{-2})(1-1.865z^{-1}+z^{-2}) \ , \tag{5.6}$$

and

$$\begin{aligned} D(z) = & \qquad (5.7) \\ & 1+(a_1 0.5-4.865+c)z^{-1}+(a_2 0.5-a_1 1.4325+9.645-c4.865)z^{-2} \\ & +(a_3 0.5-a_2 0.9325+a_1 0.9575-9.7383+c9.6450)z^{-3} \\ & +(k_1 0.5-a_3 0.4325+a_1 0.9109+5.0083-c9.7383)z^{-4} \\ & +(-k_2 0.5+k_1 0.5-a_3 0.4325+a_2 0.9325-a_1 1.4541-1.05+c5.0083)z^{-5} \\ & +(-k_2 0.5+a_3 0.5-a_2 0.5+a_1 0.525-c1.05)z^{-6} \ . \end{aligned}$$

where

$$NTF = \frac{N(z)}{D(z)} \ .$$

Table 5.1: The proposed modulator

	Double-Sampled	Single-Sampled
b_1	0.05	0.05
m_1	0.865	0.865
m_2	1	1
a_1	4.7838	3.2287
a_2	5.5097	4.3099
a_3	2.9322	2.6659
k_1	0.5285	0.6083
k_2	0.6881	0.7215
q	1	1
c	0.8368	-

The denominator is sixth-order polynomial as expected due to the extra pole introduced by the fully-floating feedback. When written in positive powers of z^{-1}, a zero at the origin is evident. To cancel this zero and to match the NTF to a 5^{th}-order target NTF, the coefficient of the z^{-6} term in the denominator is set equal to zero. The remaining terms are then matched by like powers of z^{-1} to the target NTF:

$$NTF_{target} = \frac{(1-z^{-1})(1-2z^{-1}+1.05z^{-2})(1-1.8653z^{-1}+z^{-2})}{1-1.636z^{-1}+1.476z^{-2}-0.7584z^{-3}+0.2126z^{-4}-0.02542z^{-5}} . \tag{5.8}$$

With six equations and six unknowns, a simultaneous equation solver is used to find the coefficients. For comparison purposes, the same target NTF as the single-sampled version in Chapter 3 is used, with results listed in Table 5.1:

Pole-zero locations of the NTF are plotted in Figure 5.4 which are exactly the same as the single-sampled version. The STF, on the other hand, changes due to the fully-floating feedback. New pole-zero locations of the STF are shown in

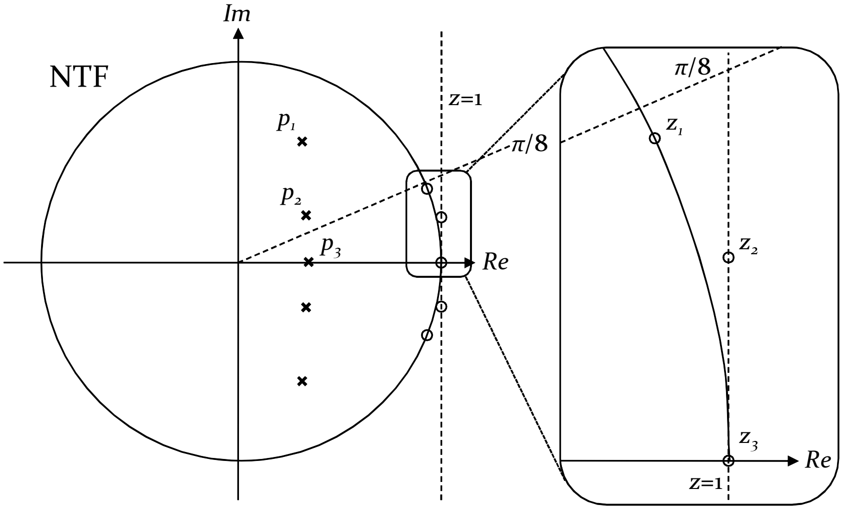

Figure 5.4: Unquantized pole-zero locations of for the proposed modulator.

Figure 5.5. Because the NTF and the STF share the same set of poles for feedforward modulators, the poles of the STF remain unchanged after double-sampling. However, the zeros have moved closer to the unit-circle in a way that exacerbates the out-of-band STF gain. The NTF and STF frequency responses are plotted in Figure 5.6 along with the STF of the single-sampled version. With the STF having higher out-of-band gain, the modulator is more sensitive to high-frequency inputs. This translates to a more demanding roll-off specification for the anti-aliasing filter to prevent quantizer overload in the presence of high-frequency signals. Zooming into the STF in Figure 5.7, the gain of the STF has risen to 8.4 (18.5-dB) from 5.1 (14.1-dB) at $\frac{F_s}{2}$, meaning an additional 3.3-dB of attenuation is required of the anti-aliasing filter. Within the passband, the ripple of the STF has increased slightly to 0.18-dB, and is shown in Figure 5.8. In a typical communication system, this amount of ripple is acceptable because the ripple contributed by preceding stages is likely on the same order-of-magnitude which can be fixed in the digital domain [26]. To measure the new modulator's pole-zero sensitivity towards coefficient variations, a test similar the sensitivity test in Chapter 3 is applied to this double-sampled

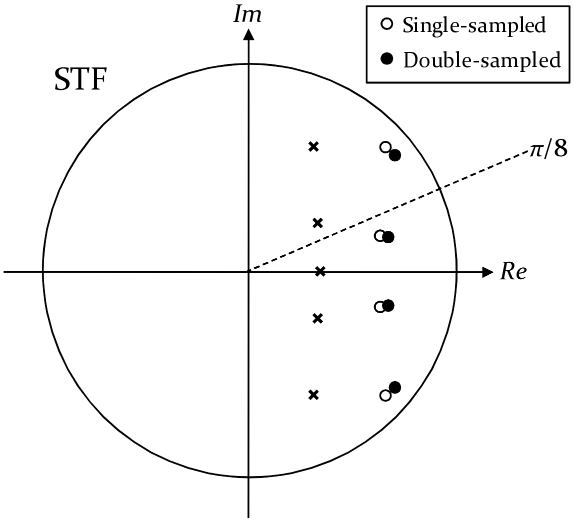

Figure 5.5: Movement of STF zeros when double-sampled.

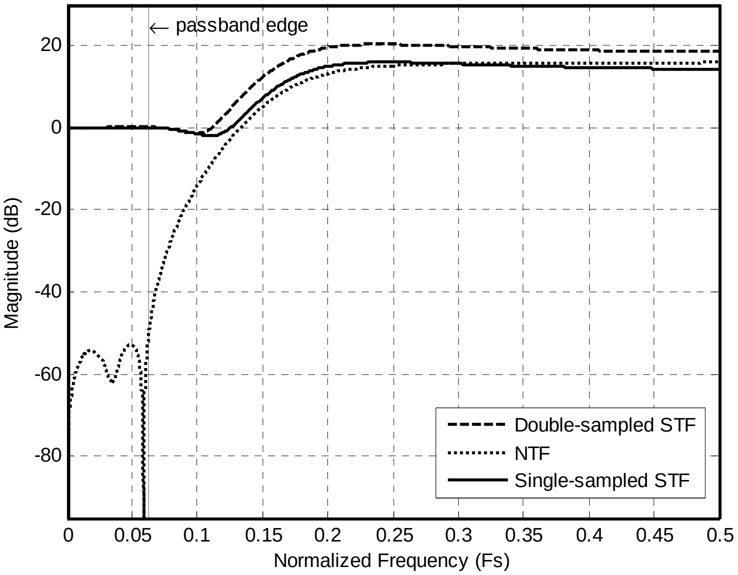

Figure 5.6: STF and NTF of double-sampled modulator.

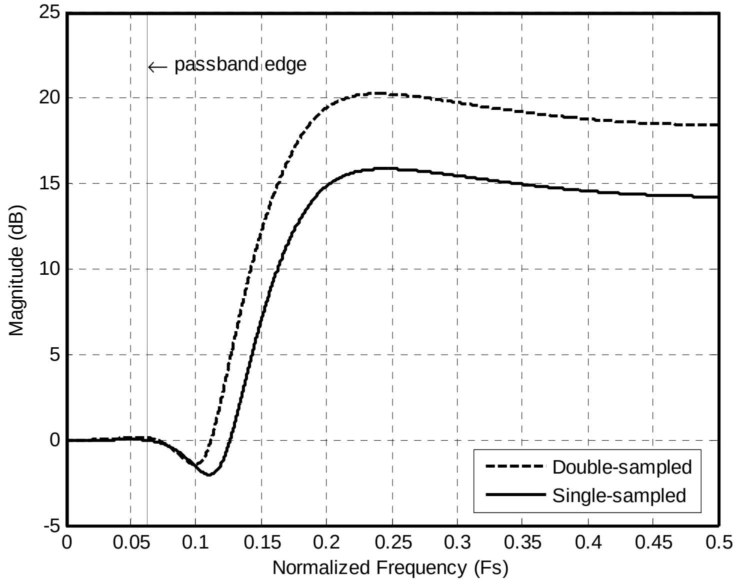

Figure 5.7: STF change after double-sampling.

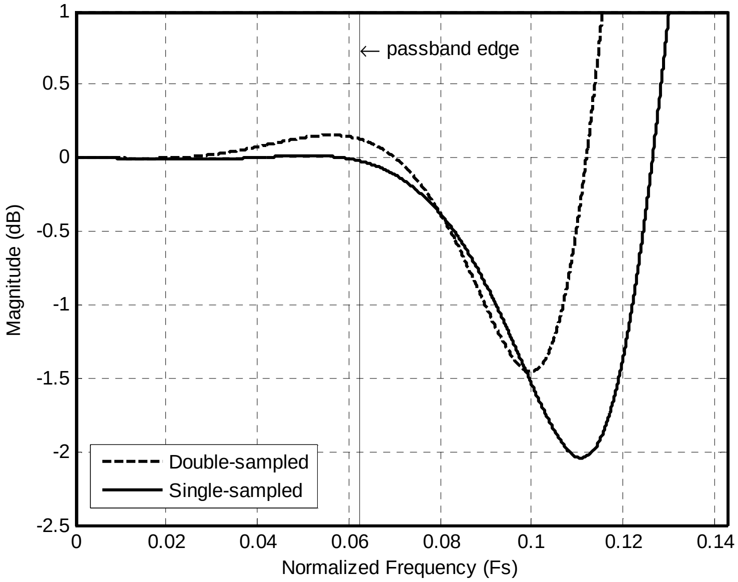

Figure 5.8: STF change after double-sampling (close-in view).

Table 5.2: The proposed double-sampled modulator coefficient sensitivity

	p_1	p_2	p_3	z_1	z_2	z_3
b_1	1.02	12.4	26.30	0	0.109	0
m_1	3.49	47.1	97.6	1.20	0	0
m_2	6.01	136	329	1.38	0	0
a_1	22.5	183	363	0	0	0
a_2	28.4	253	462	0	0	0
a_3	16.4	206	457	0	0	0
k_2	5.13	90.5	205	0	0	0
k_1	2.64	28.3	55.7	0	0	0

modulator. The results are listed in Table 5.2. Comparing the sensitivity data to the single-sampled version in Table 3.2, the poles are roughly twice as sensitive for the double-sampled version. An intuitive explanation for this property is the fact that the modulator is actually 6^{th}-order system due to the additional pole introduced by the full-floating feedback network even though it is canceled by the zero at the origin. This additional sensitivity can be a limiting factor, not necessarily because of capacitor mismatch, but primarily because nicely quantized coefficients that preserve the STF and NTF responses within an acceptable range cannot be found.

5.3 Coefficient scaling and quantization

In a conventional modulator such as CIFF or CRFF, after coefficients are obtained, it is usually necessary to redistribute the gains throughout the modulator to limit the signal swing of the integrators [18] for practical implementation. With the proposed loop-filter, however, the output swings are already within a practical range without scaling as mentioned in Chapter 3. However, to make the modulator's coefficients more predictable and to ease the layout process, coefficients are quantized into rational numbers so they can realized using simple unit-capacitor ratios. This is a time-consuming task because not all coefficients can be represented by rational numbers suitable for implementation. When a coefficient is quantized, the response of the NTF or STF can change by an amount dependent on the sensitivity of the coefficient and the absolute error between the quantized and ideal values. To arrive at the right set of numbers, designers usually go through an iterative process. After each pass, it is necessary to simulate the modulator with its quantized coefficients in discrete-time to check for maximum signal swings. If the swing of any integrator exceed practical amplifier limits, gain-scaling and re-quantization is necessary.

Using an iterative process, the double-sampled modulator is quantized and shown in Figure 5.9. A gain-of-two is intentionally shifted out of the loop-filter and into the quantizer. This is done so to lower the interstage gains of the integrators in preference for higher feedback factors, which translate to additional speed or power savings. This gain-of-two at the quantizer, as shown in the following chapter, is relatively easy to implement by scaling the reference voltage. Two of the feedforward coefficients at V_1 and V_2 are actually laid out as 3.03 and 2.97 multiples instead of 3 and 3, respectively, as shown in the figure. These changes helped bring down the out-of-band gain of the STF and NTF so that they better resemble the original STF and NTF. The author noticed that these coefficients can be safely varied over a range of 2.98-3.10 and 2.90-3.03, respectively, and still yield a stable modulator. As long as the uncertainty of the coefficient arising from the layout of non-unit-capacitors does not cause the aggregate value of the coefficient to fall outside the stable range, these optimizations are justified. In the prototype, no photolithographic invariance techniques [39] were applied. However, if more predictability is desired, the *Yiannoulos path* [39] is an excellent layout technique to implement non-integer ratioed coefficients [23].

The signal swing of all five integrators are plotted in Figure 5.10 for various

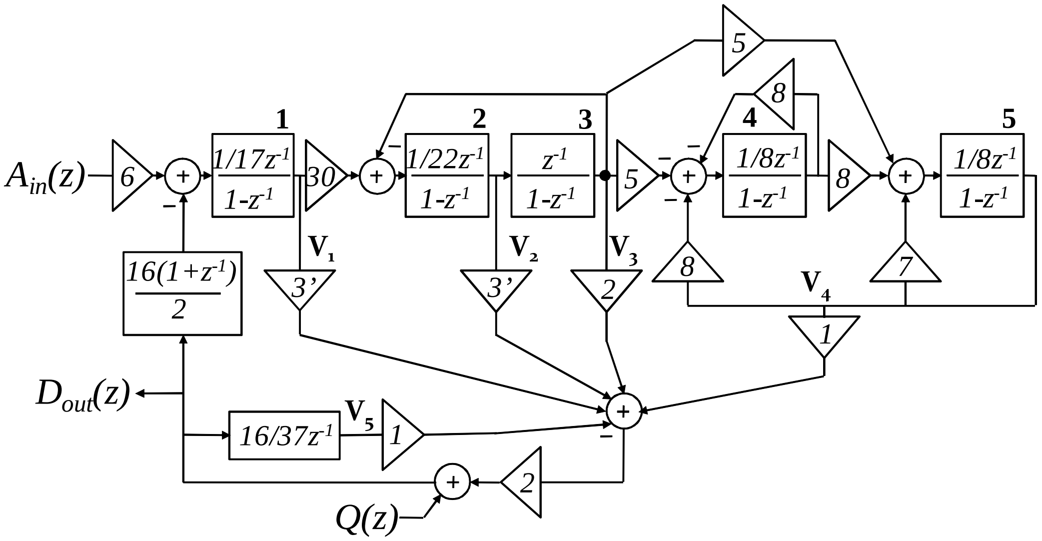

Figure 5.9: The proposed 5^{th}-order double-sampled $\Delta\Sigma$ modulator.

input signal amplitudes. At low input amplitudes, the swing is relatively constant. Beyond -10-dBFS, the swing of all integrators begin to increase. At around 0.5-dBFS, the modulator is destabilized and the swing of the integrators start to explode. This data suggests that amplifiers should have a peak-to-peak swing of roughly $0.7 \cdot V_{ref}$ for proper operation. In practice, a slightly wider margin is desired because the quantizer will introduce some offset error which can increase the signal swing of the integrators.

The new pole-zero locations of the NTF are plotted in Figure 5.11. Due to quantization, the poles have moved significantly from their intended positions. The pole that is originally designed to cancel the zero at the origin has combined with another pole on the real axis into a complex conjugate pair. The zero at the origin has no effect on the modulator. However, without the pole-zero cancelation, the modulator has become a 6^{th}-order system with six poles. The new zero locations are at approximately the same locations as the target thanks to lower coefficient sensitivity for the zeros and small quantization error.

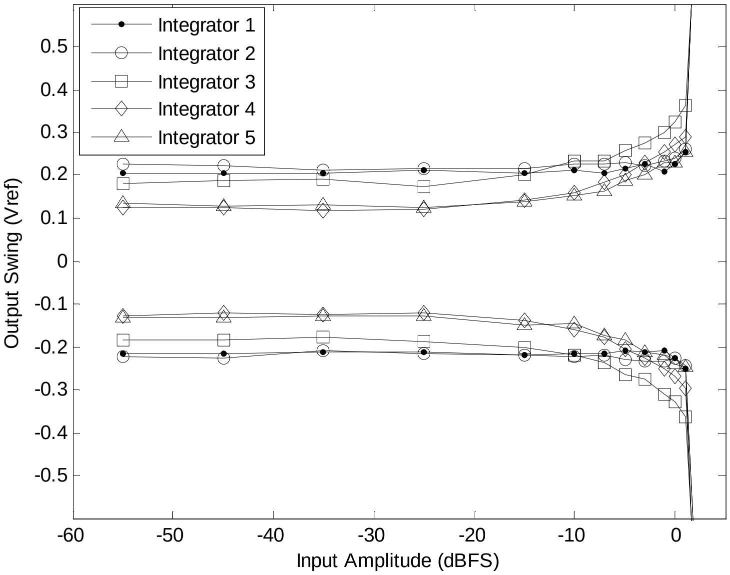

Figure 5.10: Internal signal swing for various stages after quantization.

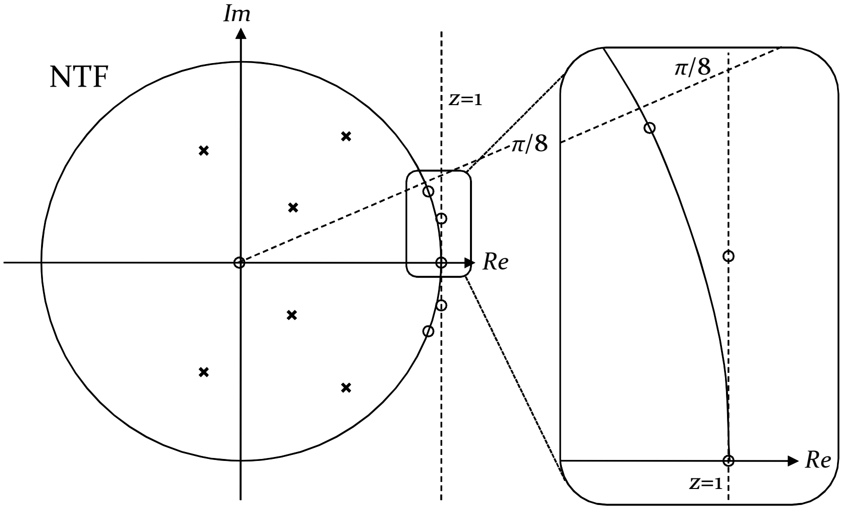

Figure 5.11: NTF pole-zero locations after quantization.

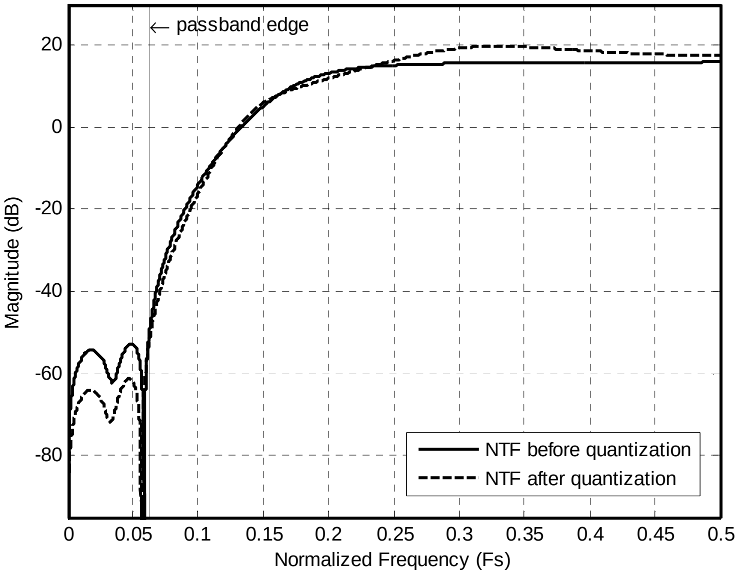

Figure 5.12: NTF before and after quantization.

The frequency response of the NTF before and after quantization are plotted together in Figure 5.12 for comparison. At $\frac{F_s}{2}$, the NTF gain has increased by 1.6-dB to 17.2-dB, or 7.2 in absolute value. This increase in out-of-band gain has shaped more of the passband gain towards higher frequencies and is evident in the NTF's passband frequency response. Taking a closer look at the passband in Figure 5.13, it is noticeable that the notches have shifted towards lower frequencies due to quantization error. Nonetheless, these shifts are relatively small and do not affect the modulator's overall performance. Continuing on with the STF, the new pole-zero locations are plotted in Figure 5.14. The poles have shifted from its intended locations because the STF shares the same poles as the NTF. The zeros have shifted closer to the unit-circle in a way that increases the out-of-band gain of the STF. Plotted in Figure 5.15 are the STF responses before and after quantization. The gain of the new STF at $\frac{F_s}{2}$ has increased by 2.5-dB to 21-dB, or 11.2 in absolute

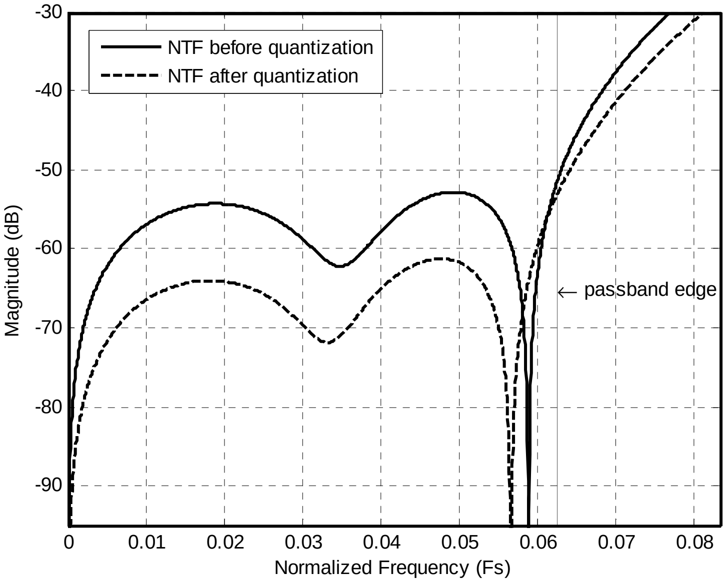

Figure 5.13: NTF before and after quantization (close-in view).

value. The peak gain, which occurs at $0.32 \cdot F_s$ is 5-dB above its original, at 25-dB. Depending on the application of this modulator, this amount of out-of-band STF sensitivity may or may not be critical, which depends on the magnitude of the out-of-band signals and the attenuation of the anti-aliasing filter. Simulation suggests that a 3^{nd}-order Butterworth anti-aliasing filter attenuates full-scale inputs at all frequencies above the passband down to the -10-dBFS level. In applications where desensitizing out-of-band gain is paramount, the coefficients can be quantized differently to yield a lower out-of-band STF gain. Close-in views of the passband responses of the STF before and after quantization are plotted in Figure 5.16. The passband ripple of both STFs are approximately 0.2-dB, which is an acceptable value in most communication applications.

If a modulator is scaled and quantized properly, the effects of thermal noise and circuit non-idealities can be relaxed progressively beyond the 1^{st} integrator.

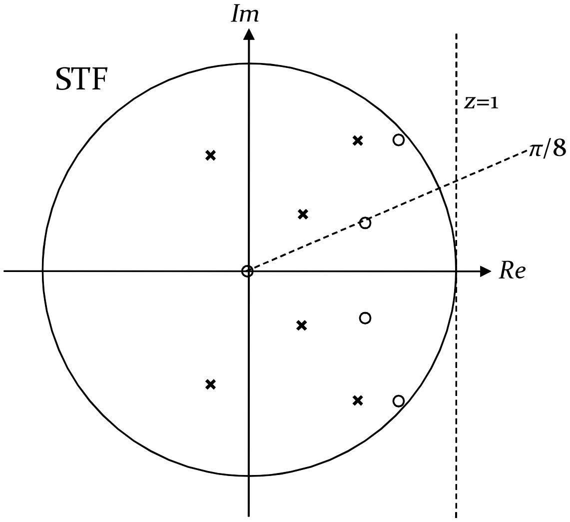

Figure 5.14: STF pole-zero locations after quantization.

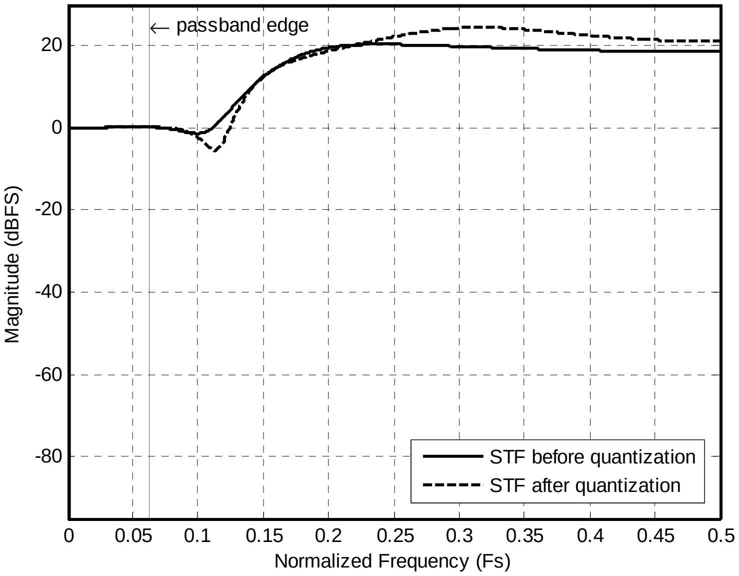

Figure 5.15: STF before and after quantization.

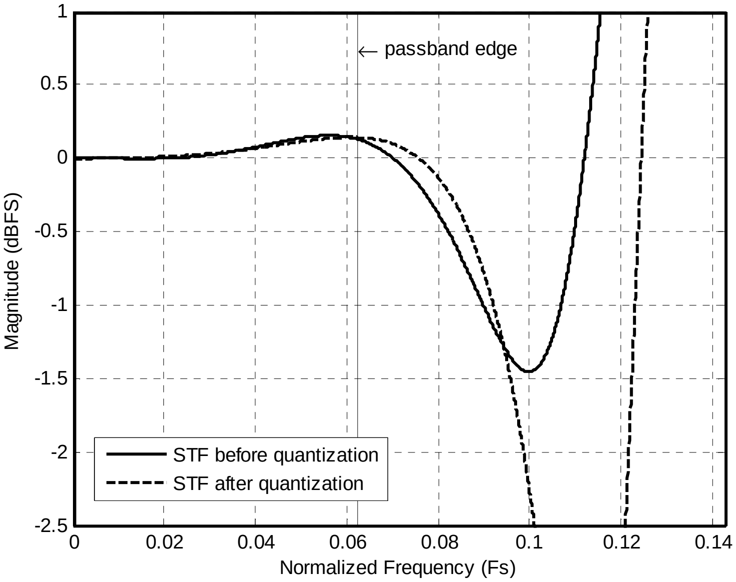

Figure 5.16: STF before and after quantization (close-in view).

If the loop-filter coefficients are assigned such that the transfer function from the output of each integrator to the output of the modulator, after referring back to the input, is below 0-dB across the passband, thermal noise and circuit requirements can be relaxed. A plot of the input-referred transfer functions is shown in Figure 5.17. NTF_1 is the input, which has no suppression across the Nyquist band. NTF_2 is the input-referred transfer function from the output of the 1^{st} integrator to the output of the modulator. NTF_3 is the input-referred transfer function from the output of the 2^{nd} integrator to the output of the modulator, and so forth. The plot shows that the stages are indeed progressively more relaxed downstream, and the input stage is expected to dominate the thermal noise budget.

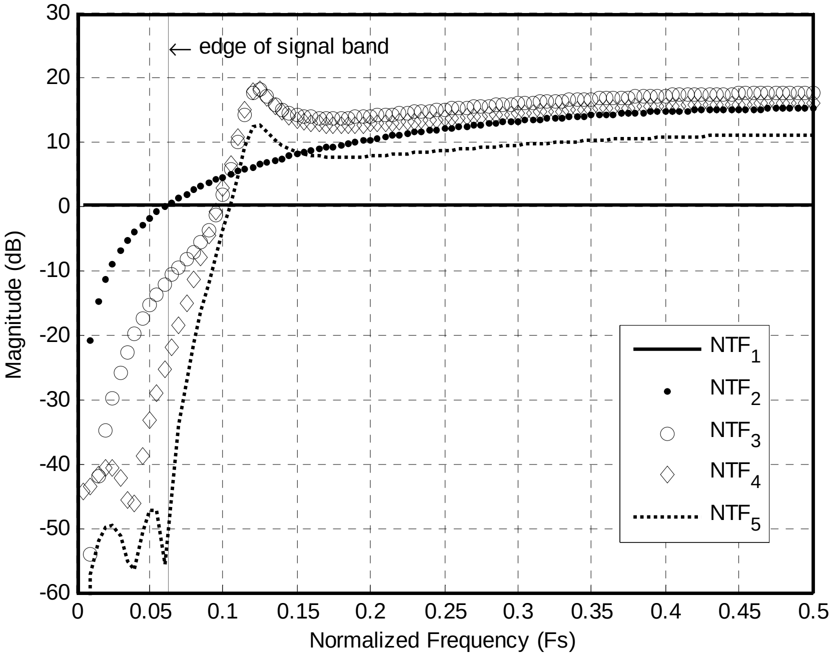

Figure 5.17: Noise transfer functions from internal nodes to the input node.

5.4 Circuit specifications

The goal in this section is to prepare the quantized modulator in the previous section for prototype implementation in a standard CMOS process. Different circuit non-idealities relating to amplifiers, dynamic element matching (DEM), path mismatch errors, isolation, quantizer offset, and jitter are analyzed. All results are normalized to a sampling-frequency F_s and can be applied to different applications fabricated in different processes. In the summary section, a set of specifications for a target 78-dB SQNR thermal-noise limited modulator is provided.

5.4.1 Amplifier

Arguably the most crucial analog component in a $\Delta\Sigma$ modulator is the amplifier. Depending on the requirements, different amplifier topologies be chosen to meet the specifications. The properties that matter most, besides 1/f and thermal noise, are its dc gain, output swing, settling time-constant (τ), and slew-rate. Finite dc gain introduces a static error, while slew-rate limited settling introduce dynamic errors. It is difficult to analyze all error sources simultaneously, so a superposition approach is taken here. Each of the error sources is studied individually, and its impact on the performance of the modulator is reported while assuming other factors are ideal.

The impact of finite amplifier dc gain on the modulator's performance can be predicted through discrete-time simulation. Since the 1^{st} integrator is the most critical, predicting its dc gain requirements can expose how feasible a particular modulator topology is in a target process for a given dynamic range objective. With a full-scale sinusoidal input at 1/3 times the highest passband input frequency, $F_{in(max)}$, the modulator is simulated in discrete-time and the SQNDR of the modulator is collected for different 1^{st} integrator amplifier dc gains. Results are plotted in Figure 5.18, and shows that to achieve an SQNDR of 90-dB, a dc gain of no less than 60-dB is required. In practice, the nominal dc gain specification is usually higher

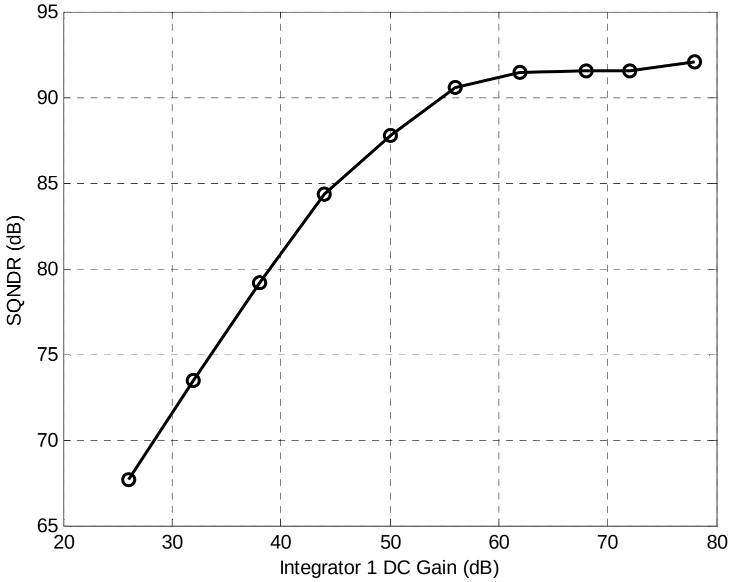

Figure 5.18: 1^{st} integrator amplifier dc gain requirement.

than the minimum required because the dc gain of the amplifier rolls off towards the edges of the output swing. Depending on the signal swing of the integrator, one amplifier topology may be chosen over another. Gain-boosting [33] is used in the prototype of this work to achieve 70-dB of dc gain for a folded-cascode amplifier. A list of the dc gain requirements for all five amplifiers are provided in Table 5.3. Because the 4^{th} and 5^{th} integrators process the signal as well as quantization noise, its dc gain requirements are more critical. For integrators that only process quantization noise, significantly lower dc gain requirements are possible [31].

Next, consider the speed and slew-rate requirements of the amplifier given a target sampling-frequency F_s, with a sampling period of T_s. It is important to note that the speed of the integrator is not the same as the speed of the amplifier because the speed of the integrator depends on the unity gain-bandwidth (GBW) of the amplifier and the feedback factor, β. In particular, the expression that relates

Table 5.3: Amplifier dc gain requirements.

Integrator	**Minimum dc gain**
1^{st} integrator	60-dB
2^{nd} integrator	30-dB
3^{rd} integrator	30-dB
4^{th} integrator	60-dB
5^{th} integrator	60-dB

the settling time-constant of the integrator, τ, to the speed of the amplifier is given by

$$\omega_{-3dB} = \frac{1}{\tau} = \beta \cdot \omega_u \ . \tag{5.9}$$

where ω_{-3dB} is the -3-dB frequency of the integrator response in radians/s and ω_u is the unity GBW of the amplifier in radians/s. Discrete-time simulation can determine the number of settling time-constants needed to achieve a given SQNDR. The normalized slew-rate requirement with respect to V_{ref} can also be determined simultaneously following the techniques described in [25]. Simulation results for the 1^{st} integrator are plotted in Figure 5.19 for different $\frac{T_s}{\tau}$ ratios, where T_s is the sampling period. The significance of the horizontal axis, SR$\cdot\tau$, can be thought of as the amount the output can travel in one time-constant. For high slew-rates, the SQNDR is the practically the same for all three $\frac{T_s}{\tau}$ ratios because the output always settles linearly. As slew-rate decreases, settling becomes partially slew-rate limited, which is fine as long the amplifier is able to reach its final value within a certain tolerance that does not degrade performance. However, as the slew-rate is further reduced causing significant non-linear settling errors, performance starts to degrade. As shown in the figure, with seven time-constants the SQNDR is almost independent of slew-rate down to at least 0.1 SR$\cdot\tau$.

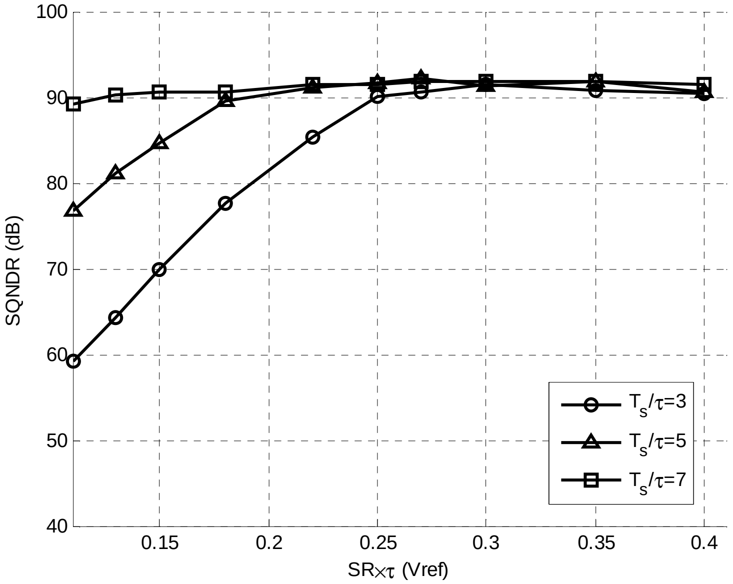

Figure 5.19: 1^{st} integrator amplifier slew-rate and settling requirements.

5.4.2 DWA feedback capacitor matching

Another important specification of high-resolution $\Delta\Sigma$ modulators with multi-bit quantizaion is the effectiveness of the linearization algorithm to cancel out the mismatch between the global feedback capacitors. Since the feedback path sums directly with the input, the mismatch limits the achievable resolution of the converter. Fortunately, with DEM, this mismatch can be partially or fully canceled out depending on the order of the modulator, the OSR, and the DEM algorithm. The simplest and among the most effective DEM algorithms is Data Weighted-Averaging (DWA) [22]. In DWA, capacitors are rotated sequentially and each capacitor receives the same amount of utilization. This algorithm is particularly effective when the assumption of a white quantization noise spectrum is valid, otherwise passband signal-dependent tones can develop. In a high-order single-loop modulators such as the one proposed in this work, the spectrum is indeed white and DWA is effective. In high-speed designs, the DEM algorithm should be simple so that the speed of the modulator is not limited by it. Additionally, DEM logic also consumes power, which can be an appreciable amount at high-speeds. For these reasons, the DWA algorithm is chosen for this modulator.

To determine the unit-capacitor matching requirements, discrete-time simulation is conducted with various amounts of mismatch (3σ) added to the capacitor array. Figure 5.20 compares the cases when DWA is applied versus when no DEM is applied. A special case of DWA, labeled as 'DWA-partial', is also plotted for comparison. The author notices that a modification to the DWA algorithm can be made to simplify the digital logic complexity without degrading performance. The idea is that the 2^n-2 output code appears so seldom that when it does appear, even without rotating the capacitor array, the SQNDR remains approximately the same. This result is valid for the modulator described here at 8× OSR with 4-b quantization. However, at different OSRs and quantizer resolutions, this optimization may or may not apply.

5.4.3 2^{nd} integrator capacitor matching

In a double-sampled modulator, all sampling capacitors are interleaved. As discussed in Chapter 4, the mismatch of the input pair does not affect passband performance as long as high-frequency energies of the input signal near $\frac{F_s}{2}$ are suppressed down to safe levels. However, the input of the 2^{nd} integrator contains a filtered version of the feedback quantization noise which has an appreciable amount of energy near $\frac{F_s}{2}$. Through the same mixing mechanism as outlined in Chapter 4, the 2^{nd} integrator's mismatch can cause a folded version of the filtered quantization noise to appear in the passband [7]. Therefore, it is important to properly model this phenomenon to determine the path mismatch requirement of the 2^{nd} integrator. A useful expression [7] that predicts the folded quantization noise spectrum can be used in conjunction

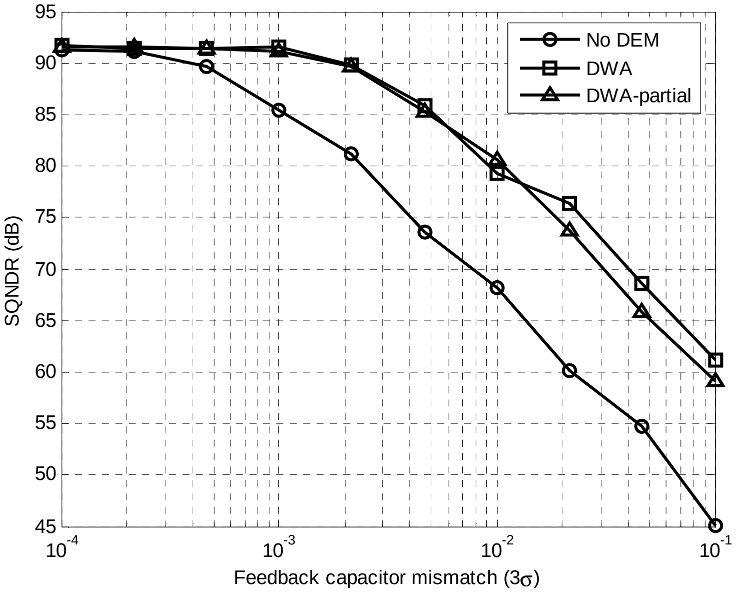

Figure 5.20: DWA capacitor matching requirement (3σ).

with discrete-time simulation:

$$N_{fold}(z) \approx \delta NTF(-z)Q(-z)\frac{(1-z^{-1})^2}{2z^{-1}(1+z^{-1})} \ . \tag{5.10}$$

Here, δ is the 3σ error of the mismatch, and *Q(-z)* represents the unfiltered folded quantization noise spectrum. It is important to note that (5.10) is specific to modulator types with a delaying integrator input. A different modulator topology may require a different expression. Plotted in Figure 5.21 is the magnitude spectrum of a modulator with 0.3% of path mismatch at the input of the 2^{nd} integrator. The solid line indicates the calculated spectrum of the folded noise into the passband using (5.10). Since the error spectrum is below the noise floor, its effects are not visible except for the notch being shallower. If δ is increased to 1% as shown in Figure 5.22, the error dominates the noise floor. This analysis confirms the validity of (5.10) for 8× OSR operation. Beyond the 2^{nd} integrator, successive integrators

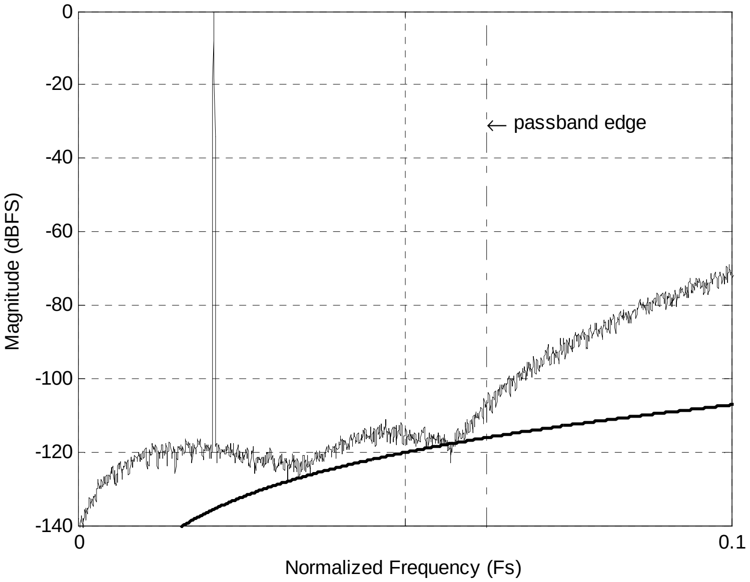

Figure 5.21: 2^{nd} integrator ±0.3% input capacitor mismatch.

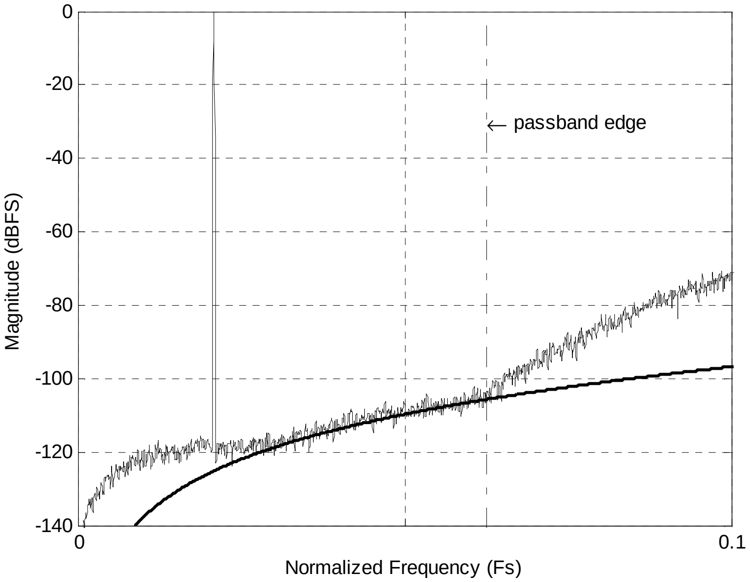

Figure 5.22: 2^{nd} integrator ±1% input capacitor mismatch.

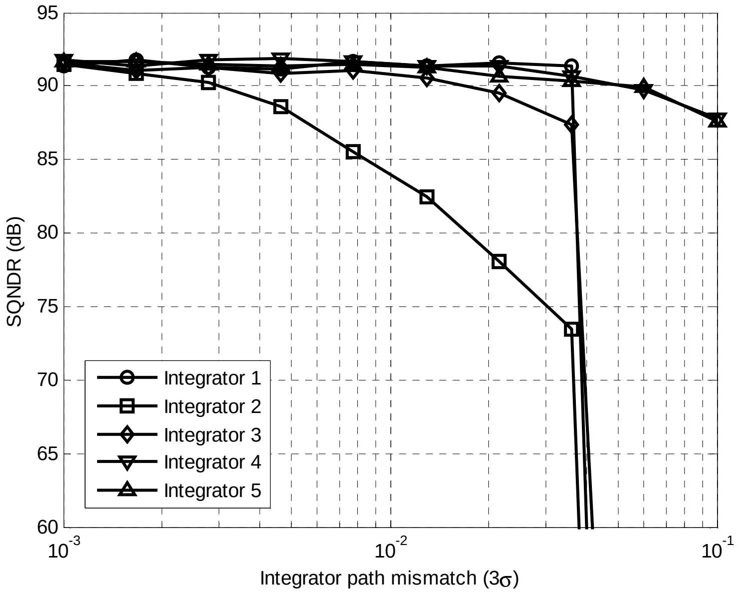

Figure 5.23: 2^{nd} integrator input capacitor mismatching requirement.

become less sensitive to path mismatch because of the filtering effect of preceding stages. Simulation data is collected for mismatch in all five integrators and plotted in Figure 5.23. Without surprise, the mismatches beyond the 2^{nd} integrator almost have no effect on performance.

5.4.4 Isolation

In almost all data converters, it is important to decouple the input signal from the reference voltage otherwise unwanted distortion can appear at the output. For $\Delta\Sigma$ modulators, it is also important to decouple any $\frac{F_s}{2}$ signals from the reference voltage because it can mix with quantization noise in the feedback path and fold down to the passband [24]. Therefore, it is sensible to model both types of coupling to predict the amount of isolation needed for a certain dynamic range objective. Here, discrete-time simulations with different amounts of coupling are added to the

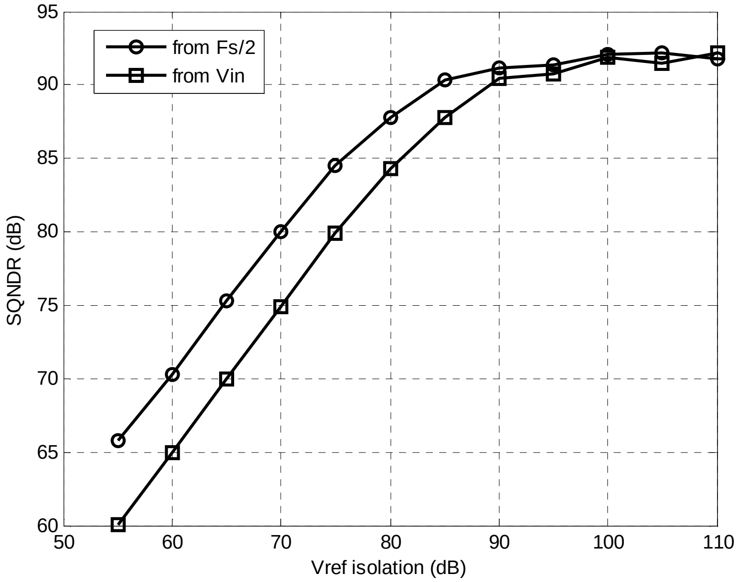

Figure 5.24: V_{ref} isolation from $\frac{F_s}{2}$ and V_{in}.

reference voltage. Results are plotted in Figure 5.24 in terms of isolation in dB. The data reveals that around 90-dB of isolation is needed if the performance of the modulator is to be completely independent of V_{in} or $\frac{F_s}{2}$ tones. This intuitively makes sense because the modulator's maximum performance is around 92-dB. In practice, 90-dB of isolation is non-trivial but achievable with proper design [24]. Above 90-dB, additional countermeasures are needed [24, 29].

5.4.5 Clock jitter

Clock jitter is an important specification for high-performance data converters. Jitter can arise from device thermal noise affecting the zero-crossing point of a clock buffer, or power supply noise affecting the propagation delay of the clock buffer. In a jitter limited ADC, the noise floor rises with respect to the input amplitude and input frequency. When jitter is determined as the bottleneck, the problems are usually difficult to fix without a full set of wafer mask revision [24]. Fortunately, jitter tolerance can be predicted with discrete-time simulation to determine whether a target dynamic objective is feasible. The jitter law [24] states that for a jitter profile that is uniformly distributed from -$\frac{\delta_t}{2}$ to $+\frac{\delta_t}{2}$, the maximum achievable dynamic range for a full-scale sinusoidal input is given by

$$DR(dB) = 20 \cdot \log(F_{in}\delta_t) - 5.172dB \ . \tag{5.11}$$

For power supply noise induced jitter, a uniform distribution is a good approximate to the first-order [24]. For thermal noise induced jitter, on the other hand, a Gaussian distributed jitter profile is more appropriate. Since the prototype developed in this work is on a die without much digital circuitry, the power supply noise is likely periodic with the clock and will not manifest itself as jitter. Therefore, the author believes, in this case, the dominant cause for jitter will be thermal noise. Applying different amounts of Gaussian distributed jitter to a normalized clock with period T_s, the modulator is simulated in discrete-time and the results are plotted in Figure 5.25. Data indicates that a 0.1% 3σ clock jitter with respect to T_s can be tolerated with almost no degradation to performance. To ensure a robust design, jitter should be controlled to ensure its noise contribution is 10-dB below the total noise of the converter [24].

5.4.6 Quantizer offset

A 4-b quantizer is used in this modulator. Since quantization happens during the non-overlapping clock period, the speed of the quantizer directly affects the amount of time available for amplifiers to settling. Therefore, it is important that the quantizers are fast and the results are simple to process. In a conventional Flash ADC, bubble correction [27] is used to reduce offset errors. However, bubble correction adds gate delays to the feedback path and is not desirable. It is possible, however,

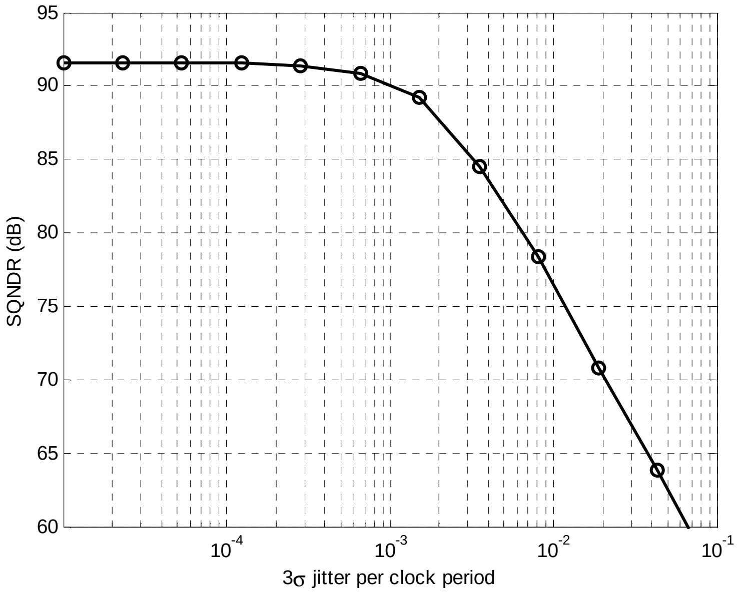

Figure 5.25: Gaussian distributed clock jitter (3σ) with respect to clock period vs. SQNDR.

to eliminate the bubble correction logic if absolute offset of every quantization level is less than 0.5 LSB. This constraint essentially requires 5-b of resolution from the comparators instead of 4-b. From a full-scale signal swing standpoint, 5-b of resolution is not difficult to achieve. However, if the signal attenuation of the feedforward passive summing network is factored in, 5-b of may not be trivial. For instance, if the attenuation factor is 8, that adds an additional 3-b to the target, putting the comparator offset requirement with respect to full-scale at 8-b, which is non-trivial, especially at high-speed.

In addition to the above constraints, it is important to determine whether 0.5 LSB of random offset does indeed yield a stable modulator. Errors in the quantizer add to the total accumulated quantization noise in the loop. When the combination of the signal and accumulated noise overflows the quantizer's input range, instability can occur [21]. Therefore, Monte Carlo simulations are conducted for different LSB

Table 5.4: Yield percentage for various 3σ quantizer offsets

	0-dBFS	-1-dBFS
0.35 LSB	97.4	99.3
0.40 LSB	92.3	98.7
0.45 LSB	88.3	95.4
0.50 LSB	80.0	91.9

offset errors. The results are plotted in Figure 5.26. A total of 1000 samples are taken to generate each plot. Depending on the desired yield and the minimum SQNDR cut-off point, different LSB offsets can be specified. With the minimum SQNDR yield cut-off set at 80-dB, the yield is 97.4% for a 3σ 0.35 LSB offset. Depending on the overall expected yield of the converter, 97.4% may or may not be adequate.

Because the instability originates from the saturation of the quantizer, reducing the input amplitude to make room for extra noise should improve yield. Therefore, the input is reduced by 1-dB (to -1-dBFS) and the Monte Carlo simulation is repeated. Results are plotted in Figure 5.27, which show that the yield improves. This result indicates that if the yield is inadequate, one of two actions can be taken. First, the quantizer offset specification can be tightened. This makes the design effort more difficult and may cost additional power and area. Second, the input can be attenuated on-chip to make room for the excess quantization noise. This is not desirable because to maintain the same SNR, the loss of 1-dB of signal means the noise must be reduced by 1-dB, which invariably requires more power and area.

5.4.7 Summary

This section considered various circuit non-idealities that can limit the performance of the double-sampled modulator. For prototype implementation, a set of realistic

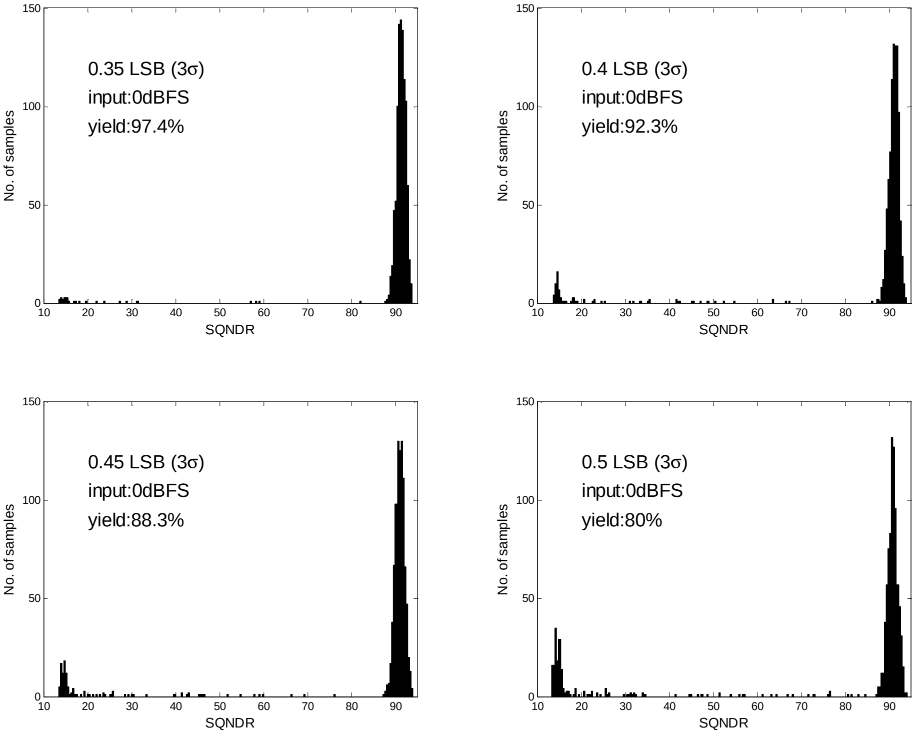

Figure 5.26: Effect of quantizer offset on overall yield at 0-dBFS input

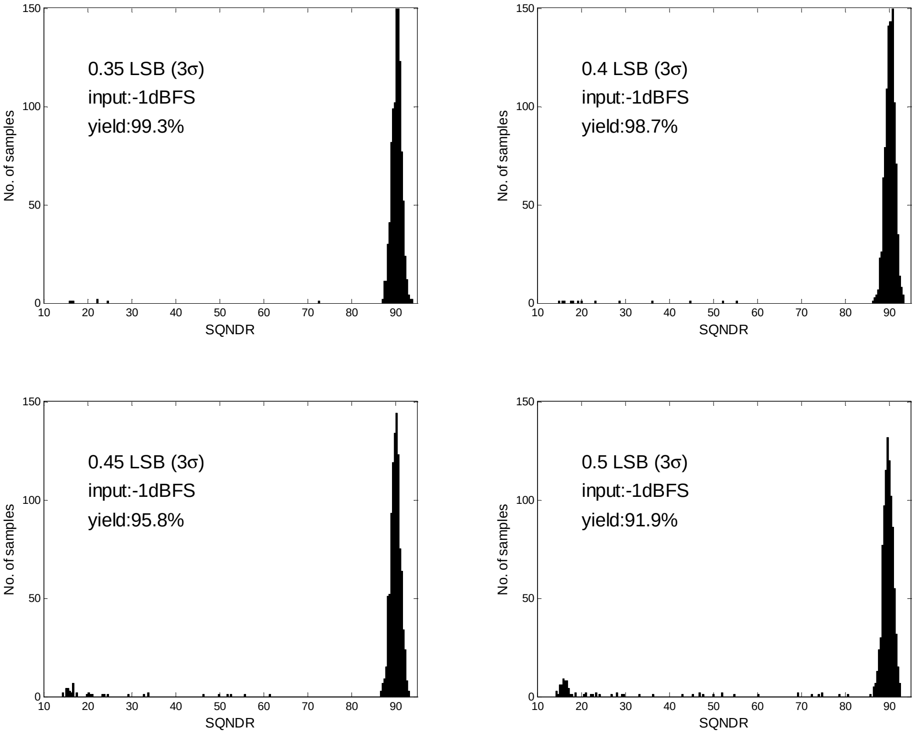

Figure 5.27: Effect of quantizer offset on overall yield at -1-dBFS input

Table 5.5: Circuit specifications chosen for 78-dB SNDR prototype

	Nominal	**Worst Case**
1^{st} integrator amplifier dc gain	70-dB	60-dB
1^{st} integrator $\frac{T_s}{\tau}$	10	7
1^{st} integrator slew-rate (SR$\cdot\tau$)	0.5	0.4
2^{nd} integrator C_s mismatch (3σ)	0.2%	0.2%
DWA C_{fb} mismatch (3σ)	0.2%	0.2%
Quantizer offset (DNL 3σ)	0.35	0.35
V_{ref} to V_{in} isolation	80-dB	75-dB
V_{ref} to $\frac{F_s}{2}$ isolation	75-dB	70-dB
Amplifier swing ($\pm V_{ref}$)	0.4	0.35
Clock jitter rel. to T_s (3σ)	0.1%	0.2%

specifications are needed. An SNDR target of 78-dB is chosen for this work. A summary of the specifications for each non-ideality discussed is listed in Table 5.5. Due to variations in process, temperature, and power supply, a value is listed for both nominal case and the worst case. For specifications that are statistically bounded by a 3σ value, the nominal and worst cases are the same because variations in process, temperate and power supply, to the first order do not affect them. Since all of the error sources are simulated independently of each other, it is sensible to simulate the modulator with all or most of the error sources combined for verification.

Chapter 6

Prototype Implementation

In this chapter, the design of some key circuit blocks of the prototype $\Delta\Sigma$ modulator is discussed. Specifications of the individual blocks are based upon the results obtained in the previous chapter. A commercially available 0.18μm CMOS process with metal-insulator-metal (MiM) capacitors is available for prototyping via a multi-project wafer (MPW) shuttle. The prototype is fabricated on a high-resistivity substrate, and the total chip area is constrained to a square block of size 2.25-mm^2 (1.5-mm by 1.5-mm), including all bond pads. A target sampling-frequency of 200-MHz is chosen based on demonstrated results of previous work [4] fabricated in roughly the same die area and a similar process. At 8× OSR, the decimated sampling-rate is 25-MS/s. Circuits are simulated using the Cadence Spectre simulator. Process corners and matching data for threshold voltages and capacitors are available to the author and are used extensively to increase the likelihood of success. The layout of the circuit is completed using a combination of Cadence Layout XL and Mentor Graphics Calibre tools.

6.1 1^{st} integrator

6.1.1 Noise analysis

In a $\Delta\Sigma$ modulator, the 1^{st} integrator is usually the most critical and dominates the noise budget. Subsequent stages contribute progressively less input-referred noise. The various types of noise sources include switch resistance thermal noise, amplifier thermal and 1/f noise, jitter and quantization noise. Assuming the modulator is dominated by thermal noise, the total input-referred noise budget can be calculated for a target dynamic range given the input swing and OSR. The OSR plays a role because thermal noise has a flat spectrum, and only the noise that falls within the passband makes it to the output after decimation:

$$\overline{v_{n,inband}^2} = \frac{\overline{v_{n,rms}^2}}{OSR} \tag{6.1}$$

Here, $\overline{v_{n,rms}^2}$ is the total input-referred thermal noise energy and $\overline{v_{n,inband}^2}$ is the inband thermal noise energy that remains after decimation.

Operating from a 1.8-V supply, the reference voltages are set at 200-mV and 1.6-V. This translates to a 2.8-V peak-to-peak differential swing for the global feedback DAC. Since the DAC processes both signal and quantization noise, the DAC's swing is *not* equal to the signal swing. For loop-filter coefficients chosen, the signal swing is about half of the DAC's range. Therefore, to find the equivalent input signal swing, the DAC's swing is divided by two and referred back to the input:

$$v_{in} = \frac{v_{dac}}{2}\frac{C_{fb}}{C_s} \tag{6.2}$$

Here, v_{dac} is 1.4-V (2.8-V peak-to-peak), C_{fb} is the feedback capacitor, and C_s the sampling capacitor. The ratio C_{fb} to C_s, according to Figure 5.9, is equal to $\frac{8}{6}$. This results in an input swing, v_{in}, of 0.93-V, or 1.86-V peak-to-peak. With v_{in}, the required inband input-referred noise can be calculated using the following:

$$DR(dB) = 10 \log \left(\frac{\overline{v_{in}^2}}{2\overline{v_{n,inband}^2}} \right) \ . \tag{6.3}$$

Substituting 78-dB for dynamic range (DR) and 0.93-V for v_{in}, the root mean-squared input-referred noise, $v_{n,inband}$, is 83-μV$_{rms}$. Next, the values of C_s and C_{fb} are found that will satisfy the modulator's $v_{n,inband}$ requirement.

When a switch opens to sample the input on the sampling capacitor, the noise sampled on the capacitor is independent of the series resistance of the switch and dependent only on the capacitance and absolute temperature [24]:

$$\overline{v_n^2} = \frac{kT}{C_s} \ . \tag{6.4}$$

Here, C_s is the sampling capacitance and k is the Boltzmann's constant. After sampling, the signal and noise charge are transferred to the integrating capacitor, C_i. At the end of the transfer, a switch opens to disconnect C_s. This action causes another independent noise sample to be sampled onto C_s, which is simultaneously transferred to C_i [24]. Each sample of the input, therefore, causes $2kT/C_s$ of noise energy to be injected into the integrating capacitor. Since the integrator is differential, two capacitors sample the input, leading to four independent noise samples, and therefore $4kT/C_s$. The fully-floating feedback capacitor can be analyzed similarly and contributes an additional $4kT/C_{fb}$ [6]. In total, the sampled noise energy, when referred to the input equals

$$\overline{v_{n1,samp}^2} = 4\frac{kT}{C_s} + 4\frac{kT}{C_{fb}} \left(\frac{C_{fb}}{C_s} \right)^2 = 4\frac{kT}{C_s} \left(1 + \frac{C_{fb}}{C_s} \right) \ . \tag{6.5}$$

The above analysis ignored the noise contribution of the amplifier on C_s during the charge-transfer phase. In practice, amplifier noise cannot be ignored. If not

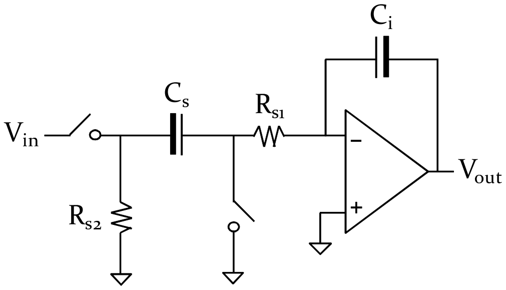

Figure 6.1: Single-ended switched-capacitor integrator during charge-transfer.

modeled properly, significant loss in dynamic range can ensue. During the original design process, the amplifier's noise contribution was not taken into account properly. This cost the prototype to miss its original dynamic range objective (discussed in Chapter 9). Therefore, it is important to study how the amplifier's noise affects the overall sampled noise on C_s.

Consider the singled-sampled, single-ended switched-capacitor integrator in Figure 6.1. Resistors R_{s1} and R_{s2} represent the resistance of two closed switches during the charge-transfer phase. When switch s_2 opens to end the transfer, noise from both the amplifier and the switches are sampled onto C_s. The noise contribution of the switches is independent of the switch resistance and the noise power is equal to kT/C_s. The noise contribution of the amplifier, on the other hand, depends the input-referred noise power of the amplifier, the -3dB frequency of the integrator, and the intrinsic 1^{st}-order filter formed by the RC combination of R_{s1} and R_{s2} and C_s. If -3-dB frequency of the integrator is lower than the filter's corner frequency, then the noise from the amplifier will not see any meaningful attenuation. In this case, the noise power of the amplifier adds directly to noise power of the switch. On the other hand, if the filter's corner frequency is lower than the integrator's -3-dB frequency, then the amplifier's noise is attenuated. In practice, the total noise power sampled onto C_s when s_2 opens is relative easy to measure in a noise analysis circuit simulation.

Purely from a noise perspective, it is sensible to reduce the size of both s_1 and s_2 to filter out as much of the amplifier's noise as possible. However, this is only beneficial up to a certain point when the error caused by incomplete settling becomes significant. Although the above discussion centers around C_s, the same principles and tradeoffs apply to the feedback capacitor (C_{fb}).

To find the values of C_s and C_{fb}, 80% of the total thermal noise budget is allocated to the sampling network of the 1^{st} integrator. The remaining budget is allocated to the noise beyond the 1^{st} integrator:

$$\overline{v_{n1,samp}^2} \approx 0.8\overline{v_{n,rms}^2} \tag{6.6}$$

Substituting (6.6) into (6.1), and writing (6.6) only in terms of C_s using the relationship $C_{fb} = \frac{8}{6} \cdot C_s$, gives the following equation which can be solved for C_s:

$$\overline{v_{n,inband}^2} = (83\mu V_{rms})^2 \approx \frac{\frac{4kT}{C_s}\left(1+\frac{8}{6}\right)}{OSR}\ . \tag{6.7}$$

The value of C_s is 866-fF, which leads to 1.15-pF for C_{fb}. To accommodate manufacturing variation in absolute capacitance, C_s and C_{fb} are both enlarged to 900-fF and 1.2-pF, respectively. Table 6.1 lists the sampling capacitance for all five integrators. The 2^{nd} integrator's C_s is chosen based on the path mismatch requirement in Table 5.5, while the C_s of the 3^{rd}, 4^{th}, and 5^{th} integrators are chosen based on the required accuracy of the loop-filter coefficients.

6.1.2 Switch-level design

A switch-level circuit diagram of the 1^{st} integrator is shown in Figure 6.2. All capacitors are unit-sized with a nominal value of 75-fF (C_u). The feedback DAC consists of 15 unit-cells which combine to realize 4-b feedback. The switches are controlled by two non-overlapping clock phases and the timing diagram is shown in

Table 6.1: Half-circuit sampling capacitance for integrators.

Integrator	C_s
1^{st} integrator	900-fF
2^{nd} integrator	900-fF
3^{rd} integrator	150-fF
4^{th} integrator (k_2)	150-fF
5^{th} integrator (k_1)	150-fF

Figure 6.3. Two delayed versions of the each clock phase are generated to minimize charge-injection errors during switching. The period of each phase is exactly 5-ns for a 200-MS/s modulator. Since quantization occurs during the non-overlapping period, 1-ns is allocated for the comparator's latch to regenerate, and for the output of the quantizer to propagate through the DWA shifters. Therefore, the settling period, T_s, is about 4-ns for both ϕ_1 and ϕ_2.

Thanks to the low input common-mode voltage of a PMOS input folded-cascode amplifier, no clock boosting beyond the supply-rails is necessary for any switch. This ensures reliability because none of the switches are stressed above 1.8-V. To suppress signal-dependent aperture delay [24] during sampling, input switches s_1 and s_5 are bootstrapped to the signal to maintain a constant V_{gs} equal to the supply voltage [30]. For a full-scale input with 3.6-V peak-to-peak differential swing, the gate voltage of the input switch actually rises above the supply- rail to approximately $2{\cdot}A_{VCC}$. However, due to bootstrapping, the input switch is never subjected to a voltage difference more than A_{VCC} across any of the terminals at any given time. Therefore, reliability is maintained. A summary for the switches is provided in Table.6.2 with details on the clocking sequence, the type of the switch, and size.

At the end of charge-transfer phase, it is important to first turn off switches s_{10} and s_{12} before turning off any other switch. This is because charge injected into the input node of the amplifier, before s_{10} and s_{12} turn off, is sampled onto the

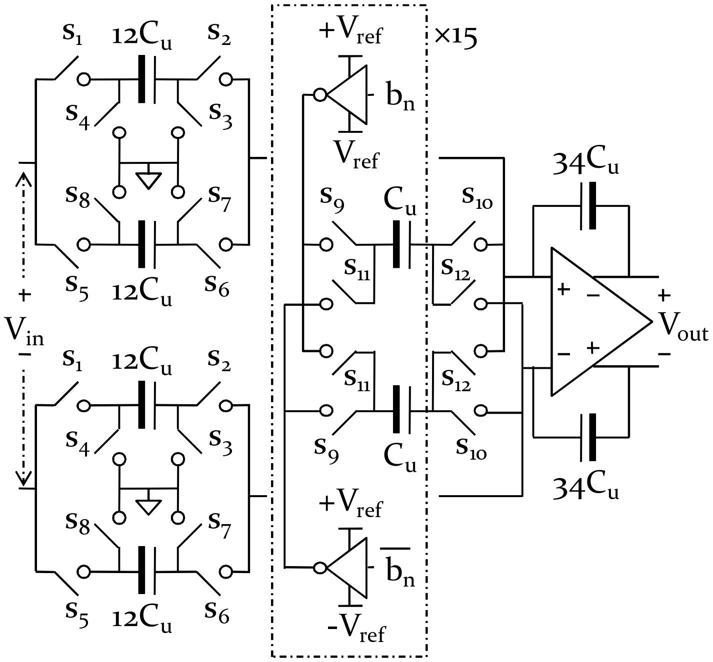

Figure 6.2: 1^{st} integrator.

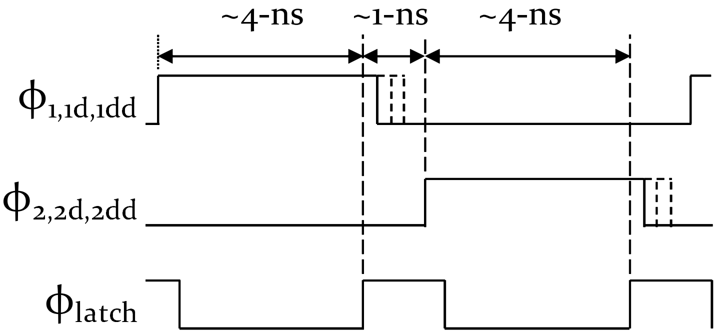

Figure 6.3: Clock phases.

Table 6.2: 1^{st} integrator switch summary.

Switch	**Clock**	**Type**	**W/L (μm/μm)**
s_1	ϕ_{1dd}	Bootstrapped NMOS	26.4/0.18
s_2	ϕ_{2dd}	NMOS	17/0.18
s_3	ϕ_{1d}	NMOS	19.2/0.18
s_4	ϕ_{2d}	NMOS	17/0.18
s_5	ϕ_{2dd}	Bootstrapped NMOS	26.4/0.18
s_6	ϕ_{1dd}	NMOS	17/0.18
s_7	ϕ_{2d}	NMOS	19.2/0.18
s_8	ϕ_{1d}	NMOS	17/0.18
s_9	ϕ_{1dd}	CMOS	N:0.86/0.18 P:3.2/0.18
s_{10}	ϕ_1	NMOS	7.52/0.18
s_{11}	ϕ_{2dd}	CMOS	N:0.86/0.18 P:3.2/0.18
s_{12}	ϕ_2	NMOS	7.52/0.18

feedback sampling capacitors [6]. In the subsequent cycle, this error charge adds directly to the sampled input signal and can deteriorate the modulator's dynamic range.

The previous subsection showed that the sampled noise of the amplifier can be minimized if the resistance of the switches responsible for charge-transfer is increased. From a speed perspective, smaller switches can increase the feedback factor, β, because it contributes less parasitic capacitance to the input node of the amplifier. Recall that the feedback factor is defined as

$$\beta = \frac{C_i}{C_i + C_s + C_{fb} + C_p} \tag{6.8}$$

where C_p is the parasitic capacitance at the amplifier's input node. According to (5.9) (repeated here),

$$\omega_{-3dB} = \frac{1}{\tau} = \beta \cdot \omega_u \tag{6.9}$$

the closed-loop settling speed of the integrator (ω_{-3dB}) is proportional to β. Therefore, smaller switches can actually increase the settling speed. Additionally, the unity-gain bandwidth of the amplifier, ω_u, is dependent on the effective load capacitance, C_{Leff}, which itself is dependent on the feedback factor:

$$C_{Leff} = (1-\beta)\cdot C_i + C_L \ . \tag{6.10}$$

Here, C_L is the shunt load capacitance at the output of the amplifier. With the switch sizes affecting so many variables, it is difficult to find the switch size that offers optimum tradeoff between speed, noise and power consumption. In this work, the sizes of s_2, s_6, s_{10} and s_{12} are chosen based on an iterative approach. An interesting study into this multi-variable optimization problem recently appeared in the literature, and the reader is encouraged to refer to [34] for more detail.

At the end of the design process after the circuit is laid out and parasitic capacitances are extracted, the effective differential load capacitance, C_{Leff}, can be found. For this prototype C_{Leff} is 7.6-pF, with C_p and C_L equal to 1.2-pF and 5.1-pF, respectively. Note that the C_p and C_L referred to here are the differential capacitance which includes both positive and negative paths. In practice, it is difficult to determine these capacitances *a priori* and estimations must be made. Using (6.8), β is found to be about 0.5 . With a T_s to τ ratio of 10 (Table 5.5) and a settling period of 4-ns, ω_u can be calculated with (6.9), resulting in $5{\cdot}10^9$ radians/s, or $\approx$ 800-MHz (f_u). In the next section, these numbers will be used to find the transconductance of the amplifier.

The analog common-mode voltage in Figure 6.2 is set at 600-mV. It is buffered on-chip with a circuit similar to the reference buffer described in [4]. The noise on the common-mode voltage is not critical to performance because the differential circuit does not see it. However, transient simulation suggests the common-mode voltage should settle quickly to guarantee proper differential settling. Therefore, a generous power budget is allocated to the buffer, which consumes 3.8-mA from the 1.8-V supply. The same buffer is shared between all five integrators. The input signal common-mode voltage is 900-mV ($\frac{1}{2} \cdot A_{VDD}$), and is governed by the input signal swinging from rail-to-rail. Under nominal conditions, this results in a 200-mV input common-mode voltage for the amplifier. Over process and temperature variations, the amplifier's input common-mode voltage varies from 0-V to 400-mV.

6.2 Gain-boosted folded-cascode amplifier

According to the specifications from the previous chapter, the 1^{st} integrator requires a dc gain of 60-dB. With 0.18μm technology, simple cascoding can only provide about 40-dB of dc gain, so here gain-boosting [33] is employed to enhance the gain to 70-dB. Amplifiers for integrators beyond the 1^{st} integrator require about half the speed performance. Therefore, the 1^{st} integrator's amplifier is scaled down by a factor of two and reused in the remaining four integrators.

6.2.1 Main amplifier

The amplifier topology is shown in Figure 6.4. A PMOS input folded-cascode is chosen for its low input common-mode voltage and wide output swing. The gain-boosting amplifiers are also fully-differential folded-cascode amplifiers. With an f_u target of 800-MHz and an effective load of 7.6-pF, the transconductance of the main amplifier can be determined [35] using

$$\omega_u = 2\pi \cdot f_u = \frac{g_m}{C_{Leff}} \ . \tag{6.11}$$

Plugging in the values for f_u and C_{Leff}, the transconductance, g_m, is 38-mS. To realize this transconductance, the amplifier's differential pair is biased with a 3.8-

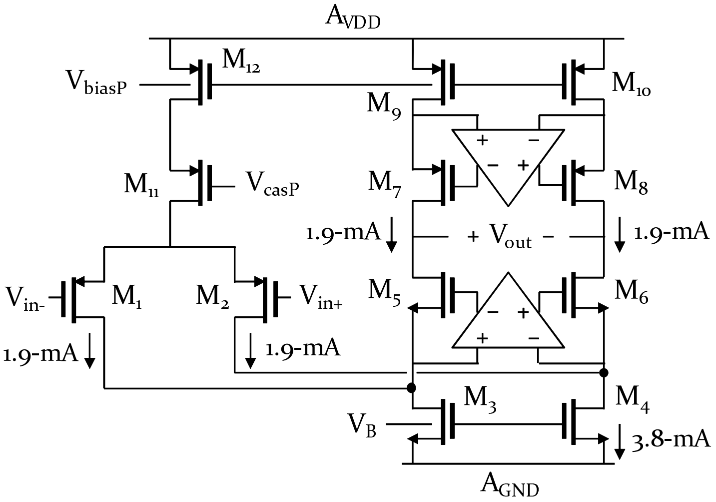

Figure 6.4: Folded-cascode amplifier with folded-cascode gain-boosting amplifiers.

mA current. A summary of the device sizes are listed in Table 6.3. The design steps outlined here are described in retrospect. In practice, C_{Leff} is not completely defined until the amplifier design is completed because C_p and C_L depend on the input and output parasitic capacitance, respectively.

For speed and for low input capacitance, the input-pair is usually realized with minimum length transistors. To meet a specific transconductance specification, the bias current and the device width can be adjusted. Large device widths can lower the bias current and save power, but doing so increases the input capacitance and lowers the feedback factor. A large bias current can reduce the device width and increase the feedback factor, but doing so consumes more power. In this design, an iterative approach is used to arrive at the final transistor size that balances bias current with the feedback factor.

To lower the input referred noise contribution of the bias transistors, their transconductance need to be less than the transconductance of the input-pair. In this design, the overdrive voltage of both the NMOS and PMOS bias transistors are about 300-mV. The cascode transistors contribute much less input-referred noise

Table 6.3: 1^{st} integrator amplifier.

Transistor	**W/L (μm/μm)**
M_1, M_2	275/0.18
M_3, M_4	102/0.27
M_5, M_6	96/0.18
M_7, M_8	256/0.18
M_9, M_{10}	358/0.36
M_{11}	512/0.18
M_{12}	717/0.36

Table 6.4: Integrator bias current.

Integrator	**Main**	**N-booster**	**P-booster**	**Total**
1^{st} integrator	7.6-mA	480-μA	960-μA	9-mA
2^{nd} integrator	3.8-mA	-	-	3.8-mA
3^{rd} integrator	3.8-mA	-	-	3.8-mA
4^{th} integrator	3.8-mA	240-μA	480-μA	4.5-mA
5^{th} integrator	3.8-mA	240-μA	480-μA	4.5-mA

because their current is defined by the bias transistor. Therefore, the g_m of both PMOS and NMOS cascode transistors can be reduced to lower the output capacitance of the amplifier. The overdrive voltages of the cascode transistors are about 250-mV, and the aggregate output swing of the amplifier is about 700-mV (1.4-V differential), which meets the specification in Table 5.5 for $\pm 0.4 \cdot V_{ref}$.

The remaining four integrators are half the size of the 1^{st} integrator's amplifier and consume half the power. Since the 2^{nd} and 3^{rd} integrators only require about 30-dB of dc gain, the gain-boosting amplifiers are removed to save additional power. The bias current for the various integrators are summarized in Table 6.4.

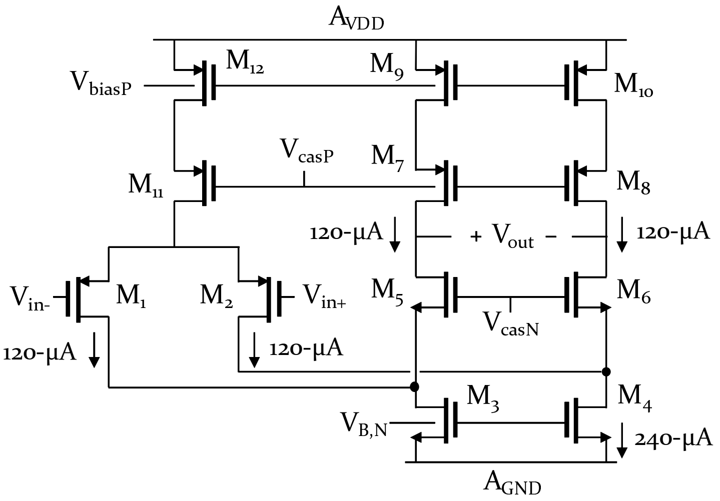

Figure 6.5: Gain-booster for NMOS cascode transistors.

6.2.2 Gain-boosters

Fully-differential amplifiers are used to boost the gain of the main amplifier. The gain-boosting amplifier for the NMOS and PMOS cascode transistors in Figure 6.4 are shown in Figure 6.5 and Figure 6.6, respectively. To ensure the speed of the gain-boosting amplifiers do not limit the settling speed of the main amplifier, the unit-gain frequency of the gain-boosting amplifier ($f_{u,boost}$) must be higher than the closed-loop -3dB frequency (f_{-3dB}) of the integrator [33]. At the same time, to guarantee stability, $f_{u,boost}$ must be lower than the main amplifier's second pole frequency [33]. In other words, the gain boosting amplifier needs to be fast enough, but not too fast that it destabilizes the main amplifier. A list of the transistor sizes for the NMOS and PMOS booster amplifiers are summarized in in Tables 6.5 and 6.6, respectively. The total bias current of the gain-boosting amplifiers are about 15% of the main amplifier's bias current, which is approximately the percentage suggested by the authors in [33].

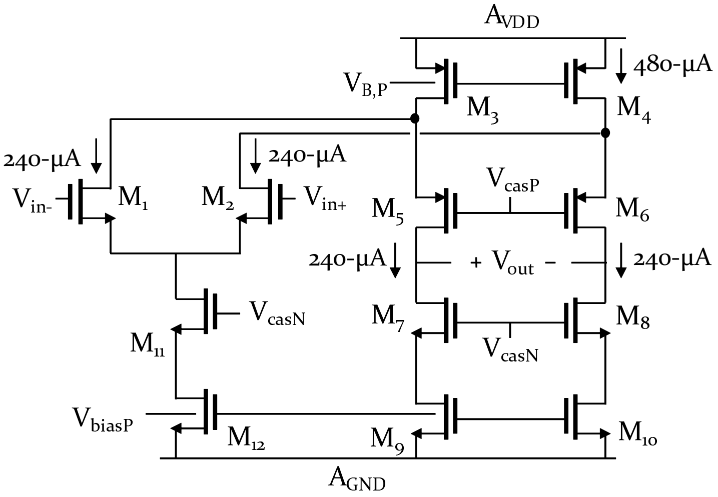

Figure 6.6: Gain-booster for PMOS cascode transistors.

Table 6.5: Gain-booster for NMOS cascode transistors.

Transistor	**W/L (μm/μm)**
M_1, M_2	17.2/0.18
M_3, M_4	6.4/0.27
M_5, M_6	6/0.18
M_7, M_8	16/0.18
M_9, M_{10}	22.4/0.36
M_{11}	32/0.18
M_{12}	44.8/0.36

Table 6.6: Gain-booster for PMOS cascode transistors.

Transistor	**W/L (μm/μm)**
M_1, M_2	16/0.18
M_3, M_4	89.6/0.36
M_5, M_6	32/0.18
M_7, M_8	12/0.18
M_9, M_{10}	6.4/0.27
M_{11}	24/0.18
M_{12}	12.8/0.27

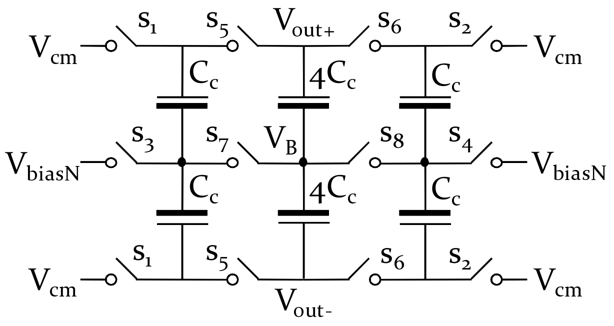

Figure 6.7: Double-sampled common-mode feedback circuit.

Table 6.7: 1^{st} integrator CMFB switch summary.

Switch	**Clock**	**Type**	**W/L (μm/μm)**
s_1	ϕ_{2d}	NMOS	0.48/0.18
s_2	ϕ_{1d}	NMOS	0.48/0.18
s_3	ϕ_{2d}	NMOS	0.48/0.18
s_4	ϕ_{1d}	NMOS	0.48/0.18
s_5	ϕ_{1dd}	CMOS	N:0.32/0.18 P:0.88/0.18
s_6	ϕ_{2dd}	CMOS	N:0.32/0.18 P:0.88/0.18
s_7	ϕ_{1d}	NMOS	0.48/0.18
s_8	ϕ_{2d}	NMOS	0.48/0.18

6.2.3 Switched-capacitor common-mode feedback

The main amplifier and the gain boosting amplifiers all employ switched-capacitor common-mode feedback (CMFB) to set the output common-mode voltage at half the supply voltage (900-mV). Since the entire modulator is double-sampled, a double-sampling CMFB circuit [36] is used. The CMFB circuit for the main amplifier is shown in Figure 6.7. Each unit-capacitor, C_c, is around 50-fF. Table.6.7 details the clocking sequence of the switches, the type of the switch, and its size.

To ensure the differential-mode signal settles quickly according to the ω_{-3dB} frequency of the main amplifier, the common-mode signal must also settle quickly so that the bias point of the amplifier can be defined for the differential-mode signal to settle. The speed of the CMFB circuit depends on the transconductance of the bias transistor the CMFB signal is fed back to. For the amplifier in Figure 6.4, this corresponds to M_3 and M_4. Although the bias transistor has a high overdrive voltage, its transconductance is still comparable to the input-pair (M_1 and M_2) because it is biased at twice the current. The -3-dB frequency of the CMFB circuit can be described by the following equation:

$$\omega_{-3dB,cmfb} = \beta_{cmfb} \cdot \omega_{u,cmfb} = \beta_{cmfb} \frac{g_{m34}}{C_{Leff,cmfb}} \ . \tag{6.12}$$

Here, $\omega_{u,cmfb}$ is the unit-gain bandwidth of the common-mode loop, β_{cmfb} is the feedback factor, g_{m34} is the transconductance of the bias transistor, and $C_{Leff,cmfb}$ is the effective common-mode load. The feedback factor, β_{cmfb}, is determined by the feedback capacitor, in this case it is $4 \cdot C_c$, and the parasitic capacitance at the gate of the bias transistor (M_3, M_4), which is approximately equal to C_{gs34}:

$$\beta_{cmfb} \approx \frac{4 \cdot C_c}{4 \cdot C_c + C_{gs34}} \ . \tag{6.13}$$

In this design, C_c is chosen so that β_{cmfb} is 0.5 as a compromise between CMFB settling speed and the additional capacitive load presented to the amplifier.

6.3 A 4-b Flash quantizer with time-interleaved offset-cancelation

In the previous chapter, Monte Carlo simulation showed that a quantizer with less than 0.35 LSB offset is needed to achieve 97% yield. To ensure the feedforward coefficients are realized accurately, a distributed passive summation network is employed. Fifteen unit-cells, each summing five inputs passively, compare the individual sums with one of fifteen threshold voltages. The gain-of-two factor assigned to the quantizer in Figure 5.9 is implemented by scaling down the threshold voltages of the reference ladder by a factor of two.

According to (3.2), if the quantized coefficients in Figure 5.9 are substituted for C_1 to C_5, the passive summing network attenuates the output by 10, assuming C_p is zero. In practice, C_p is not zero and the actual attenuation is worse. Empirically, for the unit-capacitor size chosen (20-fF), C_p (≈10-fF) causes the attenuation to increase to 10.5. Taking the factor-of-two scaling of the reference ladder into account, an otherwise full-scale signal swing (2.8-V), is now only 133-mV peak-to-peak ($\frac{1}{2}\cdot$2.8-V/10.5).

To meet specification, the quantizer must resolve a 133-mV range with 4-b resolution at no more than 0.35 LSB offset. This translates to 8.3-mV per LSB, or 2.9-mV per 0.35 LSB. Preamplification is necessary because the 3σ offset of the latch is in the tens of millivolts. For instance, if the latch has a 29-mV 3σ offset, the preamplifier must provide a minimum gain of 10 to meet the 0.35 LSB specification. This amount of gain at 200-MHz is not trivial for 0.18-μm technology, especially when the amplification has to take place while the integrators are settling. Keep in mind that this is the minimum gain required over process, temperature, and power supply variations. To achieve this minimum under extreme conditions, the nominal gain will be higher.

Further complicating the design effort, the preamplifier itself contributes offset. Increasing the size of the preamplifier's input-pair can reduce the offset. However, this is only feasible up to a certain point because C_p, which is largely due to the input capacitance of the preamplifier, can reduce the input swing according to (3.2). Therefore, offset-cancelation of some form for the preamplifier is necessary. In a double-sampled converter, however, it is not clear when the offset can be canceled given that no extra clock phase is available to perform the cancelation. Previous work has either used no cancelation at all for the 1-b case [5], or offset-averaging [37, 38] for the multi-bit case [6]. Both, however, are feedback type modulators and do not have a passive summation network that attenuates the signal by 10, and therefore the requirements here are more critical. In this work, a time-interleaved comparator architecture is proposed to solve this high-speed high-resolution quantization problem which will be described next.

6.3.1 Switch-level implementation

Shown in Figure 6.8 is the proposed time-interleaved offset-canceled comparator. The basic idea is to use two sets of preamplifiers in a time-interleaving manner so that when one set amplifies, the other performs offset-cancelation. As shown, each preamplifier is broken into two gain stages, A_1 and A_2, to make it easier to achieve the necessary gain without compromising speed. During offset-cancelation, the threshold voltage ($V_{th<n>}$) is saved on the sampling capacitors so that it can be subtracted from the summation of V_1 to V_5 in the next cycle. The preamplifiers amplify the aggregate result, and the latch makes a decision around a threshold of zero, generating the digital output for the unit-cell. Table 6.8 lists the switching sequence, type, and size of the switches in Figure 6.8.

During offset-cancelation, the unity-gain feedback loop closes and the offset of the preamplifier is stored on the sampling capacitors. During amplification, the stored offset cancels the offset of the preamplifier, essentially transforming the preamplifier into an offset-free preamplifier. This technique is referred to as input offset storage (IOS) in the literature [27]. In practice, IOS cancelation is imperfect because the gains A_1 and A_2 are finite and a residual input-referred offset term remains after cancelation. The following is the total input-referred offset of the

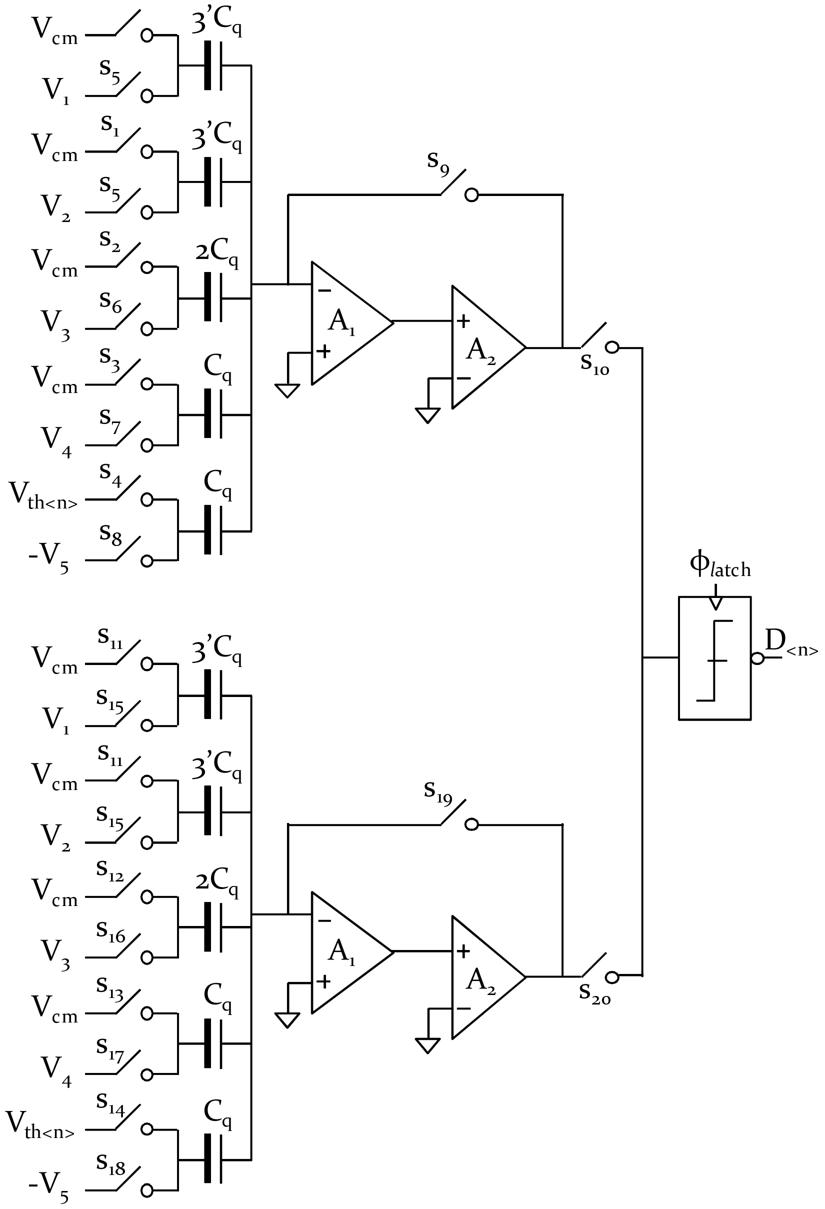

Figure 6.8: Single-ended version of time-interleaved comparator.

Table 6.8: Comparator switch summary.

Switch	**Clock**	**Type**	**W/L (μm/μm)**
s_1	ϕ_{1d}	NMOS	0.54/0.18
s_2	ϕ_{1d}	NMOS	0.36/0.18
s_3	ϕ_{1d}	NMOS	0.24/0.18
s_4	ϕ_{1d}	NMOS	(0.24 to 0.47)/0.18
s_5	ϕ_{2dd}	CMOS	N:0.48/0.18 P:1.44/0.18
s_6	ϕ_{2dd}	CMOS	N:0.36/0.18 P:1.08/0.18
s_7	ϕ_{2dd}	CMOS	N:0.24/0.18 P:0.54/0.18
s_8	ϕ_{2dd}	NMOS	0.24/0.18
s_9	ϕ_{1dd}	NMOS	1.2/0.18
s_{10}	ϕ_{1dd}	NMOS	0.42/0.18
s_{11}	ϕ_{2d}	NMOS	0.54/0.18
s_{12}	ϕ_{2d}	NMOS	0.36/0.18
s_{13}	ϕ_{2d}	NMOS	0.24/0.18
s_{14}	ϕ_{2d}	NMOS	(0.24 to 0.47)/0.18
s_{15}	ϕ_{1dd}	CMOS	N:0.48/0.18 P:1.44/0.18
s_{16}	ϕ_{1dd}	CMOS	N:0.36/0.18 P:1.08/0.18
s_{17}	ϕ_{1dd}	CMOS	N:0.24/0.18 P:0.54/0.18
s_{18}	ϕ_{1dd}	NMOS	0.24/0.18
s_{19}	ϕ_{2dd}	NMOS	1.2/0.18
s_{20}	ϕ_{1dd}	NMOS	0.42/0.18

preamplifier cascade:

$$V_{os,total} = \frac{V_{os,1} + \frac{V_{os,2}}{A_1}}{1 + A_1 A_2} + \frac{\Delta q}{C_{samp}} + \frac{V_{os,L}}{A_1 A_2} \tag{6.14}$$

The first terms is the residual offset that depends on the gain of the preamplifier, where $V_{os,1}$ and $V_{os,2}$ are the offsets of A_1 and A_2, respectively. The second term is the charge (Δq) of the reset switch (s_9 or s_{19}) absorbed by the total sampling capacitance C_{samp} when the reset switch turns off. The last term is the offset of the latch ($V_{os,L}$) after referring back to the input.

To see how much the residual offset affects the overall comparator, consider an example. Assume the gain of the preamplifier ($A_1 \cdot A_2$) is 10 and that $V_{os,2}$, Δq, and $V_{os,L}$ are all zero. Now, to achieve a worst case input-referred offset of 0.35 LSB (2.9-mV), the offset of A_1 must be less than 31.9-mV, which is a reasonable offset and cannot be overlooked. This example shows that even with IOS cancelation, it is still possible for the offset of A_1 to limit the performance of the comparator. As for the offset of A_2, since $V_{os,2}$ is further divided by the gain of A_1, its effect is less as critical.

To minimize Δq, the reset switch must be small. This is accomplished by using only an NMOS transistor to implement the switch. To do so, the input common-mode voltage of A_1 and the output common-mode voltage of A_2 must be low enough so that the switch can be turned on effectively. Therefore, an approach that uses a PMOS input first stage (A_1) in combination with a pseudo-differential NMOS input second stage (A_2) [34] is taken. The topology is shown in Figure 6.9. During transient simulation, it was discovered that the second stage (A_2) can be trapped in a stable bias point where all transistors are off. Therefore, transistors M_{14}, M_{15}, and M_{16} are added to ensure the preamplifier starts up correctly. As long as the supply voltage is greater than $3 \cdot V_{th}$, the preamplifier is guaranteed to

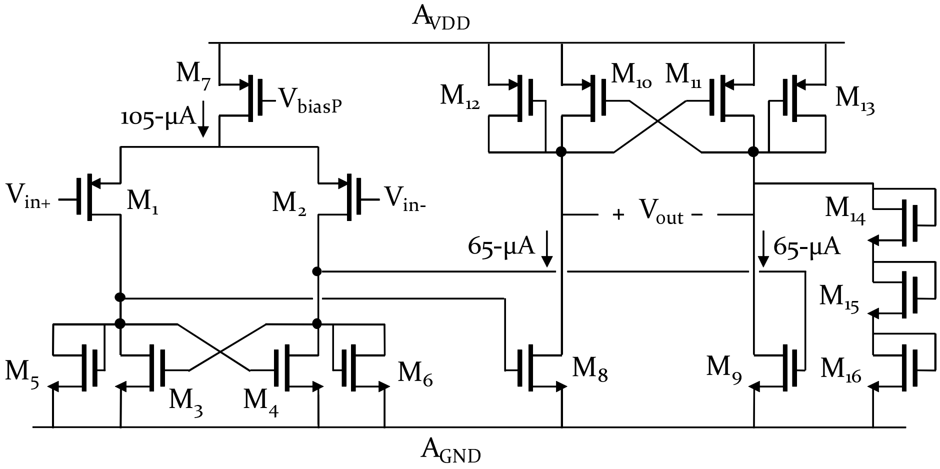

Figure 6.9: Two-stage preamplifier for comparator unit-cell.

start. Note that the startup transistors are only added to one side of A_2 because the imbalance it creates on the other side is minimal when referred to the input of the comparator.

6.3.2 Preamplifiers

To ensure the quantizer meets specification under process, temperature, and power supply variations, the nominal gain of two-stage preamplifier is set at 19. This gain is split unevenly between A_1 and A_2, with A_1 responsible for a gain of 3.7 and A_2 responsible for a gain of 5.1. Relaxing the gain of A_1 allows the input-capacitance of A_1 to be smaller, which helps to preserve the signal swing at the output of the passive summation network. The overall -3-dB frequency of the preamplifier during amplification is 518-MHz, with the -3-dB frequency of A_1 at 1.15-GHz, and the -3-dB frequency of A_2 at 709-MHz.

When the preamplifier is put in feedback mode, the capacitive loading of A_2 increases significantly. This causes the open-loop -3-dB frequency of A_2 to shift down from 709-MHz to 48-MHz, and the open-loop unit-gain frequency of the overall preamplifier to decrease from 4.4-GHz to 760-MHz. In unity-gain feedback, it is the open-loop unity-gain frequency that sets the settling speed of the preamplifier. Therefore, with a period of 4-ns, the preamplifier has about 19 time-constants to settle to its final value, which is much more than necessary. Since A_1 sees the same capacitive load during both amplification and offset-cancelation, its dominant pole frequency, which is also the non-dominant pole during offset-cancelation, stays put at 1.15-GHz. The resulting phase margin of the preamplifier with an open-loop unity-gain frequency of 760-MHz and a non-dominant pole at 1.15-GHz is 60 degrees. The bias current for A_1 and A_2 are 105-μA and 130-μA, respectively. Table 6.9 summarizes the transistor sizes for the preamplifier. The 3σ offset of A_1 ($V_{os,1}$) is estimated to be about 34-mV based on extrapolated data from the manufacturer. Under nominal conditions, this results in an input referred offset of 1.7-mV (34-mV/(1+$A_1 \cdot A_2$)).The reader is referred to [40] for more information on transistor matching models. To increase the gain of both preamplification stages, a small amount of positive feedback is added [28]. Transistors M_3 and M_4 boosts the gain of A_1 by about two through the following relationship [27]:

$$A_v = \frac{g_{m12}}{g_{m56}} \frac{1}{1 - \dfrac{g_{m34}}{g_{m56}}} \tag{6.15}$$

The ratio between g_{m34} and g_{m56} determines the multiplication factor of the gain. Using (6.15), the gain of the first and second stage are at about 3.7 and 5.1, respectively.

6.3.3 Regenerative latch

The topology of the regenerative latch is shown in Figure 6.10. A differential structure with cross-coupled positive feedback is employed. The output is buffered and latched by a digital SR-latch. Unlike conventional regenerative latches where both

Table 6.9: Comparator preamplifier.

Transistor	**W/L (μm/μm)**
M_1, M_2	4/0.18
M_3, M_4	0.24/0.24
M_5, M_6	0.48/0.24
M_7	22.4/0.36
M_8, M_9	1.8/0.36
M_{10}, M_{11}	0.44/0.18
M_{12}, M_{13}	0.68/0.18
M_{14}, M_{15}, M_{16}	0.24/0.18

NMOS and PMOS transistors are cross-coupled for positive feedback regeneration [42, 43], this topology relies only on NMOS for regeneration [41]. With NMOS-only regeneration, this topology is believed to offer higher regeneration speeds because the mobility of PMOS transistors in modern-day technologies is much lower than NMOS, resulting in diminishing returns for adding it to the circuit and loading down the output [41]. As an added benefit, this latch offers a low output common-mode voltage which helps to lower the turn-on resistance of the reset switch. During regeneration and while $\overline{\phi}_{latch}$ is asserted, the bias current of the latch is about 103-μA. The standard deviation of the input-referred offset due to threshold voltage mismatch is equal to

$$\sigma(V_{os,L}) = \sqrt{\left(\frac{g_{m34}}{g_{m12}} \cdot \frac{A_{VTN}}{\sqrt{W_{34} \cdot L_{34}}}\right)^2 + \left(\frac{A_{VTP}}{\sqrt{W_{12} \cdot L_{12}}}\right)^2} \tag{6.16}$$

where A_{VTN} and A_{VTP} are the area proportionality constants for NMOS and PMOS transistors, respectively. These constants, if not available from the manufacturer, can be estimated based on device scaling trends and published reference data points [44]. Table 6.10 lists the transistor sizes of the latch used in the prototype. Based on data from the manufacturer, the 3σ input-referred offset of the latch is about

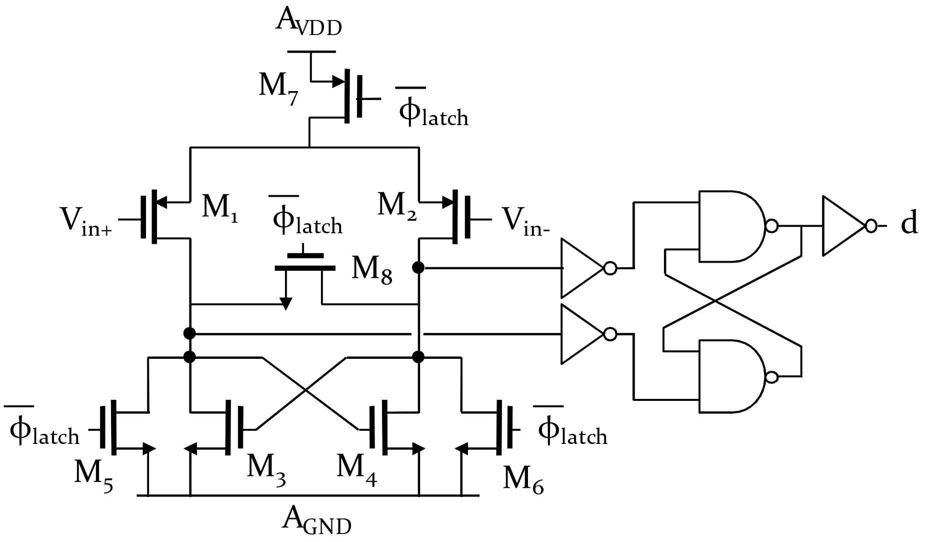

Figure 6.10: Comparator regenerative latch.

43-mV.

Referring back to the comparator's input with a preamplifier gain of 19, the contribution of $V_{os,L}$ is about 2.3-mV, or 0.28 LSB. If the offset of the second stage of the preamplifier is assumed negligible when referred back to the comparator's input, the combined 3σ offset of the preamplifier and the latch is about 2.8-mV ($\sqrt{(2.3mV)^2 + (1.7mV)^2}$), or 0.34 LSB, under nominal conditions. This is less than what is expected because the specification requires 0.35 LSB under *worst case* conditions. However, due to time constraints and the prototype nature of the project, no further effort was made to improve the design.

An important point to note is that in (6.16), the expression only takes into account of static offsets originating from threshold voltage mismatch. An improvement to the latch is possible if M_8 is clocked with a slightly delayed version of $\overline{\phi}_{latch}$ to eliminate any dynamic offsets due to output capacitance mismatch [41].

Table 6.10: Comparator latch.

Transistor	**W/L (μm/μm)**
M_1, M_2	3.84/0.18
M_3, M_4	1.28/0.24
M_5, M_6	0.24/0.18
M_7	2/0.18
M_8	0.24/0.18

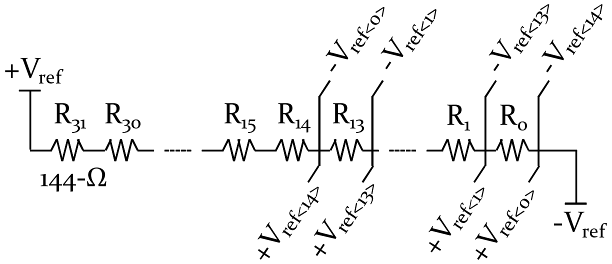

Figure 6.11: Quantizer reference ladder.

6.3.4 Reference ladder

To implement a gain-of-two coefficient for the quantizer, the reference ladder is constructed with 32 unit-sized resistors and 15 differential reference voltages are tapped off it. The ladder is shown in Figure 6.11. Each unit-resistor has a nominal resistance of 144-Ω. Instead of tapping the reference voltages from the middle of the ladder, they are tapped from the bottom so that NMOS-only switches can be used to lower the parasitic capacitance on the ladder.

6.4 Data Weighted-Averaging

The DWA algorithm [22] is used to rotate the global feedback capacitors for linearization. The goal of DWA is to give each unit-capacitor the same amount of utilization in sequential order. This results in excellent mismatch cancelation and

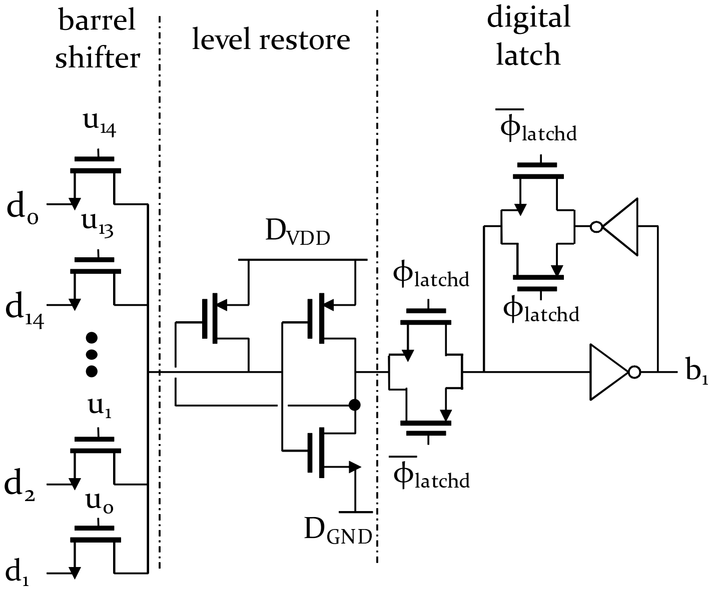

Figure 6.12: DWA feedback path.

was shown earlier in the previous chapter. At the end of a cycle, the quantizers generates a 15-b digital output. This data pases through a digital barrel shifter that has been preset to shift a number of bits equal to the previous digital output value. The propagation speed of the barrel shifter is critical because the amplifiers cannot start the next cycle until the digital feedback reaches the 1^{st} integrator. The custom digital feedback path used in the prototype is shown in Figure 6.12 for b_1 of the 15-b output. The signals u_0 to u_{14} control how the bits are shifted and are generated before the quantizer outputs are ready. To minimize parasitic capacitance in the barrel shifter, only NMOS transistors are used. This results in a low logic-high output voltage, which necessitates a level-restore buffer [4] as shown in the figure. After level-restore, the digital signal is latched until the next sample is available. In the figure, the signal $\overline{\phi}_{latchd}$ is a delayed version of $\overline{\phi}_{latch}$.

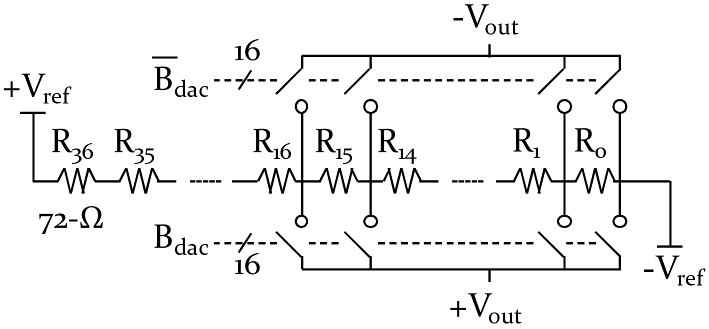

Figure 6.13: 4-b DAC.

6.5 4-b DAC

The feedback path around the quantizer is constructed with a resistor-string DAC. To implement the 16/37 coefficient, the DAC uses 37 unit-sized resistors. A total of 16 equally spaced differential voltages are tapped off the ladder. The DAC is shown in Figure 6.13. A 16-b signal, B_{dac}, turns on one of 16 switches to generate the positive output for the DAC. Similarly, $\overline{B}_{dac}$ turns on one of 16 switches to generate the negative output for the DAC. Each unit-resistor has a nominal resistance of 72-Ω. To lower the parasitic capacitance on the ladder, the DAC ladder is tapped from the bottom so that NMOS-only switches can be used.

6.6 Reference buffer

To maximize dynamic range, the reference voltages should be as wide as possible. The best scenario is to use the supply rails for reference. However, at 200-MS/s, it is uncertain how much noise is on the power supply. If the noise or the ringing on the power supply is signal dependent, it can introduce distortion at the output. Therefore, for power-supply rejection, it is sensible to buffer the voltage references $+V_{ref}$ and $-V_{ref}$ on-chip. The buffer circuits are shown in Figure 6.14 [4]. This buffer provides a lower impedance than a simple source-follower, and has a power

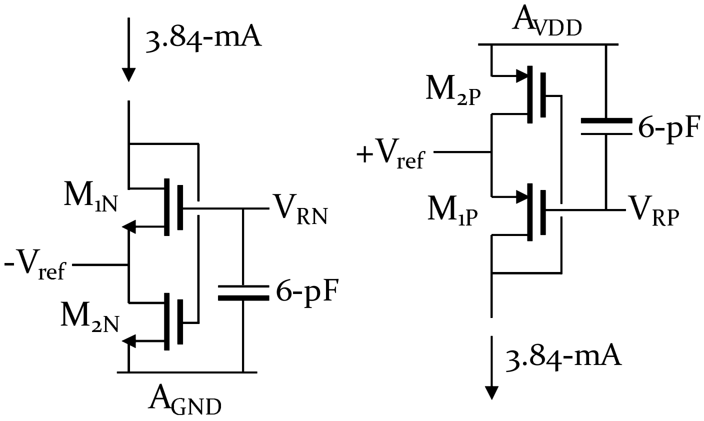

Figure 6.14: Differential reference buffers.

Table 6.11: Reference buffer

Transistor	**W/L (μm/μm)**
M_{1N}	192/0.18
M_{2N}	518/0.18
M_{1P}	512/0.18
M_{2P}	806/0.18

supply rejection of 25-dB within the passband. The buffered voltage references are nominally 200-mV and 1.6-mV for -V_{ref} and +V_{ref}, respectively, and are derived from off-chip voltages, V_{RN} and V_{RP}. Both reference buffers consume 3.84-mA. A 6-pF bypass capacitor is placed at the gate of M_{1N} and M_{2N} to low-pass filter any noise on V_{RN} and V_{RP}. As an option, the buffers can be turned off so that the supply rails become the reference. This is described in Chapter 8.

6.7 Bias circuits

A single external bias current of 240-μA controls the biasing of the entire chip. This current is mirrored and distributed to different parts of the chip where a local biasing circuit, shown in Figure 6.15, generates the local bias voltages. This ensures

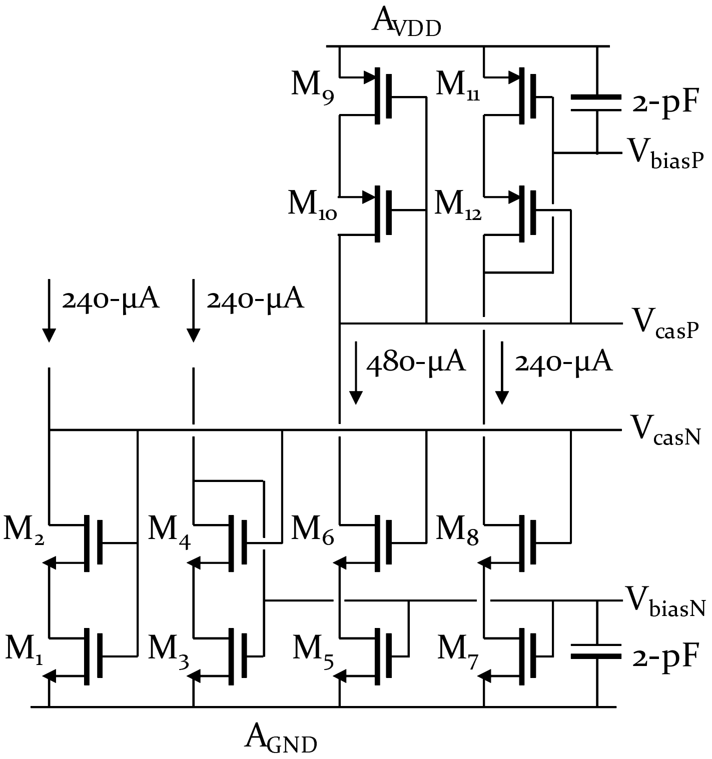

Figure 6.15: Biasing circuit for amplifiers.

the amplifiers are properly biased even if the ground voltages are not the same in different areas of the chip. Four copies of the same biasing circuit are used in the prototype. Three for biasing amplifiers and one for biasing the reference buffer. Each bias circuit consumes 1.2-mA. Table 6.12 lists the transistor sizes of the circuit.

Table 6.12: Bias circuit

Transistor	**W/L (μm/μm)**
$M_1$6.12	/0.6
M_2, M_4, M_8	12/0.18
M_3, M_7	6.4/0.27
M_5	12.8/0.27
M_6	24/0.18
M_9	33.6/0.36
M_{10}	64/0.18
M_{11}	44.8/0.36
M_{12}	32/0.18

Chapter 7

Peripheral Circuits

Apart from the circuits described in the previous chapter, a number of other circuits are important to the proper operation of the modulator. These include the Low-Voltage Differential Signaling (LVDS) clock amplifier, a set of LVDS digital output transmitters, and the electro-static discharge circuitry. Each of these circuits have its own requirements that must be satisfied and will be described in the following sections. The packaging choice, die orientation, and pin assignment are also discussed in this chapter.

7.1 LVDS clock amplifier

According to behavioral simulation results in Figure 5.25, the clock's 3σ jitter at the critical input signal sampling switch must be less than 0.2% relative to the sampling period T_s. At 200-MS/s, this translates into 10-ps 3σ jitter, or 3.3-ps$_{rms}$ jitter. Note that these calculations are based on the assumption of a Gaussian distributed jitter profile, which is appropriate if the jitter source originates from thermal noise. For power supply noise induced jitter, it is more appropriate to model it with a uniformly distributed profile [24]. Since there are few digital circuits in the prototype, the noise

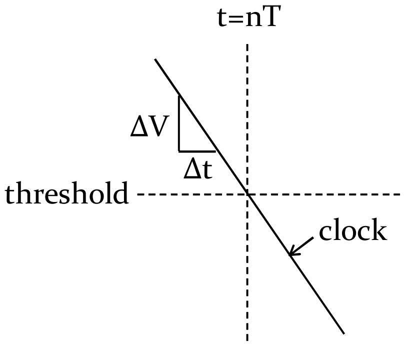

Figure 7.1: Electronic noise to jitter translation.

on the power supply is largely periodic and should not affect jitter performance.

A survey of commercially available clock sources found that Ecliptek's EL18D8 oscillator offers a reasonably good jitter performance at 700-fs$_{rms}$ and is available for purchase in small quantities. Therefore, EL18D8 is chosen for this project. The oscillator's LVDS output has a common-mode voltage of ≈1.25-V and a differential swing of 350-mV when terminated by a 100-Ω resistor. The purpose of the on-chip LVDS clock amplifier is to amplify this small external clock signal up to full-scale digital swing (1.8-V), all while satisfying the 3.3-ps$_{rms}$ jitter requirement at the sampling switch.

To see how critical this specification may be, consider Figure 7.1. The figure shows a clock signal with a slope equal to $\frac{\Delta V}{\Delta t}$ crossing a threshold at a sampling instant equal to nT, where n is an integer and T is the sampling period. The threshold represents an abstract voltage at which a sampling switch opens or a clock buffer switches from one state to the other. As shown, no error exists at the sampling instant because the clock crosses the threshold at nT. In reality, thermal noise can shift the crossing point horizontally in time. Since thermal noise has a Gaussian distributed profile, the time-domain error will also have a Gaussian profile. The modulator's specification requires the standard deviation of this time-domain error to be less than 3.3-ps.

When the LVDS clock input is amplified, noise is also amplified with it. This results in no net jitter improvement even with a noiseless amplifier. If amplifier noise is factored in, then jitter increases. Therefore, it is desirable to keep the amplifier's noise to a minimum and the gain to a maximum. A two-stage approach is taken to amplify the clock and is depicted in Figure 7.2. The first amplifier has a gain of 19.3-dB and a -3-dB frequency of 420-MHz. To minimize thermal noise, the -3-dB frequency should be no higher than necessary. For this design the -3-dB frequency is about twice the clock frequency.

A second amplifier is used to further speed up the edge of the clock. Since the second amplifier has a faster slope than the first amplifier, its bandwidth needs to be higher. Therefore, the gain is relaxed to 16.9-dB to allow the -3-dB frequency to be pushed up to 1.08-GHz. This additional bandwidth increases the noise of the second amplifier. However, it is suppressed by the slope gain of the first amplifier, and therefore justified.

Beyond the second amplifier, as long as the slope of the clock edge is maintained, the noise contribution of subsequent stages should be negligible. Finally, after the clock is brought to full-scale, it is divided down by D flip-flops to generate two complementary 100-MHz clocks. The matching of the master clock's duty cycle does not affect the matching of the two complementary clocks because the complementary clocks are triggered by the same edge of the master clock.

The transistor-level implementation of the two-stage LVDS clock amplifier is shown in Figure 7.3. An NMOS input differential pair with self-biased loads are employed in both amplifiers. The self-biased resistors are adjusted to control the bandwidth and gain of the two amplifiers. Transistors M_9 to M_{12} perform differential to single-ended conversion and converts the clipped differential 1.8-V output swing of the second amplifier to a single-ended 1.8-V digital signal. The total static bias current of the two-stage amplifier is 1.2-mA. The transistor sizes are summarized in

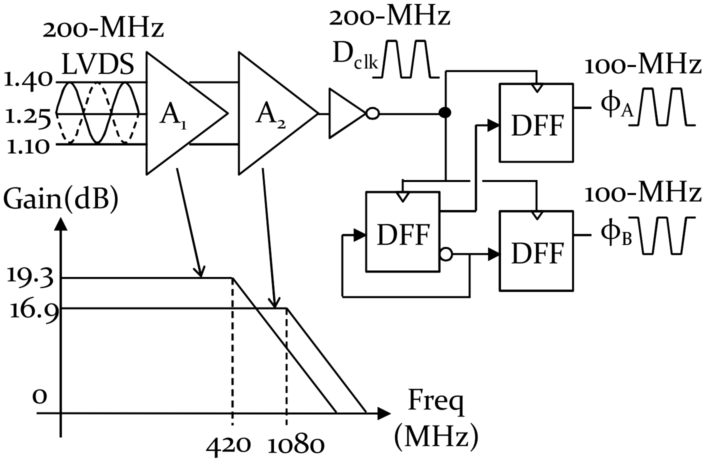

Figure 7.2: LVDS clock chain.

Table 7.1.

Due to a lack of characterization data, the clock source is assumed to be a sinusoid. This is a conservative assumption because a sinusoid has a much slower clock edge than a square wave. Using this model, transient simulation shows that the slope of the clock edge at the output of the first and the second amplifiers are $1460\frac{V}{\mu s}$ and $4930\frac{V}{\mu s}$, respectively. Noise simulation suggests that the first and second amplifiers have an output noise of 1.12-mV$_{rms}$ and 1.29-mV$_{rms}$, respectively. Translating these results to the time-domain using the following equation results in an RMS jitter 1.07-ps at the output of the second amplifier:

$$\begin{aligned}\sigma_{jitter} &= \sqrt{(\sigma_{source})^2 + \left(\frac{\sigma_{n,1}}{\frac{\Delta v_1}{\Delta t_1}}\right)^2 + \left(\frac{\sigma_{n,2}}{\frac{\Delta v_2}{\Delta t_2}}\right)^2} \qquad (7.1)\\ &= \sqrt{(0.7ps_{rms})^2 + \left(\frac{1.12mV_{rms}}{1460\frac{V}{\mu s}}\right)^2 + \left(\frac{1.29mV_{rms}}{4930\frac{V}{\mu s}}\right)^2}\\ &= \sqrt{(0.7ps_{rms})^2 + (0.77ps_{rms})^2 + (0.26ps_{rms})^2} = 1.07ps_{rms}\end{aligned}$$

It is easy to see that the first amplifier dominates the second amplifier when jitter powers are added. With a 0.7-ps$_{rms}$ source, the first amplifier adds noise to the clock and increases the accumulated jitter from 0.7-ps$_{rms}$ to 1.04-ps$_{rms}$. Similarly, the second amplifier adds noise to the clock, but the accumulated jitter changes only by 0.03-ps$_{rms}$ to 1.07-ps$_{rms}$. This suggests that noise further downstream can be neglected as long as the slope of the clock edge is maintained, assuming the sampling clock propagates through a reasonable number of buffers (less than 10) to reach the sampling switch. Table 7.2 summarizes the results obtained in this section.

7.2 LVDS transmitter

At 200-MHz, high-speed digital CMOS outputs with fast voltage transients can radiate through bondwires back into sensitive analog signals. To reduce this type of coupling, LVDS is employed to transmit digital data off-chip. With differential current-mode operation, the bondwires enjoy low voltage swings and differential cancelation. Thus improving the fidelity of sensitive analog signals. The LVDS driver implemented in the prototype is shown in Figure 7.4. It is based on the double current sources (DCS) topology [8] for low-voltage operation at 1.8-V supply.

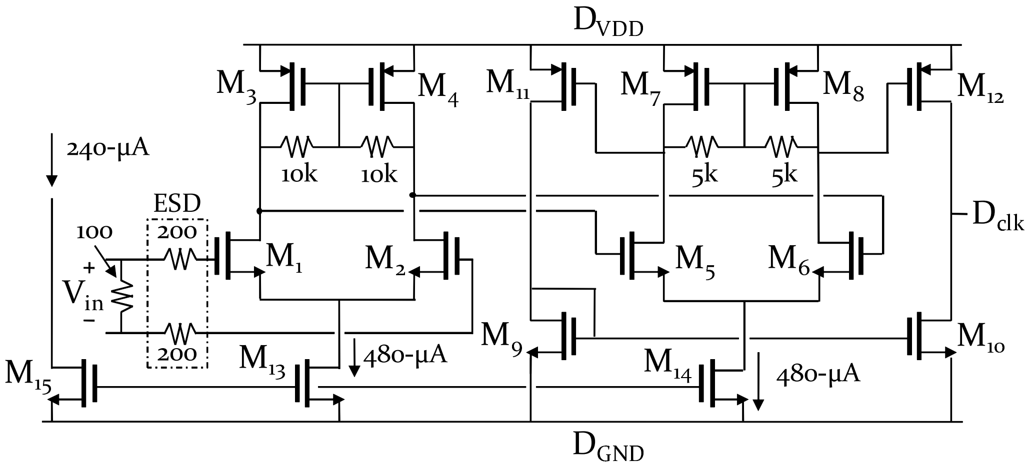

Figure 7.3: LVDS clock two-stage amplifier.

Table 7.1: LVDS clock amplifier

Transistor	**W/L (μm/μm)**
M_1, M_2	16/0.18
M_3, M_4	32/0.18
M_5, M_6	16/0.18
M_7, M_8	32/0.18
M_9, M_{10}	1.2/0.18
M_{11}, M_{12}	3.84/0.18
M_{13}, M_{14}	12.8/0.27
M_{15}	6.4/0.27

Table 7.2: LVDS clock amplifier jitter summary.

	Oscillator	**Amplifier 1**	**Amplifier 2**
dc gain	-	19.3-dB	16.9-dB
f_{-3dB}	-	420-MHz	1.08-GHz
Differential output swing	0.35-V	2.0-V,(clipped)	1.8-V (clipped)
Input slope	-	$152\frac{V}{\mu s}$	$1460\frac{V}{\mu s}$
Output slope	$152\frac{V}{\mu s}$	$1460\frac{V}{\mu s}$	$4930\frac{V}{\mu s}$
Output noise	-	1.12-mV	1.29-mV
Jitter contribution	0.7-ps$_{rms}$	0.77-ps$_{rms}$	0.26-ps$_{rms}$
Accumulated jitter	0.7-ps$_{rms}$	1.04-ps$_{rms}$	1.07-ps$_{rms}$

Table 7.3: LVDS transmitter

Transistor	**W/L (μm/μm)**
M_1, M_2	44.8/0.18
M_3, M_4	268.8/0.27
M_5, M_6	11.2/0.18
M_7, M_8	134.4/0.27
M_9	204.8/0.27
M_{10}	51.2/0.27
M_{11}, M_{13}	12.8/0.27
M_{12}	67.2/0.27

Continuous-time common-mode feedback is implemented via a differential pair to set the common-mode voltage of the driver at 1.15-mV. The total bias current is 5.28-mA per channel. The transistor sizes of the LVDS driver are listed in Table 7.3. Besides four digital data outputs, a clock with a frequency equal to $1/7^{th}$ the master clock frequency is also driven off-chip via LVDS. This clock is used to synchronize the latching instant of the four digital channels with an external LVDS deserializer[1].

---

[1] The deserializer chosen is the Texas Instruments SN65LVDS94, LVDS SerDes Receiver.

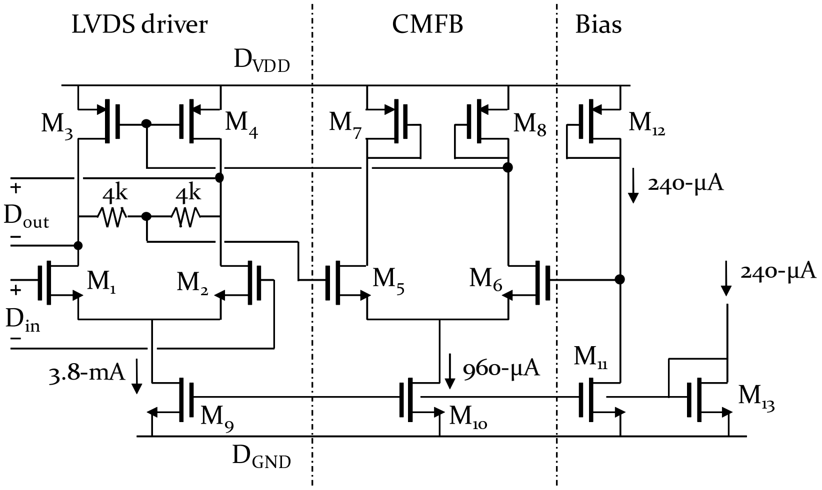

Figure 7.4: LVDS output driver.

7.3 Electro-static discharge (ESD) circuitry

Electro-static discharge (ESD) protection is important in integrated circuits because static electricity can build up on human bodies and manufacturing equipment. Even machines that bond die to package can damage the circuit through ESD. No ESD libraries are available to the author, so all ESD protection circuits are custom designed using snapback transistors [46] as the main ESD conduction element. Figure 7.5 shows the topology of the ESD protection circuitry. Only two pad rings are laid out around the chip. One is for the analog supply (A_{VDD}) and the other is for the analog ground (A_{GND}). The digital supply (D_{VDD}) and digital ground (D_{GND}) are brought on-chip via an analog I/O ESD pad just like any other I/O signal. All off-chip inputs that connect directly to the gate of any on-chip transistor are placed in series with a 200-Ω resistor to prevent any ESD spikes from damaging the gate-oxide before snapback occurs [46]. To improve the current conduction capability of the snapback devices, the drains of the snapback devices are salicide-blocked. This increases the drain's resistance so that when the device turns on, the current is more evenly distributed across its width of the device [46]. Given these ESD

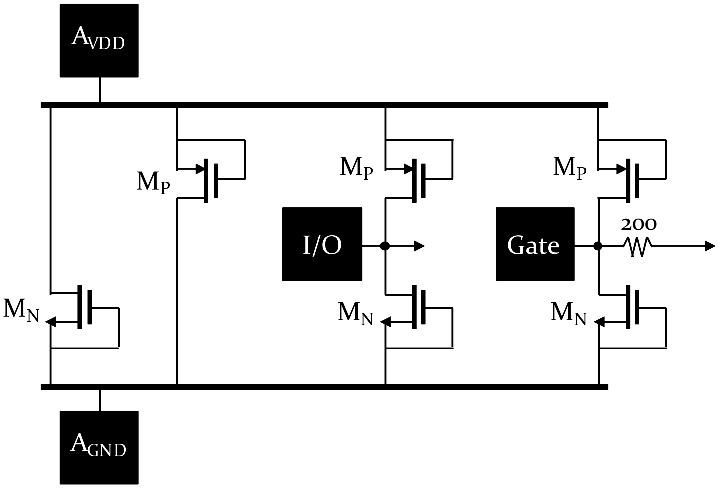

Figure 7.5: ESD topology

Table 7.4: ESD snapback transistors

Transistor	**W/L (μm/μm)**
M_N	320/0.28
M_P	400/0.28

countermeasures, according to the manufacturer's guidelines, this ESD protection circuit should withstand 2000-V Human Body Model (HBM) shock. The sizes of the snapback devices are listed in Table 7.4.

7.4 Packaging

In high-speed data converters, the right package choice can have a significant impact on performance. The issue mainly revolves around package and bondwire inductances, which cause many undesirable effects for both analog and digital circuits. Bondwire inductance in digital circuits cause power supply lines to ring and radiate energy. This energy can be picked up by nearby bondwires carrying sensitive analog signals, possibly reducing the dynamic range of the analog circuit or increasing its harmonic distortion if the digital energy is data dependent.

Package inductance can be minimized by choosing a package with no leads, such as a Quad Flat No leads (QFN) package. To minimize bondwire inductance, the length of the bondwire must be kept to a minimum. This requires the die to fit as close to the sidewalls of the package as possible. However, this is not always possible because the die may be too big or too small for a certain package with the desired pin count. For example, the prototype in this work has a die size of 1.5-mm by 1.5-mm. It can physically fit into a 4-mm by 4-mm QFN package with a die pad area of 2.3-mm by 2.3-mm plus enough space for die-attach, resulting in bondwire lengths of approximately 0.4-mm to 0.5-mm. However, QFN 4-mm by 4-mm packages are only available for pin counts up to 24 pins. This prototype requires at least 32 pins. Therefore, the prototype is forced into a 5-mm by 5-mm QFN that is otherwise too big for the die. The new die pad area is 3.3-mm by 3.3-mm, which approximately doubles the length of every bondwire from 0.5-mm to 1-mm! As a rule-of-thumb, the inductance of 1-mm of bondwire is approximately 1-nH.

Taking advantage of the fact that some pins are more sensitive than others and some require lower impedances to off-chip bypass capacitance, it is possible to situate the die in the package such that the bondwires of the sensitive pins are shortened at the expense of other less critical pins. This is shown in Figure 7.6. The picture is the actual prototype in a 5-mm by 5-mm QFN-32 package[2]. Some of the pins are double-bonded, which means two bondwires connect the same package pin to the same pad, essentially halving the inductance. Furthermore, the pins along the middle of the package have shorter bondwires and package inductances than pins near the corners. Therefore, critical signals such as the analog input should be placed in the middle, and is done so for this design.

The package offers an exposed ground pad at the bottom of the package for

---

[2] Packaged by Catalyst Microtech LLC, Austin, TX

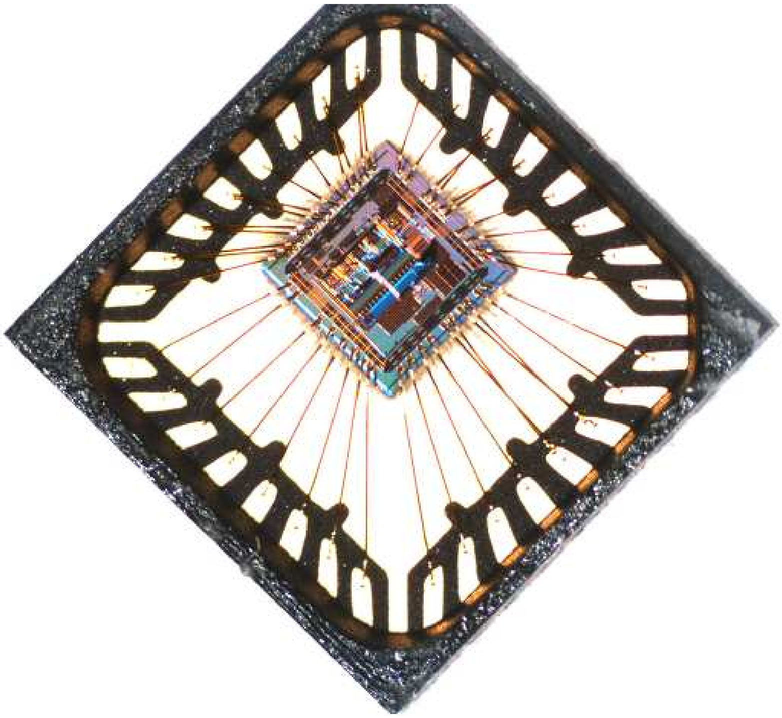

Figure 7.6: Die orientation skewed to corner of package.

improved thermal conductivity and low inductive path to the substrate. Neither of these properties are taken advantage of because the prototype dissipates less than 150-mW, and has a high-resistivity substrate that hardly benefits from a low inductive path to ground through the substrate. On the other hand, if the prototype is fabricated on a low-resistivity epitaxial wafer, the exposed ground pad can significantly improve performance [47]. Nonetheless, the backside of the die is attached to the ground pad with a thermally and electrically conductive epoxy.

7.5 Pin assignment

A great deal of attention is paid to properly assign the package pins of the prototype. Many conflicting aspects of the design have forced a compromise between performance and practicality. At the very least, the original target for the prototype is to have 44 pins, with over 10 analog supply and ground pins and multiple digital supply and ground pins. However, after multiple iterations of assigning a set of pins and then performing package parasitic simulation, it is determined that a smaller 32-pin package with less supply pins but shorter bondwires, actually outperforms the larger 44-pin package.

According to isolation requirements in Figure 5.24 between the signal and the reference voltage, the reference needs to be isolated from the input by 80-dB. This is difficult to guarantee with bondwires being so close together. However, four different techniques can be used to improve the isolation. First, all intruding and sensitive signals can be routed differentially, meaning differential signals are always assigned to adjacent pins. Second, the sensitive signals can be shielded by ground pins on both sides to improve the isolation from nearby bondwires. Third, the sensitive pin can be placed perpendicular to the intruding pin so that to first order, the bondwires do not couple to each. Fourth, the physical distance between the sensitive and the intruding signals can be increased. This is less effective than the previous three, but nonetheless is still an option to increase isolation.

The above techniques are incorporated as much as possible to the prototype's pin assignment. Shown in Figure 7.7 are the final pin assignments. Notice the analog input is perpendicular to the reference voltage (V_{RN} and V_{RP}). Also, there is only one digital supply and ground pin. However, the digital supply is double-bonded and is complemented by a large on-chip bypass capacitor having a capacitance of about 1-nF, constructed with MOS transistors. In the figure, elongated pads indicate that the pin is double-bonded. A summary of the pin assignments is provided in Table 7.5.

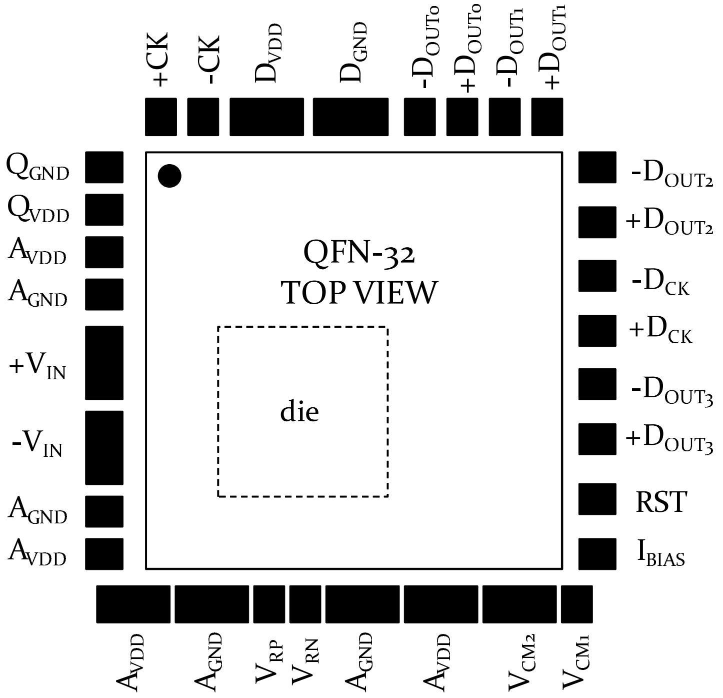

Figure 7.7: Pin-assignment.

Table 7.5: Pin summary

Signal	**Pins**	**Description**
A_{VDD}	3,8,9,14	Analog supply (1.8-V)
A_{GND}	4,7,10,13	Analog ground (0-V)
D_{VDD}	30	Digital supply (1.8-V)
D_{GND}	29	Digital ground (0-V)
$\pm V_{IN}$	5,6	Analog input
$D_{OUT,0-3}$	19,20,23,24,25-28	LVDS digital output
$\pm CK$	21,22	LVDS clock input
Q_{VDD}	2	Quiet analog supply for guard rings (1.8-V)
Q_{GND}	1	Quiet analog ground for guard rings (0-V)
RST	18	Reset
I_{BIAS}	17	Bias current (240-μA)
V_{RP}	11	Shifted, positive reference
V_{RN}	12	Shifted, negative reference
V_{CM1}	16	Shifted, analog common-mode ground
V_{CM2}	15	Analog common-mode output (0.9-V)

Chapter 8

Prototype Characterization

This chapter explains how the prototype is characterized and report on the measured performance results. A total of 80 bare die samples are provided to the author by the manufacturer, of which 20 samples are packaged. Figure 8.1 shows the die micrograph of one of the samples. Every packaged sample is tested in a high-speed test socket. No defective samples are found, and all 20 samples demonstrated similar performance. However, three samples are subsequently damaged during solder rework, and one sample is lost in the laboratory. A revision of the original printed circuit board (PCB) improved the prototype's SNDR performance from 70.2-dB to 75.1-dB. However, before the samples are tested on the new PCB, the high-speed socket is unfortunately damaged[1]. The author cannot replace the socket as it is too costly. Therefore, a sample is chosen by random and soldered onto the PCB. Results reported here are therefore specific to one sample. However, due to the similar performances observed in the original socketed tests, the author believes the results reported here are representative of all samples. At the end of this chapter, a

---

[1] The author chose to use a socket with elastomer interconnects from Ironwood Electronics: SG-MLF-7006. The socket offered very low pin inductance which is desrible in high-speed circuits. However, the author did not realize the socket cannot be cleaned with rubbing alcohol, and damaged it while doing so.

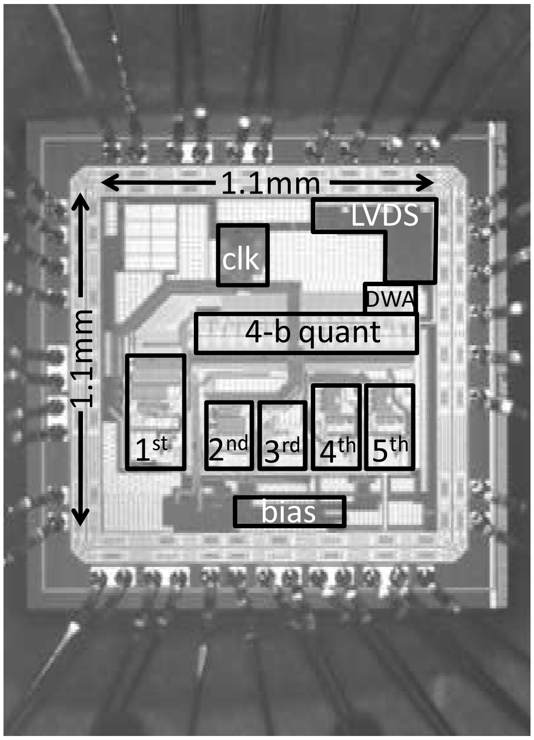

Figure 8.1: Die micrograph.

section is dedicated to the solder reflow process used to construct the PCB for this project.

8.1 Reference buffer adjustment

During transistor-level design, a decision was made to include an optional reference buffer in exchange for 25-dB of power supply rejection. This buffer turned out to be unnecessary because when it is disabled, the modulator's performance appeared to be the same. It is believed that diligent pin assignment, package choice, and die placement, helped minimize impedances to off-chip capacitance that ultimately led to supply rails quiet enough to be used as voltage references. When the buffer is disabled, the reference voltages default to A_{VDD} and A_{GND} and the bias current au-

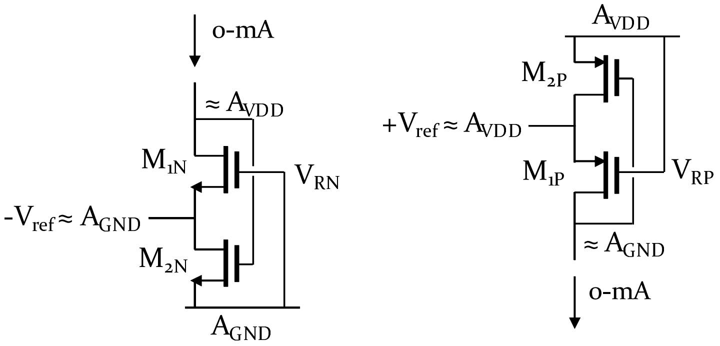

Figure 8.2: Turning off the reference buffer to set $\pm V_{ref}$ equal to the supply rails.

tomatically shuts off. Figure 8.2 shows how the buffer can be disabled by controlling V_{RP} and V_{RN} externally. When V_{RN} is dropped to ground, M_{1N} turns off and the gate of M_{2N} is pulled-up to A_{VDD} by the PMOS current source (not shown). This essentially connects -V_{ref} to A_{GND} through M_{2N}. Simulation results indicate the on resistance of M_{2N} is about 3Ω. Similarly, M_{2P} shorts $+V_{ref}$ and A_{VDD} together and has a slightly higher resistance. By shutting down the reference buffer, the total bias current is reduced by 7.6-mA. There is, however, one set of four bias currents (Figure 6.14) dedicated to the reference buffer that cannot be automatically shut off. Therefore, this bias current is subtracted from the total when the final power dissipation for the modulator is calculated.

8.2 DUT board overview

To be able to characterize the ADC, the test setup must have higher SNR and linearity than the ADC. Otherwise, the ADC will be measuring the test setup instead of the test setup measuring the ADC. The strategy is to take advantage of the available wide power supply rails (±15-V) and generate a large amplitude signal, then use passive (and noiseless) filtering to aggressively clean up the harmonics. Wide power supply rails are needed because passive components attenuate the signal.

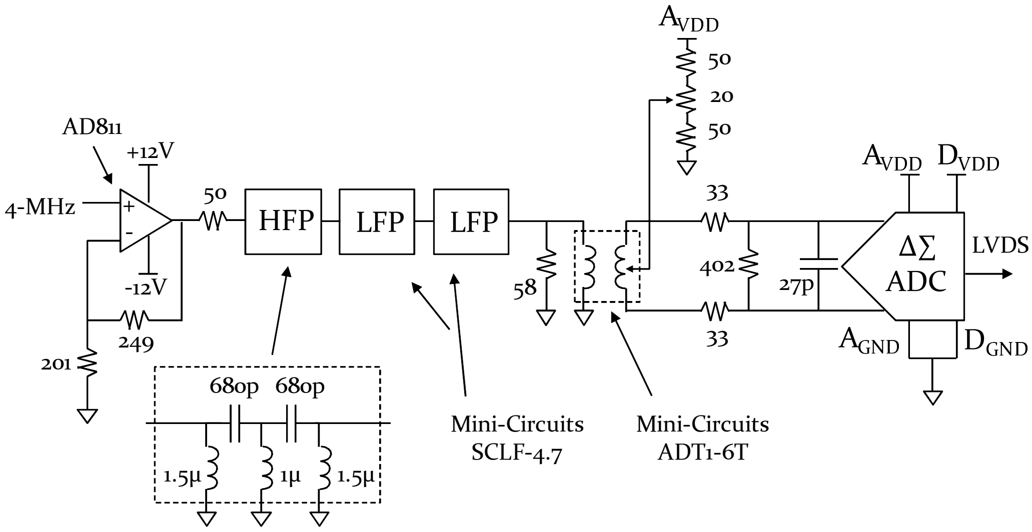

Figure 8.3: DUT board analog front-end.

Multiple stages of filtering can easily attenuate the signal by 50%. Shown in Figure 8.3 is the analog front-end of the device under test (DUT) board.

A 4.03-MHz signal is generated from a custom-built crystal oscillator circuit with an output swing of about ±7-V. This signal frequency is chosen because it is the highest frequency crystal oscillator the author can find that places the third harmonic within the 12.5-MHz passband. The Analog Devices AD811 operational amplifier is chosen to drive the ADC for its combination of low-noise, high slew-rate, wide bandwidth, and high-voltage operation. The output of the amplifier is 5^{th}-order high-pass filtered to remove 1/f noise, then low-pass filtered by two 7^{th}-order passive filters to remove harmonics. Finally, it is converted to differential-mode by a transformer and sampled by the ADC. Proper termination at the input of the ADC is required to achieve high-performance. The author used concepts from various application notes and article discussions to design components for termination, and the reader is referred to the sources [48, 49, 50, 51, 52] for more information.

The digital back-end of the DUT board involves high-speed digital data ac-

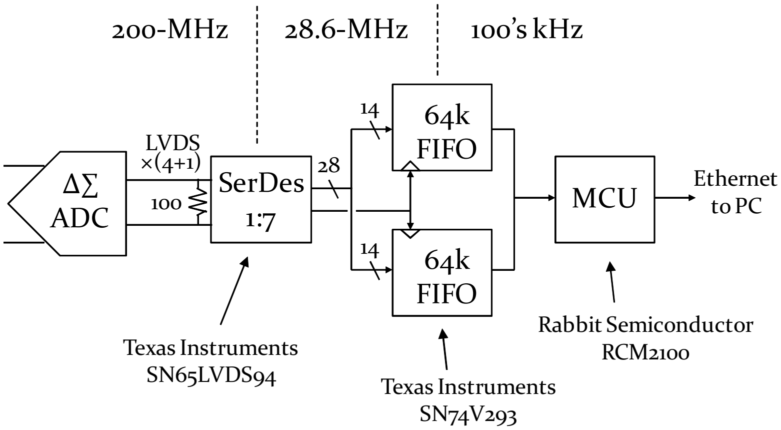

Figure 8.4: DUT board digital back-end.

quisition at 200-MS/s. With no equipment available to the author to collect data at that speed, serial-to-parallel conversion is employed to slow down the rate by a factor of 7. Figure 8.4 shows the digital section of the DUT board. Using two 18-b wide FIFO memories, the 28-b output of the deserializer, running at 28.7-MS/s, can be faithfully recorded. The FIFO memories store up to 64-k samples at 7 ADC outputs per sample. This results in a memory depth of 448-k ADC samples. When the FIFOs fill up, the microcontroller is woken up from sleep mode to transfer the data to a computer via Ethernet. A MATLAB program runs on the computer in parallel to collect the data. It calculates the SNR, SNDR, HD_2, and HD_3 and plots the magnitude spectrum. The microcontroller, after transferring all the data, resets the DUT board and repeats the process. The approximate time for one update on the computer is about 15 seconds, of which most of the time is spent transferring data to the computer.

8.3 Test measurement results

During transistor-level design, the ADC is simulated at different process corners and temperatures to ensure robustness. This has significantly increased the power consumption unnecessarily for operation under nominal conditions. In a production ADC, the bias current can be scaled with respect to temperature using a proportional to absolute temperature (PTAT) reference circuit [53]. For this reason, in the results that follow, the data is taken with the master bias current reduced by 18%. This means that all of the static currents on the chip are scaled down by the same percentage. This resulted in a measured power consumption of 89-mW, with 73.4-mW attributed to analog circuits and 15.8-mW attributed to digital circuits. It is important to note, however, that only the static power consumption changes. The dynamic power consumption, such as the reference switching current, the clock buffers, etc. remains the same.

At room temperature, the prototype reaches its peak SNR and SNDR of 75.3-dB and 75.1-dB, respectively, at full-scale input. Figure 8.5 shows the measured magnitude spectrum of a 448-K sample window. The HD_2 and HD_3 are at -91.5-dBc and -94.2-dBc, respectively. With the references set equal to the supplies, the full-scale input amplitude is about 10% above the supply voltage at around 2-V (4-V differential swing). This is a bit too high in a production environment. However, the size of the input sampling capacitor can be increased to increase the gain so that the input voltage is limited to 1.8-V (3.6-V differential swing). When the supplies are varied by about 5% i.e., at 1.7-V and 1.9-V, the performance stays relatively constant. Table 8.1 shows the measured performance data taken at room temperature for a 4.03-MHz full-scale tone relative to the supply voltage. The modulator is also tested for jitter sensitivity by increasing the input frequency to 9.80-MHz while keeping the input amplitude constant. The amplitude spectrum is plotted in Figure 8.6 and shows no sign of performance degradation at 75.3-dB SNDR. In a jitter-limited converter, as the input amplitude or the input frequency increases, the noise floor rises [24], causing a loss in dynamic range. None of which is observed here.

Table 8.1: Power supply range

	SNR	SNDR	HD_2	HD_3
1.7-V	74.4-dB	74.1-dB	-91.2-dBc	-89.2-dBc
1.8-V	75.3-dB	75.1-dB	-91.5-dBc	-94.2-dBc
1.9-V	75.4-dB	75.3-dB	-93.0-dBc	-96.5-dBc

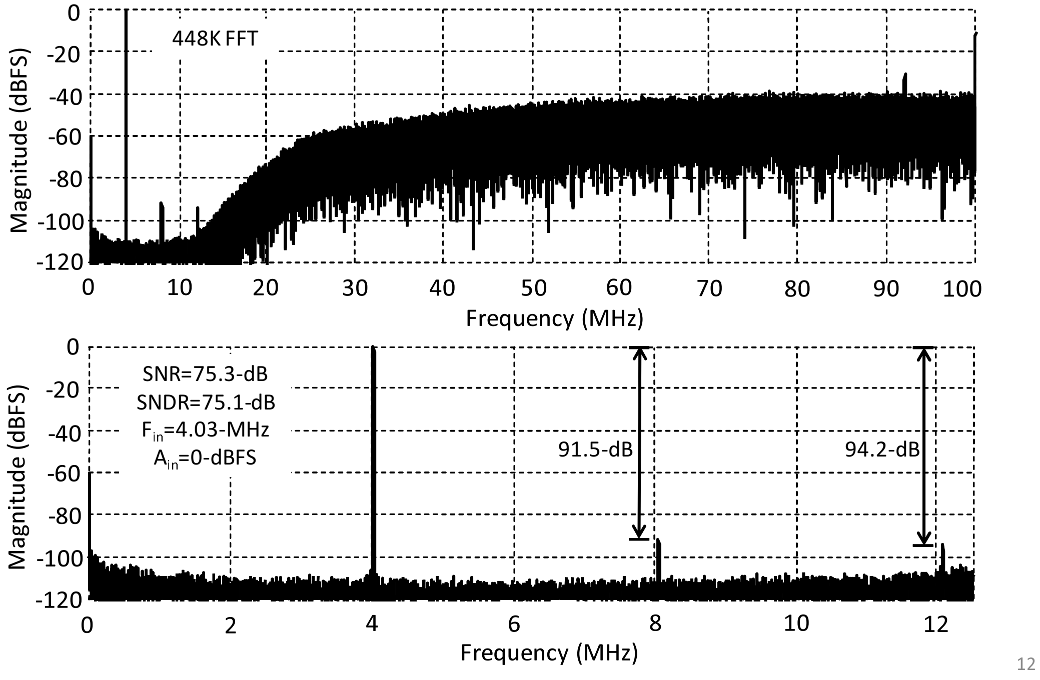

Figure 8.5: Measured spectrum (full and close-in views).

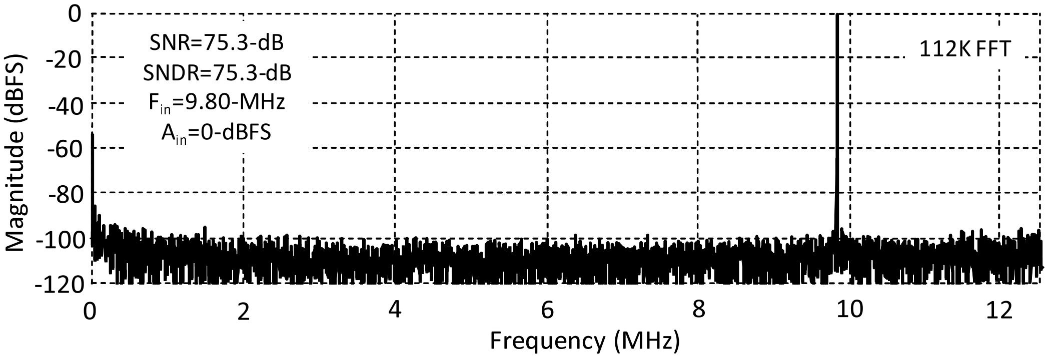

Figure 8.6: Measured spectrum to test for jitter sensitivity.

Besides testing the ADC at full-scale, it is also tested for amplitudes down to -75-dBFS where the SNR is 0-dB. Such small inputs are generated with the RACAL-DANA 9087 RF signal generator. The impact of distortion and phase noise both decrease rapidly as the input amplitude falls. Therefore, a signal generator can take the place of the crystal oscillator circuit when the amplitude is low for more flexibility without compromising test integrity. The results[2] are plotted in Figure 8.7, which demonstrates a dB per dB decrease in SNR and SNDR as the input amplitude decreases.

The breakdown of the power consumption of various circuit blocks is shown in Figure 8.8. The data is taken by measuring across three current sense resistors on the DUT board, one for A_{VDD}, one for D_{VDD}, and one for the master bias current. Four current contributions are subtracted off the measurements to obtain the final power consumption. These are: (1) 21.8-mA of bias current for the 5-channel LVDS transmitter, (2) 1-mA of mirror current for the 5-channel LVDS transmitter, (3) 0.5-mA of dynamic current for the 5-channel LVDS transmitter, and (4) one idle bias current for the dormant reference buffer. The analog and digital dynamic power consumptions are estimated based on the static consumption of on each supply.

---

[2] The 0-dBFS point is not measured with the RACAL-DANA 9087, but rather with the custom crystal oscillator circuit.

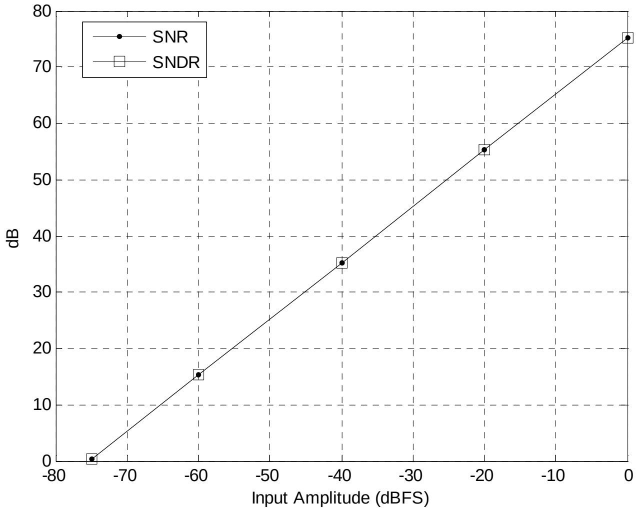

Figure 8.7: Measured SNR and SNDR vs input amplitude.

For D_{VDD}, the only static current besides the LVDS transmitters is the LVDS clock amplifier, which is about 1-mA. Dynamic analog power consists of switched-capacitor currents such as the global feedback DAC and the reference inputs of the 4-b quantizer. The effective number of bits (ENOB) can be calculated directly from SNDR using the following definition:

$$ENOB = \frac{SNDR(dB) - 1.76dB}{6.02dB} \tag{8.1}$$

With 75.1-dB SNDR, the prototype's ENOB is 12.2-b. A common figure-of-merit (FOM) for ADCs is defined as

$$FOM = \frac{Power}{2 \times 2^{ENOB} \times BW}, \tag{8.2}$$

where BW represents the signal bandwidth. The denominator represents performance, which is the product of ENOB in absolute scale and bandwidth. Naturally, since power is in the numerator and performance is in the denominator, a good FOM

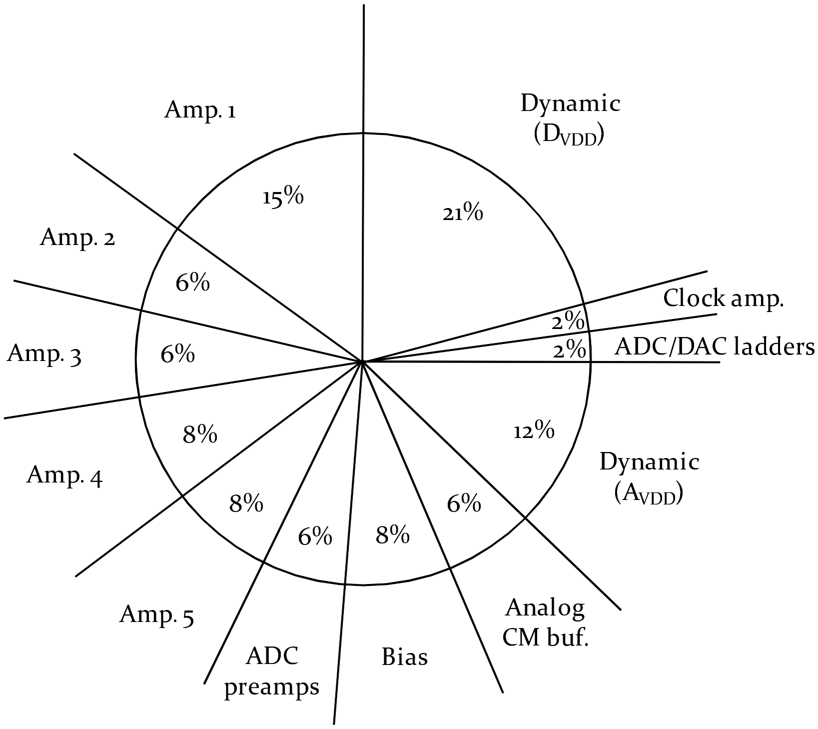

Figure 8.8: Power consumption breakdown of prototype modulator.

in the case is a small FOM. The FOM of this prototype is 0.77-pJ/conversion, which ranks among the best in all IEEE-published switched-capacitor $\Delta\Sigma$ modulators to date. Table 8.2 summarizes the results. Figure 8.9 from Chapter 1 is repeated below, where it compares this modulator's performance, defined here as $2 \times 2^{ENOB} \times BW$, with other IEEE-published discrete and continuous-time (DT and CT) modulators with at least 1-MHz of bandwidth. To the author's best knowledge, this prototype is the highest-performing low-pass DT $\Delta\Sigma$ modulator reported in IEEE literature at the time of this writing.

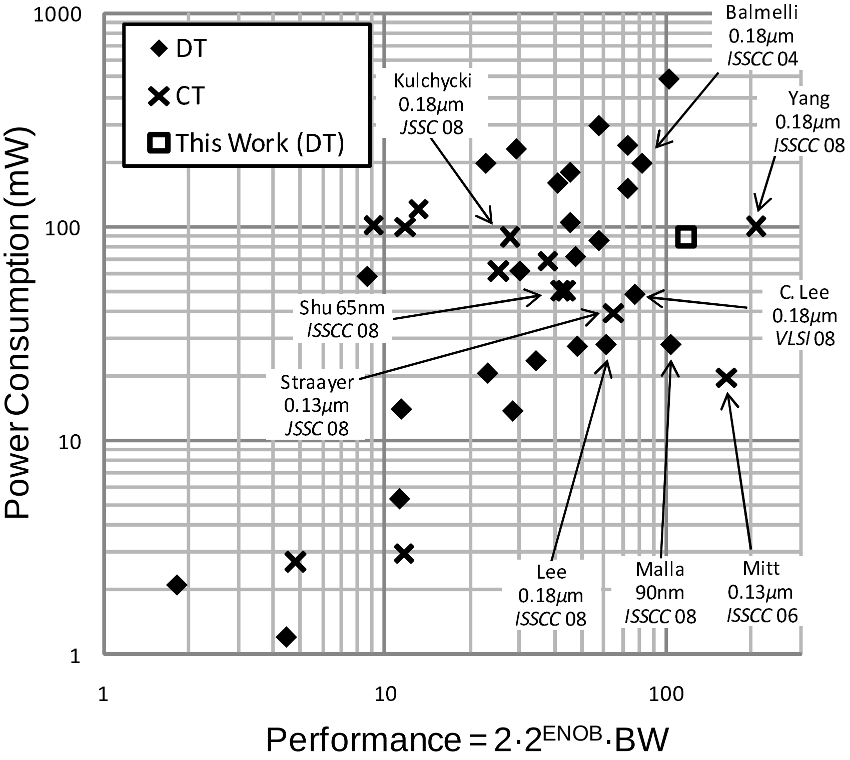

Figure 8.9: Performance comparison with IEEE-published DT and CT ΔΣ modulators.

Table 8.2: Measured performance

Conversion rate	25-MS/s
Sampling frequency	200-MS/s
Configuration	5^{th}-order, 8×OSR, 4-b, DWA
Reference	0-V, 1.8-V
SNR	75.3-dB
SNDR	75.1-dB
ENOB	12.2-b
HD_2, HD_3	-91.5-dBc, -94.2-dBc
Power consumption	89-mW @ 1.8-V
Active area	0.8-mm^2
Technology	0.18-μm 1P6M CMOS
Package	QFN-32
FOM	0.77-pJ/conversion

8.4 PCB construction

The DUT board of this project has over 100 surface mount components on the PCB. This makes it difficult and time-consuming to solder by hand. Furthermore, the modulator is packaged in a QFN package where the leads on the sidewalls are difficult to solder with an iron. Both of these reasons have forced the author to search for a more industrial method to construct the DUT board. Due to cost reasons, the tools must also be economical. Through trial-and-error and input from veteran technicians[3] at the university, a low-cost solder-reflow process with reasonably good results is developed in the laboratory.

---

[3] Daryl Goodnight and Paul Landers

8.4.1 Reflow process

Using a stencil, some solder paste, a squeegee, and a toaster oven, a PCB can be populated with surface mount components and manufactured in about 3-4 hours. The stencil is a piece of thin material with void patterns that match the surface mount landing pads of the PCB. The squeegee is used to apply the solder paste onto the PCB with the stencil sandwiched in between. After application, the stencil can be slowly peeled off, revealing a PCB with solder paste applied to surface mount landing pads. The parts can then placed on the PCB. Setting the toaster oven to the maximum temperature, the PCB is heated up in the oven, without preheating, until the surface temperature of the PCB reaches 230 degrees C. This is checked via an infrared temperature sensor. The oven is then turned off and let to vent slightly by opening the oven door. After cooling, the PCB is checked for shorts and bridges under the microscope. The author has built five PCBs this way and have an average of 4-5 shorts or bridges, which take 15-20 minutes to fix with solder wick and flux.

8.4.2 Equipment and tools for solder reflow

The stencil can be manufactured at an arts supply store equipped with a laser cutter. The author prefers stencils to be made out of 0.003” Mylar material. Thinner stencils can prevent shorts, but risk open circuits. Thicker stencils risk solder bridges. When applying solder paste or placing parts on the PCB, slight misalignments can be tolerated because during solder reflow in the oven, surface tension helps pull the parts back into place. The author used Kester’s KE1507-ND no-clean solder paste and a *convection* toaster oven for even heating across the PCB. The finished PCB is shown in Figure 8.10, and a labeled version is shown in Figure 8.11.

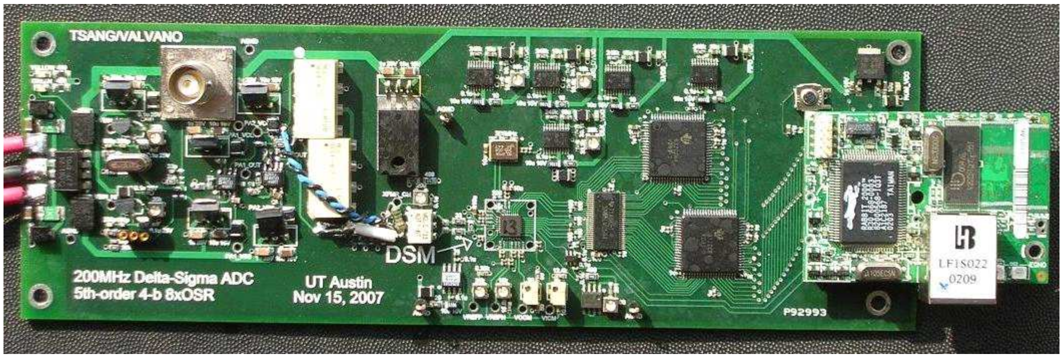

Figure 8.10: DUT board.

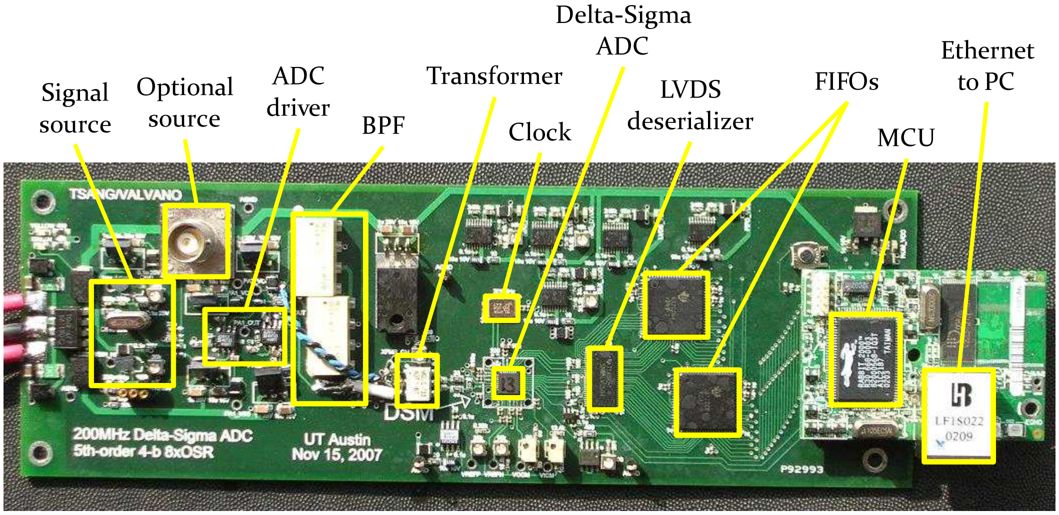

Figure 8.11: DUT board.

Chapter 9

Discussion

9.1 Target SNDR vs. measured SNDR

The original target SNDR of the modulator was 78-dB but the measured SNDR is only 75.1-dB. However, the discrepancy is actually larger than 3-dB because the 78-dB target was designed for reference voltages at 200-mV and 1.6-V. The measured results were taken with the reference voltages equal to the supply rails. This indicates a discrepancy closer to 5-dB. After investigation, it was discovered[1] that the resistance at the gate of the amplifier likely caused the amplifier to be much noisier than predicted. During simulation, the author failed to look at the noise contribution of the amplifier on the integrating capacitor during charge-transfer. This is depicted in Figure 9.1, where a noise measurement is being taken across the sampling capacitor C_{s1} to predict the noise injected into C_i. The resistors in series with C_{s1} represent switch resistance during charge-transfer.

If the amplifier is noiseless, the measurement at V_n should report a noise power ($\overline{V_n^2}$) equal to $2 \cdot \frac{kT}{C_{s1}}$. However, with the amplifier contributing excess noise, the measurement will report a value greater than $2 \cdot \frac{kT}{C_{s1}}$. This is the noise that is

---

[1] The author thanks Professor Eric Swason for pointing the author in the right direction.

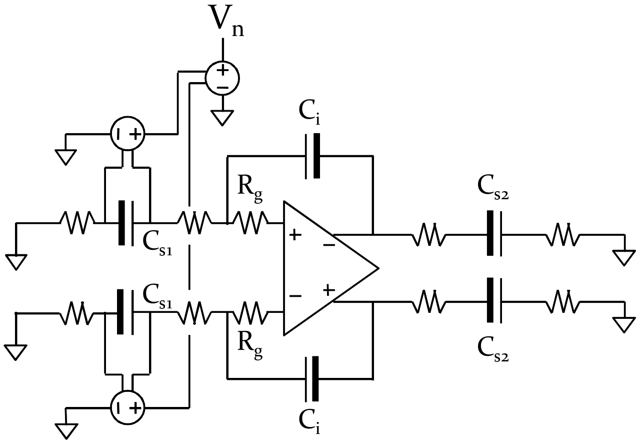

Figure 9.1: Measuring aliased amplifier noise.

sampled onto the integrating capacitor as the charge transfer switch opens. Post-fabrication simulation shows that if R_g is zero, the additional noise on C_{s1} cannot cause a 5-dB loss in SNDR. However, as R_g increases to about 50-Ω, the SNR can drop by 3-dB. Higher resistance further drops the SNR. During transistor-level simulation, because the noise on C_{s1} has never been viewed this way, the modulator's sensitivity towards R_g was thought to be insignificant and layout choices were made based on that fact to optimize other less critical signals. With this knowledge, future revisions or integrator designs should try to minimize the distance of the interconnect to the input node of the amplifier.

Chapter 10

Conclusion

10.1 Summary

At the advent of emerging wireless standards such as WiMax and mobile television that seek ever increasing bandwidths with stringent linearity requirements, new A/D conversion techniques that are power conscious need to be developed. Of particular interest are switched-capacitor $\Delta\Sigma$ modulator based A/D converters because they can achieve high resolution and linearity under limited power supply voltages, and are robust from a manufacturing standpoint with excellent yield and performance predictability. However, due to the oversampling nature of $\Delta\Sigma$ modulation, it is difficult to extend the signal bandwidth beyond a few MHz without a significant compromise in resolution. In this work, a new loop-filter that allows one to maximize bandwidth while preserving a comfortable SQNR margin at 13-b ENOB level is introduced. The new loop-filter's most unique feature is that it allows the placement of one NTF zero-pair on the unit-circle without resorting the non-delay integrator stages. This is significant because at low OSRs, zeros that are not on the unit-circle have difficulty pinning down the quantization noise spectrum within the passband. For example, the conventional CIFF topology that also strictly uses delaying integrators but with zeros spread along z=1, can only provide an SQNR of 81.5-dB at 8× OSR and 4-b quantization. This modulator, on the other hand, provides 86.5-dB of SQNR, and enjoys an 5-dB margin.

With all integrators having a z^{-1} delay associated with it, the entire modulator can be double-sampled in a straightforward manner. Implemented in 0.18-μm CMOS technology as a prototype, the new loop-filter taking advantage of double-sampling, achieved an SNDR of 75.1-dB in a 12.5-MHz signal band while consuming 89-mW from a 1.8-V power supply. This results in a 0.77-pJ/conversion figure-of-merit, and ranks among the best reported in IEEE literature in terms of efficiency. Furthermore, because of the almost-double settling-time afforded to the amplifiers compared to a single-sampled modulator, linearity is enhanced, and the modulator achieves HD_2 and HD_3 performances equal to -91.5-dBc and -94.2-dBc, respectively. Using $2 \cdot 2^{ENOB}$·Bandwidth as the performance metric, this modulator outperforms all previously published switched-capacitor $\Delta\Sigma$ modulators in IEEE literature at the time of this writing, and is also the first switched-capacitor $\Delta\Sigma$ modulator to report an ENOB $>$ 12-b and a bandwidth $>$ 10-MHz simultaneously.

In summary, switched-capacitor $\Delta\Sigma$ modulators are excellent candidates for broadband applications if double-sampling is exploited to increase bandwidth and linearity, and attention is paid to minimizing quantization noise in the passband through optimized placement of NTF zeros.

10.2 Suggestions for future work

The main drawback of the proposed loop-filter is the fact that it is a feedforward modulator and the STF and NTF are tightly coupled at high frequencies. Other feedforward topologies such as CIFF and CRFF [20] also suffer from a similar predicament. As one attempts to push more in-band quantization noise out-of-band with more aggressive noise-shaping, the STF's out-of-band gain grows proportionately with the NTF. In communications systems, nearby channels can be gained up in magnitude and can drive the modulator unstable if these signals are not attenuated sufficiently. Simulations suggest that to guarantee stable operation under full-scale excitation by out-of-band signals, a 3^{rd}-order low-pass filter with a 0.1-dB ripple Chebyshev I response is adequate. Fortunately, this filter usually comes free because the anti-aliasing filter of similar order or higher is usually already in place for suppressing signals that alias back to the passband. Nonetheless, a more relaxed out-of-band signal sensitivity is always welcomed.

Another drawback of the proposed loop-filter topology is its low feedback factor associated with the 4^{th} and 5^{th} integrators. If the coefficients feeding into the input of either of these stages can be reduced or eliminated, the feedback factor will increase and the amplifier's gain-bandwidth product can be relaxed, leading to lower power consumption and possibly higher frequency of operation. Compared to traditional loop-filters such as CIFF where successive amplifier stages can be scaled down aggressively in size and power [4], this loop-filer topology does not allow one to do so as freely.

Bibliography

[1] G. Mitteregger *et al.*, "A 20-mW 640-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 20-MHz signal bandwidth, 80dB dynamic range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641-2649, Dec. 2006.

[2] W. Yang, *et al.*, "A 100mW 10MHz-BW CT $\Delta\Sigma$ modulator with 87dB DR and -91dBc IMD," *IEEE ISSCC Dig. Tech. Papers*, pp. 498-499, Feb. 2008.

[3] P. Malla, H. Lakdawala, K. Kornegay, and K. Soumyanath, "A 28mW spectrum-sensing reconfigurable 20MHz 72dB-SNR 70-dB SNDR DT $\Delta\Sigma$ ADC for 802.11n/WiMax receivers," *IEEE ISSCC Dig. Tech. Papers*, pp. 496-497, Feb. 2008.

[4] P. Balmelli, "Broadband Sigma-Delta A/D converters," *Ph.D. Dissertation*, Swiss Federal Institute of Technology, 2004.

[5] D. Senderowicz, *et al.*, "Low-voltage double-sampled $\Sigma\Delta$ converters," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1907-1919, Dec. 1997.

[6] K. Vleugels, "Broadband oversampling analog-to-digital conversion for digital communications," *Ph.D. Dissertation*, Stanford University, 2001.

[7] P. Rombouts, J. Maeyer, and L. Weyten, "Design of double-sampling $\Sigma\Delta$ modulation A/D converters with bilinear integrators," *IEEE Trans. Circuits and Systems I*, vol. 52, no. 4, pp. 715-722, Apr. 2005.

[8] M. Chen, J. Silva-Martinez, M. Nix, and M. E. Robinson, “Low-voltage low-power LVDS drivers,” *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 472-479, Feb. 2005.

[9] R. Schreier, *The Sigma-Delta Toolbox, Delsig Matlab Toolbox*, Version 7.1 ed., 2004.

[10] R. Jiang, ”Design of a 1.8-V 14-bit $\Delta - \Sigma$ A/D converter with 8× oversampling and 4-MHz Nyquist output rate,” *Ph.D. Dissertation* Oregon State University, 2001.

[11] L. J. Breems, R. Rutten, and G. Wetzker, “A cascaded continuous-time ΣΔ modulator with 67-dB dynamic range in 10-MHz bandwidth,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2152-2160, Dec. 2004.

[12] S. Paton, A. D. Giandomenico, L. Hernandez, A. Wiesbauer, T. Potscher, and M. Clara, “A 70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11 bits of resolution,” *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056-1063, Jul. 2004.

[13] L. Dorrer, F. Kuttner, P. Greco, P. Torta, and T. Hartig, “A 3-mW 74-dB SNR 2-MHz continuous-time Delta-Sigma ADC with a tracking ADC quantizer in 0.13-μm CMOS,” *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2416-2427, Dec. 2005.

[14] Z. Li and T. S. Fiez, “A 14 bit continuous-time Delta-Sigma A/D modulator with 2.5 MHz signal bandwidth,” *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1873-1883, Sep. 2007.

[15] S. Yan and E. Sanchez-Sinencio, “A continuous-time ΣDelta modulator with 88-dB dynamic range and 1.1-MHz signal bandwdith,” *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 75-86, Jan. 2004.

[16] T. C. Caldwell and D. A. Johns, “A time-interleaved continuous-time $\Sigma\Delta$ modulator with 20-MHz signal bandwidth,” *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1578-1588, Jul. 2006.

[17] E. Swanson, N. Sooch, and D. Knapp, “Method for reducing effects of electrical noise in an analog-to-digital converter”, U.S. Patent 4746899, 1988.

[18] N. Sooch, “Gain scaling of oversampled analog-to-digital converters”, U.S. Patent 4851841, 1989.

[19] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, “Experimental resuls and modeling techniques for substrate noise in mixed-signal integrated circuits,” *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 420-430, Apr. 1993.

[20] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, New York, NY: Wiley IEEE Press, 2004.

[21] J. G. Kenny and L. R. Carley, “Design of multibit noise-shaping data converters,” Boston, MA: Kluwer Academic Publishers, Analog Integrated Circuits and Signal Processing, pp. 259-272, 1993.

[22] R. T. Baird and T. S. Fiez, “Improved $\Delta\Sigma$ DAC linearity using data weighted averaging,” *IEEE Trans. Circuits and Sys. II*, vol. 42, no. 12, pp. 753-762, Dec., 1995.

[23] Eric Swanson, *private communication*, 2008.

[24] Eric Swanson, *Mixed-signal systems design and analysis*, The University of Texas at Austin, course notes, Fall 2003.

[25] T. V. Burmas, K. C. Dyer, P. J. Hurst, and S. H. Lewis, “A second-order double-sampled delta-sigma modulator using additive-error switching ,” *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 284-293, Mar. 1996.

[26] Doug Holberg, *private communication*, 2008.

[27] B. Razavi, *Data Conversion System Design*, New York, NY: Wiley-IEEE Press, 1995.

[28] R. K. Hester, *et al.*, "Fully differential ADC with rail-to-rail common-mode range and nonlinear capacitor compensation," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 173-183, Feb. 1990.

[29] Eric Swanson, Nav Sooch, and Dave Knapp, "Method for reducing effects of electrical noise in an analog-to-digital converter," U.S. Patent 4746899, 1988.

[30] A. M. Abo, "Design for reliability of low-voltage, switched-capacitor circuits," *Ph.D. Dissertation*, The University of California, Berkeley, 1999.

[31] J. Silva, *et al.*, "Wideband low-distortion delta-sigma ADC topology," *Electron. Letters*, vol. 37, pp. 737738, Jun. 2001.

[32] K. Martin and A. Sedra, "Strays-insensitive switched-capacitor filters based on bilinear Z-transform," *Electron. Letters*, vol. 15, pp. 365-366, Jun. 1979.

[33] K. Bult and G. Geelen, "A fast-settling CMOS opamp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379-1384, Dec. 1990.

[34] K. Nam, "Design of low-voltage low-power Sigma-Delta modulators for broadband high-resolution A/D conversion," *Ph.D. Dissertation*, Stanford University, 2005.

[35] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, New Yok, NY: John Wiley & Sons, 1997.

[36] O. Choksi and L. R. Carley, “Analysis of switched-capacitor common-mode feedback circuit,” *IEEE Trans. Circuits and Systems I*, vol. 50, no. 12, pp. 906-917, Dec. 2003.

[37] K. Kattmann and J. Barrow, “A technique for reducing differential nonlinearity errors in flash A/D converters,” *IEEE ISSCC Dig. Tech. Papers*, pp. 170171, Feb. 1991.

[38] K. Bult and A. Buchwald, “An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 18871895, Dec. 1997.

[39] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design - 2nd-Edition*, Oxford University Press, New York, NY, 2002.

[40] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, “Matching properties of MOS transistors,” *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433-1440, Oct. 1989.

[41] S. Limotyrakis, “Power-efficient broadband A/D conversion,” *Ph.D. Dissertation*, Stanford University, 2004.

[42] A. Yukawa, “A CMOS 8-bit high-speed A/D converter IC,” *IEEE J. Solid-State Circuits*, vol. 20, no. 3, pp. 775-779, Jun. 1985.

[43] T. B. Cho, “Low-power low-voltage analog-to-digital conversion techniques using pipelined architectures,” *Ph.D. Dissertation*, University of California, Berkeley, 1995.

[44] P. R. Kinget, “Device mismatch and tradeoffs in the design of analog circuits,” *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1212-1224, Jun. 2005.

[45] H. Pan, “A 3.3-V 12-b 50-MS/s A/D converter in 0.6-μm CMOS with 80-dB SFDR,” *Ph.D. Dissertation*, University of California, Los Angeles, 1999.

[46] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits - 2^{nd} – Edition*, New York, NY: John Wiley & Sons, 2002.

[47] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, “Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits,” *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 420-430, Apr. 1993.

[48] R. Reeder and R. Ramachandran, “Wideband A/D converter front-end design considerations: When to use a double transformer configuration,” Analog Devices, Analog Dialogue 40-07, Jul. 2006.

[49] R. Reeder and J. Caserta, “Wideband A/D converter front-end design considerations: When to use a double transformer configuration,” Analog Devices, Analog Dialogue 40-07, Jul. 2006.

[50] R. Reeder, “Transformer-coupled front-end for wideband A/D converters,” Analog Devices, Analog Dialogue 39-04, Apr. 2005.

[51] R. Reeder, “A resonant approach to interfacing amplifiers to switched-capacitor ADCs,” Analog Devices, Application Note AN-935.

[52] E. Newman and R. Reeder, “A resonant approach to interfacing amplifiers to switched-capacitor ADCs,” Analog Devices, Application Note AN-827.

[53] B. Razavi, *Design of analog CMOS integrated circuits*, New York, NY: McGraw Hill, 2001.

[54] S. Paton, *et al.*, “A 70-mW 300-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 15-MHz bandwidth and 11 bits of resolution,” *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056-1063, Jul. 2004.

[55] L. J. Breems, R. Rutten, and G. Wetzker, "A cascaded continuous-time $\Sigma\Delta$ modulator with 67-dB dynamic range in 10-MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2152-2160, Dec. 2004.

[56] L. Dörrer, *et al.*, "A 3-mW 74-dB SNR 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2416-2427, Dec. 2005.

[57] A. Bosi, A. Panigada, G. Cesura, and R. Castello, "An 80MHz 4× oversampled cascaded $\Delta\Sigma$-pipelined ADC with 75dB DR and 87dB SFDR," *IEEE ISSCC Dig. Tech. Papers*, pp. 174175, Feb. 2005.

[58] T. Song, Z. Cao, and S. Yan, "A 2.7-mW 2-MHz continuous-time $\Sigma\Delta$ modulator with a hybrid active-passive loop filter," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 330-341, Feb. 2008.

[59] Y-S. Shu, B-S. Song, and K. Bacrania, "A 65nm CMOS CT $\Delta\Sigma$ modulator with 81dB DR and 8MHz BW auto-tuned by pulse injection," *IEEE ISSCC Dig. Tech. Papers*, pp. 500-501, Feb. 2008.

[60] A. M. Marques, V. Peluso, M. S. J. Steyaert, and W. Sansen, "A 15-b resolution 2-MHz Nyquist rate $\Delta\Sigma$ ADC in a 1-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1065-1075, Jul. 1998.

[61] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 3.3-V, 15-bit, delta-sigma ADC with a signal bandwidth of 1.1 MHz for ADSL applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 927-936, Jul. 1999.

[62] I. Fujimori, *et al.*, "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8× oversampling ratio," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820-1828, Dec. 2000.

[63] Y. Geerts, M. S. J. Steyaert, and W. Sansen, "A high-performance multibit $\Delta\Sigma$ CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829-1840, Dec. 2000.

[64] S. K. Gupta and V. Fong, "A 64-MHz clock-rate $\Sigma\Delta$ ADC with 88-dB SNDR and -105-dB IM3 distortion at a 1.5-MHz signal frequency," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1653-1661, Dec. 2002.

[65] A. A. Hamoui and K. Martin, "A 1.8-V 3-MS/s 13-bit $\Delta\Sigma$ A/D converter with pseudo data-weighted-averaging in 0.18-μm digital CMOS," *IEEE Custom Integrated Circuits Conf. Proceedings*, pp. 119-122, Sep. 2003.

[66] Y-I. Park, *et al.*, "A 16-bit, 5MHz multi-bit Sigma Delta ADC using adaptively randomized DWA," *IEEE Custom Integrated Circuits Conf. Proceedings*, pp. 115-118, Sep. 2003.

[67] J. Koh, Y. Choi, and G. Gomez, "A 66dB DR 1.2V 1.2mW single-amplifier double-sampling 2^{nd}-order $\Delta\Sigma$ ADC for WCDMA in 90nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 170-171, Feb. 2005.

[68] Y. Jiang and F. Maloberti, "A low-power multi-bit $\Delta\Sigma$ modulator in 90nm digital CMOS without DEM ," *IEEE ISSCC Dig. Tech. Papers*, pp. 168-169, Feb. 2005.

[69] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "An 11-bit 330MHz 8× OSR Σ-Δ modulator for next-generation WLAN," *IEEE VLSI Circuits Dig. Tech. Papers*, pp. 166-167, 2006.

[70] S. Kwon and F. Maloberti, "A 14mW multi-bit $\Delta\Sigma$ modulator with 82dB SNR and 86dB DR for ADSL2+," *IEEE ISSCC Dig. Tech. Papers*, pp. 161-170, Feb. 2006.

[71] K-S. Lee, S. Kwon, and F. Maloberti, “A 5.4mW 2-channel time-interleaved multi-bit $\Delta\Sigma$ modulator with 80dB SNR and 85dB DR for ADSL,” *IEEE ISSCC Dig. Tech. Papers*, pp. 171-180, Feb. 2006.

[72] Z. Cao, T. Song, and S. Yan, “A 14 mW 2.5 MS/s 14 bit $\Sigma\Delta$ modulator using split-path pseudo-differential amplifiers,” *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2169-2179, Oct. 2007.

[73] Y. Kanazawa, Y. Fujimoto, P. L. R*é*, and M. Miyamoto, “A 100-MS/s 4-MHz bandwidth 77.3-dB SNDR $\Delta\Sigma$ ADC with a triple sampling technique,” *IEEE Custom Integrated Circuits Conf. Proceedings*, pp. 53-56, Sep. 2006.

[74] Y. Fujimoto, Y. Kanazawa, P. L. R*é*, and M. Miyamoto, “An 80/100MS/s 76.3/70.1dB SNDR $\Delta\Sigma$ ADC for digital TV receivers,” *IEEE ISSCC Dig. Tech. Papers*, pp. 201-210, Feb. 2006.

[75] T. Christen, T. Burger, and Q. Huang, “A 0.13μm CMOS EDGE/UMTS/WLAN tri-mode $\Delta\Sigma$ ADC with -92dB THD,” *IEEE ISSCC Dig. Tech. Papers*, pp. 240-241, Feb. 2007.

[76] C. Lee and M. Flynn, “A 14b 23MS/s 48mW resetting $\Sigma\Delta$ ADC with 87dB SFDR 11.7b ENOB & 0.5mm^2,” *IEEE VLSI Circuits Dig. Tech. Papers*, 2008.

[77] T-H. Chang, L-R. Dung, J-Y. Guo, and K-J. Yang, “A 2.5-V 14-bit, 180-mW cascaded $\Sigma\Delta$ ADC for ADSL2+ application,” *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2357-2368, Nov. 2007.

Vita

Robin Matthew Tsang was born in Hong Kong on December 24, 1979. He is the eldest son of Patricia and Wilkie Tsang, and brother of Suzanne and Jason. He attended St. Joseph's primary and secondary schools in Hong Kong, and graduated from the Hong Kong International School at age 18. In the fall of 1998, he attended the Electrical and Computer Engineering program at the University of Texas at Austin, and received the Bachelor's and Master's degrees in Electrical Engineering in 2002 and 2004, respectively. Since 2003, he has been a teaching assistant for 11 regular semesters, instructing mostly undergraduate students in the area of microcontroller programming and interfacing. He enjoys teaching and looks forward to one day becoming a professor. Upon graduation of the Doctoral degree, he plans to join Cirrus Logic in Austin, TX, where he will design high-precision mixed-signal data conversion products.

Permanent Address: 30 Tsiu Keng, Pang Uk,
Sheung Shui, N.T.,
Hong Kong

This dissertation was typeset with LaTeX 2_ε[1] by the author.

---

[1] LaTeX 2_ε is an extension of LaTeX. LaTeX is a collection of macros for TeX. TeX is a trademark of the American Mathematical Society. The macros used in formatting this dissertation were written by Dinesh Das, Department of Computer Sciences, The University of Texas at Austin, and extended by Bert Kay, James A. Bednar, and Ayman El-Khashab.