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DEVELOPMENT OF AN INNOVATIVE FABRICATION METHOD FOR n-MOS to p-MOS TUNABLE SINGLE METAL GATE/HIGH-κ INSULATOR DEVICES FOR MULTIPLE THRESHOLD VOLTAGE APPLICATIONS

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by

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Dedication

Deo Optimo Maximo

To my Mother for her love, support, encouragement, and inspiration

To my Ph.D. Committee, The University of Texas at Austin, and SEMATECH for providing me the opportunity to conduct my research

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DEVELOPMENT OF AN INNOVATIVE FABRICATION METHOD FOR n-MOS to p-MOS TUNABLE SINGLE METAL GATE/HIGH-κ INSULATOR DEVICES FOR MULTIPLE THRESHOLD VOLTAGE APPLICATIONS

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Aggressive scaling required to augment device performance has caused conventional electrode materials to approach their physical scaling limits. Alternative metal gate/high dielectric constant (MG/High-κ) stacks have been implemented successfully in commercial devices and hold promise for further scaling based performance advances. Existing MG/High-κ technology does not achieve a single metal n-MOS to p-MOS effective work function (EWF) tuning range suitable for bulk silicon (Si) device applications. Dual metal gates (DMGs) utilizing a separate metal for n-MOS and p-MOS electrodes increases the cost and complexity of fabrication.

The research presented herein introduces a method by which the cost and complexity of MG/High-κ device fabrication may be reduced. Innovative fin field effect

transistors (FinFETs) incorporating 3 dimensional ultra thin body silicon on oxide (3-D UTB-SOI) technology display superior electrical characteristics compared to bulk Si devices at the nanometer (nm) dimension and require only a +/-200meV n-MOS to p-MOS EWF tuning range around the Si mid-gap. Single metals capable of achieving this +/-200meV EWF tuning range have been evaluated herein and the tuning mechanisms investigated and engineered to develop a single MG/High-κ FinFET the fabrication complexity of which is reduced by 40%.

More specifically, the research shows that the metal thickness of titanium nitride/hafnium silicon oxide ($TiN/HfSiO_x$) gate stack may be engineered to achieve an n-MOS (thinner TiN) to p-MOS (thicker TiN) appropriate FinFET EWF tuning range. FinFETs may be fabricated by depositing a single p-MOS appropriate TiN thickness which may be selectively etched back to achieve thinner, n-MOS appropriate films. Similar electrical behavior is exhibited by etched back and as deposited TiN electrode FinFETs. The single metal etch back fabrication method removes many of the additional steps required for DMG fabrication and preserves the integrity of the MG/High-κ interface between n-MOS and p-MOS devices. These advantages result in reduced fabrication complexity and improved reliability and reproducibility.

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET) SCALING: A DEVELOPING CHALLENGE FOR CONVENTIONAL MOSFET TECHNOLOGY

The electronics industry has relied upon scaling to increase computational power and enhance product performance by concentrating more logic devices in a smaller area. G.E. Moore recognized this trend in 1965, noting that improvements in device design and processing result in a 40% performance increase and a doubling in circuit density approximately every two years [1]. Dubbed Moore's Law, this dimension scaling rate has become a central component of the International Technology Roadmap for Semiconductors (ITRS), a tool for technology assessment [2, 3, 4 at p.469].

Conventional materials used in device fabrication are reaching their fundamental scaling limits. Although strain engineering [5-11], innovative geometries [12-15], and novel device structures [3, 13] are being implemented to extend feasibility, conventional materials are not expected to remain viable at dimensions beyond 22nm [2, 3]. Alternative gate stack materials able to enhance performance at existing dimensions and to provide opportunities for future scaling are being investigated to replace the conventional polysilicon gate and silicon dioxide dielectric (poly-Si/SiO_2) electrode stack [3, 16, 17]. Figure 1.1 is a timeline of demonstrated and expected performance advances in devices incorporating conventional as well as alternative materials and device structures.

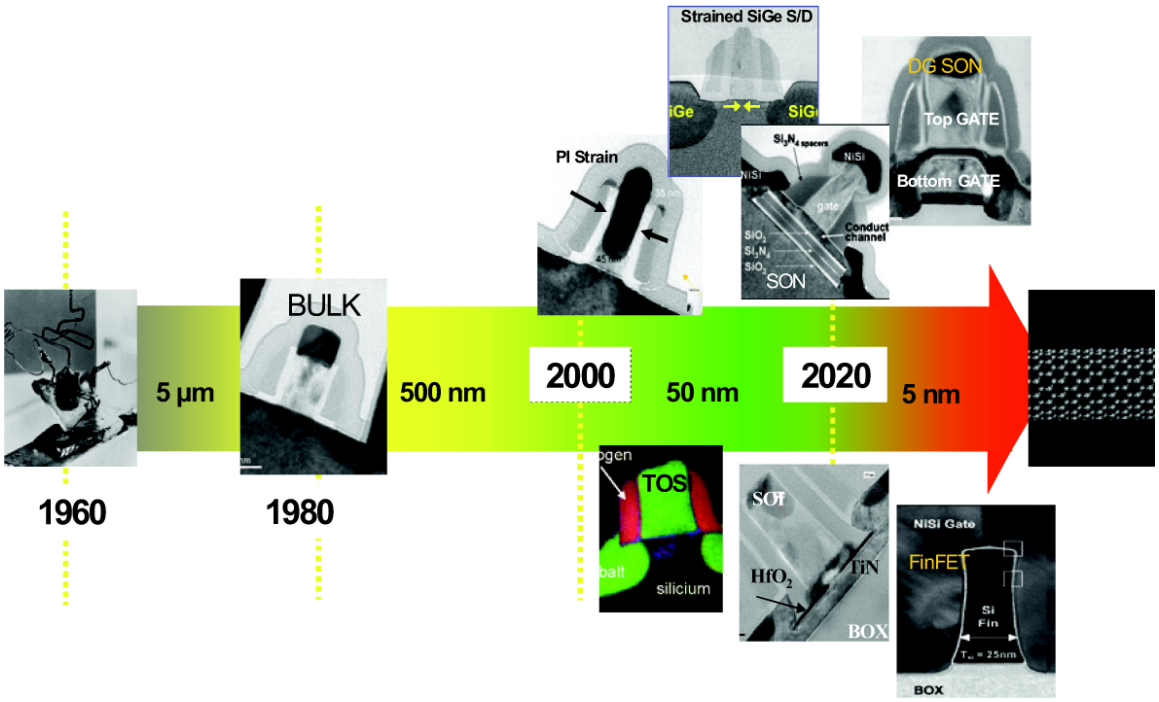


Figure 1.1: Developments in conventional and alternative device materials and structures implemented to maintain expected scaling and performance goals [from 13]

The first metal gate/high-κ dielectric (MG/High-κ) alternative gate stacks were successfully introduced in 2008 and remain central to emerging scaling technology [17, 18]. MG/High-κ gate stacks tend to be costly and complex to fabricate; efforts are proceeding to enhance cost effectiveness and simplicity.

1.1.1 Conventional Device Structures

Figure 1.2 illustrates a conventional planar bulk MOSFET structure consisting of a lightly doped n-type or p-type silicon (Si) substrate and heavily doped source (S) and drain (D) wells. Current flow through a channel volume formed within the first few nanometers of the substrate between S and D may be regulated by applying voltage to a gate electrode fabricated above the channel [4 at p. 438, 19 at p. 257]. The gate electrode includes a metal or metal-like gate material separated from the channel by an insulating dielectric layer which passivates surface states at the dielectric/substrate interface and

establishes a high input impedance. In conventional MOSFETs, the electrode consists of a poly-Si gate separated from the channel by an SiO_2 insulator.

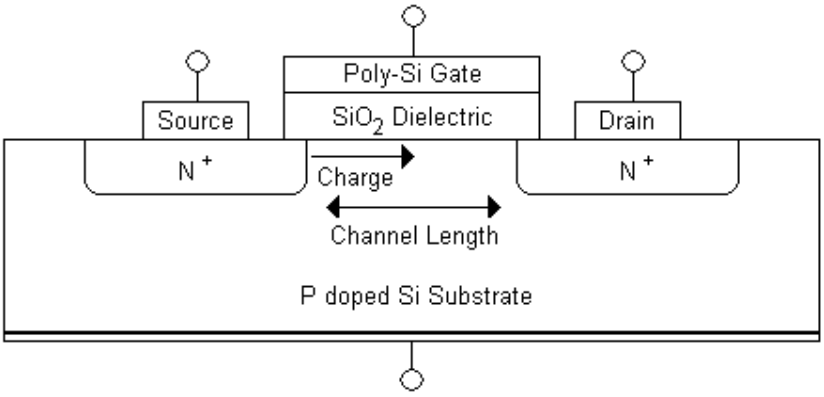


Figure 1.2: Conventional planar MOSFET structure

Channel length is an important scaling parameter affecting threshold voltage (V_{th}) stability, mobility, and drive current [4 at pp. 315 and 469, 19 at p. 313, 20, 21]. At the 45nm dimension and beyond, the dielectric equivalent oxide thickness (EOT) must be less than 1nm in thickness to effectively control the channel and achieve target performance [3, 13, 22]. SiO_2 dielectrics encounter unacceptable gate leakage and reliability issues as the EOT thickness approaches values less than 1nm [13].

1.1.2 Poly-Si gate on SiO_2 Dielectric: Characteristics

Historically, poly-Si/SiO_2 gate stacks have proven exceptionally well suited for MOSFET applications. Among the advantages of SiO_2 dielectrics:

- SiO_2 is an abundant and robust material easily produced at reasonable cost,
- SiO_2 affords excellent thickness control during oxide growth and produces a highly pure film incorporating few trapped charges and defects,
- affinity between SiO_2 and the Si substrate results in an abrupt interface minimizing interface defects and enhancing electrical stability and performance,
- SiO_2 remains amorphous during high temperature processing, evading grain boundary current leakage plaguing crystallized interfaces.

The exemplary characteristics of SiO_2 dielectrics result in outstanding device reliability and performance [3, 24 at p. 149].

During the 1980's, poly-Si replaced aluminium (Al) gates to facilitate the self-aligned S/D technology implemented to ensure gate overlap with the S/D regions [19 at p. 294]. The overlap reduces scaling induced short channel effects (SCEs). Among the advantages of poly-Si:

- poly-Si withstands the high temperature anneals inherent in MOSFET fabrication processes,
- dopant concentration determines poly-Si's metallicity; tight V_{th} control may be easily engineered through gate and/or channel doping even as dimensions scale [19 at p. 433].

Less advantageous poly-Si characteristics include poly-depletion related parasitic series capacitance, high sheet resistance, and Fermi level pinning caused by p-type dopant migration into the dielectric. These effects have begun to severely degrade device performance as increased scaling deteriorates the robustness of the SiO_2 dielectric [3].

1.1.3 Scaling

Scaling channel length enhances transistor drive current and response time by increasing channel control and reducing carrier travel distance, respectively [4 at p. 486]. Dielectric thickness, among other device dimensions, must linearly scale with the channel to maintain constant voltage and electric field effects which ensure appropriate device performance [25]. V_{th}, the minimum gate voltage required to induce channel formation, must be carefully engineered to accommodate power supply margins [19 at p.257].

V_{th} is determined from the flat band voltage (V_{fb}), dielectric capacitance, charge, and channel doping. V_{fb} is the voltage which must be applied to the gate to remove band bending and is related to the difference in work function (WF) potential between the MG and the substrate (Φ_{ms}). Φ_{ms} may be engineered to determine V_{fb}, and thereby control V_{th},

by adjusting the substrate doping, reducing interface charge, or adjusting oxide thickness and/or dielectric constant [3, 19 at p. 272, 26, 27, 28].

Drain current (I_D) is determined by the relationship between channel width (W), channel length (L), channel carrier mobility (μ), gate dielectric capacitance density of the inverted channel (C_{inv}), gate voltage (V_G), drain Voltage (V_D) and V_{th} according to the gradual channel approximation:

$$I_D = \frac{W}{L}\mu C_{inv}\left(V_G - V_{th} - \frac{V_D}{2}\right)V_D \quad (1).$$

The maximum saturation current is determined when VD is equal to VG – Vth:

$$I_{D,sat} = \frac{W}{L}\mu C_{inv}\frac{\left(V_G - V_{th}\right)^2}{2} \quad (2).$$

Reducing channel length and/or increasing capacitance will increase ID. At very short channel lengths, equations (1) and (2) must be adjusted to capture quantum effects [3, 19 at p. 313].

Maintaining a constant voltage with channel scaling requires that C_{OX} also be scaled [4 at p.471, 20, 28]. As the channel length decreases, charge sharing between S, D, and gate causes V_{th} lowering SCEs [19 at p.313]. Concomitant gate oxide scaling increases capacitance and improves gate control of the channel while maintaining V_{th} [3, 13, 29]. The general scaling factor for channel length, channel width, and oxide thickness is approximately .7 per device generation in order to maintain a constant channel resistance [3].

Effective scaling requires balancing interests in high performance with competing interests in power efficiency. Low standby power (LSTP) and low operating power (LOP) devices are less heavily scaled than high performance (HP) devices [30, 23 at p. 45]. Although LSTP and LOP devices are more power efficient and extend battery life,

they have a higher V_{th}, respond more slowly, and are impractical for complex, high-speed applications [3, 30, 23 at p. 45]. Most products, particularly those developed for portable applications, incorporate integrated circuits (ICs) supporting multiple V_{th} which reduce power consumption by activating HP lines only when required [4 at p.486, 19 at p.241, 23 at p. 45]. As dimensions continue to scale, gate leakage and SCEs become a detriment for LOP as well as HP structures [3, 13].

1.1.4 Detrimental Effects on Device Performance of Gate Oxide Scaling in Conventional Poly-Si/SiO_2 Devices

An SiO_2 dielectric 1.5nm thick comprises only 5 atomic layers; at less than 1nm, the SiO_2 dielectric is approximately 3 atomic layers thick [2, 26, 30, 31]. Direct gate tunneling replaces Fowler-Nordheim tunneling (F-Nt) at such narrow SiO_2 thickness; the gate leakage increases exponentially with continued scaling, deleteriously degrading both stand-by power and reliability [16, 32]. The 16nm and 11nm dimension devices the ITRS predicts will be introduced by 2018 and 2022, respectively, are well beyond the capacity of SiO_2 to achieve [2].

As the SiO_2 dielectric thickness scales, the poly-depletion effect in conventional devices increases. A parasitic series capacitance occurs which decreases total gate capacitance, increases both drive current and transconductance (g_m), and impedes dielectric scaling by inducing a thicker EOT [33, 34]. Increased poly-Si doping reduces depletion capacitance; however, there is a doping limit of approximately $10^{21}/cm^{-3}$ beyond which device behavior deteriorates [26]. Boron (B) in p-MOS poly-Si gates more easily migrates through highly scaled SiO_2 into the channel. Increased charge at the SiO_2/substrate interface causes an unintended V_{th} shift and Fermi level pinning [3, 26]. Resultant devices lack reliability and are unable to achieve suitable electrical characteristics.

1.1.5 Resolving the Scaling Dilemma: Adapting Conventional Materials and Introducing Innovative Structures and Materials

Industrial fabrication standards have developed around conventional dielectric stacks. The inherent advantages of these stacks and their central role in existing fabrication technology have spurred research intended to sustain poly-Si and SiO_2 beyond the 32nm dimension [3, 13]. Innovative software engineering, structural design, packing, and materials engineering have all been implemented to achieve equivalent performance improvement and response time without physical scaling [12, 13, 14]. These methods exploit conventional fabrication equipment and methods to limit costs required to otherwise modify or redesign fabrication facilities to accommodate alternative stack materials [13].

Pipelining and parallelism have been implemented to increase data throughput [13]. Logic functions have been designed to implement more efficient, use-specific methods and structures such as carry look ahead, ripple carry, synchronous/asynchronous circuit design, and pass gate/normal gate topologies. Shift register frequency and SRAM layout have also been independently exploited to obtain 45nm performance expectations at 65nm [24 at p.45].

Gate and body bias optimization for LOP and HP interoperation reduce leakage and dynamic power by as much as 90% and 50%, respectfully [35]; stacked transistor layouts are also credited with leakage reduction [36]. Silicon on Insulator (SOI) technology has been introduced to reduce leakage currents by improving gate insulation [3, 37-41]. Multigate FETs (MugFETs) more effectively control channel current and are particularly useful when implemented in 3 dimensional fully depleted SOI (FD-SOI) and partially depleted SOI (PD-SOI) fin field effect transistors (FinFETs) [20, 37, 41-44].

Improvements in response time achieved through scaling have been reproduced utilizing denser wiring, shorter interconnects, and less resistant interconnect metals [13].

Strain engineering has also been developed to enhance mobility by increasing carrier concentration and reducing scattering and resistance within the channel [5, 6, 10]. Response time has been observed to increase by 35% without affecting power consumption in strained Si channels [5].

Channel materials having intrinsic high carrier concentrations are being studied as alternatives to doped Si. Germanium (Ge), the material from which the first transistor and IC were demonstrated, is being reconsidered due to its high carrier concentration and mobility despite integration concerns [3, 13, 45-48]. Silicon Germanium (SiGe) and III-V materials are also promising channel options [13, 49-51].

1.2 ALTERNATIVE: THE METAL GATE/HIGH-κ DIELECTRIC ELECTRODE

Despite the performance advances continuing to be achieved with conventional electrodes, alternative gate stack materials will be necessary to maintain long term scaling. Investigation of High-κ dielectrics capable of producing reliable devices, high yield, and enhanced performance at low power began in the mid-1990's [13, 44]. The first commercially available processors incorporating MG/High-κ were introduced in 2007 for 45nm dimension devices. Similarly fabricated electrodes will be introduced for the 32nm dimension in 2009 [52]. Exhaustive research was required to establish appropriate electrode composition and to understand the materials interactions and WF tuning mechanisms which may be engineered to optimize the electrical behavior observed.

1.2.1 High-κ Development

The relationship between capacitance, physical thickness, and dielectric constant is represented by:

$$C_{OX} = \frac{\varepsilon_0 \kappa}{T_{phys}} \quad (3)$$

In this equation, C_{OX} is the gate capacitance, ε_0 is the vacuum permittivity (a constant equal to 8.85×10^{-12} F/m), κ is the insulator dielectric constant (3.9 for SiO_2), and T_{phys} is the insulator physical thickness. C_{OX} may be increased either by reducing the oxide physical thickness or by increasing the insulator's dielectric constant.

Comparison of the C_{OX} of SiO_2 and alternative dielectrics using (3) results in a relationship providing the advantage achieved under ideal circumstances when a higher κ dielectric is used:

$$t_{eq} = \frac{t_{high-\kappa} \kappa_{OX}}{\kappa_{high-\kappa}} \quad (4)$$

In this formula, t_{eq} is the thickness of the equivalent SiO_2 layer, t_{OX} is the thickness of the SiO_2 layer, κ_{OX} is the dielectric constant of SiO_2 and $\kappa_{high-\kappa}$ is the dielectric constant of the alternative material. High-κ insulators achieve the same EOT for a specific capacitive value at a greater physical thickness than SiO_2 [53]. This greater physical thickness eliminates/reduces gate leakage current and provides the opportunity for further scaling.

The dielectric/substrate and gate/dielectric interfaces must be considered when determining the total capacitance of alternative electrodes [26]. Interface interactions may cause capacitance to vary greatly from that expected for an insulator with abrupt gate and substrate interfaces. If the interface is not abrupt or if migration into or through the dielectric occurs at either interface, the full advantage of the higher κ may be lost [3, 13, 26, 30].

Initially, small increases in dielectric constant between 3.9 and 7 were achieved by incorporating nitrogen (N) into SiO_2 to form oxynitrides such as SiO_xN_y [3, 13, 54]. Binary compounds and ternary oxides are materials of interest capable of achieving even higher κ [3, 55, 56]. High-κ dielectrics incorporating hafnium (Hf), titanium (Ti), tantalum (Ta), strontium (Sr), aluminium (Al), and/or their oxides have a much larger

dielectric constant (between 10 and 80) and are gaining favor as reliable insulator materials [3, 13, 26, 44, 57, 58]. Commercially available processors incorporate Hf based dielectrics [13, 26, 44, 52].

1.2.2 Metal Gate Development

Aluminium gates were replaced with poly-Si in the 1980's because poly-Si is more resilient during high temperature anneals and is conducive to self aligned gate fabrication [59]. The inherent drawbacks poly-Si gates exhibit become deleterious to device performance as the SiO_2 dielectric becomes thinner; refractory metals capable of sustaining high temperature anneals have been investigated to replace poly-Si [3, 33, 60, 61]. Ideally, the gate stack dielectric thickness of an electrode incorporating a MG is solely that of the SiO_2 and less aggressive dielectric scaling is required [3, 13, 26, 55].

Metals investigated as alternative gate materials consist of the following types: elemental metals, metal silicides, bi-metal alloys, conducting metal oxides, binary and ternary metal nitrides, and multi-layer metal stacks [62-66]. Ruthenium (Ru) compounds and conducting metal nitrides such as TiN_x, TaN_x, $TaSi_xN_y$, and $TiSi_xN_y$ are particularly promising MG alternatives [3, 13, 26, 44, 67-71]; however, interactions between SiO_2 and the MGs investigated affect reliability and inhibit performance [3, 26, 27, 28, 44].

1.2.3 Metal Gate/High-κ: Challenges and Advances

Exhaustive investigation of poly-Si/High-κ stacks and MG/SiO_2 stacks indicate that neither arrangement is extraordinarily promising. In addition to the poly-depletion, poly-Si/High-κ gates experience greater, less controllable dopant migration [3, 26, 44, 55]. The poly-Si/High-κ interface is substantial; poor film quality and oxygen defects cause increased gate leakage and hysteresis which degrade performance [3, 27, 28, 31]. V_{th} pinning caused by poly-Si/High-κ interface defects and mobility limiting phonon scattering result in high switching voltages and slow transistor switching speed [27, 31,

72]. MG/SiO_2 stacks exhibit performance degrading silicidation of elemental metals at high temperatures [3, 23, 26]. While advantageous in fully silicided (FUSI) gates, optimization is required to ensure reliability and performance gains [13, 73-75]. Metal/SiO_2 mixing also results in interface effects and stress induced damage to the dielectric detrimental to device performance [60].

MG/High-κ stacks are more compatible than either poly-Si/High-κ or MG/SiO_2 electrodes and have already been incorporated in commercially available IC packages [13, 26, 55]. Materials compatibility and fabrication effects must still be analyzed to achieve optimal performance. Deposition method, materials thickness, stress effects, etch method and materials, anneal conditions, relative materials concentration ratios and various other factors all influence the final gate electrode parameters [3, 61]. For example, the concentration of N in oxynitride improves device characteristics until an optimal concentration is reached; additional N will then degrade performance [3].

Promising High-κ dielectrics should incorporate the following six characteristics [3, 26]:

- Dielectric constant high enough to be reasonably scaled well into the future,
- Thermal stability at the oxide/substrate interface,
- Kinetic stability during high temperature process flows,
- Band offsets greater than 1eV with Si for minimal carrier injection into the band,
- Excellent electrical interface with the substrate,
- Minimal electrically active bulk defects.

Each of these requirements affords its own challenges, requiring analysis and optimization to achieve.

As presented in Figure 1.3, dielectric constant is inversely proportional to band gap [26]. The higher the dielectric constant, the less likely the bandgap to be greater than

the ~1.1eV necessary for compatibility with an Si substrate and the greater the probability SCEs from field induced barrier lowering (FIBL) will occur [76-81].

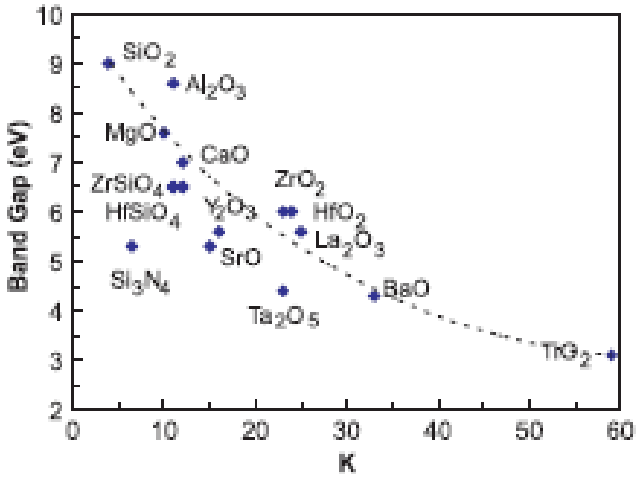


Figure 1.3: Comparison of bandgap with dielectric constant [from 26]

High-κ dielectrics do not tend to form abrupt interfaces with either the substrate or MG due to thermal instability; high interface state density (D_{it}), fixed charges, and bulk dielectric charges may cause C-V hysteresis and V_{th} shifting which affect stack stability and device reliability [3, 26, 82]. The interface structure may unexpectedly lower the final dielectric constant achieved from its expected value [2, 3, 82]. Evolution of the dielectric structure during fabrication often causes oxygen diffusion and related dipole formation and V_{fb} roll off [31, 84-86]; grain boundaries caused by dielectric crystallization may contribute to gate leakage [60, 87]. The MG WF is strongly dependent on the underlying H-κ, as well [61]. Figure 1.4 displays the structure of the MG/High-κ stack and the various effects which must controlled to optimize performance.

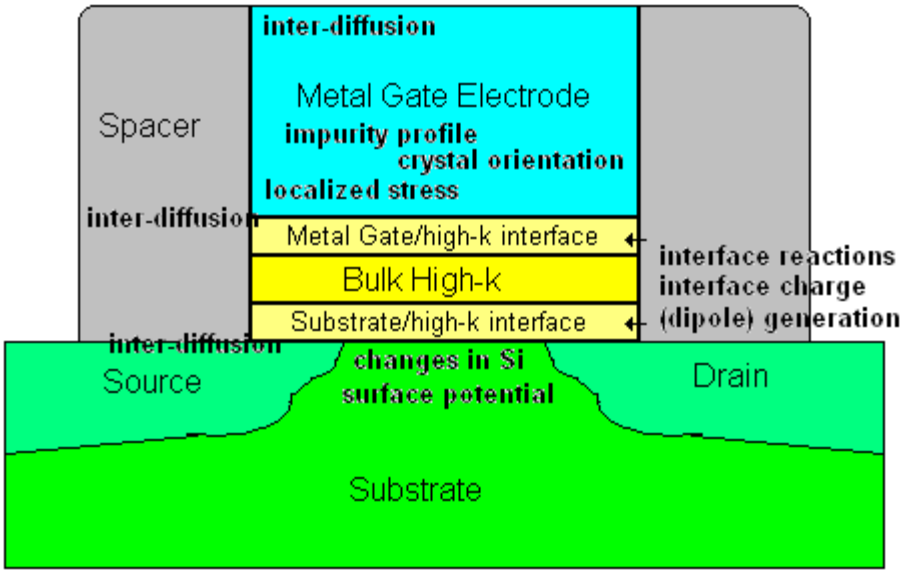


Figure 1.4: Planar MG/High-κ stack displaying challenges of the fabrication process

High temperature fabrication effects are central to the stability and reliability of MG/High-κ electrodes. In low temperature, gate last fabrication the gate stack is formed after the high temperature fabrication processes have been completed and there is less destabilization of the stack structure [29, 88]. The fabrication process flow must be drastically adapted to accommodate gate last processing [13, 44, 89, 90]. Commercially available ICs incorporating MG/High-κ are produced using the gate last method [13, 89]. Gate first fabrication methods require greater optimization to ensure stack stability; however, the method is more cost effective and considered preferable because it may be seamlessly incorporated into conventional fabrication processes [89-91].

1.3 WORK FUNCTION TUNING

Unlike poly-Si gates the WF of which may be engineered by channel and gate doping, MGs have a more limited WF tuning range. As shown in Figure 1.5, the WF of the metal incorporated in an electrode may differ greatly from the metal's vacuum WF value. This non-vacuum WF value is referred to as the effective work function (EWF)

[28, 82, 93]. The EWF achieved is determined by the dielectric and its thickness [28, 31, 94-96], deposition conditions and process [31, 97], MG composition [3, 13, 55, 98] and relative material ratios in multiple metal layer gates [25, 26, 99-102]. EWF may change radically during high temperature processing as strain develops, the interface roughens, and orientation or grain size evolve [31]. Controlled tuning is used to engineer EWF values appropriate for a specific Vth range. Si ratio [102] and ion implant [27, 103, 104] are among the many methods utilized to tune EWF.

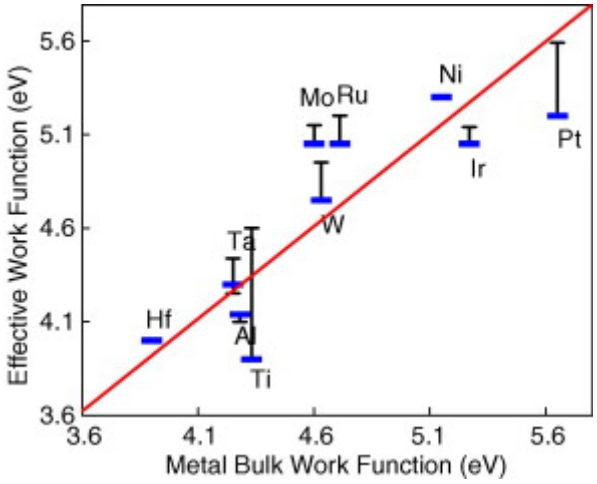


Figure 1.5: Effective work function on SiO_2 versus bulk work function for various metal electrodes reported in literature [from 31]

1.3.1 Engineering Work Function Tuning Range

Single MG materials must have an EWF tunable across the Si bandgap and within .2eV of the Si conduction and valence band edges (~4.1eV and ~5.2eV, respectively) for bulk devices [27, 93]. Poly-Si gates may easily achieve the required ~1.1eV tuning range through channel and gate doping. Doping may also be used to achieve multiple threshold voltage tuning of both types for better LOP and HP power efficiency [30, 105].

MGs do not achieve appropriate EWF tuning for single MG bulk Si applications [27, 31, 106]. While the mid-gap metals investigated have not been capable of achieving the +/-.4eV WF tuning required for bulk devices, many metals may be engineered to

obtain either n-MOS or p-MOS appropriate EWF values [31, 107, 108]. Figure 1.6 represents the EWF of various MG/dielectric stacks after 1,000˚C anneal; circled data indicates stacks which achieve targeted n-MOS and p-MOS EWF values.

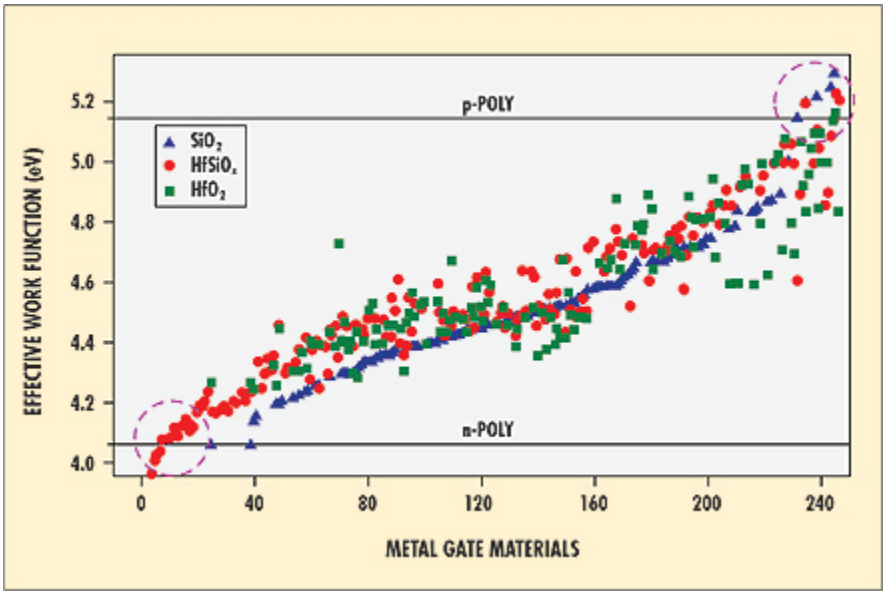


Figure 1.6: Metal work function tuning ranges: n-MOS compatible, p-MOS compatible, and mid-gap [from 107]

Dual metal gates (DMGs) incorporating a separate metal for n-MOS and for p-MOS compatible electrodes, respectively, have been adopted by industry to commercially develop MG/High-κ devices [3, 13, 26, 108]. Incorporating DMGs substantially increases fabrication cost and complexity. Numerous additional fabrication steps are required to selectively remove the first gate metal and deposit the second [3, 13, 109-111]. The first deposited dielectric might also be removed and another deposited for the second MG stack [3, 20, 107, 109]. Figure 1.7 presents a generalized DMG fabrication scheme in which both the first metal and dielectric are etched back and replaced.

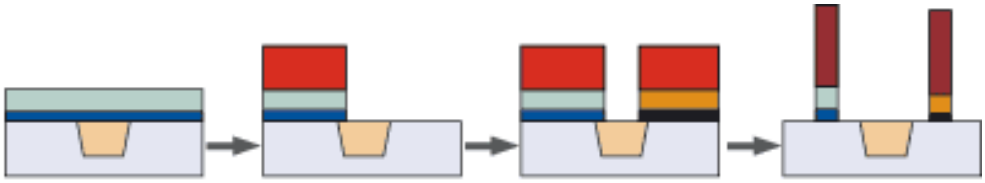


Figure 1.7: DMG fabrication requiring both metal and dielectric variation between n-MOS and p-MOS gates [from 109]

The DMG EWFs achieved may differ radically from those expected if the fabrication processes are not optimized and carefully monitored. All DMG etchants, dielectrics, metals, and fabrication processes must be mutually compatible [7, 109, 112]. The dielectric surface must not be damaged or unduly roughened during the first metal etch and wet etch undercutting must be minimal [2, 109, 111, 112].

1.3.2 Structure Specific Work Function Tuning Range: Bulk v. SOI

Planar and non-planar ultra thin body silicon on insulator (UTB-SOI) structures capable of meeting scaling demands beyond the 10nm dimension have been introduced as alternatives to bulk technology [3, 13, 112-114]. As exemplified in Figure 1.8, planar UTB-SOI structures consist of a very thin (≤ 10nm) partially (PD-SOI) or fully (FD-SOI) depleted Si channel layer between the gate and a buried oxide (BOX) layer while non-planar devices consist of a three dimensional (3-D) Si fin field effect transistor (FinFET) surrounded on two or more sides by the MG/High-κ dielectric stack.

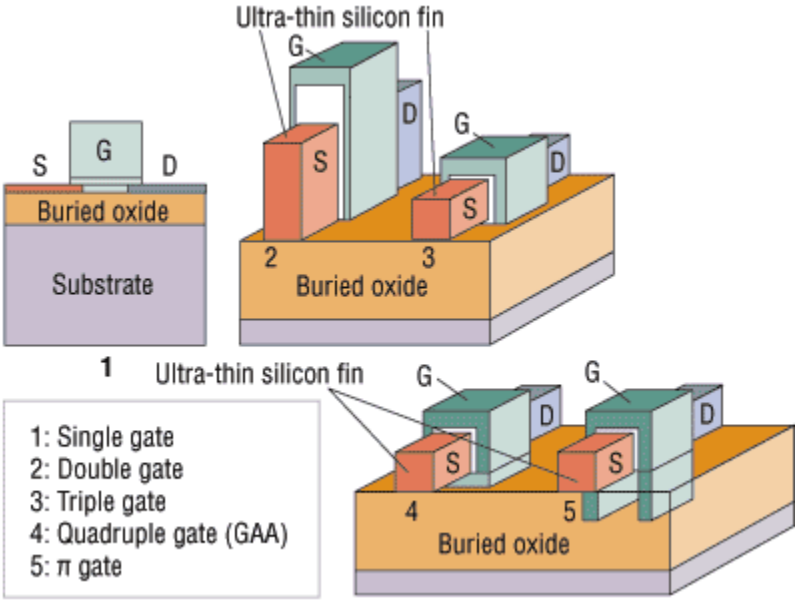


Figure 1.8: UTB-SOI planar and non-planar device structures [from 114]

UTB-SOI technology provides many advantages over conventional bulk structures. The undoped/low doped channel is immune to V_{th} variation with Si film thickness and contributes to higher mobility and a reduction in junction leakage [115]. UTB-SOI devices have lower junction capacitance than bulk structures and are immune from latch-up [3, 113, 116, 117]; SCEs are also suppressed at the reduced Si thicknesses required for sub-micron applications [43, 113, 117].

Multigate FETs (MugFETs) such as the FinFET which have been optimized to limit roughness and thickness variation provide additional advantages. The multigate structure enhances current drive and I_{on}/I_{off} ratios while affording better SCE control [10, 13, 44, 114, 116]. FinFETs with varying channel lengths may be fabricated in close proximity for more compact and efficient system on a chip (SOC) design. Figure 1.9 compares the properties of bulk, planar UTB-SOI, and multiple gate UTB-SOI structures.

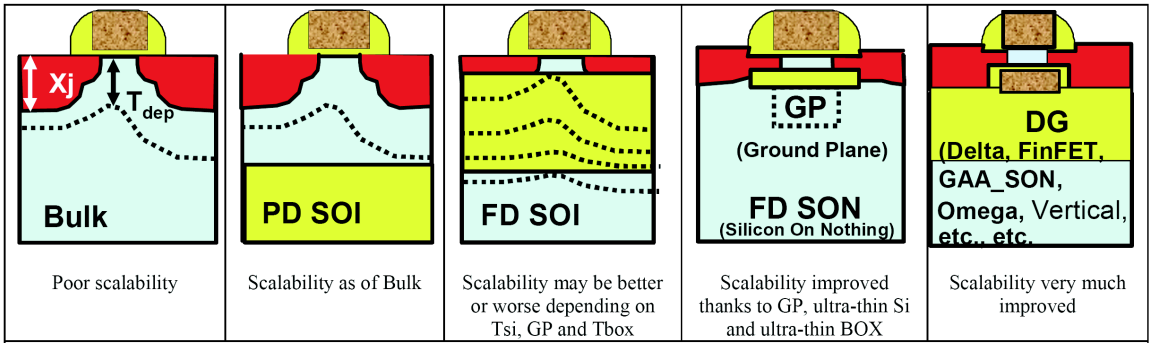


Figure 1.9: Comparison of the properties of bulk structures with planar and multiple gate SOI devices [from 13]

The most important advantage of UTB-SOI technology for MG development is the decreased WF range necessary for n-MOS to p-MOS V_{th} tuning. Because the channel is undoped or lightly doped, only +/- .2eV change from mid-gap is necessary to achieve n-MOS (~4.4eV) to p-MOS (~4.9eV) EWF tuning [13, 27, 93]. Many MG materials are capable of achieving the UTB-SOI tuning range; a simpler and less costly option to DMG fabrication is possible for UTB-SOI implementation [13, 20].

1.3.3 Engineering SOI Appropriate Single Metal Work Function Tuning Range

EWF values depend on both the metal and dielectric used, as shown in Figure 1.6. Tuning may be achieved by engineering the characteristics of the materials used. Changes in composition or composition ratios between components resulting from implantation [7, 118, 119] or inter-diffusion [109] influence structure, crystallinity, thermal stability and, finally, EWF. Much research must be invested to determine appropriate tuning methods which will maintain the integrity of the underlying material. TaN_x, TiN_x, and $TiSi_xN_y$ MGs on Hf based dielectrics (HfO_2 and $HfSiO_xN_y$) are promising mid-gap gate stack materials capable of achieving the +/-200meV EWF tuning appropriate for n-MOS to p-MOS UTB-SOI FinFET structures. These gate stack structures have been rigorously investigated and proven stable and reliable [3, 43, 44].

1.4 DISSERTATION OUTLINE

The purpose of the research herein is twofold. First, MG/High-κ dielectric stacks capable of +/-.2eV EWF tuning around mid-gap are determined and the tuning mechanism analyzed. Second, a simple single MG integration method is developed for SOI FinFET fabrication incorporating insight gained from the metal EWF tuning mechanism analysis.

EWF extraction is an important but complicated issue; an effective analysis method has only recently been developed. Chapter 2 provides an introduction to the myriad issues which have confounded researchers' attempts to accurately determine the EWF of MG/High-κ dielectric stacks. A description of the terraced oxide EWF extraction method and the difference between the factors which must be included in the EWF analysis of MG/High-κ stacks compared with analysis of conventional gate stacks is provided.

Chapter 3 investigates MG/High-κ stacks promising EWF tuning ranges appropriate for n-MOS to p-MOS tunable single mid-gap MG UTB-SOI FinFET applications. Insight is provided into the mechanisms causing the +/-.2eV EWF tuning around mid-gap through materials and electrical analysis. Methods of utilizing these mechanisms to further simplify the fabrication process are proposed.

Device structures implementing the tuning mechanisms analyzed in Chapter 3 are fabricated in Chapter 4. Thickness variation is proven to provide appropriate single MG stack n-MOS to p-MOS work function tuning for UTB-SOI structures. An innovative fabrication method is introduced engineering the thickness tuning mechanism to further simplify fabrication resulting in a 40% reduction in fabrication steps compared to DMG.

Chapter 5 summarizes the research conducted herein and provides suggestions for future research based upon the results and insight gathered.

CHAPTER 2

EFFECTIVE WORK FUNCTION EXTRACTION

2.1 MOTIVATION

When the gate, insulator, and semiconducting regions of a MOSFET are brought into contact, differences in potential between the gate and semiconductor work functions (WFs) cause band bending in the semiconductor [93, 120]. The flat band voltage (V_{fb}) is the voltage required to compensate for the band bending [93]. Although WF values are difficult to evaluate directly, V_{fb} values may be easily extracted from simple electrical measurements using conventional polysilicon (poly-Si)/silicon dioxide (SiO_2) structures and the relationship between V_{fb} and WF to calculate gate WF values indirectly [26].

Successfully extracting the EWF values of metal gate (MG) stacks has proven far less straightforward than WF evaluation in conventional stacks. While poly-Si/SiO_2 interfaces are abrupt and interface states may be neglected when calculating WF, MG/High-κ dielectric interfaces are substantial, interface charges and charges in the High-κ bulk significantly affect the final EWF [26, 27, 31, 82]. Even minor differences in the fabrication process may significantly affect interface states in MG/High-κ stacks of the same composition resulting in drastically different EWF values [26, 27, 66, 82].

An innovative method using terraced oxide wafers and a modified charge distribution analysis to effectively determine MG/High-κ EWF has become the standard for EWF evaluation [31]. The terraced oxide method is central to the EWF analysis to be presented in Chapter Three; a comprehensive description of the method and a summary of complementary EWF extraction methods are presented herein.

2.2 EFFECTIVE WORK FUNCTION EXTRACTION METHODS

EWF is generally determined by application of one or more of three central parameter analysis methods: internal photo emission (IPE), capacitor-voltage (C-V), and current density-voltage (J-V) [26]. Each method analyzes the EWF from a different perspective. The results obtained may be compared between analysis methods to confirm their mutual consistency [120].

2.2.1 Internal Photo Emission (IPE) [121]

IPE is a direct measurement surface analysis technique [26, 120, 122]. In IPE, a metal's Schottky barrier height is ascertained by bombarding the metal with incident electromagnetic radiation. EWF is equal to the minimum frequency for which photo-emission occurs multiplied by Plank's constant ($h = 6.63x10^{-34}$ J/s).

IPE analysis is an involved process and difficult to implement for ultra-scaled device analysis. Specially designed MOS capacitors (MOSCAPs) must be engineered to include a thin, light transparent metal layer and a dielectric layer thick enough to prevent leakage current from contributing to the photo induced current observed [122]. IPE analysis suggested a broader MG EWF tuning range than that observed using conventional C-V analysis; EWF values obtained using C-V and the terraced oxide method are in better agreement with IPE results [26].

2.2.2 Current Density - Voltage Analysis (J-V) [93, 103, 120]

Like IPE, the J-V method is a direct measurement technique; EWF values observed are independent of Q_f and other charge [93, 103]. J-V analysis uses the metal/dielectric barrier height (Φ_b) to determine EWF with respect to vacuum. I-V measurements are taken on capacitors of various thicknesses to determine the applied voltage (Φ_b/q) at which Fowler-Nordheim Tunneling (F-Nt) transitions to direct

tunneling, as illustrated in Figure 2.1[93, 120]. This voltage is related to Φ_b at the metal/dielectric interface and occurs at the voltage peak, $\delta(\ln(J_g))/\delta V$ [93, 103].

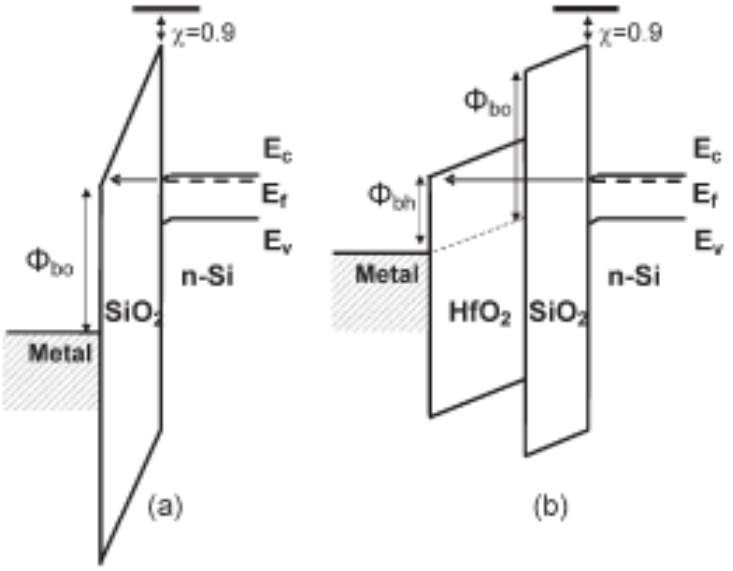


Figure 2.1: Band diagrams expressing bending related to Fowler-Nordheim and direct tunneling [from 120]

Drawbacks of the J-V method include breakdown of the dielectric films during measurement of the tunneling current and difficulty in obtaining a priori knowledge of the effective electron mass in the dielectric films [26, 120]. A detailed description of the J-V method may be found in Zafar [93] and Wen [120].

2.2.3 Capacitance - Voltage Analysis (C-V)

The C-V method is conventionally used to extract EWF because it is straightforward, efficient, and may be used with conventional MOSCAP structures. The method uses the relationship between capacitance and threshold voltage to extract equivalent oxide thickness (EOT) and V_{fb}.

Poly-Si/SiO_2 and MG/SiO_2 stack WF is obtained from the C-V method using MOSCAPs fabricated on multiple wafers, each wafer having a different insulator

thickness [27, 28, 66, 123]. C-V measurements are taken at the various insulator thicknesses and the V_{fb} and EOT values extracted according to the relationships:

$$1/C = EOT/\varepsilon_{ox} + 1/C_s(\varepsilon_{ox}) \qquad (1)$$

$$V_g = E_{ox}T_{eq} + \varphi_s(\varepsilon_{ox}) + V_{fb}\ [97] \qquad (2)$$

In these equations, E_{ox} is the effective electric field across a gate dielectric while $C_s(\varepsilon_{ox})$ and $\varphi_s(\varepsilon_{ox})$ are substrate surface capacitance and potential, respectively. EOT is the equivalent oxide thickness and V_{fb} is the flat band voltage. ε_{ox} is the insulator dielectric constant.

Generally, the experimentally obtained C-V curves are fitted to modeled curves generated using known parameters such as substrate doping. Experimentally measured C-V curves which are within 1σ confidence level of the simulated curve are used to extract the relevant V_{fb} and EOT values [25]. Experimental data which strongly diverges from the curve model may indicate inconsistencies in the measurement methodology or differences between the intended and actual fabrication steps implemented [25, 82].

In highly scaled structures with insulator thicknesses <2nm, quantum mechanical (QM) effects and, in the case of conventional poly-Si/SiO_2 gate stacks, poly-depletion effects must be considered [25]. There is an ongoing effort to ensure appropriate C-V curve modeling methods for ultra scaled device analysis [97, 99]. The North Carolina State University Capacitance Voltage Characterization (NCSU CVC) program effectively incorporates the most salient QM issues affecting highly scaled devices in its simulations and is the program used to extract V_{fb} and EOT values related to this research [25].

V_{fb} v. EOT plots incorporating data obtained from the MOSCAPs of varying insulator thickness should generally exhibit a linear relationship represented by the equation:

$$V_{fb} = \Phi_{ms} - \frac{Q_f * EOT}{\varepsilon_{OX}} \quad (3)$$

In equation 3, Φ_{ms} is the difference between the metal and Si substrate work function, the Si work function value being either that of intrinsic Si or a value determined by the substrate doping [123]. Q_f is the fixed charge at the insulator/silicon substrate and ε_{ox}, the permittivity of the oxide used [27, 66, 123].

The intercept of the equation at EOT = 0 is the value of Φ_{ms}; the value of Φ_s may be subtracted from the intercept value to obtain Φ_m using the equation:

$$\Phi_m = V_{fb} \text{ intercept} - \Phi_s \text{ [66, 120]} \quad (4)$$

$\frac{Q_f}{\varepsilon_{OX}}$ is the slope of the line in the V_{fb} v. EOT relationship and indicates the fixed charge at the Si/SiO_2 interface. A shift in slope between V_{fb} v. EOT plots indicates a difference in fixed charge at the interface. When the comparison is between plots of annealed and unannealed MOSCAPS having the same stack structure, the mechanism causing the change often warrants further investigation [27].

2.3 METAL GATE/HIGH-κ STACK EFFECTIVE WORK FUNCTION EXTRACTION

The conventional method used to extract EWF from metal and poly-Si gates deposited on SiO_2 is effective because the abrupt Si/SiO_2 interface produces a relatively constant Q_f value across multiple wafers [26, 27]. SiO_2 also tends to be a thermally stable insulator incorporating negligible bulk charges [26]. These characteristics ensure uniform and predictable MOSCAP behavior despite the use of separate wafers for each dielectric thickness [66]. The assumption of low Q_f and negligible bulk charge cannot be assumed for gate stacks incorporating High-κ dielectrics [27, 66, 123].

2.3.1 Metal Gate/High-κ Anomalies

High-κ dielectrics generally have significant bulk charge and tend to form interfaces with the MG and substrate which incorporate significant charge traps and foster dipole formation [26, 27, 66]. These charges produce non-uniformities between the individual wafers of independent High-κ thickness which interfere with accurate EWF estimation [27]. As illustrated in Figure 2.2, charge non-uniformity produces non-linearity in the conventionally derived V_{fb} v. EOT plot. The small number of data points generally used for conventional EWF extraction and evaluation exacerbate the problem; a different EWF may be derived depending upon which points in the graph are used for the actual extraction [26, 27].

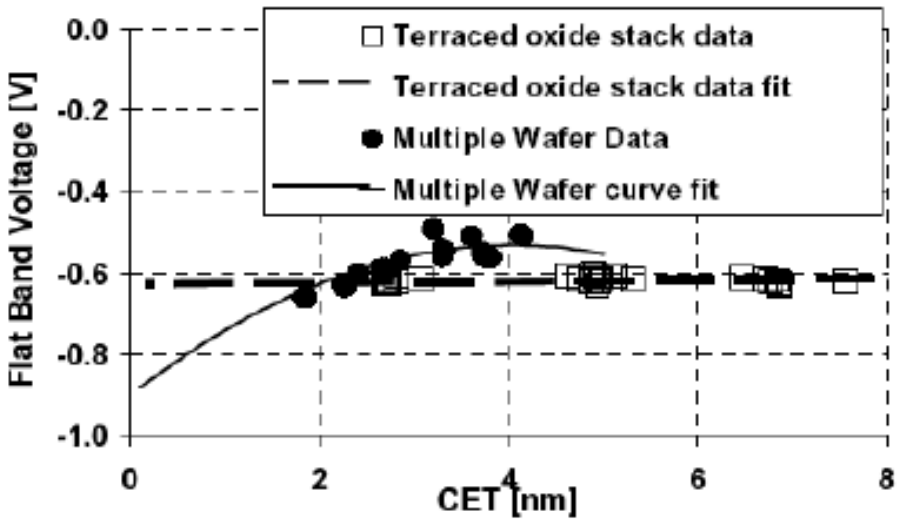


Figure 2.2: Comparison of EWF extracted from terraced oxide wafer and multiple wafers [from 27]

Initial research using the conventional C-V extraction method produced inconsistent EWF values, as displayed in Figure 2.3, even for the same gate stack structure and fabrication procedure [28, 66].

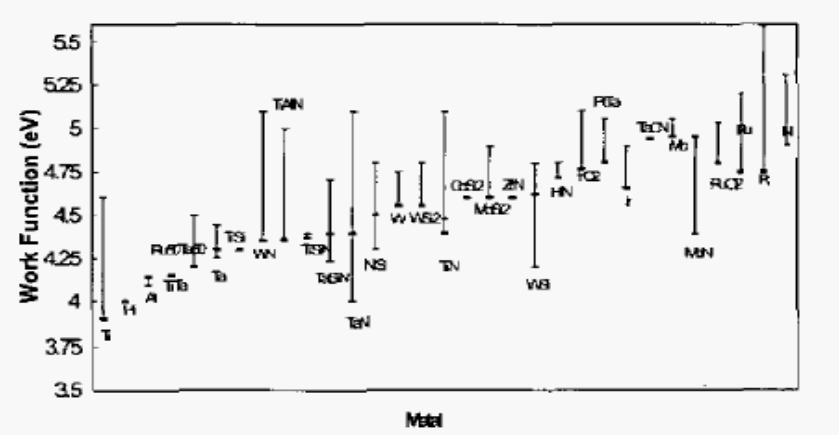


Figure 2.3: EWF spread extracted from reported values obtained using conventional C-V extraction from independent wafers with varying High-κ thickness [from 28]

These somewhat haphazard results once led researchers to conclude that Fermi level pinning effects might make p-MOS appropriate metal gates impossible to obtain [26, 100, 101]. In order to effectively extract EWF values from MG/High-κ dielectrics, the entire extraction method has been revised to ensure the nature of the MG/High-κ structure is appropriately addressed.

2.3.2 Charge Distribution Modeling

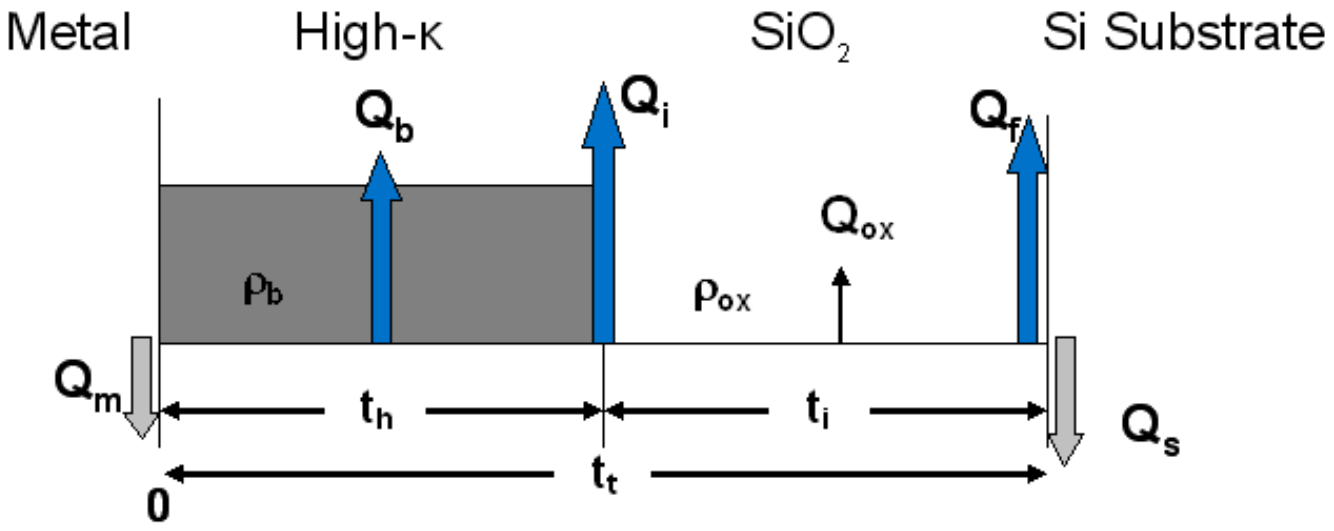


Figure 2.4: Charge distribution model for MG/High-κ stack [after 66]

The model used to determine EWF for a MG/High-κ stack must incorporate the charges determining EWF illustrated in Figure 2.4 [27]. In the model, Q_m represents the charge at the MG/High-κ interface, Q_b is the effective bulk charge in the High-κ dielectric (with center at centroid of High-κ derived from bulk charge density (ρ_b)), Q_i is the interface charge between the High-κ and SiO_2, Q_{ox} is the effective bulk charge in the SiO_2 region due to oxide bulk charge (ρ_{ox}), Q_f is the fixed charge at the Si/SiO_2 interface, t is the total thickness of the film, t_h is the physical thickness of the H-κ, and t_i is the thickness of the SiO_2 interface.

In order to effectively accommodate all of the charge within the stack and to precisely determine the EWF, a four charge analysis model has been developed to incorporate: (1) the SiO_2-substrate interface charge, (2) the interfacial oxide/High-κ interface charge, (3) the interfacial oxide bulk charge, and (4) the High-κ bulk charge [123]. The resulting equation:

$$V_{fb} = \Phi_{ms} + \frac{1}{\varepsilon_h}\int_0^{t_h} x\rho_b(x)dx - \frac{Q_i * EOT_h}{\varepsilon_h} + \frac{1}{\varepsilon_{OX}}\int_{t_h}^{t} x\rho_i(x)dx - \frac{Q_f * EOT}{\varepsilon_{OX}} \quad \text{[66]} \quad (5)$$

is quadratic and complex to solve [82]. The equation may be simplified by excluding charge terms which have only a nominal effect on the EWF [27]. For example, ρ_i is generally negligible because it is so much smaller than the Q_f contribution and may be excluded with minimal effect on the accuracy of the EWF values obtained [66]. The resulting equation is a three charge model [27, 66, 120]:

$$V_{fb} = \Phi_{ms} - \frac{Q_i * EOT_h}{\varepsilon_{OX}} - \frac{\rho_b * (\frac{\varepsilon_h}{\varepsilon_{OX}}) * EOT^2{}_h}{2 * \varepsilon_{OX}} - \frac{Q_f * EOT}{\varepsilon_{OX}} \quad \text{[27, 120]} \quad (6).$$

If ρ_i happens to be large for a particular sample, this will be obviated by errors in the model and the more complex equation may be used instead [27, 66].

When the V_{fb} v. EOT plot is created using data obtained from terraced oxide wafers, the technique and its importance to be explained in 2.3.3, the High-κ layer is uniform in thickness [27, 66]. This uniformity causes the first three terms of equation (6):

$$\Phi_{ms} - \frac{Q_i * EOT_h}{\varepsilon_{OX}} - \frac{\rho_b * (\frac{\varepsilon_h}{\varepsilon_{OX}}) * EOT^2{}_h}{2 * \varepsilon_{OX}}$$

, to be constant in value so that only High-κ related charges affect the intercept value and equation (6) takes on the general form of equation (3) [27]. Equation (6) may be used to extrapolate EWF from the linear relationship of the V_{fb} v. EOT plot, the slope of the line again representing Q_f, as illustrated in Figure 2.5 [27, 120].

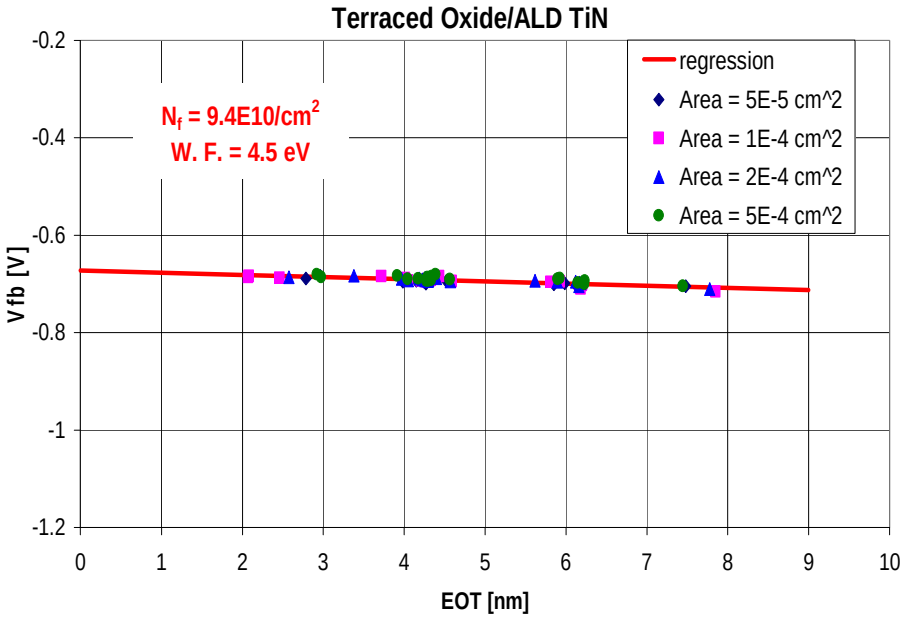


Figure 2.5: Linear V_{fb} v. EOT obtained using terraced oxide wafer [from 66]

The role of the second and third terms of equation (6) related to Q_i and ρ_b determine the ordinate intercept of the equation and may be investigated by varying the High-κ thickness to determine their magnitude [27].

2.3.3 Terraced Oxide Wafers: Crucial Element in Three Charge Model Effective Work Function Extraction

Conventional poly-Si/SiO_2 EWF extraction from multi-wafer C-V data is accurate because the dielectric has a low oxide bulk charge and Q_f is relatively fixed [27]. These characteristics ensure consistency in charge distribution between wafers despite any variation in SiO_2 deposition conditions. In High-κ dielectrics, bulk charge and Q_f vary significantly with insulator thickness and show dependence upon the deposition method [27, 28, 66]. It is extremely difficult to maintain bulk charge and Q_f values sufficiently consistent across multiple wafers to obtain a linear V_{fb} v. EOT relationship which may be used to extrapolate the EWF. Applying the four charge model is complex and defeats the goal of the C-V extraction method to efficiently and simply determine EWF values [66]. The three charge model simplifies EWF extraction; however, multiple wafer measurement is not conducive to its application [27].

2.3.3.1 Terraced Oxide Wafer Fabrication [27]

A single wafer MOSCAP fabrication method implementing a terraced oxide surface upon which a constant High-κ thickness is deposited has been established to support simple EWF extraction using the three charge model. The terraced oxide wafer is fabricated by deposition of a thick (10nm) thermal SiO_2 layer upon an Si substrate. The wafer is spun horizontally using a spin processor (SEZ^{TM} model 203) and a benign hydrofluoric acid (Hf) etchant stepped across the wafer using a nozzle dispenser [66]. The etchant is stepped from the center of the wafer to the edge to create three to four distinct oxide thicknesses (often a 20Å - 80Å thickness range with a 20Å step between the individual terraces) distributed in a radial pattern across the wafer. Figure 2.6 presents the thickness distribution visibly distinguishable by the distinct color regions created by the thickness variation. Thickness distribution is very consistent across multiple wafers, as Figure 2.7 illustrates.

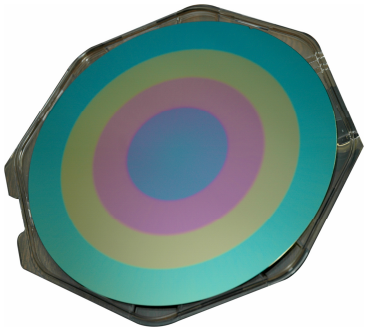


Figure 2.6: Terraced oxide wafer [from 102]

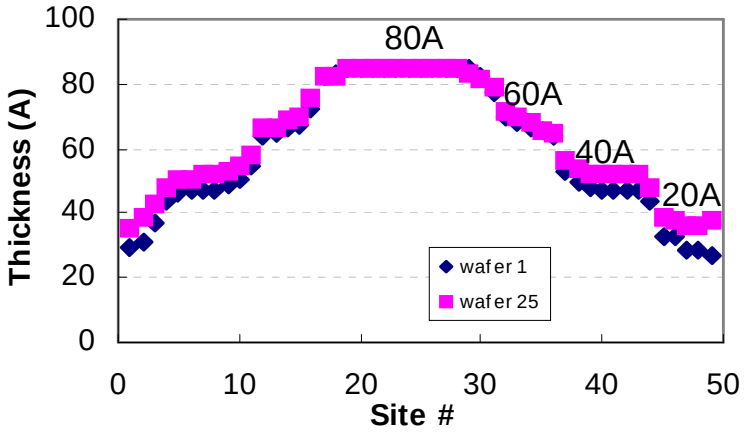


Figure 2.7: Consistent SiO_2 thickness across multiple terraced oxide wafers [from 66]

2.3.3.2 EWF Extraction

Once the terraced oxide wafer has been fabricated, the High-κ insulator is deposited at a uniform thickness across the wafer [27]. In Figure 2.8, the metal gate is deposited atop the High-κ to create MOSCAPs with varying insulator thickness upon a single wafer.

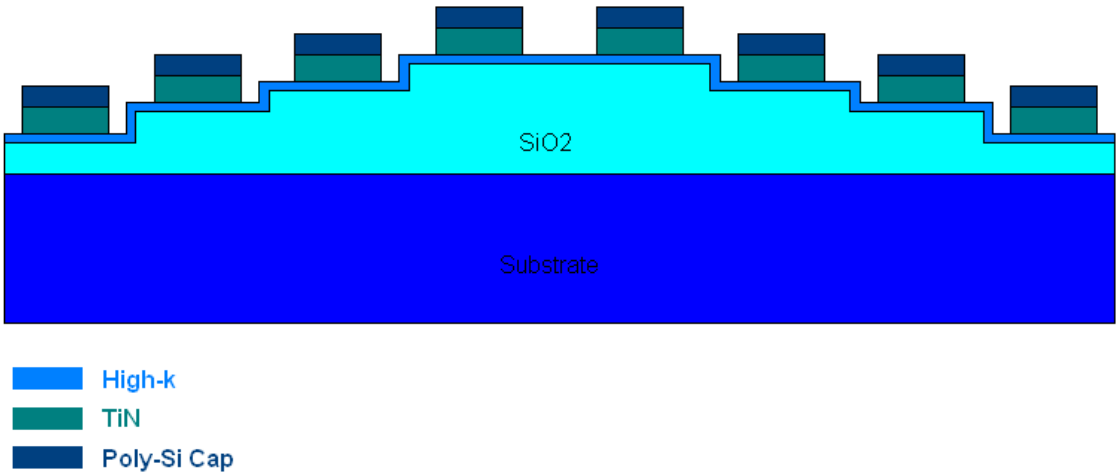


Figure 2.8: Terraced oxide MOSCAP structure

The variation in thickness of the specific MOSCAP is determined by the total thickness of the uniform High-κ and the underlying SiO_2 [27, 28].

MOSCAP fabrication on a single wafer with varying insulator thickness creates uniformity in the High-κ and various interfaces which cannot be achieved using independently fabricated wafers of varying thickness [28, 66]. The uniform High-κ thickness ensures consistent bulk charge throughout the insulator and the single SiO_2 deposition provides a constant Q_f value [27]. Consistency of the High-κ bulk and Q_f charge are illustrated by the linearity of the V_{fb} v. EOT slope for the terraced oxide stack in Figure 2.5, above.

The consistency of the data and resulting extracted EWF has also been improved by inclusion of a larger data field [26, 27]. As presented in Figure 2.9, the EWF values obtained from the three charge extraction method using terraced wafer structures are in excellent agreement with values obtained from the J-V barrier height estimation method [120]. This agreement supports the mutual validity of the two methods.

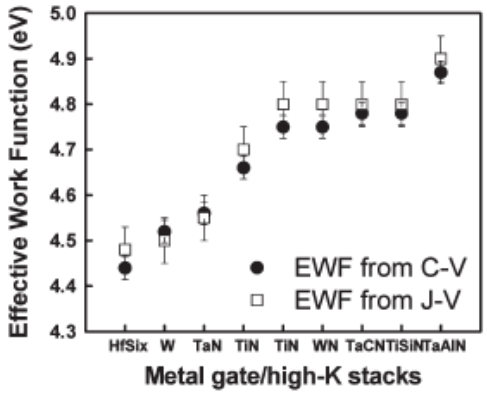


Figure 2.9: Comparison of EWF obtained on the same gate stack from J-V and C-V methods [from 120]

2.4 CONCLUSIONS

The three charge extraction method using terraced oxide structures has been established to provide consistent EWF results [27, 66]. The method is powerful and provides insight into the underlying mechanisms affecting gate stack charge distribution which had been neglected before the method's advent. The three charge/terraced oxide

method has established that metal gates have larger tuning ranges than initially assumed possible. This greater tuning range has led to progress in determining p-MOS appropriate gate materials and candidates for single metal bulk and UTB-SOI gates [20, 53, 94-96, 102, 104, 124-126]. The method has also provided insight into the nature Fermi level pinning and its role in EWF [31, 53]. V_{fb} roll off and a fundamental understanding of its nature and mechanics are central discoveries resulting from three-charge terraced oxide C-V analysis [84, 86, 104, 127]. Due to the advantages of its simplicity and accuracy as well as its growing popularity as the standard for EWF extraction, the three charge/terraced oxide method has been used to determine and analyze EWF within this thesis.

CHAPTER 3

TITANIUM NITRIDE ACHIEVING +/- 200meV EWF TUNING RANGE AROUND SILICON MID-GAP THROUGH THICKNESS MODULATION: METHOD AND MECHANISMS

3.1 INTRODUCTION

Single metal gate (MG)/High-κ dielectric electrodes cannot presently achieve the 1.1eV EWF tuning range required for bulk silicon (Si) applications. Dual metal gate (DMG) technology resolves this dilemma but introduces additional complexity and expense into the fabrication process. A single MG option would significantly simplify MG/High-κ fabrication and reduce cost.

Ultra thin body silicon on insulator (UTB-SOI) device structures require only a +/-.2eV single MG tuning range around the Si mid-gap to achieve n-MOS to p-MOS compatible effective work function (EWF) values. UTB-SOI technology is considered the most viable option for scaling through the 10nm dimension [44, 128-130]; advances have been made to simplify UTB-SOI integration and to improve performance and reliability [7, 20, 13, 44, 131, 132]. Metals achieving the required UTB-SOI tuning range have been identified [7, 13, 20, 98, 118, 119, 133, 134] and efforts have begun to develop single MG/High-κ devices [20, 128].

Titanium Nitride (TiN) is a mid-gap refractory metal which has been proven to provide stable and reliable MG/High-κ electrodes with an appropriate EWF tuning range for single MG UTB-SOI complementary metal on insulator (CMOS) fabrication [3, 7, 133, 135]. TiN mid-gap EWF is partially determined by the dielectric with which it is paired and by fabrication conditions [7, 131, 133, 136-139]. Thickness, deposition

method, and Si incorporation have been proven to effectively tune the TiN EWF around mid-gap [7, 20, 133, 134, 136-138, 140, 141].

This chapter investigates thickness modulated TiN EWF tuning. The research suggests that thickness dependent crystalline structure and related diffusion effects during high temperature annealing act as EWF modulation mechanisms [7, 60, 67, 133, 135, 136, 140-144]. Thickness modulated EWF engineering will be central to the innovative, simple and cost effective fabrication process introduced in Chapter 4.

3.2 TiN METAL GATE EWF TUNING: THICKNESS MODULATION

TiN has long been recognized as a durable coating material and, more recently, a reliable metal capable of producing stable gate electrodes on both High-κ and SiO_2 dielectrics [3, 44, 145, 146]. The material is a mid-gap metal already used in semiconductor device fabrication as a diffusion barrier and for high-efficiency interconnects [147]. TiN is commonly utilized as an n-type electrode in dual metal gate research; as a result, the TiN electrode is exceptionally well understood and fabrication has been optimized to produce reliable, repeatable behavior [3, 66, 135, 141]. TiN has been reported capable of achieving the continuous EWF tuning between ~4.3eV and ~4.8eV required for single MG UTB-SOI applications [6, 133]. Electrical analysis of conventionally fabricated metal on semiconductor field effect transistor (MOSFET) and capacitor (MOSCAP) structures and materials analysis of the gate stack provide insight into the EWF tuning mechanism and how it may be engineered.

3.2.1 Experimental

The mechanism governing TiN EWF thickness tuning was investigated using C-V MOSCAP analysis. Individual MOSCAPs were fabricated to include various combinations of TiN metal gate thickness, metal deposition method, dielectric material, and dielectric thickness. Preliminary analysis involved atomic layer deposition (ALD) of

TiN at 5, 20, 50, 100, 200, and 400 cycles (producing ~ .5, 2 ,5 ,10 , 20, and 40nm films) using $TiCl_4$ and NH_3 precursors on 3nm thick SiO_2, $HfSiO_x$ or HfO_2 dielectric which had been ALD deposited on the terraced oxide structures described in Chapter 2. The High-κ dielectrics were nitrided prior to TiN deposition using a 60 second 700˚C post deposition anneal (PDA) in NH_3 or N_2 [139, 148, 149]. The resultant electrode received a 5 second 1000˚C rapid thermal anneal (RTA) after being capped with a 150nm n+ polysilicon (poly-Si) capping layer [133].

Analysis of the TiN deposition method on EWF thickness modulation involved electrical characterization of MOSCAPs incorporating ALD, CVD, or PVD TiN metal gates of varying thickness (50, 100, 150, 200, and 400 cycles) deposited as previously described with the exceptions that the High-κ dielectric was 2nm HfO_2 and the post-poly-Si deposition RTA was conducted for 10 seconds [137]. EWF values were extracted from EOT v. V_{fb} plots determined from MOSCAP C-V measurements using the NCSU CVC extraction method described in Chapter 2.

The process flows of the various TiN metal gate stacks were duplicated on blanket wafers and materials analysis conducted to investigate thickness related changes in the stack which may provide insight into the EWF modulation mechanism. The physical analyses conducted include: x-ray diffraction (XRD) and grazing incident angle x-ray diffraction (GI-XRD), x-ray photoelectron spectroscopy (XPS), x-ray reflectometry (XRR), ellipsometry, and high resolution transmission electron microscopy (HRTEM). Secondary ion mass spectrometry (SIMS), electron energy loss spectroscopy (EELS) and dispersive x-ray analysis (EDX) were conducted on device structures [128, 135]. Stress within the stack was measured by analyzing changes in substrate curvature before and after TiN deposition using a Tencor Alphastep surface profiler.

Physical analysis data was used to establish density, roughness, thickness, chemical composition, relative grain size, crystallinity, and both the chemical and physical profiles of the gate stack [6, 133, 135, 137]. Particular attention has been given to the MG/dielectric interface, the effect of metal thickness on MG/dielectric interface, and the effect of metal thickness on the Ti:N ratio within the metal film.

3.2.2 EWF Evolution with TiN Thickness: Results and Analysis

TiN deposited on 2nm HfO_x		**Intended Thickness (Ångstroms)**				
		50	**100**	**150**	**200**	**400**
PVD	**Thickness XRR (Å)**	**54.98**	**107.93**	**164.68**	**224.15**	**448.93**
	EWF (eV)	**4.45**	**4.61**		**4.73**	
	Stress (dyne/cm^2)	**-9.13 x 10^{10}**	**-6.32 x 10^{10}**	**-5.05 x 10^{10}**	**-4.29 x 10^{10}**	**-2.90 x 10^{10}**
	Resistivity (μΩ-cm)	**388.68**	**155.84**	**99.157**	**73.37**	**37.377**
	Density (g/cm^3)	**5.02**	**5.03**	**4.98**	**4.93**	**4.86**
	Roughness (Å)	**7.7**	**9.47**	**10.53**	**11.67**	**15.53**
CVD	**Thickness XRR (Å)**	**43.21**	**97.87**	**146.23**	**173.53**	**403.3**
	EWF (eV)	**4.45**	**4.65**		**4.8**	**4.8**
	Stress (dyne/cm^2)	**-6.52 x 10^{10}**	**-1.37 x 10^{10}**	**-7.84 x 10^{08}**	**3.35 x 10^{09}**	**1.69 x 10^{10}**
	Resistivity (μΩ-cm)	**1411.2**	**519.19**	**332.92**	**276.78**	**113.12**
	Density (g/cm^3)	**4.23**	**3.99**	**3.94**	**3.94**	**3.91**
	Roughness (Å)	**9.77**	**8.93**	**9.5**	**9.83**	**13.47**
ALD	**Thickness XRR (Å)**	**54.65**	**90.58**	**132.6**	**155.35**	**325.84**
	EWF (eV)	**4.46**	**4.61**		**4.75**	**4.75**
	Stress (dyne/cm^2)	**-5.59 x 10^{10}**	**-2.38 x 10^{10}**	**-8.93 x 10^{09}**	**-4.09 x 10^{09}**	**9.50 x 10^{09}**
	Resistivity (μΩ-cm)	**727.37**	**161.3**	**95.93**	**76.68**	**28.78**
	Density (g/cm^3)	**4.87**	**5.03**	**5.02**	**5.03**	**5.02**
	Roughness (Å)	**12.5**	**13**	**15**	**16.3**	**24.87**

ALD TiN deposed on various (3nm) dielectrics	**TiN Cycles (1.1 Ångstrom/cycle)**						
	5	**10**	**20**	**50**	**100**	**200**	**400**
SiO_2	**4.23**	**4.24**	**4.30**	**X**	**4.45**	**X**	**4.67**
$HfSi_xO_y$	**4.38**	**4.41**	**4.46**	**4.52**	**4.62**	**4.76**	**4.71**
HfO_x	**4.31**	**4.32**	**4.38**	**4.53**	**4.58**	**4.72**	**4.65**

Table 3.1: TiN Metal Gate EWF values: varying metal thickness, deposition process, and dielectric

Data obtained for EWF and gate stack evolution from electrical and materials analyses are reported in Table 3.1. Importantly, MG EWF increases with metal nitride thickness independent of the dielectric used [6, 133]. An EWF tuning range of

approximately +/-.2eV around mid-gap has been achieved for ALD TiN on $HfSi_xO_y$, HfO_x, and SiO_2. The EWF tuning achieved with PVD and CVD TiN on HfO_x is also promising. Though some reported PVD and CVD TiN EWF values are more suitable for p-type tuning, thinner films are expected to achieve an EWF tuning trend similar to that observed for ALD TiN on $HfSi_xO_y$, HfO_x, and SiO_2.

3.2.2.1 Preliminary Observations: TiN Thickness EWF Modulation

EWF is observed to vary with TiN thickness and dielectric material [60, 133, 135] in Table 3.1. TiN gates deposited on $HfSi_xO_y$ tend to have a higher EWF and related higher V_{th}, as described in Table 3.1 and illustrated in Figures 3.1 and 3.2, than similarly fabricated electrodes of the same TiN thickness on either HfO_2 or SiO_2 [133, 139, 150]. The higher EWF and V_{th} of the gate stacks incorporating nitrided $HfSi_xO_y$ result from the material's higher dielectric constant and greater stability [139]. HfO_x has a more reactive surface bonding structure at the substrate and MG interfaces which may affect interface states and influence the final EWF values achieved [139, 151].

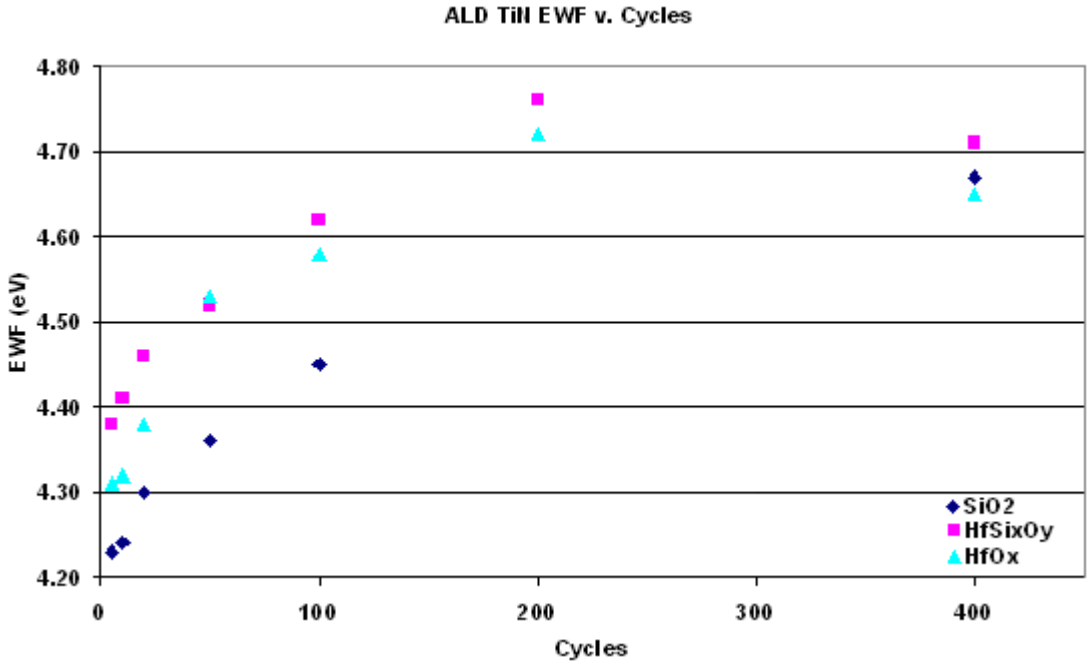


Figure 3.1: EWF variation with thickness and dielectric [as partially reported in 133]

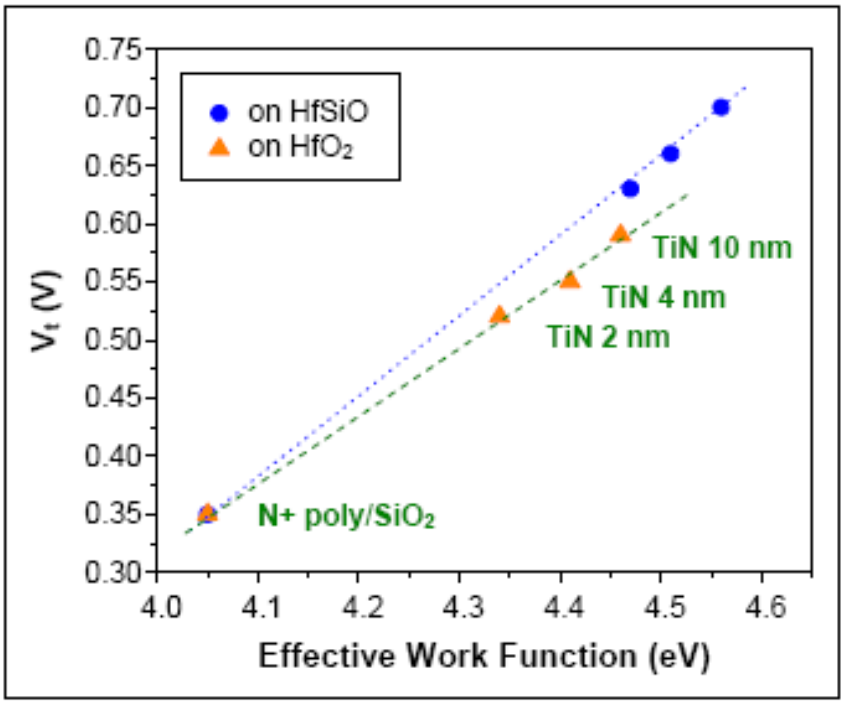


Figure 3.2: Comparison: V_{th} v. EWF (n-MOSFET) for TiN_x (2 -10nm thick) on HfO_x and $HfSi_xO_y$ dielectrics [as reported in 133]

Closer inspection of the relationship between EWF, thickness, and dielectric in Figure 3.3 indicates that the EWF between dielectrics maintain a constant ratio difference at each thickness until TiN_x reaches 5nm [133]. As thickness increases beyond 5nm, the EWF ratio between SiO_2 and $HfSi_xO_y$ remains relatively constant while that between $HfSi_xO_y$ and HfO_x decreases by approximately half after the two EWF values almost converge at 5nm. The EWF values continue to increase at the new ratio with respect to one another beyond 5nm until all the EWF values somewhat plateau and, in the case of the stacks incorporating High-κ dielectrics, slightly drop at 40nm.

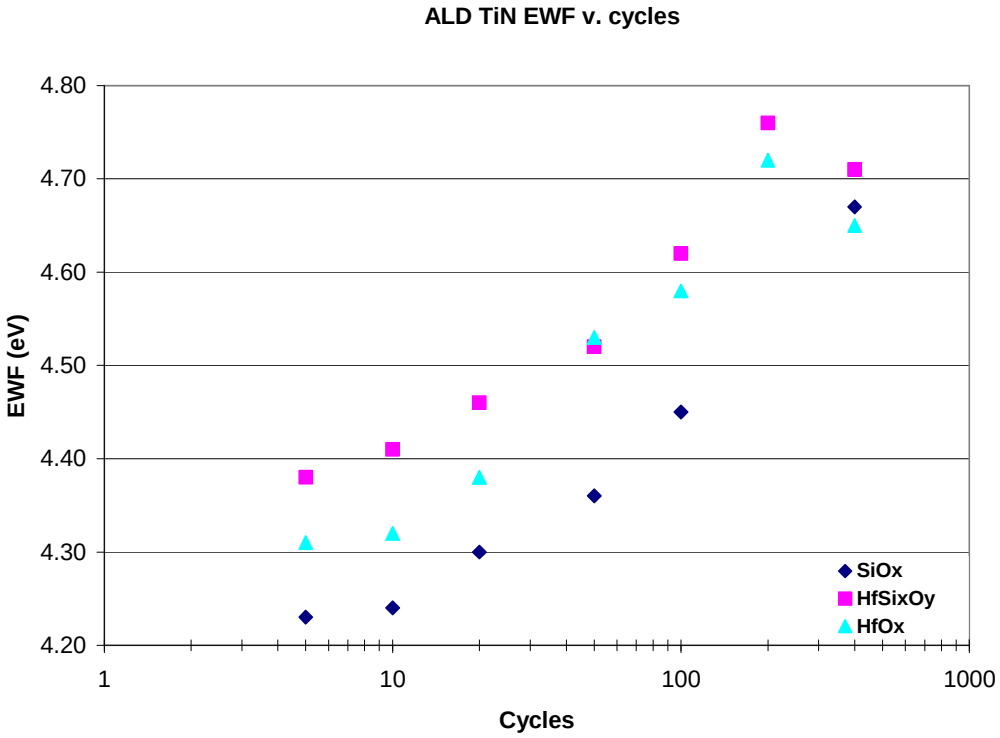


Figure 3.3: Log scale rendering of TiN EWF tuning on various dielectrics [as partially reported in 133]

Similarities in stability account for the consistency between SiO_2 and nitrided $HfSi_xO_y$ EWF ratio [139]. HfO_x is less stable [139, 152]; interactions at the HfO_x interfaces may account for the change in EWF ratio between $HfSi_xO_y$ and HfO_x at 5nm [139, 144, 152]. Changes in TiN crystallinity and composition at 5nm may promote diffusion which may affect the HfO_x interfaces more greatly than those of $HfSi_xO_y$ and SiO_2 [139, 152].

TiN EWF saturation begins across the dielectrics at 20nm. An EWF value of ~4.68eV for 20nm thick TiN on SiO_2 is reported [133]. The EWF for 40nm thick TiN on High-κ dielectrics drops slightly while that for TiN on SiO_2 essentially remains constant. The EWF decrease associated with 40nm TiN on High-κ dielectrics may be related to changes in the TiN crystal orientation and grain size between 20 and 40nm TiN [67, 70] which may influence diffusion during RTA or to the stability of the 1:1 Ti:N ratio at the

greater thickness [144]. The EWF ratio between $HfSi_xO_y$ and HfO_x remains constant between 10 and 40nm.

Generally EWF is observed in Table 3.1 to increase as stress in the substrate becomes less compressive, resistivity decreases, and roughness increases. Figures 3.4, 3.5 and 3.6 illustrate the relationship between stress and EWF, roughness and EWF, and density and EWF, respectively. Density tends to decrease somewhat with increasing EWF and thickness for PVD and CVD TiN while increasing slightly for ALD TiN. Density remains relatively constant as thickness and EWF increase. Roughness and strain evolution do not correlate well with EWF saturation at greater TiN thicknesses. Most probably bulk rather than interface properties of the film determine the EWF achieved at these greater thicknesses [133, 151].

Figure 3.4: Stress and EWF v. thickness for ALD, CVD, and PVD TiN on HfO_x

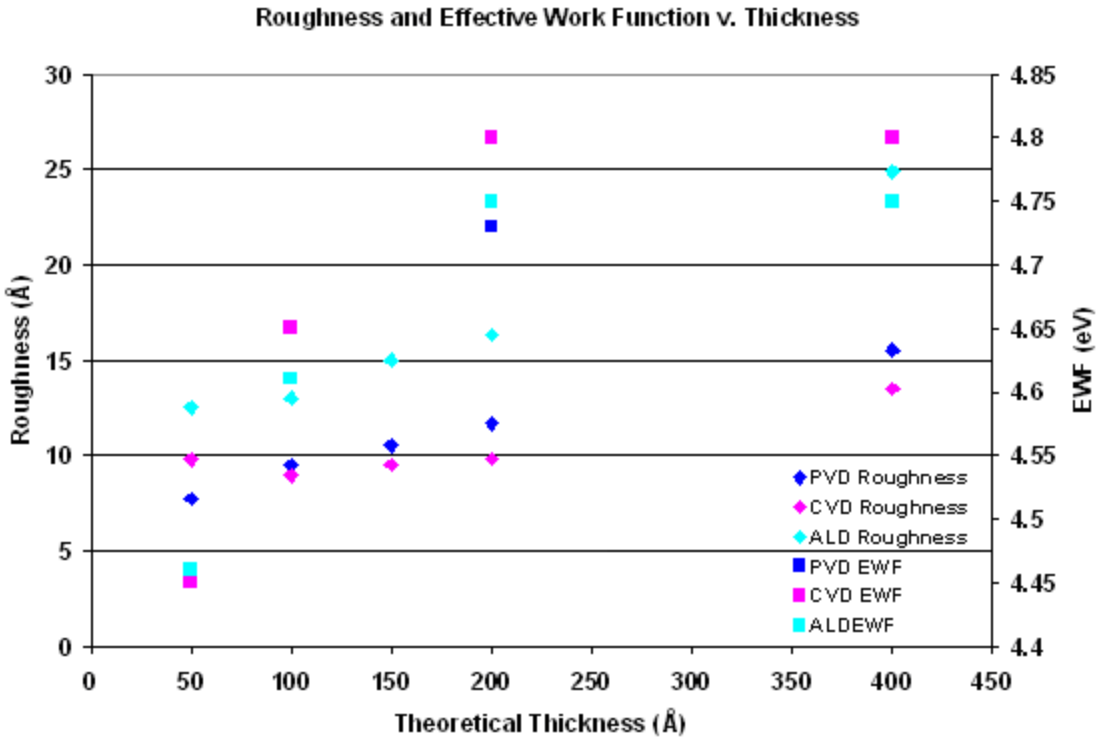


Figure 3.5: Roughness and EWF v. thickness for ALD, CVD, and PVD TiN on HfO_x

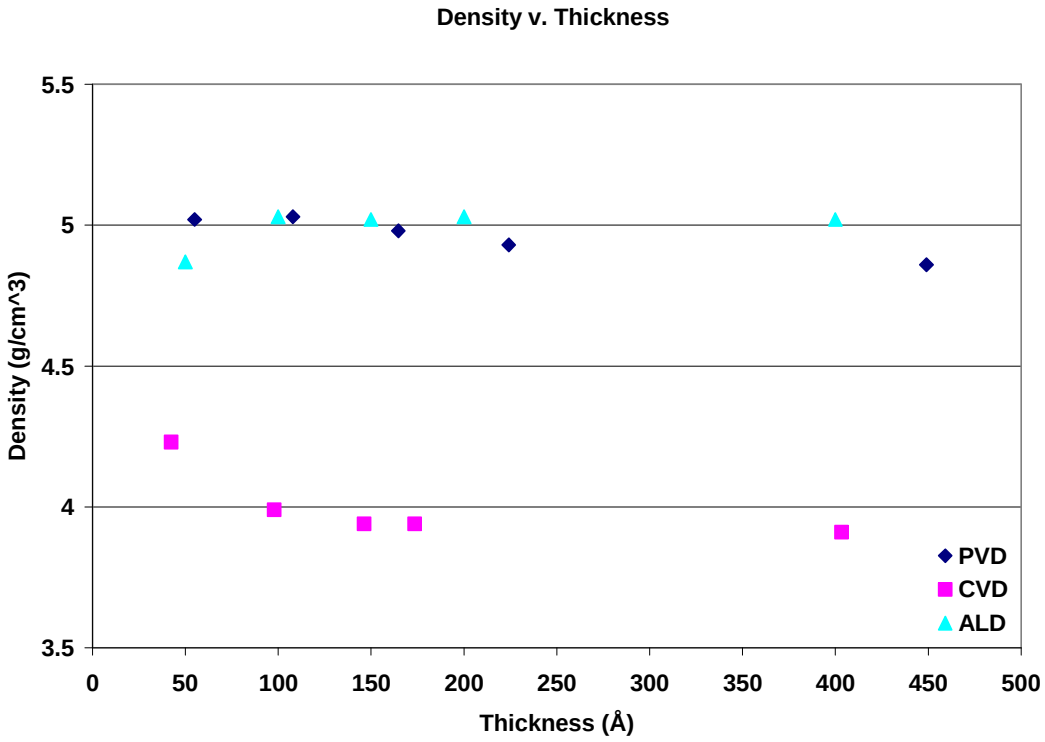


Figure 3.6: Density v. thickness for ALD, CVD, and PVD TiN on HfO_x

The trends observed are relatively weak and suggest strain, resistivity, roughness, and density are concomitant to EWF modulation rather than central to the modulation mechanism. The results suggest MG and interface composition and structure may be essential elements of the TiN thickness tuning mechanism which may explain EWF evolution in stacks utilizing the same dielectric and differences in EWF values observed between stacks integrating different dielectrics [133, 139, 152].

Strain and roughness at the MG/High-κ interface have been proposed to explain EWF evolution with TiN thickness [133]. The strain investigation reported herein was conducted with respect to the substrate. Although the method applied to measure and analyze strain within the stack was designed to capture strain at each of the interfaces, it is possible changes in strain within the various films constituting the stack may mask a large increase in strain at the MG/High-κ interface [153]. The strain data reported here is not wholly inconsistent with strain having a more important role in EWF thickness modulation than observed herein. The data reported herein suggest that roughness and density may have a less important role in EWF thickness tuning than previously reported [133].

3.2.2.2 TiN EWF Thickness Tuning Mechanism: Electrical Data Analysis

EWF tuning and saturation have been explained to result from transformation of the MG/dielectric interface during high temperature annealing caused by thickness dependent differences in metal gate crystalline structure [60, 133, 135]. Choi has established the existence of three key thickness regimes for TiN: (I) below 2nm, (II) between 2 and 20nm, and (III) greater than 20nm in thickness [133].

Regime I is characterized by a sharp increase in EWF explained to result from the coexistence of TiN islands and n+-poly-Si at the dielectric/metal gate interface. The EWF increases from that of the n+-poly-Si to that of nitrogen (N) deficient TiN as the

islands become contiguous and begin to form a nearly continuous film at 2nm. The N deficiency causes the EWF in this regime to be low (Ti metal-like (3.9 eV)) [133, 148].

The difference in EWF between dielectrics and the uniformity in the EWF rate of increase after a continuous film is achieved in Regime II (2 - 20nm) are attributed to the unique atomic arrangement at the interface for each dielectric and bulk related properties of the TiN film, respectively. EWF evolution is much slower in Regime II than in Regime I. Thickness sensitive bulk properties (diffusion profiles/stress) regulate EWF tuning in Regime II. Beyond 20nm (Regime III) TiN bulk properties dominate and the metal/dielectric interface becomes less central to the EWF obtained. The EWF values in Regime III begin to saturate and converge to a single constant value for each of the stack types [133, 135].

The EWF convergence of $HfSi_xO_y$ and HfO_x at 5nm TiN thickness as well as the peak and subsequent decrease in EWF noted at 20 and 40nm, respectively, indicate that the mechanisms regulating EWF tuning undergo important changes at these thicknesses for HfO_x based high-k dielectrics. Data previously reported for 5 and 30nm TiN films deposited on HfO_2 indicate that 5nm thick films have low stress, a relatively smooth metal/dielectric interface and a relatively low interface trap density compared to 30nm films [60, 133]. The change in TiN dielectric coverage from discontinuous (<2nm) to thin, contiguous or continuous and regular (2 - 20nm) and then to relatively thick and rough (>20nm) may be crucial to the trap density at the metal/dielectric interface and may account for the EWF tuning trends observed [6, 137, 140]. Interface trap density differs with metal gate deposition process and may be one reason EWF values differ between TiN deposition methods [154].

Interface bonds, strain within those bonds, dielectric specific diffusion and other characteristics related to bonding/strain may account for the difference in EWF values

obtained for TiN on varying dielectrics despite the general trend remaining relatively constant independent of the dielectric used [60, 135, 155 at p. 81]. Hf-O bonding characteristics cause greater intermixing and diffusion in hafnium based dielectrics than in SiO_2 [135]. Evolution of the metal film structure may trigger Hf or O to diffuse toward the high-κ/substrate interface or into the metal gate [60, 133, 135, 142]. Si may move from the substrate into the High-κ [135, 156, 158].

A shift in the V_{fb} v. EOT slope for 20nm TiN on $HfSi_xO_y$ in Figure 3.7 may indicate that the peak EWF values achieved result from a change in the fixed charge at the H-κ/substrate interface [67]. Diffusion toward/away from the interface may be triggered by changes to the metal gate crystalline structure and the MG/High-κ interface [135]. EWF remains stable on SiO_2 between 20 and 40nm compared to the decrease observed for High-κ electrodes. The difference may indicate that Hf or O diffusion occurs due to differences in bonding strength when compared to SiO_2 [6, 60, 135].

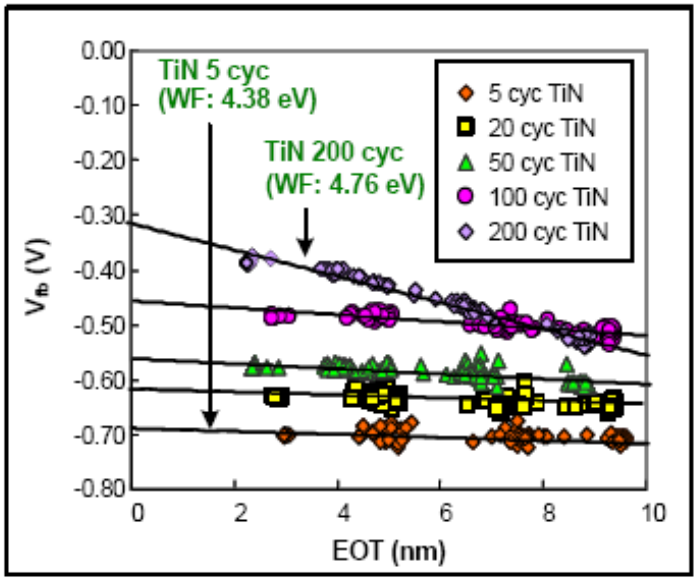


Figure 3.7: V_{fb} v. EOT for TiN (varying thickness) on $HfSi_xO_y$ [as reported in 133]

For PVD, ALD, and CVD TiN, Table I and Figure 3.8 indicate that the EWF does not differ greatly across metal deposition processes. PVD and ALD deposited TiN

have an especially similar EWF. The uniformity primarily results from optimization of the deposition processes. Actual thickness differs greatly from theoretical thickness between deposition methods beyond 100Å. This result may partially explain the small differences in EWF observed at the various thicknesses.

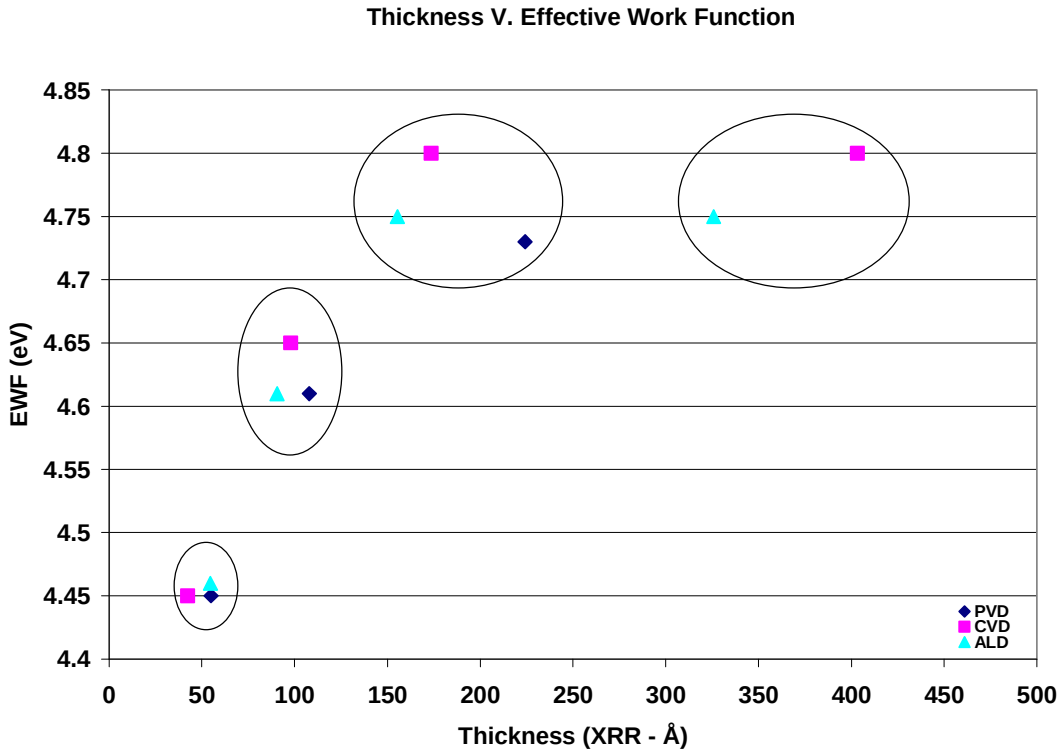


Figure 3.8: EWF v. thickness, effect of deposition method noting difference between actual and attempted thickness

The EWF ratio observed at each thickness remain constant between the different deposition methods. In Figure 3.8, all of the various deposition methods produce a saturated EWF without the dip in EWF observed between the 20 and 40nm TiN ALD samples receiving a 5 second rather than 10 second anneal. This result may be related to structural stabilization caused by the longer anneal healing pinholes and other anomalies within the structure [155 at p. 81].

3.2.2.3 TiN EWF Thickness Tuning Mechanism: Materials Analysis

In order to understand the metal gate thickness dependent EWF tuning behavior observed in PVD, ALD, and CVD TiN on HfO_x and ALD TiN on $HfSi_xO_y$, HfO_x, and SiO_2, materials analysis of the gate stacks was conducted to determine the stacks' crystallinity, crystal orientation, density, and composition. The data obtained suggest crystallinity and preferred crystal orientation determine EWF by influencing diffusion and bonding within the stack [133, 144, 157]. Thickness determined changes in the ratio of Ti to N at the MG/High-κ interface are also central to the EWF tuning achieved.

XRD analysis of the various stacks was used to determine crystallinity, orientation, and grain size [159]. CVD, PVD, and ALD XRD data in Figure 3.9 provide insight into preferential crystalline orientation as well as general information regarding grain size and stress for thicknesses within Regimes II (5 and 10nm) and III (40nm) [6, 133, 146, 151, 160-164].

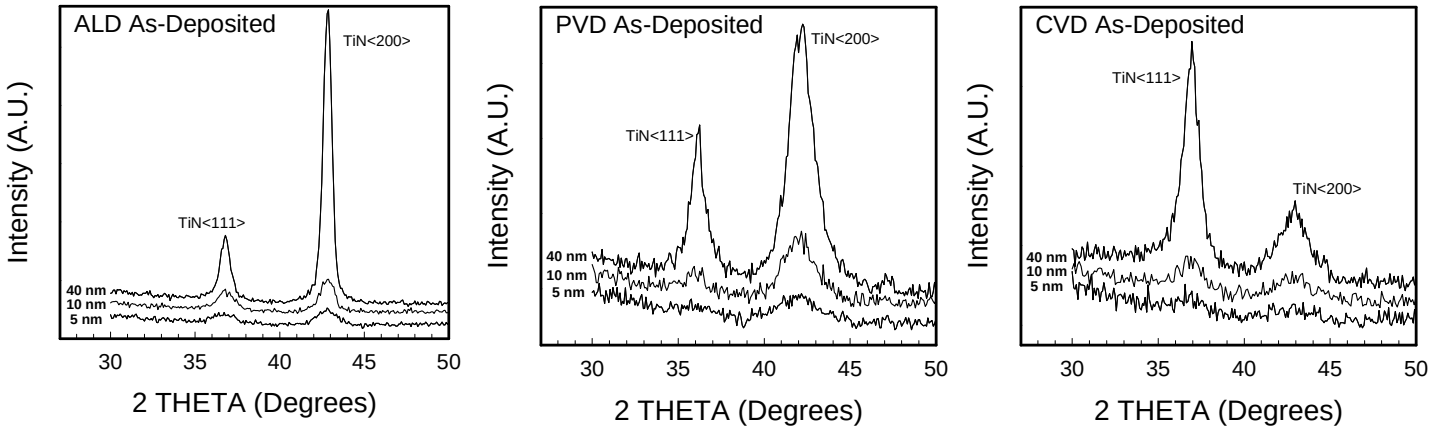


Figure 3.9: ALD, PVD, and CVD TiN XRD at 5, 10, and 40nm TiN thickness on 2nm HfO_x

The XRD data in Figure 3.9 indicates that 5nm TiN films are largely amorphous, though (111) and (200) oriented crystallization is apparent in all the samples. The broad peak between 20-25 degrees in Figure 3.10 also suggests that films between 2nm and 5nm are almost completely amorphous. Amorphous films tend to have better barrier

characteristics which may explain the relative consistency in the EWF behavior between deposition methods and dielectric used in regime II [133, 146, 160, 164, 165].

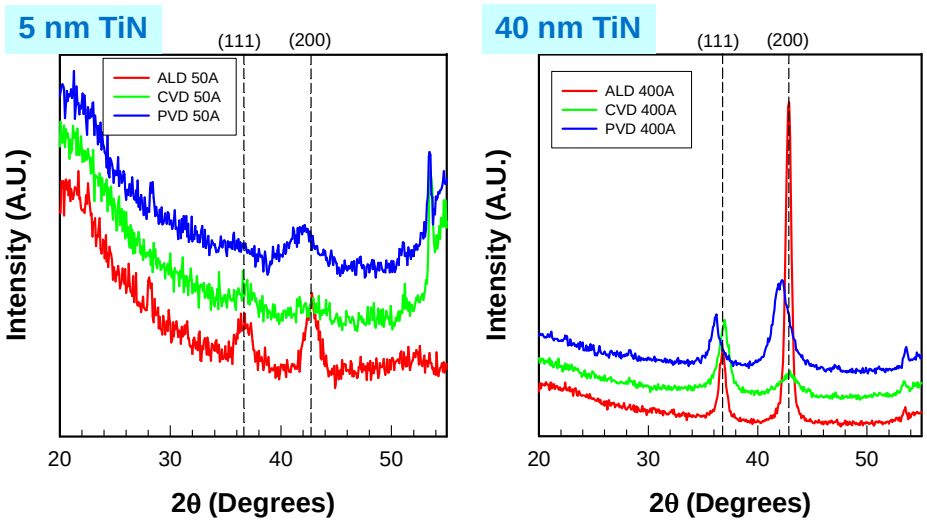


Figure 3.10: Comparison: ALD, CVD, and PVD TiN at 5 and 40nm

The films exhibit greater crystallinity above 5nm and well into regime III; increased diffusion through the stack may occur as a result, causing the EWF to increase [67, 139, 144, 165]. Figure 3.7 illustrates an increase in substrate/dielectric interface charge at 40nm thickness which may result from diffusion through the more crystalline TiN. The appearance of crystal formation and related diffusion may be one reason changes in the EWF ratio begin to appear at a TiN thickness of 5nm, as illustrated in Figure 3.3.

Peak heights and widths in Figures 3.9 and 3.10 indicate that ALD TiN has the largest crystal size and greatest crystallinity, respectively, of the three deposition methods at 40nm. This increased crystallinity may lead to greater diffusion along the grain boundaries and an increase in EWF through diffusion related changes at the High-κ interfaces and within the bulk films [60, 133, 142, 159, 161, 164, 165]. Differences in the dielectric composition and stability may result in differences in diffusion and film

structure/intermixing which would further explain the EWF changes observed in Figure 3.3.

ALD, PVD, and CVD TiN have similar EWF values while the films are relatively thin and either relatively amorphous or competition between (200) and (111) orientations exists. In thicker films having an established preferred orientation, EWF values for (200) preferentially oriented ALD and PVD TiN remain similar while (111) oriented CVD TiN exhibits a higher EWF at the same TiN thickness. These results emphasize the importance of crystal orientation to EWF thickness tuning in TiN. The similarity in density between PVD and ALD TiN displayed in Table 3.1 and Figure 3.6 most probably arises from their similar preferential (200) crystalline structure. The lower density in CVD TiN indicates that it has more loosely packed grains which may promote diffusion and a comparatively higher EWF than ALD and PVD TiN.

(200) preferential crystallization for ALD and PVD TiN and (111) preferential crystallization in CVD films become apparent at 5nm in Figures 3.9 and 3.10; however, the (111) and (200) crystal orientations are still relatively equal in distribution. Competition between (111) and (200) crystal growth illustrated in Figure 3.9 may cause high compressive stress within the relatively thin films. An increase in film thickness to 10nm causes all three films displayed in Figure 3.9 to express definite preferential (111) (CVD) or (200) (ALD and PVD) orientation and a concomitant decrease in compressive stress as illustrated in Figure 3.4 [70, 133, 144]. At 40nm, only PVD TiN, which has a definite (200) preferential crystal orientation and a much larger expression of the (111) orientation than the CVD and ALD films, retains compressive stress. CVD ((111) preferential) and ALD ((200) preferential) TiN gain modestly tensile stress at 40nm [6, 42, 155 at p. 81, 160, 165].

The XRD data in Figures 3.9 and 3.10 and the strain data in Figure 3.5 indicate that competition between preferred crystal orientations may be more important to EWF

thickness tuning than grain size and strain [67, 144]. This competition may also result in the decrease in compressive strain observed as TiN thickness increases. Highly amorphous TiN films have compressive stress. The slight shift in XRD peak location for 40nm PVD TiN shown in Figure 3.10 indicates an additional strain related to the deposition process may exist [6, 135, 137, 140, 162]. As crystallization begins, compressive strain within the films relaxes; increased crystallization in a preferred single crystal orientation, independent of grain size, further relaxes strain and may finally change the strain orientation from compressive to tensile. Whether competition between crystal orientation results from the additional compressive strain in the PVD TiN film or acts to maintain the strain, the presence of two competing crystal orientations is indicative of compressive strain within the gate stack [146, 160-164].

STM-EELS/EDX analysis of ALD TiN films on HfO_x after poly-Si removal displayed in Figure 3.11 indicates that film composition is also central to EWF TiN thickness tuning. The MG/dielectric interface at .5nm consists of TiN islands interspersed with poly-Si on the dielectric surface [133, 148, 155 at p. 31]. EELS analysis reveals a gate stack which is highly intermixed at the dielectric/metal gate interface. The metal gate is devoid of N and there is almost a 1:1 Ti:O relationship. These results support the claim that the EWF is Ti metal like in Regime I and that the proximity of the poly-Si cap to the dielectric may account for the low EWF and relatively sharp EWF evolution observed in this region, possibly because the poly-Si acts as a conduit for diffusion [133]. There is a large amount of interaction between materials at the High-κ interfaces at .5, 2, and 10nm.

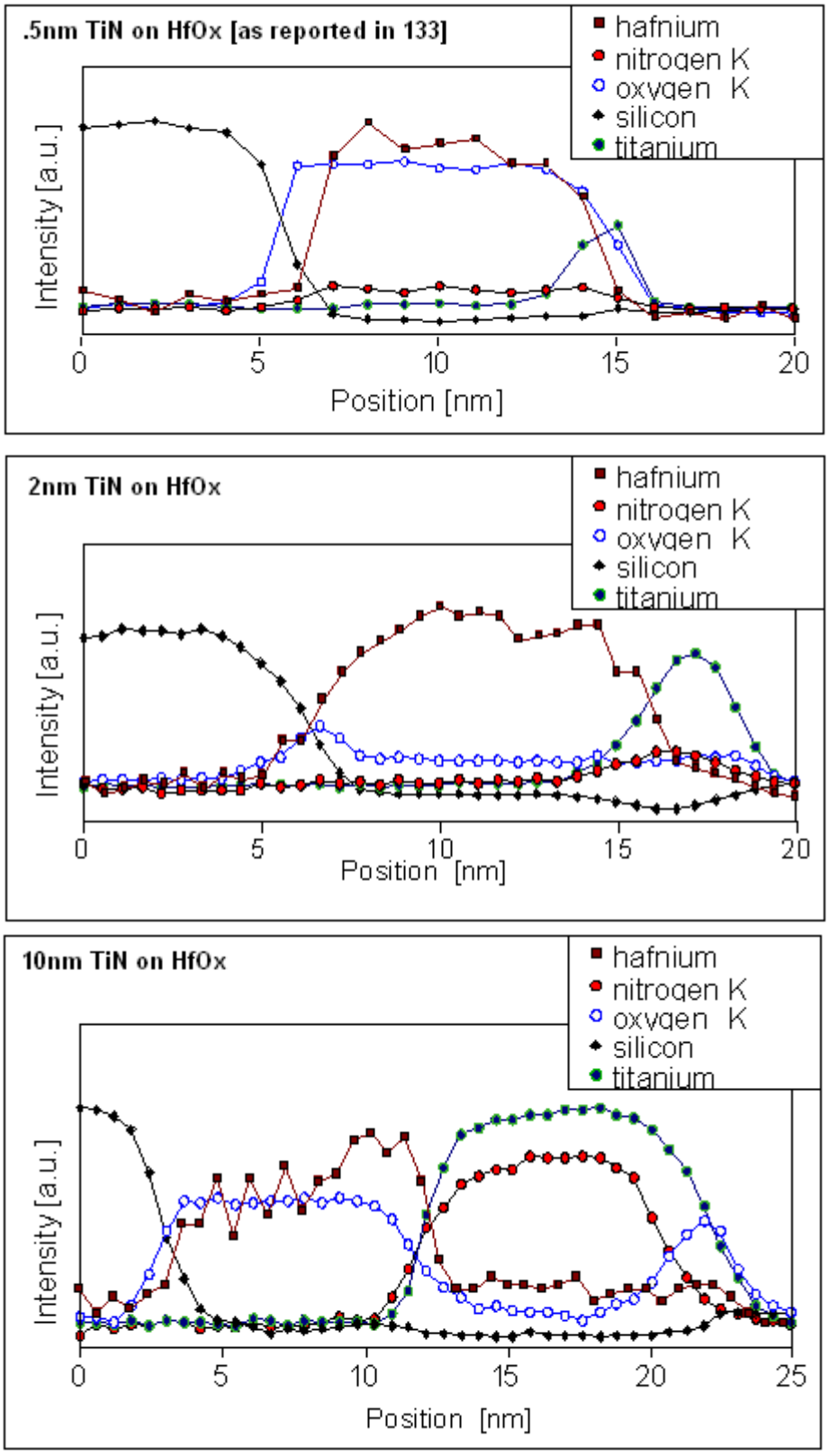


Figure 3.11: EELS Data for .5, 2, and 10nm TiN on 3nm HfO_x

At 2nm, EELS analysis indicates a thin, Ti rich TiN_x film has evolved and completely separates the poly-Si from the dielectric. Amorphous TiN_x would tend to prevent a great deal of diffusion into or out of the stack. The 2nm film is still Ti rich; however, there is more N present within this film than in the .5nm film. There is much less intermixing within the film and the oxygen content is lower both in the dielectric and in the MG. An oxygen build up does exist at the substrate/dielectric interface, though there is no SiO_x film development. The observed results may be due to the amorphous TiN_x film which has developed. The slower increase in EWF in Regime II may be due to reduced diffusion within the stack and to an increase with thickness of the N content in the TiN_x. The interface between the TiN_x and the dielectric is also more abrupt and relatively smooth indicating stability and supporting the slow EWF increase with thickness [133].

10nm TiN_x films show an almost 1:1 O:Hf ratio in the dielectric similar to that of the .5nm films. Unlike the .5nm films, the 10nm films do not exhibit SiO_x formation between the substrate and dielectric. The thicker film has a Ti:N ratio of ~ 1:1. A larger amount of Hf and O exist within the 10nm metal gate than the .5nm gate; like the .5nm films, the outer edge of the TiN film is oxygen rich and N deficient.

TiN has high thermal stability and low resistivity [67]. The decrease in resistivity with thickness recorded in Table 3.1 is in accord with the EELS data in Figure 3.11 indicating the Ti:N ratio approaches 1:1 as thickness increases. The data supports the conclusion that the EWF is N concentration dependent [67, 70]; as N content increases, the EWF increases from a value similar to that of pure Ti to that of 1:1 Ti:N. Once 1:1 TiN has been achieved, the EWF saturates. TiN_x becomes more stable as it approaches TiN [144]; in Figure 3.11, the MG/High-κ interface becomes sharper as N content in the metal increases with thickness.

Similarities between O distribution between the 10nm and .5nm TiN_x thicknesses may partially explain the similarity in EWF ratio for $HfSiO_x$ and HfO_x discussed in section 3.2.1, above. While the higher EWF is tied to the greater amount of N in the metal gate, the higher O concentration in the dielectric and in the metal gate outer edge as well as the larger amount of Hf in the metal gate may indicate similar diffusion and similar interface structure at the interfaces for both thicknesses. The XRD analysis indicates that there is definite crystallinity at 10nm thickness; diffusion along the grain boundaries may account for the distributions observed in the EELS data.

SIMS analysis in Figure 3.12 of TiN on $HfSiO_x$ also supports diffusion as important to EWF. EWF saturation at higher TiN thickness results from a more stable chemical structure. Between 5 and 20nm TiN, the concentration of carbon (C) contamination, O, and Si within the films decreases significantly while Chlorine (Cl) contamination increases. Increasing Si tends to drive EWF to midgap EWF [147]. The large drop in Si between thicknesses indicates that Si concentration is important to EWF evolution with thickness. Greater Si in the metal gate film seems to lead to lower EWF. Less O in the metal film also seems to trigger an EWF increase.

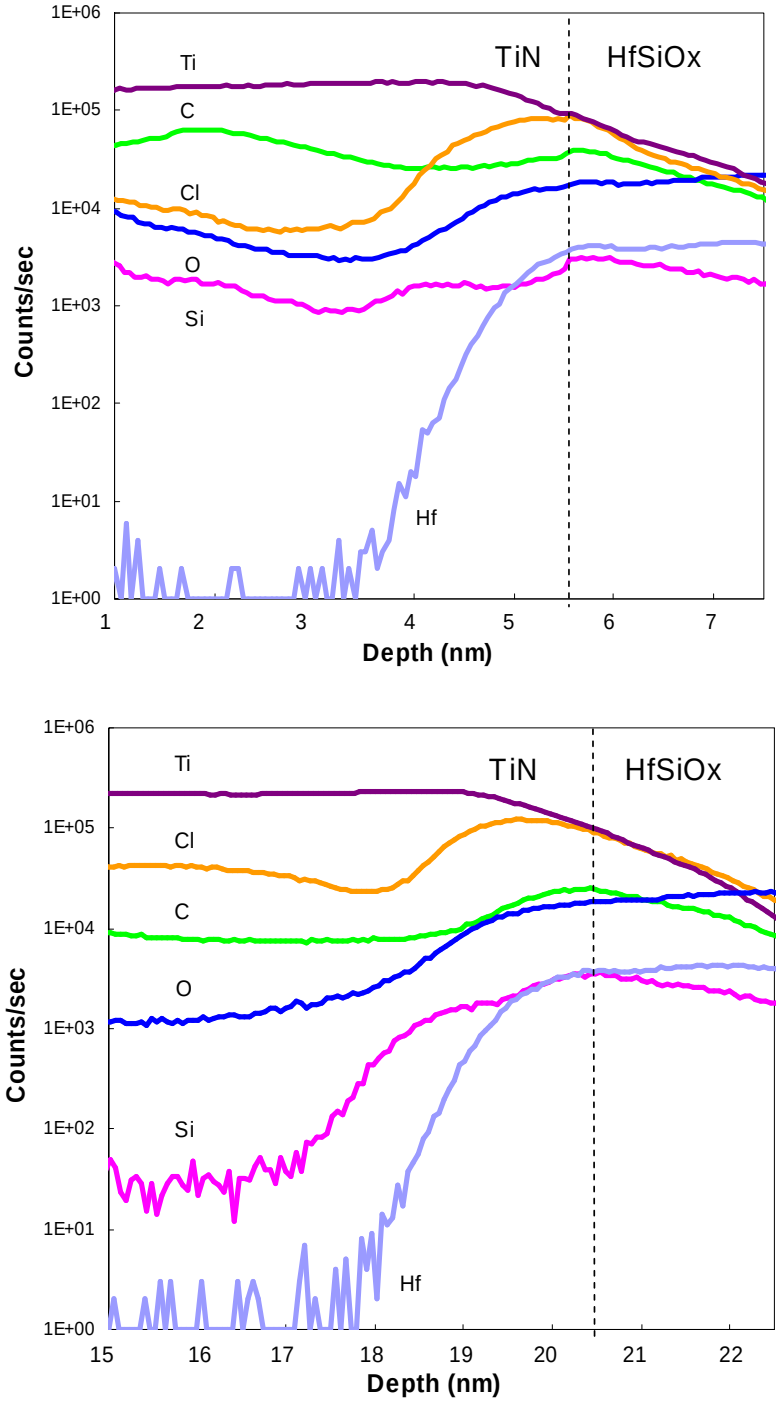


Figure 3.12: SIMS of ALD TiN_x on $HfSiO_x$ at 5 and 20nm, respectively

At the MG/High-κ interface, the Cl, O, and Si values remain relatively constant between 5 and 20nm thick TiN; C is the only component the concentration of which

decreases greatly. Film, rather than interface, composition plays the central role in EWF tuning for thicker films. Stability in materials concentrations at 20nm may result in EWF saturation [133]. RBS data not included herein confirms the thickness related evolution of Cl, O, N, and Si content within the films observed in the SIMS data.

3.3 CONCLUSIONS

TiN thickness dependent EWF tuning is influenced by preferred Ti:N ratio, crystal orientation, film crystallinity, and diffusion through the stack. These characteristics vary with dielectric and gate deposition method. Interdiffusion and atomic affinities will determine how atoms will move through the stack and where they will finally congregate/bond.

Very thin films (<2nm) comprise TiN_x islands separated by the poly-Si cap on the dielectric interface [133]. Materials analysis indicates the stack experiences extensive interdiffusion. The metal gate is oxidized and Ti rich. These factors produce a low EWF similar to poly-Si for very thin films and a value approaching Ti EWF for thicker films.

Films between 2 and 20nm have a metal gate/dielectric interface which is relatively abrupt. At the lower end (5nm) the metal gate is still Ti rich, accounting for its lower EWF when compared to 20nm TiN_x. The metal gate is also relatively amorphous at 5nm which may explain the more moderate EWF tuning in regime II. There is probably less diffusion through the metal gate than that experienced at <2nm and >20nm. An increase in crystallinity within the metal gate structure becomes visible at 10nm. This crystallinity may allow greater diffusion through the metal gate and result in, at greater thicknesses (200Å and 400Å) greater stability in the EWF values as equilibrium is reached within the stack. Cl in the metal gate at 40nm has most likely been incorporated during the deposition process. Whether it has some independent effect on EWF has not been established; however the Cl is known to contribute to roughness, as observed here.

Bulk TiN behavior is established as films thicken. EWF increases to TiN EWF (mid-gap value) with increasing thickness as the film becomes more amorphous during the development of Regime II. As regime III begins to develop, EWF tuning above mid-gap probably results due to diffusion regaining the dominance held in regime I. The TiN structure, the High-κ substrate interface, and the dielectric/metal gate interface are all affected and play integral roles in the final EWF achieved.

CHAPTER 4

n-MOS TO p-MOS THICKNESS TUNABLE METAL GATE/HIGH-κ ELECTRODE FinFETS UTILIZING AN INNOVATIVE FABRICATION PROCESS

4.1 INTRODUCTION

Metal gate/High-κ dielectric (MG/High-κ) stacks are the leading solution being developed to enhance device scalability and performance beyond the 32nm dimension [13, 20, 44]. Conventional polysilicon (poly-Si)/silicon oxynitride (SiO_xN_y) gate stacks, though well understood and simple to fabricate, experience excessive gate leakage at highly scaled dimensions and are not considered viable options as device dimensions continue to shrink [3, 13, 14, 166]. Integrating MG/High-κ stack technology into existing processes has required major innovation and investment [5, 7, 20. 38, 44, 167, 168].

After over 15 years of development, MG/High-κ devices have only recently begun entering the market. Intel introduced the first commercially viable MG/High-κ devices (45nm technology) in 2008; Intel, IBM and other microelectronics technology leaders expect to introduce 32nm technology MG/High-κ devices in late 2009 [17, 52]. Dual metal gate (DMG) fabrication is the industry standard for MG/High-κ stacks [3, 13, 28, 66, 107, 169]. The process is complex and costly compared to the techniques utilized in conventional gate stack fabrication [112, 165].

DMG is required for MG/High-κ fabrication because the n-MOS to p-MOS compatible tuning range required for bulk devices (~4.0eV to ~5.0eV) cannot be reliably achieved by any of the metal gate materials investigated to date [3, 13, 20, 21, 170]. In dual metal gate fabrication, a first gate metal is deposited and then selectively etched to expose the High-κ surface in areas intended to have opposite compatibility. A second metal is then deposited in these exposed areas and the remaining fabrication steps

completed. Additional lithography and etch steps must be included in conventional fabrication processes to independently deposit the two metal gates. Compatible etch chemistries must be established between the two metals to be used; the first metal etch may affect the High-κ surface and cause reliability issues for the second metal deposited devices [2, 7, 109, 111, 112, 149, 165, 169].

The research herein develops an innovative single metal gate fabrication method which is 40% less complex than DMG. Single metal n-MOS to p-MOS tuning is achieved by fabricating devices on ultra thin body silicon on insulator (UTB-SOI) substrates. Depleted UTB-SOI device channels receive little to no implantation; as a result, the n-MOS to p-MOS tuning range required for UTB-SOI structures is only one fourth of the Si band gap (~ 4.35eV to ~ 4.9eV), a more reasonable range for single metal tuning [13, 20, 107]. Development of compatible DMG etch chemistry is no longer required because the same fabrication method may be used for both the n-MOS and p-MOS single metal gates.

The titanium nitride (TiN) thickness controlled effective work function (EWF) tuning mechanisms presented in Chapter 3, have been engineered herein to further simplify gate stack fabrication. Etch back of thick (p-MOS compatible) TiN to a thinner (n-MOS) compatible film eliminates many of the additional fabrication steps required for DMG second metal electrode fabrication and protects the dielectric surface from etch related damage.

The fabrication method introduced here is proven to be effective for 3-dimensional (3-D) fin field effect transistor (FinFET) fabrication. FinFETs are considered the most promising device structures for 22nm technology and beyond as a result of the excellent control of short channel effects (SCEs) the structure affords [13, 20, 43, 171].

4.2 Fabrication and Preliminary Threshold Voltage (V_{th}) Analyses of As Deposited Variable Thickness TiN Metal Gates

Initial measurements were taken on FinFETs fabricated with 30Å, 100Å and 200 Å as deposited TiN. FinFET devices were fabricated on (100) SOI (90nm Si on 125nm buried oxide), using 193nm 45° rotational lithography to produce (001)[010] channels along the (110) Si planes and Hafnium (Hf) terminated surface preparation of the channel areas prior to dielectric deposition. The resulting fins were 20nm wide and 80nm high with a 4:1 aspect ratio. Each Multigate FET (MUGFET) consists of 20 fins. The fins were deposited with 2nm thick hafnium silicate ($HfSi_xO_y$) and the dielectric nitrided. TiN metal gates were deposited on the dielectric at thicknesses of 30Å, 100Å, and 200Å. Both the dielectric and metal were atomic layer deposited (ALD) at 1.1Å/cycle. A poly-Si capping layer was deposited over the MG/High-κ stacks. To control SCEs, a lightly doped drain (LDD) region was formed for the n-FET devices. The structures received a low temperature forming gas anneal (FGA), as well [112, 134, 137, 140].

V_{th} comparison of as deposited 30Å, 100Å, and 200Å thick TiN for n-MOS and p-MOS FinFETs in Figure 4.1 indicates that it is possible to achieve fairly symmetric, tunable n-MOS and p-MOS compatible V_{th} through TiN thickness engineering [20]. As expected, the 30 Å TiN (thin) causes V_{th} to decrease for n-MOS devices while V_{th} for p-MOS devices at 200Å is observed to increase [5, 7, 133].

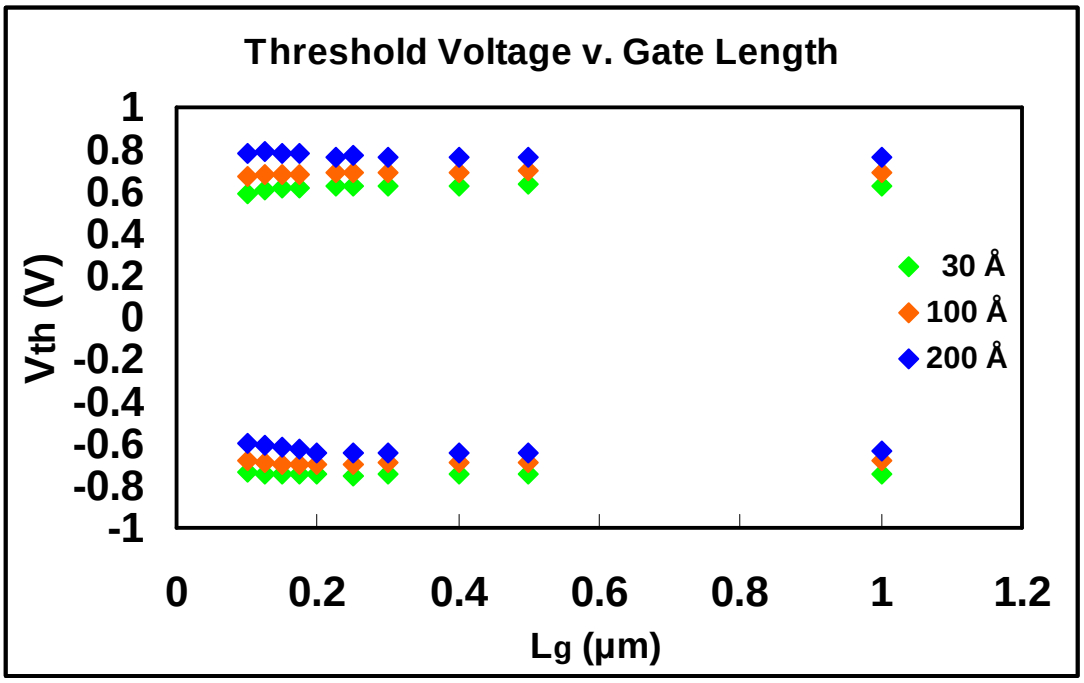


Figure 4.1: V_{th} v. gate length (L_g) for as deposited 30Å (n-MOS), 100Å (midgap), and 200Å (p-MOS) appropriate TiN gate FinFETs

Though a single metal gate reduces etch compatibility issues, DMG-like fabrication is required to independently deposit the two separate metal thicknesses [20]; the fabrication process remains costly and complex as a result. The metal etch back method introduced below is the culmination of the research herein and serves as a simple, cost effective alternative for MG/High-κ gate fabrication.

4.3 SIMPLIFIED ETCH BACK FABRICATION METHOD AND ELECTRICAL RESPONSE ANALYSIS

Single metal/High-κ gates retaining MG/dielectric interface integrity and electrically stable response may be simply and cost effectively fabricated by depositing a uniform, p-MOS appropriate TiN thickness layer and selectively etching back the TiN of n-MOS designated structures to a thickness expected to achieve n-MOS appropriate EWF. Since the first metal deposited is not completely etched away, the dielectric is never exposed to the first metal etchant and the dielectric surface remains consistent between n-MOS and p-MOS devices [112, 165, 172]. Fewer steps are necessary to

complete the fabrication process because the initial metal deposited does not need to be selectively removed from the dielectric surface and a second metal deposition is no longer required.

4.3.1 Fabrication

The etch back fabrication method introduced herein requires deposition of a hardmask on the metal gate material. The hard mask is patterned using conventional lithography and then dry etched to expose the regions intended to be n-MOS. The exposed TiN receives a controlled wet etch to a thinner, n-MOS appropriate thickness. After etch back, the hardmask is removed, a poly-Si cap deposited, and the gate etched [112, 165, 169]. Figure 4.2 presents a schematic of the general fabrication process.

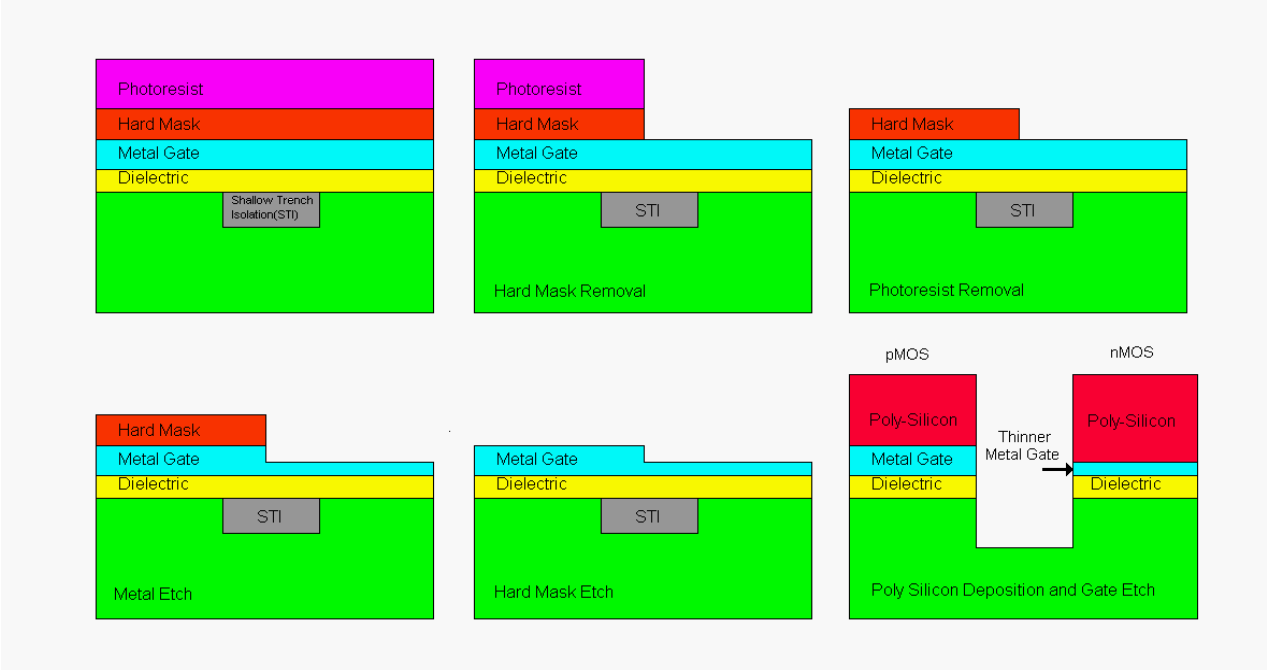


Figure 4.2: Schematic of the novel metal-as-deposited/etched-back fabrication method

Substrate preparation and dielectric deposition for device fabrication were conducted as described in Section 4.2. TiN was deposited on the dielectric at thicknesses of 30Å, 100Å and 200Å. The 200Å metal was either maintained at 200Å or submitted to a DI:H2O2:NH4OH (SC1) cold wet metal etch to reduce metal thickness to 100Å (15 minutes) or 30Å (25 minutes). Halo implants for both n-MOS (Boron (B)) and p-MOS

(Arsenic (As)) devices were conducted; only n-MOS devices received an LDD implant (As). After poly-Si cap deposition, the 30Å as deposited and etched back wafers received an SC1 cold metal etch for 10minutes, while all the others received an SC1 etch of 5 to 7 minutes. Full CMOS integration was completed through formation of a nitride spacer, source/drain implantation, nickel silicide (NiSi) processing, and aluminium (Al) metallization [5-7, 112, 165].

Capacitors of varying TiN thickness were fabricated to establish thickness related EWF tuning. High resolution transmission electron microscopy (HRTEM) images were taken of the as deposited metal gate FinFET transistor n-MOS and p-MOS substrate/dielectric interfaces described in Section 4.2.

4.3.2 Results and Analysis

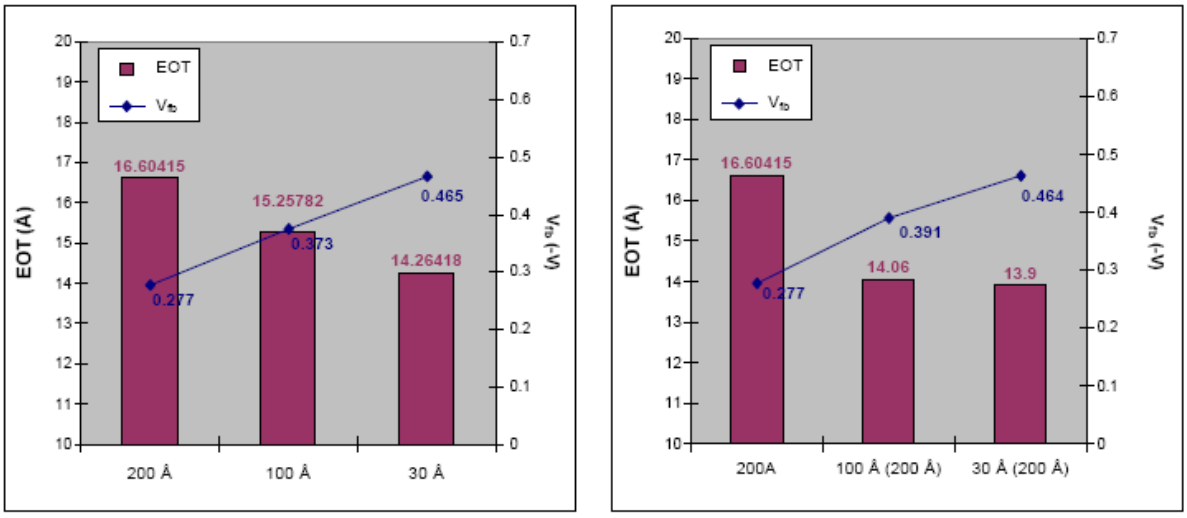
4.3.2.1 EWF and EOT Variation with TiN Thickness

In order to prove that metals etched back from one thickness to another would have the same effect as deposited metals at the specific thickness, ALD capacitors with TiN thicknesses of 200Å, 100Å and 30Å were deposited. Equivalent oxide thickness (EOT) and flat band voltage (V_{fb}) values calculated for the as deposited capacitors were compared with values obtained from ALD TiN capacitors deposited at 200Å and etched back to 100Å and 30Å.

Etched back thicknesses have been assumed from etch time to thickness relationships developed from XRR analysis conducted to develop the relevant etch recipes. Etched back thicknesses achieved are generally found to be reasonably close to the targeted thickness. Etch time has been used to establish etched back gate thickness in the research presented herein. Neither XRR nor alternative thickness measurement techniques have been utilized to confirm etched back thickness. The electrical results reported in this research support the accuracy of the etch time method to achieve metal

thicknesses reasonably similar to the targeted value, particularly in the case of TiN exposed to shorter etch times.

In Figure 4.3, EOT decreases and V_{fb} becomes more negative as TiN thins in both as deposited and etched back gates [20, 133, 165, 169]. The more negative V_{fb} and markedly thinner EOT of etched back compared to as deposited TiN at 100Å may result from differences in crystallinity, structure, and grain size between the two gates caused by divergence of the etched back TiN thickness achieved from the targeted value [5, 133, 169]. The etched back TiN may be physically thinner than the targeted 100Å; over etching is not obvious in the 30Å etched back capacitors. Though thickness dependent structural differences may influence diffusion which may then affect interface and bulk TiN characteristics [133, 165, 169], 30Å and thinner films may experience similar diffusion during RTA.



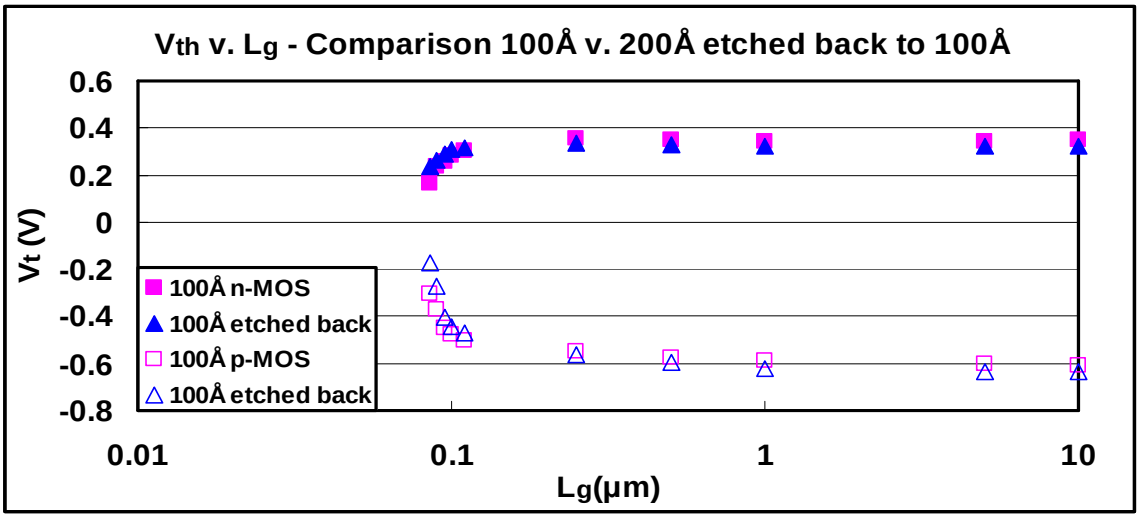
a) as-Deposited Thickness Difference

b) Etchback Thickness Difference

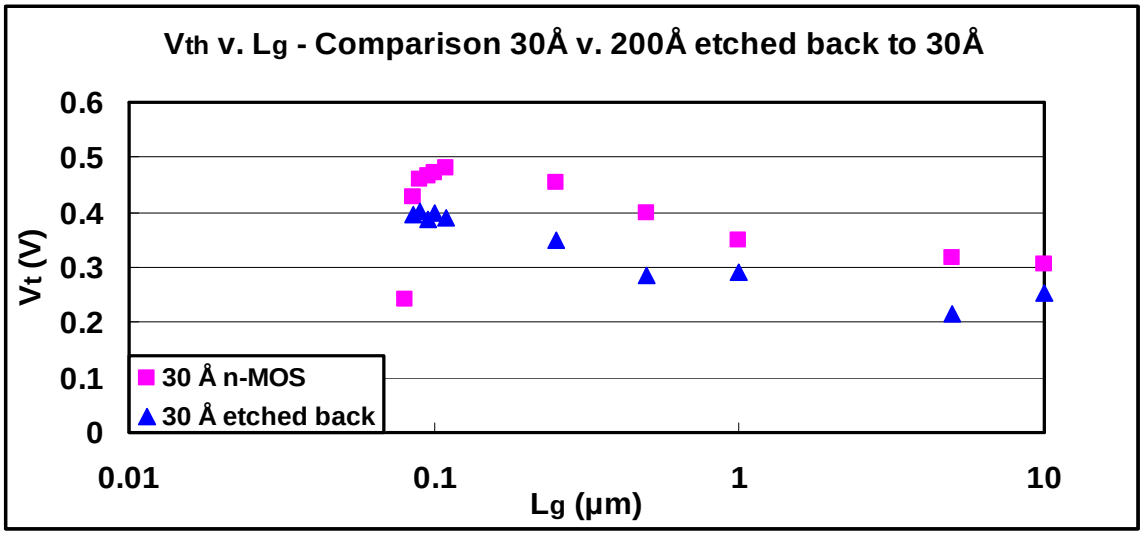
Figure 4.3: Difference in EOT and V_{fb} for as deposited and etched back TiN at 30Å, 100Å, and 200Å [etched back thickness estimated per §4.3.2.1 ¶ 2, p. 75]

4.3.2.2 FinFET Electrical Response and Analysis

Etched back and as deposited MG transistor electrical behavior is exemplified by the V_{th} v. L_g characteristics displayed in Figures 4.4(a) and 4.4(b). Generally, similar trends are exhibited in the V_{th} of both etched back and as deposited MG transistors. The less than ideal V_{th} characteristics and lack of p-MOS yield for transistors with 30Å TiN gates indicates that thin TiN fabrication processes must be optimized.



(a) V_{th} v. L_g comparing 100Å and 200Å etched back to 100Å TiN



(b) V_{th} v. L_g comparing 30Å and 200Å etched back to 30Å TiN

Figure 4.4: V_{th} v. L_g comparison between electrodes incorporating as deposited and etched back TiN [etched back thickness estimated per § 4.3.2.1 ¶ 2, p. 75]

In Figure 4.4(a), V_{th} values are very similar between 100Å as deposited and etched back TiN for both n-MOS and p-MOS devices. The V_{th} roll off with decreasing channel length is expected and indicates the uniformity of the fabrication process [20, 112]. Importantly, and similar to the V_{th} data presented in Figure 4.1 for as deposited TiN at various thicknesses, the n-MOS and p-MOS values are relatively symmetric for both the as deposited and etched back 100Å TiN devices, at least for very short L_g [20].

Electrical behavior is markedly different between the as deposited and etched back n-MOS Vth presented in Figure 4.4(b) for 30Å TiN gates; however, general trends remain consistent. Although the less than ideal electrical behavior for devices incorporating both as deposited and etched back 30Å TiN results from the fabrication process itself, the divergence between as deposited and etched back TiN V_{th} values may result from differences between the physical thickness expected and achieved during the etch back process. Since the metal is thin, Ti:N ratio is important to the V_{th} achieved; even minor differences in etched back and as deposited TiN thicknesses may cause V_{th} to vary more than in thicker films having a similar discrepancy between etched back and as deposited film thicknesses [133]. 30Å p-MOS devices did not yield, most probably because the p-MOS underlap and halo characteristics require optimization in order to withstand full CMOS processing of thinner films.

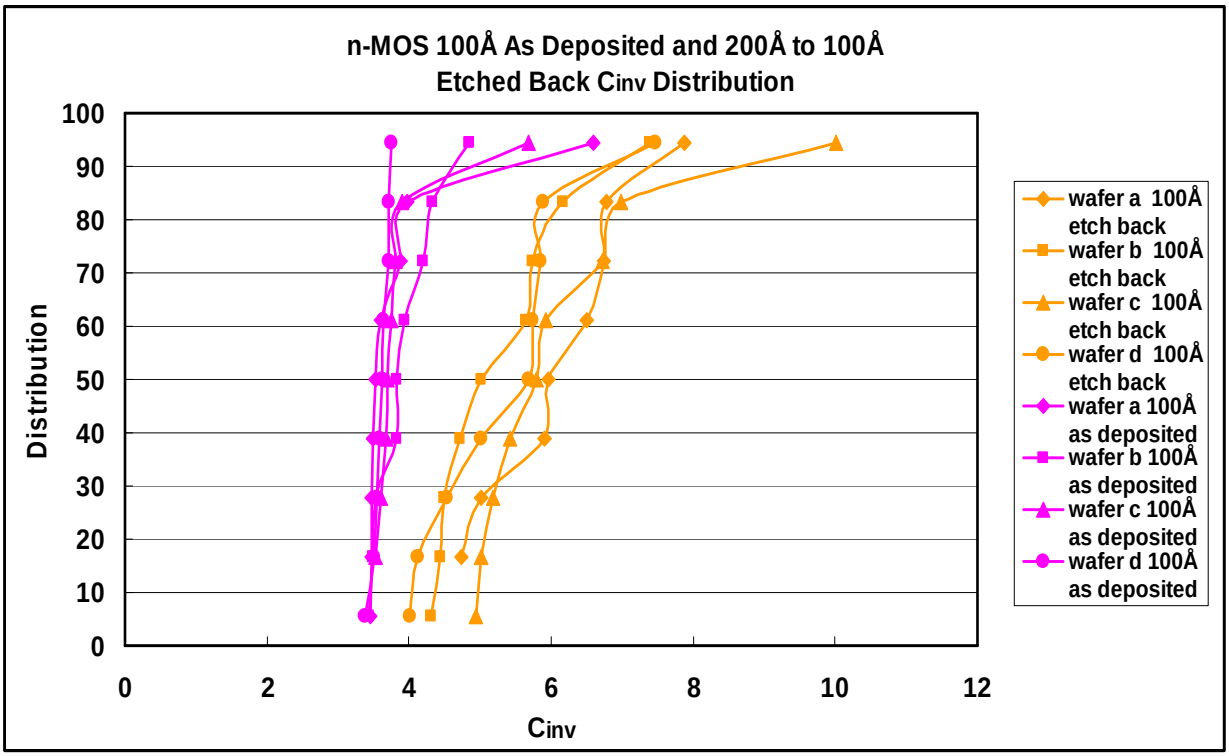


Figure 4.5: C_{inv} ($\mu F/cm^2$) distribution for n-MOS as deposited and etched back 100Å TiN [etched back thickness estimated per § 4.3.2.1 ¶ 2, p. 75]

Figure 4.5 compares the inversion layer capacitance (C_{inv}) distribution across multiple wafers of etched back and as deposited TiN. The C_{inv} values of 200Å TiN etched back to 100Å experience wider distribution than as deposited 100Å TiN. Slight variations in inter-wafer and intra-wafer TiN thickness caused by localized and general wafer strain effects on the TiN etch rate during the etch back process may be responsible for the observed C_{inv} spread [6, 112, 133, 137, 140, 168]. Etchant related changes to the dielectric interfaces and slight differences in the etch time between wafers might also contribute to the wide distribution of the etched back devices [165, 169, 137, 168].

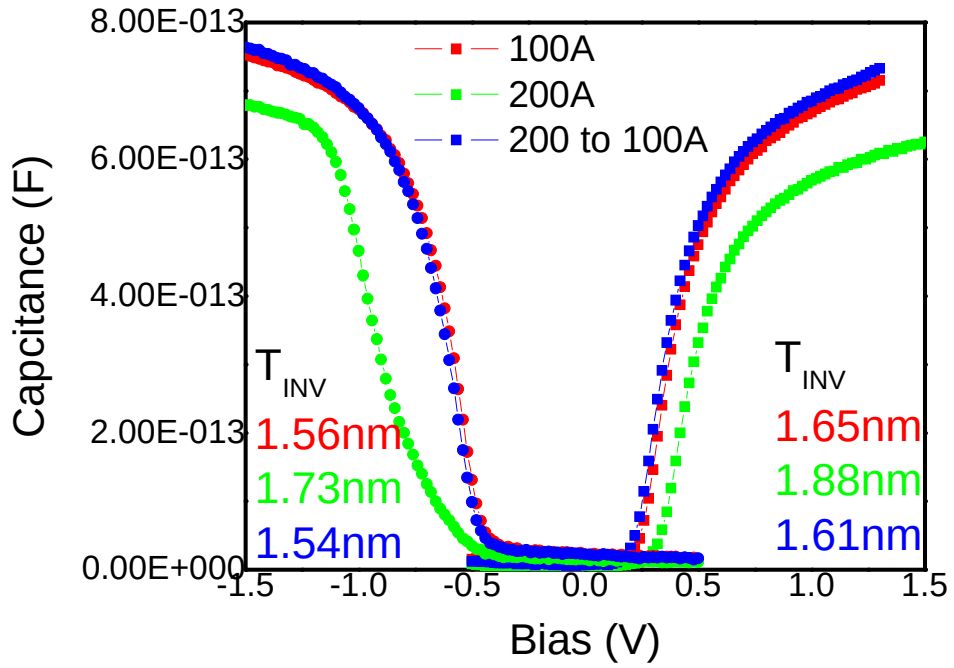


Figure 4.6: Capacitance and inversion layer thickness (T_{inv}) for etched back and as deposited 100Å TiN (C_{inv} values at |1.5| V were used to calculate T_{inv} under the gate) [etched back thickness estimated per § 4.3.2.1 ¶ 2, p. 75]

Capacitance-Voltage (C-V) curves in Figure 4.6 indicate TiN etched back to 100Å tracks as deposited 100Å TiN capacitance well; as expected, 200Å etched back 100Å TiN C-V values are much higher than those for as deposited 200Å TiN. n-MOS and p-MOS C-V are relatively symmetric; T_{inv} values for n-MOS and p-MOS are also reasonably similar. The slight differences between as deposited and etched back T_{inv} and C_{inv} values, respectively, result from either differences in expected and actual etched back thickness or interface effects in the etched back stack occurring during the anneal process.

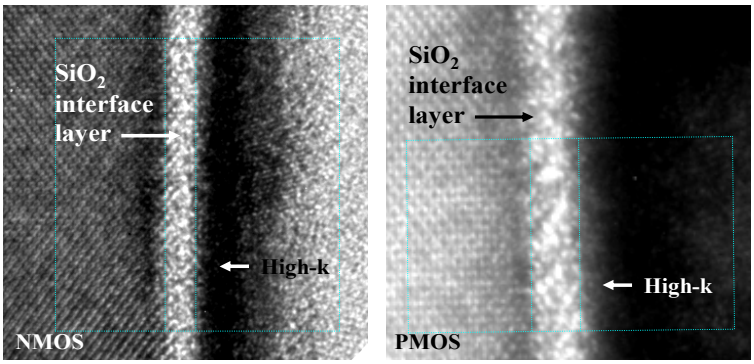
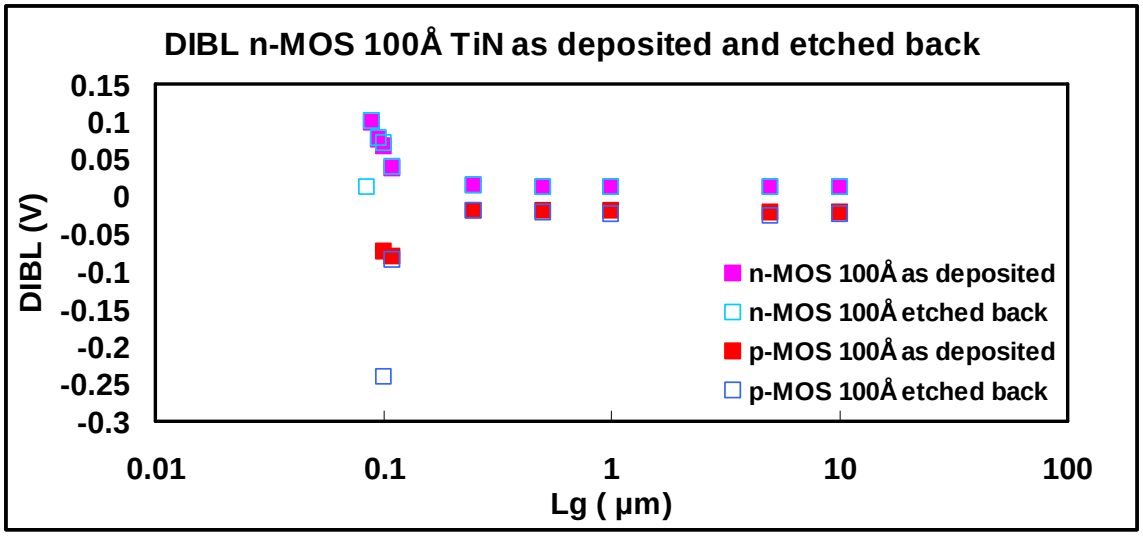


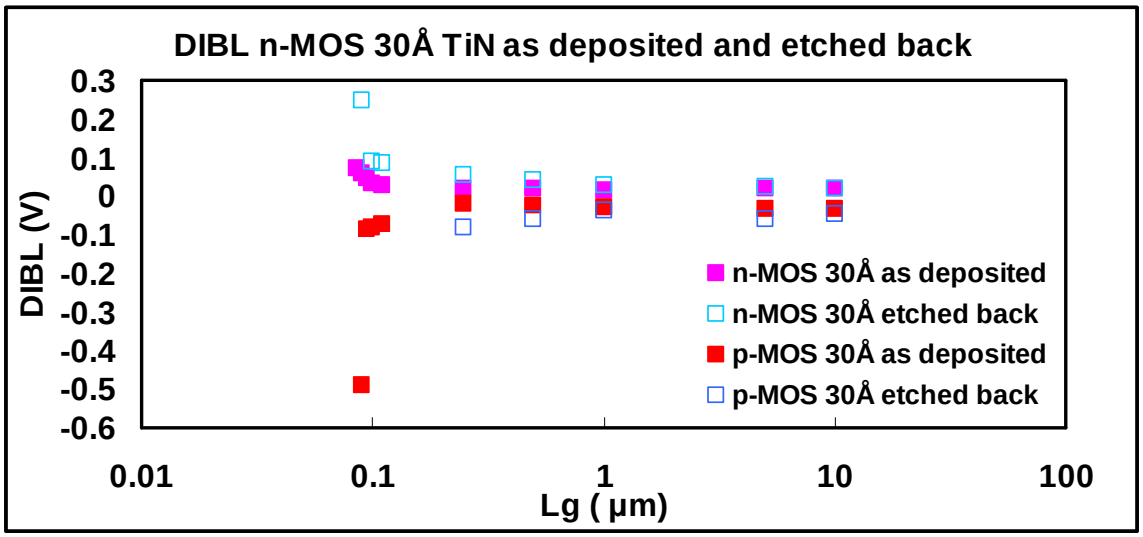
Figure 4.7: HRTEM cross section of n-MOS and p-MOS fins showing a thicker p-MOS bottom interface layer compared to the n-MOS interface layer for as deposited 30Å and 100Å TiN

HRTEM images in Figure 4.7 of 100Å and 30Å as deposited TiN gate stacks reveal that thicker, p-MOS appropriate TiN stacks develop a thicker interfacial oxide (SiO_2) layer between the channel and dielectric than thinner, n-MOS appropriate TiN stacks. The similarity in behavior between 100Å as deposited and etched back TiN in Figure 4.6 as well as the difference between this behavior and that displayed by the 200Å TiN stacks suggests the thickness of the interfacial oxide layer evolves post etch back, during RTA processing. More rapid diffusion through the thinner metal gate may account for the differences in interfacial oxide thickness [165, 169].

Drain induced barrier lowering (DIBL) values demonstrating change in threshold to drain voltage ($\Delta V_{th}/\Delta V_d$) between linear and saturation current v. gate voltage (I_d-V_{gs}) curves are provided in Figures 4.8(a) and 4.8(b) for FinFETs incorporating 100Å and 30Å TiN electrodes, respectively. DIBL indicates a decrease in V_{th} and concomitant increase in I_d caused when the drain voltage contributes to channel regulation. As deposited and etched back n-MOS FinFETS display similar DIBL at both 30Å and 100Å TiN gate thicknesses. The DIBL values display the expected inverse relationship to gate length caused when the drain voltage begins to assert greater influence on the I_d at smaller dimensions. Optimization of the fabrication process is expected to improve the DIBL values achieved.



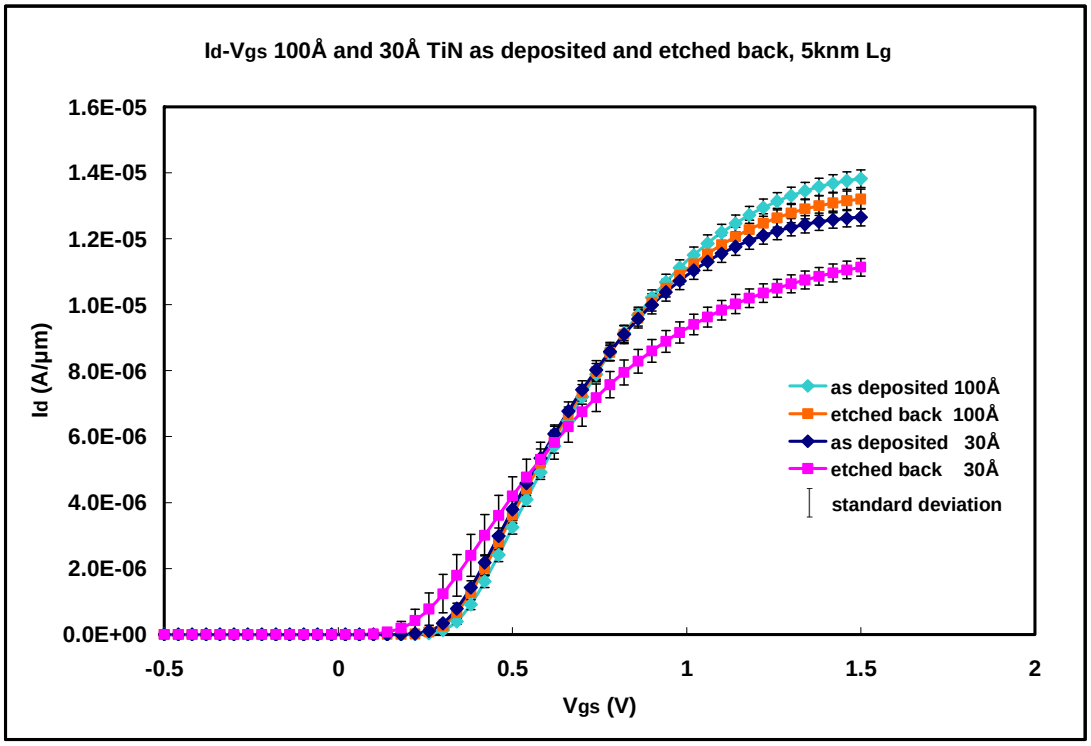
(a) DIBL of n-MOS 100Å as deposited and etched back



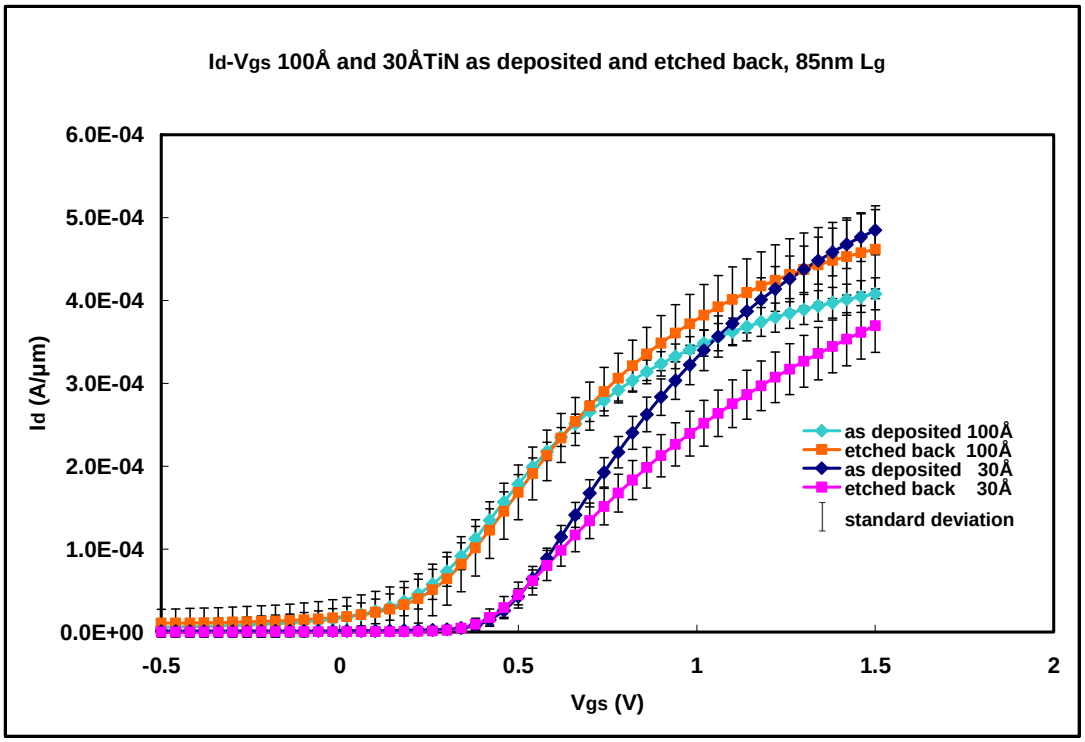
(b) DIBL of n-MOS 30Å TiN as deposited and etched back

Figure 4.8: n-MOS DIBL comparison between electrodes incorporating as deposited and etched back TiN [etched back thickness estimated per § 4.3.2.1 ¶ 2, p. 75]

I_d-V_g, transconductance (g_m), and current v. drain voltage (I_d-V_d) FinFET data in Figures 4.9, 4.10, and 4.11, respectively, indicate greater consistency between 100Å as deposited and etched MG transistors than between 30Å MG devices. Etched back TiN MGs tend to underperform as deposited TiN devices. The electrical behavior is generally worse for the shorter channel FinFETs [173, 174, 175].



(a) 100Å and 30Å as deposited and etched back TiN I_d-V_{gs}, 5µm L_g



(b) 100Å and 30Å as deposited and etched back TiN I_d-V_{gs}, 85nm L_g

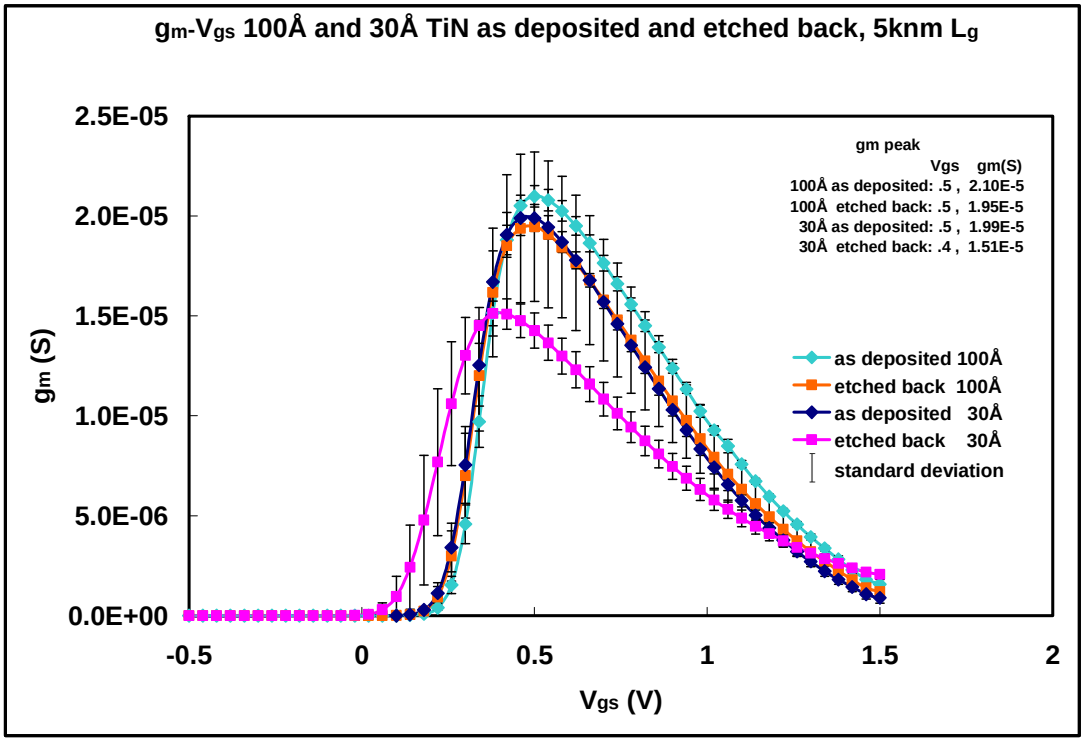
Figure 4.9: I_d-V_{gs} of 100Å and 30Å as deposited and etched back TiN gated FinFETs at 5µm and 85nm L_g [etched back thickness estimated per § 4.3.2.1 ¶ 2, p. 75]

I_d-V_g data presented in Figure 4.9(a) indicates comparable drive current between 5μm L_g devices with 100Å as deposited, 100Å etched back, and 30Å as deposited TiN gates [3]. The significantly degraded drive current etched back 30Å TiN gated transistors exhibit may result from fin roughening caused by the etch back process or from composition differences resulting from differences between targeted thickness and etched back thickness achieved.

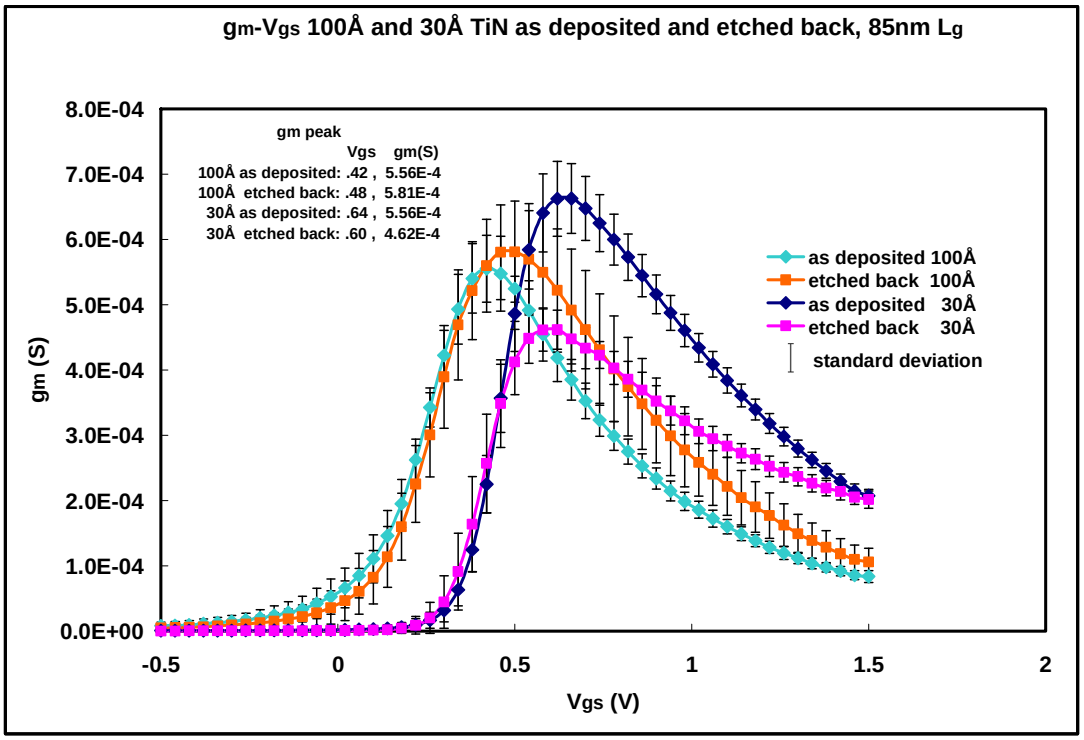
Higher drive currents for the shorter L_g (85nm) FinFETs in Figure 4.9(b) than for the longer gated devices in Figure 4.9(a) may indicate better gate control of the channel or more pronounced SCEs (DIBL) affecting the shorter L_g devices [173]. The percentage change in as deposited and etched back drive current for 30 Å TiN remains consistent between long and short L_g devices. Divergence is greater between 100Å as deposited and etched back TiN gated transistor drive current at 85nm L_g than at 5μm L_g.

Interestingly, the etched back 100Å TiN gate exhibits a higher drive current than the as deposited MG electrode transistors. In all other cases, etched back gated devices have lower drive current than devices with as deposited gates. The higher drive current for the etched back 100Å TiN gate most probably results from the thickness achieved being less than the targeted thickness. The differences observed between long and short L_g I_d-V_g may relate to differences in etch uniformity over the longer gate lengths.

In Figure 4.10(b), 30Å TiN gated transistor g_m is shifted right of 100Å TiN gated devices. The shift indicates a TiN thickness dependent change in V_{th} at short L_g which is not so obvious in the longer L_g structures of Figure 4.9(a). Inter and intra wafer I_d spread is much larger for shorter L_g 100Å and 30Å TiN gated devices. Electrical behavior is degraded in the shorter L_g devices, particularly those incorporating very thin etched back TiN. The etched back method may affect interface composition/Ti:N ratio. Optimization is required to improve the single metal gate etch back fabrication method.



(a) 100Å and 30Å as deposited and etched back TiN g_m-V_{gs}, 5µm L_g

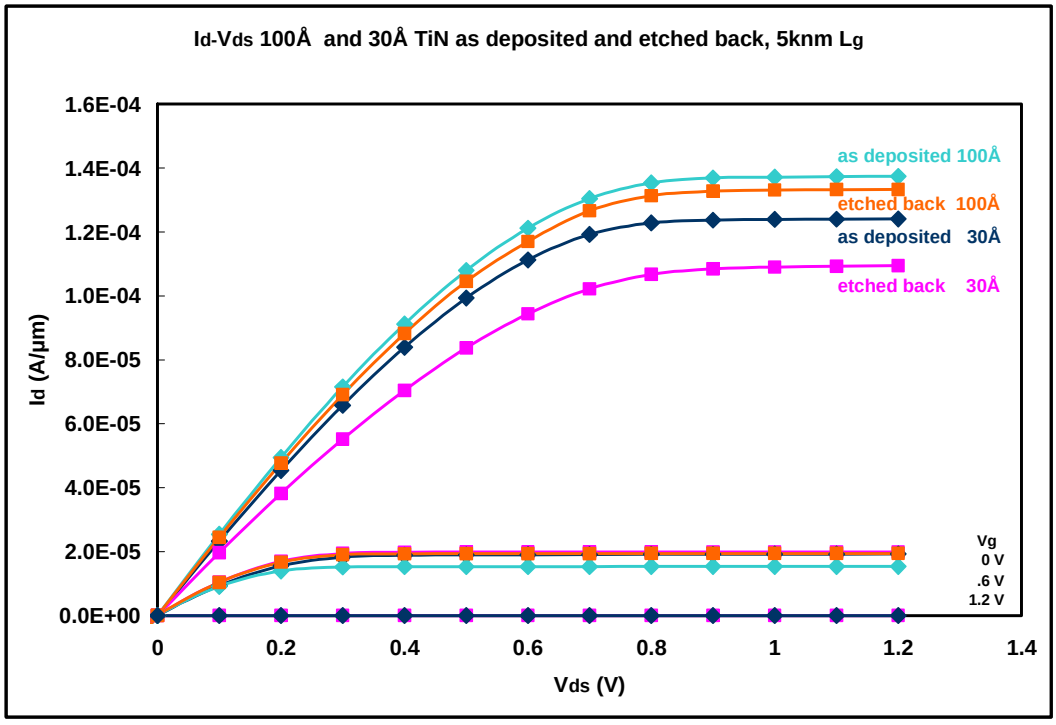


(b) 100Å and 30Å as deposited and etched back TiN g_m-V_{gs}, 85nm L_g

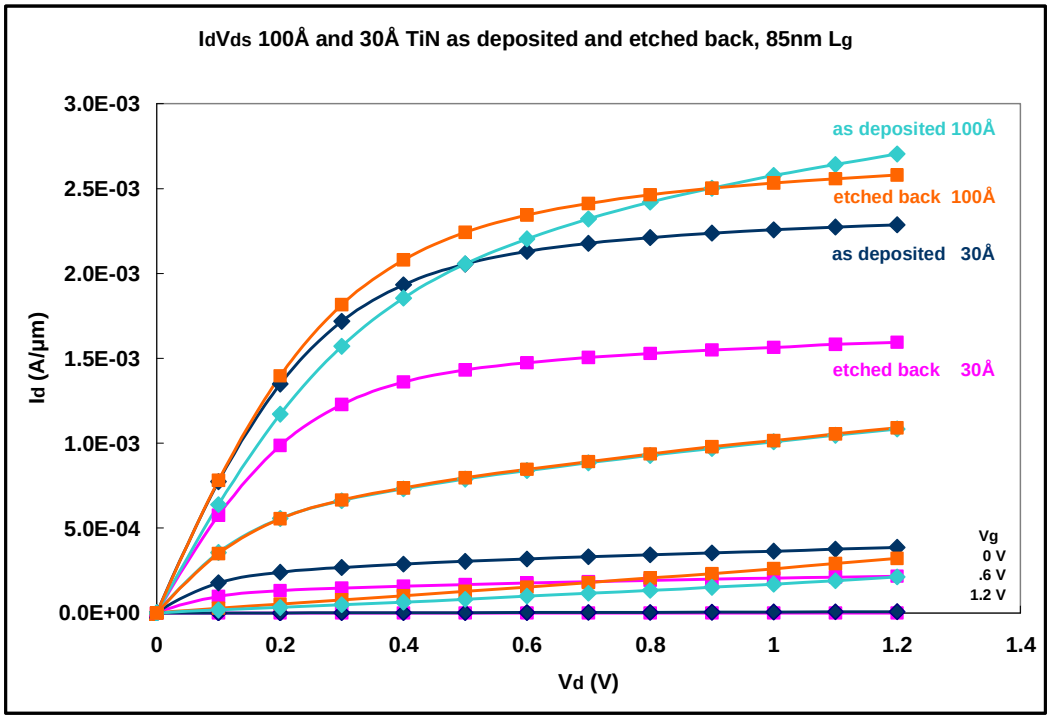
Figure 4.10: g_m-V_{gs} of 100Å and 30Å as deposited and etched back TiN gated FinFETs at 5µm and 85nm L_g [etched back thickness estimated per §4.3.2.1 ¶ 2, p.75]

Transconductance ($g_m = \partial I_D / \partial V_G$) values for the 30Å and 100Å long and short L_g TiN gated FinFETs presented in Figures 4.10(a) and 4.10(b), respectively, indicate that there is a decrease in mobility between as deposited and etched back 30Å TiN. In keeping with the increase in drive current of 85nm L_g 100Å etched back TiN FinFETs, the g_m for these FinFETs in Figure 4.10(b) is greater than that of the as deposited 100Å TiN gate devices. With the exception of 85nm L_g 100Å etched back TiN gated FinFETs, the g_m of the etched back devices in Figures 4.10(a) and 4.10(b) is lower than as deposited g_m values. This decrease in mobility may indicate an increase in interface traps (D_{it}) or scattering points which might be the result of incorporation of atoms into the TiN or roughness introduced on the TiN surface by the etch.

The increased g_m observed in the etched back short channel 100Å FinFETs may result from greater strain induced because the etched back thickness is thinner than the as deposited thin metal gate [137]. As expected from the I_d-V_{gs} data presented in Figure 4.9(b), the g_m and peak values of the as deposited 100Å, 30Å, and etched back 100Å TiN 5μm L_g devices are similar. 30Å etched back TiN has a substantially lower peak g_m value somewhat shifted to lower V_{gs} values.



(a) 100Å and 30Å as deposited and etched back TiN I_d-V_{ds}, 5µm L_g



(b) 100Å and 30Å as deposited and etched back TiN I_d-V_{ds}, 85nm L_g

Figure 4.11: I_d-V_{ds} of 100Å and 30Å as deposited and etched back TiN gated FinFETs at 5µm and 85nm L_g [etched back thickness estimated per § 4.3.2.1 ¶ 2, p. 75]

I_d-V_{ds} curves obtained at V_{gs} = 0V, .6V and 1.2V are presented in Figures 4.11(a) and 4.11(b). For 5μm L_g, I_d values for etched back and as deposited 100 Å TiN gates are very similar. The I_d values are substantially larger for longer channel as deposited 30Å TiN gate devices than for etched back 30Å TiN gated structures. As expected from the I_d-V_g and g_m data in Figures 4.9 and 4.10, the as deposited 30Å TiN Id values are very similar to those of the as deposited and etched back 100Å I_d. Values for both 100Å and 30Å etched back and as deposited devices are essentially the same at .6V and 0V gate voltages.

In Figure 4.11(b), etched back and as deposited shorter L_g 100Å TiN devices display similar behavior, although the variation between etched back and as deposited TiN gate devices is greater than that for the devices with larger L_g in Figure 4.11(a). 30Å etched back and as deposited devices display a larger percentage difference in Id than the 30Å devices at 5μm L_g. There is greater spread, as well, between 100Å and 30Å TiN gate devices at .6V V_{gs}. While 100Å etched back and as deposited TiN gate devices have the same I_d values, there is spread in the 30Å as deposited and etched back I_d. At 0V V_{gs}, the I_d-V_{ds} for 30Å as deposited and etched back devices are essentially zero. Interestingly, there is greater spread between 100Å etched back and as deposited I_d values; these are also greater than zero at 0V V_{gs}.

4.4 CONCLUSIONS

Generally, the electrical data analyzed herein proves that single metal TiN gates fabricated on High-κ dielectrics may be tuned between n-MOS and p-MOS compatible V_{th} for UTB-SOI, specifically FinFET, devices using a simplified metal etch back fabrication method to engineer TiN thickness. Thinner TiN is appropriate for n-MOS devices while thicker TiN is appropriate for p-MOS devices. Etch back of thicker TiN is shown to be generally as effective as TiN deposited at 30Å and 100Å in achieving n-MOS and p-MOS appropriate V_{th} values. The resulting etched back devices behave

relatively well although they must be optimized before they may be considered a viable alternative to existing DMG technology.

Etching back thick as deposited TiN achieves a 40% step reduction in the gate fabrication process, a lithography sub-module reduction of six steps, and mitigation of overlay issues by elimination of a reverse lithography step required in DMG. The etch-back method is user friendly and may be implemented for metals the EWF of which may be tuned across the appropriate range by thickness engineering, implantation, and bi-metal layering.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 SUMMARY AND CONCLUSIONS

The research developed herein provides a simple to integrate, low cost alternative to existing dual metal gate (DMG) high-k/metal gate fabrication methods. The unique gate stacks engineered introduce n-MOS to p-MOS thickness tunable single metal gates for SOI FinFET applications; an innovative thicker to thinner metal etch back fabrication method produces single metal n-MOS and p-MOS devices with reasonable electrical behavior at lower cost and complexity than conventional complete first metal etch DMG fabrication processes.

More specifically, the research herein has introduced:

- Insight into the mechanism controlling TiN thickness related EWF tuning between n-MOS and p-MOS appropriate values; specifically, Ti:N ratio and interface structure.
- A simplified alternative to DMG high-k dielectric/metal gate incorporating thicker to thinner metal etch back; specifically, depositing a mask layer over a thick single metal gate, exposing areas to be etched back, etching back the thickness of the exposed areas, removing the remaining mask, and completing full CMOS integration.
- Full scale single metal gate SOI FinFET devices incorporating the etched back metal gate fabrication method displaying reasonable, though not optimized, behavior proving that etched back and as deposited gates exhibit similar behavior.
- Possible mechanisms through which thickness EWF tuning is achieved.

5.2 FUTURE WORK

The devices fabricated and results presented herein provide a proof of concept. Future research will include optimizing the fabrication and gate etch process of the same

gate metal at two different thicknesses to produce tighter electrical behavior. Materials analysis delving into the mechanism causing the difference between etched back and as deposited electrical behavior would be useful in determining how the fabrication process might be optimized, particularly in the case of 30Å devices. The research would greatly benefit from reliability analyses to determine whether the etched back gates are as resilient as TiN as deposited metal gates and to better understand the tuning mechanism and how it may be effectively engineered. In addition, etched-back fabrication may be investigated as an alternative for other thickness tunable metals and for metals the EWF of which may be tuned by ion implantation.

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