Interdigitated Capacitor Sensor for Complex Dielectric Constant Sensing

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Dedicated to my family

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Interdigitated Capacitor Sensor for Complex Dielectric Constant Sensing

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The University of Texas at Austin, 2010

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The objective of this thesis is to develop a complex dielectric properties sensor using interdigitated capacitor (IDC) structure. IDCs are easy to fabricate and because of its planar structure, it can be easily integrated with other sensing components and signal processing electronics. The design, fabrication, modeling, and testing of IDC sensor are presented in this thesis. Design parameters and their influence on sensor's output signals are discussed. Previous IDC models are reviewed and the limitations are studied. A new equivalent circuit model based on the fringing electric field distribution and a novel iterative data extraction algorithm combining Finite-Element Method (FEM) and the equivalent circuit model is studied. Results suggest that the algorithm can accurately extract relatively low dielectric constant and conductivity of material under test (MUT) from measured impedance data.

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Chapter 1

Introduction

Since the first introduction of Micro-Electro-Mechanical Systems (MEMS) by Feynman in the 1960's [2], it has been the driving force for advances in miniaturized sensors, actuators, and structures in many areas of science and engineering, including mechanical, chemical and electrical engineering. Such interdisciplinary applications made it possible to realize a multifunctional micro-system on a single chip.

One interesting area of the MEMS is the application of interdigitated capacitor (IDC) sensors. The term interdigitated capacitor is selected for use throughout this thesis. There are other names such as "interdigital", "periodic", "comb" and etc used in other publications [3]. IDC refers to a fingerlike periodic pattern of parallel thin film electrodes used to build up the capacitance associated with the electric fields that penetrate into the material above the electrodes. There are various applications including humidity sensor [4], sensors that monitoring curing process [5], chemical gas sensor [6], pressure sensor [7], surface-acoustic wave sensor [8], and wireless gas dielectric constant sensor [9]. Because of the similar structure of IDC and coplanar wave guide and micro-strips, there have been extensive studies on the capacitance calculation and modeling of the IDC [1, 10–12].

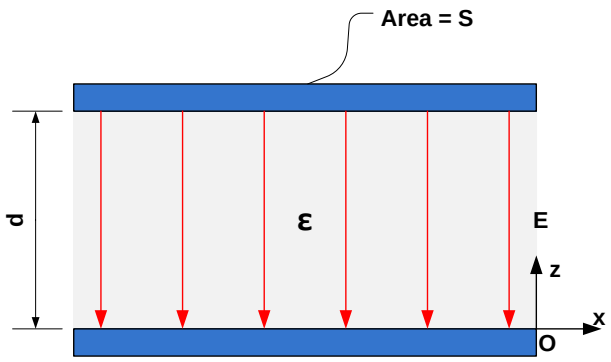


Figure 1.1: Illustration of a parallel plate capacitor

In the following sections, basics of capacitive sensor and complex dielectric constant are briefly introduced. Then the basic idea and sensing mechanism of IDC sensor are discussed.

1.1 Capacitive Sensor

Capacitive sensors work by detecting changes in capacitance when an object is placed between two capacitor plates. The capacitive change could come from changing of distance between two capacitor plate or changing of electric properties of the material placed between the capacitor plates. In this section, the sensing mechanism of a capacitive sensor is discussed using parallel plate capacitor, which is the most straightforward structure of capacitive sensors, as an example. The configuration of the parallel plate capacitor is shown in Figure 1.1.

Capacitance of a two conductor system is defined as the ratio of the magnitude of the total charge on either conductor to the magnitude of the

potential difference between conductors, expressed as follows

$$C = \frac{Q}{V_0} \tag{1.1}$$

The total charge on the capacitor plate is calculated using surface integral as follows.

$$Q = \oint_S \epsilon \mathbf{E} \cdot d\mathbf{S} \tag{1.2}$$

and the potential difference is calculated by carrying a unit positive charge from the negative to the positive surface.

$$V_0 = -\int_-^+ \mathbf{E} \cdot d\mathbf{L} \tag{1.3}$$

Apply the equations to a infinite parallel plates with separation d in Figure 1.1. Assume a uniform sheet of surface charge $\pm\rho_S$ on each plate, and choose the lower plate at $z = 0$ and upper plate at $z = d$. The electric field between the two plates is calculated as

$$\mathbf{E} = \frac{\rho_S}{\epsilon}(-\mathbf{z}) \tag{1.4}$$

where the negative sign means the electric field is pointing in negative z direction. Thus the potential difference between the two plates is

$$\begin{aligned} V_0 &= -\int_-^+ \mathbf{E} \cdot d\mathbf{L} \\ &= -\int_0^d -\frac{\rho_S}{\epsilon} dz \\ &= \frac{\rho_S}{\epsilon} d \end{aligned} \tag{1.5}$$

Since the plates are infinitly large, the capacitance is also infinite. Hence we need to consider one portion of the infinite plates having area of S. The total charge is calculated as

$$Q = \rho_S S \tag{1.6}$$

and therefore the capacitance is calculated as

$$C = \frac{W}{V_0} = \frac{\epsilon S}{d} \tag{1.7}$$

It can be seen that the capacitance of a parallel plate capacitor depends on the dielectric constant ϵ of the material between the two plates, the area of the capacitor S, and the distance between the two plates d. For certain application such as capacitive pressure sensor, the variable is the distance d. By changing environment pressure the capacitor plates gets closer or further apart, thus changing the capacitance. For application in this thesis, the variable is dielectric constant ϵ. Since different materials under test (MUT) would have different dielectric constant, the capacitance will change when different MUT is being present.

1.2 Lossy Materials and Complex Dielectric Constant

In the previous section, the sensing mechanism of capacitive sensor is discussed. The calculation of the capacitance is based on assumption that the conductivity of the MUT is infinite, that is, the sensor is a ideal capacitor.

However, in real application, the MUT more or less has finite conductivity σ. Such materials are called lossy materials. Generally for one material,

when $\sigma/(\omega\epsilon) >> 1$, it is considered as good conductor and lossy material; when $\sigma/(\omega\epsilon) << 1$, it is considered as lossless or low-loss material.

When dealing with lossy material, conduction current needs to be taken into consideration. The current density flowing in a lossy medium is expressed as

$$\begin{aligned} \mathbf{J_{tot}} &= \mathbf{J_{conduction}} + \mathbf{J_{displacement}} \\ &= \sigma\mathbf{E} + j\omega\epsilon'\mathbf{E} \\ &= j\omega\epsilon'(1 - j\frac{\sigma}{\omega\epsilon'}\mathbf{E}) \end{aligned} \tag{1.8}$$

where ϵ' is the real part of complex dielectric constant. Complex dielectric constant is defined as

$$\epsilon = \epsilon' - j\epsilon'' \tag{1.9}$$

where

$$\epsilon'' = \frac{\sigma}{\omega} \tag{1.10}$$

The ratio of ϵ'' and ϵ' is usually called loss tangent ($\tan\delta$) of the medium.

Because the loss exists in material, when measuring the capacitive sensor on a impedance analyzer, one can see the result is usually not an ideal capacitor. Instead it has a resistor component caused by finite conductivity of the MUT. By building a equivalent circuit model properly, extraction of both real and imaginary part of complex dielectric constant can be done.

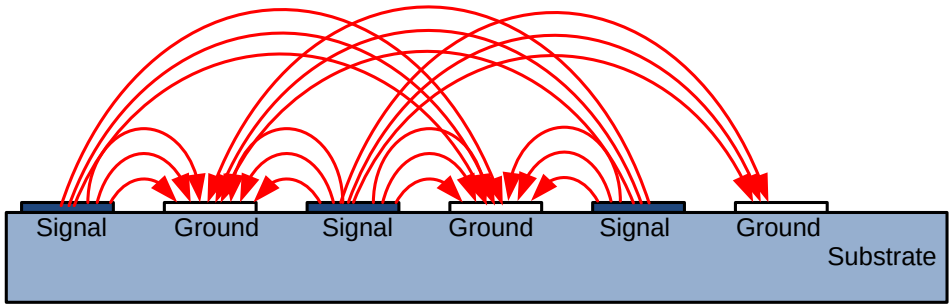


Figure 1.2: Illustration of an IDC

1.3 Interdigitated Capacitor Sensors Basics

Interdigitated Capacitor (IDC) has interdigitated finger-like electrodes as two port of the capacitor, as shown in Figure 2.2. Unlike uniformly distributed electric field in parallel capacitor, the electric field of an IDC starts from one group of signal electrodes having higher potential, coming up and penetrating into the material under test (MUT), then going down to another group of ground electrodes. The electric flux is also shown in Figure 2.2.

The sensing mechanism of an IDC is essentially the same as other capacitive sensors. The dielectric properties will change by changing the MUT, resulting capacitance or impedance change at output of the IDC. By properly modeling the IDC, the dielectric properties could be extracted from specific extraction algorithms.

One major reason to choose IDC rather than parallel capacitor is ease of fabrication. It is easier to fabricate an IDC than a parallel capacitor using microelectronics fabrication techniques, and if designed properly, the capac-

itance of an IDC could be equal or greater than a parallel plate capacitor of same size. Fabricating a parallel plate capacitor usually requires multiple fabrication steps, and most likely will need to deposit a layer of sacrificing material and etch it away in later steps, in order to build a fixed gap between the two capacitor plates. For IDC, the sensor has a planar structure, and the sensing mechanism is essentially one-sided. Therefore, simple evaporation and lithography techniques are enough to pattern the electrodes on substrate.

Another advantage is that it is easy to integrate the sensor to other components of the sensing system. Ong *et. al.* [9] reported a wireless sensing system by connecting a IDC to a inductor, hence forming a RLC resonant circuit which is detectable by external reader coil. It is also possible to integrate IDC into a electronic system and control the electrodes individually in order to sense different layers of materials [13]. Because of its planar structure and one-sided sensing scheme, chemically or biologically sensitive films could be easily integrated with the IDC, thus increase the sensitivity of the sensor.

One drawback of IDC is that no closed form analytical expression of capacitance/impedance with respect to dielectric constant and conductivity has been derived. Existing calculation methods are more or less limited to specific applications, which will be discussed in later chapters. Therefore the relationship between measurements and electric properties of MUT must be calculated numerically after building an equivalent model of the sensor.

1.4 Thesis Outline

In Chapter 2, the design of IDC is discussed. The design parameters including number of electrode pairs, effects of electrode width and spacings, electrode length and thickness, and liquid container height and substrate thickness are studied. Five groups of IDC designs are presented.

In Chapter 3, fabrication process of the IDCs is presented. Detailed process steps of depositing insulation layer and building ultra-thick liquid container structures are discussed.

In Chapter 4, the modeling of IDC sensor is studied. Previous conformal mapping calculation method and its limitation is studied. A novel equivalent circuit model and iterative dielectric properties extraction algorithm is introduced.

In Chapter 5, the measurement and extraction of fabricated IDC are presented. The results of iterative extraction algorithm are discussed. It is shown that the iterative extraction algorithm could accurately extract both liquid and solid dielectric constant and conductivity when the dielectric constant is not very large.

Chapter 2

Sensor Design

In this chapter, the design and fabrication of IDC sensor are discussed. In order to maximum the capacitive output of the sensor, various design parameters are studied. The sensor layout is then presented.

2.1 Sensor Structure

In this section, the structure is IDC sensor is presented. Figure 2.1 shows a 3-Dimensional illustration of the sensor. The gray bulk part is the substrate; the yellow layer is the insulator; the blue patterns are the IDC electrodes; the light blue part is the liquid container. Note that the electrodes shown in the figure are placed above the insulator for easier illustration. In reality, the electrodes are covered by the insulator to prevent contact between MUT and electrodes.

The sensor is fabricated on quartz glass slides provided by G.M. Associates, Inc. Quartz is a relatively low loss, low dielectric constant material. The dielectric constant of quartz is 3.9, thus the capacitance component from substrate is minimized. In the sensor fabrication, we chose the substrate having thickness of 1 mm. The electrode width and spacing of the sensors designed is around 20 to 200 μm. One millimeter could be seen as infinite thick from

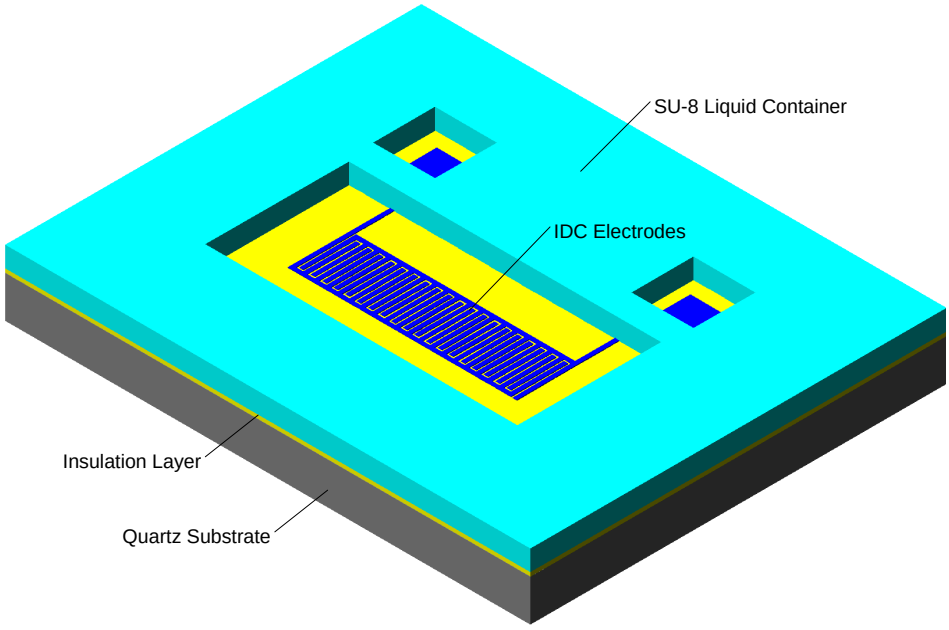


Figure 2.1: 3-Dimensional illustration of the sensor structure. Note that the electrodes (blue) are covered by the insulation layer (yellow) in real devices

the electrodes' point of view, because the electric field at 1 mm away from the electrodes is so small that it doesn't have significant effect on total capacitance.

The aluminum electrodes are evaporated and patterned on the substrate, covered by a thin insulation layer. The insulation layer needs to be chemically inert to most of MUTs. We used negative photoresist SU-8 to form the insulation layer. Both of them are very chemically inert. The thickness of the insulator should be as thin as possible in order to minimize the loss and maximize the capacitance component of insulation layer. Note that the capacitance of the insulation layer is in series with the capacitance of MUT, thus the greater the capacitance of insulation layer, the less it will affect total

capacitance of the IDC, detailed capacitance components relationships will be discussed in Chapter 4.

On top of the insulation layer is the MUT container fabricated by SU-8. After hard bake for 30 minutes under 150 ℃, SU-8 structure is left as part of the device and its properties will not change in the future. The height of container is 200 μm, higher than all the penetration depth of our IDC design. The penetration depth of IDCs is discussed in Section 2.2.5.

2.2 Design Parameters

In order to get insights of effects of sensor's dimension on total capacitance, and without getting into complicated details of multiple layer capacitance calculation, we used single layer conformal mapping calculation method, which is part of Igreja's multiple layer IDC capacitance calculation [10], as our design reference guide.

Two important design parameters of an IDC are spacial wavelength of the IDC, which is double the length of electrode width plus and spacing between electrodes, as shown in Figure 2.2; and the metalization percentage of the electrodes, which is essentially the ratio between electrode width and spacing. Other parameters that can affect total capacitance significantly include number of electrode pairs and electrode length. Electrodes thickness and substrate thickness has much less effect than the spacial wavelength and metalization percentage in our design.

The spacial wavelength and metalization percentage is not two param-

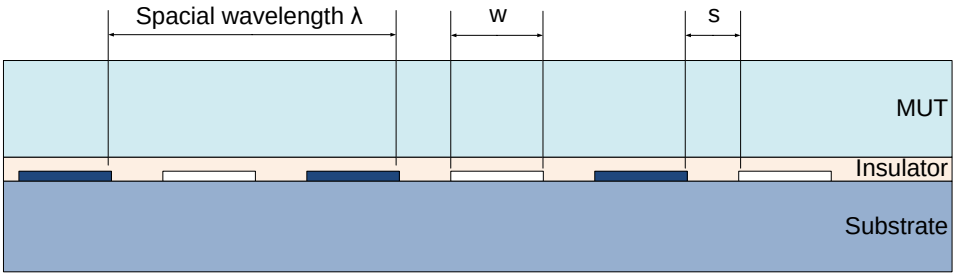


Figure 2.2: Cross section of an IDC

eter that can be dealt with separately. For the same spacial wavelength, there can be different metalization percentage; and it is also possible to have different wavelength with same metalization percentage. Furthermore, design with same sensor area is also of interest.

In summary, in order to have a clear insight, we need to know the following parameter effects. First, the capacitance change when number of electrodes pairs is changing, while spacial wavelength and metalization percentage is fixed. Second, the capacitance change when spacial wavelength is changing which metalization percentage and number of electrodes are fixed. Third, the capacitance change when metalization percentage is changing while spacial wavelength and number of electrodes is fixed. Fourth, the capacitance change when sensor's area and metalization percentage is fixed, while spacial wavelength is changing.

2.2.1 Number of Electrode Pairs

By intuitively studying the electric field distribution, It can be seen that the field distribution is the same between any two adjacent electrodes except

the out-most two fingers. The same distribution results from symmetric sensor design. Two adjacent electrodes are defined as one unit cell of the IDC, and the whole IDC consists different numbers of unit cells depending on different design. Since the environment of one unit cell is the same as another, the field distribution must be almost the same in different cells. Note that the IDC is not totally symmetric since it does not have infinite number of unit cells. Field distribution in two unit cell might be slightly different. As shown in Figure 2.3, in an IDC having 3 unit cells, the field distribution of unit cell A is different from that of unit cell B. However, the difference caused by asymmetry could be ignored since the field strength from one electrode to another electrode located more than one unit cell away is significantly weaker. Thus, the total capacitance of an IDC should change linearly with the number of electrode pairs. If the capacitance of one unit cell is C_{unit}, and the number of electrode pairs is N, total capacitance is expressed as

$$C_{total} = N \times C_{unit} \tag{2.1}$$

The calculation result shown in Figure 2.4 confirms that.

2.2.2 Effects of Spacial Wavelength and Metalization Percentage

The most significant design parameter of a IDC are its electrode width and the spacing between adjacent electrodes. Here one IDC's spacial wavelength (λ) is defined to be the length from edge of one electrode to the edge of the closest electrode of same voltage, as shown in Figure 2.5. Therefore

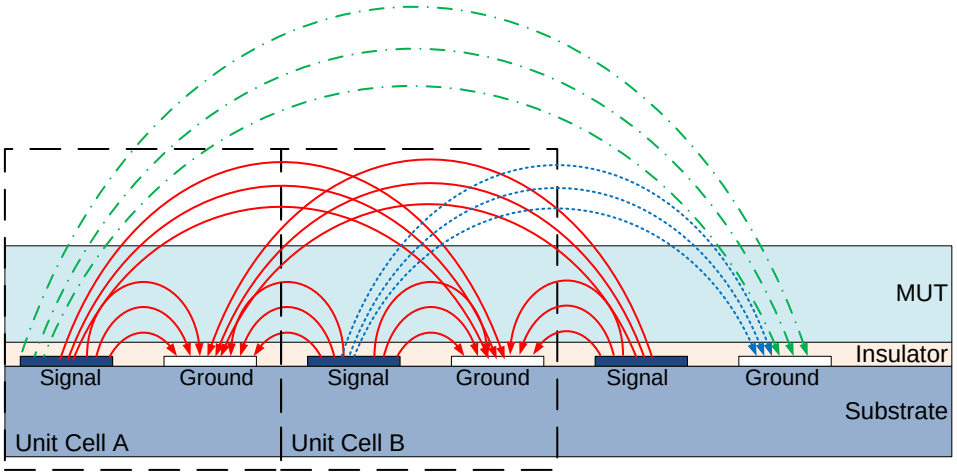


Figure 2.3: Field distribution of two different unit cells in a six-finger IDC. The blue and green field lines represents the field distribution difference between the two unit cells

spacial wavelength could be expressed as

$$\lambda = 2 \times (W + S) \tag{2.2}$$

where W is the electrode width, and S is the spacing between adjacent electrodes. The metalization percentage is defined (η) as the ratio of electrode width and half spacial wavelength

$$\eta = \frac{W}{2\lambda} \tag{2.3}$$

By comparing IDC to parallel plate capacitor, it is obvious that the spacial wavelength is analogous to the width of the electrode plates and the distance between the plates, and metalization percentage is analogous to the ratio of width and distance of plates.

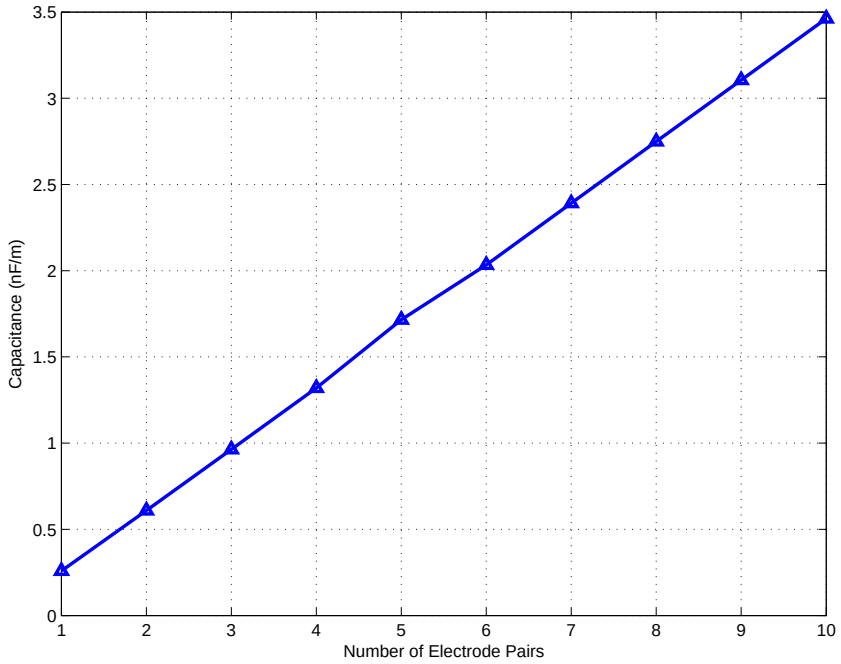


Figure 2.4: FEM simulation of single layer IDC capacitance per unit length with respect to number of electrode pairs. The widths of electrodes are 100 μm, and spacing between electrodes are 40 μm. The dielectric constant of MUT and substrate are 25 and 4, respectively

When spacial wavelength increases while metalization percentage is fixed, the total area of electrodes increases, which will increase total capacitance. At the same time, the spacing between electrodes will increase as well, which will decrease the total capacitance. In the parallel plate capacitor case, if the metalization percentage is fixed, the ratio of width and distance does not change, thus the total capacitance remains the same as the sum of width

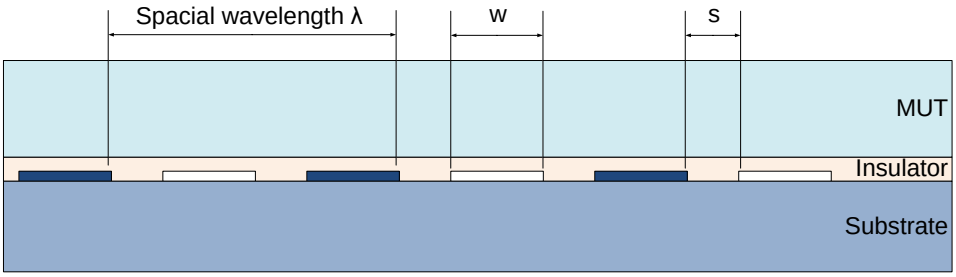


Figure 2.5: Illustration of design parameters: spacing wavelength

and distance changes, expressed as follows

$$\begin{aligned} C_{total} &= \epsilon \times \frac{S}{d} \\ &= \epsilon \times L \times \frac{W}{d} \\ &= \epsilon \times L \times \textbf{Constant} \end{aligned} \tag{2.4}$$

where L is the length of the plates.

However in the IDC case, the effect of increasing spacing between adjacent electrodes plays a more important role than electrode width. The reason is that the effect of increase of spacing between electrodes needs to multiply a factor when reflected in the total capacitance. As shown in Figure 2.3, electric flux from one electrode travels in a circle path to another electrode. Hence the factor is approximately 2π. By considering the effect of both increase of area and increase of distance between electrodes, total capacitance will decrease a little bit as λ increases and η remains the same, as shown in Figure 2.6(a).

When metalization percentage increases while the spacial wavelength is fixed, total capacitance will increase more obviously, as shown in 2.6(b). The

reason is that the spacing between electrodes will decrease and the electrode area will increase. Both changes will increase total capacitance instead of the increase/decrease trade-off in the previous discussion.

Another factor worth looking at is the total IDC area. When total area is fixed, the number of electrode pairs is related to spacial wavelength. As spacial wavelength decreases, number of electrode pairs will increase significantly, thus contribute to total capacitance. Note that decreasing spacial wavelength itself can increase capacitance also, although the effect is not so obvious when number of electrode pairs is fixed. Figure 2.7 shows the capacitance change when total area and metalization percentage is fixed.

2.2.3 Electrode Length

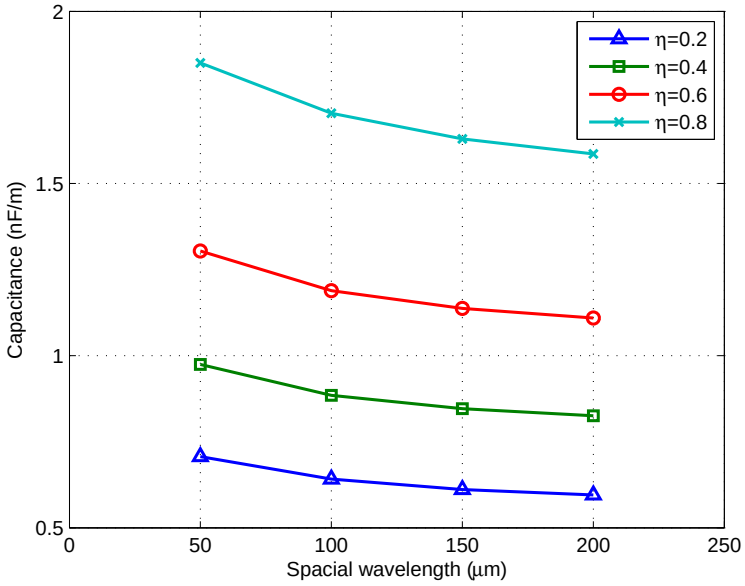
The electrode length is defined as the overlap length of two adjacent electrodes as shown in Figure 2.8. The length is proportional to the total capacitance of IDC, as follows.

$$C_{total} = LC_{unitlength} \tag{2.5}$$

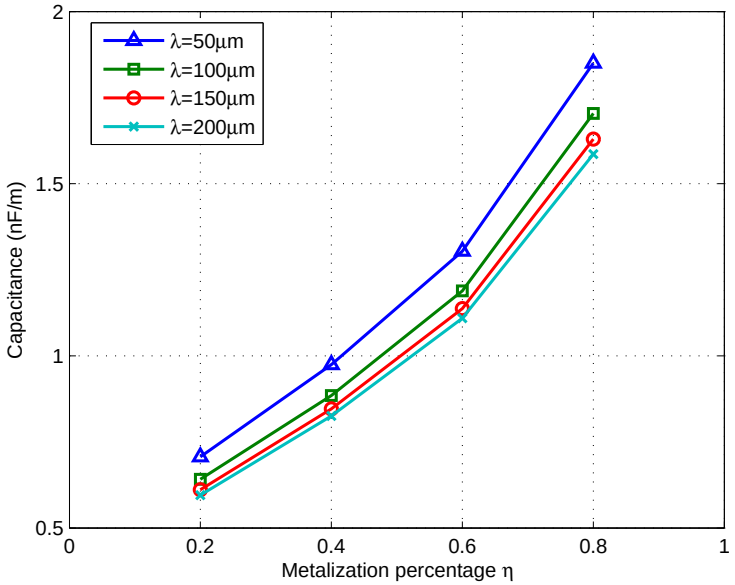
where C_{total} is total capacitance of IDC, $C_{unitlength}$ is capacitance per unit length, and L is electrode length.

2.2.4 Electrode Thickness

Another parameter is the thickness of the electrodes. By increasing the thickness, the total capacitance will increase a little bit. The mechanism of



(a)



(b)

Figure 2.6: Changes of total capacitance as spacial wavelength and metalization percentage change

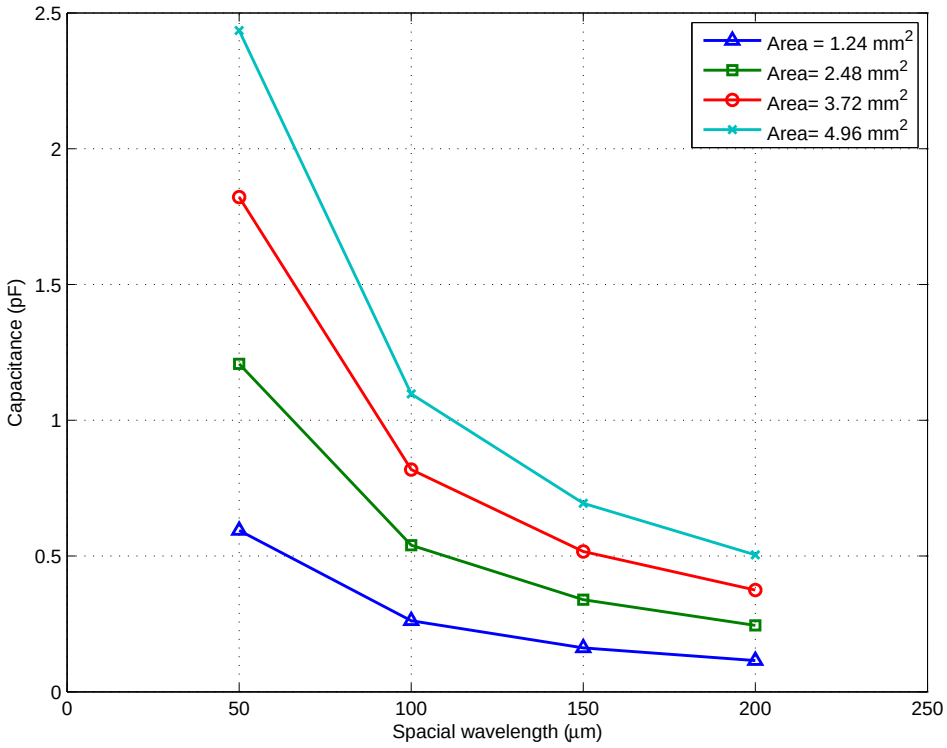


Figure 2.7: Changes of total capacitance as spacial wavelength changes and total IDC area fixed

electrodes thickness increasing total IDC capacitance is by effectively increasing the area of the electrodes. The electric field coming from one electrode to another is either from the top face of the electrodes or the side walls, as shown in Figure 2.9. Increasing thickness will increase the side wall area, hence increase the total capacitance.

In our application, the electrodes thickness are in the range of 0.1 μm to 0.2 μm. The increase of capacitance due to area increase on the side wall is very small compared to total capacitance, as shown in Figure 2.10. When the

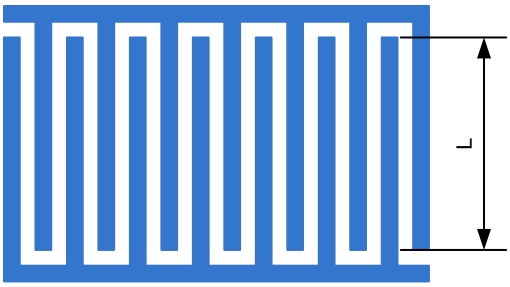


Figure 2.8: Illustration of electrode length of an IDC

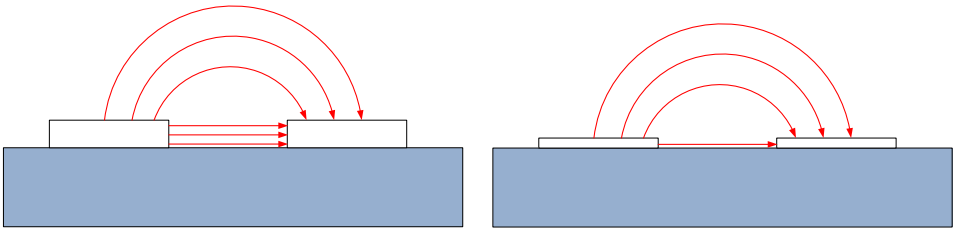


Figure 2.9: Comparison of electric field of IDCs with different electrodes thickness

thickness in increased from 0.1 μm to 0.3 μm, the capacitance only increased by 0.9%.

Therefore, the electrodes thickness is not a major design parameter that can change total capacitance significantly in planar IDCs.

2.2.5 Container Height and Substrate Thickness

In order to decide container height and substrate thickness, we need to find out how far the electric field can penetrate into the material above and under the electrodes plane. We define the penetration depth as the distance where if we remove the material in area farther than this distance, the total capacitance change is less than 1%, as penetration depth. Basically the ma-

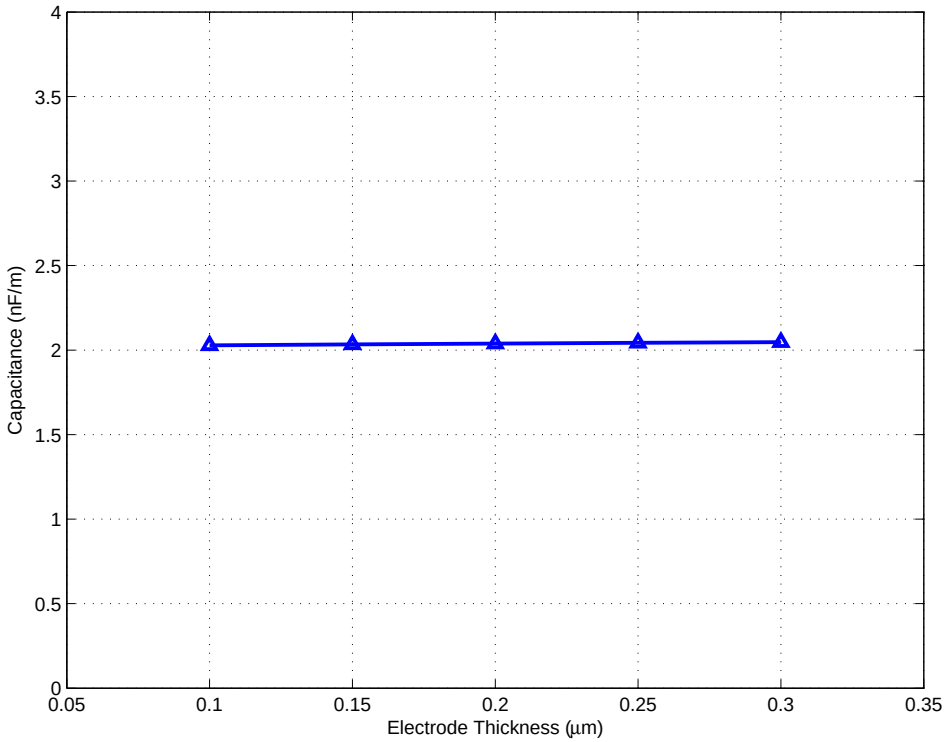


Figure 2.10: IDC capacitance variation with respect to electrodes thickness. The widths of electrodes are 100 μm, and spacing between electrodes are 40 μm. The dielectric constant of MUT and substrate are 25 and 4, respectively

terial within the penetration depth will be sensed, and will effect the total capacitance, and the error is small enough.

As discussed in previous chapter, the capacitance between two electrodes is calculated as

$$C = \int_A^B \epsilon(z)\mathbf{E}(\mathbf{z}) \cdot d\mathbf{z} \tag{2.6}$$

where z is the coordinate, which is the distance to the electrode plane, ϵ is dielectric constant between the two electrodes, and E is the electric field.

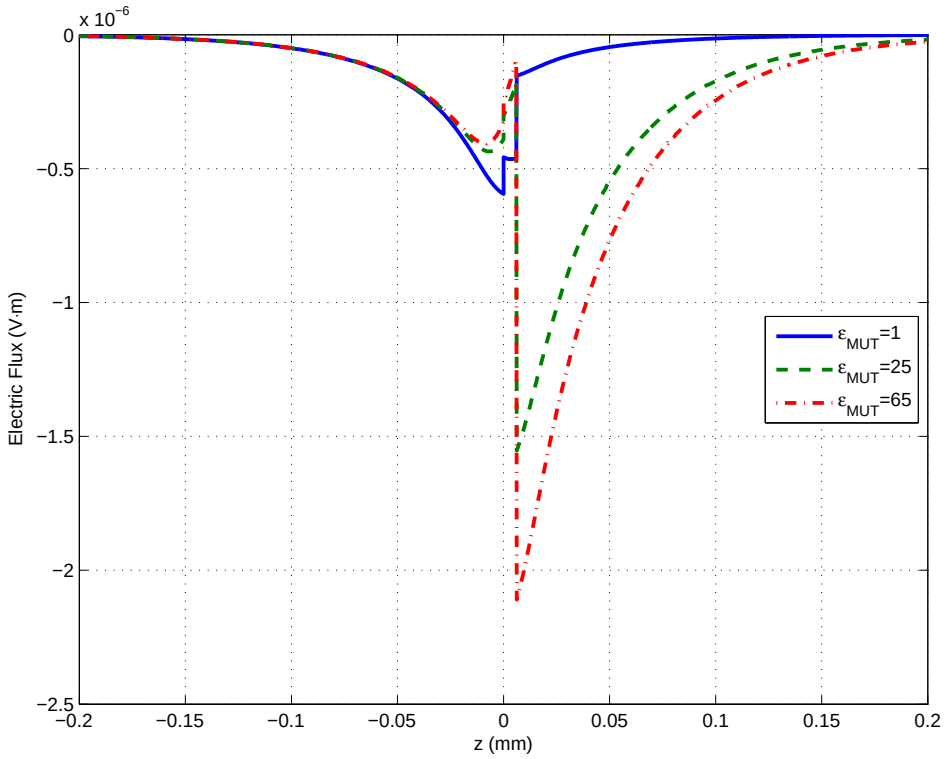


Figure 2.11: Electric flux at midpoint between two adjacent electrodes

Simulations of IDC with 100 μm width, 40 μm spacing, 6 μm insulation layer, and infinite thick layer of material with relative dielectric constant of 1, 25, and 65 have been done. Figure 2.11 shows the electric flux data extracted from simulation from bottom of the IDC's substrate to above MUT. Then integrate the electric flux from electrode plain ($z = 0$) to different distance from the plain to get partial capacitance value, and divided by the value by

integrating from electrode plane to infinity.

$$C_{partial} = \int_0^z \epsilon(z)E(z)dz \tag{2.7}$$

$$C_{total} = \int_0^{+\infty} \epsilon(z)E(z)dz \tag{2.8}$$

$$C_{normalize} = \frac{C_{partial}}{C_{total}} \tag{2.9}$$

In Figure 2.12 it can be seen that in order for the partial capacitance value to be greater than 99% of total capacitance value, that is, normalized capacitance is greater than 0.99, the distance needs to be around 210 μm for $100\mu m/40\mu m$ structure. Hence, for decent measurement accuracy, thickness of MUT should at least be one and half spacial wavelength. When designing IDC for measuring dielectric properties of thin layers, the spacial wavelength should be small enough so that most of the electric flux are confined below the top surface of MUT. We define this minimum thickness as IDC's penetration depth D_p

$$D_p = 1.5 \times \lambda \tag{2.10}$$

2.3 Mask Design

In order to observe the above discussion regarding the effects of sensor dimensions, various sensor dimensions are designed.

Group #1 The purpose of this group is to observe the effect of different metalization percentage. The spacial wavelength of IDCs in this group is

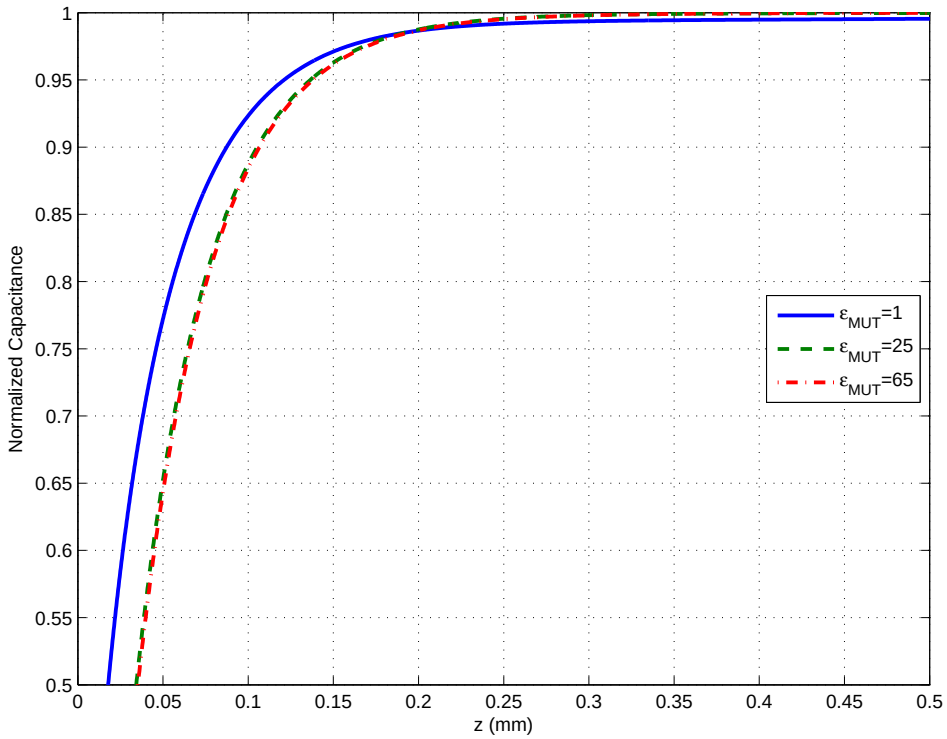


Figure 2.12: Normalized capacitance

the same, 60 μm, while the metalization percentage, or the ratio between electrodes width and spacing (w/s) are different. Deign 1-a has w/s ratio of 5; 1-b has w/s ratio of 2; and 1-c has w/s ratio of 1. The number of pairs of electrodes are all 40.

Design	Width/Spacing (μm)	Electrode Pairs	Electrode Length (μm)
1-a	50/10		
1-b	40/20	40	2000
1-c	30/30		

Table 2.1: IDC design parameters of design group #1

Group #2 The purpose of this design group is to observe the effect of different metalization percentage under a greater spacial wavelength comparing to group #1. The spacial wavelength of IDCs in this group are also the same, but with a greater value, 90 μm. The metalization percentage of design 2-a, 2-b and 2-c are the same with design 1-a, 1-b, and 1-c respectively. The number of pairs of electrodes are all 40.

Design	Width/Spacing (μm)	Electrode Pairs	Electrode Length (μm)
2-a	75/15		
2-b	60/30	40	2000
2-c	45/45		

Table 2.2: IDC design parameters of design group #2

Group #3 The purpose of this design group is to observe effect of different spacial wavelength while maintaining the same sensor area. The spacial wavelength of IDCs in this group are different, being 60 μm, 120 μm, and 300 μm respectively. The metalization percentage are all 5. The total area of three IDCs are the same. To have the same area for three IDCs, the number of pairs of electrodes are set to 40, 20, and 8 for design 3-a, 3-b, and 3-c respectively.

Design	Width/Spacing (μm)	Electrode Pairs	Electrode Length (μm)
3-a	50/10	40	
3-b	100/20	20	2000
3-c	250/50	8	

Table 2.3: IDC design parameters of design group #3

Group #4 In this group, the IDCs have different spacial wavelength and metalization percentage, only the area are the same.

Design	Width/Spacing (μm)	Electrode Pairs	Electrode Length (μm)
4-a	50/10	40	
4-b	20/10	80	2000
4-c	10/10	120	

Table 2.4: IDC design parameters of design group #4

Group #5 The two designs in this group are inherited from previous graduate student working on this project. The designs are included to check the consistency.

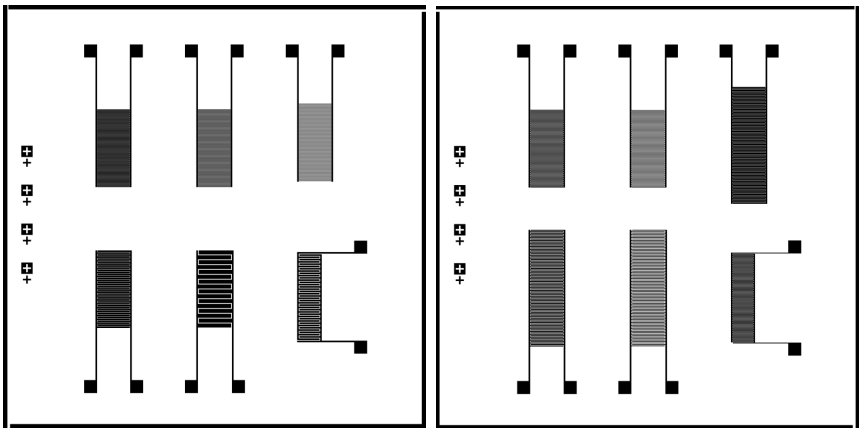
Design	Width/Spacing (μm)	Electrode Pairs	Electrode Length (μm)
5-a	100/40	20	1240
5-b	50/20	40	

Table 2.5: IDC design parameters of design group #5

All the IDCs in these groups has same electrode thickness, insulation layer thickness and liquid container height, as shown in Table 2.6.

Parameter	Value
Electrode thickness	1500 Å
Insulation layer thickness	6 μm
Container height	250 μm

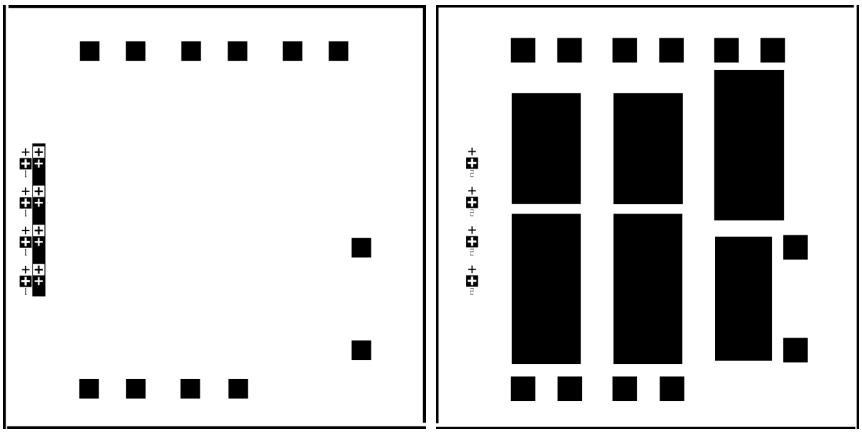
Table 2.6: IDC general design parameters



(a) (b)

Figure 2.13: Two sets of IDC design layout

Figure 2.13 and 2.14 are the layouts of the sensors mask designs.



(a) Negative PAD window mask for SU-8 insulation layer process

(b) Negative liquid container window mask

Figure 2.14: Mask # 2 and Maks # 3 for opening vias and defining liquid container

Chapter 3

Sensor Fabrication

In this section, fabrication of the IDC sensor is discussed. There are three major steps in the fabrication. First, IDC electrodes evaporation and patterning. Second, deposition of insulation layer. Third, MUT liquid container fabrication. Details are presented in the following sections.

3.1 Electrodes Patterning

Before any fabrication steps, the quartz slides are cleaned using piranha solution, which is a 3:1 mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2).

After dehydration, the quartz substrates are put into CHA E-Beam Evaporator, and a layer of aluminum with thickness of 1500 Å is evaporated. After evaporation step, the substrate is all covered by aluminum.

The next step is photolighography using mask #1. Then the samples are etched using Aluminum Etch 16-1-1-2. After etching step, the IDC electrodes are patterned on the substrate.

3.2 Insulation Layer Deposition

The insulation layer material is SU-8. In this section, detailed process steps are presented

The SU-8 used in fabrication is SU-8 2015 provided by MicroChem Corp. to fabricate the insulation layer. According to data-sheet of SU-8 2100 [14], the following fabrication recipe is used after minor adjustments. Figure 3.1 shows the process flow of fabricating SU-8 structures.

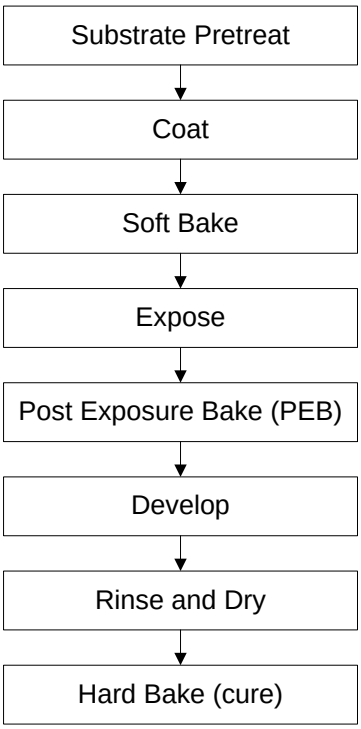


Figure 3.1: Process flow of SU-8

Substrate Pretreat SU-8, like most photoresist, is very sensitive to dust and moisture. In order to obtain maximum process reliability, substrates should be cleaned with a piranha wet etch (H_2SO_4 & H_2O_2) followed by a de-ionized water rinse. Since the electrodes are already patterned on substrate, samples are washed in Acetone, IPA and DI-water. Then the samples are put into 150 ℃ oven for 10 minutes to dehydrate.

Coat Dispense 1 ml of resist for each inch (25 mm) of substrate diameter. Spin the substrate at 500 rpm for 30 seconds with acceleration of 100 rpm/second. Then increase the spin rate for 30 seconds with acceleration of 300 rpm/second to 2000 rpm, and spin for 30 seconds.

Soft Bake The samples are put on a level hotplate to evaporate the solution in the coated resist. For 6 μm thickness, the temperature is set to 95 ℃ for 3 to 5 minutes.

Exposure According to the datasheet, exposure energy for 6 μm film is 110 to 140 mJ/cm^2. The exposure time is set to 22 seconds based on the aligner's power setting in cleanroom.

Post Exposure Bake (PEB) After exposure, PEB step is needed to let exposed area cross-link. The PEB time and temperature is set to 5 minutes at 95 ℃. Note that the substrate needs to cool down gradually after PEB to prevent thermal shock.

Develop For 6 μm film, the develop time is around 3.5 minutes. After the film is fully developed, rinse the sample with IPA.

Hard Bake To keep SU-8 as a inert structure on the chip, a hard bake step is needed. The substrate is put in 150 ℃ oven for 10 minutes.

3.3 MUT Liquid Contaner Fabrication

As discussed in Section 2.2.5, the container height needs to be at least 1.5λ. Therefore, 250 μm should be enough for all our designs except design 3-c, which has spacial wavelength of 600 μm.

In order to fabricate and pattern such thick structures, SU-8 2100 provided by MicroChem Corp has been chosen. The process flow is almost the same as fabricating insulation layer. According to data-sheet of SU-8 2100 [14], the following fabrication recipe is used after minor adjustments.

Substrate Pretreat This step is the same as described in Section 3.2.

Coat Dispense $1ml$ of resist for each inch ($25mm$) of substrate diameter. Spin the substrate at 500 rpm for 30 seconds with acceleration of 100 rpm/second. Then increase the spin rate for 30 seconds with acceleration of 300 rpm/second to 2000 rpm, and spin for 30 seconds.

Soft Bake The substrates are put on a level hotplate to evaporate the solution in the coated resist. For 250 μm thickness, the temperature is first set to 65 ℃ for 7 to 10 minutes, then 95 ℃ for 45 to 60 minutes. The purpose of the stepped heating is to prevent thermal shock to the resist layer. Another reason is to let the resist reflow (SU-8's glass temperature T_g is around 50 ℃).

To optimize the baking time and conditions, MicroChem suggests remove the substrate from the hotplate after some time. After cool down the substrate to room temperature, return it to the hotplate. If the resist film wrinkles, leave the substrate on the hotplate for more time.

Exposure According to the datasheet, exposure energy for 250μm film is 350 to 370 mJ/cm^2. The exposure time is set to 66 seconds splitting into three intervals with 22 seconds each. Splitting exposure time is to prevent burn on the surface of SU-8 film due to long time UV expose.

Post Exposure Bake (PEB) After exposure, PEB step is needed for exposed area to cross-link. The PEB time and temperature is set to 5 minutes at 65 ℃ then 15 minutes at 95 ℃. Note that the substrate needs to cool down gradually after PEB to prevent thermal shock.

Develop For 250 μm film, the develop time is around 30 minutes. We put the beaker with developer on a 65 ℃ hotplate in order to accelerate the process. The method to check whether the film is fully developed is to rinse the

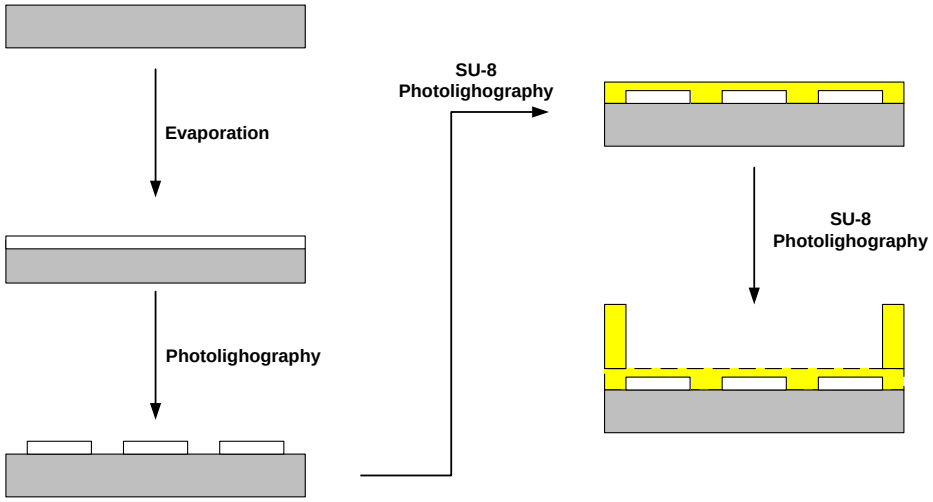


Figure 3.2: Illustration of IDC's fabrication process

substrate with Isopropyl alcohol (IPA). A White film produced during rinse means the SU-8 film is under-developed.

After the film is fully developed, rinse the substrate with IPA then DI-water.

Hard Bake To keep SU-8 as a inert structure on the chip, a hard bake step is needed. The substrate is put in 150 ℃ oven for 20 minutes.

3.4 Summary

Figure 3.2 shows the fabrication steps of evaporation, first photolithography to pattern the electrodes, second lithography to deposit insulation layer and open vias for pads, and third lithography to build liquid container.

Chapter 4

Sensor Modeling

4.1 Conformal Mapping Calculation Method

In this section, traditional conformal mapping method of calculating coplanar waveguide and interdigitated capacitor (IDC) is introduced. The limitation of conformal mapping method on liquid dielectric constant sensor modeling is discussed.

4.1.1 Capacitance Calculation Using Conformal Mapping Method

Calculations of capacitance of IDC are first developed based on calculations of wave characteristic impedance of coplanar waveguide (CPW), which could be seen as a three-finger IDC, as shown in Figure 4.1.

Conformal mapping calculation of CPW is first presented by Wen [11] and further developed by Veyres and Hanna for CPW with an insulation layer

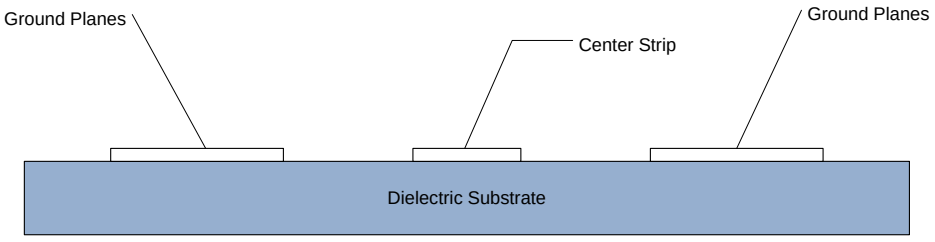


Figure 4.1: Coplanar wave guide (CPW)

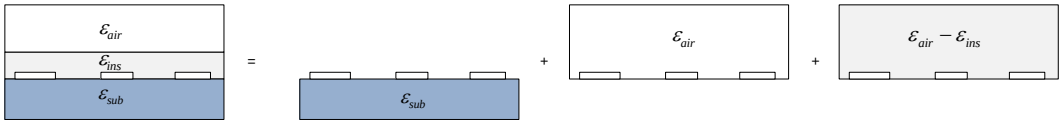


Figure 4.2: Splitting of a CPW with insulation layer according to Veyres and Hanna's capacitance model

on top of the coplanar strips [12]. Applications of the conformal mapping model on IDC calculation were presented by Gevorgian *et. al.* [1] and Igreja *et. al.* [10].

The conformal mapping methods generally used "partial capacitance technique" to create a compact equivalent circuit [10, 12, 15, 16]. For IDC with two layers of materials in the upper half plane, and one substrate, the total capacitance is splitt into three parts in parallel connection: the substrate capacitance C_{sub}, capacitance in the absence of the dielectric above the substrate C_1, capacitance when assuming that all the electric field is concentrated in the dielectric with relative dielectric constant $(\epsilon_r - 1)$. The concept of splitting the total IDC capacitance is shown in Figure 4.2.

The total capacitance is then calculated as

$$C_{total} = \epsilon_{sub} C_{sub,h=h_{sub}} + \epsilon_{air} C_{1,h=\infty} + (\epsilon_{ins} - \epsilon_{air}) C_{2,h=h_{ins}} \tag{4.1}$$

Note that $C_{sub,h=h_{sub}}$,$C_{1,h=\infty}$, and $C_{2,h=h_{ins}}$ are all geometric capacitance of one layer, which depends only on the geometric parameters of the electrodes and the height of dielectrics. Therefore, they must multiply by the dielectric constant of respective dielectrics in order to calculate the total capacitance. The

subscripts $h = h_{sub}$, $h = h_{ins}$, $h = h_{\infty}$ represents the thickness of dielectrics in particular partial capacitor.

Another issue in modeling the IDC is the fringing field at the two out-most electrodes. Gevorgian *et. al.* presented more accurate models taking into account of capacitance correction due to different electric field distribution at two out-most electrodes, as well as fringing fields effect at the ends of the electrodes when electrodes are not very long, that is, the ratio of electrode length and width is very large ($L/W >> 1$) [1]. For IDC with more than three electrodes, the total capacitance roughly increases linearly with respect to the total number of electrodes, as discussed in previous chapter.

In the following paragraphs, the conformal mapping calculation by Gevorigan *et. al.* is reviewed. Note that final results of Veyres, Gevorigan and Igreja's calculation are slightly different due to different conformal mapping sequence, but the value of them are roughly the same.

Because of the symmetry of the electrodes, the capacitance between half strips of adjacent electrodes is equal to the capacitance between one of the half strips and a virtual equipotential strip of height h laying at CC', as shown in Figure 4.3(a) and 4.3(b). The first step is mapping the semi-infinite strip $\overline{0364}$ of the Z-plane in Figure 4.3(b) on to the upper half of the T-plane in Figure 4.3(c) using function

$$T = \cosh^2(\frac{\pi z}{2h}) \tag{4.2}$$

Then the electric field lines are mapped from $\overline{01}$ to $\overline{52}$ in Figure 4.3(b)

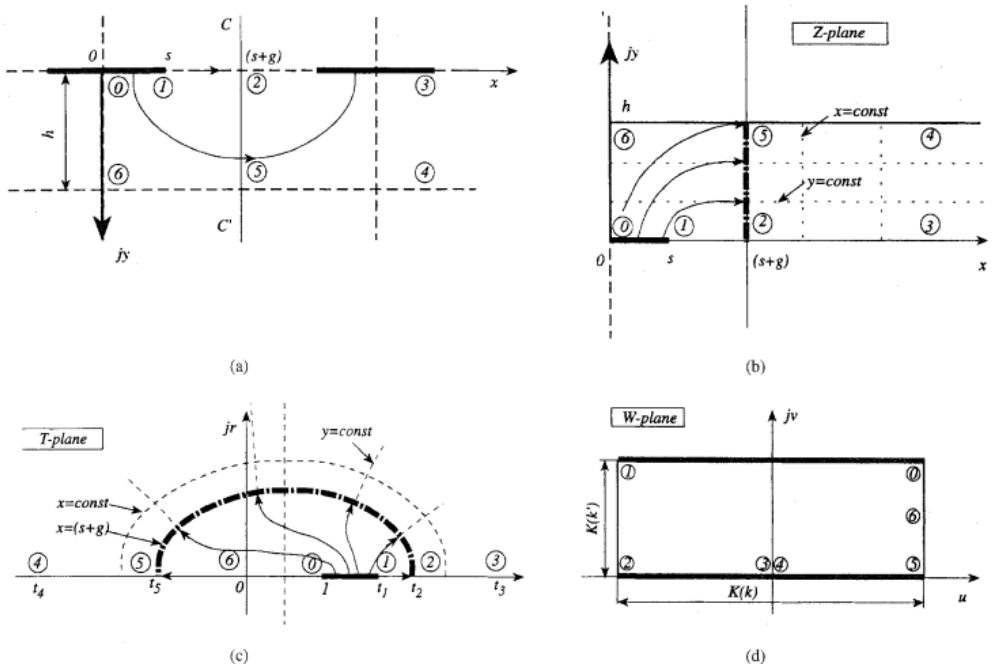


Figure 4.3: One section of a periodical electrode structure in IDC (a) and its mapped planes (b), (c), (d) [1]

to $\overline{01}$ to $\overline{52}$ in Figure 4.3(c). The vertices of the polygon in Figure 4.3(c) are

$$\begin{aligned} t_0 &= 1, \\ t_1 &= \cosh^2(\frac{\pi z}{2h}), \\ t_3 &= t_4 = \infty, \\ t_5 &= -\sinh^2(\frac{\pi(s+g)}{2h}) \\ t_6 &= 0. \end{aligned}$$

The next step is to map the upper half of T-plane to the interior of the

rectangle in W-plane in Figure 4.3(d), using function

$$w = A \int_{t}^{t_5} \frac{dt}{\sqrt{(t-t_0)(t-t_1)(t-t_2)(t-t_5)}} + B \tag{4.3}$$

From the W-plane graph, the capacitance can be calculated as

$$C_{geo} = \frac{K(k)}{K(k')} \tag{4.4}$$

where $K(k)$ is the elliptic integrals of the first kind, and k' is the complementary modulus of k, $\sqrt{1-k^2}$. The value of k is given by

$$k = \frac{\sinh(\frac{\pi s}{2h})}{\sinh(\frac{\pi(s+g)}{2h})} \sqrt{\frac{\cosh^2(\frac{\pi(s+g)}{2h}) + \sinh^2(\frac{\pi(s+g)}{2h})}{\cosh^2(\frac{\pi s}{2h}) + \sinh^2(\frac{\pi(s+g)}{2h})}} \tag{4.5}$$

Since the conformal mapping is applied to $\overline{0256}$ in Figure 4.3(a), the capacitance calculated above is in series connection with another capacitor having same value because of the symmetry. Thus, a factor of 1/2 needs to be added to C_{geo} formula.

$$C'_{geo} = \frac{1}{2} \frac{K(k)}{K(k')} \tag{4.6}$$

By plugging $h = h_{sub}$, $h = \infty$, and $h = h_{ins}$ to Equation 4.6, values of $C_{sub,h=h_{sub}}$, $C_{1,h=\infty}$ and $C_{2,h=h_{ins}}$ can be calculated. Note that in the case of $h = \infty$,

$$C'_{geo,h=\infty} = \frac{K(k_0)}{K(k'_0)} \tag{4.7}$$

where

$$k_0 = \frac{s}{s+g} \tag{4.8}$$

The above calculations are for one pair of half electrode strips. For IDC having $N/2(N > 3)$ pairs of electrodes, the total capacitance is parallel connection of $N-1$ unit capacitor. Thus the total capacitance is calculated as follows

$$C_{IDC} = (N-1)\left[\epsilon_{sub}C'_{geo,h=h_{sub}} + \epsilon_{air}C'_{geo,h=\infty} + (\epsilon_{ins} - \epsilon_{air})C'_{geo,h=h_{ins}}\right] \quad (4.9)$$

4.1.2 Limitation of the Conformal Mapping Technique

The conformal mapping calculation is quite accurate when the medium above the insulation layer is air, which has a dielectric constant of 1. Igreja *et al.* compared the calculation with Finite Element Method (FEM) calculation, and the error is under 5% [10]. Thus, the conformal mapping calculation is well suited for applications where the medium around IDC is air.

During experiments, it is found out that the calculation will introduce significant error when the medium has larger dielectric constant than air. By analyzing Equation 4.9, it can be seen that the capacitance value has linear relation ship to the dielectric constant of the medium, if ϵ_{mut} is substituted for ϵ_{air} as follows

$$C_{IDC} = (N-1)\left[\epsilon_{sub}C'_{geo,h=h_{sub}} + \epsilon_{mut}C'_{geo,h=\infty} + (\epsilon_{ins} - \epsilon_{mut})C'_{geo,h=h_{ins}}\right] \quad (4.10)$$

Figure 4.4 is the calculation result of conformal mapping method for ϵ_{mut} from 1 to 100. It can be seen that the capacitance value is a linear function of dielectric constant of ϵ_{mut}.

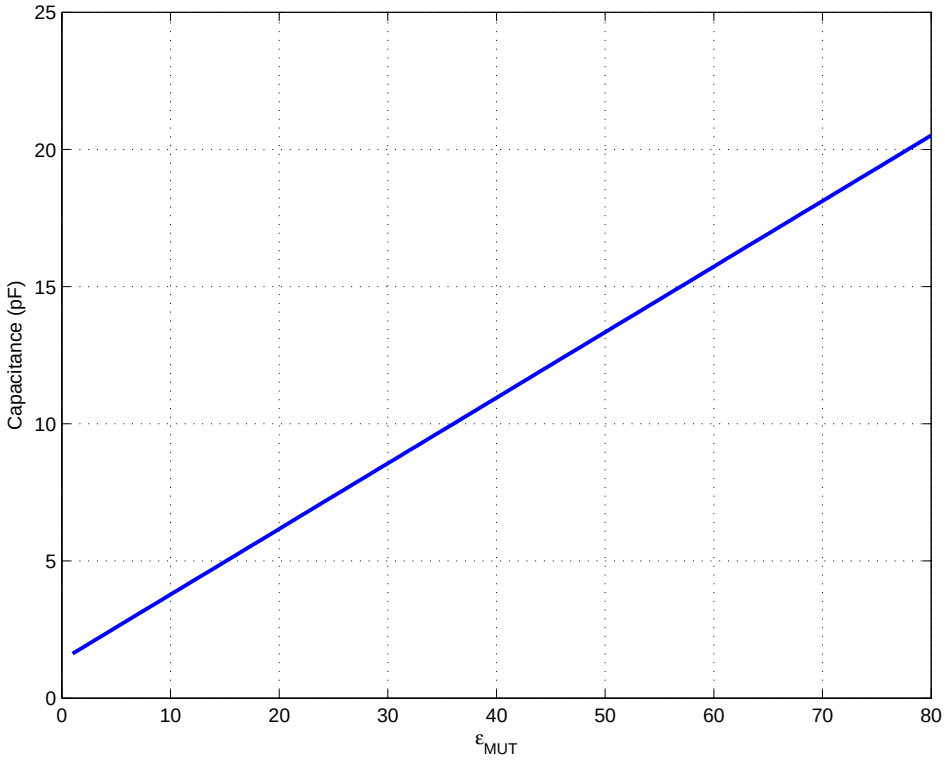
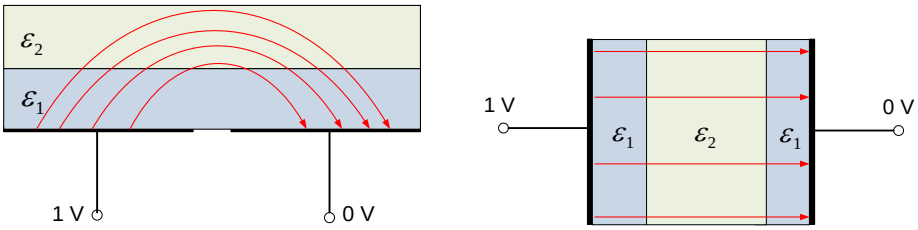


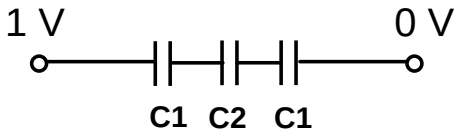
Figure 4.4: Capacitance calculation results using conformal mapping method

However, the capacitance value of a capacitor with multiple dielectrics, two in this case, is not a linear function of one dielectric constant. Instead, the capacitance will increase first and finally saturate at a maximum value. Take the parallel plate capacitor with two different dielectrics between the two plates for example. As shown in Figure 4.5, the electric fields penetrate both dielectric #1 and #2 in IDC and parallel capacitor. Thus the parallel capacitor could be actually thought of as an closed up IDC. According to basic electrostatics, the equivalent circuit of two dielectrics parallel capacitor is two capacitor connected in series, as shown in Figure 4.5(c), and total capacitance



(a) Electric field distribution in an IDC

(b) Electric field distribution when IDC is folded into a parallel plate capacitor



(c) Equivalent circuit based on field distribution

Figure 4.5: Comparison of electric field distribution between IDC and parallel plate capacitor.

is calculated as

$$\begin{aligned} C_{tot,para} &= \frac{1}{2 \times C_1^{-1} + C_2^{-1}} \\ &= \frac{1}{(2 \times \frac{\epsilon_1 S}{t_1})^{-1} + (\frac{\epsilon_2 S}{t_2})^{-1}} \end{aligned} \tag{4.11}$$

where S is the area of the parallel capacitor, t_1 and t_2 are the thickness of two dielectrics, respectively. As ϵ_1 goes to infinity while ϵ_2 remains the same, $C_{tot,para}$ is calculated as

$$C_{tot,para}|_{\epsilon_1 -> \infty} = \frac{\epsilon_2 S}{t_2} = C_2 \tag{4.12}$$

Thus, total capacitance of a parallel capacitor with two dielectrics will increase at first as ϵ_1 increases, and will approach C_2 as ϵ_1 goes to infinity. Because of similar structure, similar behavior of capacitance change is expected

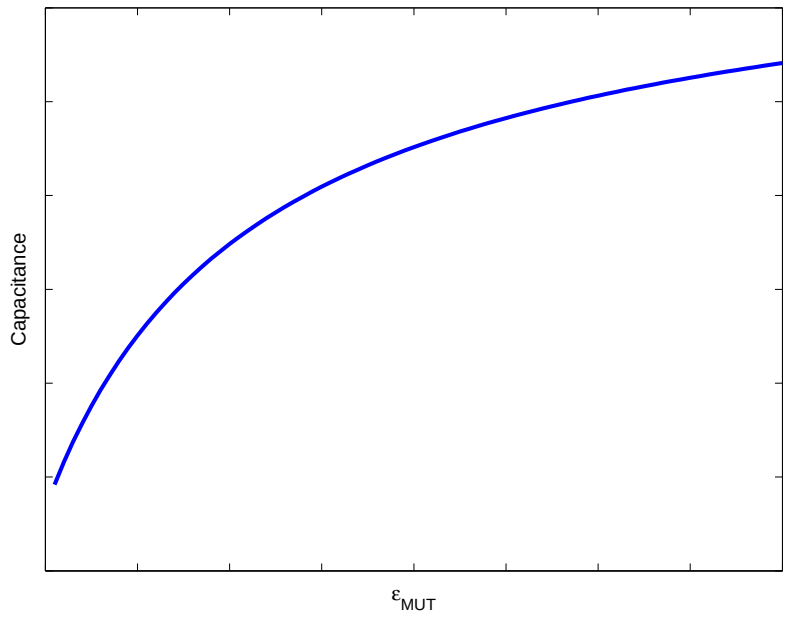


Figure 4.6: Correct capacitance behavior of two dielectrics capacitor. Note that the graph is an illustration of expected changes in capacitance, no real value is shown.

in IDC with one insulation layer. The result of Finite-Element Method (FEM) confirms this behavior, which will be discussed in following sections. Figure 4.6 shows the correct capacitance changing behavior of one capacitor with two dielectric between the plates(electrodes).

The reason of this error is introduced in the partial capacitance technique. As shown in Equation 4.1, the capacitance components are calculated as the multiplication of dielectric constant of partial dielectrics and geometric capacitance. The geometric capacitances are functions of capacitor dimensions only, which doesn't change once an IDC is designed. Therefore the total

capacitance must change linearly with dielectric constant.

However, this technique of calculating geometric capacitance is based on the assumption that conformal mapping is valid, which is not correct. Since the electric fields penetrate two different dielectrics, the fields are not continuous at the interface of the two dielectrics. The conformal mapping cannot take the discontinuity of electric fields at interface into account. Therefore, conformal mapping calculation of geometric capacitance is only valid when there is only one dielectrics, and fails when there are multiple dielectrics.

Interestingly, despite the error, the conformal mapping calculation is very close to correct value when the dielectric above the insulation layer is air, as shown in Figure 4.7. That is because air has the lowest dielectric constant, 1, thus the MUT capacitance component of air is lowest. So the capacitance component of insulation layer is assumed to be much greater. Since the capacitance components are series connected, the total capacitance is close to capacitance of IDC without insulation layer, in which case the conformal mapping holds.

Another limitation of conformal mapping calculation is that it cannot account for the losses in the IDC, since the mapping is only for electric fields and does not include the conduction currents.

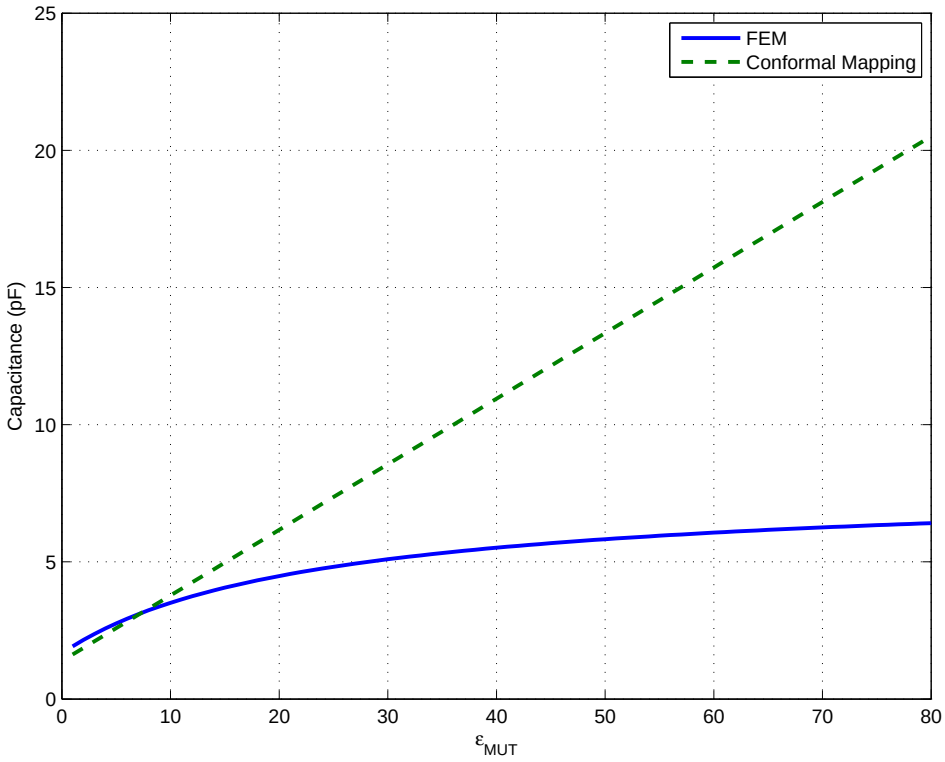


Figure 4.7: Comparison of capacitance calculation using Finite-Element Method and conformal mapping method

4.2 Finite Element Method and Limitation

4.2.1 Simulation

Since no closed analytical expression of capacitance of multiple layer IDC exists, Finite Element Method (FEM) is used to find more accurate relationship between total capacitance C_{tot} and dielectric constant of MUT ϵ_{MUT}. FEM is essentially a numerical technique to solve partial differential equations. In our particular example, the equation needs to be solved is Gauss's Law in

different subdomains or material layers

$$- \bigtriangledown \cdot d\epsilon_0\epsilon_r \bigtriangledown V = d\rho \tag{4.13}$$

while having the following boundary conditions

$$Q = C \cdot V \tag{4.14}$$

$$V = 0 \tag{4.15}$$

$$\mathbf{n} \cdot \mathbf{D} = 0 \tag{4.16}$$

where the first boundary condition applies to the interface between signal electrodes and surrounding materials, the second condition applies to the interface between ground electrodes and surrounding materials, and last condition applies the exterior boundary of the model system.

The model structure is shown in Figure 4.8. An air layer is put on top of MUT layer and below the substrate layer in order to simulate real conditions when making measurements, although as discussed in Section 2.2.5, the air layers does not affect final results significantly as long as the MUT layer is thick enough.

Figure 4.9 shows the meshed structures. Note that the thickness of electrode (1500 Å) is much smaller than the thickness of the insulation layer (6 μm), meshing of the insulation layer is separated into several parts in order to get decent meshing grid distribution.

Figure 4.10 is the simulation result. The potential distribution is illustrated in Figure 4.10(a). By looking at more closed up illustration in Figure

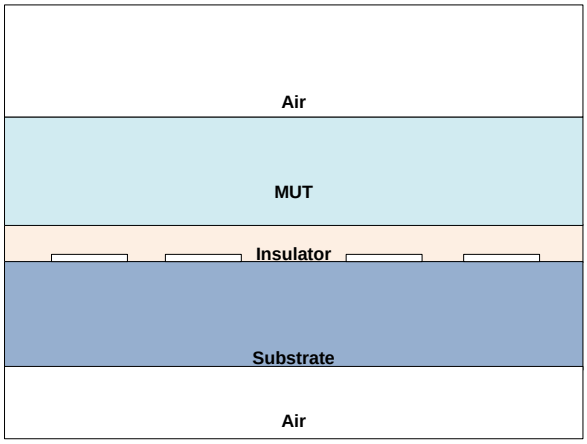


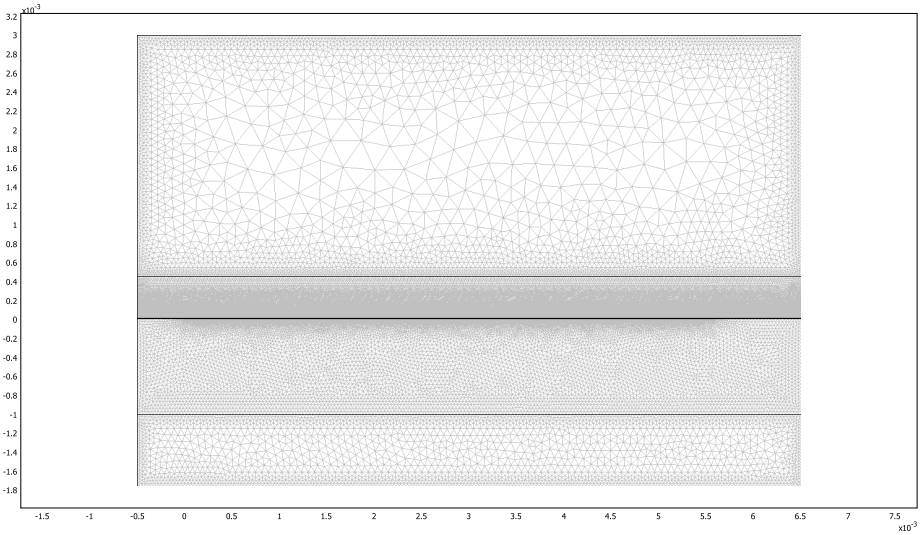
Figure 4.8: IDC and surrounding environment model in FEM simulation

4.10(b), it can be seen that the potential at midpoint between two adjacent electrodes is roughly 0.5 Volt as expected since the signal electrode potential is 1 Volt and ground electrode potential is 0 Volt.

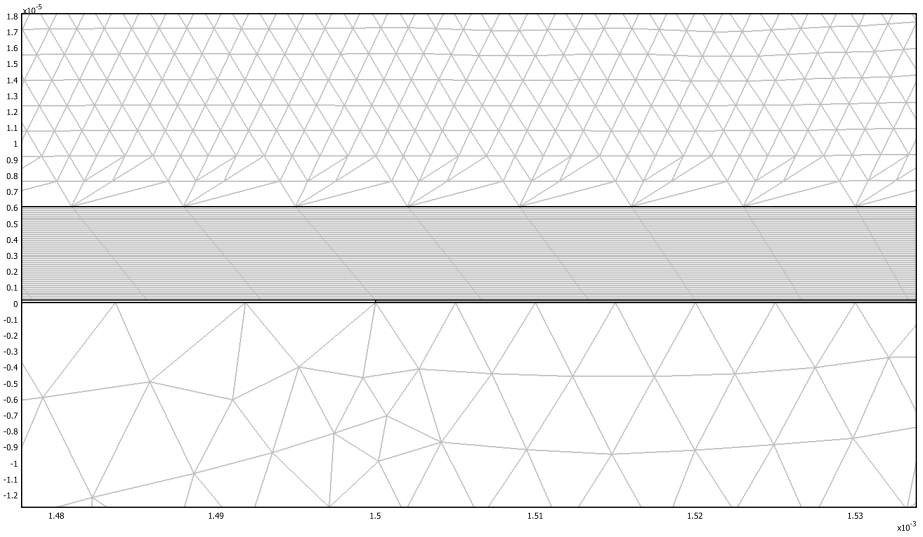
Figure 4.11 shows the simulated capacitance of IDC when the dielectric constant of MUT varies from 1 to 100 with increment step of 0.1. It can be seen that the capacitance increases as dielectric constant relatively faster at lower dielectric constant region, and the increase slows down when dielectric constant is over 50.

4.2.2 Limitation

Since FEM solves partial differential equations numerically, the results should reasonably accurate as long as the meshing is fine enough. However, the above simulation considers only the dielectric constant of MUT, and assumes the conductivity is zero, meaning there is no loss introduced by the material,

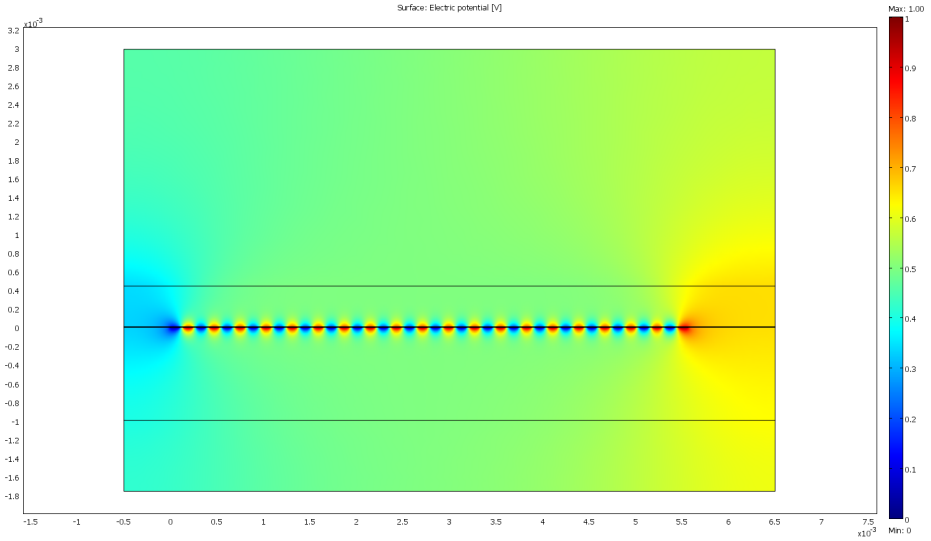


(a) Meshing results of IDC

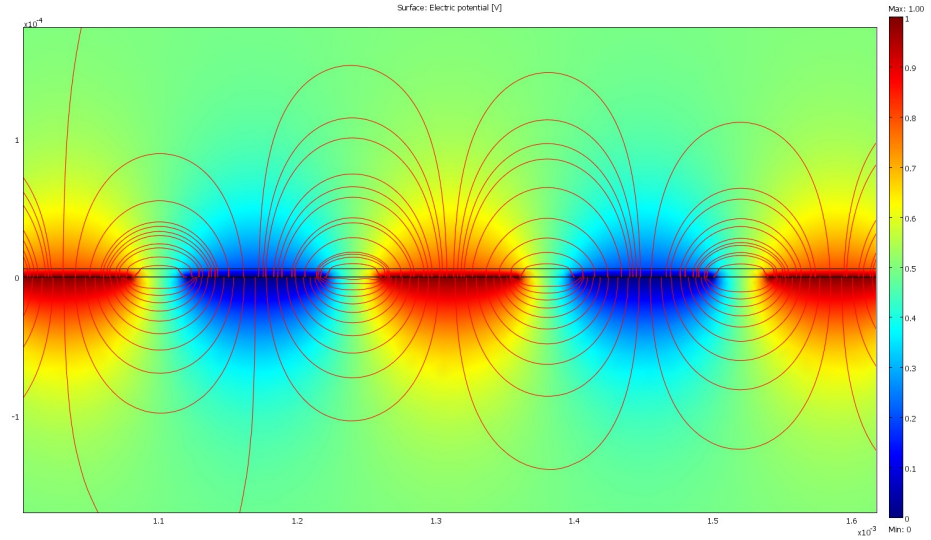


(b) Detailed illustration of meshing around IDC electrodes

Figure 4.9: Meshing results of IDC in FEM software



(a) Illustration of simulation results of whole IDC structure



(b) Closed up illustration of results near IDC electrodes

Figure 4.10: FEM simulation results. Note that the streamline represents electric field and surface plot represents potential

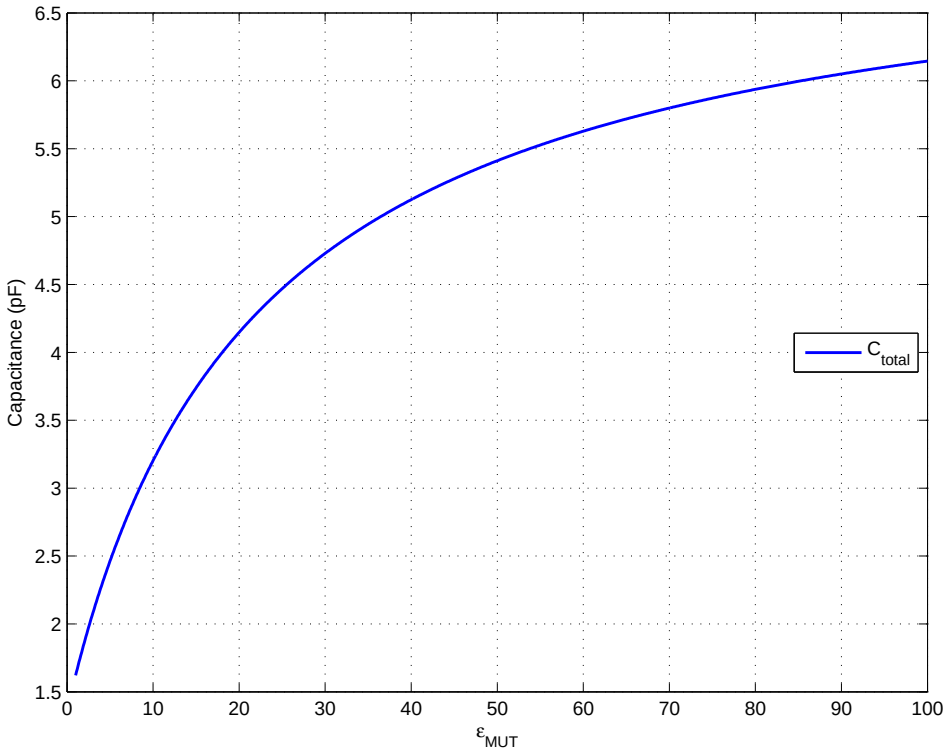


Figure 4.11: Capacitance simulation results of FEM

which does not suit our application very well.

Another options when simulating IDCs is to setting the conductivity of MUT material, and the partial differential equation in subdomains becomes

$$- \bigtriangledown \cdot d(\sigma \bigtriangledown V - \mathbf{J_e}) = dQ_j \tag{4.17}$$

where σ is the conductivity of the material, $\mathbf{J_e}$ is external current density. Hence, the conductivity property is also included in the simulation model.

However, one major drawbacks of setting conductivity of MUT is that the number of possible conductivity values is nearly infinite, unlike the value

of relative dielectric constant is almost always smaller than 100. Since the conductivity could be either very small or very large, a huge variable space needs to be covered in simulation. Considering the simulation speed of FEM is already slow[1], and there are multiple designs of IDCs, including conductivity into the simulation is not a viable solution. Hence, equivalent circuit model is still needed in order to extract conductivity from measurements, which will be discussed in the following section.

4.3 Equivalent Circuit Model Based on Electric Field Distribution

In order to utilize FEM simulation results in complex dielectric constant measurements when the MUT has finite conductivity, an equivalent circuit model needs to be built.

In conformal mapping calculation, the equivalent circuit is three parallel connected capacitance developed from partial capacitance technique, as shown in Figure 4.12.

As discussed in Section 4.1.2, the partial capacitance technique is not suitable for liquid dielectric constant sensor. Furthermore, the second term $(\epsilon_{ins} - \epsilon_{MUT})C'_{geo,h=h_{ins}}$ in Equation 4.10 will be negative if dielectric constant of MUT is greater than that of insulation layer, rendering the term negative, which does not have any physical meaning.

In order to build a equivalent circuit model that can be explained more

[1]Simulation of one ϵ_{MUT} case takes 1 minutes for the model presented in previous section

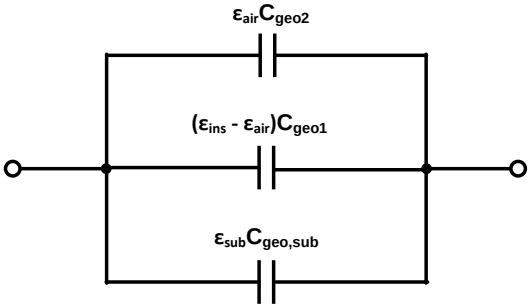


Figure 4.12: Equivalent circuit model used in conformal mapping technique, developed from partial capacitance technique

clearly in physical world, the fringing electric field path from one electrode to another needs to be analyzed . it makes more sense that both the capacitance of the insulation layer and the capacitance of MUT must be connected in series, and there might be another capacitance component representing the electric field confined in the insulation layer.

Figure 4.13 is the shows a schematic diagram of cross section view of IDC sensor with a superimposed new equivalent circuit model [17].

In the new equivalent circuit model, there are virtual electrodes on top of the insulation layer, directly above the real electrodes. Using the virtual electrodes, analyzing electric fields is more clearly. The following are the discussions of capacitance components.

MUT Capacitance ($\mathbf{C_{MUT}}$) and Substrate Capacitance ($\mathbf{C_{sub}}$) C_{MUT} is capacitance component of MUT. The electric field comes from virtual signal electrodes to virtual ground electrodes. The value of C_{MUT} is actually

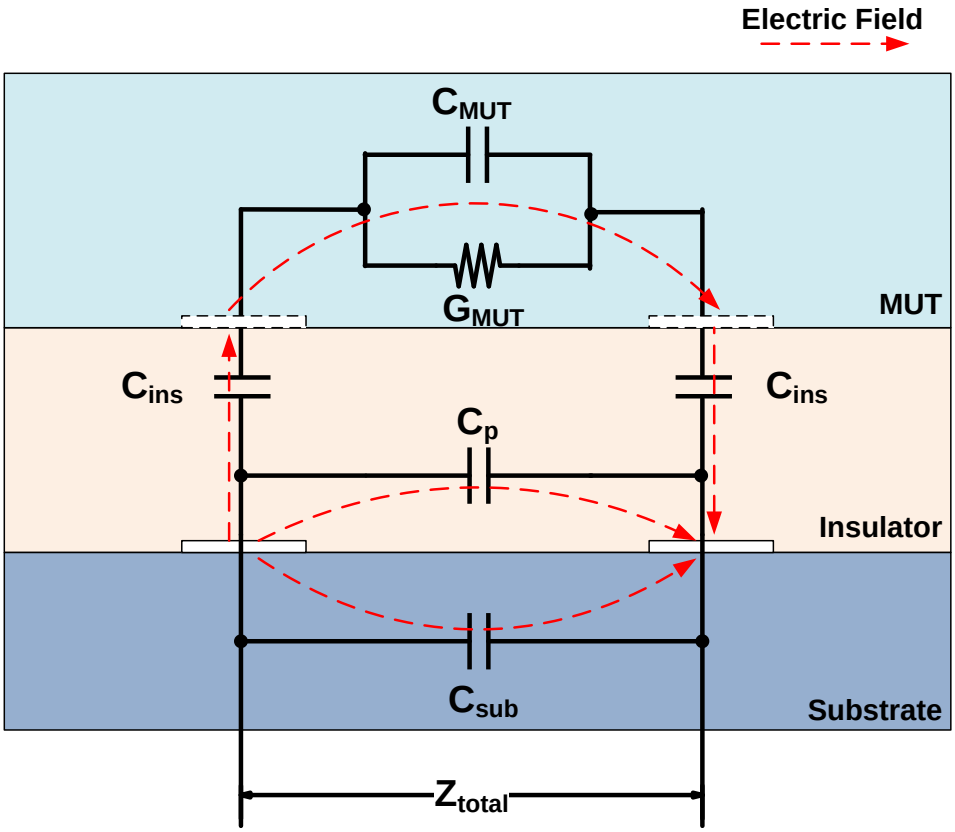


Figure 4.13: Equivalent circuit model developed from electric field distribution

capacitance of MUT component of IDC without insulation layer. Similar to C_{MUT}, substrate capacitance component is also a single layer IDC capacitance component, representing electric field in the substrate.

Insulation Layer Capacitance ($\mathbf{C_{ins}}$) C_{ins} consists of two parts. One is due to electric field coming from signal electrodes to the virtual electrodes above them. Another is due to electric field coming from virtual ground electrodes to the ground electrodes below them.

The structure and electric field distribution of C_{ins} looks like a parallel plate capacitor. For parallel plate capacitor, the capacitance depends on dielectric constant of the medium between the two plates. However, for capacitor component C_{ins} the capacitance value not only depends on dielectric constant of insulation layer, but also depends on dielectric constant of MUT. The reason is that changing dielectric constant of MUT will change the electric field distribution in insulation layer. Take two extreme cases as examples, if MUT has a huge dielectric constant, It can be thought of as a metal plate. Then most of the electric field will go directly up toward the metal plate. In this case the value of C_{ins} is similar to a parallel capacitor with same dimension. If MUT has a extreme small dielectric constant, most of the electric field will be confined in the insulation layer, resulting almost zero C_{ins} value. Therefore C_{ins} should increase as ϵ_{MUT} at first, and finally saturate at a value close to parallel capacitance of same dimension as ϵ_{MUT} continues increasing. Since the value is ϵ_{MUT} dependent, calculation or simulation needs to be done to get C_{ins} with respect to ϵ_{MUT}, which will be discussed in Section 4.4.2.

"Internal Capacitance" $\mathbf{C_p}$ C_p is the component representing electric field confined in the insulation layer. For the same reason that C_{ins} is a function of ϵ_{MUT}, C_p will be changing with ϵ_{MUT} as well because of the changing of electric field. However, the value of C_p is expected to be very small compared to other capacitor components since the thickness of insulation layer is very small.

Like C_{ins}, there is no closed form equation for C_p available. In FEM analysis, C_p could be extracted by two methods. First method is to simulate a extreme case where ϵ_{MUT} is really small in order to confine all the electric flux in the insulation layer, as explained in Section 4.4.2.2. Second method is to integrate electric field in the insulation layer area, as explained in Section 4.4.2.3. Note that the first method gets a approximate value of C_p, and the second method gets a C_p versus ϵ_{MUT} relationship.

Loss Component in MUT G_{MUT} In order to measure the conductivity of the MUT, a loss component must be incorporated into the model. G_{MUT} is parallel connected to C_{MUT} and the expression is given by

$$G_{MUT} = \frac{\sigma_{MUT}}{\epsilon_{MUT}} C_{MUT} \tag{4.18}$$

Therefore, the total impedance of the IDC is expressed as

$$Z_{tot} = \left\{ j\omega(C_{sub} + C_p) + \left[\frac{2}{j\omega C_{ins}} + \frac{1}{G_{MUT} + j\omega C_{MUT}} \right]^{-1} \right\}^{-1} \tag{4.19}$$

where

$$G_{MUT} = \frac{\sigma_{MUT}}{\epsilon_{MUT}} C_{MUT} \tag{4.20}$$

Note that the loss component of insulation layer is not included in the new equivalent circuit model. For SU-8, the loss tangent data provided by MicroChem Corp. is 0.015 at 1 GHz. Lucyszyn calculated loss tangent of SU-8 as 0.14 at 1 THz and 0.08 at 100 GHz [18]. For Si_3N_4, the loss tangent depends on deposition process. Since the insulation layer is fabricated as a

thin layer, the loss within it could be ignored compared to loss introduced by MUT.

4.4 Circuit Model Components Calculation and Simulation

In this section, capacitance components of IDC's equivalent circuit model is calculated or simulated. The IDC dimension used in this section is: 100 μm width, 40 μm spacing, 1240 μm length, and 20 pairs.

4.4.1 Single Layer Capacitance Simulation

First, the relationship between capacitance of MUT layer, C_{MUT} is needed. Since this capacitance component is essentially a single layer IDC, the calculated capacitance value by conformal mapping technique is very close to the FEM method. As shown in Figure 4.14 and Figure 4.15, the error of conformal mapping technique is around 5%. In fact, unlike C_{tot}, the error of conformal mapping calculation decreases as ϵ_{MUT} increases. In data extraction, FEM simulation results are used as C_{MUT}'s values.

4.4.2 Insulation Layer Capacitance Calculation

As discussed in Section 4.3, there is no closed form expression for C_{ins} available because of electric field distribution changing with ϵ_{MUT}. By analyzing electric field distribution, it can be seen that the value of C_{ins} should be close to the parallel plate capacitance C_{para} when ϵ_{MUT} is large, and smaller than C_{para} when ϵ_{MUT} is small.

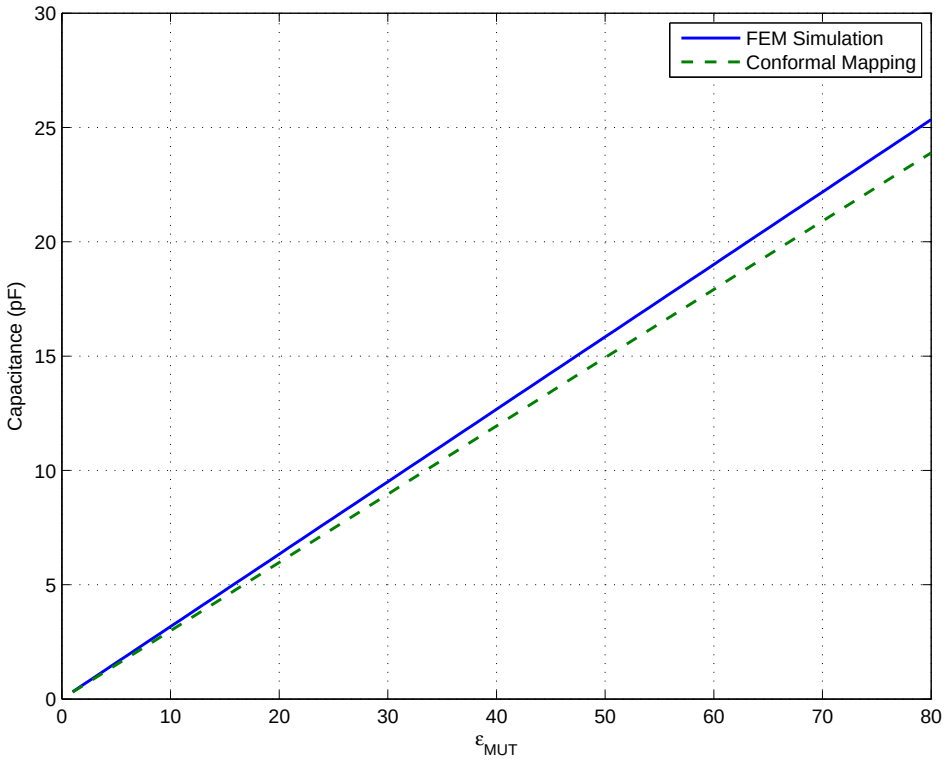


Figure 4.14: Capacitance value of C_{MUT} calculated/simulated by FEM and Conformal mapping technique

For 6 μm thickness of SU-8 layer, the parallel capacitance is calculated as follows:

$$C_{para} = N \times \frac{\epsilon_{SU8} S}{t} \tag{4.21}$$

where N is number of electrode pairs, ϵ_{SU8} equals to 3 according to MicroChem's datasheet [14], t is thickness of the layer, and S is the area of capacitor plate, which is calculated as

$$S = W \times L \tag{4.22}$$

where W and L are the width and length of electrodes, respectively. After

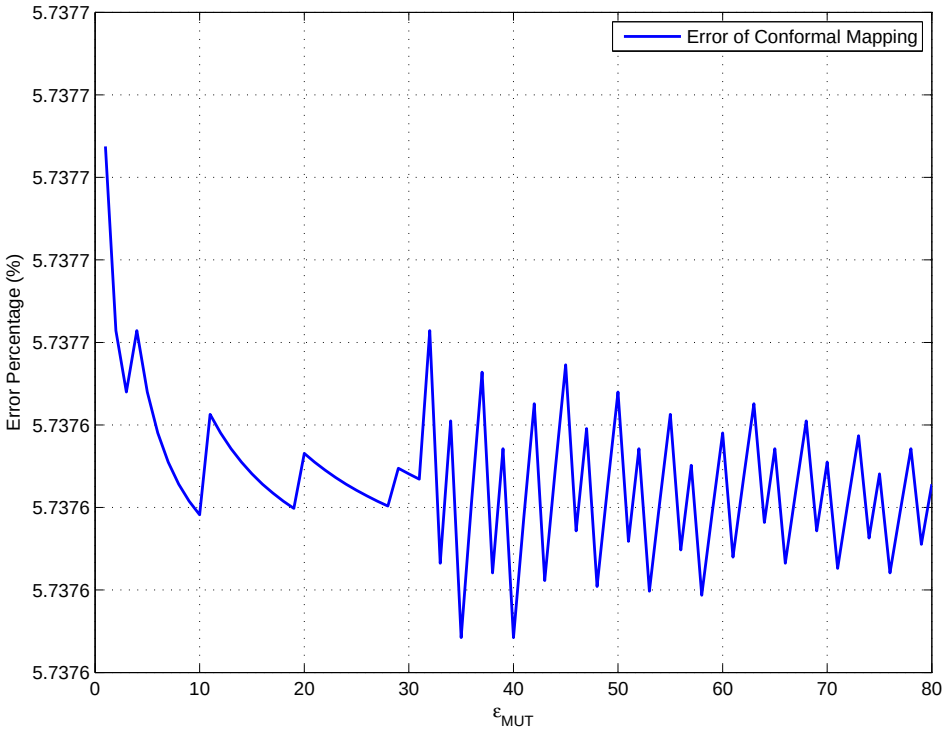


Figure 4.15: Calculation error of conformal mapping technique with respect to FEM in calculating C_{MUT}

plug in the numbers, the parallel capacitance is 10.974 pF, and this number could be used as reference in C_{ins} calculation.

Figure 4.16 shows the equivalent circuit model of IDC. It can be seen that the lower part of the model consists of C_p and C_{sub} doesn not change much with ϵ_{MUT}. Hence, C_{ins} and C_{MUT} are combined into C_{up} as follows

$$C_{up} = \frac{1}{2 \times C_{ins}^{-1} + C_{MUT}^{-1}} \tag{4.23}$$

In Section 4.4.1, capacitance of C_{MUT} is calculated. Therefore if the relationship between C_{up} and ϵ_{MUT} is known, C_{ins} can be easily calculated as

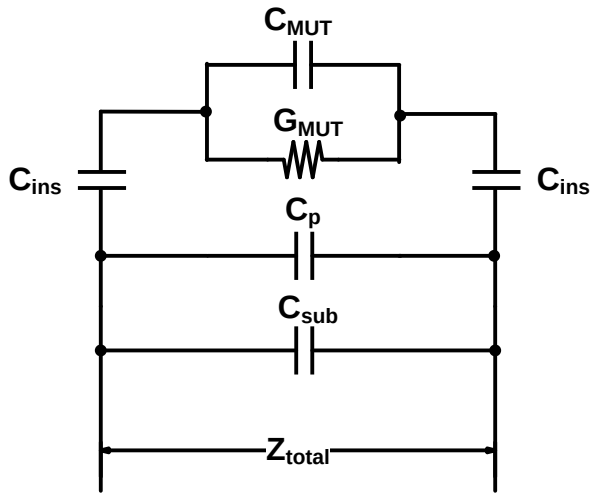


Figure 4.16: Equivalent circuit model of IDC

follows

$$C_{ins} = \frac{1}{2} \cdot \frac{1}{C_{up}^{-1} - C_{MUT}^{-1}} \tag{4.24}$$

In The following sections, three methods of deriving the relationship between C_{up} and ϵ_{MUT} are presented and results of C_{ins} calculations are compared.

4.4.2.1 Method #1: Modeling $C_{up} = C_{total} - C_{air}$

The first method is to model C_{up} equals to $C_{total} - C_{air}$, where C_{air} is total IDC capacitance when air is the MUT. Since air's relative dielectric constant is one, which is the lowest of all materials, it can be assumed that C_{MUT} of air is much smaller than that of any other materials. Also, most of the electric flux would be confined in the insulation layer, contributing to C_p, the value of C_{ins} would be small too. Therefore the C_{up} value of IDC with

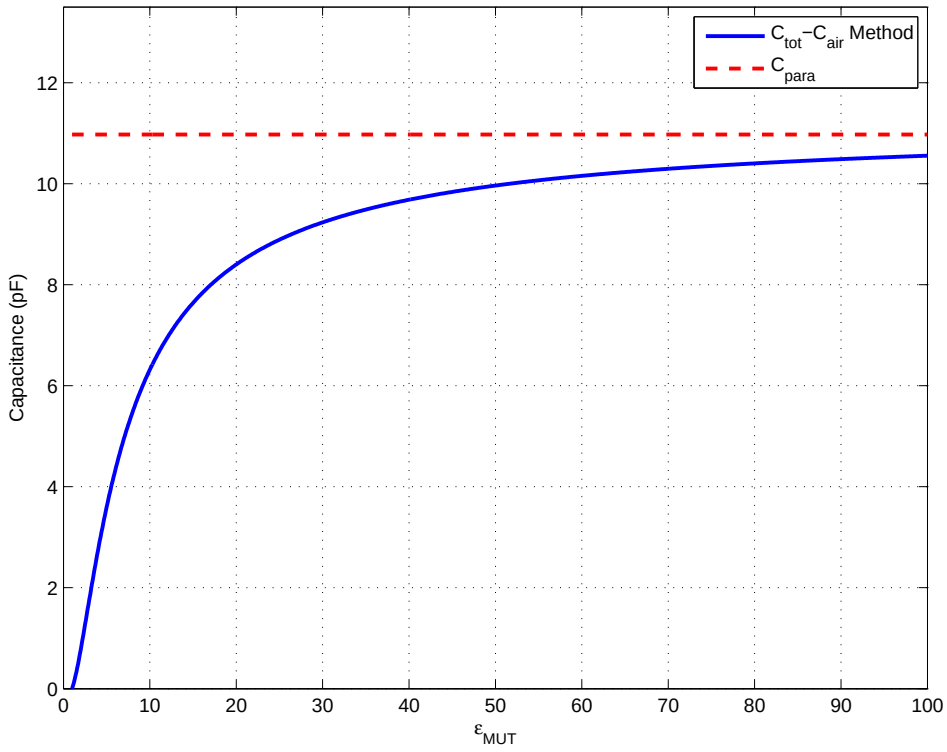


Figure 4.17: C_{ins} calculated by modeling $C_{up} = C_{tot} - C_{air}$

air as MUT is much smaller than that of other MUT, and C_{tot} of air should approximately be the sum of C_p and C_{sub}. Hence, at any dielectric constant value, we simulate the C_{tot} value via FEM, then subtract C_{tot} by C_{air} to get C_{up} value at that dielectric constant. After C_{up} is calculated, plug the value into Equation 4.24 to get C_{ins} value. Figure 4.17 shows the C_{ins} calculated by this method.

This method is the crudest method because it underestimates the value of C_{up} by subtracting too much (C_{air}) from the total IDC capacitance. It can be seen that at ϵ_{MUT} is one, C_{ins} equals to zero, which is clearly not accurate

because there must be some electric flux going up into the MUT even the dielectric constant of air is very small. Also, at higher dielectric constant of MUT, the value of C_{ins} is smaller than C_{para}. Although this method is not accurate enough in modeling, the idea of modeling C_{up} as $C_{tot} - C_{air}$ could be used in real measurement when calibration is hard to perform, which will be discussed in following sections.

4.4.2.2 Method #2: Modeling $C_{up} = C_{total} - C_0$

The second method is to model C_{up} as $C_{total} - C_0$, where C_0 is simulated with FEM when ϵ_{MUT} is extremely small. As discussed in previous sections, all the electric flux needs to be confined in the insulation layer in order to get sum of C_p and C_{sub} while suppressing C_{ins} and C_{MUT}. By setting dielectric constant of MUT extremely small, for example, $1 \times 10^{-}9$ in FEM simulation, an environment where ϵ_{MUT} is close to 0 can be realized, which cannot be realized in real situations.

As shown in Figure 4.18, the capacitance at low dielectric constant is larger compared to 4.17, which means this method is a little more close to the real values. At higher dielectric constant, specifically when the dielectric constant is larger than 60, C_{ins} calculated by this method is larger than C_{para}, meaning that this method overestimates C_{ins} at high dielectric constant region.

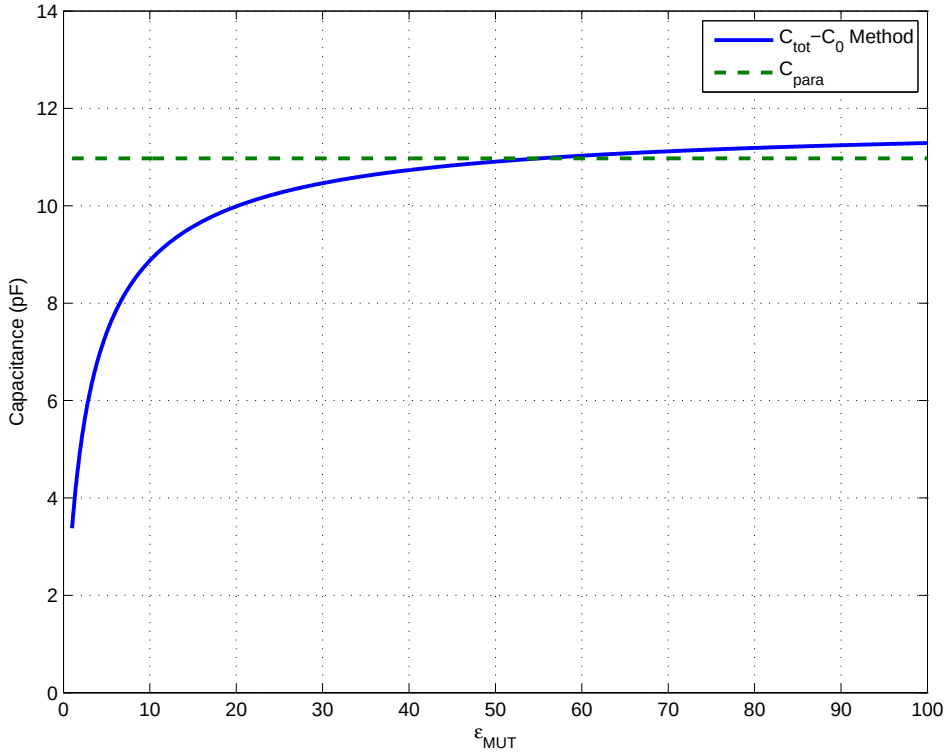


Figure 4.18: C_{ins} calculated by modeling $C_{up} = C_{tot} - C_0$

4.4.2.3 Method #3: Extraction from Capacitance Components Calculated from Electric Field Integration

The third method involves integrating electric flux in certain region to get several capacitance components respectively. As shown in Figure 4.19, the electric field at the midpoint between two electrodes should only have x component because of symmetry in this electric field distribution. Hence,the electric flux can be categorized into three kinds, as shown in Figure 4.19. And by analyzing the electric flux, it can be seen that they contribute to C_{up}, C_p and C_{sub} respectively. Therefore, the capacitance of these three components

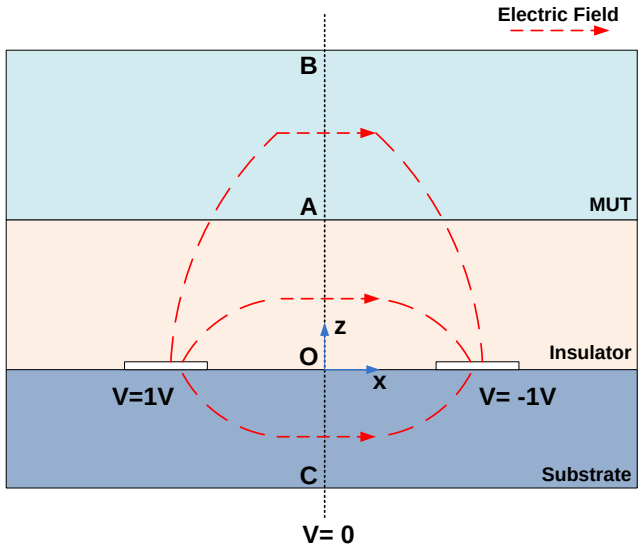


Figure 4.19: C_{ins} calculated by calculating C_{up} using integration of electric field

could be calculated by definition as follows

$$C_{up} = \frac{\int_A^B \epsilon_{MUT} E(z) \cdot dS}{V} = \frac{L \int_A^B \epsilon_{MUT} E(z) dz}{V} \tag{4.25}$$

$$C_p = \frac{\int_O^A \epsilon_{ins} E(z) \cdot dS}{V} = \frac{L \int_O^A \epsilon_{ins} E(z) dz}{V} \tag{4.26}$$

$$C_{sub} = \frac{\int_O^C \epsilon_{ins} E(z) \cdot dS}{V} = \frac{L \int_O^C \epsilon_{sub} E(z) dz}{V} \tag{4.27}$$

where A, B, C, O are coordinates in Figure 4.19, $E(z)$ is the electric field along $\overline{ABOC}$, which could be extracted from FEM simulation results, L is the length of electrodes, and V is the potential difference between signal and ground electrodes.

The capacitance components calculated by integration is shown in Figure 4.20. It can be seen that C_p is much smaller than other components, and

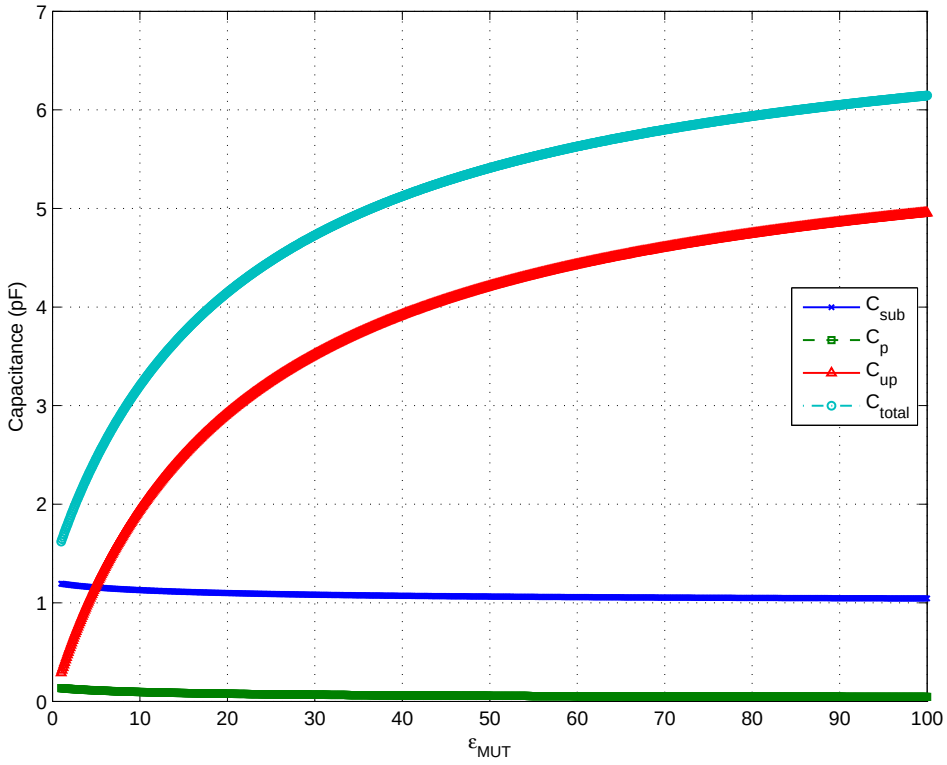


Figure 4.20: Capacitance components calculated by integration technique

C_p and C_{sub} are nearly constant as expected.

After plug the C_{up} numbers into Equation 4.24, C_{ins} could be calculated and shown in Figure 4.21 along with C_{ins} calculated by previous two methods and C_{para} as reference.

It can be seen that at lower dielectric constant region, C_{ins} calculated by integration method is closest to C_{para}, further measurement and extraction shows that this is the most accurate model in this region, which will be discussed in following chapters. At higher dielectric constant region how-

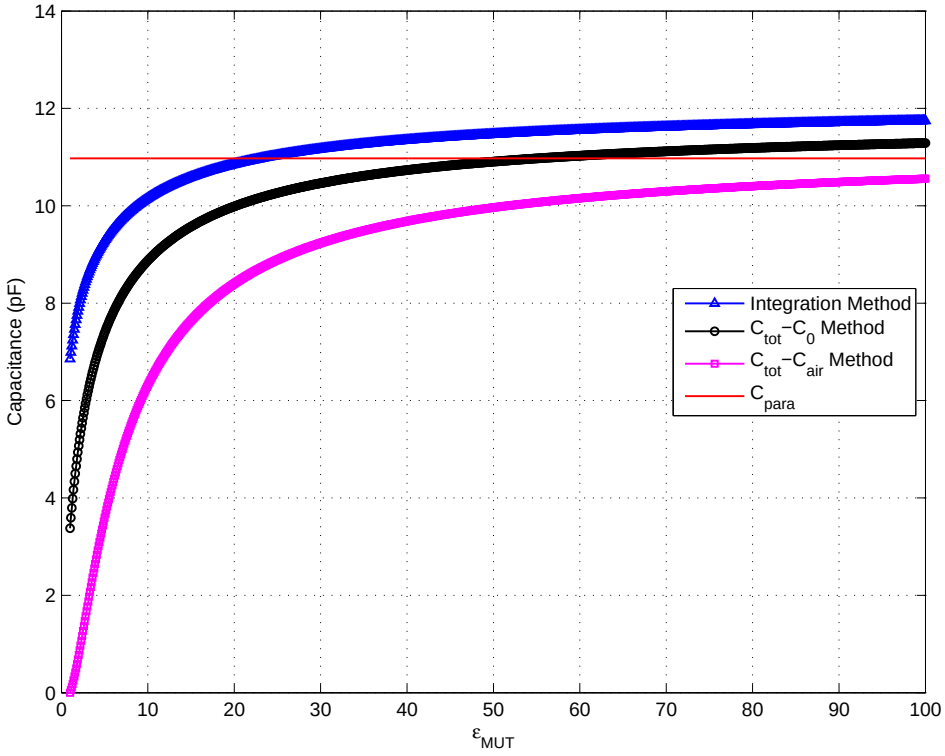


Figure 4.21: Comparison of three methods of calculating C_{ins}

ever, integration method tends to overestimate C_{ins}, and by modeling C_{up} as $C_{tot} - C_0$ renders result closest to C_{para} reference.

4.5 Iterative Parameter Extraction Algorithm

Now that all the capacitance components of the equivalent circuit model are derived and presented in Section 4.3, a method to extract the liquid dielectric properties needs to be developed when the total impedance of the IDC with MUT on top is known and dielectric properties needs to be extracted. In this section, a iterative algorithm for extracting dielectric constant and

conductivity of MUT is presented.

4.5.1 Iteration Algorithm

Since the dielectric properties are contained in component G_{MUT}, C_{ins} and C_{MUT}, the primary objective is to extract the admittance[2] of insulation layer and MUT layer Y_{up}. That could be obtained by subtracting C_p and C_{sub} from Y_{total}

$$Y_{up,measured} = Y_{total,measured} - j\omega C_{p,model} - j\omega C_{sub,model} \tag{4.28}$$

and $C_{up,measured}$ could be calculated from imaginary part of $Y_{up,measured}$

$$C_{up,measured} = \frac{\Im(Y_{up,measured})}{\omega} \tag{4.29}$$

After $C_{up,measured}$ is calculated, it is compared to $C_{up,model}$ from one of the three method presented in the previous section to get a crude estimate of $\epsilon_{MUT,est}$. Note that this $\epsilon_{MUT,est}$ is far from the final extraction because $C_{up,model}$ value is derived from FEM simulation and does not have any loss considered.

The next step is to go back to Y_{up}, shown in Figure 4.22 to start iterative calculation. According to our equivalent circuit model, Y_{up} could be expressed

[2]The reason to choose admittance instead of impedance is that C_p and C_{sub} are parallel connected in the circuit, so using admittance would render easier calculation.

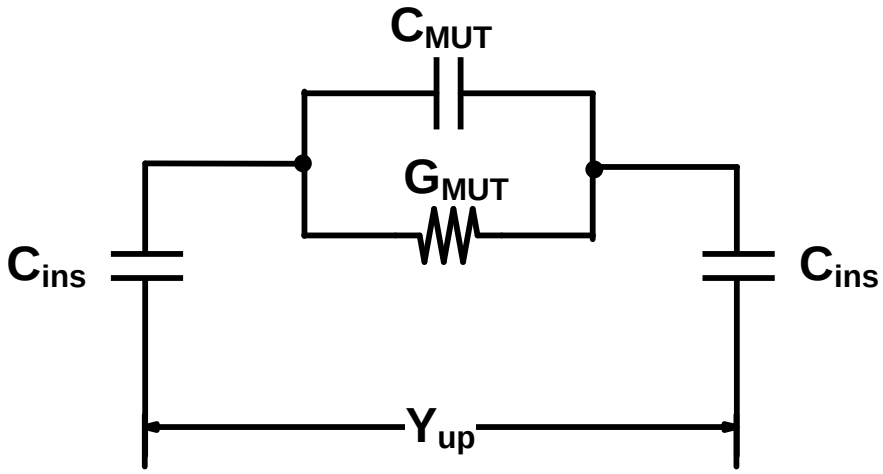


Figure 4.22: Equivalent Circuit of Y_{up}

as follows

$$\begin{aligned} Y_{up} &= \frac{Y_{ins}Y_{MUT}}{Y_{ins}+Y_{MUT}} \\ &= \frac{j\omega C_{ins}(G_{MUT}+j\omega C_{MUT})}{G_{MUT}+j\omega(C_{MUT}+C_{ins})} \end{aligned} \tag{4.30}$$

where

$$G_{MUT} = \frac{\sigma_{MUT}}{\epsilon_{MUT}} C_{MUT} \tag{4.31}$$

Note that C_{MUT}, C_{ins} and G_{MUT} are all functions of dielectric constant ϵ_{MUT}, and G_{MUT} is a function of conductivity σ_{MUT} as well. After expanding Equation 4.30, the real and imaginary part can be separated, and both part should be function of ϵ_{MUT} and σ_{MUT}. The function should look like this

$$Y_{up} = G_{up}(\epsilon_{MUT}, \sigma_{MUT}) + j\omega C_{up}(\epsilon_{MUT}, \sigma_{MUT}) \tag{4.32}$$

Since the estimate value of ϵ_{MUT} is derived from the imaginary part, we now plug $\epsilon_{MUT,est}$ into the real part of $Y_{up,measured}$, and solve for $\sigma_{MUT,iter1}$.

Then plug $\sigma_{MUT,iter1}$ into imaginary part of $Y_{up,measured}$ to solve for $\epsilon_{MUT,iter1}$. After several iteration, converged value of ϵ_{MUT} and σ_{MUT} can be derived as extraction results. The following steps summarized the how the iterative algorithm is realized.

1. Measured Y_{total} at specific frequency range
2. At one frequency, get $Y_{up} = Y_{total} - Y_{down}$
3. Get $\epsilon_{MUT,est}$ from imaginary part of Y_{up}
4. Plug $\epsilon_{MUT,est}$ to real part of Y_{up} and solve for σ_{MUT}
5. Plug σ_{MUT} to real part of Y_{up} and solve for $\epsilon_{MUT,est}$
6. Repeat step 4 and 5 until converge
7. Repeat step 2 to 6 to get extracted ϵ_{MUT} and σ_{MUT} at every frequency point

Chapter 5

Measurements and Discussion

In this section, the measurement setup of IDCs is presented. Then the measurement results as well as dielectric properties extraction results are presented and discussed. Finally, the limitation and error source of this measurement setup is discussed.

5.1 Measurement Setup

HP4194A impedance analyzer is used to measure the IDCs. The frequency range of the impedance analyzer is 100 Hz to 40 MHz, which is enough fro our impedance analysis.

The real problem when measuring the IDCs is that the impedance (or capacitance) of the IDCs are relatively small. Hence the cable connecting the impedance analyzer with IDCs will introduce significant parasitic capacitance and inductance. Although Open-Short-Load compensation is provided in the impedance analyzer and can remove most of the parasitics, the result of the compensation is still not good enough, since we are effectively subtracting a large impedance (parasitics) from a small impedance (IDC).

Therefore, in order to proceed to next experiments, removing the par-

asitic long cable from the measurement is necessary.A direct measuring approach is used by connecting the IDC to a RCA-BNC connector, and plug the connector directly to the impedance analyzer. Two wires are soldered to RCA-BNC connector, and then attached to the IDC pads using silver epoxy.

The advantage of this direct measurement approach is that it removes all the parasitics introduced from the long cable by moving the connection to IDC back to the impedance analyzer. Also, since there is only one connector between IDC and impedance analyzer, the parasitics remains a constant once the connections are made, unlike using cable when movement of cable will also introduce variable parasitics.

5.2 Impedance Measurement Results

In this section, the measurement results are presented. Although the impedance analyzer has build-in equivalent circuit models, "raw" impedance data are still needed in order to use our extraction algorithm. Hence, the data from impedance analyzer are most basic frequency versus magnitude and phase of the impedance. We then calculated real and imaginary part of the impedance and get total capacitance and conductance after that. The equations we used are as follows

$$Z_{tot} = Y_{tot}^{-1} = R_{total} + \frac{1}{j\omega C_{tot}} \tag{5.1}$$

$$C_{tot} = \frac{\Im(Y_{tot})}{\omega} \tag{5.2}$$

$$G_{tot} = \Re(Y_{tot}) \tag{5.3}$$

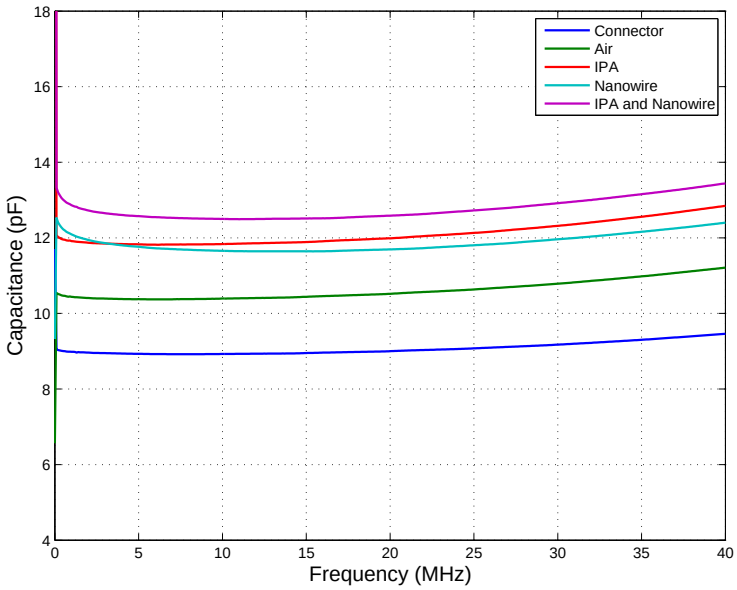


Figure 5.1: "RAW" capacitance values of measured materials

Figure 5.1 shows the "raw" capacitance value of different measurements. Note that the capacitance values here also include the RCA-BNC connector, hence we call them "raw" values. The capacitance of bare connector is also shown in the figure. The germanium nanowires are provided by Dr. Brian Korgel's research group in Department of Chemical Engineering in The University of Texas at Austin. Table 5.1 shows the known relative dielectric constant of the materials measured. It can be seen that the values of "raw" capacitance are as expected, as material with higher dielectric constant would have higher capacitance.

Material	Relative Dielectric Constant ϵ_r
Air	1
Germanium	10
Isopropyl Alcohol	18
DI Water	80

Table 5.1: Relative dielectric constant of measured materials

Figure 5.2 shows the conductance of measurements with different MUTs. Figure 5.3 shows the loss tangent of the same measurements. The conductance and loss tangent represents the conductivity or how lossy is the MUT. The loss tangent is calculated as

$$tan\delta = \left| \frac{\Re(Z_{tot})}{\Im(Z_{tot})} \right| \tag{5.4}$$

It can be seen that air has lowest loss. IPA having such high loss tangent is unexpected, since IPA is normally considered as a low loss material. The reason will be discussed in following section.

5.2.1 Method of Removing Connector Parasitics

Although using direct connection measurement could reduce parasitics introduced by cable, it can be seen that the capacitance of the bare connector is very close to IDCs with MUT applied. So the problem of removing parasitics of measurement setup still exists. Figure 5.4 shows the equivalent circuit model of IDC connected with admittance of connector. Since the connector is parallel

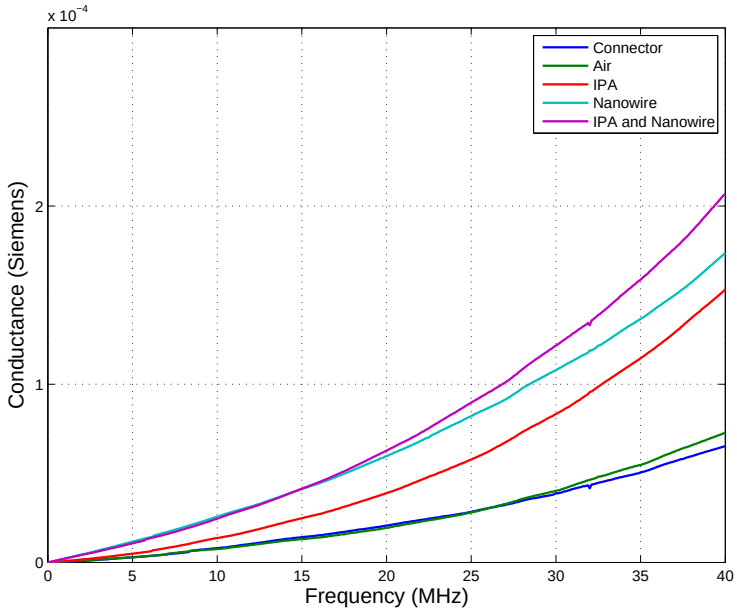


Figure 5.2: "RAW" conductance values of measured materials

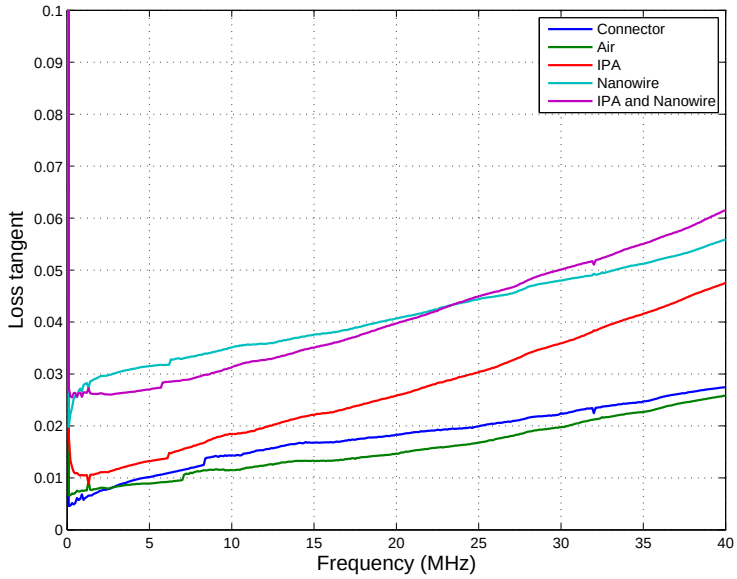


Figure 5.3: "RAW" loss tangent values of measured materials

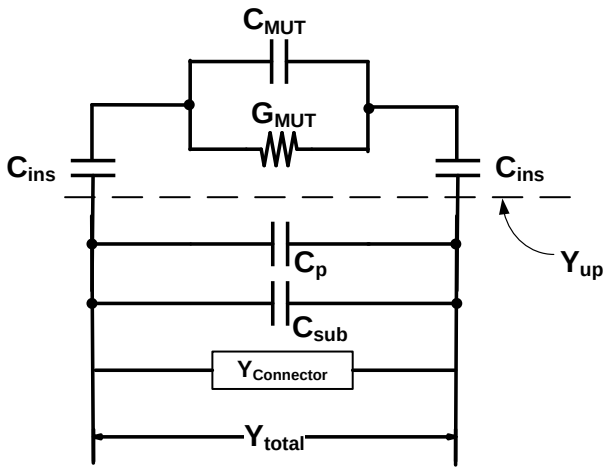


Figure 5.4: Equivalent circuit model with admittance of connector added.

connected with the IDC, the admittance of IDC is simply total admittance measured minus admittance of the connector.

One approach is to measure the connector without IDC attached first and get admittance data of the connector. Then in the extraction period, this admittance data could be subtracted from total admittance of IDC and connector. However, the drawback of this approach is that when attaching the connector to IDCs, the admittance of the connector will change more or less. Hence the value becomes an unknown again.

Another approach is to subtract the admittance of IDC in air from admittance of IDC with other MUT applied. As discussed in Section 4.4.2.1, admittance of IDC in air is the lowest admittance one can get in real measurement. Also note that by subtracting admittance of IDC in air from other measured admittance not only connector admittance is removed, but also ca-

pacitance of substrate C_{sub} and internal capacitance C_p, which means the admittance left should be close to Y_{up} needed in the iteration algorithm. The drawback of this approach is that the dielectric properties of air or any material with relative dielectric constant close to 1 can not be extracted accurately.

5.3 Extraction Results

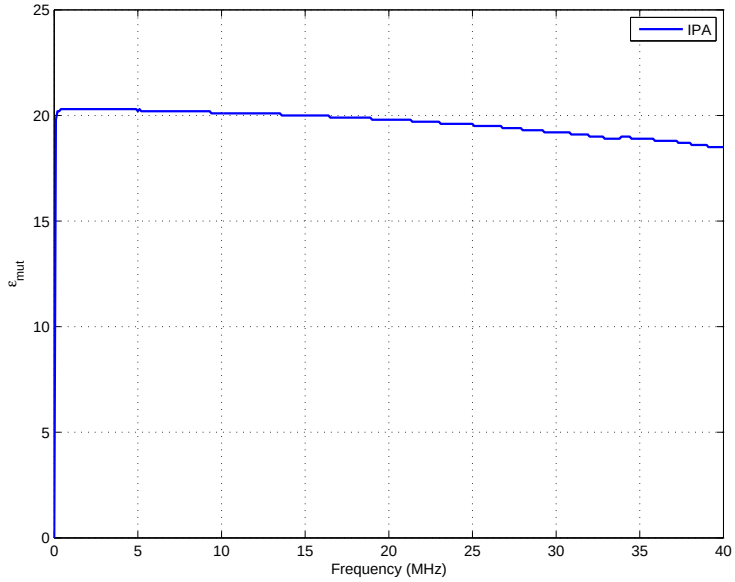
In this section, the extraction results of different MUT are presented. The second approach of removing connector parasitics is used by subtracting admittance of IDC in air from each measured admittance.

5.3.1 IPA Measurements

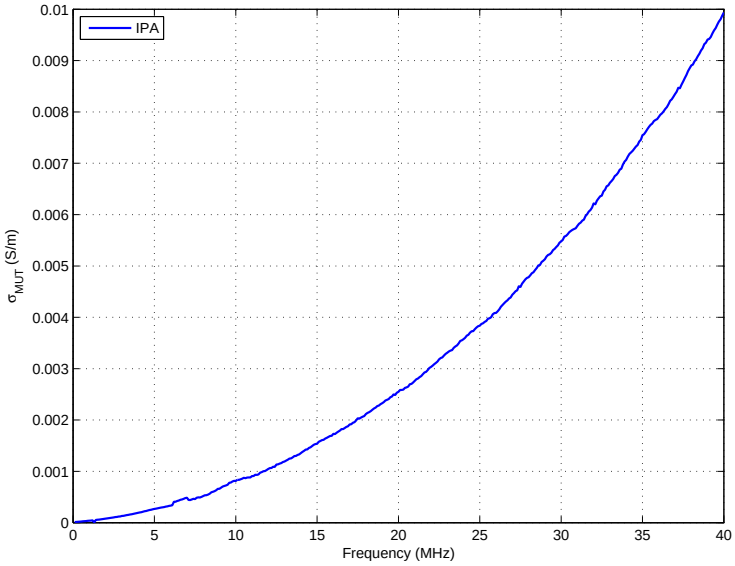
Figure 5.5 shows the extracted relative dielectric constant and conductivity of IPA. The extracted data is around 19 at frequency range of 100 Hz to 40 MHz, which is close to IPA's recorded relative dielectric constant 18.3. The error is about 3 %. Figure 5.5(b) shows the unexpected high conductivity of IPA. IPA should have conductivity 3.5 $\mu S/cm$ at room temperature [19]. The extracted value is clearly too high for IPA. The reason for such high extracted conductivity or loss will be discussed in Section 5.5.

5.3.1.1 Comparison of Three Methods of Calculating C_{up}

Figure 5.6 shows the extraction results using three different C_{up} modeling methods introduced in Section 4.4.2. It can be seen that the third method of using integration to calculate C_{up} renders closest extraction of dielectric



(a) Extracted dielectric constant of IPA



(b) Extracted conductivity of IPA

Figure 5.5: Extraction of dielectric properties of IPA

constant of IPA. Table 5.2 compares the error of extraction using the three methods

C_{up} Modeling method	Error of extracted relative dielectric constant
$C_{up} = C_{tot} - C_{air}$	25.6% - 36%
$C_{up} = C_{tot} - C_0$	9.3% - 14.7%
Integration	1.6% - 9.3%

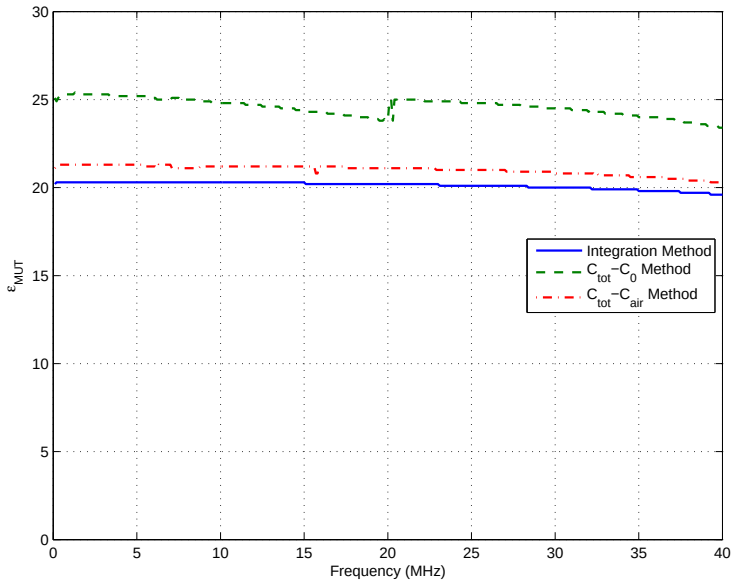
Table 5.2: Error of relative dielectric constant extraction using three different C_{up} modeling method

5.3.2 Germanium Nanowire Measurements

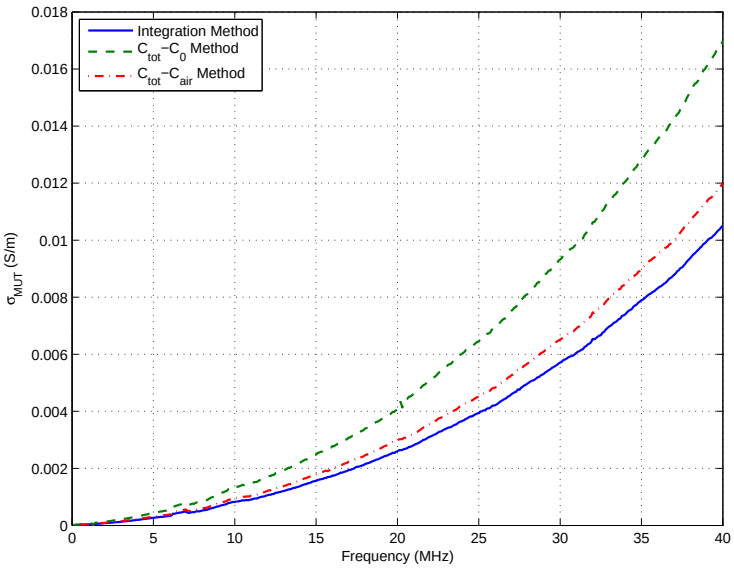
In this section, the measurements of dry and wet Ge nanowire are presented. The Ge nanowire is synthesized by Dr. Korgel's Group. After nanowire synthesis, a nanowire sheet is fabricated on filter in high pressure environment. Figure 5.7 shows picture of nanowire sheet and SEM picture of the sheet. The nanowire sheet is sticked to the IDC on top of the insulation layer by dropping a few IPA. After IPA evaporates, the dry nanowire sheet is attached on the insulation layer surface.

5.3.2.1 Dry Germanium Nanowire

Figure 5.8 shows the dielectric constant and conductivity extraction of dry Ge nanowire sheet. It can be seen that in the low frequency range, the dielectric constant is abnormally high at 20, and it drops to around 8 at higher frequency. Considering the nanowire sheet is not necessary solid but has air

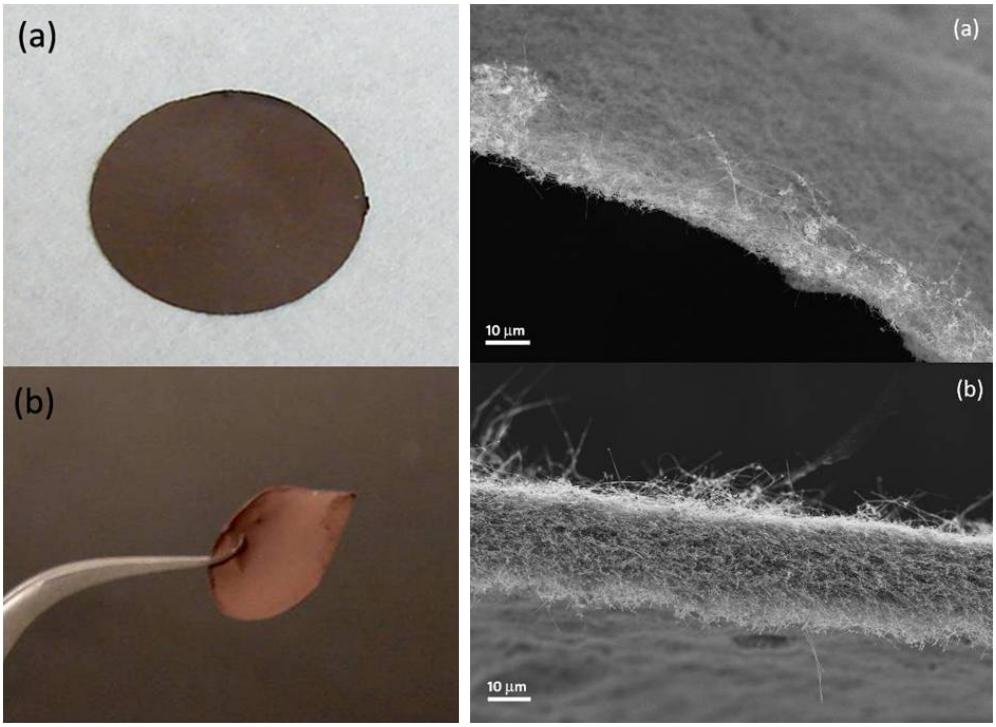


(a)



(b)

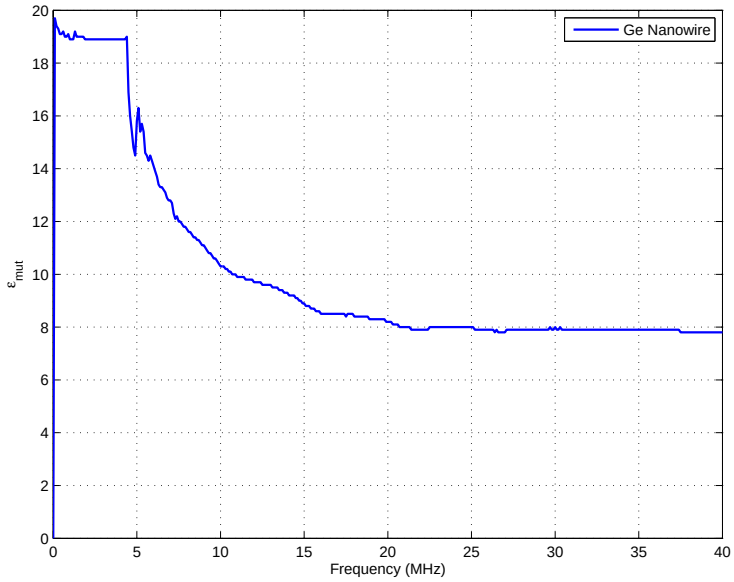
Figure 5.6: Extraction of dielectric property of IPA using three different modeling methods



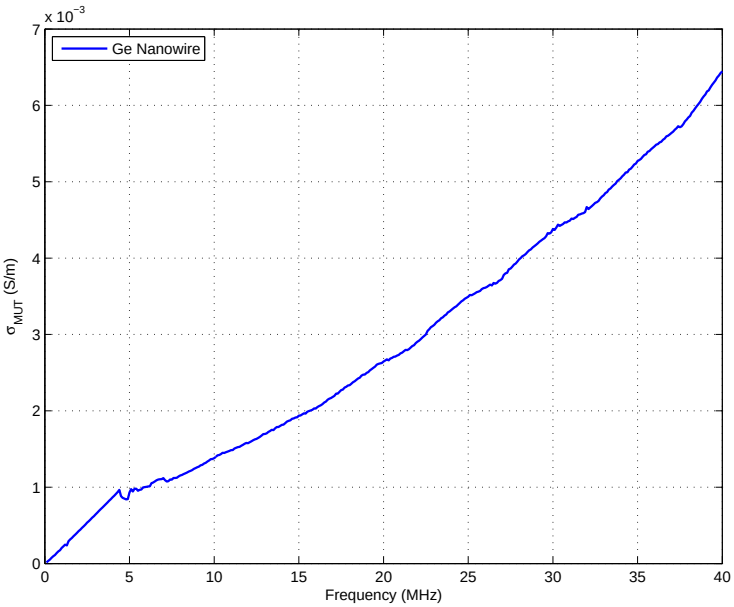
(a) (b)

Figure 5.7: Pictures of Ge nanowire sheet.

gaps in it, the extracted dielectric constant should be lower than solid Ge's dielectric constant 10. Hence 8 is a reasonable accurate extraction. Another reason why the extracted dielectric constant is lower than 10 might be the nanowire sheet is not thick enough, thus the air above the sheet also plays a role in the MUT. The extracted conductivity is in the order of $10^{-3}S/m$, which is a value close to conductivity of undoped bulk Ge.



(a) Dielectric constant extraction of dry Ge nanowire sheet



(b) conductivity extraction of dry Ge nanowire sheet

Figure 5.8: Extractions of dry Ge nanowire sheet

5.3.2.2 Germanium Nanowire Emersed in IPA

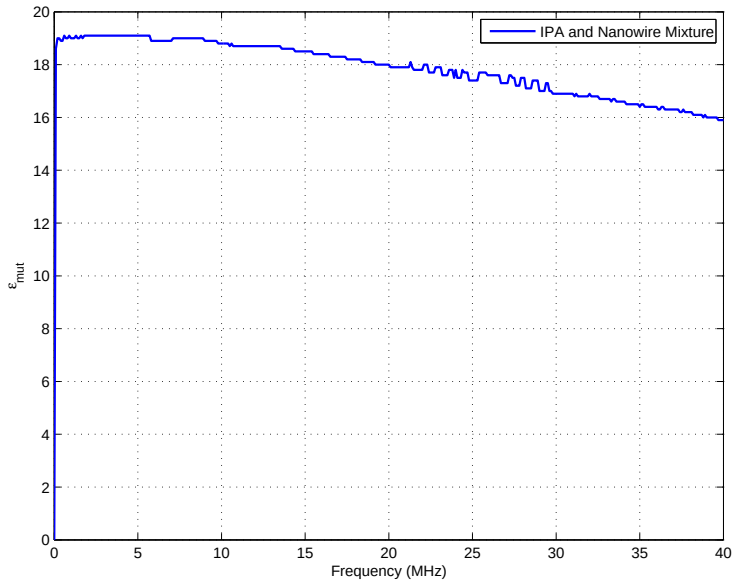
Figure 5.8 shows the dielectric constant and conductivity extraction of wet Ge nanowire sheet. We applied several drops of IPA on the nanowire sheet and measured the nanowire and IPA mixture. It can be seen that the extracted dielectric constant is close to 20 in Figure 5.9(a) but lower than the extracted dielectric constant of IPA as shown in Figure 5.10. Such behavior is expected because in the nanowire and IPA mixture, IPA fills up the gaps between nanowires and covers the entire nanowire sheet area, hence increased the effective dielectric constant of MUT, and due to the exist of nanowire sheet, the effective dielectric constant of MUT should be lower than IPA only. Figure 5.10 compares the extraction of IPA, dry nanowire, and wet nanowire in IPA.

5.3.3 Water Measurements

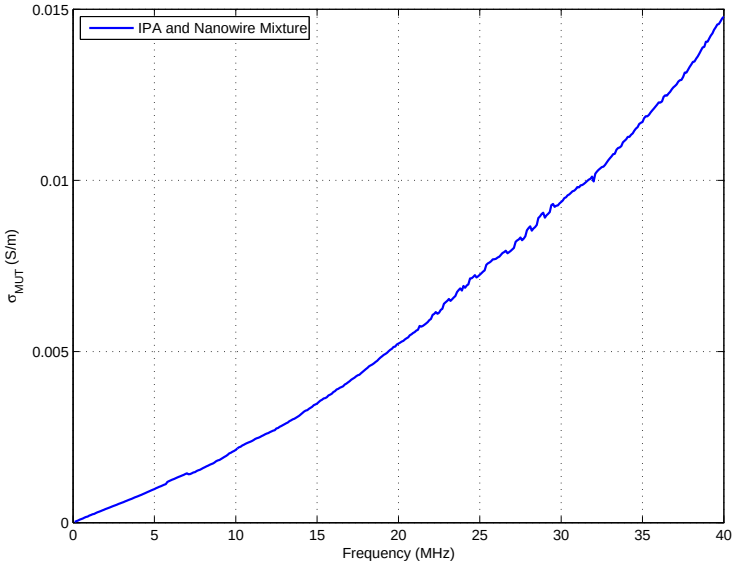
In this section, the measurement and extraction of DI-water is presented. The DI-water used in the measurement is taken from cleanroom in a pre-cleaned container. As shown in Figure 5.11, the dielectric constant is much lower than the expected value 80. The reason for such huge error is discussed in Section 5.5.2.

5.4 Back-extraction of Dielectric Constant of SU-8

In this section, an approach to back-extract the dielectric properties of insulation layer is presented. The motivation is that although MicroChem



(a) Dielectric constant extraction of wet Ge nanowire sheet



(b) Conductivity extraction of wet Ge nanowire sheet

Figure 5.9: Extraction of wet Ge nanowire sheet in IPA

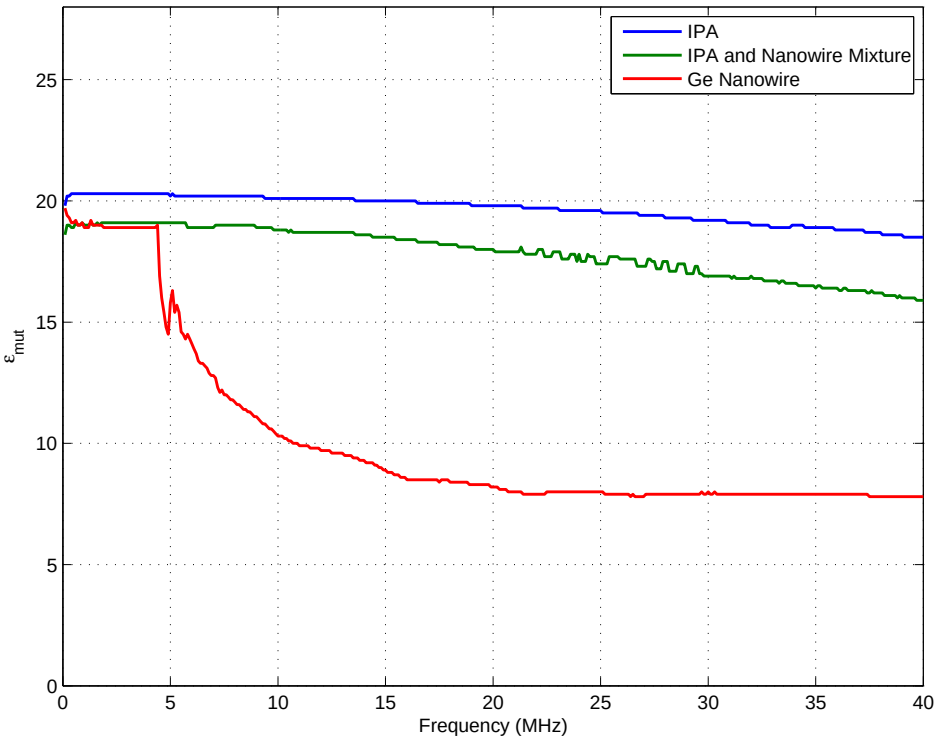
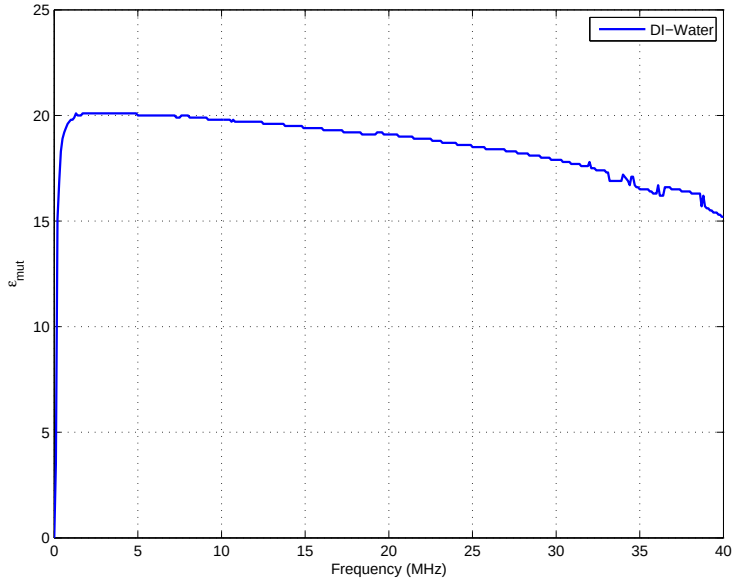


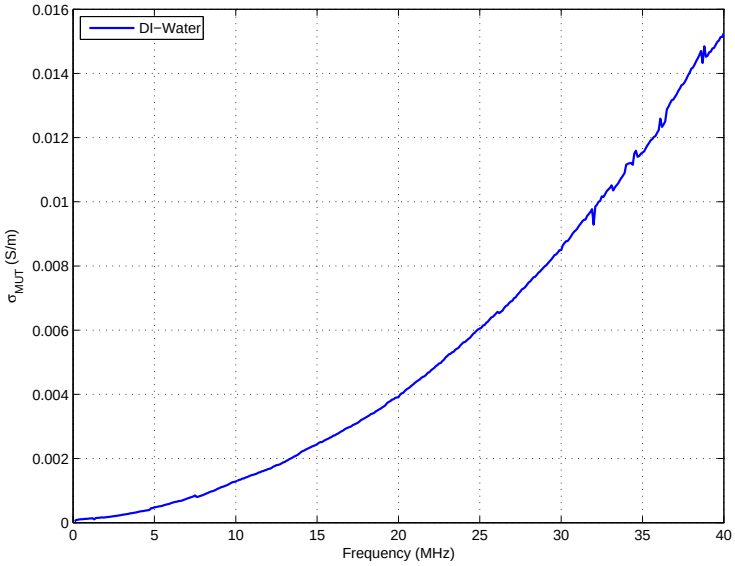
Figure 5.10: Extracted dielectric constant comparison between IPA, dry Ge nanowire sheet and wet Ge nanowire sheet in IPA

provided the dielectric constant of SU-8 as 3.2, but the dielectric constant would change if the fabrication process of the SU-8 layer is different. Using the algorithm presented in Section 4.5.1, the dielectric constant of insulation layer could be extracted if the dielectric constant of MUT is known.

First a low loss MUT should be picked and regular measurement needs to be done. In the experiment IPA is used as reference. Since the unknowns are now in the insulation layer, and the MUT is known as a low loss, the equivalent circuit model would look like Figure 5.12. Note that the G term is



(a) Dielectric constant extraction of DI-water



(b) Conductivity extraction of DI-water

Figure 5.11: Extraction of DI-water

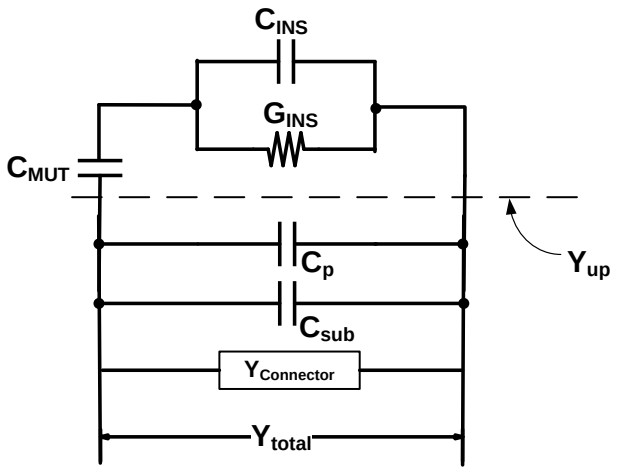
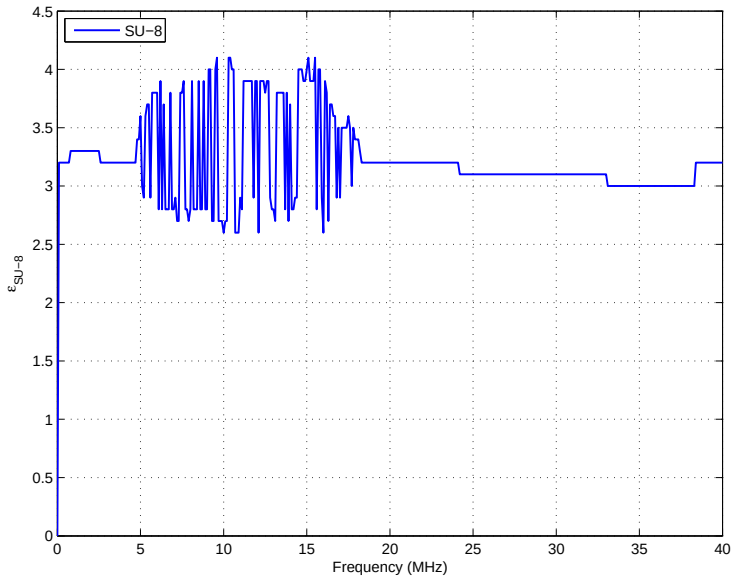


Figure 5.12: Equivalent circuit model used in back-extracting dielectric properties of insulation layer

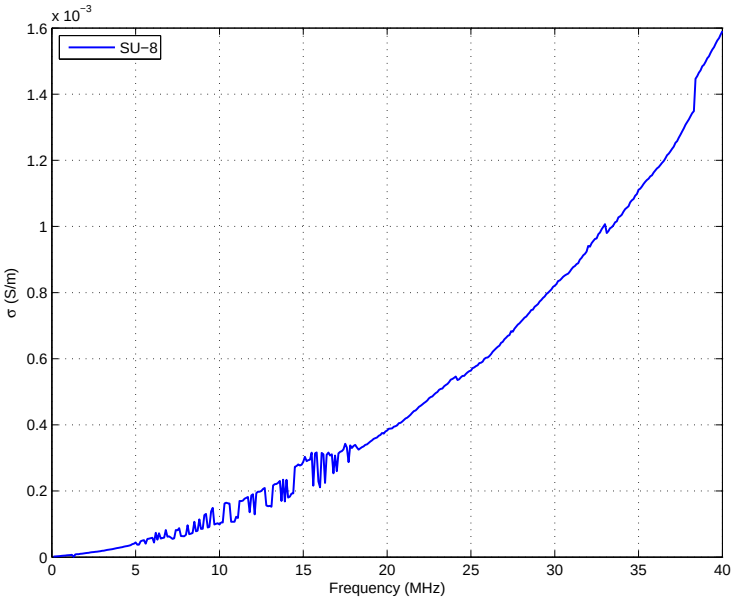
now parallel with C_{ins}, and there is no G_{MUT} term.

Since the equivalent circuit model is much like the original model, the extraction algorithms could be applied in the same way. In the new model, C_{MUT} value is already known in single layer IDC simulation/calculation. The relationship between C_{ins} and ϵ_{ins} needs to be simulated. The rest of the algorithm remains the same: first get estimated ϵ_{ins} from imaginary part of Y_{up}, then plug the estimation into real part to solve for σ_{ins}, and iteratively solve for ϵ_{ins} and σ_{ins} until converge. The extraction results are shown in Figure 5.13

It can be seen that although there are some noises around 10 MHz, the extracted dielectric constant of SU-8 is very close to the datasheet value 3.2.



(a) Extraction of dielectric constant of SU-8



(b) Extraction of conductivity of SU-8

Figure 5.13: Back-extraction of dielectric properties of insulation layer

5.5 Discussion

In this section, the problems encountered in measurement and extraction are discussed. The first problem is about conductivity extraction. Second problem is the algorithms limitation when the dielectric constant of MUT is high.

5.5.1 Conductivity extraction

It can be seen that the extracted conductivity of IPA and wet Ge nanowire in IPA are much higher than expected considering IPA is a low loss material. There are two possible source of the loss. First is the loss coming from SU-8 or connector. Second is the loss from the MUT, meaning that the IPA measured is not low loss in the first place.

Loss from the connector should be low, since the admittance of IDC in air is subtracted from the processed data. This step should remove most if not all the loss in the connector. Also, by looking at extracted conductance of dry Ge nanowire sheet, it can be seen that the conductivity is in the order of 10^{-3}, which is close to conductivity of solid Ge. This means the connector does not introduce much loss in the measurement and extraction.

Loss from insulation layer is more possible than the connector. As discussed in previous chapter, when building the equivalent circuit model, we assume the insulation layer is low loss, thus the G_{ins} term is not included in the model. Although we extracted conductivity of SU-8 in Section 5.4, the value is very close to the extracted conductivity of IPA in Section 5.3.1, as shown

in Figure 5.5(b) and Figure 5.13(b). Since we only modeled one G component in each extraction, all the loss would go to that term, hence the extracted conductivity in both case is relatively close. This means that the loss should indeed in the Y_{up} part of the equivalent circuit model. But the Ge nanowire measurement again proved that there should not be much loss introduced by SU-8. Also by comparing measurement of dry and wet Ge nanowire sheets, the addition of IPA increased the extracted conductivity dramatically, as shown in Figure 5.8(b) and Figure 5.9(b).

The most possible source of the loss would be the loss in measured IPA in the first place. The IPA we measured is brought out from cleanroom in clean bottles. During measurement, it is possible that IPA is polluted by ambient air and the conductivity is increased.

5.5.2 High dielectric constant material extraction

As shown in Section 5.3.3, the extracted dielectric constant of DI-water is only around 20, which is much lower than expected value around 80. The reason is probably because the over estimation of C_{ins} value. Figure 4.21 shows that at higher dielectric constant region, both integration method and $C_{up} = C_{tot} - C_0$ method has C_{ins} value greater than parallel plate estimation C_{para}, which does not reflect the real case. C_{ins} should never be greater than C_{para} because there will always be some electric flux constrained inside the insulation layer.

In the extraction, we are essentially calculating C_{MUT} from known C_{ins}

versus ϵ_{MUT} relationship and measured C_{up}, then trying to fit calculated C_{MUT} to known C_{MUT} versus ϵ_{MUT} relationship and get extracted ϵ. Since C_{ins} is overestimated at this region, C_{MUT} calculated is effectively underestimated. Hence the extracted ϵ_{MUT} would be smaller than real value when fitting calculated C_{MUT} to known curve.

Chapter 6

Conclusion

6.1 Summary of Work

The objective of this thesis is to develop a interdigitated capacitor (IDC) sensor to detect the dielectric properties of material under test (MUT). The design, fabrication, modeling and measurement have been done and discussed in previous chapters.

The design parameters and their effects on IDC's total capacitance is studied. The most significant parameters: spacial wavelength and metalization ratio and their relationship to the electric field penetration depth are discussed. It is shown that the thickness of MUT should be at least 1.5λ to avoid the electric field penetrating into air above the MUT. Simulation and calculation have been done to study the effect of number of electrode pairs, electrode length, electrode thickness, and substrate thickness. It is shown that the number of electrode pairs and electrode length is linearly related to total capacitance, and electrode thickness and substrate thickness has little effect on the total capacitance. Based on the parameter studies, IDC's having different dimensions are designed and fabricated.

In the modeling work, previous calculations of IDC capacitance using conformal mapping method is reviewed. The limitation of this method is that

it cannot model the electric field correctly when there are multiple insulation layers present on top of the IDC electrodes. The Finite-Element Method (FEM) simulation is also introduced. However, such simulation is also limited because it is too slow to simulate all the possible scenarios when the conductivity is taken into consideration.

Based on the electric field distribution, a novel equivalent circuit model is introduced. The model has each capacitor components modeled from the location of electric flux. Three different method of modeling capacitor component C_{up} are presented and compared. The capacitor components are calculated and simulated using FEM. An iterative dielectric properties extraction algorithm is developed in order to extract the dielectric constant and conductivity from "raw" impedance measurement data.

It is shown that the novel circuit model and iterative extraction method could accurately extract dielectric properties of both liquid (IPA) material under test (MUT), solid MUT (Germanium nanowire sheet), and liquid/solid mixture (Germanium nanowire sheet immersed in IPA).

6.2 Future Work

The modeling of IDC capacitor when MUT has high dielectric constant should be improved. Current model overestimates capacitor component C_{in} resulting in the extracted dielectric constant too low. Both simulation and calculation needs to be done to find out the reason. Especially the reason why the integration method based on FEM simulation could not predict the

capacitor components accurately at high dielectric constant region should be studied.

The robustness of the sensor packaging can be improved. Currently the sensor is connected to an RCA-BNC connector by soldering wire to the connector and attache wire using silver epoxy to the sensor pad. Such connection or packaging method has great variation between different samples because the wire position and distance could all affect sensor's impedance. The sensor chip could easily fall off during the measurement because the connection does not have enough strength to hold the sample. One possible solution is to use a PC Board to form a platform of the sensor. The connection could be realized by wire-bonding at sensor end, and using a BNC-PCB mound connector at the other end. Such platform structure is quite standard and is easier to realize than attaching wires to sensor pads by hand.

Another possible improvement for the sensor is to integrate an inductor into the system so that the signal could be detected by a wireless reader. Ong *et. al.* already presented a wireless IDC sensor connecting two separate IDC and inductor [9]. Such structure is very easy to model because it contains only two major circuit elements. However, it is hard to balancing the area of inductor and capacitor. Both of them needs relatively large area in order to have reasonable resonant frequency. One idea is to integrate the IDC "into" the inductor. Conventionally, the distributed capacitance of an inductor should be as small as possible. But in the capacitive sensor example, the capacitance should be large enough to be detected. Hence, by introducing

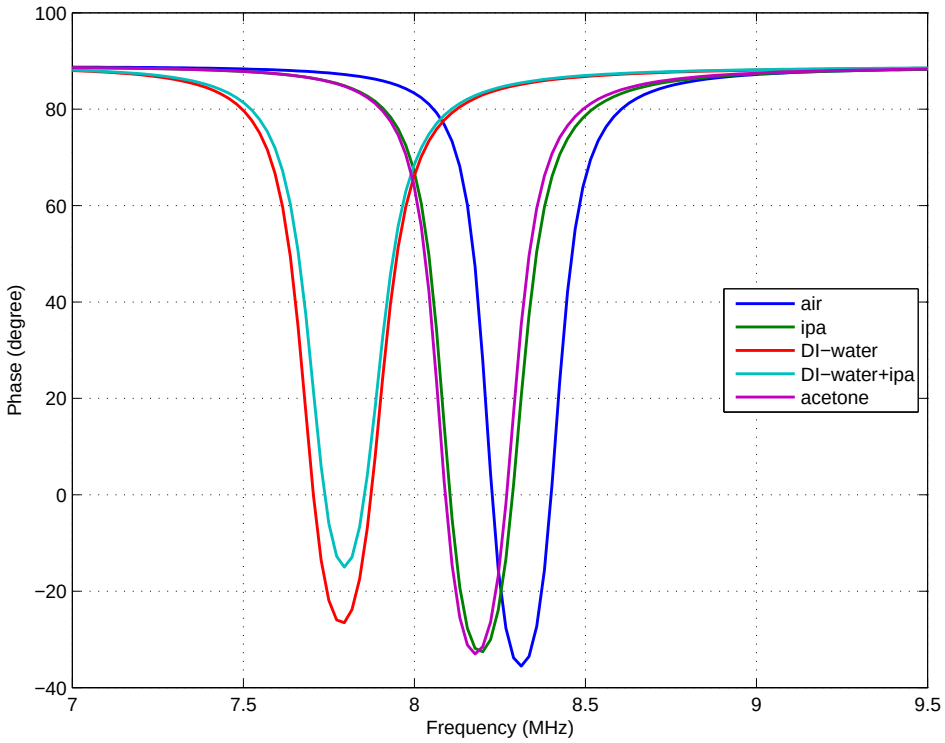


Figure 6.1: Phase dips when measuring different MUTs using EAS tag

IDC into the spacing of inductor segments could increase the distributed capacitance, hence sensing the dielectric properties changes in the environment. Preliminary measuring of different MUT using commercial Electronic-Article-Surveillance (EAS) tags is shown in Figure 6.1.

The EAS tags have fixed capacitor connecting to a fixed inductor, and the resonant frequency shift is only because of the change of distributed capacitance in the inductor.

Appendix

Appendix 1

Matlab Programs

1.1 Conformal Mapping Calculation

The following is the conformal mapping capacitance calculation method suggested by Igreja *et. al.* [10].

File: Igreja.m

```
function cIDC = igreja(n,h,w,g,l,sub,ins,mut)
%IDC specification
epsilon0 = 8.854187817e-12; %Electric constant
L = l; %Finger length
eta = w/(w + g);
lamda = 2*(w + g);
r = h/lamda;
epsilonsub = sub;
epsilonins = ins;
epsilonmut = mut;

%%CI calculation

q = exp(-4*pi*r);
m = inversenomeq(q);
k=sqrt(m);
t2 = ellipj(ellipke(k^2)*eta, k^2);
t4 = 1/k;
kI = t2*((t4^2 - 1)/(t4^2 - t2^2))^0.5;
kIprime = (1 - kI^2)^0.5;
kIinf = sin(eta*pi/2);
kIinfprime = cos(eta*pi/2);

cI = epsilon0*((epsilonins - epsilonmut)*ellipke(kI^2)...
    /ellipke(kIprime^2)+ (epsilonmut + epsilonsub)...
```

```
    *ellipke(kIinf^2)/ellipke(kIinfprime^2));

cIair = epsilon0*epsilonmut*ellipke(kIinf^2)...
    /ellipke(kIinfprime^2);
cIins = epsilon0*(epsilonins - epsilonmut)*ellipke(kI^2)...
    /ellipke(kIprime^2);
cIsub = epsilon0*(epsilonsub)*ellipke(kIinf^2)...
    /ellipke(kIinfprime^2);

%%CE calculation

t3 = cosh(pi*(1 - eta)/(8*r));
t5 = sinh(pi*(1 + eta)/(8*r)); %t4 in the paper
kE = ((t5^2 - t3^2)/(t5^2 - 1))^0.5/t3;
kEprime = (1 - kE^2)^0.5;
kEinf = 2*eta^0.5/(1 + eta);
kEinfprime = (1 - kEinf^2)^0.5;
cE = epsilon0*((epsilonins - epsilonmut)*ellipke(kE^2)...
    /ellipke(kEprime^2) + (epsilonmut + epsilonsub)...
    *ellipke(kEinf^2)/ellipke(kEinfprime^2));
cEair = epsilon0*epsilonmut*ellipke(kEinf^2)...
    /ellipke(kEinfprime^2);
cEins = epsilon0*(epsilonins - epsilonmut)*ellipke(kE^2)...
    /ellipke(kEprime^2);
cEsub = epsilon0*(epsilonsub)*ellipke(kEinf^2)...
    /ellipke(kEinfprime^2);

%%Total capacitance calculation

cair = ((n - 3)*cIair/2 + 2*cIair*cEair/(cIair + cEair))*L;
cins = ((n - 3)*cIins/2 + 2*cIins*cEins/(cIins + cEins))*L;
csub = ((n - 3)*cIsub/2 + 2*cIsub*cEsub/(cIsub + cEsub))*L;
cIDC = cair+cins+csub;
end
```

1.2 Iterative Parameter Extraction Code

The following is the iterative extraction code discussed in Chapter 4. The capacitance component data are stored in separate files.

File: iter-extraction.m

```
clear all
clc
close all
%% Use C_mut_comsol & C_air_comsol and C_tot_comsol to Get C_ins
epsilon_0=8.854187e-12;
C_ins_load=load('Cins_inte.txt');
C_ins=C_ins_load(:,2);
A=load('C_single_layer.txt');
C_mut_comsol=A(:,2);
epsilon=A(:,1);
C_comsol_load=load('cap.txt');
C_comsol=C_comsol_load(:,2);
%% Calculate Y_up = Y_ipa - Y_air
[G_ipa B_ipa Freq] = load_adm('ipa4-329');
[G_air B_air Freq] = load_adm('air4-329');
Omega=Freq*2*pi;
Y_up =(G_ipa + i*B_ipa)-(G_air + i*B_air);
C_up = imag(Y_up)./(Omega); % Get measured C_up value
G_up = real(Y_up);
B_up = imag(Y_up);

%% Get epsilon est
C_up_model=C_comsol-C_comsol(1);
%have a first guess
C_ins=C_ins/2;
Omega=Freq*2*pi;
for j=1:1:401
    er_guess(j)=0;
    er(j)=0;
end
%%  Iteration at each frequency point
for i=2:1:401
    [value index]=min(abs(C_up_model-C_up(i)));
    epsilon_guess(i)=epsilon(index);
    epsilon_new=epsilon_guess(i);
% Plug in to Real part of Y_up and solve for conductivity
    a(i)=G_up(i)*(C_mut_comsol(index)^2)...
        /(epsilon_guess(i)*epsilon_0)^2;
    b(i)=-(Omega(i)^2)*C_mut_comsol(index)*...
        (C_ins(index)^2)/(epsilon_guess(i)*epsilon_0);
    c(i)=(Omega(i)^2)*G_up(i)*(C_mut_comsol(index)+...
        C_ins(index))^2;
    p=[a(i) b(i) c(i)];
    result=roots(p);
    sigma2(i)=result(2);
```

```
    sigma_old=sigma2(i);
    sigma_new=1;
    epsilon_old=epsilon_guess(i);
    epsilon_new=er_guess(i);
    error_sigma=1;
    while (abs(epsilon_old-epsilon_new)>0.4 &&...
            abs(error_sigma)>0.5) % Iteration stop conditions
        epsilon_old=er_guess(i);
        sigma_old=sigma2(i);
         for er=1:1:size(epsilon,1)
            LHS_up=((C_ins(er)*C_mut_comsol(er)^2*Omega(i)*...
                sigma2(i)^2/(epsilon(er)*epsilon_0)^2)+...
                C_ins(er)^2*C_mut_comsol(er)*Omega(i)^3+...
                C_ins(er)*C_mut_comsol(er)^2*Omega(i)^2);
            LHS_down=C_mut_comsol(er)^2*sigma2(i)^2/...
                (epsilon(er)*epsilon_0)^2+Omega(i)^2*...
                (C_ins(er)+C_mut_comsol(er))^2;
            LHS(i)=LHS_up/LHS_down;
            diff(er)=(LHS(i)-B_up(i));
         end
        [diff_freq(i) index2(i)]=min(abs(diff));
        er_guess(i)=epsilon(index2(i));
        epsilon_new=er_guess(i);
%Plug back to real part
    a(i)=G_up(i)*(C_mut_comsol(index2(i))^2)/...
        (er_guess(i)*epsilon_0);
    b(i)=-(Omega(i)^2)*C_mut_comsol(index2(i))*...
        (C_ins(index2(i))^2);
    c(i)=(Omega(i)^2)*G_up(i)*(C_mut_comsol(index2(i))...
        +C_ins(index2(i)))^2*er_guess(i)*epsilon_0;
    p=[a(i) b(i) c(i)];
    result=roots(p);
    sigma2(i)=result(2);
    sigma_new=sigma2(i);
    error_sigma=(sigma_new-sigma_old)/sigma_new;
    end

end
%% Calculate loss
sigma=sigma2(2:401);
er1=er_guess(2:401);
Freqn=Freq(2:401);
for i=1:1:400
    loss(i)=sigma(i)/2/pi/epsilon_0/Freq(i+1)/er1(i);
```

```
end
%% Wrap up
temp=mean(er);
sigma=sigma2(2:401);
plot(Freq(2:401)/10^6,sigma)
xlabel('Frequency (MHz)')
ylabel('\sigma (S/m)')
title('Conductivity')
grid on
figure
plot(Freq/10^6,er_guess);
ylabel('\epsilon_{mut}')
xlabel('Frequency (MHz)')
title('Dielectric constant')
%ylim([0 20])
grid on
```

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