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Design, Modeling and Control of A 12.47 kV Isolated Three Phase Power Factor Correction Rectifier

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Design, Modeling and Control of A 12.47 kV Isolated Three Phase Power Factor Correction Rectifier

by

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Dedication

To my grandparents, LinChao Ye and Baoling Meng

And

My parents, ChaoQuan Tang and Ping Ye

Your love, inspiration, drive and support make me what I am today. I would love to continue the journey with you by my side.

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I am grateful to all my committee members for their continuous help and support.

A special thanks to my friends and colleagues at the UT-Austin semiconductor power electronics center (SPEC) and Eaton Asheville Medium Voltage Motor Drive and Control team.

Abstract

Design, Modeling and Control of A 12.47 kV Isolated Three Phase Power Factor Correction Rectifier

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The University of Texas at Austin, 2019

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A novel three-phase rectifier with power factor correction feature is proposed for the medium voltage (MV) high power (HP) applications. A typical application is to use it as the front-end circuit to interface with power grid and supply the power to a customized load, including medium voltage variable frequency drive (MV-VFD), electric vehicle bus charger, cargo ship and renewable energy source. The proposed topology has numerous advantages over conventional systems in regarding of the system efficiency, reactive power consumption, power density and operating flexibility. On the other side, this system has some challenges in semiconductor selection, control logic development, current harmonics elimination, modular implementation and system protection strategy design.

The advanced silicon carbide (SiC) MV isolated three-phase power factor correction rectifier (MV-PFC) is targeting to the MV-VFD application. Chapter 1 is a system review of the industrial MV-VFD products in regarding of its major industrial applications, grid voltage and power ratings, motor control requirements, popular semiconductor devices and recognized circuit topologies. Following the chapter 1, chapter 2 reviews the popular topologies cited in both academic projects and industrial products. Each topology is analyzed and investigated thoroughly.

Then, a table summarizes the pros and cons of each circuit in terms of the system flexibility, regeneration capability, galvanic isolation rating, system power density, operating redundancy, power module rating, switching frequency, modulation complexity, power quality and operating efficiency. Next, a novel MV three-phase PFC topology is proposed to boost up the system performance to the next level. In another word, this topology meets all the system operating demands with higher efficiency and better power density. Furthermore, it improves the system operating flexibility and the fault tolerance margin.

A silicon carbide metal-oxide semiconductor field-effect transistor (SiC MOSFET) module, rated at 12.5 kV and 375 A, is developed as the core component for the power circuit. Its internal chip layout is designed accordingly. Both the electric and thermal features of this power module are characterized to describe its performance envelope. Furthermore, the device mathematic model is implemented for system power loss and thermal energy distribution studies.

After finalizing the circuit architecture design, a novel control scheme including both modulation feedforward control and output feedback regulation is developed. The internal loop uses the power command reference, grid input and DC output to calculate the MOSFET firing angles for the next switching event. The outer loop generates the power command reference and evenly assigns it to all three phases based on the real-time load condition. Then, an application state machine, including I/O management, soft start-up strategy and system protection scheme, is designed to promote the overall design close to the industrial product. The soft start-up strategy effectively limits the inrush current and charges the output DC bus from zero to full energy level safely. For the sake of the functional validation, the system steady state study includes different loading conditions. Considering the long-term operating reliability, the case study covers the power grid oscillation situation and four different fault scenarios. The protection scheme is developed to accurately detect the fault location and recover the system from the fault when possible.

An issue is found from the system steady state study, which is the input grid current distortion at the ultra-light load condition. In order to resolve this problem, an additional hardware

circuit including a separate inductor and bypass breaker is added, which increases the damping effect in the middle-stage circuit. The control scheme is modified to coordinate with the improved topology. As a result, the system can operate safely and reliably at the ultra-light condition with the minimum current harmonics.

As an alternative design approach for the integrated system structure, the modular dual-active-bridge (DAB) PFC rectifier is developed. The modular structure greatly decreases the device and component power stress and brings in some operating redundancy. In the meanwhile, the difference coming from module hardware arises the challenge to the inter-module power and voltage balancing control. A novel inter-module balance control layer is described in the chapter 6. As a result, the unbalance coefficient between modules is less than 1%. In addition, the protection strategy for the modular system is developed, which can cut off the defective power module and bring the rest of the system back to the 100% performance status within the half line cycle.

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1 Introduction to MV-VFD System

Modern power electronics have pioneered the path to revolutionize the medium voltage motor drive (MVD) industry by introducing the variable frequency drive (VFD) technology (also known as Adjustable Speed Drive (ASD) or Frequency Converters (FC)). VFD technique not only improves the system efficiency and productivity, but also brings some advanced features to attract new customers. Medium voltage (MV) VFD products have been widely deployed in eight major industrial applications, including mining/cement, petrochemical, metals, paper/pulp, marine, oil/gas, power generation and water/waste water (fig. 1.1) [1] – [5].

Fig. 1.1 MV VFD Industrial Applications

A MV-VFD product improves energy efficiency and meets the end users' requirements by controlling the motor at an optimal speed and torque in both transient or steady states [6]- [8]. In the meanwhile, it dynamically changes the system operational status to prevent the harmonics introduced by the machine from affecting the power grid stability. A MV-VFD design is specified as the power rating, grid voltage level, motor terminal voltage, circuit topology and semiconductor device being selected. The majority of the installed systems is summarized as table 1.1 [9]-[11].

Table 1.1 Majority of Installed MVDs

Power	0.4 to 200 MW
Grid Voltage	2.3 to 13.8 kV, 50/60 Hz
Motor Voltage	2.3 to 6.6 kV
Semiconductor Device	Diode, Thyrisitor, GTO, IGCT/GCT/SGCT, IGBT/HV-IGBT/IEFT, etc.
Circuit Topology	Voltage Source Converter (VSC), Current Source Converter (CSC), etc.

Author is about to propose a novel rectifier topology targeting to the next generation MV-VFD products. A cross-comparison between the proposed and existing topologies is given to emphasize the novelty and performance advantages brought by the novel AC-DC rectifier. Then, the overall system architecture and its performance envelope are illustrated as the design guideline.

2 A Novel Isolated Medium Voltage Power Factor Correction (MV-PFC) Circuit

The MV-VFD products have been available in the market for more than half century. Numerous mature topologies have been successfully commercialized and self-proved through the years. In the meanwhile, the market keeps challenging the research and design groups for a novel topology with higher power density, higher operating efficiency, more operating flexibility and better reliability. Starting with the existing structures, next couple sections are about the circuity analysis and try to specify what can be improved in the next generation system design. The front-end AC-DC rectifier is the research target in this thesis.

2.1 Literature Review

The rapid growth of the semiconductor industry greatly benefits the MVD products by producing the high-performance power switches. Once the power device is selected, the peripheral circuit is developed to switch the devices properly and achieve its performance goal. Numerous motor drive topologies have been studied since 1970s. Given the limited pages, these selected systems are required to meet these three criteria.

a. The circuitry is designed for the medium-voltage and high-power applications. To be specified, the system is rated above 1.2 kV and 0.4 MVA.
b. The system is connected to a three-phase power grid with either wye or delta configuration.
c. The topology gains attention from both academic and industrial worlds.

Fig. 2.1 is a typical modular multilevel cascade converter (MMCC). With no active front end (AFE) required, a multi-pulse phase-shifting isolated rectifier is installed on the input side which consists of a line frequency phase-shifting transformer and three-phase diode rectifiers. Each module has its own DC link to decouple the AC-DC rectifier from the DC-AC inverter. Either H-bridge or chopper is the popular choice for the DC-AC inverter circuit. The inverter blocks are divided into three groups to provide three-phase power to the electrical machine(s).

Fig. 2.2 is another MMCC topology. Differ to the fig. 2.1 system, it has the bi-directional power flow capability. A controlled power cell is used at the front side instead of the multi-phase isolated rectifier block. Inside of each power module, the rectifier and inverter are identical and back-to-back connected through a common DC link. Similar to the fig. 2.1 system, H-bridge or chopper circuit is the popular choice for both rectifier and inverter design.

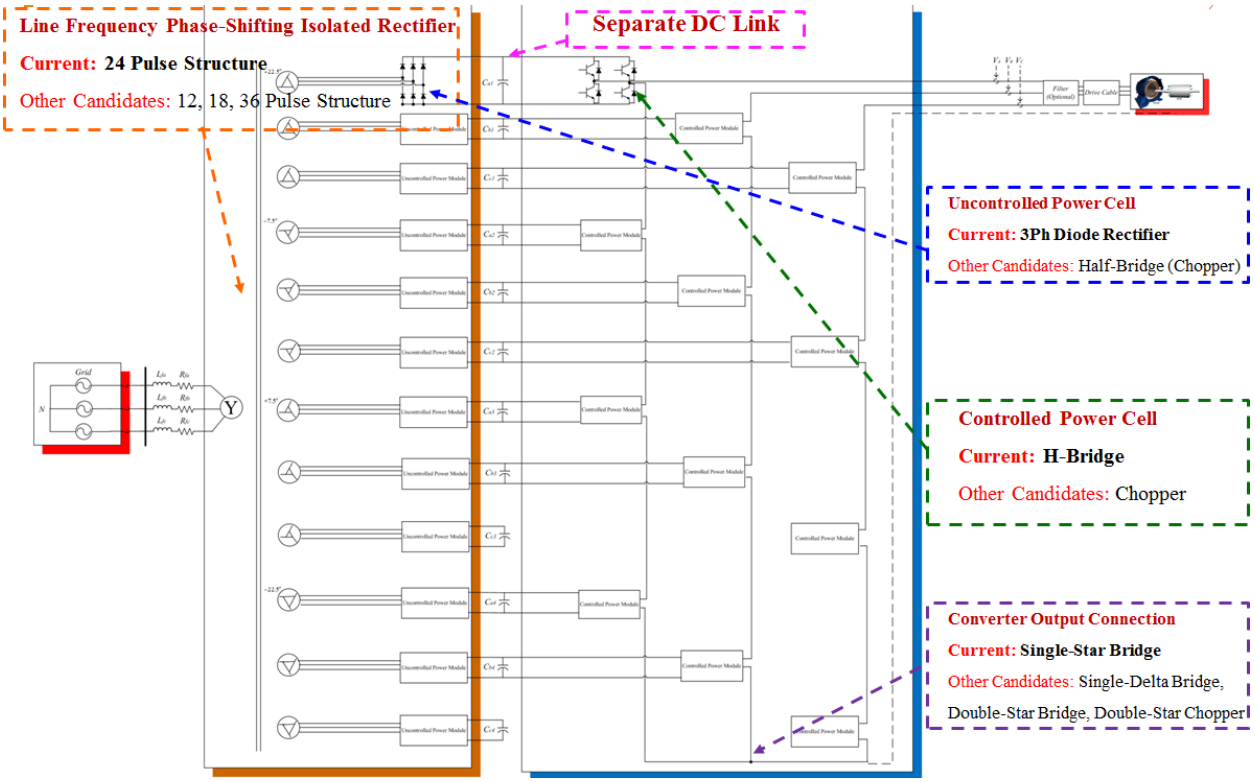


Fig. 2.1 MMCC without AFE

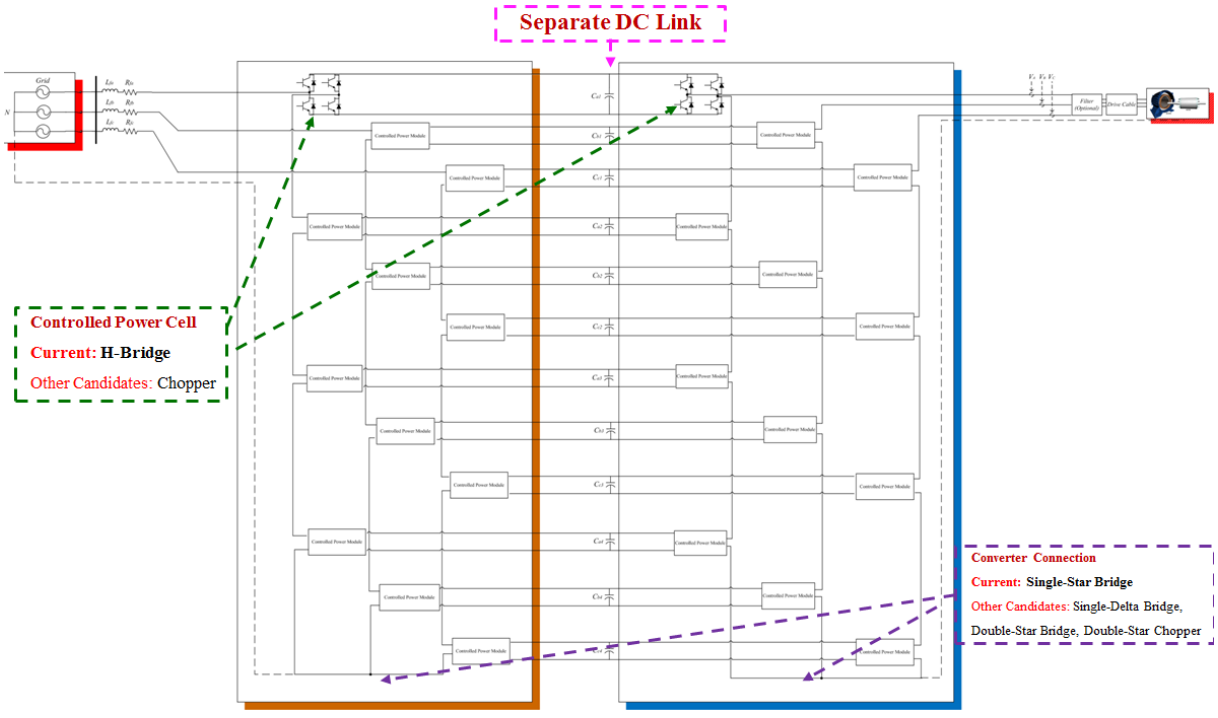


Fig. 2.2 MMCC with AFE

The MMCC technology is used by Siemens industry in its “Robicon Perfect Harmony” drives and ABB in its “ACS5000” products. In the academic world, many papers discussed the MMCC architectures, control strategies, fault tolerance and applications [12]-[22]. The characteristics of the MMCC are summarized as below,

a. Flexible output voltage by adding or subtracting the power modules.
b. No AFE option has the galvanic isolation capability.
c. Redundant stage and fault tolerance.
d. High switching frequency, simple modulation algorithm.
e. Complicated inner and inter module communication interface.
f. Large footprint and low power density.
g. Large number of the electrical components.
h. High system installation and maintenance fee.

As the counterpart of the modular converter, integrated multilevel structure is favored by many end users due to its compact design and small footprint. As an example, a modern three-level neutral-point clamped inverter (3L-NPC) MVD product, equipped with the phase-shifting transformer, is presented in fig. 2.3. With no AFE required, diode-based rectifier is back-to-back connected to the 3L-NPC inverter. Twenty-four pulse transformer rectifier unit improves grid side power quality being compliant to the IEEE Std 519 harmonic control requirement. Except for the twenty-four-pulse rectifier, twelve, eighteen, thirty-six pulse topologies are available for different applications. Output dv/dt or sinusoid filter is optional to protect the motor winding from over voltage caused by the long motor cables and pulse width modulation (PWM) inverter control scheme.

Fig. 2.4 is an integrated multilevel converter (IMC) with AFE feature. The multilevel AC-DC rectifier and DC-AC inverter normally have the same topology and share the DC link. Except for the 3L-NPC circuit, other options include but not limit to the three-level active neutral-point clamped converter (3L-ANPC), five-level H-bridge neutral-point clamped converter (5L-HNPC), five-level H-bridge active neutral-point clamped converter (5L-HANPC) and four-level flying capacitor converter (4L-FC).

The IMC topology is used by Toshiba in its "T300MVi" drives and Eaton in its "SC9000" products. In the academic world, many papers talk about the IMC's topologies, modulation techniques and industrial applications [23]-[41]. The characteristics of the IMC are summarized as below,

a. Small footprint and high-power density.
b. Simple system communication interface.
c. Small number of the electrical components.
d. Low system installment and maintenance fee.
e. Customized design for different electrical machines.
f. No redundant stage or fault tolerance.
g. Integrated circuit design requires high voltage and high current semiconductor devices.
h. Low switching frequency, complicated modulation algorithm.
i. No AFE option uses a complicated multi-winding phase-shifting transformer.
j. No AFE option has the galvanic isolation capability.

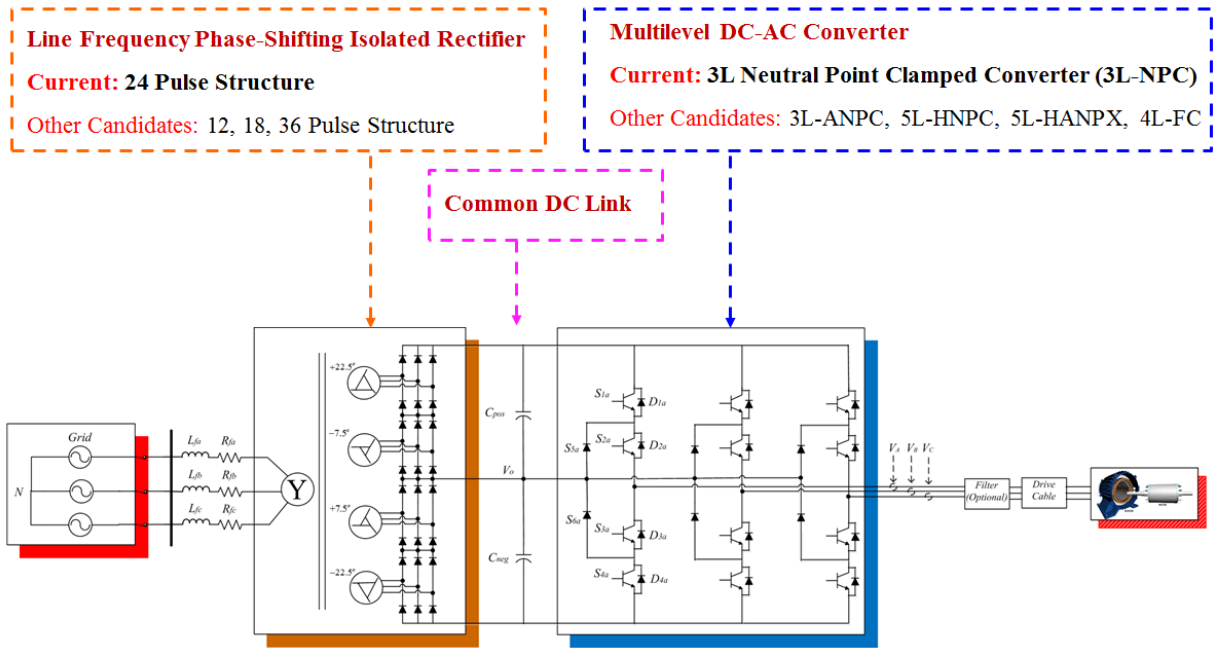


Fig. 2.3 IMC without AFE

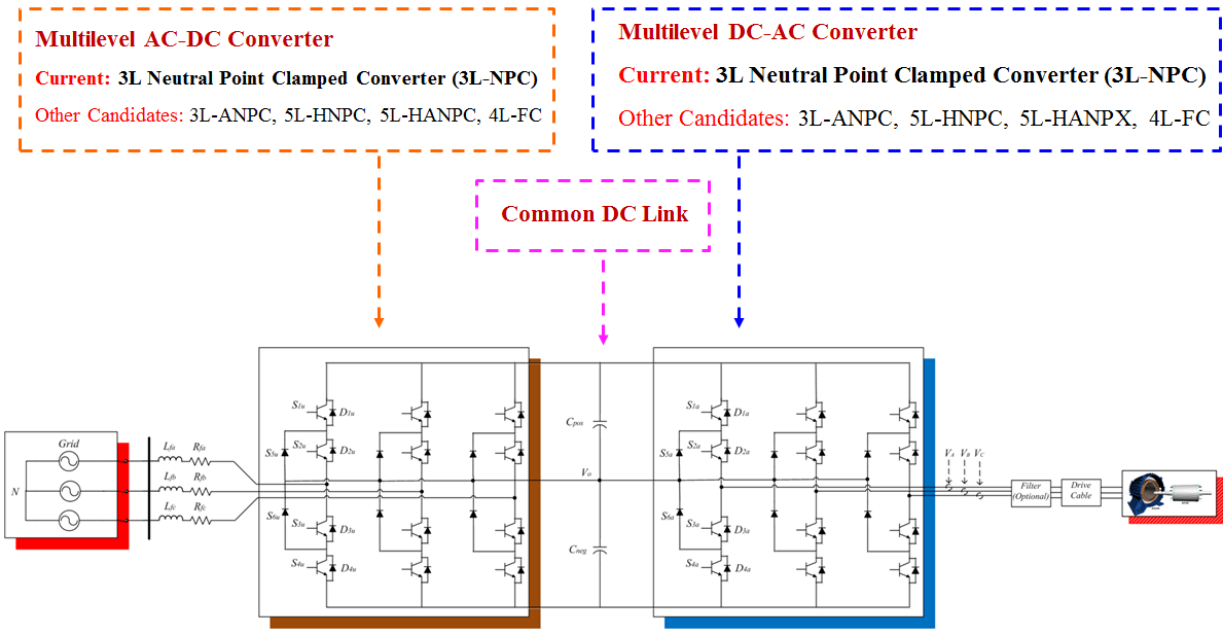


Fig. 2.4 IMC with AFE

Both MMCC and IMC topologies have their own pros and cons. The MMCC has the redundant stage, simple modulation technique and flexible inverter output voltage. The IMC has its advantages as the high-power density and low switching frequency. Table 2.1 and 2.2 compare above all four topologies in terms of ten critical criteria.

Table 2.1 Topology Cross Comparison - I

Option	Topology	Flexible output	Regeneration	Galvanic isolation	Power density	Redundancy
1	MMCC (No AFE)	Low	Low	High	Low	High
2	MMCC (with AFE)	High	High	Low	Medium	High
3	Integrated multilevel conv (No AFE)	Low	Low	High	Medium	Medium
4	Integrated multilevel conv (with AFE)	Medium	High	Low	High	Medium

Table 2.2 Topology Cross Comparison - II

Option	Topology	Power module rating	Switching frequency	Modulation complexity	Power quality	Efficiency
1	MMCC (No AFE)	Medium	Medium	Low	High	Medium
2	MMCC (with AFE)	Medium	Medium	Low	High	Medium
3	Integrated multilevel conv (No AFE)	High	Low	Medium	High	Medium
4	Integrated multilevel conv (with AFE)	High	Low	High	High	Medium

2.2 A Novel MV-PFC Topology

In the modern industry, customers keep challenging the MVD products for better performance, more operational flexibility and some advanced features. Although the MMCC and IMC systems have many benefits, there are four features which are not realized by the conventional topologies. First one is associated with the normal operating cost. The utility company charges the MVD customers for both active and reactive power usage. How to reduce the total amount of reactive power consumption is a popular topic. The second one is to improve the system operational efficiency. The semiconductors contribute most of the power loss. Thereby, the system efficiency can be greatly improved if part of the semiconductor power loss could be eliminated. The third one is to guarantee the premium power quality on the grid side in regardless of the motor loading profile. The existing systems cannot perfectly decouple the motor from the power grid. Some harmonics introduced by machines get transferred back to the power grid and then deteriorates the grid power quality. The fourth feature is to interface with a wide range of the input voltage without additional hardware. The power grid voltage level varies from area to area and country to country. This feature standardizes the system design and promotes the product deployment to the different applications.

In order to fulfill all four requirements, the author proposes a novel three-phase MV-PFC converter [42]. It has the power factor correction (PFC) function built-in which lowers the utility bill by eliminating the reactive power under all conditions. The novel switching strategy, named as zero-voltage switching (ZVS) technique, is applied to reduce the semiconductor switching loss and further improve the system efficiency. In addition, the circuitry is capable of handling different loads and serves as a buffer between the power grid and the machines. All the major harmonics

are isolated and filtered by the circuit. Finally, it is able to accept a wide range of the input voltage from 2.4 kV to 13.8 kV, which is compatible with most of the power grid in the Americas, Asia, Europe and Africa. In a word, it is a great candidate for the next generation MVD products.

Fig. 2.5 is the diagram of the proposed MV isolated three-phase PFC VFD. A novel MV three-phase PFC rectifier replaces the traditional rectifier block and keeps the inverter as the multilevel converter structure. My research target is about the AC-DC rectifier circuit since no change is made in the inverter section. This is an integrated system design with small footprint which is suitable for high-voltage, direct current (HVDC) and intelligent energy management (IEM) applications. In the MV world, the galvanic isolation is highly preferred for safe operational requirements. The proposed rectifier has a high frequency (HF) transformer included to isolate the power grid input from the output load. Furthermore, this rectifier can supply power to single or multiple inverters because of its technical, operational and economic feasibilities.

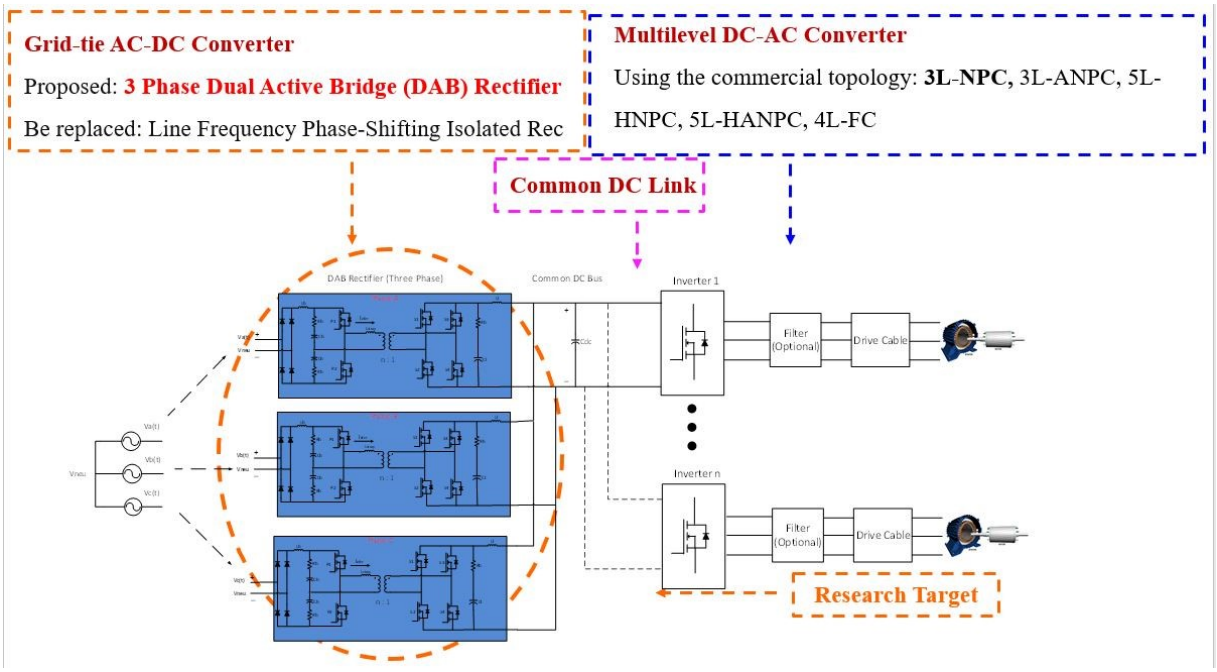


Fig. 2.5 A Novel MV Isolated Three-Phase PFC MVD

Fig. 2.6 is the single-phase DAB PFC module. All the sensors are color coded and categorizes as either “must have” or “good to have”. Generally speaking, only the input and output ports need to be monitored and used for control purpose. Other sensors are mainly for data collection, system protection, operating status monitoring of the HF transformer and the semiconductor devices.

Table 2.3 summarizes the system operating conditions and parasitic component parameters. More details will be elaborated in the following chapters.

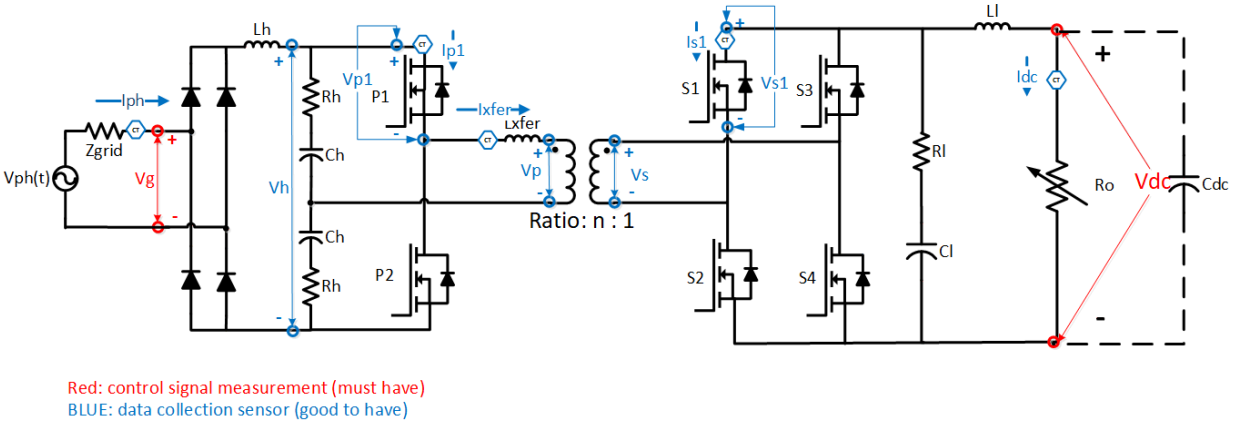


Fig. 2.6 Single-Phase MV Isolated PFC Converter

Table 2.3 System Parameters and Operating Ratings

System Operating Condition	
Grid Voltage	12.5k (7.2k per phase)
Line Frequency	60 Hz
DC Bus	6 kV
Pout	1 MVA
Xfer Primary Side	
Lh (input filter)	6 mH
Ch (input filter)	1.3 uF
Lxfer / Lstray	1 mH
Xfer Secondary Side	
Ll (output filter)	15 uH
Cl (output filter)	75 uF

3 Loss Model of a 12.5 kV, 375 A SiC MOSFET Power Module

3.1 Literature Review

The semiconductor device serves as the core component in the power converter design because its physical characteristics determine the system performance limits and specify the peripheral hardware design requirements, including the module cooling system and device gate driver. In order to operate the proposed MV isolated PFC rectifier at the premium status and maximize its full potential, an advanced power module is a necessary.

The development of silicon (Si) insulated-gate bipolar transistor (IGBT) since 1980s has promoted the development of the high power MVD based on the voltage source converter (VSC) topology. Si IGBT has numerous advantages including easy gate drive, low conduction loss, mature packaging technology and superior ruggedness and reliability. In response to the market needs, semiconductor manufacturers have released numerous high power IGBT modules. Infineon has 6.5 kV module rated from 250 to 750 A using the third generation Trench Field Stop technology (IGBT3-E3).

However, silicon is not an ideal material for the next generation MV-VFD because the wide band gap (WBG) materials have better performance. Recently, the WBG semiconductor industry has witnessed rapid growth and many commercial products based on the silicon carbide (SiC) and gallium nitride (GaN) have been introduced. SiC power devices based on the vertical device structure are particularly suitable for the high-power applications because they can be scaled to higher voltage ratings more easily compared to the lateral GaN power transistors [43]-[45]. SiC material has about ten times the electric field strength than Si as well as much higher thermal conductivity [46]. This means that higher current density can be achieved for SiC semiconductors for a given breakdown voltage. Fig. 3.1 is a summary of SiC, GaN and Si materials in terms of the energy gap, melting point, saturation drift velocity, thermal conductivity and breakdown field.

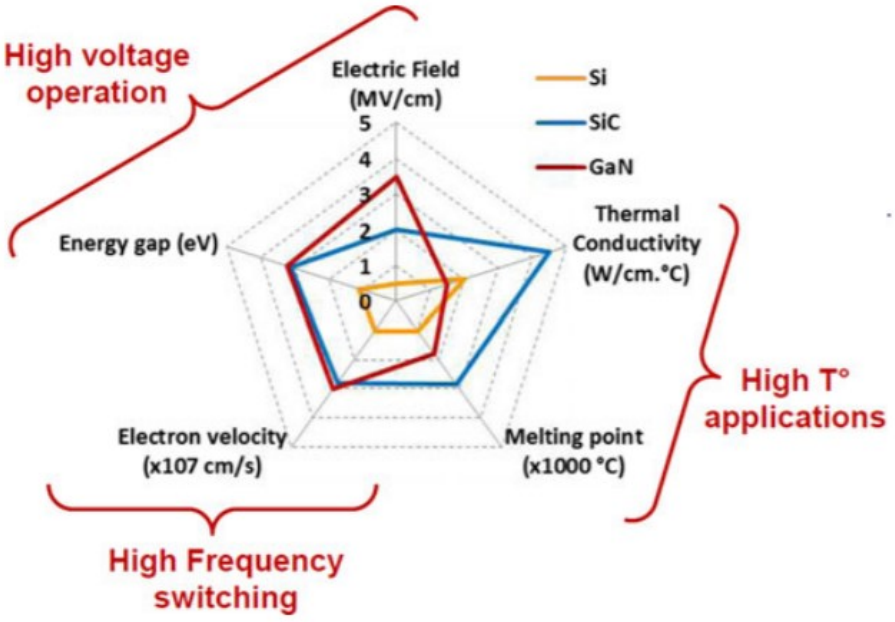


Fig. 3.1 Summary of Si, SiC and GaN Relevant Material Properties [47]

Refer to the device selection, IGBT is not an ideal choice for the next generation MV-VFD because its bipolar current conduction mechanism limits the switching speed, especially for high power modules [48]. Normally, its switching frequency is capped at 2 kilo-hertz (kHz). The negative effects include the large parasitic components and low power density. In addition, given the same operational condition, IGBTs have larger switching loss than other choices (for example, MOSFETs), which complicates the heat sink design and compromises the system operating efficiency.

The novel three-phase PFC rectifier put two critical requirements on the semiconductor device which make Si IGBT not applicable. First, the switching frequency needs to be as fast as 50 kHz with minimal switching loss. Second, the input of the circuit connects to a high voltage power grid. So, the voltage rating of the device is 12.5 kV which is much higher than the existing 6.5 kV Si IGBT modules on the market.

3.2 A Novel SiC MOSFET Module

Compared with Si IGBT, the SiC MOSFET module is a great choice for the next generation MV-VFD. A novel SiC high power MOSFET module rated at 12.5 kV and 375 A is proposed, investigated and introduced to the MV three-phase PFC rectifier. Huang gave a full review of the commercial SiC power devices [49]. The hybrid SiC module is rated up to 1700 V and 1200 A.

The full SiC module is rated up to 1700 V and 383 A. A prototype 15 kV, 10 A SiC MOSFET samples have been developed by Wolfspeed and tested by the authors' group [50] [51]. Starting with the prototype chip, some analyses and derivation are used to design the hypothetical SiC MOSFET chip parameters [52]. The modified SiC chip is a cost-out version, rated at 10.5 A and 12.5 kV, remains the same size as the prototype. This module includes thirty-six SiC chips, which are connected in parallel and boost the load current up to 375 A. The physical size and chip layout are shown in fig. 3.2.

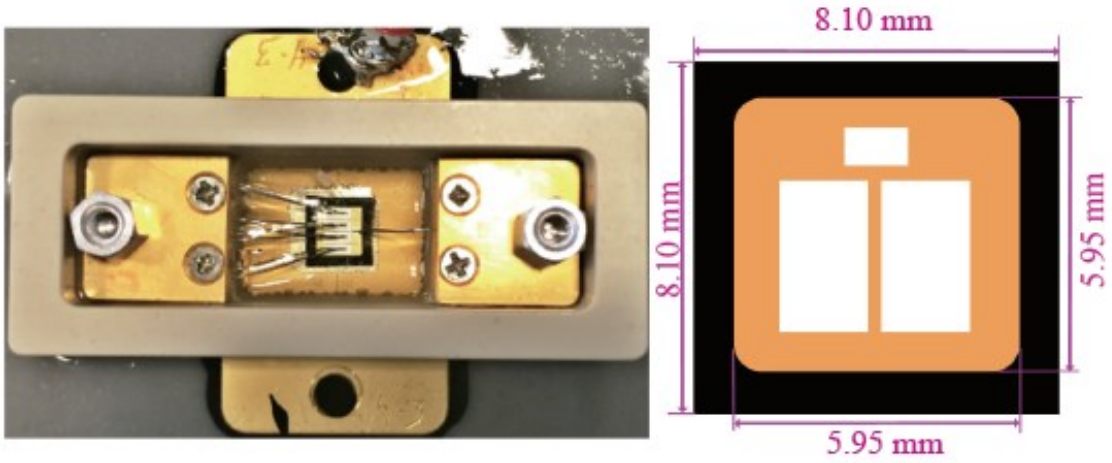


Fig. 3.2 SiC MOSFET Die, Packaged Module & Die Dimension [50]

(Active Chip: 35.40 mm^2, Chip size 65.61 mm^2)

Typically, separate SiC junction barrier Schottky (JBS) diodes are added for a practical reason. The MOSFET body diode has the undesirable reverse recovery performance when the massive carriers are implanted by the PN junction. Besides, the device performance degradation and lifetime reduction occur because of the forward conduction of the PN junction. The additional JBS diodes avoid the body diode conduction on the hardware level.

Some research teams have reported this degradation issue been resolved in 1200 V SiC MOSFETs. Assume this similar technology would be applied to this 12.5 kV module, the body diode can at least conduct for a short period of time without the performance degradation. The strategy is to operate the SiC MOSEET as a synchronous rectifier and conduct current bi-directionally. The body diode only works during the dead time period which is several microseconds per switching event. Therefore, the conduction loss is mitigated due to the low

voltage drop across the MOSFET chip. The whole power module is designed more cost-effectively since there is no need to add additional JBS diodes.

Fig. 3.3 is a cutaway drawing of a SiC 375R12500 (12.5 kV, 375 A) MOSEFT module. The location of the SiC die, die attach, power substrate, substrate attach and based plate are highlighted for manufacturing reference. In order to reduce the module footprint, only single MOSFET module is packaged per case. The plastic case of Infineon FZ750R65KE3 (6.5 kV, 750 A) is selected to standardize the packaging procedure.

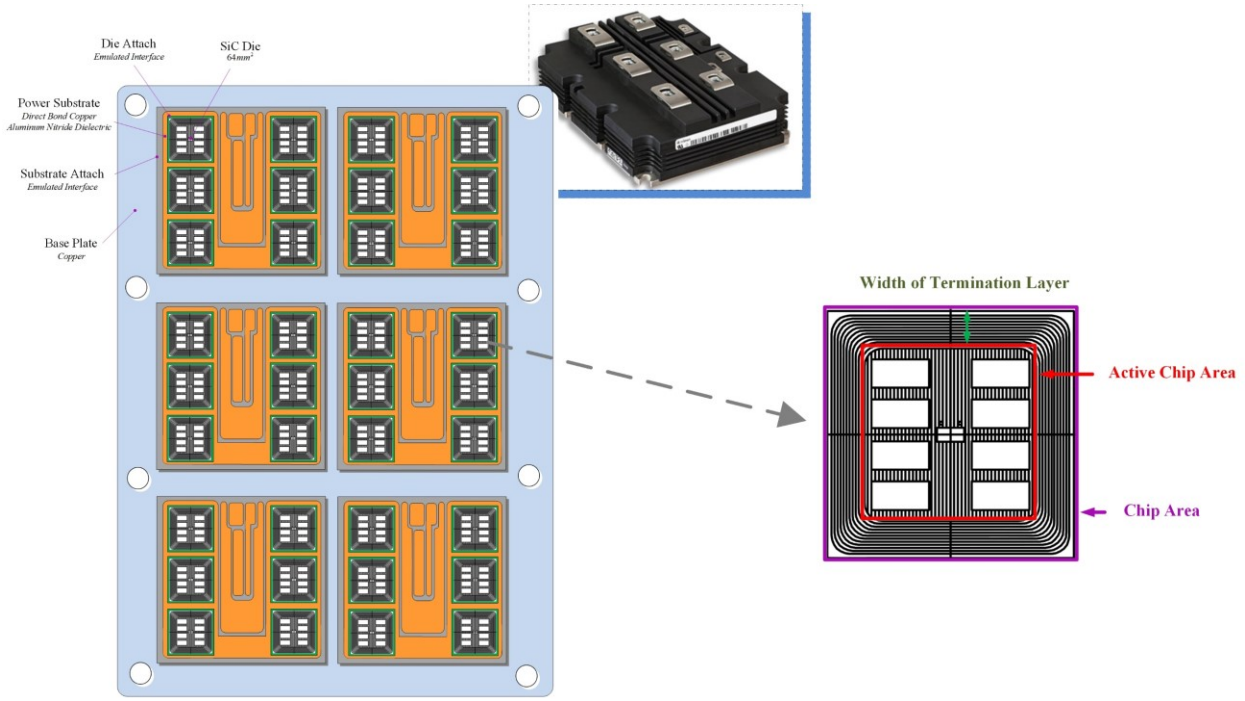


Fig. 3.3 A Cutaway Drawing of SiC 375R12500 (12.5 kV, 375A) MOSFET Module

The power loss model of the proposed SiC MOSFET is developed for system evaluation purpose. Based on the test results of a 15 kV, 10 A SiC MOSFET sample [51] [53] and the datasheet of Infineon FZ750R65KE3 Si IGBT module, the parameters and characteristics of a SiC 375R12500 (12.5 kV, 375 A) MOSEFT module are debrided as below,

The relationship between the chip area and the thermal impedance from junction to the heat sink is required to describe the power modules' thermal properties.

$$R_{th,JS(SiCMOSFET)} = R_{th,JS(SiIGBT)} \times \frac{A_{chip(Si)} \times N_{Si}}{A_{chip(SiC)} \times N_{SiC}} \approx 38.86\ (K/kW) \qquad \text{Equation 3.1}$$

The SiC MOSFET module conduction loss depends on the load current and drain-source on resistor which is temperature dependent. Table 3.1 lists the on-resistance values under different temperatures.

Table 3.1 Drain to Source Resistance of SiC375R12500 SiC MOSFET Module

Temperature (^oC)	$R_{DS(on)}$ $(m\Omega)$, $V_{GS} = 20$ (V)
25	10.6
75	16.4
125	26.0
175	41.5
225	59.8

Theoretically, there is no turn-on loss because of the zero-voltage switching (ZVS) implementation. The turn-off loss is reduced because of these two arguments. One, the turn-off loss is ultra-low due to the load current limiting parasitic capacitance charging process. Second, the stored energy gets dissipated or recovered in the next turn-on event because of the ZVS function. For the future reference, the switching loss model is developed. The energy per switching event is associated with the chip area, transient current, voltage drop between collector and emitter. The switching frequency is involved in the switching loss calculation. Equation 3.2 and 3.3 are numerical expressions for the module switching losses.

$$\begin{cases} E_{on}(I) = N_{chip} \times E_{on}(0A) \times \sqrt{\dfrac{15}{12.5}} + 0.5 \times I \ (mJ) \\ \qquad\quad \approx 36 \times 4.5 \times 1.10 + 0.5 \times I \ (mJ) \\ E_{off}(I) \approx 0 \ (mJ) \end{cases} \qquad \text{Equation 3.2}$$

$$P_{Swiching} = f_s \times [E_{on}(A_{chip}, I_{ds}, U_{ds}) + E_{off}(A_{chip}, I_{ds}, U_{ds})] \qquad \text{Equation 3.3}$$

The device power loss model is implemented in Piecewise Linear Electrical Circuit Simulation (PLECS) platform. The three-dimensional (3D) diagrams are used to describe both turn-on and turn-off dynamics. In the meanwhile, a two-dimensional (2D) diagram is used to simulate the output characteristics at different temperatures. Refer to the thermal equivalent circuit, the foster network is established, and the transient thermal impedances are calculated accordingly.

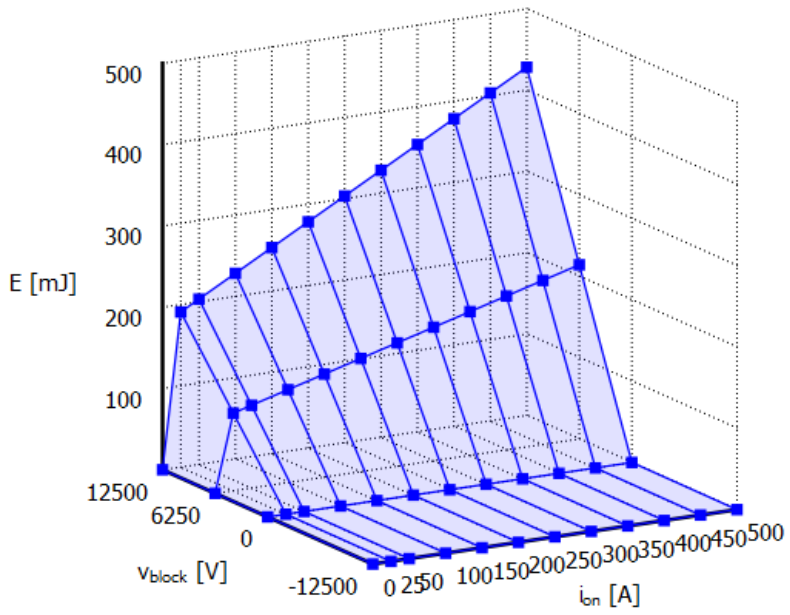


Fig. 3.4 SiC 375R12500 (12.5 kV, 375A) MOSFET Model, Turn-on Energy Model

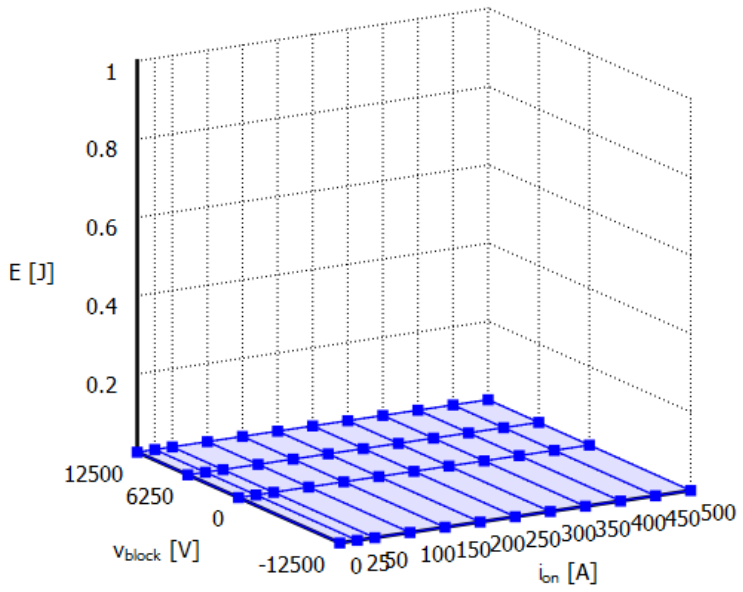


Fig. 3.5 SiC 375R12500 MOSFET, Turn-off Energy Model

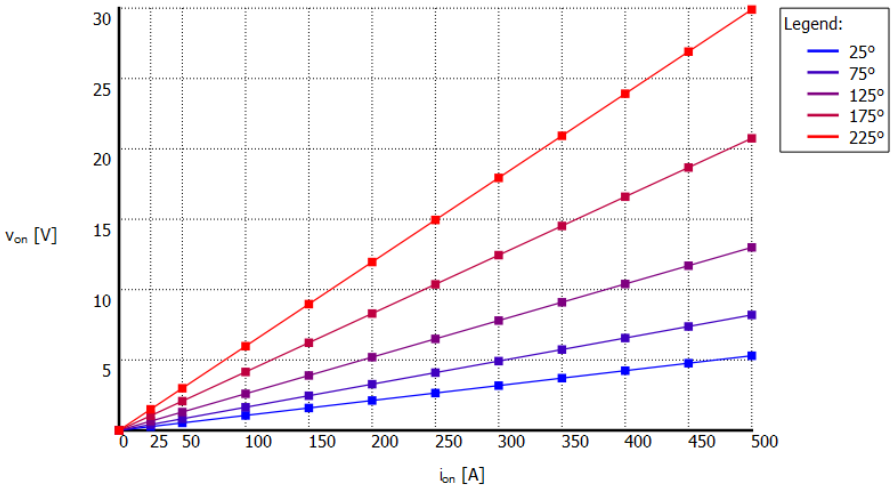
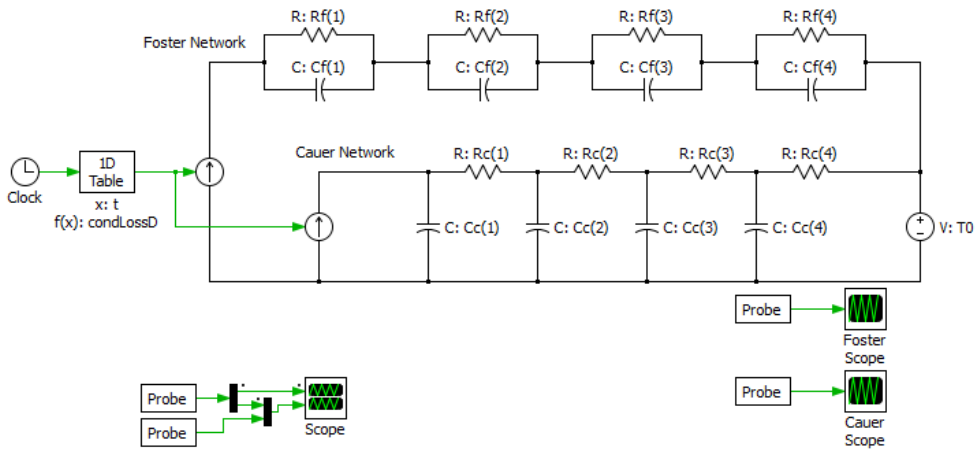


Fig. 3.6 SiC 375R12500 MOSFET, Output Characteristics



	1	2	3	4
R	0.0027 K/W	0.0115 K/W	0.0028 K/W	0.0016 K/W
τ	0.005 s	0.048 s	0.313 s	3.348 s

Fig. 3.7 SiC 375R12500 MOSFET, Transient Thermal Impedance

The device electrical and thermal models are used for the overall system performance evaluation which provides some guidelines for the thermal management and heatsink design. The next step is to implement the proposed SiC MOSFET device model in a 1 MVA DAB VFD system and complete the system-level study. For comparison purpose, the traditional 1 MVA silicon (Si) 3-level neutral-point clamped rectifier power loss distribution is presented.

Table 3.2 1 MVA SiC MV Isolated Three-Phase Rectifier Power Loss Distribution

（Switching Frequency: 10 kHz ~ 50 kHz）

Location	Designator	Conduction Loss (W)	Switching Loss (W)
Transformer Primary Side	P1	305	0
	P2	307	0
Transformer Secondary Side	S1	420	0
	S2	426	0
	S3	442	0
	S4	427	0

Table 3.2: continued

SiC MV Isolated 3 Phase Rectifier	6981	0
HF Transformer	~ 10000	
System Efficiency	98.3%	

Table 3.3 1 MVA Conventional Si 3L-NPC Rectifier Power Loss Distribution
(Switching Frequency: 540 Hz)

Description	Conduction Loss (W)	Switching Loss (W)
IGBTs-Outer	2	162
Diodes-Outer	140	506
IGBTs-Inter	43	1806
Diodes-Inter	140	0
Clamped Diodes	83	23
Single Phase Circuit	338	2497
Si MV Non-Isolated 3 Phase Rectifier	1037	7531
24-Pulse Phase-Shifting Line Frequency Transformer	~ 15000	
System Efficiency	97.64%	

Per above tables, the proposed SiC PFC DAB rectifier has around 30% power loss less than the traditional Si 3L-NPC converter. Besides, it operates as kilo-Hz range which is over 10 times faster than the traditional circuit. Kilo-Hz operating mode brings many benefits, like high power density and premium power quality. In a commercial 1 MVA MV-VFD (fig. 3.8), the 24-pulse line frequency phase-shifting transformer and the diode-based rectifier is as large as 127 cm (depth), 165 cm(width), 234 cm(height) and 4445 kilogram(kg). Per fig. 3.9, a 1 MVA SiC MV isolated three-phase rectifier is sized as 76 cm (depth), 58 cm(width), 46 cm(height), which is 96% smaller than the conventional products. Moreover, it is designed as a portable system and can be mounted on a frame with rollers.

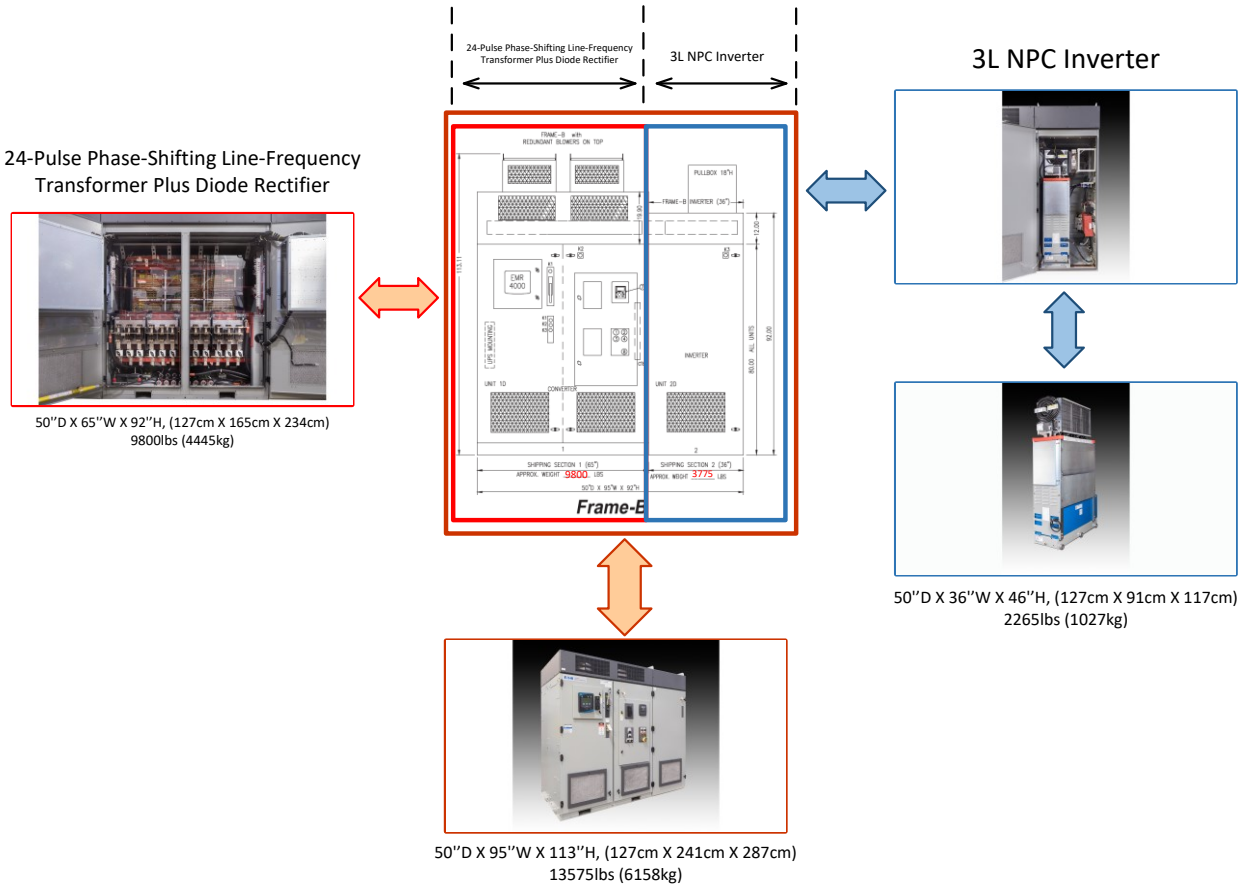


Fig. 3.8 The Drawing of An Industrial 1 MVA MV-VFD Product (Eaton SC9000)

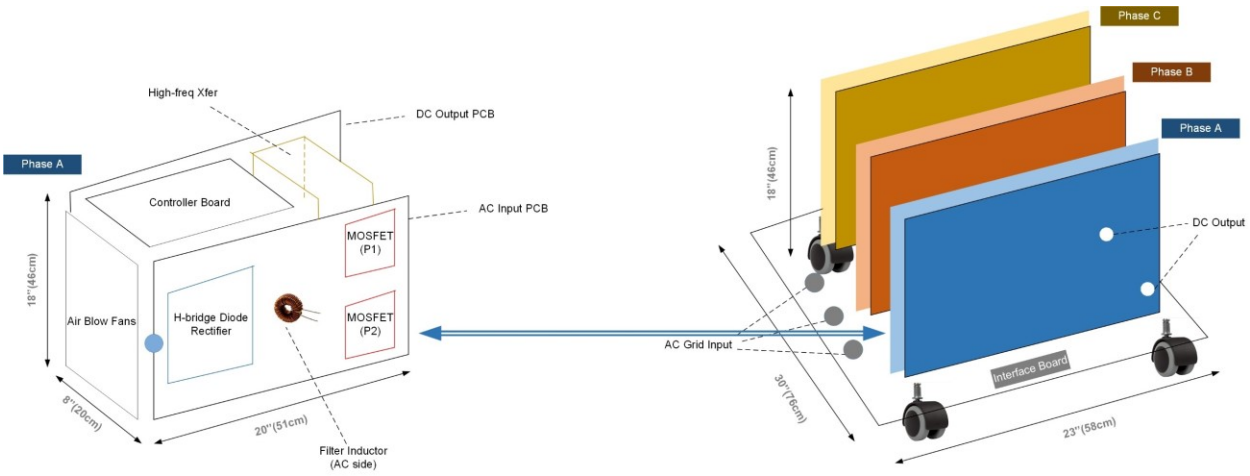


Fig. 3.9 The Drawing of 1 MVA MV-PFC Rectifier

4 Control Scheme of the MV-PFC

4.1 Literature Review

The proposed SiC MV-PFC AC-DC rectifier is based on the isolated dual-active bridge (DAB) theory. The DAB circuit earns its reputation in the high-frequency link (HFL) DC-DC power conversion systems (PCSs), which serves as a core part in the electricity infrastructure when an output DC link is demanded [54]-[57]. Compared with the transformer-less topologies, the DAB circuit provides the galvanic isolation which improves the overall system safety under the catastrophic failures. The DAB converter has been researched and targeted to some LV applications, like electric vehicles, storage batteries for the uninterruptible power supplies (UPS) or energy interface of photovoltaic (PV) panels.

Recently, solid-state transformer (SST) theory introduces DAB circuit to the AC-DC world as a two-stage combo system. Inside of the SST, an H-bridge is placed at the input side to rectify the AC power to the DC output. A DAB converter is followed to regulate the DC voltage at different level. Hence, the DAB is still controlled in the DC-DC mode. Many papers talk about its control algorithm for reactive energy elimination, efficiency optimization and extended power operating range [58]-[63].

My proposal is to improve the DAB structure to accept AC input without adding additional rectifier circuit. The proposed SiC PFC rectifier is classified as a one-stage integrated system and converts AC power to the DC output directly, that requires a novel AC-DC control scheme. Differ to the conventional DC-DC operating mode, AC-DC topology needs to coordinate with time-variant input power. Besides, the control system needs to meet the demands of the electrical machine operation. In the steady state, the system needs to operate as an ideal voltage source and interface with different loads since the motor can be lightly loaded or heavily loaded. Talking about the transient states, the system needs to provide enough power to the loads since motor would stall or jam if inadequate energy. In order to meet all the requirements, an advanced control scheme consisting of the system-level control and modulation technique is developed.

4.2 A Novel MV-PFC Control Scheme

The control scheme and the key signals are highlighted in fig. 4.1 - 4.2. The system-level control consists of two layers. The external layer is of the voltage feedback control, which monitors and

regulates the DC output bus at the rated level by keeping updating the power transfer command. Besides, it balances the power command between three phases. The internal layer is a feedforward modulator. Each power module has its own dedicated modulator. Using the DC bus voltage, AC grid input and power command coming from the voltage feedback loop, the modulator calculates and provides the MOSFET gating signals for next switching cycle. Furthermore, the performance demands can be categorized as the key function blocks, basic function modules and advanced function features. The key function logic includes the power factor correction (PFC), zero-voltage switching (ZVS) and reactive power minimization. The basic function modules are to control the total amount of the power transfer and mitigate the power grid current total harmonic distortion (THD) in compliance with IEEE Std 519, harmonic control in electric power system. As the internal control loop, its time coefficient needs to be much small than the external loop. Last but not least, the advanced features are to accept the wide range of grid voltage and provide the enough power in regardless of the system loading profiles during both transient or steady states.

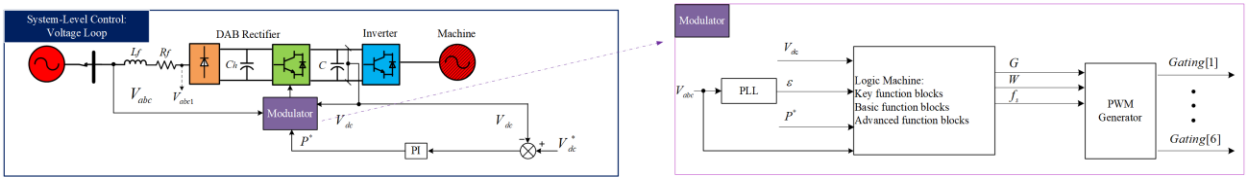


Fig. 4.1 A Two-Layer Control Scheme

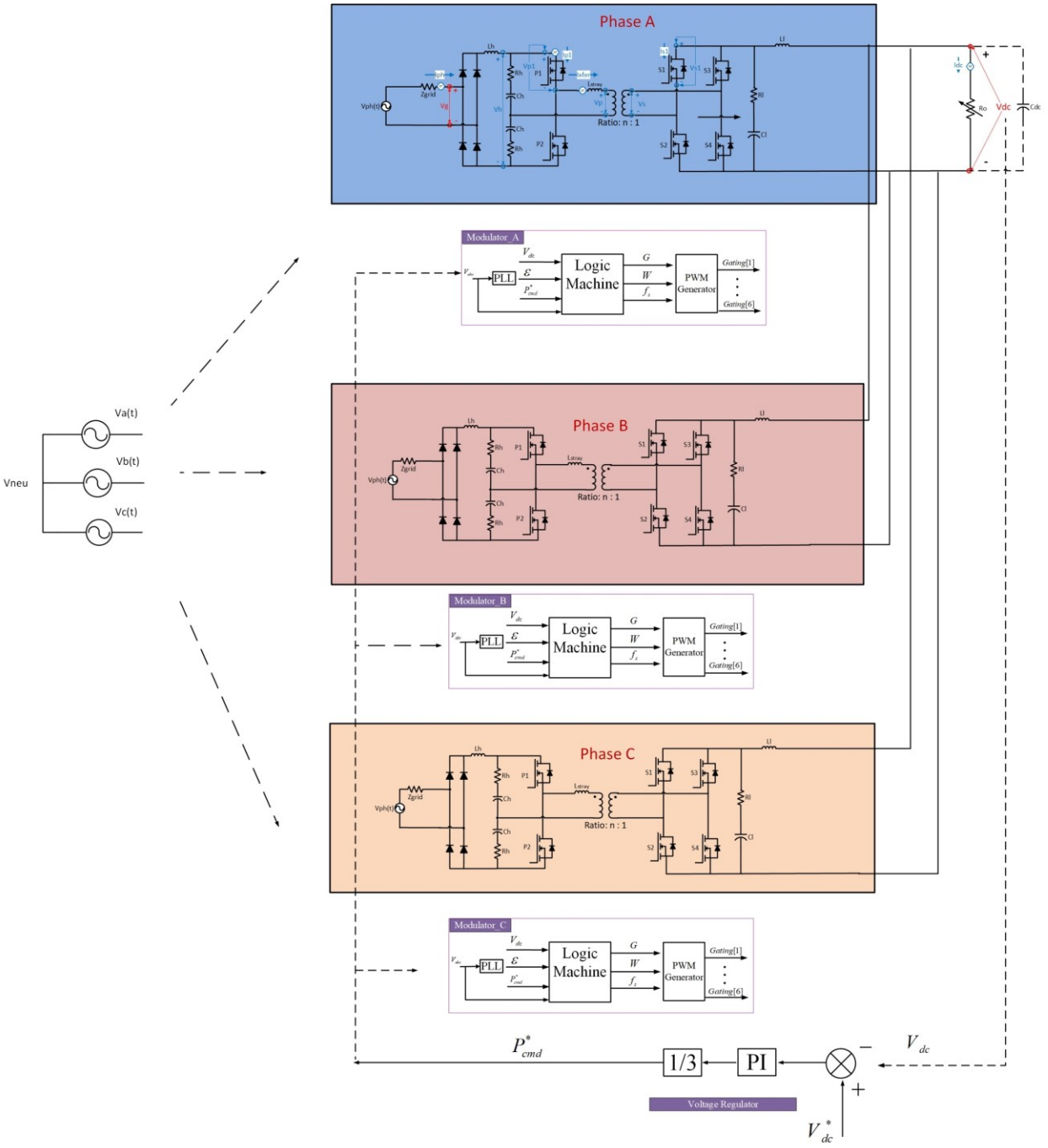


Fig. 4.2 Three-Phase PFC DAB Converter with DC Output Volt Feedback Control

Table 4.1 Feedback Loop Control Parameters

Voltage Loop	
Voltage Control Parameters (P, I)	(0.01, 0.1)

4.3 An Advanced Modulation Technique

The control scheme has both external and internal layers. The external layer is a typical DC output feedback control. The main purpose is to sample and regulate the DC bus to follow the real-time load condition. The internal modulator can be categorized as one of the feedforward controls. Based on the grid voltage, DC bus output voltage, power command and its embedded phase-lock loop (PLL) function, the gating firing signals for next switching cycle are calculated.

A review of the relationship between PWM gating signals and system operating conditions is presented. Zhao [55] listed four different circuit operation modes based on the phase-shifting relationship between power legs. The relationship between firing signals and system transients is shown in fig. 4.3. A large variety of the firing signal combination manipulates the transformer voltage and leakage inductance current waveforms, then achieve different control goals. From left to right, there are single phase shift (SPS), extended phase shift (EPS), dual phase shift (DPS) and triple phase shift (TPS).

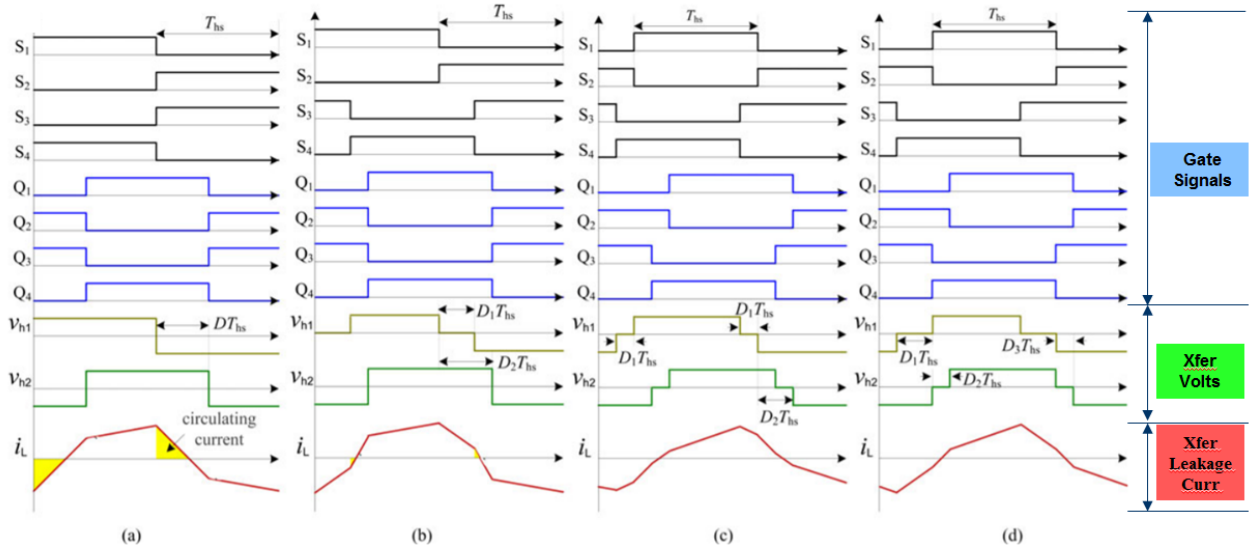


Fig. 4.3 Firing Signal VS System Transients for A Typical DAB Converter [55]

Based on the proposed topology, only SPS and EPS are valid because of the half-bridge circuit on the transformer's primary side. Except for the traditional control variables, the device switching frequency and duty ratio can be used to give additional control freedom. Fig. 4.3 illustrates six firing signals, high-frequency (HF) transformer's voltage and leakage current for both SPS and

EPS control algorithms. Both SPS and EPS are programmed in the PWM generator and ready to be activated under different circumstances.

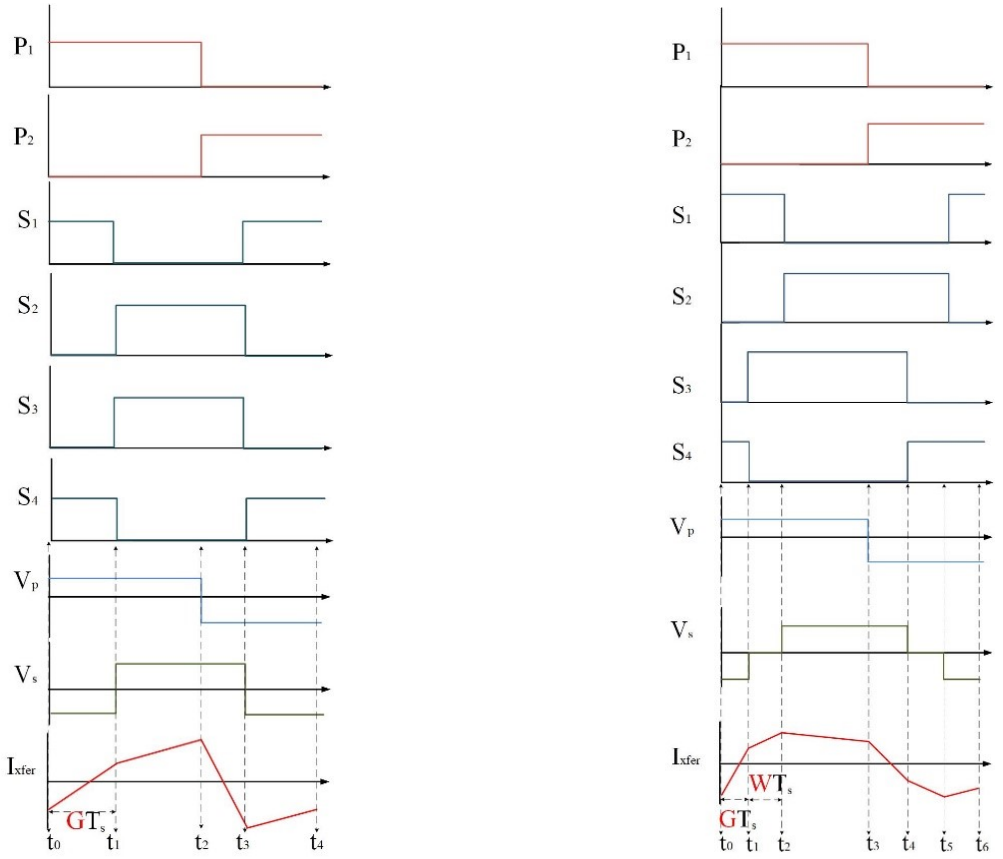


Fig. 4.4 Firing Angles VS Circuit Operating Conditions (Left: SPS, Right: EPS)

Next, it is time to discuss how to calculate the gating signals based on the functional requirements. Per mentioned before, there are three types of the logic blocks, namely key function blocks, basic function blocks and advanced function blocks. The key function blocks achieve four operational goals, such as PFC, ZVS and two optimization goals. The first optimization is to mitigate the transformer reactive power and second one is to limit the leakage current as small as possible. Differ to the key function blocks, the basic and advanced function blocks have different responsibilities. The basic function blocks guarantee the conservation of energy, premium power grid quality and harmonic-free DC output. The advanced blocks introduce self-tuned capability for different grid voltage and produce enough power to the machine during both transient and steady states. In a word, this is a three-degree-of-freedom system and the control variables are defined as below,

a. The device switching frequency *(fs)*.
b. The phase shift between primary side half bridge and secondary side full bridge circuits *(G)*.
c. The phase shift between two legs of the full bridge sitting on the secondary side of the HF transformer *(W)*.

There are two SPS modes used to meet different operating and performance demands. The control variables of SPS1 are calculated from equation 4.1 – 4.3.

In the SPS1 ($f_s < f_{upper}$) mode, the conservation of energy needs to be guaranteed for the safe operating requirement, per equation 4.1.

$$\begin{cases} p_t = \dfrac{|v_g| nV_{dc}(G-2G^2)}{2f_s L_{xfer}} \\ p_t^* = \hat{V}_g \hat{I}_{ph}^* \sin^2(\omega t) - \dfrac{\omega(C_h + C_h)}{4} \hat{V}_g^2 \sin(\omega t)\cos(\omega t) \end{cases} \quad \text{Equation 4.1}$$

In the meanwhile, the modulator computes the numerical values of three control variables by achieving PFC, ZVS and minimum reactive power operation through equation 4.2.

$$\begin{cases} G(t) = \dfrac{1-k+4f_s k\sqrt{C_{eq}L_{xfer}}}{4} \\ W(t) = 0 \\ f_s(t) = \dfrac{|v_g| nV_{dc}(1-2G)G}{2p_t L_{xfer}} \end{cases} \quad \text{Equation 4.2}$$

Furthermore, there are three perquisites for this logic.

$$\begin{cases} k = \dfrac{|v_g|}{2nV_{dc}} < 1 \\ s_i(4.2us \times f_s) \le G(t) \le \dfrac{1}{2} \\ 5k \le f_s(t) \le 50k \end{cases} \quad \text{Equation 4.3}$$

When the switching frequency hits the pre-defined upper level, 50 kHz, the EPS mode is activated. Similar to the SPS1, the safe operating condition is considered first, per equation 4.4.

$$\begin{cases} p_t = \dfrac{\left|v_g\right| nV_{dc}(4G^2 + 4GW + 2W^2 - 2G - W)}{-4 f_s L_{xfer}} \\ p_t^* = \hat{V}_g \hat{I}_{ph}^* \sin^2(\omega t) - \dfrac{\omega(C_h + C_h)}{4} \hat{V}_g^2 \sin(\omega t)\cos(\omega t) \end{cases} \quad \text{Equation 4.4}$$

Next, the three control variables are calculated by resolving polynomial 4.5.

$$\begin{cases} [G(t), W(t)] \Rightarrow \begin{cases} k + 4G + 2W - 1 = \dfrac{4 i_{s1} f_{upp} L_{xfer}}{nV_{dc}} \\ (4G-1) \times k + 1 - 2W = \dfrac{4 i_{s2} f_{upp} L_{xfer}}{nV_{dc}} \\ p_t = p_t^* \end{cases} \\ f_s(t) = f_{upper} \end{cases} \quad \text{Equation 4.5}$$

In addition, three perquisites (4.6) need to be meet in resolving equation 4.5.

$$\begin{cases} k = \dfrac{|v_g|}{2nV_{dc}} < 1 \\ s_i(4.2us \times f_s) \le G(t) \le \dfrac{1}{2} \\ f_s(t) = 50k \end{cases} \quad \text{Equation 4.6}$$

In most cases, SPS1 and EPS are good enough to cover all the operating conditions. However, the waveform distortion at the voltage zero-crossing is observed. As a solution, a special SPS logic, namely SPS2, is developed and enabled only when the input voltage is close to zero. The idea is to allow more reactive power flow which improve the waveform distortion issue under this condition. The control variables are computed from 4.1, 4.7 and 4.8.

$$\begin{cases} G(t) = \dfrac{1}{4} + \sqrt{\dfrac{1}{16} - \dfrac{p_t f_{upp} L_{xfer}}{|v_g| nV_{dc}}} \\ W(t) = 0 \\ f_s(t) = f_{upper} \end{cases} \quad \text{Equation 4.7}$$

$$\begin{cases} k = \dfrac{|v_1|}{2nV_2} < 1 \\ f_s(t) = 50k \\ s_i(4.2us \times f_s) \le G(t) \le \dfrac{1}{2} \end{cases}$$ Equation 4.8

Given the modulator updates fs, G, W every switching cycle, the massive computing workload is assigned to the controller. One option is to use the powerful controller, like Xilinx or Intel FPGA with hard-core processor(s) embedded. Another option is to use traditional digital signal processor (DSP) and have data map pre-calculated and stored in the non-volatile memory. In this case, instead of calculating the variables every cycle, the DSP does a quick search from the data map and get the answers based on the system real-time operating condition. Both of these two implementation approaches have the similar results.

4.4 System Modeling and Description

A time-domain simulation platform has Piecewise Linear Electrical Circuit Simulation (PLECS) for circuitry thermal model been co-simulated with control algorithm implemented in MATLAB/Simulink environment. The system operating conditions, the parasitic components and semiconductor device ratings are summarized as,

Table 4.2 1 MVA MVD System Parameters

System Operating Condition	
Grid Voltage	12.5k (7.2k per phase)
Line Frequency	60 Hz
DC Bus	6 kV
Pout	1 MVA
Xfer Primary Side	
Lh (input filter)	6 mH
Ch (input filter)	1.3 uF
Lstray	1 mH
Transformer Turns Ratio	2:1
Xfer Secondary Side	
Ll (output filter)	15 uH

Table 4.2: continued

Cl (output filter)	75 uF
Semiconductor (SiC MOSFETs) Ratings	
Voltage Rating	12.5 kV
Current Rating	375 A
Switching Frequency	< = 50 kHz

4.5 Soft Start-up Strategy and Application State Machine

System operating safety is an inevitable design topic in any power electronic systems. Normally, the power converter shuts down and restarts multiple times during its life time for regular maintenance purpose. The conventional boost PFC rectifier has the huge inrush current and requires the additional shunt resistor. The earlier literatures barely talked about circuitry soft start-up strategy. Some researchers claimed to eliminate the potential inrush energy by regulating the control reference signal. This chapter first introduces a practical start-up procedure to mitigate the inrush current and gently bring the DC output bus up to its rated level.

The solution is to develop an application state machine which includes the system soft start-up procedure. Fig. 4.6 is of a graphic state flow diagram of the application state machine. This application state machine is another layer added above the control logic machine. The soft start-up procedure shown in fig. 4.6 has the inrush current limiting capability by coordinating the timing of closing the line contactor and firing the MOSFETs. In this case, the inrush current coming from the high DC bus is effectively limited. Except for the soft start-up, it is also in charge of the I/O management and the system protection scheme. The system protection scheme will be discussed in chapter 4.7. The I/O management includes the following logics.

a. Analog Input (AI): grid voltage, DC output voltage, SiC MOSFET device voltage and current (measured by its gate driver). high DC bus voltage (optional), HF transformer leakage current (optional), load current (optional), HF transformer primary and secondary voltage (optional). grid current (optional).
b. Digital Input (DI): start/stop (2-wire logic), fault reset, main contactor axillary feedback.
c. Digital Output (DO): close main contactor (relay output), fault light indicator.
d. Fiber Optic (FO): six MOSFET firing signals, six MOSFEC acknowledgement signals

e. Communication Port (Comm): a controller area network (CAN bus), Ethernet IP, RS485.

The I/O management works as the basic function module to support many application and control blocks (fig. 4.5). For example, a succeed soft start-up procedure requires the I/O function involvement.

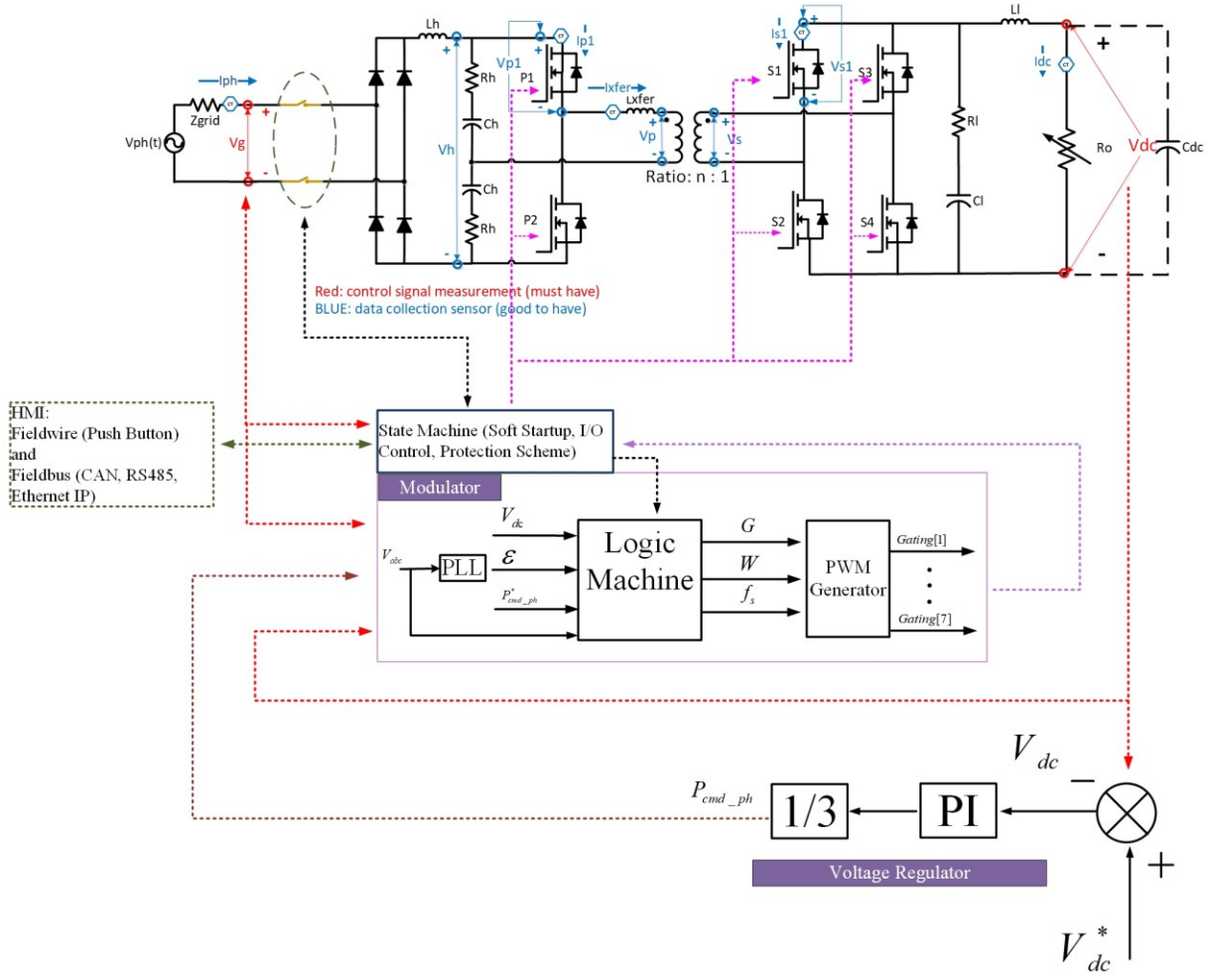


Fig. 4.5 System Application Layer, I/O Management

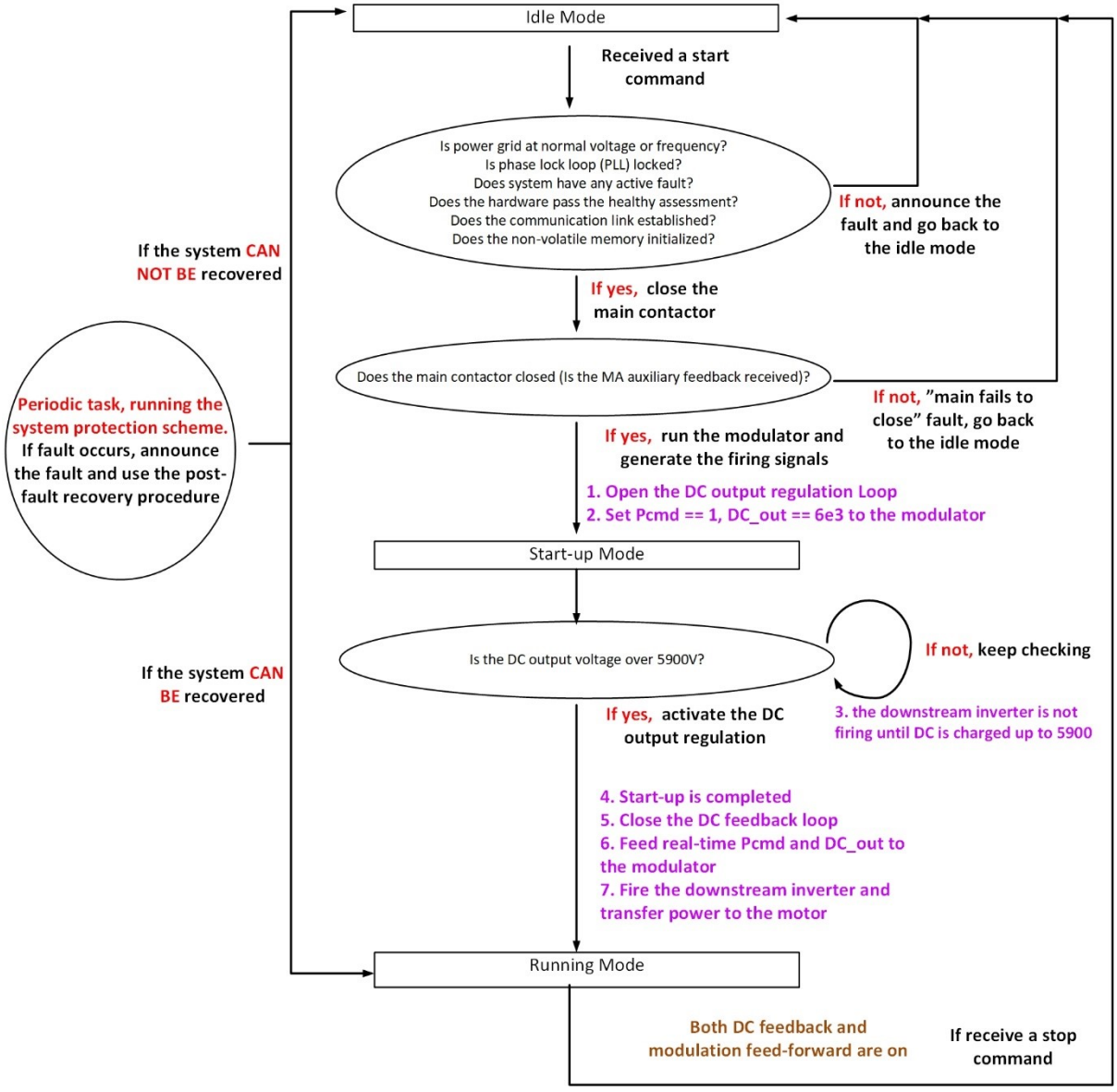


Fig. 4.6 System Application Layer State Machine

Moving to the DC output side, two practical soft start-up approaches can be used to safely charge the output DC bus to its rated value. One is to use an external pre-charge circuit which charges energy storage component, DC output capacitor, before the system starts. This method does not need to change the control logic but require the additional pre-charge circuit. this method is not favored because of the pre-charge hardware footprint and cost. Another option is to temporarily disable the DC output feedback loop until it goes above certain level. Author prefers this option because of its flexibility and no extra monetary investment required. The logic can be stated as below,

a. After receiving the system start-up command, keep minoring the DC output value.
b. Given the DC output value is less than 98% rated value (5900 V), enable the modulator feedforward logic and disable DC output regulation control.
c. Once the DC output value is ever above the 98% rated value (5900 V), enable both modulator feedforward and DC output feedback control. Then, start transferring power to the downstream circuits.

Fig. 4.7 – fig. 4.11 are of the grid voltage and current, output waveforms and SiC MOSFET voltage and current during the soft start-up procedure. No inrush current is observed.

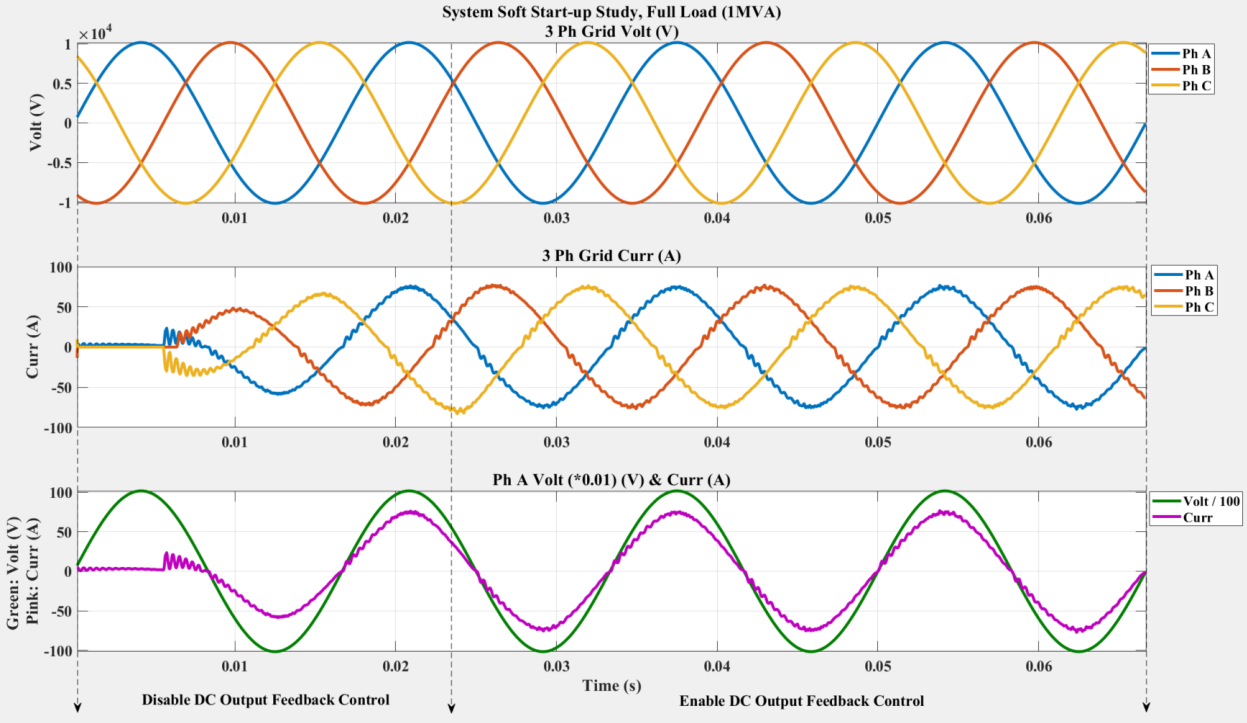


Fig. 4.7 AC Input of The System Soft Start-up Study, Full Load

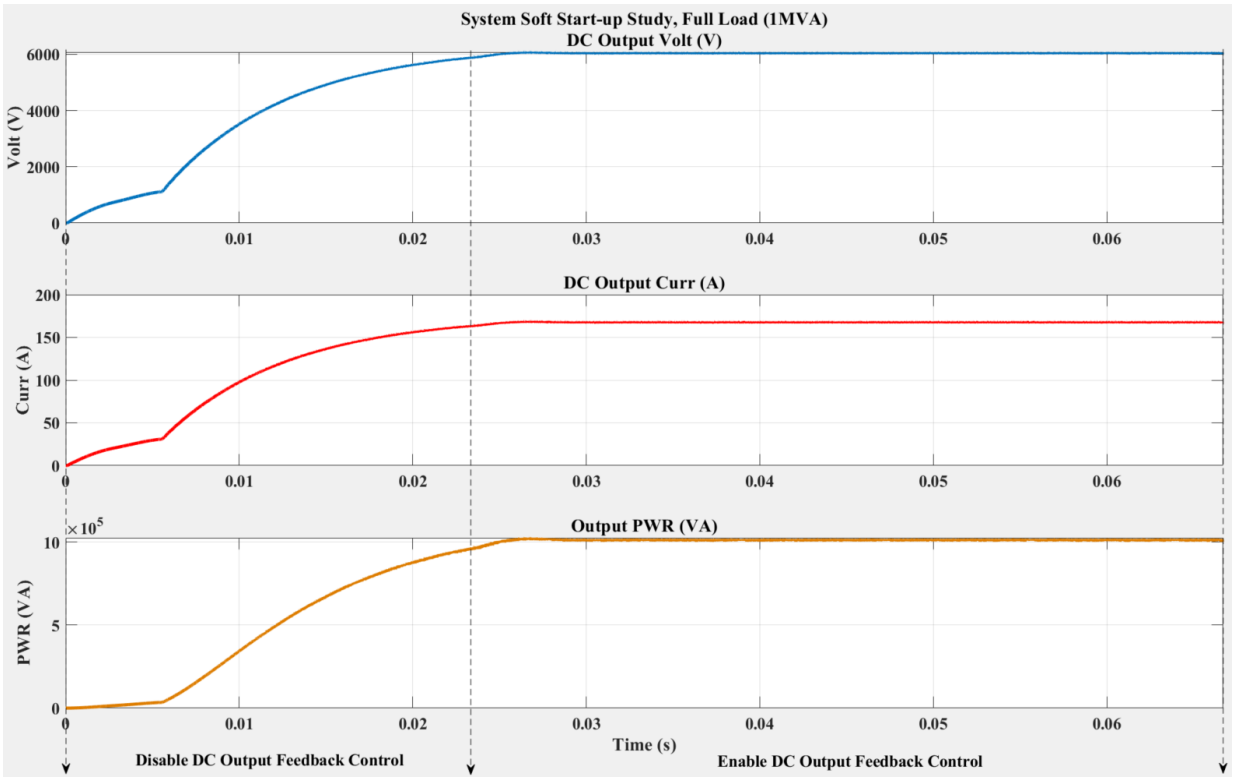


Fig. 4.8 DC Output of The System Soft Start-up Study, Full Load

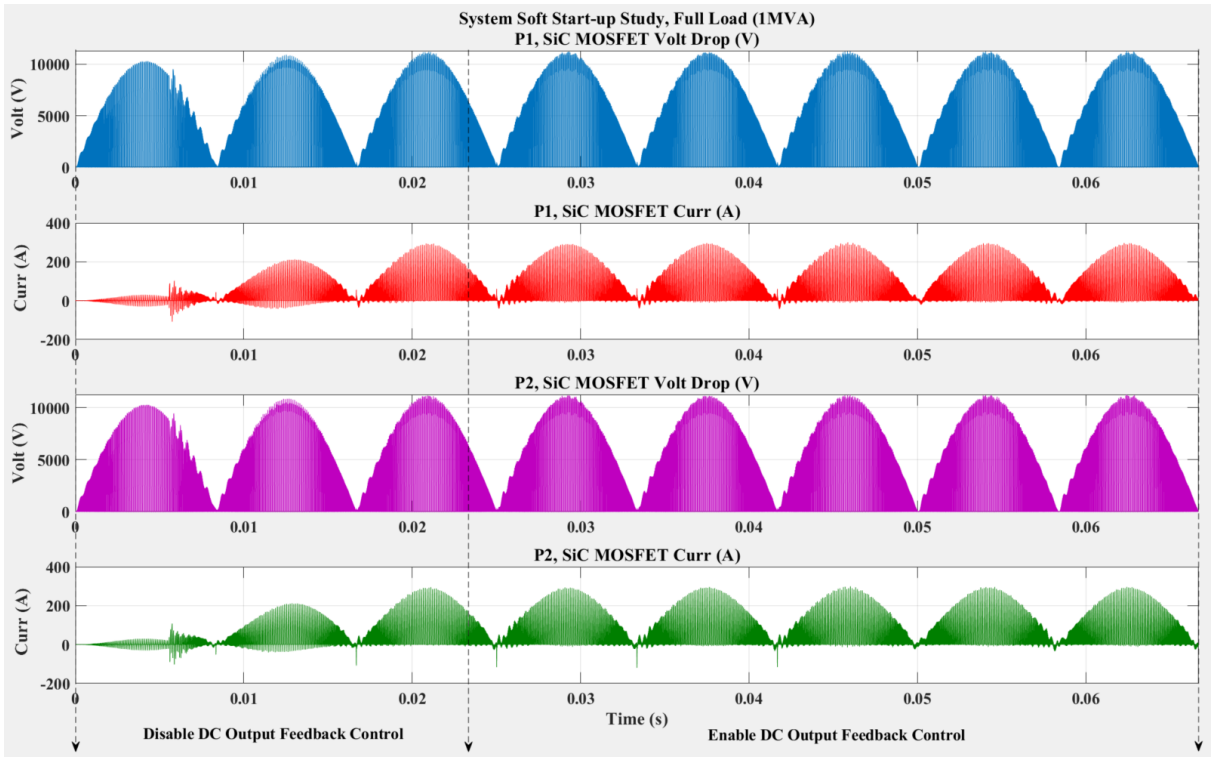


Fig. 4.9 Device P1, P2 Volt & Curr of The System Soft Start-up Study, Full Load

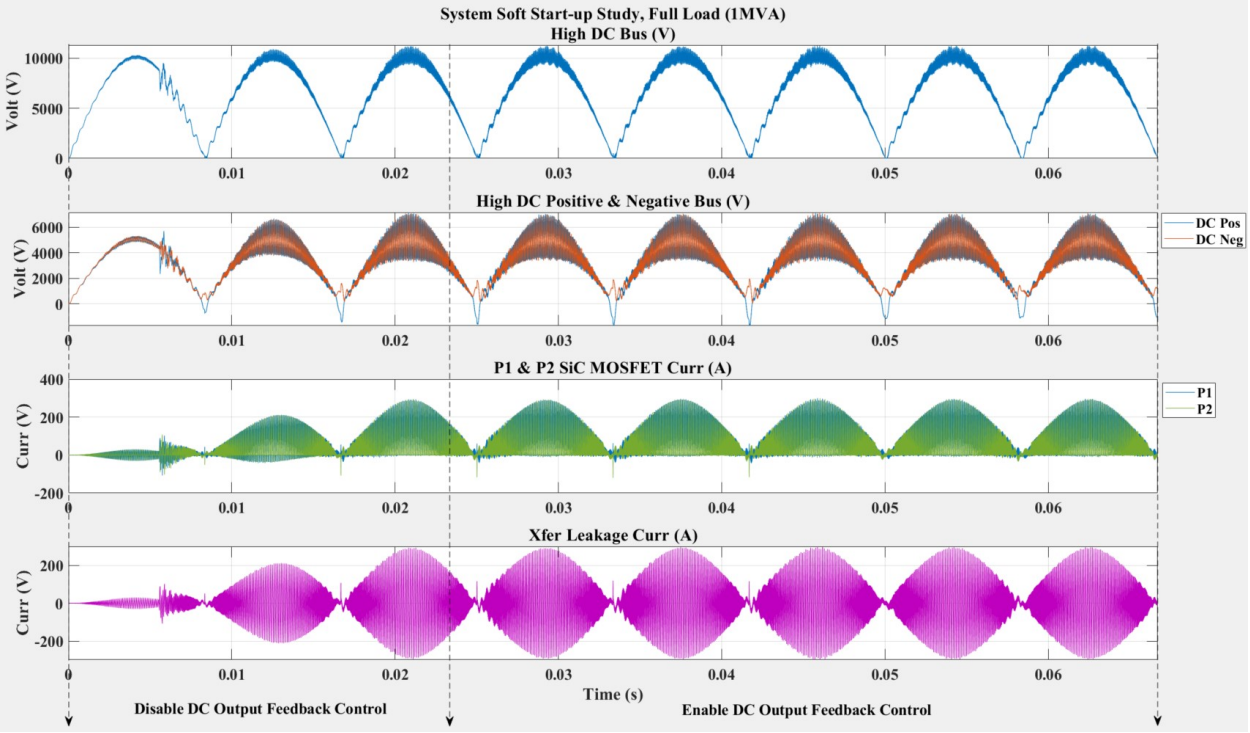


Fig. 4.10 High DC Bus and Resonant Curr of The System Soft Start-up Study, Full Load

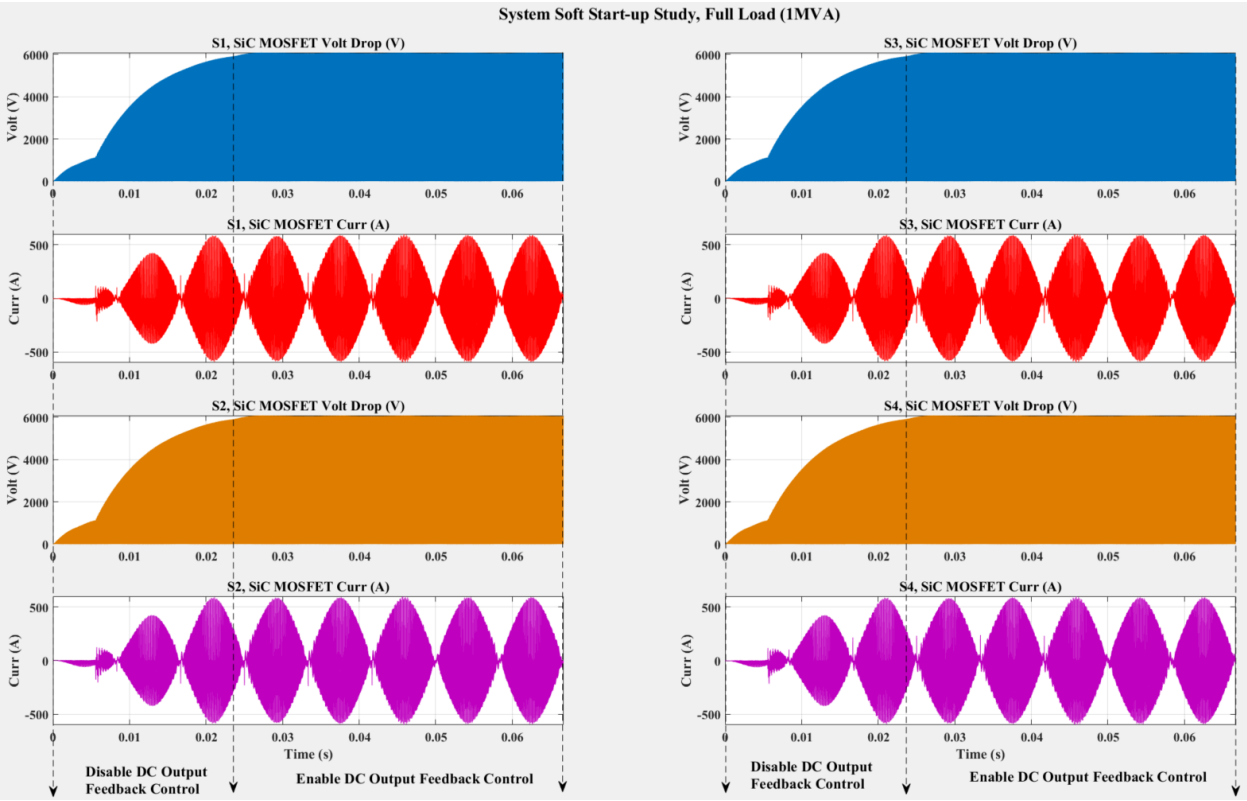


Fig. 4.11 Device S1 – S4 Volt & Curr of The System Soft Start-up Study, Full Load

The proposed system soft start-up procedure ensures no inrush current during the normal start-up sequence. It takes about 0.022 second, less than two-line cycles, to bring the DC output bus to its full level. At that moment, the system soft start-up procedure is completed and ready to be in the service. The DC output capacitor charging time can be treated as the unpredictable time delay in the control loop. The strategy is to ignore this period by deactivating the DC bus feedback control. The timing of closing the DC bus control loop is highlighted in the waveforms. This case study proves the system can ramp up from stop to the full energy states safely and quickly.

4.6 Steady State Performance

The system steady state study includes two sections. First, the feedforward modulator is developed and demonstrated from light-load to over-load conditions. The relationship between the gird input and three control variables is emphasized. These three control variables are the inputs to the gate firing generator. Second, the DC output voltage feedback loop is added and coordinates with the feedforward modulator. The three-phase grid input and DC output are evaluated. The functional modules, like zero-voltage switching (ZVS) and self-tuning capability for the customized load profiles are demonstrated.

The bellowing figures show the waveforms of phase A grid voltage, current and three control variables (G, W and Freq) under different loads. The control variables are calculated based on the grid waveforms in real-time. It needs to emphasize that input voltage and current are in phase and the unity power factor feature is guaranteed in regardless of the load condition.

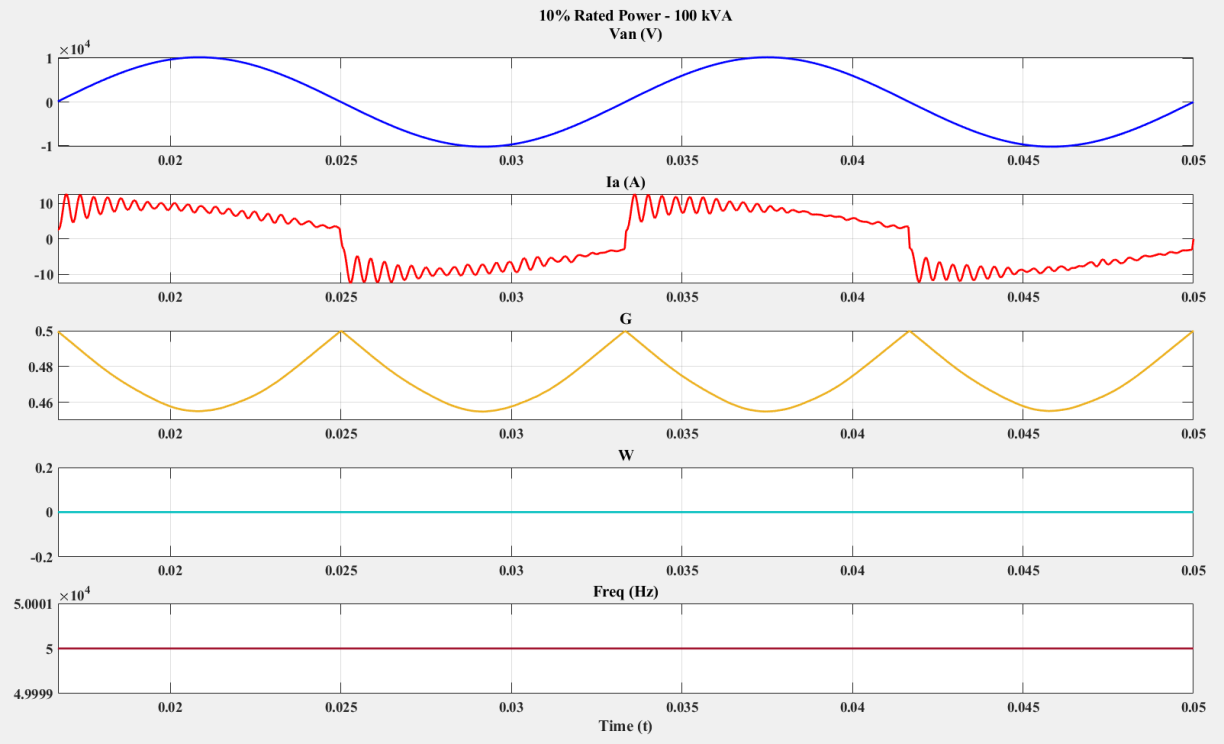


Fig. 4.12 Steady State Waveforms at 100 kVA Load

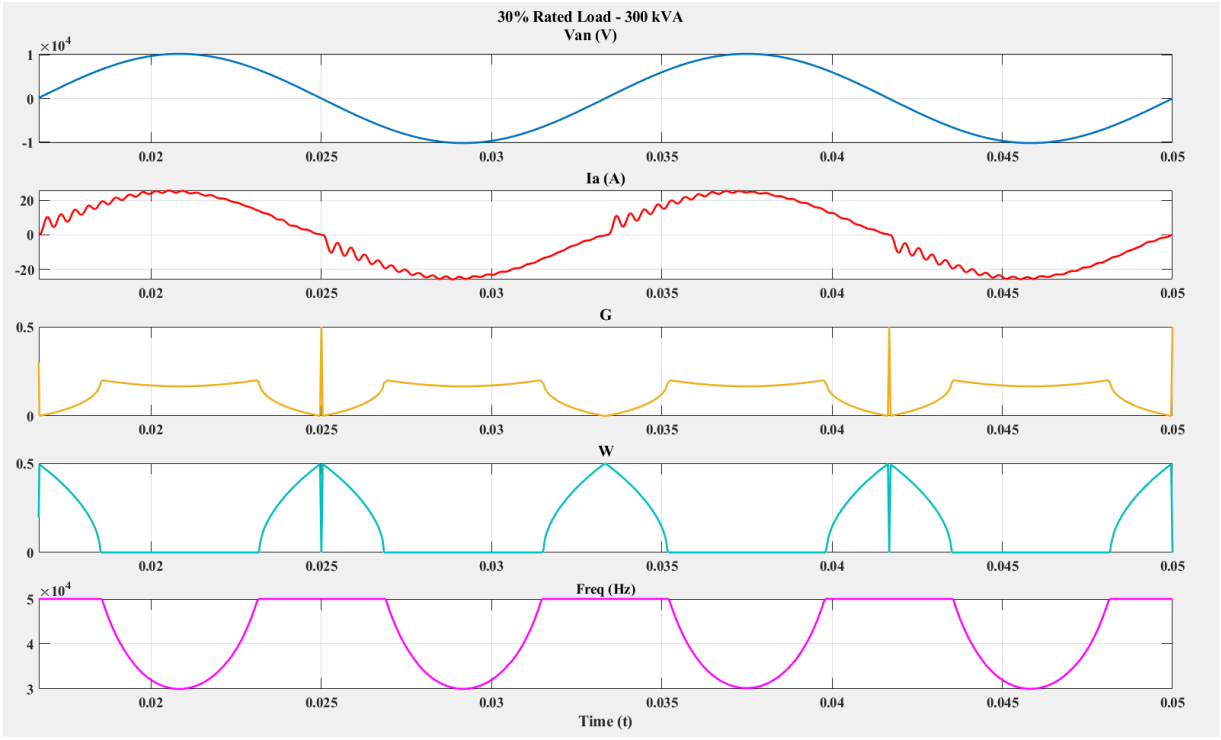


Fig. 4.13 Steady State Waveforms at 300 kVA Load

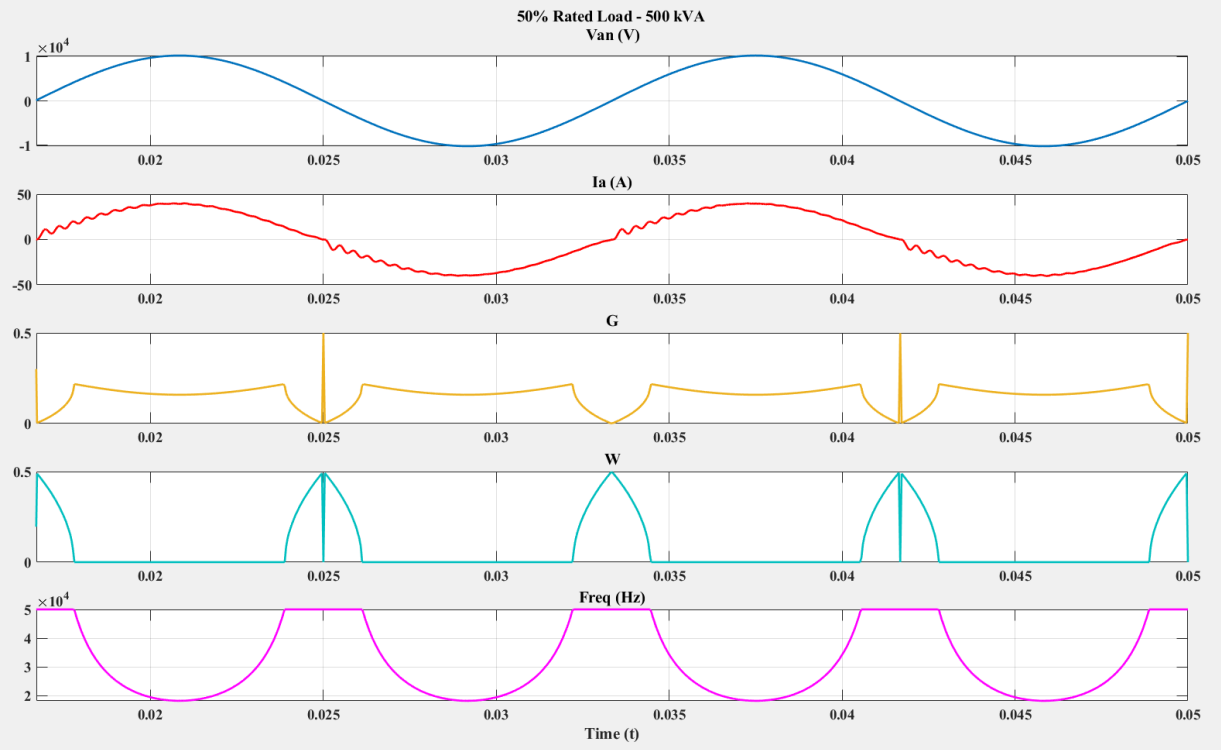


Fig. 4.14 Steady State Waveforms at 500 kVA Load

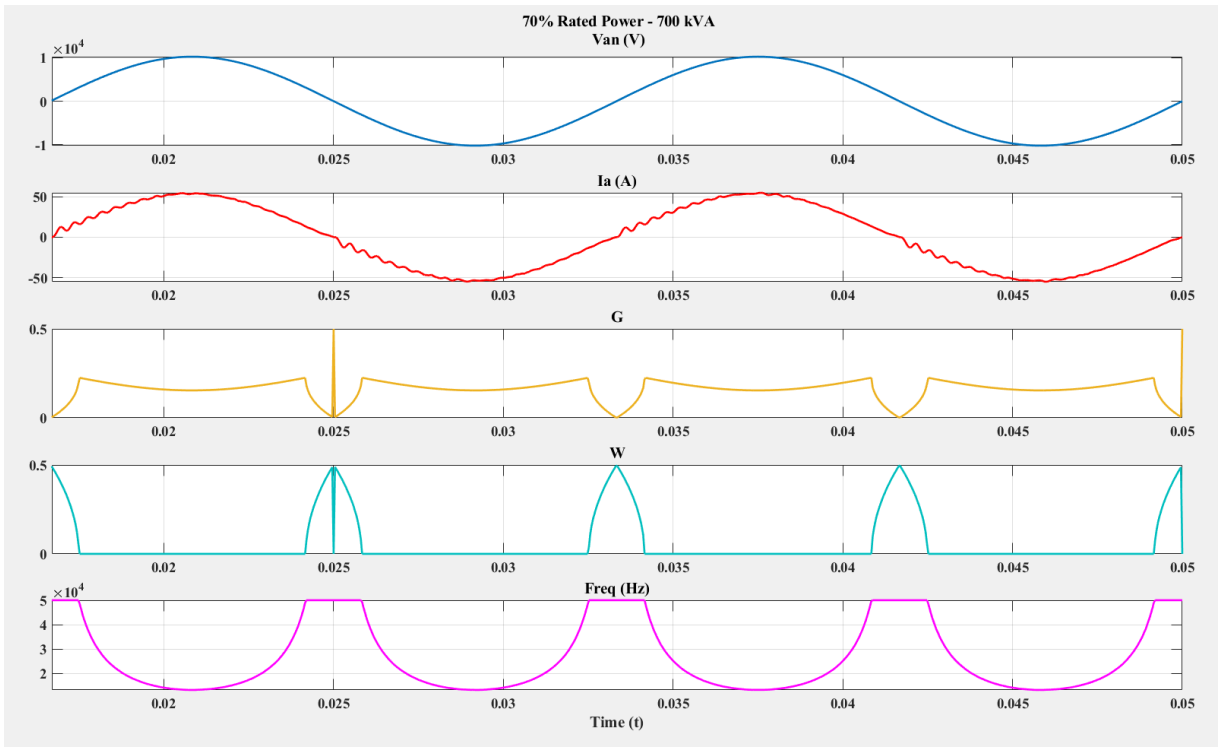


Fig. 4.15 Steady State Waveforms at 700 kVA Load

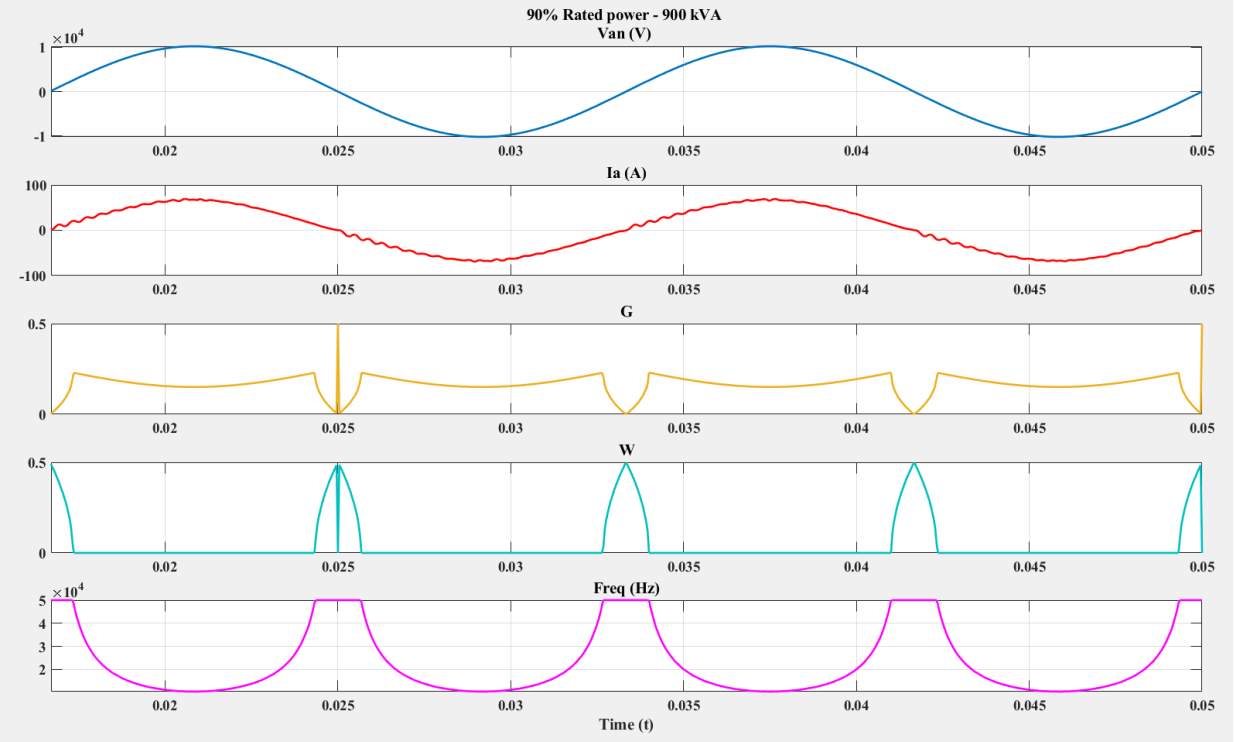


Fig. 4.16 Steady State Waveforms at 900 kVA Load

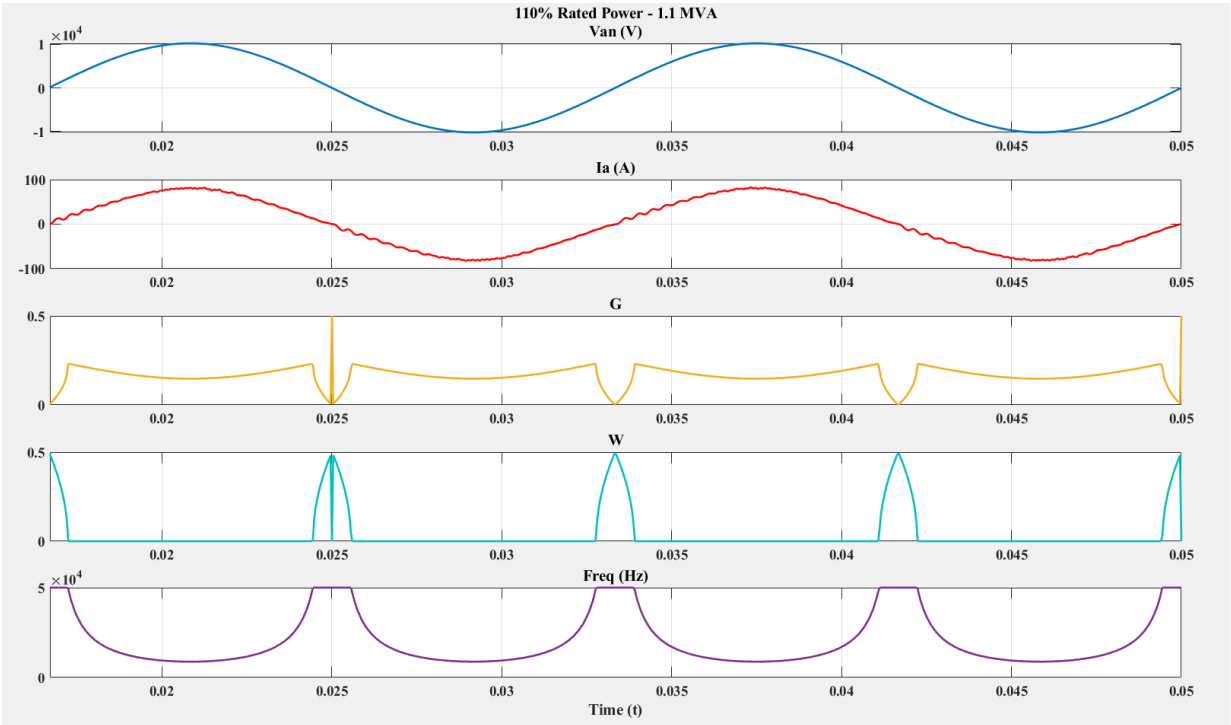


Fig. 4.17 Steady State Waveforms at 1.1 MVA Load

The modulator technique delicately smooths out the current ripple when the voltage zero-crossing occurs. However, apparently, the grid current distortion is worsened when load gets lighter. Generally speaking, the grid current keeps as the sinusoid shape with premium power quality when more than 20% load is connected. The relationship between current THD and the amount of the load power is shown as below,

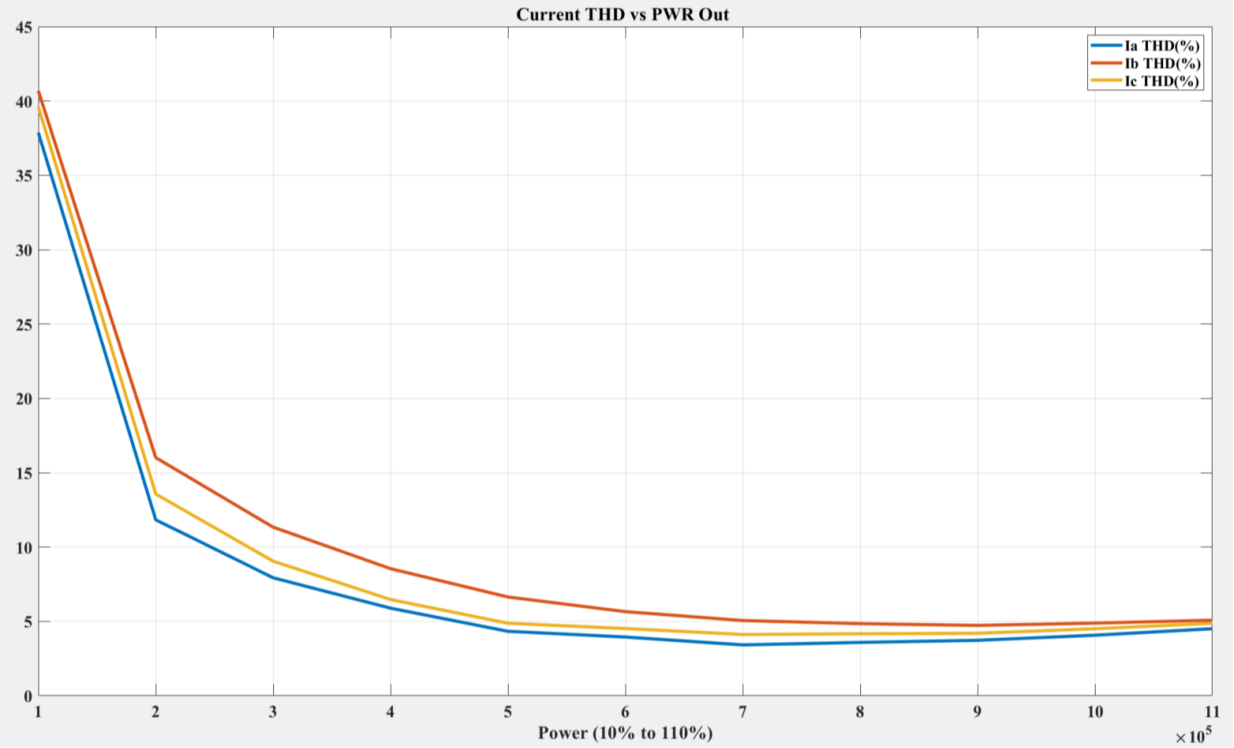


Fig. 4.18 Grid Current THD VS Power Output

The modulator technique already proves its flexibility and adaptability by applying different loads. It is time to close the DC voltage feedback loop and complete the control scheme design. Based on a fully loaded system, 1 MVA, the following study is to validate the system functionalities.

The three-phase grid inputs, common DC bus output, transformer voltage and current are used to demonstrate the overall system performance. Given these are two modulation types, SPS and EPS, the ZVS feature needs to be validated under both conditions. The most attractive benefits brought by ZVS, which is the less switching loss and higher system power density, can be achieved all the time.

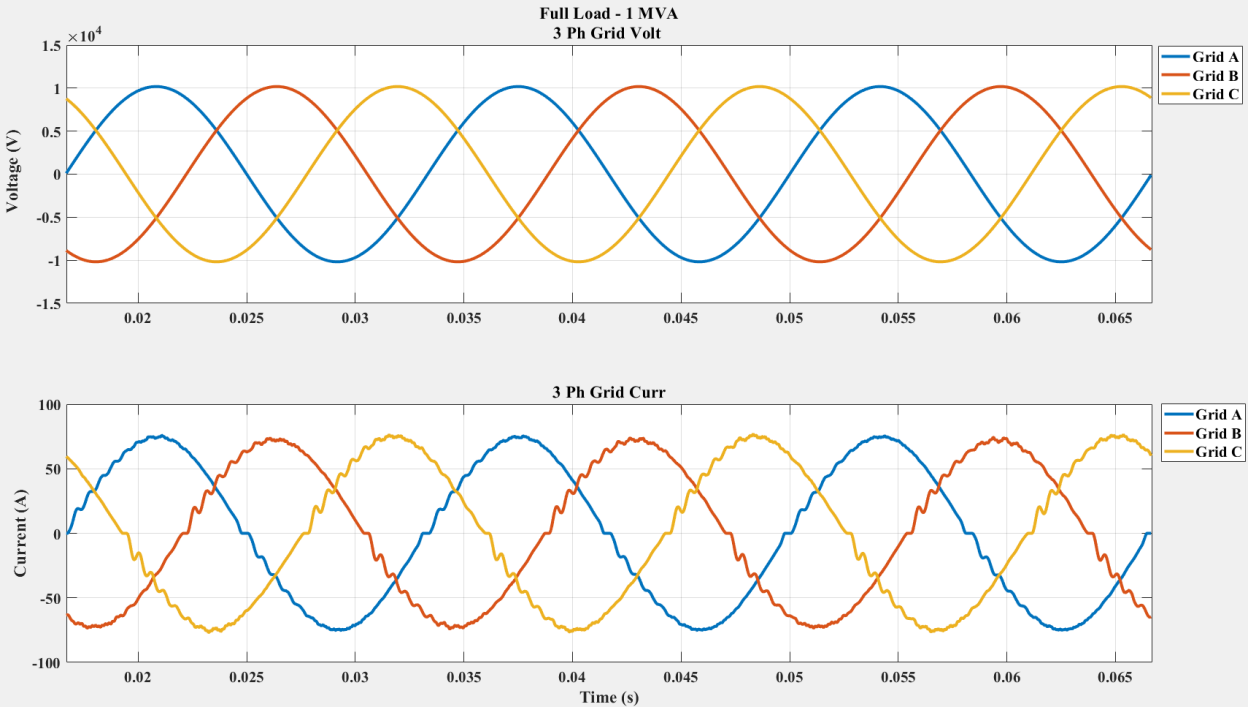


Fig. 4.19 Three-Phase Grid Volt & Curr at 1 MVA Load

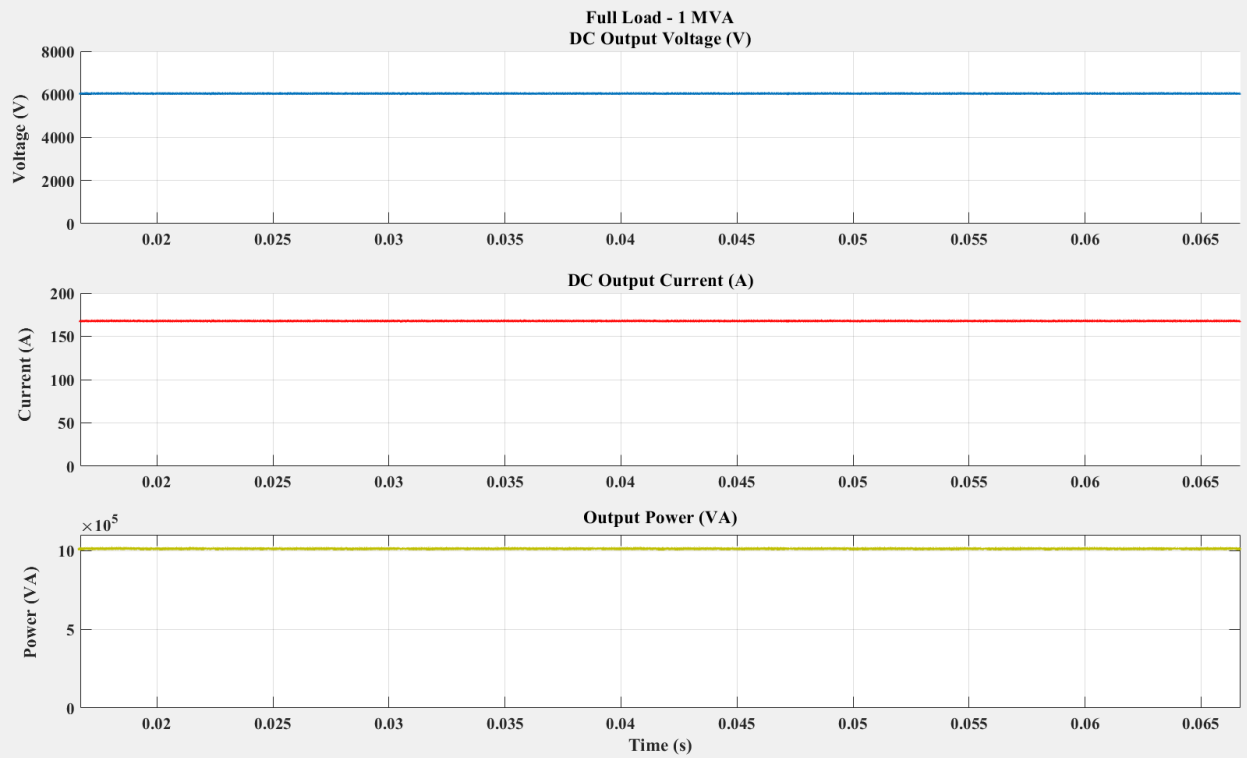


Fig. 4.20 DC Output Voltage, Current, Power

Fig. 4.21 to fig. 4.24 are of the transformer's waveforms. The primary, secondary winding voltages and the leakage current are selected to demonstrate the system behaviors in both SPS and EPS modes. Besides, the transformer current has the significant value since it is directly present the total amount of the power flow. The main reason for the mixed SPS and EPS strategy is to reduce the RMS value of the transformer current at the same power rating.

Fig. 4.25 and fig. 4.26 present the voltage and current of two MOSFETs; i.e. P1 (primary side device) and S1 (secondary side device). ZVS turn-on checking points are highlighted in purple and achieved under both SPS and EPS operational circumstances.

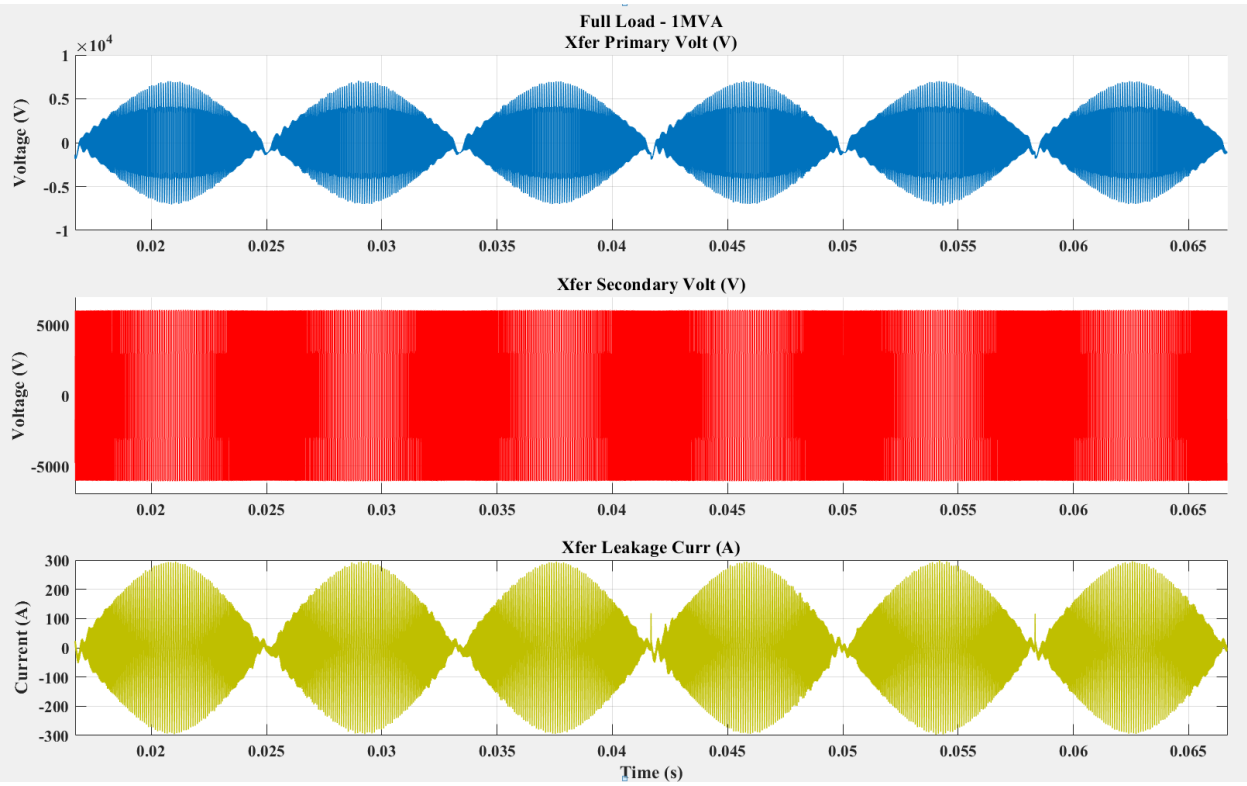


Fig. 4.21 Transformer Voltage and Current

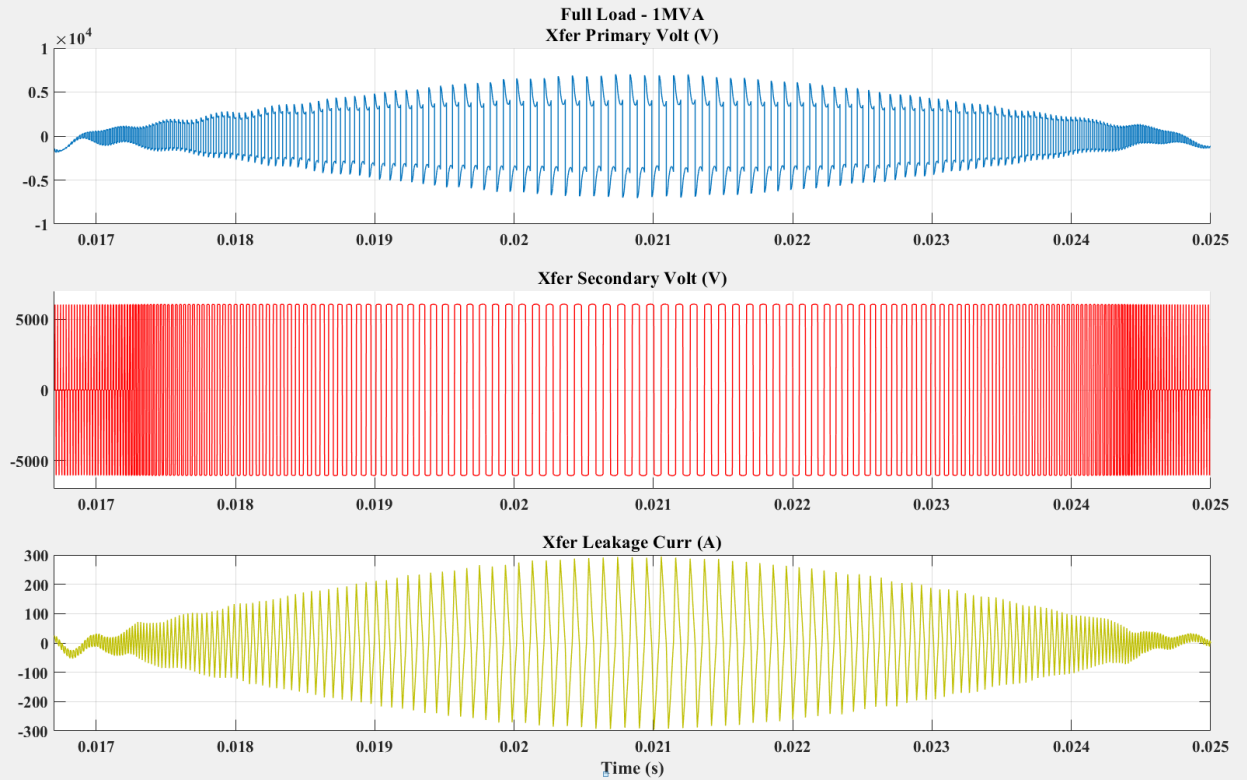


Fig. 4.22 Transformer Voltage and Current (Half Line Cycle)

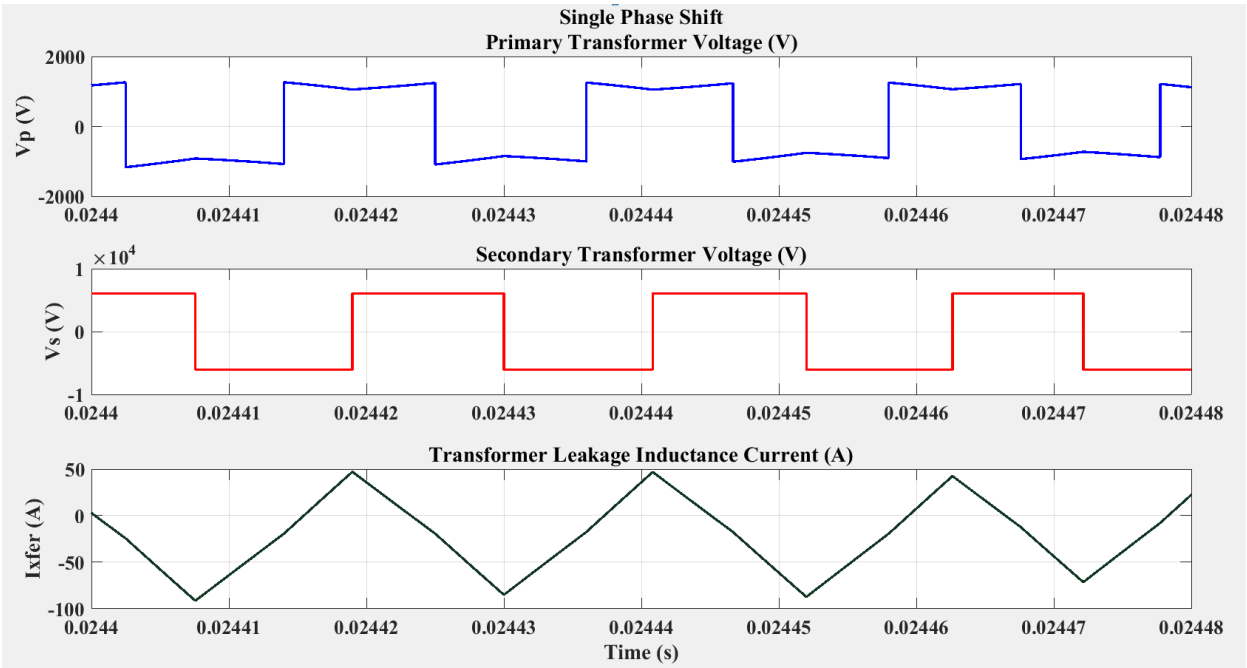


Fig. 4.23 Transformer Waveforms in SPS Mode

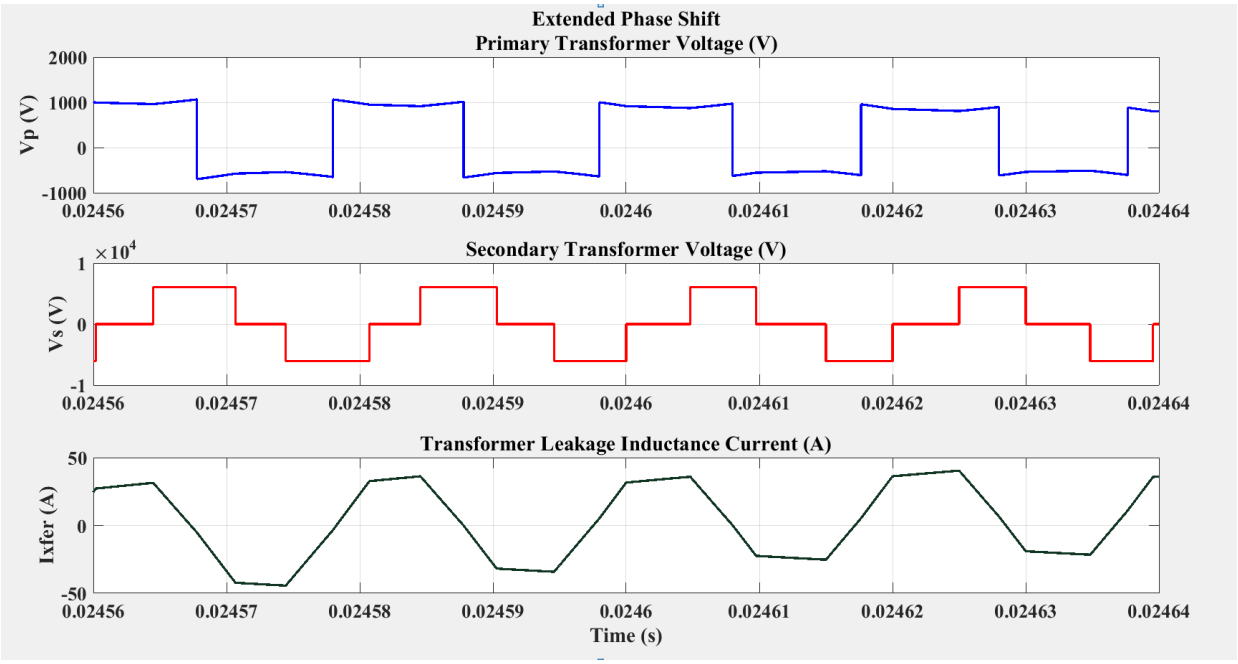


Fig. 4.24 Transformer Waveforms in EPS Mode

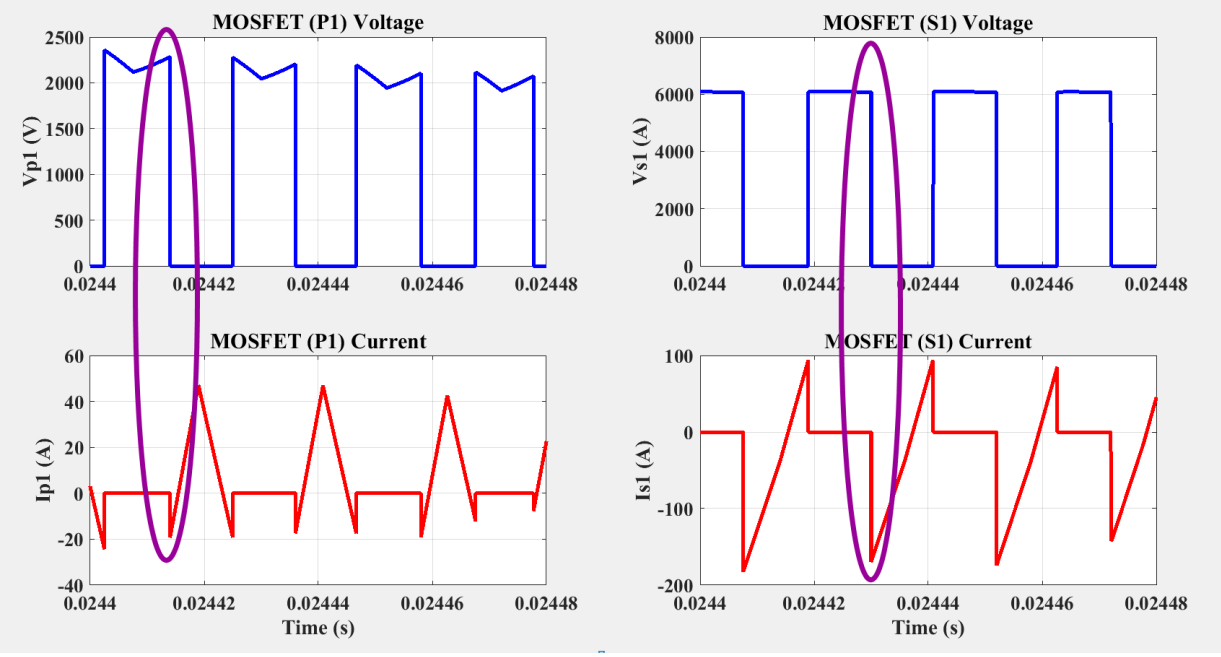


Fig. 4.25 ZVS Turn-on Checking of Primary Side MOSFET (P1) and Secondary Side MOSFET (S1) in SPS Mode

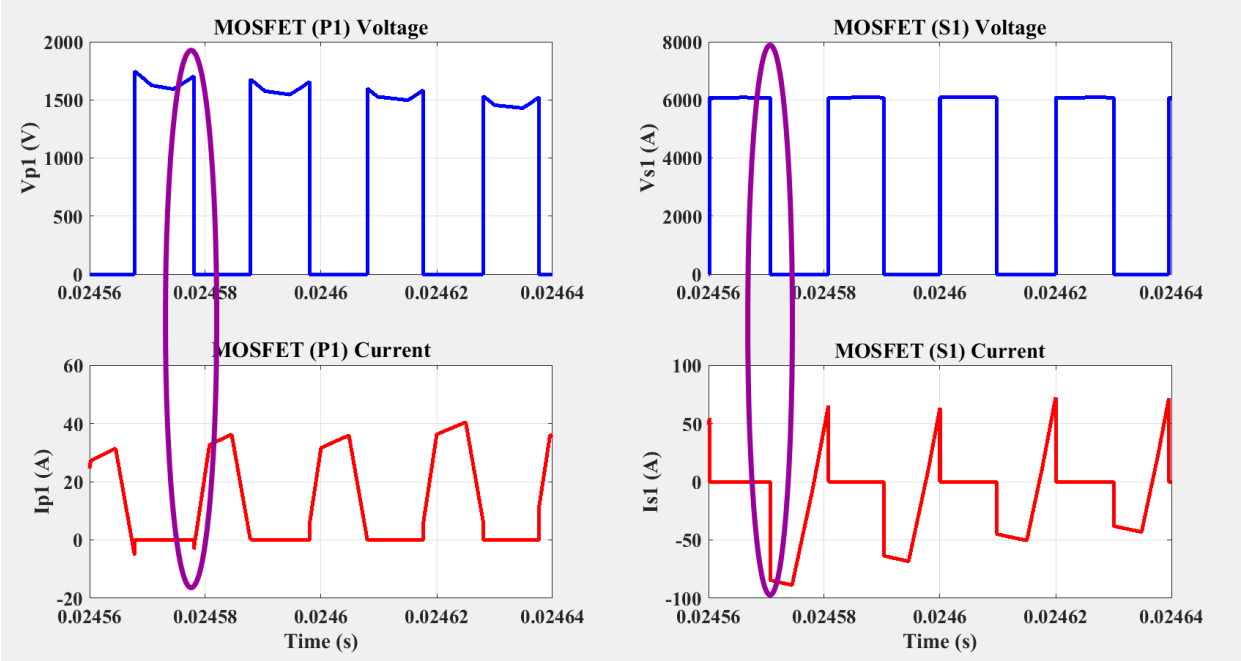


Fig. 4.26 ZVS Turn-on Checking of Primary Side MOSFET (P1) and Secondary Side MOSFET (S1) in EPS Mode

Furthermore, the system has the self-tuned capability inherited. In another word, the modulator is smart enough to change its status according to the grid voltage input and motor loading condition in real-time. Fig. 4.27 – fig. 4.29 demonstrates the modulator dynamics given different input voltage. To be specific, with different input voltage, the utilization percentage of either SPS and EPS is changed. The same story is applied to the different motor loading profile, which is shown from fig. 4.30 to fig. 4.32. The control variables, also the gate firing angles, are recalculated or recalled for every switching cycle. The negative effect is the heavy computing workload.

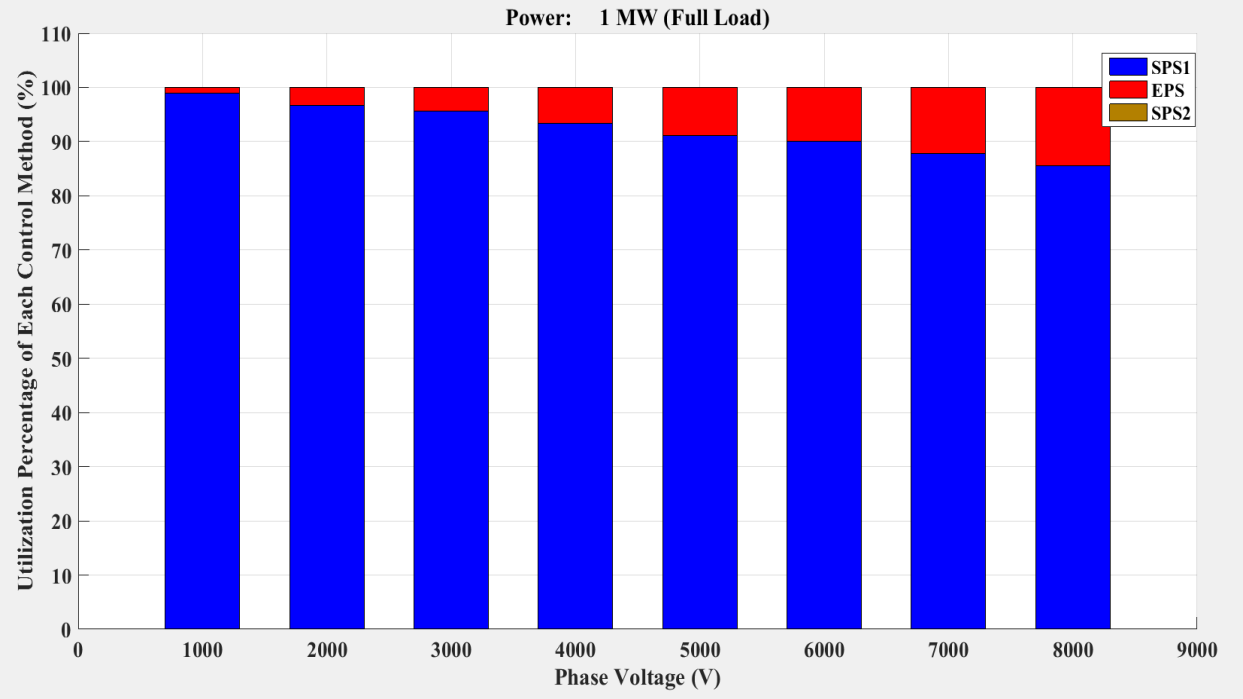


Fig. 4.27 Utilization Percentage of SPS and EPS at Different Grid Voltage (Full Load)

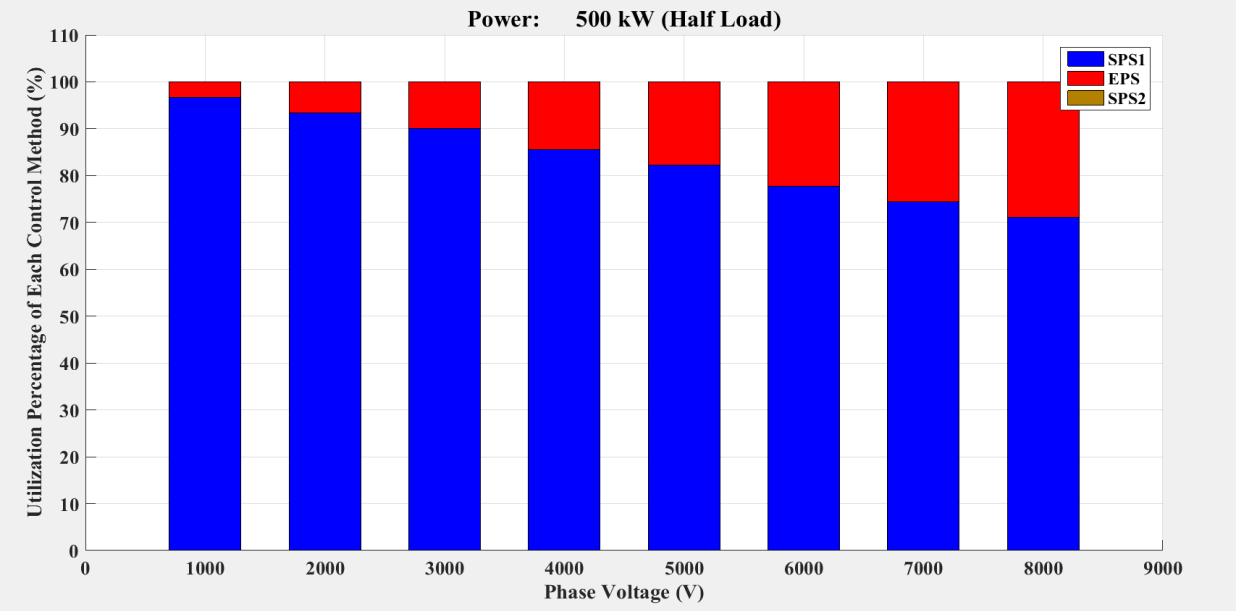


Fig. 4.28 Utilization Percentage of SPS and EPS at Different Grid Voltage (Half Load)

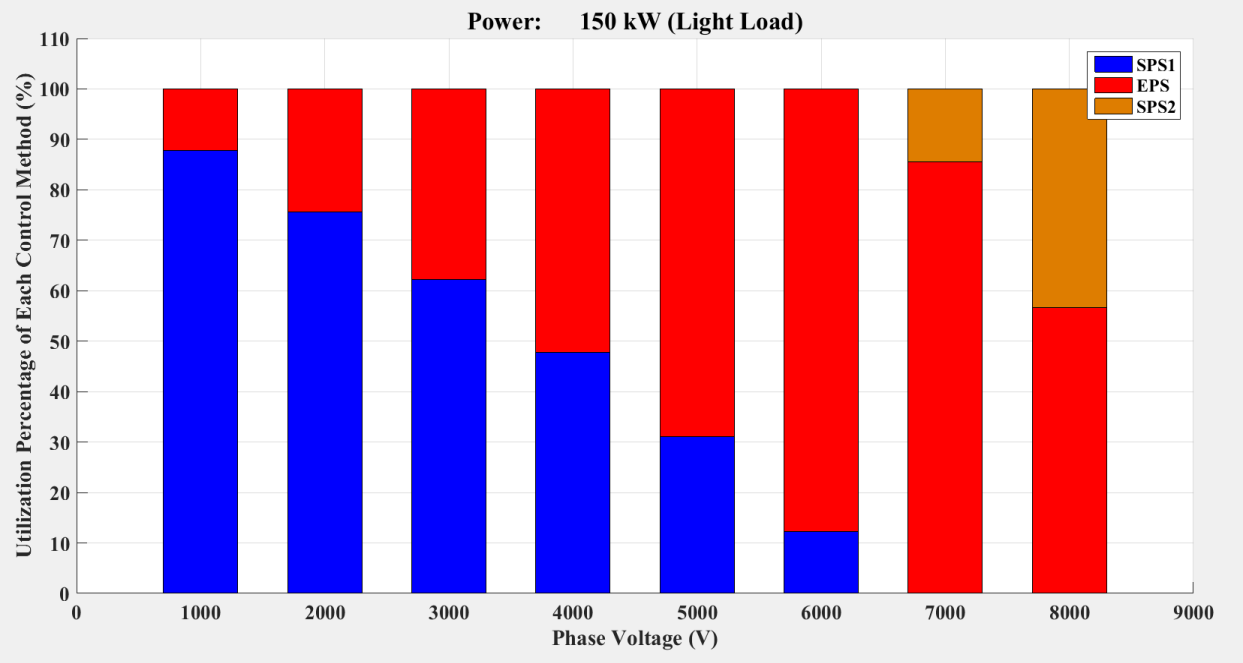


Fig. 4.29 Utilization Percentage of SPS and EPS at Different Grid Voltage (Light Load)

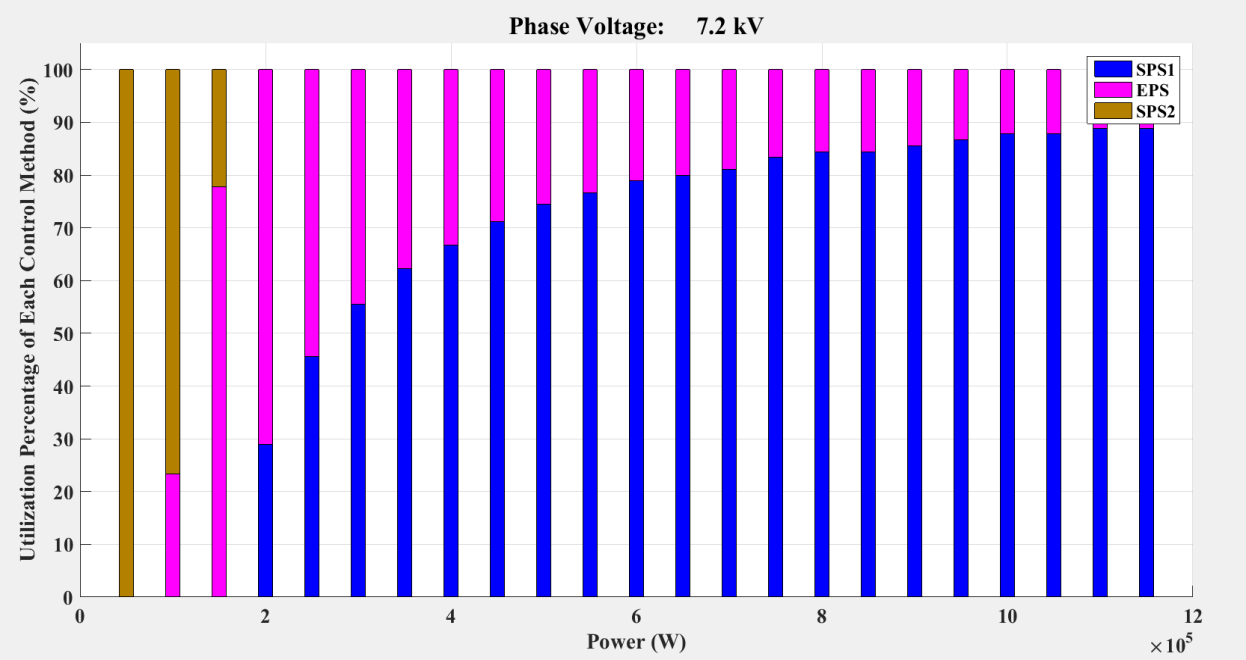


Fig. 4.30 Utilization Percentage of SPS and EPS at Different Loads (7.2 kV Grid Volt)

Fig. 4.31 Utilization Percentage of SPS and EPS at Different Loads (4 kV Grid Volt)

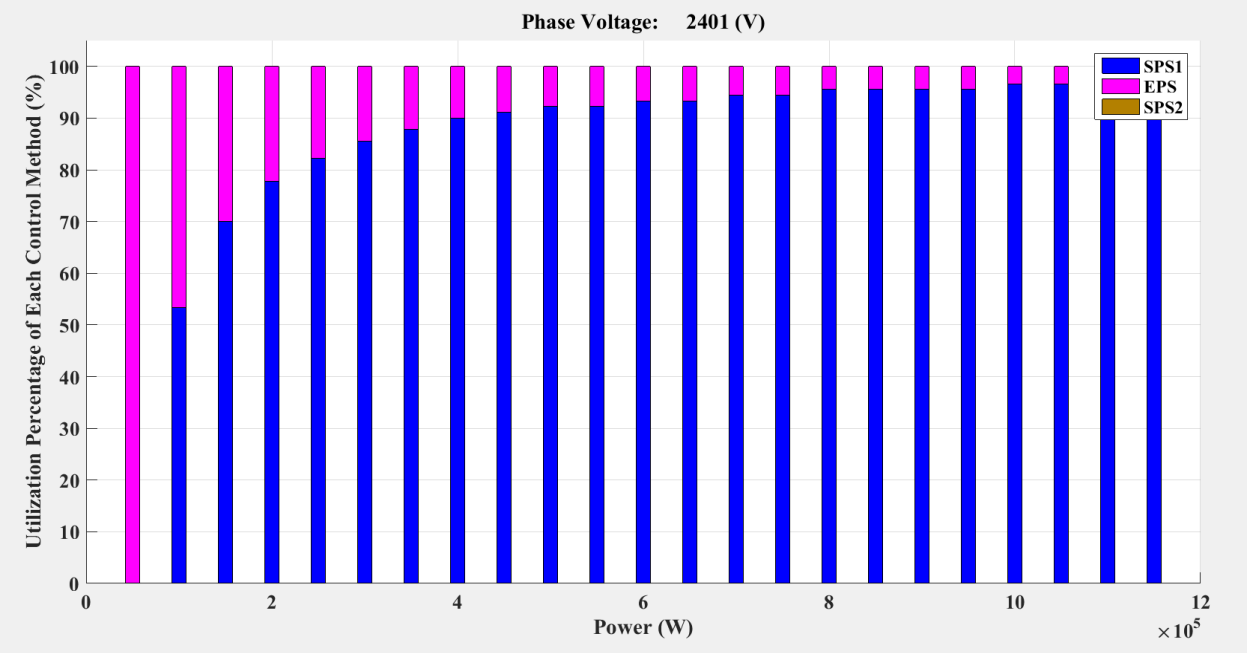


Fig. 4.32 Utilization Percentage of SPS and EPS at Different Loads (2.4 kV Grid Volt)

Before moving to the system transient state study, the relatively high current distortion in the light load condition needs to be mitigated or improved. Chapter 6 will discuss more details and propose an advanced topology exclusively for the ultra-light load case. Then, the system dynamic performance will be fully evaluated by changing the load condition during the normal operation.

4.7 System Fault Ride Through (FRT) and Protection Scheme

Circuitry long-term operating stability is one of the popular topics in the system-level analysis, especially when the engineers are trying to commercialize the proposed circuit as the industrial product. Given the system is running at 24 hours 7 days, it is inevitable for the circuit to witness the power grid fluctuation and voltage sag. It is highly preferred for the circuit can operate at full performance level or maintain the key functions under these four conditions, including under voltage ride through (UVRT), over voltage ride through (OVRT), under frequency ride through (UFRT) and over frequency ride through (OFRT). All these four scenarios are belonging to the grid fault category.

Next, the focus moves to the module itself and the load side. The weakness of the power circuit is always the semiconductor module. The SiC MOSFET is faulted as shorted first given too much current flows through. Then, the device losses the current blocking capability and contains too much energy in a short period of time. Too much energy easily burns out the devices and causes the second failure, which is open device fault. The protection scheme needs to consider both situations and behave properly. Another fault case is in related to the downstream circuits. On the load side, the internal fault in the downstream circuits are equal to either open or short faults on the output of the DAB rectifier. The DAB rectifier may not be informed by the operating condition of the downstream circuits. It should be able to detect the fault by itself and response properly. Without redundancy, it is impractical to keep the circuit continuing operating under these fault conditions. The research topic is about how to accurately detect the fault, get the system offline quickly and protect the rest of the circuit from damaging.

4.7.1 Grid Fluctuation Immunity Study (Case 1-4)

First thing goes first, the system's immunity to the grid fluctuation will be evaluated under these four abnormal operating conditions. The UVRT, OVRT, UFRT and OFRT are defined as below,

a. Case 1: over voltage ride through (OVRT). Phase A is fed by 150% rated voltage at 60 Hz. For comparison purpose, phase B and C have 100% grid voltage input at 60 Hz.
b. Case 2: under voltage ride through (UVRT). Phase A is fed by 80% rated voltage at 60 Hz. For comparison purpose, phase B and C have 100% grid voltage input at 60 Hz.

c. Case 3: under frequency ride through (UFRT). Phase A is fed by 100% rated voltage, but at 55 Hz. For comparison purpose, phase B and C have 100% grid voltage input at 60 Hz.
d. Case 4: over frequency ride through (OFRT). Phase A is fed by 100% rated voltage, but at 65 Hz. For comparison purpose, phase B and C have 100% grid voltage input at 60 Hz.

In addition, case 0 is defined as the normal operating condition. In the case study, the system starts with the normal operating condition (case 0), then moves to case 1, 2, 3, 4 consequently and goes back to case 0 normal operating mode. It is worth mentioning that the three phases are running at different frequencies in case 3 and 4, which breaks the balancing relationship between phases. For an unbalanced three-phase system, the grid current contains more harmonics when trying to balance the total power transfer between three phases. For the same reason, the DC output has the oscillation and affects the loads at certain level. In another word, the proposed system can still function for the short term under OVRT, UVRT, UFRT and OFRT. However, the current THD index is not compliant to the long-term power system stable operating requirements.

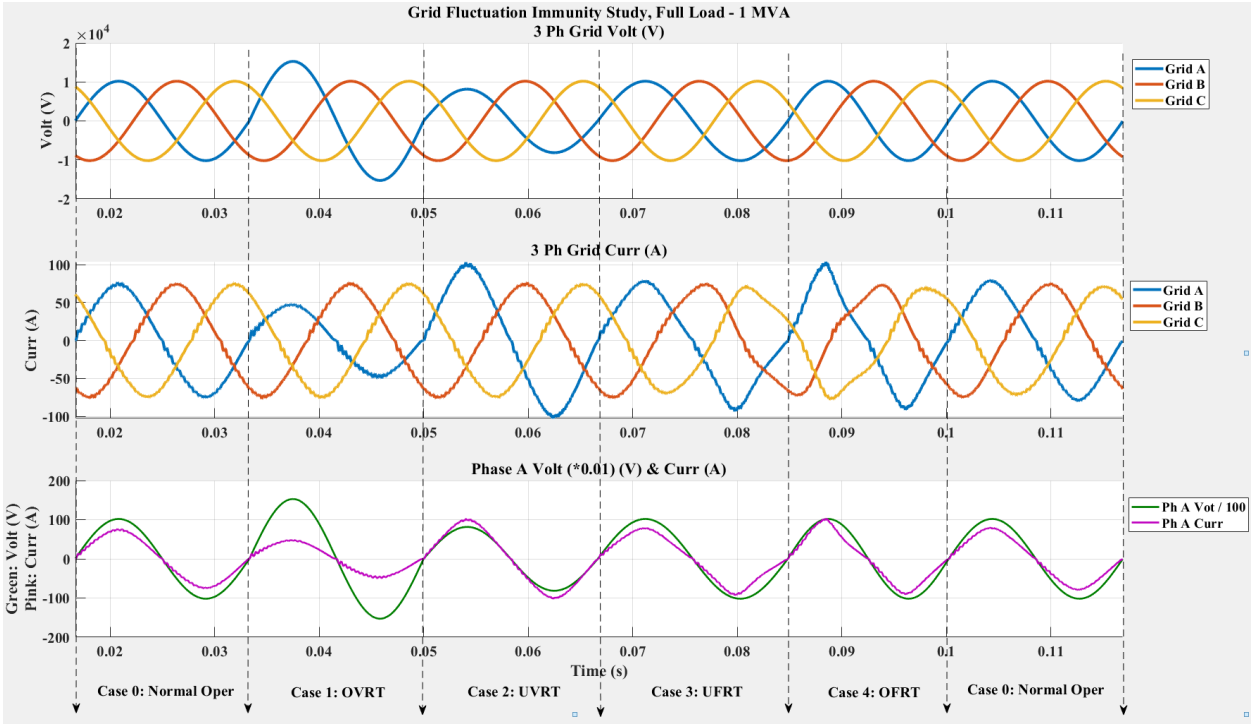


Fig. 4.33 AC Input of Grid Fluctuation Immunity Study, Full Load

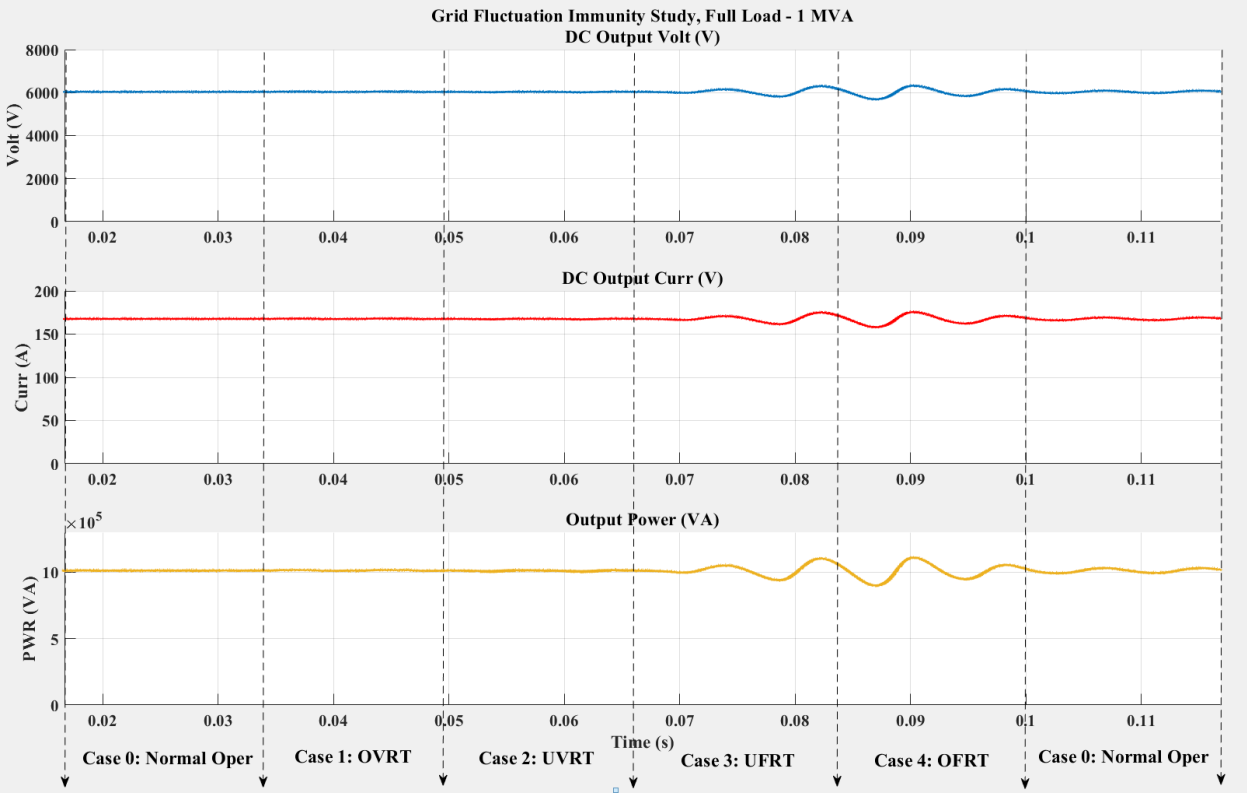


Fig. 4.34 DC Output of Grid Fluctuation Immunity Study, Full Load

Next, the system behaviors under the semiconductor device fault and output fault need to be investigated. All the different system faults are classified as,

a. Case 5: SiC MOSFET device fault as short. Choose P1 module fault in the case study.
b. Case 6: SiC MOSFET device fault as open. Choose P1 module fault in the case study.
c. Case 7: output DC bus fault as short.
d. Case 8: output DC bus fault as open.

4.7.2 Device Fault as Short Study (Case 5)

The device short fault (case 5) is one of the common device faults. The cause is a very high voltage, very fast transient spike (which may be positive or negative polarity). If such a spike gets onto the drain of a MOSFET, it gets coupled through the MOSFETs internal capacitance to the gate. If enough energy gets coupled, the voltage on the gate rises above the maximum allowable level and the MOSFET dies instantaneously. The process takes less than a nanosecond. The initial spike destroys the gate-body insulation, so that the gate is connected to the body. Once that has

happened, the MOSFET explodes in a cloud of flame and black smoke. The explosion faults the device second times and makes it as permanently open, which is fault case 6.

Fig. 4.35 to fig. 4.37 are of the AC input, DC output, device voltage and current when SiC MOSFET P1 is faulted as short.

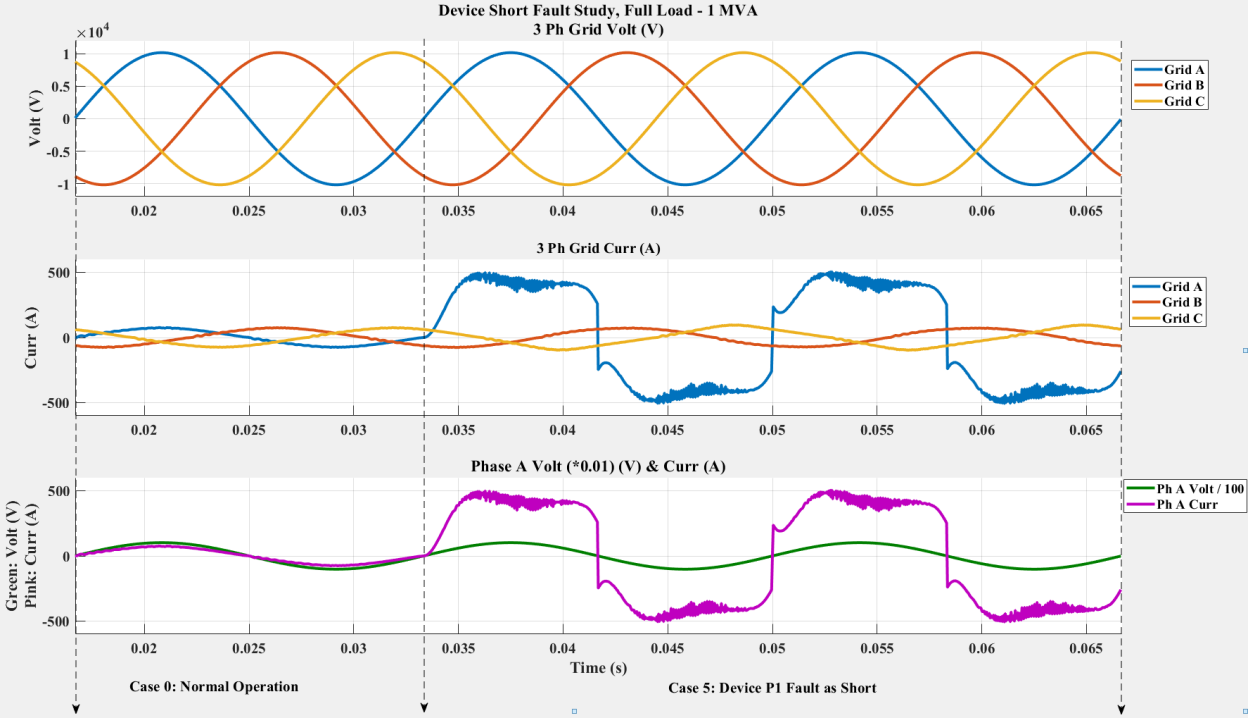


Fig. 4.35 AC Input When Device Fault as Short (No Protection), Full Load

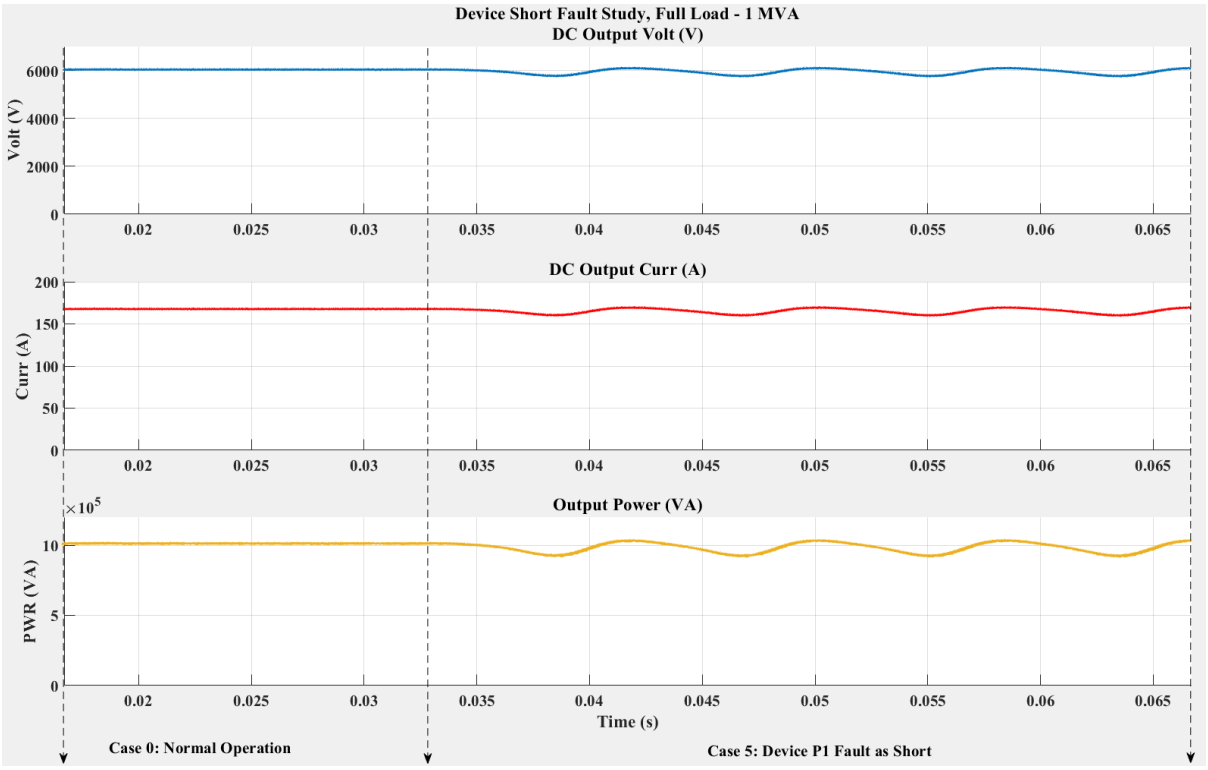


Fig. 4.36 DC Output When Device Fault as Short (No Protection), Full Load

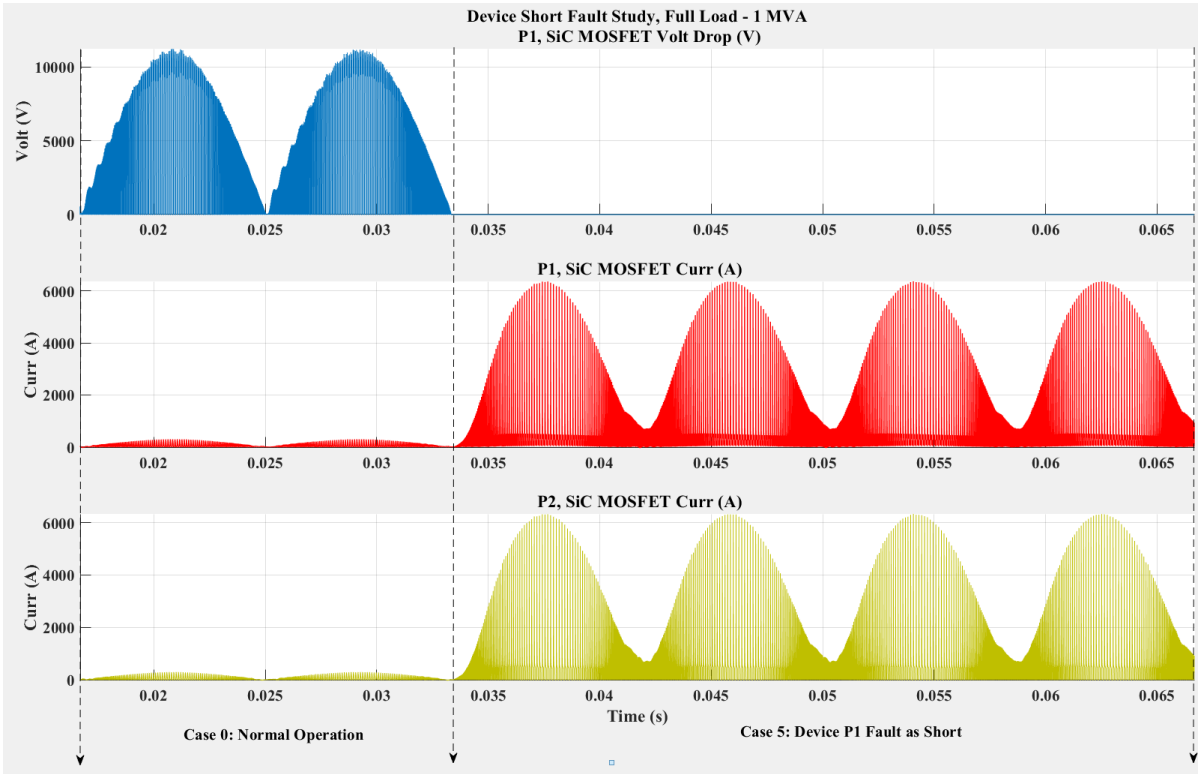


Fig. 4.37 Device Volt & Curr When Device Fault as Short (No Protection), Full Load

Per fig. 4.38, the faulted P1 device creates a short circuit path including the high DC bus (Ch) when P2 device is closed. The worst-case scenario is to have a huge short circuit current flowing through the high DC bus and two SiC MOSFETs. In the meanwhile, the grid current has the overshoot and gets heavily distorted. It is obvious that the system needs to be shut down to prevent P2 device from overcurrent damage.

The protection strategy is the classic desaturation function. Desaturation function is used to detect power transistor short-circuit scenario and takes protective measures to prevent power transistors from EOS damage. By adding the desaturation logic, once the protection logic detects the overcurrent existence, all the gating firing are removed immediately. As a result, the system is offline until the device being repaired. The system response is graphically presented from fig. 4.39 to fig. 4.41.

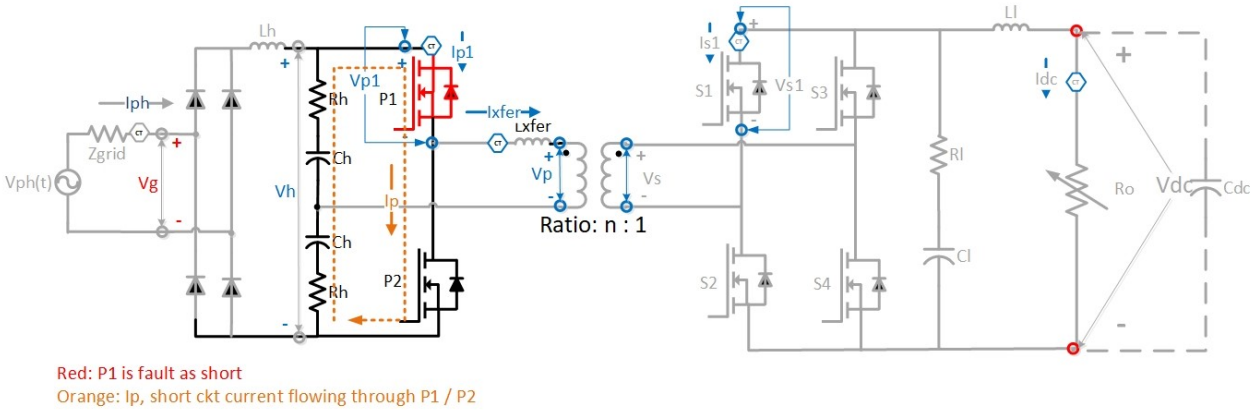


Fig. 4.38 Short Ckt Current Path When Device Fault as Short

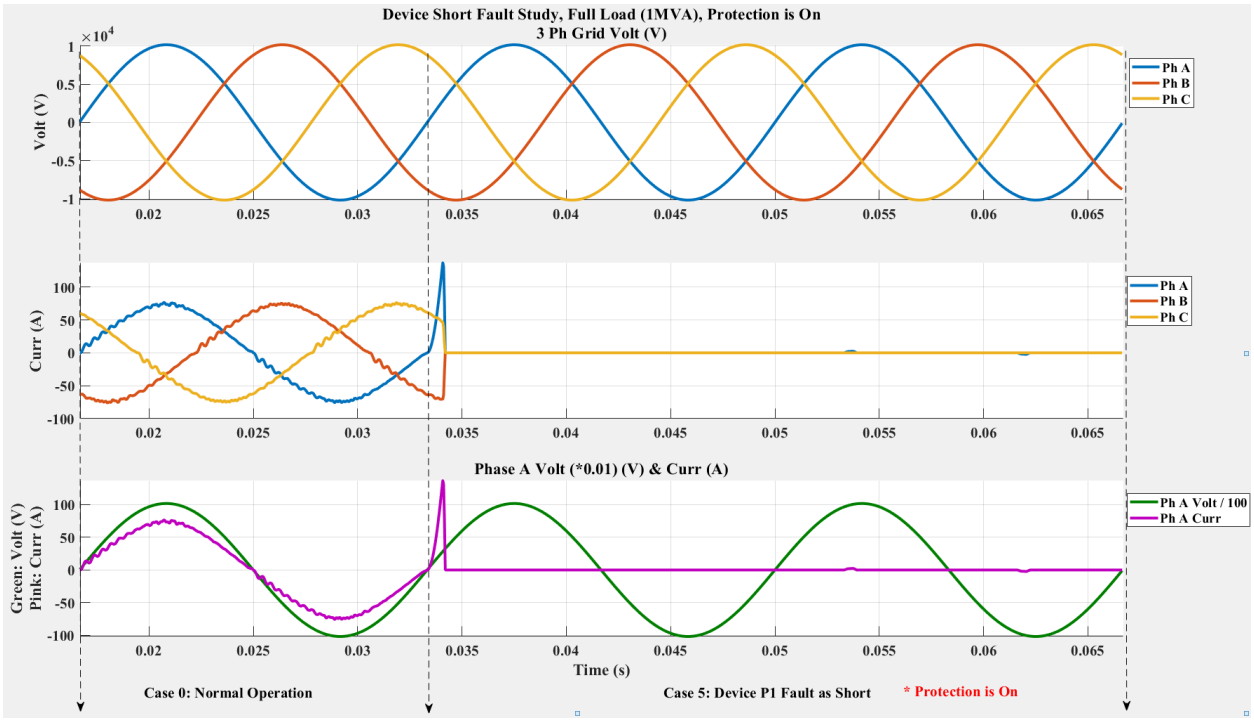


Fig. 4.39 AC Input When Device Fault as Short (with Protection on), Full Load

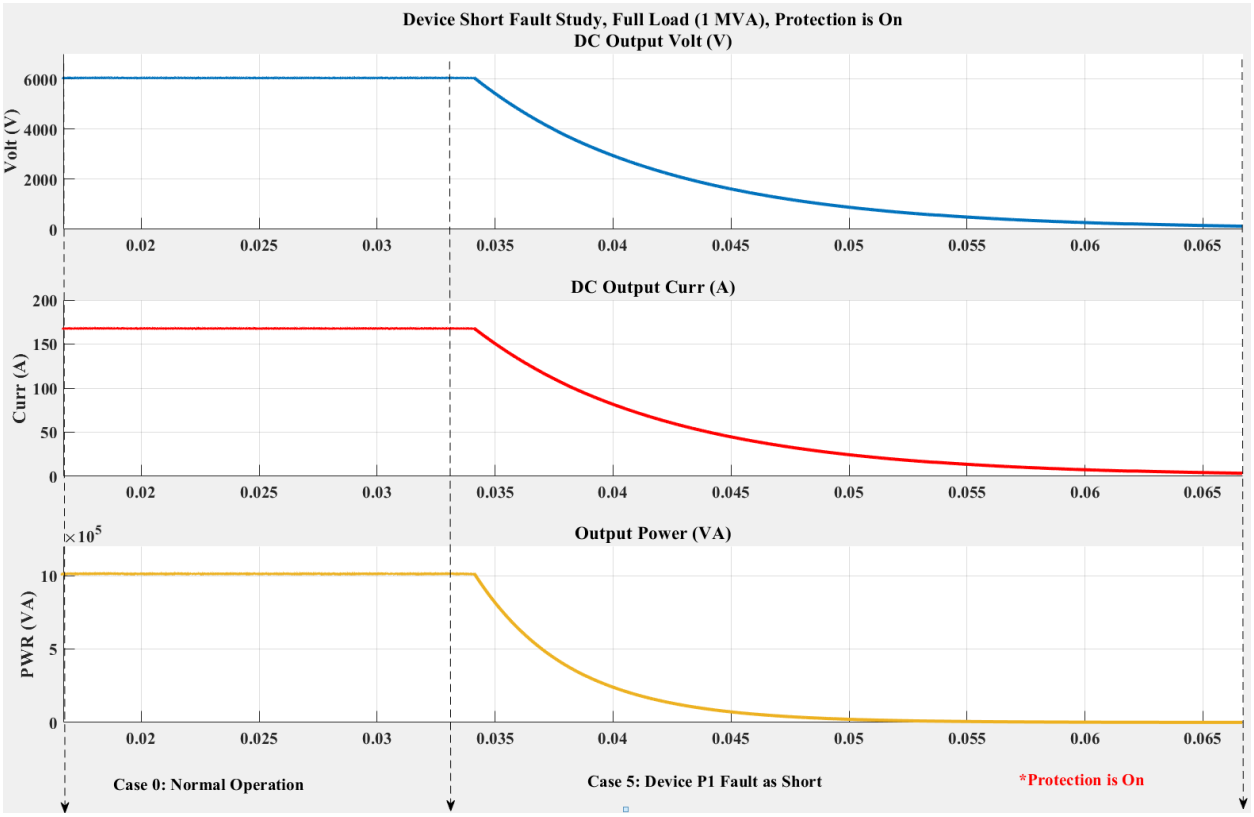


Fig. 4.40 DC Output When Device Fault as Short (with Protection on), Full Load

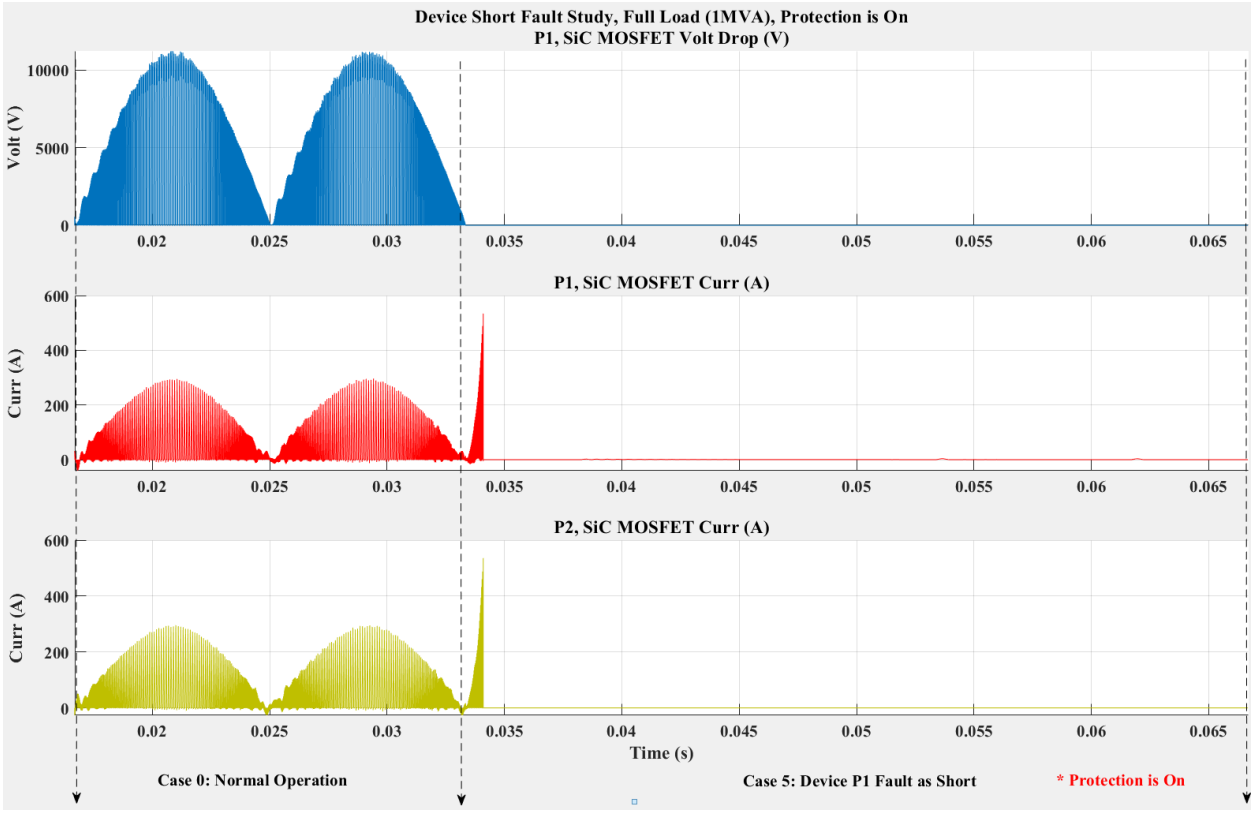


Fig. 4.41 Device Volt & Curr When Device Fault as Short (with Protection on), Full Load

Fig. 4.39 to fig. 4.41 demonstrate the desaturation protection function when fault case 5 occurs. The P1 device short fault creates a possibility to short the high DC bus when P2 MOSFET is closed. In that case, the huge short current flows through Rh(pos), Ch(pos), Rh(neg), Ch(neg), P1 and P2. The desaturation protection detects the over current and inhibits all the gate firing signals, which limits the short current flowing through the MOSFETs effectively. Also, the response time to shut down the defective circuit is less than 2 us.

4.7.3 Device Fault as Open Study (Case 6)

Similar to case 5, case 6 is another classic device failure. In some cases, it occurs because the protection scheme fails to detect the device short fault. The shorted device losses the capability of blocking the short-circuit current. Given a short period of time, the short-circuit current generates the huge thermal energy inside of the device and then causes the thermal failure as next step. The explosion is a typical way to distribute the stored thermal energy. After this catastrophic failure, the collector and emitter are permanently open and the device losses the gating control. Without

the protection, the AC input, DC output and device waveforms are shown from fig. 4.42 to fig. 4.45.

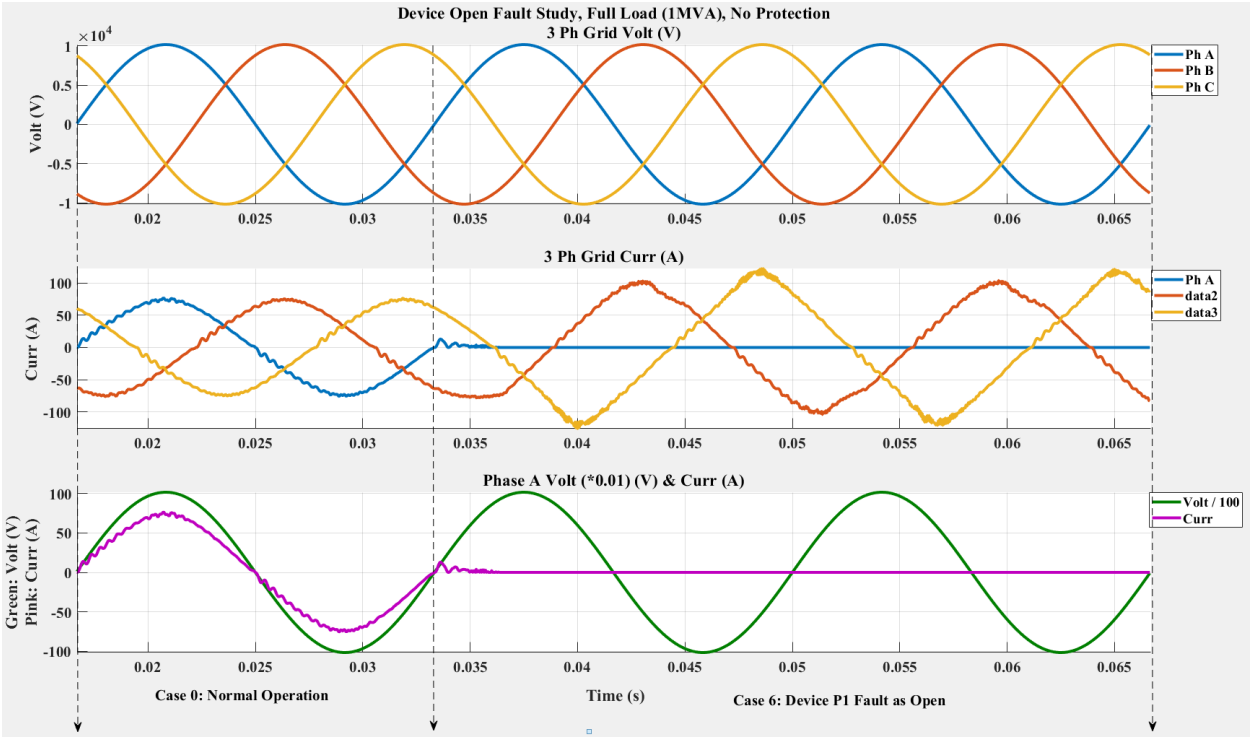


Fig. 4.42 AC Input When Device Fault as Open (No Protection), Full Load

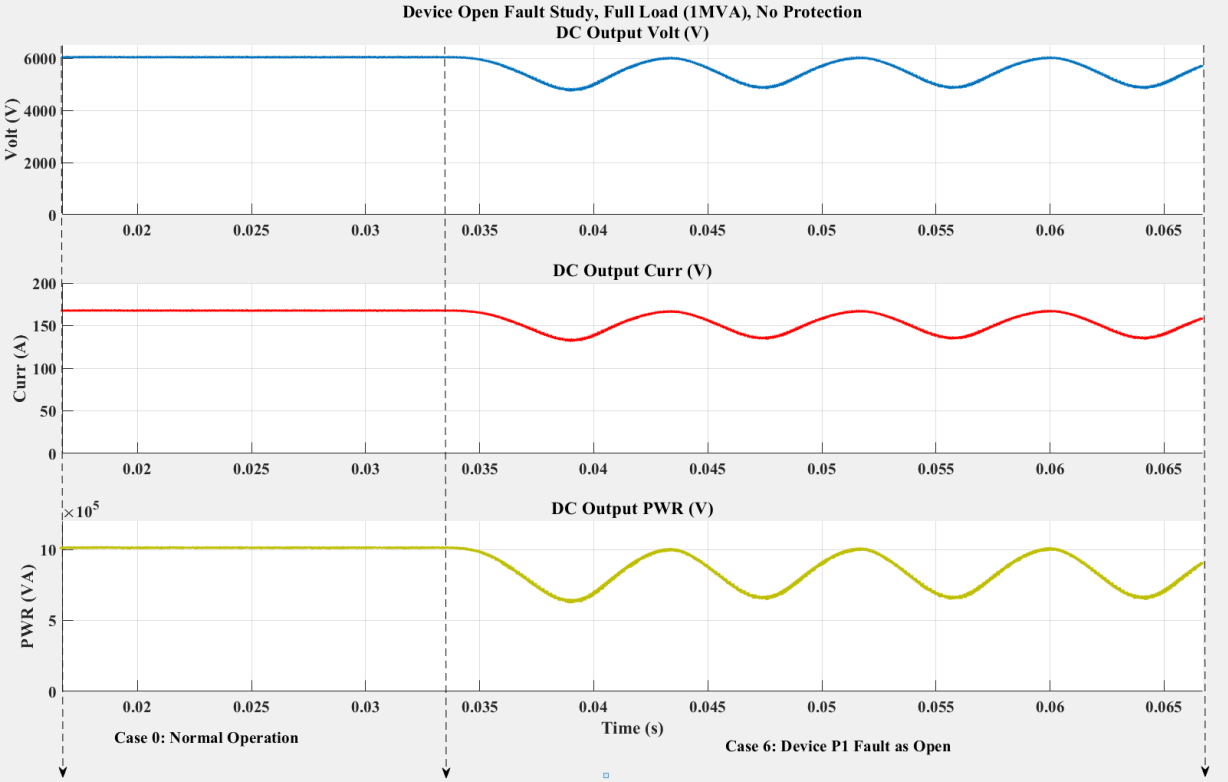


Fig. 4.43 DC Output When Device Fault as Open (No Protection), Full Load

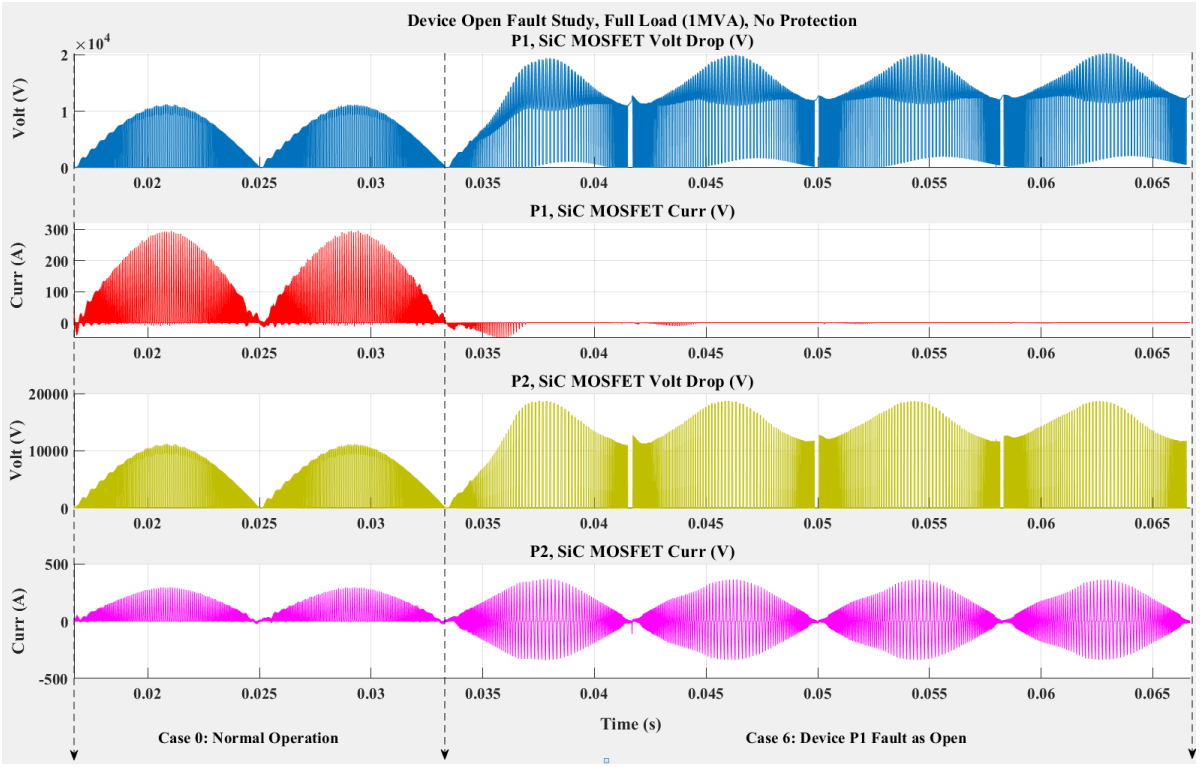


Fig. 4.44 Device Volt & Curr When Device Fault as Open (No Protection), Full Load

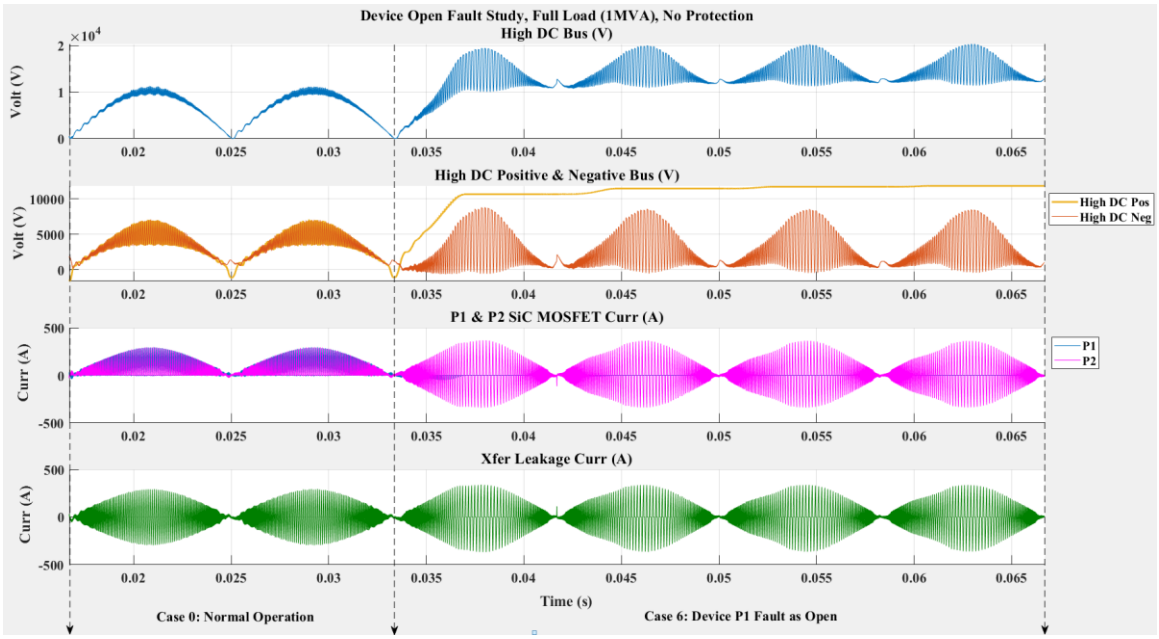


Fig. 4.45 High DC Bus and Resonant Curr When Device Fault as Open (No Protection), Full Load

Once the device open fault happens, the overall system operation changes dramatically. The root of cause is the loss of the half high DC bus. The voltage and energy stored in the Rh(positive) and Ch(positive) cannot be transferred to the load any more. So, the positive high DC bus is charged up to the same level of the grid voltage. The total high DC bus is clamped by the front-end circuit and line reactor Lh. In this case, the negative DC bus is clamped and has very limited power transfer capability. As a result, the RMS value of the resonant current is almost zero. The phase A losses the power transfer capability and its 33.33% power transfer task are assigned to phase B and C. The unbalance current waveforms can be witnessed on the grid input.

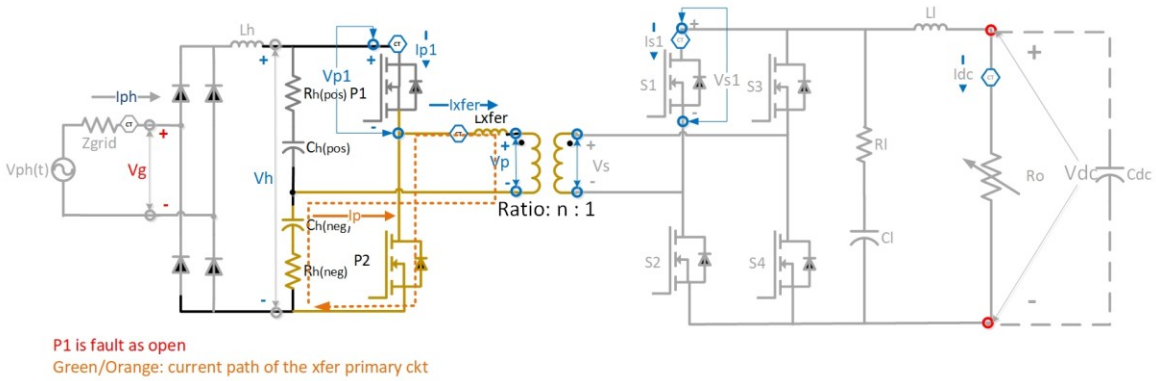


Fig. 4.46 Fault Ckt Current Path When Device Fault as Open

The protection for the device open fault has two options. The first choice is to detect the voltage unbalance between positive DC bus and negative DC bus. The DC bus unbalance means the current flowing through P1 and P2 is different over a line cycle, which indicates the device fault. The second option is to add the MOSFET over-voltage detection to the gate driver. The unbalanced DC bus causes the abnormal voltage stress shown on the device. The second option is selected because it locates the faulted device directly. The device over-voltage protection scheme is developed and added to the model. Fig. 4.47 to fig. 4.50 demonstrate the system self-protection dynamic response when device P1 is faulted as open.

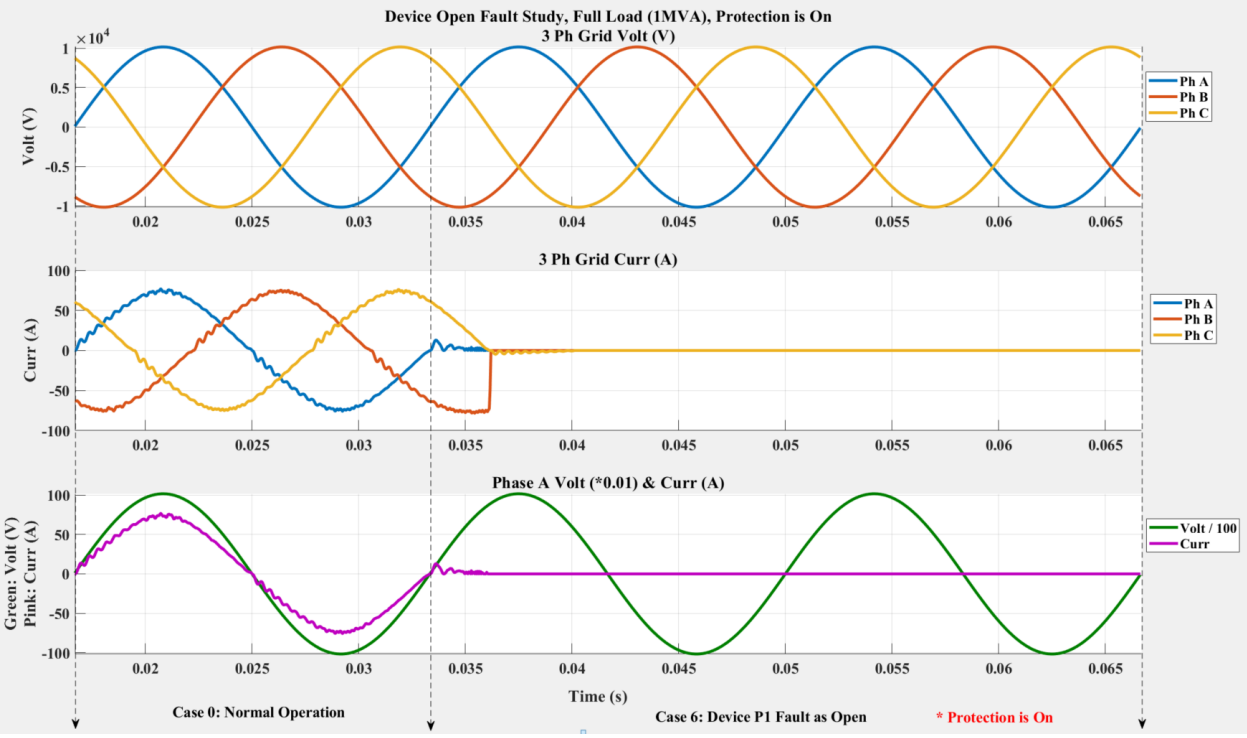


Fig. 4.47 AC Input When Device Fault as Short (With Protection On), Full Load

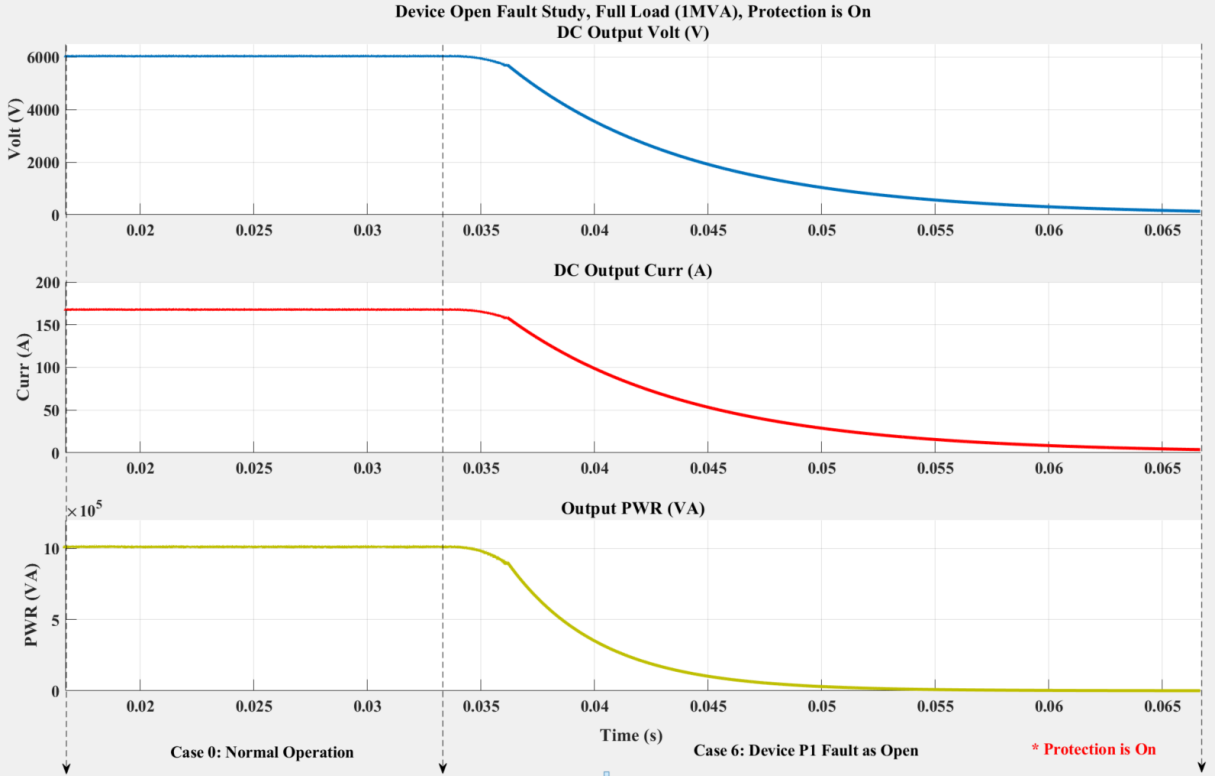


Fig. 4.48 DC Output When Device Fault as Short (With Protection On), Full Load

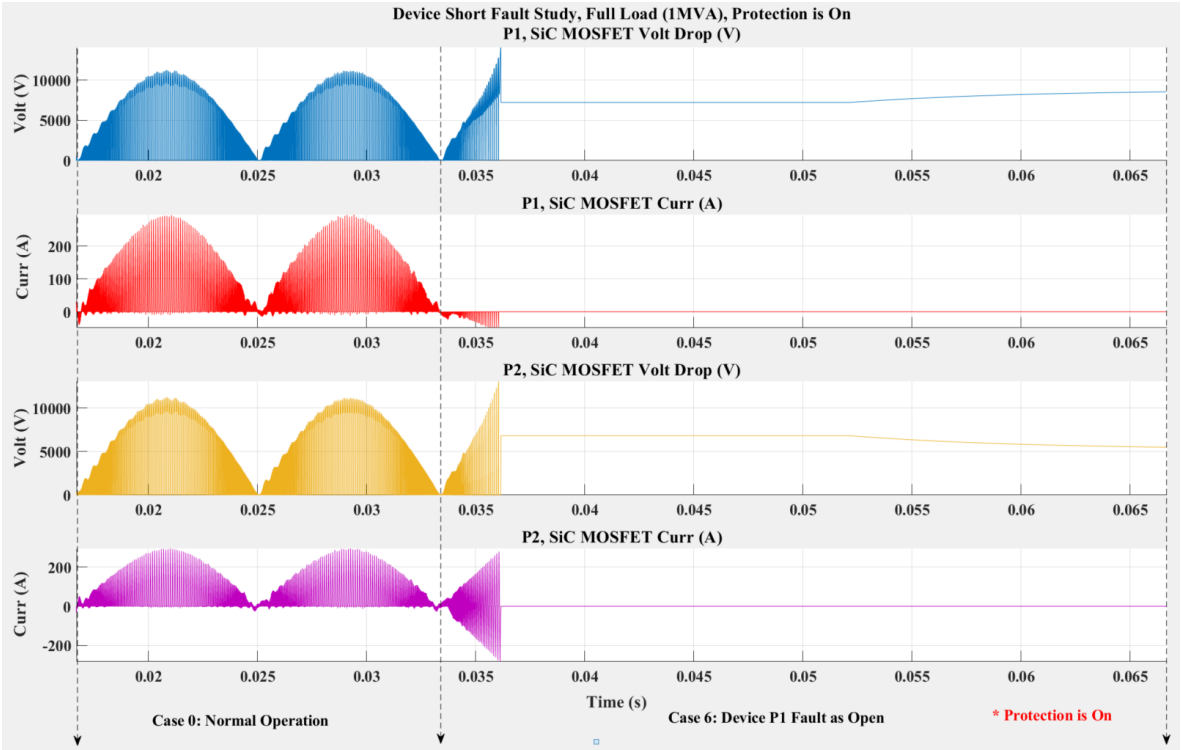


Fig. 4.49 Device Volt & Curr When Device Fault as Open (With Protection On), Full Load

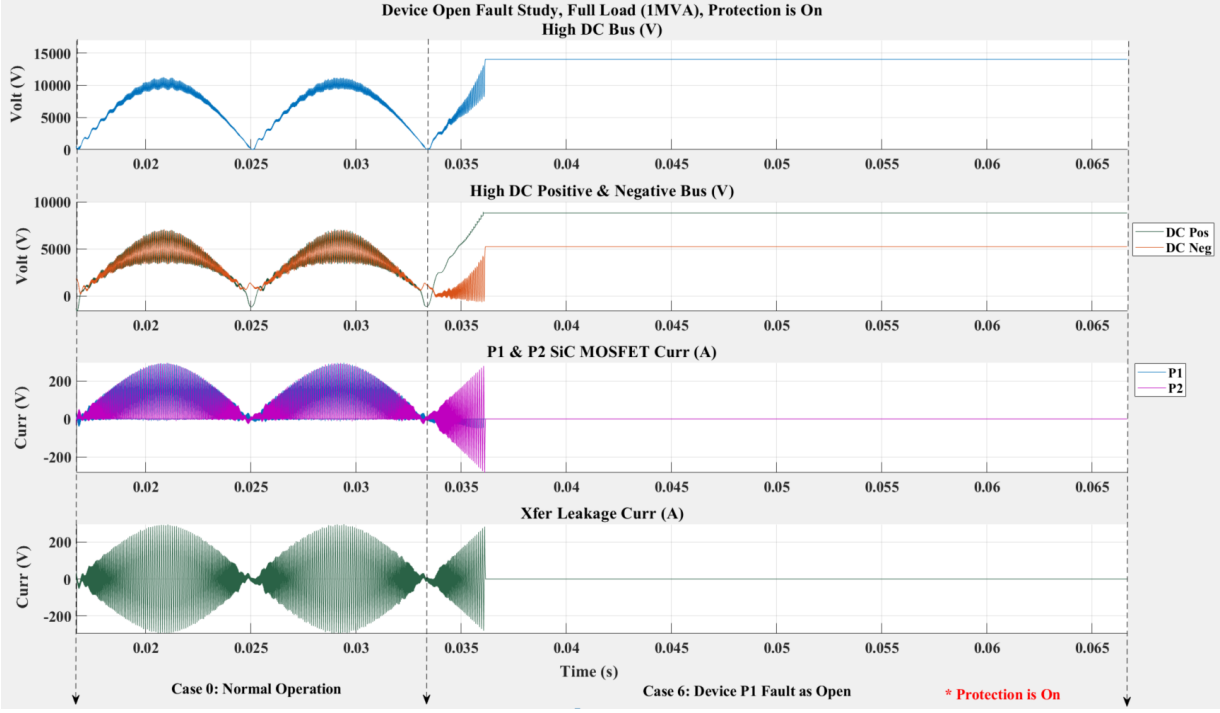


Fig. 4.50 High DC Bus and Resonant Curr When Device Fault as Open (With Protection On), Full Load

Fig. 4.47 to fig. 4.50 demonstrate the functionality and validity of the device over-voltage protection. The protection hardware is a voltage divider circuit which monitors the voltage between the collector and emitter. The protection software is to sample and monitor the voltage and trip the system once the over-voltage occurs. The benefits are to detect the P1 open fault accurately and remove a three-phase unbalanced system from the power grid quickly.

4.7.4 Output DC Bus Fault as Short Study (Case 7)

Next, it is time to investigate the system performance when the fault is on the circuit output, namely downstream circuit failure. Looking into the load, the abnormal operations behave as either short or open fault. Case 7 is proposed to cover the output DC bus short fault. The inherited voltage feedback loop clamps the power command at 120% rated value, which kindly limits the current flowing through the circuit. As a result, the DC output voltage collapses to a small value. The DC output is sampled and monitored all the time for the voltage regulation purpose. The protection is to shut down the system if the DC output drops more than 20% of its rated value. Fig. 4.51 to 4.54 demonstrate the post-fault system response.

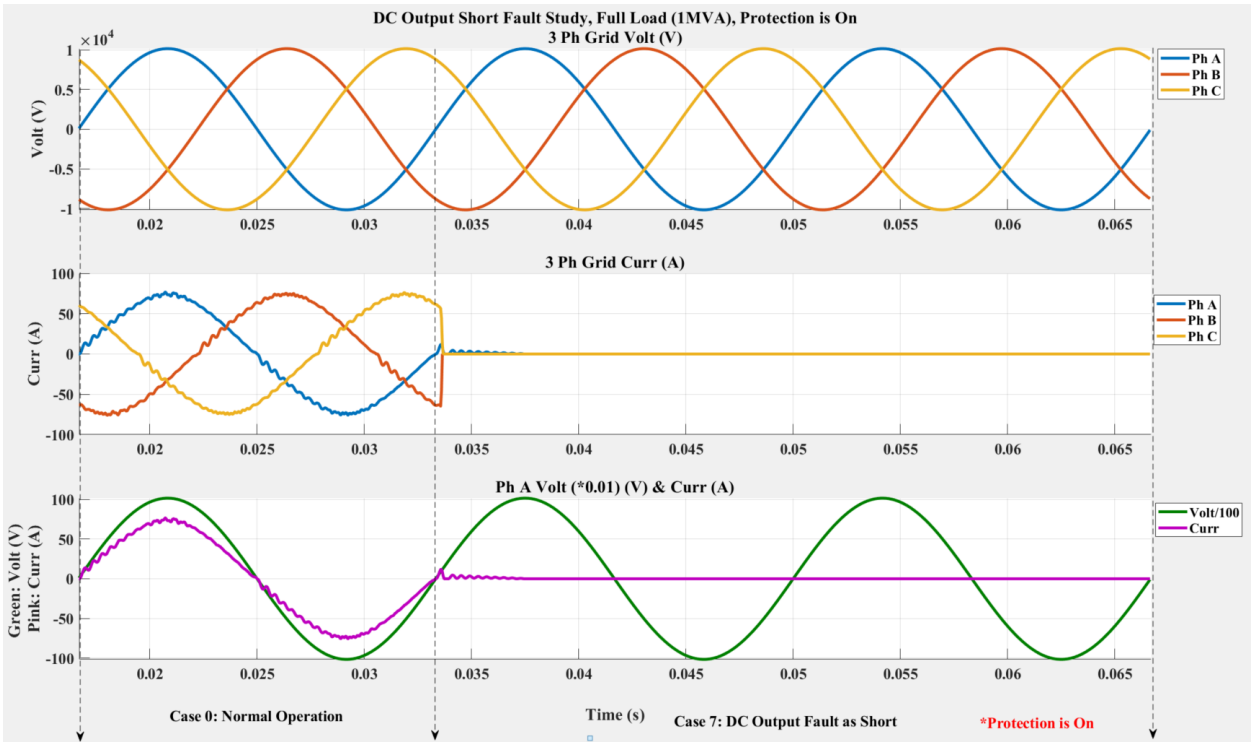


Fig. 4.51 AC Input When DC Output Fault as Short (With Protection On), Full Load

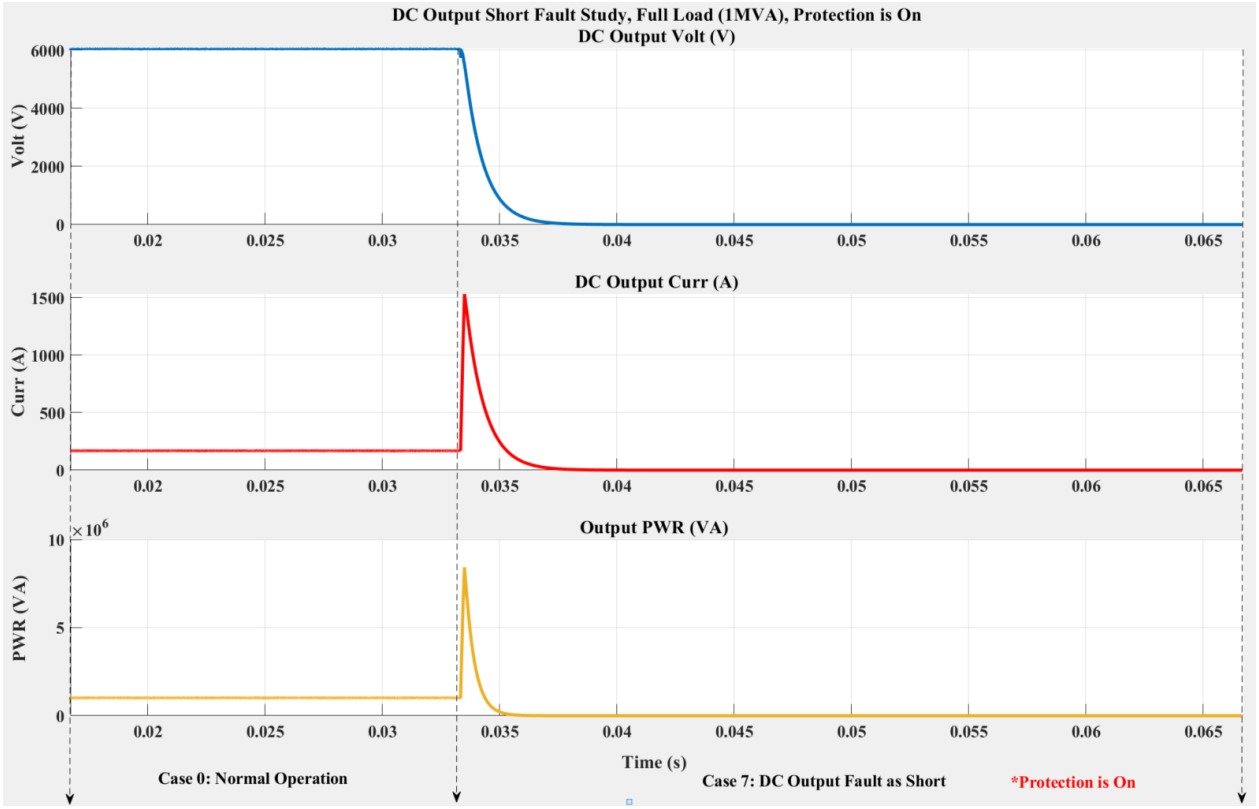


Fig. 4.52 DC Output When DC Output Fault as Short (With Protection On), Full Load

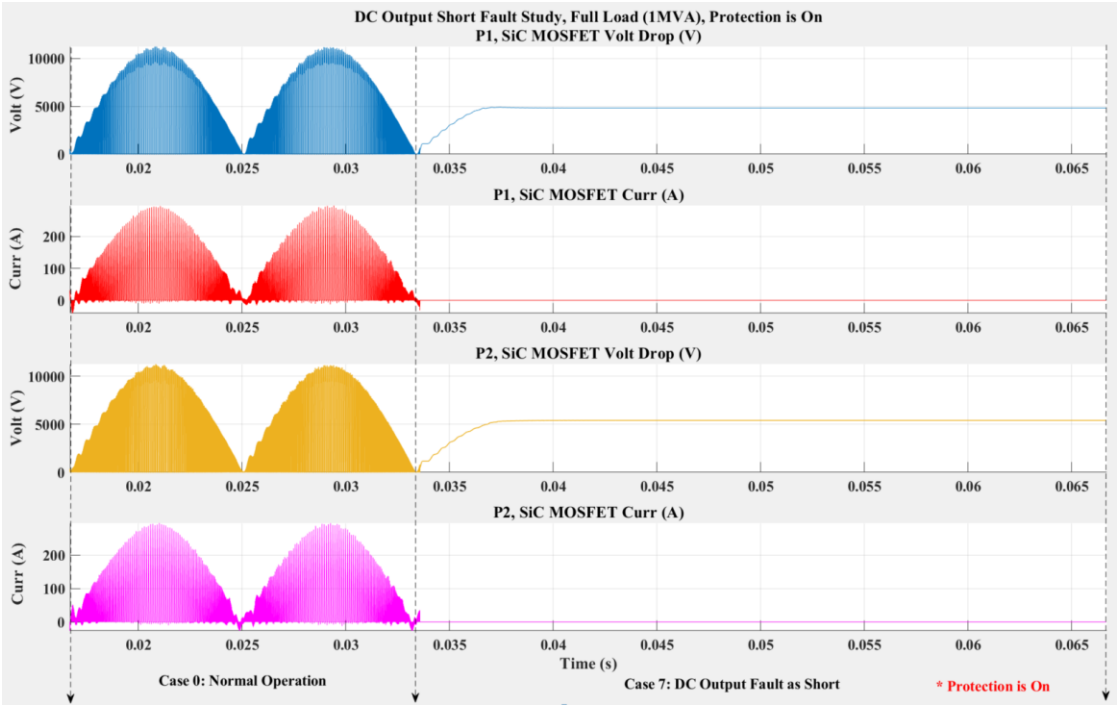


Fig. 4.53 Device P1, P2 Volt & Curr When DC Output Fault as Short (With Protection On), Full Load

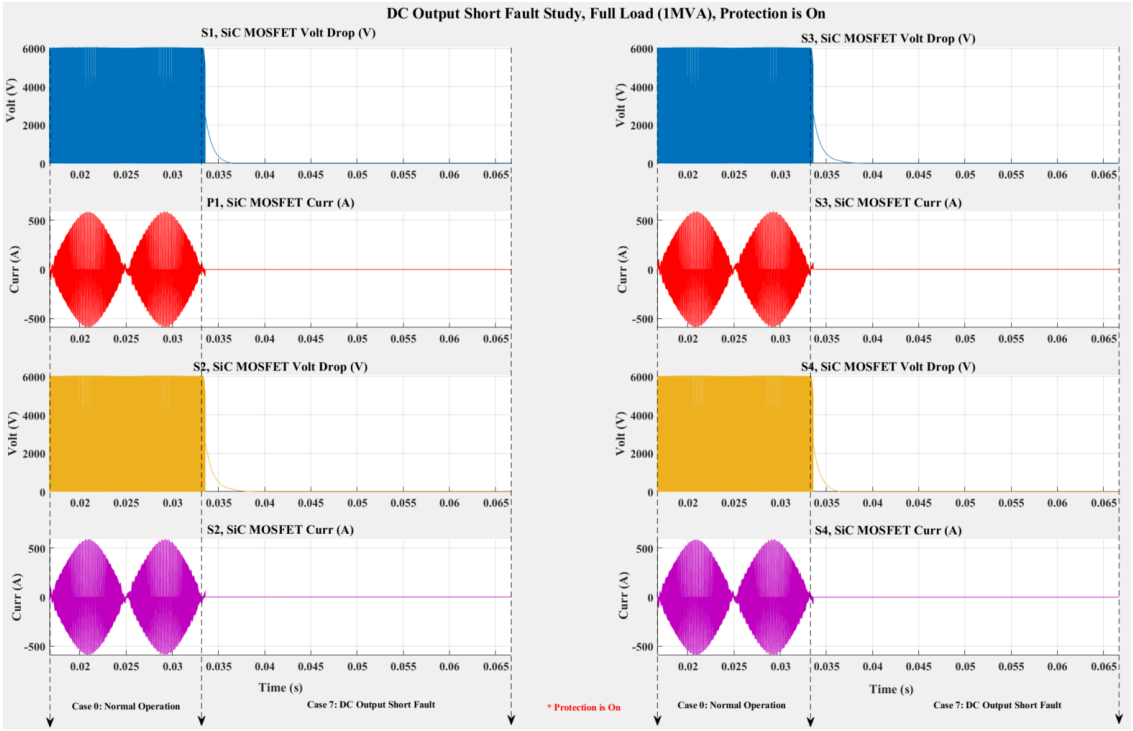


Fig. 4.54 Device S1 – S4 Volt & Curr When DC Output Fault as Short (With Protection On), Full Load

The post-fault study proves the validity of the DC under-voltage protection logic. Both voltage and current waveforms of all six SiC MOSFETs are presented to illustrate no destructive voltage or current level being observed. In another word, the three-phase DAB converter is carefully protected and offline safely. Once the DC output fault is cleared, the system can be brought online at any time. Although no over-current is found in the DAB converter, there is some high current flowing through the load reactor. That is because the energy stored in the DC output filter, including Cl, Ll and Rl, finds its way to dissipate. The equivalent circuit is shown as fig. 4.55.

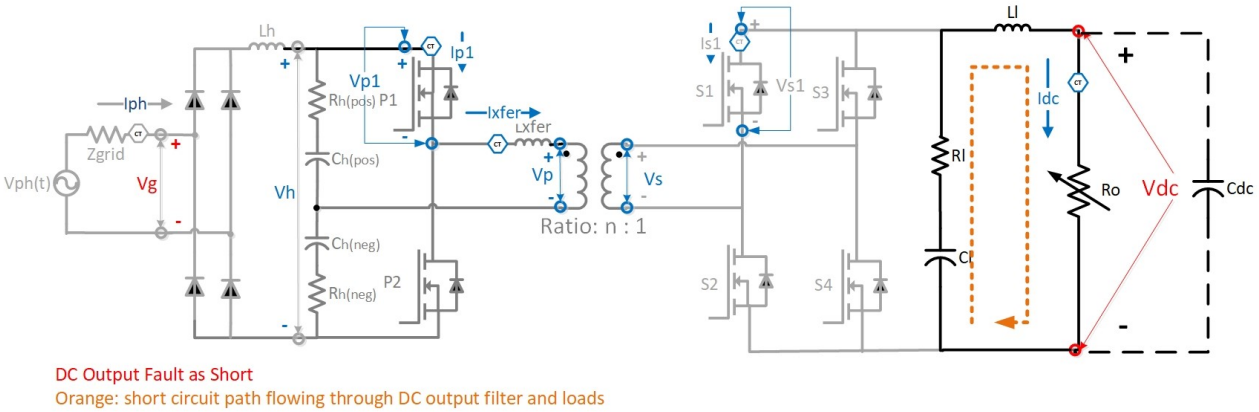


Fig. 4.55 Fault Ckt Current Path When DC Output Fault as Short

4.7.5 Output DC Bus Fault as Open Study (Case 8)

Case 8 is reserved for output DC bus open fault. It usually happens because the motor is under the abnormal operating conditions. The motor protection relay reports this problem and inverter stops firing. Thereby, the MV-PFC cannot transfer the power to the downstream circuit. The energy is stored in the DC output capacitor instead of been consumed by the motor. DC output bus keeps increasing until the protection kicks in.

In the MV-PFC's operation, this fault is no different than the extremely light load. The voltage feedback loop continues looking for the DC output and adjusting the power command. According to the chapter 4.6, the MV-PFC can operate for the long-term in the wide load range which is from 0.2 to 1.1 p.u (200 kVA to 1.1 MVA). The grid current is heavily distorted at the light load (less than 0.2 p.u), including this fault condition, and thereby injects too much harmonics back to the power grid. In a word, this fault would not cause the damage to the circuit, which makes it not

time-sensitive to shut the system down. In the case study, the fault response time is of 16 ms. The inputs, outputs and device waveforms before and after the faults are shown from fig. 4.56 to 4.59.

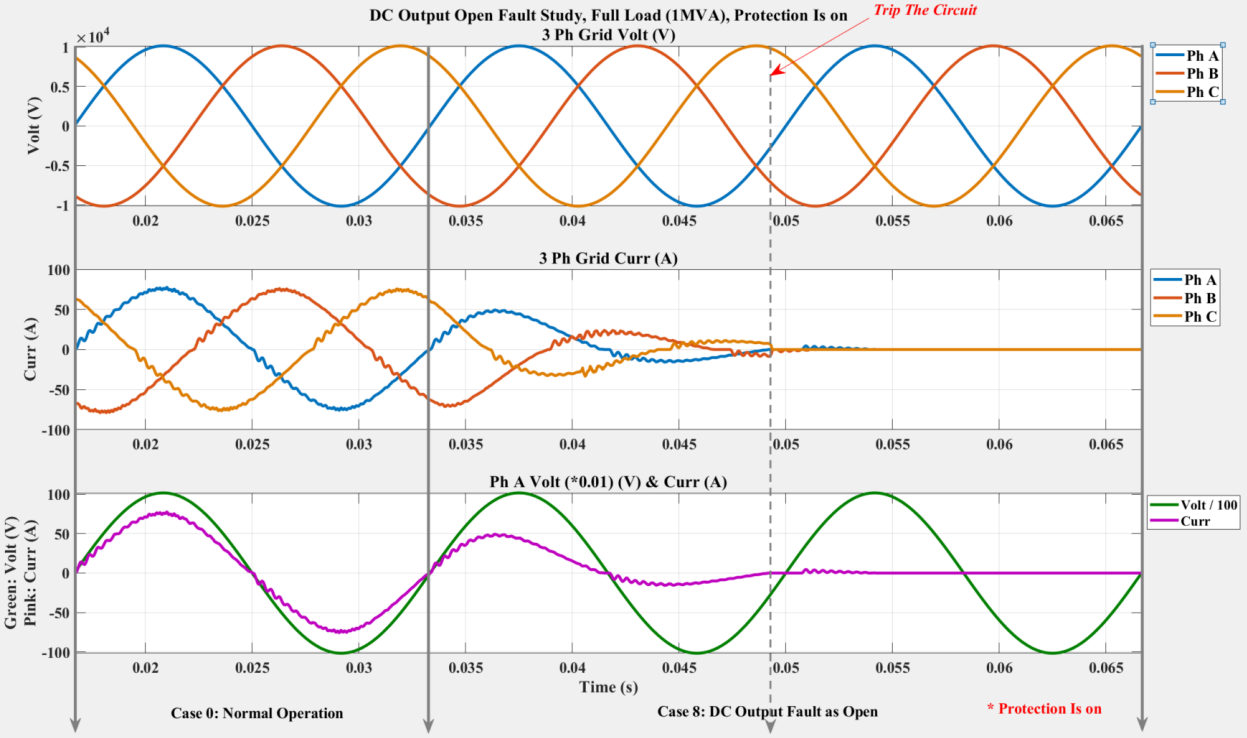


Fig. 4.56 AC Input When DC Output Fault as Open (Protection On), Full Load

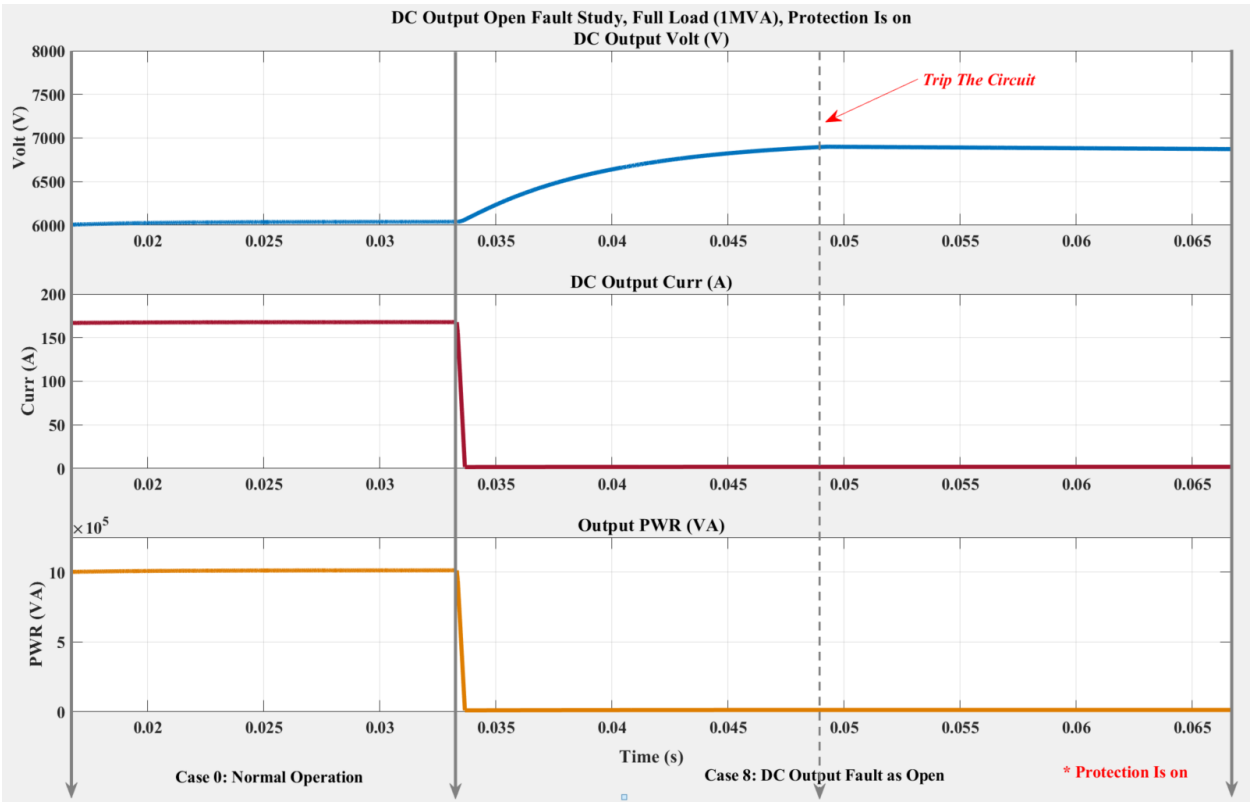


Fig. 4.57 DC Output When DC Output Fault as Open (Protection On), Full Load

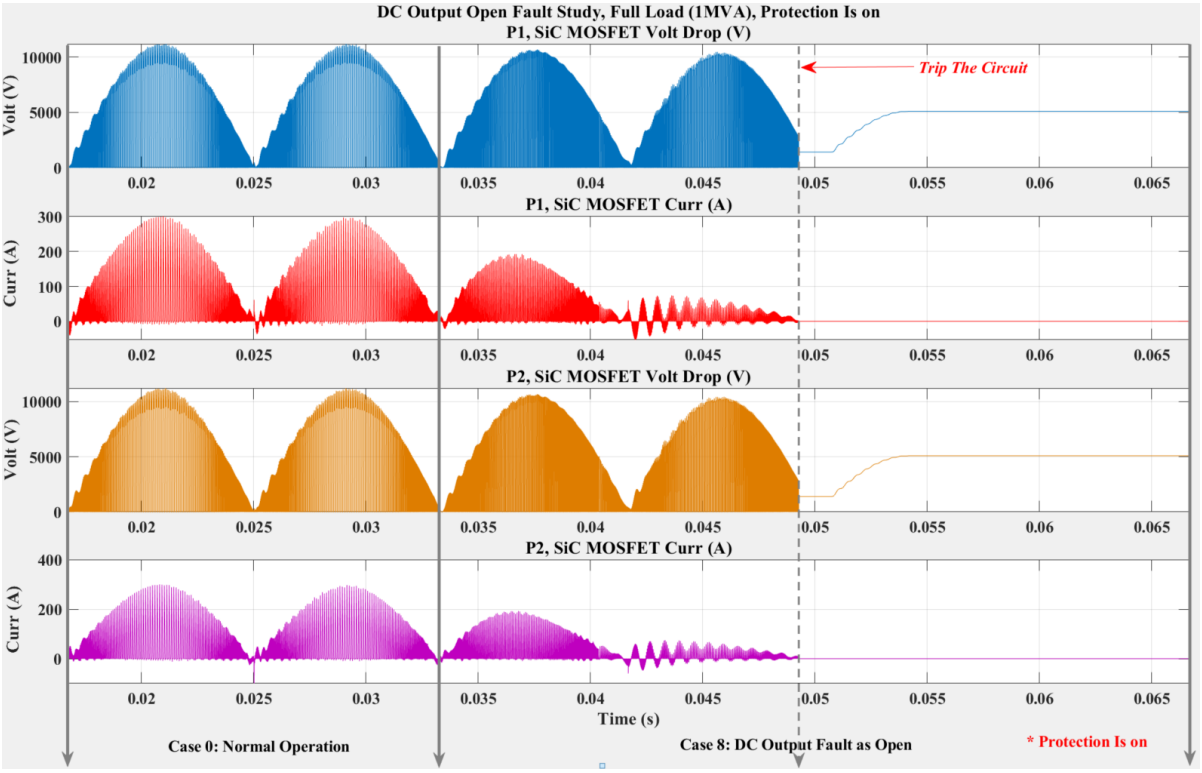


Fig. 4.58 Device P1, P2 Waves When DC Output Fault as Open, Protection On, Full Load

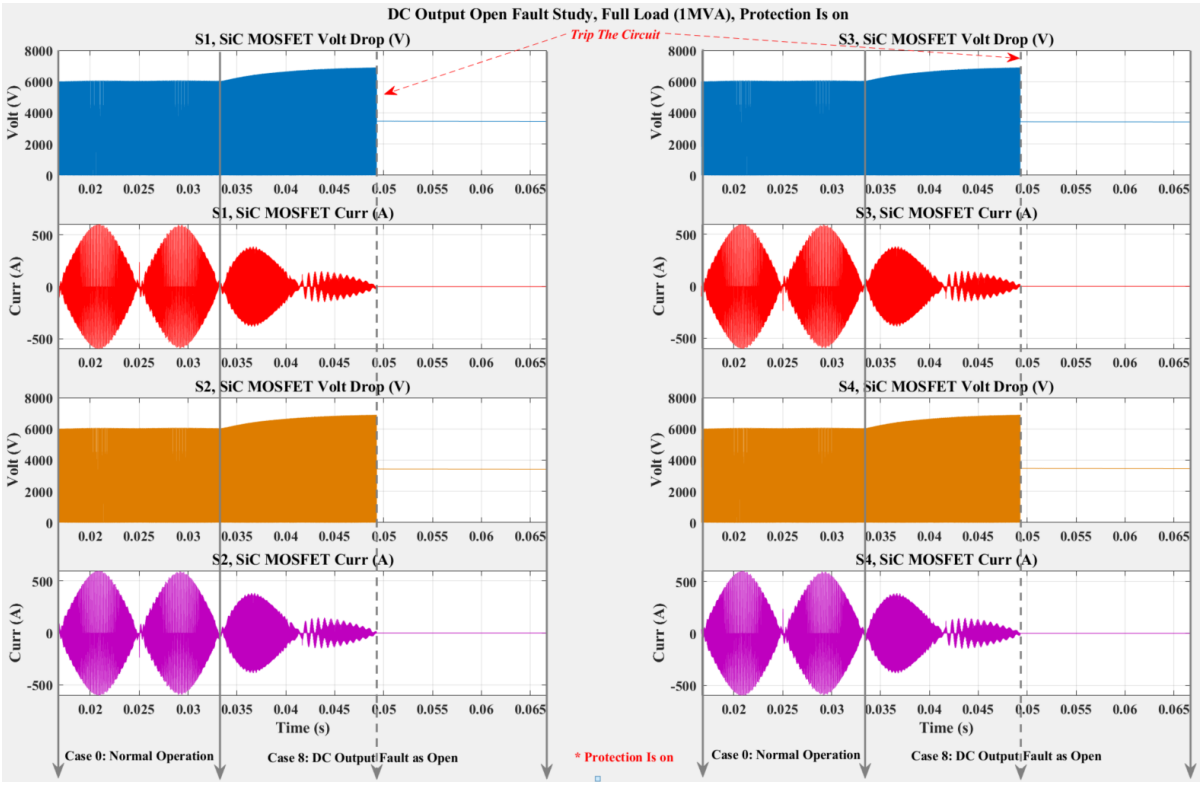


Fig. 4.59 Device S1 – S4 Volt & Curr When DC Output Fault as Open, Protection On, Full Load

Once the motor fault is confirmed, the downstream inverter inhibits the device firing signals and stops absorbing the power from the MV-PFC. In the circuit operating point of view, case 8 is like dropping off all the load and creating a very high impedance circuit. The most current flows through the DC output capacitor (Cdc) and charges it up. In the meanwhile, the overall system losses the power transfer capability and injects the harmonics back to the power grid. As a solution, the protection scheme is designed to shut down the system if

a. The amount of the power transfer is less than 10%.
b. The DC output over-voltage is detected.

In the field operation, the DC link capacitor need to be discharged by using a bleeding resistor circuit for the safety purpose. Once the motor fault is cleared, the MV-PFC rectifier can be brought online immediately.

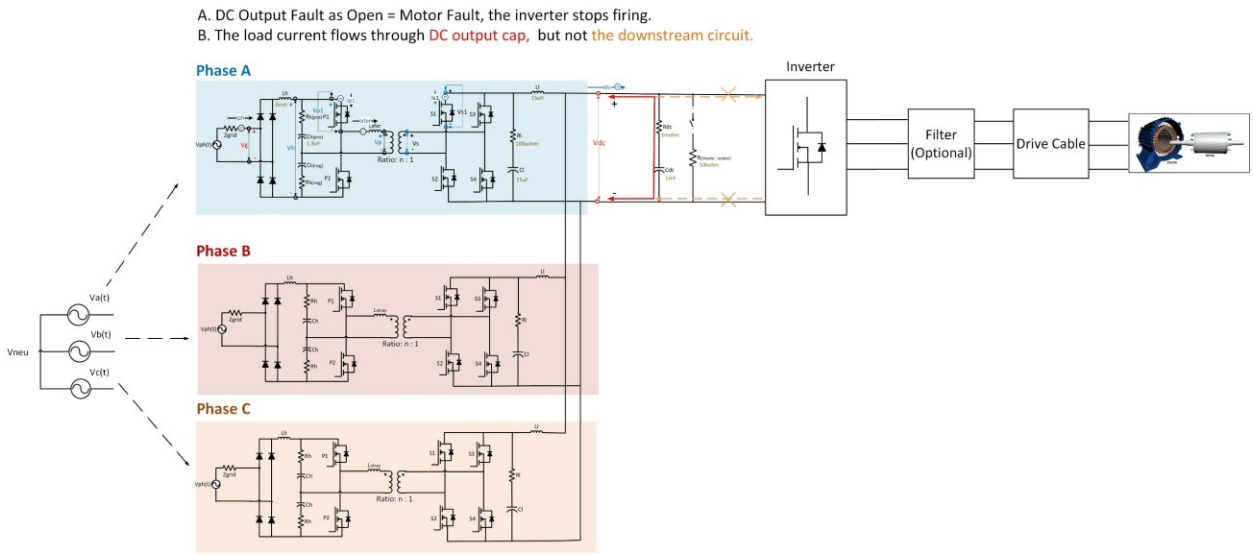


Fig. 4.60 Fault Ckt Current Path When DC Output Fault as Open

In a summary, table 4.3 lists all the faults discussed in this section. The protection strategy has been developed targeting to each fault. The design goal is to detect the fault quickly and accurately, then ensure less impact to the rest of the system.

Table 4.3 System Fault Scenarios and Protection Strategies

	Fault Location	Fault Scenario	Protection Strategy
Case 0	None	Normal Operation	None
Case 1	Inputs	Over Voltage Ride Through (OVRT).	None. The system is immune to the grid fluctuation.
Case 2	Inputs	Under Voltage Ride Through (UVRT).	None. The system is immune to the grid fluctuation.
Case 3	Inputs	Under Frequency Ride Through (UFRT).	None. The system is immune to the grid fluctuation.
Case 4	Inputs	Over Frequency Ride Through (OFRT).	None. The system is immune to the grid fluctuation.
Case 5	Power Module	SiC MOSFET Device Fault as Short	Device desaturation protection to protect the devices from over-current flowing through.

Table 4.3: continued

Case 6	Power Module	SiC MOSFET Device Fault as Open	Device over voltage protection.
Case 7	Outputs	Output DC Bus Fault as Short	DC output under-voltage protection.
Case 8	Outputs	Output DC Bus Fault as Open	a. Grid current distortion protection to shut down the system if the amount of the power transfer is lower than 10%. b. DC output over-voltage protection.

4.8 Conclusions

This chapter develops a full control scheme for the novel SiC MV isolated PFC rectifier. The first challenge is to operate the system in the AC-DC mode which is greatly different to the traditional DC-DC mode. A sophisticated feedforward modulator is proposed to calculate the gating signals based on power command, AC grid input and DC output. The control goal of this feedforward control logics is to realize the zero-voltage switching (ZVS), unity power factor (UPF), reactive power minimization under customized load profile.

After the core control function being developed, an application state machine is designed to resolve some practical problems. It includes I/O management, soft start-up procedure and system protection scheme. The soft start-up procedure coordinates with the I/O management system to effectively limit the inrush current and safely charges the output DC link from zero to full energy level,

Next, the system overall steady state performance is demonstrated under different load condition and large range of the grid voltage, which is in consistent with theoretical analysis. Furthermore, the system long-term operating reliability is investigated under different fault scenarios. The fault cases include the power grid fluctuation, SiC device short or open fault, DC output short or open fault. The system performance before and after fault is presented and the short current path is highlighted. Furthermore, the protection scheme for the different faults is proposed to prevent the system from entering the second failure and bring it offline quickly. All protection features have been thoroughly discussed and validated.

5 Ultra-Light Load THD Improvement of The Three-Phase MV-PFC Rectifier

5.1 Literature Review

Last chapter investigated the system dynamic response when there is a disturbance on either grid or load side. Furthermore, as a key performance index, the current THD was investigated given various load profiles. The grid current THD is one of the significant factors to evaluate the system stability and potential fault vulnerability. According to the IEEE Std 519, harmonic control in electric power system, there are some grid current THD limits based on the different applications. Generally speaking, the premium operating system has the grid current THD less than 5%. The normal operating system is capable to handle the grid current THD up to 15%. The situation which has current THD over 15% needs to be avoided. Otherwise, its operating time needs to be reduced to the minimum level.

Refer to the proposed three-phase PFC rectifier, the current THD does not keep constant over its wide operating zone. Bellowing picture tells the trend of the current distortion at different loads. In a summary, the lighter the load, the worse the THD. The system can operate when at least 20% load is applied, which keeps the current THD lower than 12%. For the premium operation, 40% or more load needs to be connected. The main purpose of this chapter is to resolve this issue to some levels. To be specific, there are two research goals,

a. Mitigate the current THD at light load condition when power output is below 0.2 p.u. 0.2 p.u at 1MVA is about 200 kVA.
b. Extend the system operating to the ultra-light load condition. The transferred power is as low as 0.025 p.u, 25 kVA.

Bellowing picture presents the relationship between average current THD and power output. Some papers talked about the efficiency improvement at light load conditions. Others talked about the methods to avoid the current surge and distortion at the light load condition. However, they did not give the numerical value about how much THD can be improved. [64-70]

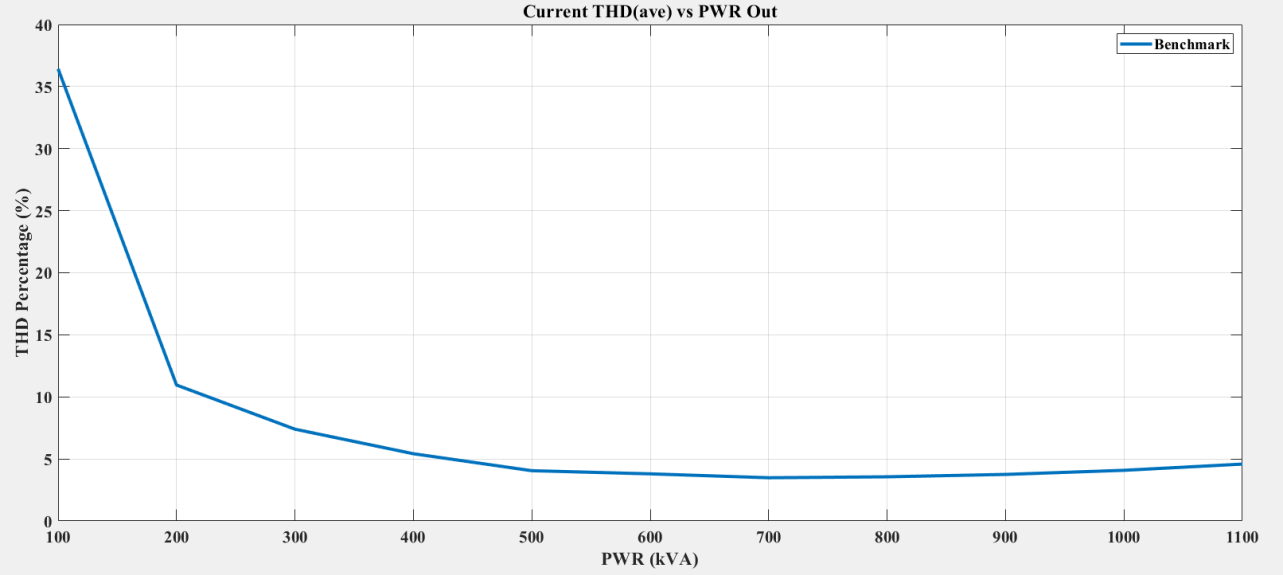


Fig. 5.1 Grid Current THD VS Power Flow

Four potential solutions had been investigated to improve the system performance by studying the operating conditions of a DAB converter. These development ideas are presented graphically in fig. 5.2. First choice is to move the inductor (Lh) to the grid side and treat it as the part of the grid filter. This option is to prevent the current ripple from transferring back to the power grid. The second and third options are to keep the hardware as it is and mitigate the current distortion by improving the control strategy. The thought behind these options is about the phase shift brought by the diode-based H-bridge which causes the asynchronization in the control loop. The waveform distortion is observed as one of the side effects. The solution is to use the high voltage bus, instead of grid voltage, as the reference for the PLL calculation. Alternatively, the sensors can stay at the same location. The phase shift brought by the diode-based rectifier is compensated in the control scheme. The last option is to tune the parasitic components in the resonant tank sitting on the primary side of the transformer. An overdamped circuit can effectively absorb the current oscillation and reduce the overall damping time. So, the influence brought by the oscillation to the fundamental waveform is minimized.

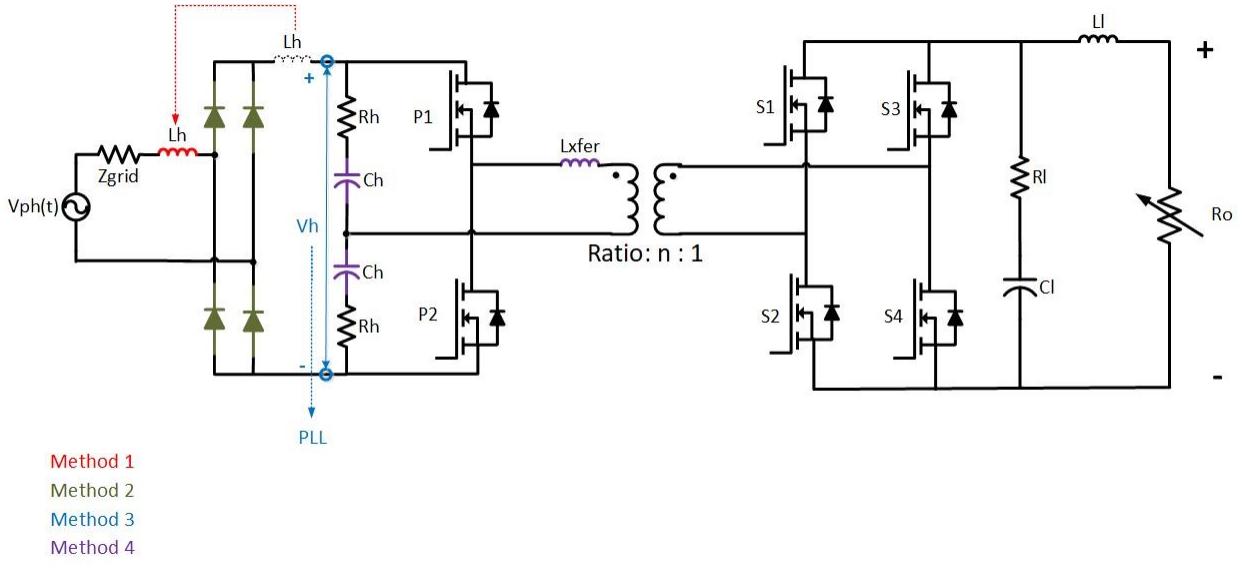


Fig. 5.2 Four Development Approaches

A comprehensive system analysis is required for the root cause analysis. Then, the end results are predicted based on the above proposed solutions. The simulation results are presented to prove the validity of the proposal.

5.2 A Novel Topology for The Ultra-Light Load Operation

Two conclusions about the grid current ripple are drawn by studying the circulating current paths in the diode-based H-bridge and mid-stage DAB. Most of the current ripple comes from the DC capacitor charging behavior. The high voltage capacitors are charged from almost zero to the peak voltage every 120 Hz. Besides, the parasitic components make the primary side of the DAB converter underdamped which deteriorates the problem. Weighing all the pros and cons, the front-end diode rectifier is kept for the compact system structure. The main task is to redesign the primary side of the DAB converter. The first three methods described in fig. 5.2 do not greatly improve the current THD as expected. The fourth method provides some promising results.

An advanced topology is proposed with an additional stray inductance added to the mid-stage circuit. This component is connected in series with HF transformer leakage inductor, which increases the damping coefficient. Fig. 5.3 shows the physical location of this stray inductor. Besides, the sensors are categorized in two groups, “must have” and “good to have”.

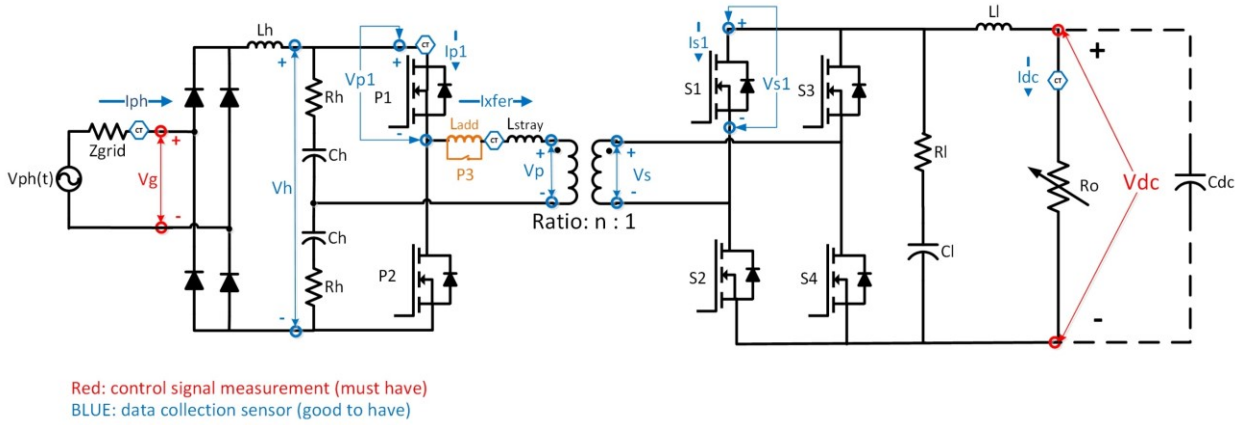


Fig. 5.3 A Noval Topology for Ultra-Light Load Operation (Single-Phase)

The system parameters are itemized in table 5.1. The newly added component is a 3 mH high voltage AC inductor. It is equipped with a bypass switch which snaps it when needed. Others remain the same as the original topology.

Table 5.1 System Parameters for The Proposed Topology

System Operating Condition	
Grid Voltage	12.5k (7.2k per phase)
Line Frequency	60 Hz
DC Bus	6 kV
Pout	1 MVA
Xfer Primary Side	
Lh (input filter)	6 mH
Ch (input filter)	1.3 uF
Lstray	1 mH
Ladd	3 mH
Transformer Turns Ratio	2 : 1
Xfer Secondary Side	
Ll (output filter)	15 uH
Cl (output filter)	75 uF
Semiconductor (SiC MOSFETs) Ratings	
Voltage Rating	12.5 kV

Table 5.1: continued

Current Rating	375 A
Switching Frequency	< = 150 kHz

5.3 The Control Strategy and Simulation Results

Based on the control scheme developed in the last chapter, the controller has an additional task to determine when to close the bypass switch and introduce the stray inductor to the resonant tank. In the light of achieving the premium operating condition, the upper limit of the switching frequency is capped at 150 kHz when lightly loaded. In details, three control strategies are activated independently based on the power command provided by the voltage feedback loop. It is worth emphasizing the timing to close the bypass switch.

d. Given the power command being below 100 kVA, put Lstray (3 mH) in the resonant tank and increase the frequency upper limit up to 150 kHz.
e. Given the power command being from 100 kVA to 400 kVA, put Lstray (3 mH) in the resonant tank and limit the frequency at 50 kHz.
f. Given the power command being over 400 kVA, bypass Lstray (3 mH) and keep the frequency upper limit as 50 kHz.

The physical characteristics of the inductor do not allow sudden change of the flowing current. Given this fact, once the bypass switch closing signal is generated, the controller acknowledges the command and closes the switch once the current zero-crossing is detected.

Fig. 5.4 gives the grid current THD at different loading conditions. Compared with original proposal, the newly proposed topology improves the grid current THD at light load condition. To be specific, the current THD gets reduced from 32% to 15% when system load is about 120 kVA (0.12 p.u). Furthermore, the amount of system power flow is as low as 25 kVA (0.025 p.u), which is about 25% of previous minimum operating point.

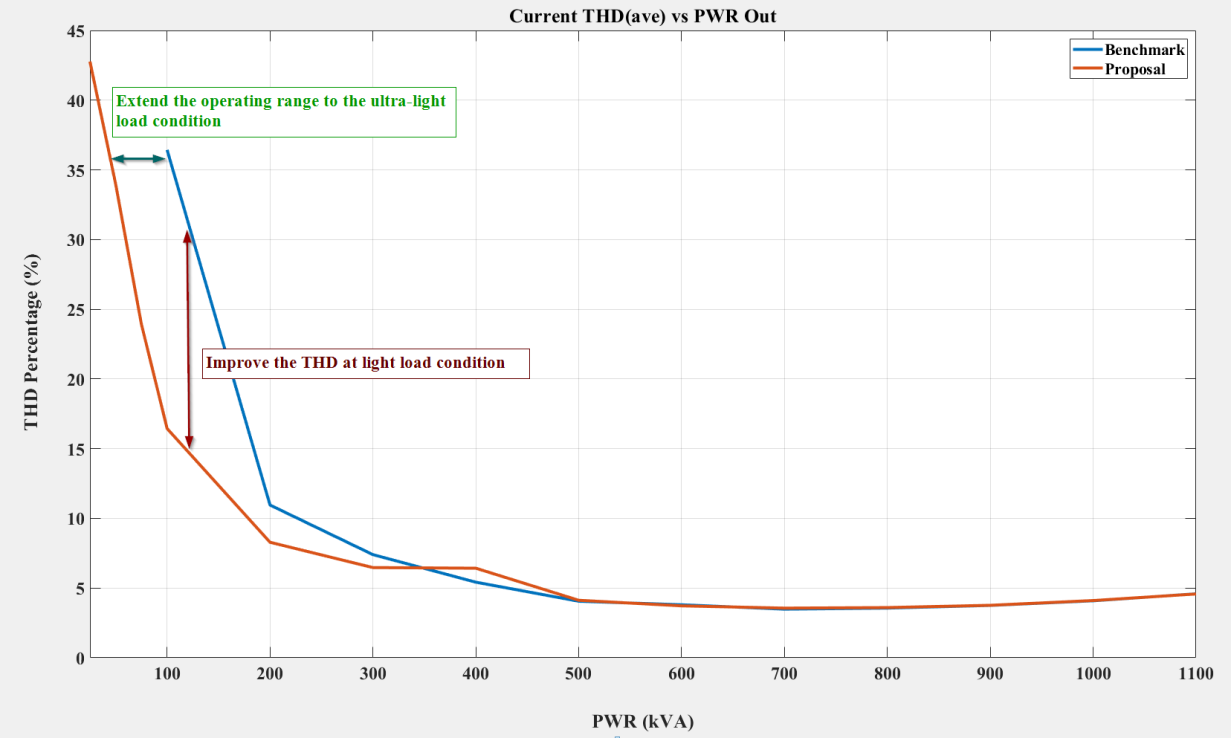


Fig. 5.4 Grid Current THD VS Power Flow by Using Proposed Topology

5.4 Transient State Performance

In order to evaluate the overall system performance per design specification, a case study is designed to demonstrate the system dynamic and transient performance. In the beginning, the system operates normally under the ultra-light load. Then, more loads get connected. From 0 to 33 ms, the load is about 0.025 p.u. Then, it goes up to 0.2 p.u at 33 ms and jumps to 1 p.u around 50 ms after the system start. Fig. 5.5, 5.6, 5.7 use the power grid, transformer waveforms and control variables to present the system dynamic response when the load varies.

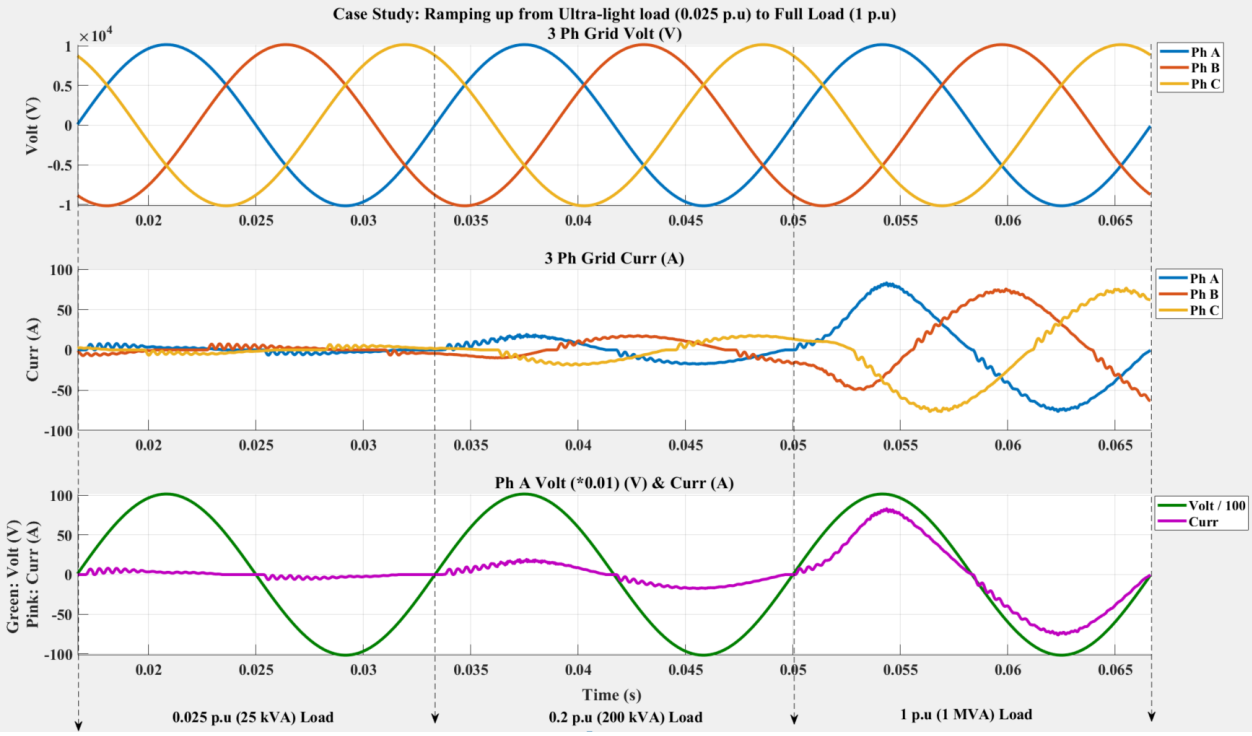


Fig. 5.5 AC Input When Load Varies

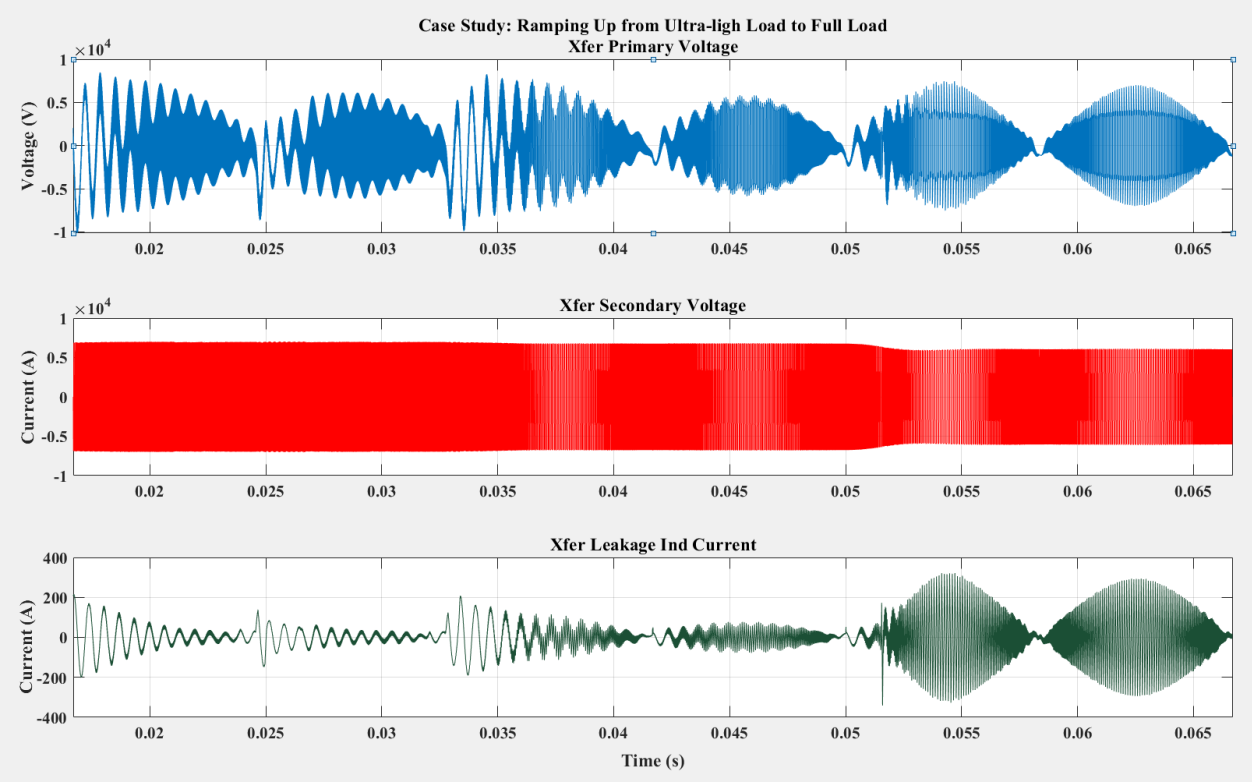


Fig. 5.6 Transformer Waveforms When Load Varies

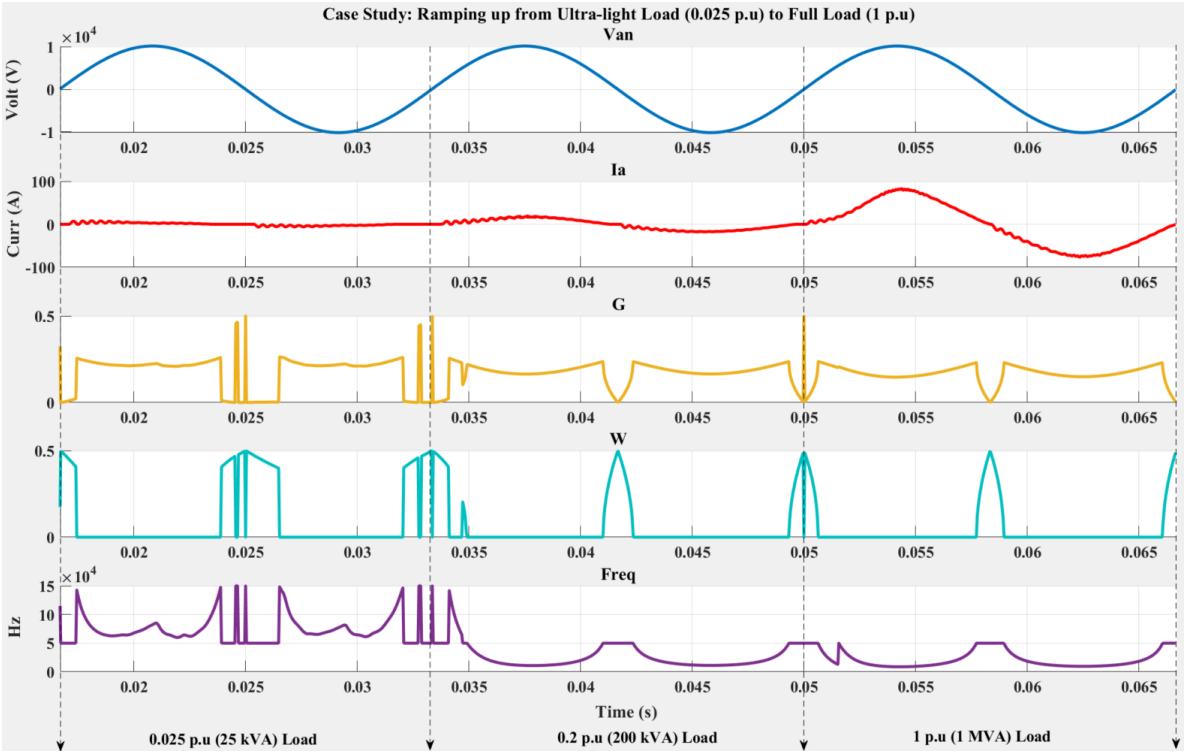


Fig. 5.7 Phase Voltage, Current and Control Variables When Load Varies

In this case study, the system tracks the power command by monitoring the load. The above diagrams also prove the newly added inductor and its exclusive bypass switch work seamlessly with the existing three-phase DAB PFC converter. The system has the operating flexibility under different load condition. In addition, the overall system performance is guaranteed and greatly improved at the ultra-light load situation.

5.5 Conclusions

This chapter proposes an upgrading option for the SiC MV isolated PFC rectifier to improve the performance weakness which is related to the grid current distortion at the ultra-light load condition. Thanks to the additional stray inductor, the circuit damping coefficient increases, which gives the better chance to smooth out the charging current ripple from the high voltage capacitors. In addition, different control strategies are activated depending on the real-time loading condition. With the proposed upgrade, the grid current THD gets improved and system can operate as low as 0.025 p.u load been applied. A case study of gradual load increase proves the system operating flexibility and performance stability.

6 Modular Implementation of the MV-PFC

6.1 System Description

Last few chapters discussed the integrated SiC MV three-phase PFC rectifier with the small footprint and high system operational efficiency. As an alternative design approach, the modular SiC MV three-phase PFC rectifier is investigated which has two advantages against the integrated structure. One is about the redundant stage to improve the system long-term reliability. For the integrated structure, the system needs to be offline and repaired if any power module is faulted. However, the modular structure normally has one redundant module as the backup. Assume a module is faulted, the system can bypass the defective module and bring the redundant module online, which reduces the system downtime and improves the fault tolerance. Another advantage brought by the modular design is to relax the device voltage and current stress. The low power semiconductor device can be used instead of the high-power device which lowers down the overall system cost.

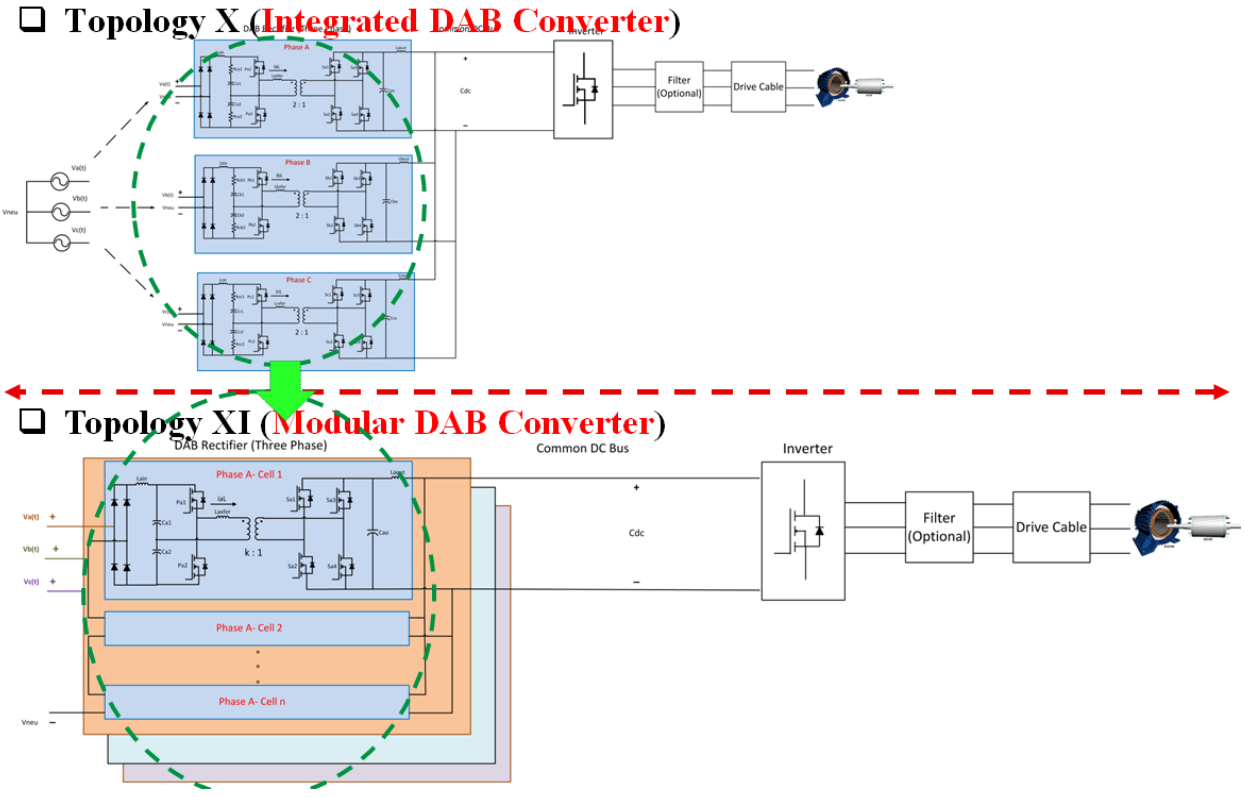


Fig. 6.1 Modular SiC MV Isolated Three-phase PFC Rectifier

Although the modular design brings many attractive features, it also has some problems which need to be carefully addressed. Two major issues are discussed and resolved in this chapter. The first one is about the negative effects coming from the individual module difference. It is not practical to build up the exact same module with the massive manufacturing volumes. The second one is to develop a self-protection mechanism to recover the system from the faults. Per described before, the defective module needs to be quickly and accurately detected and isolated. Then, the rest of the system need to be online and achieve the performance goals.

6.2 A Novel Inter-Module Balance Control

Traditionally, the DAB based modular converter has two stages, AC-DC rectifier and DC-DC converter. A separate AC-DC circuit sitting in the front side is to rectify the DC bus at the reference level. Then, the DC bus directly connects to the DC-DC sub-module. With the same voltage input, the main control goal of the DC-DC stage is to monitor and control its input current at the reference level [71] – [80]. At the system point of view, every module witnesses the same voltage input and carries the same amount of power flow.

Differ to the conventional topology, my proposed modular SiC MV three-phase PFC rectifier (fig. 6.2) has some new control challenges because of its one power stage structure. The first challenge is the lack of upstream circuit to balance the input voltage between modules. The system has to handle and balance the input voltage by itself. The second challenge is to realize the PFC function by itself. In a word, the proposed compact topology needs to achieve the same performance requirements with less control freedom.

Before discussing the solution, this paragraph investigates the possible hardware difference causing the unbalancing problem. Refer to the proposed modular SiC rectifier structure, the differences from semiconductor modules and capacitors are small, therefore could be neglected. However, the value of the stray inductance and HF transformer leakage inductance, varies in a relatively large range due to the parasitic parameter effects at high frequency. ANSI/IEEE (C57.12.00-2010) and IEC (60076-1) specifies the tolerance of the transformer's turns-ratio less than 0.5%. However, the impedance error is as high as (plus or minus) 7.5% to (plus or minus) 10% with different impedance range. Talking about the industrial products, the air core inductor manufacturers claim the 20% tolerance in the production volume.

A case study is used to illustrate the problem introduced by the inductor difference. Per fig. 6.2, the phase A has two modules connected as input-series output-parallel (ISOP) structure. Phase B and C only have one module. Each phase carries equal amount of power and has its own local controller. At the starting point, the control scheme is adapted from the one designed in the chapter 4 and simply assigned 50% power command to each module in the phase A. At the full load condition, sub-module A1 and A2 are supposed to carry 166.7 kW power flow. Besides, the voltage stress on the input and output current stress are 50% in the ideal case. The single module assigned to phase B and C has 333.3 kW power flow and see the full level of voltage and current.

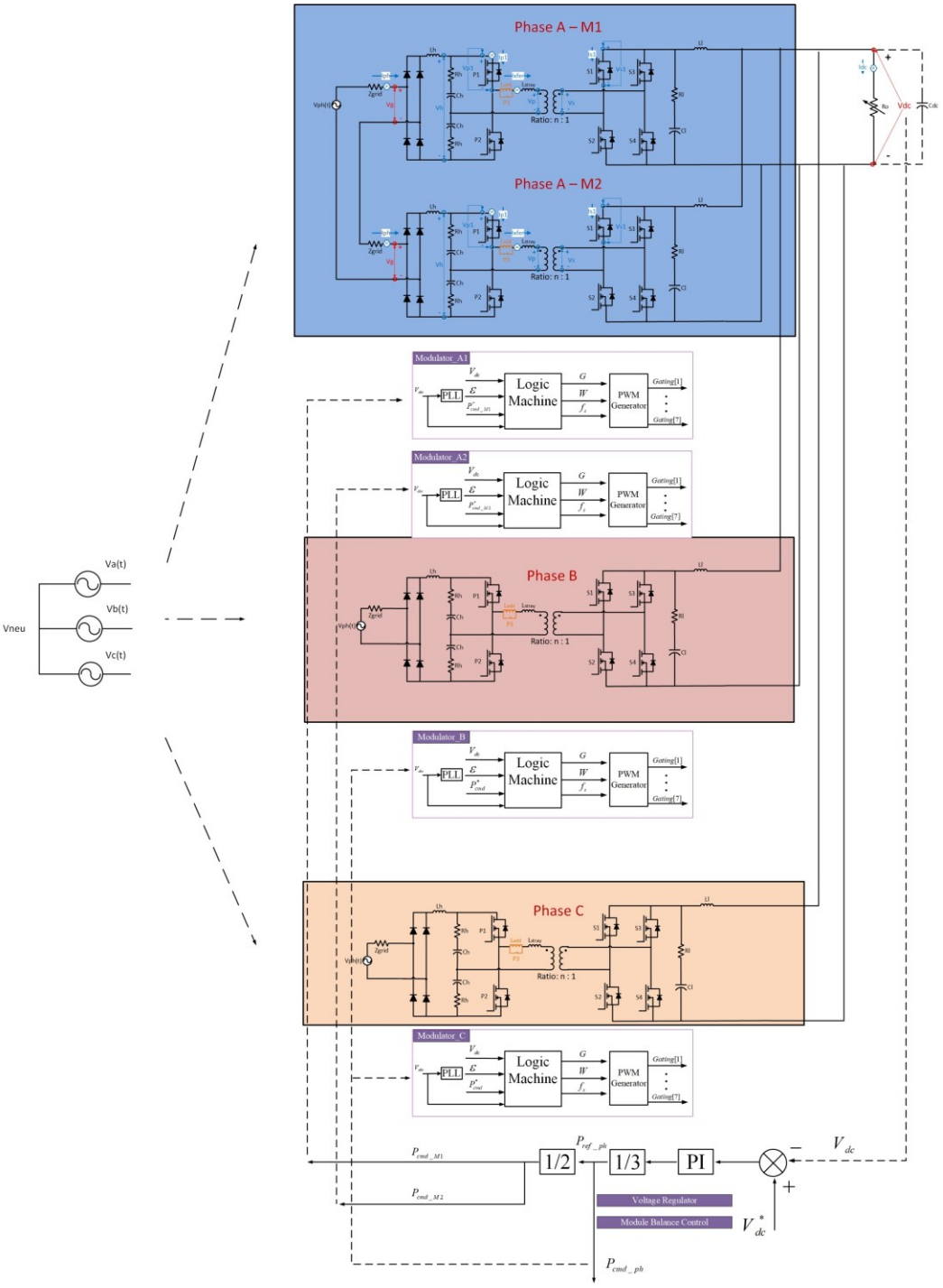


Fig. 6.2 Modular Three-Phase PFC DAB Converter with No Balance Control

Table 6.1 System Parameters for The Proposed Modular DAB Topology

System Operating Condition			
Grid Voltage		12.5k (7.2k per phase)	
Line Frequency		60 Hz	
DC Bus		6 kV	
Pout		1 MVA	
Xfer Primary Side (Normal)		Xfer Primary Side (Abnormal)	
Lh (input filter)	6 mH	Lh (input filter)	6 mH
Ch (input filter)	1.3 uF	Ch (input filter)	1.3 uF
Lstray	1 mH	Lstray	1.2 mH
Ladd	3 mH	Ladd	3.6 mH
Transformer Turns Ratio	2 : 1	Transformer Turns Ratio	2 : 1
Xfer Secondary Side			
Ll (output filter)		15 uH	
Cl (output filter)		75 uF	
Semiconductor (SiC MOSFETs) Ratings – Single Module Per Phase		Semiconductor (SiC MOSFETs) Ratings – Two Modules Per Phase	
Voltage Rating	12.5 kV	Voltage Rating	6.25 kV
Current Rating	375 A	Current Rating	375 A
Switching Frequency	< = 150 kHz	Switching Frequency	< = 150 kHz

Both half load and full load conditions are used to demonstrate the negative effects brought by the hardware difference. For the ISOP circuit, the modules have the same input current, but different voltage drop. The different voltage drop is proportional to the total amount of power transfer. Strictly speaking, the hardware difference causes the different power virtual impedance. Power always tries to flow thought the smallest impedance path. As a result, both the input power and voltage are influenced and show the difference between modules.

Using the system parameters listed in table 6.1, the system operates at either full load (1 MVA) or half load (500 kVA) to illustrate the power unbalancing issue between different modules. The system performance has slightly difference under these two cases.

Starting with half load condition, the three-phase power is balanced and gets regulated based on the real-time load. The hardware difference does not affect the power transfer between three phases because each phase is controlled separately to have 33.33% of total power flow.

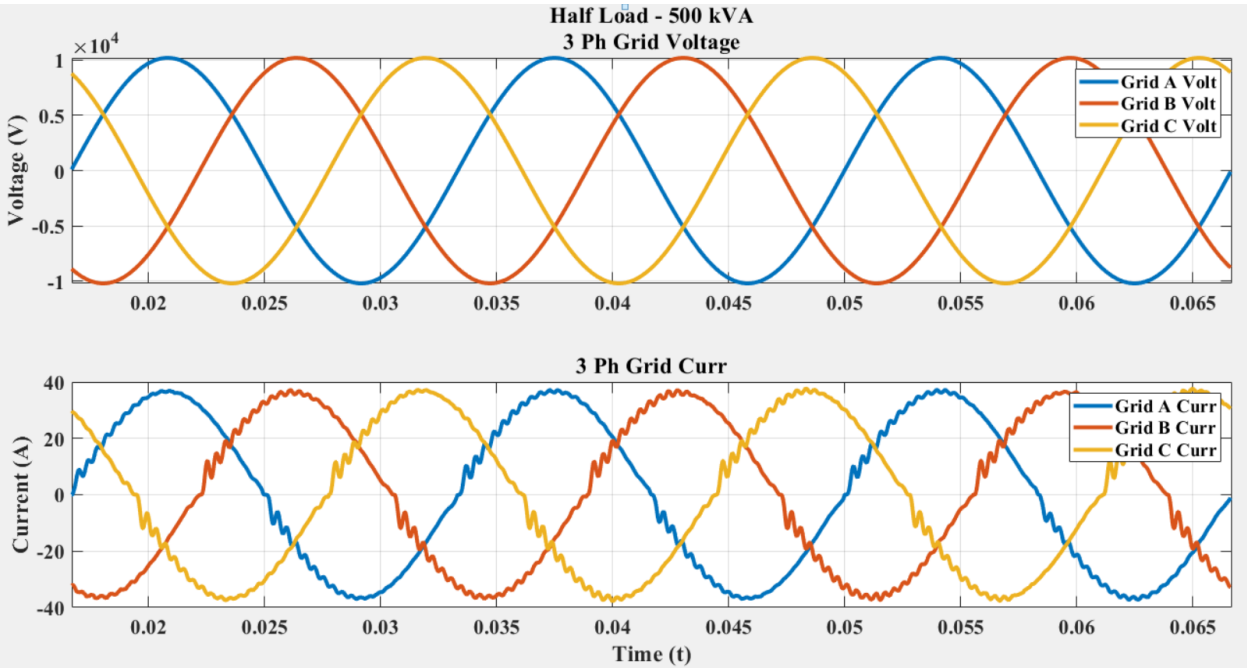


Fig. 6.3 Three-Phase Grid Volt & Curr at 500 kVA Load

Inside of phase A, two sub-modules have different power flow and witness different input voltage because of the inductor difference. Without the additional inter-module balancing mechanism, the main controller automatically assigns 50% power command to either submodule a and b in phase A. As a result, the inductor difference causes the input and high DC bus voltage difference across two submodules. In fig. 6.4, sub-module input voltage, grid current, high DC bus half sinusoid waveform and voltage / power command are presented. In this case, the voltage, also the power, has the difference as high as 4.3% when half-loaded.

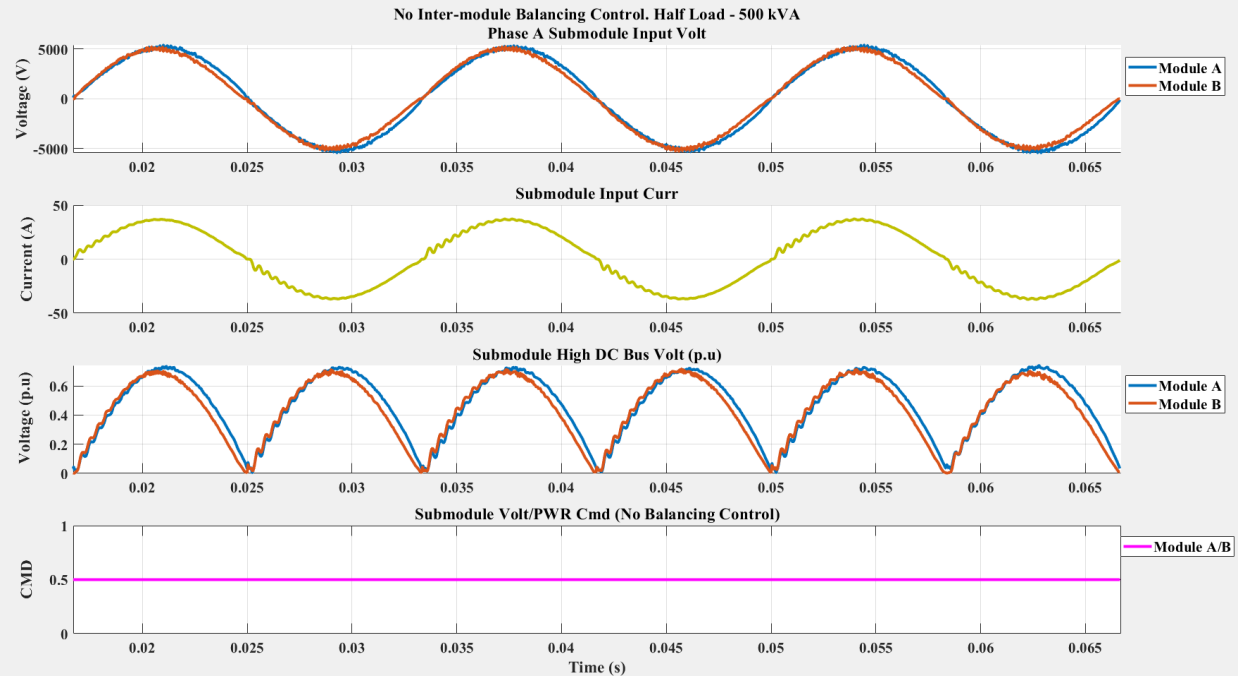


Fig. 6.4 Sub-module Waveforms at 500 kVA Load Without Balancing Control

The additional 50% load is added which makes the system fully loaded, 100 MVA. Like half load condition, the three-phase power is balanced and gets regulated to track DC bus output.

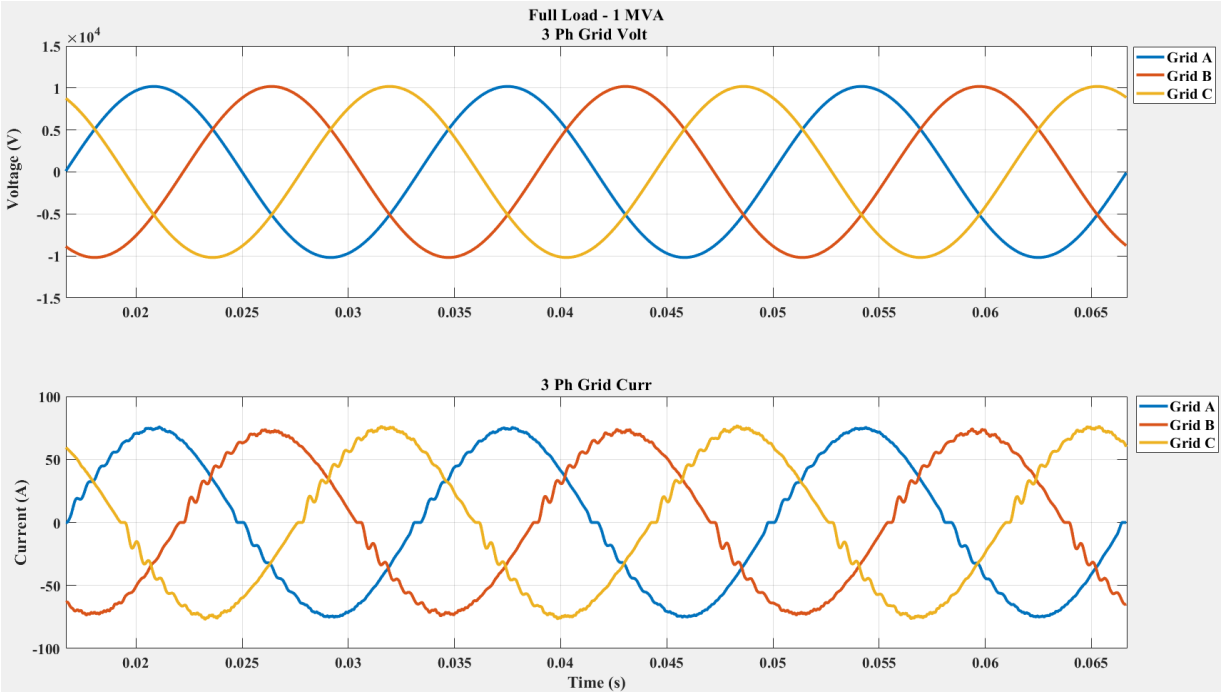


Fig. 6.5 Three-Phase Grid Volt & Curr at 1 MVA Load

Inside of phase A, there is a voltage / power unbalancing issue. Fig. 6.6 tells the difference as high as 4.42%. It is worth mentioning that the DC bus does not collapse with minor inductance difference.

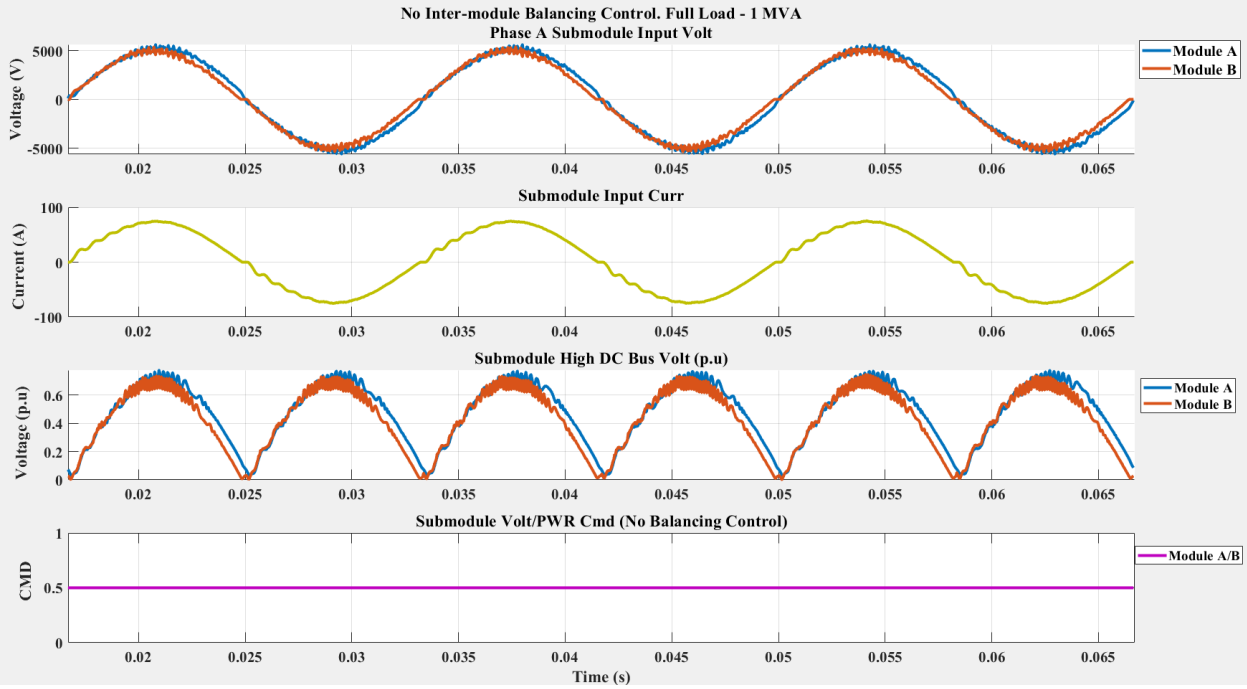


Fig. 6.6 Sub-module Waveforms at 1 MVA Load Without Balancing Control

The previous two case studies demonstrate the negative effects brought by the module hardware difference. An inter-module balancing logic is proposed and added to the existing control scheme. The proposed novel control scheme, shown in fig. 6.7, does not evenly assign the 50% to each sub-module, but actively balance the power transfer between modules by monitoring the high DC bus voltage. For better performance, the PI values for balancing control are changed based on the load profile (table 6.2). Fig. 6.8 and 6.9 are the sub-module waveforms at either half load or full load with the balancing control on.

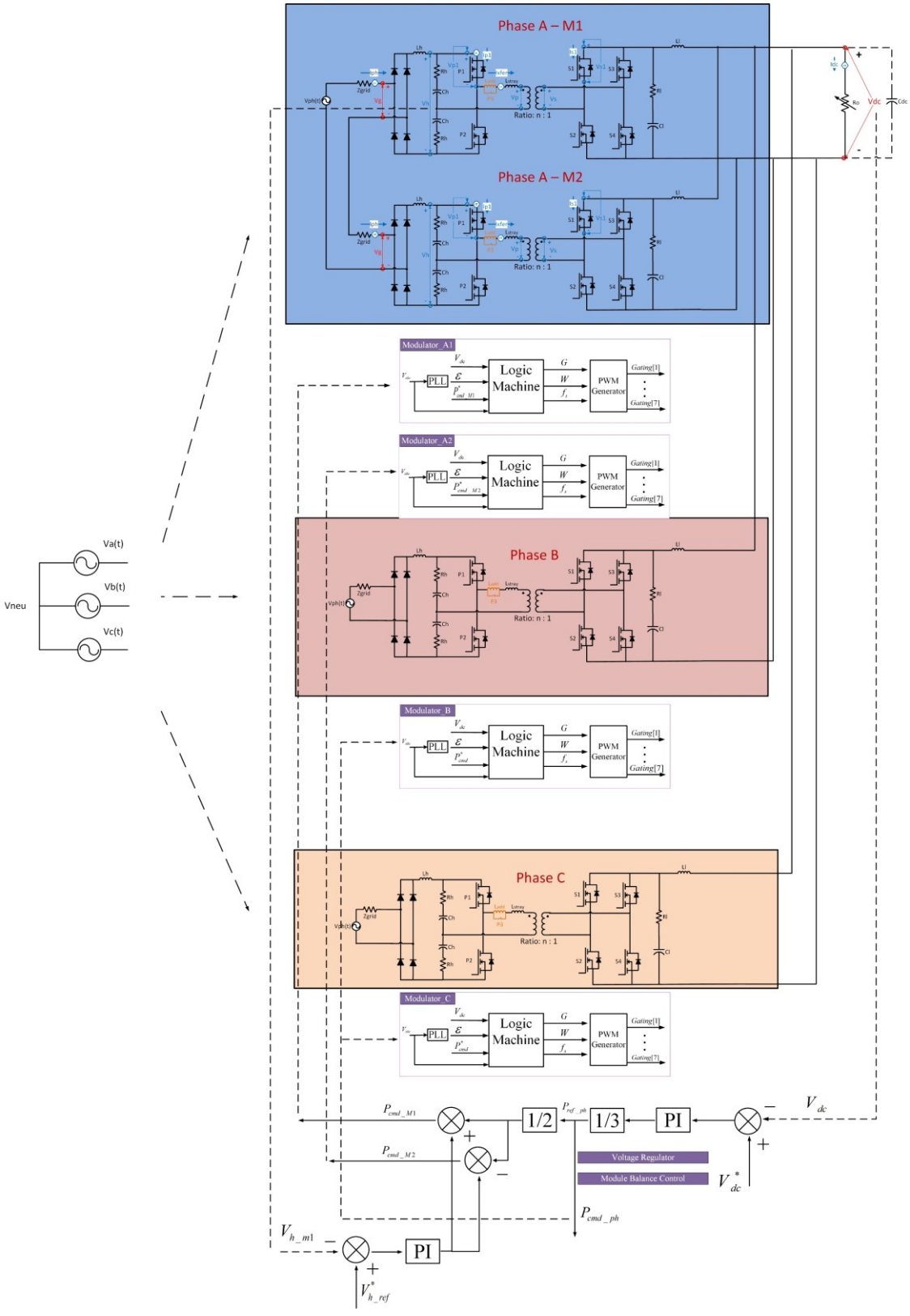


Fig. 6.7 Modular Three-Phase PFC DAB Converter with Balancing Control

Table 6.2 Inter-Module Balancing Control Parameters

Balancing Control Loop		
At Half Load	(P, I) Parameters	(2.5, 25)
At Full Load	(P, I) Parameters	(7.5, 75)

Thanks to the additional balancing control, the voltage difference, also power difference, between two sub-modules are reduced from 4.3% to 0.673% and 4.42% to 0.413%. The inter-module balancing is achieved successfully.

Table 6.3 Inter-Module Difference with or without Balancing Control

Balancing Control Loop		
No Inter-Module Balancing Control	At Half Load	4.3%
	At Full Load	4.42%
With Inter-Module Balancing Control	At Half Load	0.673%
	At Full Load	0.413%

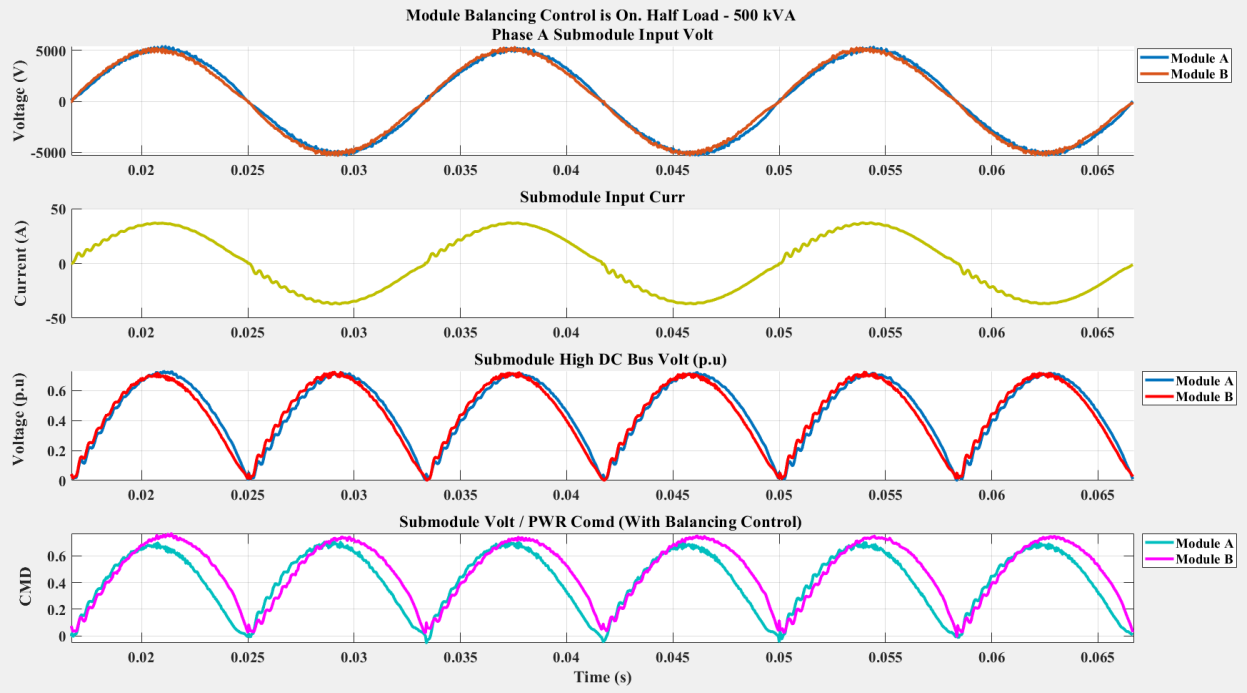


Fig. 6.8 Sub-module Waveforms at 500 kVA Load With Balancing Control On

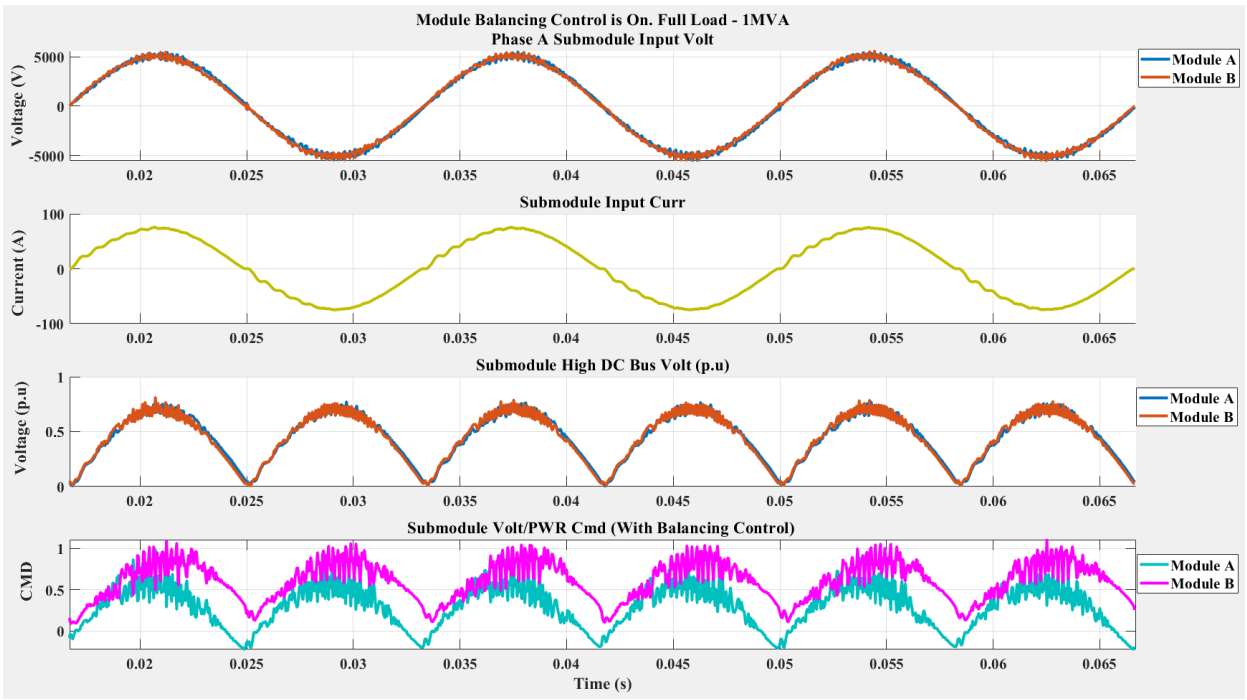


Fig. 6.9 Sub-module Waveforms at 1 MVA Load With Balancing Control On

6.3 System Protection Scheme

Circuitry long-term operating stability is one of the popular topics in the system-level analysis, especially when the engineers are trying to commercialize the proposed circuit as the industrial product. Similar to the integrated structure discussed in chapter 4.7, the system fault can be categorized by its location, like system input, module itself and DC output. There is no difference for either integrated topology and modular topology when the fault occurs at either power grid input or DC output. In order to avoid the verbosity and repetition, only case 5 (SiC MOSFET device fault as short) and case 6 (SiC MOSFET device fault as open) are discussed in this section.

When the fault happens inside of the module, the integrated topology has no choice but gets offline. Otherwise, the power unbalance issue happens between phases. However, the modular system can detect the defective power module and bypass it. Then, the healthy module needs to transfer more power to compensate the loss of the bad module. In this case, the system can be still in the commissioning and is not impacted by the fault. During the next shutdown maintenance, the defective module can be replaced and brought back to the system.

In the normal operating condition, per fig. 6.10, the line breaker for each module is open for series-connection input and the load breakers are left as closed for parallel-connection output. Both modules are in the circuit and carries 50% amount of the power transfer. Once the fault case 5 or case 6 occurs, assume M2 module is faulted, the breakers change the status as fig. 6.11. The line breaker is closed to reject the grid voltage input and load breaker is opened to disconnect the downstream circuit. Thereby, the defective module is in the isolation mode and can be brought offline safely. The traditional high voltage circuit breaker can be used and usually takes about 100 ms to function and suppress the potential arcing during the current interruption.

The case study is developed to validate the system performance when module is faulted. Differ to the case 5 and 6 discussed in chapter 4, this section also includes the impact brought by the faulted module to the health module locating in the same phase. The module internal faults are defined as,

a. Case 9: SiC MSOFET device fault as short. Choose P1 in phase A submodule 2 in this case study.

b. Case 10: SiC MSOFET device fault as open. Choose P1 in phase A submodule 2 in this case study.

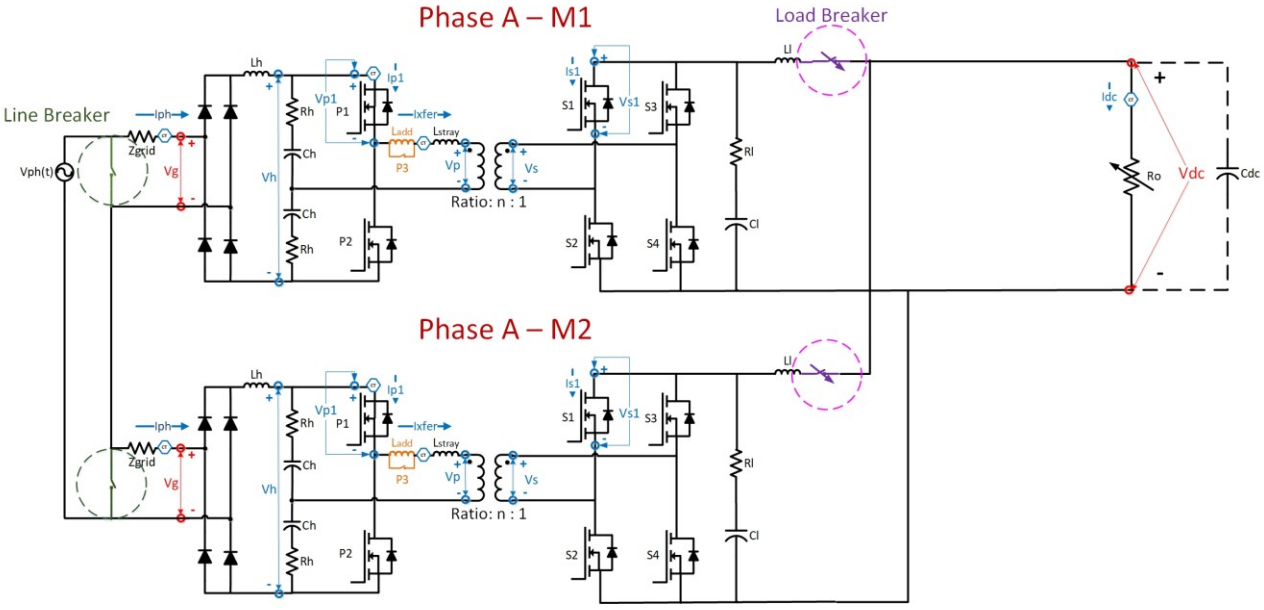


Fig. 6.10 Line Breaker and Load Breaker Status at Normal Operation

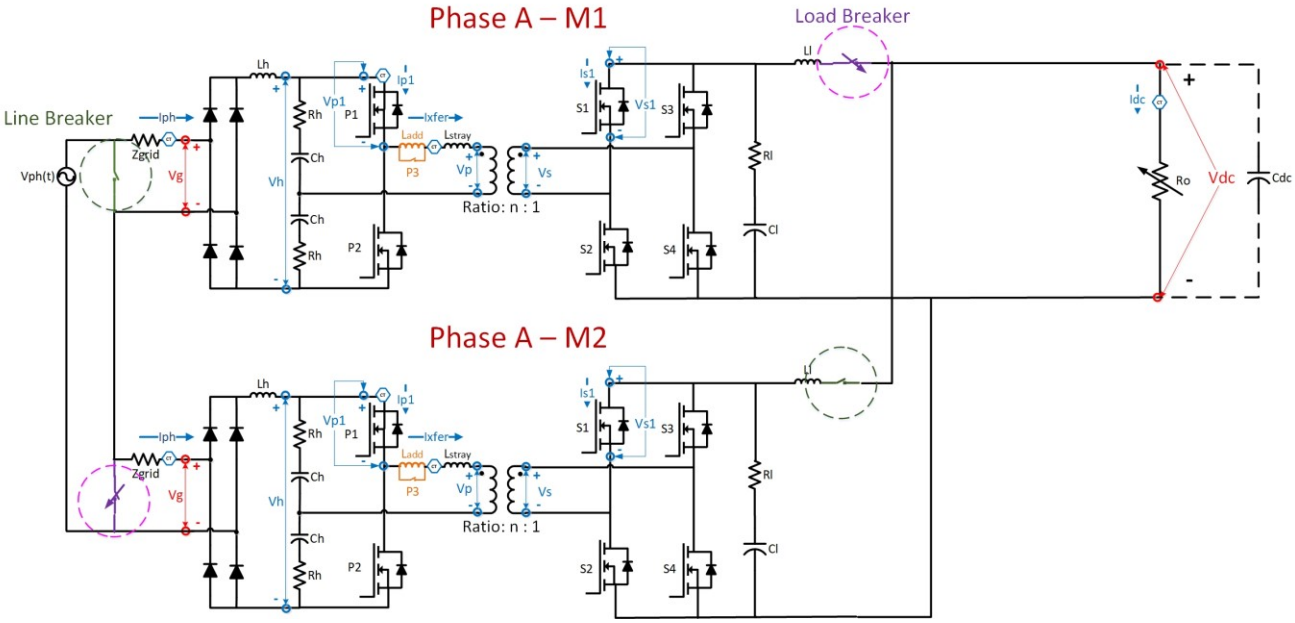


Fig. 6.11 Line Breaker and Load Breaker Status When M2 Is Bypassed

6.3.1 Device Fault as Short Fault Study in Modular Structure (Case 9)

Following the case study in the section 6.2, a fully loaded system with inter-module balance control is selected as the benchmark system. The system starts as the normal operating mode, then the device short fault is introduced. The AC grid input, DC output and module waveforms are selected to show the system response before and after the fault.

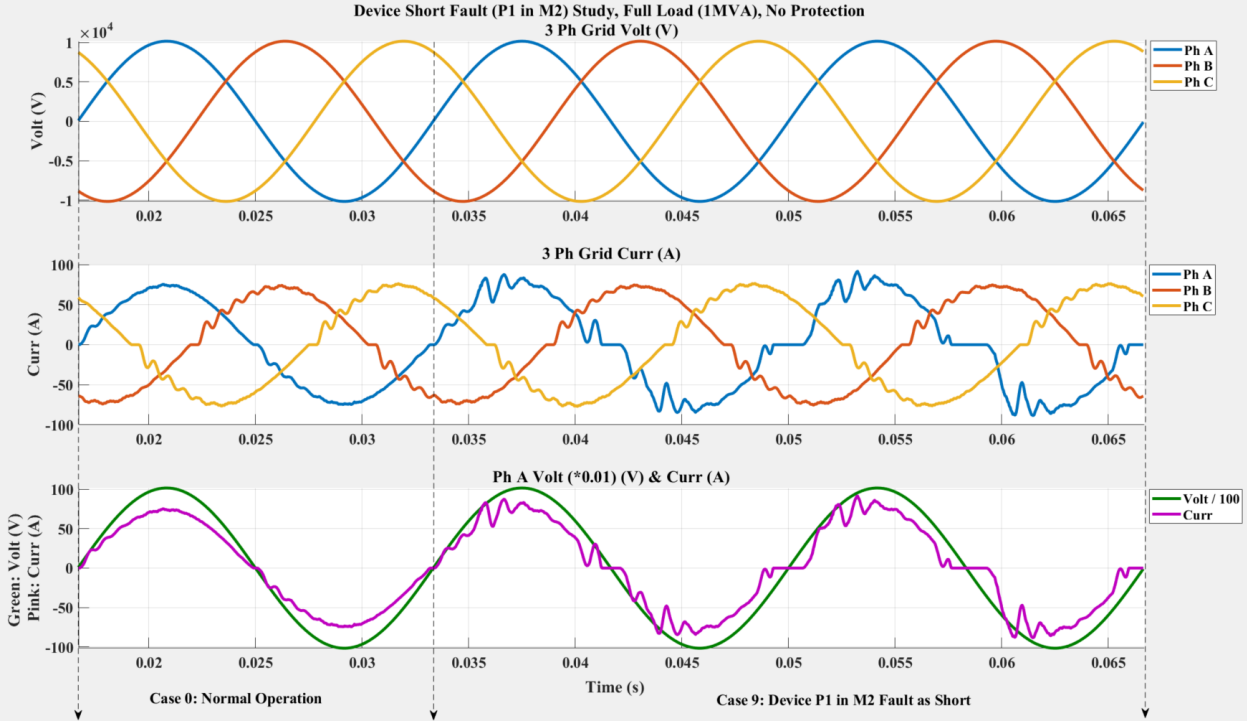


Fig. 6.12 AC Input When Device Fault as Short (No Protection), Full Load

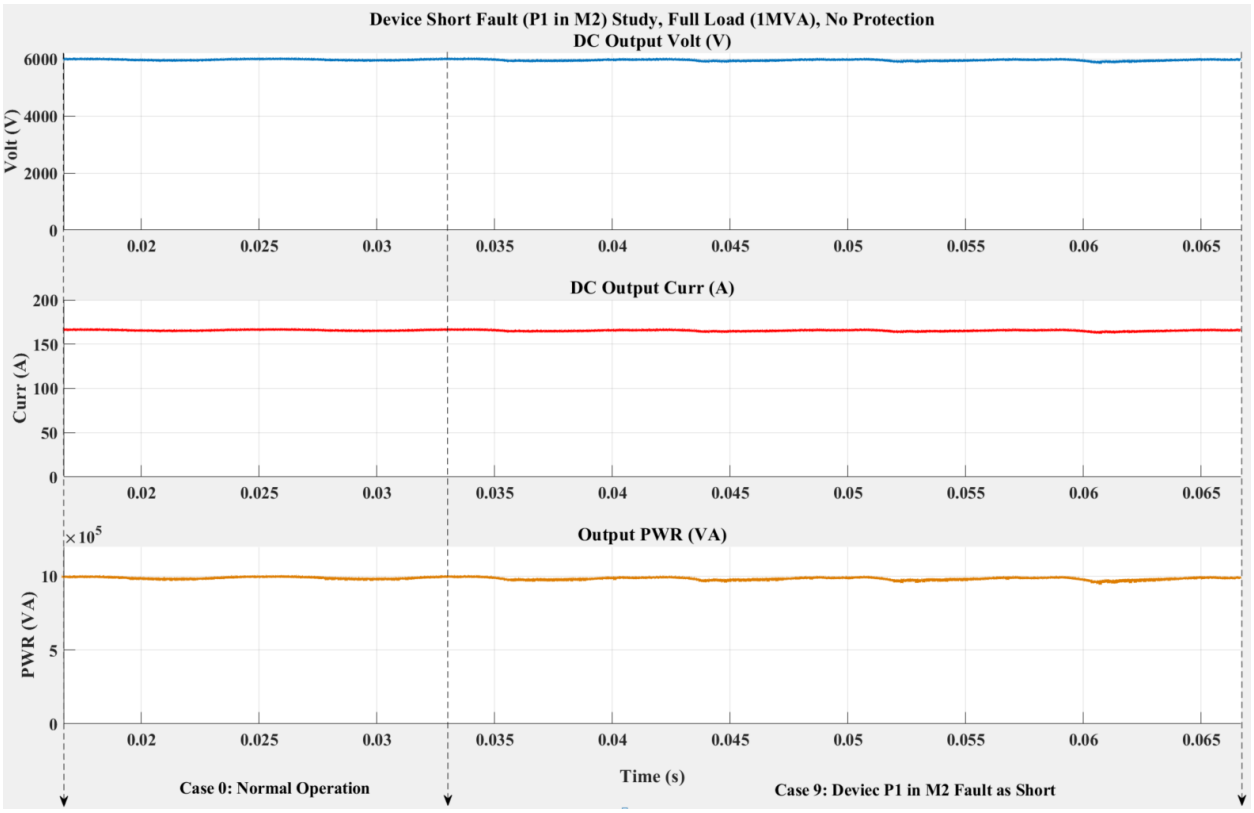


Fig. 6.13 DC Output When Device Fault as Short (No Protection), Full Load

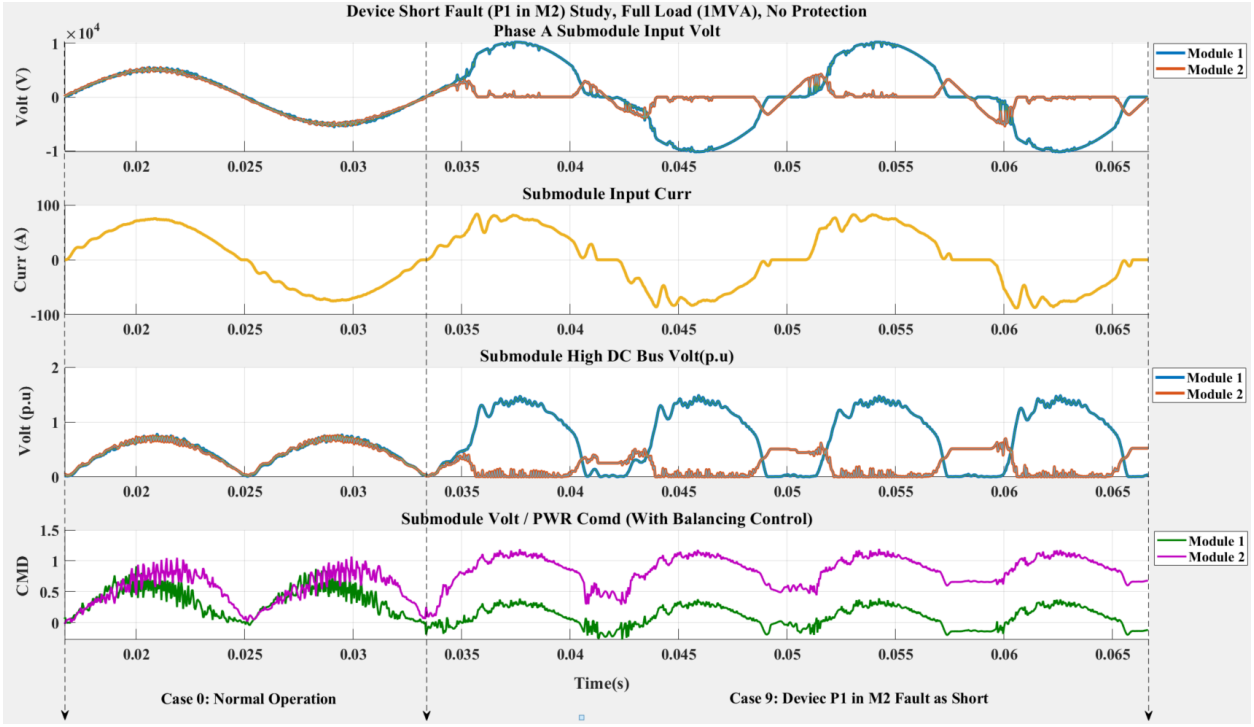


Fig. 6.14 Sub-module Waveforms When Device Fault as Short (No Protection), Full Load

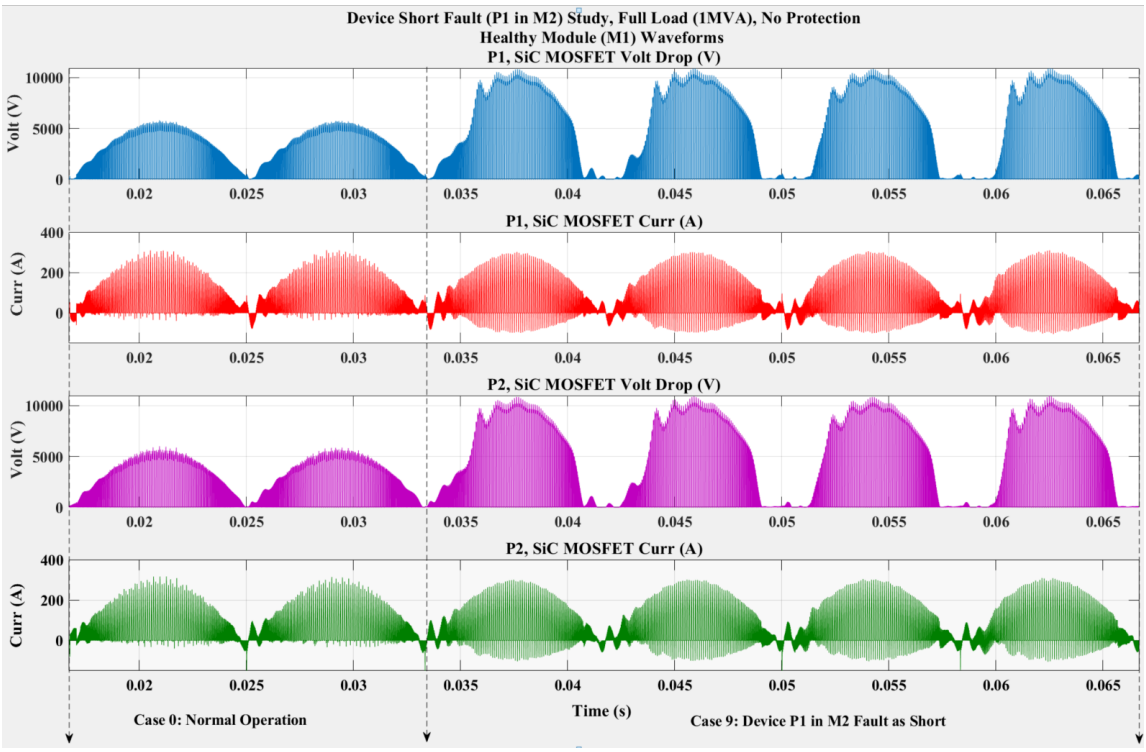


Fig. 6.15 Healthy Module (M1) Device Volt & Curr When Device Fault as Short (No Protection), Full Load

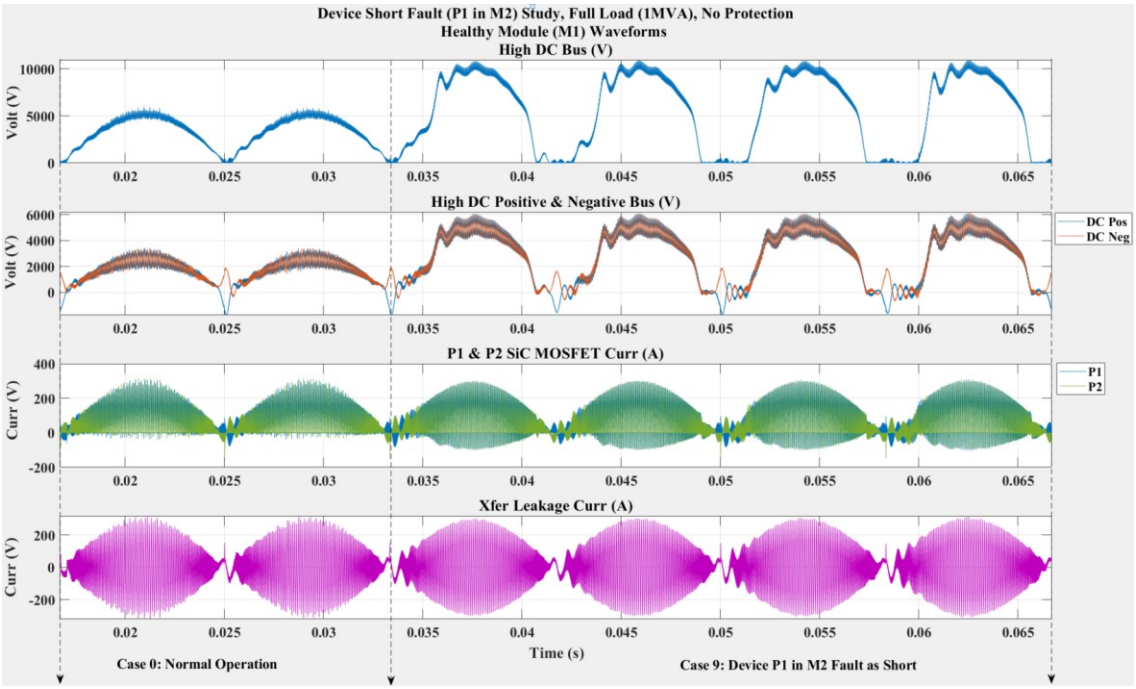


Fig. 6.16 Healthy Module (M1) High DC Bus and Resonant Curr When Device Fault as Short (No Protection), Full Load

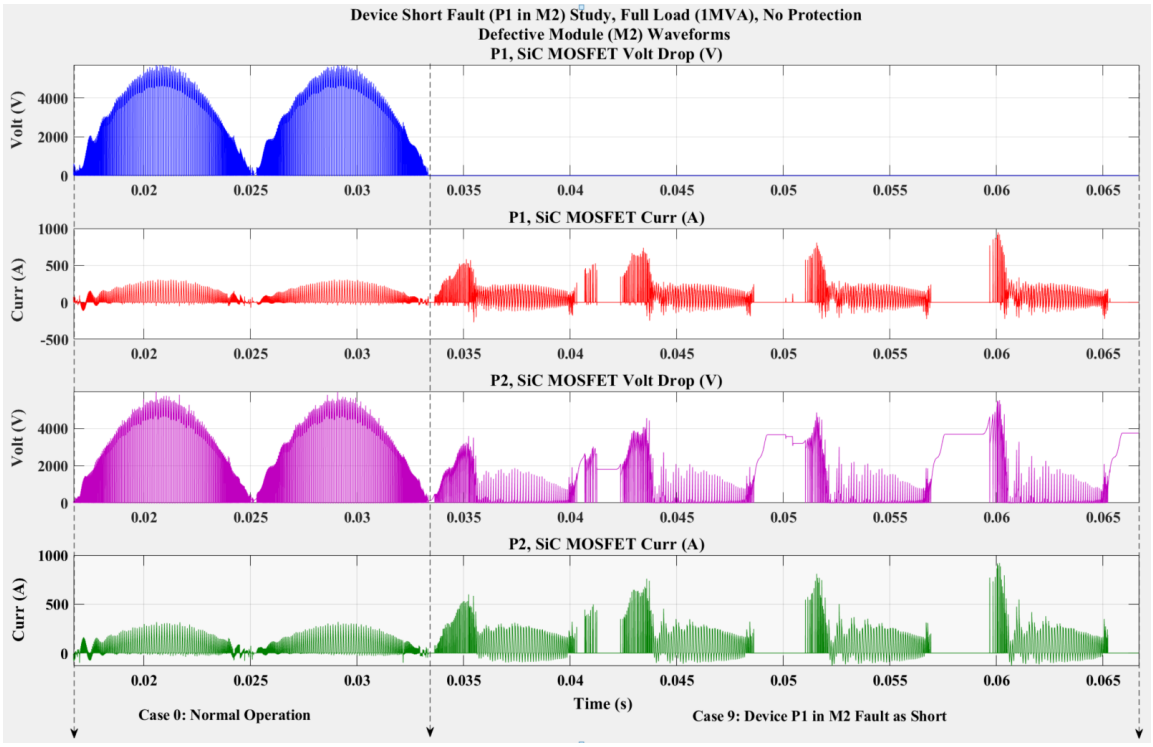


Fig. 6.17 Defective Module (M2) Device Volt & Curr When Device Fault as Short (No Protection), Full Load

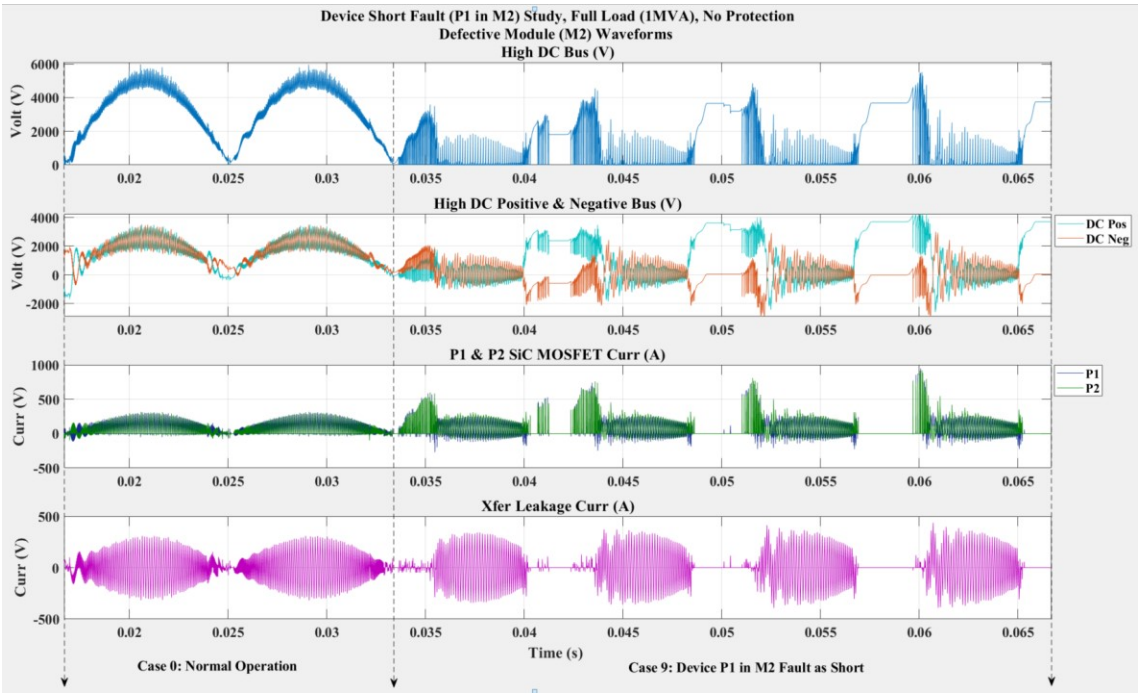


Fig. 6.18 Defective Module (M2) High DC Bus and Resonant Curr When Device Fault as Short (No Protection), Full Load

Per fig. 6.19, the faulted P1 device creates a short circuit path including the high DC bus (Ch) when P2 device is closed. The worst-case scenario is to have a huge short circuit current flowing through the high DC bus and two SiC MOSFETs. Thereby, the high DC bus gets collapses in the defective module, M2. For each module, the high DC bus and input grid voltage have the same RMS value by ignoring the voltage drop across the front-end diode rectifier. Given the fact that the high DC bus in M2 gets collapses, its input grid voltage is also affected. Inside of phase A, M1 and M2 share the input voltage evenly with developed inter-module control mechanism before the fault. After the fault, the system losses the capability to balance the power between the sub-module M1 and M2. As a result, the M2 has tiny voltage input left and M1 almost sees the whole AC grid input. Furthermore, in the proposed topology, the voltage drop is positively proportional to the amount of power transfer. The healthy module, M1, has the most power transferred. The defective module, M2, has been isolated automatically. There is no effect on the DC output load. However, it does not mean the protection is not necessary since the existence of the M2 creates lots of the current harmonics to the grid. In another word, it needs to be bypassed as soon as possible. The defective module can be cut off by closing the line breaker and open the load breaker.

Similar to the single module topology, the device short fault can be protected by the classic desaturation function. Desaturation function is used to detect power transistor short circuit scenario and takes protective measures to prevent power transistors from EOS damages. By adding the desaturation logic, once the protection logics detects the existence of overcurrent, all the gating firing are removed immediately. Then, the defective module is removed by controlling both line and load breakers. The healthy module takes the power transfer task which was assigned to the defective module. In this case, the total amount of power transferred by M1 increases from 50% to 100% phase load. The system can continue operating without being affected by this fault. For comparison purpose, the system waveforms are shown before and after the fault when the desaturation protection is activated.

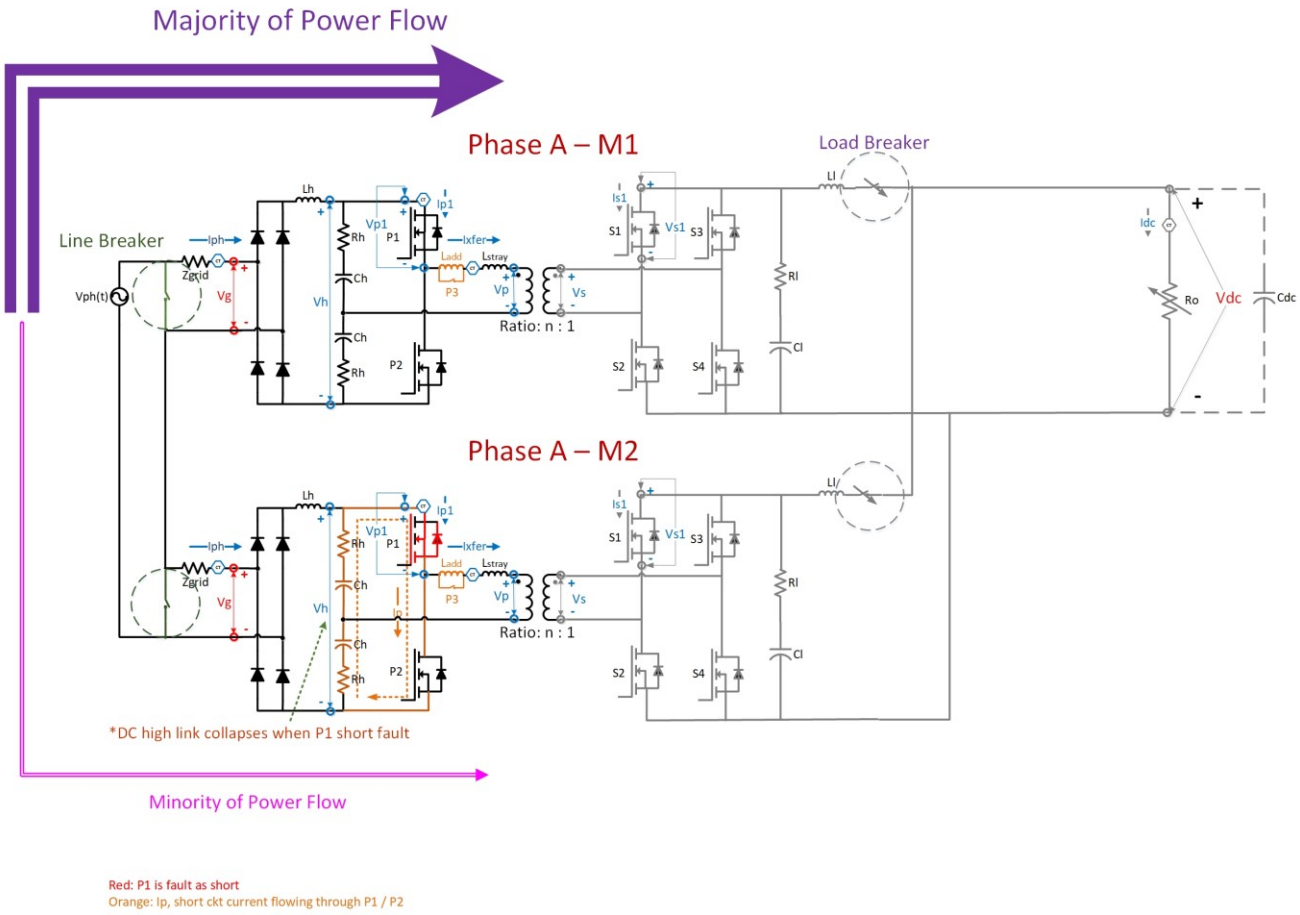


Fig. 6.19 Equivalent Circuit When Device (P1 in M2) Fault as Short

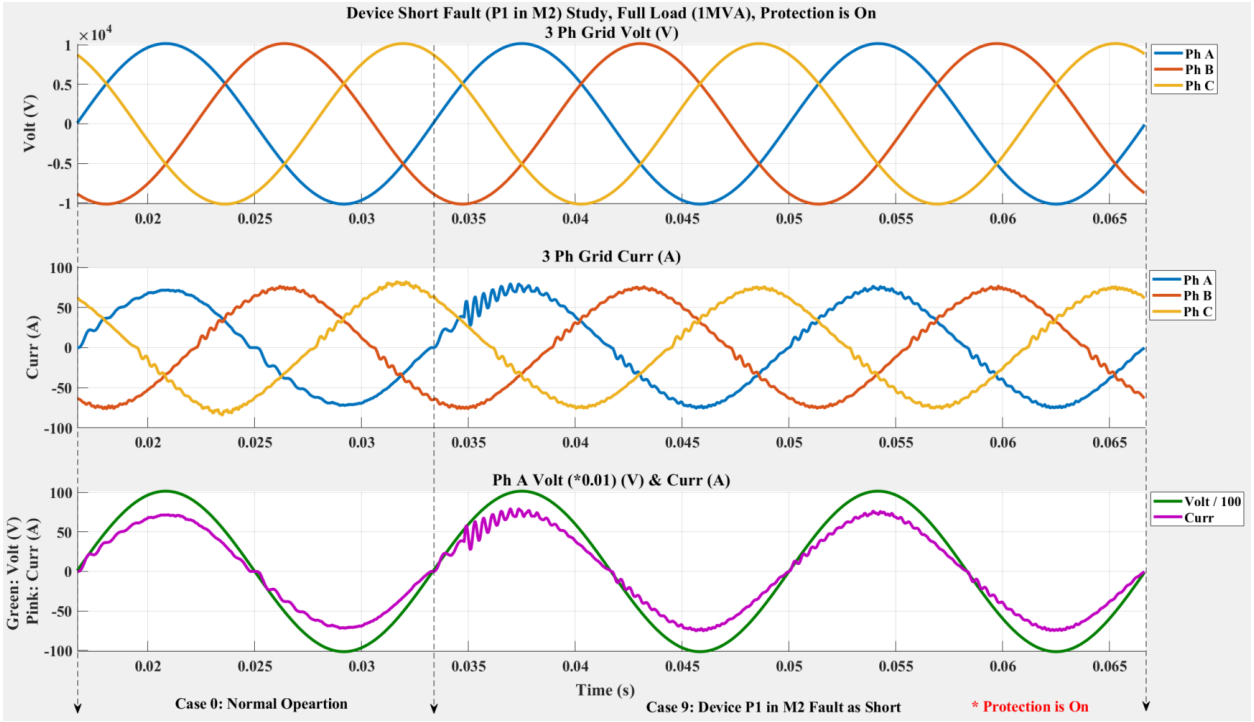


Fig. 6.20 AC Input When Device Fault as Short (With Protection On), Full Load

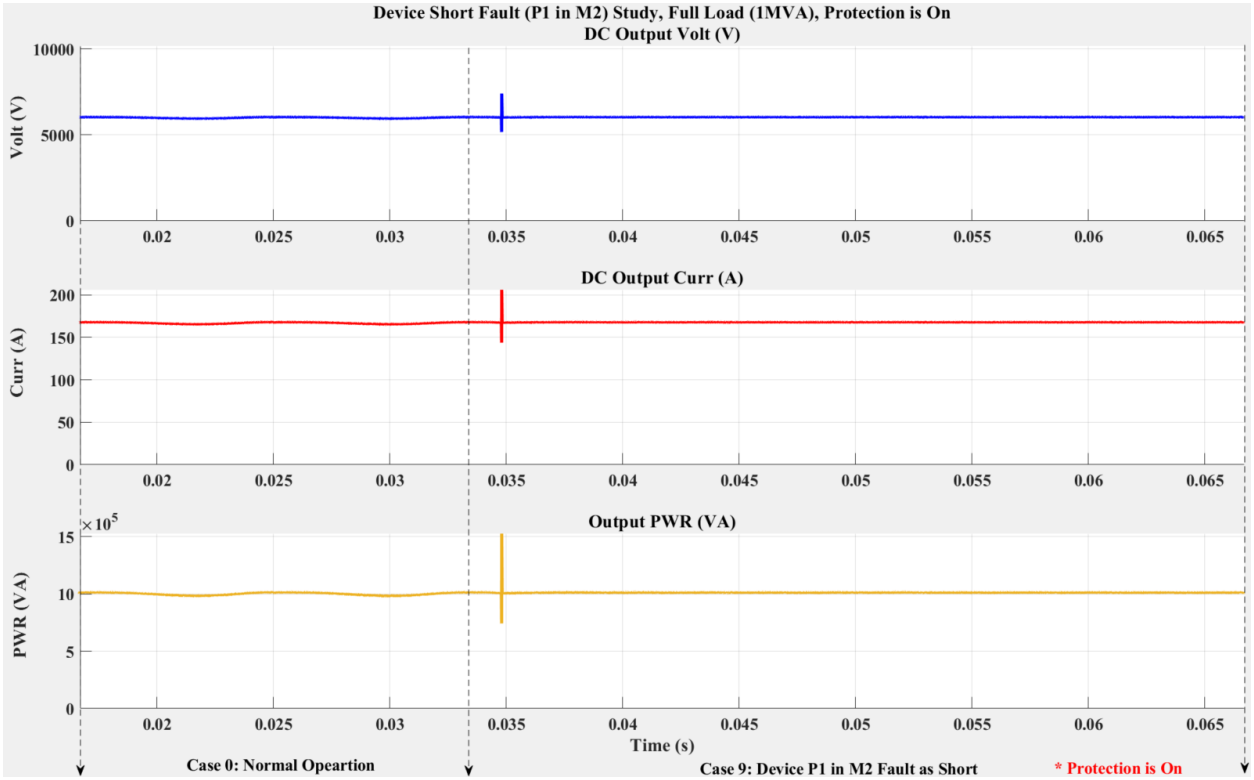


Fig. 6.21 DC Output When Device Fault as Short (With Protection On), Full Load

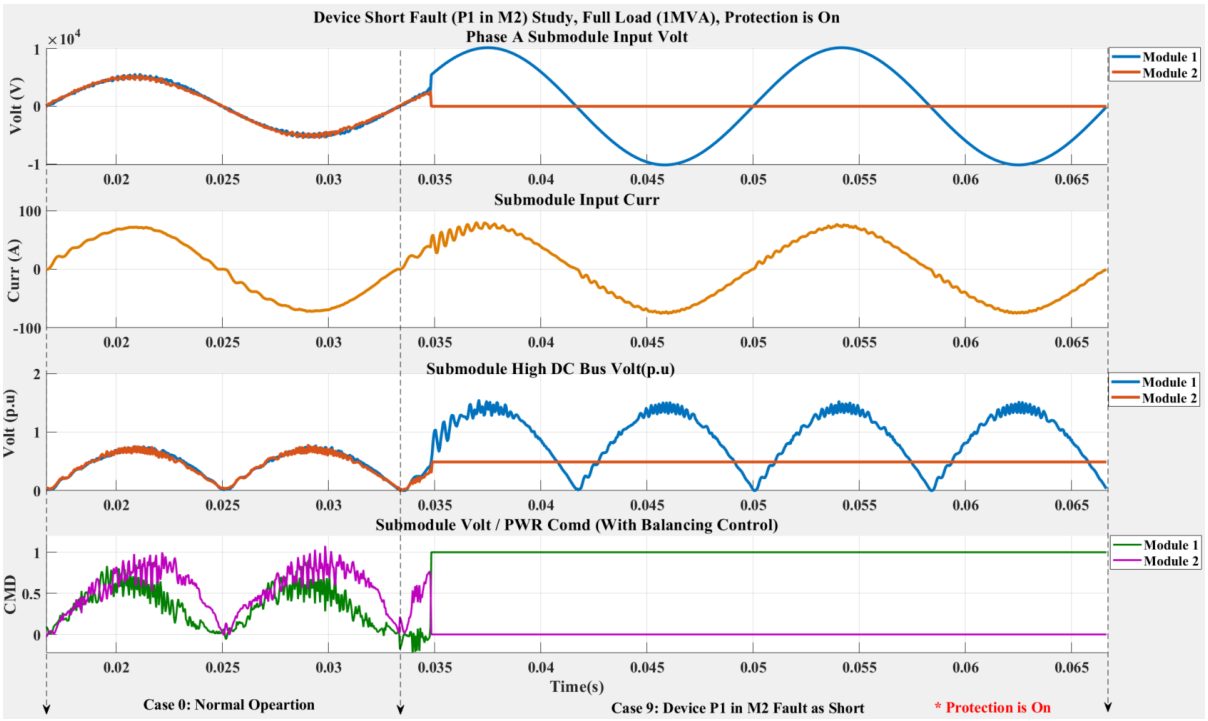


Fig. 6.22 Sub-module Waveforms When Device Fault as Short (With Protection On), Full Load

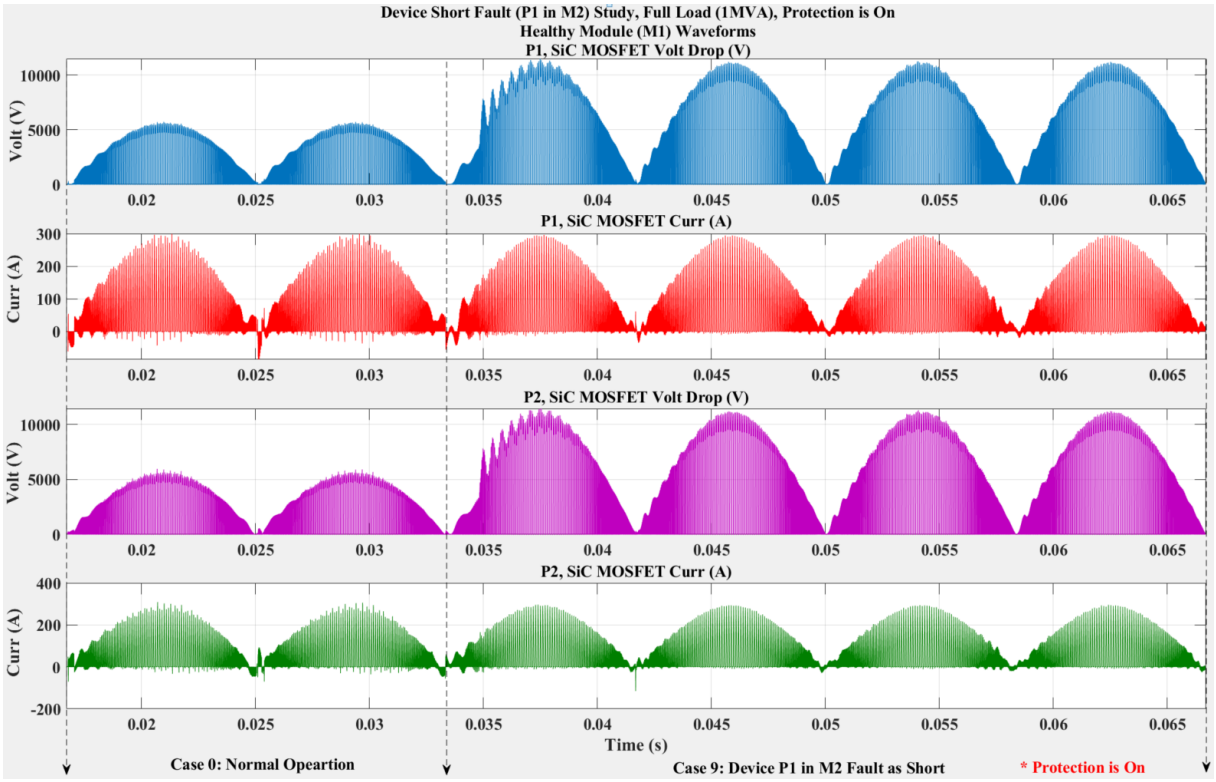


Fig. 6.23 Healthy Module (M1) Device Volt & Curr When Device Fault as Short (With Protection On), Full Load

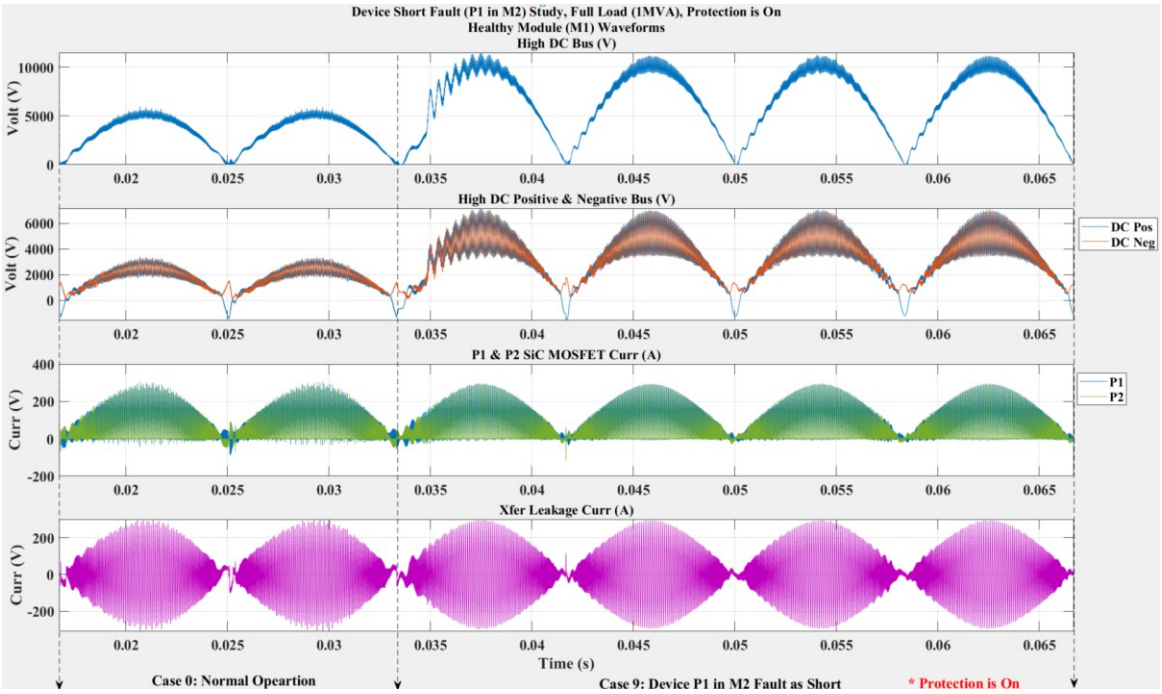


Fig. 6.24 Healthy Module (M1) High DC Bus and Resonant Curr When Device Fault as Short (With Protection On), Full Load

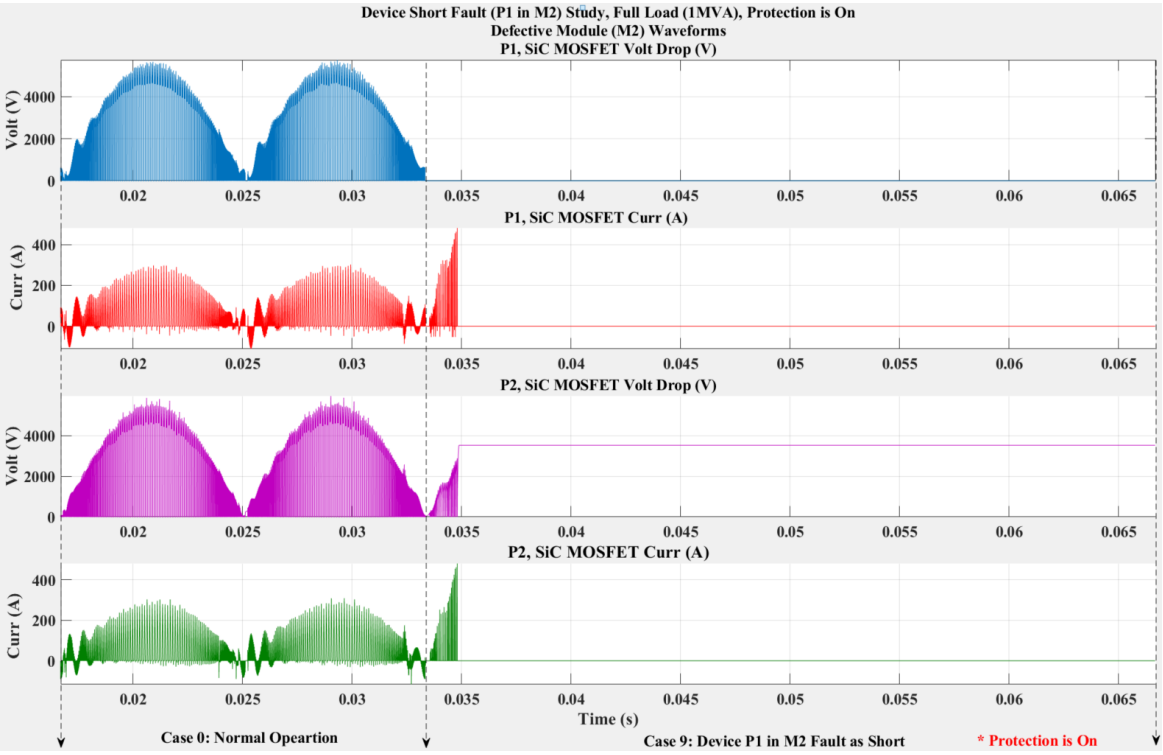


Fig. 6.25 Defective Module (M2) Device Volt & Curr When Device Fault as Short (With Protection On), Full Load

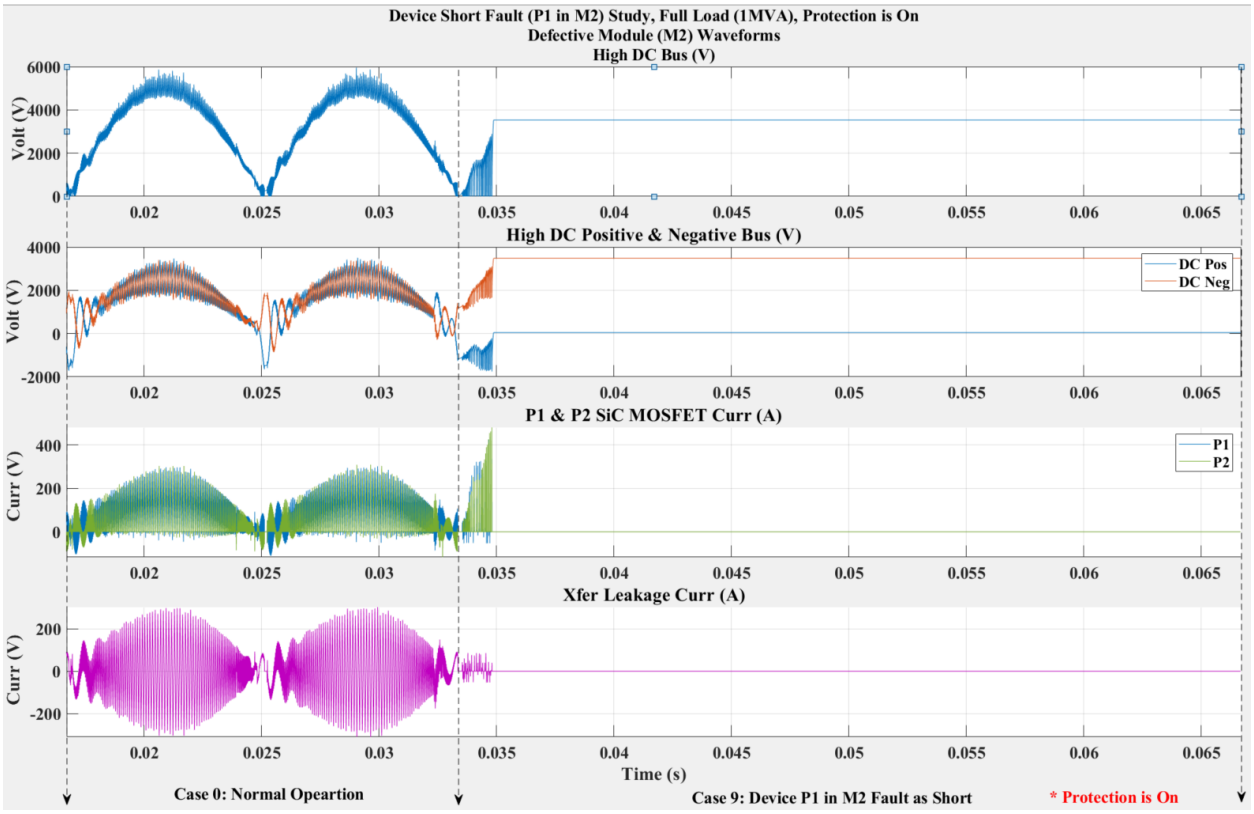


Fig. 6.26 Defective Module (M2) High DC Bus and Resonant Curr When Device Fault as Short (With Protection On), Full Load

Thanks to the device desaturation protection scheme, the device short fault is quickly detected. The protection logic can further locate the damaged semiconductor module. To recover the system from this type of failure, the defective DAB module is bypassed by closing the line breaker and opening the load breaker. Therefore, the healthy module doubles the total power transfer and the overall system gets back to the normal operating condition.

6.3.2 Device Short as Open Fault Study in Modular Structure (Case 10)

Next, the focus shifts to another typical semiconductor module fault, which is device open fault. In some cases, the device open fault can always be treated as the overheat failure. The thermal energy gets accumulated inside of the module package in the switching or conducting modes. Assume this energy is not dissipated quickly, the device is likely exploded, and the outer package is cracked. The system behaviors when this kind of fault happens are shown as below.

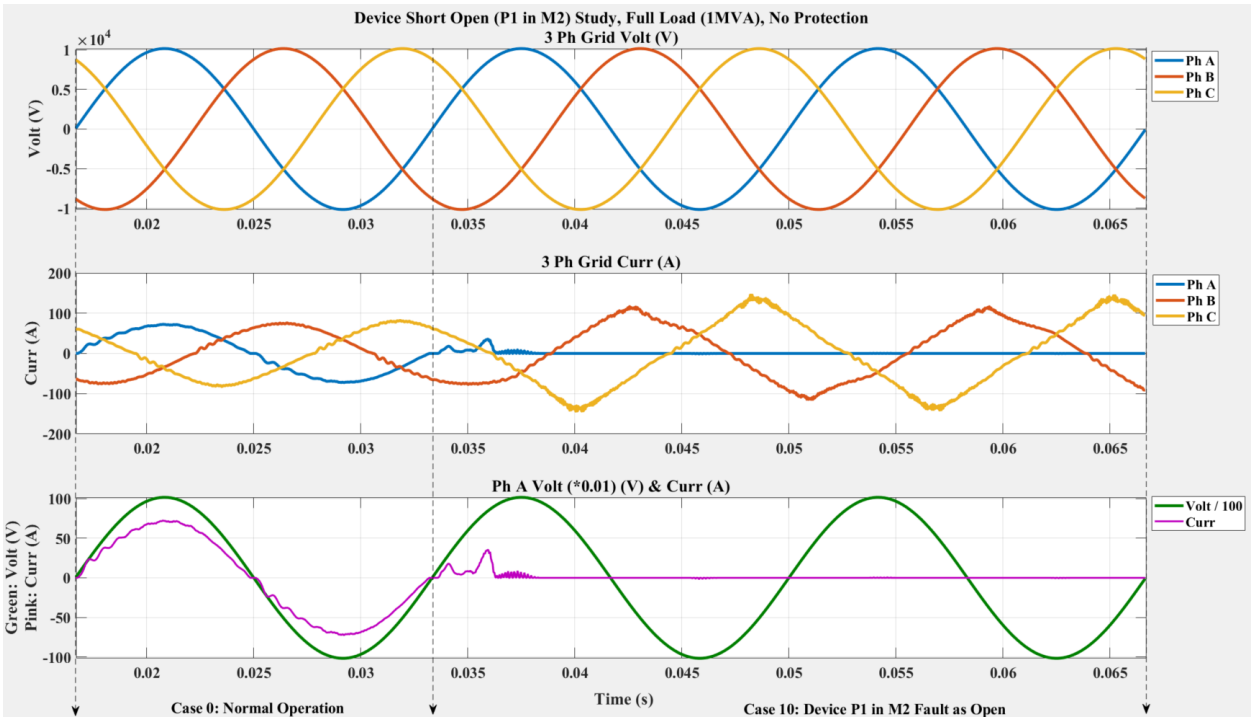


Fig. 6.27 AC Input When Device Fault as Open (No Protection), Full Load

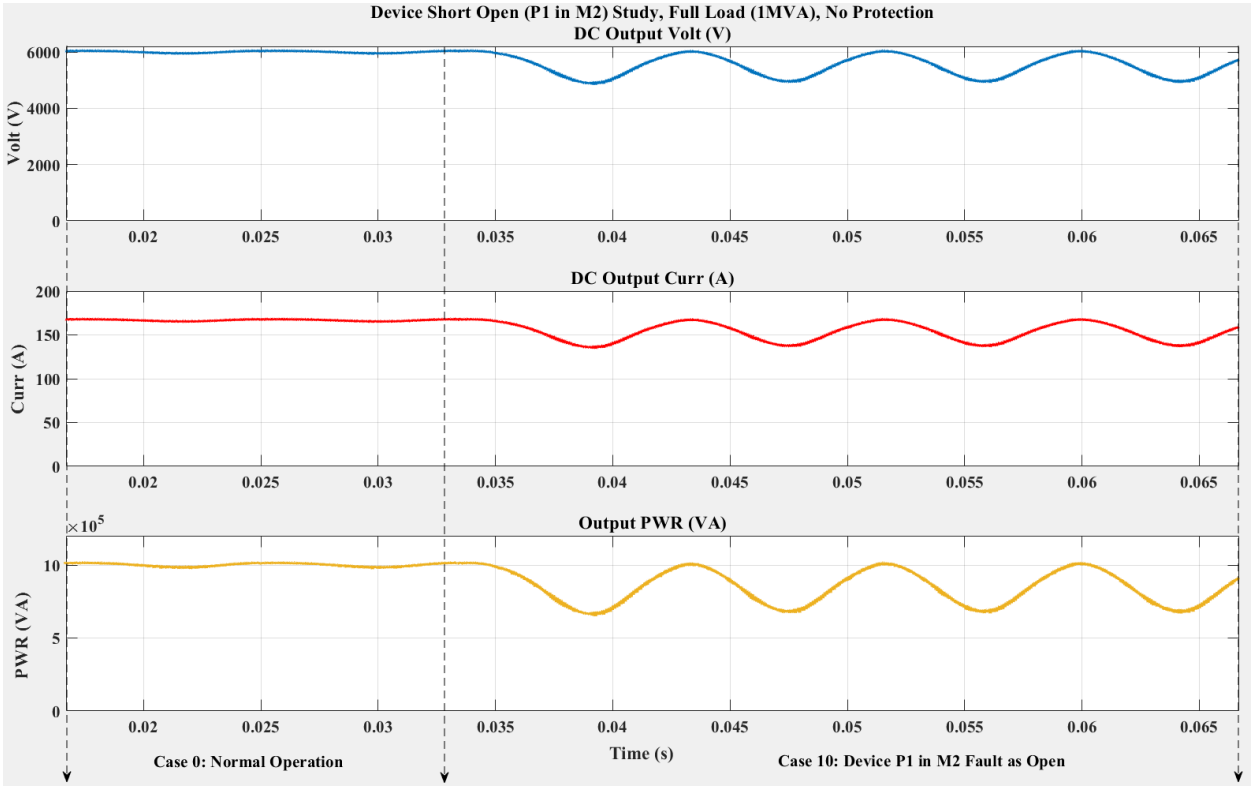


Fig. 6.28 DC Output When Device Fault as Open (No Protection), Full Load

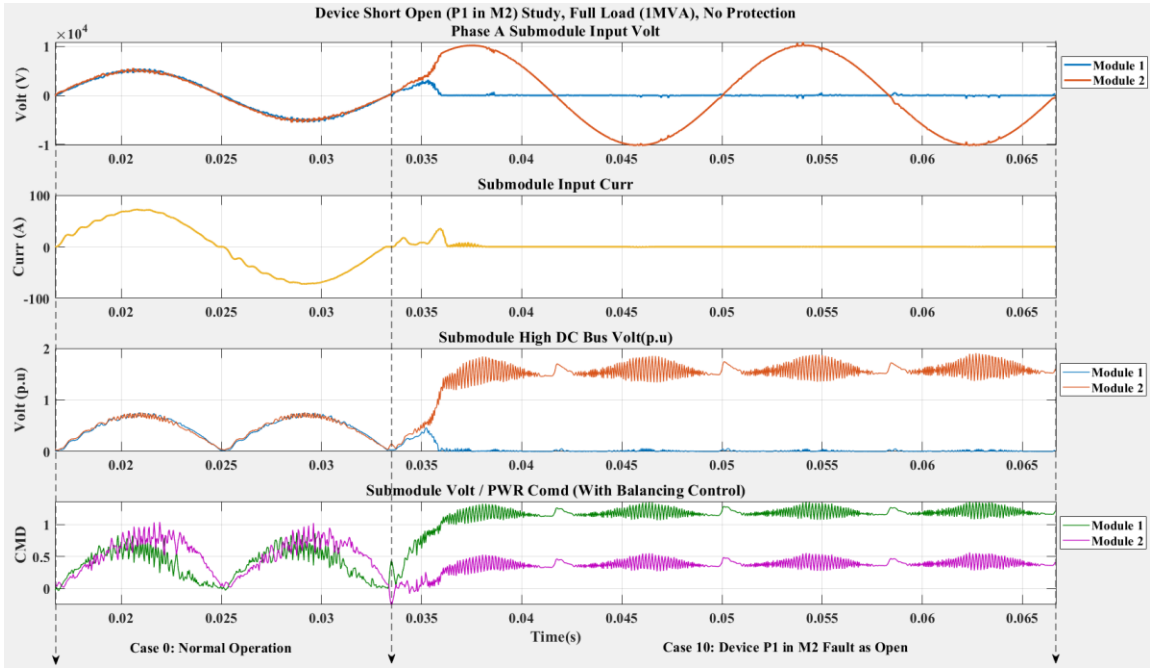


Fig. 6.29 Sub-module Waveforms When Device Fault as Open (No Protection), Full Load

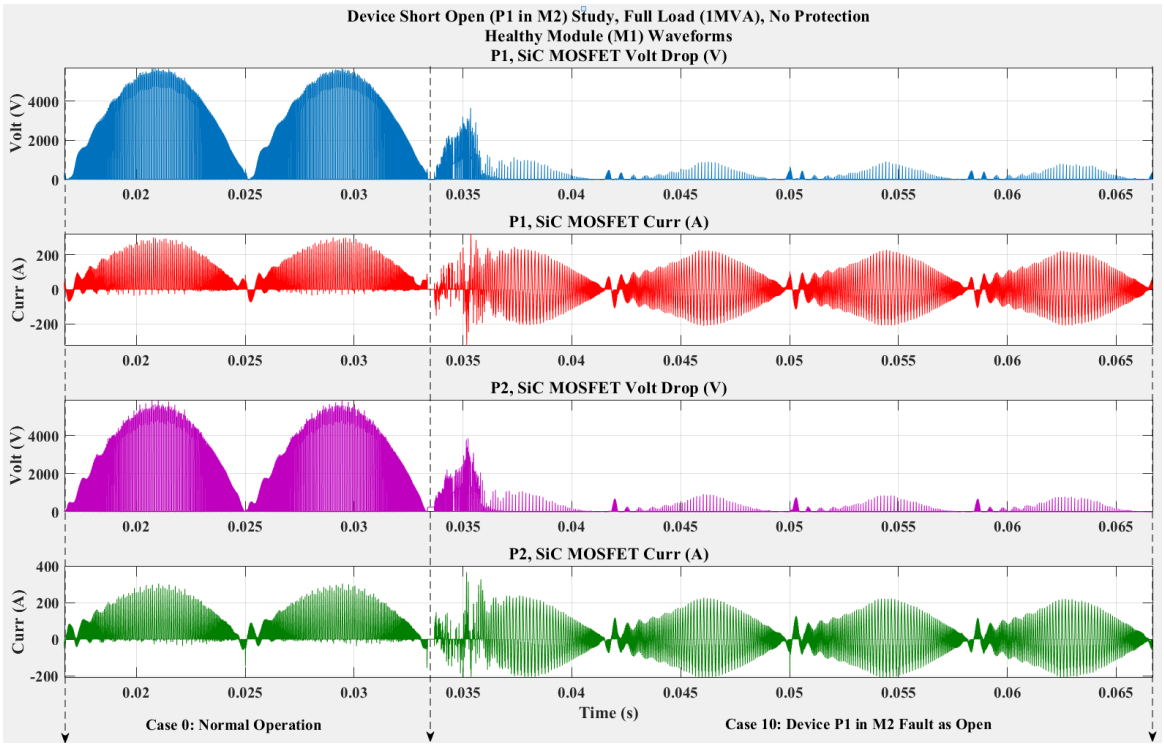


Fig. 6.30 Healthy Module (M1) Device Volt & Curr When Device Fault as Open (No Protection), Full Load

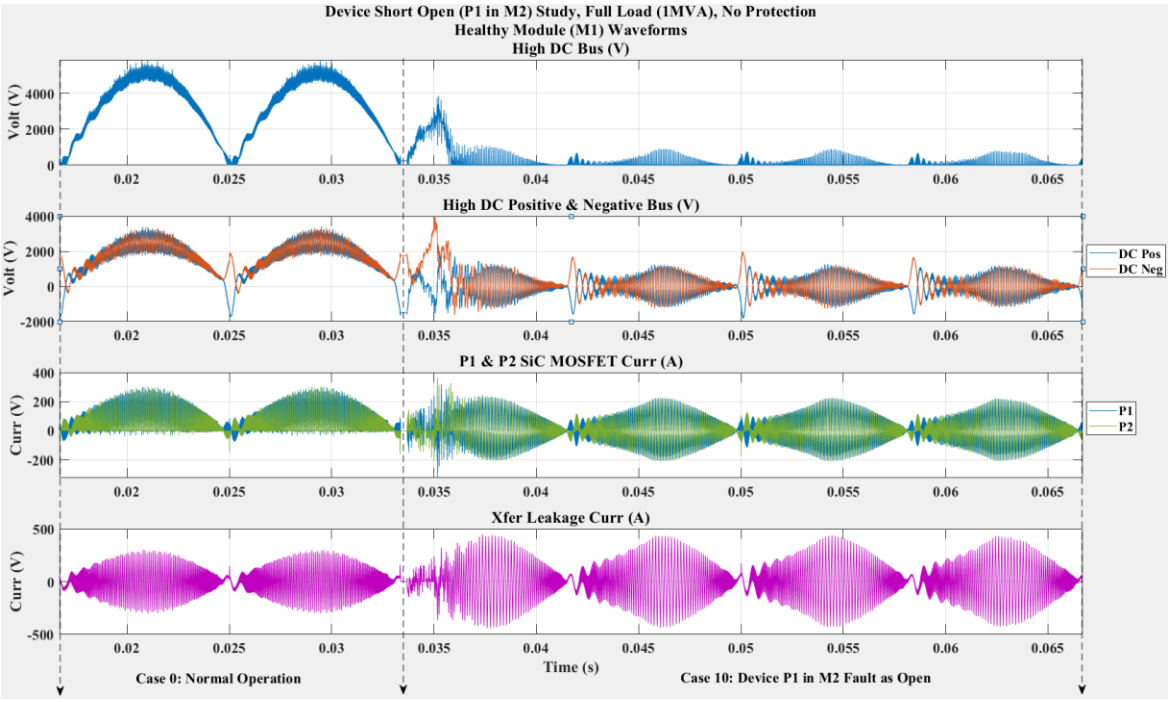


Fig. 6.31 Healthy Module (M1) High DC Bus and Resonant Curr When Device Fault as Open (No Protection), Full Load

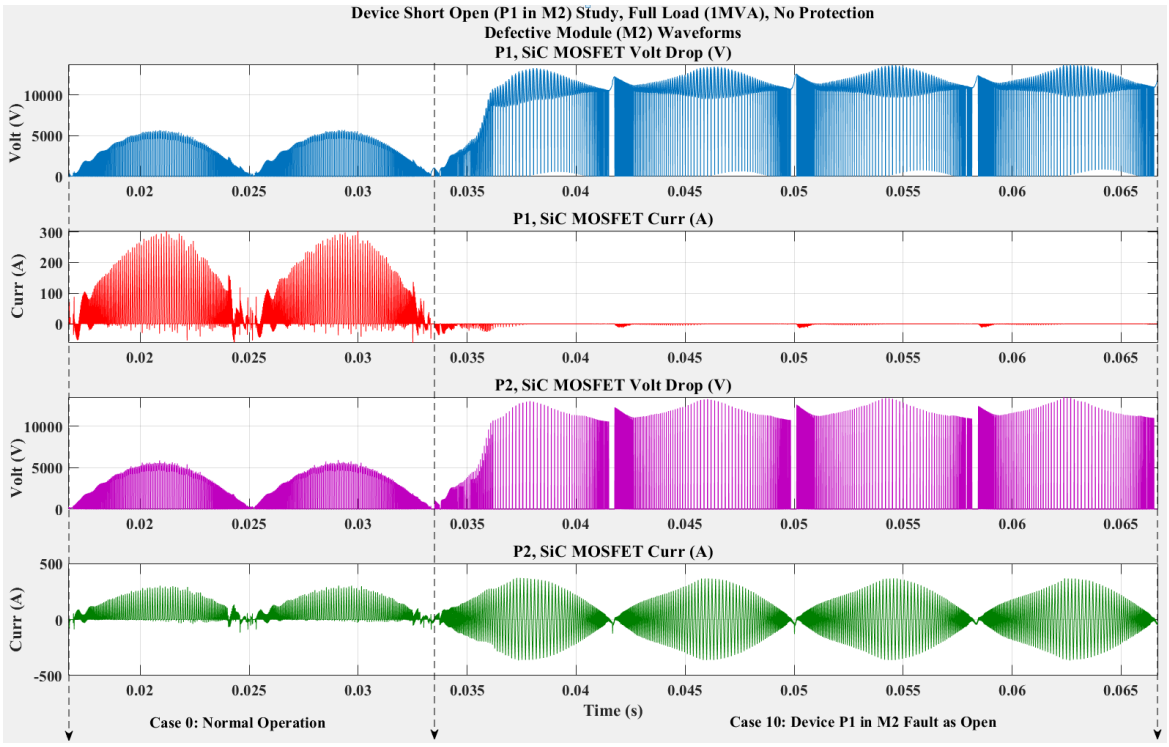


Fig. 6.32 Defective Module (M2) Device Volt & Curr When Device Fault as Open (No Protection), Full Load

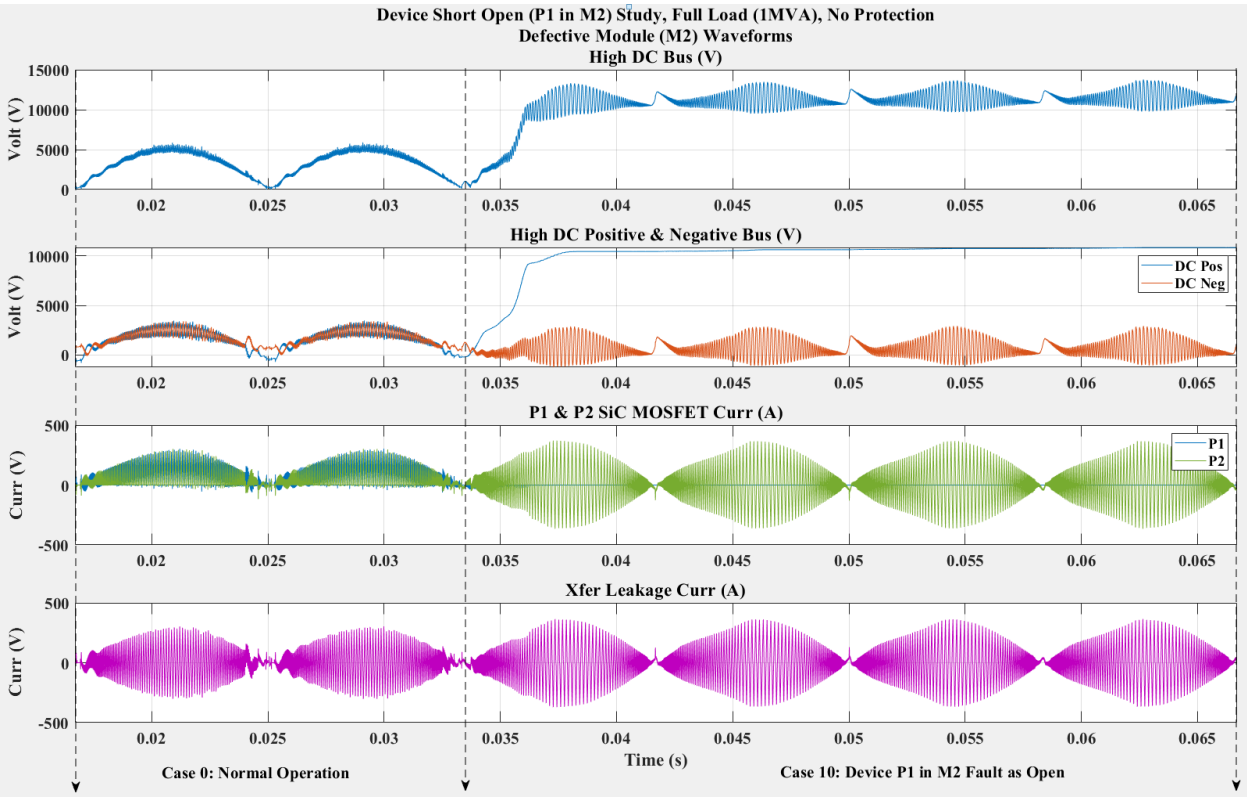


Fig. 6.33 Defective Module (M2) High DC Bus and Resonant Curr When Device Fault as Open (No Protection), Full Load

Per fig. 6.34, the faulted P1 device creates an open circuit including the high DC bus (Ch). Therefore, the energy charged in the high DC link bus never has change to be transferred to the load. The total DC bus jumps from half to nearly the full input voltage. Given the conclusion that high DC bus level equals to the total amount of power transfer, the faulted DAB module has to transfer almost double power flow which even worsen the condition. Based on the circuitry analysis, the faulted module creates a high-power impedance path which almost blocks the power transfer in the phase A. The external DC output feedback loop has to increase the power command for other two phases which creates the grid current unbalancing issue. Talking about DC output, the waveforms are oscillated and under the rated value because both phase B and C hit the power transfer limit.

Similar to fault case 6, the protection scheme is the device over-voltage protection residing on the gate driver. The SiC module witness as much as half DC link voltage under normal condition. However, the voltage drop across the device increases almost twice when there is open device

fault. Once the device voltage stress is over the threshold value, the protection scheme is activated and removes the defective DAB module from the phase A by controlling both line and load breakers. The following figures are the system waveforms before and after the fault when the over-voltage protection is enabled.

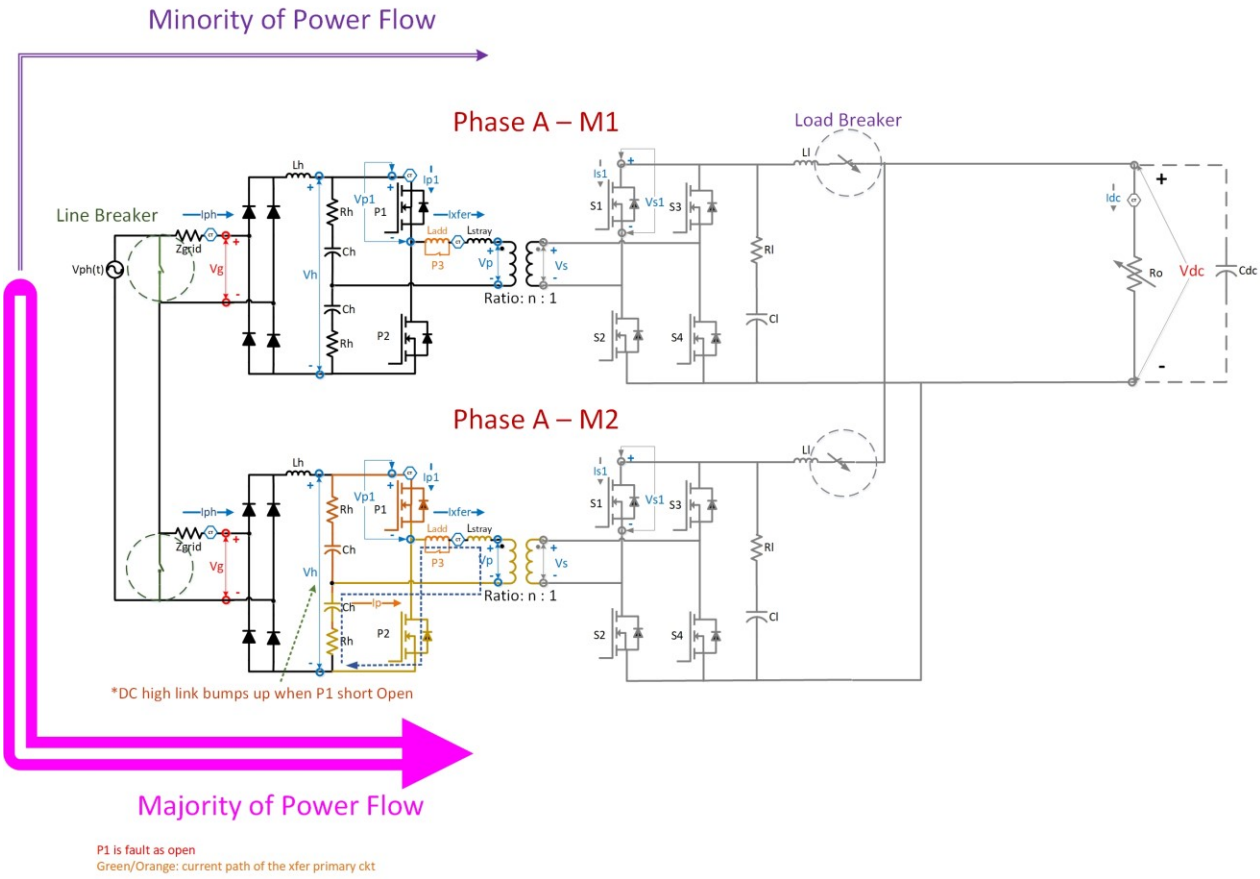


Fig. 6.34 Equivalent Circuit When Device (P1 in M2) Fault as Open

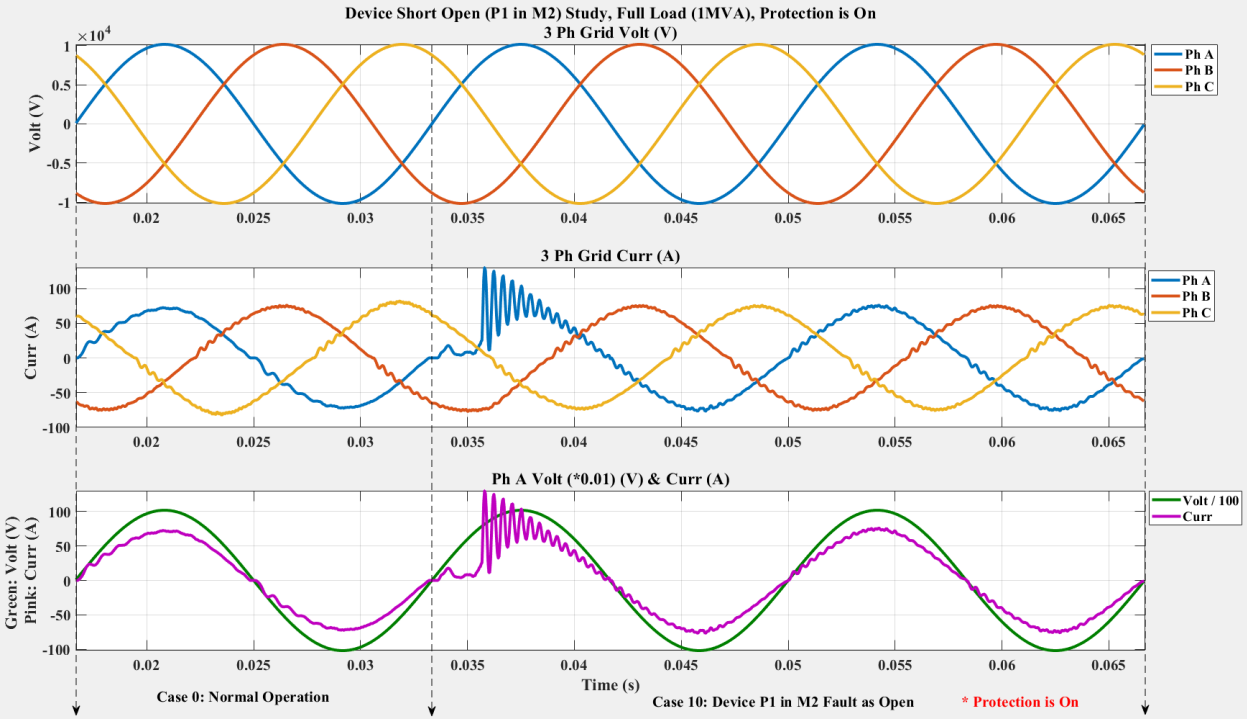


Fig. 6.35 AC Input When Device Fault as Open (With Protection On), Full Load

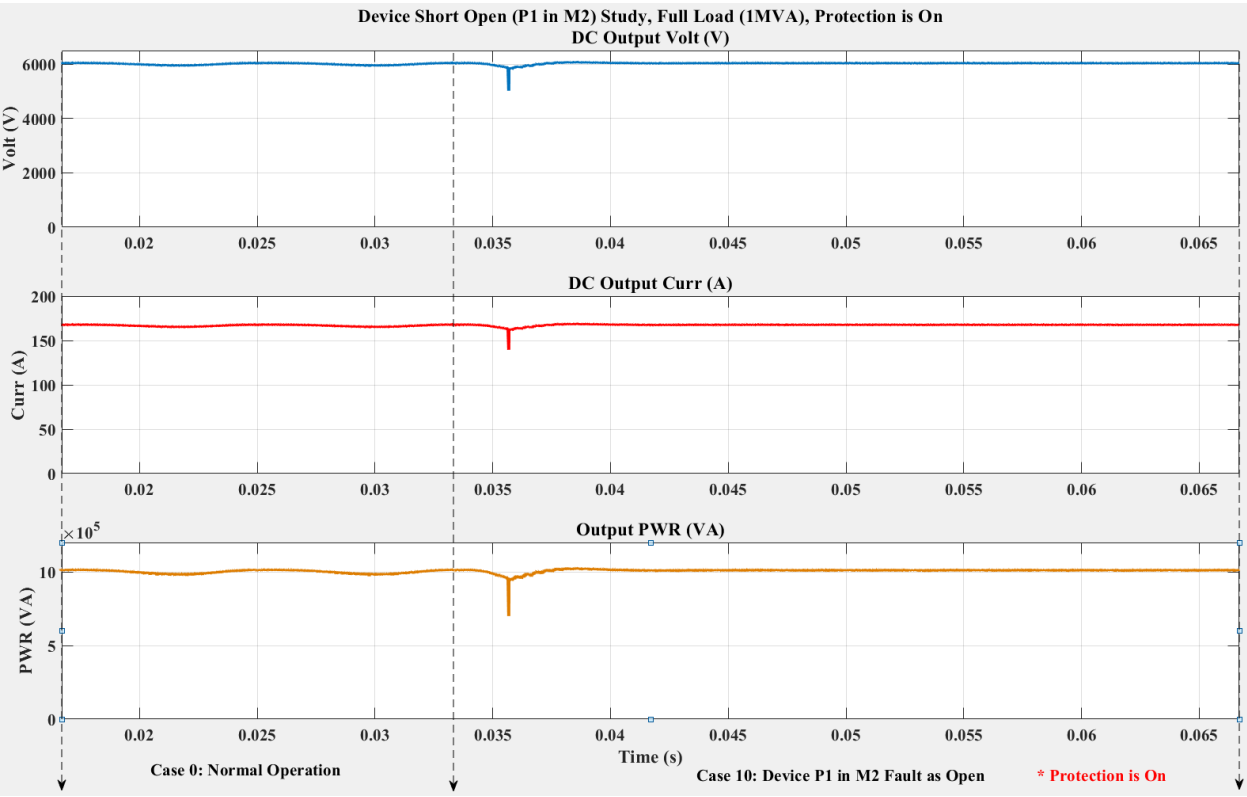


Fig. 6.36 DC Output When Device Fault as Open (With Protection On), Full Load

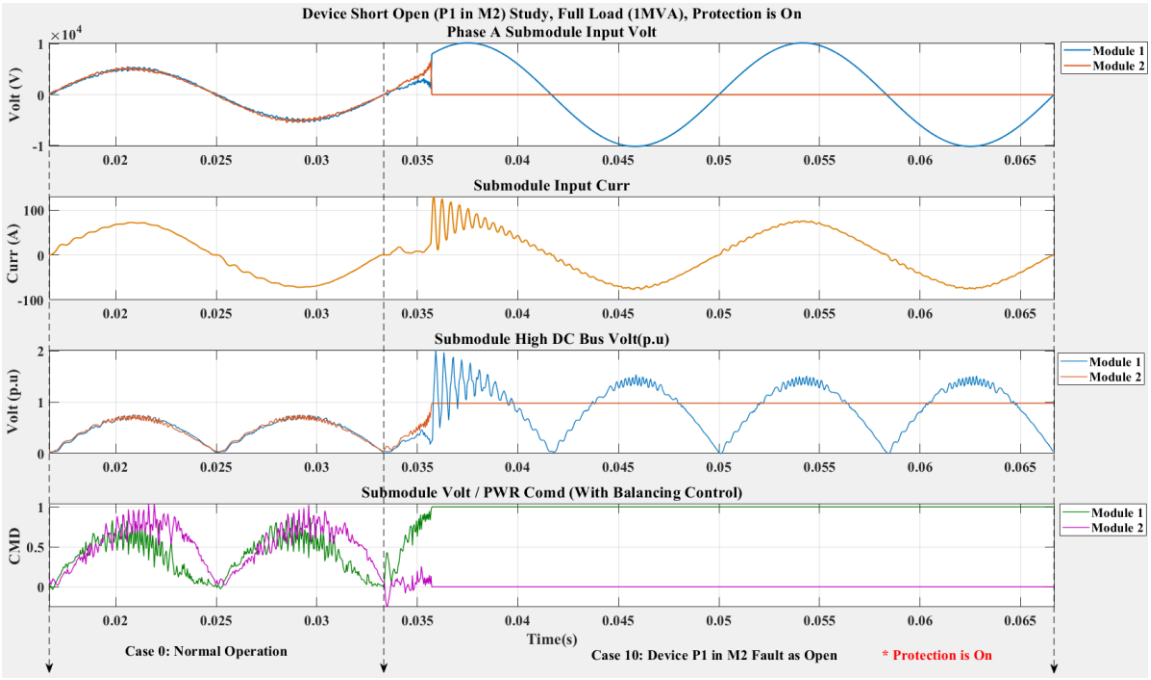


Fig. 6.37 Sub-module Waveforms When Device Fault as Open (With Protection On), Full Load

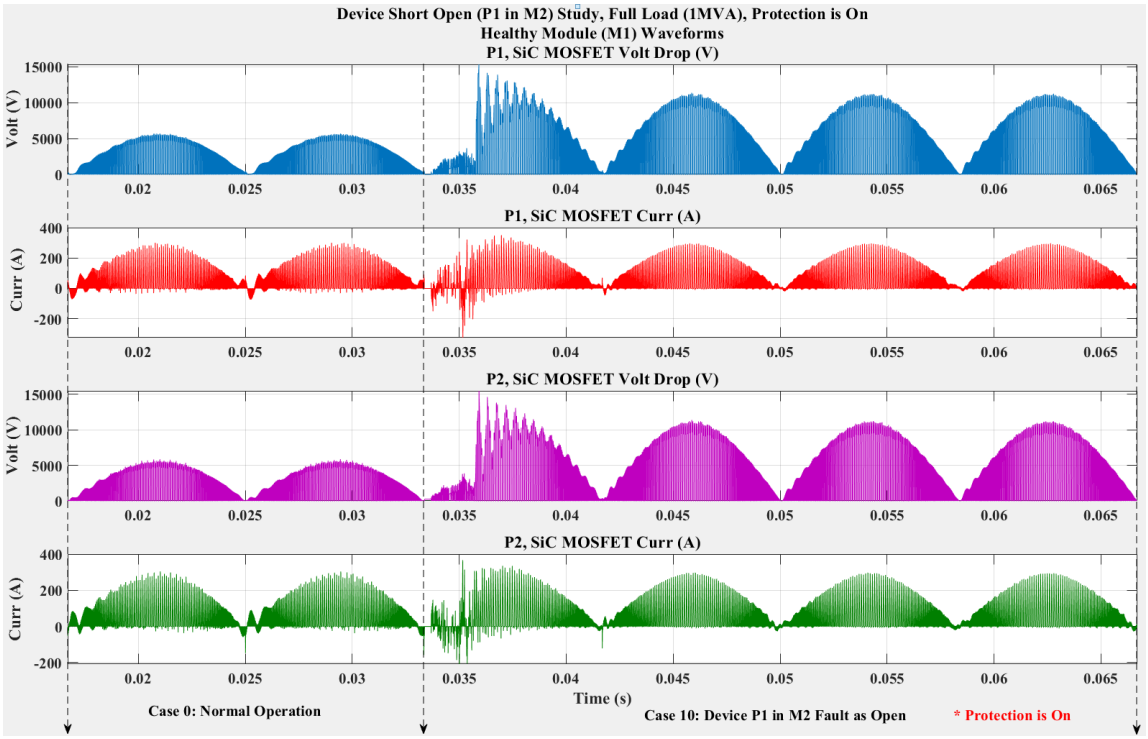


Fig. 6.38 Healthy Module (M1) Device Volt & Curr When Device Fault as Open (With Protection On), Full Load

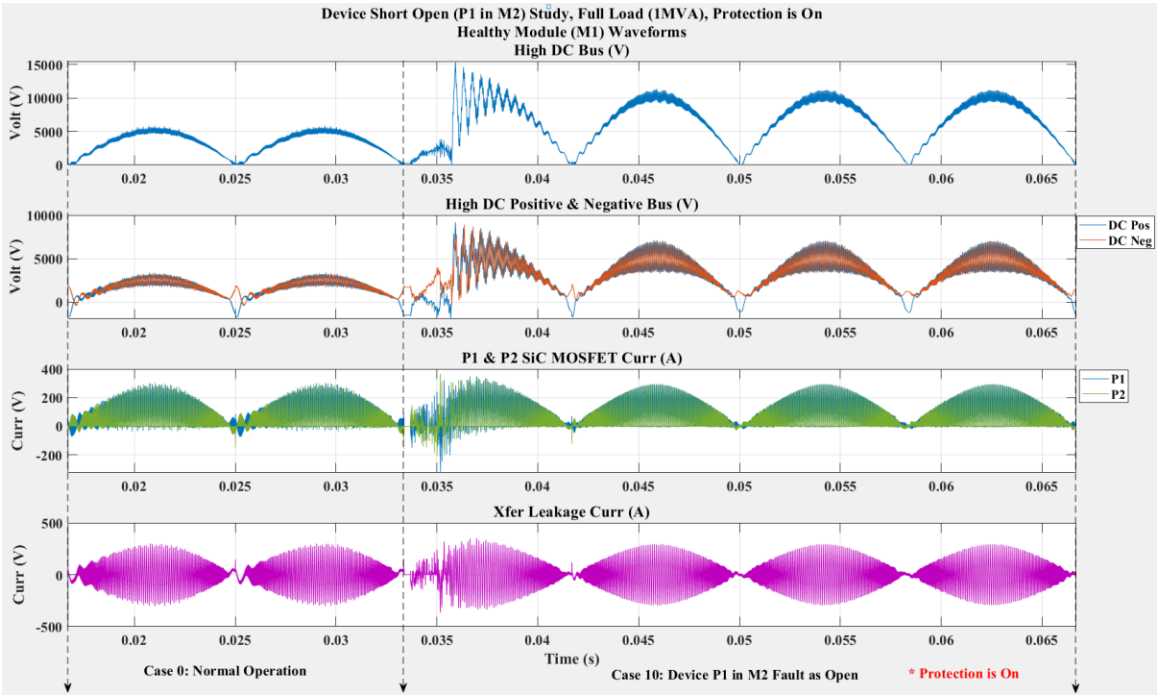


Fig. 6.39 Healthy Module (M1) High DC Bus and Resonant Curr When Device Fault as Open (With Protection On), Full Load

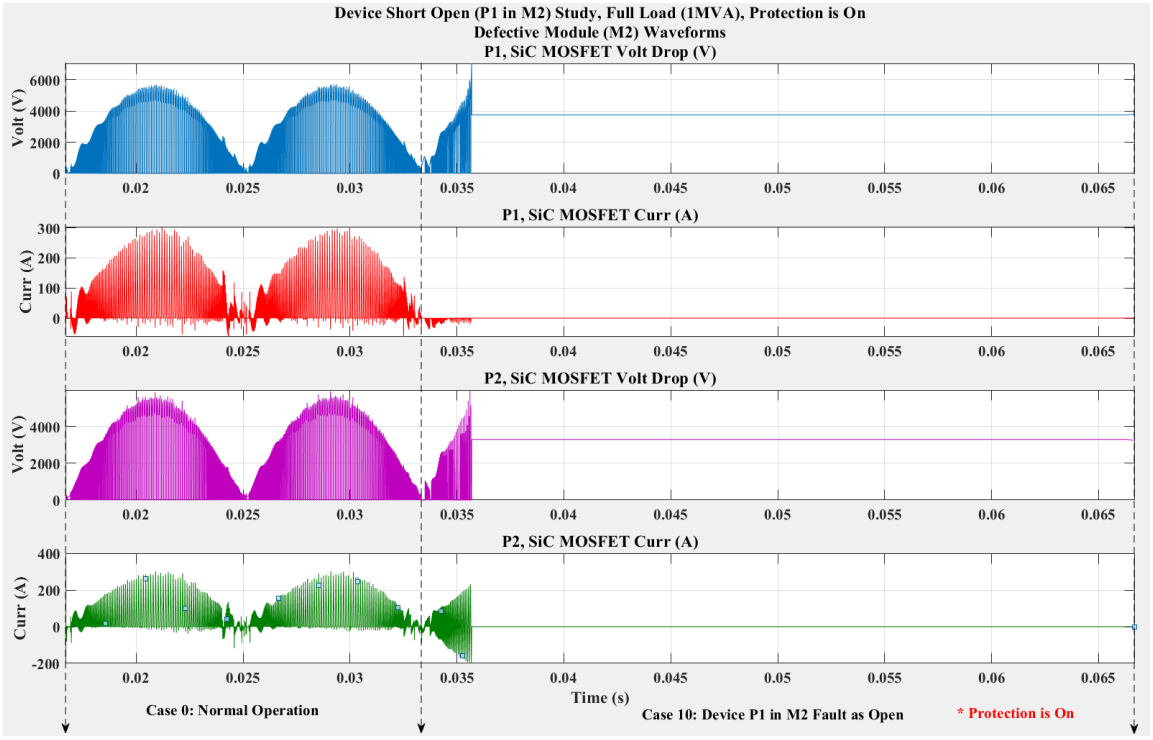


Fig. 6.40 Defective Module (M2) Device Volt & Curr When Device Fault as Open (With Protection On), Full Load

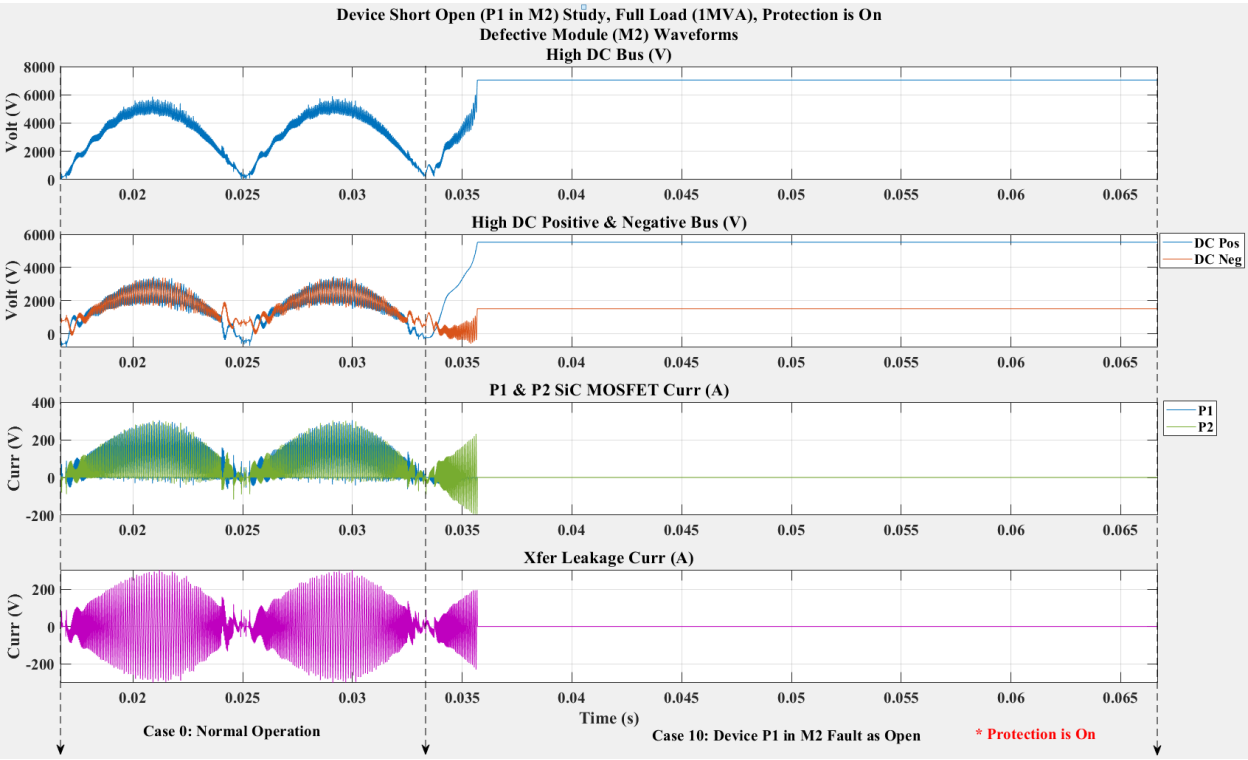


Fig. 6.41 Defective Module (M2) High DC Bus and Resonant Curr When Device Fault as Open (With Protection On), Full Load

Above figures demonstrate the functionality of the protection scheme for the fault case 10. The strategy is to locate the defective device and isolate its DAB module from the rest of the circuit as quick as possible. In the meanwhile, the control scheme reassigns and rebalances the power transfer between healthy modules to make sure no negative influence on both DC output and AC input. In the study, the system is recovered from the fault and get back to the normal operating condition within less than half line cycle.

6.4 Conclusions

This chapter investigates the modular SiC MV isolated three-phase PFC rectifier. A common issue in any modular converters is about the module hardware difference. This difference causes the power and voltage unbalancing between the modules. A novel inter-module balance control is proposed to balance the power distribution with the hardware difference existence. The power difference between modules is improved from 6% to less than 1% at both half and full load conditions. Furthermore, the system operating redundancy is proved through the device fault studies. The developed protection scheme accurately locates the damaged components and

bypasses the overall DAB power module by controlling both line and load breakers. The response time is less than half line cycle and system is fully recovered from the device fault.

7 Conclusions and Summary of Contribution

A novel three-phase SiC MV isolated three-phase power factor correction (PFC) rectifier is first introduced to the MV variable frequency drive (MV-VFD) systems. Compared with traditional MMCC and IMC topologies, the proposed topology not only meets all the fundamental operating requirements, but also brings some advanced features. The one is of the PFC which eliminates the reactive power consumption and lowers the operational cost. Another one is of zero-voltage switching (ZVS) which reduces the semiconductor switching loss, therefore improves the system efficiency.

The SiC MV PFC rectifier puts some challenges on the semiconductor module in related to the switching frequency and voltage rating, which makes the traditional Si IGBT not suitable. A novel SiC MOSFET module, rated at 12.5 kV, 375 A, is developed. The SiC die dimension, the module internal layout and packaging, the thermal loss model are investigated accordingly. Then, the device power loss model is implemented and evaluated in the system-level study.

Next, a system control scheme is developed including both feedforward modulation technique and DC output feedback control loop. As the inter control loop, the modulator consists of peripheral circuits, logic machine and PWM generator to achieve nine functions. The outer DC bus regulator keeps regulating the DC output as the rated level to coordinate with real-time load condition. Then, an application state machine, including I/O management, soft start-up procedure and protection scheme, is designed as an additional layer. A case study illustrates its validation and shows how to charge the DC output bus from zero to full energy safely. In the meanwhile, the inrush current is effectively mitigated. In addition, the system steady state performance is demonstrated under different loads. Moreover, the system long-term operating reliability is evaluated through the system fault ride through (FRT) and protection scheme study. First one is to verify the system noise immunity to the grid power fluctuation. Second one is to develop a protection scheme under different fault conditions.

From the previous study, a problem gets author's attention. That is the large grid current distortion at the ultra-light condition. In order to overcome this issue, the topology is improved to include the additional hardware. The theory is to smooth out the current ripple by increasing the damping

coefficient of the mid-stage DAB circuit. The case study proves the validity and practicality of the proposed topology.

As an alternative design approach, the modular dual active bridge (DAB) PFC three-phase rectifier is proposed and investigated. One of the biggest challenges in the modular structure is the power and voltage unbalance brought by the hardware difference. This problem is resolved by employing a novel inter-module balance control strategy. The power unbalance is reduced to less than 1% at either half or full load. Furthermore, a dedicated system protection scheme is developed to identify and remove the damaged power module from the rest of the system, then recover the system from the fault within less than half line cycle. This protection logic verifies the redundancy feature inherited in the modular topologies.

8 Future Work

One task is to prototype the overall power circuit and standardize the module design. The high frequency hardware implementation requires some design efforts. Besides, the noise immunity and susceptibility of both power circuit and control system need to be carefully evaluated per IEC 61000-4-2 (Electrostatic discharge immunity test), IEC 61000-4-3 (Radiated, radio-frequency, electromagnetic field immunity test), IEC 61000-4-4 (Electrical fast transient/burst immunity test), IEC 61000-4-5 (Surge immunity test), IEC 61000-4-6 (Immunity to conducted disturbances, induced by radio-frequency fields), IEC 61000-4-8 (Power frequency magnetic field immunity test), IEC 61000-4-11 (Voltage dips, short interruptions and voltage variations immunity tests), IEC 61000-4-12 (Ring wave immunity test), IEC 61000-4-18 (Damped oscillatory wave immunity test), IEC 61000-4-29 (Voltage dips, short interruptions and voltage variations on DC input power port immunity tests).

Another task is to include more power modules in the system design and further reduce the voltage and power stress on the semiconductor devices. The total system cost can be further reduced by using the low power devices. However, more power modules being added complicates the controller network design. The central controller needs to coordinate with many local controllers by using reliable and timely commutation link.

References

[1] J. Leon, S. Kouro, L. Franquelo, J. Rodr´ıguez, and B. Wu, “The essential role and the continuous evolution of modulation techniques for voltage source inverters in past, present and future power electronics,” *IEEE Trans. Ind. Electron*., vol. 63, no. 5, pp. 2688–2701, May 2016.

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, “Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[3] Markets-and-Markets, “Variable Frequency Drives Market- Global Market Trends & Forecast to 2017,” 2013.

[4] E. Levi, "Multiphase Electric Machines for Variable-Speed Applications," in IEEE Transactions on Industrial Electronics, vol. 55, no. 5, pp. 1893-1909, May 2008.

[5] B. K. Bose, "Power Electronics and Motor Drives Recent Progress and Perspective," in IEEE Transactions on Industrial Electronics, vol. 56, no. 2, pp. 581-588, Feb. 2009.

[6] F. Zare, P. Davari and F. Blaabjerg, "A Modular Active Front-End Rectifier With Electronic Phase Shifting for Harmonic Mitigation in Motor Drive Applications," in IEEE Transactions on Industry Applications, vol. 53, no. 6, pp. 5440-5450, Nov.-Dec. 2017.

[7] Y. S. Kumar and G. Poddar, "Control of Medium-Voltage AC Motor Drive for Wide Speed Range Using Modular Multilevel Converter," in IEEE Transactions on Industrial Electronics, vol. 64, no. 4, pp. 2742-2749, April 2017.

[8] M. Hagiwara, I. Hasegawa and H. Akagi, "Start-Up and Low-Speed Operation of an Electric Motor Driven by a Modular Multilevel Cascade Inverter," in IEEE Transactions on Industry Applications, vol. 49, no. 4, pp. 1556-1565, July-Aug. 2013.

[9] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, M. Perez, “Powering the future of industry: High-power adjustable speed drive topologies,” IEEE Industry Applications Magazine., vol. 18, Issue 4, pp. 26-39, July 2012.

[10] E. P. Cornell and T. A. Lipo, "Modeling and Design of Controlled Current Induction Motor Drive Systems," in IEEE Transactions on Industry Applications, vol. IA-13, no. 4, pp. 321-330, July 1977.

[11] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," in IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2930-2945, Dec. 2007.

[12] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," in IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3119-3130, Nov. 2011.

[13] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 24, no. 7, pp. 1737-1746, July 2009.

[14] M. Hagiwara, R. Maeda and H. Akagi, "Control and Analysis of the Modular Multilevel Cascade Converter Based on Double-Star Chopper-Cells (MMCC-DSCC)," in IEEE Transactions on Power Electronics, vol. 26, no. 6, pp. 1649-1658, June 2011.

[15] Z. Zhao, K. Li, Y. Jiang, S. Lu and L. Yuan, "Overview on reliability of modular multilevel cascade converters," in Chinese Journal of Electrical Engineering, vol. 1, no. 1, pp. 37-49, Dec. 2015.

[16] F. Deng and Z. Chen, "A Control Method for Voltage Balancing in Modular Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 66-76, Jan. 2014.

[17] H. Iman-Eini, J. Schanen, S. Farhangi and J. Roudet, "A Modular Strategy for Control and Voltage Balancing of Cascaded H-Bridge Rectifiers," in IEEE Transactions on Power Electronics, vol. 23, no. 5, pp. 2428-2442, Sept. 2008.

[18] M. R. Islam, Y. Guo and J. Zhu, "A High-Frequency Link Multilevel Cascaded Medium-Voltage Converter for Direct Grid Integration of Renewable Energy Systems," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4167-4182, Aug. 2014.

[19] F. Z. Peng, W. Qian and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," The 2010 International Power Electronics Conference - ECCE ASIA -, Sapporo, 2010, pp. 492-501.

[20] S. Kouro, B. Wu, Á. Moya, E. Villanueva, P. Correa and J. Rodríguez, "Control of a cascaded H-bridge multilevel converter for grid connection of photovoltaic systems," 2009 35th Annual Conference of IEEE Industrial Electronics, Porto, 2009, pp. 3976-3982.

[21] G. Konstantinou, J. Pou, S. Ceballos and V. G. Agelidis, "Active Redundant Submodule Configuration in Modular Multilevel Converters," in IEEE Transactions on Power Delivery, vol. 28, no. 4, pp. 2333-2341, Oct. 2013.

[22] J. Böcker, B. Freudenberg, A. The and S. Dieckerhoff, "Experimental Comparison of Model Predictive Control and Cascaded Control of the Modular Multilevel Converter," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 422-430, Jan. 2015.

[23] B. Wu, High-Power Converters and AC Drives. New York: Wiley-IEEE Press, Mar. 2006.

[24] B. Wu, Y. Lang, N. Zargari, and S. Kouro, Power Conversion and Control of Wind Energy Systems. New York: Wiley-IEEE Press, June 2011.

[25] R. H. Baker, “High-voltage converter circuit,” U.S. Patent 4 203 151, May 13, 1980.

[26] R. H. Baker, “Bridge converter circuit,” U.S. Patent 4 270 163, May 26, 1981.

[27] A. Nabae, I. Takahashi, and H. Akagi, “A neutral-point-clamped PWM inverter,” in Conf. Rec. IAS Annu. Meeting, Cincinnati, OH, Sep. 28–Oct. 3, 1980, vol. 3, pp. 761–766.

[28] T. Bruckner, S. Bernet, and H. Guldner, “The active NPC converter and its loss-balancing control,” IEEE Trans. Ind. Electron., vol. 52, no. 3, pp. 855–868, June 2005.

[29] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, “Voltage balancing control of diode-clamped multilevel converters with passive front-ends,” IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1751–1758, July 2008.

[30] D. G. Holmes and T. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice, 1st ed. New York: Wiley-IEEE Press, Sept. 2003.

[31] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, “Multilevel converters: An enabling technology for high-power applications,” Proc. IEEE, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[32] J. A. Dickerson and G. H. Ottaway, “Transformerless power supply with line to load isolation,” U.S. Patent 3 596 369, Aug. 3, 1971.

[33] T. Meynard and H. Foch, “Dispositif e´lectronique de conversion d’e´nergie e´lectrique,” French Patent 267 971 5B1, Jan. 29, 1993.

[34] C. M. Wu, W. H. Lau, and H. Chung, “A five-level neutral-point clamped H-bridge PWM inverter with superior harmonics suppression: A theoretical analysis,” in Proc. IEEE Int. Symp. Circuits Syst., Orlando, FL, May 30–June 2, 1999, vol. 5, pp. 198–201.

[35] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, “Active neutral-point-clamped multilevel converters,” in Proc. IEEE 36th Power Electron. Spec. Conf., June 16, 2005, pp. 2296–2301.

[36] J. Dixon and L. Mora´n, “High-level multistep inverter optimization using a minimum number of power transistors,” IEEE Trans. Power Electron., vol. 21, no. 2, pp. 330–337, Mar. 2006.

[37] V. Guennegues, B. Gollentz, F. Meibody-Tabar, S. Rael, and L. Leclere, “A converter topology for high speed motor drive applications,” in Proc. 13th EPE, Oct. 2009, p. 8.

[38] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro, “Current source converter and cycloconverter topologies for industrial medium voltage drives,” IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2786– 2797, July 2008.

[39] R. Bhatia, H. U. Krattiger, A. Bonanini, et al., “Adjustable speed drive with a single 100-MW synchronous motor,” ABB Rev., no. 6, pp. 14–20, 1998.

[40] U. Henning, R. Hoffmann, and J. Hochleitner, “Advanced static power converter and control components for TRANSRAPID maglev system,” in Proc. PCC Osaka, Apr. 2–5, 2002, vol. 3, pp. 1045–1049.

[41] K. Lee and G. Nojima, "Quantitative Power Quality and Characteristic Analysis of Multilevel Pulse Width-Modulation Methods for Three-Level Neutral-Point-Clamped Medium-Voltage Industrial Drives," in IEEE Transactions on Industry Applications, vol. 48, no. 4, pp. 1364-1373, July-Aug. 2012.

[42] H. Tang and A. Q. Huang, "A design investigation of A 1 MVA SiC medium voltage three phase rectifier based on isolated dual active bridge," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 2409-2416.

[43] J. Biela, M. Schweizer, S. Waffler and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," in IEEE Transactions on Industrial Electronics, vol. 58, no. 7, pp. 2872-2882, July 2011.

[44] A. Q. Huang, "New unipolar switching power device figures of merit," in IEEE Electron Device Letters, vol. 25, no. 5, pp. 298-301, May 2004.

[45] J. Wang et al., "Characterization, Modeling, and Application of 10-kV SiC MOSFET," in IEEE Transactions on Electron Devices, vol. 55, no. 8, pp. 1798-1806, Aug. 2008.

[46] "SiC Power Devices and Modules," ROHM Semiconductor Application Note 13103EAY01, 2013. Available: http://www.rohm.com/documents/11303/2861707/sic_app-note.pdf

[47] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014.

[48] X. She, A. Q. Huang, Ó. Lucía and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8193-8205, Oct. 2017.

[49] A. Q. Huang, "Power Semiconductor Devices for Smart Grid and Renewable Energy Systems," in Proceedings of the IEEE, vol. PP, no. 99, pp. 1-29, June, 2017.

[50] A. Q. Huang, Q. Zhu, L. Wang and L. Zhang, "15 kV SiC MOSFET: An enabling technology for medium voltage solid state transformers," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 2, pp. 118-130, 2017.

[51] G. Wang, A. Q. Huang et al., "Static and dynamic performance characterization and comparison of 15 kV SiC MOSFET and 15 kV SiC n-IGBTs," 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD) , Hong Kong, 2015, pp. 229-232.

[52] H. Tang and A. Q. Huang, "Assessment of medium voltage SiC MOSFET advantages in medium voltage drive application," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017, pp. 801-807.

[53] A. Q. Huang, Li Wang, Q. Tian, Qianlai Zhu, Dong Chen and Wensong Yu, "Medium voltage solid state transformers based on 15 kV SiC MOSFET and JBS diode," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 6996-7002.

[54] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," in IEEE Transactions on Industry Applications, vol. 28, no. 6, pp. 1294-1301, Nov.-Dec. 1992.

[55] B. Zhao, Q. Song, W. Liu and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4091-4106, Aug. 2014.

[56] S. Falcones, R. Ayyanar and X. Mao, "A DC–DC Multiport-Converter-Based Solid-State Transformer Integrating Distributed Generation and Storage," in IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 2192-2203, May 2013.

[57] F. Krismer and J. W. Kolar, "Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications," in IEEE Transactions on Industrial Electronics, vol. 59, no. 7, pp. 2745-2760, July 2012.

[58] H. Bai and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge DC–DC Converters Using Novel Dual-Phase-Shift Control," in IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2905-2914, Nov. 2008.

[59] G. G. Oggier, G. O. GarcÍa and A. R. Oliva, "Switching Control Strategy to Minimize Dual Active Bridge Converter Losses," in IEEE Transactions on Power Electronics, vol. 24, no. 7, pp. 1826-1838, July 2009.

[60] G. Oggier, G. O. García and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-DC converter under soft switching in the whole operating range," in IEEE Transactions on Power Electronics, vol. 26, no. 4, pp. 1228-1236, April 2011.

[61] H. Zhou and A. M. Khambadkone, "Hybrid Modulation for Dual-Active-Bridge Bidirectional Converter With Extended Power Range for Ultracapacitor Application," in IEEE Transactions on Industry Applications, vol. 45, no. 4, pp. 1434-1442, July-aug. 2009.

[62] H. Fan and H. Li, "High-Frequency Transformer Isolated Bidirectional DC–DC Converter Modules With High Efficiency Over Wide Load Range for 20 kVA Solid-State Transformer," in IEEE Transactions on Power Electronics, vol. 26, no. 12, pp. 3599-3608, Dec. 2011.

[63] H. Shi et al., "Minimum-Backflow-Power Scheme of DAB-Based Solid-State Transformer With Extended-Phase-Shift Control," in IEEE Transactions on Industry Applications, vol. 54, no. 4, pp. 3483-3496, July-Aug. 2018.

[64] Q. Tian et al., "A novel light load performance enhanced variable-switching-frequency and hybrid single-dual-phase-shift control for single-stage dual-active-bridge based AC/DC converter," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1227-1232.

[65] G. Guidi, M. Pavlovsky, A. Kawamura, T. Imakubo and Y. Sasaki, "Improvement of light load efficiency of Dual Active Bridge DC-DC converter by using dual leakage transformer and variable frequency," 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, 2010, pp. 830-837.

[66] T. Hirose, M. Takasaki and Y. Ishizuka, "A Power Efficiency Improvement Technique for a Bidirectional Dual Active Bridge DC–DC Converter at Light Load," in IEEE Transactions on Industry Applications, vol. 50, no. 6, pp. 4047-4055, Nov.-Dec. 2014.

[67] A. K. Jain and R. Ayyanar, "Pwm control of dual active bridge: Comprehensive analysis and experimental verification," in IEEE Transactions on Power Electronics, vol. 26, no. 4, pp. 1215-1227, April 2011.

[68] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando and J. Sebastián, "Different Purpose Design Strategies and Techniques to Improve the Performance of a Dual Active Bridge With Phase-Shift Control," in IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 790-804, Feb. 2015.

[69] X. Liu et al., "Novel Dual-Phase-Shift Control With Bidirectional Inner Phase Shifts for a Dual-Active-Bridge Converter Having Low Surge Current and Stable Power Control," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 4095-4106, May 2017.

[70] A. Taylor, G. Liu, H. Bai, A. Brown, P. M. Johnson and M. McAmmond, "Multiple-Phase-Shift Control for a Dual Active Bridge to Secure Zero-Voltage Switching and Enhance Light-Load Performance," in IEEE Transactions on Power Electronics, vol. 33, no. 6, pp. 4584-4588, June 2018.

[71] T. Zhao, G. Wang, S. Bhattacharya and A. Q. Huang, "Voltage and Power Balance Control for a Cascaded H-Bridge Converter-Based Solid-State Transformer," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1523-1532, April 2013.

[72] S. Shao, M. Jiang, J. Zhang and X. Wu, "A Capacitor Voltage Balancing Method for a Modular Multilevel DC Transformer for DC Distribution System," in IEEE Transactions on Power Electronics, vol. 33, no. 4, pp. 3002-3011, April 2018.

[73] P. Zumel et al., "Modular Dual-Active Bridge Converter Architecture," in IEEE Transactions on Industry Applications, vol. 52, no. 3, pp. 2444-2455, May-June 2016.

[74] X. She, A. Q. Huang and X. Ni, "Current Sensorless Power Balance Strategy for DC/DC Converters in a Cascaded Multilevel Converter Based Solid State Transformer," in IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 17-22, Jan. 2014.

[75] J. Shi, W. Gou, H. Yuan, T. Zhao and A. Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," in IEEE Transactions on Power Electronics, vol. 26, no. 4, pp. 1154-1166, April 2011.

[76] S. P. Engel, N. Soltau, H. Stagge and R. W. De Doncker, "Dynamic and Balanced Control of Three-Phase High-Power Dual-Active Bridge DC–DC Converters in DC-Grid Applications," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1880-1889, April 2013.

[78] S. Hwang, X. Liu, J. Kim and H. Li, "Distributed Digital Control of Modular-Based Solid-State Transformer Using DSP+FPGA," in IEEE Transactions on Industrial Electronics, vol. 60, no. 2, pp. 670-680, Feb. 2013.

[79] B. Zhao, Q. Song, J. Li, Q. Sun and W. Liu, "Full-Process Operation, Control, and Experiments of Modular High-Frequency-Link DC Transformer Based on Dual Active Bridge for Flexible MVDC Distribution: A Practical Tutorial," in IEEE Transactions on Power Electronics, vol. 32, no. 9, pp. 6751-6766, Sept. 2017.

[80] Z. Zhang, H. Zhao, S. Fu, J. Shi and X. He, "Voltage and power balance control strategy for three-phase modular cascaded solid stated transformer," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 1475-1480.