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The Mechanism of the Flatband Voltage Shift by Capping a Thin Layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2-based Dielectrics

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by

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Dedicated

To my mother

Miao Li

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The Mechanism of the Flatband Voltage Shift by Capping a Thin Layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2-based Dielectrics

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Continuing to scale down the transistor size makes the introduction of high-k dielectric necessary. However, there are still a lot of problems with high-k transistors such as worse reliability and Fermi-level pinning. In HfO_2, low crystallization temperature, fixed charge in the bulk and low quality of the Si/HfO_2 interface cause reliability problems. Fermi-level pinning results in high threshold voltage.

For the first work in this dissertation, forming $Hf_{1-x}Ta_xO$ through doping HfO_2 with Ta is used to improve the crystallization temperature and electron mobility.

Then, the fluorine passivation of high-k dielectrics is studied. With fluorine passivation, the electron mobility was improved in NMOSFETs with

gate stacks of poly-Si/TaN/HfO_2/p-Si with thin TaN layers. Inserting a 1.5nm layer of HfSiON between TaN and HfO_2 completely blocked the fluorine atoms so that they could not reach the Si interface. Thus, no mobility was improved even with fluorine implantation.

In order to decrease threshold voltage, we must study mechanisms of Fermi level pinning (FLP) in high-k gate stacks. We summarize three FLP mechanisms: (1) the dipole formation at the interface between metal gate and high-k dielectric due to hybridization; 2) the dipole formation through oxygen vacancy mechanism; (3) the dipole formation at the interface between high-k dielectric and interfacial SiO_2.

The rest of dissertation focuses on the mechanism of V_{fb} shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2-based high-k dielectrics with TaN, W and Pt metal gate. It is proposed that the negative V_{fb} shift with TaN metal gate be due to the dipole formation at the interface between Me_2O_3 and the interfacial SiO_2. An XPS (X-ray photoelectron spectroscopy) study of Gd_2O_3 capping on SiO_2 indicates clear Si, O and Gd related bonding state change at the interface between Gd_2O_3 (or GdSiO) and the interfacial SiO_2. So the bonding state change is the root cause of the dipole formation. When there is an oxygen deficiency in Me_2O_3, another dipole formation through oxygen vacancy mechanism can also be observed. For a full understanding of the V_{fb} shift, all three FLP mechanisms must be considered.

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Chapter 1

Introduction

1.1 Necessity for the high-k dielectric introduction

Moore's law states that the density of transistors on chips doubles every 24 months or so. To keep on the Moore's Law curve, the size of transistors must be halved. Such a scaling of integration technology has been the crucial element for Si-based microelectronics industry for more than 40 years. The size reduction of transistors includes both gate length and gate oxide thickness. Fig.1.1 shows technology node and transistor physical gate length in Intel microprocessors [1].

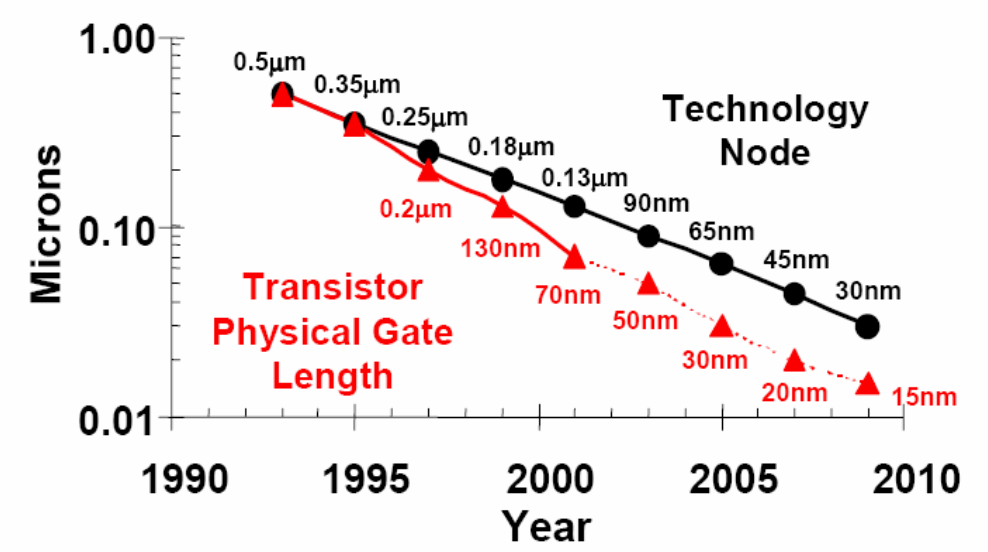

Fig.1.1 Technology node and transistor physical gate length in Intel microprocessors [1].

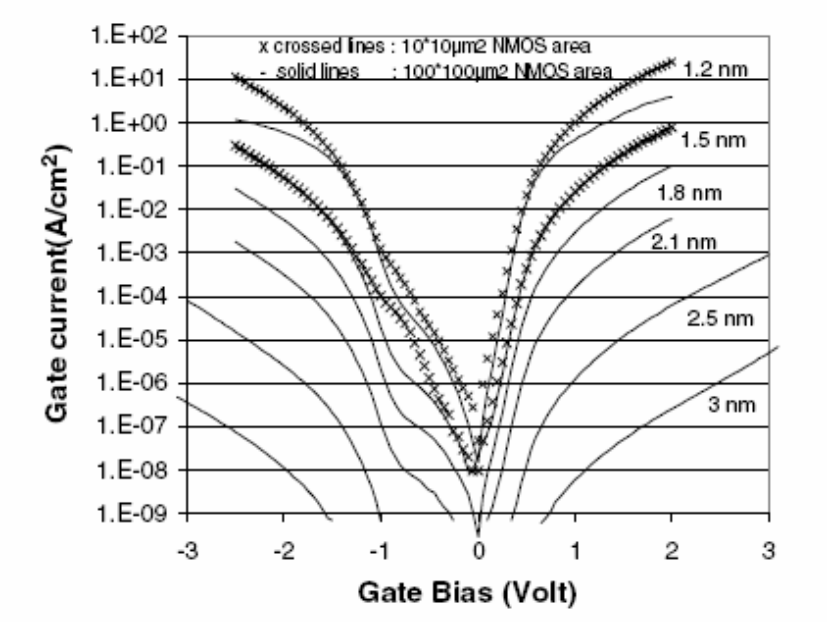

Fig.1.2 NMOSFET current densities versus gate bias with varying SiO_2 thickness with N+ Poly electrode and an area of 100×100 μm^2. Additional data on a smaller area of 10×10 μm^2 were shown by crosses for the two lowest thicknesses (1.2 and 1.5 nm). The series resistance in p-silicon substrate for negative bias and the additional channel resistance for positive bias increasingly impacted the leakage current in thin gate oxide. The smaller area decreased the influence of the channel resistance [2].

At 90 and 65 nm nodes, the gate oxide has been reduced to 1.2nm already, about 5 Si atoms thick. The gate oxide can not be scaled down anymore. High leakage current due to tunneling wastes too much power and heats the chips. Fig.1.2 shows the leakage current of n-channel metal-oxide-

semiconductor field effect transistors (NMOSFET) with varying gate SiO_2 thickness [2].

The solution is to introduce high-k materials in the gate oxide. High-k materials such as HfO_2, ZrO_2 and La_2O_3 have high dielectric constant (>20) compared to SiO_2 (~4). So a thicker physical thickness of high-k materials can have the same capacitance as a thinner thickness of SiO_2. Thus, a thicker layer of high-k materials with a lower leakage current can have the same controllability over channel as a thinner SiO_2 layer with a higher leakage current. The thickness of SiO_2 layer is called the equivalent oxide thickness (EOT) of the high-k layer, as both layers give the same capacitance. Intel 45nm technology has used high-k dielectrics in transistors with fivefold reduction in leakage at the same drive current.

1.2 Issues with high-k dielectrics

The criteria for high-k dielectrics are high dielectric constant, thermodynamic stability and proper conduction and valence band offset on Si. HfO_2 based dielectrics were first zeroed in as good candidates. However, initial implementation of high-k dielectrics into transistors encountered two problems [3]:

(1) Degraded mobility due to scattering of interfacial dipole between SiO_2 and HfO_2, phase separation and crystallization, fixed charges, remote phonon and remote surface roughness.

(2) High threshold voltage due to Fermi-level pinning (FLP) at the interface between HfO_2 and poly-Si gate electrode.

A lot of efforts have been done to understand the mechanisms and improve material qualities during the last decade.

Develop the new deposition method

Besides physical vapor deposition (PVD) such reactive sputter and metal organic chemical vapor deposition (MOCVD), a new deposition approach called atomic layer deposition (ALD) has been developed. High-k dielectric grown by ALD has shown less fixed charge and remote surface roughness, and is as smooth as a layer of atoms.

Improve crystallization temperature

Using HfSiO, HfSiON or doping HfO_2 with another high-k metal oxide such asTiO_2, Ta_2O_5, La_2O_3 are found to increase the high-k crystallization temperature and improve the transistor performance greatly.

Introduce metal gates

Instead of poly-Si gate electrode, the adoption of metals such as TaN and TiN as gate electrode (called metal gate) is found to remove the poly-depletion effect and decrease remote phonon scattering. At the same time, FLP is also relaxed. However, it does not disappear and becomes more serious after the high temperature anneal for low EOTs (~1nm) [6, 13].

1.3 Fermi-level pinning in high-k dielectrics

There are three mechanisms of the FLP:

(1) The dipole formation at the interface between metal gate and high-k dielectric due to hybridization [7-10].

(2) The dipole formation through oxygen vacancy (Vo) mechanism, which is especially important for poly-Si and p-metal after high-temperature anneal [9, 11-13].

(3) The dipole formation at the interface between high-k dielectric and interfacial SiO_2 [14-17]. It is not a FLP according to the strict definition of FLP.

All three mechanisms were identified but not fully understood.

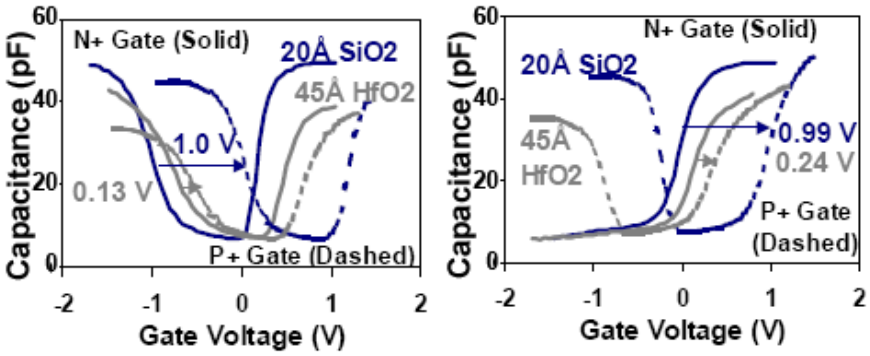

Fig.1.3 NMOSFET and PMOSFET high frequency CV characteristics of ALD HfO_2 and SiO_2 with n+ and p+ poly-Si gates [3]. The ALD HfO_2 has 9Å interfacial SiO_2.

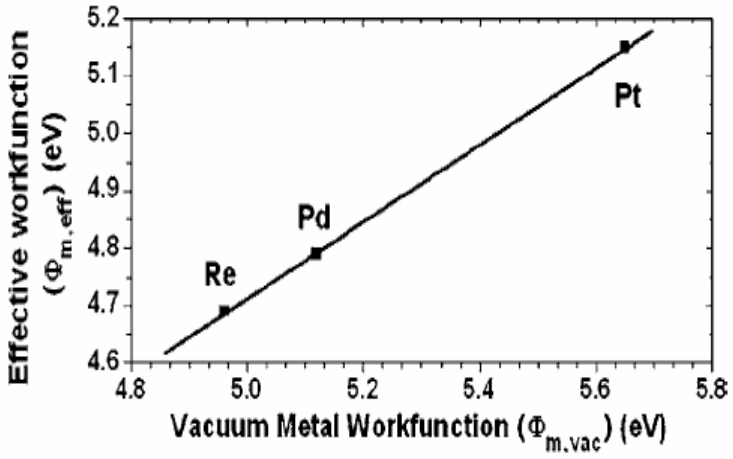

Fig.1.4 Effective work function for Re, Pd and Pt on HfO_2. HfO_2 was deposited by ALD. Post deposition annealing (PDA) was done in NH_3. Re, Pd and Pt was sputtered on the photoresist patterned oxide. Samples were annealed in forming gas at 400 ^oC after the backside Al contact deposition [5].

Fig.1.3 shows NMOSFET and PMOSFET high frequency capacitance-voltage (CV) characteristics of ALD HfO_2 and SiO_2 with n+ and p+ poly-Si gates [4]. Unlike SiO_2, changing the poly-Si doping from n+ to p+ does little to shift the HfO_2 CVs. The reason is the Fermi-level pinning (FLP) at poly-Si/HfO_2 interface. By switching to metal gates, FLP is relaxed but does not appear. It is found that the effective work function of a metal gate extracted from EOT-V_{fb} analysis is different from metal's vacuum work function [5, 8-10].

Fig.1.4 shows effective work function of Re, Pd and Pt on the ALD grown HfO_2 [5]. The stacks did not go through any high temperature anneal. This kind of work function reduction is due to the dipole formation at the interface between metal and high-k dielectric due to hybridization [8-10].

Even the effective work function of a PMOSFET metal gate in a gate stack with a thin interfacial SiO_2 layer is near Si valence bandedge initially, it will decrease when the whole gate stack goes through a high temperature anneal. Fig.1.5 shows universal PMOSFET V_t vs. T_{inv} curve for multiple HfO_2/metal stacks after 1000ºC, 5s rapid thermal anneals (RTAs) [6]. Here V_t is threshold voltage of a PMOSFET. T_{inv} is the equivalent oxide thickness of a MOSFET in the inversion region. This V_t roll-off is caused by the FLP through the oxygen vacancy (Vo) mechanism [13].

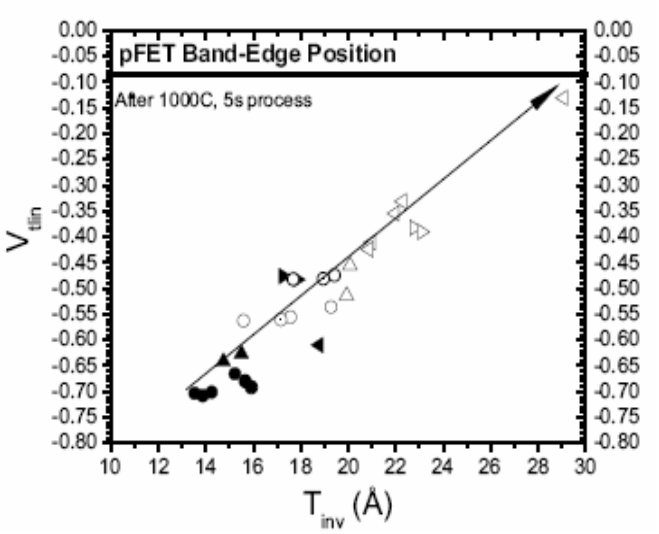

Fig.1.5 Universal PMOSFET V_t vs. T_{inv} curve for multiple HfO_2/metal stacks after 1000ºC, 5s rapid thermal anneals (RTAs) [6].

As the FLP through Vo mechanism causes the flatband voltage (V_{fb}) to shift to the negative direction, a NMOSFET metal gate with an effective work function near 4.0 eV is relatively easy to realize. TaC is such a candidate. A PMOSFET metal gate with an effective work function near 5.1 eV is very difficult to realize for EOT ~1nm [6, 13]. Intel 45nm technology has adopted the gate-last approach to circumvent high temperature anneal for the metal gates. Other companies are still working hard to realize the gate-first approach.

1.4 Outline

Chapter 1 has given an introduction about challenges of scaling SiO_2 and the necessity of the high-k dielectric introduction**.** Issues of high-k dielectrics and FLP mechanisms in a gate stack of poly-Si (metal gate)/high-k dielectric/Si-substrate are briefly explained.

Chapter 2 studies doping HfO_2 with Ta to form $Hf_{1-x}Ta_xO$. Electron mobility is shown to increase with the increase of the crystallization temperature of $Hf_{1-x}Ta_xO$. The highest crystallization temperature and the maximum mobility was observed at x=0.4.

Chapter 3 studies the fluorine passivation of high-k dielectrics through ion implantation. The electron mobility was shown to improve in NMOSFETs with gate stacks of poly-Si/TaN/HfO_2/Si-substrate with thin TaN thickness. Inserting a 1.5nm layer of HfSiON between TaN and HfO_2 completely blocked the fluorine atoms so that they could not reach the interface. Thus, no mobility was improved.

Chapter 4 reviews literature studies on three mechanisms of Fermi level pinning:

(1) The dipole formation at the interface between metal gate and high-k dielectric due to hybridization.

(2) The dipole formation through oxygen vacancy (Vo) mechanism, which is especially important for poly-Si and p-metal after high-temperature anneal.

(3) The dipole formation at the interface between high-k dielectric and interfacial SiO_2

The status of literature studies on the oxygen vacancy (Vo) mechanism in a high-k gate stack is reviewed and some drawbacks in Shiraishi's model and Guha's model are pointed out. Finally, a general expression of flatband voltage with a dipole layer and a bulk charge distribution in the dielectric is introduced.

Chapter 5 reviews literature studies of oxides (Me_2O_3) of lanthanides as high-k gate dielectrics. The negative V_{fb} shift with TaN, TiN and TaC is proposed to be related to the interaction between Me_2O_3 and interfacial SiO_2. The positive V_{fb} shift with Pt is shown to be related to the Pt/high-k dielectric interface. We show that in order to understand the mechanism of the V_{fb} shift with a thin layer of Me_2O_3 capping, we must study two dipoles together: the dipole at Me_2O_3/SiO_2 interface and the dipole at metal/high-k dielectric interface. For low EOT, all three FLP mechanisms must be considered.

Chapter 6 studies TaN characteristics versus N_2 flow rate during TaN deposition. The V_{fb} shift for gate stacks with HfO_2 and SiO_2 gate dielectrics without and with a high temperature anneal (PMA) is characterized. The

formation of a thin layer of TaON is proposed after PMA, which determines the dipoles at TaN/SiO_2 and TaN/HfO_2 interfaces.

Chapter 7 (with TaN) and 8 (with W and Pt) study the mechanisms of the V_{fb} shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2 based-dielectrics. It is shown that among MeHfO, MeSiO, the dipole at the interface of metal gate and high-k dielectrics, none is the reason of the negative V_{fb} shift for thick interfacial SiO_2 layers (or large EOTs). The root cause is found to be the interaction between Me_2O_3 and the interfacial SiO_2. A MeSiO layer forms due to the solid reaction between Me_2O_3 and the interfacial SiO_2 layer, and a dipole appears at the interface of the MeSiO layer and the interfacial SiO_2 layer. An XPS (X-ray photoelectron spectroscopy) study of Gd_2O_3 capping on SiO_2 indicates clear Si, O and Gd related bonding configuration change at the interface between Me_2O_3 (or MeSiO) and the interfacial SiO_2. When there is an oxygen deficiency in Me_2O_3, another dipole formation through oxygen vacancy mechanism can also be observed. Three metal gates of TaN, W and Pt have been studied. Experiments were also performed to explore possible interaction among three dipoles for thin interfacial SiO_2 layers (or small EOTs): the dipole at the interface of metal gate and high-k dielectrics, the dipole induced by the interaction between Me_2O_3 and the interfacial SiO_2, and the dipole formation through oxygen vacancy mechanism.

Chapter 9 gives an introduction to X-ray photoelectron spectroscopy (XPS). A new method based on the measured binding energy profile of the metal element in a metal gate is proposed to study the effective work function of the metal gate.

Chapter 10 summarizes the work done in this dissertation, and possible future works are suggested.

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Chapter 2

Doping HfO_2 with Ta to Form HfTaO Gate Dielectrics

2.1 Overview

In this chapter, n-channel metal-oxide-semiconductor transistors (NMOSFETs) using HfTaO with varying Ta composition (20%, 30%, 40% and 50%) have been fabricated and characterized. Crystallization temperatures of HfTaO with varying Ta composition were also measured. It was found that HfTaO with 40% Ta exhibited the highest crystallization temperature of 900^{o}C, while 35% and 52% HfTaO showed crystallization temperature of 800^{o}C. The results demonstrate that HfTaO NMOSFETs exhibit higher electron mobility than controlled HfO_2 devices. Of them, the transistor with 40% Ta shows the highest electron mobility.

2.2 Introduction

Hf-based dielectrics have been studied extensively and are considered to be the most promising high-k material for the metal-oxide-semiconductor transistor (MOSFET) application [1-4]. Excellent device performance has been achieved. However, "undoped" HfO_2 possesses low crystallization temperature (< 600^{o}C). Incorporating Si and N can improve the crystallization temperature greatly [5-7]. Another method to increase crystallization temperature is using the

multi-metal oxide approach. Both the mixture of Hf and Ti and that of Hf and Ta have been reported, and reasonable good device performance has been demonstrated [8, 9]. Since Ti and Ta tend to react with Si substrate causing large leakage current, a barrier layer between Si substrate and the oxide of Ti or Ta is needed. Surface nitridation has been used to form such a barrier layer [8], but it causes the mobility degradation and sometimes very leaky dielectrics. Depositing a thin Hf layer at the bottom is another way to form a barrier layer and has demonstrated for HfTiO system [9]. In this chatper, we have developed multi-metal oxide MOSFETs using HfTaO/HfO_2 bi-layer structure as gate dielectrics with varying Ta composition.

2.3 Experimental

For the purpose of characterizing the crystallization temperature of HfTaO, 150 Å multi-metal oxides of Hf and Ta on 50 Å SiO_2 were co-sputtered in Ar using varying power ratios and then annealed at varying temperatures for 1 min in N_2. X-ray diffraction (XRD) was used to characterize the crystallization temperature of HfTaO. The n-type MOSFET (NMOSFET) structure with TaN/HfTaO/HfO_2/p-Si was used in this study. After field oxide growth and active area patterning, Hf or Hf and Ta mixture were sputtered at room temperature. The thickness of dielectrics was measured by an elipsometer. Post-deposition annealing (PDA) was done in a

furnace at 500 ^{o}C in N_2 for 5 min. TaN gate electrode (2000 Å) was deposited using reactive sputtering and etched using reactive ion etching (RIE) in CF_4 gas. For transistor fabrication, after TaN etching, Phosphorous was implanted using the energy of 50 KeV and the dose of 5×10^{15} cm^2. Implantation activation was done at 900 ^{o}C for 1 min using rapid thermal annealing (RTA). After activation, each wafer was cut into two pieces. One piece was then annealed in D_2/N_2 gas at 600 ^{o}C for 20 min and the other piece skipped this step. Finally to finish the transistor fabrication, Al was deposited on the backside of wafers and annealed in forming gas at 400 ^{o}C for 30 min.

2.4 Results and discussion

Fig.2.1 shows the crystallization temperature of HfTaO for Ta composition varying from 15% to 50%. HfO_2 was found to crystallize at temperature as low as 400^{o}C. HfTaO with 40% Ta sample exhibited the highest crystallization temperature of 900^{o}C. Both 30%- and 50%-Ta HfTaO crystallized at 800 ^{o}C.

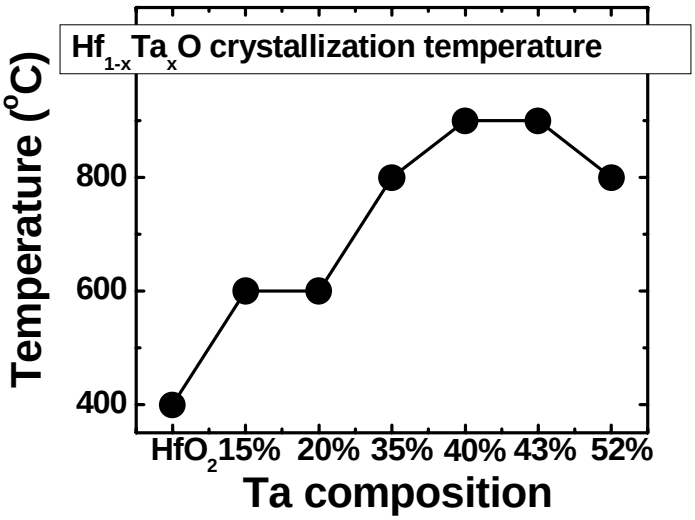


Fig.2.1 Crystallization temperature of HfTaO with different Ta composition measured by XRD. The incident angle of X-ray: 3 ^{o} was used.

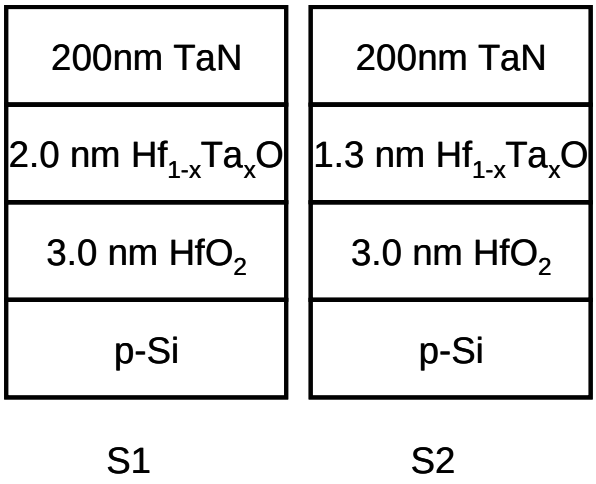


Fig.2.2 Gate stacks used for MOSFET fabrication

The stack structures of dielectrics used here is HfTaO/HfO_2/Si substrate. Two thicknesses (S1 and S2) of HfTaO were chosen (Fig.2.2). In S1, 20Å $Hf_{1-x}Ta_xO$ with x=0, 20%, 30%, 40%, 50% were deposited. In S2, 13Å $Hf_{1-y}Ta_yO$ with y=30%, 40%, 50% were deposited. The 30 Å HfO_2 barrier layer was chosen in both S1 and S2 to avoid the diffusion of Ta to Si substrate while maintaining small equivalent oxide thickness (EOT).

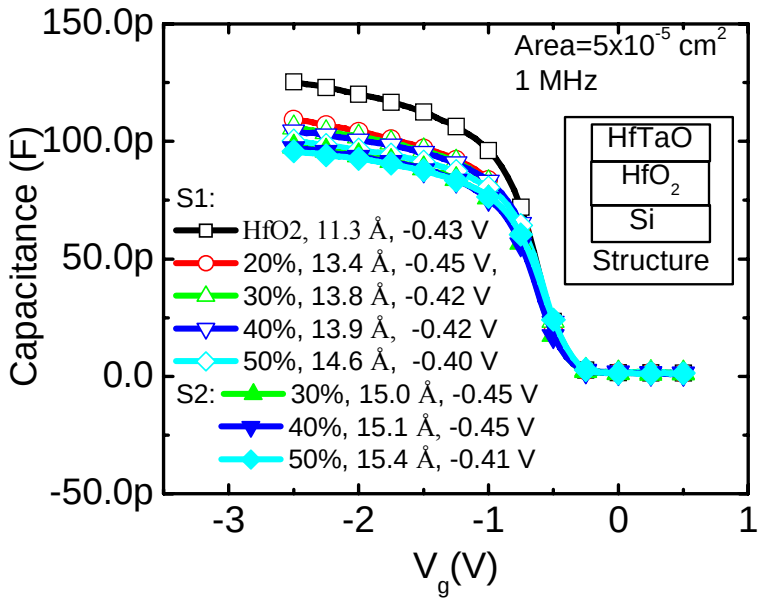
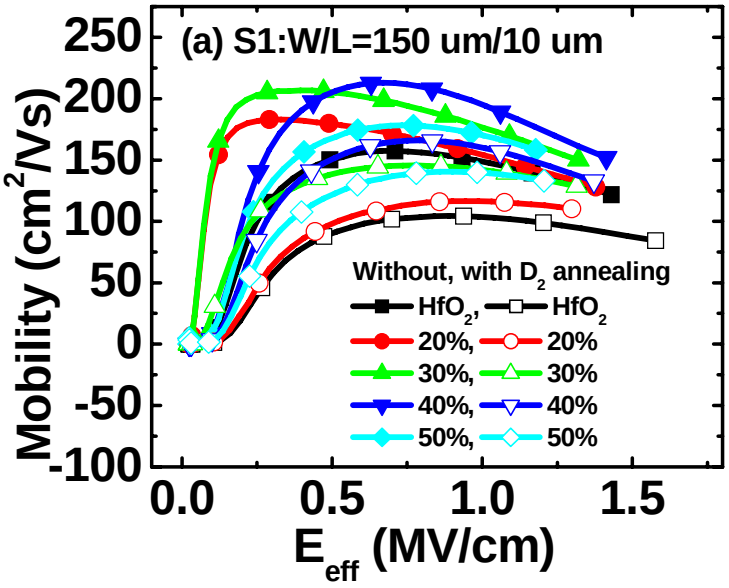


Fig.2.3 CV curves of capacitors with an area of 5×10^{-5} cm^2 at 1 MHz without D_2 annealing. The gate stack structure HfTaO/HfO_2/Si is shown in the inset. In the structure of S1, the thickness of the top HfTaO layer is 20 Å; in S2, it is 13 Å.

Fig.2.3 shows capacitance versus voltage (CV) curves of capacitors with an area of 5×10^{-5} cm^2 at 1 MHz. These capacitor patterns were on the transistor wafers without D_2 annealing. CV curves were simulated using the CVC program, and the EOT and the flat-band voltage V_{fb} were extracted. Their values were presented in the figure. As can be seen, the higher the Ta composition, the higher the EOT. V_{fb}'s for different Ta composition are almost the same, indicative of no much extra charge introduced by Ta incorporation. Capacitors in S2 have larger EOTs than those in S1.



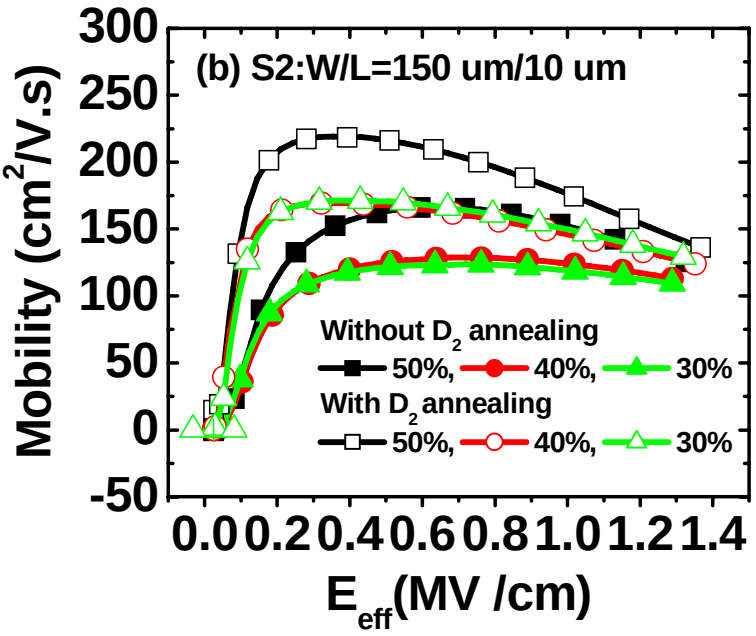
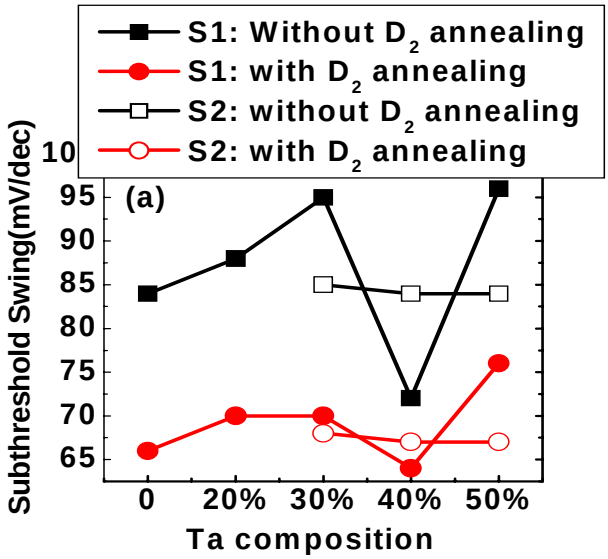


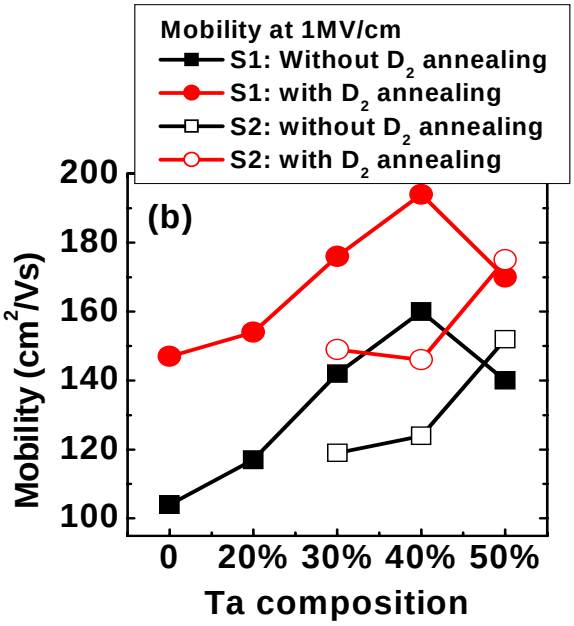
Fig.2.4 Effective mobility of HfTaO NMOSFETs (S1) without and with D_2 annealing: (a) S1, (b) S2.

Fig.2.4 shows the effective mobility characteristics of the n-MOSFETs in S1 and S2. Fig.2.5 shows threshold swing, mobility at 1MV/cm and V_{th} versus Ta composition. Without 600 ^{o}C D_2 annealing, typical threshold voltages (V_{th}) and the corresponding -threshold swings (S) of $Hf_{1-x}Ta_xO$ transistors (S1) with x=0, 20%, 30%, 40%, and 50% were V_{th} (S)=0.427 (84), 0.445 (88), 0.475 (95), 0.420 (72) and 0.425 V(96 mV/decade), respectively. With 600 ^{o}C D_2 annealing for 20 min, threshold voltages and the corresponding -threshold swings became

V_{th} (S)= 0.326 (66), 0.325 (70), 0.335 (70), 0.365 (64), 0.380 V (76 mV/decade), respectively. At 1 MV/cm, the values of the effective mobility (μ_{eff}) of $Hf_{1-x}Ta_xO$ transistors (S1) with x=0, 20%, 30%, 40%, and 50% were 104, 117, 142, 160, and 140 cm^2/Vs, respectively. The effective mobility was calculated the split CV method. After D_2 annealing, the corresponding values were 147, 154, 176, 194, and 170 cm^2/Vs. D_2 annealing improved the mobility by passivating the dangling bonds in high-k dielectrics Of all HfTaO transistors (S1) with different Ta composition, the transistor with 40% Ta gives the best S and μ_{eff}; the transistors with 30% and 50% Ta composition show the next best results. This trend is in agreement with the change of the crystallization temperature of HfTaO with different Ta composition. In order to determine the lowest thickness of HfTaO which can keep such a performance trend, we fabricate n-MOSFETs with 13 Å top HfTaO layer (S2). Without 600 ^oC D_2 annealing, threshold voltages (V_{th}) and the corresponding -threshold swings (S) of $Hf_{1-y}Ta_yO$ transistors (S2) with y= 30%, 40%, and 50% were V_{th} (S)=0.470 (85), 0.472 (84), 0.525 V (84 mV/decade), respectively. With 600 ^oC D_2 annealing for 20 min, threshold voltages and the corresponding -threshold swings changed to V_{th} (S)= 0.346 (68), 0.336 (67), 0.390 V(67 mV/decade), respectively. At 1 MV/cm, the values of the effective mobility (μ_{eff}) of $Hf_{1-y}Ta_yO$ transistors (S2) with y=30%, 40%, and 50% were 119, 124 and 152 cm^2/Vs, respectively. With D_2 annealing, the corresponding values increased to 149, 146 and 175 cm^2/Vs,

respectively. Of three Ta compositions in S2, the transistor with 50% shows the highest mobility. The difference from S1 might be due to: (1) in S2, the thickness of $Hf_yTa_{1-y}O$ is not large enough to follow the trend of the crystallization temperature change; (2) during the implantation activation, Ta diffused to Si substrate and changed the Ta composition of the top $Hf_yTa_{1-y}O$.




Mobility at 1MV/cm
S1: Without D2 annealing
S1: with D2 annealing
S2: without D2 annealing
S2: with D2 annealing
(b)
Mobility (cm2/Vs)
200
180
160
140
120
100
0
20%
30%
40%
50%
Ta composition

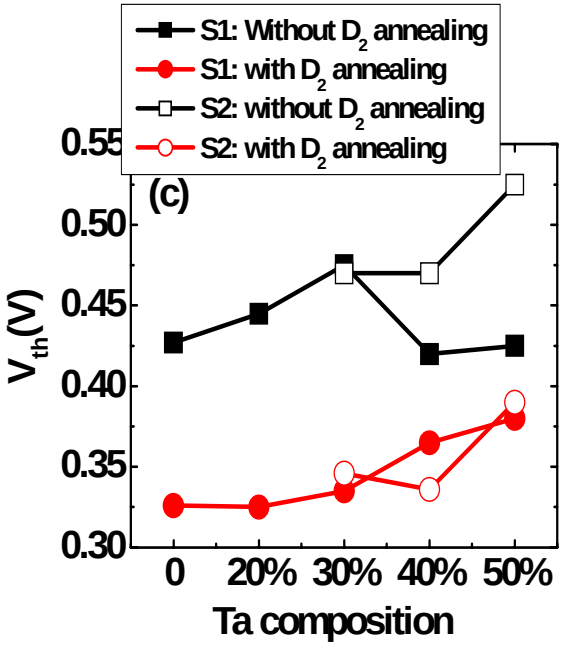

S1: Without D2 annealing
S1: with D2 annealing
S2: without D2 annealing
S2: with D2 annealing
(c)
Vth(V)
0.55
0.50
0.45
0.40
0.35
0.30
0
20%
30%
40%
50%
Ta composition

Fig.2.5 (a) Subthreshold swing, (b) Mobility at 1MV/cm and (c) V_{th} versus Ta composition.

Fig.2.6 shows the leakage current (J) vs. EOT characteristics at $|V_g-V_{fb}|$=1.0 V. Without post metal-deposition annealing (PMA), the leakage current of capacitors consisting of variable thickness of 35% $Hf_{1-x}Ta_xO$ on 30 Å HfO_2 followed the line of J vs. EOT for HfO_2. The leakage current of capacitors in S1 and S2 after transistor fabrication was one order of magnitude higher than that for HfO_2, but still two orders lower than that for SiO_2. D_2 annealing at 600 ^oC for 20 min resulted in slightly higher leakage current and an EOT increase of about 1 Å.

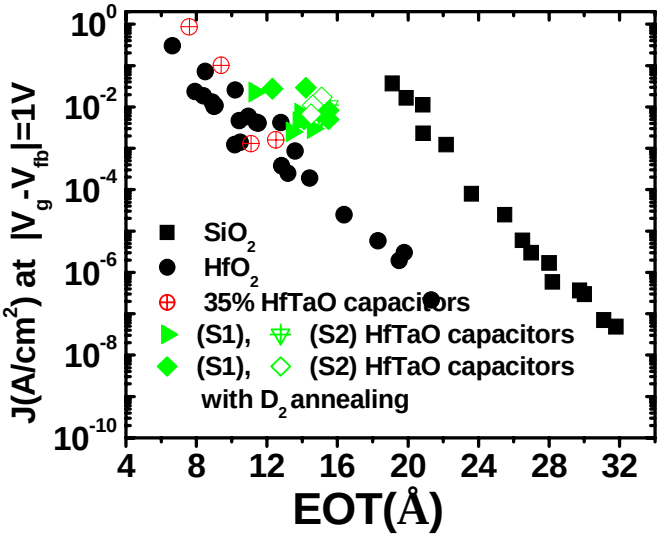


Fig.2.6 Leakage current density (J) vs. EOT for HfTaO dielectrics measured on capacitors with an area of 5×10^{-5} cm^2.

2.5 Summary

In summary, NMOSFETs using HfTaO as gate dielectrics with varying Ta composition and HfO_2 bottom barrier layer have been fabricated. HfTaO with 40% Ta showed the highest crystallization temperature of 900^{o}C. These NMOSFETs exhibited higher driving current and mobility compared to the control HfO_2 devices. The performance of transistors using 20 Å top HfTaO layers follows the trend of the crystallization temperature with Ta composition.

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Chapter 3

Fluorine Passivation in Gate Stacks of Poly-Si/TaN/HfO_2 (and HfSiON/HfO_2)/Si

3.1 Overview

In this chapter, fluorine passivation in poly-Si/TaN/HfO_2/p-Si and poly-Si/TaN/HfSiON/HfO_2/p-Si gate stacks with varying TaN thickness through gate ion implantation has been studied. It has been found that when TaN thickness was less than 15nm, mobility and threshold swing improved significantly in HfO_2 NMOSFETs; while there was little performance improvement in HfSiON/HfO_2 NMOSFETs due to the blocking of F atoms by the HfSiON layer in gate dielectrics, as has been proved by the electron energy loss spectroscopy (EELS) mapping.

3.2 Introduction

Significant progress has been made on high-k dielectrics in last several years. However, threshold voltage (V_{th}) instability and device degradation are still major concerns for metal-oxide-semiconductor field effect transistors (MOSFETs) using high-k gate dielectrics due to high interface and bulk trap density [1]. Hydrogen (H) and deuterium (D) anneals have been found to help passivate these traps with significantly improved device performance [2].

However, the bonding between high-k dielectric (and Si) and H is still not sufficiently stable to meet the requirement of reliability. Recent studies show that fluorine (F) passivation is very robust and can be used to improve the reliability of high-k dielectric MOSFETs [5-7]. The bonding energy for a single Si-F is 5.81 eV [4], which is much larger than that (3.6 eV) for a single Si-H bond [3]. Tseng *et al* studied F passivation in poly-Si/Ta_xC_y/HfZrO gate stacks through gate implantation [5]. With F passivation, V_{th} instability was improved and the stressed induced leakage current (SILC) decreased greatly. Inoue *et al* compared channel implantation (done prior to dielectric formation) and gate implantation (into poly-Si gate) to incorporate F into poly-Si/HfSiON gate stacks [6]. They found that channel F implantation was more effective in lowering V_{th} and improving negative bias temperature instability (NBTI). Seo *et al* incorporated F through the ultraviolet (UV) radiation assisted reaction between F_2 and the HfO_2/SiO_2 gate stack [7]. They showed that F incorporation decreased the flat-band voltage (V_{fb}) shift and suppressed the interface state generation. Thus, F incorporation is an effective way to passivate defects in high-k dielectrics. However, how a thin TaN layer in the gate electrode or a thin HfSiON layer in HfO_2 gate dielectric affects the effectiveness of F passivation have not been studied systematically. In this paper we have investigated these aspects by comparing fluorine (F) passivation in poly-Si/TaN/HfO_2/p-Si and

Poly-Si/TaN/HfSiON/HfO_2/p-Si gate stacks with varying TaN layer thickness through gate ion implantation.

3.3 Experimental

After field oxide growth and active pattern formation, high-k dielectrics were deposited using PVD on dilute HF dipped p-type Si substrates. Two dielectric structures were chosen: A) 5 nm HfO_2 (called HfO_2 structure in the following), B) 1.5 nm HfSiON/3.5 nm HfO_2, the so-called TSN structure (top silicon nitridation) [2]. The composition of Si defined as [Si]/([Si]+[Hf]) in HfSiON was 0.4. Post deposition annealing (PDA) was done at 600 ^oC for 40 s in N_2. Then TaN layer with the thickness varying from 5 to 20 nm with a step of 5 nm was deposited in another PVD chamber for each dielectric structure. On the top of the TaN layer, 200 nm poly-Si was grown at 550 ^oC. For comparison, TaN-only (200 nm thick) control devices were also fabricated. Fig.3.1 shows gate stacks for both dielectric structures (HfO_2 and TSN). Poly-Si/TaN or TaN gate were patterned and etched using CF_4 reactive ion etching (RIE). After etching, each wafer was cut into two pieces. One split of pieces were subjected to F implantation with the energy and the dose of 30 keV, 2×10^{15} cm^{-2}. The stopping range of F ions is about 72 nm through a TRIM simulation [8]. The other split has no F implantation. Then phosphorous implantation was done on all two splits of pieces with the energy and the dose of 50 keV, 5×10^{15} cm^{-2}.

Activation was done at 900 ^{o}C for 1 min. Finally, Aluminum (Al) contacts were formed on both sides of wafers and annealed in forming gas at 450 ^{o}C for 30 min. Capacitance and leakage current density characteristics were measured on metal-oxide-semiconductor capacitors (MOSCAPs) with an area of 5×10^{-5} cm^2. Fig.3.2 shows process splits. The equivalent oxide thickness (EOT) was extracted through the CVC program. NMOSFET characteristics were measured on transistors with W/L=150/10 μm.

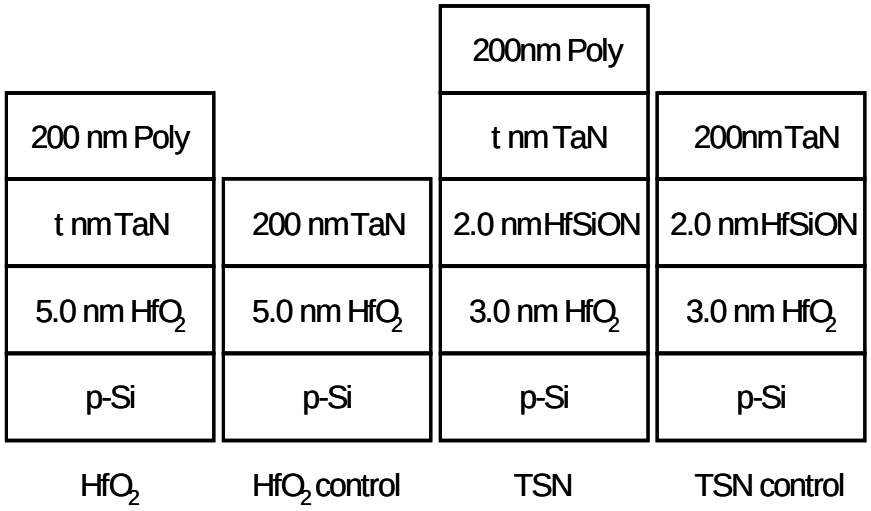


Fig.3.1 Gate stacks for both dielectric structures: HfO_2 and TSN. t=5, 10, 15 and 20 nm for TaN thickness.

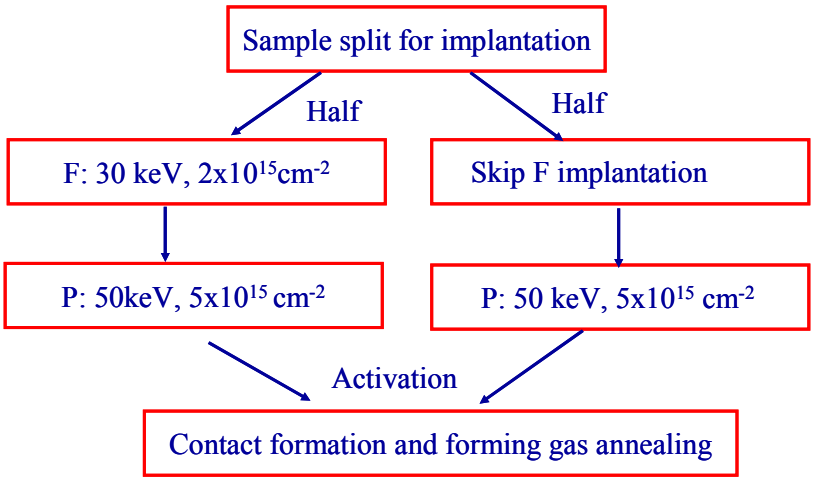
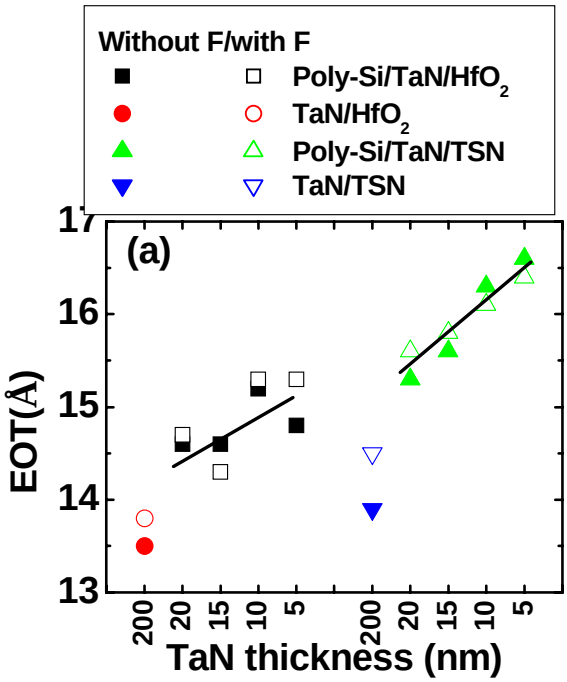


Fig.3.2 process splits

3.4 Results and discussion

Fig.3.3 (a) shows EOT versus TaN thickness for both dielectric structures (HfO_2 and TSN). For both cases, TaN-only (i.e. without poly-Si) control sample exhibited the lowest EOT value. EOT increased with decreasing TaN thickness in poly-Si/TaN gate electrodes. As TaN layer and poly-Si were deposited in different systems, oxygen might be absorbed on the surface of the poly-crystal TaN and diffused into the dielectric layer during poly-Si deposition. The possibility increased for thinner TaN layers. TaN-only device skipped this step and thus, had the smallest EOT. The leakage current density (J) at V_g-V_{fb}=-1 V was found to increase with decreasing TaN thickness in both gate structures

(Fig.3.3(b)). Incorporating F reduced the leakage current by more than half an order of magnitude. The anomalous increase of the leakage current with increasing EOT was due to the reaction in gate stacks. One possibility is that in devices with thin TaN layers, both O and Ta atoms diffused into the dielectric layer and led to higher EOT and leakage current density. Similar trend has also been observed in TaN formed by chemical vapor deposition [9].



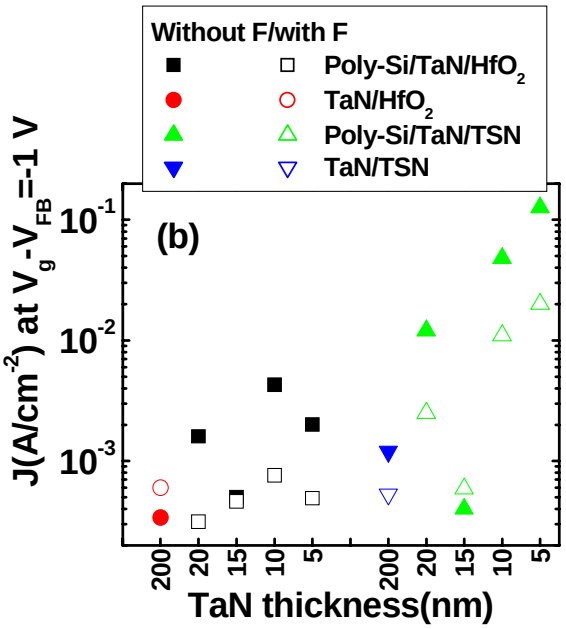


Fig.3.3 (a) EOT and (b) leakage current density versus TaN thickness for both dielectric structures (HfO_2 and TSN).

Fig.3.4 compares the channel mobility of NMOSFETs without and with F incorporation for both HfO_2 and TSN gate structures. As can be seen, in F-incorporated device, the mobility increased with decreasing TaN thickness in HfO_2 structure, while it did not change very much in TSN structure. Nearly 200% mobility improvement was obtained in the HfO_2 NMOSFET with 5 nm TaN in comparison to the TaN-only control device. This suggests that F atoms diffused through TaN to passivate HfO_2 and the interface, while they were blocked in the TSN structure. For TaN-only devices, the F passivation came

from implanted F atoms in the source and drain region, they only passivated the side walls of the gate. Thus, their efficiency was not as good as F atoms which diffused through the thin TaN layer into high-k dielectrics in the TaN/poly-Si devices.

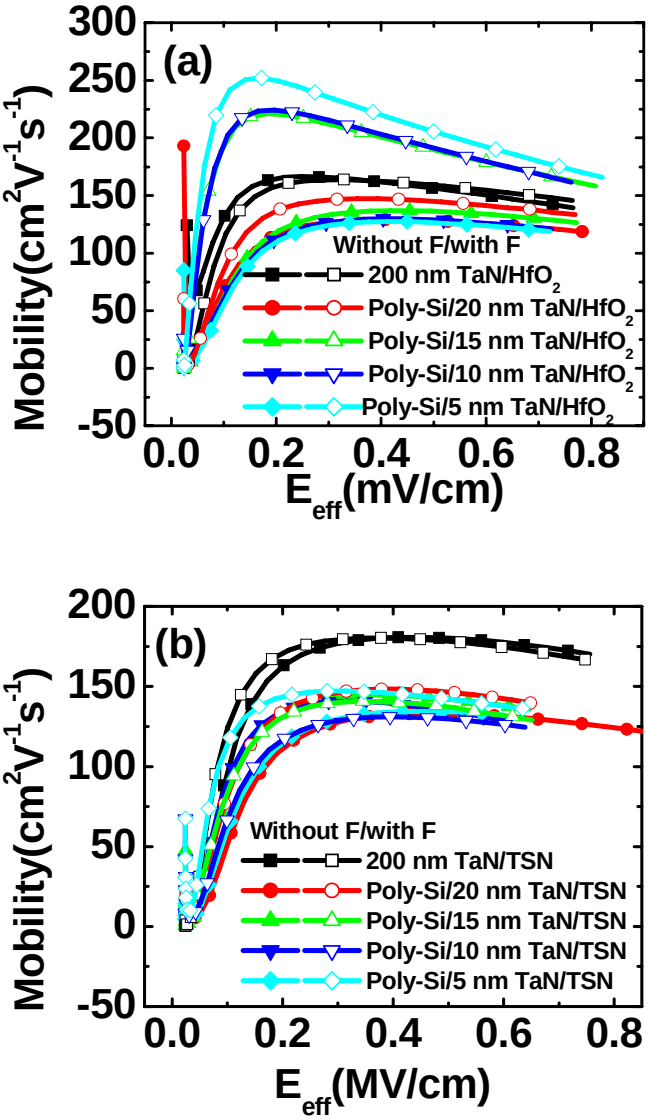


Fig.3.4 Channel mobility of NMOSFETs without and with F incorporation for both (a) HfO_2 and (b) TSN gate structures.

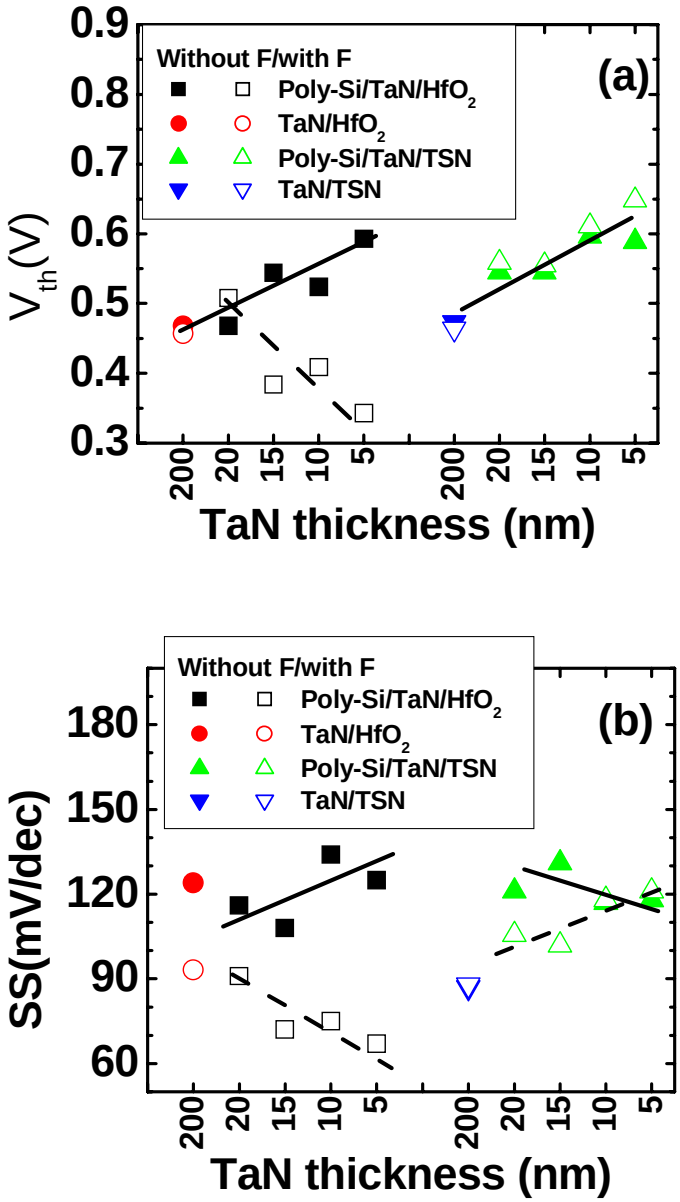


Fig.3.5 (a) Threshold voltage (V_{th}) and (b) subthreshold swing (SS) versus TaN thickness without and with F incorporation

Fig.3.5(a) shows the threshold voltage (V_{th}) with TaN thickness without and with F incorporation. Without F incorporation, V_{th} increased with decreasing TaN thickness in HfO_2 NMOSFETs, while with F incorporation, V_{th} decreased significantly with decreasing TaN thickness. In contrast, V_{th} changed very little in the TSN structure without and with F incorporation. These results support the contention that the F atoms are blocked by HfSiON layer. Fig.3.5 (b) presents the effect of F incorporation on the threshold swing (SS). It decreased greatly in HfO_2 NMOSFETs with decreasing TaN thickness. For the TSN structure, SS improved slightly in transistors with thicker TaN thickness. This improvement might come from the F passivation on the side walls of the gate, because the number of F atoms which diffused through a thicker TaN layer should be smaller.

In order to locate F atom distribution in devices, cross-section transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) mapping have been done on the devices with 10 nm TaN layer. EELS mapping was performed in the TEM mode with the energy filter set at the K edge (685 eV) of fluorine, Fig.3.6 presents pictures of high resolution TEM and F distribution mapping in both HfO_2 ((a) and (b)) and TSN structure ((c) and (d)). The thickness of TaN layer is 9.1 nm determined from another thinner specimen, in which Si substrate became amorphous after focused ion beam (FIB) cutting. Thus, in HfO_2 structure, the thickness of HfO_2 layer was 6.4 nm;

in TSN structure, the total thickness of dielectric layer was 7.1 nm. The thickness of F distributing layer is 15.5 nm in HfO_2 structure (Fig.3.6(b)), which was equal to the total thickness of both TaN and HfO_2 layer in Fig.3.6(a). In order to have enough F atoms to diffuse to the dielectric-substrate interface, thinner TaN layer is better. In contrast, the thickness of F distributing layer is 13.8 nm in TSN structure (Fig.3.6(d)), which was smaller than the total thickness of both TaN and TSN dielectric layers in Fig.3.6(c). F atoms were blocked by HfSiON layer and could not reach the interface between the gate dielectric and Si substrate.

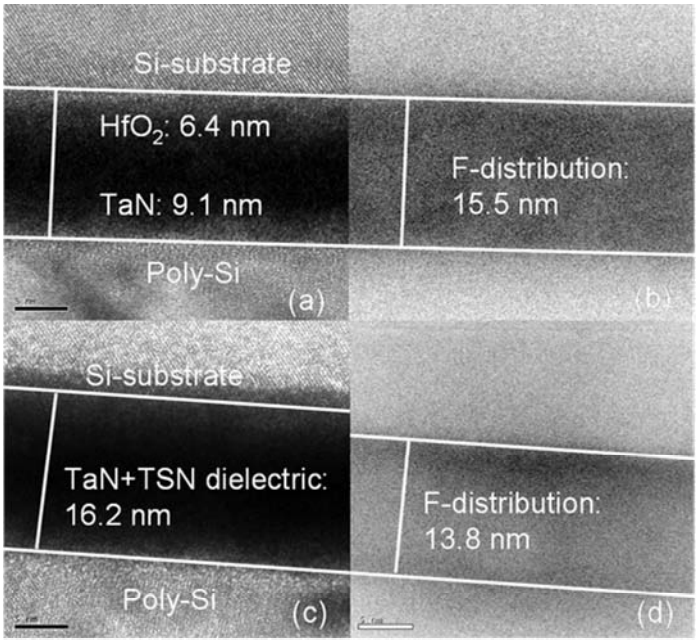


Fig.3.6 High resolution TEM and F distribution mapping in both HfO_2 ((a) and (b)) and TSN structure ((c) and (d)).

3.5 Summary

In summary, F passivation in poly-Si/TaN/HfO_2 (and TSN)/Si gate stacks through gate implantation has been studied. When TaN thickness was less than 15 nm, the channel mobility and the threshold swing improved significantly for HfO_2 NMOSFETs. In contrast, there was very little performance improvement for HfSiON/HfO_2 (TSN) NMOSFETs due to the blocking of F atoms by the HfSiON layer so that F atoms could not reach to the interface. Further study is needed to improve the stability of the thin TaN layer.

3.6 References

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Chapter 4

Literature Review of Fermi-level Pinning Mechanisms in a High-k Gate Stack

4.1 Overview

As we discussed in chapter 1, there are three mechanisms of Fermi-level pinning: The dipole formation at the interface between metal gate and high-k dielectric due to hybridization.

(1) The dipole formation through oxygen vacancy (Vo) mechanism, which is especially important for poly-Si gate and p-metal gate after high-temperature anneals.

(2) The dipole formation at the interface between high-k dielectric and interfacial SiO_2.

All three mechanisms were identified but not fully understood. In this chapter, we want to review some studies on these mechanisms in order to understand the mechanism of the V_{fb} shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2 based dielectrics. We will review the status of studies on the Vo mechanism and point out some drawbacks in Shiraishi's model. Finally, a general expression of flatband voltage with a dipole layer and a bulk charge distribution in the dielectric is introduced.

4.2 Fermi level pinning mechanisms

4.2.1 The dipole formation at the interface between metal gate and high-k dielectric due to hybridization

A model based on Tersof's theory of the metal-semiconductor interface was proposed by Yeo *et al* to describe the metal-dielectric interface [1, 2]. In this model, the effective metal work function was purely determined by the charge neutrality level (ϕ_{CNL}) and the electronic component (ε_{∞}) of dielectric constant of the dielectric material. The model can explain some trends, but it can not explain some phenomena at the interface between metal and high-k dielectric. For example, W/HfO_2, Pt/HfO_2 and Pt/La_2O_3 interfaces show very different characteristics after forming gas anneals (FGA) and oxygen gas anneals(OGA) at 250~450 ^{o}C. Later Shiraishi *et al* points out the concept of conventional ϕ_{CNL} is only applicable when the metal induced gap states (MIGS) penetrate sufficient deep into a dielectric and the metal density of states (DOS) is featureless [3]. In HfO_2, the MIGS penetration length is only 1~2 atomic layers and the occupied DOS is much larger than the unoccupied DOS in typical p-metals. A generalized charge neutrality level (ϕ^{G}_{CNL}) was proposed based on metal-dielectric hybridization by Shiraishi *et al* [3]. However, this new model has not been compared with experimental data quantitatively and extensively.

Experimentally, the most used method to study this dipole is to use V_{fb}-EOT analysis to extract metal effective work function (EWF). A new method is

proposed to extract the EWF by measuring XPS binding energy shift [4]. However, this method is not fully developed yet. The difficulty in this method is to distinguish the binding energy shift caused by the Fermi level change from that caused by the chemical shift. We will discuss it in chapter 8.

.

4.2.2 The dipole formation through oxygen vacancy mechanism in high-k dielectrics

The Vo mechanism was proposed by Shiraishi *et a*l [5-7], and by Guha *et al* [8]. Although the FLP through Vo formation is getting accepted by a lot of people, its full process and theoretical foundation have not been established yet. In the following, I will show some drawbacks in Shiraishi's model.

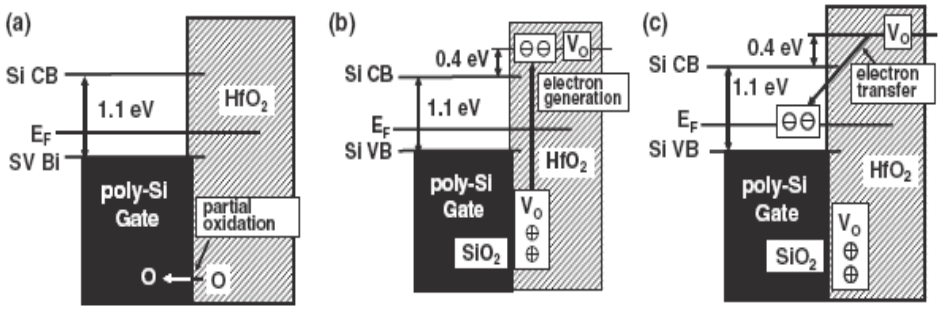


Fig.4.1 Schematic illustrations of Vo formation in HfO_2 with partial oxidation of poly-Si gate and sequent electron transfer into the gate electrodes. (a) Partial poly-Si oxidation by pulling out an O atom from HfO_2. (b) Two electron generation inside the HfO_2 region. (c) Subsequent electron transfer into the poly gate [6].

Fig.4.1 shows the Vo model in poly-Si/HfO_2 system proposed by Shiraishi [6]. The caption is directly taken from Ref. [6]. According to Shiraishi's model, the dipole formation process in the Vo mechanism progresses as following [6]:

(1) Partial poly-Si oxidation by pulling out an O atom from HfO_2, which can be understood to take place in 3 steps:

- An oxygen vacancy generates in HfO_2 (positive or neutral?).
- An interstitial oxygen atom diffuses through HfO_2 and through the interface into Si (How does it diffuse?).
- O+Si$\rightarrow$ Si oxidation (It gets the energy from the electron transfer which happens at a later time?).

(2) Two electrons generate at the vacancy energy level in HfO_2.

(3) The two electrons transfer from the oxygen vacancy energy level in HfO_2 to the poly-Si valence band by generating and transferring energy to the reaction of O+Si$\rightarrow$ silicon oxide. In the end, a positive charged Vo^{2+} is formed in HfO_2 (Note: the formation energy of a Vo^{2+} is smaller than that of a neutral Vo^0 in HfO_2 from *ab initio* computation).

(4) The two electrons in the poly-Si valence band form a dipole with the positive charged Vo^{2+} in HfO_2.

It is easily seen that there are a lot of logical problems in above argument. How a Vo generates in HfO_2 at first and how the oxygen atom from

the Vo site diffuses in HfO_2 are not clear here. How is the energy generated by electron transfer give to the Si oxidation reaction supposed to happen at an earlier time according to the argument? How do the two electrons still keep the correlation with the oxygen atom after they are separated in space? In my opinion, it is possible unless the negatively charged interstitial oxygen ion is the diffusion specie in HfO_2 and SiO_2. If so, how does it enhance the Si oxidation?

Guha *et al* have studied the V_{fb} shift of $Re/HfO_2/SiO_2/p\text{-}Si$ after annealing in oxygen gas with varying pressure and temperature [8]. A rate equation model based on the Vo formation in HfO_2 and the atomic oxygen diffusion was established. The extracted V_{fb} shift and interfacial SiO_2 growth versus oxygen pressure were in good agreement with experimental data. The model describes the oxygen exchange between metal gate and HfO_2, and between the dielectric and the interfacial SiO_2. However, oxygen interstitials (O_I) is not mentioned. The rate constants were not quantified, either. As they govern the kinetics of different processes of defects, it is very important to explore their dependence on the temperature, formation energies and diffusion mechanisms of defects further.

Comparing with Guha's model, Shiraishi' model suggests if the negative charged oxygen ions are the diffusion oxygen species in the interfacial SiO_2, they might be important to reduce the activation energy of Si oxidation reaction compared to neutral oxygen molecules. There are a lot of theoretical studies on

the characteristics of different defect species in HfO_2: oxygen vacancies (Vo) and oxygen interstitials (O_I) [9-12]. The diffusion oxygen species might be different in HfO_2 and SiO_2, as the formation energy and the diffusion barrier of a defect (both Vo and O_I) change from HfO_2 to SiO_2 [12, 13]. In addition, their values also decrease with decreasing the distance from the defect to HfO_2/Si interface [14-18]. The direct experimental studies of oxygen diffusion in HfO_2 and ZrO_2, and the interfacial SiO_2 growth in the HfO_2/Si system have also been performed [19-22]. Atomic oxygen species have been proposed to diffuse through the crystal HfO_2 in the exchange mechanism and proved to be one of mechanisms in real gate stacks. Other mechanisms such as oxygen diffusing through grain boundaries [19, 23, 24] or the OH-group [20] in HfO_2 have also been proposed based on experimental studies. For the interfacial SiO_2 growth, it is important to compare diffusion mechanisms of different oxygen species in both HfO_2 and SiO_2 experimentally, which is not very clear yet. The energy gain of Si oxidation due to the electron transfer proposed by Shirashi *et al* has not been proved yet. Nevertheless, the Vo mechanism of FLP is getting more and more theoretical and experimental support. Fig.4.2 shows the Vo mechanism of FLP in a metal/high-k (HfO_2)/Si system schematically. Future work needs to compare and identify diffusion mechanisms of different oxygen species in both HfO_2 and SiO_2. A better equation is needed to describe the whole process.

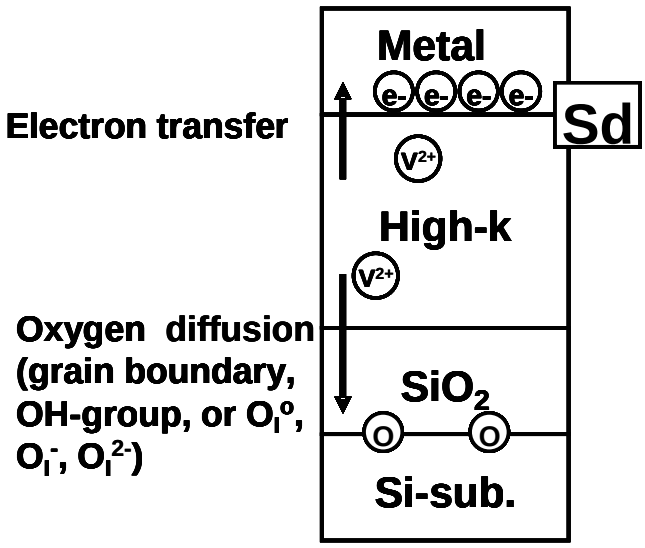


Fig.4.2 The dipole formation (**Sd**) through Vo mechanism in a meteal/high-k (HfO_2)/Si system. Vo^{2+} is the most stable specie among the neutral and charged oxygen vacancies in HfO_2. Oxygen diffuses to Si substrate by several possible mechanisms: grain boundary, OH-group or interstitial atomic oxygen (O_I^0, O_I^-, O_I^{2-}). Electrons transfer to gate metal leaving Vo^{2+} in HfO_2. The Coulomb interaction between electrons and Vo^{2+} gives rise to the dipole (**Sd)**.

In above discussion, Vo is formed during high temperature annealing. If an oxygen deficiency is generated in a high-k dielectric layer during the deposition, then a dipole can form by electron-only transfer.

A direct evidence of dipole formation through Vo mechanism was observed in HfO_2 deposited under an oxygen deficient condition using x-ray photoelectron spectroscopy (XPS). In Ref. [25], HfO_2 films were deposited on a

p-Si (100) substrate at a temperature of 700 °C using 3 Hz pulses of an excimer laser (λ=248 nm) with an intensity of 0.75 J /cm^2. The laser pulses were targeted on the stoichiometric HfO_2 pellet under a base pressure of 2×10^{-8} mbar. The *in situ* XPS measurements were performed using a Mg *Kα (*1253.6 eV) source. To circumvent band-bending and charging-related effects, all the spectra were aligned so that the Si 2*p* peak from the substrate is fixed at a binding energy (BE) of 99.3 eV. Fig.4.3 shows relative XPS spectra of (a) Hf 4*f* and (b) Si 2*p* core levels of the HfO_2/SiO_2 /p-Si system as a function of the HfO_2 deposition time (thickness).

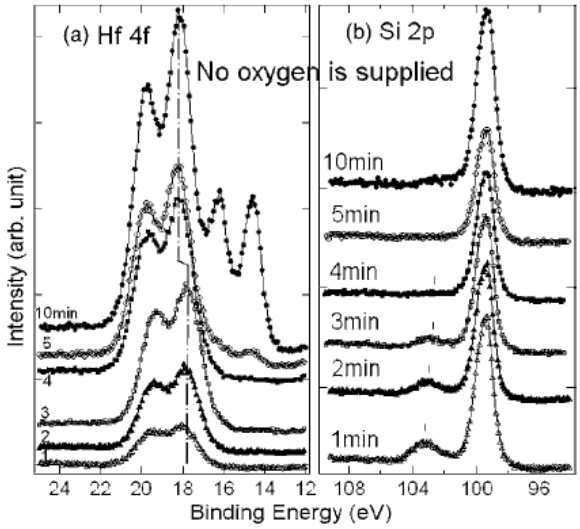


Fig.4.3 Relative XPS spectra of (a) Hf 4*f* and (b) Si 2*p* core levels of the HfO_2/SiO_2 /p-Si system as a function of the HfO_2 deposition time (thickness). The equivalent film thicknesses are about 2, 5, 8, 11, 14, and 31 Å for deposition times of 1, 2, 3, 4, 5, and 10 min. No additional oxygen was supplied during the

pulsed laser deposition (PLD). The shift of the Hf 4*f* main peak is shown with a guideline, which reflects the transition from Hf silicate to oxygen deficient $HfO_{x<2}$. All the spectra were aligned so that the Si 2*p* peak from the substrate is fixed at a binding energy (BE) of 99.3 eV.

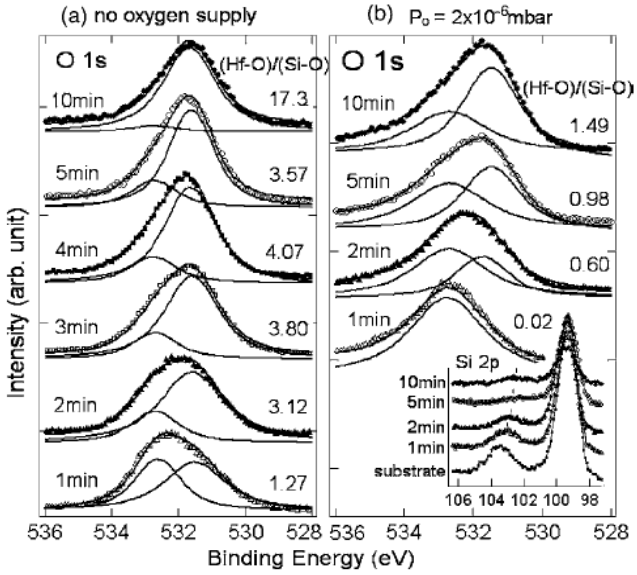


Fig.4.4. XPS O 1*s* spectra of the HfO_2 /SiO_2 /Si system prepared under two conditions: (a) no additional supply of oxygen and (b) oxygen supply at a partial pressure of $Po=2\times10^{-6}$ mbar. Each spectrum is fitted by two Voigt functions that correspond to the Hf–O bond and Si–O bond. The intensity ratio is shown at the upper-right corner of each spectrum. Si 2*p* spectra for the same oxygen pressure are shown in the inset of (b).

Fig.4.4 shows XPS O 1*s* spectra of the HfO_2 /SiO_2 /Si system prepared under two conditions: (a) no additional supply of oxygen and (b) oxygen supply at a partial pressure of $Po=2\times10^{-6}$ mbar. From both Fig.4.3-4, it is concluded

that the absolute binding energy Si^0 2p should decrease. This decrease was due to electron transfer from oxygen vacancy (Vo) in HfO_2, which caused the Fermi level to shift up at the Si interface. It is a direct evidence of the dipole formation through the Vo mechanism.

4.2.3 The dipole formation at the interface between high-k dielectric and interfacial SiO_2

We will propose the mechanism when we study the negative flatband-voltage (V_{fb}) shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2 based dielectrics. We will talk about this in chapter 5, 6, 7, and 8 in detail. It will be shown that among MeHfO, MeSiO and the dipole at the interface of metal gate and high-k dielectrics, none is the reason of negative flatband voltage shift. A MeSiO layer forms between Me_2O_3 and the interfacial SiO_2 layer, and a dipole is proposed to form at the interface between the MeSiO layer and the interfacial SiO_2 layer. An XPS (X-ray photoelectron spectroscopy) study of Gd_2O_3 capping on SiO_2 indicates clear Si, O and Gd related bonding configuration change at the interface between Me_2O_3 (or MeSiO) and the interfacial SiO_2. So the bonding configuration change is the root cause to the dipole formation. When there is an oxygen deficiency in Me_2O_3, another dipole through Vo mechanism is observed to form and causes V_{fb} to shift negatively.

In Ref [26], the direct contact HfO_2/Si interfaces, which has virtually no interfacial SiO_2 layer, is shown to exhibit characteristic interface-charge

distribution. Such interfaces demonstrated a negative V_{fb} shift that is reduced by the insertion of a ~0.5nm-thick SiO_2 layer. It was proposed that the observed negative V_{fb} shift is mainly caused by an electrostatic dipole (0.5V) formed at the HfO_2/Si interface rather than fixed charges. In our study, interfacial SiO_2 layers thicker than 1.2nm are used, so such a dipole formation at the direct contact HfO_2/Si interfaces is not expected to happen.

4.3 Flatband voltage of a metal-oxide-semiconductor capacitor with a dipole in the gate stack

Now we want to talk about the flatband voltage of a metal-oxide-semiconductor capacitor (MOSCAP) with a dipole in the gate stack. The following analysis is mostly based on the work of Hickmott [27].

The gate voltage V_G of a MOSCAP is generally obtained by an inspection of the electron energy band diagram (Fig.4.5(a)). For p-silicon substrate, if there is neither charge in surface states Q_{SS} nor bulk charge in the oxide $\rho(x)$,

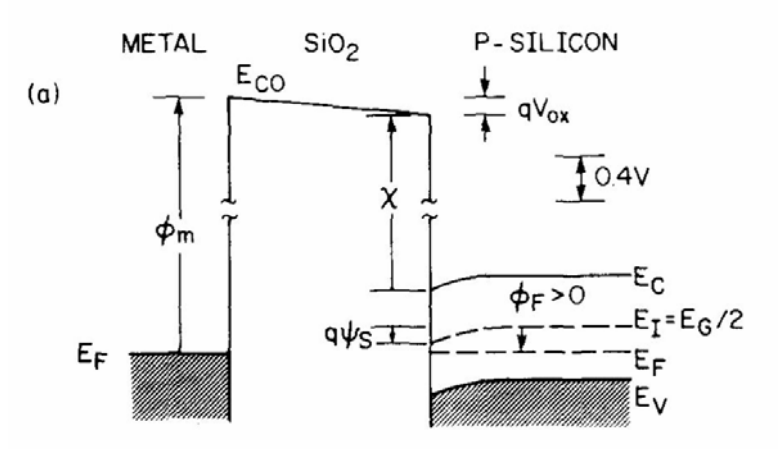
$$qV_G=\phi_m-(\chi+1/2E_G)+q\psi_S-q\phi_F+qV_{ox}, \qquad (1)$$

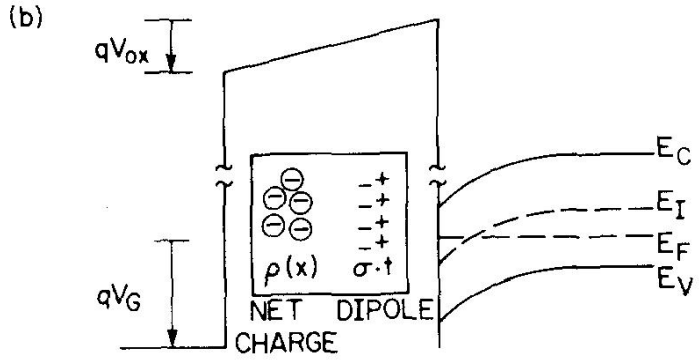
where ϕ_m is the metal-insulator work function, the energy to raise an electron from the metal into the conduction band of SiO_2, χ is the electron affinity of the silicon-SiO_2 interface, the energy to raise an electron from the conduction band of silicon E_C to the conduction band of SiO_2, E_{CO}, V_{ox} is the potential drop across the insulator layer, E_G is the band gap of silicon, ψ_S is the surface

potential of the silicon measured from the intrinsic Fermi level E_I, and q is the magnitude of the electron charge. The Fermi potential is given by

$$\phi_F=(kT/q)\ln[N_A/n_i(T)], \qquad (2)$$

where N_A is the number of acceptors per cm^3, $n_i(T)$ is the intrinsic number of carriers per cm^3, T is the absolute temperature and k is Boltzmann's constant. The units of ϕ_m, χ and E_G are electron volts while ψ_S, ϕ_F, V_G and V_{ox} are in volts.





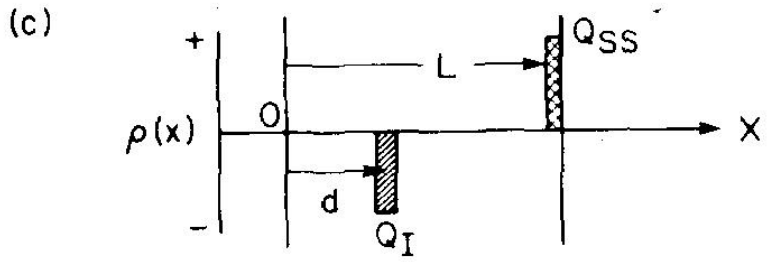


Fig. 4.5 (a) Schematic energy-band diagram for a metal-SiO_2-semiconductor capacitor on a p-silicon substrate. (b) Energy band diagram with applied bias, and with schematic dipole layer and charge distribution in the oxide, (c) Schematic charge distribution with charge centroid in the oxide Q_I and charge in surface states Q_{SS} [27].

The work function difference ϕ_{ms} with respect to the intrinsic energy level E_I, can be defined as

$$q\phi_{ms} \equiv \phi_m - (\chi + 1/2E_G). \qquad (3)$$

At flatband voltage V_{fb}, there is no net charge in the silicon, $\psi_S = 0$, so

$$V_{fb} = \phi_{ms} - \phi_F + V_{ox}, \qquad (4)$$

for an insulator with no bulk charge $\rho(x)=0$, but with the charge Q_{SS}/cm^2 at the Si-SiO_2 interface.

With $V_{ox} = -Q_{SS}/C_{ox,}$ Eq.4 can be rewritten as

$$V_{fb} = \phi_{ms} - \phi_F - Q_{SS}/C_{ox} = \phi_{ms} - \phi_F - Q_{SS}(L/\varepsilon_{ox}), \qquad (5)$$

where L is the oxide thickness, ε_{ox} is the dielectric constant of SiO_2, and C_{ox} is the oxide capacitance. Q_{SS} includes both fixed charges and charges in interface states.

Usually an electron at rest in vacuum, far removed from a metal surface, is defined to have zero energy. A metal is characterized by its work function ϕ_e which is the difference in energy of the metal when one electron is removed from the Fermi level of the metal at 0^o K and placed away from the influence of the metal. An insulator and a semiconductor are characterized by an energy gap E_g and by an electron affinityχ, which is the energy to remove an electron from the bottom of the conduction band to infinity. When three components (metal, oxide, and semiconductor) of a MOSCAP are joined together, charges in the system adjust until the Fermi level of metal and semiconductor are at the same energy with respect to vacuum: $\phi_m=\phi_e-\chi_{SiO2}$, and $\chi,=\chi,_{Si}-\chi,_{SiO2}$.

If the bulk charge $\rho(x)$ is not zero (Fig.4.5(b)), it gives a shift of V_{fb}:

$$\Delta V_{fb}=-1/(LC_{ox})\int x\rho(x)dx. \qquad (6)$$

The integration region of Eq.6 is from 0 to L. The integral can be approximated by a centroid of charge Q_I at a distance d from the metal-SiO_2 interface [27]:

$$\Delta V_{fb}=(d/L)(Q_I/C_{ox}). \qquad (7)$$

A dielectric can support a dipole layer. An ideal dipole layer in a dielectric is a sheet of positive charge of density σ/cm^2 separated by a distance t from a sheet

of negative charge of equal magnitude, as shown in Fig. 4.5 (b). Such a configuration has no net charge but adds a term to V_{fb},

$$\Delta V_{fb}=-\sigma t/\varepsilon_{ox}, \qquad (8)$$

which is independent of oxide thickness. A dipole layer can exist at either an interface or at any position in the dielectric. We will study the dipole layer at the metal/dielectric interface in chapter 6-9 and the dipole layer at Me_2O_3 (Me=Gd, Y and Dy) and SiO_2 interface in chapter 7-9. Iwamoto *et al* have shown the dipole formation at Al_2O_3/SiO_2 interface [28]. The V_{fb} shift is shown to saturate at 1.0nm of Al_2O_3, which gives an estimate to t. Eq.8 is not valid to the dipole formation through Vo mechanism, as Vo's are distributed in the whole dielectric layer [8].

By combining different cases, a general expression for V_{fb} of a MOSCAP can be written as

$$V_{fb}=\phi_{ms}-\phi_F-\sigma t/\varepsilon_{ox}-(d/L)(Q_I/C_{ox})-Q_{SS}(L/\varepsilon_{ox}). \qquad (9)$$

For each dipole, a term is needed to add in Eq.9. For high-k dielectric layer, the above equation is still valid.

4.4 Summary

In summary, there are three FLP mechanisms in high-k gate stacks. Even though a lot of studies have been done, more works need to do to in order to have a better understanding of FLP mechanisms.

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Chapter 5

Literature Review of Studies on Oxides of Lanthanides as High-k Gate Dielectrics

5.1 Overview

In this chapter, we want to review some literature studies on oxides of lanthanides (Me_2O_3) as high-k gate dielectrics. These metal oxides have some similar properties, so the mechanism of the V_{fb} shift might be from the same origin. Comparing these oxides together gives a clue to the physical mechanism. We find that it is necessary to consider two dipoles together: the dipole at Me_2O_3/SiO_2 interface and the dipole at metal/high-k dielectric interface.

5.2 Introduction

Capping a thin layer of Me_2O_3 (including HfLaO) on SiO_2 and HfO_2 based high-k dielectrics with metal gates such as TaN, TiN and TaC, the V_{fb} has been shown to shift to the negative direction after high temperature annealing. However, capping a layer of HfLaO on SiO_2 with Pt metal gate, the V_{fb} has been shown to shift to the positive direction after high temperature annealing. With different models in literature, a contradiction appears in explaining the behavior

of the V_{fb} shift for HfLaO [16, 17]. Several mechanisms have been proposed: (1) the dipole change at metal/high-k dielectric interface, (2) the formation of a dipole due to the doping of HfO_2, (3) the formation of a silicate layer ($Me_xSi_yO_z$). In this chapter, we want to review some literature studies on oxides of lanthanides (Me_2O_3) as high-k gate dielectrics. By comparing these oxides together, we will get a clue to the physical mechanism of V_{fb} shift.

When oxides of lanthanides or lanthanides are deposited on a Si substrate directly, oxygen atoms can easily diffuse to Si to cause enhanced Si oxidation. The metal atoms near the Si interface can weak Si-Si bonds [1, 2]. When lanthanides are deposited on a SiO_2 buffer layer, they can reduce SiO_2 to form silicide, silicate and oxides of lanthanides [3]. In this chapter, we want to review some literature results using oxides of lanthanides as a capping layer to modulate the effective work function of metal gates. We consider four oxides: Y_2O_3, Gd_2O_3, Dy_2O_3 and La_2O_3.

5.3 Literature studies on Y_2O_3, Gd_2O_3, Dy_2O_3 and La_2O_3

Y_2O_3

Material properties of Y_2O_3, silicide (YSi) and silicate (YSiO) such as XPS and CV characterization have been studied [4, 5]. Structural defects in the interfacial SiO_2 on the $Y_2O_3/SiO_2/Si$ stack has been studied by Auger electron

spectroscopy [2]. [SiO_4] with smaller size (4-5) rings were identified at the interface between SiO_2 and Y_2O_3. NMOSFETs with a smaller threshold voltage (V_{th}) compared to the HfO_2 control device through Y_2O_3 capping on SiO_2 and HfO_2 were reported in Ref. 6 with TaN metal gate and Ref. 7 with Ni-silicide metal gate.

Gd_2O_3

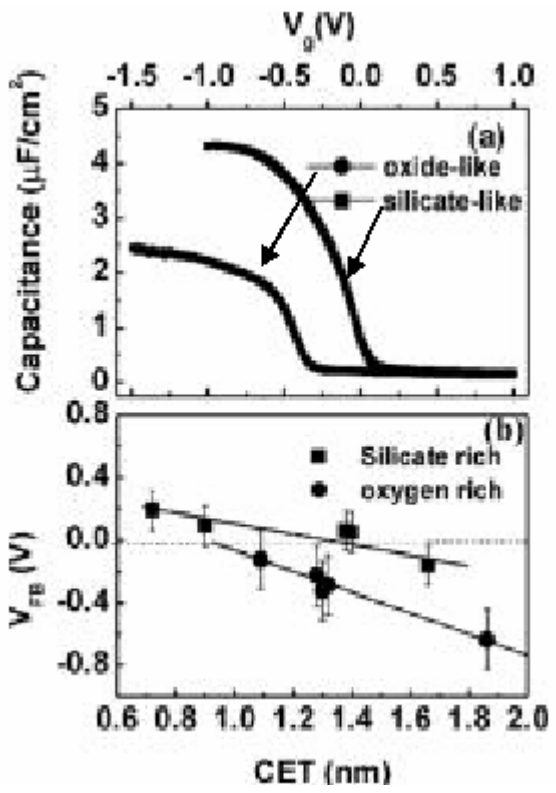


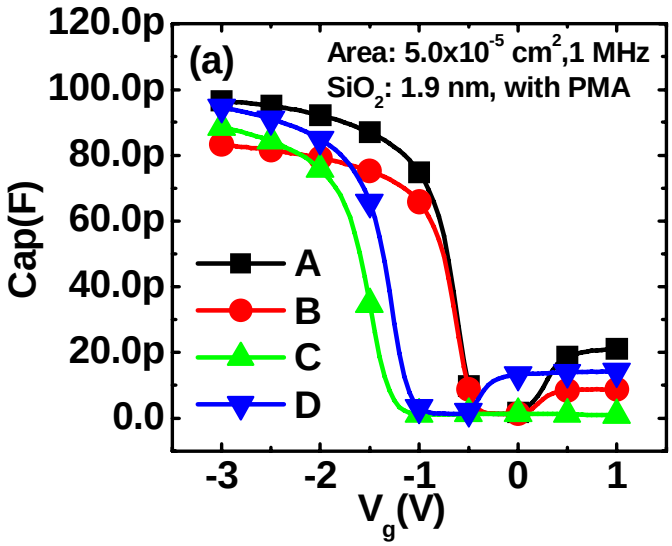
Fig.5.1 (a) CV characteristics of 4.2nm thick Gd_2O_3 thin films with oxide and silicate-like interfaces on p-type Si substrates, measured at 10kHz. (b) The

dependence of V_{fb} on the capacitance equivalent thickness (CET) for the Gd_2O_3 layers on p-Si with two different interfaces.

Material properties of Gd_2O_3, silicide (GdSi) and silicate (GdSiO) such as XPS have been studied in [1]. Laha *et al* have studied Gd_2O_3 growth using molecular beam epitaxy (MBE) [8]. By controlling growth conditions, they could grow Gd_2O_3 with and without (almost) an interfacial SiO_2 layer. They called them oxide-like and silicate-like, respectively. Fig.5.1 shows CV characteristics of 4.2nm thick Gd_2O_3 thin films with oxide and silicate-like interfaces on p-type Si substrates [8]. The result indicates the existence of SiO_2 is necessary for the negative V_{fb} shift. NMOSFTETs with a bilayer gate stack structure of TaN/Gd_2O_3/HfO_2/p-Si have been successfully demonstrated [9]. The devices showed a negative V_{fb} shift compared to the HfO_2-only device.

We have designed the metal-oxide-semiconductor capacitors (MOSCAPs) with following structures: A) TaN/5.0nm HfO_2/1.9nm SiO_2/p-Si; B) TaN/1.5nm Gd_2O_3/3.5nm HfO_2/1.9nm SiO_2/p-Si; C) TaN/5.0nm Gd_2O_3/1.6nm SiO_2/p-Si; D) TaN/1.5nm HfO_2/3.5nm Gd_2O_3/1.9nm SiO_2/p-Si. The resistivity of p-Si (001) substrates is 5~22 Ohm cm. The bottom SiO_2 layer is thermally grown in a furnace at 700 ^oC. TaN is deposited by DC reactive sputtering. Post metal-deposition anneal (PMA) is performed at 900^oC/1min/N_2. Fig.5.2 shows 1 MHz CV curves and V_{fb} values after PMA. It can be seen that as the Gd_2O_3 layer in B was isolated from the bottom SiO_2, the V_{fb} value was almost the same as the

HfO_2-only stack in A. In C and D, as the Gd_2O_3 layers contact SiO_2 directly, V_{fb} values shift to the negative direction. The result suggests that negative V_{fb} is due to direct contact interaction between Gd_2O_3 and the interfacial SiO_2.



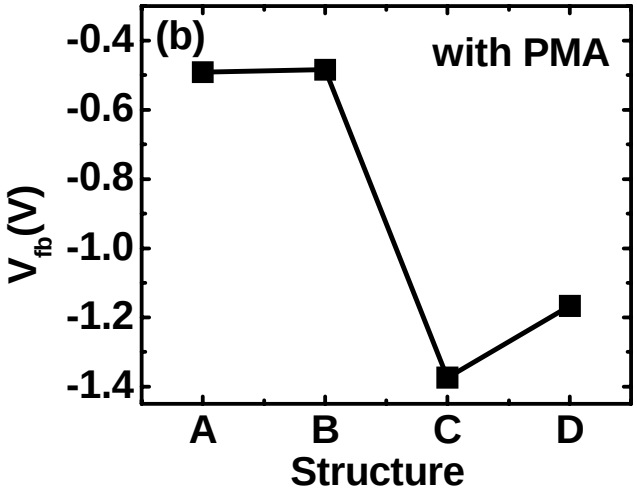


Fig.5.2 1 MHz CV curves and V_{fb} values of MOSCAPs with structure A, B, C, and D after PMA ($900^{o}C/1min/N_2$).

Dy_2O_3

NMOSFETs with low V_{th} have also been demonstrated through Dy_2O_3 capping with Mo(O, N) [10], TaC_x [11] and TaN [12] metal gates.

La_2O_3

La_2O_3 as a gate oxide has been studied extensively. Oxidizing a La metal layer on a Si substrate directly without a SiO_2 buffer resulted in voids and a rough interface [13]. When La metal was deposited on a 1.1nm SiO_2 buffer, the solid-reaction between La and SiO_2 resulted in a high quality LaSiO oxide layer.

NMOSFETs with La_2O_3 capping and TiN (or TaN) metal gates have been fabricated [14-16]. Both NMOSFETs and PMOSFETs with HfLaO gate dielectrics have been demonstrated in [17, 18]. Fig.5.3 shows *C–V* curves for MOS HfO_2 and HfLaO capacitors with different La concentrations [17]. For a p-Si substrate with TaN metal gate, the V_{fb} of a HfLaO (15% and 50% La composition) capacitor was shown more negative than a HfO_2 capacitor. For a n-Si substrate with Pt metal gate, the V_{fb} of a HfLaO (50% only) capacitor was shown more positive than a HfO_2 capacitor.

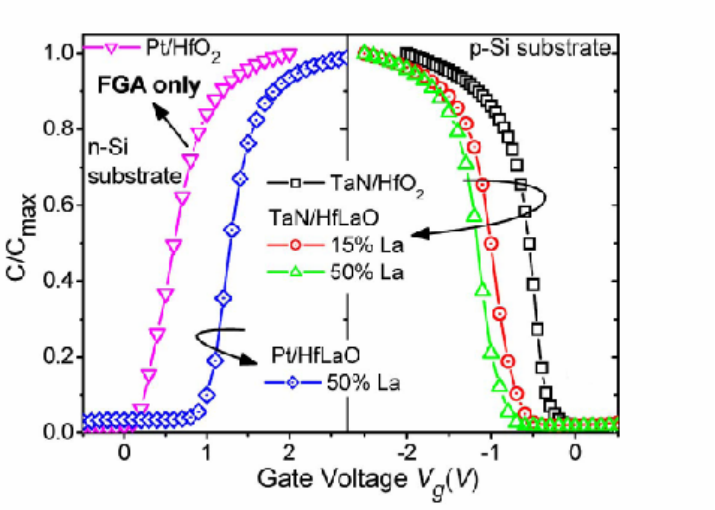


Fig.5.3 Comparison of typical *C–V* curves for MOS HfO_2 and HfLaO capacitors with different La concentrations (La concentrations of 50%, 15%, and 0%, respectively) after a PMA of 1000-^{o}C RTA/5s. Pt/HfO_2/n-Si was only subjected to FGA at 420 ^{o}C for 30 min. Obvious V_{fb} shift can be seen after La incorporation. (Note: Doping concentration for both p- and n-substrates is 6×10^{15} cm^{-3}) [17].

Ohmori *et al* have studied MOSCAPs of La_2O_3 on p-Si substrates with W and Pt metal gate [19]. Fig.5.4 shows V_{fb} dependence on annealing ambient as a function of the Pt composition ratio R_{Pt} in the W-Pt electrode [19]. A much larger positive V_{fb} shift for Pt/La_2O_3 compared to Pt/HfO_2 was observed after an oxygen gas annealing (OGA) sequent to a forming gas annealing (FGA).

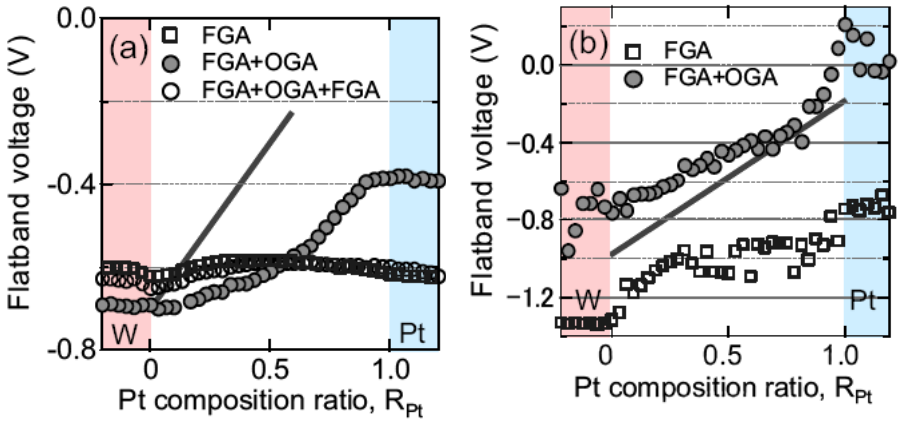


Fig.5.4 V_{fb} dependence on annealing ambients as a function of the Pt composition ratio R_{Pt} in a Pt-W electrode. (a) HfO_2 dielectric film after FGA and OGA (300°C). (b) La_2O_3 dielectric film after FGA and OGA (300°C). A much larger positive V_{fb} shift for Pt/La_2O_3 compared to Pt/HfO_2 after an OGA sequent to a FGA was observed [19].

5.4 Comparison of different oxides of lanthanides

By comparing the results about Y_2O_3, Gd_2O_3, Dy_2O_3 and La_2O_3, it seems that the interaction between SiO_2 and Me_2O_3 is the reason of the negative V_{fb} shift for gate stacks with TaN, TiN, MoON and TaC. Sivaramani *et al* have proposed a dipole model for the interaction between SiO_2 and Me_2O_3 [16]. For La_2O_3 gate stacks with Pt, the dominant contribution to the positive V_{fb} shift is from Pt/La_2O_3 interface after an OGA. Thus, in order to understand the V_{fb} shift of a gate stack with a thin layer of Me_2O_3 (Me=Gd, Y, Dy and La) capped on the

Hf-based high-k dielectric layers, we must consider two dipoles: the dipole at Me_2O_3/SiO_2 interface and the dipole at metal/high-k dielectric interface. The different behavior of V_{fb} shift in TaN/HfLaO/SiO_2/Si- and Pt/La_2O_3/SiO_2/Si- suggests that it is important to compare relative contribution of each dipole and to explore their possible interaction. Fig.5.5 shows the two-dipole formation in a gate stack schematically.

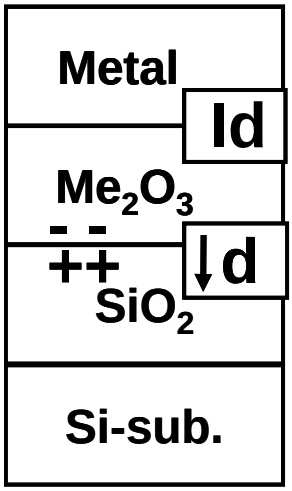


Fig.5.5 Two-dipole formation in a gate stack with a thin Me_2O_3 layer capped on a thick SiO_2.

5.5 Summary

In summary, oxides of lanthanides have some similar properties. The mechanism of the V_{fb} shift by capping a thin layer of lanthanide oxides on SiO_2 and HfO_2-based dielectrics might be from the same origin. Comparing these oxides together will give a clue to the physical mechanism. By reviewing the literature studies, we find that we must study two dipoles together: the dipole at Me_2O_3/SiO_2 interface and the dipole at metal/high-k dielectric interface. In following chapters, we will discuss Gd_2O_3, Y_2O_3 and Dy_2O_3 capping with TaN, W and Pt metal gates. No sputter target of La_2O_3 was available during this work, so we did not do any experimental work on La_2O_3.

5.6 References

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Chapter 6

V_{fb} shift of SiO_2 and HfO_2 with TaN Metal Gate: Varying N_2 Flow during TaN Deposition

6.1 Overview

In this chapter, TaN deposition condition is calibrated by changing N_2 flow rate during TaN deposition. A window of N_2 flow rate has been found to deposit TaN with low resistivity and good thermal stability. Then the V_{fb} shift of TaN/SiO_2/p-Si and TaN/HfO_2/SiO_2/p-Si after PMA are compared. The formation of a thin layer of TaON (or TaSiON if the dielectric layer containing Si at TaN interface) at TaN interface is proposed, which is responsible for the dipole formation at TaN/dielectric interfaces.

6.2 Motivation

In order to study the reason of the negative V_{fb} shift induced by capping a thin oxide layer of rare earth metals such as La_2O_3 and Gd_2O_3 on SiO_2 and HfO_2 based dielectrics with TaN metal gate, the dipole property at the TaN/SiO_2 (or HfO_2) interface must be understood. Previous students have optimized the TaN deposition condition. In our Kurt J. Lesker two-chamber sputter system, the target in Ta chamber is 6 inch in diameter. Our TaN deposition condition is

1.1kW/20sccm Ar/6.5sscm N_2/10mTorr. The properties of TaN change usually when a new Ta target is installed. However, other unidentified factors may also affect the TaN deposition. It is noticed that sometimes TaN surface becomes dark and shows a mosaic structure after a PMA. As we want to the study the V_{fb} shift due to a thin oxide layer of Me_2O_3 capping on SiO_2 or HfO_2, it is important to make sure that the V_{fb} of TaN/SiO_2 (or HfO_2) does not change very much due to unintentional changes of TaN deposition condition. The present work studies how resistivity, thermal stability and the effective work function of TaN change by varying N_2 flow rate during the deposition.

6.3 Experimental

For material analysis, 160nm TaN was deposited on 4.0nm SiO_2 1.1kW/20sccm Ar/10mTorr. The N_2 flow rate changed from 6.0 to 7.75 sccm (step: 0.05 sccm). Samples were divided into two splits. One split went through a post metal-deposition anneal (PMA) at 900 ^oC/1min/N_2. Then resistivity and X-ray diffraction (XRD) were measured.

For MOSCAPs, two stacks of TaN/5nm HfO_2/4nm SiO_2/p-Si and TaN/4nm SiO_2/p-Si were formed. The post-deposition-anneal (PDA) condition of HfO_2 was 500 ^oC/ 5min/N_2. The N_2 flow rate changed from 6.0 to 7.75 sccm. Samples were also divided into two splits. One split went through a PMA at 900 ^oC/1min/N_2.

6.4 Results and discussion

. Fig.6.1 shows resistivity measurement result without and with PMA. As can be seen that resistivity increased for N_2 flow rate higher than 6.5 sccm and decreased for N_2 flow rate lower than 6.5 sccm with PMA. Before PMA, the surface color of TaN changed from yellow to deep yellow with increasing N_2 flow rate (picture not shown). After PMA, it became very dark for N_2 flow rate lower than 6.5 sccm, but it did not change very much for higher N_2 flow rate. The 6.5 sccm N_2 flow rate was a turning point, whose after-PMA surface color changed from one experiment to the other. Fig.6.2 shows optical pictures of TaN surface with PMA. Some mosaic structures can be observed on surfaces of TaN under an optical microscope with N_2 flow rate at 6.0 and 6.25 sccm.

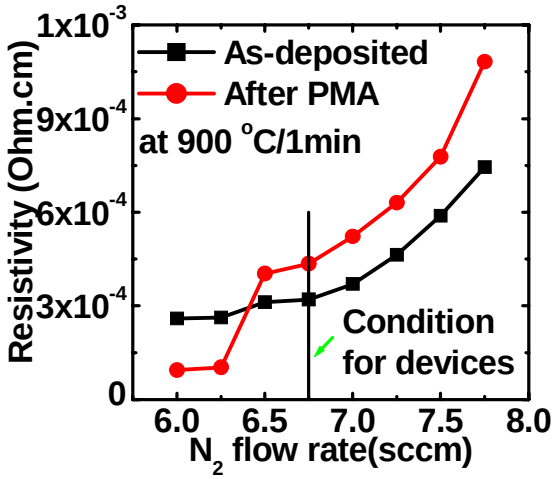


Fig.6.1 The resistivity of 160 nm TaN versus N_2 flow rate during TaN deposition (1.1kW, 10 mTorr, 20 sccm Ar) without and with PMA at 900°C/1min/N_2 anneal.

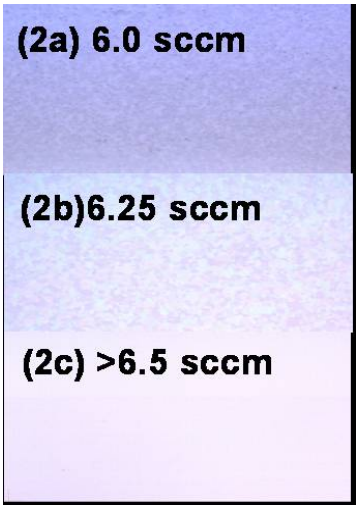


Fig.6.2 TaN surface color under an optical microscope after PMA.

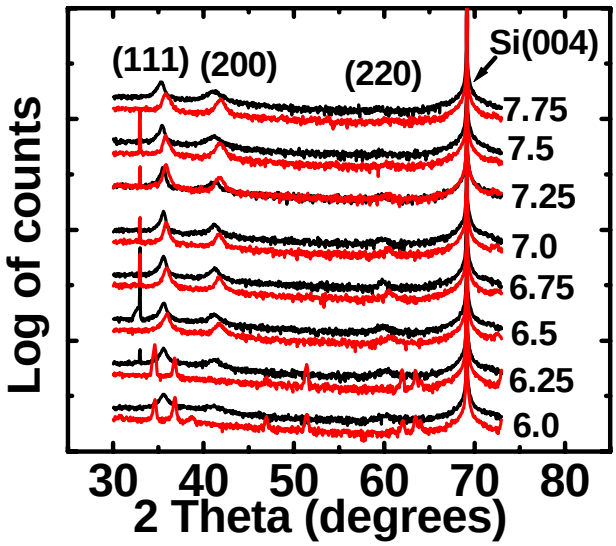
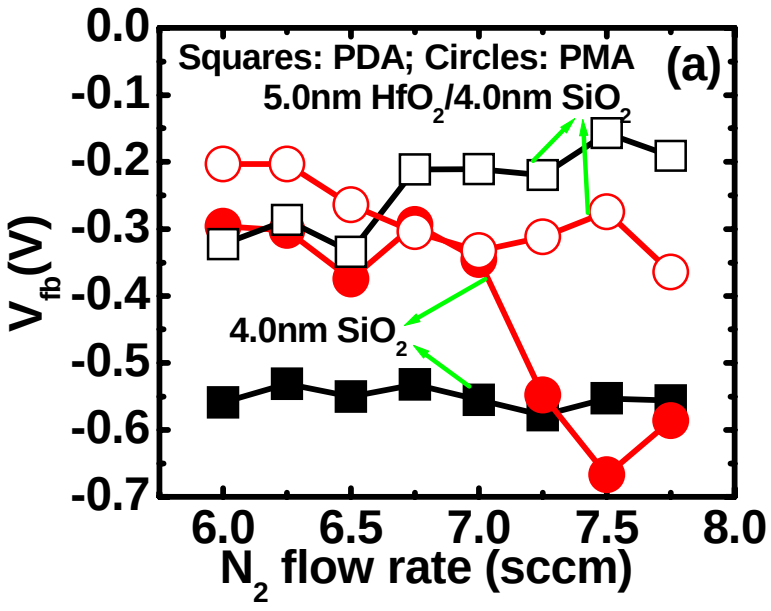


Fig.6.3 X-ray diffraction measurement of TaN under the 2theta-omega mode: Black (black): without PMA; Red (gray): after PMA.

The structural change of TaN versus N_2 flow rate was measured by X-ray diffraction (XRD). For as-deposited (before PMA) samples, all showed (111), (200) and (220) TaN peaks (Fig.6.3). After PMA, TaN peaks disappeared and new peaks appeared for the samples for N_2 flow rate at 6.0 and 6.25 sscm. The results indicated TaN was thermally unstable for N_2 flow rate below 6.5sccm. In addition, the intensity of TaN (220) peak was found to decrease with increasing the N_2 flow rate. The peak position shift has been observed for (111), (200) and (220) after PMA, indicating the stress change happened after PMA.



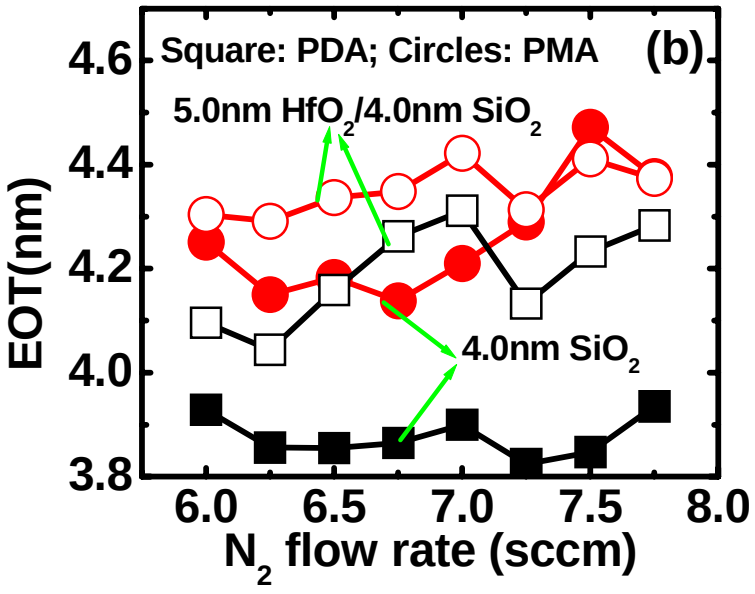


Fig.6.4 V_{fb} (a) and EOT (b) versus N_2 flow rate for 4.0 nm SiO_2 and 5.0nm HfO_2/4.0 nm SiO_2/p-Si_ without and with PMA.

Fig.6.4 shows V_{fb} and EOT versus N_2 flow rate for 4.0 nm SiO_2 and 5.0nm HfO_2/4.0 nm SiO_2/p-Si without and with PMA (900^{o}C/1 min in N_2). A very large positive V_{fb} shift (0.25 V) was observed for TaN/SiO_2/p-Si substrate with PMA at low N_2 flow rate, and a small negative V_{fb} shift (< 0.1 V) at high N_2 flow rates. A similar trend was observed for TaN/5.0nm HfO_2/4nm SiO_2/ p-Si substrate but with positive and negative V_{fb} shift (~0.1 V).

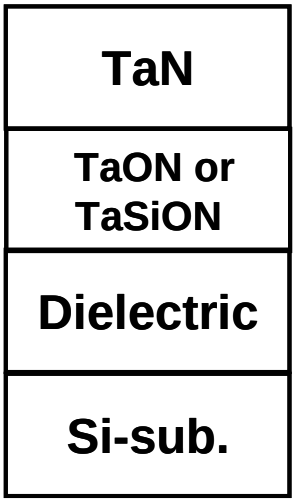


Fig.6.5 The schematic diagram of a gate stack with TaN metal gate after PMA. A thin layer of TaON or TaSiON forms at the interface between TaN and dielectric.

In order to explain the above V_{fb} shift, we propose that a thin layer of TaON form at TaN-dielectric interface after PMA. Fig.6.5 shows the schematic diagram of a gate stack with TaN metal gate after PMA. Y. Sugimoto *et al* have studied effective work function modulation of TaN metal gate on HfO_2 and SiO_2 with PMA temperature [1, 2]. They found that V_{fb} shifted positively. At the same, more Ta-O bonds formed at the TaN-dielectric interface with increasing PMA temperature. This indicates there is a correlation between V_{fb} shift and Ta-O bonds at the interface. Our results further point out the effect of N and Si and formation of TaON or TaSiON at the interface in general. It is proposed that a dipole related to this TaON/TaSiON layer shifts V_{fb}.

In later experiments, N_2 flow rate is set at 6.75 sccm in order to have both low resistivity and good thermal stability.

6.5 Summary

In summary, TaN deposition condition is calibrated by changing N_2 flow rate during TaN deposition. A window of N_2 flow rate has been found to deposit TaN with low resistivity and good thermal stability. Then the V_{fb} shift of TaN/SiO_2/p-Si and TaN/HfO_2/SiO_2/p-Si after PMA are compared. The formation of a thin TaON or TaSiON layer at TaN interface and a dipole related to this interfacial are proposed.

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Chapter 7

Capping a Thin Layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2 with TaN Metal Gate

7.1 Overview

In this chapter, we want to study the mechanism of the negative V_{fb} shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2 with TaN metal gate. Keeping three mechanisms of Fermi-level pinning in mind, we want to examine the V_{fb} shift by studying:

(1) The interfaces of TaN/HfO_2, TaN/Me_2O_3 and HfO_2/Me_2O_3, HfO_2/SiO_2 and Me_2O_3/SiO_2;

(2) The mixture of MeSiO, and MeHfO;

(3) The interaction between Me_2O_3 and S-SiO_2 (sputtered SiO_2) with and without a thick HfO_2 barrier layer to separate Me_2O_3/S-SiO_2 from the bottom interfacial SiO_2;

(4) The effects of different deposition conditions of Me_2O_3;

(5) XPS study of bonding configuration change due to capping Gd_2O_3 on SiO_2;

(6) NMOSFETs with Me_2O_3 capping on the interfacial SiO_2 layers.

We have found that the dipoles at TaN/HfO_2 and TaN/Me_2O_3 (Me=Gd, Y, and Dy) interfaces are almost same. Neither MeHfO nor MeSiO is the reason of the negative V_{fb} shift after capping a layer of Me_2O_3 on SiO_2. The direct contact interaction beween Me_2O_3 and SiO_2 should be responsible for the negative V_{fb} shift based on the V_{fb} shift analysis. XPS study of capping Gd_2O_3 on SiO_2 shows clear Si and O bonding change at the interface between Me_2O_3 and SiO_2. So a dipole forms at this interface, which causes the negative V_{fb} shift.

7.2 Experimental

The beveled SiO_2 with varying thickness was thermally grown at 850 ^oC on p-Si (001) substrates (5~22 Ohm.cm). HfO_2 and Me_2O_3 (Me=Gd, Y and Dy) were formed by DC sputtering in Ar from pure metal targets with PDA at 500 ^oC/5min in N_2. TaN was deposited by DC sputtering. TaN was patterned using CF_4 Reaction ion etching (RIE). PMA was performed at 900 ^oC/1min in N_2. After an Al backside contact formation by sputtering, a forming gas annealing was performed at 400^oC for 30min.

7.3 V_{fb} analysis of MOSCAPs with different gate stacks

Our initial experiments showed the negative V_{fb} shift appeared when Me_2O_3 contacted the beveled SiO_2 layer directly. In order to examine whether

the interaction between Me_2O_3 and SiO_2 is the cause, the following studies have been performed.

7.3.1 Varying the thickness of the HfO_2 barrier layer between Me_2O_3 and the beveled SiO_2

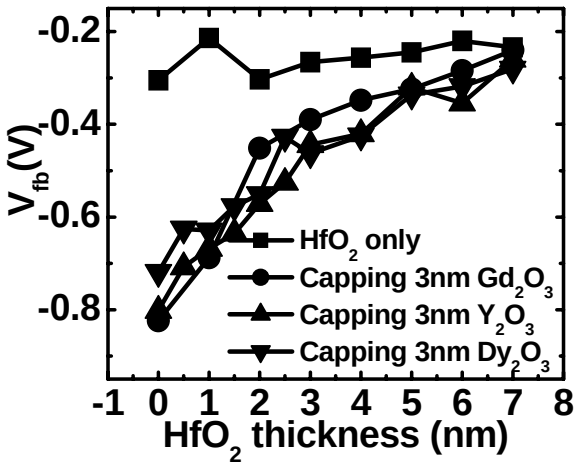


Fig.7.1 V_{fb} of MOSCAPs of TaN/3nm Me_2O_3/HfO_2/4.0nm SiO_2/p-Si after PMA versus HfO_2 barrier thickness.

Fig.7.1 shows V_{fb} of MOSCAPs of TaN/3nm Me_2O_3/HfO_2/4.0nm SiO_2/p-Si after PMA (900 ^oC/1min) versus HfO_2 barrier thickness. For the present PMA condition, 7 nm HfO_2 can "block" Me_2O_3 electrically in the sense of no V_{fb} shift compared to the HfO_2-only stack (TaN/ /HfO_2/4.0nm SiO_2/p-Si).

7.3.2 Mixing HfO_2 with Me_2O_3

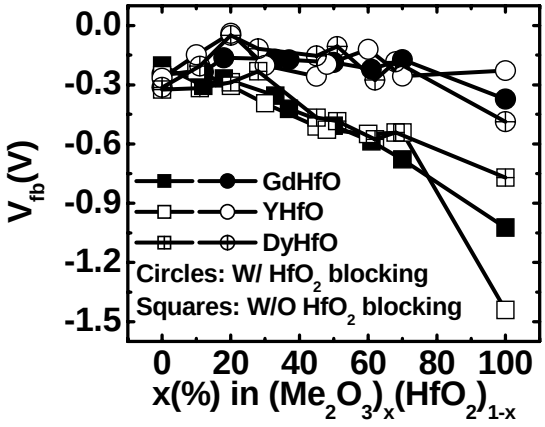
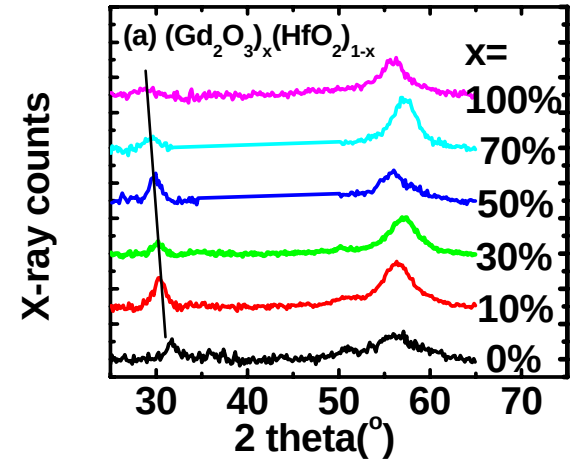
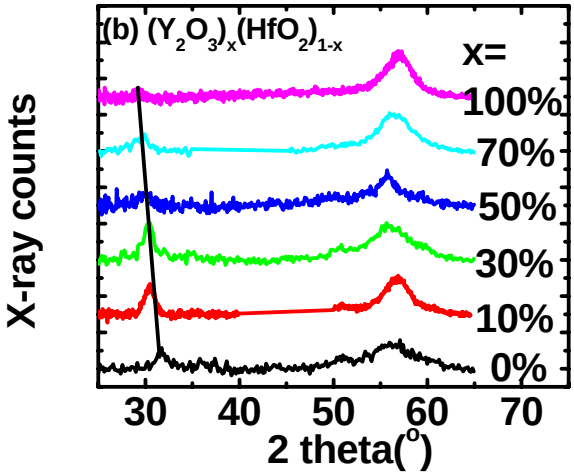


Fig.7.2 V_{fb} of MOSCAPs of TaN/5nm $(Me_2O_3)_x(HfO_2)_{1-x}$/HfO_2 (0 or 5nm)/4nm SiO_2 /p-Si versus x after PMA.

Fig.7.2 shows V_{fb} of MOSCAPs of TaN/5nm $(Me_2O_3)_x(HfO_2)_{1-x}$ /5nm HfO_2 /4nm SiO_2/p-Si (circles) and TaN/5nm $(Me_2O_3)_x(HfO_2)_{1-x}$/4nm SiO_2/p-Si (squares) versus x after PMA. A 5 nm HfO_2 barrier layer was used. This result shows that the mixing of HfO_2 and Me_2O_3 did not cause the negative V_{fb} shift.

However, there was a structural change of $(Me_2O_3)_x(HfO_2)_{1-x}$ (Me= Gd, Y and Dy) versus x, as has been proved by XRD. The mixing did not improve the crystallization temperature, but it did change the structure from monoclinic for HfO_2 to tetragonal or cubic phase for Me_2O_3 (Fig.7.3). Stress might change with x, too.


(a) (Gd2O3)x(HfO2)1-x
x=
100%
70%
50%
30%
10%
0%
X-ray counts
30
40
50
60
70
2 theta(o)


(b) (Y2O3)x(HfO2)1-x
x=
100%
70%
50%
30%
10%
0%
X-ray counts
30
40
50
60
70
2 theta(o)

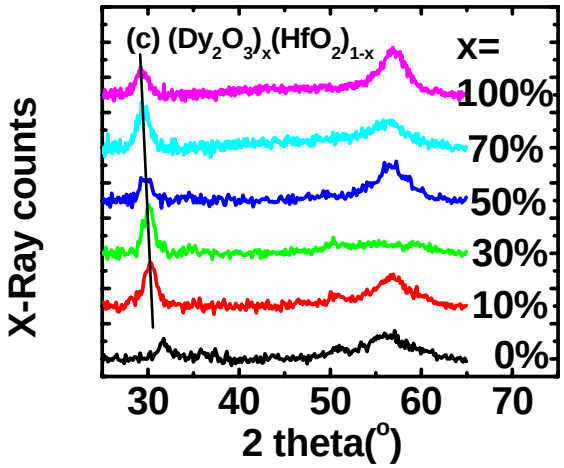


Fig.7.3 XRD measurement of $(Me_2O_3)_x(HfO_2)_{1-x}$ versus x using grazing incident (5^o): (a) Me=Gd, (b) Me=Y, (c) Me=Dy.

7.3.3 Gd_2O_3 stacks on n- and p- Si substrates

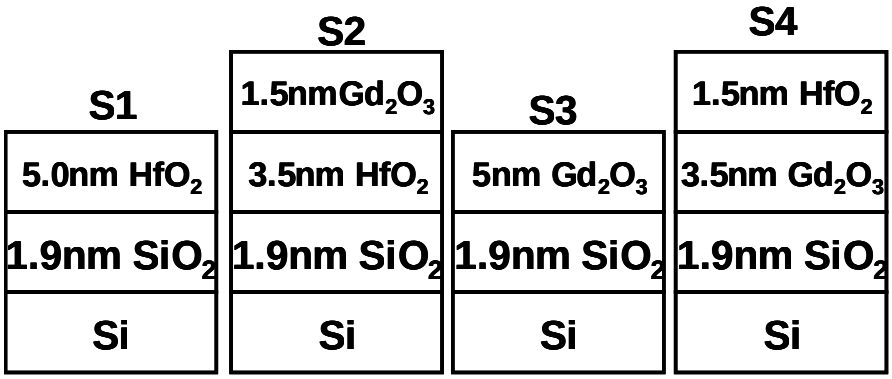


Fig.7.4 Structures of gate stack S1, S2, S3 and S4.

In this experiment, MOSCAPs with four dielectric structures have been studied: S1) TaN/5nm HfO_2/1.9nm SiO_2/Si; S2) TaN/1.5nm Gd_2O_3/3.5nm HfO_2/1.9nm SiO_2/Si; S3) TaN/5nm Gd_2O_3/1.9nm SiO_2/Si; S4) TaN/1.5nm HfO_2/3.5nm Gd_2O_3/1.9nm SiO_2/Si (Fig.7.4). Fig.7.5 (a) presents V_{fb} values for the four structures on both n- and p-Si (001) substrates without and with PMA. It can be seen that V_{fb} values of both S3 and S4 shifted to the negative direction compared to S1 and S2 for both n- and p-MOSCAPs. Fig.7.5(b) shows V_{fb}(n)-V_{fb}(p), whch is equal to the Fermi-level difference of n- and p-Si substrates (note: the doping levels in both n- and p- substrates are about $3.0x10^{15}$ cm^{-3}). The value was affected by fixed charges in gates stacks before PMA. After PMA, it was almost same for S1 and S2 and S3, and slightly different for S4, indicating that the mechanism of V_{fb} shift does not depend on the doping type in Si substrates. So the V_{fb} shift through Vo mechanism did not happen for 1.9nm beveled SiO_2. Due to this reason, only p-Si substrates were used in other experiments.

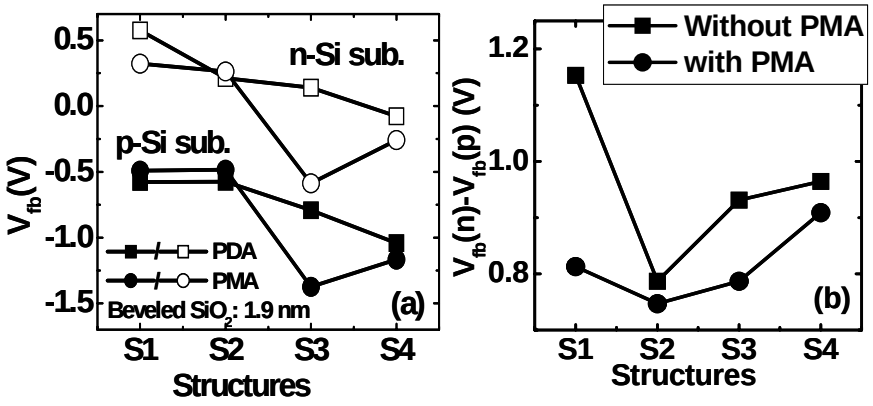


Fig.7.5 (a) V_{fb} shift of MOSCAPs with four structures of S1, S2, S3 and S4 on both n- and p- Si (001) substrates. (b) V_{fb}(n)-V_{fb}(p)

7.3.4 V_{fb} shift analysis: the effect of the different interfaces (TaN/HfO_2, TaN/Me_2O_3, HfO_2/SiO_2 and Me_2O_3/SiO_2)

Gate structures of S5, S6, S7 and S8 are designed to compare the effect of the different interfaces (Fig.7.6). S5 and S6 focus on TaN/HfO_2 and TaN/Me_2O_3, and S7 and S8 on HfO_2/SiO_2 and Me_2O_3/SiO_2**.** As can be seen that V_{fb} of S5 and S6 are almost same for Me=Gd, Y and Dy. The large negative V_{fb} shift was observed for both S7 and S8. The different magnitude of V_{fb} shift in S7 and S8 result from HfO_2 capping on Me_2O_3 in S8. The same V_{fb} shift in S5 and S6 indicates the contribution from the dipole at TaN/HfO_2 and TaN/Me_2O_3 is almost same. It seems that the negative V_{fb} shift is due to the direct contact of Me_2O_3 with the beveled SiO_2 layer.

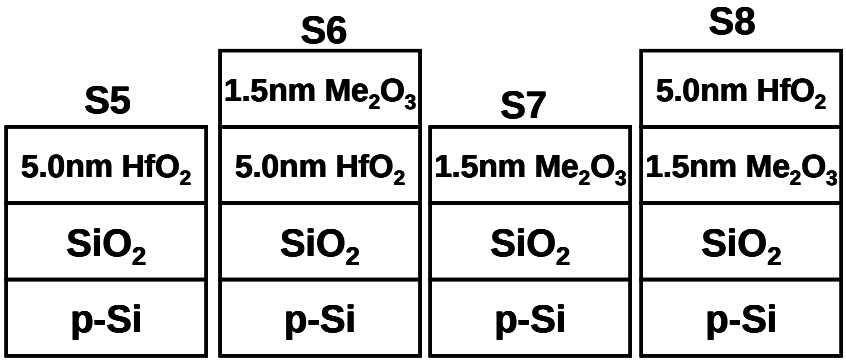


Fig. 7.6 Gate structures of S5, S6, S7 and S8.

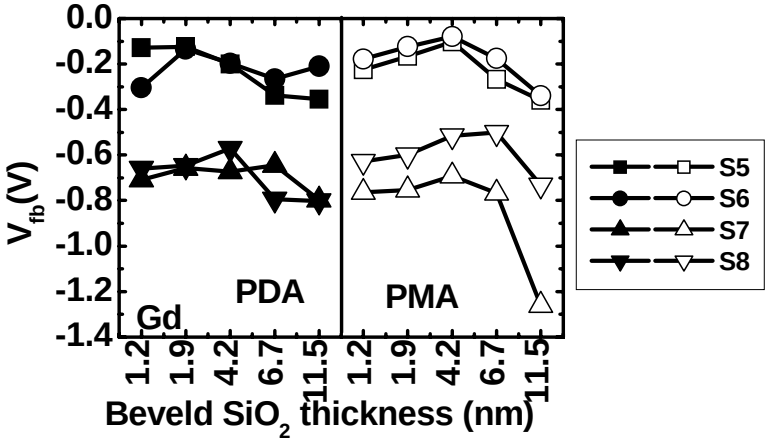


Fig.7.7 (a) V_{fb} of S5, S6, S7 and S8 with Me= Gd without and with PMA at 900 $^{o}C/1min/N_2$.

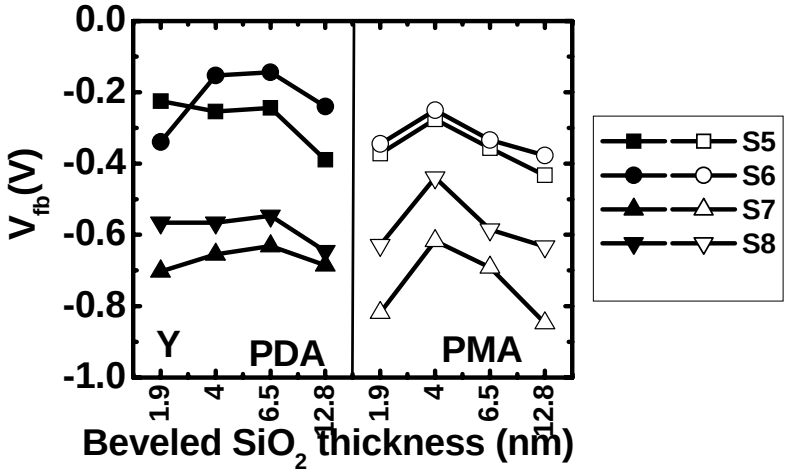


Fig.7.7 (b) V_{fb} of S5, S6, S7 and S8 with Me= Y without and with PMA at 900 $^{o}C/1min/N_2$.

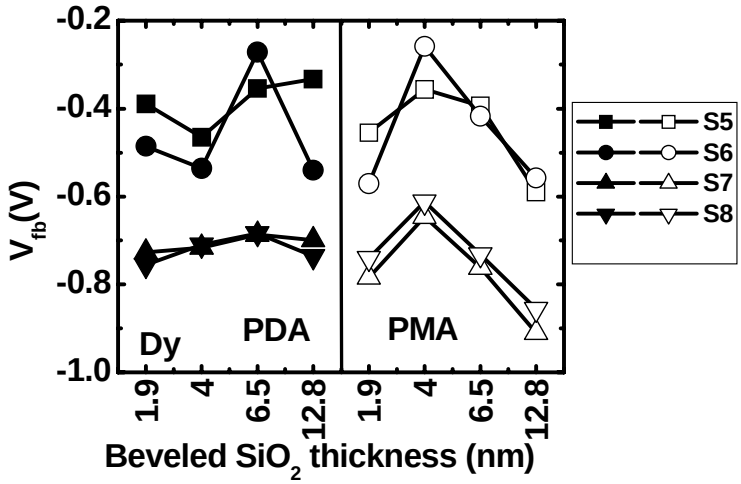


Fig.7.7 (c) V_{fb} of S5, S6, S7 and S8 with Me= Dy without and with PMA at 900 $^{o}C/1min/N_2$.

7.3.5 V_{fb} shift analysis: the effect of varying the beveled SiO_2 and Me_2O_3 thickness

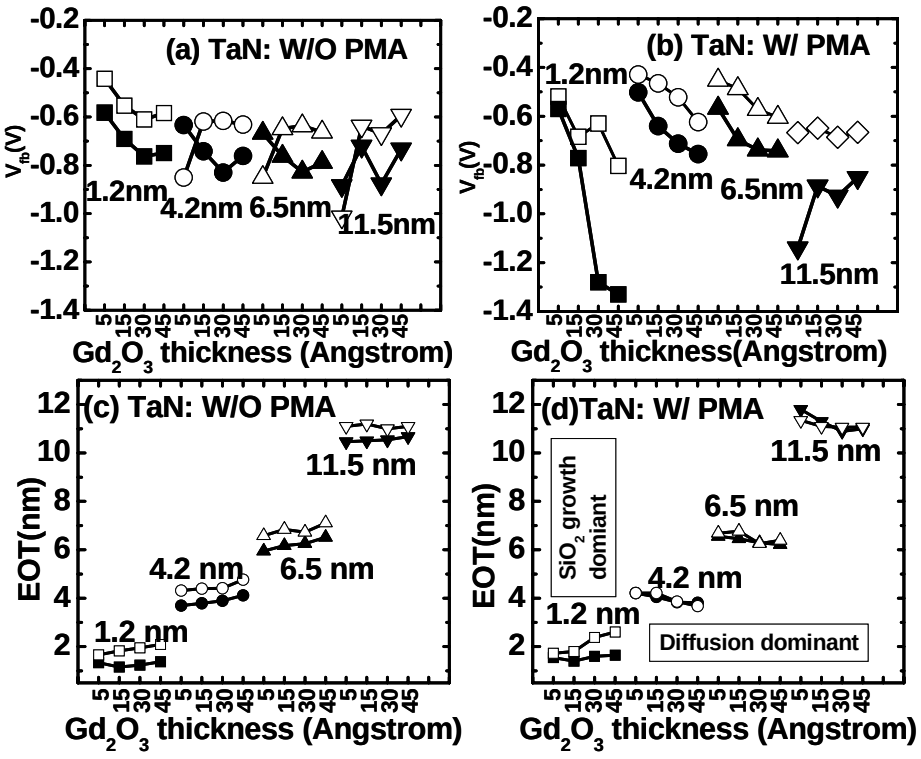


Fig.7.8 The change of V_{fb} and EOT in S7 and S8 with varying the thicknesses of both Gd_2O_3 and SiO_2 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm.

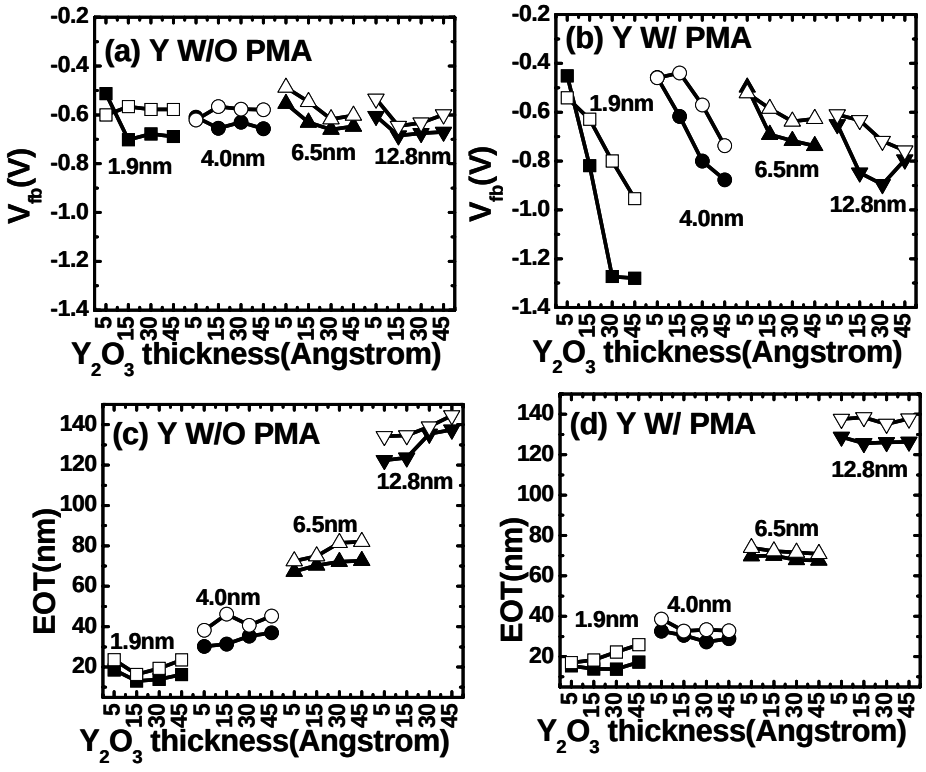


Fig.7.9 The change of V_{fb} and EOT in S7 and S8 with varying the thicknesses of both Y_2O_3 and SiO_2 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm.

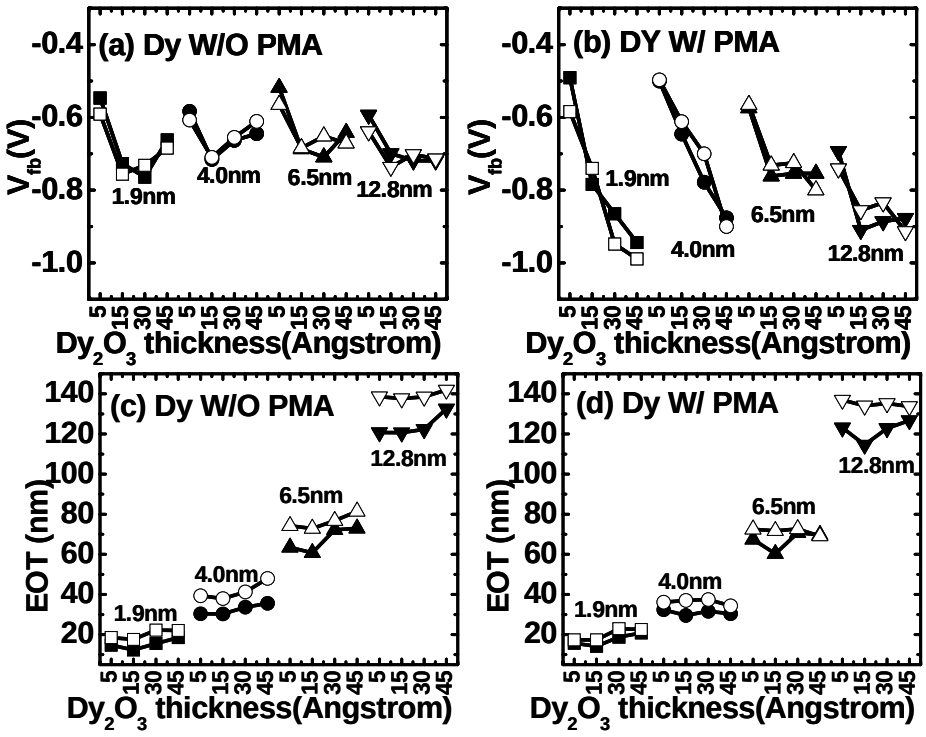


Fig.7.10 The change of V_{fb} and EOT in S7 and S8 with varying the thicknesses of both Dy_2O_3 and SiO_2 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm.

In (7.3.4), the negative V_{fb} shift is observed in both S7 and S8, indicating it is caused by the interaction between Me_2O_3 and SiO_2. In order to understand the interaction, we study the V_{fb} shift by varying the thickness of both Me_2O_3 and SiO_2 in S7 and S8 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm. From Fig.7.8-10, it can be seen that the negative V_{fb} shift is almost constant with increasing the beveled SiO_2 thickness before PMA. It increases with increasing

Me_2O_3 thickness after PMA. Between S7 and S8, it is larger in S7. Among Gd_2O_3, Y_2O_3 and Dy_2O_3, the difference is the smallest in Dy_2O_3. After PMA, Me_2O_3 diffused into the beveled SiO_2 in S7 forming a silicate layer (MeSiO), and decreased the EOT of the gate stack. The formation of the silicate layer might also drive HfO_2 in S8 to diffuse into the beveled SiO_2, and make a stronger EOT decrease in S8. There are two regions in EOT change: (1) the interfacial SiO_2 growth dominant region for thin beveled SiO_2; (2) the diffusion-dominant region for thick beveled SiO_2. In the interfacial SiO_2 growth-dominant region, oxygen diffuses through the gate dielectric to the Si interface and results in the growth of the interfacial SiO_2. In the diffusion-dominant region, the interfacial SiO_2 thickness does not change very much and the dominant process is the silicate formation.

7.3.6 Interaction between sputtered SiO_2 and Me_2O_3 with a HfO_2 barrier

In this experiment, we want to compare V_{fb} and EOT change of TaN/Me_2O_3/6nm S-SiO_2/7nm HfO_2/4.0nm SiO_2/p-Si and TaN/Me_2O_3/6nm S-SiO_2/6.5nm SiO_2/p-Si. S-SiO_2 was sputtered SiO_2. Here the bottom SiO_2 layers (4.0nm and 6.5nm) were thermally grown at 850 ^oC/30min. S-SiO_2 was sputtered SiO_2 (6nm). Me_2O_3 (Me=Gd, Y and Dy) was also sputtered. Its thickness was 1, 2, and 3nm. The processing steps are as following:

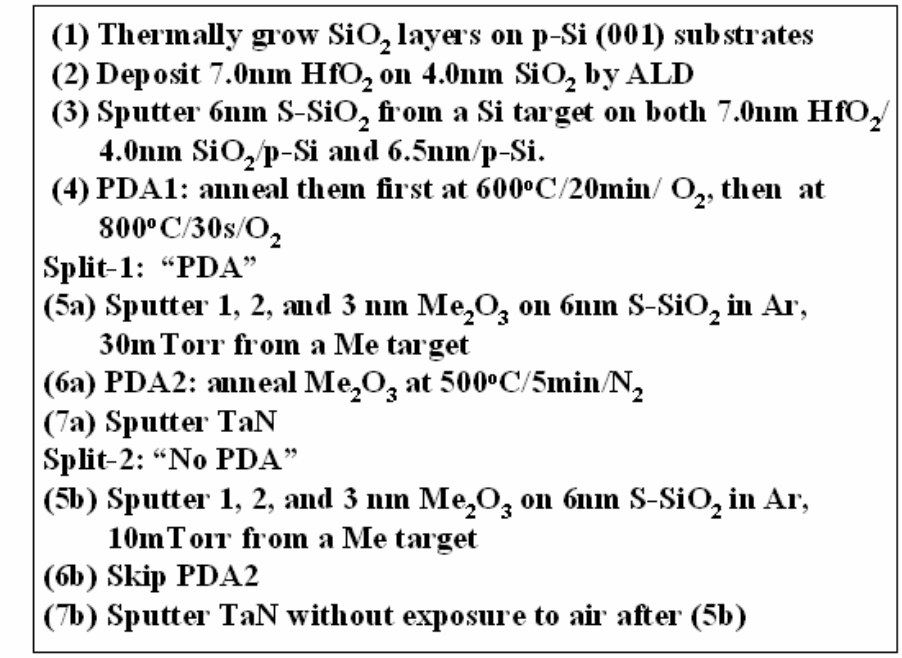


Fig.7.11 Process flow of forming a bilayer of Me_2O_3/S-SiO_2 with a 7nm ALD HfO_2 barrier layer.

Fig.7.11 shows the process flow of forming a bilayer of Me_2O_3/S-SiO_2 with a 7nm ALD HfO_2 barrier layer. There were two conditions for Me_2O_3 formation: (1) For the usual "**PDA**" condition, Me_2O_3 was sputtered from a Me target in Ar and 30 mTorr. The PDA (PDA2) was performed at 500°C/5min/N_2. (2) For the "**No PDA**" condition, Me_2O_3 was sputtered from a Me target in Ar and 10 mTorr. TaN was deposited with no PDA (skip PDA2) and no air exposure for the Me_2O_3 layer. In this way, an oxygen deficient Me_2O_3 layer was formed.

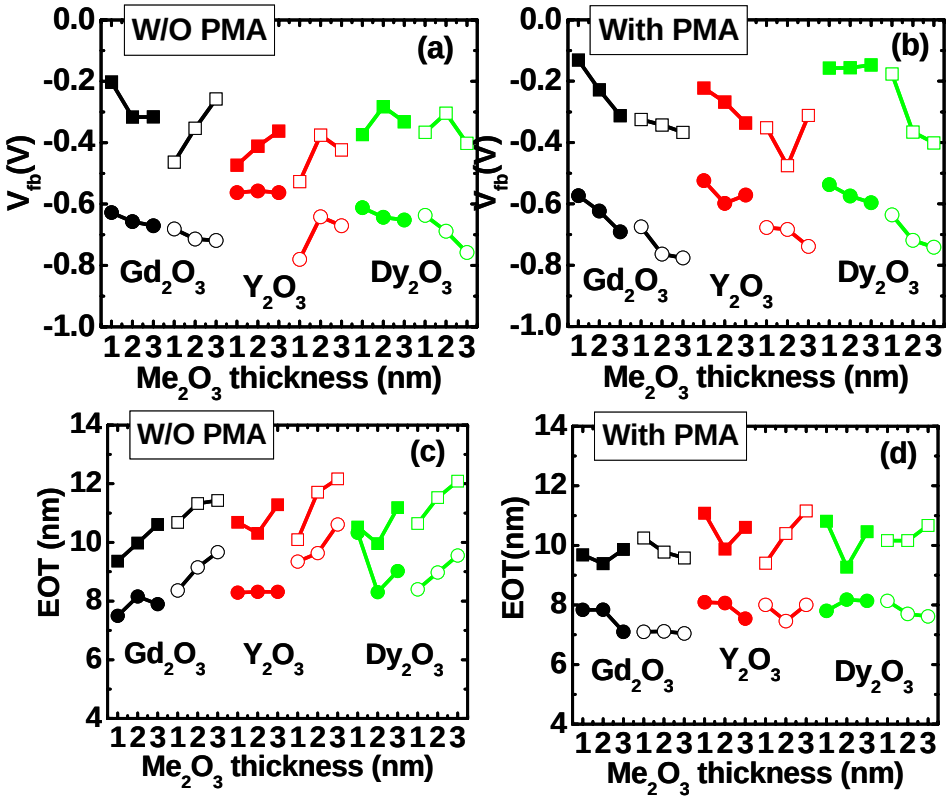


Fig.7.12 V_{fb} and EOT change of TaN/Me_2O_3/6nm S-SiO_2/7nm HfO_2/4.0nm SiO_2/p-Si (Squares) and TaN/Me_2O_3/6nm S-SiO_2/6.5nm SiO_2/p-Si (Circles) without (W/O) and with PMA. The Me_2O_3 thickness is 1, 2 and 3nm. The two deposition conditions of the Me_2O_3 layer are "**PDA**" (Solid) and "**No PDA**" (Hollow).

Fig.7.12 shows V_{fb} and EOT change of TaN/Me_2O_3/6nm S-SiO_2/7nm HfO_2/4.0nm SiO_2/p-Si and TaN/Me_2O_3/6nm S-SiO_2/6.5nm SiO_2/p-Si without and with PMA. Comparing with Fig.7.8-10, there is almost no negative V_{fb} shift in TaN/Me_2O_3/6nm S-SiO_2/7nm HfO_2/4.0nm SiO_2/p-Si, while there is still a large negative V_{fb} shift in TaN/Me_2O_3/6nm S-SiO_2/6.5nm SiO_2/p-Si. After

PMA, there is a slight negative V_{fb} shift in TaN/Me_2O_3/6nm S-SiO_2/7nm HfO_2/4.0nm SiO_2/p-Si for the "**No PDA**" Me_2O_3. It implies that the large negative V_{fb} shift in TaN/Me_2O_3/6nm S-SiO_2/6.5nm SiO_2/p-Si is not caused by the interface Me_2O_3/S-SiO_2, but by the interface Me_2O_3/SiO_2. Some Me diffused through the 6nm S-SiO_2 and reached the bottom SiO_2 layer. Another conclusion is that the "**No PDA**" Me_2O_3 enhances the negative V_{fb} shift and MeSiO formation.

7.3.7 Interaction between sputtered SiO_2 and Me_2O_3 without a HfO_2 barrier layer

(1) Thermally grow a 6.5 nm SiO_2 layer on p-Si (001) substrates
(2) Sputter 3 and 6nm S-SiO_2 from a Si target
(3) PDA1: anneal them first at 600°C/20min/O_2, then at 800°C/30s/O_2
Split-1: "**PDA**"
(4a) Sputter 1, 2, and 3 nm Me_2O_3 on S-SiO_2 (0, 3, and 6nm) in Ar, 30mTorr from a Me target
(5a) PDA2: anneal Me_2O_3 at 500°C/5min/N_2
(6a) Sputter TaN
Split-2: "**No PDA**"
(4b) Sputter 1, 2, and 3 nm Me_2O_3 on S-SiO_2 (0, 3, and 6nm) in Ar, 10mTorr from a Me target
(5b) Skip PDA2
(6b) Sputter TaN without exposure to air after (4b)

Fig.7.13 Process flow forming a bilayer of Gd_2O_3/S-SiO_2 on 6.5nm thermal SiO_2 (without a HfO_2 barrier layer)

In this experiment, we want to study the V_{fb} shift of gate stacks of TaN/Me_2O_3/S-SiO_2/SiO_2/p-Si by varying thicknesses of both Me_2O_3 and S-SiO_2. Here the bottom SiO_2 layer (6.5nm) was thermally grown at 850 ^oC/30min. S-SiO_2 was sputtered SiO_2 (0, 3 and 6nm). Me_2O_3 (Me=Gd, Y and Dy) was also sputtered. Its thickness is 1, 2, and 3nm. The processing steps are shown in Fig.7.13.

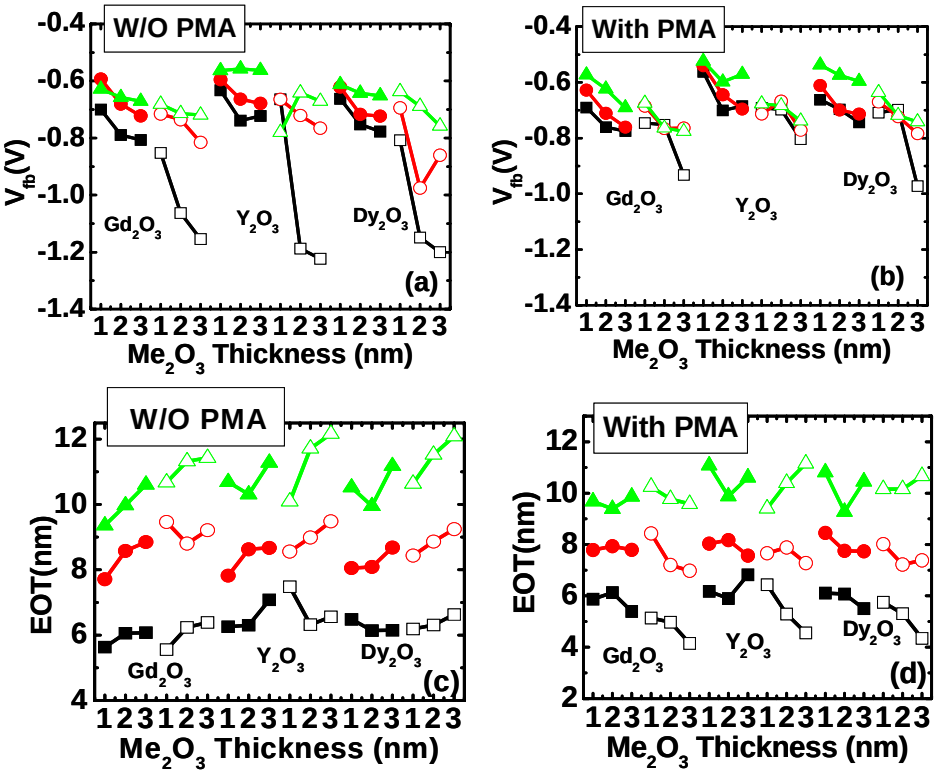


Fig.7.14 V_{fb} and EOT change of gate stacks of TaN/Me_2O_3/S-SiO_2/SiO_2/p-Si without (W/O) and with PMA. The three S-SiO_2 thicknesses are 0nm (Squares), 3nm (Circles) and 6nm (Triangles). The Me_2O_3 thicknesses are 1, 2 and 3nm.

The two deposition conditions of the Me_2O_3 layer are "**PDA**" (Solid) and "**No PDA**" (Hollow).

Fig.7.14 shows V_{fb} and EOT change of gate stacks of TaN/Me_2O_3/S-SiO_2/SiO_2/p-Si without and with PMA. The "**No PDA**" Me_2O_3 has the strongest effect on the V_{fb} when S-SiO_2 is zero, which is saying that Me_2O_3 is directly deposited on the thermally grown SiO_2. It enhances the negative V_{fb} shift, especially without PMA. The S-SiO_2 decreases the effect of "**No PDA**" Me_2O_3. The "**No PDA**" Me_2O_3 is clearly seen to enhance the negative V_{fb} shift and the silicate (MeSiO) formation.

7.3.8 Interaction between sputtered SiO_2 and $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$ without and with a HfO_2 barrier layer

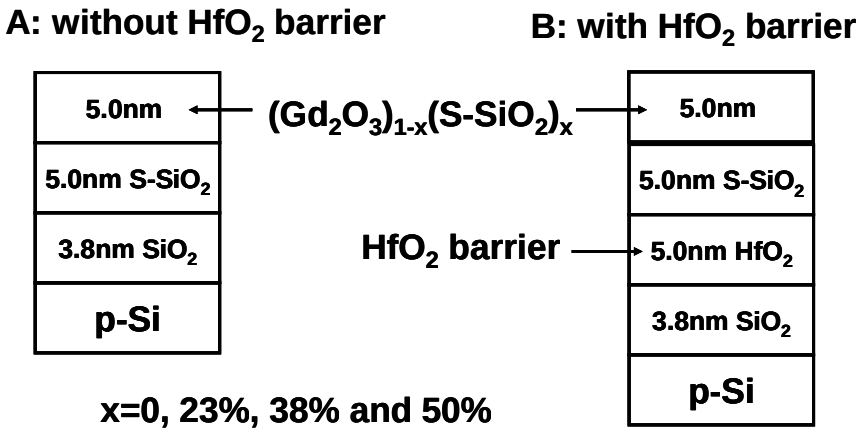


Fig.7.15 Gate stacks to study interaction interaction between sputtered SiO_2 and $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$: (A) without and (B) with a HfO_2 barrier layer.

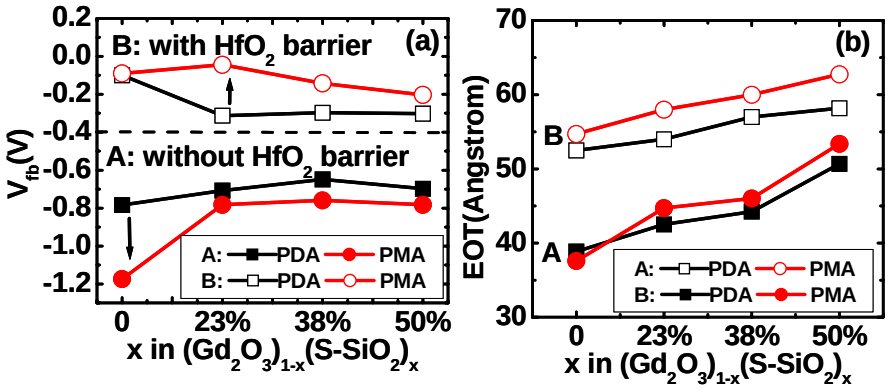


Fig.7.16 (a) V_{fb} and (b) EOT of gate stacks shown in Fig.7.15 versus x in $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$ without and with PMA.

Fig.7.15 shows gate stack structures to study interaction between sputtered S-SiO_2 and $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$ without and with a HfO_2 barrier layer. $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$ was formed by co-sputtering Gd and Si in Ar with PDA at 600 ^oC/5min in N_2. The composition x was changed through changing the DC power applied to the Si target. PMA was performed at 900 ^oC/1min in N_2 as usual. Fig.7.16 shows V_{fb} and EOT of gate stacks versus x in $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$ without and with PMA.

For gate stacks without a HfO_2 barrier, x=0 (Gd_2O_3) had a slight larger magnitude of negative V_{fb} shift than x≠0 (GdSiO) before PMA. After PMA, V_{fb} shifted more negatively for all x but with the largest magnitude for x=0. For gate stacks with x≠0, V_{fb} did not change very much when x increased from 23% to

50% without and with PMA. EOT decreased for x=0 due to more silicate formation and increased for x≠0 after PMA.

With a 5.0nm HfO_2 barrier, the gate stack with x=0 (Gd_2O_3) did not have a negative V_{fb} shift, and the stacks with x≠0 (GdSiO) had a small negative V_{fb} shift of about 0.2V compared to the gate stack with x=0 before PMA. After PMA, V_{fb} of the gate stack with x=0 did not change very much while V_{fb} of the stacks with x≠0 shifted positively. Such kind of positive V_{fb} shift might be due to two reasons for the gate stacks with x≠0: (1) the change of oxygen deficiency in the $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$ layer and/or (2) the change of bonding state in the interfacial layer of TaSiON after PMA (see chapter 6).

From the above results, two conclusions can be drawn: (1) The dominant negative V_{fb} shift is due to the interaction between Gd (or Gd_2O_3) and the bottom thermal SiO_2, (2) V_{fb} of the gate stacks with x≠0 does not change very much with x. In addition, no negative V_{fb} shift was observed when a layer of $(Gd_2O_3)_{1-x}(S\text{-}SiO_2)_x$ was deposited directly on a thick HfO_2 layer (data not shown). So the silicate (GdSiO) is not the reason for the dominant negative V_{fb} shift.

7.4 XPS study of Gd_2O_3 capping

7.4.1 Thick beveled SiO_2 layers

In this experiment, we studied 1nm Gd_2O_3 capping on a thick beveled SiO_2 layer (38.6nm). Samples were not grounded. The take-off angle was 45^o.

Three samples: 1) 38.6nm SiO_2; 2) 1.0nm Gd_2O_3 deposited on above SiO_2 with PDA at 500 ^oC/5min/N_2; 3) further annealing the deposited Gd_2O_3 at 900 ^oC/ /1min in N_2 (PMA).

Fig.7.17 shows XPS spectra around Si 2p and O 1s. For Si 2p, besides the peak of Si^{+4} (104.2eV), another peak appeared at 102.6eV in two Gd_2O_3- capped samples. This peak was between the usual Si^{+3} (103.1 eV) and Si^{+2} (102.eV) [2]. For O 1s, besides Si-O bonding at 533.5 eV, another peak appeared at 531.9 eV in Gd_2O_3-capped samples.

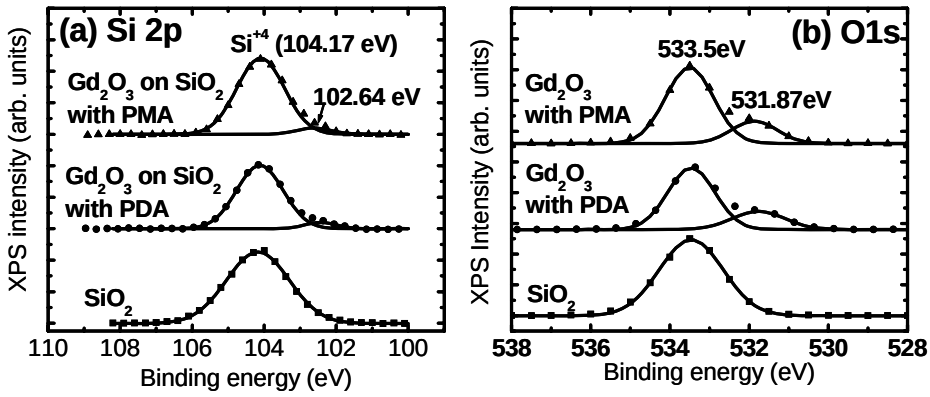
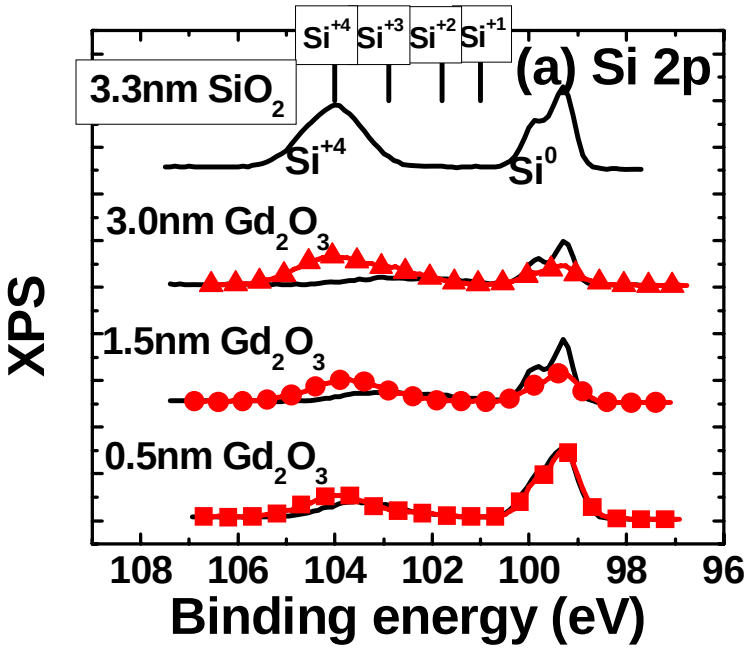


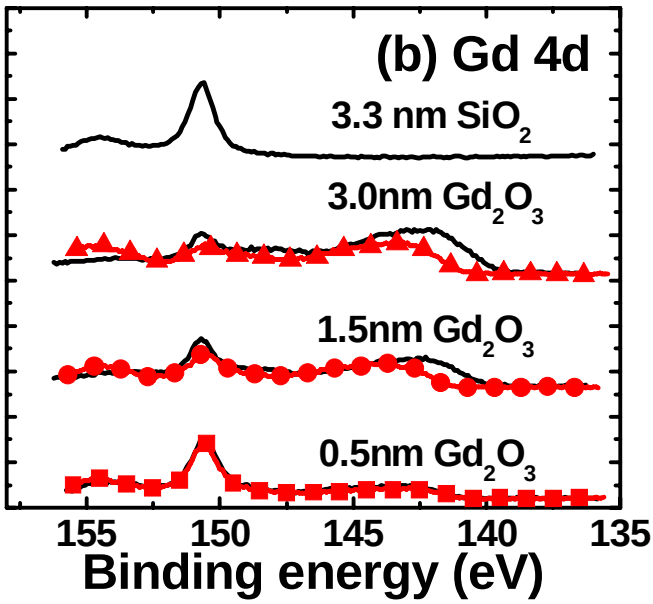
Fig.7.17 XPS spectra of (a) Si 2p and (b) O1s for 1nm Gd_2O_3 capping on a 38.6nm thermal SiO_2 layer. Samples were not grounded. The take-off angle was 45^o.

7.4.2 Thin beveled SiO_2 layers

In this experiment, we studied Gd_2O_3 capping on a thin beveled SiO_2 layer (1.5nm). After RCA cleaning, 1.5nm thermal oxide was grown on p-Si (001)

substrates (5~22 Ω cm) at 700 ^{o}C in a furnace. Then 0.5, 1.5 and 3.0nm Gd_2O_3 were sputtered on the top of the 1.5nm SiO_2 layer. PDA was performed at 500 ^{o}C/5min/N_2. Samples were divided into two splits, and one split went through another annealing at 900 ^{o}C/1min/N_2 (PMA condition). The control sample was 3.3nm thermal SiO_2 grown at 850 ^{o}C. Backside Al was sputtered and annealed at 450 ^{o}C/3min/N_2 in a rapid thermal annealing (RTA) chamber. During XPS measurement, samples were grounded (see Chapter 9), and the take-off angle was 75^{o}. XPS spectra were realigned to Si^0 2p (99.3 eV) to remove the effect of the remaining charging.




(b) Gd 4d
3.3 nm SiO2
3.0nm Gd2O3
1.5nm Gd2O3
0.5nm Gd2O3
155
150
145
140
135
Binding energy (eV)

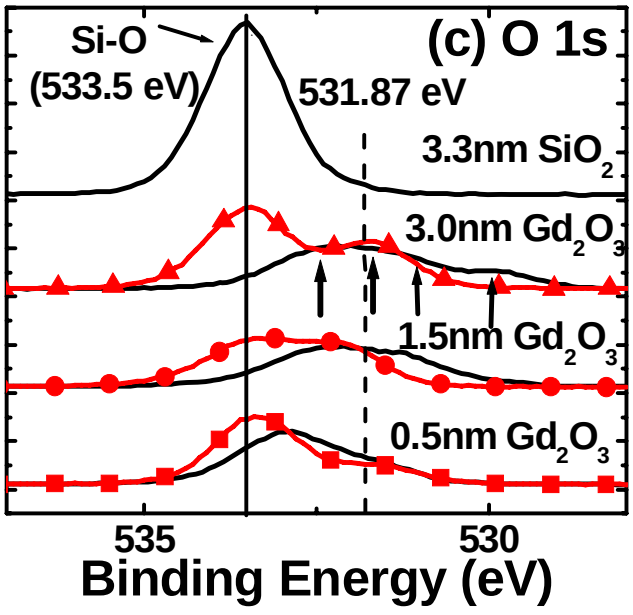
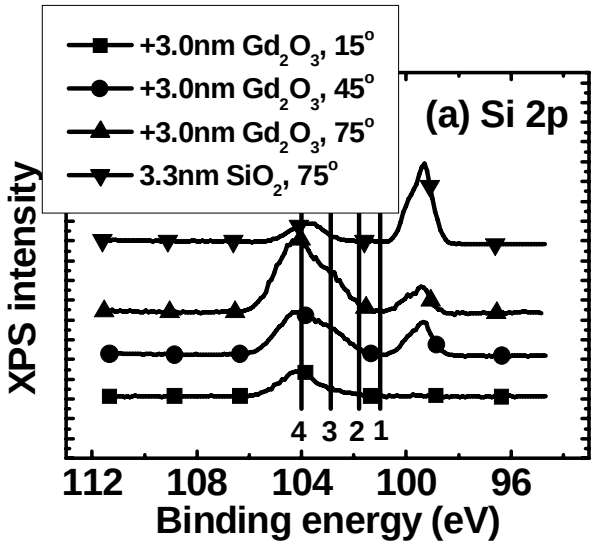

Si-O
(533.5 eV)
531.87 eV
(c) O 1s
3.3nm SiO2
3.0nm Gd2O3
1.5nm Gd2O3
0.5nm Gd2O3
535
530
Binding Energy (eV)

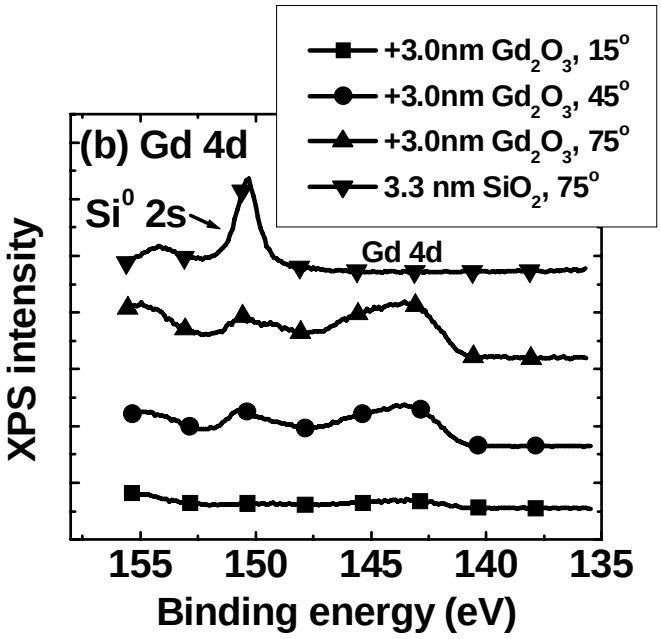
Fig.7.18 Binding energies of (a) Si 2p, (b) Gd 4d and (c) O 1s for samples of 0.5, 1.5 and 3.0nm Gd_2O_3 on 1.5nm SiO_2 and 3.3nm thermal SiO_2. Solid line: after PDA; Solid line + symbols: after PMA. The Binding energy positions of Si^{+4} (104.0 eV), Si^{+3} (102.9eV), Si^{+2} (101.8 eV) and Si^{+1} (101 eV) shown in (a) are from [2]. The arrows in (c) indicate multiple oxygen bonding states with thick Gd_2O_3 capping (Before PMA). Solid line (Si-O: 533.5 eV) and dashed line (531.87 eV) in (c) correspond to two O 1s related peaks in Fig. 71.16(b), respectively.

Fig.7.18(a) implies that thicker Gd_2O_3 layers enhanced the interfacial SiO_2 growth during PMA. The intensity of Si-O bonding was found to decrease with increasing Gd_2O_3 thickness before PMA. Both silicide (Si-Gd) and silicate (Si-O-Gd) bonds might exist. From Fig.7.18(b), the binding energy of Gd increased after PMA, indicating more Gd-O or Si-Gd bonds converted to the silicate bonds (Si-O-Gd). From Fig. 7.18(c), there were several oxygen related bonding states in thicker Gd_2O_3 layers.

7.4.3 Angle-resolved XPS measurement

In this experiment, an angle resolved XPS measurement was performed on a sample with a layer of 3.0nm Gd_2O_3 on 1.5nm SiO_2. Three take-off angles of 15^o, 45o and 75^o were chosen. Samples went through a PDA at 500 $^oC/5min/N_2$ after Gd_2O_3 deposition and another annealing at 450 $^oC/3min/N_2$ after a backside Al deposition. The control sample was 3.3nm thermally grown SiO_2.They were grounded during XPS measurement.


+3.0nm Gd2O3, 15°
+3.0nm Gd2O3, 45°
+3.0nm Gd2O3, 75°
3.3nm SiO2, 75°
(a) Si 2p
XPS intensity
4 3 2 1
112 108 104 100 96
Binding energy (eV)


+3.0nm Gd2O3, 15°
+3.0nm Gd2O3, 45°
+3.0nm Gd2O3, 75°
3.3 nm SiO2, 75°
(b) Gd 4d
Si0 2s
Gd 4d
XPS intensity
155 150 145 140 135
Binding energy (eV)

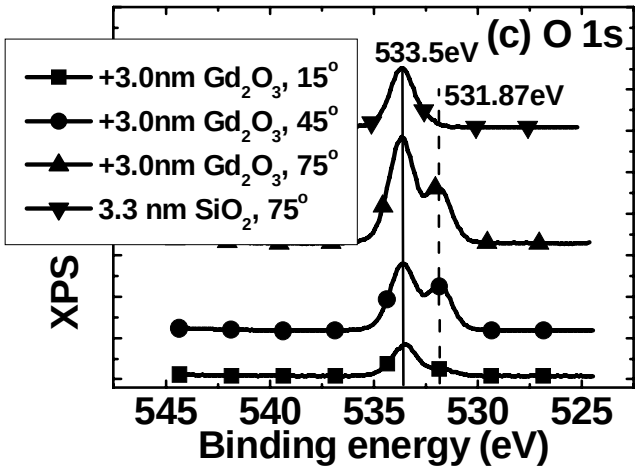


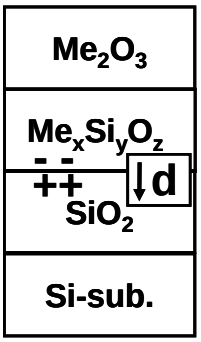
Fig.7.19 Angle-resolved XPS measurement of 3.0nm Gd_2O_3 on 1.5nm SiO_2: (a) Si 2p. Vertical lines:1 (Si^{+1}:101 eV)), 2(Si^{+2}:101.8eV), 3(Si^{+3}:102.9eV), 4(Si^{+4}:104eV) [2].(b) Gd 4d, (c) O 1s. Vertical solid line: (Si-O: 533.5eV), vertical dashed line: (Gd-induced peak: 531.87eV). The take-off angle was 15^o, 45^o and 75^o.

At the take-off angle of 75^o, XPS detected the deepest thickness of the samples. From Fig.7.19 (a) and (c), at the interface between Gd_2O_3 and SiO_2, Gd induced Si^{+3}-like bonding and O-bonding change.

At the take-off angle of 15^o, XPS detected the outmost surface layer of the sample. By carefully examining Fig.7.19 (a)-(c), we could conclude the outmost surface layer was Si-rich. It indicated that Si diffused though the Gd_2O_3 layer and piled at the outmost surface. Indeed, for rare-earth metal oxides deposited on Si (001) substrates, a silicate layer forms after high-temperature annealing with Si as the dominant diffusing species. It is found that Si diffuses more easily

into rare earth metal oxides with larger metal ion radii such as La_2O_3 and Pr_2O_3 [3, 4].

7.5 The model of the negative V_{fb} shift due to Me_2O_3 capping on SiO_2



Reaction mechanisms:

$x\ Me + y\ O_2 + SiO_2 \rightarrow Me_xSiO_{2y+2}$ (1)

Or

$x\ Me + 3\ SiO_2 \rightarrow 3\ Me_{(x-4)/3}Si + 2\ Me_2O_3$ (2)

$x\ O_2 + Me_ySi \rightarrow Me_ySiO_{2x}$ (3)

$x\ Me_2O_3 + y\ SiO_2 \rightarrow Me_{2x}Si_yO_{3x+2y}$ (4)

Here, Me=Gd, Y and Dy.

Fig.7.20 (L) Schematic diagram of the structure and the dipole formation at the interface of the silicate layer and the beveled SiO_2 layer. (R) Reaction mechanisms: Reaction (1) is valid for O-rich Me_2O_3; Reaction (2), (3), and (4) are valid for oxygen deficient Me_2O_3. In the latter case, Si-Me bonds might form [5].

Iwamoto *et al* have shown that the dipole formation at the Al_2O_3/SiO_2 interface and this interface is more important in controlling V_{fb} shift than the metal gate/high-k interface [6]. The V_{fb} value saturates when Al_2O_3 thickness increases more than 1.0nm. The almost constant negative V_{fb} shift versus beveled SiO_2 thickness before PMA in Fig. 7.8-10 indicates its dipole origin based on the general V_{fb} formula (Eq.9) in chapter 4 if we assume small contribution of the bulk charges. The dipole forms at the interface between

Me_2O_3 and interfacial SiO_2. The magnitude of negative V_{fb} shift increases with increasing Me_2O_3 thickness after PMA. A MeSiO layer is formed between Me_2O_3 and SiO_2. It is proposed that there are additional contributions to the negative V_{fb} shift after PMA. The above XPS data have shown that the silicon and oxygen bonding configuration change due to Gd_2O_3 capping before and after PMA. Another important question is at what Me_2O_3 thickness, the V_{fb} shift saturates. Before PMA, the negative V_{fb} shift saturates when Me_2O_3 thickness is larger than 1.5nm from Fig.7.8-10. After PMA, the V_{fb} shift does not saturate even for 4.5nm Me_2O_3. What causes this difference? LeBeau *et al* have studied Dy_2O_3 and Ho_2O_3 capping on HfSiON with TaN metal gate [7]. After 1000 ^oC/5s annealing, they observed the similar negative V_{fb} shift compared to the reference HfSiON MOSCAP with neither Dy_2O_3 nor Ho_2O_3 capping. They also observed the reduction of interfacial SiO_2 due to the oxygen deficiency in Dy_2O_3 and Ho_2O_3 and some crystallite grains extending from Dy_2O_3 or Ho_2O_3 into HfSiON. Based on this result, it is suggested that further transmission electron microscopy (TEM) investigation is needed to study why the magnitude of negative V_{fb} shift increases with increasing Me_2O_3 thickness in Fig 7.8-10.

From above discussion, we conclude that a dipole forms at the interface between Me_2O_3 (or MeSiO) and the interfacial SiO_2 layer. The dipole formation is due to the bonding configuration change (Si, O and Me) at the interface. When there is an oxygen deficiency in Me_2O_3, another dipole through Vo

mechanism is expected to form (Fig. 7.14(a)). As oxygen vacancies have already formed during Me_2O_3 deposition ("**No PDA**"), only electron transfer from Me_2O_3 to TaN is needed for the dipole formation. In addition, with oxygen deficiency in Me_2O_3, SiO_2 can be reduced and Si-Me bonds might form at the interface between MeSiO and the interfacial SiO_2 [5]. Thus the interfacial dipole is changed and an enhanced negative V_{fb} shift due to two-dipole formation (One dipole at the interface and the other one induced by oxygen vacancy) is observed. Fig.7.19 shows such a model. The small negative V_{fb} shift at the interface between S-SiO_2 and Me_2O_3 indicates the interface dipole critically depends on the microstructure at the high-k/SiO_2 interface.

7.6 NMOSFETs with Me_2O_3 capping on the beveled SiO_2 layers

In this experiment, we have studied NMOSFETs with a thin Me_2O_3 capping on the beveled SiO_2 layers in gate stacks. We also studied the effect of capping a HfO_2 layer on the Me_2O_3 layer. Table 7.1 gives structures of two kinds of gate stacks. The beveled SiO_2 thickness was 1.3, 4.0 and 6.5nm. The control stack is TaN/4nm HfO_2/1.3nm SiO_2/Si. As we have seen in above studies, capping a HfO_2 layer on Me_2O_3 results in a larger V_{fb} shift for Me=Gd and Y, and a much smaller one for Me=Dy. The reason is still not clear yet, but it is interesting to see that how such a difference affects the transistor

performance. PDA was performed at 600 ^{o}C for 5min in N_2 to make sure that there was not oxygen deficiency in Me_2O_3. We want to focus on the effects of the dipole at the interface between Me_2O_3 (or MeSiO) and interfacial SiO_2 only. Fig.7.21 shows the process flow for NMOSFET fabrication.

Table 7.1 Gate stack structures for NMOSFETs with 0.5nm Me_2O_3 on the beveled SiO_2 layers.

Beveled SiO_2	**The top part of a stack**
Control: 1.3nm SiO_2	**TaN/4nm HfO_2**
1.3nm SiO_2	**A) TaN/3nm HfO_2/0.5nm Me_2O_3**
4.0nm SiO_2	**A) TaN/3nm HfO_2/0.5nm Me_2O_3** **B) TaN/0.5nm Me_2O_3**
6.5nm SiO_2	**A) TaN/3nm HfO_2/0.5nm Me_2O_3** **B) TaN/0.5nm Me_2O_3**

- Field oxide growth and active pattern formation
- RCA clean and the beveled thermal SiO_2 growth
- Me_2O_3 and HfO_2 sputter from Me and Hf targets
- PDA: $600^oC/5min/N_2$
- TaN (200 nm) deposition and patterning using CF_4 RIE
- S/D implantation: $P/50keV/5\times10^{15}/cm^2$
- Dilute HF dip and LTO (200nm) deposition
- Contact etching and implant activation ($900^oC/1min/N_2$)
- Front Al deposition and patterning
- Backside Al deposition
- Forming gas anneal at $400^oC/30min$

Fig.7.21 Process flow for NMOSFET fabrication

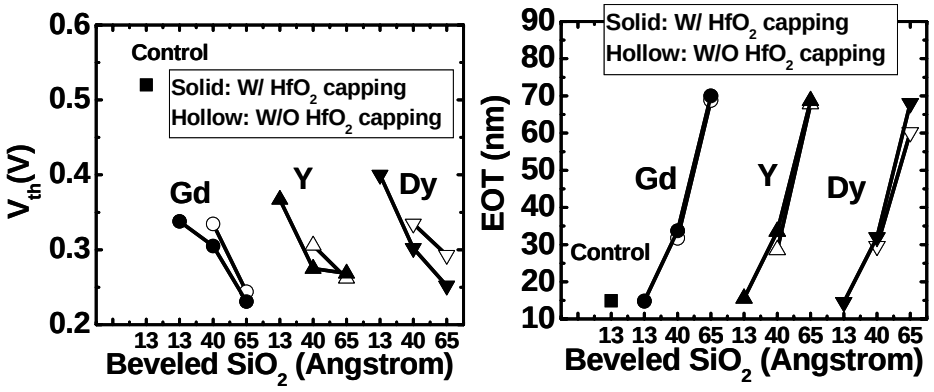


Fig.7.22 V_{th} and EOT of NMOSFETs versus the beveled SiO_2 thickness with Me_2O_3 capping (Me=Gd, Y, and Dy).

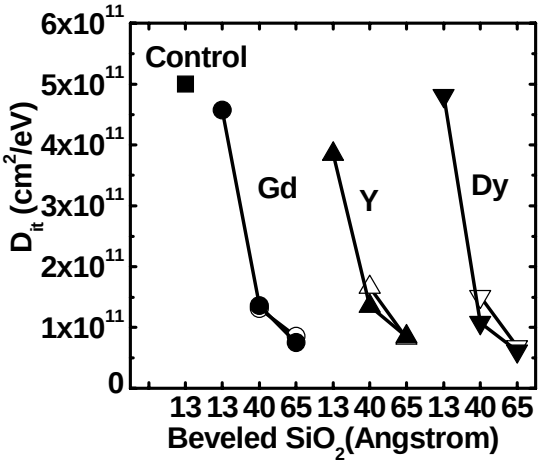


Fig.7.23 The density of interface states (D_{it}) versus the beveled SiO_2 thickness measured by the charge- pumping technique with (Solid) and without (Hollow) HfO_2 capping layer on Me_2O_3.

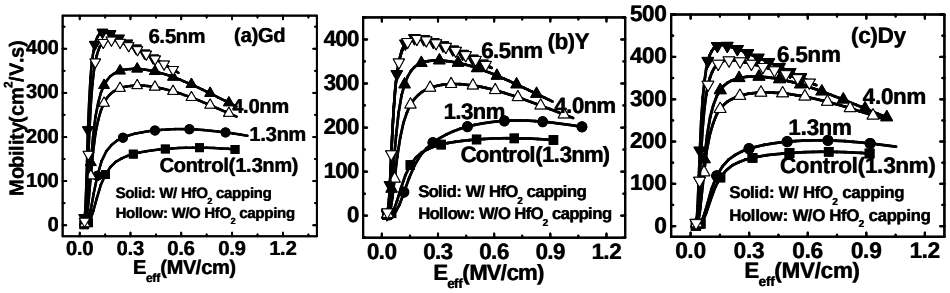


Fig.7.24 Electron mobility versus E_{eff} for NMOSFETs with Gd (a), Y (b) and Dy (c), respectively. Solid and Hollow symbols are for devices with and without 3nm HfO_2 capping, respectively.

Fig.7.22 shows threshold voltage (V_{th}) and EOT. Comparing with the control HfO_2 stack, capping Me_2O_3 makes V_{th} decrease at least 250 mV. For the same beveled SiO_2 thickness, it is slightly decreased by capping 3nm HfO_2 on 0.5nm Me_2O_3. It is different from the trend extracted on MOSCAPs. One possible reason is that the thickness of Me_2O_3 is too thin (See Fig.7.8-10). Another trend of V_{th} decreasing with increasing beveled SiO_2 thickness is very clear. In Fig.7.7, even in the case of only HfO_2 capping, V_{fb} shift versus beveled SiO_2 thickness is not a constant for a fixed high-k layer after PMA. So it is not clear at this moment whether V_{th} decreasing with increasing beveled SiO_2 thickness is caused by the interaction between Me_2O_3 and SiO_2 or by other reasons. Fig.7.23 presents the density of interface states (D_{it}) measured using the charge pumping technique. The D_{it} decreases with increasing the beveled SiO_2 thickness. For 1.3nm beveled SiO_2 thickness, capping 0.5nm Me_2O_3 on SiO_2 does not degrade the interface quality compared to the control device. Fig.7.24 shows electron mobility versus effective electric field. The MOSFETs of 3nm HfO_2/0.5nm Me_2O_3/1.3nm SiO_2/Si exhibit a higher mobility than the control device. For 4.0 and 6.5nm SiO_2, the mobility is higher for the stack with the 3nm HfO_2 capping.

7.7 Summary

In summary, we have studied the mechanism of the negative V_{fb} shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2-related high-k dielectrics with TaN metal gate. We have shown that due to the interaction between Me_2O_3 and SiO_2, a dipole forms at the interface between the MeSiO layer and the remaining interfacial SiO_2 layer. This dipole is due to the local bonding configuration change (Si, O and Me) at the interface between MeSiO and the interfacial SiO_2. Our data on NMOSFETs have shown that the dipole could decrease the threshold voltage at least 250 mV. In addition, with Me_2O_3 capping, the electron mobility was also improved compared to the HfO_2 control device.

7.8 References

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Chapter 8

Me_2O_3 (Me=Gd, Y and Dy) Capping on SiO_2 and HfO_2 with W and Pt Metal Gate

8.1 Overview

In this chapter, we study mechanism of the V_{fb} shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2 with W and Pt metal gate. We have observed the V_{fb} shift due to the dipole change at M-D interfaces for W and Pt after a forming gas anneal or an oxygen gas anneal. For thin interfacial SiO_2 layers, it is shown to be possible for another dipole to form through the Vo mechanism. The study suggests it is interesting to explore the possible interaction among three dipoles: the dipole at the M-D interface, the dipole at the interface between the silicate layer (MeSiO) and the interfacial SiO_2, and the dipole formed through the oxygen vacancy (Vo) mechanism.

8.2 Motivation

As we have discussed in chapter 4, the dipole formation at the interface between metal gate and high-k dielectric (M-D) is one of Fermi-level pinning mechanisms. This dipole changes with materials and processes. For example, Ohmori *et al* have shown that the dipoles at the interfaces of W/HfO_2 and Pt/HfO_2 change after a forming gas anneal (FGA) or an oxygen gas anneal

(OGA) at temperature from 250 to 450 ^{o}C [1]. W and Pt have a relatively large difference in work function (4.7 and 5.5 eV for W and Pt, respectively) with the number of valence electrons changing from ($5d^4 6s^2$, W) to ($5d^9 6s^1$, Pt). By using a W-Pt mixture as the metal gate, they have measured V_{fb} shift versus Pt ratio in the W-Pt gate (Fig.8.1). We want to study Me_2O_3 (Me=Gd, Y and Dy) capping on SiO_2 and HfO_2 with W and Pt metal gate. Our goal is to explore the possible interaction among three dipoles: the dipole at the M-D interface, the dipole at the interface between the silicate layer (MeSiO) and the interfacial SiO_2, and the dipole formed through the oxygen vacancy (Vo) mechanism [2].

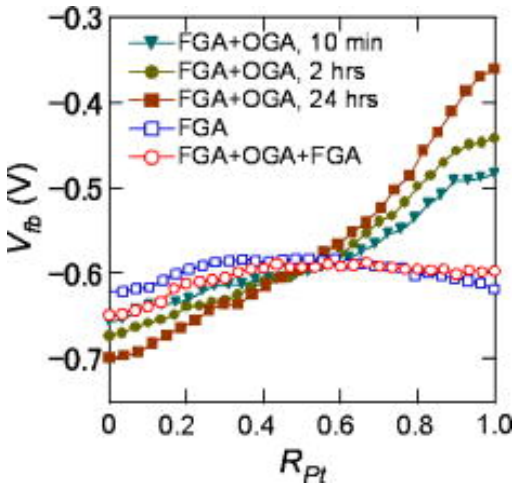

Fig. 8.1 V_{fb} dependence on annealing ambient as a function of the Pt ratio (R_{Pt}) in the W-Pt mixture metal gate. The V_{fb} curves for all annealing conditions cross over at R_{Pt}=0.46. The annealing conditions are:(1) FGA at 450 °C, (2) FGA at 450 °C+OGA at 250 °C with OGA annealing times of 10 min, 2 and 24 h, and

(3) FGA at 450 °C +OGA at 300 °C/30min+FGA at 450 °C. FGA was performed for 30 min. The resistivity of the *p*-type Si is 0.01–0.02 Ω cm [1].

8.2 V_{fb} shift analysis: comparison of different gate stacks with W gate

8.2.1 V_{fb} shift analysis: the effect of the different interfaces (W/HfO_2, W/Me_2O_3, HfO_2/SiO_2 and Me_2O_3/SiO_2)

Gate structures of S5, S6, S7 and S8 in Chapter 7 were shown here again to compare the effect of the different interfaces (Fig.8.2). S5 and S6 focus on W-HfO_2 and W/Me_2O_3, and S7 and S8 on HfO_2/SiO_2 and Me_2O_3/SiO_2**.** As can be seen that V_{fb} of S5 and S6 are almost same for Me=Gd, Y and Dy. The large negative V_{fb} shift was observed for both S7 and S8. The same V_{fb} shift in S5 and S6 indicated the contribution from the dipole moments at W/HfO_2 and W/Me_2O_3 was same. The negative V_{fb} shift was due to the direct contact interaction between Me_2O_3 and the beveled SiO_2 layer.

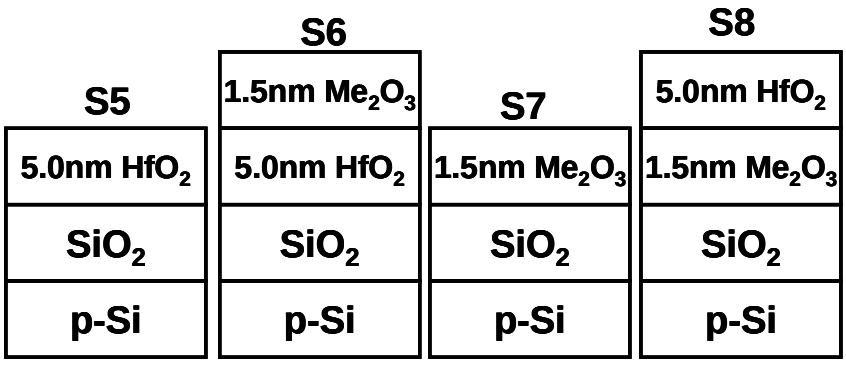

Fig. 8.2 Gate structures of S5, S6, S7 and S8.

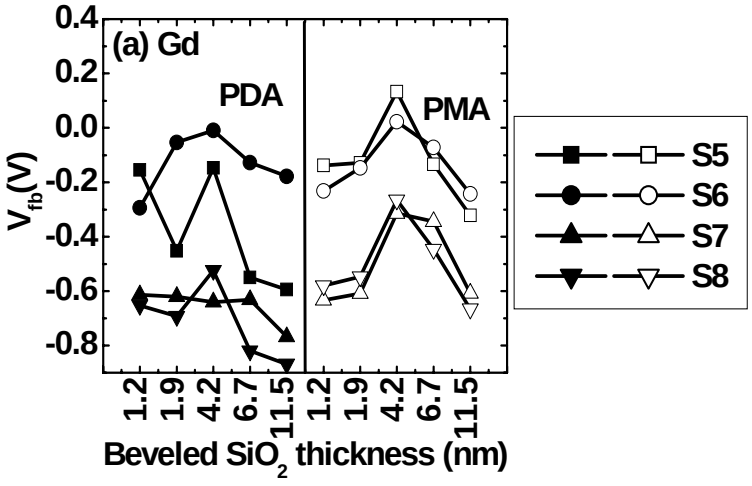

Fig.8.3 (a) V_{fb} of S5, S6, S7 and S8 with Me= Gd without and with PMA at 900 ^{o}C/1min/N_2.

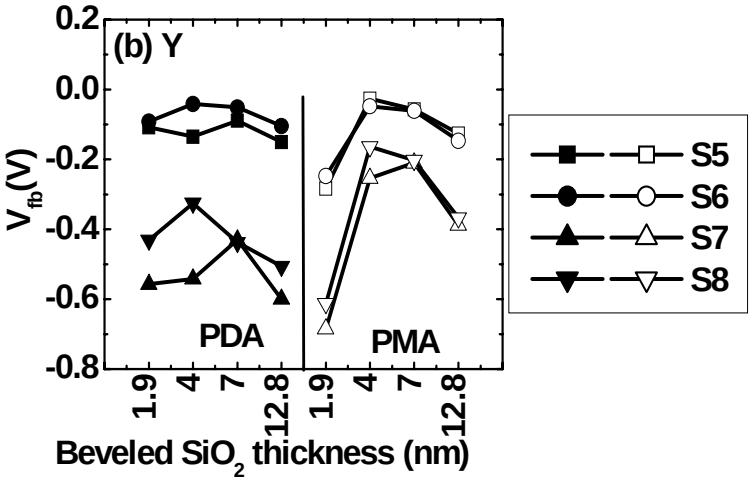

Fig.8.3 (b) V_{fb} of S5, S6, S7 and S8 with Me= Y without and with PMA at 900 ^{o}C/1min/N_2.

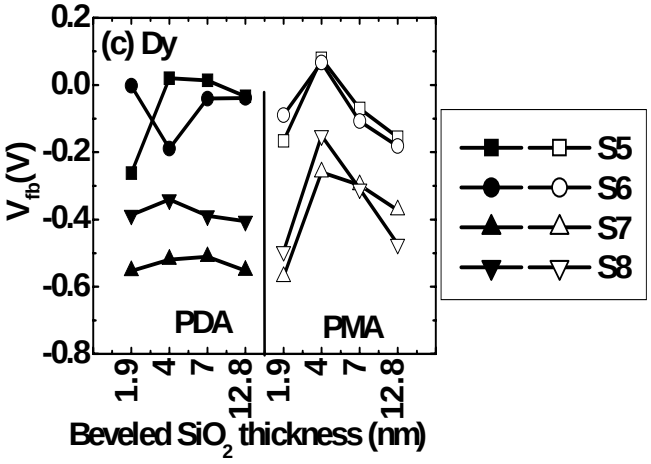

Fig.8.3 (c) V_{fb} of S5, S6, S7 and S8 with Me= Dy without and with PMA at 900 $^{o}C/1min/N_2$.

8.2.2 V_{fb} shift analysis: the effect of varying the beveled SiO_2 and Me_2O_3 thickness

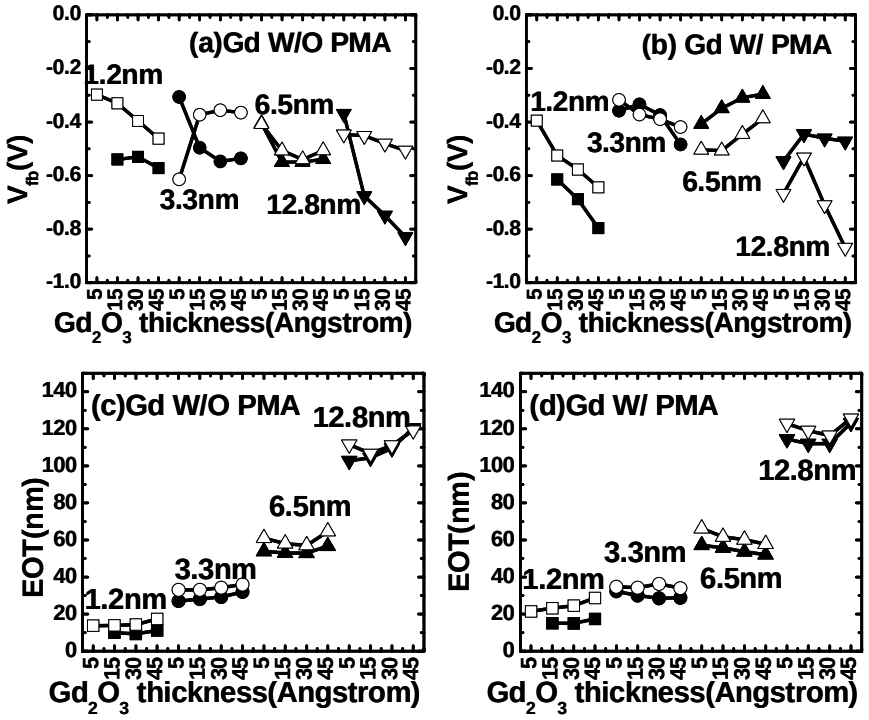

Fig. 8.4 The change of V_{fb} and EOT in S7 and S8 with varying the thicknesses of both Gd_2O_3 and SiO_2 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm.

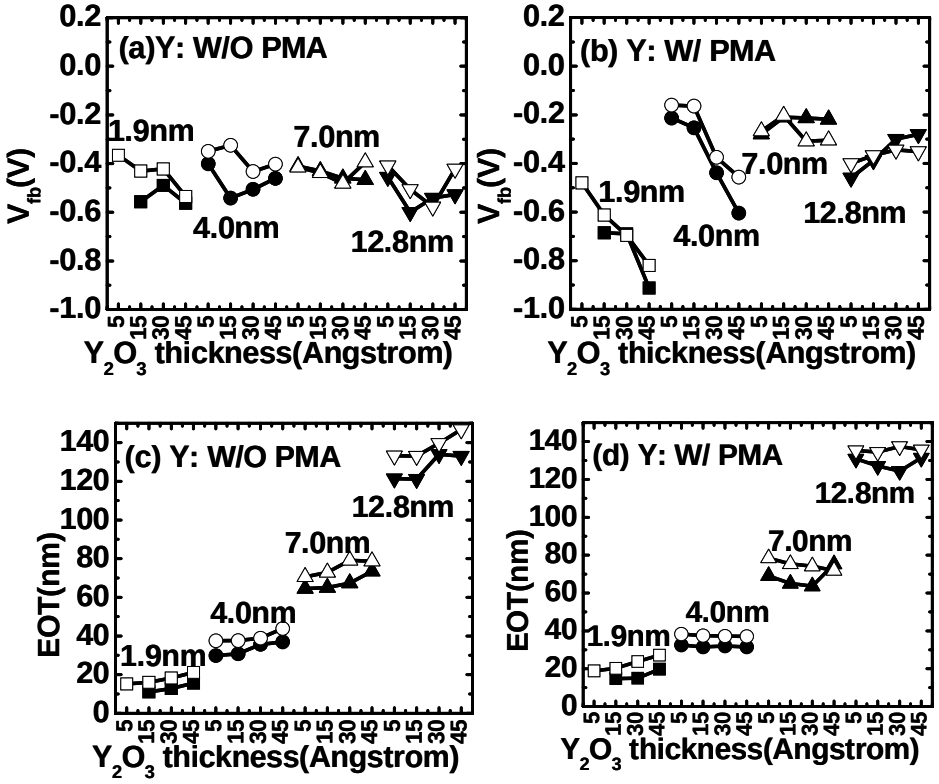

Fig.8.5 The change of V_{fb} and EOT in S7 and S8 with varying the thickness of both Y_2O_3 and SiO_2 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm.

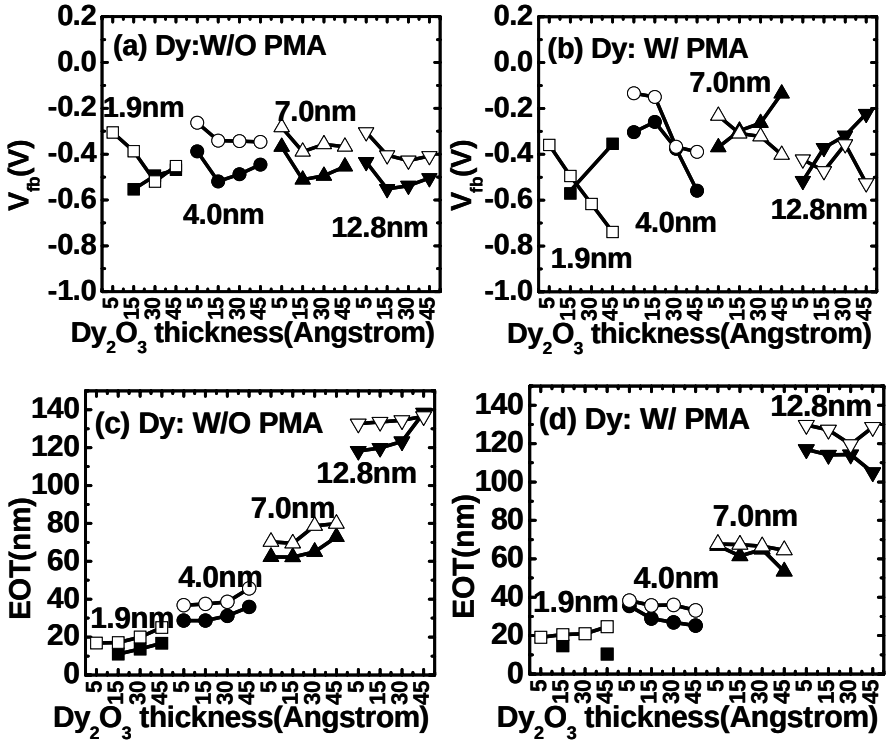

Fig.8.6 The change of V_{fb} and EOT in S7 and S8 with varying the thicknesses of both Dy_2O_3 and SiO_2 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm.

We further studied the V_{fb} shift by varying the thicknesses of both Me_2O_3 and SiO_2 in S7 and S8 while keeping the thickness of capping-HfO_2 in S8 at 5.0nm (Fig.8.5-7). Between S7 and S8, the negative V_{fb} shift was larger in S7 without PMA. It became larger in S8 for thick Me_2O_3 layers and thick beveled SiO_2 layers (the diffusion dominant region) after PMA. The trend change was

very clear for Gd_2O_3. The underlying reason is still not clear yet. It might be related to the dipole change at the M-D interface related to W-O bonds [1].

8.3 V_{fb} shift analysis: comparison of different gate stacks with Pt gate

8.3.1 Thick beveled SiO_2 layers

Fig.8.7 shows 12 gate stacks used to study the V_{fb} shift with Pt gate. The beveled SiO_2 layer was thermally grown. Me_2O_3 was deposited by DC sputtering with Me=Gd, Y and Dy. The PDA condition was 500^{o}C/5 min/N_2. Pt gate (25nm) was deposited by DC sputtering and etched in HCl:HNO_3=3:1 at 70^{o}C. After the backside Al contact deposition, samples went through a forming gas annealing (FGA) at 450^{o}C for 30 min. Then samples were divided into 2 splits, and one of them went through an oxygen gas annealing (OGA) at 400^{o}C for 60 min.

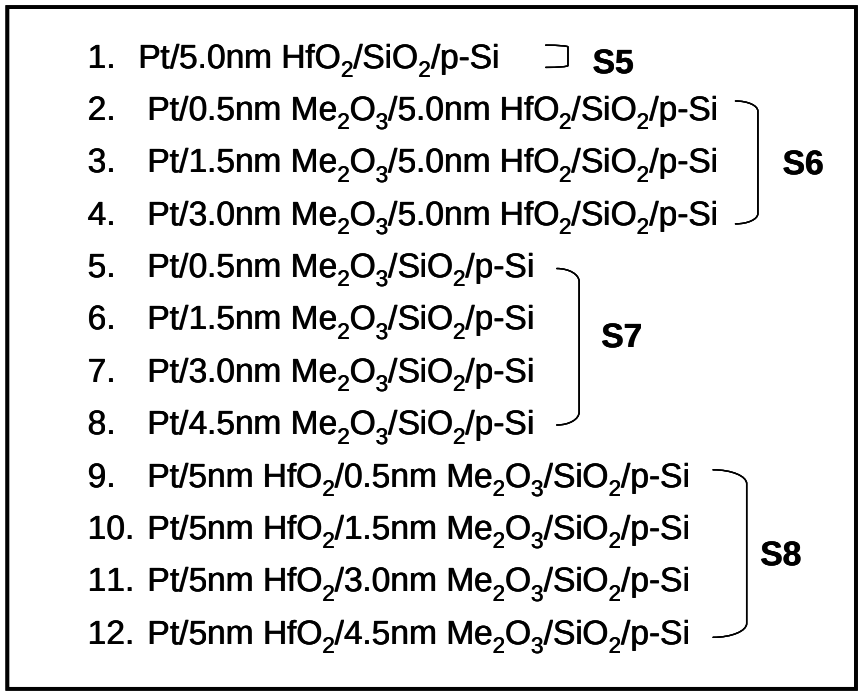

Fig.8.7 Gate stacks used to study the V_{fb} shift with Pt gate for Me=Gd, Y and Dy. The thickness of Pt was 25nm deposited by sputtering. As shown in the figure, they correspond to S5, S6, S7 and S8, respectively.

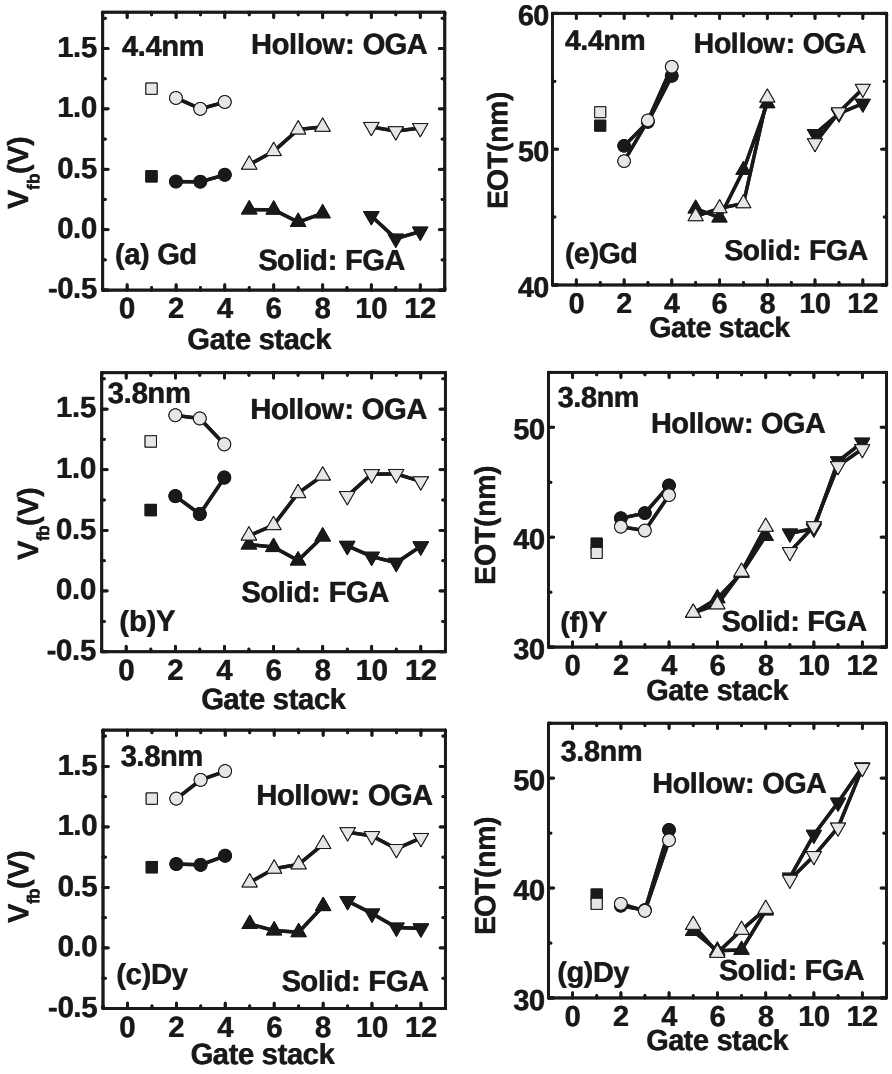

Fig.8.8 V_{fb} and EOT of 12 gate stacks for Me=Gd, Y and Dy after a FGA at 450 ^{o}C/30min and a sequent OGA at 400 ^{o}C/60 min. The beveled SiO_2 thickness was also shown in each figure.

Fig.8.8 shows V_{fb} and EOT of 12 gate stacks (corresponding to four structures: S5, S6, S7 and S8) for Me=Gd, Y and Dy after a FGA at 450 ^{o}C/30min and a sequent OGA at 400 ^{o}C/60 min. The beveled SiO_2 thickness was about 4.0nm. It can be seen that the gate stacks corresponding to S7 and S8 have smaller V_{fb} values than those corresponding to S5 and S6, indicating the negative V_{fb} shift due to the dipole induced by Gd_2O_3 capping on SiO_2. The positive V_{fb} shift after OGA was observed for all gate stacks due to the dipole change at the M-D interface [3]. From S5 and S6-type gate stacks, the order of the dipole change at M-D interfaces are Pt/Dy_2O_3~Pt/Y_2O_3>Pt/HfO_2>Pt/Gd_2O_3 after an OGA. The positive V_{fb} shift is still much smaller than Pt/La_2O_3 after an OGA [4]. The data in Fig. 8.8 (e), (f) and (g) also show that EOT almost did not increase after the OGA.

In the following we want to compare V_{fb} shift by capping a Gd_2O_3 layer on gate dielectrics with a thin (1.3nm) and a thick beveled SiO_2 layer (4.4nm).

8.3.2 Thin beveled SiO_2 layers

Fig.8.9 shows V_{fb} and EOT of 12 gate stacks with Gd_2O_3 capping after a FGA at 450 ^{o}C/30min and a sequent OGA at 400 ^{o}C/60min. Two different beveled SiO_2 thicknesses (1.3 and 4.4nm) were compared. For the 1.3nm beveled SiO_2 thickness, the positive V_{fb} shift of S7 and S8-type gate stacks after the OGA was smaller than that for the 4.4nm beveled SiO_2 thickness. At the

same time, a 0.2nm EOT increase was also observed. We explain the data by considering another dipole formation through oxygen vacancy (Vo) mechanism, which is expected to be important for thin beveled SiO_2 layers [3]. It is also expected that for thin beveled SiO_2 layers, the Vo mechanism would also enhance the dipole moment induced by Gd_2O_3, because it is sensitive to the oxygen deficiency. Fig.8.10 shows formation of three dipoles in a gate stack

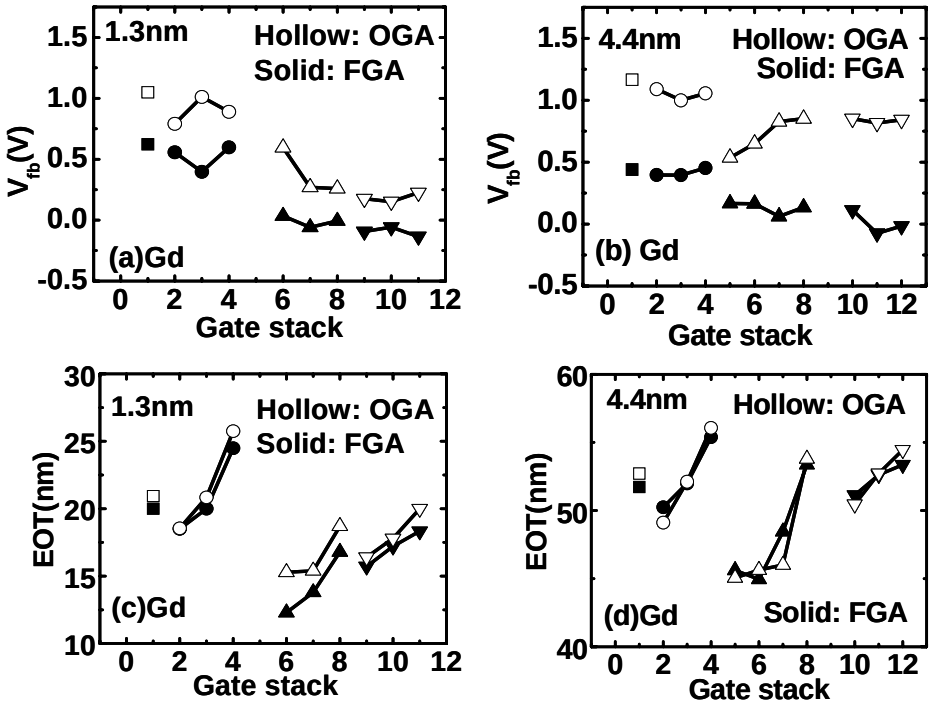

Fig.8.9 V_{fb} and EOT of 12 gate stacks for Gd_2O_3 capping after a FGA at 450 ^oC/30min and a sequent OGA at 400^oC/60min. The beveled SiO_2 thicknesses (1.3 and 4.4nm) were shown in each figure.

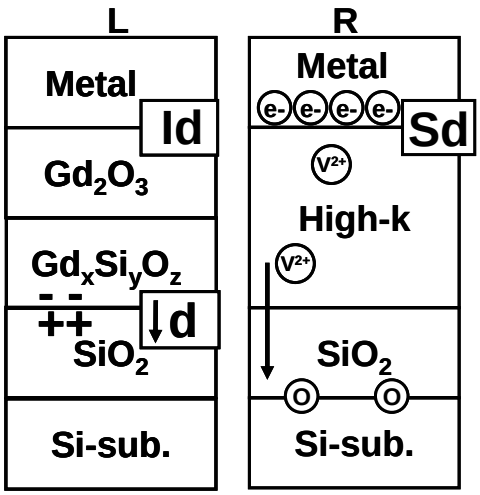

Fig.8.10 (L) schematic diagram of the dipole (**Id**) at the metal/dielectric (M-D) interface, and the dipole (**d**) at the interface between $Gd_xSi_yO_z$ and the beveled SiO_2; (R) for thin beveled SiO_2 layers, the dipole (**Sd**) formation through Vo mechanism.

8.4 Summary

We have studied Me_2O_3 (Me=Gd, Y and Dy) capping on SiO_2 and HfO_2 with W and Pt metal gate. We have observed the V_{fb} shift due to the dipole change at M-D interfaces for W and Pt after a forming gas anneal or an oxygen gas anneal. It is shown to be possible for additional dipole to form through the Vo mechanism for thin interfacial SiO_2 layers. The study suggests a new way to explore the possible interaction among the dipole at the M-D interface, the

dipole at the interface between the silicate layer (MeSiO) and the interfacial SiO_2, and the dipole formed through the oxygen vacancy (Vo) mechanism.

8.5 References

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Chapter 9

XPS Study of Gate Metal Bonding State Change at the Metal-dielectric Interface

9.1 Overview

In this chapter, XPS material analysis has been done Gd_2O_3 capped gate stacks to understand the bonding state change. In addition, we propose an ex situ method to measure the binding energy profile of the metal element in a metal gate versus the distance to the metal/dielectric interface using XPS. It can provide us some very important information about the effective work function of the metal gate.

9.2 XPS technique

X-ray photoelectron spectroscopy (XPS) is a powerful tool to study bonding in high-k dielectrics. In XPS, a core electron is emitted into the free space by absorbing an x-ray photon. This emitted electron is called a photoelectron. The kinetic energy of the photoelectron is

$$KE_0=h\upsilon-(BE_F+\phi_{sample}). \qquad (1)$$

Here ϕ_{sample} is the work function of the sample. BE_F is the binding energy with respect to the Fermi level of the sample.

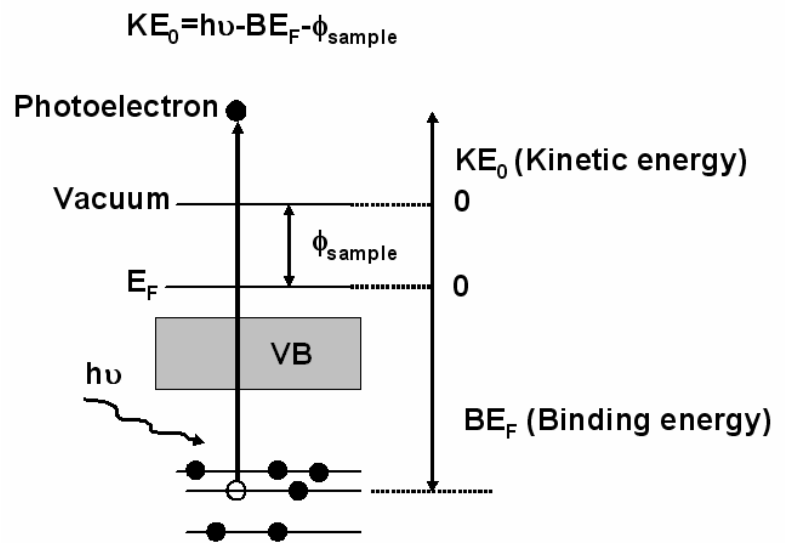

Fig.9.1 Schematic process of generating an x-ray photoelectron. Vacuum is the vacuum level. E_f is the Fermi level. VB is the top valence band. KE_0 is the kinetic energy of the photoelectron. BE_F is the binding energy with respect to the Fermi level of the sample.

In XPS spectrum, intensities of photoelectrons versus BE_F or KE_0 are measured. Due to different work function in the sample and the photoelectron spectrometer, the final kinetic energy (KE) is different from its initial value (KE_0) when a photoelectron is just emitted from the sample. Fig.9.2 shows the energy diagram in XPS [1]. By grounding both the sample and the spectrometer, a common Fermi-level can be achieved in the sample and the spectrometer. In this way, the binding energy can be measured by

$$BE_F = h\upsilon - KE - \phi_{spec.} \qquad (2)$$

Here ϕ_{spec} is the work function of the spectrometer and KE is the electron kinetic energy measured by the spectrometer directly.

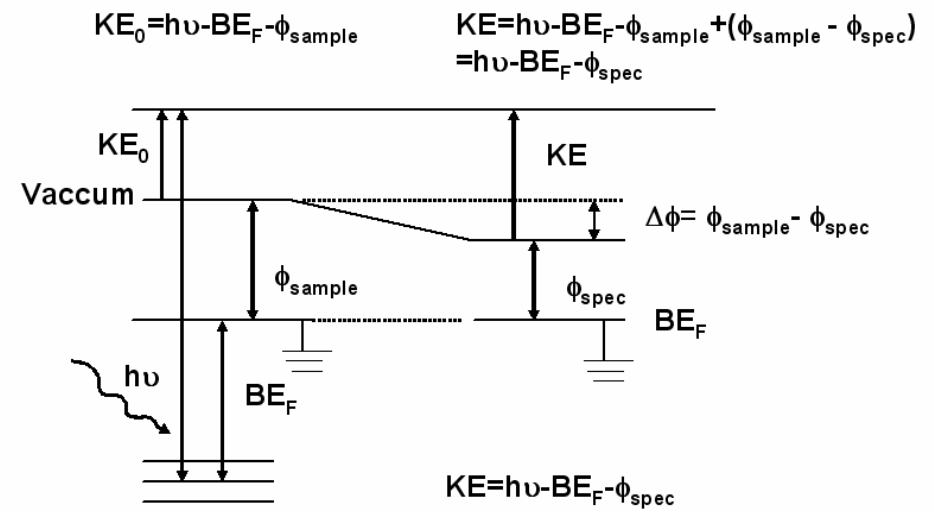

Fig.9.2 Kinetic energy measurement and binding energy reference in XPS.

Most often, the sample is not grounded and the charging causes the Fermi-level to float in the sample. So the binding energy changes from one experiment to another. In our experiment, we deposited a backside Al electrode and used a metal sample holder to ground the sample. However, for thick high-k dielectric layers, charging can not be removed completely even with the help of an electron neutral gun.

Assuming the sample has the same Fermi level with the spectrometer, Lebedinskii proposed a method to measure the effective work function of a

metal gate on HfO_2 [1]. If there is no chemical shift for Hf or O near the metal gate in a gate dielectric stack, then the binding energy shift will reflect the effective work function change of metal gate. In principle, this method works for XPS measurement with *in situ* metal gate deposition. In reality, however, it is often very difficult to judge whether there is chemical shift or not.

We propose an *ex situ* method to measure the binding energy profile of the metal element in a metal gate near the metal/dielectric interface using XPS. A gate stack can go through high temperature anneal and thus has a very high chemical shift of the metal binding energy near the metal/dielectric interface. For two different gate dielectrics with same metal as metal gates, if the binding energy profiles of the metal gates are almost same, it is proposed that the metal gates on two stacks should have the same effective work function. Although this method is not able to measure the effective work function directly, it can provide us some important information about the effective work function. We will show some data of TaN and Pt on HfO_2 and Gd_2O_3 capped gate stacks.

9.3 Experimental

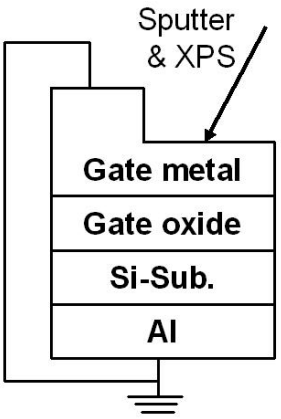

Fig.9.3 Schematic diagram to measure bonding states of metal gate using XPS profiling by sputtering metal gate little by little.

In this experiment, we proposed a new method to study metal gate bonding change near metal-dielectric interface based on XPS. Fig.9.3 shows the schematic diagram. Far from the metal-dielectric (M-D) interface, the binding energy was determined by the intrinsic property of metal gate. By sputtering away metal little by little, we could measure the metal binding energy change versus the distance. This profile could give us some important information about the dipole at the M-D interface.

Fig.9.4 shows the binding energy shift versus sputter time for (a) Hf $4f_{7/2}$ and Ta $4f_{7/2}$ with TaN, and (b) Hf $4f_{7/2}$ and Pt $4f_{7/2}$ with Pt. The four studied stacks were S5: 5nm HfO_2/4nm SiO_2/p-Si, S6: 1.5nm Gd_2O_3/5nm HfO_2/4nm SiO_2/p-Si, S7: 1.5nm Gd_2O_3/4nm SiO_2/p-Si and S8: 5nm HfO_2/1.5nm Gd_2O_3/4.0nm SiO_2/p-Si. They went through a FGA at 400^oC/20min after contact

deposition. No PMA was performed. The top TaN and Pt thickness were 16 and 12nm, respectively. For TaN metal gate, the binding energy of Ta $4f_{7/2}$ at the M-D interface is almost same for all four stacks, while for Pt metal gate, the binding energy of Pt $4f_{7/2}$ for S7 is different from the other three stacks at the M-D interface. One reasonable explanation was the Si out-diffusion in S7, which altered the dipole at the M-D interface. Fig.9.5 shows there are two kinds of Pt bonding states near the M-D interface. The bonding state with the stronger intensity is chosen for Fig. 9.4 (b).

We have observed a large V_{fb} shift in MOSCAPs with Pt metal gate upon an OGA. It suggests that the Pt bonding state changes after an OGA. It is desirable to use this method to study Pt bonding states at the M-D interface after an OGA in the future.

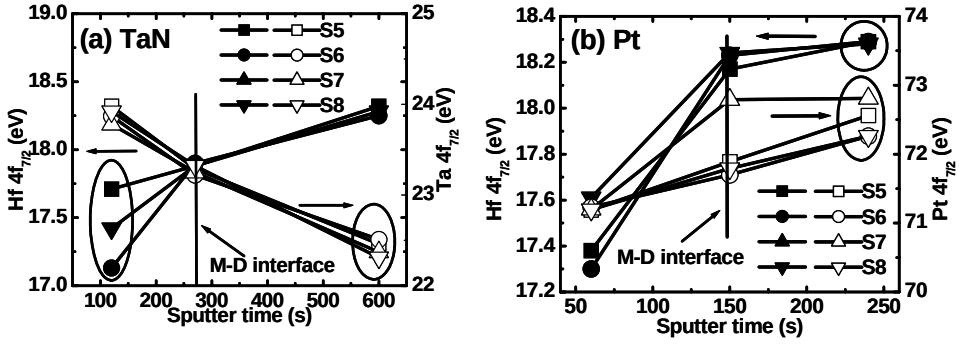

Fig.9.4 The binding energy versus sputter time: (a) Hf $4f_{7/2}$ and Ta $4f_{7/2}$ and (b) Hf $4f_{7/2}$ and Pt $4f_{7/2}$. The take-off angle was 45 ^{o}.

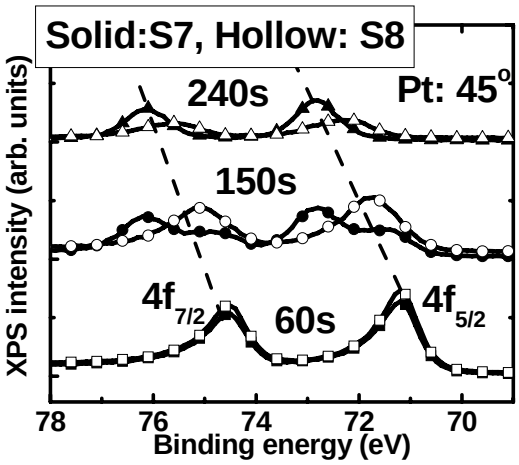

Fig.9.5 The binding energy versus sputter time: (a) Hf $4f_{7/2}$ and Ta $4f_{7/2}$ and (b) Hf $4f_{7/2}$ and Pt $4f_{7/2}$. The take-off angle was 45 ^{o}.

9.4 Summary

We have used XPS to study the bonding states in Gd_2O_3 capped SiO_2 gate stacks. We have found that capping a layer of Gd_2O_3 on SiO_2 resulted in silicide or silicate formation. For a thin interfacial SiO_2 layer, thick Gd_2O_3 layers enhanced the Si oxidation after high temperature annealing. Some Si atoms are found to diffuse to the outmost surface layer. Finally we propose a new method to study metal gate bonding change near the metal-dielectric interface based on XPS. We have applied this method to TaN and Pt metal gate on Gd_2O_3-capped gate dielectrics.

9.5 References

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Chapter 10

Summary and Future Work

10.1 Summary

Continuing to scale down the transistor size makes the introduction of high-k dielectric necessary. However, there are a lot of problems with high-k transistors such as bad reliability and Fermi-level pinning. In HfO_2, low crystallization temperature, defects or charges in the bulk HfO_2 and low quality of the Si/HfO_2 interface cause bad reliability. Fermi-level pinning causes the problem of high threshold voltages.

In chapter 2, forming $Hf_{1-x}Ta_xO$ through doping HfO_2 with Ta is used to improve the crystallization temperature. Electron mobility is shown to increase with the increase of the crystallization temperature. The highest crystallization temperature and the maximum mobility is observed at x=0.4.

In chapter 3, the fluorine passivation of high-k dielectrics is studied. The bonding energy (5.81 eV) for a single Si-F is much larger than that (3.6 eV) for a single Si-H bond. With fluorine passivation, the electron mobility was shown to improve in NMOSFETs with gate stacks of poly-$Si/TaN/HfO_2$/Si-substrate with thin TaN layers. Inserting a 1.5nm layer of HfSiON between TaN and HfO_2 completely blocked the fluorine atoms so that they could not reach the Si

interface. Thus, no mobility improvement was observed even with fluorine implantation.

In order to get a low threshold voltage, mechanisms of Fermi level pinning (FLP) in high-k gate stacks must be studied. We summarize three FLP mechanisms: (1) the dipole formation at the interface between metal gate and high-k dielectric due to hybridization, 2) the dipole formation through oxygen vacancy (Vo) mechanism, which is especially important for poly-Si and p-metal after high-temperature anneal, (3) the dipole formation at the interface between high-k dielectric and interfacial SiO_2. It is not a FLP according to the strict definition of FLP. We take it as one FLP mechanism because the dipole induced by this mechanism has the similar effect to the flatband voltage or threshold voltage as the dipoles induced by the other two mechanisms.

For poly-Si/HfO_2 interface, the FLP is through the Vo mechanism. For PMOSFETs with metal gate and high-k dielectrics, the roll-off of the flatband voltage (V_{fb}) at low EOT is also caused by the FLP through the Vo mechanism. Changing the metal and high-k dielectric combination may change the dipole at metal/high-k dielectric interface and thus change the V_{fb}.

Experimentally, it is found that capping a thin layer of lanthanide oxides (Me_2O_3) on SiO_2 and HfO_2 with TaN, TiN and TaC metal gate causes the V_{fb} to shift negatively; With Pt metal gate, it causes V_{fb} to shift positively after an oxygen gas anneal (OGA) due to the dipole change at Pt/high-k interfaces.

Pt/La_2O_3 interface gives a higher positive V_{fb} shift than Pt/HfO_2 interface. The rest of dissertation (from chapter 4 to 9) focuses on the mechanism of V_{fb} shift by capping a thin layer of Me_2O_3 (Me=Gd, Y and Dy) on SiO_2 and HfO_2 with TaN, W and Pt metal gate. For a full understanding of the V_{fb} shift, all three FLP mechanisms must be considered. Experiments have been designed to examine the contribution of each mechanism.

We rule out MeHfO, MeSiO and the dipole change at TaN/Me_2O_3 as the reason of the negative V_{fb} shift. We show that the direct contact interaction between Me_2O_3 and the interfacial SiO_2 is one of the reasons of the negative V_{fb} shift with TaN. A silicate layer (MeSiO) forms due to the reaction between Me_2O_3 and SiO_2, and a dipole is proposed to form at the interface of $MeSiO/SiO_2$. An XPS (X-ray photoelectron spectroscopy) study of Gd_2O_3 capping on SiO_2 indicates clear Si, O and Gd related bonding configuration change at the interface between Me_2O_3 (or MeSiO) and the interfacial SiO_2. So the bonding configuration change is the root cause to the dipole formation. When there is an oxygen deficiency in Me_2O_3 formed during Me_2O_3 deposition, another dipole formation through oxygen vacancy mechanism can also be observed. NMOSFETs with Me_2O_3 capping layers on SiO_2 have been fabricated. Comparing with the HfO_2-only device, the Me_2O_3 capping does not degrade the electron mobility.

The V_{fb} values of Pt/Me_2O_3/HfO_2/SiO_2/p-Si are almost same as that of Pt/HfO_2/SiO_2/p-Si after a forming gas anneal (FGA) at 450^{o}C/30min. The positive V_{fb} shift component of Pt/Me_2O_3/HfO_2/SiO_2/p-Si after a sequent oxygen gas anneal (OGA) at 400^{o}C/60min has the following order: Y_2O_3~Dy_2O_3>HfO_2>Gd_2O_3. However, in contrast with Pt/La_2O_3, the difference is not very large (<0.2V) for Y_2O_3, Dy_2O_3, HfO_2 and Gd_2O_3. Pt metal gate with Me_2O_3 capping provides us a system to study the interaction between the dipole induced by Me_2O_3 capping and the dipole at Pt/dielectric interface. For small EOT (thin interfacial SiO_2), another dipole formation through oxygen vacancy mechanism is expected to happen. In this case, all three FLP mechanisms must be considered.

We also propose a new method to study metal gate bonding change at metal-dielectric interface based on XPS. Far from the metal/dielectric interface, the binding energy is determined by the intrinsic property of metal gate. By sputtering away metal little by little, we can measure the metal binding energy change versus the distance. This profile can give us some important information about the dipole at the metal/dielectric interface.

10.2 Future work

10.2.1 Clarifying the V_{fb} shift of TaN/HfO_2/SiO_2/p-Si versus the beveled SiO_2 thickness

In chapter 8, V_{fb} value of TaN/5nm HfO_2/SiO_2/p-Si versus the beveled SiO_2 thickness is not constant. V_{fb} decreases with decreasing the SiO_2 thickness (<4.0nm), and decreases with increasing the SiO_2 thickness (>4.0nm). There are several reasons for this. One is due to the SiO_2 growth recipe. Due to equipment limitation, the beveled SiO_2 (<4.0nm) was thermally grown at 700 ^oC in a furnace in N_2 with a short time. The thick beveled SiO_2 (≥4.0nm) was thermally grown at 850 ^oC in a furnace in O_2 with the time longer than 5min. As the gate stack of TaN/5nm HfO_2/SiO_2/p-Si is the reference to study the V_{fb} shift by capping Me_2O_3 on SiO_2 and HfO_2 based high-k dielectrics, the V_{fb} shift of TaN/5nm HfO_2/SiO_2/p-Si versus the beveled SiO_2 thickness must be clarified.

10.2.2 Clarifying the dipole formation at the interface between MeSiO and the interfacial SiO_2 on the atomic scale

We have shown that the negative V_{fb} shift induced by Me_2O_3 capping is caused by a dipole formation at the interface between MeSiO and the interfacial SiO_2. However, the picture of the dipole formation on the atomic scale is still not available.

In Fig. 7.8-10, chapter 7, the magnitude of the negative V_{fb} shift after PMA is seen to increase with increasing of Me_2O_3 thickness. A rough interface between MeSiO and SiO_2 and the extending of crystallite grains of Me_2O_3 into SiO_2 might be the reasons. A TEM analysis will be helpful to answer the question.

Another important question is that at what thickness of the Me_2O_3 capping layer, the V_{fb} shift starts to saturate. Before PMA, the V_{fb} shift saturates when Me_2O_3 thickness is larger than 1.5nm from Fig.7.8-10. After PMA, the V_{fb} shift does not saturate even for 4.5nm Me_2O_3 (Fig.7.8-10). What causes this difference? It is the half part of the dipole: Me_2O_3. What happens to the other part of the dipole: SiO_2? What is the effect on the V_{fb} shift if small amounts of Me diffuse into SiO_2?

10.2.3 Further study of V_{fb} shift of Me_2O_3 capping with Pt metal gate

For thick interfacial SiO_2 layers, V_{fb} study of Me_2O_3 capping with Pt metal gate after a FGA or an OGA gives us an opportunity to explore the interaction between the dipole induced by Me_2O_3 capping and the dipole at Pt/dielectric interface. For small EOT (thin interfacial SiO_2), another dipole formation through the Vo mechanism is expected to happen. Further V_{fb} study of Me_2O_3 capping with Pt metal gate after a FGA or an OGA will let us study the

interaction among three dipoles formed through three different FLP mechanisms.

10.2.4 Further XPS study of binding energy profile of the metal element in a metal gate

We propose an *ex situ* method to measure the binding energy profile of the metal element in a metal gate near the metal/dielectric interface using XPS. Although this method is not able to measure the effective work function directly, it can provide us some important information about the effective work function. A gate stack can go through a high temperature anneal and thus might have a very high chemical shift of the metal binding energy near the metal/dielectric interface. For two different gate dielectrics, if the binding energy profiles of the metal gate are almost same, it is proposed that the metal gate should have the same effective work function on the two different gate stacks. Further work is needed to examine this hypothesis.

Appendix: Publications

Journal papers:

[1] **Zhang, M.H.**; Rhee, S.J.; Kang, C.Y.; Choi, C.H.; Akbar, M.S.; Krishnan, S.A.; Lee, T.; Ok, I.J.; Zhu, F.; Kim, H.S.; Lee, Jack C. "Improved electrical and material characteristics of HfTaO gate dielectrics with high crystallization temperature", Appl. Phys. Lett. **87**, 232901 (2005).

[2] **Zhang, M.H.**; Ok, I.J.; Kim, H.S.; Zhu, F.; Lee, T.; Thareja, G.; Yu, L.; Lee, Jack C., "Characteristics of sputtered $Hf_{1-x}Si_xO_2$/Si/GaAs gate stacks", Appl. Phys. Lett. **89**, 042902 (2006).

[3] **M. H. Zhang**, F. Zhu, T. Lee, H. S. Kim, I. J. Ok, G. Thareja, L. Yu, and Jack C. Lee, "Fluorine passivation in poly-Si/TaN/HfO_2 through ion implantation", Appl. Phys. Lett. **89**, 142909 (2006).

[4] **M. H. Zhang**, M. Oye, B. Cobb, F. Zhu, H. S. Kim, I. J. Ok, J. Hurst, S. Lewis, A. Holmes, J. C. Lee, S. Koveshnikov, W. Tsai, M. Yakimov, V. Torkanov, S. Oktyabrsky, "Importance of controlling oxygen incorporation into HfO_2/Si/n-GaAs gate stacks", J. Appl. Phys. **101**, 034103 (2007).

[5] **M. H. Zhang**, F. Zhu, H. S. Kim, I. J. Ok and Jack C. Lee, "Fluorine passivation in gate stacks of poly-Si/TaN/HfO_2 (and HfSiON/HfO_2)/Si through gate ion implantation", IEEE Electron Device Letters*,* **28,** 195 (2007*)*.

[6] **Manhong Zhang**, Feng Zhu, In-Jo Ok, Hyoung- Kim, Han Zhao, Sung-Il Park, Jung-Hwan Yum, and Jack C. Lee, "Mechanism of Flatband voltage shift in SiO_2 and Hf-based gate dielectric stacks by capping Gd_2O_3", mitted to IEEE Electron Device Letters.

Conference papers:

[1] **Manhong Zhang**, F. Zhu, I. J.Ok , H. S. Kim, L.Yu, M. Oye, J.Hurst, B. Cobb, S. Lewis, A. Holmes and Jack C. Lee, Criticality of controlling oxygen incorporation into HfO_2/Si/GaAs gate stacks", Oral presentation on IEEE Semiconductor Interface Specialists Conference 2006, S6.4.

[2] **Manhong Zhang,** Feng Zhu, In-Jo Ok, Hyoung- Kim, Han Zhao, Jack C. Lee "Mechanism of flatband voltage shift in SiO_2 and Hf-based gate dielectric stacks by capping Gd_2O_3", Oral presentation on IEEE Semiconductor Interface Specialists Conference 2007.

[3] **Manhong Zhang,** Feng Zhu, In-Jo Ok, Hyoung- Kim, Han Zhao, Jack C. Lee "Mechanism of flatband voltage shift capping Me_2O_3 (Me=Gd, Y, Dy)", accepted by DRC 2008.

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