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Millimeter-Wave and Sub-Terahertz On-Chip Antennas, Arrays, Propagation, and Radiation Pattern Measurements

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by

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DISSERTATION

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Dedicated to my loving family.

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Millimeter-Wave and Sub-Terahertz On-Chip Antennas, Arrays, Propagation, and Radiation Pattern Measurements

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This dissertation focuses on the development of next generation wireless communications at millimeter-wave and sub-terahertz frequencies. As wireless providers experience a bandwidth shortage and cellular subscribers demand faster data rates and more reliable service, a push towards unused carriers frequencies such as 28 GHz, 60 GHz, and 180 GHz will alleviate network congestion while simultaneously providing massive bandwidths to consumers. This dissertation summarizes research in understanding millimeter-wave wireless propagation, the design and fabrication of millimeter-wave and sub-terahertz on-chip antenna arrays on an integrated circuit semiconductor process, and the accurate measurement of on-chip antenna radiation patterns in a wafer probe station environment.

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Chapter 1

Introduction

Wireless communications is an important area of electrical engineering and a pervasive technology that facilitates our daily lives. Early scientists and inventors such as David Edward Hughes (1831-1900), James Clerk Maxwell (1831-1879), Heinrich Hertz (1857-1894), Nikola Tesla (1856-1943), Guglielmo Marconi (1874-1937) and many others discovered, developed, and commercialized wireless technology in the late 1800s which revolutionized human history. The wireless era is now stronger than ever with billions of wireless devices produced and used each year, and smartphones becoming the primary device to access the Internet and communicate with others. The deployment of wireless technology has been so successful that wireless providers today are saturated with user congestion and need solutions to provide faster and more reliable data rates to consumers. A push towards higher frequencies with larger bandwidths can alleviate this paramount problem.

Concurrently with wireless development over the past 100+ years, the invention of integrated circuits (ICs) in the computing world in 1958 by Jack Kilby (1923-2005) while employed at Texas Instruments has allowed electronics to physically shrink while simultaneoulsy becoming more powerful than

ever before. As predicted by Moore's law, billions of tiny transistors are now produced on a single IC (also known as a "chip") the size of a fingernail which allows sophisticated logic, dense memories, complex computational tasks, and fast multimedia processing in small handheld devices. Each new generation of semiconductor technology reduces transistor size while also increasing the maximum frequency of operation. This unlocks the potential of inexpensive wireless communications at higher carrier frequencies and more information to be sent over-the-air due to larger available bandwidths. Today, CMOS transistors can produce frequencies of several gigahertz (GHz) (billions of voltage oscillations per second) and are being used to create radio frequency integrated circuits (RFICs) to generate, transmit, receive, amplify, and decode wireless signals at multi-GHz frequencies. With semiconductor technology continuing to scale down year-after-year, experimental CMOS transistors are now operating at millimeter-wave (mm-wave), sub-terahertz (sub-THz), and terahertz (THz) (trillions of oscillations per second) frequencies [1][2][3][4]. Wireless engineers, just like computer engineers, must understand IC technology and the concepts and capabilities it offers. Additionally, the high frequency, and thus, small wavelength, allows utilization of small antennas since antenna size is correlated to wavelength (e.g. the free space wavelength at 180 GHz is 1.67 mm). These high frequency antennas are physically small and can be integrated into the IC to create an on-chip antenna, and hence antenna designers also need to be skilled in the art of IC design, production, and testing.

In this new era of mm-wave and sub-THz wireless communications, the

disjoint electrical engineering sub-fields of circuit design, communications, and electromagnetics will merge together to design and create the next generation of wireless devices. The wireless electrical engineer of the future will need to possess interdisciplinary skills as entire systems become lumped together and form a highly integrated system-on-chip. Digital logic ICs will become integrated with analog, RF, and antenna components to create a complete wireless transceiver on a single chip. The push towards higher frequencies allows massive bandwidths, while at the same time shrinking devices, increasing integration capabilities, and reducing device cost.

This dissertation focuses on mm-wave and sub-THz wireless ICs with potential to deliver multi-Gbps data rates using standard, low-cost CMOS technology. Currently, industry is commercializing the unlicensed 60 GHz wireless band (e.g. IEEE 802.11ad/WiGig) for indoor short-range communication networks [1][5]. The atmospheric attenuation property of 60 GHz was one of the driving forces for regulatory agencies such as the U.S. FCC to unlicense multi-GHz of bandwidth at 60 GHz [6]. The 180 GHz band, which possesses the same atmospheric absorption properties as 60 GHz, is predicted to be the next unlicensed band for short-range high data rate communications beyond 60 GHz, and more research is needed at this frequency band such as how to design and measure on-chip antennas. To help understand how to design mm-wave and sub-THz on-chip antennas, a wireless propagation study at 28 GHz was conducted in New York City to predict future cellular communications at millimeter-wave frequencies[7][8][9][10]. This measurement campaign provides

early knowledge about mm-wave propagation for future 5G cellular communications. With this knowledge, mm-wave and sub-THz wireless ICs can be better designed and fabricated for reliable real-world deployment. A sub-THz 45 nm SOI CMOS IC was designed and fabricated with a 2x2 patch antenna array. Designing at high frequencies is a challenge due to higher material losses and parasitics. In addition, an on-chip antenna measurement system was also developed and constructed in a wafer probe station environment to measure the radiation patterns of on-chip antennas. The probe station environment uses a waveguide-fed Ground-Signal-Ground (GSG) RF wafer probe to measure on-chip antennas at mm-wave and sub-THz frequencies such as 140-220 GHz. Performing on-chip antenna testing in a wafer probe station instead of a custom-built chip-only system (commonly seen in literature) is desirable since post-silicon wafer-level testing is conducted in this environment prior to ICs being diced, packaged, and integrated into final products. The cost to debug a flawed chip design grows exponentially the further the "bug" is found in a production line (i.e. it is least expensive to find design flaws early in production rather than later), thus catching "bugs" early is highly desirable. Therefore, from a manufacturing perspective, it is very important and practical to perform on-chip antenna testing in a probe station environment in conjunction with post-silicon wafer-level testing of digital, analog, and RF circuitry. This dissertation demonstrates how to measure on-chip antenna radiation patterns at 180 GHz in a probe station environment and compares the measured patterns with simulations. In addition, environmental studies were performed to

understand the effect of the RF probe, a nearby DC probe, and RF absorbing material on on-chip antenna radiation pattern measurements in a probe station environment.

This dissertation is organized as follows: Chapter 2 provides background information about semiconductor processes and a literature review about state-of-the-art on-chip antennas and antenna measurement systems at mm-wave and sub-THz frequencies. Chapter 3 discusses a 28 GHz wireless propagation measurement campaign conducted in New York City to understand how mm-wave cellular signals will propagate in dense urban environments. Chapter 4 discusses the design and fabrication of the on-chip antenna array at 180 GHz as well as key design considerations when implementing on-chip antennas in CMOS. Chapter 5 describes the construction of the on-chip antenna measurement system in a probe station environment. Chapter 6 presents the measured performance of the sub-THz on-chip antennas as well as the results of the environmental studies in the probe station environment. Chapter 7 will conclude the dissertation highlighting the key contributions of this research and areas of further work.

Chapter 2

Background Information and Literature Review

This chapter contains useful background information about semiconductor processes and a literature review of millimeter-wave and sub-terahertz on-chip antenna designs and on-chip antenna measurement systems.

2.1 Overview of Integrated Circuit Technology

To grasp the complexity of an IC and the various materials used within the chip, Figure 2.1 shows an example cross section of an integrated circuit. The cross section of the IC can be divided into two major sections: the semiconductor substrate and the interconnect. The substrate, also known as the front-end-of-line (FEOL), is where active components such as transistors and diodes are created. They are patterned on the semiconductor through photolithography and connected together using the interconnect. Transistors are created only a few micrometers (μm) deep into the semiconductor; however, for mechanical stability, the substrate thickness can range from 100 to 750 μm depending on manufacturer and post-processing steps such as wafer thinning.

The types of semiconductor substrates can vary, but the most common

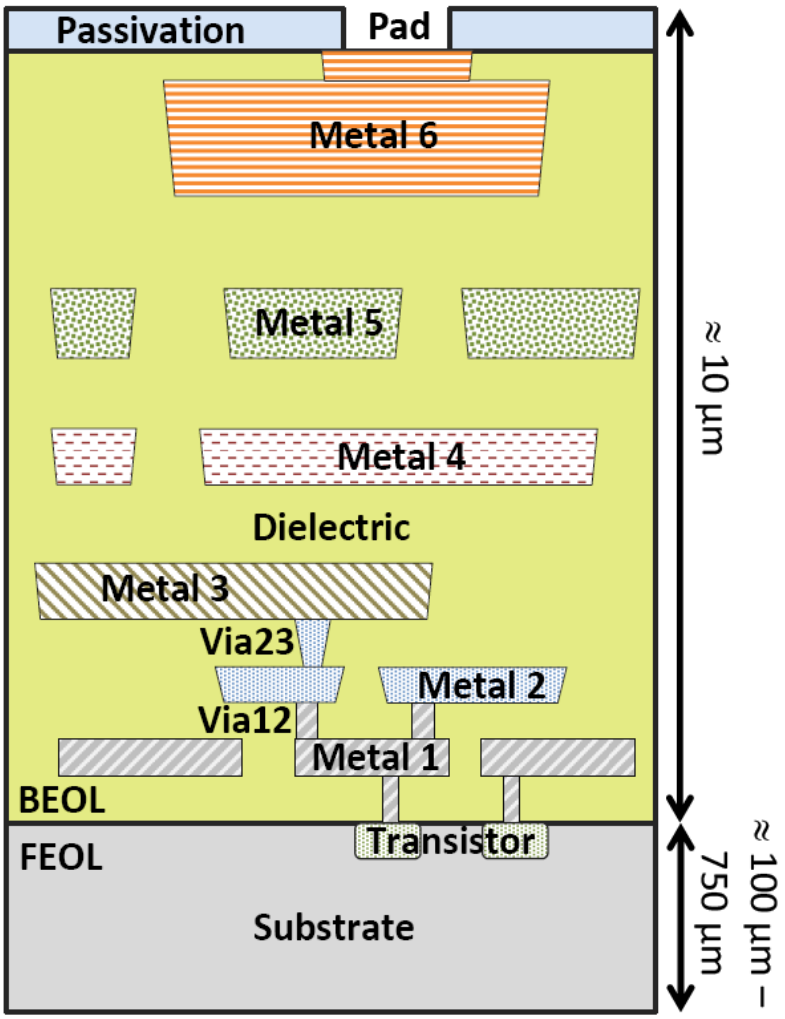

Figure 2.1: Example cross section (side view) of an IC (not to scale). A network of metal layers and interconnecting vias within a dielectric material is designed and fabricated on top of a substrate that contains transistors. In CMOS, the metal layers are typically aluminum or copper, the substrate is doped silicon, and the dielectric is typically silicon dioxide (SiO_2). The passivation layer is a dielectric layer that protects the chip from the environment. To send/receive voltage signals to/from the chip through a bond wire or probe, a pad is created which is a cut in the passivation layer to expose a contact point to the top most metal layer.

and inexpensive is silicon [11]. CMOS fabrication technology uses heavily doped silicon to create a semiconductor and is used in the vast majority of today's digital electronics. Silicon Germanium (SiGe) is a good choice for RF/analog ICs due to higher electron mobility; however, the cost of manufacturing SiGe ICs is much higher compared to CMOS. To have a complete system-on-chip (SoC) containing digital, analog, and RF components integrated on one semiconductor, silicon CMOS is the most cost effective and mass producible choice for fabrication. Each generation of CMOS technology is described as a "technology node" and the semiconductor industry has labeled each technology node using specific values of lengths such as "0.18 μm," "0.13 μm," "90 nm," "65 nm," "45 nm," etc. This length is roughly the minimum length of a transistor that can be fabricated in that technology node. Newer technology nodes have smaller lengths, for example, the newest CMOS technology node is currently 22 nm. In a Silicon-on-Insulator (SOI) CMOS process, a thin layer of dielectric exists within the silicon substrate just below the transistors. This insulator is typically SiO_2 and is mainly used to isolate transistors from each other which helps avoid latchups that cause undesired short circuits within the semiconductor.

The second section that is created above the substrate is the interconnecting layers simply called the "interconnect," metallization, or the back-end-of-line (BEOL). The interconnect contains a highway-like system of metal layers within a dielectric to connect transistors and devices within the substrate. The interconnect is $\approx$10 μm in thickness, but contains many layers of

metal, dielectric, and vias to connect from layer-to-layer. For example, a 0.18 μm CMOS process can have six metal layers within a SiO_2 dielectric with 0.5 μm of spacing between each metal layer. As seen in Figure 2.1, the top metal layers are thicker than the bottom metal layers and the dielectric thickness also increases with higher metal layers. Newer semiconductor processes contain more metal layers and can have multiple dielectrics than previous generations; however, the overall thickness of the BEOL remains the same, thus, metal layers are becoming thinner with each new process. For example, a 45 nm CMOS process can have up to 11 metal layers with 3 different dielectrics, yet still maintains an overall BEOL thickness of 11 μm. Vias are created during fabrication of the IC to tunnel through the dielectric and connect one metal layer to another (ex: Via12, Via23, Via34, etc. as seen in Fig. 2.1). Larger vias are used in higher metal layers compared to lower metal layers. In CMOS, the interconnect is mainly used in digital circuits to provide power and connect transistors that are buried in the semiconductor; however, in RFIC design, the interconnect is also used to create passive components such as capacitors, inductors, or transmission lines. For mm-wave and sub-THz wireless devices, the interconnect is used to create the on-chip antennas.

Accurate knowledge of the interconnect material properties such as the conductivity of the metal, the permittivity of the dielectric, and loss tangents of the dielectric, helps design, simulate, and fabricate precise antennas and transmission lines [12]. Figure 2.2 shows a sample simulation of the impedance match of a transmission line when varying the dielectric relative permittivity

from 3.0 to 5.0 in increments of 0.2. The input impedance of the transmission line changes significantly which causes the center frequency to shift by several GHz. This figure illustrates the importance of accurately knowing material properties in designing transmission lines and antennas especially at mm-wave and sub-THz frequencies; however, often times, the semiconductor foundry may not have material property data at mm-wave and sub-THz frequencies. Test structures are then needed in the IC to measure the material properties at the desired frequency of interest.

The passivation layer is the top most layer that serves as a protection barrier between the chip and external environment. To send and receive signals to and from the chip, the passivation needs to be etched out so that the top most metal (i.e. metal 6 in Figure 2.1) is exposed. The exposed metal is called a "pad" and is typically rectangular to allow a bond wire or probe to physically connect to the chip. When using probes, a DC probe or RF probe can be used to test the chip by sending and receiving signals through the pads. A wafer probe station such as the Cascade Microtech Summit 11101B with RF probes and a Vector Network Analyzer (VNA) such as the Agilent E8361A can be used to directly probe the IC and measure reflected/transmitted energy (i.e. scattering parameters or "S-parameters") of the various test structures on the IC. An example of the wafer probe station and VNA can been seen in Figure 2.3 and the RF wafer probes can be seen in Figure 2.4.

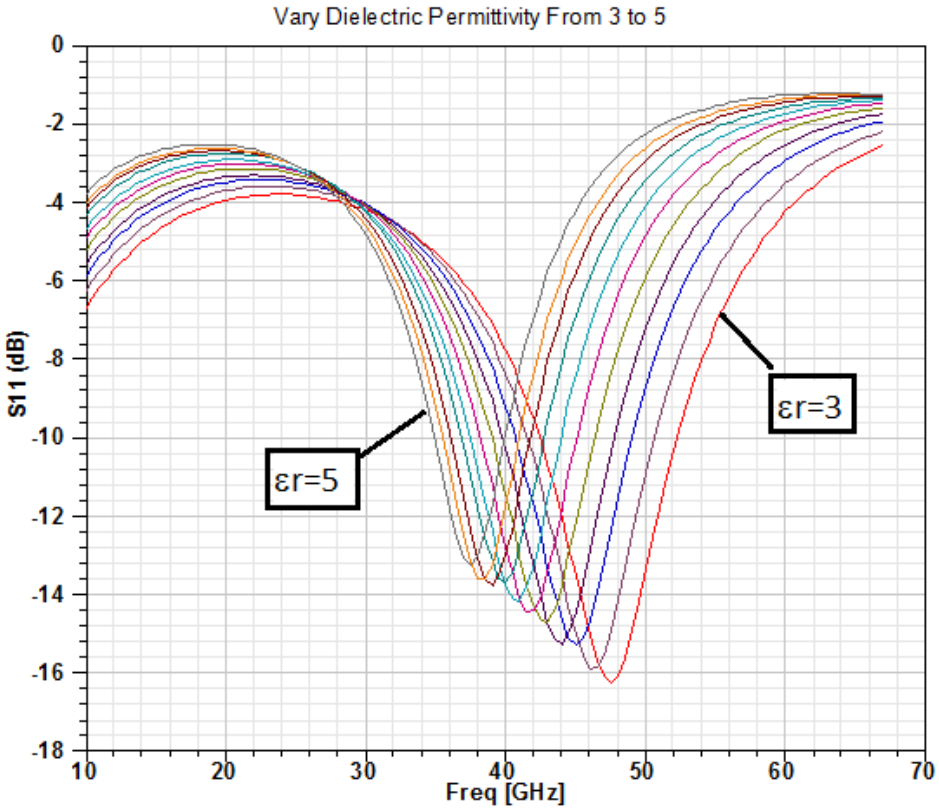

Figure 2.2: Changing the material properties of an IC such as dielectric relative permittivity can create a large effect on IC performance, especially at mm-wave and sub-THz frequencies. These HFSS simulations illustrate how a transmission line's impedance match can shift drastically by slightly adjusting the dielectric relative permittivity from 3.0 to 5.0 with increments of 0.2.

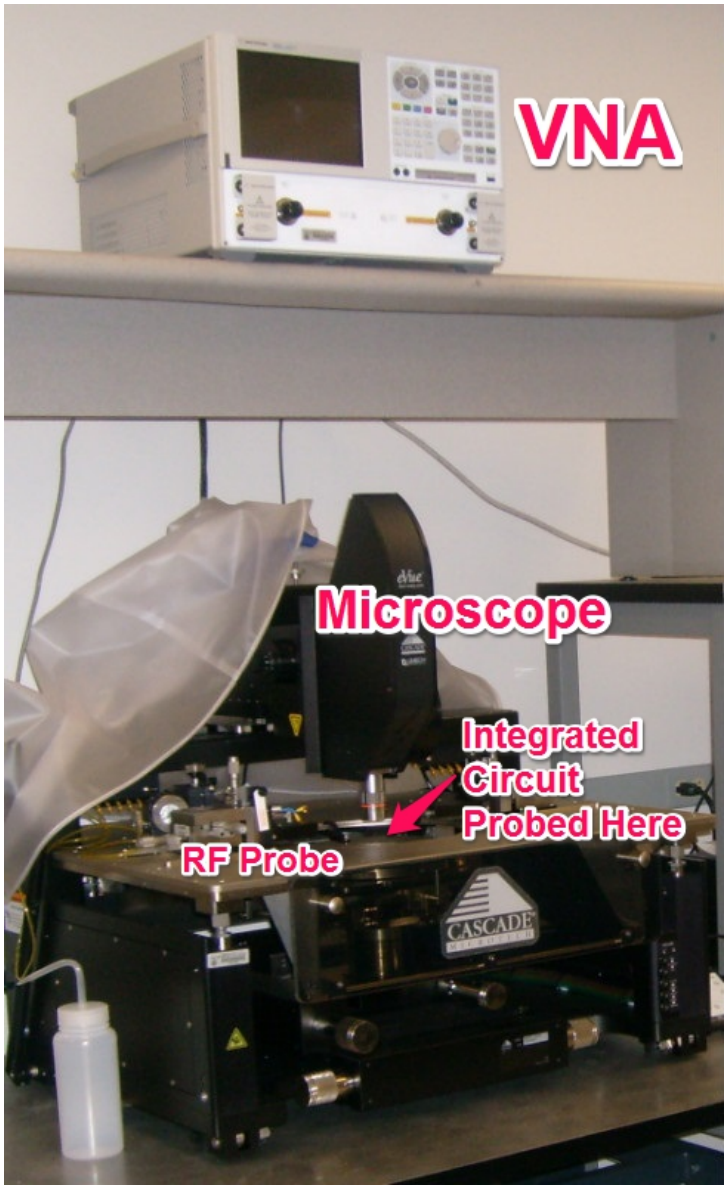

Figure 2.3: A Vector Network Analyzer (VNA) sits above a Cascade Microtech Summit 11101B wafer probing station. This setup allows direct probing of integrated circuits to measure on-chip structures up to millimeter-wave and sub-terahertz frequencies.

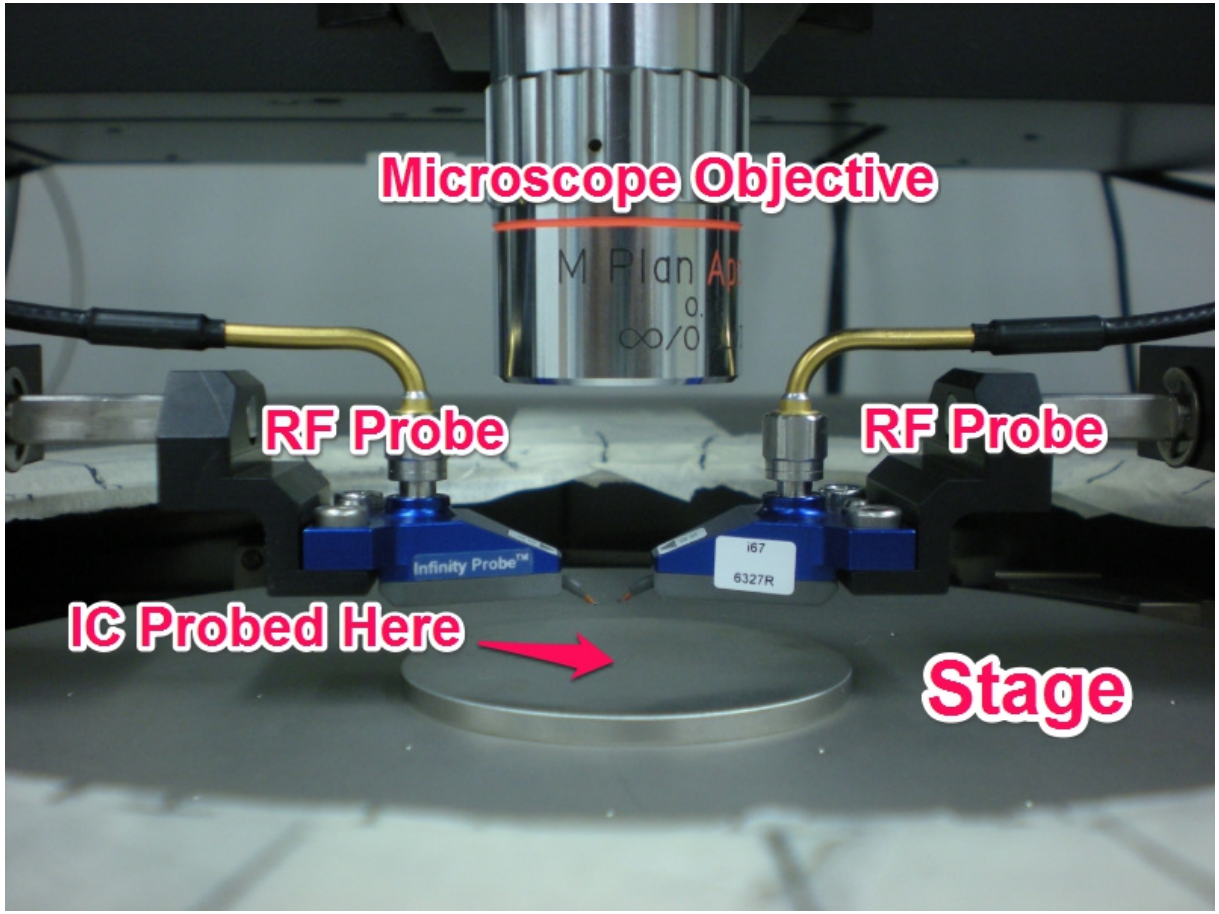

Figure 2.4: A picture of the Cascade Microtech wafer probe station with blue RF probes. A wafer or a single chip is placed in the center of the stage where RF probes can contact the IC probe pads and measure scattering parameters. An overhanging microscope and precision XYZ probe positioners orient the probes to carefully contact the IC.

2.2 Millimeter-wave & Sub-THz On-Chip Antennas and Measurement Systems

This section contains a literature review of state-of-the-art millimeter-wave and sub-terahertz on-chip antennas and on-chip antenna measurement systems. Extensive literature review shows that recently fabricated antennas have been constructed for 60 GHz [1] [13][14][15][16][17][18], 77 GHz [3][19][20], 135 GHz [21], 140 GHz [22], 170 GHz [23], 240 GHz [24], 410 GHz [4], and up to 600 GHz [25] which is a strong indicator of future wireless communications at mm-wave and sub-THz frequencies. These papers use a variety of semiconductor processes such as SiGe and silicon CMOS. Within silicon CMOS, the process technology can range between 0.18 μm to 45 nm technology. Most papers design single on-chip antennas with a few exceptions designing antenna arrays. In many of the papers, however, the on-chip antenna performance such as radiation patterns are simply simulated and never verified through extensive measurements [21][22][4][25], which indicates that mm-wave and sub-THz antenna measurement systems are scarce and still under development. The on-chip antenna pattern measurement systems that do exist are custom-built [26][24][27][28], and rely on an RF probe-based method to measure accurate patterns. The first half of this section will review recent on-chip antennas and antenna arrays fabricated for mm-wave and sub-THz frequencies. The second half of this section will review the on-chip antenna measurement systems.

The idea of integrating small antennas directly into the IC is very attractive and considerably lowers the manufacturing cost. The drawback is the

extremely low radiation efficiency typically less than 10% [16] which many authors attribute to the highly doped and lossy silicon substrate [29]. On-chip antenna design techniques need to be understood to overcome the low radiation efficiency. Researchers have attempted to modify the fabricated ICs using dielectric lenses and cavities as seen in [20][19][3][30][31][21] to help reduce substrate losses and focus antenna beams; however, this potential solution requires specialized post-fabrication techniques which is not feasible for mass production. The dielectric lenses to be created and placed near the antenna as well as etching the substrate to create cavities adds to manufacturing costs and production time. The best option is to design an antenna in standard CMOS without additional post-fabrication modifications.

In 2005, Zhang et al. [16] implemented both inverted-F and quasi-Yagi on-chip antennas on a low resistivity silicon substrate (10 Ωcm) for 60 GHz. These antennas were implemented with a "specialized BEOL technology" to overcome the challenges caused by the substrate. In this fabrication, proton implantation was used to increase the substrate resistivity, reduce substrate losses, and improve radiation efficiency. The Yagi antenna had a maximum gain of -12.5 dBi at 65 GHz, and the inverted-F antenna had a maximum gain of -19 dBi at 61 GHz. The bandwidths of these antennas were 12.5 GHz for the inverted-F antenna, and 9 GHz for the Yagi antenna. The simulated radiation efficiencies for the Yagi and inverted-F antenna were 5.6% and 3.5%, respectively. If developed in conventional CMOS, the simulated radiation efficiencies would be 2% and 1.7%, respectively. The chip area was $\approx 1.1mm^2$.

Only simulated radiation patterns were provided for this on-chip antenna.

Researchers from National Cheng Kung University created an on-chip 3-element Yagi antenna in standard 0.18 μm CMOS technology in 2008 [32]. No radiation measurements were made for the on-chip antenna. Antenna gain was measured to be -10.6 dBi at 60 GHz with a bandwidth of 10 GHz, and a simulated radiation efficiency of 10%. The chip area was $1.05mm^2$. These authors also fabricated a triangular monopole antenna using 0.18 μm CMOS technology [33]. The maximum gain value was measured from S-parameters to be -9.4 dBi at 60 GHz with a bandwidth of 10 GHz. The simulated radiation efficiency was approximately 12%. The chip area was $1.81mm^2$.

In 2009, Wu et al. [17] from the University of Florida at Gainesville, explored the idea of using a bond wire from a CMOS chip to printed circuit board (PCB) as an antenna for 60 GHz. Bond wires connect chips to packages so that signals from a PCB can be sent and received to and from the chip. The bond wire antenna was made of gold and was $\approx$ 720 μm in length and 1 mil in diameter. One drawback to this approach is that manufactured bond wires experience length variation ($\pm 50\mu m$) and the length of the bond wire is 0.144 λ which can lead to impedance mismatches. The author notes that the parasitic capacitance and resistance of the bond pads are critical to determine the impedance match with the antenna. The PCB board material (e.g. FR4) is also a concern for radiation losses. The measured antenna gain is $\approx$ -3 to -4 dBi with a radiation efficiency of 15%. This type of antenna can be used for inter-chip communications up to a 10 cm distance, but would not be

sufficient for large scale distances such as indoor wireless or outdoor cellular communications.

In 2010, Huang and Wentzlof [15] created a 60 GHz on-chip patch antenna on 0.13 μm CMOS technology. This patch antenna was designed with the top four metal layers and allows the bottom metal layers to be used as normal interconnect for digital circuits. The patch antenna centered at 60.51 GHz and had 810 MHz of bandwidth. The peak antenna gain and radiation efficiency were -3.32 dBi and 15.87%, respectively. The researchers developed a metal filling scheme to satisfy the foundry design rules by using an "H-tree" metal filling technique between the patch antenna and ground plane. This metal filling technique had little impact on antenna performance. The on-chip patch antenna had an area of 1220 $\mu m \times$ 1580 μm. No radiation pattern measurements were performed.

Chuang et al. [13] from National Cheng Kung University in Taiwan constructed an on-chip Yagi antenna and bandpass filter on 0.18 μm CMOS technology for 60 GHz. The Yagi antenna contains a driven element, a reflector element, a director element, and a ground plane. The top most metal (metal 6) is used to create the driven element and director element. The antenna and filter had an area of 1.1 $\times$ 1.34 mm^2, a peak antenna gain of -14.1 dBi, a center frequency of 60 GHz, and a bandwidth of 10 GHz. This is one of the first papers to demonstrate on-chip radiation pattern measurements in a probe station environment. A signal generator with an RF probe was used to excite the Yagi antenna while a V-band horn antenna measured the received

power using a spectrum analyzer. Both co-polarized and cross-polarized patterns were measured. The measured radiation patterns agree very well with simulations. Additionally, RF probe tests demonstrate that the RF probe does not interfere with the on-chip radiation pattern measurements since the Yagi antenna radiates 30 dB more power than the RF probe by itself.

Peng et al. [18] from University of Manchester in 2011 presented an on-chip patch antenna at 60 GHz using 0.13 μm CMOS technology. This patch antenna contained an artificial magnetic conductor (AMC) with a uniplanar Compact Photonic Band Gap (UC-PBG) which was fabricated using a single metal layer (i.e. metal 1) to eliminate substrate loss at millimeter-wave frequencies. Without the AMC, the patch antenna had a peak gain of -10 dBi; however, with the AMC, the peak gain was -7.28 dBi at 64 GHz with a bandwidth of 12 GHz from 54 GHz to 66 GHz. The size of the antenna with AMC was $2.1 \times 1.7\ mm^2$. No radiation pattern measurements were performed.

In 2012, Hirano et al. [14] from Tokyo Institute of Technology fabricated an on-chip patch antenna for 60 GHz in 0.18 μm CMOS technology. The patch antenna used the top metal layer to construct the patch and the lowest metal layer (i.e. metal 1) to construct the ground plane. The height of the patch was 5 μm above the ground plane. The antenna had a center frequency of 62.5 GHz and a bandwidth of $\approx$ 1 GHz. The peak antenna gain was -14.5 dBi and radiation efficiency was 1%. The patch size was $1.15 \times 1.15\ mm^2$. Only simulated radiation patterns were provided.

The problem of low radiation efficiency is common when studying millimeter-

wave on-chip antennas on CMOS. In the following 77 GHz papers, researchers attempt to mitigate the substrate losses using dielectric lenses; however, the drawbacks of using this technique is the need for custom modifications which increases device cost and production time. For example, Babakhani et al. [3][19] in 2006 constructed an array of four 77 GHz on-chip dipole antennas on a 130 nm IBM SiGe BiCMOS process. Using dipole antennas, 95% of radiated energy was lost through substrate coupling; however, the authors created a specialized hemispherical dielectric lens with similar dielectric permittivity to the silicon substrate to channel energy from surface modes into useful radiation. This lens was attached to the backside of the chip. The lens provided at least 10 dB of antenna gain at 77 GHz and the peak measured antenna gain for the array was +2 dBi. Each dipole antenna had an area of 0.02 mm^2. Unfortunately, this design has many drawbacks including many post-fabrication modifications such as creating electrically-large dielectric lenses, wafer thinning, and placing slabs of undoped silicon to form a uniform dielectric constant.

Nagasaku et al. [20] created a 77 GHz radar sensor using Gallium Arsenide (GaAs) p-HEMT technology with an on-chip patch antenna. A dielectric dome-shaped resin lens was placed exterior to the chip package and boosted transmit power by 11 dB. The antenna with dielectric lens had a 3 dB beamwidth of 40°. The package consumed an area of 6.5 $mm\times$ 6 mm. Measured radiation patterns were provided but no information about the radiation measurement system is provided. No information was provided about

the antenna gain, radiation efficiency, bandwidth, nor antenna size.

Wenig and Weigel [30], created a 77 GHz frequency modulation continuous-wave (FMCW) radar front end and used a linear array of patch-subarrays to feed a cylindrical lens. The lens increased antenna gains by 9 dB. As noted by Cheng et al. [31], FMCW radar is usually employed in vehicular radar since target distance is found by "counting the difference frequency between transmitting signal and its echo." In Cheng [31], a lens antenna is fed by a horn antenna located at the lens focal point. The horn antenna is fed by a microstrip patch antenna. The peak antenna gain of the entire system was 28.5 dBi with a half-power beam width of about 2.5°.

More specialized techniques have been used to try to improve antenna gains and radiation efficiencies, but like dielectric lenses, these techniques are custom post-fabrication modifications which add to device cost and production time. For example, by suspending the antenna in air over a high dielectric constant substrate, Lee et al. [34] created a 77 GHz CPW-fed patch antenna with a simulated radiation efficiency of 94%. The antenna was mechanically supported by posts and hovered 200 μm above the substrate surface. The area of the patch was $1.7mm \times 1.7mm$ and had a 9 GHz bandwidth. Antenna gain was +9 dBi. Gardner et al. [35] used a custom-built air-spaced wideband microstrip antenna array with a gain of 15.5 dBi and a 25% bandwidth.

Both Montusclat et al. [36] and Morschbach et al. [37] investigated how integrated antennas behave on a non-standard less lossy substrate, HR (High Resistivity) silicon. HR silicon is ion-implanted to reduce substrate

conductivity and reduce energy loss. Montusclat used a 500 μm substrate thickness and constructed a half-wave dipole antenna to operate at 40 GHz. The antenna gain was -2 dBi, 6 dB better than the same antenna in standard bulk substrate. Morschbach created two separate antenna array designs at 80 GHz operation on HR SOI. One design consisted of a 1-D series fed antenna with 10 elements, and the 2nd design was a 2-D array of patch antennas. The 1-D antenna had 6.2 dBi gain with a simulated radiation efficiency of 22.93%. The 2-D design had 10 dBi gain with a simulated radiation efficiency of 53.9%. Ion implantation is much more costly compared to standard CMOS, thus other solutions are needed to overcome low radiation efficiency.

Several researchers have pushed beyond 60 GHz and 77 GHz and are designing in the sub-THz region. For example, in 2011, Pan et al. [22] from the University of California at Irvine designed and simulated four on-chip antennas at 90 GHz and 140 GHz. All on-chip antennas were simulated. One on-chip antenna was a bowtie-shaped slot antenna with a simulated antenna gain of -1.5 dBi at 90 GHz and a bandwidth of 30 GHz. A cavity-backed slot antenna had a simulated antenna gain of -2 dBi at 140 GHz with 5 GHz of bandwidth. A waveguide-slot antenna had a simulated antenna gain of -1 dBi at 140 GHz with a bandwidth of 3 GHz. Lastly, an on-chip patch antenna had a simulated peak gain of -2 dBi with 10 GHz of bandwidth. No radiation pattern measurements were performed.

In 2008, Laskin et al. [23] from the University of Toronto created a 170 GHz transceiver on a SiGe HBT process. Three on-chip antenna designs at 170

GHz were discussed for integration with a 0.13 μm CMOS process including a patch antenna, a tapered dipole, and a metal-filled dipole. The authors note that the patch antenna was simulated to have -8 dBi antenna gain with a size of $475\mu m \times 450\mu m$. The authors state that the patch antenna and tapered dipole do not satisfy the metal density rules of the 130-nm SiGe BiCMOS process and can not be fabricated. To compensate, the authors add a metal-fill pattern below the tapered dipole to create the metal-filled dipole which satisfies the design rules and helps reduce antenna size. The tapered dipole had dimensions of $262\mu m \times 225\mu m$ and the metal-filled dipole had dimensions of $124\mu m \times 123\mu m$. The measured antenna gains for all three antennas were below -25 dBi. The metal-filled dipole antenna had about 8 dB more gain than the patch antenna. No results were provided regarding bandwidth nor radiation efficiency.

In 2013, H. Gulan et al. [24] from the Karlsruhe Institute of Technology and Fraunhofer Institute for Applied Solid State Physics in Germany created a 240 GHz patch antenna array on GaAs. They also created a custom-built on-chip antenna radiation pattern measurement system from 220 GHz to 325 GHz. The patch antenna array was a 2x2 grid with a corporate feed network connected to a Cascade Microtech GSG RF probe. In this GaAs process, the bottom of the substrate was metallized, thus the 50 μm thick GaAs substrate forms the dielectric of the patch antenna. The elements were separated by half wavelength in free space and the feed network uses quarter-wavelength transformers to impedance match to a 50 Ω microstrip transmission line. The

array had a center frequency of 240 GHz with 6 GHz of bandwidth. The measured antenna gain was +9 dBi and agrees very well with simulations. The radiation patterns were measured and also agree very well with simulation. The array size was 700 $\mu m \times$ 700 μm.

In 2013, Bredendiek et al. [38] produced a 240 GHz radar transceiver with integrated patch antennas on a SiGe HBT process. Two patch antennas were fabricated for transmitting and receiving. The on-chip antennas were differentially fed and the simulated antenna gain was +2 dBi. The authors estimate 5 dB of radiation losses. The antenna size was 326 $\mu m \times$ 326 μm. No details were reported for the antenna's construction, bandwidth, radiation efficiency, or radiation pattern.

In 2008 and 2010, Seok et al. [4][25] produced on-chip terahertz oscillators with on-chip patch antennas at 410 GHz and 589 GHz. In [4], the patch antenna had a center frequency of 390 GHz and was constructed on a 6-metal 45 nm CMOS process. In [25], the patch antenna had a center frequency of 600 GHz and was constructed on a 0.12 μm SiGe BiCMOS process. The patch antennas were created since commercially available RF probes at these frequencies were not available to directly measure the output of the oscillators. In [4], the patch was made using the top most metal layer while the ground plane was constructed using metal 1 to metal 5 with interconnecting vias. Slots were added to the patch antenna and ground plane to satisfy design rules. The patch size was 200 $\mu m \times$ 200 μm with a 4 μm spacing between the patch and ground. The simulated directivity of the patch antenna was 5

and had a radiation efficiency of 22% (i.e. the antenna gain was 0.4 dBi). In [25], the patch was also constructed using the thick top metal layer and the ground plane was made using multiple metal layers with interconnected vias. The patch size was 240 $\mu m \times$ 240 μm with a 4 μm spacing between the patch and ground. Slots were also added to this patch antenna and ground plane to satisfy design rules. The patch antenna had two resonances at 300 GHz and 600 GHz. At 300 GHz, the input impedance of the antenna was 8 Ω and the simulated antenna gain was +0.8 dBi with a radiation efficiency of 26%. At 600 GHz, the input impedance of the antenna was 26 Ω and the simulated antenna gain was +1.7 dBi with a radiation efficiency of 42%. In both these papers, only simulated radiation patterns were provided.

Several researchers have been attempting to build accurate mm-wave and sub-THz on-chip antenna radiation pattern measurement systems. Most of these researchers use a custom-built apparatus to probe the on-chip antenna and measure the received power by sweeping a receiver antenna across a measurement sphere. One drawback of creating such a system is its uniqueness. From a IC production standpoint, building an antenna measurement system within standard semiconductor test equipment, such as a wafer probe station, is highly desirable than creating a custom-built one-of-a-kind single-chip antenna measurement system. If mm-wave and sub-THz RFICs with on-chip antennas are predicted to be in high demand just like 3G/4G cellular chips today, an antenna measurement system must be compatible and easily integrated with normal IC testing equipment and procedures at the foundry.

Below are examples of the state-of-the-art on-chip antenna radiation pattern measurement systems.

Simon's [39] early work in 2002 built one of the first radiation pattern measurement systems for on-wafer reconfigurable patch antennas. A probe station was modified in this setup and an open-ended waveguide was used as a reference antenna and rotated around the antenna under test (AUT) using a Plexiglass arm and stepper motor. However, the drawback of this system is only the ability to measure a single "cut" of radiation. Additionally, Simons states that reflection of signals from probe station positioners and other metallic object is "one of the major sources of error" as well as misalignment of antennas.

In 2004, Zwick et al. [40] from IBM developed an antenna measurement system to measure mm-wave SiGe ICs up to 60 GHz. The system used a VNA with ports connected to the AUT and a WR-15 horn antenna. The AUT was placed within an anechoic chamber on a custom sample holder and probed with an RF probe. The WR-15 standard gain horn antenna was mounted on a rotational arm at a distance of 38 cm from the AUT to ensure a far field condition from the AUT. Three orthogonal radiation pattern cuts can be measured with this system, and a 90° twist waveguide can be added to test co-polarized and cross-polarized radiation. A Vivaldi antenna was created to test this antenna measurement system and the measured radiation patterns were in agreement with simulations. The RF probe was also measured by itself without an AUT, and the worst case gain of the RF probe was -15.5 dBi which

sets the baseline system sensitivity. This coincides with [41] which simulated a GSG RF probe of -12 dBi antenna gain when probing a 50 Ω non-radiating load.

In 2009, Pilard et al. [42] from STMicroelectronics constructed a 60 GHz on-chip antenna measurement system for silicon ICs (CMOS, BiCMOS, SiGe, SOI, etc.). The custom-built system does not use any metallic materials in order to minimize reflections. The AUT is placed on a rotational custom-built chuck made of Rexolite and is probed using a Cascade Microtech GSG RF probe. A horn antenna moves along a Rexolite arch and records measurements from the AUT as it sweeps across the arch (i.e. an elevation cut). This measured elevation pattern cut can be repeated for any rotational angle on the chuck (i.e. the azimuth angle). The measurement system uses an Agilent VNA to measure S_{21} measurements between the horn and the on-chip antenna, and radiation patterns can be calculated by removing the free space path loss and the horn antenna gain. An SOLT (Short-Open-Load-Thru) calibration removes any cables losses/mismatches and moves the measurement plane of the VNA to the ends of the coaxial cables. The horn can also be rotated 90° which allows both co-polarized and cross-polarized antenna radiation measurements. The entire system is within an anechoic chamber lined with RF absorbing material. Two on-chip antennas were measured with this system: a dipole antenna and a folded-slot antenna. The dipole was fabricated on standard low-resistivity silicon and had a center frequency of 40 GHz, $\approx$ 10 GHz of bandwidth, and an input impedance of 46-j2 Ω. The dipole antenna had an

antenna gain of -11.9 dBi. The folded-slot antenna was fabricated on a high-resistivity silicon-on-insulator (SOI) process and had a center frequency of 58.2 GHz, $\approx$ 10 GHz of bandwidth, and an input impedance of 49-j2 Ω. The folded-slot had an antenna gain of -0.4 dBi. The radiation patterns of both antennas were measured in both E-plane and H-plane. The researchers did a similar experiment to Zwick [40] to study the probe radiation when contacting a 50 Ω non-radiating load, and found a probe radiation of -16.3 dBi at 60 GHz which sets the minimum sensitivity level of the measurement system.

In 2009, Ranvier [43] (and carried forward in 2011 and 2012 through Titz et al.[44][45][27][46][47]) built a nearly 3-D measurement system for 60 GHz antennas. Two stepper motors were used to move two arms with a receiver horn antenna and provide nearly full 360° spherical coverage. A mixer was mounted on the arm and down-converted the received RF signal from the horn antenna to IF which was fed to a spectrum analyzer. This system used a 60 GHz Picoprobe GSG RF probe to probe and excite the 60 GHz on-chip antenna. LabVIEW by National Instruments was used to automate the data acquisition and mechanical arm movement. The horn antenna could also be rotated 90° to measure co-polarization and cross-polarization patterns. No metallic parts were used in this system and the on-chip antenna is probed on a foam holder to allow pattern measurements underneath the chip. A study of the probe radiation was also investigated just like [42] with the probe contacting a 50 Ω non-radiating load. The RF probe had a measured average gain of -28 dBi with a maximum peak of -22 dBi which sets the sensitivity

of the measurement system. Results also showed a connector vs. probe fed on-chip antenna produces significant measurement differences. The probe-fed method is preferred since connector-fed methods create "additional resonances in return loss" and "create strong sidelobes." A 60 GHz planar omni-directional antenna was used to test the antenna radiation measurement system as well as a circularly polarized 60 GHz patch antenna. This system had an accuracy of $\pm$ 0.8 dB and the measured radiation pattern agreed with the simulated pattern. The authors are currently upgrading the system for 140 GHz.

Ito et al. [26], in 2009, built a system based on a waveguide arm rotating around a probed AUT. This system measures up to three radiation pattern cuts from a GSGSG Cascade Microtech probe-fed on-chip antenna using a mechanical adjustment of the waveguide arm. Absorbing material was placed on possible scatterers in the anechoic chamber and uses a removable microscope that slides through an opening in the chamber to verify accurate probing of the antenna. This system used a spectrum analyzer which limited dynamic range to 20 dB; however, there was good agreement between measured and simulated antenna patterns. The authors verified their system by probing a 60 GHz PCB dipole antenna.

One on-chip antenna measurement system by [13] performed the radiation pattern measurements in a wafer probe station environment. A 67 GHz signal generator was connected to the on-chip antenna using a GSG RF probe operating up to 67 GHz. The on-chip antenna transmitted a carrier wave while a receiver horn antenna rotated across the probe station to perform a

planar radiation pattern cut. The horn antenna was connected to a 50-75 GHz harmonic mixer to downconvert the received signal to an IF frequency which is fed to a spectrum analyzer. The receiver horn antenna could be rotated 90° to measure co-polarization and cross-polarization radiation patterns. To test their measurement system, the authors measured a 60 GHz CPW-fed Yagi antenna fabricated on a 180 nm CMOS process. Their antenna pattern measurements were in agreement with the HFSS simulation results.

In 2011, Fu et al. [48] investigated the feeding techniques of measuring radiation patterns from on-chip antennas. Three RF probes were investigated: a standard Cascade Microtech GSG RF probe, a custom-built extended version of the GSG RF probe in which the probe tips were extended by 50 mm, and a custom-built probe with the 50 mm extension as well as a reverse connector. The main advantage of the custom-built 50 mm extended probes is being able to measure more angles that were not blocked by the probe body. There is also slightly less ripple in the measured S_{21} when using the extension probes. This is most likely due to less reflections and scattering off the RF probe body and positioner since multipath reflections can cause rippling in S_{21} measurements. The extension probes do provide some improvement in accuracy ($\approx$ 1-2 dB) compared to the standard probe; however, all three probes had good agreement between measured and simulated radiation patterns.

In 2013, Tsai et al. [49] created an antenna measurement system up to 75 GHz within a probe station environment. As stated in the introduction, these authors agree that the majority of on-chip antenna measurement sys-

tems are custom-built with specialized chip holders which requires additional costs to standard IC measurement facilities. Additionally, if producing on-chip antennas on a massive scale, measurement times of hours per chip [27] is infeasible. It is far more desirable to build an antenna measurement system around a standard IC probe station especially for mass-produced foundries where IC testing is rapid and automated. In [49], the on-chip antenna measurement system uses a VNA to measure S_{21} and determine the radiation pattern of the on-chip antenna. A conical horn antenna is fed with a series of rigid waveguides from a VNA V-Band extension module, and is used to receive the transmitted signal from the on-chip antenna. The on-chip antenna is probed using an RF wafer probe connected to the other V-Band extension module. The horn uses a 2-axis planar positioner to precisely move and measure the on-chip radiation pattern over an XY-planar grid located 4 cm above the AUT. RF absorbing material is used extensively throughout the probe station environment to reduce any multipath reflections which can distort radiation pattern measurements. The authors label this system as "near-field," however, the authors incorrectly determine this using the far-field distance of the horn antenna rather than the AUT [50]. If using small on-chip antennas of several millimeters in diameter as the AUT, the far-field distance of the AUT might be only a few millimeters which would designate this system as a far-field antenna measurement system (more details can be found in [50] and is discussed in Chapter 5). To verify their system and the near-field-to-far-field mathematical transformation, the authors use a large horn antenna as

the AUT which indeed does make this a near-field measurement when using a large antenna as an AUT as discussed in the near-field measurement systems in [51][52]. The measured and simulated radiation patterns agree very well for this on-chip antenna radiation measurement system in a probe station environment.

In 2010, Beer [28] presented a nearly 3-D probe-based on-chip antenna radiation pattern measurement system with a capability to measure up to 110 GHz. The authors used a VNA and custom-built wafer chuck to probe the on-chip antenna while a bent waveguide with a horn antenna is used to measure the 3D pattern and provide proper calibration. The author used stepper motors and a 2-arm system to mechanically move the receiving horn antenna. Measurements could be performed in both V-Band (50-75 GHz) and W-Band (75-110 GHz) by changing harmonic mixers. A movable and removable microscope allowed the user to precisely probe the on-chip antennas. A VNA-based solution rather than a spectrum analyzer increased the dynamic range and allowed simultaneous measurements of "return loss, a proper gain calibration, and gating in the time domain." Accurate E-plane and H-plane antenna pattern measurements were acquired from a Vivaldi antenna at 77 GHz. The authors state that reflections from the metallic probe were hard to suppress and could be responsible for the small differences between measured and simulated results.

The work by Gulan et al. [24] in 2013 used a custom-built RF probe-based measurement setup on a specialized wafer chuck to characterize antennas

from 220 GHz to 325 GHz. The authors used an Agilent PNA-X, OML T/R frequency converters, and a Cascade Microtech waveguide-fed GSG RF probe to excite the on-chip antenna array while a horn antenna and a harmonic mixer downconverted the received signal back to the VNA. The measurement system used a small removable microscope to ensure proper probing. The horn was attached and rotated around the AUT with two rotary stages. Minimal RF absorbing material is seen in the pictures of measurement system. The authors constructed a 240 GHz 2x2 patch antenna array on a GaAs substrate to verify the measurement system. The measured radiation patterns of the on-chip antenna were in agreement with the simulated patterns.

From this literature review, the main challenge with developing on-chip antennas at mm-wave and sub-THz frequencies is the poor radiation efficiency. Antenna and circuit designers must develop creative yet simple solutions to increase radiation efficiency while still adhering to the foundry design rules. Additionally, rapid and reliable methods to measure the performance of on-chip antennas is challenging, but are needed and should be compatible with existing IC fabrication equipment such as a wafer probe station. Most on-chip antenna measurement systems seen in literature are custom-built systems and only have the capability of testing one chip at a time. An ideal measurement system should test an entire wafer of on-chip antennas concurrently with any DC, analog, and RF testing early in the IC fabrication cycle. As seen in literature, a standard RF probe can radiate small amounts of RF energy around -23 dBi to -15 dBi, but this radiation has not interfered with measuring accurate

on-chip antenna radiation patterns. Most antenna measurement systems can only test chips up to 75 GHz with the exception of [28] at 110 GHz and [24] at 220-325 GHz. No measurement system has been presented yet to measure at the sub-THz frequencies around 180 GHz. In this dissertation, a measurement system similar to [13] and [49] is constructed to measure 140 GHz to 220 GHz on-chip antenna patterns in a wafer probe station environment. Additionally, a sub-THz antenna array similar to [24] has been constructed on 45 nm CMOS technology to verify the antenna measurement system and demonstrate how to design a sub-THz on-chip antenna. Most literature uses expensive fabrication technologies such as GaAs and SiGe to implement mm-wave and sub-THz on-chip antennas instead of CMOS. To the author's knowledge, these are the first CMOS 180 GHz on-chip antenna pattern measurements that use a standard wafer probe station.

Chapter 3

Millimeter-wave Outdoor Propagation in Urban Environments

To design mm-wave and sub-THz wireless ICs, the wireless channel in which the devices will operate must first be understood. This chapter discusses a 28 GHz wireless propagation study in the dense urban environment of New York City. The results of this measurement campaign provide new knowledge about millimeter-wave propagation for future cellular communications.

3.1 28 GHz Channel Sounder Hardware

A 28 GHz channel sounder with an RF bandwidth of 800 MHz was used to measure propagation statistics in the dense urban environment of New York City. The hardware and measurement campaign are similar to a 38 GHz propagation campaign in Austin, Texas [53][54][55]. The channel sounder uses a spread spectrum sliding correlator technique to measure and resolve multipath as small as 2.3 ns. Figure 3.1 shows a block diagram of the channel sounder which uses a pseudo-random noise generator (PN generator) clocked at 400 MHz to produce a spread spectrum baseband signal. This PN sequence is then upconverted to an intermediate frequency (IF) of 5.4 GHz

and then upconverted again to an RF carrier frequency of 28 GHz using a local oscillator (LO) signal of 22.6 GHz. The transmit power is +30 dBm prior to being connected to the transmitter (TX) antenna. The RF signal is sent over the wireless channel to the receiver (RX). The TX and RX use identical horn antennas each with 24.5 dBi antenna gain and 10° half-power beamwidth. The received signal at the RX is downconverted from 28 GHz to the IF of 5.4 GHz, filtered and amplified, and then downconverted from IF to baseband where it is then correlated with the transmitted PN sequence. The output of the sliding correlator produces a power delay profile (PDP) which is the received multipath signal versus excess delay (i.e. the channel impulse response of the propagation environment). This waveform is digitized using a National Instruments USB-5133 digitizer and saved to a laptop for post-processing. Figure 3.2 shows a picture of the channel sounder in the field. The channel sounder is capable of measuring path loss up to 168 dB using the 24.5 dBi horn antennas. The electric field that is sent from the TX and being received by the RX is vertically polarized. Waveguides that twist 90° can be inserted to create horizontal polarization if needed. The transmitter and receiver are mounted on rotational motors to precisely position the antennas at specific azimuth and elevation angles. The receiver is also mounted on a linear motor which allowed local area small-scale measurements of $\lambda/2 = 5.35$ mm at 28 GHz. The motors and data acquisition are controlled by a laptop running a LabVIEW program. A sample screenshot of the program can be seen in Figure 3.3 which shows a sample received multipath signal. The data

is written to the laptop hard disk in CSV format (i.e time (ns), voltage (V)) to be post-processed into mathematical channel models.

3.2 Environment and Test Procedure for Measuring Millimeter-wave Propagation

Midtown Manhattan on the New York University campus was chosen to conduct the measurements which includes parks, high-rise commercial buildings, and dense vehicular and pedestrian traffic. The transmitter is setup at three different rooftop locations labeled as TX-COL1, TX-COL2, and TX-KAU as seen in Figure 3.4. TX-COL1 and TX-COL2 are on the rooftop of a 1-story building located 7 meters above ground. TX-KAU is located on a 5-story balcony located 17 meters above ground. 25 RX sites are pseudo-randomly chosen around the university area based upon AC power availability such as sidewalks, plazas, and other pedestrian areas. All three TX sites try to connect to the 25 RX sites creating up to 75 TX-RX unique measurement pairs. Not all TX-RX combinations can create a link. Most TX-RX combinations are Non-Line-Of-Sight (NLOS) with an obstruction between TX and RX. The RXs are chosen across several city blocks in a 400 m x 400 m area.

At each TX-RX combination, the RX horn antenna rotates in the azimuth direction (i.e. a sweep along the horizon) in 10° angular steps (i.e. the half-power beamwidth of the horn antenna) while the TX maintains a fixed position. Thus, up to 36 PDPs could be measured per azimuth angular sweep at the RX. Note that not all RX azimuth angles can acquire a signal. For each

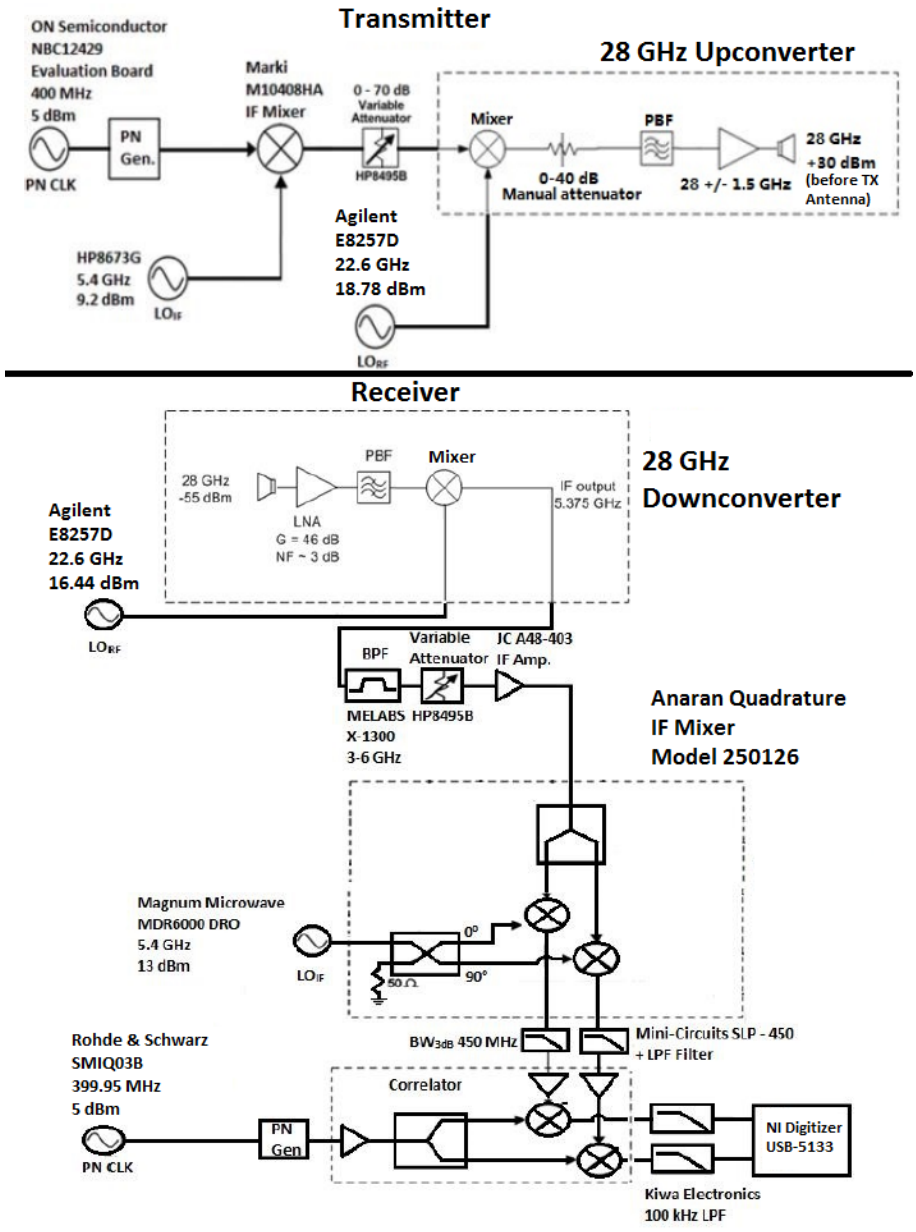

Figure 3.1: Block diagram of the 28 GHz channel sounder to measure millimeter-wave cellular signals. The system uses a spread spectrum sliding correlator technique to measure multipath in a wireless channel. The system can resolve multipath as small as 2.3 ns and measure path loss up to 168 dB.

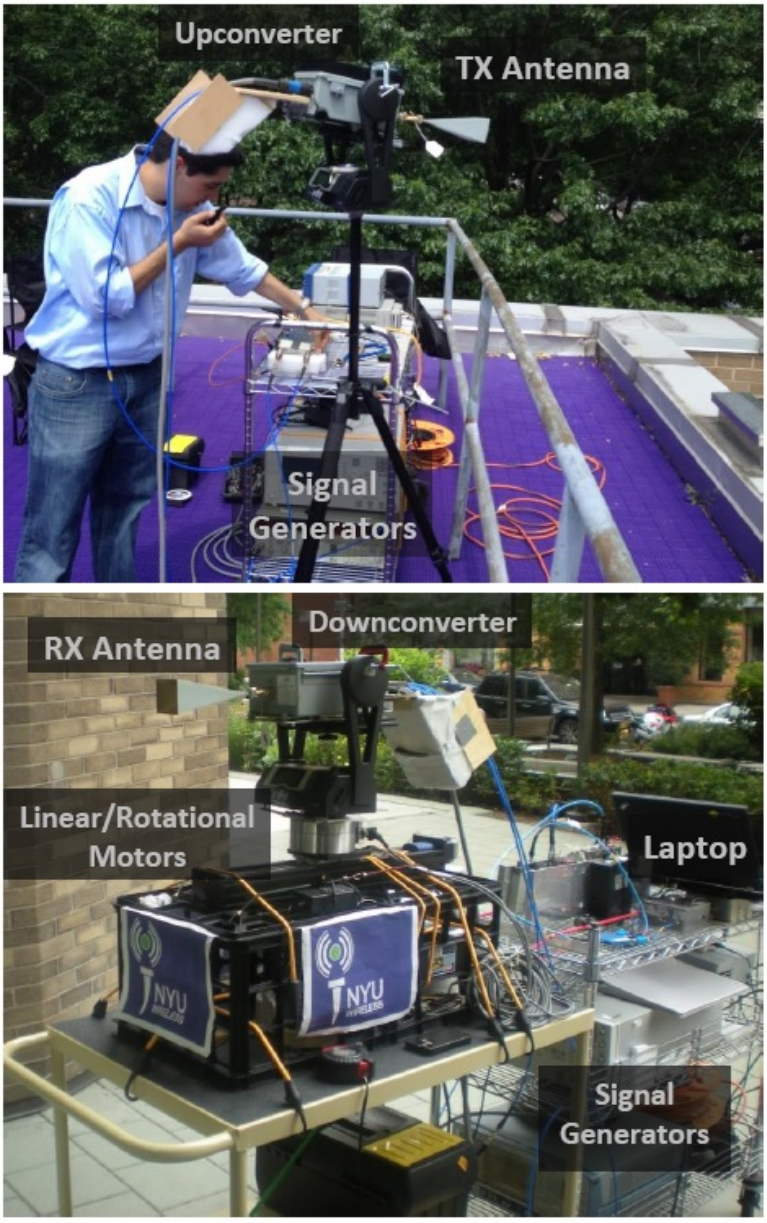

Figure 3.2: The 28 GHz channel sounder deployed in New York City to measure multipath in a dense urban environment. The transmitter (top picture) broadcasts a wideband signal from rooftops while the receiver (bottom picture) receives the impulse response from the wireless channel.

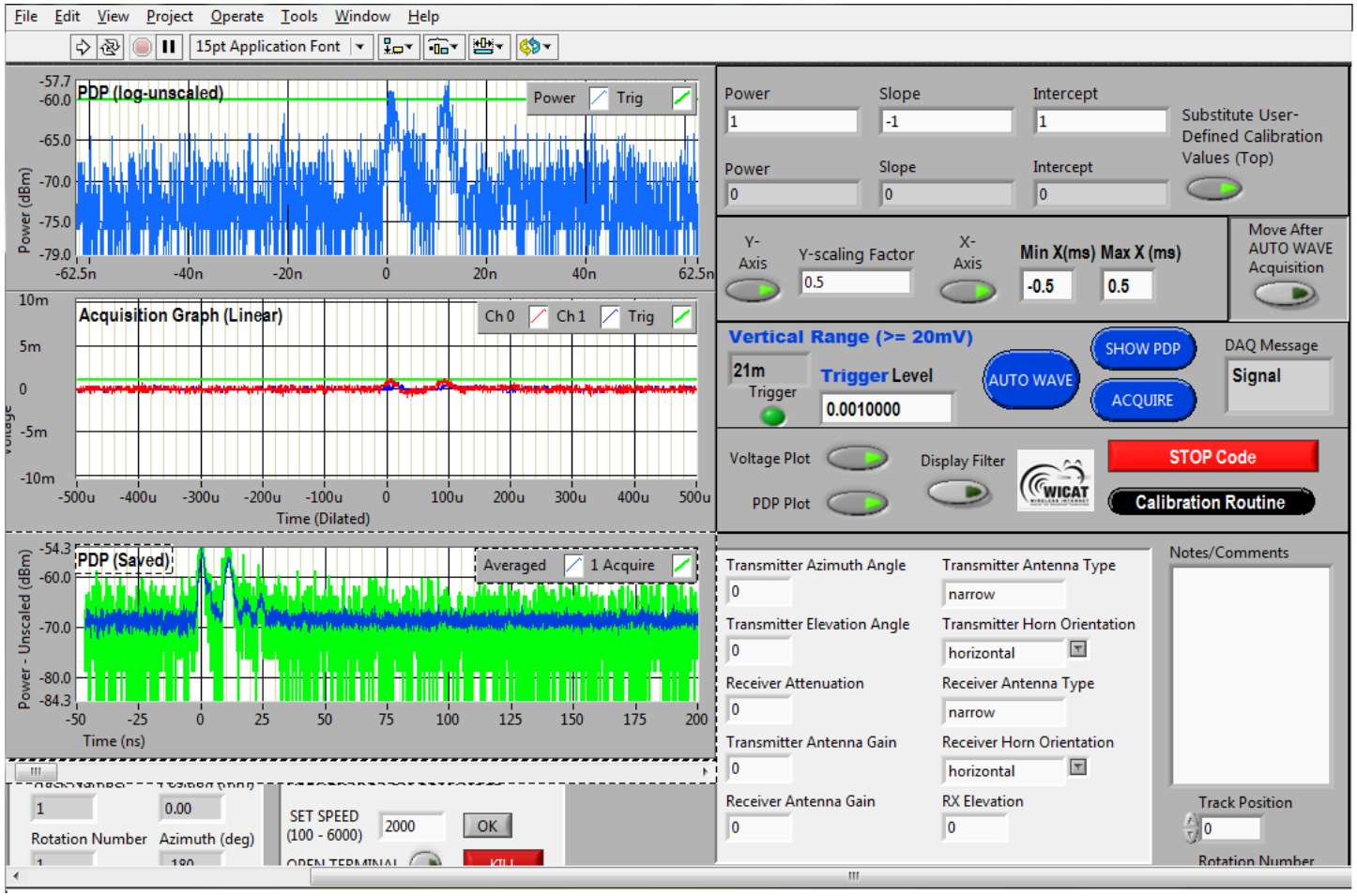

Figure 3.3: A screenshot of the channel sounder laptop running the LabVIEW program by National Instruments. This program manages the data acquisition and controls the rotational and linear motors that accurately position the channel sounder antennas.

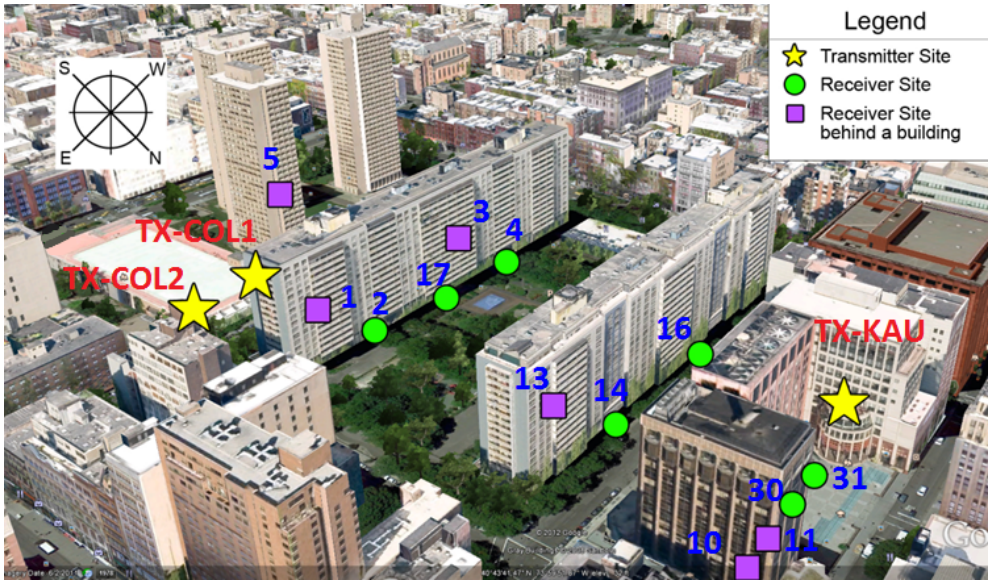

Figure 3.4: The channel sounder TX and RX locations in midtown Manhattan. There are 3 TX locations (TX-COL1, TX-COL2, and TX-KAU) located on rooftops and balconies, and 25 RX locations (not all shown above) scattered across the New York University campus. Most TX-RX combination pairs are Non-Line-Of-Sight. RX 30 and 31 are Line-Of-Sight single measurements to TX-KAU for verification of free space path loss.

RX azimuth angular sweep, the RX is positioned at three different elevation angles: (-20° (i.e. towards the ground), 0° (i.e. towards the horizon), and +20° (i.e. towards the sky)). Additionally, for each RX elevation angle, the TX also is positioned at three different azimuth angles: (-5° (i.e. towards the left), 0°, and +5° (i.e. towards the right)). The 0° TX azimuth direction is determined beforehand as the TX azimuth angle with the strongest received power using an exhaustive search of both the TX/RX elevation/azimuth pointing angles. The TX antenna is always pointed at an elevation angle of -10° just below the horizon. Thus, there are nine different angular settings for every combination of TX/RX azimuth/elevation settings (i.e. three elevation settings for RX, and three azimuth settings for TX). A 10th measurement is also conducted in which the RX remains stationary in the direction of the strongest received power, while the TX performs an angular sweep in the azimuth direction in 10° angular steps.

The linear motor is used only for a small subset of measurements to investigate small-scale fading. For only a handful of locations, the TX/RX is pointed in the direction of strongest received signal, and a PDP is acquired at each linear step of $\lambda/2 = 5.35$ mm. 21 linear steps and PDPs are acquired over a length of $10\lambda = 107$ mm. This measurement helps determine the small-scale fading over a local area by comparing the 21 PDPs over the track length (see [56] for examples).

Additionally, a study is conducted to measure the reflectivity and penetration loss of various building materials at 28 GHz. As seen in Figure 3.5, the

transmitter and receiver are positioned to measure common building materials such as brick, concrete, drywall, clear non-tinted glass, and tinted glass.

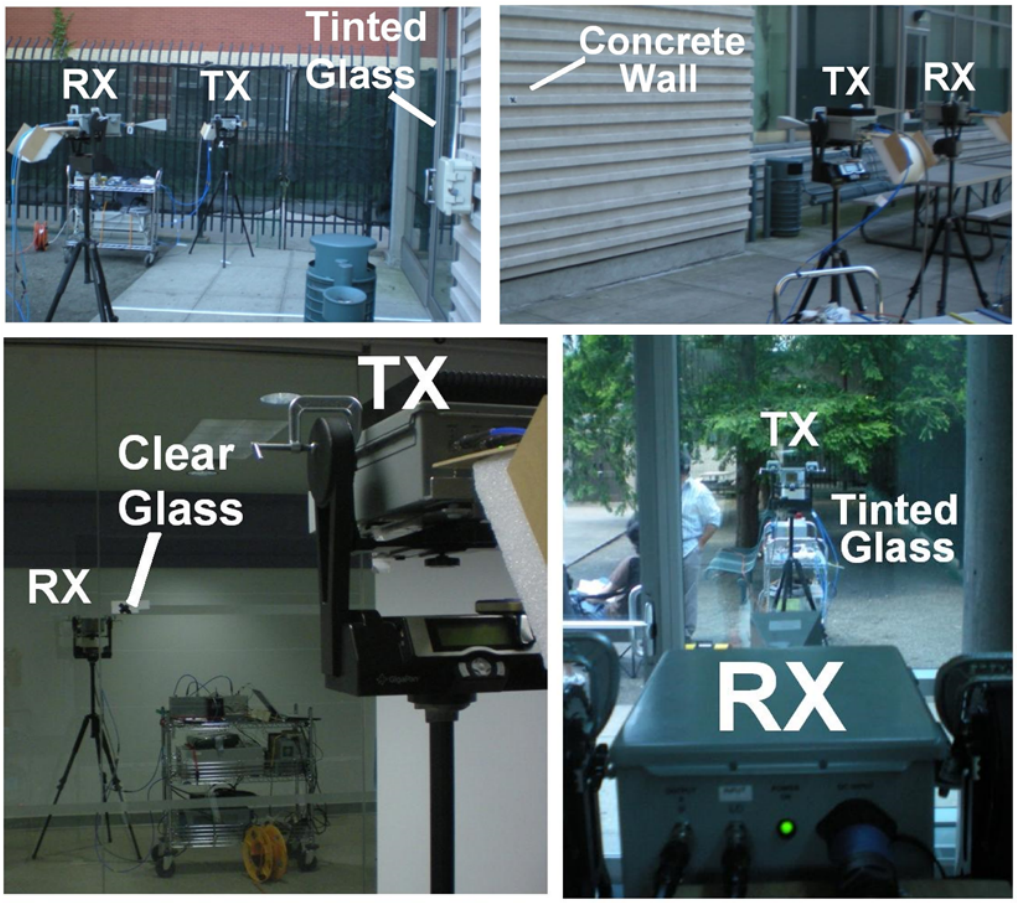

Figure 3.5: Reflectivity and penetration loss measurements are conducted for common building materials at 28 GHz.

In total, over 150 GB of raw data was collected over several months. These rich datasets are the first measurements of millimeter wave cellular communications in dense urban environments and provides academia and industry a way to model the wireless channel based on real-world measurements.

3.3 Millimeter-wave Propagation Analysis and Conclusions

The propagation data collected during this measurement campaign is continually being processed by many students and researchers today to produce meaningful channel modeling statistics for mm-wave cellular; however, early results have been found as reported in [8][7][9][10].

The first key result is that small-scale fading is not significant when the TX and RX are pointed in the direction of maximum received energy as seen in Figure 3.6 [7]. This figure shows the PDPs and angular received energy do not fluctuate over a local area and the channel is nearly constant with no significant drops in signal strength. This important finding could ease receiver design requirements.

The next key result is that building materials are highly reflective at mm-waves. Of the four materials tested, tinted glass, an outdoor-indoor material, had the highest reflection coefficient of 0.896 followed by concrete at 0.815, clear glass at 0.740, and drywall at 0.704 [9]. This finding can be useful outdoors when trying to complete links around large obstructions and using buildings as reflectors to complete a link between a transmitter and receiver; however, this can also be problematic when users enter a building as outdoor RF energy will not be able to penetrate into the building. A handoff technique from outdoor-to-indoor wireless networks will be needed for millimeter-wave cellular communications.

Another key result is that RF energy can be received in all azimuth an-

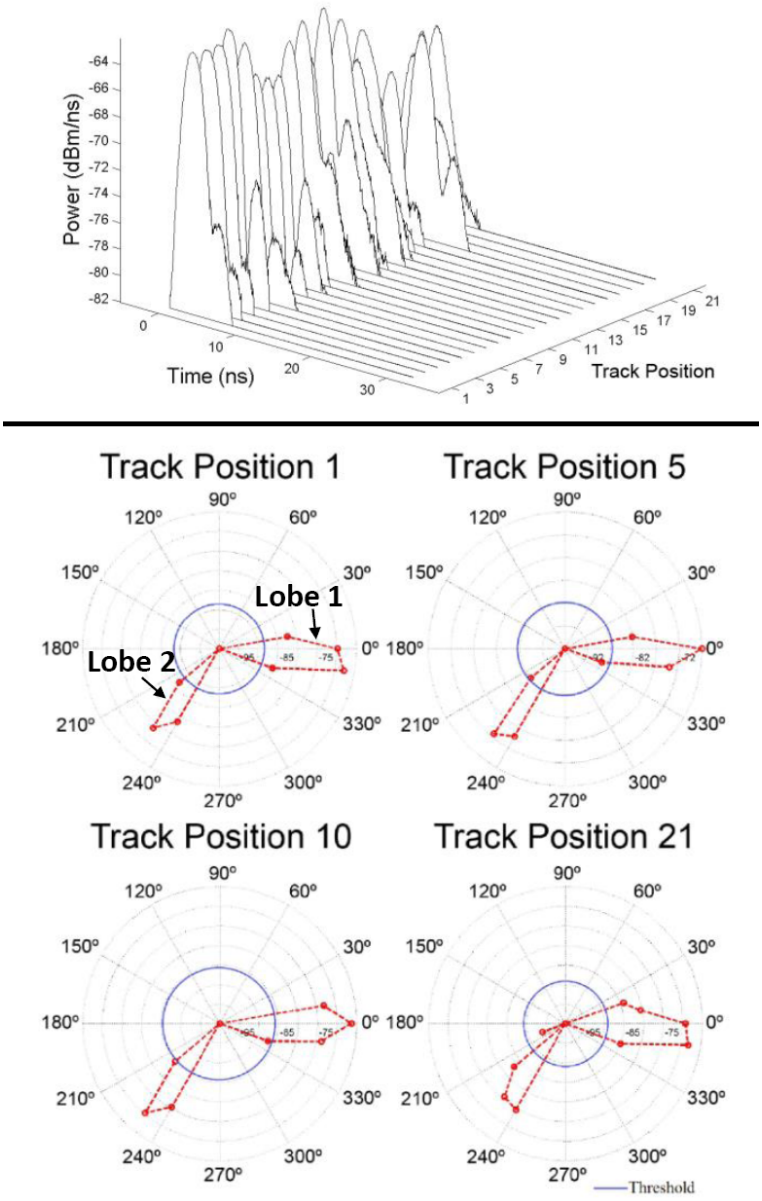

Figure 3.6: Very little small-scale fading is seen at millimeter-wave communications when using directional antennas. The top graph shows the power delay profiles do not change drastically over a local area of $10\lambda = 107$ mm. The bottom graph shows that the angle of arrival of RF energy also remains unchanged over the local area.

gular directions with a uniform distribution [7]. As seen in Figure 3.7 showing the combination of TX-RX azimuth angles, a link could be created at virtually any RX azimuth angle when the TX was pointed in the general direction of the RX (i.e. 0° TX azimuth). Thus, antenna and circuit designers must design on-chip antennas with the ability to receive energy in any direction by either using omnidirectional antennas or beamforming techniques to electrically point an antenna array in any desired direction.

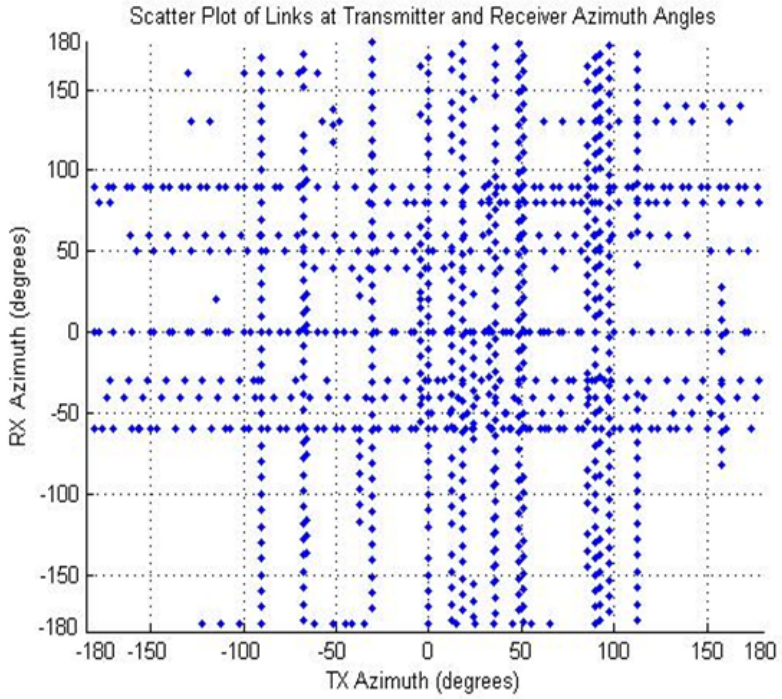

Figure 3.7: A uniform distribution exists when determining the angle-of-arrival of RF energy. Millimeter-wave wireless devices will need to be able to transmit and receive energy in any direction to complete the link.

The next key result is that the coverage radius and the ability to create

a link between TX and RX is limited to $\approx$ 200 m, which is the average radius of a cellular picocell tower. Beyond 200 m, signal can not be acquired at a majority of the RX locations when using the full transmit power of +30 dBm [8]. Additionally, the average path loss exponent (n) (i.e. the slope of the best fit line mapping received power versus distance) is 5.76 as seen in Figure 3.8 [8]. As a reference, a path loss exponent of 2 corresponds to $1/r^2$ power decay. This path loss exponent is found when considering all TX-RX angular links; however, when only considering the pointing angles with the strongest received power at each RX location, the path loss exponent reduces to 4.58 which is common in today's cellular systems [56]. This key result demonstrates the feasibility of deploying mm-wave cellular in dense urban environments.

Given the NLOS environment, path loss exponents that can approach 5.76, RF energy that can uniformly arrive in any direction, and the high reflectivity of building materials, antenna and circuit designers should create high gain antennas with beamsteering capabilities to help complete the TX-RX link. This implies a phased antenna array which will increase antenna gain and offer the potential of electrically steering the antenna beam to bounce off objects in the environment and complete the NLOS link. Given that small scale fading is minimal, the phased array will not need to aggressively search for the best antenna pointing angle over a local area, which can reduce system complexity and communication overhead. These key findings in [8][7][9][10][53] as well as new channel statistics currently being developed by students and researchers today provide engineers a firm understanding on how to design

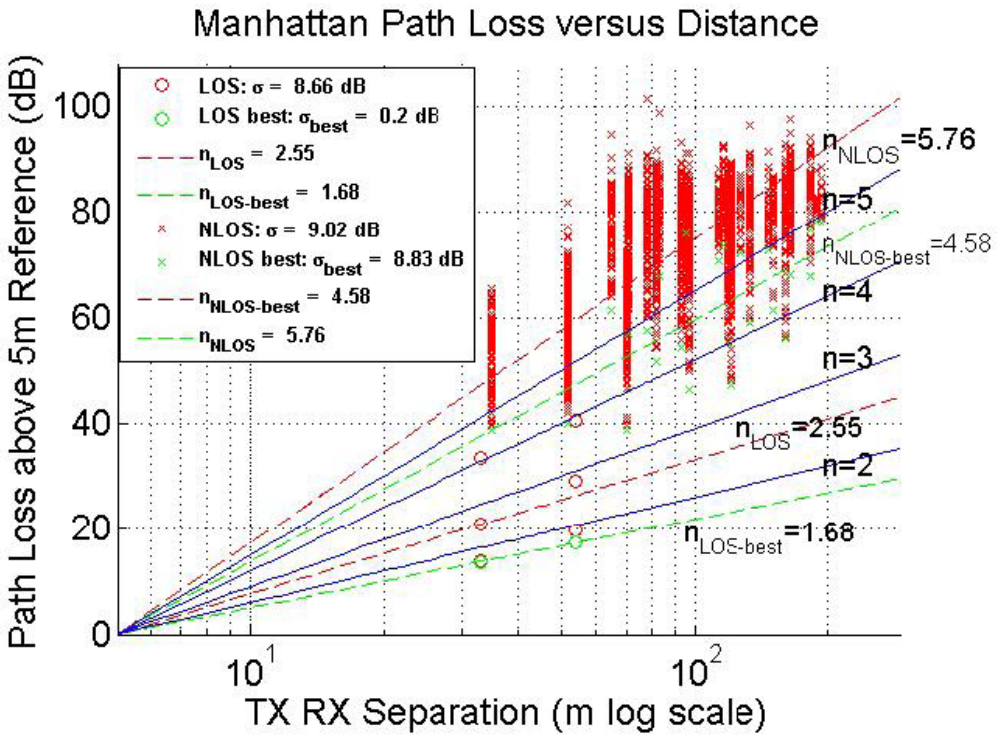

Figure 3.8: The average path loss exponent of the 28 GHz wireless channel in a dense urban environment was 5.76 when considering all NLOS pointing angles; however, when only considering the pointing angles with the strongest received power per RX location, the path loss exponent reduces to 4.58. No signal was acquired beyond 200 meters between the TX and RX.

millimeter-wave wireless communications.

Chapter 4

Millimeter-wave and Sub-Terahertz On-Chip Antennas and Arrays

This chapter discusses the design and fabrication of on-chip antenna using a 45 nm CMOS Silicon-On-Insulator (SOI) process. Given the potential of massive bandwidths at mm-wave and sub-THz frequencies such as 28 GHz [7][8][9][10], 38 GHz [53][54][55], 60 GHz [1][57][58][6][59][60][5], and 77 GHz [3][19][30][34][20], this on-chip antenna is designed to operate at 180 GHz within the WR-5 frequency band which has similar propagation characteristics and atmospheric absorption properties as the unlicensed 60 GHz band. As semiconductor processes improve and transistors achieve higher frequencies of 100s of GHz and as wireless carriers demand greater bandwidths to service their users, mm-wave and sub-THz bands such as 180 GHz will become unlicensed. Given the higher free space path loss at mm-wave and sub-THz frequencies, the on-chip antenna is implemented as a phased array to increase antenna gain, directionality, and enable the possibility of beamsteering. This is one of the first fabricated on-chip antenna arrays on a CMOS process to be designed and measured in the WR-5 frequency band.

4.1 Key Fabrication Concerns for On-Chip Antennas and Arrays

There are several key concerns that should be understood when designing an on-chip antenna. Most of these concerns involve fabrication limitations such as metal density requirements and metal geometry limitations. Before attempting to design and simulate an on-chip antenna, the first step is to study and understand the semiconductor process design rules. These design rules are provided by the semiconductor foundry within the Process Design Kit (PDK) and determine the feasibility and limitations of fabricating chips. For example, the design rules dictate how close two metal traces can be fabricated to each other, the minimum and maximum metal density in any given area of the designed chip, the allowable angles for metal trace bends, the minimum distance that metal can be placed near the chip edge, etc.

In this particular 45 nm CMOS process, the design rules do not allow 45° metal trace bends. Thus, only 90° metal trace bends are allowed, which is important when designing the antenna feed network as well as trying to implement certain types of antenna designs containing oblique angles such as the patch antenna in [21]. Another key design rule involves metal density. In a viewing window of 25 $\mu m \times 25$ μm, there must be at least 20% and at most 80% metal in each metal layer in the chip design, thus the on-chip antenna can not have large areas without metal, and in the areas that do contain large areas of metal, the metal area must have holes or "slots" as seen in Figure 4.1 to reduce density to 80%. This process is also known as "cheesing" the metal

since the metal will have holes like Swiss cheese.

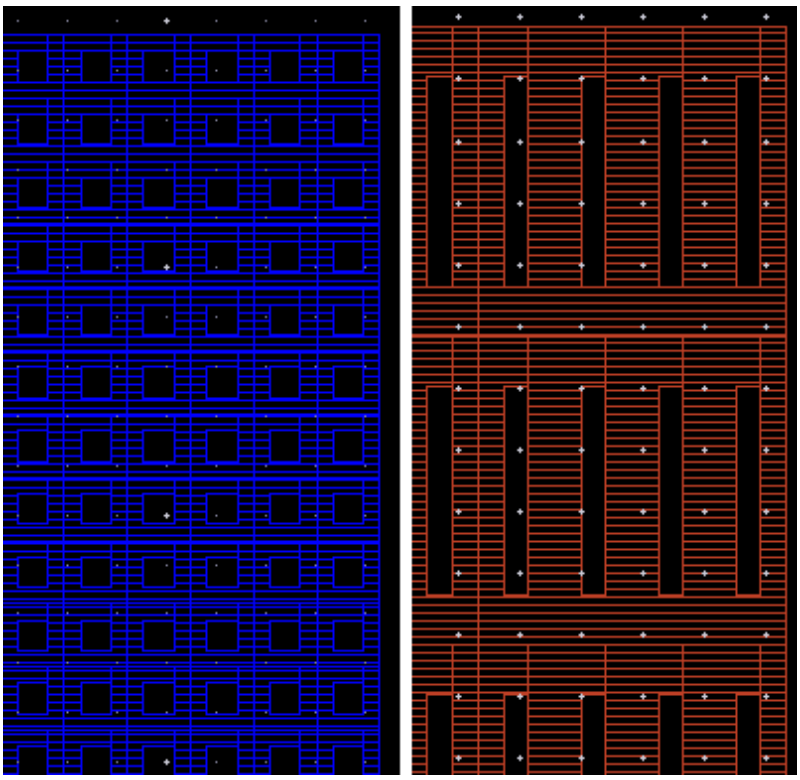

Figure 4.1: Examples of slots added to large areas of metal as required by the semiconductor foundry. Slots should be oriented to minimize impedance to current flow. Understanding the process design rules provided by the foundry is important when designing on-chip antennas and circuits.

It is good practice for these "slots" to be rectangular and oriented parallel to the anticipated current flow in the metal. This slot orientation helps reduce any increased impedance as is also done in [4][25][61]. In addition, there must be a smooth gradient between an area of high metal density to an area of low metal density, thus small blocks of dummy metal fill should transition between the areas of 80% metal density to areas of 20% metal density.

Another key concern when designing on-chip antennas in CMOS is the lossy silicon substrate underneath the antenna which can reduce radiation efficiency and antenna gain [6][3][29]. Several researchers have attempted to mitigate the substrate losses using complex solutions such as creating silicon lenses under the chip [3][30] or etching out the substrate to create air or polymer cavities under the antenna [21][34]; however, these custom-built solutions should be avoided to reduce manufacturing costs and production time. The last important concern when designing on-chip antennas is that the foundry may add metal fillings throughout the submitted chip design to be fabricated. After a researcher has submitted a chip design that passes all foundry design rules, the foundry will execute a proprietary algorithm which scans the design and adds additional metal fill to the chip. This obviously is a problem to antenna designers as any metal placed adjacent to an antenna has the capability to de-tune and degrade the intended antenna performance [62]. The chip designer does have some flexibility to add metal fill "EXCLUDE" areas to parts of the on-chip antenna, which instructs the foundry to not add any metal fill; however, the use of metal fill EXCLUDE layers is very limited in area. The final antenna design should be robust to any potentially adjacent metal fill that is added by the foundry.

Given all these key constraints by the foundry design rules, a patch antenna with a microstrip feed network was chosen as the best candidate to be fabricated on the 45 nm CMOS process. Patch antennas are simple planar antennas which are ideal for on-chip implementation and can be designed at

any frequency of interest. As seen in Figure 4.2, patch antennas operate using two conductors much like a parallel-plate capacitor with the top conductor fed with the RF signal while the bottom conductor provides a ground plane. The height of the top conductor above the ground determines the bandwidth of the antenna (i.e. a larger height allows larger bandwidths) [51]. The fringing electromagnetic fields at the top and bottom edges of the top conductor are responsible for producing the radiation into free-space as seen in Figure 4.2. When presented in literature, patch antennas are some of the most efficient on-chip antennas at about 20% radiation efficiency [4][25][61][15]. The ground plane of the patch antenna isolates the RF signal from the silicon substrate which helps prevent radiation losses in the silicon and increase radiation efficiency. A phased array can also be easily created using individual patch antennas. The next sections provide details about the design of the 180 GHz on-chip patch antenna, antenna array, feed network, and RF probe pads.

4.2 Design of A Single On-Chip Patch Antenna

Using the key design considerations presented in the previous section, the on-chip patch antenna and array are designed and fabricated on a 45 nm CMOS process operating at the sub-terahertz frequencies around 180 GHz. The 45 nm CMOS process contains 11 metal layers (labeled "1" to "11" from lowest to topmost layer) made of copper and aluminum, three dielectric layers with various permittivities in between the 11 metal layers, and one passivation layer which is the topmost layer that encapsulates and protects the chip from

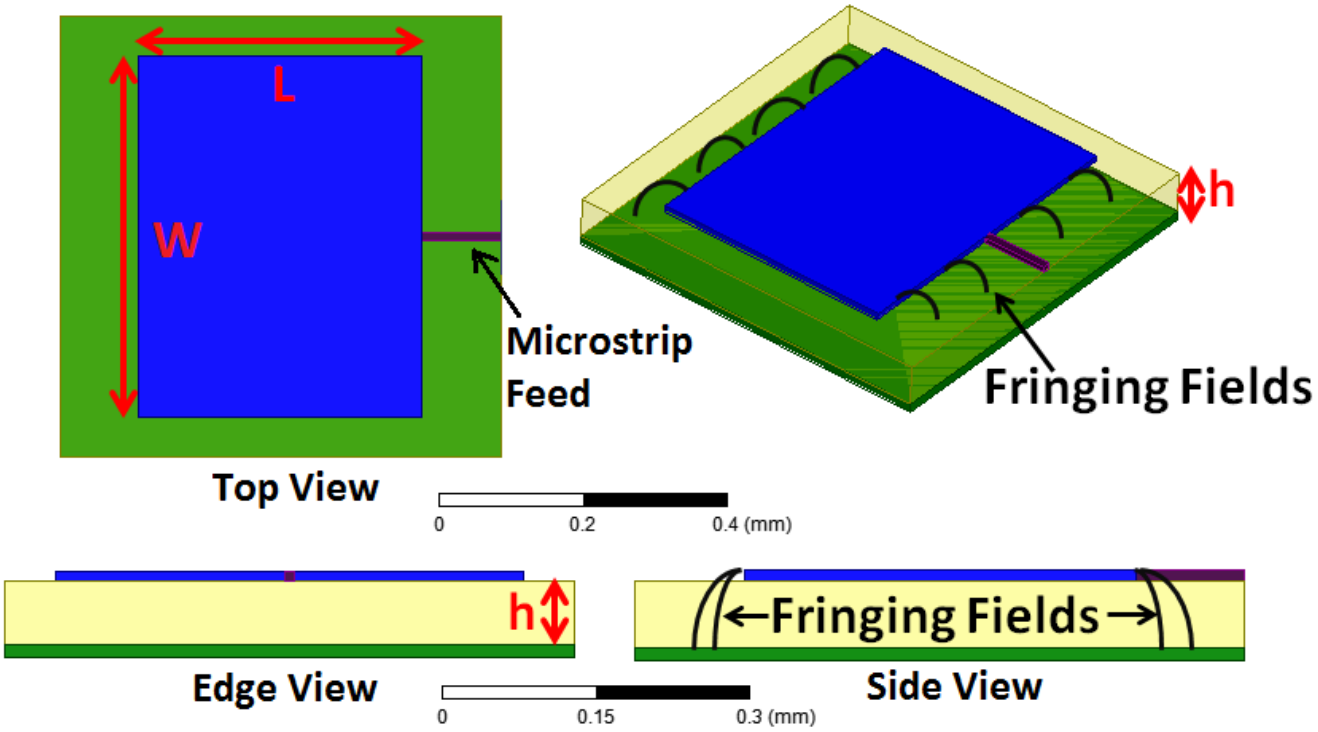

Figure 4.2: A general patch antenna. The RF signal is applied to the microstrip line (purple) which feeds the top conductor (blue) with respect to the ground plane (green). The width W and length L of the patch antenna are adjusted to tune the antenna to a specific frequency of operation. The height h of the patch also helps tune the antenna and increase the bandwidth of operation. The fringing fields of the patch at the top and bottom edge are responsible for producing radiation into free space.

the environment. Each metal and dielectric layer is of various thickness with the topmost layers having the largest thicknesses $\approx 2.2\ \mu m$. The entire thickness of all 11 metal layers with dielectrics is $\approx 11\ \mu m$. The patch antenna should be designed to have a 50 Ω impedance at 180 GHz with return loss $(S_{11}) \leq$ -10 dB. The width W and length L of the patch antenna as seen in Figure 4.2 are two parameters that can tune the antenna's impedance and frequency of operation.

To maximize bandwidth, the height of the patch antenna above the ground plane should be as high as possible. An ideal patch antenna design would place the patch conductor on metal 11 and the ground plane on metal 1; however, metal fill requirements prevent entire metal layers from missing (i.e. metal layers 2 to 10). Thus, a metal fill design is needed on the layers in between the patch conductor and ground plane similar to [15] which used two layers of metal fill between the patch antenna and ground plane. Additionally, to maximize the patch height above ground, the thickest metal layers just below the patch conductor should be metal filled. The final patch design has metal layer 11 as the patch conductor, metal layers 10 and 9 as metal filled, and metal layers 8 to 1 as the ground plane with interconnecting vias (note that if circuitry was needed beneath the antenna, metal layers 1-7 could be used to route signals throughout the chip while only metal 8 would serve as the ground plane for the patch antenna as was done in [15]). This produces a patch height of $h = 6.3\ \mu m$ above the ground. To create metal fill in metal layers 10 and 9, small rectangular pieces of metal are placed between the patch

and ground in a staggered fashion until the 20% metal density rule is achieved as seen in Figure 4.3. Metal fill EXCLUDE layers are drawn over the patch antenna to prevent the foundry from adding dummy metal fill. The metal fill EXCLUDE layers cover the entire patch including a 50 μm border beyond the patch antenna edges. Simulations showed that the ground plane does not need to extend more than 50 μm beyond the patch antenna edge, and any dummy metal fill located beyond 50 μm (as seen in Figure 4.4) does not effect the on-chip patch antenna performance.

Using patch antenna design equations in Balanis [51] (see Chapter 14.2, Eqns. 14-1 to 14.7), an initial starting point of $W = 507$ μm and $L = 397$ μm is modeled and simulated in HFSS. Given the unique nature of the on-chip patch antenna with multiple dielectrics and metal fill, the HFSS optimization routine is used to adjust W and L while maximizing antenna gain at 180 GHz. The final optimized size is $W = 497$ μm and $L = 393.7$ μm and an antenna gain of -3.21 dBi. The ground plane extends 50 μm beyond each patch edge as seen in Figure 4.5. The input impedance of the patch antenna is 42.12+j2.06 Ω with the lowest return loss at 178.2 GHz and a bandwidth of 3.64 GHz. The simulation data of return loss, impedance, and radiation pattern is plotted and compared directly with measured data in Chapter 6.

The microstrip feed line to the patch antenna is also optimized to a characteristic impedance of 50 Ω using the 2-D electromagnetic simulation tool ANSYS Q3D Extractor. To match the design of the on-chip patch antenna, the microstrip signal line is also fabricated on metal 11. Metal layers 8, 9, and 10

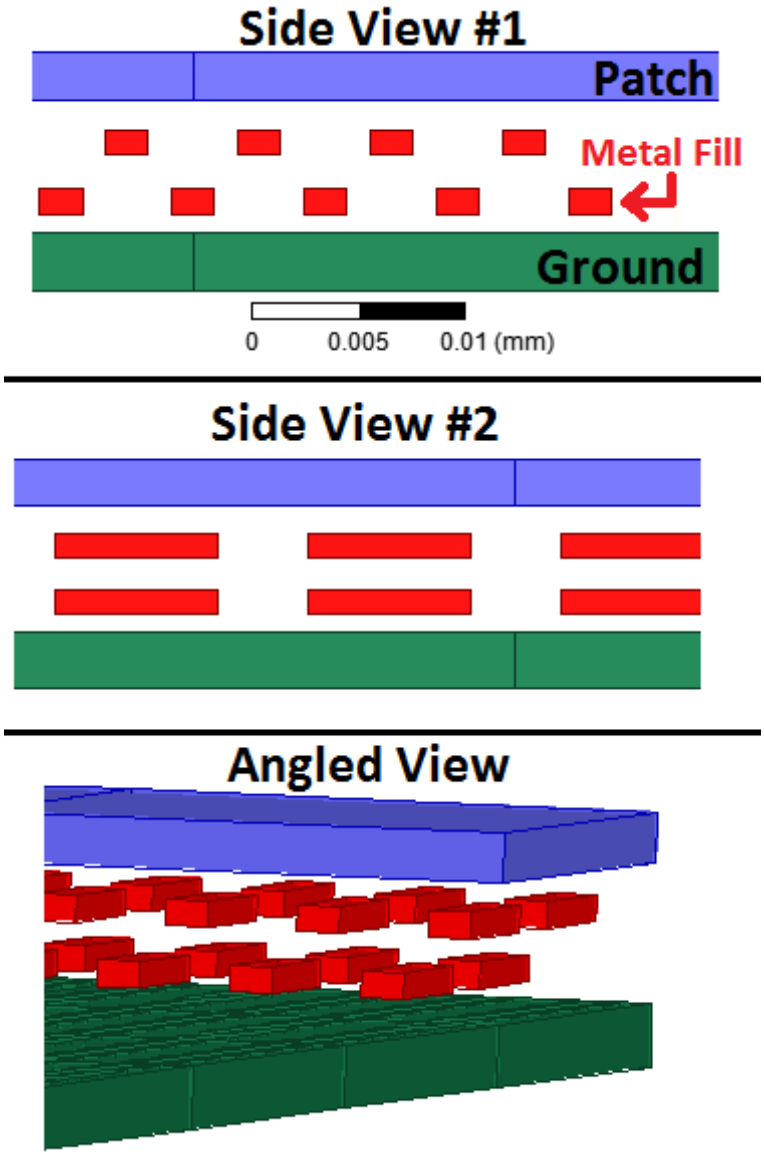

Figure 4.3: At least 20% metal density is required per metal layer as dictated by the foundry design rules, thus dummy metal fill (red) is placed between the patch and ground plane on metal layers 9 and 10. Metal layer 11 produces the patch (blue) and metal layers 1-8 are interconnected with vias to produce the ground plane (green).

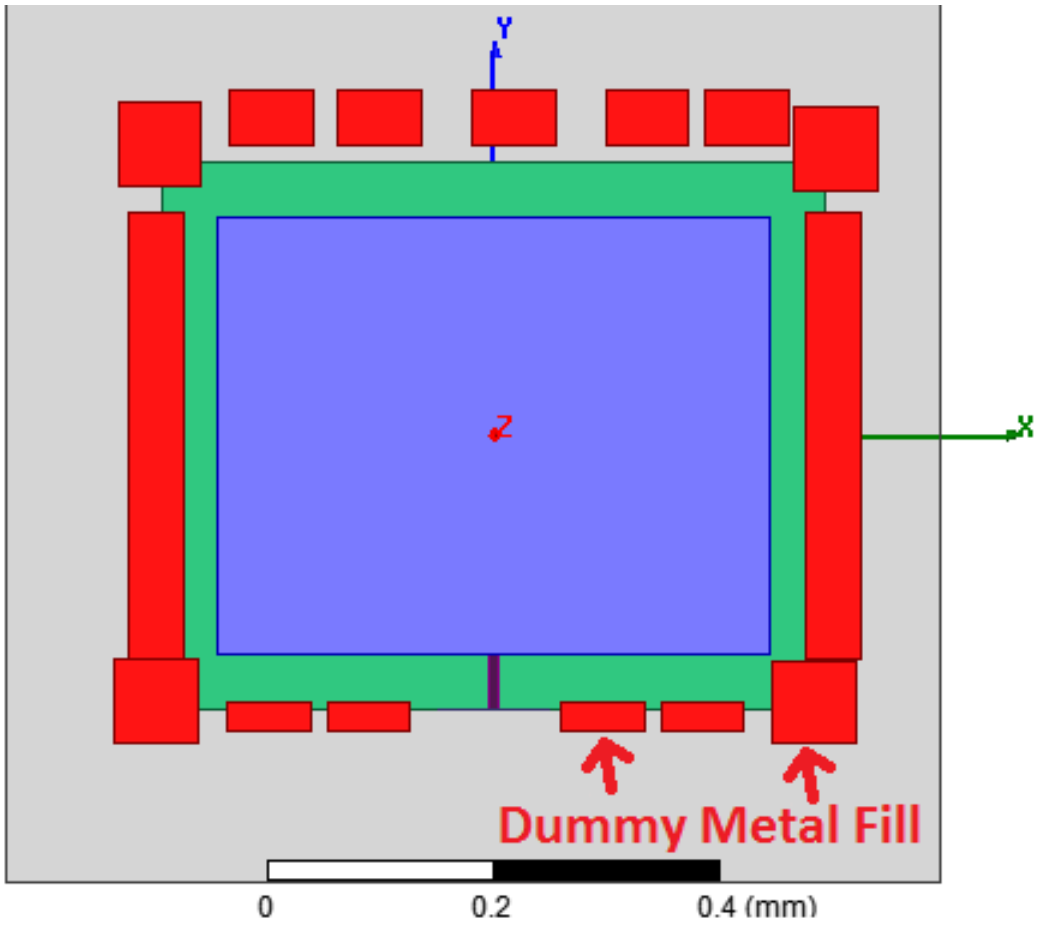

Figure 4.4: Dummy metal fill (red) is added around the patch antenna to simulate metal fill added by the foundry. This metal fill could potentially degrade antenna performance. Simulations showed that the ground plane and any dummy metal beyond 50 μm from the patch antenna edges did not effect antenna performance, thus the ground plane was truncated to 50 μm beyond the patch edges. Additionally, metal fill EXCLUDE layers were placed on the patch antenna area including a 50 μm border to prevent the foundry from adding metal fill to these sensitive areas.

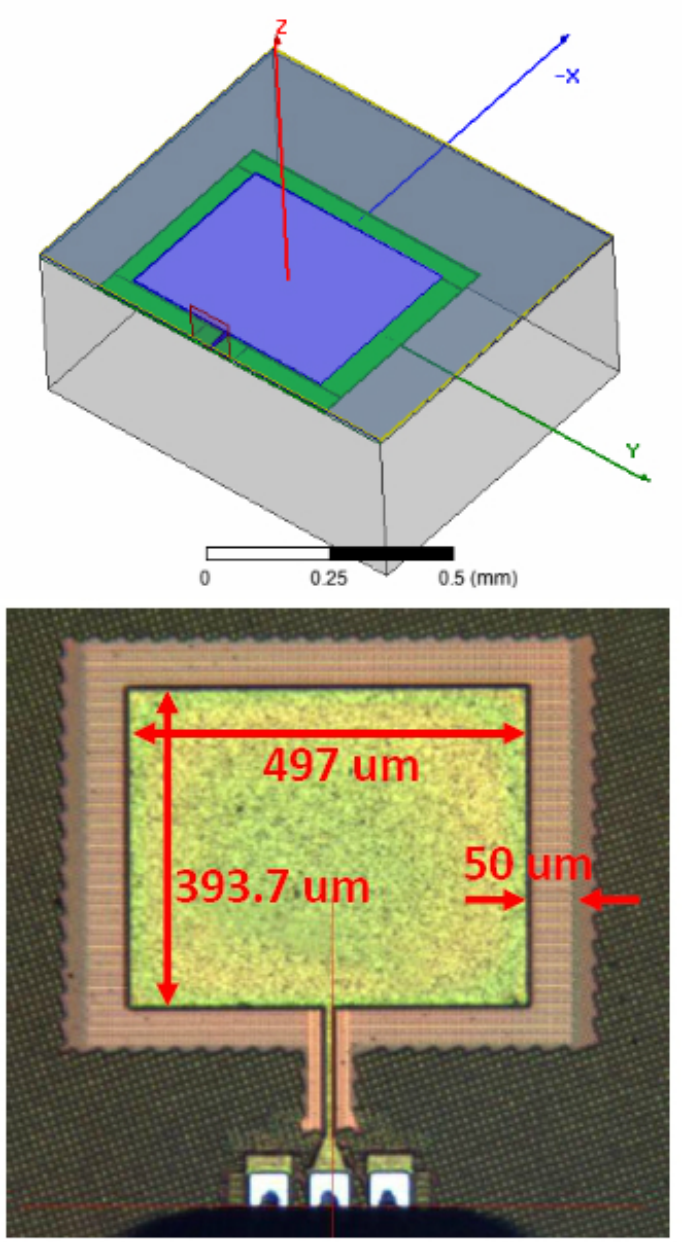

Figure 4.5: The HFSS-optimized patch antenna has a geometry of $W = 497$ μm, $L = 393.7$ μm, and $h = 6.3$ μm which produces an antenna gain of -3.21 dBi at 178.2 GHz and a bandwidth of 3.64 GHz. The simulation results are compared with measured results in Chapter 6.

are metal fill, and metal layers 1-7 are the ground plane with interconnecting vias as seen in Figure 4.6. The width of the signal trace is adjusted to 9.9 μm to obtain a characteristic impedance of 50.3-j0.9 Ω across the WR-5 frequency band of 140 GHz to 220 GHz.

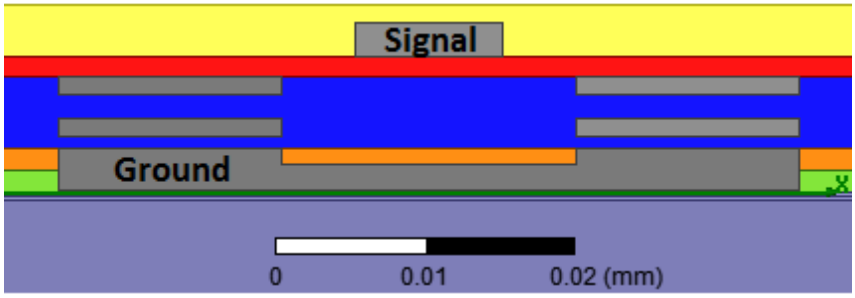

Figure 4.6: The cross section of the simulated microstrip transmission line using ANSYS Q3D Extractor. The signal trace uses metal 11, and the ground plane is made of metal 1-7 using interconnecting vias (vias not shown). Metal layers 8, 9, and 10 are metal fill. A line width of 9.9 μm produces a characteristic impedance of 50.3-j0.9 Ω.

4.3 Design of the On-Chip Patch Antenna Array with Feed Network

Once the single patch antenna design is optimized, the phased array can be designed. Large arrays provide the advantage of higher antenna gains, narrow beamwidths, and beamsteering capability; however, in the context of on-chip antenna arrays, there exists a tradeoff between large arrays and device cost. Chip area is one of the most important factors that circuit designers must consider, and a large array will cover a larger chip area which can dramatically increase the cost of fabrication. During design, a balance must be

struck between the added benefit of a larger array versus the financial costs of the larger chip area. For this prototype project, an array of 2x2 antenna elements in a square grid formation was chosen to demonstrate the increased benefit of an array. Antenna arrays can be configured in various types such as broadside, end-fire, Hansen-Woodyard, binomial, and Dolph-Tschebyscheff depending on the direction(s) of maximum radiation [51]. Given the nature of the patch antenna element with maximum radiation pointed towards the Z-axis (as seen in Figure 4.5), a broadside array was chosen in which the direction of maximum radiation is in the same direction as the single patch elements. The antenna element spacing is $d = \lambda/2$ which is 833 μm at 180 GHz. This array element spacing theoretically increases directivity by 4 which is 6 dB using Equation 4.1 from [51] p. 315. The directivity increase is also confirmed using electromagnetic simulations.

$$D_0 = 2N(\frac{d}{\lambda}) \tag{4.1}$$

where D_0 is the array directivity, $N = 4$ is the number of antenna elements in the array, $d = 833\ \mu m = \lambda/2$ is the spacing between the antenna elements, and λ is the free space wavelength of the desired frequency.

With the antenna element spacing set and the patch antenna elements positioned in a 2x2 grid, the feed network can be designed. The array uses a corporate feed network containing quarter-wavelength transformers at each T-junction as seen in Figure 4.7 (recreated from [51] p. 866) similar in design to a Wilkinson power divider [63].

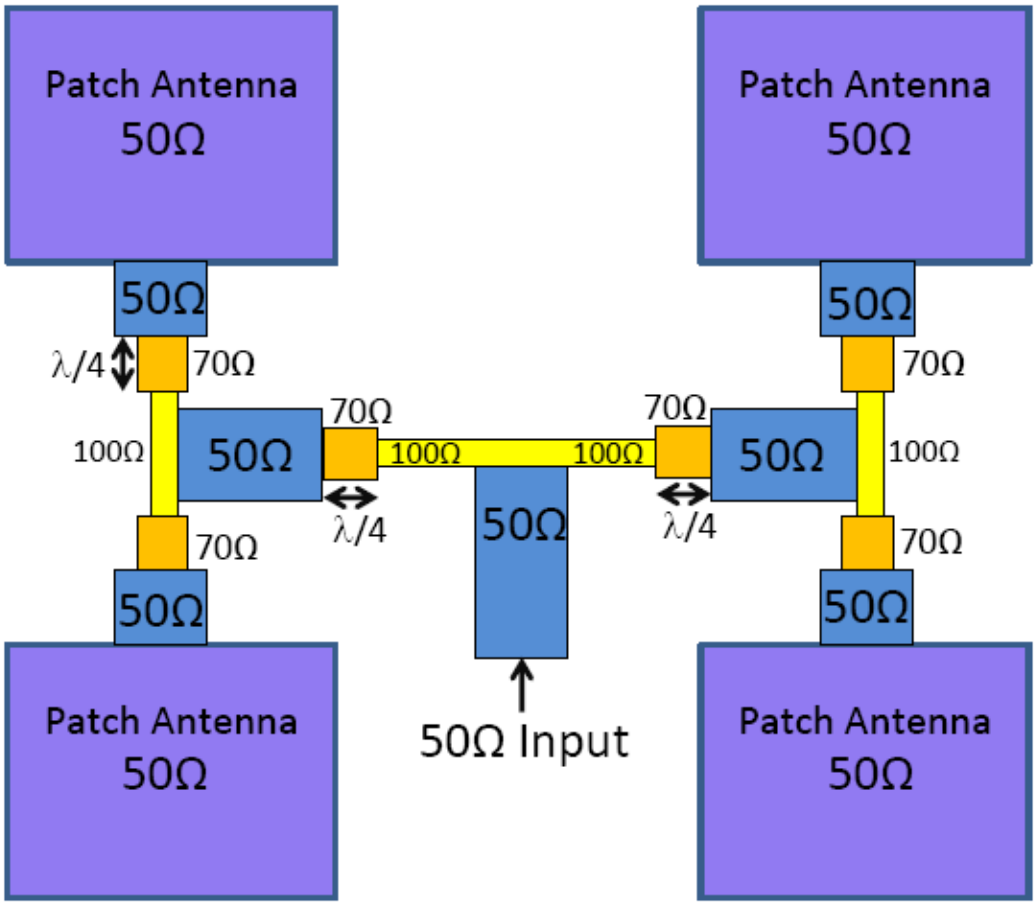

Figure 4.7: A diagram of the 180 GHz patch antenna array with feed network. The feed network is a corporate feed that uses quarter-wavelength transformers at each T-junction. The quarter-wavelength transformers convert the 50 Ω load impedance into a 100 Ω impedance using a transmission line with characteristic impedance of 70.7 Ω and length 225.5 μm. The two parallel 100 Ω impedances create a 50 Ω load impedance for the input.

Since the patch antenna elements are designed with an input impedance of 50 Ω, and the transmission lines feeding each patch antenna also have a 50 Ω characteristic impedance, then without any impedance transformation, the impedance of each branch of the T-junction will also be 50 Ω. This will cause an impedance mismatch to the input of the T-junction since two 50 Ω load impedances in parallel would appear as a 25 Ω load impedance. Therefore, at the T-junction, each branch should have an impedance of 100 Ω which creates an equivalent load impedance of 50 Ω, and allows the T-junction input (a 50 Ω transmission line) to have a good impedance match. Quarter-wavelength transformers are needed on each branch of the T-junction to convert from 50 Ω branches to 100 Ω branches. The quarter-wavelength transformer uses a transmission line with a characteristic impedance of 70.7 Ω based upon Equation 4.2 and Figure 4.8 (recreated from [63] p. 241).

$$Z_x = \sqrt{Z_0 Z_L} = \sqrt{(100)(50)} \approx 70.7\Omega \tag{4.2}$$

where $Z_x = 70.7\ \Omega$ is the characteristic impedance of the inserted transmission line of length $l = \lambda/4 = 225.5\ \mu m$ (λ is the wavelength within the transmission line at the frequency of operation), Z_L =50 Ω is the real load impedance, and $Z_0 = 100\ \Omega$ is the desired input impedance of each branch of the T-junction as seen in Figure 4.7.

The 70.7 Ω transmission line is designed the same way as the 50 Ω transmission line in Figure 4.6 using ANSYS Q3D Extractor. The signal width

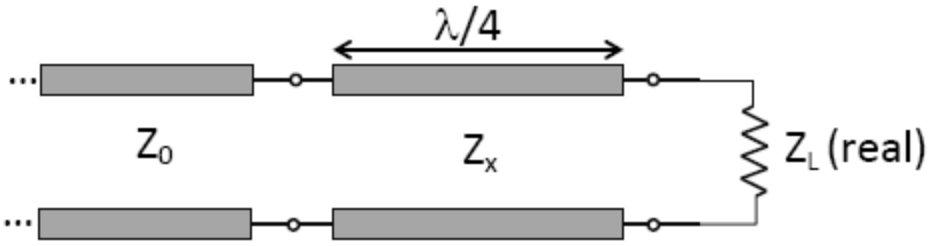

Figure 4.8: A quarter-wavelength transformer converts a load impedance, Z_L, to the source impedance, Z_0, using a short transmission line with a characteristic impedance, Z_x, calculated using Equation 4.2. To convert a 50 Ω load impedance to an input impedance of 100 Ω at 180 GHz, a 70.7 Ω transmission line of length 225.5 μm is inserted between the source and load.

is shortened to 4 μm to produce a simulated characteristic impedance of 71.8-j1.4 Ω. The simulated wavelength for the transmission line is 902.02 μm, thus the length of the $\lambda/4$ transmission line is 225.5 μm. To help measure and estimate the attenuation of the feed network, a sample 50 Ω transmission line was added to the chip with RF probe pads. By measuring the insertion loss of this sample transmission line, the attenuation of the entire feed network can be calculated and de-embedded from the measured gain of the patch antenna array as performed in Chapter 6.

To correctly phase the antenna elements so that the maximum radiation is pointed normal to the chip towards the Z-axis, the lengths of the transmission lines to all of the patch antenna elements must be identical. With identical lengths, all the phases from each of the antenna elements constructively add together. During layout, the top two patch antenna elements had shorter transmission lines to the RF probe pad compared to the bottom two antenna

elements, thus extra transmission line was needed for the top elements. A transmission line bend was inserted between the top two antenna elements as seen in Figure 4.9. Figure 4.9 shows both the final layout of the patch antenna array in simulation as well as the fabricated chip. The final size of the array is 1430.33 $\mu m\times$ 1327.03 μm and has a simulated antenna gain of +2.81 dBi at 178.2 GHz. The input impedance of the patch antenna array is 44.35-j5.68 Ω at 178.2 GHz and a simulated bandwidth of 9.84 GHz. The simulation data of return loss, impedance, and radiation pattern is plotted and compared directly with measured data in Chapter 6.

4.4 RF Probe Pad Design

The design of the RF probe pad depends on the RF probe to be used to measure the chip. After consulting with Cascade Microtech and other industry RF circuit designers, the probe that was chosen was the Cascade Microtech Infinity I220-T-GSG-75-BT Ground-Signal-Ground RF probe. The probe pitch (i.e. the distance between the center signal probe tip and the coplanar ground probe tips) is 75 μm and is important when designing the RF probe pad. When probing down, the probe will make initial contact with the probe pad and begin to be pressed into the pad to make good contact with the chip. The probe is pressed downward (i.e. "overdrive") at least 25 μm, but no more than 50 μm to make good contact. As the probe presses downward after contact, it will begin to skid (i.e. "skate") towards the device it is measuring. The probe skate is up to 25 μm, and thus, the probe pad is designed to be rectangular

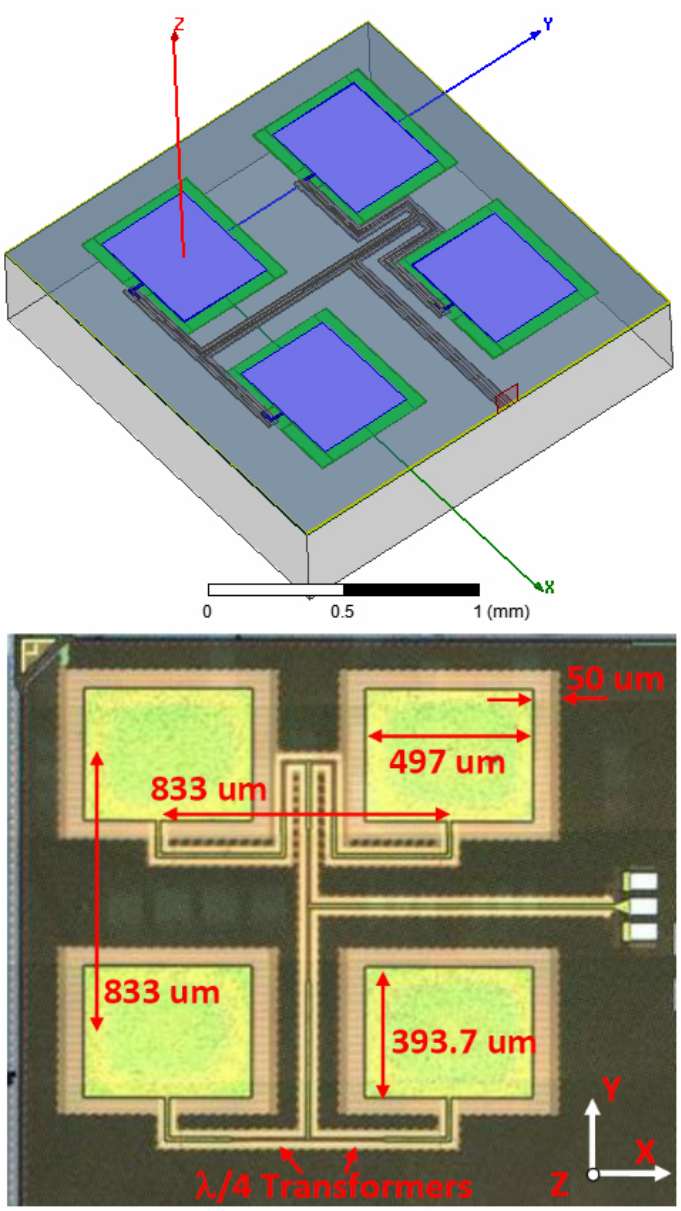

Figure 4.9: The 2x2 180 GHz patch antenna array. The array size is 1430.33 $\mu m\times$ 1327.03 μm and has a simulated antenna gain of +2.81 dBi at 178.2 GHz. The input impedance is 44.35-j5.68 Ω and has a simulated bandwidth of 9.84 GHz. The simulation results are compared with measured results in Chapter 6.

with the longer side in the direction of the probe skate as seen in Figure 4.10. The size of each pad is 45 $\mu m \times$ 75 μm with a pitch of 75 μm. Additionally, it is extremely important to properly and consistently align the RF probe within the probe pad especially at millimeter-wave and sub-terahertz frequencies [64][65]. Chip measurements can have significant errors if the probe is misaligned, overskates, or underskates. Thus, to ensure proper and consistent skate by the RF probe, a miniature ruler was added along the sides of the probe pad as seen in Figure 4.10. This ruler uses 5 μm tick marks of metal 11. Thus, when measuring a chip, the user can simply use the microscope crosshairs to properly align the probe tip and skate the RF probe exactly 25 μm as seen in Figure 4.11.

This chapter discussed the design and fabrication of the sub-terahertz antennas, phased array, feed network, and RF probe pads. The next chapter discusses the design and construction of the on-chip antenna measurement system.

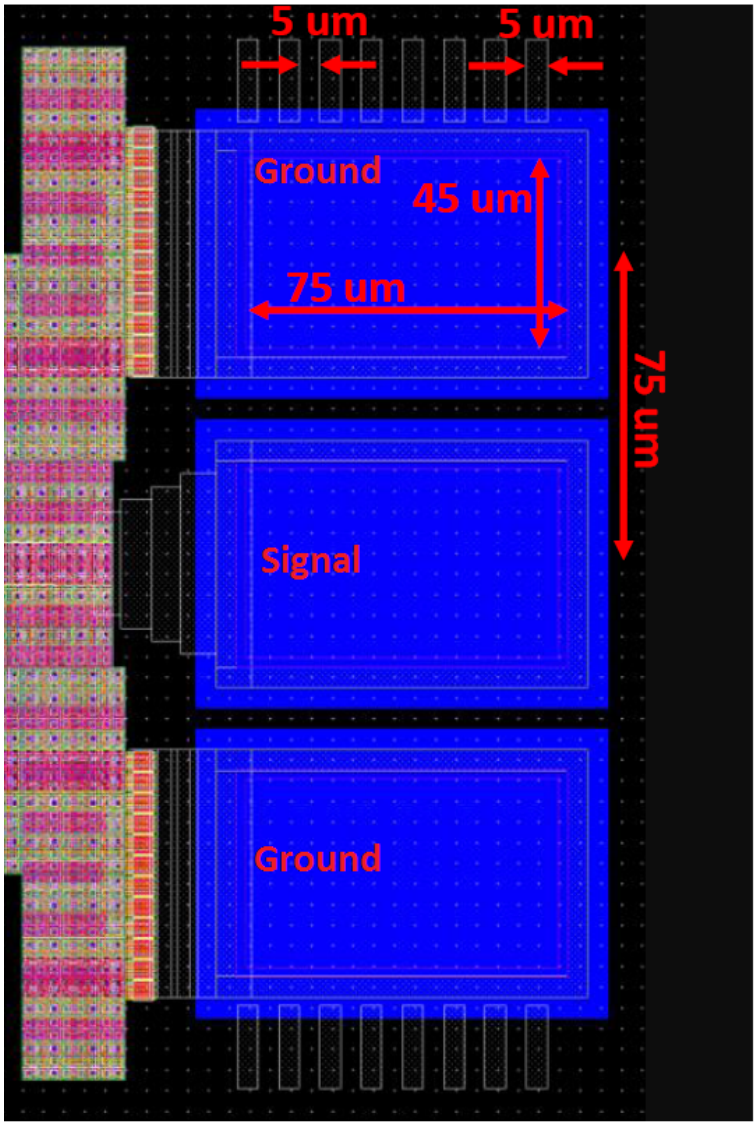

Figure 4.10: The Ground-Signal-Ground RF probe pads are rectangular with dimensions of 45 $\mu m \times$ 75 μm and a pitch of 75 μm (the distance between the center of the signal pad and the center of the ground pads). A miniature ruler was created using 5 μm strips of metal 11, the top most metal, which helps with proper probe placement and skate.

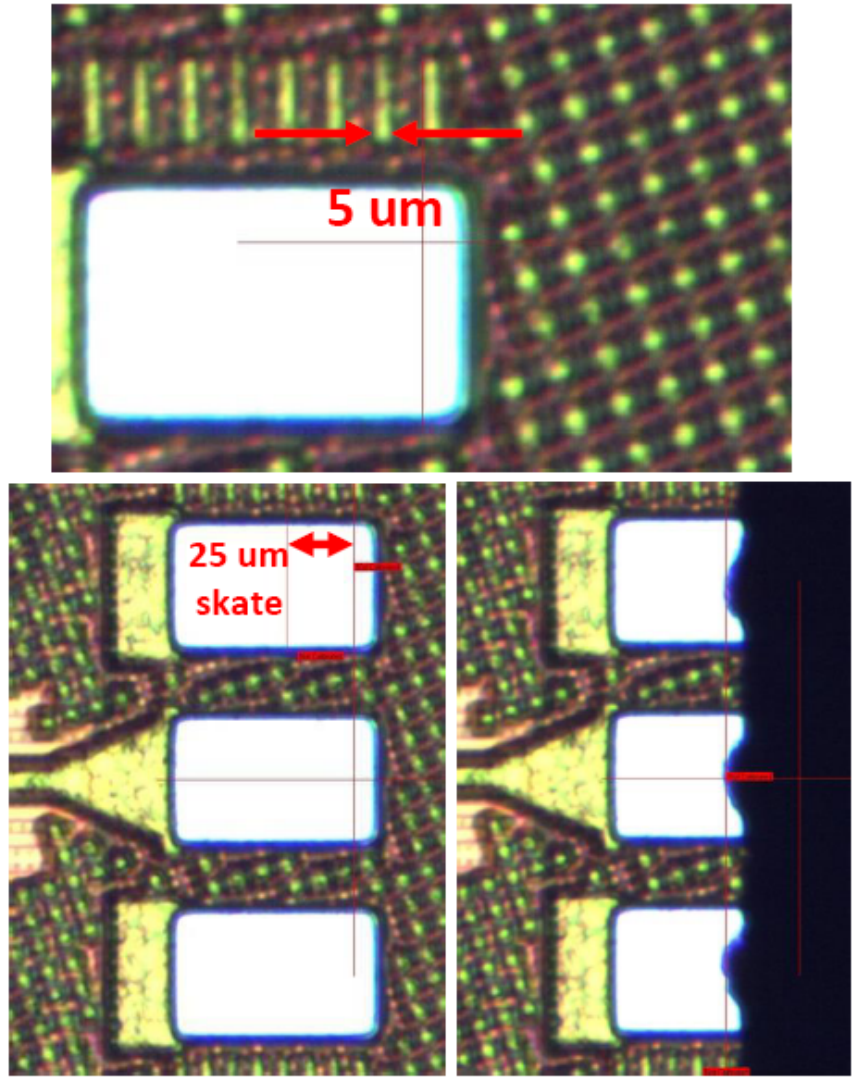

Figure 4.11: The miniature ruler and microscope crosshairs help align the RF probe to a consistent and repeatable position within the probe pad. The ruler helps to measure proper probe skate which is extremely important especially at sub-terahertz frequencies. Cascade Microtech recommends up to 25 μm of probe skate.

Chapter 5

On-Chip Antenna Radiation Pattern Measurement System

To characterize, measure, and understand on-chip antennas at millimeter wave or sub-terahertz frequencies, an antenna measurement system was constructed around a Cascade Microtech wafer probe station Summit 11000B as seen in Figure 2.3 and Figure 2.4. The purpose of using a wafer probe station environment is that all mass-produced integrated circuits are tested extensively prior to wafer dicing. Only the chips that pass testing are packaged after dicing and sent further through the production line. When testing integrated circuits, both digital and analog signals are applied and measured using DC and RF probes as seen in Figure 5.1. If on-chip antennas are to be fabricated and integrated with digital, analog, and RF circuits on a single integrated chip, then antenna measurements should be performed in conjunction with all other wafer-level testing procedures. Thus, it is important to perform antenna measurements in a probe station environment to verify antenna radiation performance prior to packaging. This chapter discusses the construction of a sub-terahertz on-chip antenna measurement system with capability to measure 140 - 220 GHz.

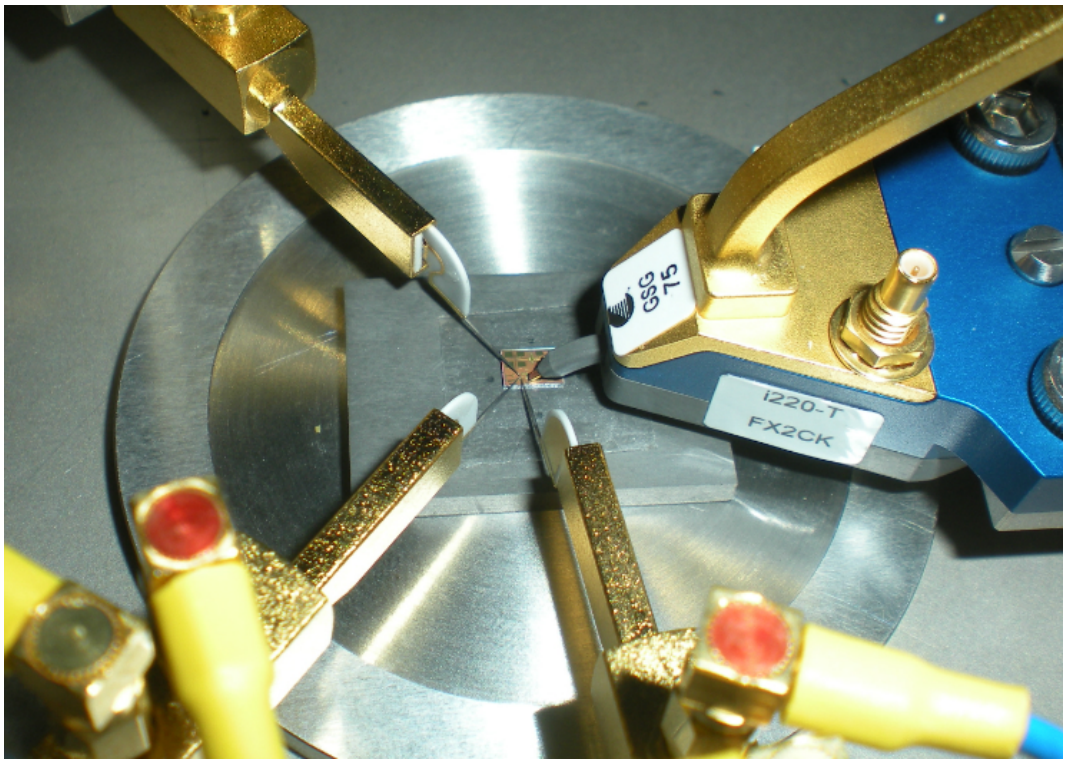

Figure 5.1: An example of a diced integrated circuit being tested with three DC probes and one RF probe in a wafer probe station.

5.1 Key Concerns For Accurate Antenna Testing

Creating an antenna measurement system requires attention to detail as can be seen in the 135-page IEEE Standard Test Procedures for Antennas (IEEE Std. 149-1979 (R2008)) [50]. This IEEE standard was consulted extensively to construct an accurate far-field antenna measurement system in a probe station environment. One possible way for testing the radiation pattern of an antenna under test (AUT) is to place the AUT in a fixed position and transmit a constant power level. A receiver antenna with known gain will then measure the received amplitude, phase, polarization, and power gain over a measurement sphere of constant radius R from the AUT phase center. However, traditionally, the AUT is in receiving mode while a source antenna transmits and illuminates the AUT with a uniform plane wave. The source antenna is positioned at various pointing angles with respect to the AUT and maintains a constant radius R. This antenna range configuration is known as a "moveable-line-of-sight configuration" since the source antenna is moving while the AUT is fixed. This configuration was used for the probe station antenna measurement system since the AUT is an on-chip antenna and must remain in a fixed position while being probed.

The ideal electromagnetic wave impinging on the AUT should be a uniform plane wave (i.e. a wavefront with constant amplitude and phase over the AUT region). A uniform plane wave can be accomplished using a "free-space range" in which the source antenna is at a distance far enough from the AUT that the spherical waves approach a plane wave across the AUT

aperture. It is important that only a single plane wave with constant phase and amplitude illuminates the AUT at every spatial position and that all reflections from the environment such as from walls and reflective objects be eliminated. RF absorbing material is typically used to suppress reflections in the antenna test environment and is applied to all walls, surfaces, and nearby objects that could potentially reflect radio waves.

As stated in [50], a wave with nearly constant amplitude should illuminate the AUT and recommends no more than $\pm$ 0.25 dB amplitude variation which is maintained by a constant distance R between the source antenna and AUT. On page 8 [50], the IEEE standard states that a phase variation criterion also needs to be established for the illuminating field over the AUT. It states that, "for most practical situations the phase variation is a function solely of the separation between the source antenna and the AUT. If, in the absence of reflections, the 0.25 dB criterion for amplitude variation is adhered to, then the corresponding phase variation will be very close to that of a spherical wave emanating from the phase center of the source antenna. This is true for spacings considerably less than $2d^2/\lambda$, where d is the diameter of the source antenna" and λ is the frequency of operation. Thus, phase variation across the AUT can be determined by "assuming that the phase front at the test antenna is a sphere." It further states that an AUT of diameter D and separated by a distance R from a source antenna will have a phase variation of

$$\triangle\phi \approx \frac{\pi D^2}{4\lambda R} \tag{5.1}$$

as shown in [66][52]. The minimum allowable separation between source and AUT restricts $\triangle\phi$ to be less than $\pi/8$ (i.e. 22.5°)[51][52]. This results in the well known far-field distance criterion of $R \geq 2D^2/\lambda$ which is used in many textbooks and far-field measurement systems [51][52][43][41][46][49]. Thus, the distance between the source antenna and AUT only depends on the AUT diameter and the frequency of operation. Balanis [51] on page 1002 illustrates this concept as seen in Figure 5.2.

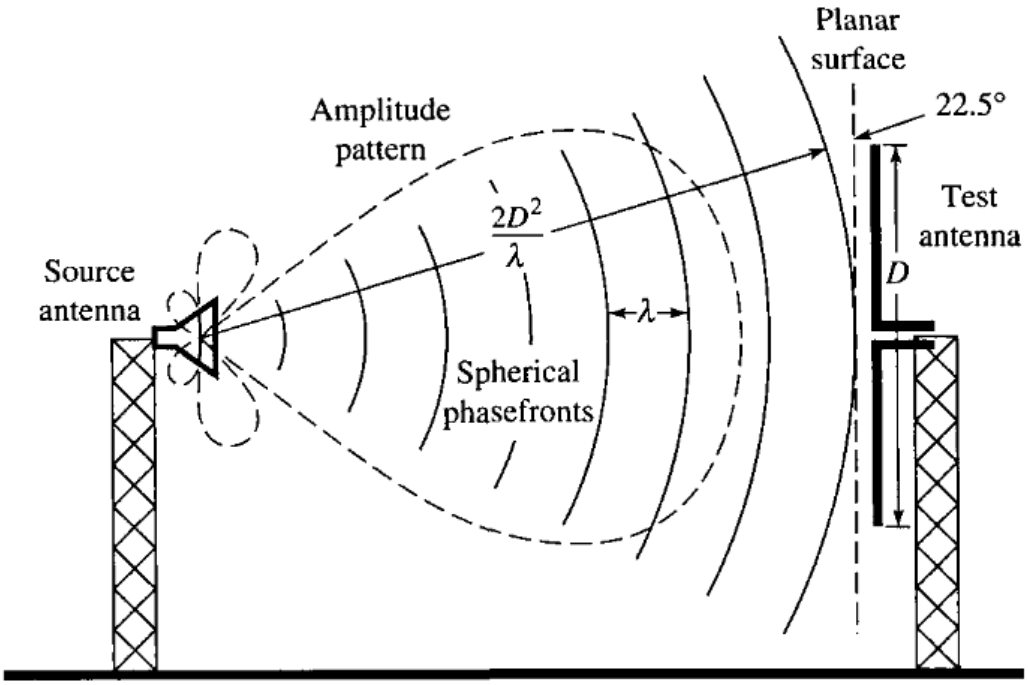

Figure 5.2: Figure depicting the minimum separation distance $R \geq 2D^2/\lambda$ between source antenna and AUT. The AUT diameter D and wavelength of operation λ determine the phase variation seen across the surface of the AUT. Thus, the size of the AUT determines the separation distance.

To help with measuring antenna radiation patterns, the polar coordi-

nate system as seen in Figure 5.3 from [50] is typically used in which theta (θ) represents the angle from the Z-axis at 0° to the XY-plane at +90° and phi (ϕ) represents the angle within the XY-plane starting from the X-axis at 0° and rotating counter clockwise towards the Y-axis at +90° [50]. The polar coordinate system also helps indicate the type of electric field polarization (i.e. E_θ or E_ϕ) being transmitted by the source antenna and illuminating the AUT.

Several methods can be used to determine the antenna gain of the AUT. Each method relies on the Friis transmission formula (see Equation 5.2) where antenna gain of a receiver antenna (G_r) can be calculated if the received power (P_r), transmitted power (P_t), transmitter antenna gain (G_t), and measurement distance(R) are known [50][51][56].

$$P_r = P_t G_t G_r (\frac{\lambda}{4\pi R})^2 \tag{5.2}$$

The first method to measure antenna gain is called the "two antenna method" in which two identical antennas of unknown gain are pointed toward each other at boresight and measured in a free-space environment. Since the antennas are identical, their gains are identical (i.e. $G_t = G_r$) and Equation 5.2 can be solved since all other variables are known. If the two antennas are not identical, a third antenna is needed which is called the "three antenna method" in which case three antennas each with unknown gain can be measured in a free-space measurement test. Three measurements are required for each possible combination of antennas. This produces a system of equations

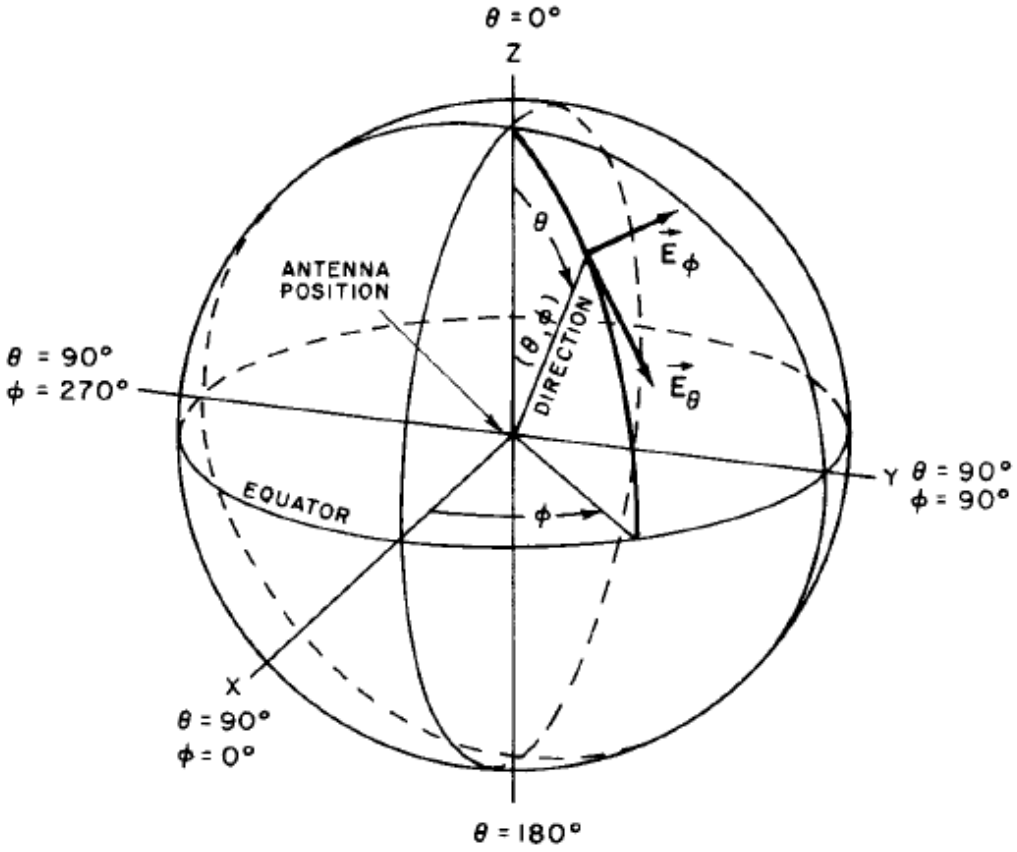

Figure 5.3: The standard polar coordinate system using theta (θ) and phi (ϕ) to represent angles is commonly used in antenna measurement systems. The theta/phi designation also helps to specify the polarization of the electric field (i.e. E_θ or E_ϕ).

containing three Friis transmission equations with three unknowns, which can be solved to calculate the gain of all three antennas. The most commonly used method to measure the gain of an AUT is called the "gain transfer method" where the AUT is replaced with an antenna of known gain such as a standard horn antenna. The received power measured by the standard horn antenna is subtracted from the received power measured by the AUT. This difference is then added to the known antenna gain of the standard horn antenna which computes the AUT antenna gain[50][51].

For the on-chip antenna measurement system, the source antenna gain is first calculated by using either the "two-antenna method" or "gain transfer method". Once the transmitter antenna gain is known, Equation 5.2 is used to compute the gain of the on-chip antenna. Note that Equation 5.2 relies on a free-space measurement test which requires a reflection-less environment. For the on-chip measurement system, RF absorbing material (Eccosorb HR-25/ML) was used extensively to cover reflective objects in the probe station environment. This material has excellent attenuation properties and has been tested to attenuate reflections by at least 50 dB at microwave and millimeter-wave frequencies.

5.2 Design of the Sub-Terahertz Antenna Measurement System

The sub-terahertz on-chip antenna measurement system uses a Cascade Microtech probe station, a Cascade Microtech GSG RF probe (Infinity

I220-T-GSG-75-BT), a Rohde & Schwarz ZVA-67 VNA which connects to two ZVA-Z220 WR-5 140 GHz to 220 GHz frequency converters, a Rohde & Schwarz ZV-WR05 waveguide calibration kit, a Cascade Microtech Impedance Standard Substrate (ISS) 138-356, and Eccosorb RF absorber material. The VNA provides S-parameter measurements (particularly S_{21}) which can be used to determine the radiation pattern and gain of an on-chip antenna. A block diagram of the electrical equipment and interconnections is shown in Figure 5.4. Figure 5.5 shows a picture of the equipment with a simplified diagram of the system.

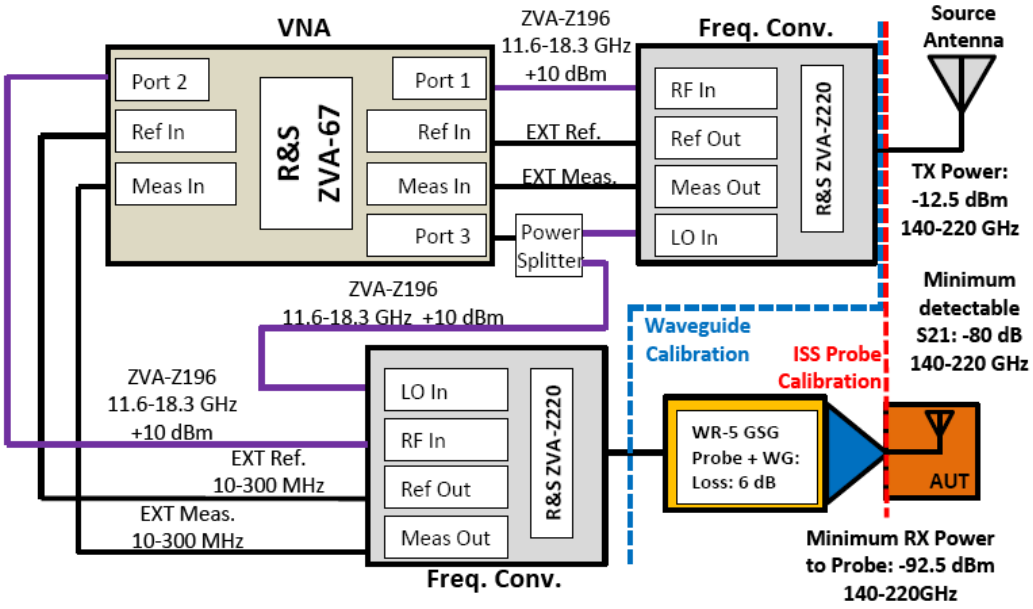

Figure 5.4: A block diagram showing the sub-terahertz antenna measurement equipment. A Rohde & Schwarz VNA measures S-parameters from 140 GHz to 220 GHz which are used to measure the radiation pattern and gain of the on-chip AUT.

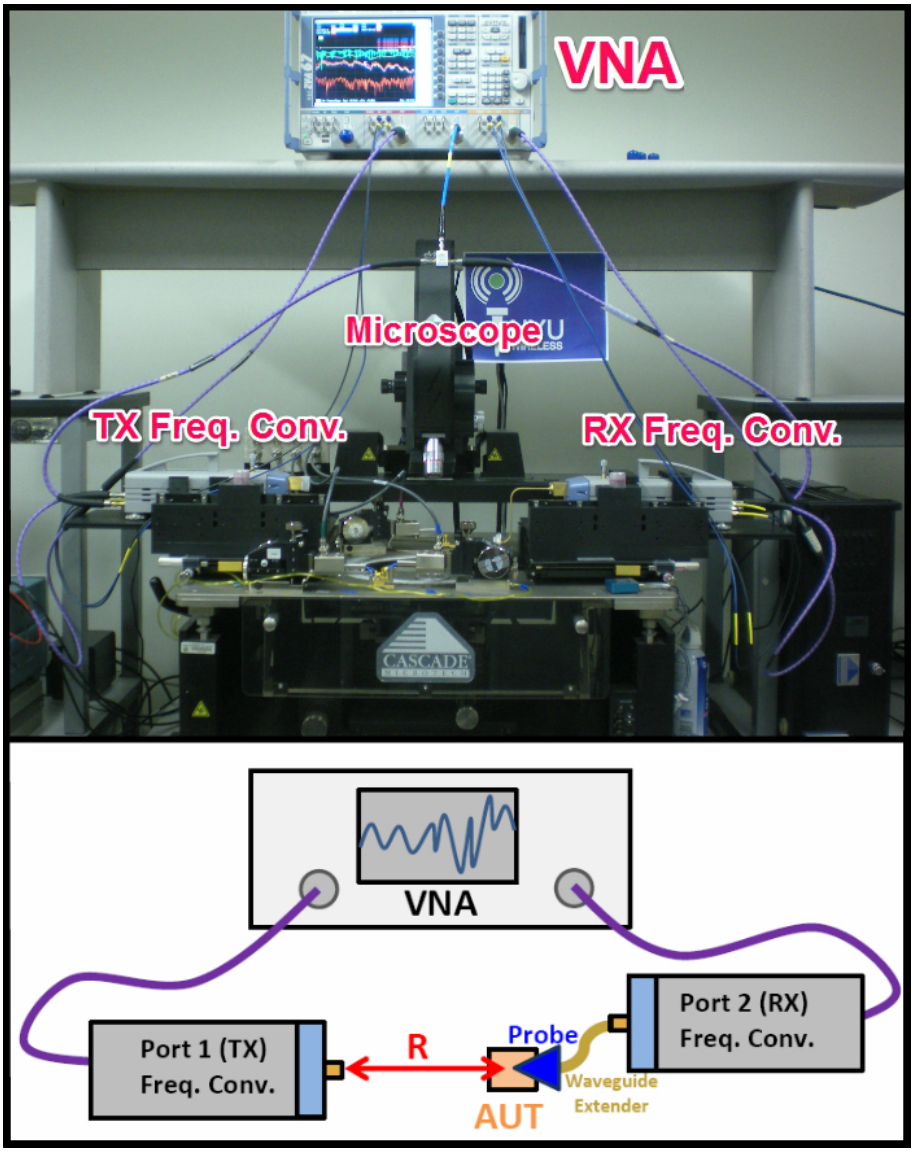

Figure 5.5: A picture and simplified diagram of the sub-terahertz antenna measurement system in a wafer probe station. The Rohde & Schwarz VNA connects to the frequency converters using coaxial cables. The overhanging microscope is used for proper probing of the GSG RF probe onto the on-chip AUT (not shown).

Port 1 of the VNA connects to one of the ZVA-Z220 frequency converters using coaxial cables labeled as "ZVA-Z196," "EXT Ref," and "EXT Meas" as seen in Figure 5.4. The frequency converter upconverters/downconverts signals from 11.6-18.3 GHz to the WR-5 frequency band of 140 GHz to 220 GHz. Port 1 is designated as the transmitter of the antenna measurement system and thus, this frequency converter will be moveable and pointed towards the on-chip antenna during testing. At maximum power, the ZVA-Z220 will output -12.5 dBm of power at the WR-5 frequency band of 140 GHz - 220 GHz through a WR-5 rectangular waveguide and UG-385 flange. The frequency converter and test port head can be seen in Figure 5.6.

Port 2 of the VNA connects to the other ZVA-Z220 frequency converter using coaxial cables as seen in Figure 5.4 and will act as a receiver. This frequency converter will attach to the GSG RF probe through a WR-5 waveguide extension and must remain in a fixed position on the wafer probe station. The GSG RF probe will probe the on-chip antenna at the center of the probe station as seen in Figure 5.7.

Prior to attaching the RF probe and measuring the antenna, calibration must first be performed to move the measurement plane of the VNA to the AUT. Two calibration routines are actually performed: first a waveguide calibration followed by an ISS probe calibration. As seen in Figure 5.4 as a dotted blue line, the first calibration is a waveguide calibration which only involves the two frequency converters and the WR05 calibration kit (i.e. the measurement plane is moved to the blue line and the VNA measures to the

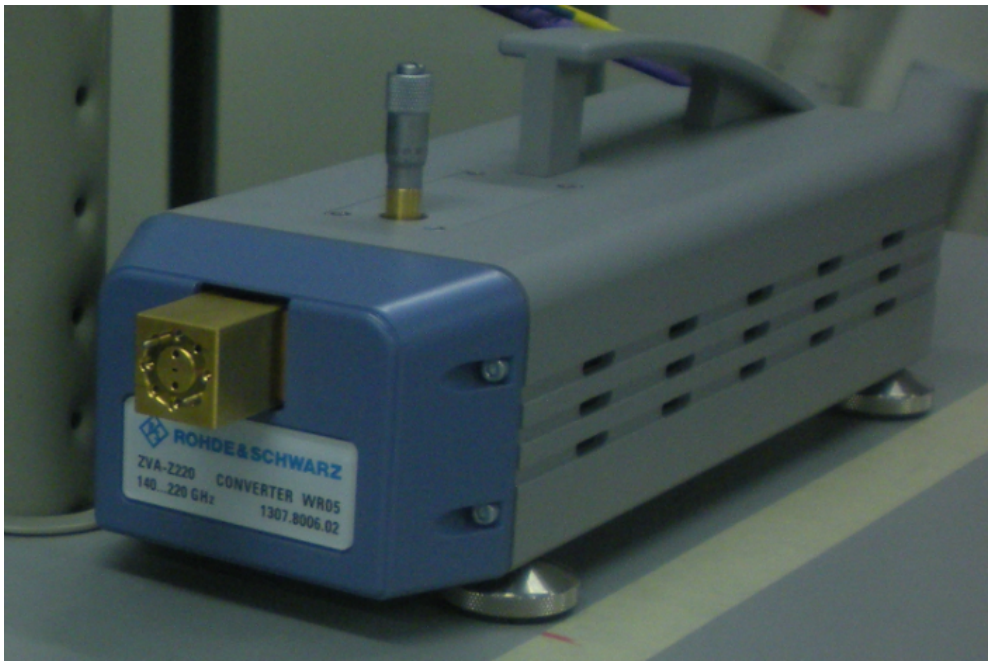

Figure 5.6: One of the Rohde & Schwarz ZVA-Z220 frequency converters which outputs a frequency of 140 GHz to 220 GHz at -12.5 dBm of power. The output port is a WR-5 waveguide with UG-385 flange.

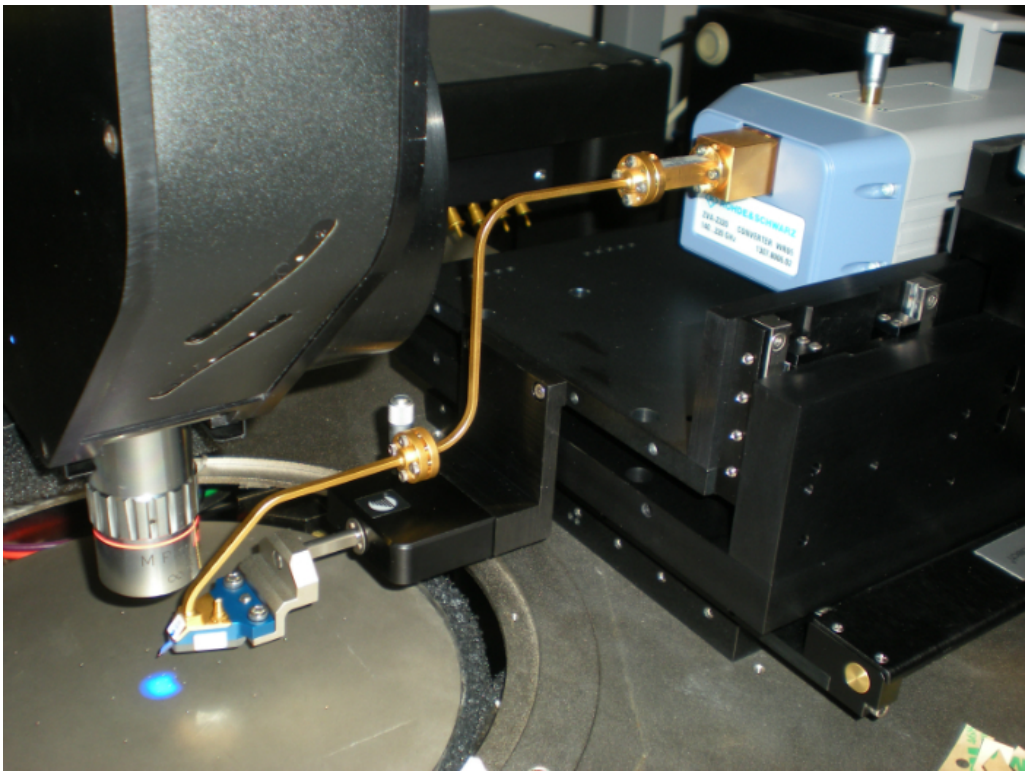

Figure 5.7: A picture of the Rohde & Schwarz ZVA-Z220 frequency converter connected to the GSG RF probe. The probe will receive energy from the on-chip antenna at 140-220 GHz.

right of the blue line). This R&S WR05 calibration kit as seen in Figure 5.8 provides a short, match, and shim to perform a TOSM (Thru, Open, Short, and Match) calibration and moves the measurement plane of the VNA to the test port heads of the frequency converters (marked as a dotted blue line in Figure 5.4).

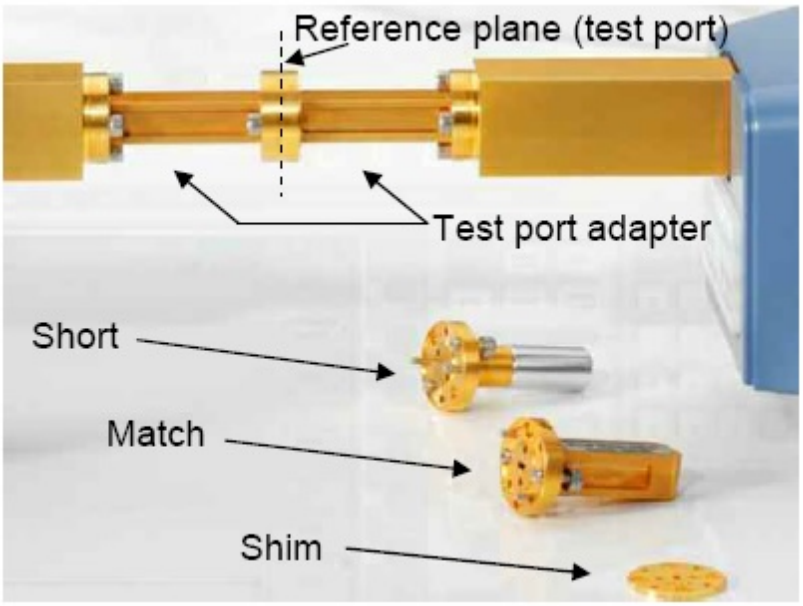

Figure 5.8: The Rohde & Schwarz WR05 calibration kit containing a short, match, and shim. This calibration routine will move the measurement plane of the VNA to the ends of the frequency converters.

After the waveguide calibration, the frequency converter on Port 2 is attached to the RF probe and a 2nd tier 1-Port SOL calibration is performed which further moves the measurement plane to the tip of the Cascade Microtech GSG RF probe (seen as the red dotted line in Figure 5.4). A Cascade Microtech Impedance Standard Substrate (ISS 138-356) containing a short,

open, and 50 Ω load standard is used to perform a 1-port SOL calibration routine.

Once calibrated, the system is ready to perform antenna measurements. Using an IF bandwidth of 1 KHz, and a maximum output power of -12.5 dBm, the dynamic range of the system is 80 dB with a minimum detectable power of -92.5 dBm at the tip of the RF probe. A link budget analysis was used to calculate the link margin available to measure the on-chip antenna given R (i.e. the TX-RX separation distance). Additionally, a sensitivity analysis was also performed to determine the tolerable deviation of R (i.e. ΔR) in order to maintain a nearly constant amplitude plane wave at the AUT. Recall that the minimum separation distance between source antenna and AUT in a far-field antenna measurement system is $2D^2/\lambda$ where D is the largest dimension of the AUT and λ is the wavelength of operation. The size of the largest AUT (i.e. the on-chip antenna array) was 1433.33 μm, and the smallest wavelength to be tested (i.e. 220 GHz) was 1.36 mm, thus the minimum separation distance is 3.02 mm. This separation distance is very small compared to traditional antenna measurements at lower frequencies such as 900 MHz. While a small R provides large link margins by reducing free space path loss, ΔR dramatically decreases to maintain a nearly constant amplitude plane wave at the AUT. To determine ΔR at different R, simply use Friis transmission formula (Eqn. 5.2) and vary P_r by $\pm$ 0.25 dBm. For example, when $R = 3$ mm at 180 GHz, $\Delta R = \pm$ 8.51 μm (i.e. the frequency converter must not deviate radially by more than $\pm$ 8.51 μm) to maintain a

plane wave at the AUT with amplitude variation less than $\pm$ 0.25 dB. The requirement of $\Delta R = \pm$ 8.51 μm is physically infeasible without expensive precision positioning equipment. Larger separation distances relax the ΔR requirement. For example, when R = 19 cm instead of 3 mm, ΔR increases to $\pm$ 5.4 mm which is much more physically feasible. The drawback of setting R = 19 cm is more free space path loss (i.e. 63.1 dB at 180 GHz) which attenuates the transmitted signal and provides less incident power ($\approx$ -75 dBm) to the AUT. It is likely that the received power at the RF probe is barely detectable by the VNA when considering R = 19 cm, a transmitted power of -12.5 dBm, and an AUT with negative antenna gain. To compensate for a larger R with larger path loss, a standard gain horn antenna (A-INFOMW JXTXLB-15-25-C-1.85F) was connected to the transmitter as seen in Figure 5.9.

While this horn antenna was designed to be operated at the WR-15 frequency band of 50-75 GHz, antenna measurements showed a nearly flat antenna gain of $\approx$ 25 dBi around 180 GHz. The horn antenna gain was measured using the frequency converters separated by 19 cm and using the VNA to measure the increase in received power. One additional benefit to using a narrow beamwidth source antenna (as stated in [50]) is to reduce any received multipath reflections from the test environment and thus reduce measurement error. As stated in [50] p. 7, "the use of broader beamwidth source antennas usually results in an increased error due to the reflections." However, with a narrower beamwidth, the alignment of the source antenna becomes more crit-

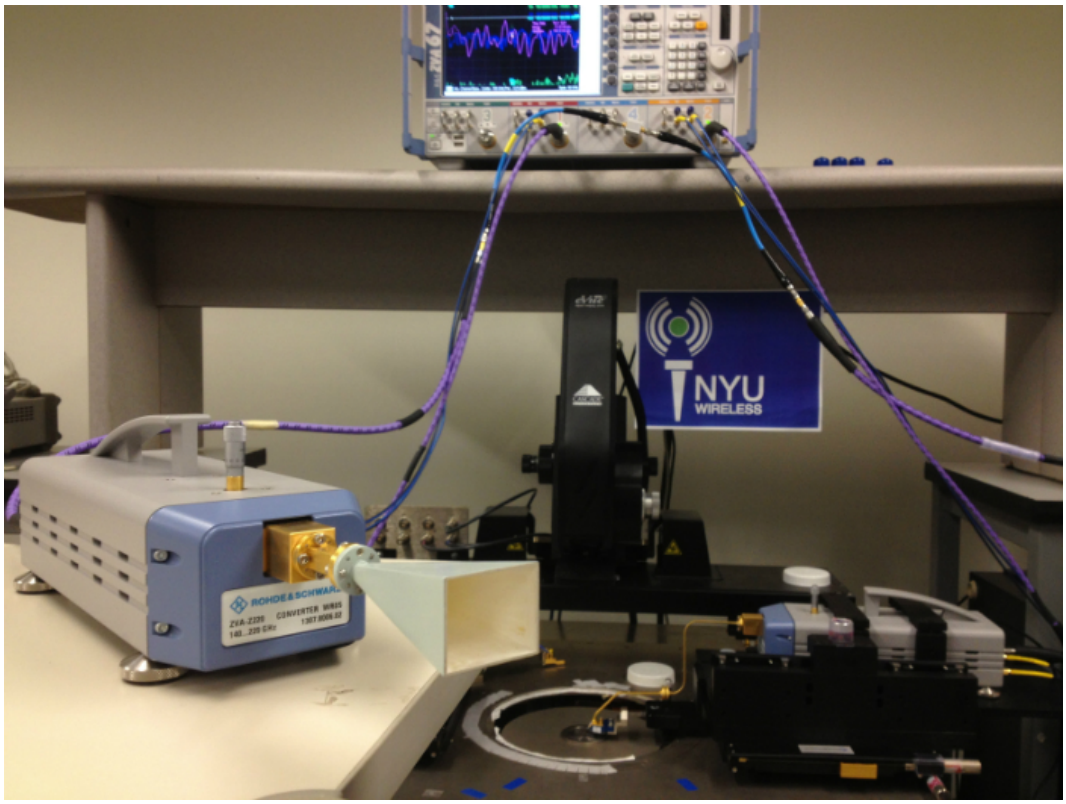

Figure 5.9: The sub-terahertz antenna measurement system with the attached horn antenna (25 dBi at 180 GHz) on the transmitter. The horn is needed to compensate for additional path loss at 140 GHz to 220 GHz.

ical and "care shall be exercised in orienting the source antenna so that the peak of its beam is centered on the test antenna." Given the high gain of the horn, one possible cause for concern is radiating near-field components that could still be present at the AUT as is the case in any far-field measurement system [50], p. 93. However, as stated in [52] on pages 375 and 469-470, the radiating near field from an antenna's aperture "approximates a nearly uniform plane wave, as conceptualized by Fig. G-1 of Appendix G. Existence of this approximation to a plane-wave field permits, for antennas within this radiating near-field, the measurement of far-field patterns within a compact range." In other words, a uniform plane wave approximation still exists and will be incident on the AUT if the AUT happens to be within the radiating near field. The source antenna is still radiating a spherical wave [50] p. 8, and since the source antenna is located in the far-field of the AUT, a uniform plane wave approximation can be assumed across the small on-chip aperture ($\approx 1.5mm \times 1.5mm$) and a valid far-field measurement can be conducted.

With the addition of the horn antenna, the transmitted power is $\approx$ +12.5 dBm, and at 19 cm (measured from the neck of the horn to the AUT), the incident power at the AUT is -50.62 dBm at 180 GHz. The dynamic range of the system increases to 105 dB and the link margin to measure an on-chip antenna is increased to 42 dB. Thus, if an on-chip antenna were to have a gain of -20 dBi, sidelobe levels up to -22 dB below boresight can still be measured.

Maintaining a constant R can be challenging especially when ΔR should be less than $\pm$5.4 mm. If a researcher is physically holding the frequency

converter as is done in this measurement system, the VNA can help the researcher maintain a nearly consistent and constant R by using the S_{21} group delay trace. The group delay trace provides a time delay trace between signal launch and signal received. If a user should maintain a constant R with variation no more than $\pm$ 5.4 mm, then the group delay trace should not fluctuate by more than $\pm$ 17.7 picoseconds. Thus, the researcher can adjust the radius of the frequency converter in real-time as the group delay trace updates on the VNA. Maintaining a constant pointing angle is also important. This requires attaching an accurate protractor to the frequency converter with constant monitoring. If a researcher is physically orienting and pointing the TX frequency converter towards the AUT, there will likely be small pointing angle offsets which create errors since boresight is not pointed towards the AUT. To overcome this problem, the VNA "Max Hold" function is used. When the "Max Hold" function is enabled, the current measurement trace will be stored to temporary memory. If an updated measurement trace contains frequency points with stronger power (e.g. higher S_{21}) compared to the stored trace in memory, the higher power value overwrites the memory trace only at those specific frequency points. If the updated measurement trace has a lower power level than memory, the memory trace remains unchanged. Thus, only the strongest power values are saved at each frequency point and the memory trace will monotonically increase to a steady level and never decrease until the memory is reset by the user. This helps to remove any pointing error offsets since the researcher can now physically sweep the pointing angle of the fre-

quency converter across the AUT knowing that the most powerful signal (i.e. the highest S_{21}) is received and saved when boresight points directly to the AUT.

The antenna measurement system should be designed to measure both linearly co-polarized and cross-polarized radiation patterns by illuminating the AUT with two orthogonal linear polarizations. By default, the frequency converters transmit a linearly polarized electric field as seen in Figure 5.10. If the frequency converter is placed upright on a flat surface, the transmitted electric field would appear as vertically polarized and the AUT can be illuminated with this polarization. To transmit the orthogonal (i.e. horizontal) polarization, simply rotate the frequency converter to its side as seen in Figure 5.10 and repeat the pattern measurement.

A coordinate system for the chip/probe station was established to correlate pattern measurements with the physical antenna and environment as suggested in Figure 5.3. As seen in Figure 5.11, the XY-plane represents the ground plane of the probe station that is parallel to the wafer stage and the Z-axis points toward the ceiling (i.e. the zenith). This same coordinate system was used for the on-chip antenna when being probed on the probe station as seen in Figure 5.12. The X-axis is pointed the right of the probe station, and the Y-axis is pointed towards the rear of the probe station. Thus, theta (θ) is the angle measured from the Z-axis toward the XY-plane, and phi (ϕ) is the angle measured within the XY-plane starting with the X-axis as 0° and the Y-axis as $+90^\circ$. For elevation pattern cuts along the YZ-plane, positive

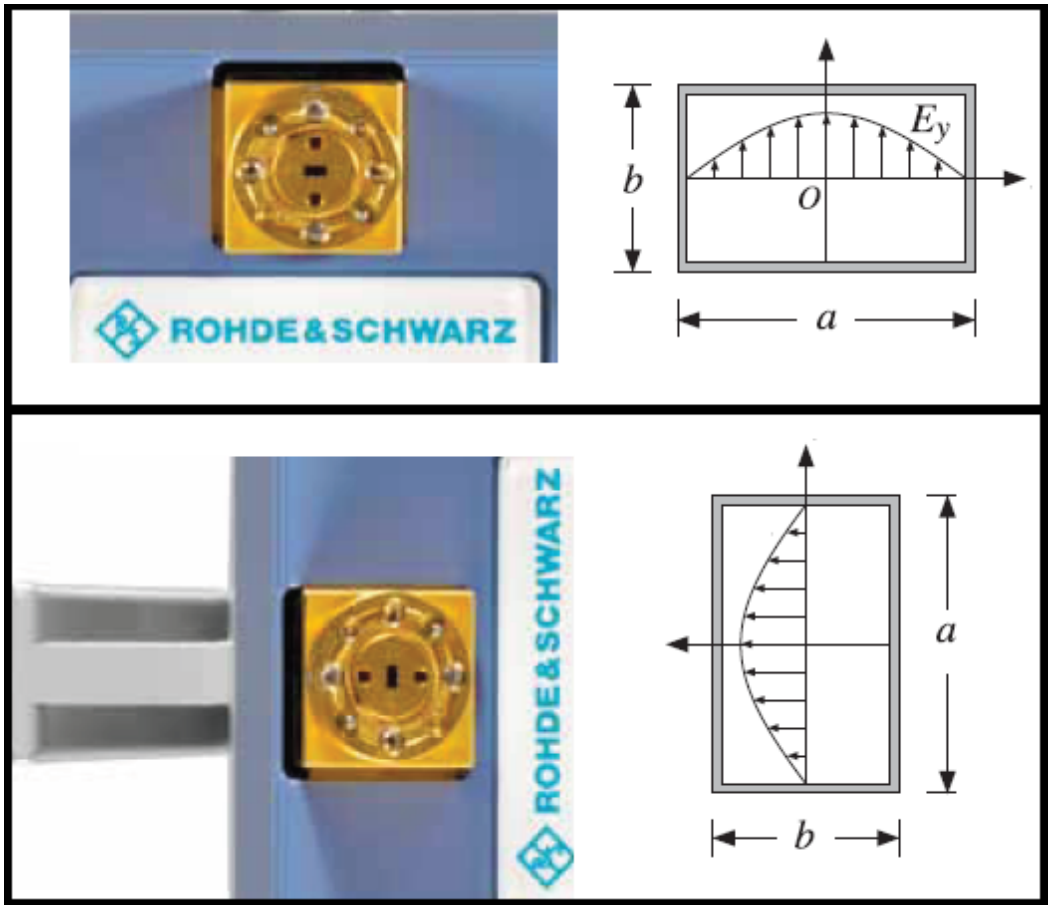

Figure 5.10: The ZVA-Z220 frequency converters transmit a linearly polarized electric field (i.e. a vertical polarization seen in the top figure). To transmit an orthogonal polarization (i.e. horizontal polarization seen in the bottom figure), simply rotate the frequency converter by 90°.

theta is the angle towards the user, and negative theta is towards the probe station. For elevation pattern cuts along the XZ-plane, positive theta is the angle towards the left of the user, and negative theta is towards the right of the user. This same coordinate system is used to specify the polarization of the transmitted field. For example, if the user is holding the frequency converter upright and pointed in parallel to the Y-axis, this would correspond to theta-polarization. If the frequency converter is rotated 90° and placed on its side to illuminate horizontal polarization, this would correspond to phi-polarization.

It is also necessary to specify different radiation pattern cuts such as the E-plane cut and the H-plane cut. Based upon the on-chip antenna simulations, the boresight of the patch antenna array should point upwards towards the Z-axis. Also, the patch antenna array is simulated to be linearly polarized with the electric field aligning with the Y-axis direction. Thus, the E-plane radiation cut for the on-chip patch antenna array is designated as the plane that contains both the Y-axis and Z-axis (i.e. the YZ-plane). The H-plane radiation cut for the on-chip patch antenna array is then designated as the plane that contains the X-axis and the Z-axis (i.e. the XZ-plane). Note that the E-plane and H-plane are with respect to the AUT orientation, thus, antennas that are rotated compared to the on-chip patch antenna array will have different E-plane and H-plane orientations.

A protractor was mounted on the TX frequency converter to measure the pointing angle towards the AUT. Measurements can be conducted at any angular step the user desires to accurately sample the radiation pattern; how-

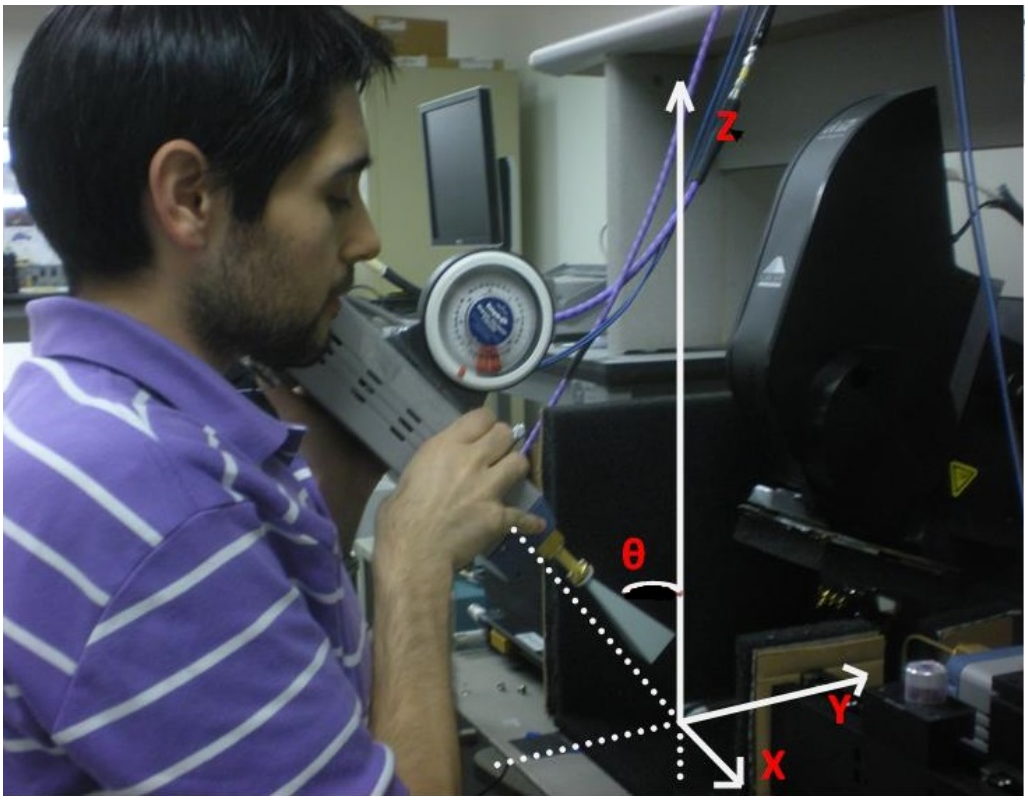

Figure 5.11: An coordinate system was established for the probe station and chip environment. The Z-axis points directly upward toward zenith while the X-Y plane represents the ground plane of the wafer stage. Theta and phi which represent the polar coordinates are also used to help relate radiation measurements and polarizations to the physical environment.

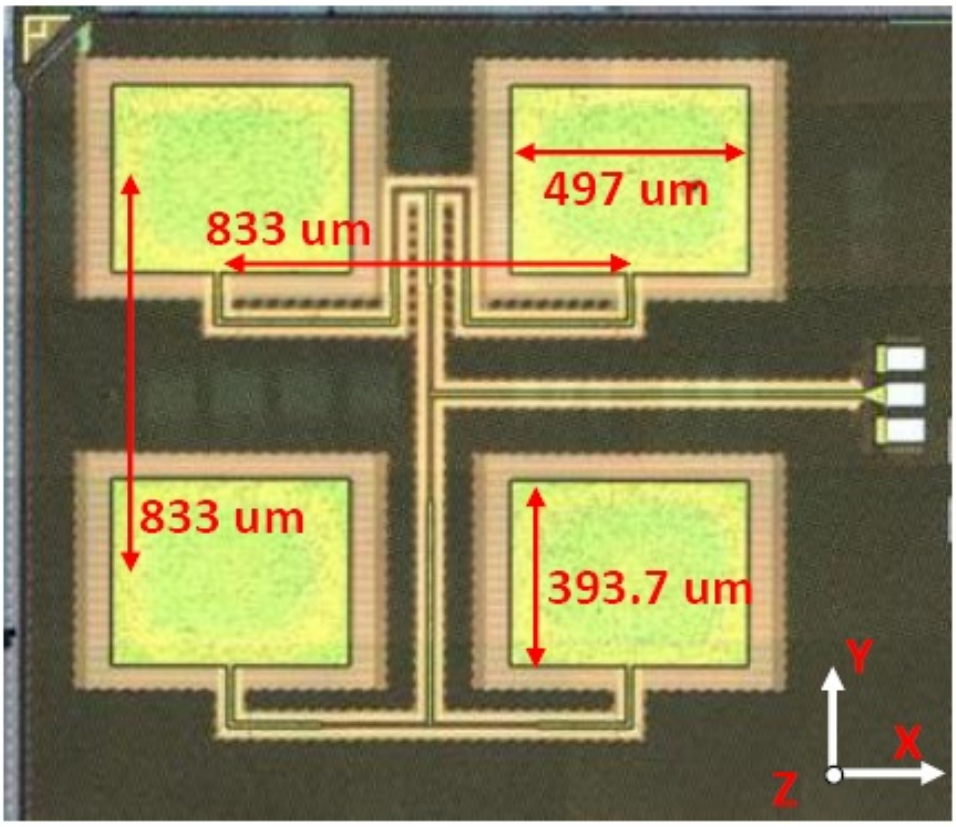

Figure 5.12: The on-chip AUT also uses the same coordinate system established for the probe station.

ever, given that the AUT is simulated to have a half-power beamwidth of 56°, a 10° angular step was more than sufficient to capture the radiation pattern. The overhanging microscope limits the elevation range of measurements from 20° to 70° and prevents the boresight measurement at 0°; however, removing the microscope (once proper probing has been verified) increases the measurement range in both E-plane and H-plane from −20° to 70° including the boresight measurement.

To reduce multipath reflections in the test environment, RF absorbing material was applied to nearly all metallic surfaces and objects on the probe station as seen in Figure 5.13. The AUT was placed on a Cascade Microtech rigid microwave absorber which is normally used during the ISS calibration to reduce substrate modes. A vacuum pump holds down the chip to the rigid microwave absorber while the RF probe touches down. The rigid absorber can be seen in Figure 5.13 as well as earlier in the chapter in Figure 5.1.

5.3 Testing Procedure of the Antenna Measurement System

This section provides a simplified procedure to measure on-chip antenna radiation patterns. The first step is to prepare the VNA for the measurement such as frequency span, number of frequency points, IF bandwidth, transmit power, etc. Once the VNA has the correct settings, perform a TOSM waveguide calibration using the frequency converters. The VNA provides a step-by-step procedure to perform the TOSM calibration. Once the frequency

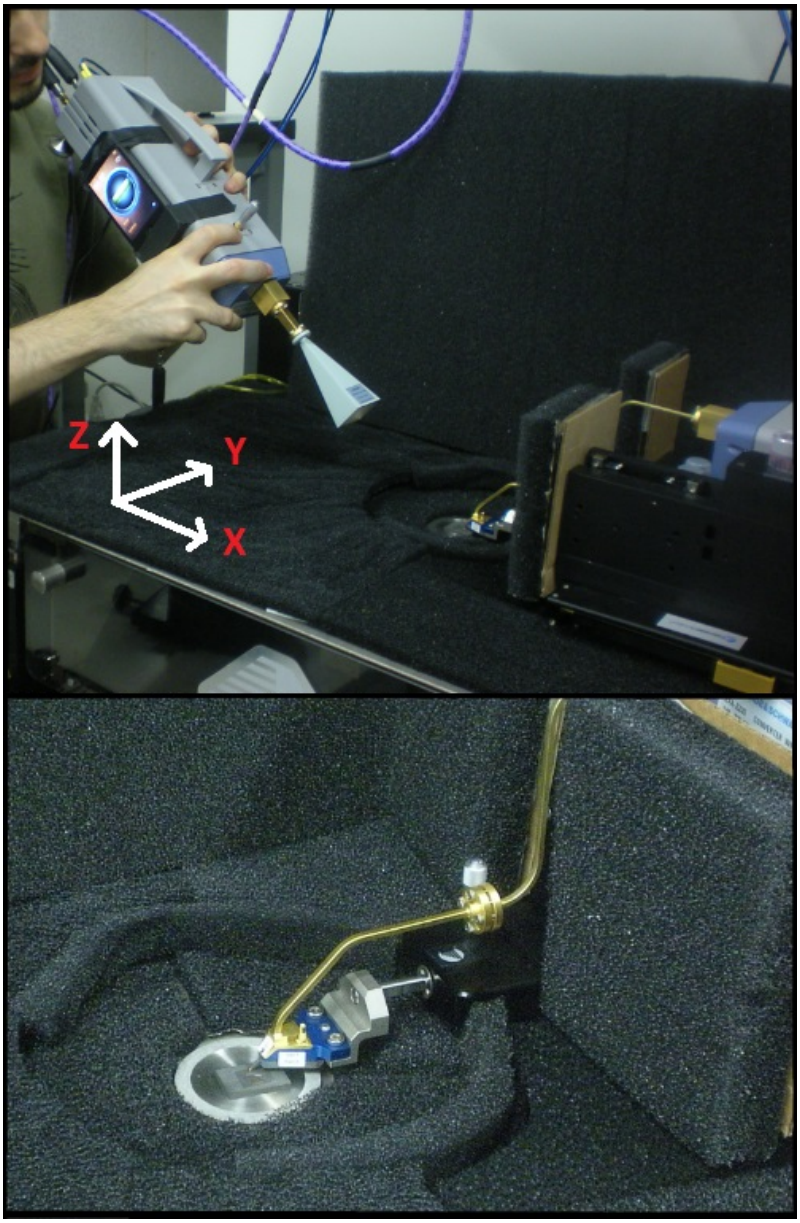

Figure 5.13: RF absorber material seen as black spongy sheets was added to all surfaces in the antenna measurement system to reduce multipath reflections. The on-chip AUT was placed on a Cascade Microtech rigid microwave absorber and probed using the GSG RF probe.

converters are calibrated, move the Port 2 frequency converter to the probe station and secure it to the wide-area positioner. Attach the GSG RF probe to the frequency converter and begin a 2nd tier 1-port SOL probe calibration. This calibration first requires planarizing the RF probe using the "Contact Substrate" provided by Cascade Microtech, followed by measuring the ISS. Cascade Microtech's WinCal XE software provides a step-by-step procedure to calibrate to the probe tip. Once calibrated to the tip of the RF probe, replace the ISS with the AUT in the center of the probe station. Apply any RF absorber material to the probe station environment as needed. Using the microscope, probe down on the AUT probe pads. Use a recommended skate of 25 μm. The miniature ruler as seen in Figure 4.11 provides help for accurate probing and skate. Record the S_{22} of the AUT and save the trace to the VNA memory. Lift the RF probe from the AUT using the platen arm. Proceed to remove the microscope as carefully as possible. It is important to NOT remove the microscope if the RF probe is still contacting the AUT as any small vibration during removal will damage the sensitive RF probe and/or AUT. Once the microscope is removed, re-probe the AUT again using the platen arm and verify that S_{22} has not changed by comparing the new trace to the trace stored in memory. If the S_{22} has changed, lift the RF probe, reattach the microscope, and re-align the RF probe to the AUT probe pad. If the S_{22} has not changed, then prepare the Port 1 frequency converter by attaching a source antenna and protractor. It is very important to not bump or rest the frequency converter against the probe station while the RF probe is contacting

the AUT as any small vibration or mechanical offset on the probe station will overdrive the RF probe beyond its safe limits and damage the probe and/or AUT. The Port 1 frequency converter can now begin the measurement sweep and be positioned at different angular positions (i.e. $[\theta,\phi]$). To maintain a constant R, the user should monitor the S_{21} group delay trace carefully and re-adjust the frequency converter radially to maintain a constant time delay. At each angular position, record the S_{21}. The S_{21} trace can be saved as a standard *.SnP file or a *.csv file. To ensure boresight hits the AUT aperture, enable the VNA "Max Hold" function and slightly sweep the pointing angle across the AUT. Note that when "Max Hold" is enabled, phase information is lost and only magnitude is saved as a *.csv file. To illuminate the AUT with a different polarization, simply rotate the frequency converter as seen in Figure 5.10. To calculate the antenna gain of the AUT, use the boresight S_{21} for Equation 5.2 (i.e. $|S_{21}|^2 = P_r/P_t$).

Several environmental tests were conducted beyond the measurement of the on-chip AUTs. The first environmental test helps determine how much interference the RF probe creates when measuring an AUT. Instead of probing an AUT, the RF probe contacts a precision 50 Ω load using the ISS. The radiation pattern from this test determines how much the RF probe interferes when probing a well-matched antenna. The second environmental test places a DC probe adjacent to the patch antenna array to determine how much interference a nearby probe creates. The DC probe is placed near the chip's edge where DC pads are normally located and used for testing. If digital circuits

were to be tested in conjunction with antenna measurements on a single chip (see Figure 5.1 as an example), it is important to know how much interference adjacent probes create. The last environmental test determines the effect of RF absorbing material on the accuracy of the radiation pattern measurements. Back-to-back on-chip antenna radiation pattern measurements are conducted with and without RF absorbing material present in the environment. This test determines the importance of using RF absorbing material in a probe station environment. All environmental test results are presented in the next chapter.

Chapter 6

On-Chip Antenna Measurements, Radiation Patterns, and Analysis

This chapter presents and analyzes the results of the sub-terahertz on-chip patch antenna measurements such as return loss, bandwidth, impedance, radiation patterns, gain, directivity, and radiation efficiency. Both a single patch antenna as well as the patch antenna array fabricated on 45 nm CMOS SOI are measured and analyzed. As stated in the previous chapters, all measurements are conducted in a standard wafer probe station environment. In addition, the impact on radiation patterns from the RF probe, an adjacent DC probe, and the use of RF absorbing material is also investigated in this chapter.

6.1 Single Patch Antenna Performance

The first AUT is the on-chip single patch antenna and is measured using the Cascade Microtech wafer probe station and antenna measurement system. The patch antenna is probed using a standard Cascade Microtech RF probe (Infinity I220-T-GSG-75-BT). An RF probe calibration is performed prior to measuring the on-chip patch antenna using a Cascade Microtech Impedance

Standard Substrate (ISS 138-356) and a 1-port SOL calibration routine. The return loss (S_{11}) of the AUT is measured with a frequency sweep over the entire WR-5 band (140 GHz to 220 GHz). Figure 6.1 shows a microscope image of the single patch antenna being probed, and Figure 6.2 compares the measured and simulated return loss. The simulated S_{11} of the patch antenna has a center frequency of 178.2 GHz and a bandwidth ($S_{11} < -10dB$) of 3.64 GHz (i.e. 2.04% of the simulated carrier frequency) from 176.38 GHz to 180.02 GHz. The measured S_{11} of the patch antenna has a slightly lower center frequency but larger bandwidth compared to simulation. The measured patch has a center frequency of 172.4 GHz and a bandwidth ($S_{11} < -10dB$) of 4.34 GHz (i.e. 2.52% of the measured carrier frequency) from 169.86 GHz to 174.2 GHz. To make a fair comparison between measured and simulated data, simulations are performed at the ideal simulated resonant frequency of 178.2 GHz, while all measurement analysis is performed at the ideal measured resonant frequency of 172.4 GHz.

Using the complex return loss data (both magnitude and phase data of S_{11}), the measured impedance of the patch antenna can be calculated using standard $StoZ$ transformation equations such as those in [63] or using software such as Cascade Microtech's WinCal XE. The Rohde & Schwarz VNA also has the capability of displaying the measured Z-parameters directly. Figure 6.3 shows the impedance of the simulated and measured patch antenna across the 140 GHz to 220 GHz frequency band. The simulated impedance of the patch antenna at its center frequency of 178.2 GHz was 42.12+j2.06 ohms. The

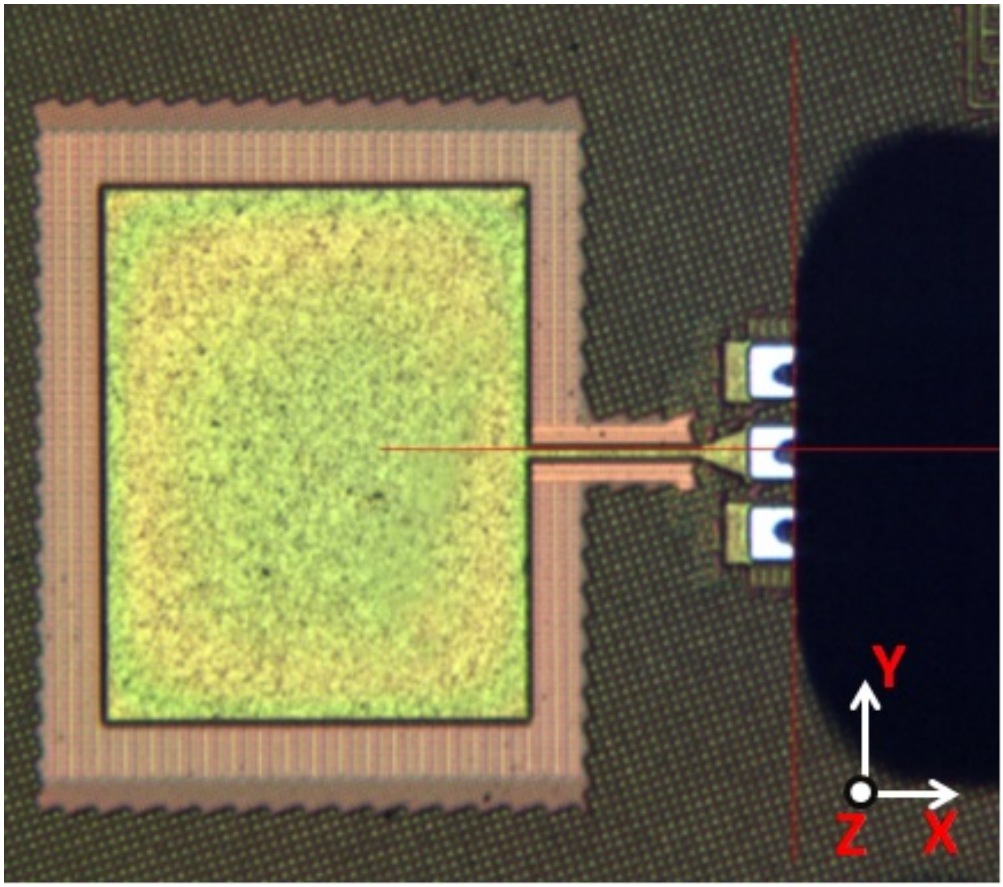

Figure 6.1: Microscope image of the single patch antenna being probed by a Cascade Microtech RF probe (Infinity I220-T-GSG-75-BT). An SOL calibration routine was preformed prior to probing which moves the VNA measurement plane to the tip of the RF probe.

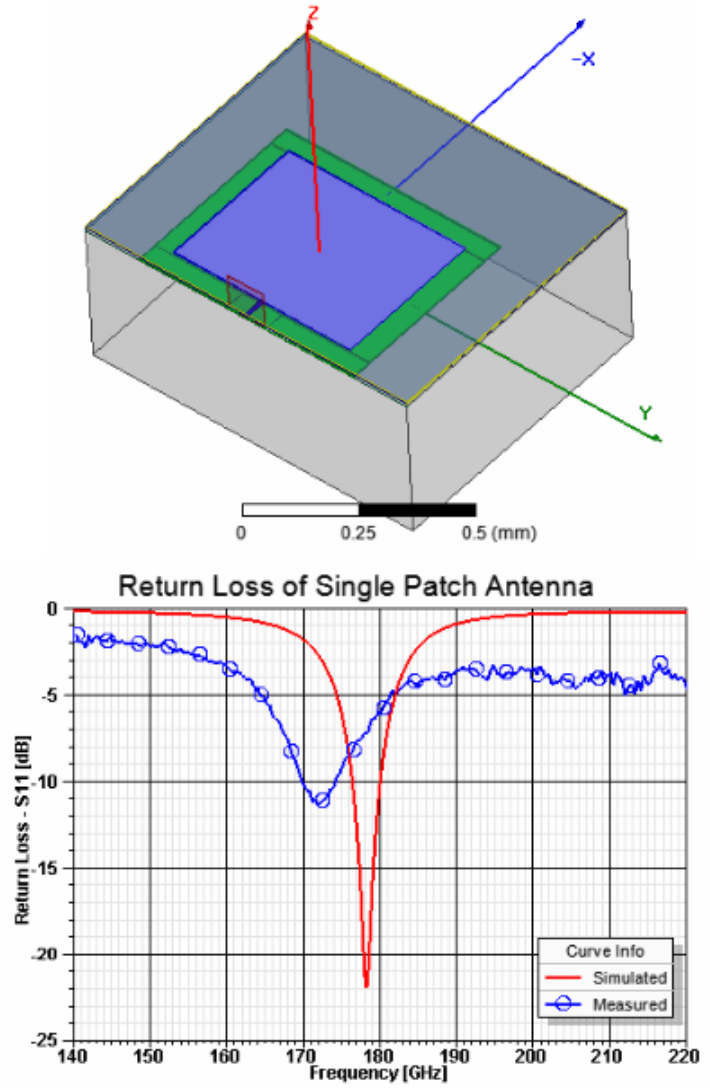

Figure 6.2: The return loss (S_{11}) of the on-chip single patch antenna over the WR-5 frequency band. The simulated patch has a center frequency of 178.2 GHz with 3.64 GHz of bandwidth (i.e. 2.04% bandwidth of the carrier frequency) below -10 dB S_{11}. The measured patch has a center frequency of 172.4 GHz with 4.34 GHz of bandwidth (i.e. 2.52% bandwidth of the carrier frequency) below -10 dB S_{11}.

measured impedance of the antenna at its center frequency of 172.4 GHz was 40.02-j23.82 ohms. The peak resistance of both the measured and simulated patch antenna match very well and are close to the desired 50 Ω impedance. The measured antenna has a lower reactance than simulation; however, the inflection point of the reactance (≈ 176-178 GHz) matches very well between simulation and measurement.

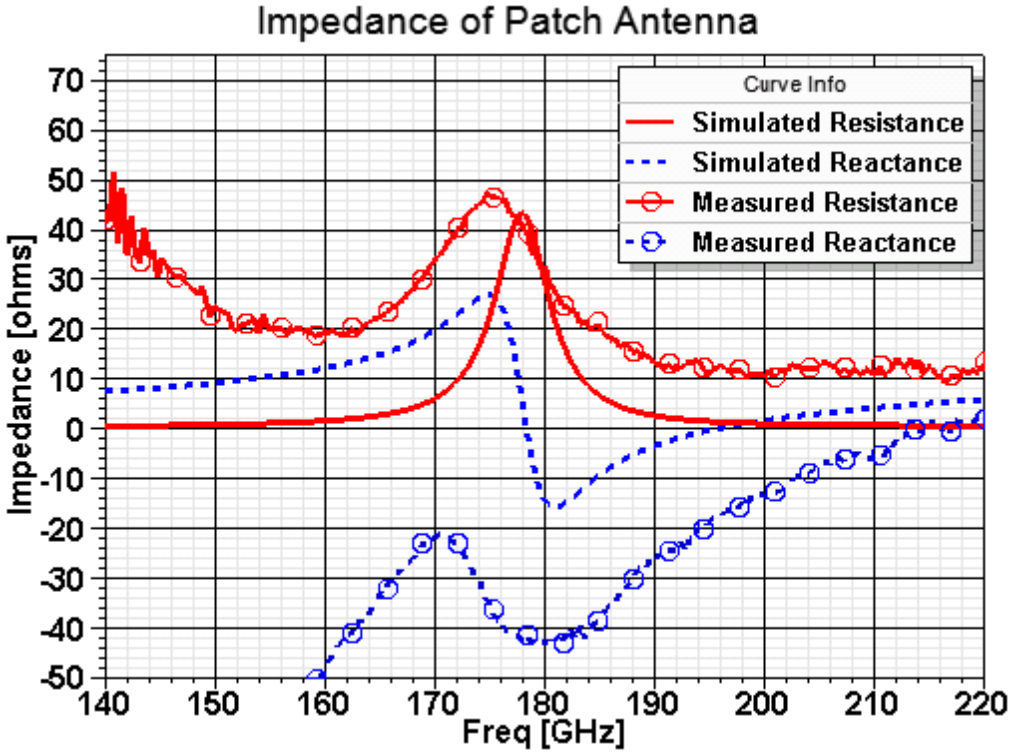

Figure 6.3: The simulated and measured impedance of the single on-chip patch antenna across the WR-5 frequency band. The simulated impedance of the patch antenna at 178.2 GHz is 42.12+j2.06 ohms. The measured impedance of the patch antenna at 172.4 GHz is 40.02-j23.82 ohms.

Radiation pattern cuts are measured for the on-chip patch antenna us-

ing the antenna measurement system described in Chapter 5. The radiation patterns are measured at the resonant center frequency of 172.4 GHz. This center frequency also produces the highest measured S_{21} values across the entire WR-5 frequency band of 140 GHz to 220 GHz. Both E-Plane and H-Plane radiation pattern cuts are measured for the single patch antenna. Using the chip coordinate system described in Chapter 5, the E-plane corresponds to the XZ-plane and the H-plane corresponds to the YZ-plane (also seen in Figure 6.1). Both co-polarized and cross-polarized pattern cuts are measured from the AUT by rotating the illuminating radiation towards the AUT by 90° as discussed in Chapter 5. Given the patch antenna orientation, co-polarization radiation (labeled as "Co-Pol.") corresponds to theta-polarization in the E-plane and phi-polarization in the H-plane where theta and phi are the standard polar coordinates. Cross-polarization radiation (labeled as "X-Pol.") corresponds to phi-polarization in the E-plane and theta-polarization in the H-plane. The radiation patterns were measured in 10° angular steps up to the physical limits of the equipment and environment (i.e. limited cable lengths, ground planes, various objects blocking the signal, etc.). For both E-plane and H-plane cuts, the 0°-mark corresponds to the zenith directly above the chip on the Z-axis. Positive angles in the E-plane correspond to angles from the Z-axis to the -X-axis. Positive angles in the H-plane correspond to angles from the Z-axis to the -Y-axis. $+/-90°$ on the radiation pattern cuts correspond to the XY-plane (i.e. the horizon of the ground plane). Figure 6.4 and Figure 6.5 show the radiation pattern cuts for the E-plane and H-plane, respectively. The

simulated and measured boresight of the antenna is pointed directly upward towards the Z-axis. Solid lines correspond to co-polarization measurements while dashed lines correspond to cross-polarization measurements. The simulated co-polarization and cross-polarization patterns are displayed in absolute gain, while the measured co-polarization and cross-polarization patterns are displayed in relative gain (i.e. the peak of the pattern is 0 dB). This helps overlay the measured data with simulated data and helps to compare the curvature of the patterns between simulated and measured data. The cross-polarized measurements are also relative to the co-polarized measurements. A "Noise Floor" line is added to the polar plots to show the measurement limit of the VNA (i.e. noise measurements).

Figure 6.4 and Figure 6.5 show the measured patch antenna is linearly polarized and agrees with simulation within 1-2 dB especially at angles near boresight. The simulated co-polarized half power beamwidth (labeled as "HPBW") in the E-plane is 116° while the measured HPBW is 100°. In the H-plane, the simulated co-polarized HPBW is 72° while the measured HPBW is 50°.

Figure 6.6 shows the 3D chip model and the simulated 3D radiation pattern at 178.2 GHz for both theta-polarization and phi-polarization. The 3D model orientation is matched to the 3D patterns. Recall that the E-plane cuts along the XZ-plane and the H-plane cuts along the YZ-plane. Figure 6.7 shows the total simulated pattern of the AUT which accounts for all polarizations. The simulated directivity of the patch is +3.83 dBi at 178.2 GHz. The

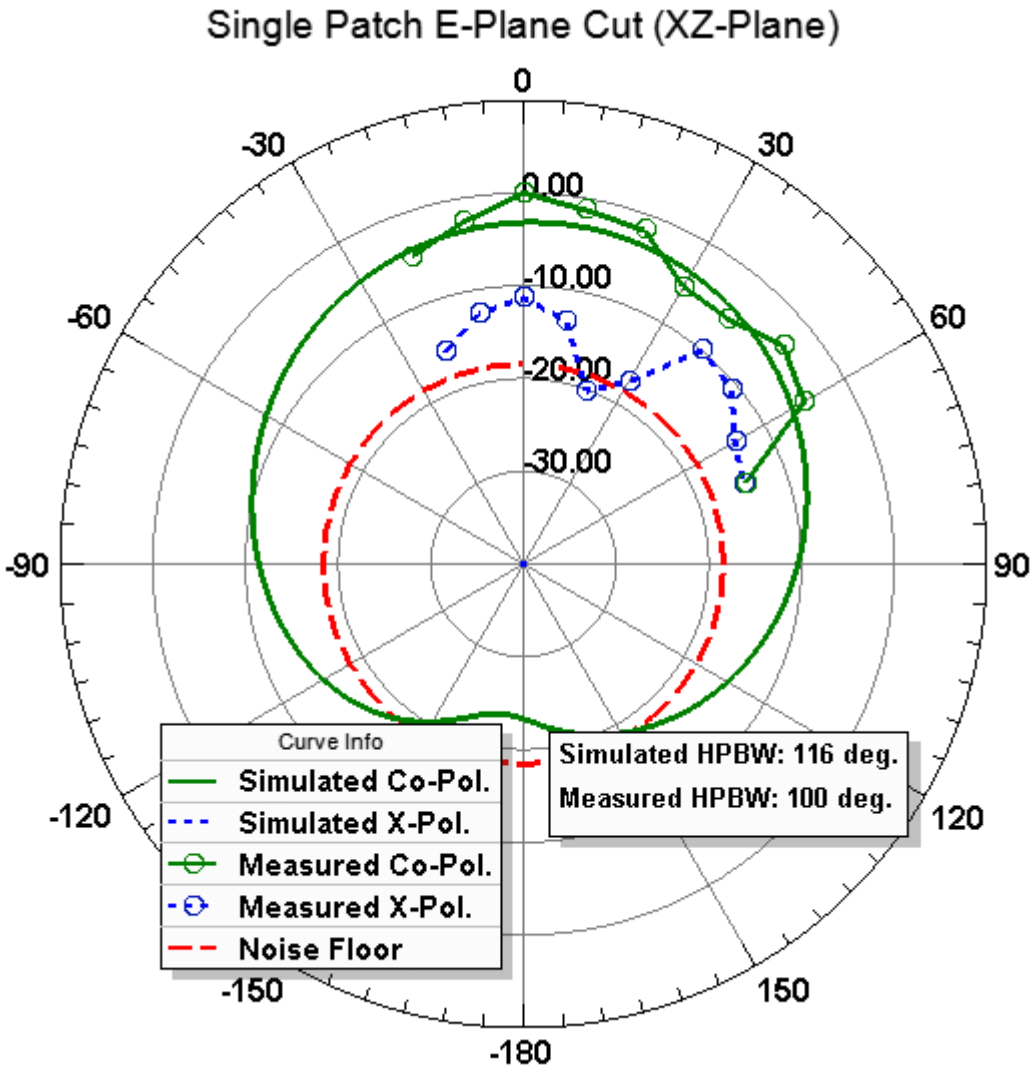

Figure 6.4: The measured E-plane pattern (XZ-plane) of the on-chip patch antenna at 172.4 GHz closely matches the simulated pattern at 178.2 GHz. As simulated, the patch antenna is linearly polarized with much weaker cross-polarized radiation (the "Simulated X-Pol." data is below scale) by up to -15 dB compared to co-polarized radiation. The simulated co-polarized half power beamwidth was 116° while the measured half power beamwidth was 100°.

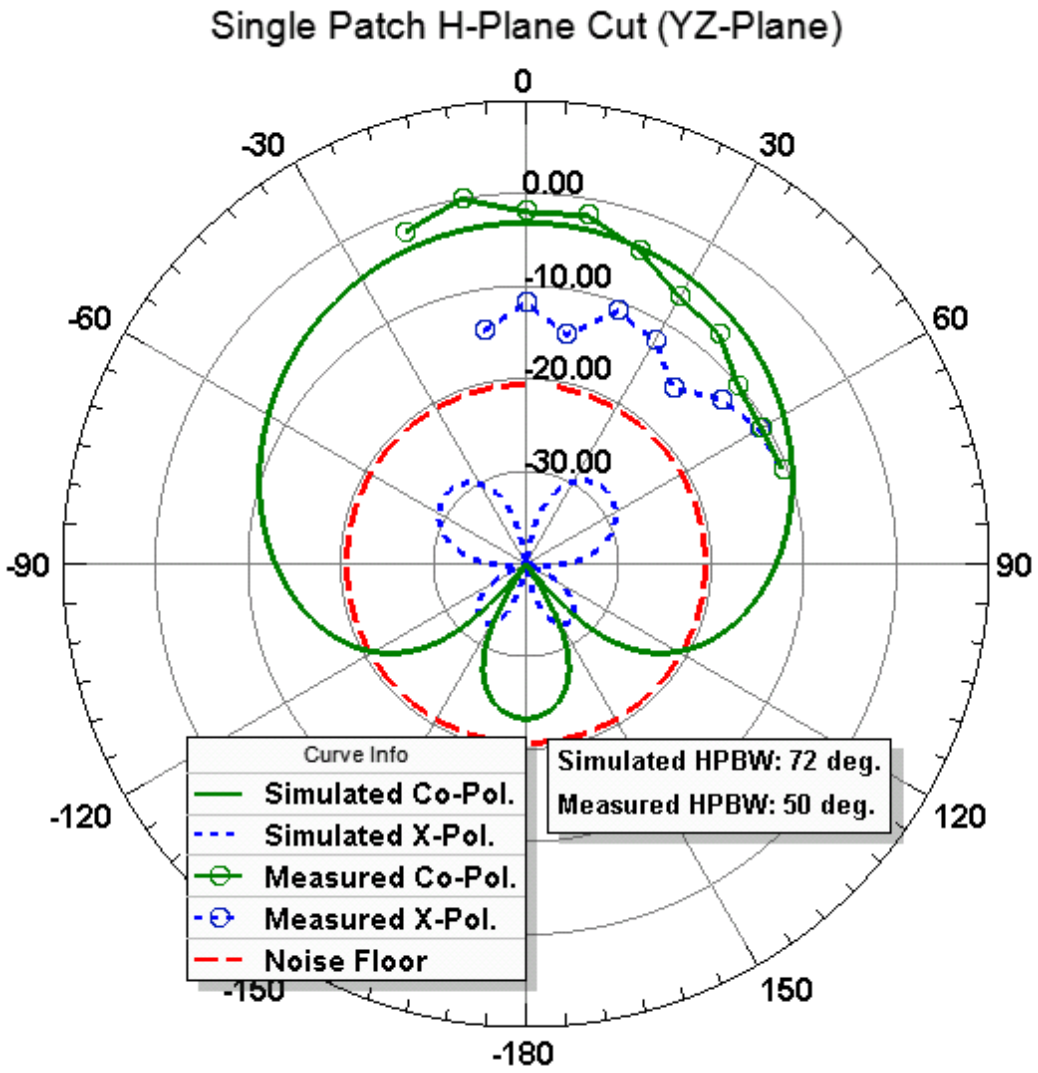

Figure 6.5: The measured H-plane pattern (YZ-plane) of the on-chip patch antenna at 172.4 GHz closely matches the simulated pattern 178.2 GHz. The patch antenna is linearly polarized with about 10 dB difference between co-polarized and cross-polarized radiation at boresight. The simulated co-polarized half power beamwidth was 72° while the measured half power beamwidth was 50°.

simulated antenna gain of the AUT is -3.21 dBi at 178.2 GHz. If simulated at the measured resonant frequency of 172.4 GHz, the AUT simulated gain would be -6.42 dBi as seen in Figure 6.8. Additionally, the simulated radiation efficiency is 20.27%. Recall that radiation efficiency is the percentage of accepted power by the AUT that is converted into radiated energy rather than losses such as ohmic losses.

To measure the antenna gain of the on-chip patch antenna, a modified Friis transmission equation can be used [56][42][61][67] which takes into account any mismatch losses, transmitter antenna gain, path loss, and receiver antenna gain as seen in Equation 6.1.

$$\frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} = G_t G_r (\frac{\lambda}{4\pi R})^2 \tag{6.1}$$

The S_{21} measurement from the VNA provides the ratio of the transmitted power to the received power. The highest measured S_{21} for the patch antenna is -59.405 dB at 172.4 GHz which is measured at -10° elevation on the H-plane with co-polarized illumination. Free space path loss is assumed between transmitter and receiver and calculated to be 62.748 dB for a TX-RX separation distance of 19 cm (i.e. $R = 19cm$) at 172.4 GHz (i.e. $\lambda = 1.74mm$). The transmit horn antenna gain (i.e. G_t) at 172.4 GHz is 26.225 dBi and was measured previously using a free space path loss test. Since the horn antenna and AUT are well matched to a 50 Ω impedance at this frequency, S_{11} and S_{22} are nearly zero. Using these values, the measured antenna gain of the

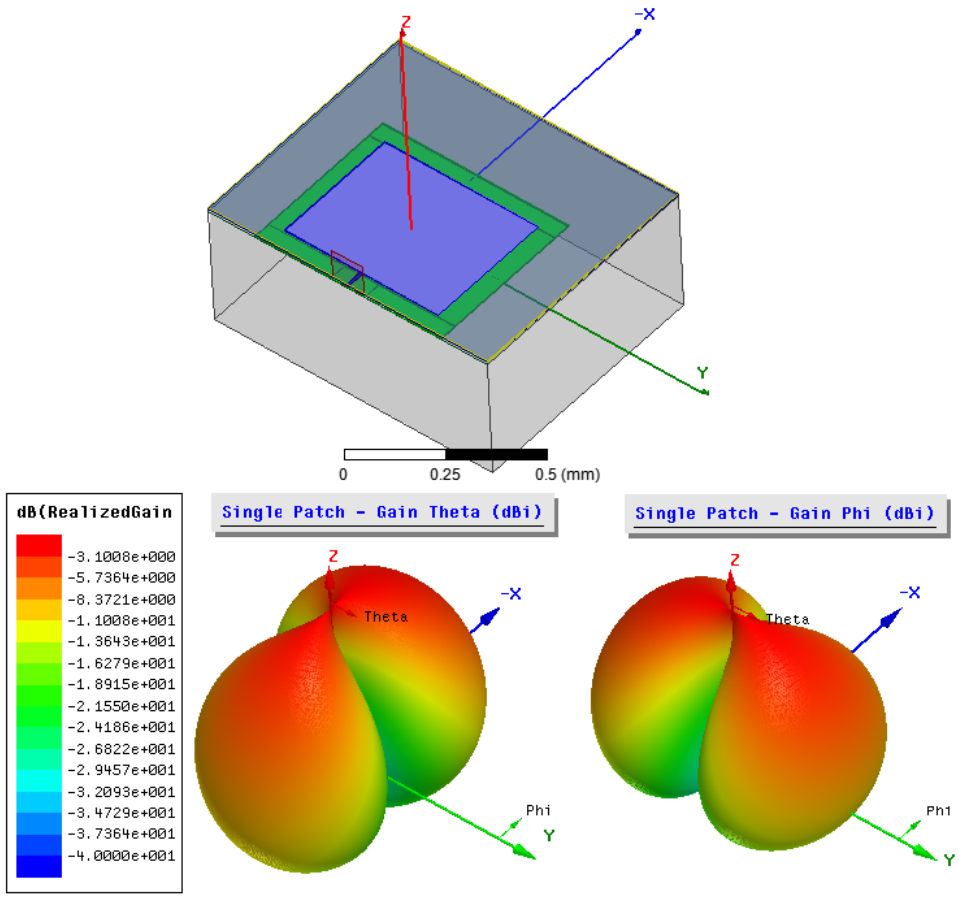

Figure 6.6: The full 3-dimensional radiation pattern of the on-chip patch antenna at 178.2 GHz. The two 3D patterns represent theta-polarization and phi-polarization. The on-chip patch antenna has a simulated gain of -3.21 dBi with boresight pointed towards the Z-axis.

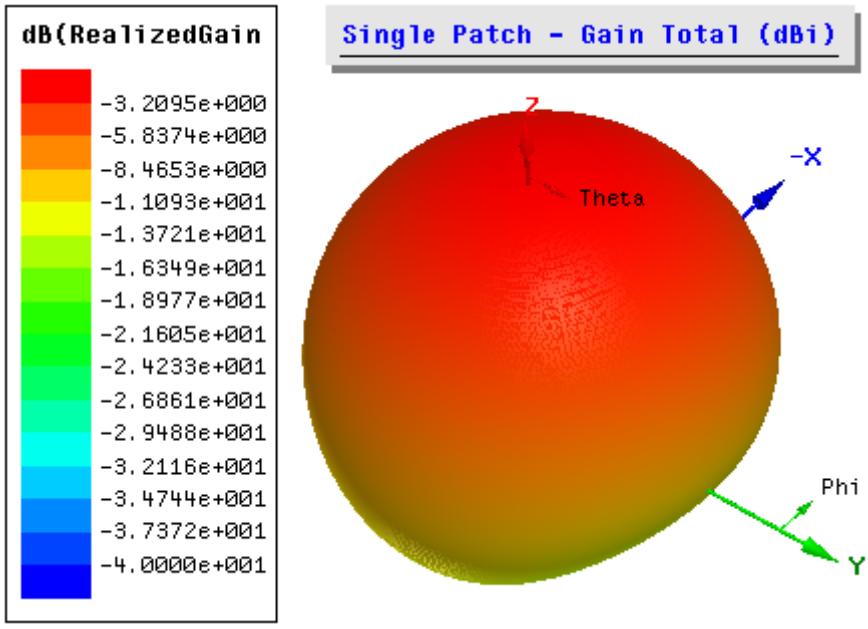

Figure 6.7: The full 3-dimensional radiation pattern of the on-chip patch antenna at 178.2 GHz. All polarizations are taken into account in this plot. The on-chip patch antenna has a simulated gain of -3.21 dBi with boresight pointed towards the Z-axis.

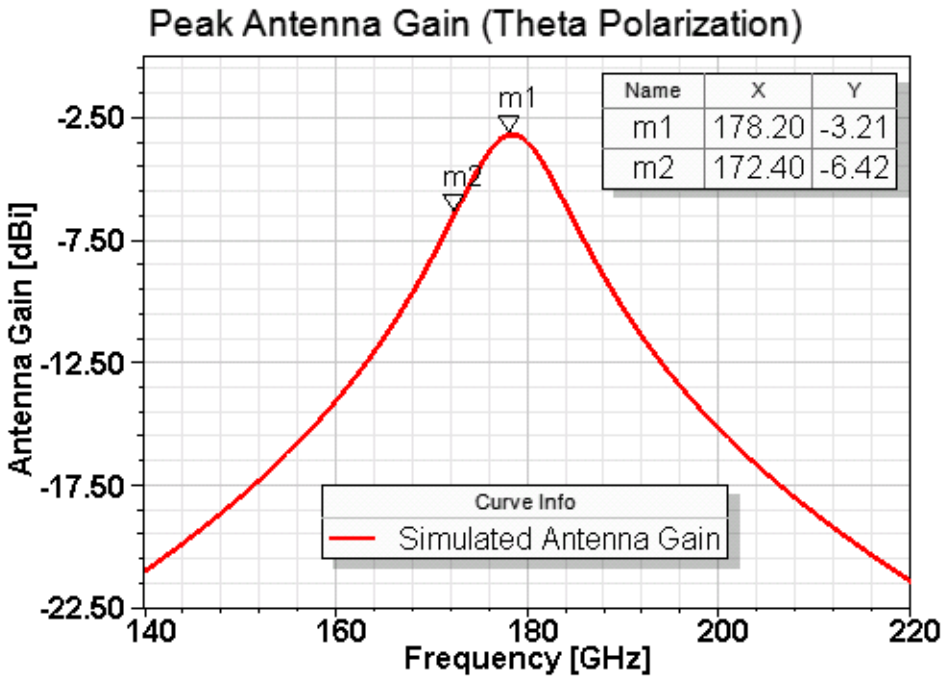

Figure 6.8: The peak antenna gain for a single patch antenna across the entire WR-5 frequency band (140 GHz to 220 GHz). The maximum simulated antenna gain was -3.21 dBi at 178.2 GHz.

AUT (i.e. G_r) is -22.88 dBi at 172.4 GHz, which is much different than the simulated gain of -3.21 dBi. The difference between simulated gain and measured gain is discussed at the end of this chapter. The main reason for the disparity in antenna gain is that the simulation model does not include all losses for all materials at 180 GHz such as possible dielectric loss tangents and lower metal conductivity. These values are unknown by the foundry especially at the WR-5 band. When including possible dielectric loss tangents or less than ideal conductivity in the simulation model, the simulated antenna gain decreases.

6.2 Patch Antenna Array Performance

In this section, the on-chip patch antenna array is measured, and the results such as return loss, bandwidth, impedance, radiation patterns, gain, directivity, and radiation efficiency are presented. As was done in the previous section with the single patch antenna, the on-chip patch antenna array is measured using the Cascade Microtech wafer probe station and antenna measurement system. The feed network of the patch antenna array is probed using a standard Cascade Microtech RF probe (Infinity I220-T-GSG-75-BT). Figure 6.9 shows a microscope image of the patch antenna array being probed. An RF probe calibration is performed prior to measuring the on-chip array using a Cascade Microtech Impedance Standard Substrate (ISS 138-356) and a 1-port SOL calibration routine. This calibration routine moves the VNA measurement plane to the tip of the RF probe. The return loss (S_{11}) is mea-

sured over the entire WR-5 frequency band (140 GHz to 220 GHz). Figure 6.10 compares the measured and simulated S_{11}. Since the feed network of the patch array is included in the return loss measurements, several resonances are produced at around 142 GHz, 172 GHz, and 210 GHz; however, knowing the measured behavior of the single patch antenna as seen in Figure 6.2, the true resonance of the patch array is at the 172 GHz band. Additionally, the highest measured S_{21} values of the patch array were also in the 172 GHz band.

The simulated S_{11} of the patch antenna has a center frequency of 180 GHz and a bandwidth ($S_{11} < -10dB$) of 9.84 GHz (i.e. 5.47% of the simulated carrier frequency) from 174.19 GHz to 184.03 GHz. The measured S_{11} of the patch antenna has a lower center frequency but larger bandwidth compared to simulation. The measured patch antenna array has a center frequency of 171.2 GHz and a bandwidth ($S_{11} < -20dB$) of 14.39 GHz (i.e. 8.41% of the measured carrier frequency) from 166.40 GHz to 180.79 GHz. To make a fair comparison between measured and simulated data of the on-chip patch array, simulations are performed at 178.2 GHz which has the highest simulated antenna gain, while measurements are performed at the resonant frequency of 171.2 GHz which has the highest measured S_{21} values.

The measured impedance of the on-chip patch antenna array is calculated using the complex return loss data (both magnitude and phase data of S_{11}) as is done for the single patch antenna in Figure 6.3. Figure 6.11 shows the impedance of the simulated and measured patch antenna array across the 140 GHz to 220 GHz frequency band. The simulated impedance of the patch

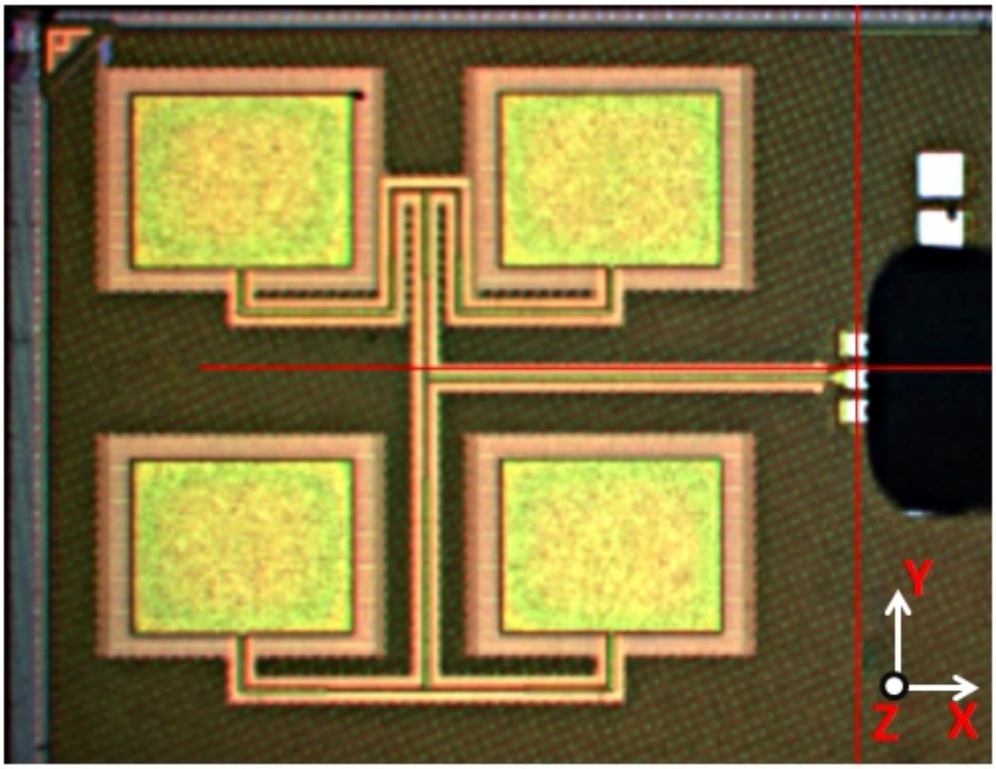

Figure 6.9: Microscope image of the patch antenna array being probed by a Cascade Microtech RF probe (Infinity I220-T-GSG-75-BT). An SOL calibration routine was preformed prior to probing which moves the VNA measurement plane to the tip of the RF probe.

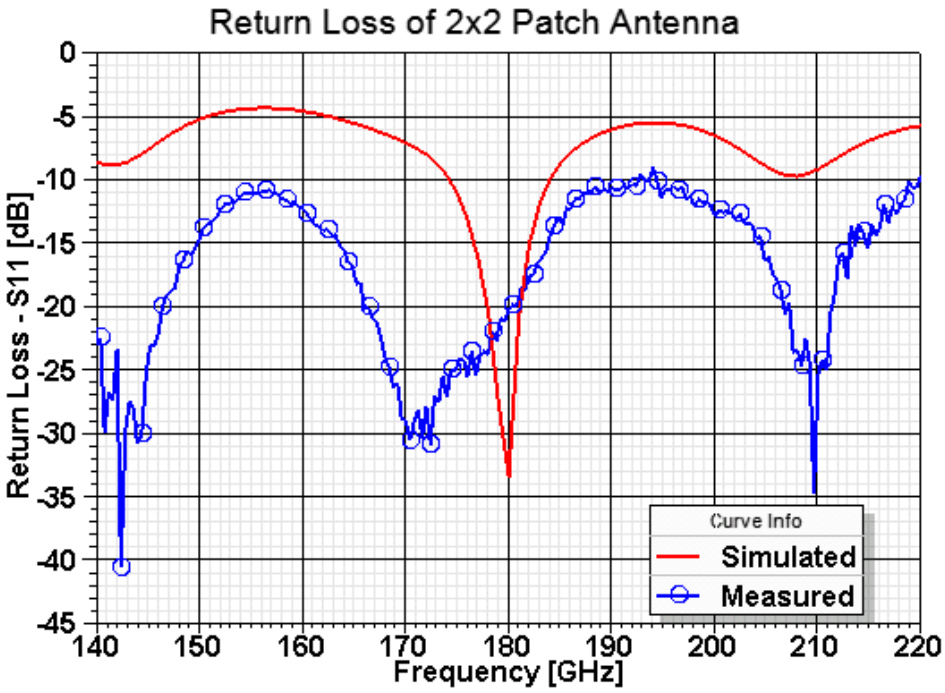

Figure 6.10: The return loss (S_{11}) of the on-chip patch antenna array over the WR-5 frequency band. The simulated patch array has a center frequency of 180 GHz with 9.84 GHz of bandwidth (i.e. 5.47% bandwidth of the carrier frequency) below -10 dB S_{11}. The measured patch array has a center frequency of 171.2 GHz with 14.39 GHz of bandwidth (i.e. 8.41% bandwidth of the carrier frequency) below -20 dB S_{11}.

antenna at its center frequency of 178.2 GHz is 44.35 - j5.68 ohms. The measured impedance of the patch antenna array at its center frequency of 171.2 GHz is 53.83-j1.44 ohms. The resistance of both the measured and simulated antenna are in agreement at nearly 50 ohms. In addition, the zero-crossing of the measured and simulated reactance are also in agreement ($\approx$ 176-180 GHz).

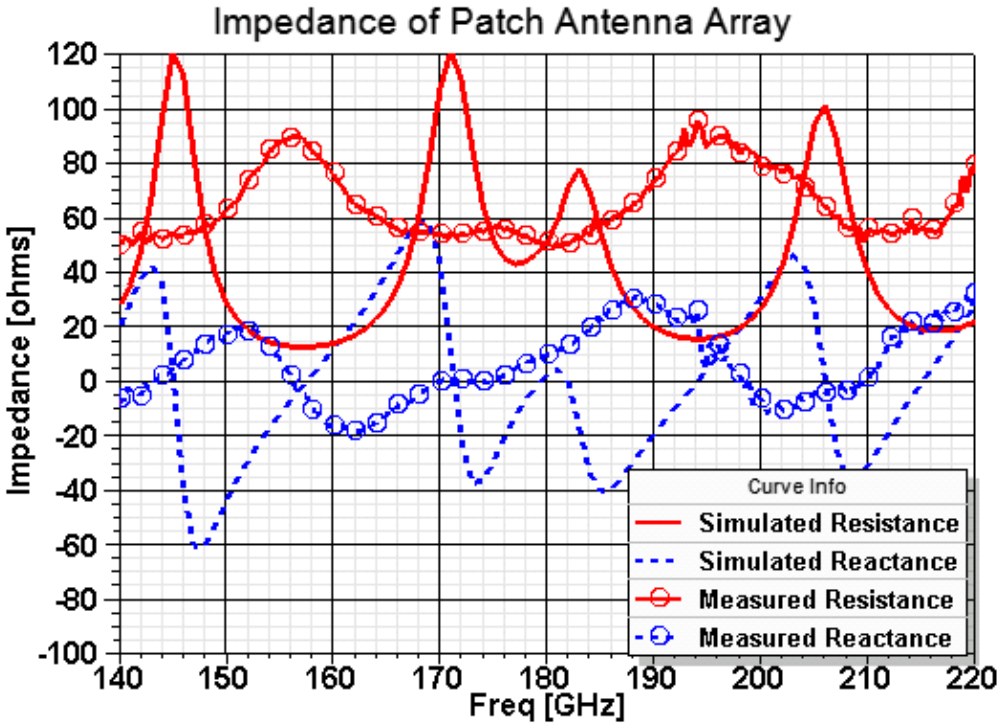

Figure 6.11: The simulated and measured impedance of the on-chip patch antenna array across the WR-5 frequency band. The simulated impedance of the antenna array at 178.2 GHz is 44.35-j5.68 ohms. The measured impedance of the antenna array at 171.2 GHz is 53.83-j1.44 ohms.

Similarly to the single patch antenna, radiation pattern cuts are measured for the on-chip patch antenna array using the antenna measurement

system described in Chapter 5. The radiation pattern cuts are performed at the measured resonant center frequency of 171.2 GHz. This center frequency also produced the highest measured S_{21} values across the entire WR-5 frequency band of 140 GHz to 220 GHz. Both E-Plane and H-Plane radiation pattern cuts are measured. The chip coordinate system described in Chapter 5 is used. Note that since the patch antenna array is 90° rotated clockwise on the chip compared to the single patch element in the previous section, the YZ-plane is now the E-plane for the patch array, and the XZ-plane is now the H-plane. Both co-polarized (labeled as "Co-Pol.") and cross-polarized (labeled as "X-Pol.") radiation pattern cuts are measured from the AUT. The patterns are measured in 10° angular steps up to the physical limits of the equipment and environment. As described in the previous section for the single patch antenna, the 0°-mark for both E-plane and H-plane cuts correspond to the zenith directly above the chip on the Z-axis. Positive angles in the E-plane correspond to angles from the Z-axis to the -Y-axis. Positive angles in the H-plane correspond to angles from the Z-axis to the -X-axis. $+/-90°$ on the radiation pattern cuts correspond to the XY-plane (i.e. the horizon of the ground plane). Figure 6.12 and Figure 6.13 show the radiation patterns cuts for the E-plane and H-plane, respectively. The simulated and measured boresight of the antenna is pointed directly upward towards the Z-axis. A "Noise Floor" line is added to the polar plots to show the measurement limit of the VNA (i.e. noise measurements). Solid lines correspond to co-polarization measurements while dashed lines correspond to cross-polarization measurement.

The simulated co-polarization and cross-polarization patterns are displayed in absolute gain, while the measured co-polarization and cross-polarization patterns are displayed in relative gain (i.e. the peak of the pattern is 0 dB). This helps overlay the measured data with simulated data and helps to compare the curvature of the patterns between simulated and measured data.

Figure 6.12 and Figure 6.13 show the measured patch antenna array is linearly polarized and agrees with simulation within 1-2 dB especially at angles near boresight. The measured E-plane pattern has a boresight at 0° which verifies the feed network is properly combining cophasal waves between the elements of the array in the Y-direction (i.e. the top and bottom patch elements). The measured H-plane pattern has a boresight slightly tilted towards +20° for both the co-polarized and cross-polarized measurements which indicates some slight transmission line delay for the left elements in the patch array. As predicted from simulation, the measured radiation pattern is narrower compared to the single patch element patterns in Figure 6.4 and Figure 6.5. The simulated co-polarized half power beamwidth (labeled as "HPBW") in the E-plane is 56° while the measured HPBW is 70°. In the H-plane, the simulated co-polarized HPBW is 52° while the measured HPBW is 40°.

Figure 6.14 shows the 3D chip model of the patch antenna array and the simulated 3D radiation pattern at 178.2 GHz for both theta-polarization and phi-polarization. The 3D model orientation is matched to the 3D patterns. Recall that the E-plane cuts along the YZ-plane and the H-plane cuts along the XZ-plane for the patch antenna array. Figure 6.15 shows the total

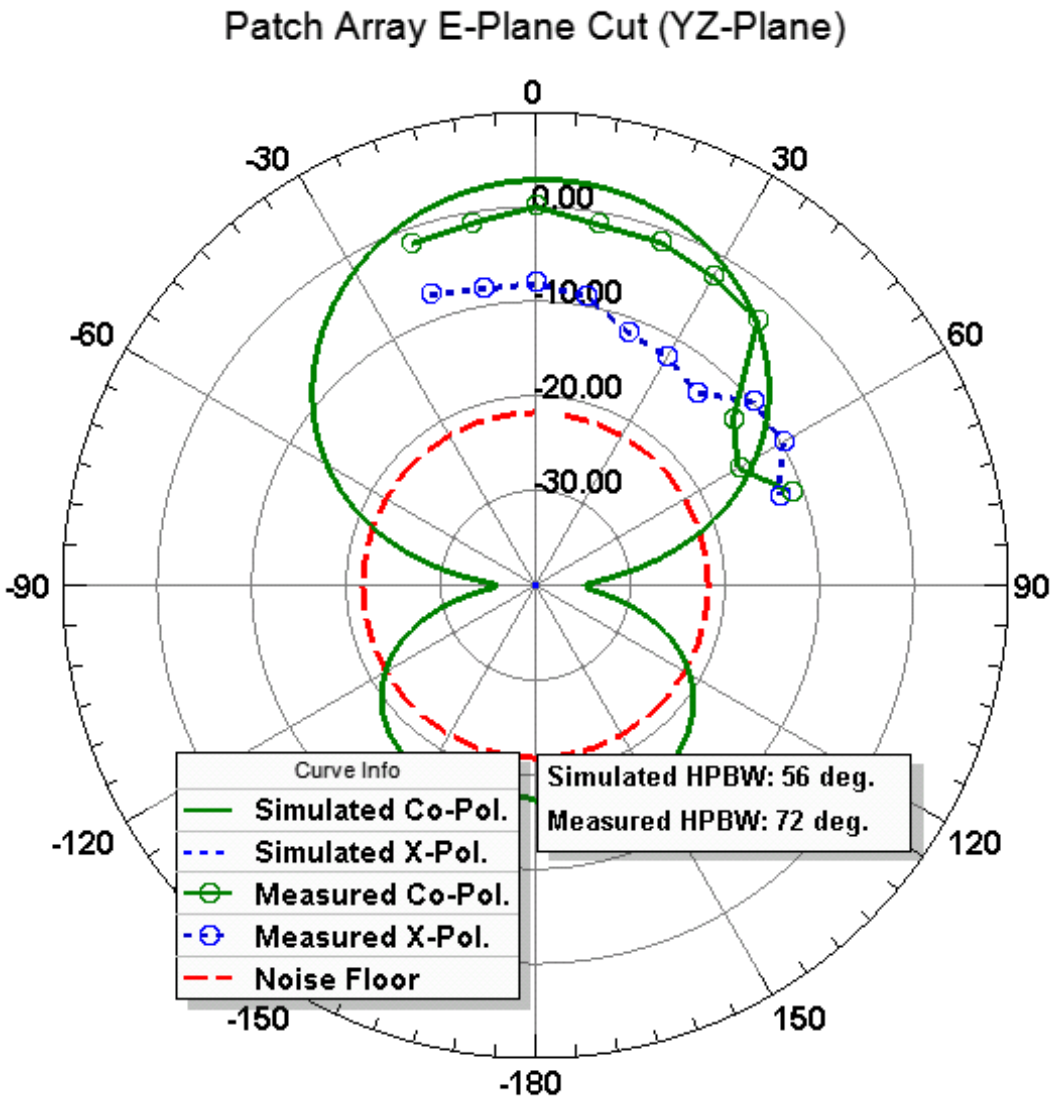

Figure 6.12: The measured E-plane radiation pattern (YZ-plane) of the on-chip patch antenna array at 171.2 GHz closely matches the simulated pattern at 178.2 GHz. As simulated, the patch antenna is linearly polarized with about 6-10 dB difference between co-polarized and cross-polarized radiation near boresight. The simulated co-polarized half power beamwidth is 56° while the measured half power beamwidth is 72°.

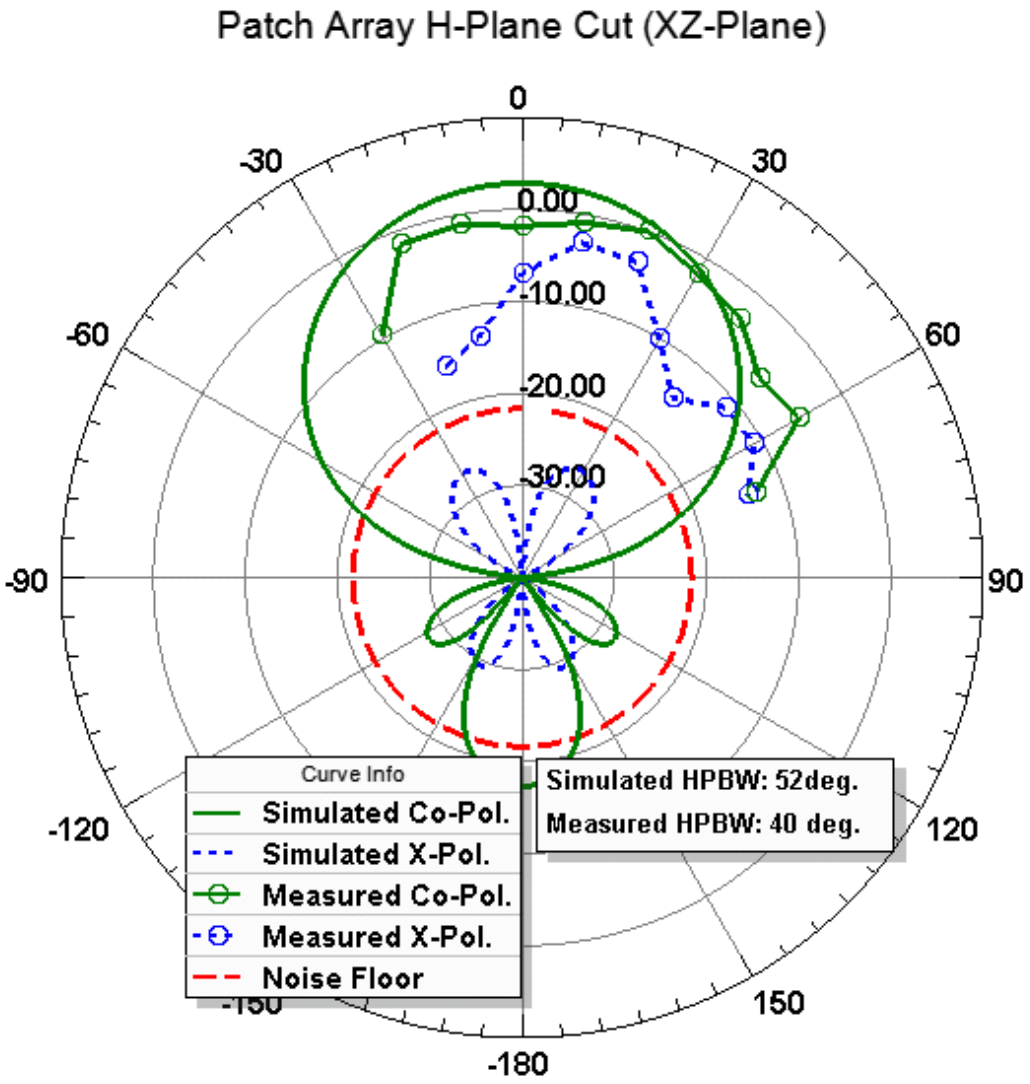

Figure 6.13: The measured H-plane radiation pattern (XZ-plane) of the on-chip patch antenna at 171.2 GHz closely matches the simulated pattern at 178.2 GHz. Transmission line delays on the left elements of the patch array cause the boresight to shift slightly to +20°. The patch antenna array is linearly polarized, and has a higher cross-polarized component near boresight as compared to the E-plane measurement. The simulated co-polarized half power beamwidth is 52° while the measured half power beamwidth is 40°.

simulated pattern of the AUT which accounts for all polarizations. The simulated directivity of the patch is +9.79 dBi at 178.2 GHz, the simulated gain is +2.81 dBi, and the simulated radiation efficiency is 20.35%.

To calculate the measured gain of the patch antenna array, Equation 6.1 is used. The highest measured S_{21} for the patch antenna array is -58.085 dB at 171.2 GHz which is measured at +20° elevation on the H-plane with co-polarized illumination. Free space path loss is assumed between transmitter and receiver and calculated to be 62.687 dB for a TX-RX separation distance of 19 cm (i.e. $R = 19cm$) at 171.2 GHz (i.e. $\lambda = 1.75mm$). The transmit horn antenna gain (i.e. G_t) at 171.2 GHz is 25.72 dBi and was measured previously using a free space path loss test. Since the horn antenna and AUT are well matched at this frequency, S_{11} and S_{22} are nearly zero. Using these values, the measured antenna gain of the AUT (i.e. G_r) is -21.12 dBi at 171.2 GHz. Recall that the gain of the single patch antenna at 172.4 GHz is -22.88 dBi. If the simulated array gain is 6.02 dB, one would expect the antenna gain of the array to be 6 dB stronger than the single patch (i.e. $\approx$ -16.88 dBi). The reason why a 6 dB increase is not measured from the patch array is that the transmission line feed network attenuates the received signal which diminishes the antenna array gain. To determine the true gain of the patch array, the attenuation of the transmission lines must be removed as is done below. Additionally, even after removing the attenuation of the feed network, the difference between simulated gain and measured gain is drastically different, and the reason for this disparity is that the simulation

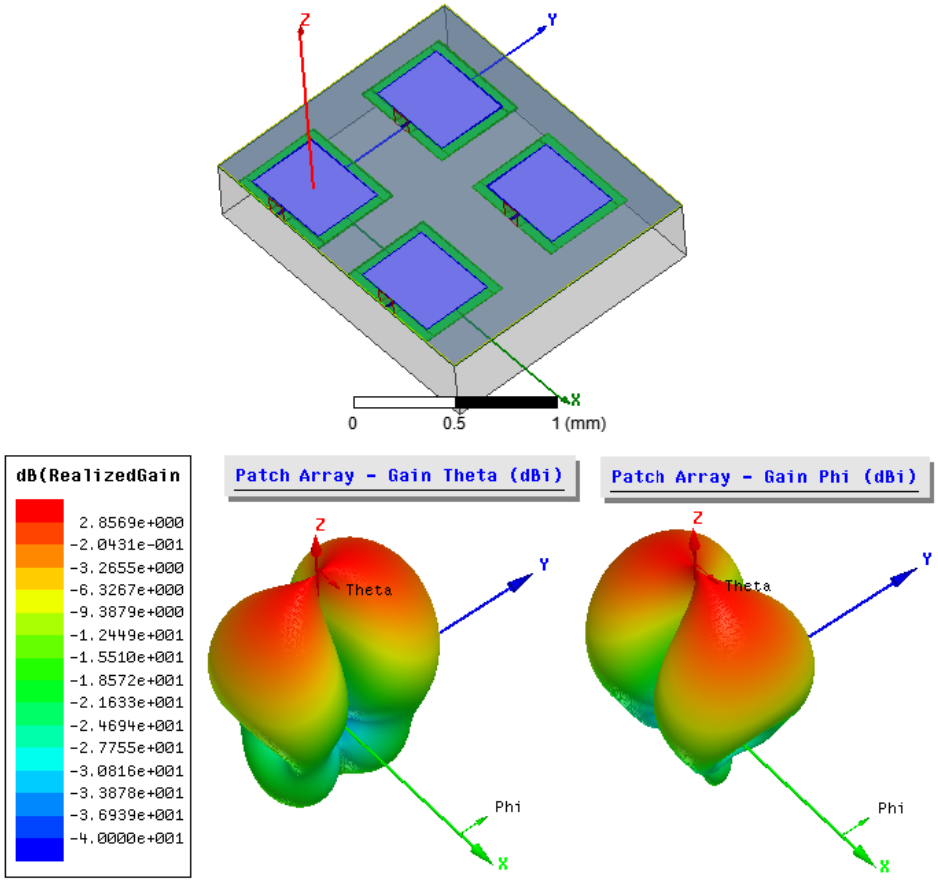

Figure 6.14: The full 3-dimensional radiation pattern of the on-chip patch antenna array at 178.2 GHz. The two 3D patterns represent theta-polarization and phi-polarization. The on-chip 2x2 patch antenna array has a simulated gain of +2.81 dBi (an increase of 6.02 dB compared to the single patch antenna) with boresight pointed towards the Z-axis.

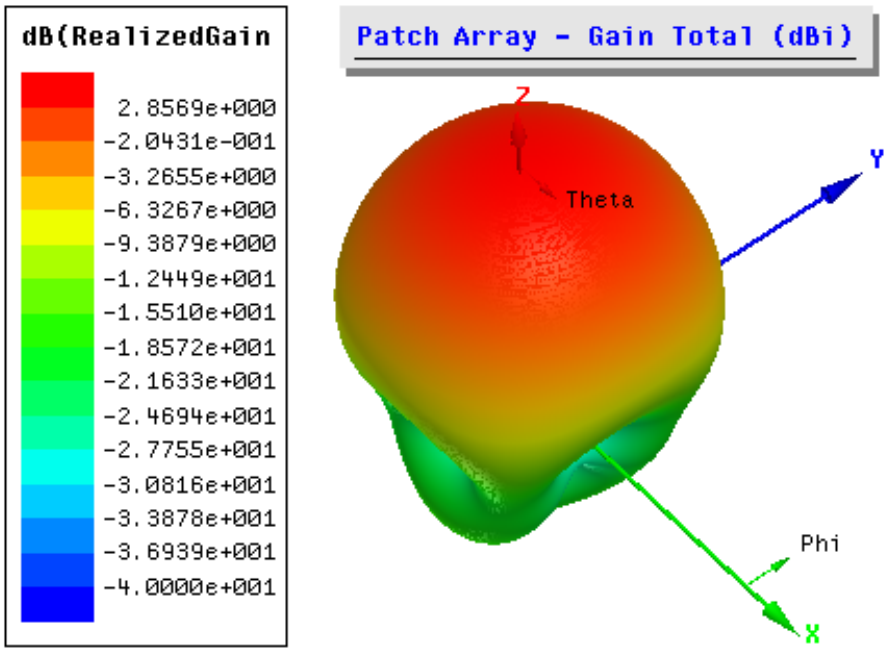

Figure 6.15: The full 3-dimensional radiation pattern of the on-chip patch antenna array at 178.2 GHz. All polarizations are taken into account in this plot. The on-chip patch antenna array has a simulated gain of +2.81 dBi with boresight pointed towards the Z-axis.

model does not include all possible material losses at 180 GHz which are unknown by the foundry. For example, the dielectrics used in the process could contain abnormally high dielectric loss tangents or the conductors could have less than ideal conductivity both of which would increase losses in the feed network and antenna. An attempt is made to estimate the additional losses. It is very possible that the losses could be a combination of both dielectric and conductor losses, but given this measurement method, there is no way to separate the material losses.

To determine the true measured gain of the patch antenna array, the attenuation of the feed network must be calculated and removed. Since a stand-alone transmission line feed network was not fabricated on-chip to measure attenuation, a pseudo-measurement/simulation estimate is used to determine the attenuation of the feed network. A sample transmission line from the feed network was fabricated on the chip. The transmission line is 505 μm in length and has a characteristic impedance $\approx$ 50 Ω (exact value: 50.3-j0.9 Ω) at 171.2 GHz using the 2D electromagnetic simulator ANSYS Q3D Extractor. The simulated transmission line cross section for a 50 Ω and 70.7 Ω line can been seen in Figure 6.16 and Figure 6.17, respectively. Recall that the feed network is composed of both 50 Ω and 70.7 Ω transmission line sections (exact values: 50.3-j0.9 Ω and 71.8-j1.4 Ω, respectively).

This sample transmission line is probed and measured to determine the insertion loss (i.e. $-|S_{21}|$) as seen in Figure 6.18. The measured loss is -2.172 dB at 171.2 GHz after removing any S_{11}/S_{22} mismatch losses. This

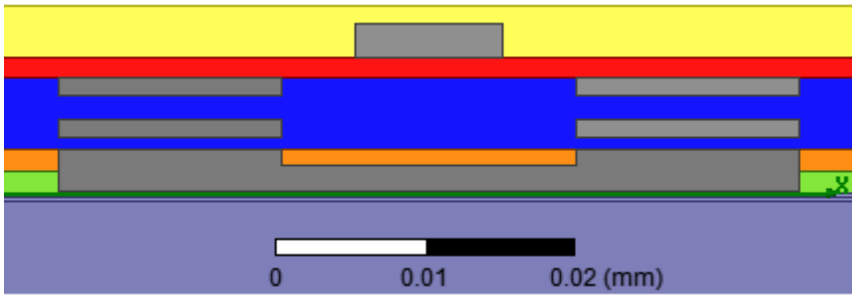

Figure 6.16: The cross section of the simulated 50 Ω transmission line using ANSYS Q3D Extractor. The ground conductor is constructed using several metal layers with interconnecting vias (vias not shown). The line width is 9.9 μm.

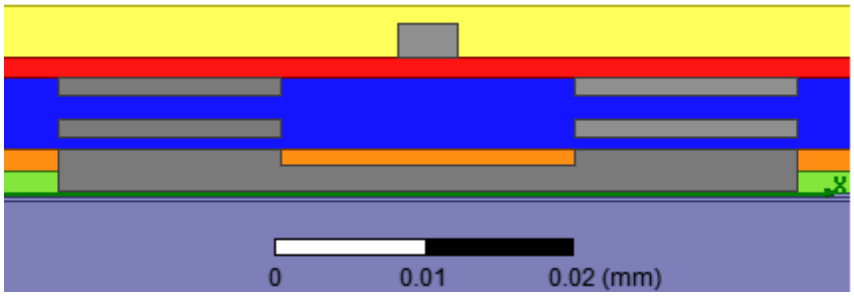

Figure 6.17: The cross section of the simulated 70.7 Ω transmission line using ANSYS Q3D Extractor. The ground conductor is constructed using several metal layers with interconnecting vias (vias not shown). The line width is 4 μm.

corresponds to an attenuation of 4.3 dB/mm, which is much greater than the simulated transmission line loss of 1.278 dB/mm using ideal metals and dielectrics. If you assume that all loss is completely due to less conductive metal, a conductivity of 1.5×10^6 siemens/meter (as compared to an ideal conductivity of 3.8×10^7 S/m) would produce the same measured attenuation of 4.3 dB/mm. Likewise, if you assume that all loss is completely due to a high dielectric loss tangent, a loss tangent of 0.46 would produce the same measured attenuation. To increase the attenuation of the simulated transmission line, the loss tangent of the dielectric between the signal and ground conductors (colored as red in Figures 6.16 and 6.17) is increased from 0.0 to 0.46. Using a loss tangent value of 0.46 produces a 4.29 dB/mm attenuation at 171.2 GHz for the simulated 50 Ω transmission line, and 1.87 dB/mm for the 70.7 Ω transmission line. Using these simulated attenuation values based upon measurements, the attenuation of the feed network can be calculated by summing the line lengths of all 50 Ω and 70.7 Ω lines. Thus, the estimated loss of the patch antenna array feed network is 7.622 dB. Removing this feed network loss, the true measured antenna gain of the patch antenna array is -13.5 dBi. The measured antenna gain is still much different compared to the simulated antenna gain of +2.81 dBi, and the reason for this difference is due to the material losses, as discussed in the next section.

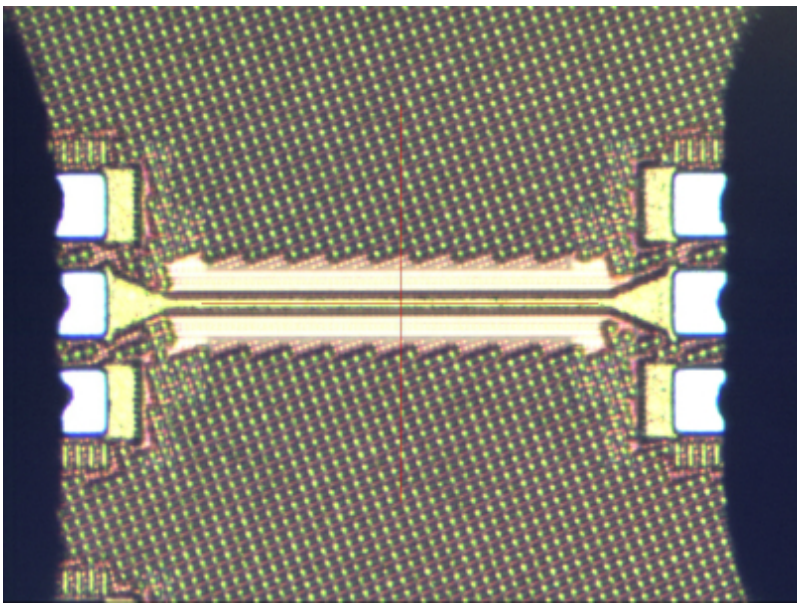

Figure 6.18: A microscope image of a sample transmission line from the patch antenna array feed network being probed using two standard Cascade Microtech RF probes (Infinity I220-T-GSG-75-BT). The measured attenuation of this transmission line helps estimate the attenuation of the feed network to be 7.622 dB.

6.3 Antenna Gain Differences Between Simulation and Measurement

The measured and simulated antenna gains for both the single patch antenna and the antenna patch array were drastically different. For example, the single patch antenna has a simulated antenna gain of -3.21 dBi, while the measured gain is -22.88 dBi. For the patch antenna array, the simulated antenna gain is +2.81 dBi, while the measured gain is -13.5 dBi. In literature, many authors state that the lossy and highly conductive silicon substrate underneath the on-chip antenna is the reason for low-gain antennas as seen in Chapter 2; however, when removing the lossy silicon substrate from simulation, there is very little difference in antenna gain. This is intuitive as the ground plane of the patch antenna shields the radiated fields from the silicon. Instead of the silicon substrate, the dielectric and/or metal in which the patch antenna is constructed is the main reason for low antenna gain. As mentioned in the previous section, the simulation models do not include dielectric loss tangents as assume ideal metal conductivities. When constructing the 3D model from the foundry's design kit, the dielectric loss tangents were not known especially at the WR-5 band of 140 GHz to 220 GHz. Lossless dielectrics and high conductive metals simulate much less attenuation compared to measurements as is seen when comparing the measured vs. simulated attenuation of the sample on-chip 50 Ω transmission line. When the loss tangent is 0.0 for the dielectric between the signal and ground conductors (i.e. the red layer in Figures 6.16 and 6.17), the simulated transmission line attenuation is 1.278 dB/mm;

however, if you assume that all loss is due to the dielectric, and the dielectric loss tangent is increased to 0.46, the simulated transmission line attenuation is 4.29 dB/mm which matches the measured attenuation of 4.3 dB/mm. This identical process is applied to the single patch antenna simulation, in which the loss tangent of the same dielectric layer between the patch and ground conductor is increased from 0.0 to 0.3. As seen in Figure 6.19, the antenna gain of the simulated radiation pattern decreases. Note that the curvature and shape of the radiation pattern remains nearly unchanged. At a loss tangent of 0.3, the simulated antenna gain is -23.5 dBi and its radiation pattern almost perfectly aligns with the measured radiation pattern with a measured gain of -22.88 dBi. Figure 6.20 shows how different dielectric loss tangents effect the simulated antenna gain and simulated radiation efficiency. Using this graph, an estimated loss tangent of 0.2916 would produce the measured -22.88 dBi antenna gain. The radiation efficiency is then estimated to be 7.89%.

From the measured data of the transmission line and on-chip radiation pattern cuts, the dielectric loss tangent is estimated between 0.29 and 0.46. More on-chip structures and measurements would be needed to produce a more accurate estimate and determine if dielectric, metal, or a combination of both is responsible for the losses. This behavior emphasizes the importance of not only understanding the silicon conductivity but also the dielectric loss tangents and metal conductivities when designing on-chip antennas. The foundry must also analyze and minimize the loss of their materials at millimeter-wave and sub-terahertz frequencies if high-gain on-chip antennas are to be produced for

future wireless communications.

6.4 Effects of RF probes, DC Probes, and RF Absorber on Antenna Radiation Patterns

In addition to studying the on-chip antennas, several environmental condition tests are also conducted. The first test determines the interference of the RF probe when measuring radiation patterns of on-chip antennas. The next test determines the interference of a nearby DC probe when measuring radiation patterns. This particular test is useful for testing future integrated circuit chips that contain a combination of digital logic, analog, RF, and antenna structures each of which need to be tested with DC and RF probes. In production line wafer-level testing, many chips are rapidly tested in succession using DC and RF probes to input/output test signals. If on-chip antenna testing is simultaneously performed with DC and RF testing, these DC probes have the potential to interfere with antenna measurements. Thus, this environmental test places a DC probe adjacent to the on-chip antenna array, and a radiation pattern is measured to determine the effect of the DC probe. The last environmental test determines the effects of RF absorbing material on measured antenna radiation patterns by comparing patterns with and without RF absorbing material on the probe station.

To determine the interference of the RF probe when measuring on-chip antennas, a radiation pattern cut is measured when the RF probe is probing a dummy load of 50 Ω. The Cascade Microtech Impedance Standard Substrate

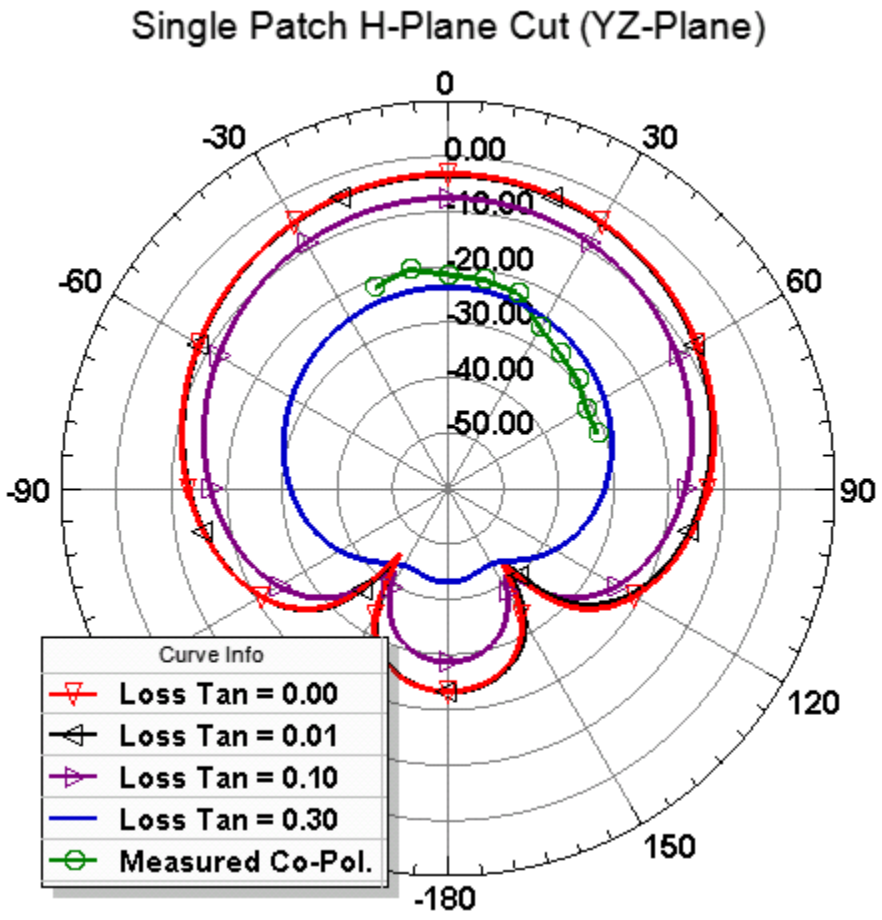

Figure 6.19: By increasing the dielectric loss tangent from 0.0 to 0.3, the simulated antenna gain at 178.2 GHz decreases; however, the shape and curvature of the radiation pattern remains the same. A loss tangent of 0.3 nearly aligns the measured and simulated antenna radiation patterns.

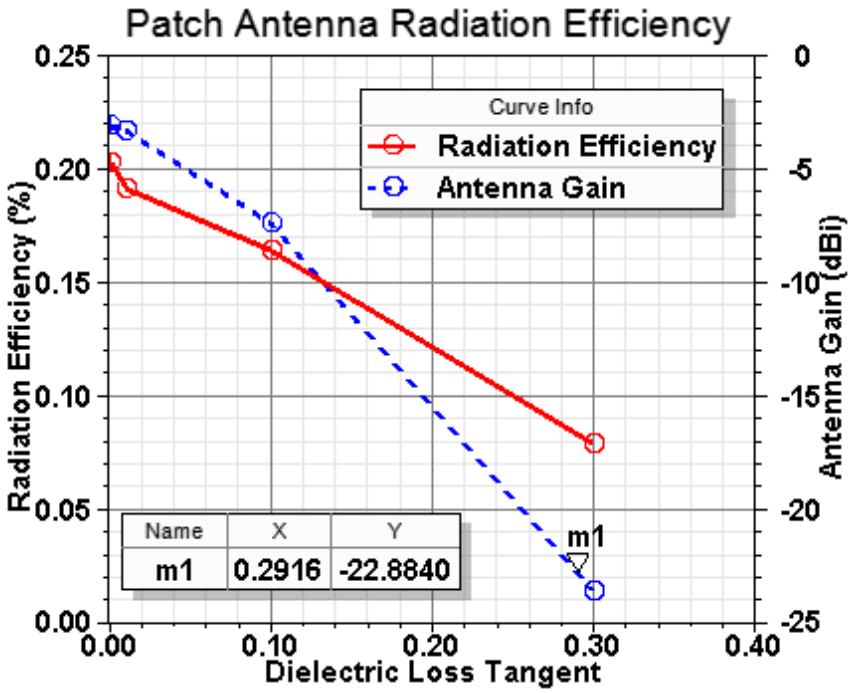

Figure 6.20: This graph shows how antenna gain and radiation efficiency at 178.2 GHz are effected by increasing the dielectric loss tangent. A loss tangent of 0.2916 produces the same measured antenna gain of -22.88 dBi and a radiation efficiency of 7.89%.

is used which contains several precision 50 Ω loads. Figure 6.21 shows a microscope image of the 50 Ω load being probed. Figure 6.22 shows a picture of the probe making contact with the ISS in the probe station environment which was coated with black RF absorber. The E-plane and H-plane radiation pattern cuts are measured and compared to the patch antenna array measurements in Figures 6.23 and 6.24, respectively. Several conclusions can be made from these plots. In the E-plane, the received power from the RF probe is much less as compared to probing the AUT. At boresight, the co-polarized received power from the RF probe is at least 15 dB less than the AUT. Near the AUT boresight, the power from the RF probe is just above the noise floor and increases to 10 dB above noise floor at angles close to the horizon. Additionally, the probe shows stronger cross-polarized received power than the received AUT co-polarized power (i.e. the RF probe is cross-polarized with the AUT). The same behavior is seen in the H-plane as well. Near boresight, the co-polarized received power from the RF probe is essentially noise measurements. The probe also has stronger received power from cross-polarized illumination rather than co-polarized illumination. Thus, this test shows that the RF probe does not interfere with the on-chip antenna measurements since the probe radiation is much weaker compared to the AUT, as well as being cross-polarized with the AUT.

In the second test, a DC probe is placed just above the chip adjacent to the patch antenna array as seen in the microscope image in Figure 6.25. The DC probe does not contact the chip and simply hovers above the on-

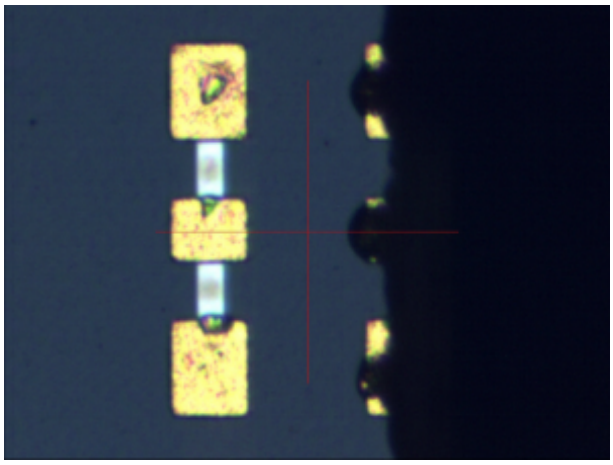

Figure 6.21: Microscope image of a precision 50 Ω load being probed. The radiation pattern cut from this environmental test determines how much interference the RF probe creates when measuring an on-chip antenna.

chip antenna as seen as a dark blurred line in Figure 6.25. Since DC probe pads are located along the perimeter of a chip, this is most likely where a DC probe would be placed during chip testing. Figure 6.26 shows a picture of the DC probe as the RF probe begins to probe the on-chip antenna array. RF absorbing material was placed around the DC probe positioner to reduce possible reflections.

In the third test, all RF absorbing material is removed from the probe station as seen in Figure 6.27. This environmental test determines how much the RF absorbing material improves the accuracy of the radiation pattern measurements.

The E-plane and H-plane radiation pattern measurements for the DC probe interference test and the RF absorber removal test are shown in Figures

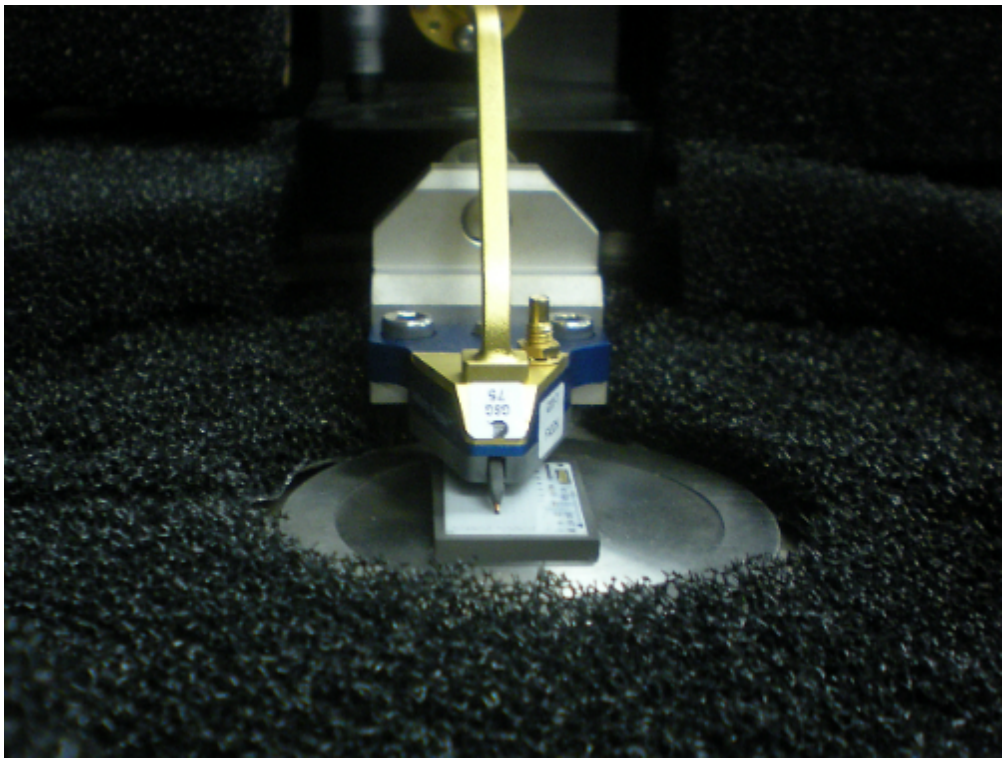

Figure 6.22: A picture of the RF probe probing a 50 Ω load on the Cascade Microtech Impedance Standard Substrate (ISS).

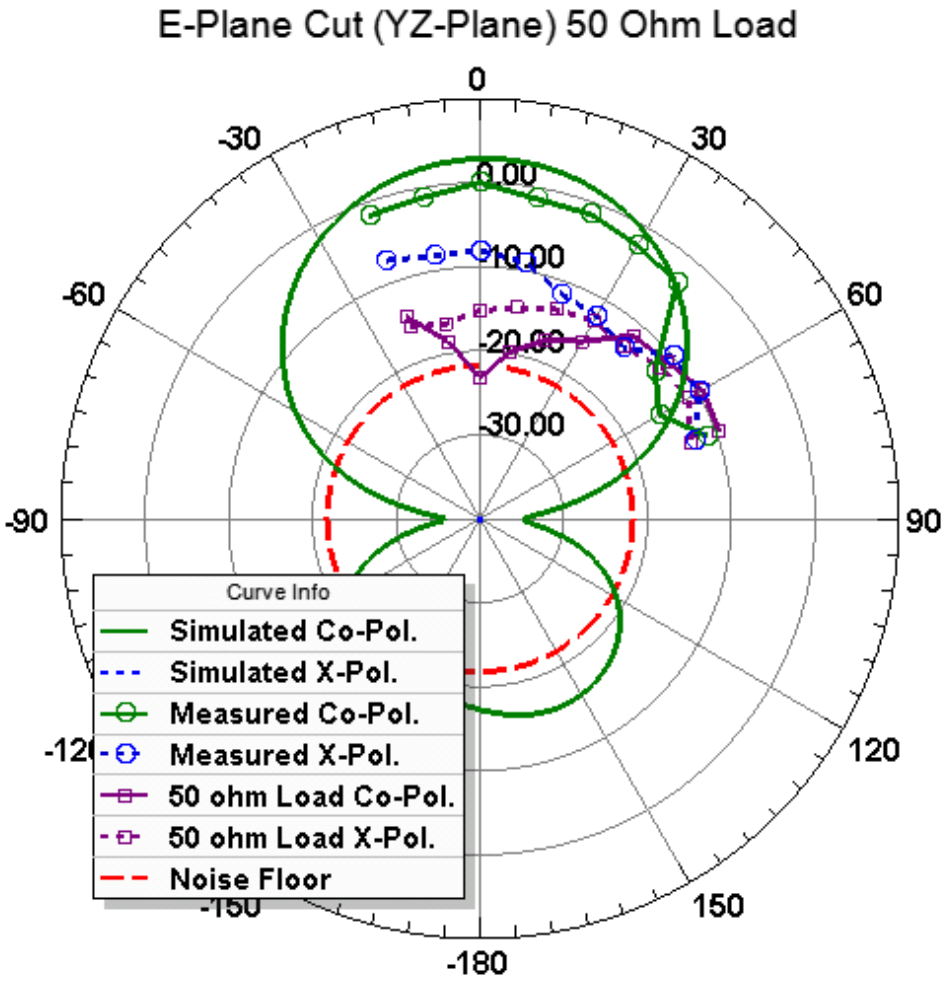

Figure 6.23: This E-plane radiation pattern test shows the RF probe does not effect the antenna pattern measurements of the on-chip patch antenna array. For co-polarized illumination at boresight, the received power from the RF probe is at least 15 dB less compared to the on-chip patch antenna array. Additionally, the RF probe is cross-polarized with the AUT which helps reduce its interference.

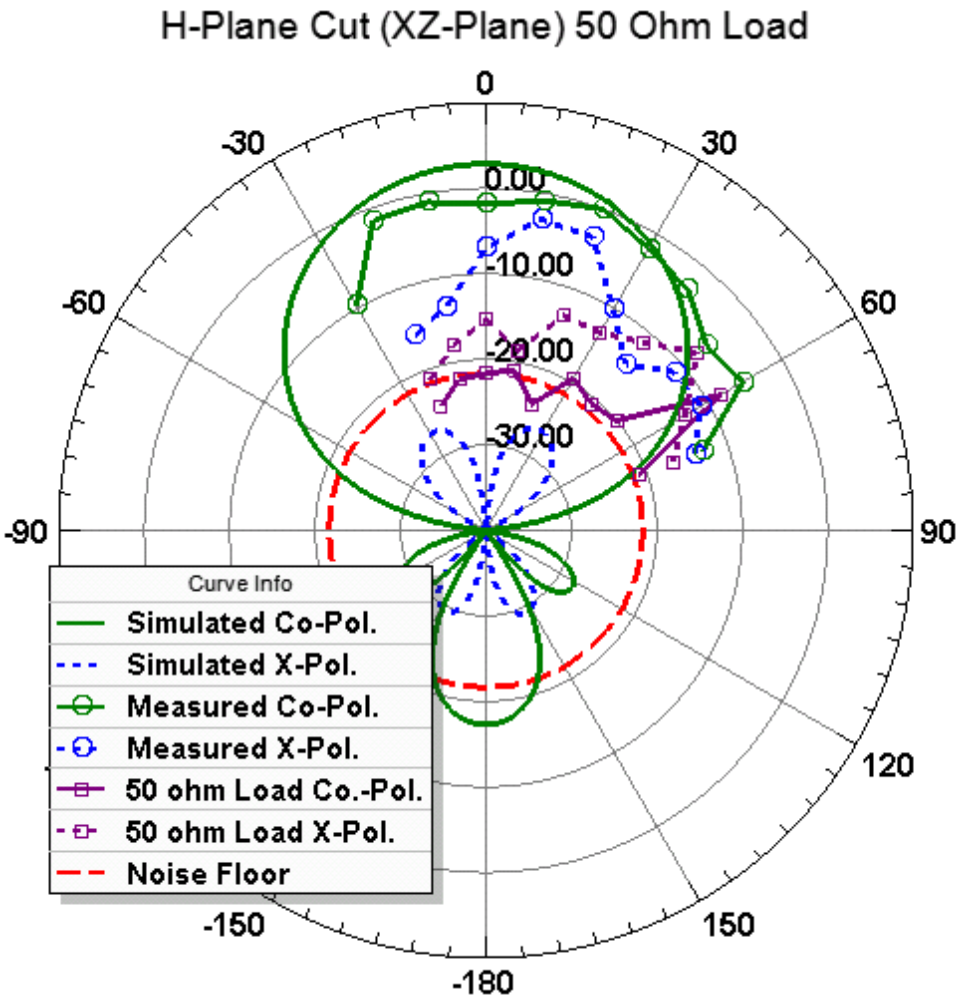

Figure 6.24: This H-plane radiation pattern test shows the RF probe does not effect the antenna pattern measurements of the on-chip patch antenna array. Most of the co-polarized measurements from the RF probe are noise measurements. Additionally, the RF probe is cross-polarized with the AUT which helps reduce its interference.

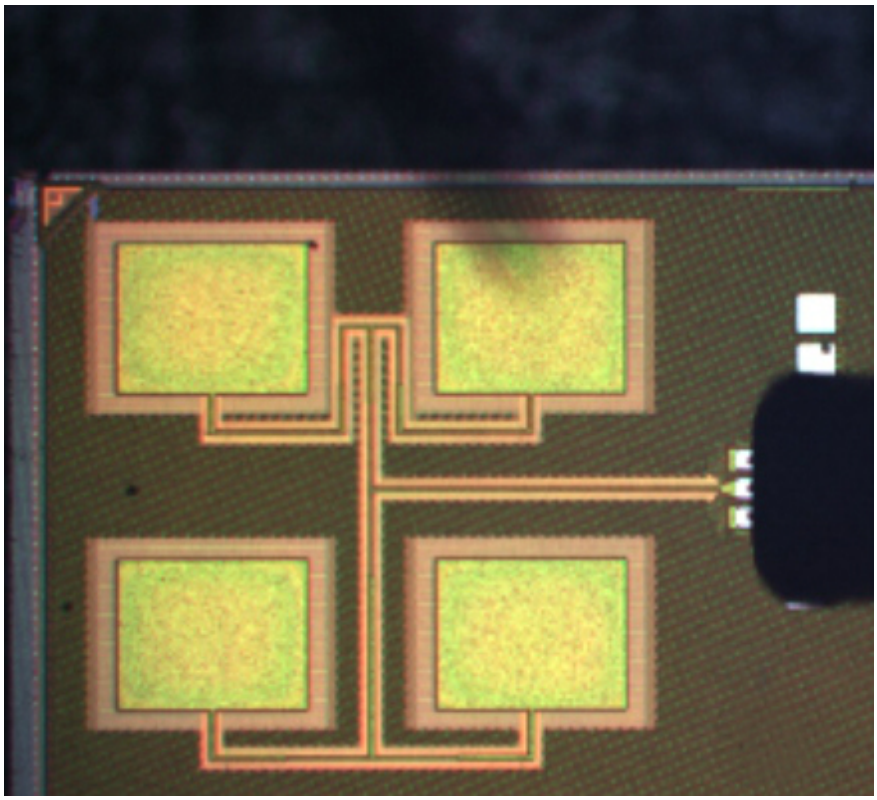

Figure 6.25: Microscope image of DC probe placed just above the on-chip patch antenna array as seen as a blurred dark line. The radiation pattern cut from this environmental test determines how much interference the DC probe creates when measuring an on-chip antenna.

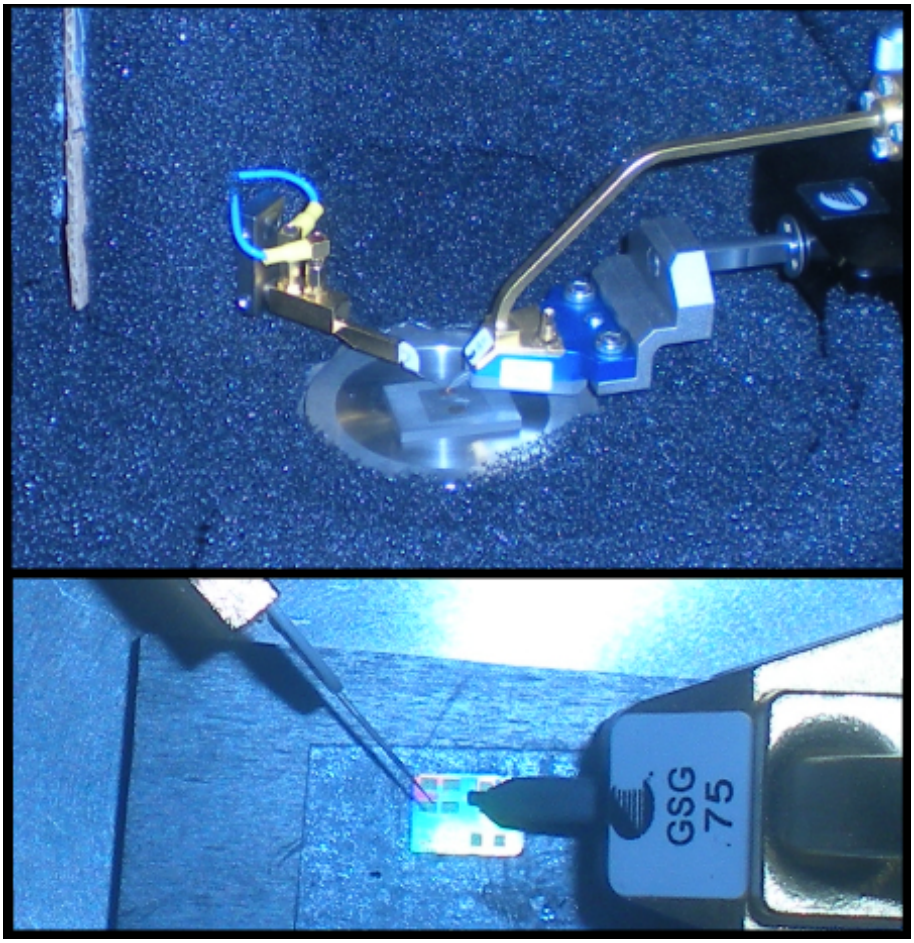

Figure 6.26: A picture of the interfering DC probe hovering just above the on-chip patch antenna array while the RF probe is probing the array. RF absorbing material was applied around the DC probe positioner to reduce reflections.

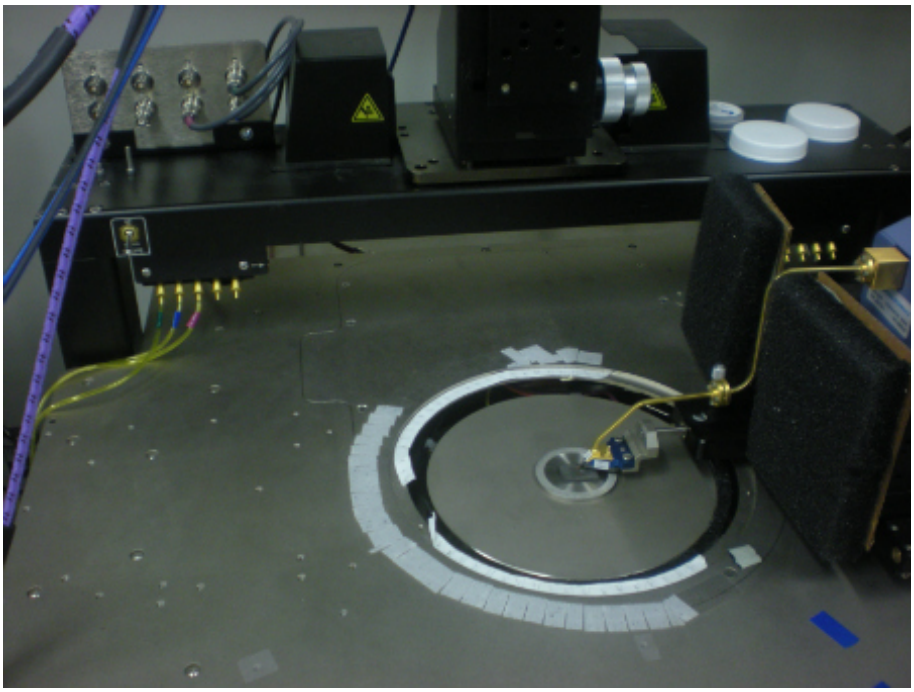

Figure 6.27: A picture of the probe station without RF absorbing material.

6.28 and 6.29, respectively. In both the E-plane and H-plane cuts, very little measurement difference is seen when adding a DC probe or removing RF absorbing material. This is seen for both co-polarized and cross-polarized measurements. In the E-plane, only 1-2 dB variations are measured which can be due to measurement repeatability error. In the H-plane boresight, the DC probe environment does reduce boresight gain by about 2 dB. $+60^{\circ}$ is the only angle that shows deviation up to 5 dB; however, this is mostly seen in the cross-polarized pattern without RF absorber. These environmental tests indicate that on-chip antenna pattern measurements at sub-terahertz frequencies in a probe station environment are quite robust and can be integrated with other wafer-level testing such as digital logic, analog, and RF testing.

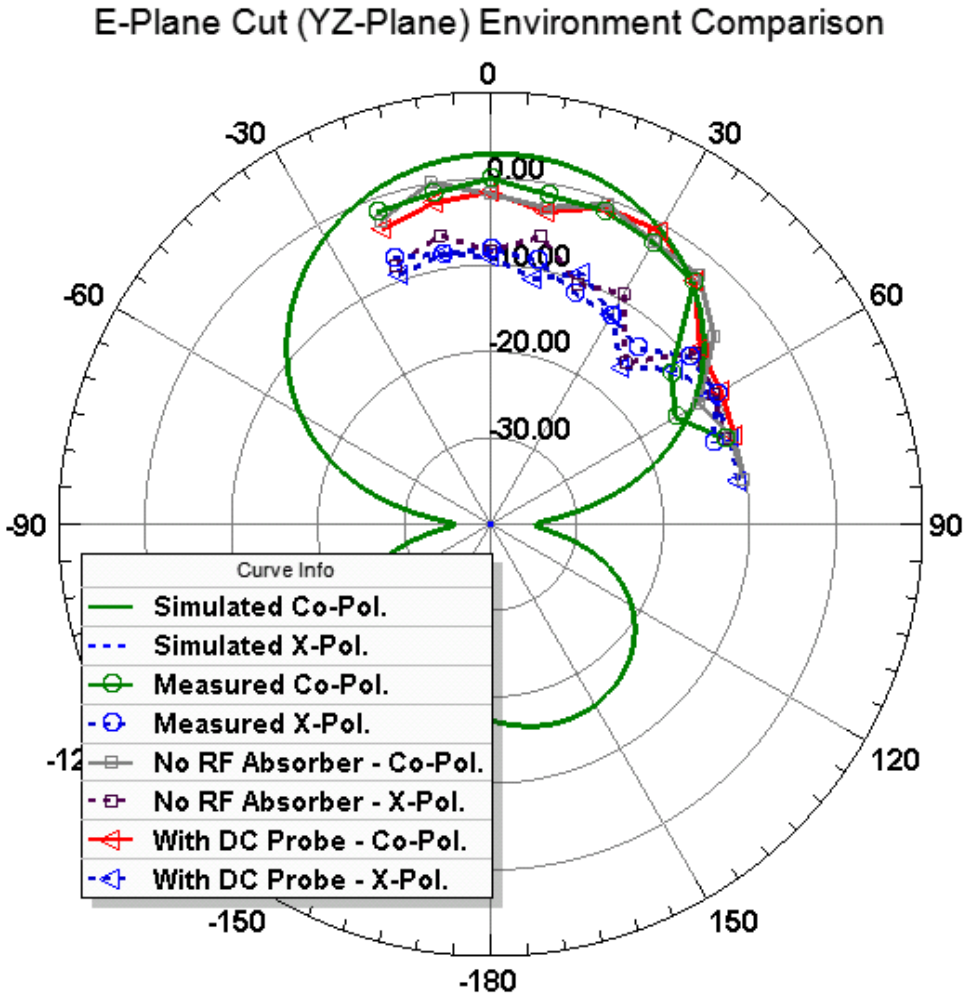

Figure 6.28: When a DC probe is adjacent to the on-chip antenna array, almost no difference is seen in the E-plane radiation pattern measurement. When the RF absorbing material is removed from the probe station environment, almost no difference is seen as well. This indicates that millimeter-wave/sub-terahertz on-chip antenna pattern measurements can be robust in a probe station environment.

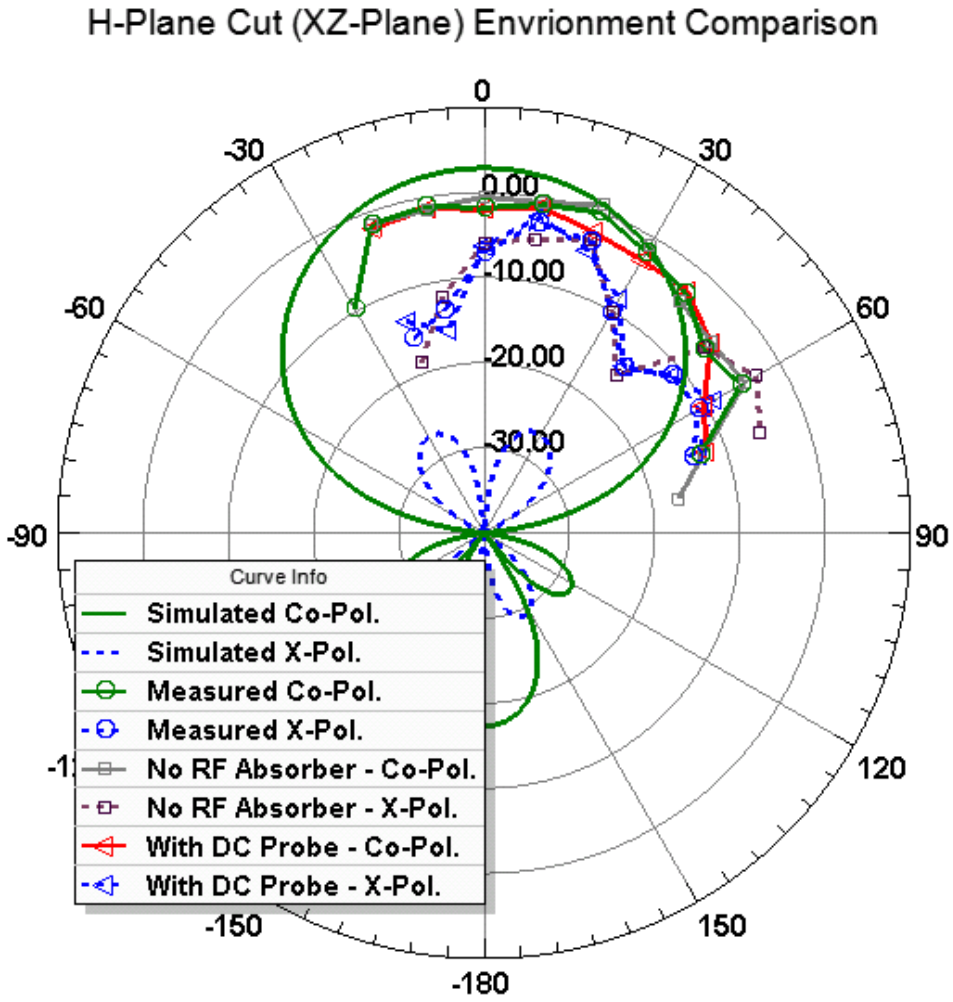

Figure 6.29: When a DC probe is adjacent to the on-chip antenna array, very little difference in the H-plane radiation pattern is measured. At +20°, the DC probe environment reduced gain by about 2 dB, and at +60° the cross-polarized pattern had a deviation up to 5 dB when RF absorber was removed. Other than these two instances, all other angles and polarizations were nearly identical, which indicates that millimeter-wave/sub-terahertz on-chip antenna pattern measurements can be robust in a probe station environment.

Chapter 7

Conclusion And Future Work

This dissertation has focused on designing, fabricating, and testing millimeter-wave and sub-terahertz on-chip antennas using a standard, inexpensive 45 nm SOI CMOS process. This technology has the capability to deliver multi-Gbps data rates in future millimeter-wave and sub-terahertz wireless communications. The recent trends in literature as well as the demand from wireless service providers to alleviate congested cellular networks, indicate that millimeter-wave and sub-terahertz communications are poised to be deployed within the next 10-15 years. These high carrier frequencies provide massive bandwidths and the wireless devices operating at these unprecedented frequencies can be realized using inexpensive CMOS technology. This dissertation provides new technical knowledge in the following ways: 1) understanding how 28 GHz millimeter-waves propagate in dense urban environments for future cellular communications, 2) the design and fabrication of a sub-terahertz on-chip phased antenna array using standard CMOS technology, 3) how to design and construct an accurate sub-terahertz on-chip antenna radiation pattern measurement system in a wafer probe station environment, 4) discovered the negligible effects of nearby DC probes and RF absorbing material in an on-chip antenna pattern measurement system, and 5) highlighted the importance

of designing on-chip antennas in low-loss materials in addition to overcoming the silicon substrate losses.

Before on-chip antennas are widely fabricated and deployed in next-generation wireless communications, several research problems still need solutions. Research on boosting radiation efficiency of on-chip antennas is needed to create high gain antennas while still being compatible with low-cost semiconductor processes. Another open research problem is to understand and quantify any potential self-interference between a radiating on-chip antenna and the underlying DC, analog, and RF electronics on the chip as well as how to overcome this self-interference. Future research work must also understand how an IC package effects the antenna radiation pattern, gain, impedance, and bandwidth of the on-chip antenna. New IC packages may need to be developed to appear electrically invisible to the on-chip antennas much like radomes for radar systems. Lastly, to have reliable mm-wave and sub-THz communications, the on-chip phased antenna arrays must be able to quickly and adaptively steer the antenna beam towards directions that complete the link. Research is then needed on designing and fabricating phase shifters to electrically steer the antenna beam as well as smart searching algorithms to find the best direction to point the antenna. If these research problems are addressed, the future of wireless in the next 10 years will migrate towards millimeter-wave and sub-terahertz frequencies where unused massive bandwidths are available.

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