Pulsed-Duty Characterization of Turn-Off for a Population of SCRs and the Effect of Variation on Equalization Circuit Design

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***Abstract*-- Turn-off characteristics of silicon-controlled rectifiers (SCRs) drive the design of snubber circuits for single devices in power converters. Turn-off characteristics also drive the design of equalization circuits for series-connected devices in power converters. For single devices, the important characteristics are peak recovery current, recovery time, and recovered charge. These characteristics are also important for series-connected devices, but it is the variation in these characteristics that define the equalization requirements. In fact, these variations are used to determine the size and power dissipation of the equalization circuit.**

A population of SPCO 402b pulse-rated silicon controlled rectifiers was tested and recovery characteristics were measured. The differences in recovery characteristics were tabulated and discussed. A method of equalization circuit design based on circuit variations was discussed and circuit design trades are made in light of the variations in recovery characteristics.

I. INTRODUCTION

In the design of converter protection circuits, the turn-off characteristics of the SCR must be accounted for properly. Voltage and current transients at turn-off may damage the device or lead to its unexpected re-triggering. When multiple SCRs are used in series, an additional consideration comes into play, namely the unavoidable range of characteristics among the different devices that lead to unequal voltage and current sharing. It is common practice to protect each SCR individually by means of auxiliary circuits (commonly called snubbers) even when SCRs are used in series and/or parallel combinations. In this case, however, the protective circuits have the additional duty of minimizing the differences in voltages among the SCRs and are referred to as equalizer circuits.

Equalizer circuits are typically divided into two types: static and dynamic, depending on whether their function is to protect the SCR after steady state has been achieved or during transients. We shall limit our discussion to the case of SCRs connected in series and to the simplest and most common form of equalizer circuit (Fig. 1). The equalizer circuit is composed of a single resistor connected in parallel with the SCR, (the static equalizer branch), and a series combination of a capacitor and a resistor in parallel with the SCR (the dynamic equalizer branch).

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II. BACKGROUND

The dynamic equalizer circuit addresses variations, from device to device and in the carrier lifetime. The carrier lifetime is controlled through the introduction of recombination centers within the wafer. Manufacturers use the design of the doping profile and doping technique to distinguish their products from those made by others. Variations of pre-existing defects within wafers and variations in the doping process can both contribute to variations in carrier lifetime from sample to sample.

The reverse recovery charge Q_{rr} is defined [1] as the time integral of the reverse current during recovery, which can be approximated by the expression:

$$Q_{rr} \approx k(di/dt)\ t_s t_{rr} \quad (1)$$

where k is a constant typically of the order of 0.4, di/dt is the time rate of change of the current in the device, t_s is the time interval between the current first crossing zero as it reverses and the current reaching its maximum reverse value, and t_{rr} is the time interval between the current first crossing zero as it reverses and device turnoff. Because both t_s and t_{rr} are proportional to the carrier lifetime [1], the reverse recovery charge varies as the square of the carrier lifetime.

As a result, the voltage and current distributions during device turn-off, unless the external circuit is designed to control the behavior, are determined by the carrier lifetime as is the forward voltage drop during operation. Because this parameter cannot be sufficiently controlled from device to device or from lot to lot, appropriate external circuitry must be used.

III. RECOVERY TEST

In order to properly design an equalizer, it is important to have a realistic characterization of the SCRs during recovery.

For example, our application called for the use of a Silicon Power SPT402B. Tests to determine the recovery characteristics were conducted by discharging a capacitor bank into an inductor. The circuit was adjusted so that with an initial voltage of 2,000 V the peak current was approximately 13.2 kA at 125 μs. A summary of the test data is reported in Table 1 with terms defined in Fig. 2. Note that the externally controlled parameters, I_{pk} and di/dt_{off}, have a standard deviation of less than 1%. The measured value for t_{rr} as a standard deviation of about 2%, and the other measured quantities have a standard deviation between 3.5% and 4.5%. These data suggest that the carrier lifetime is consistent from wafer-to-wafer under the tested conditions.

The values for I_{rm} were correlated with those furnished by the SCR manufacturer for each device and the results shown in Fig. 3. It can be seen that although a general correlation exists, that correlation is not very high. This is likely due to the fact that the manufacturer's tests were done at a lower voltage and current (1,000 V, 4,000 A, 11 A/μs). Under these test conditions, it is less likely to attain a small standard deviation due to the nonlinear relationships among the various parameters of interest. Therefore, the degree of correlation is probably an indication of the difficulty in making robust measurements under all conditions rather than an indication of variation in device behavior.

IV. EQUALIZATION CIRCUIT DESIGN

A primary concern of a converter designer is the protection of the switching devices from spurious turn on, too-fast turn on, overheating, and over voltage [1,2]. Because thyristors are often stacked in series strings in order to achieve higher operating voltage, there is a particular concern regarding over voltage. This concern arises from the fact that SCRs connected in series do not share voltage equally, either during steady-state or recovery [3]. This problem is addressed through the use of a static and a dynamic equalizer.

Under steady-state conditions, a static equalizer (a grading resistor) is needed to force the voltages across each series SCR to be equal. The choice of the grading resistor must balance the need for sufficient current draw to provide an effective equalization and the need to minimize the power loss. At steady state, the worst-case voltage imbalance in a stack of SCRs in series will occur when one SCR has the lowest leakage while the others have the maximum. As a result, the first SCR will have to withstand a higher voltage than the others. The relationship of leakage current versus voltage in each SCR can be modeled as a piecewise linear function with zero leakage for voltages less than a minimum v_0 and a straight line of different slope for voltage beyond the minimum. This slope allows replacement of each SCR in the stack with an equivalent resistor. Then we simply need to solve the resistor network made up of the SCR's equivalent resistors and the grading resistors. For example, in the case of three SCRs stacked in series, R is the value of the grading resistors, R_1 is the resistance of the two high-leakage SCRs, and R_2 is the resistance of the low-leakage SCR. Then, if V is the voltage across the whole stack, the voltage v_2 across the low leakage SCR will be given by (see Fig. 4)

$$v_2 = \frac{\left[(a+1)V - 2av_0\right]x + 2av_0}{(a+3)x + 2a} \qquad (2)$$

where $x = R_2/R_1$ and $a = R/R_1$. The more x exceeds the ideal value of 1, the more v_2 exceeds the ideal value of $V/3$. This allows us to establish limits for v_2 and choose a grading resistor accordingly.

The function of a dynamic equalizer is to force voltage sharing under transient conditions. A dynamic equalizer is the same in form as a snubber. In fact, a complete design of a protection circuit must account for equalizing, voltage limiting, and dv/dt limiting functions. The final circuit design will be the result of several iterations and final compromise between the needs of dynamic equalization and those of individual SCR protection. Details about the dynamic equalizer section when working as a snubber are given in a concomitant paper [4]. Here we are concerned only with the equalizing role of the circuit.

The required analysis can be carried out in a manner similar to that of the static equalizer. If we concern ourselves only with the turn-off process, the analysis shows that a crucial role is played by the quantities that define the recovery characteristics of the SCRs. This is not surprising as it mirrors the situation already discussed for the static equalizer, where the leakage parameters were the defining factors in the circuit performance. Although the model one assumes for the SCR during recovery has an impact on the results [5,6], we need only be concerned with the recovery characteristics shown in Fig. 5.

Fig. 5 shows the response of two different thyristors during recovery in identical circuits with identical driving functions. The difference in the two circuit responses arises from the differences in stored charge in each device. When a string of thyristors switches from the conducting state to the blocking state, the time required for conduction to stop and for reverse blocking to occur is a function of the junction's recovered charge (Q_{rr}). Because no two cells are ever manufactured exactly alike, the charge recovered by any two cells is different. As a result, the device with less recovered charge turns off more quickly than the device with more recovered charge.

If these two (or more) devices are connected in series, then the device that turns off first supports the entire impressed voltage for the interval of time represented by $t_5 - t_3$. Note that the time intervals $t_3 - t_1$ and $t_5 - t_1$ are distinct from the time required for the devices to support forward voltage (or turn-off interval), T_q. If the devices were connected in series in the first place in order to achieve a higher operating voltage than was possible using only a single device, then a device

over-voltage, and potentially failure, would almost certainly occur. This situation is exacerbated by the fact that the reduction in reverse current for the second device will lengthen its recovery time, and therefore the time before it is able to support reverse voltage.

The difference between the recovery characteristics of the device is

$$\Delta Q = q_2 - q_1 \tag{3}$$

where

$$q_1 \approx \int_{t_1}^{t_3} i_1 dt < q_2 \approx \int_{t_1}^{t_5} i_2 dt \,. \tag{4}$$

Adequate voltage sharing between thyristors in series is achieved by connecting shunt elements, as shown in Fig. 6. These elements provide a current path around the faster devices during recovery. As a result, the voltage on a thyristor is limited by the rate at which the shunt capacitor charges. Therefore, the capacitor must be chosen based on the worst-case operating conditions. These conditions are defined by $\Delta Q_{\max}$ for a population of thyristors, the impressed voltage during recovery, the number of devices connected in series and the voltage rating of the devices in the string. The worst case for dynamic voltage sharing occurs when one device has the minimum recovered charge, and therefore the fastest recovery, and all of the other devices in the string have the maximum stored charge, and therefore the slowest recovery.

Fig. 7 shows a string of n thyristors connected in series along with a shunt-connected capacitor. The resistance required to limit the capacitor discharge current is neglected. The voltage is dropped along each element so that

$$V_s = V_1 + V_2 + ... + V_n \tag{5}$$

so that, for perfect sharing,

$$V_1 = V_s \big/ n \,. \tag{6}$$

Because the recovery characteristics of the devices are not the same, the shunt capacitors do not charge at the same rate or to the same voltages

$$V_{cap} = 1 \big/ C \int i dt \approx \frac{i\Delta t}{C} \approx \frac{q}{C} \,. \tag{7}$$

Following the method in [3] and neglecting the differences in shunt capacitors, the maximum difference in capacitor voltage is

$$\Delta Q_{\max} = C_n \Delta V_{\max} \,. \tag{8}$$

With reference to Fig. 7, if $V_2 = V_3 = \ldots = V_n = V_0$, then $V_s = V_1 + (n-1)V_0$, but also $\Delta V_{\max} = V_1 - V_0$ by definition. Therefore, combining these last two relationships with (8) we obtain the voltage on the worst-case cell

$$V_1 = \frac{V_s}{n} + \frac{\Delta Q}{C_n}\frac{n-1}{n}, \tag{9}$$

where $n-1$ represents the ΔQ condition of devices $n = 2, 3, \ldots n$.

Let V_{rated} be the maximum voltage allowed on a single device. If the condition $V_1 < V_{rated}$ is imposed, then

$$V_{rated} > \frac{V_s}{n} + \frac{\Delta Q}{C_n}\frac{n-1}{n} \tag{10}$$

which can be solved for the minimum value of shunt capacitance

$$C > \frac{\Delta Q(n-1)}{nV_{rated} - V_s} \,. \tag{11}$$

The worst-case analysis should also include variations in the capacitors. The nominal capacitance of each capacitor in a population of capacitors is

$$C_{nom} = \frac{C_1 + C_2 + ... + C_n}{n} \,. \tag{12}$$

If the case described above is modified by the additional consideration that

$$C_1 < C_2 = C_3 = \ldots C_n \tag{13}$$

and

$$C_1 = C_{nom} - C_{tol} C_{nom} \tag{14}$$

where C_{tol} represents the maximum variation in capacitance, then (10) is modified so that

$$V_{rated} > V_s \frac{1 + C_{tol}}{n + C_{tol}} + \frac{\Delta Q}{C_n}\frac{n-1}{n + C_{tol}} \tag{15}$$

and

$$C_n > \frac{\Delta Q(n-1)}{V_{rated}(n + C_{tol}) - V_s(1 + C_{tol})} \,. \tag{16}$$

One of the results of the testing described above was the tabulation of recovered charge for a population of devices under various operating conditions. Table 1 shows recovered charge tabulated against peak current and di/dt_{off}. It is apparent that the amount of recovered charge is, at best, a weak function of both of these variables for the range tested. Consequently, for the test conditions used in this investigation, the variation in stored charge can be assumed a device variation and not a variation due to operation.

The variations in recovery characteristic have a substantial impact on the design of the circuit. From (11) it can be seen that the size of the capacitor is dependent on the worst-case difference in charge, the numbers of devices in series, the impressed voltage, and the device rated voltage. As an example, the capacitor mass per device was calculated for a 5 kV device for four different series combinations. In each case, the impressed voltage was set such that the voltage on each device was near its rating. The capacitor mass-per-thyristor was calculated using off-the-shelf capacitor technology based on the resulting capacitance value. From Fig. 8, it is obvious that capacitor mass increased with device variability. Perhaps a less obvious result is that, as impressed voltage is increased and more devices are required in series, capacitor mass is greater for the same $\Delta Q_{\max}$.

In order to complete the trade analysis, $\Delta Q_{\max}$ was held constant at 9 mC while n and the impressed voltage were varied. Fig. 9 shows that capacitor mass falls dramatically as a few cells are added in series but quickly levels. This shows that if recovered charge variation is high, then adding a large

number of cells in series will not significantly reduce equalization circuit mass. This result is in contrast to traditional snubber circuit and voltage overshoot limiting circuit design, where the dv/dt or overshoot on an individual cell is always reduced by adding more series cells and the protection circuit capacitances on each cell can therefore be reduced.

V. CONCLUSION

The influence of SCR turn-off characteristics on the design of equalizer circuits has been examined in detail for both cases of static and dynamic equalizers. General expressions useful in the selection of circuit components have been derived for the case of multiple SCRs connected in series. Additionally, the impact of the variability of the capacitance value in the snubber circuit has been discussed. Test results obtained with SCR type SPCO-402b have also been presented and the results of the foregoing analysis have been applied to this specific case exemplifying some of the design trades possible.

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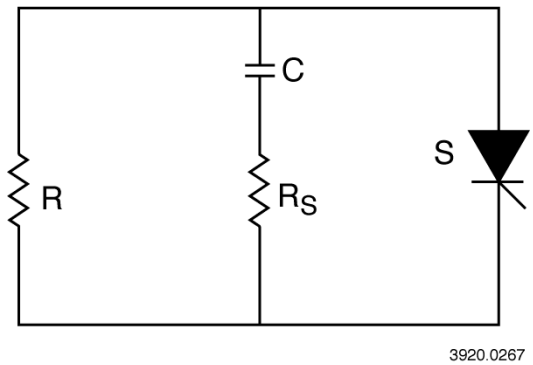

Fig. 1. SCR with equalizer circuit

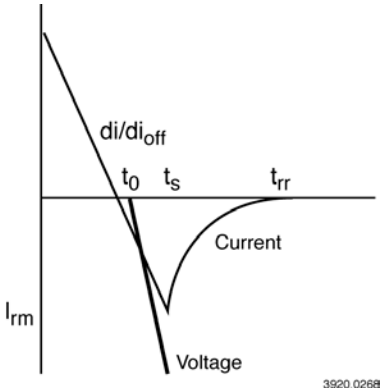

Fig. 2. SCR characteristic curves and quantities during recovery

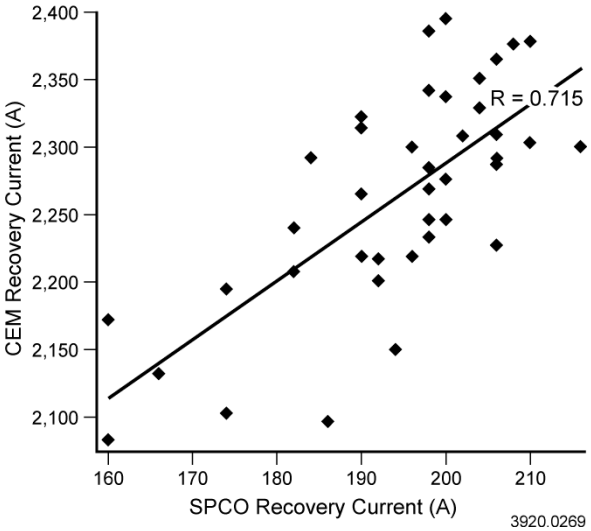

Fig. 3. Correlation of reverse recovery current measurements at UT-CEM and SPCO.

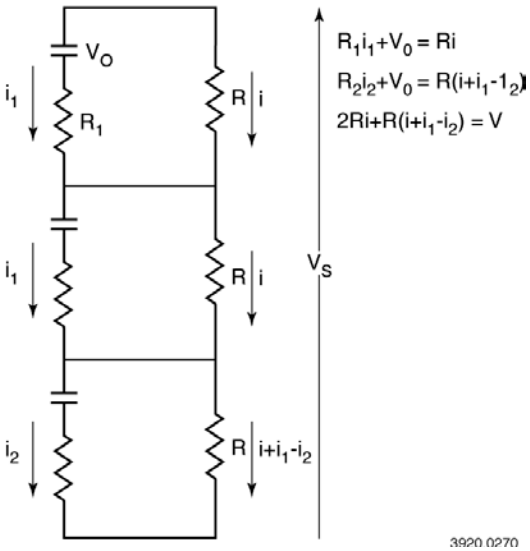

Fig. 4. Static circuit for evaluation of grading resister requirement.

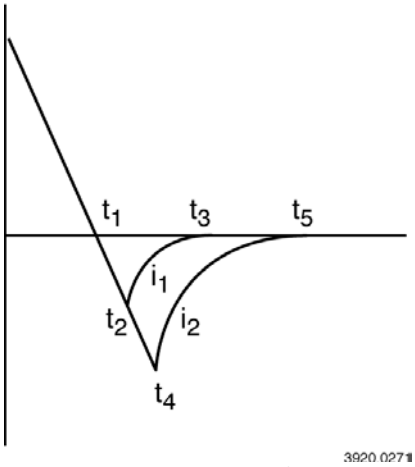

Fig. 5. Recovery characteristic of two thyristors.

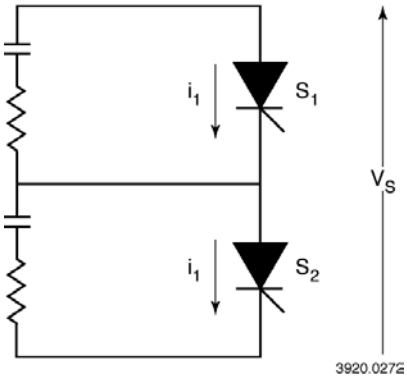

Fig. 6. Series thyristors with an elementary equalization network.

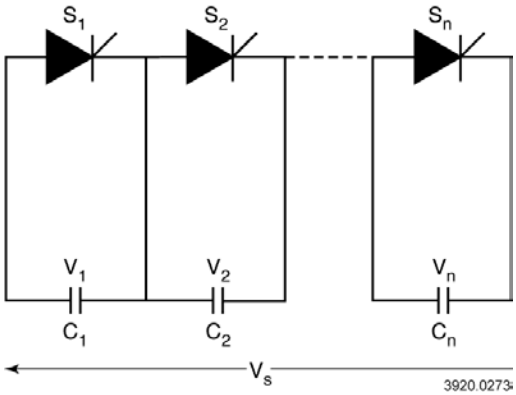

Fig. 7. A string of thyristors with shunt capacitors.

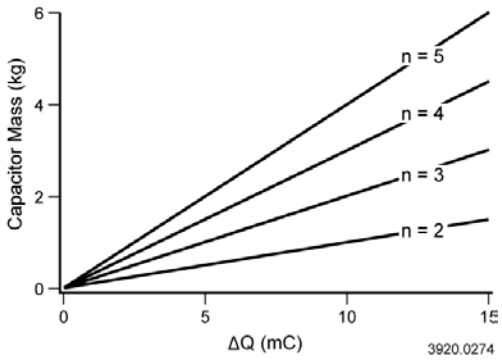

Fig. 8. Capacitor mass as stored charge and n are varied.

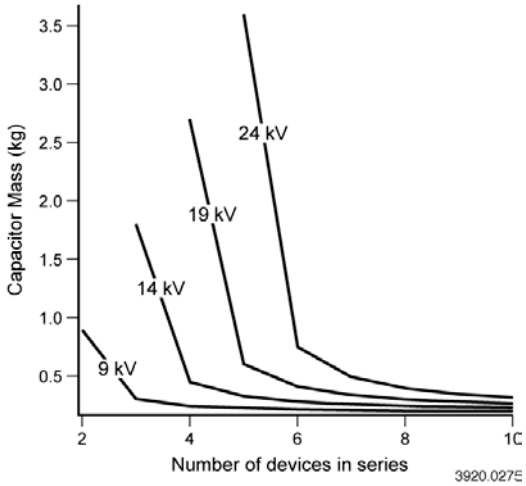

Fig. 9. Capacitor mass as n and impressed voltage are varied

TABLE 1
SUMMARY OF SCR TESTS

Device	di/dt_{off} (A/μs)	I_{rm} (A)	t_0 (ms)	t_s (ms)	t_f (ms)	t_{rr} (ms)	Q_{rr} (C)	I_{pk} (A)
1	159.73	2,284.8	0.0110	0.0161	0.0298	0.0459	0.046	13,180
2	159.59	2,216.6	0.0106	0.0157	0.0302	0.0459	0.044	13,173
3	160.97	2,103.4	0.0102	0.0146	0.0318	0.0464	0.041	13,260
4	164.77	2,171.6	0.0100	0.0148	0.0318	0.0466	0.043	13,571
5	159.66	2,291.8	0.0111	0.0162	0.0293	0.0455	0.047	13,163
6	156.48	2,328.9	0.0110	0.0167	0.0275	0.0442	0.047	12,913
7	160.69	2,314.1	0.0110	0.0162	0.0291	0.0453	0.047	13,234
8	159.79	2,245.5	0.0109	0.0158	0.0302	0.0460	0.045	13,185
9	159.17	2,276.4	0.0108	0.0161	0.0294	0.0455	0.046	13,108
10	160.28	2,322.1	0.0115	0.0162	0.0290	0.0452	0.047	13,177
11	158.14	2,207.9	0.0106	0.0158	0.0311	0.0469	0.045	13,041
12	159.38	2,287.3	0.0109	0.0161	0.0285	0.0446	0.046	13,138
13	159.45	2,341.6	0.0115	0.0165	0.0286	0.0451	0.048	13,108
14	160.62	2,376.3	0.0112	0.0167	0.0280	0.0447	0.049	13,210
15	161.45	2,364.8	0.0112	0.0165	0.0289	0.0454	0.049	13,253
16	159.24	2,227.3	0.0106	0.0157	0.0298	0.0455	0.044	13,167
17	159.66	2,096.8	0.0102	0.0147	0.0311	0.0458	0.040	13,194
18	160.36	2,246.1	0.0107	0.0157	0.0296	0.0453	0.044	13,226
19	160.14	2,083.1	0.0099	0.0147	0.0326	0.0473	0.041	13,220
20	159.93	2,132.3	0.0102	0.0160	0.0316	0.0476	0.042	13,213
21	160.07	2,269.0	0.0109	0.0160	0.0291	0.0451	0.045	13,223
22	159.93	2,303.3	0.0109	0.0162	0.0289	0.0451	0.046	13,209
23	158.62	2,195.0	0.0107	0.0155	0.0306	0.0461	0.044	13,094
24	160.00	2,239.8	0.0106	0.0158	0.0303	0.0461	0.045	13,218
25	159.86	2,200.6	0.0106	0.0155	0.0317	0.0472	0.044	13,212
26	160.00	2,149.9	0.0104	0.0151	0.0327	0.0478	0.043	13,217
27	160.14	2,308.1	0.0111	0.0162	0.0288	0.0450	0.046	13,219
28	159.79	2,300.0	0.0109	0.0162	0.0289	0.0451	0.046	13,217
29	162.77	2,351.3	0.0112	0.0163	0.0291	0.0454	0.047	13,439
30	160.00	2,337.4	0.0113	0.0165	0.0293	0.0458	0.047	13,227
31	160.07	2,264.5	0.0110	0.0161	0.0296	0.0457	0.045	13,225
32	159.86	2,291.1	0.0110	0.0162	0.0297	0.0459	0.046	13,207
33	159.73	2,378.4	0.0115	0.0169	0.0292	0.0461	0.049	13,208
34	160.07	2,395.0	0.0113	0.0167	0.0278	0.0445	0.049	13,156
35	159.38	2,284.3	0.0113	0.0161	0.0288	0.0449	0.044	13,198
36	160.28	2,385.8	0.0117	0.0167	0.0283	0.0450	0.049	13,168
37	159.66	2,219.3	0.0107	0.0157	0.0307	0.0464	0.044	13,200
38	160.00	2,233.7	0.0107	0.0158	0.0308	0.0466	0.044	13,226
39	160.14	2,232.6	0.0107	0.0157	0.0307	0.0464	0.044	13,228
40	159.24	2,219.3	0.0107	0.0157	0.0291	0.0448	0.040	13,177
Avg	159.98	2,261.9	0.010858	0.0159	0.0298	0.0457	0.045	13,200
StdDev	1.20	80.5	0.000416	0.0006	0.0013	0.0009	0.002	96
Max.	164.77	2,395.0	0.0117	0.0169	0.0327	0.0478	0.049	13,571
Min.	156.48	2,083.1	0.0099	0.0146	0.0275	0.0442	0.040	12,913

Note: I_{pk} = peak current during discharge; $t_f = t_{rr} - t_s$