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Intrinsic Unipolar SiO_x-based Resistive Switching Memory: Characterization, Mechanism and Applications

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Intrinsic Unipolar SiO_x-based Resistive Switching Memory: Characterization, Mechanism and Applications

by

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Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

August, 2015

To my parents

Acknowledgements

First and foremost, I would like to express my gratitude to my Ph.D. advisor Professor Jack C. Lee for being such a great mentor guiding me throughout my research and study. He has always been responsible, supportive, attentive and encouraging. I would like to thank him for all the valuable discussions which consolidate my knowledge on device physics and lead me into the cutting-edge research. His effective management style helps to keep me on the right tract of research while also leave me enough space to advance myself and bring out new ideas. It is a great experience working under Professor Lee's supervision, not only because of his knowledge on semiconductor research and industry, but also his active personality that teaches me to be open-minded and always keep heads up.

I'm grateful for all the supports from my dissertation committee Prof. Deji Akinwande, Prof. Edward T. Yu, Prof. Paul S. Ho and Dr. Burt W. Fowler. I would like to thank them for their suggestions and advices to make this Ph.D. work better.

I would like to thank my group members and colleagues for their continuous support. This dissertation could not be accomplished without their assistance. I really appreciate the help and guide from senior group member Dr. Yen-ting Chen and Dr. Burt W. Fowler, who trained me on all the device fabrication and characterization techniques. Without their solid work and rich experiences on SiO_x-based resistive switching devices, I would not be able to initiate my research on SiO_x-based resistive switching devices so smoothly. I would like to thank them for being so generous to pass down their knowledge and experiences. Special thanks go to my colleague Fei Zhou, who gives me tremendous help throughout my research. Without his help, the fabrication process for scaled devices

could not be set up in such a short time. I would like to thank him for his sincere encouragement and caring. I'd also like to extend my gratitude to my fellow group members Dr. Yanzhen Wang, Dr. Fei Xue, Pai-Yu Chen, and Brad Bringhurst for their assistance and support.

I would like to express my deepest gratitude to my family. I appreciate my parents for their selfless love and endless support. Words won't be enough to thank them for being there for me whenever I need them. Many thanks to my beloved wife Chen for making my life colorful, easing my nerves, and encouraging me to pursue my dreams.

Finally, I'm grateful for this Ph.D. journey. What I learned here is far beyond research itself. I think the biggest difference between us human beings and the other animals is that we accumulate knowledge. No matter how far away the goal is, it can be reached step by step. No matter how huge the task is, it can be finished piece by piece. Even if at the end you couldn't get to the finish line yourself, someone else will carry on. Or, maybe there isn't any finish line. That's how we keep reaching. So don't worry if you don't see any improvement today, or your device failed, or your boss think your idea is worthless. Just keep your head up, and show the world the most undefeatable human stubbornness.

Intrinsic Unipolar SiO_x-based Resistive Switching Memory: Characterization, Mechanism and Applications

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The University of Texas at Austin, 2015

Supervisor: Jack C. Lee

Floating gate (FG) nonvolatile memory has been the main structure of nonvolatile memory devices, since its invention in 1967 by D. Kahng and S. M. Sze. They have been widely employed in the portable electronic products such as mobile phones, digital cameras, notebook computers, mp3 players and USB flash drives. However, as device size continues to shrink, the typical flash memory device will continue to suffer from issues of retention and endurance. In order to solve the problems, researchers have considered new storage layers and novel structures in nonvolatile memory devices to replace the conventional floating gate device. Therefore, a great deal of potential memory structures have been proposed, with some transferring into a production line, such as phase change memory (PCM), magnetic random access memory (MRAM) and ferroelectric random access memory (FeRAM). In the innovation of memory devices, resistance random access memories (ReRAMs) have gained significant research interest as an alternative for next-generation nonvolatile memory due to its high density, low cost, low power consumption, fast switching speed and simple cell structure.

In this dissertation, the intrinsic unipolar silicon oxide (SiO_x-based) Resistive-RAM (ReRAM) characterization, mechanism and applications have been presented. I investigate device structures, material compositions and electrical characteristics to

realize ReRAM cells with high ON/OFF ratio, low static power consumption, low switching power, and high readout-margin using complementary metal-oxide-semiconductor (CMOS) compatible SiO_x-based materials. These ideas are combined with the use of horizontal and vertical device structure designs, composition optimization, electrical controlling and external factors for understanding resistive switching mechanism. Modeling of resistive switching mechanism, including temperature effect, pulse response and carrier transport behaviors are performed, to develop a compact model in energy diagram, trap-level information in SiO_x resistive switching layer, even for computer-aided design (CAD) in very-large-scale integration (VLSI) design. Finally, synapse-based neuromorphic system is demonstrated in SiO_x-based ReRAM, combining with bio-inspiration and biomimetics process illustrations. This work presents the comprehensively investigation of SiO_x-based resistive switching characteristics, mechanisms, applications for future post-CMOS devices era.

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Chapter 1: Introduction

1.1 History of Memory

If there was no record of culture relics and words for civilization, the era never existed in the past. People portrayed everything of life at different times in natural materials, such as stone, metal, and wood, to inherit the experience of life and prove the existence of once to be passed along. However, because the carriers of civilizations are bulky and difficult to be depicted and wrote by people, the life experience and scientific civilization can only be spread in the same place. When a major disaster or a big famine comes to here, people are forced to migrate to other environments, leading to the accumulated experience and knowledge of civilization making a fresh start. With the evolution of the times, the inventions of paper and printing bring people a convenient and light carrier of words, which causes the appearance of book. Not only the knowledge and ideas can be duplicated in books, but also they can be easily spread around the world. These inventions will make many people share the achievements of civilization. Owing to the continuous accumulation and growth of knowledge, the amount of papers and books used to store all civilizations also increase dramatically. In order to conserve these books and record the civilizations, people continue to set up the library around the world. But the space is limited; people are bound to find new ways to store knowledge. As the advent of the digital age, the problem of expansion of knowledge and information will be solved for human being.

Since the advent of the digital era, the way of digital memory is continuously in progress. Since the holes cards, magnetic matrix, tapes, magnetic cards, and hard disk used successively to nowadays flash memory invented by Simon M. Sze, the capacity and density of digital memory continues to upgrade and the speed also continuously increases. With the rise of portable electronic and Internet operations, knowledge of

people around the world communicates and delivers fast anytime and anywhere. The uploaded content is no longer just text but using the manner of photos, video, and sound to record moments of life in detail, even using the websites, blogs, Facebook, etc. to communicate with each other. These progress and development are attributed to digital electronic technology and digital memory evolution.

1.2 Evolution of Nonvolatile Memory

In Floating gate (FG) nonvolatile memory has been the main structure of nonvolatile memory devices, since its invention in 1967 by D. Kahng and S. M. Sze. They have been widely employed in the portable electronic products such as mobile phones, digital cameras, notebook computers, mp3 players and USB flash drives. The typical structure of a nonvolatile flash memory device is shown in Figure 1.1. The operating principle of conventional nonvolatile memory is based on the use of polycrystalline silicon as a floating gate to store charges injected from a channel [1]. Once charges are present in the floating gate, the threshold voltage of the memory device is changed. The logical signal “0” and “1” is thereby defined by the level of threshold voltage. However, as device size continues to shrink, the typical flash memory device will continue to suffer from issues of retention and endurance. As the typical flash memory device scales down to the nanoscale, stored charges in the floating gate can easily tunnel through the tunnel oxide to the Si substrate [2]. The reason for this is that the thickness of the scaled tunnel oxide cannot provide enough blocking effect to keep the stored charges. Additionally, the presence of leakage paths in the tunneling oxide, created after thousands of operations, will cause a rapid and complete loss of stored charges in a floating gate with a continuous polycrystalline semiconductor layer.

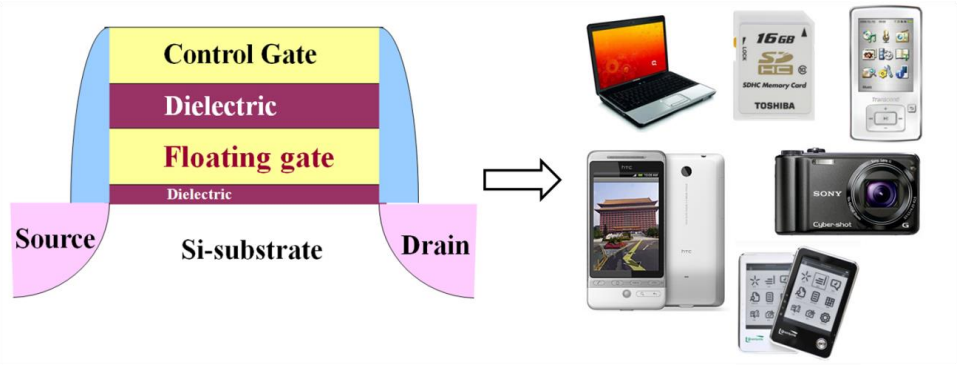

Figure1.1 Device structure of conventional nonvolatile flash memory and its application on electronics products

In order to solve the above-mentioned problems, researchers have presented two main methods to improve memory devices with different storage technologies: (1) methods which change the storage layer without changing the device structure and (2) methods proposing novel structures. In order to change the storage layer, either silicon nitride (served as a trapping layer in SONOS (silicon/oxide/nitride/oxide/silicon)) [3-6] or discrete nanocrystals [7-11] have been employed as storage cells (Figure 1.2). The stored charges can exist in the trap states of the charge trapping layer or can be retained in the distributed nanocrystals to maintain the memory function, even if localized leakage paths are present in the tunneling oxide.

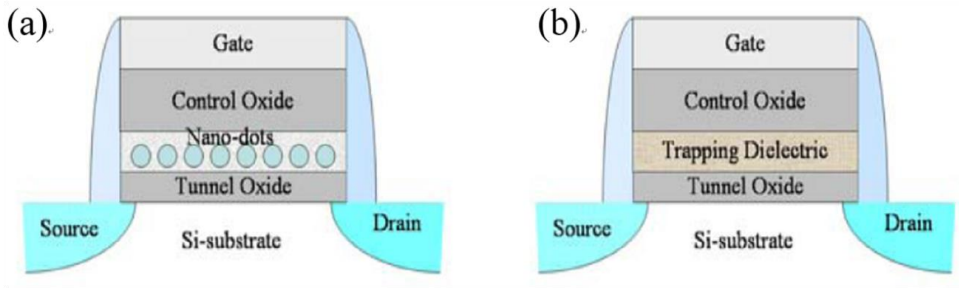

Figure1.2 Nonvolatile memory with (a) nanocrystal structure and (b) trapping dielectric structure.

However, making changes to the storage layer still cannot solve issues of scale-down and program/erase speed. Therefore, researchers have considered new storage layers and novel structures in nonvolatile memory devices to replace the conventional floating gate device. The new nonvolatile memory devices must exhibit better program/erase speed and endurance. As for the scale-down requirements, the new device should be compatible with cross-point structure. Therefore, a great deal of potential memory structures have been proposed (Figure 1.3), with some transferring into a production line, such as phase change memory (PCM) [12], magnetic random access memory (MRAM) [13] and ferroelectric random access memory (FeRAM) [14]. In the innovation of memory devices, resistance random access memories (ReRAMs) have gained significant research interest as an alternative for next-generation nonvolatile memory [15-20] due to its high density, low cost, low power consumption, fast switching speed and simple cell structure. In addition, ReRAMs can possess program/erase speeds as high as SRAM, density as high as DRAM and nonvolatility for flash memory; therefore, ReRAMs demonstrate an extremely high potential for replacing NAND flash and DRAM to become the next-generation nonvolatile memory.

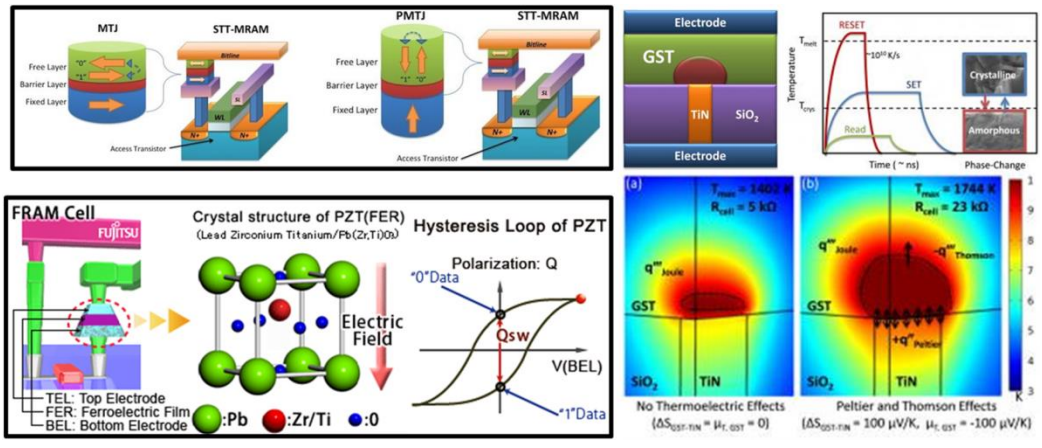

Figure1.3 Potential memory structures: MRAM, FeRAM, and PCM.

1.3 NOVEL DEVICE ARCHITECTURE – RESISTIVE RAM (RERAM)

The structure of ReRAM devices consists of sandwiched metal/insulator/metal (MIM) layers. By applying voltage or current, the resistance of the device can be changed, thereby giving the device data storage characteristics (Figure 1.4). ReRAM first originated from Hickmott in the 1960s; he discovered that the resistance of AlO_x could be modified after voltage or current operation. In recent years, the resistive switching behaviors of a large variety of materials have been reported, including binary metal oxides such as NiO, CuO and HfO_x. The logic state "0" or "1" is defined by different resistance values, and can be read by applying a low voltage to measure the resistance state (Figure 1.5). ReRAM devices exhibit good nonvolatile characteristics, and the stored data can be retained until the next data is written. It does not suffer from the issues of conventional flash memory does, which uses a continuous polycrystalline semiconductor layer as storage layer, in which the presence of leaky paths in the tunneling oxide will cause a rapid and complete loss of stored charges after thousands of operations. Unlike conventional flash memory, ReRAM uses resistance value to define the data state, and because its resistance state can be retained for a long time, ReRAM has better data storage capability (including switching speed, switching energy, and operation voltage) (Table 1.1) [21-23]. Characteristics such as low operation voltage, a fast program/erase speed and good scale-down capability make ReRAM a suitable candidate for the next-generation of nonvolatile memory. Hence, ReRAM is gaining significant interest in academia and industries for its high practicality and potential for commercial uses.

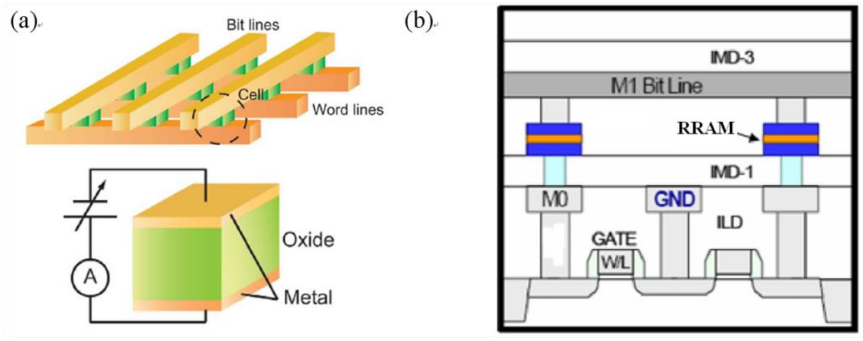

Figure1.4 Schematic structures of (a) 1R (ReRAM) device and (b) 1T (transistor) - 1R (ReRAM).

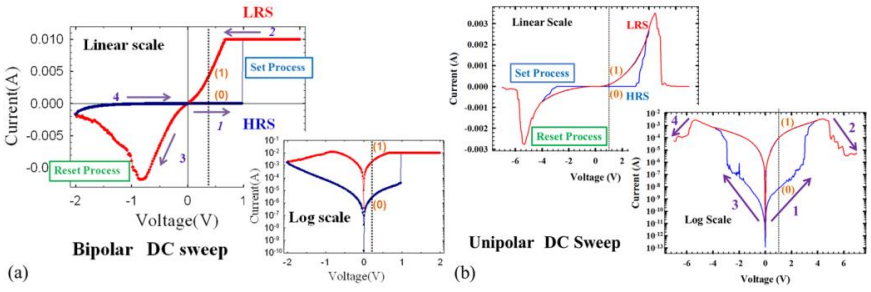

Figure1.5 Switching characteristics of ReRAM device (a) bipolar-type and (b) unipolar-type of SiO_x-based ReRAM.

	Prototypical (Table ERD3)			Emerging (Table ERD5)					
					Redox RRAM				Others
Parameter	FeRAM	STT-MRAM	PCRAM	Emerging ferroelectric memory	Conducting bridge	Metal Oxide: Bipolar Filament	Metal Oxide: Unipolar Filament	Metal Oxide: Bipolar Interface Effects	Carbon-based Memory, Mott Memory, Macro-molecular Memory, Molecular Memory
Scalability	☹	😐	☺	😐	☺	☺	☺	☺	?
MLC	☹	☹	☺	☹	☺	😐	😐	😐	?
3D integration	☹	😐	☺	☹	😐	☺	☺	☺	?
Fabrication cost	😐	😐	😐	😐	😐	☺	😐	😐	?
Retention	😐	😐	😐	😐	😐	☺	😐	☹	?
Latency	☺	☺	😐	☺	😐	😐	😐	😐	?
Power	☺	😐	☹	☺	☺	😐	☹	😐	?
Endurance	☺	☺	😐	😐	😐	😐	☹	😐	?
Variability	☺	☹	😐	😐	😐	☹	☹	☺	?

	☹	😐	☺
Scalability	F_{min} >45 nm	F_{min}=10-45 nm	F_{min} <10 nm
MLC	difficult	possible	feasible
3D integration	difficult	possible	feasible
Fabrication cost	high	medium	low
Retention	poor (<<1yr)	modest (>1yr)	long (>10yrs)
Latency	long (>10us)	medium (0.3-10us)	short (<300ns)
Power	high	medium	high
(Demonstrated Write) Endurance	≤1E5 cycles	≤1E10 cycles	>1E10 cycles
Variability	problematic	reasonable	low

Table 1.1. Potential of the current prototypical and emerging memory.

1.4 EMERGING ACTIVE MATERIAL – SILICON OXIDE (SiO_X)

There have been many studies of binary metal oxide-based and perovskite oxide-based resistance switching characteristics for electronic device development [24, 25], which can have operating instability issues due to difficulty in controlling stoichiometric compositions [26, 27]. Therefore, a simple process that is compatible with conventional complementary metal-oxide semiconductor (CMOS) fabrication allows multi-layer compositional engineering and provides good electrical stability and high yield, which are critical requirements for neuro-electronics realization [28]. Silicon oxide (SiO_x) has long been used as gate dielectrics for metal-oxide-semiconductor field-effect transistors. In addition to excellent insulating properties, resistive switching properties have been observed in SiO_x materials as early as 1962 by Hickmott and 1967 by J. G. Simmons and R. R. Verderber, with additional modeling being done by G. Dearnaley in the 1970s [29-31]. They observed that a simple metal-insulator-metal structure (e.g. Au/SiO_x/Al, MIM) can form an active memory device based on its repeatable negative resistance phenomenon. Recently, Yao et al. have reported SiO_x-based resistive switching behaviors in vacuum, indicating that this traditionally passive material can be converted to an active memory element and controlled by external electrical activation [32-37]. Amount of recent reports also describe and indicate that using SiO_x as the active switching medium in resistive switching memory devices [38-41]. We have further demonstrated a Si diode (1D) with low reverse-bias current integrated with a SiO_x-based memory element (1R) using nano-sphere lithography and deep Si etching to pattern a P++/N+/N++ epitaxial Si wafer [42]. The above achievements for intrinsic SiO_x-based ReRAM indicate: 1) High device yield, forming-free operation, reduced operating voltage, excellent scalability (to dimensions < 40 nm in 1D-1R architectures without scarifying the device performance, such as the retention of multilevel states and endurance reliability) and good device

stability; 2) Pulsed programming in the 50 ns-regime and low reverse current with large rectification ratio to meet low-energy consumption criteria (>10^6 for high-conductance states and negative-bias current) for integrated 1D-1R nano-pillar architectures; and 3) wide programming resistance dynamic range (potentially up to 10^8), multi-level states, and excellent reliability. However, the resistive switching mechanisms in SiO_x are not well understood and use as an electronic synaptic device has not previously been demonstrated.

1.5 OUTLINE

This research work aims at exploring the possibility of SiO_x layer as potential resistive switching material and developing emerging memory device and architectures for next generation nonvolatile memory applications. SiO_x-based materials are selected here for low-power portable electronics, highly-integrated of compact memory design, and other applications. This research work started from investigating device structures, material compositions and electrical characteristics to realize ReRAM cells with high ON/OFF ratio, low static power consumption, low switching power, and high readout-margin using CMOS compatible SiO_x-based materials in both metal-insulator-semiconductor (MIS) and metal-insulator-metal (MIM), and one diode - one resistive switching element (1D-1R) architectures. Then the study of modeling of resistive switching mechanism, including temperature effect, pulse response and carrier transport behaviors will be performed, to develop a compact model in energy diagram, trap-level information, dipole polarization in SiO_x resistive switching layer, even for computer-aided design (CAD) in very-large-scale integration (VLSI) design. An intriguing non-Von Neumann computing architecture, named synapse-based neuromorphic system, will

be demonstrated in SiO_x-based ReRAM, combining with bio-inspiration and biomimetics process illustrations. The novel applications in the physiology and pathology discussions in reactive oxygen species (ROS) production and regulation processes will be clarified. This work will present the comprehensively investigation of SiO_x-based resistive switching characteristics, mechanisms, applications for future post-CMOS devices era.

In chapter 2, device structure, materials and electrical controlling for SiO_x-based ReRAM were investigated. MIS architecture was fabricated with various post-deposition anneal using rapid thermal annealing. Polarity effects of resistive switching characteristics and RESET process were studied. Horizontal and vertical device structure designs, and composition optimization (SiO_x, $x < 2$) by sputtering process have been fabricated in MIS architecture. Device characteristics including SET/RESET voltage, high/low resistive state (HRS/LRS), forming process and electrical controlling characterizations with various compliance current limitations and stopped voltage values have been compared. Effect of ambient dependence in SiO_x-based ReRAM has also been examined.

In chapter 3, to further understanding the resistive switching mechanism for SiO_x-based ReRAM, edge and bulk device structures has been applied. An unusual backward-scan effect with DC and AC electrical response were studied. The switching behavior of the backward-scan effect is incorporated into Verilog-A simulations to characterize integration strategies for future circuit-level applications. Oxide stoichiometry effects by PECVD process on reversible switching and program window optimization has been fabricated and examined to achieve autoforming process. Different electrode materials have also been applied into SiO_x-based ReRAM to achieve flexible manufacturing process. Modeling of resistive switching mechanism, including temperature effect, pulse response and carrier transport behaviors will be performed, to develop a compact model

in energy diagram, trap-level information, dipole polarization in SiO_x resistive switching layer, even for computer-aided design (CAD) in very-large-scale integration (VLSI) design.

In chapter 4, a Si diode (1D) with low reverse-bias current is integrated with a SiO_x-based memory element (1R) using nano-sphere lithography (NS lithography, or NSL) and deep-Si-etching (DES) to pattern a $P^{++}/N^{+}/N^{++}$ epitaxial Si wafer. Nano pillar type 1R and 1D-1R architectures with NSL forming a self-aligned process have been fabricated with various pillar size down to 40nm, high density, large-scale nano-pillar (NP) array architecture. The nanostructures fabricated using NSL can be well controlled in shape, size, and inter-pillar spacing through direct assembly of polymer nanospheres on the wafer-scale. Performance of 1R and 1D-1R structures are characterized and show that the integrated nano-pillar 1D-1R configuration offers low static-power for suppression of sneak-path issues. The work demonstrated here provides an efficient fabrication process and low reverse-bias current in a SiO_x-based 1D-1R configuration for potential use in future ultra-large-scale nonvolatile memory applications.

In chapter 5, we realize a device with biological synaptic behaviors by integrating silicon oxide (SiO_x) resistive switching memory with Si diodes. Minimal synaptic power consumption due to sneak-path current is achieved and the capability for spike-induced synaptic behaviors is demonstrated, representing critical milestones for the use of SiO_2–based materials in future neuromorphic computing applications. Biological synaptic behaviors such as long-term potentiation (LTP), long-term depression (LTD) and spike-timing dependent plasticity (STDP) are demonstrated systematically, and represent interesting potential applications for SiO_x-based resistive switching materials.

In chapter 6, the contribution of this dissertation is summarized and suggestions on future work have been proposed.

Chapter 2: Device Structure, Materials and Resistive Switching Behaviors

Recent reports by Yao *et. al.* on SiO_x-based resistive switching in vacuum indicate that this traditionally passive material can be converted to an active memory material by external electrical activation [43, 44]. Although many resistive switching mechanisms have been reported for various materials, the exact switching mechanisms in SiO_x-based materials have yet to be identified and may be different than traditional materials [45, 46]. Therefore, characterizing the polarity dependence of device switching is a top priority for the non-polar, SiO_x-based resistive switching memory. Specifically, analyzing and understanding device RESET switching parameters will help develop a resistive switching model. Here, SiO_x-based resistive switching memory is realized by fabricating a tantalum nitride (TaN)/SiO_2/heavily doped n-type (n^{++}) Si-substrate structure. Device switching characteristics and stability were investigated with and without a post-deposition anneal (PDA). The polarity dependence of switching characteristics suggests that the switching region is located at the cathode side, potentially due to the asymmetrical thermal-dissipation structure of the TaN/SiO_2/n^{++} Si device. In addition, the oxygen content effect in SiO_x-based ReRAM has been investigated by controlling the oxygen flow during reactive sputter deposition. It has been found that device yield, switching characteristics and stability are improved for oxygen-rich devices. The effects of SiO_x thickness, device area, and multilevel operation by controlling compliance current and stopped voltage values suggest that the switching region is located at the interface and is localized rather than uniformly throughout the bulk SiO_x layer. One of the key phenomena: the sensitivity to oxygen in SiO_x-based ReRAM has also been investigated by controlling the ambient gas pressure and monitoring resistive switching characteristics. Operating stability measurements in

vacuum, nitrogen and oxygen-nitrogen ambients show that SiO_x-based ReRAM is sensitive to oxygen partial pressure, where resistive switching is temporarily disabled. A subsequent vacuum recovery process restores normal functionality. The statistical distribution of electrical parameters in the oxygen-induced device failures can be described using bi-modal Monte Carlo simulations and additional failure analysis. For reliability issue, data retention tests in the high-resistance state (HRS) and low-resistance state (LRS) for over 10^4 sec confirm the nonvolatile nature of the device. Testing several different device structures and ambient effect enable development of a possible resistive switching model to aid characterizing SiO_x-based devices for use in future ReRAM applications.

The SiO_x-based devices were fabricated on n^{++} (100) Si ($1\text{-}7\times10^{19}$ cm^{-3}) substrate as bottom electrode with resistivity of 0.001-0.005 ohm-cm. Surface native oxide was removed by 1% dilute HF. A various thickness of SiO_x layer (10 nm, 30 nm, 45 nm, and 60 nm) was deposited by magnetron sputtering of silicon target in Ar and O_2 ambient at 200 °C with different O_2 flow rate during deposition (denoted as "1, 5, 10, 15-sccm samples"), followed by 5 min PDA at 500°C in O_2 (denoted as "w/ annealed sample"). The top electrode, 200 nm-thick TaN, was sputtered onto the SiO_x film and patterned in a square (various device sizes). Control samples without PDA (denoted as "w/o annealed sample") were also prepared using the same process. CF_4-based plasma chemistry was used to etch TaN and CHF_3/O_2 was used to etch the SiO_2 layer. I-V characteristics were measured using an Agilent B1500A semiconductor device analyzer in vacuum ambient ($<1\times10^{-4}$ mbar) or N_2 purge (1 atm). "SET Current/RESET Current $(I_{set})/(I_{reset})$" and "SET Voltage/RESET Voltage $(V_{set})/(V_{reset})$" are defined as the values of absolute current and voltage measured at the beginning of resistance switching from HRS/LRS to

LRS/HRS, respectively. The definition of the "LRS Current"/"HRS Current" is the measured current in the LRS/HRS at 0.2 V bias magnitude.

2.1. POST-DEPOSITION ANNEAL (PDA) AND POLARITY EFFECTS [47]

Figure 2.1 shows I-V characteristics of 30 switching cycles for a sample (structure: 40 nm thickness SiO_x and a square of 540 μm edge length, as shown in inset of Figure 2.1) with PDA. Voltage was applied to the top electrode and the bottom electrode was grounded. Before switching cycle measurements, an electroforming process is required, where leakage current fluctuations are observed with increasing bias, as shown in the right inset of Figure 2.1. Forming voltage and the corresponding forming current are typically about 14 V and 1 μA, respectively, which implies that the electroforming process is related to soft breakdown rather than permanent, hard-breakdown. The memory cell can then be operated as a reversible switch by an external bias. After electroforming, resistive switching phenomena are observed by sweeping the voltage from 0 V to positive or negative values (7 V or -7 V). At a voltage defined as V_{reset}, the current begins to decrease from a LRS and, in some memory cells, gradually reaches a HRS. However, in some cells, the decrease in current from LRS to HRS occurs rapidly over a small voltage range. In all devices, absolute current increases suddenly at V_{set} when using either positive or negative voltage sweeps (4 V or -4 V), and the device transitions to a LRS. In addition, the absolute RESET voltage is always larger than the absolute SET voltage, which is a dramatic and unique difference as compared to unipolar or non-polar resistive switching devices based on other materials.

The electrical characteristics of the SiO_x-based device, specifically the electrical stability of the memory window, could be improved by introducing a PDA into the

fabrication process, as shown in Figure 2.2 (a) and (b). By comparing the LRS and HRS current for samples with and without PDA, enhanced stability of the HRS current is observed in the samples with PDA. Furthermore, a memory window (LRS/HRS current) of at least one order of magnitude could be maintained without degradation after 30 switching cycles for both sweep polarities. Larger HRS current was measured in the sample without PDA for a negative reset sweep as compared to a positive reset sweep (-/- represents a negative SET process and a negative RESET process), but, no HRS current dependence was observed as a function of SET polarity, as shown in Figure 2.2 (b). This implies that, for devices electroformed with positive polarity, the negative RESET process may be less effective than the positive RESET process; in other words, when using positive RESET polarity, the device is programmed to a HRS with higher resistance as compared to using negative RESET polarity.

In order to further investigate the observed polarity effect and its impact on RESET capability, the statistical mean values of the RESET switching parameters were extracted from the 30-cycle test for samples w/ and w/o PDA, as shown in Figure 2.3 (a). For the mean, absolute value of RESET voltage, a negative RESET voltage sweep results in larger RESET voltage values as compared to a positive RESET process. On the other hand, the RESET current and RESET power (inset in Figure 2.3 (a)) demonstrate the opposite trend where a negative RESET results in smaller values as compared to the positive RESET process. The polarity of the SET process had no observable effect on RESET switching characteristics. According to previous studies, as a result of the electroforming process, Si nano-filaments are expected to be formed near the device edge. Also, the resistive switching characteristics were independent of electrode material and oxide thickness. Based on recent simulation results, RESET current and power would be expected to provide sufficient Joule-heating to rupture the conductive path. For our

device architecture, the asymmetric reset power characteristics and the sweep polarity effect may result from two possible effects: (1) oxygen-vacancy clustering and (2) asymmetric thermal-mass structures. Oxygen vacancy clustering would be expected to increase the oxygen vacancy concentration near both electrodes, with less concentration near the middle due to oxygen-ion absorption (oxygen-sink) by the electrodes and dielectric-breakdown-induced nonstoichiometric oxygen deficiency in SiO_x. When electrons are injected into the filament from the cathode, they would flow through a filament cross section determined by the vacancy concentration. Since the vacancy concentration is high near the cathode, we expect a thin cross section (vacancy clustering) with high current density. As the current enters the middle region, it must spread-out since there is lower vacancy concentration, and the current density will decrease. Finally, when the electron current reaches the anode, even though there is now increasing vacancy concentration, it remains spread-out and flows with low current density. This scenario would predict that the filament cross section will always be thinner at the cathode due to current spreading near the middle of the filament, and can explain why the device might always switch at the cathode.

The top TaN electrode has lower thermal conductivity ($< 8.8\ W \times m^{-1} \times K^{-1}$) than the bottom n^{++} Si-substrate ($151\ W \times m^{-1} \times K^{-1}$), leading to an asymmetric thermal-mass structure. Due to the distinct thermal-dissipation difference between TaN and n^{++} Si, and even for similar electrode materials (for example a polycrystalline silicon/SiO_2/n^{++} Si-substrate structure), as shown in Figure 2.3 (b), a positive RESET process requires higher power than a negative RESET, but only if the resistive switching region is located at the cathode-side rather than at the anode-side. As a result, the RESET switching characteristics of SiO_x-based resistive memory devices may depend on the thermal-dissipation efficiency of the electrodes, and this will affect both the HRS and LRS

current, where the LRS current has larger values for a positive RESET than for a negative RESET, as shown in Figure 2.2. It may be noted that, for both samples, the RESET voltage trend is opposite to that of the RESET current trend, which may result from a constant power consumption during the RESET switching process. This may indicate that the energy required for state transformation from HRS-to-LRS is similar to the energy required for the LRS-to-HRS transition. In this case, the trend in V_{reset} with polarity would be opposite to that of the I_{reset}, and constant RESET power would be required regardless of sweeping polarity when an asymmetric power dissipation structure is excluded.

Based on the above analyses, a preliminary resistive switching mechanism for SiO_x-based resistive switching behavior can be proposed. For the LRS, under a higher positive or negative bias (7 V or -7 V), the connected filament would be ruptured or broken, in concept due to current-induced Joule heating, which provides sufficient energy to recover defect trap levels or to oxidize the resistive switching layer near the cathode. As a result, for positive bias sweeping, the resistive switching location would be near the bottom n^{++} Si electrode; whereas for negative bias sweeping, the switching location would be near the top TaN electrode due to the oxygen-vacancy clustering effect. For devices in the HRS, the filament would be re-connected regardless of SET voltage polarity. Compared to using a TaN electrode, resistive switching in polycrystalline-silicon electrode devices exhibits less stable operation, potentially due to an inefficient O recovery process, as shown in the inset of Figure 2.3 (b). Although these findings support a thermally-driven RESET process, determination of the detailed resistive switching mechanisms in SiO_x-based devices will require further investigations including an analysis of device current transport behavior as a function of temperature.

Figure 2.4 shows data retention performance of SiO_x-based resistive switching memory devices w/ PDA in positive (+/+) and negative (-/-) operating conditions. The readout of LRS and HRS is performed after applying 4 V / 7 V or -4 V / -7 V cycles, and then, after every decade of cycles, LRS and HRS current are measured at + 0.2 V. In Figure 2.4, the retention reliability test for both measurement conditions are stable with a resistance ratio of at least one order of magnitude and no degradation is observed for more than 10^4 sec, indicating that a 10-year lifetime might be expected and further confirming the nonvolatile nature of the SiO_x-based resistive switching device.

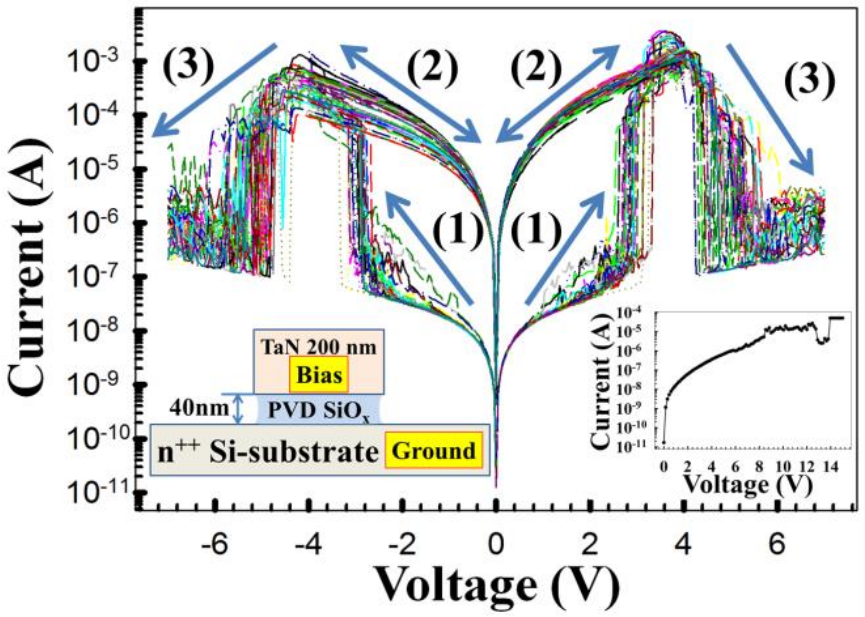

Figure 2.1. 30 cycles of resistive switching behavior in samples with PDA. Insets show a schematic representation of the $TaN/SiO_2/n^{++}$ Si-substrate structure, and an I-V plot of electroforming data.

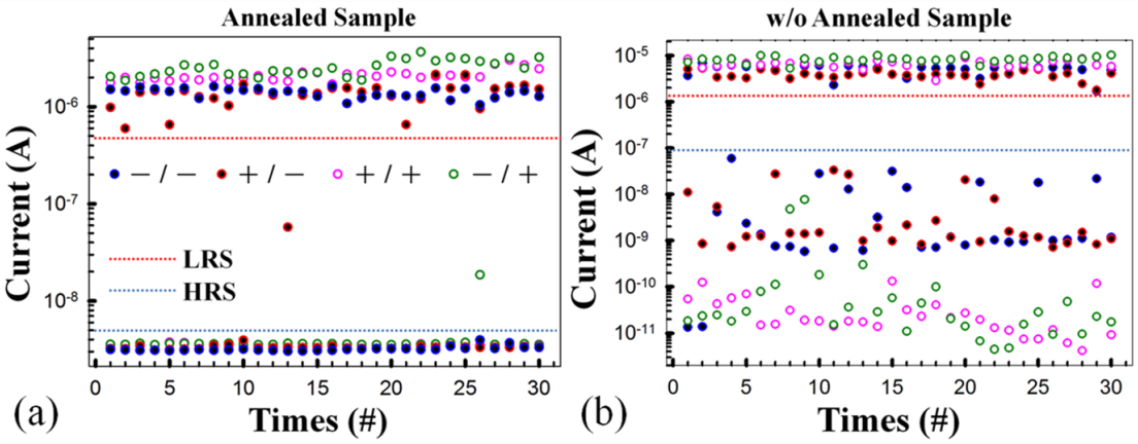

Figure 2.2. Polarity dependence (-/- means negative SET/negative RESET) of LRS and HRS distributions across 30 cycles for samples (a) w/ and (b) w/o 5min 500°C PDA in O_2.

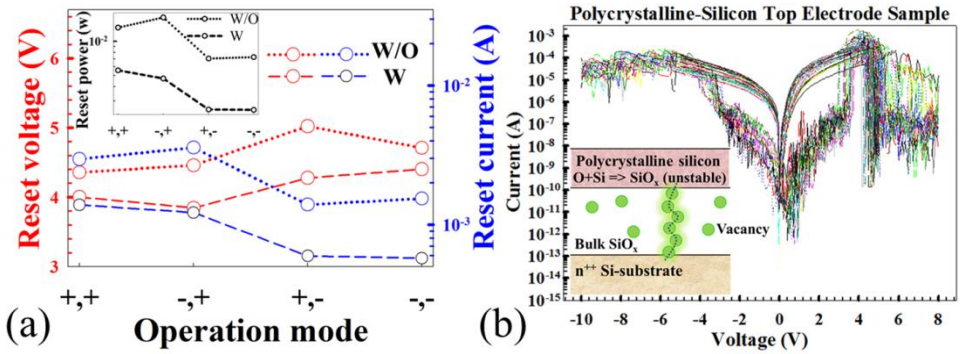

Figure 2.3. (a) Polarity dependence of RESET voltage, RESET current, and RESET power for samples w/ and w/o PDA. (b) Polycrystalline-silicon top electrode device switching characteristics.

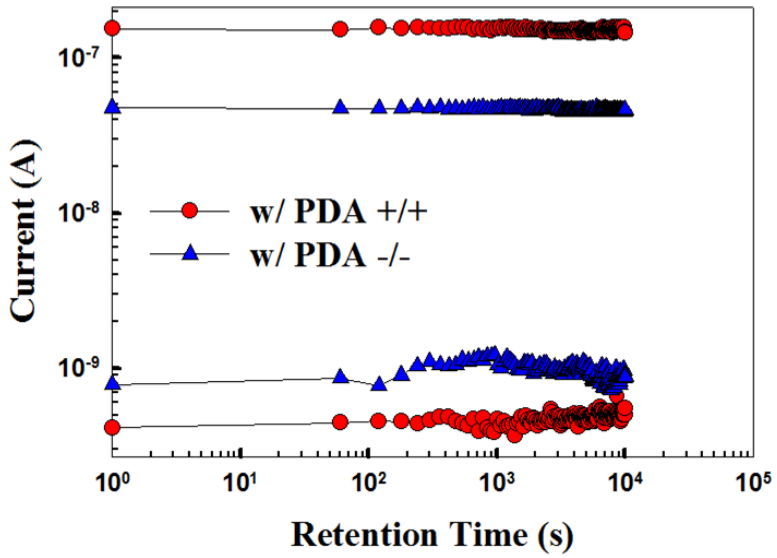

Figure 2.4. Retention test at room temperature for samples w/ PDA in positive and negative polarity conditions.

2.2. Device Structure Designs, Composition, and Multilevel Operation [48]

Figure 2.5 (a) shows *I-V* characteristics of the electroforming process for 15-sccm samples. Voltage was applied to the top electrode (60 nm-thick SiO_x layer and 80 μm edge length) and the bottom electrode was grounded without any compliance current limitation. As bias is increased beyond the Fowler-Nordheim tunneling regime, current fluctuations are observed at the forming voltage (V_F). Typical values for V_F and forming current are 20 V and 1 μA, respectively. The electroforming process is completed during the backward voltage sweep from 20 V to 0 V, leading to a LRS (Figure 2.5 (a)). Figure 2.5 (b) shows the "number of working devices" and the corresponding relative dielectric constant (ε_r) of the SiO_x layer, extracted by AC capacitance values, as a function of oxygen flow rate during SiO_x deposition. The difference in relative dielectric constant values implies that the SiO_x layer composition is changed by controlling the oxygen flow

rate, with “oxygen-rich” devices being deposited at the higher O_2 flow rates (ε_r close to 3.9 indicates stoichiometric SiO_2) or ”silicon-rich” devices at lower O_2 flow rates (ε_r > 3.9 indicates non-stoichiometric SiO_x). Note that oxygen-rich devices, such as the 10-sccm or 15-sccm samples, show higher device yield than the silicon-rich devices. This may imply that the concentration of defective traps is affected by the stoichiometry of the SiO_x layer.

Figure 2.6 (a) and (b) show *I-V* characteristics of the 5-sccm and 10-sccm samples for 30 switching cycles, respectively. Voltage was applied to the top electrode while the bottom electrode was ground. The compliance current was limited to 1 mA during each 4 V forward/reverse sweep used to program the device to the LRS. Unipolar switching is observed for both devices. By sweeping the voltage to 8 V, the current begins to decrease at V_{reset} and the device is programmed into a HRS. On the other hand, the current increases suddenly at V_{set} to return a LRS when sweeping the voltage to 4 V. The HRS/LRS resistance ratios for both structures are $\sim 10^3$, which easily satisfies the requirement for sensing. However, the variances of V_{set}, V_{reset}, HRS current and LRS current in the low oxygen-flow samples are larger than the high oxygen-flow variances, as shown in Figure 2.6 (c) and (d). For example, the coefficient of variation (the ratio of the standard deviation to the mean), of V_{set}, V_{reset}, and HRS and LRS current in the 5-sccm samples are 6.75 %, 11.7 %, 167 % and 38.7 %, which are much larger than those for the 10-sccm samples (5.62 %, 1.42 %, 113 % and 14.5 %). The relation between switching parameter variance and SiO_x layer stoichiometry may imply a difference in defect concentration between the two sample types. The variation in defect concentration

may be related to a change in the average hopping distance between adjacent traps or the available electron energy levels within the filament, both of which would be expected to affect the filament rupture and formation in a localized region. In addition, the RESET voltage is always larger than the SET voltage, which is unique as compared to other material systems. Metal filament formation, for example a Ta filament resulting from metal atoms diffusing into the SiO_x layer, can be ruled out in this case since the *I-V* response maintains the characteristic response for SiO_x materials.

To further investigate the conduction mechanism of the SiO_x-based ReRAM, a set of *I-V* curves for LRS and HRS is plotted as ln(*I/V*) versus square root of voltage (see insets of Figure 2.5 (a) and Figure 2.6 (a), respectively). Ohmic behavior is observed for both LRS and HRS at low bias voltage (Region 1). This suggests that, at low bias, current transport behavior is dominated by thermal generation. On the other hand, at higher bias (1 V ~ 2 V), a modified Frenkel-Pool characteristic is observed. Therefore, the observed *I-V* curves in LRS and HRS are in good agreement with Frenkel-Pool charge transport. The conduction mechanism of Frenkel-Pool is related to trap sites in the insulating material. It is believed that these defective traps come from the non-stoichiometric SiO_x composition.

The effects of SiO_x thickness and area on the characteristics of 10-sccm SiO_x-based ReRAM are shown in Figure 2.7. It is found that smaller-area devices require larger voltage to be electroformed, presumably due to fewer electrically weak points per unit area (top inset of Figure 2.7 (a)). The SET and RESET power (voltage × current) and LRS and HRS current at 0.2 V are independent of device area, illustrating that resistive

switching is an inhomogeneous, filament-type phenomenon (bottom inset in Figure 2.7 (a)). Figure 2.7 (b) shows the electroforming voltage (top inset), SET and RESET powers, and HRS and LRS current (bottom inset) as a function of SiO_x thickness. The electroforming voltage decreases with SiO_x thickness until hard breakdown and the irreversible switching occurs at 60 Å thickness. The thinner samples exhibit lower "yield" and less stable switching behavior than thicker samples, suggesting that the effective thickness of the "switchable filament" is approaching the physical thickness of the SiO_x layer in the thinner samples (100 Å). Kim *et. al*. have reported that the "switchable filament" in the localized region is about 3-10 nm thick near the interface between insulating layer and anode electrode. It should be noted that other parameters such as SET voltage and RESET voltage are fairly independent of SiO_x thickness, indicating that device switching occurs in a small segment of the filament rather than throughout the entire bulk SiO_x layer. The device *I-V* response remains essentially unchanged for a large range of SiO_2 thicknesses and electrode areas, indicating that SiO_x-based devices most likely follow a filament-type resistive switching characteristic rather than interface-type resistive switching.

The multilevel effect as a function of compliance current limitation and stopped voltage value has been studied. Figure 2.8 shows the unipolar switching response for the 10-sccm samples under a series of compliance current limitations (i.e. 5 μA - 1 mA during the set process with stopped voltage fixed at 7 V) and under a series of stopped voltages (i.e. 5 V - 10 V during the reset process with compliance current fixed at 1 mA). The stopped voltage is defined as the maximum value of sweeping voltage. One

can see that the resistive state of the SiO_x-based ReRAM can be "tuned" by controlling external electric conditions. A higher compliance current limit results in a higher total switching power to achieve a larger LRS current (Figure 2.8 (a)). This suggests that when a "stronger" filament is formed in the resistive switching material, it can withstand much larger current. In order to achieve a stable and repeatable HRS current level, a series of stopped voltages were investigated for each compliance current condition, and then a specific stopped voltage was selected to achieve a nearly constant current level in the HRS. A larger stopped voltage results in more complete recovery from LRS to HRS. The recovery process is likely related to localized Joule heating, possibly assisted by an increasing electrical field, that alters filament morphology to a degree depending on the level of RESET achieved (as determined by analyzing the stopped voltage effect, Figure 2.8 (b)). Conceptually, filament morphology can be altered to achieve higher resistance by reducing the filament cross sectional area, forming a gap in the filament with larger width, or by reducing the concentration of conductive defects relative to non-conducting defects in a certain "weak point" along the filament. Thus, higher resistive states with smaller HRS current can be programmed by either increasing stopped voltage during RESET or by decreasing compliance current during the SET process.

Figure 2.9 shows summary statistics for RESET voltage (inset), current, and power as a function of compliance current. Most of the RESET process parameters, such as RESET voltage, RESET current and RESET power, increase with compliance current. The increasing trend in these RESET parameters suggest that a higher compliance current limitation results in the formation of more "robust" filaments that

subsequently need larger RESET current or RESET power to rupture the filament. The relation between average RESET current for a series of compliance current limitations is shown in the inset of Figure 2.9 (b). Since the RESET current is consistently higher than the compliance current limit used to program the device, it can be concluded that initiation of the RESET process is based on a thermal-assisted switching mechanism. This is also consistent with the increasing trend of RESET voltage values with compliance current limitation. Therefore, it can be understood that the resistive switching mechanism in the SiO_x-based device is dependent mainly on applied power (i.e. a comprehensive effect of RESET voltage and RESET current).

Figure 2.10 shows the statistics of SET voltage, current and power as a function of stopped voltage. For SET electrical parameters, it is observed that SET voltage increases slightly with stopped voltage (Figure 2.10 (a)). This is in contrast to the SET current, which decreases with increasing stopped voltage (see inset of Figure 2.10 (a)). The SET power is found to slightly reduce and saturate with increasing stopped voltage (Figure 2.10 (b)). We believe that the total resistance of the filament can be separated into two parts: (1) the resistance of the "intact" filament (r_d), which is a nearly constant value after the electroforming process, and (2) the resistance of the "switchable filament" (R_s), which can be tunable by external electric power in the SiO_x-based device. To confirm this idea, the average SET resistance ($R_{set} \equiv V_{set}/I_{set}$) is assumed to be equal to the sum of two resistors ($R_{set} = r_d + R_s$), and, most importantly, a prerequisite condition is used as required for a power-induced mechanism since the effective switching power ($I_{set}^2 R_s$) under

different stopped voltage conditions is assumed to be equal when transforming the resistive state from HRS to LRS. This leads to the following six algebraic equations

$$I_{set|5V,\ 6V,\ 7V\ldots10V}{}^{2} \times R_{s|5V,\ 6V,\ 7V\ldots10V} = \text{constant} \quad (1)$$

Since V_{set} and the corresponding I_{set} in each stopped voltage condition are known quantities, R_{set} can be calculated and one prerequisite condition can be used to verify the two-sectional filament assumption by plotting the relation between R_{set} and $1/I_{set}^2$ under a series of stopped voltages, as shown in the inset of Figure 2.10 (b). The linearity (about 0.96) of these data confirms that the power dissipation model applied to two resistors in series is consistent with a constant transformation energy being required for resistive switching, and also provides a possible mathematical quantification for multilevel programming operations.

The breakdown properties for devices with and without a sidewall were measured. In devices without a sidewall, the breakdown voltage was ~ 69 V, corresponding to an electric field of about 11.5 MV/cm. Devices with a sidewall exhibit current fluctuations up to ~ 1 - 10 μA during the initial forward voltage sweep of the electroformation process. This initial current fluctuation is believed to be the result of surface conduction along the sidewall as opposed to bulk conduction. Since soft breakdown in MOS devices is associated with current fluctuations of similar magnitude, it is reasonable to assume that that the initial forward voltage sweep produces soft breakdown events. These leakage paths are conveniently modeled as percolation pathways comprised of defects on the sidewall surface, similar to conventional models of soft breakdown and time-dependent dielectric breakdown (TDDB) in bulk amorphous-SiO_2 (a-SiO_2) (Figure 2.11 (a)).

Structural changes during the transition from percolation pathway to reversible filament would be expected, most likely driven by high-energy electron impacts at defect sites along the pathway and the associated Joule heating. Achieving a current of ~ 100 μA at 4 V during the reverse sweep implies that a reversible filament has formed. It may be noted that multiple filaments could form during this process, potentially forming a filament network with a definable cross-section. If electron-assisted processes are involved in filament formation, the cross-section would be expected to grow primarily along the plane of the sidewall surface since there are more defects at the surface to conduct electrons as compared to bulk a-SiO_2 regions, as shown in Figure 2.11 (b). However, filament growth extending into the a-SiO_2 some distance from the sidewall surface cannot be ruled out. After the electroforming process, the device is in a high-conductance state (Figure 2.5 (a)). Applied voltage in the range from ~ 4 - 15 V drives the device into a lower-conductance state, where the higher the applied voltage the lower the measured current at 1 V. This suggests that a region along the filament has been altered to form a thinner cross-section or a gap with width depending on the applied voltage magnitude (which is also confirmed by the SET power saturation phenomena due to the stopped voltage effect, Figure 2.10 (b)).

Because of these electroformation and switching characteristics, it seems reasonable to model the reversible filament as a collection of defects forming a percolation pathway with high current flow in the ON state, but having a gap in the filament that blocks current flow when the device is programmed to a low-conductance state. With this model, only the region where the gap is located need be considered when

describing the switching characteristics of the device. To estimate the thickness of the "switchable" gap (g), the breakdown voltage (V_{BD}) values on 16 devices with a sidewall were measured, which show that breakdown occurs at 28.5 V +/- 7.1 V. Also, the mean value of breakdown current (I_{BD}) in these devices just prior to breakdown was ~ 5 μA. If we model the filament as a resistor, we can estimate the maximum gap width, g_{max}, using the formula

$$\alpha E_{ox} = (V_{BD} - V_f)/g_{max} \quad (2)$$

where $\alpha = E_f/E_{ox}$ is the ratio of the breakdown field in devices with a formed filament (E_f) to that of the bulk oxide devices without a sidewall (E_{ox}). The breakdown field is known to increase as oxide thickness decreases. As a result, α is a function of g_{max}, and can be expressed as $\alpha = 1 + 1.9\times\exp\{- g_{max}/20\}$. The voltage drop across the intact filament, outside the region of the gap, just prior to breakdown is $V_f = I_{BD}\times R_f$, where $R_f = R_{on}\times(1- g_{max}/d)$ is the resistance of the intact filament, and d is the thickness of the a-SiO_2 layer. The ON-state resistance, R_{on}, is measured directly from the low-voltage I-V response. Substituting these expressions into equation (1) results in

$$g_{max}\times E_{ox}[1+1.9\times\exp\{-g_{max}/20\}\ ] = [V_{BD}- I_{BD}\times R_{on}(1 - g_{max}/d)] \quad (3)$$

Solving this transcendental equation leads to g_{max} = 12.5 nm +/- 5.1 nm for the 16 devices in this experiment. This provides an estimate of the maximum gap width in the OFF state of the device that is consistent with a minimum device thickness of ~ 10 nm identified in the experiment characterizing the effect of device thickness on device electroforming yield (Figure 2.7 (b), top inset).

Simplified energy band diagrams of the filament are shown in Figure 2.11 (c-d). The gap is represented in the physical model as a cylindrical region with diameter defined by the filament cross-section in the ON state and length determined by g_{max} in the OFF state. Using this physical model allows the device switching characteristics to be described without having any specific knowledge of the microscopic switching mechanisms, and provides a general model of the filament that is consistent with conventional percolation theory.

Current flow can be modeled by starting with the simple expression $J = qnv$, where $J = I/A$ is the current density, I is the current and A is the cross-sectional area of the filament. The variable n is the total defect concentration in the gap region, and v is the average electron velocity through the device. For conduction along a filament having two regions with different conductance connected in series, $J_1 = qn_1v_1$ is used to describe the current density in the region with higher conductance (intact filament) and $J_2 = qn_2v_2$ is used for the region with lower conductance (gap), where n_1 and v_1 are the defect concentration and average electron velocity in the intact filament and n_2 and v_2 are the concentration and average velocity in the gap region. To account for the fact that the region with smallest average electron velocity will dominate charge transport, standard practice is to write the average electron velocity through the device as $1/v = 1/v_1 + 1/v_2$. Re-writing this in terms of the current density components leads to $n/J = n_1/J_1 + n_2/J_2$. In the ON state, $n_1 >> n_2$ and type 1 defects dominate charge transport so that $J = J_1 = J_{on}$, whereas, when a significant fraction of the n_1 defects are converted to type 2 defects so that $n_1 << n_2$, the device is in a low-conductance, OFF state so that $J = J_2 = J_{off}$. In this

model, switching the device only affects the gap region. As a result, current flow through the filament is determined solely by the conductivity of the gap region. By considering the filament as a collection of defects that are converted between two defect types, type n_1 with high conductivity and type n_2 with low conductivity, the total defect concentration, $n = n_1 + n_2$, within the gap region can be considered to be constant so that $(n_1+n_2)/n = \eta_1+ \eta_2 = 1$, where η_1 and η_2 are state variables. This allows the current flow model to be expressed as

$$J = J_{on}/[1+ \eta_2(J_{on}/ J_{off}-1)] \quad (4)$$

where η_2 has a value ranging from 0 in the ON state to 1 when the device is programmed to a fully-OFF state and the gap width reaches its maximum value, g_{max}. The state variables are conveniently modeled as Fermi-Dirac distribution functions

$$\eta_1 = 1/(1+\exp\{(V_1-V)/E_1\}) \text{ and } \eta_2 = 1/(1+\exp\{(V_2-V)/E_2\}) \quad (5)$$

where V_1 corresponds to the ON-state transition in the *I-V* response, V_2 corresponds to the OFF-state transitions occurring at $V > V_{reset}$, and V_{reset} is measured directly from the *I-V* response where the current is maximum, thus corresponding to the point in the *I-V* response where conductance $G = dI/dV = 0$. The sharp ON-state transition observed in the *I-V* response at $V_1 \sim 3$ V (see Figure 2.6 (b)) is fit using a small value for E_1 of ~ 0.01 V, whereas the much broader OFF-state transition is fit using a larger value for E_2. Because of the stochastic nature of the *I-V* response above V_{reset}, the state variable controlling the OFF-state transition is better represented by

$$\eta_2 = \sum [F_i/(1+\exp\{(V_{2i}-V)/E_{2i}\})] \quad (6)$$

where the summation is carried out from i = 1 to N, with N representing the number of transitions occurring in the *I-V* response for $V > V_{reset}$. Introducing the parameters $-1 < F_i < 1$ allows each transition to be weighted properly for the most accurate least squares fit. When the device is programmed with a large voltage magnitude, $\eta_2 = \sum[F_i]$ approaches 1 and the device is driven to a fully-OFF state, whereas, for programming voltages higher than V_{reset} but substantially less than ~ 15 V, the value of η_2 is between 0 and 1.

In the model fit shown in Figure 2.12, N = 3 was determined using a least-square fitting method, resulting in η_2 = 5.01E-6. The remaining parameters in the model were also determined by least-squares fitting to be V_1 = 2.71 V, E_1 = 0.014 V, and the ON/OFF conductance ratio was J_{on}/J_{off} = 1.57E+8. Of note, the fully ON/OFF ratio is determined by the cases where no compliance current limitation is used to program the ON state and the maximum stopped voltage value is used to program the OFF state.

The current flow model can be used to investigate different charge transport characteristics that may be present in the device. For example, the ON-state current, J_{on}, can be modeled using a variable-range hopping charge transport characteristic. The current density J_{off} is defined as the current response in the low-voltage region (< 2 V) when the device is programmed to the lowest-conductance state. The voltage dependence of J_{off} can be modeled as Frenkel-Poole charge transport. These modeling activities are currently in progress and will be reported in future publications. The current flow model as presented here allows all of the salient features of the *I-V* response, and the multilevel

effect shown in Figure 2.13 (a) and Figure 2.13 (b), to accurately be captured without having any specific knowledge of microscopic switching mechanisms.

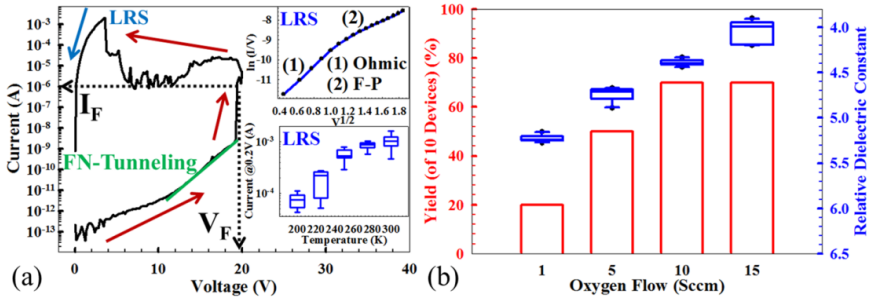

Figure 2.5. (a) The electroforming process. Insets show plots of temperature-related in LRS. (b) The device yield and permittivity as function of oxygen flow rate.

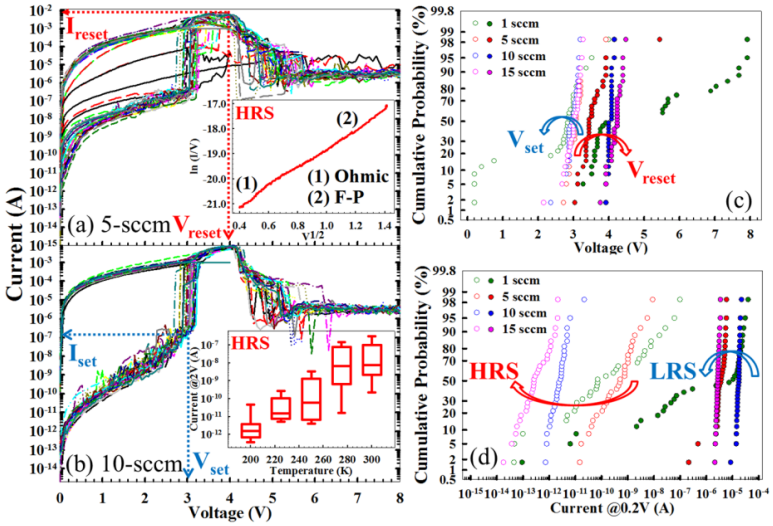

Figure 2.6. Switching behaviors of (a) 5-Sccm and (b) 10-Sccm samples. Insets plot temperature-related in HRS. The distribution of oxygen-flow dependence (c) V_{set}/V_{reset} and (d) HRS/LRS.

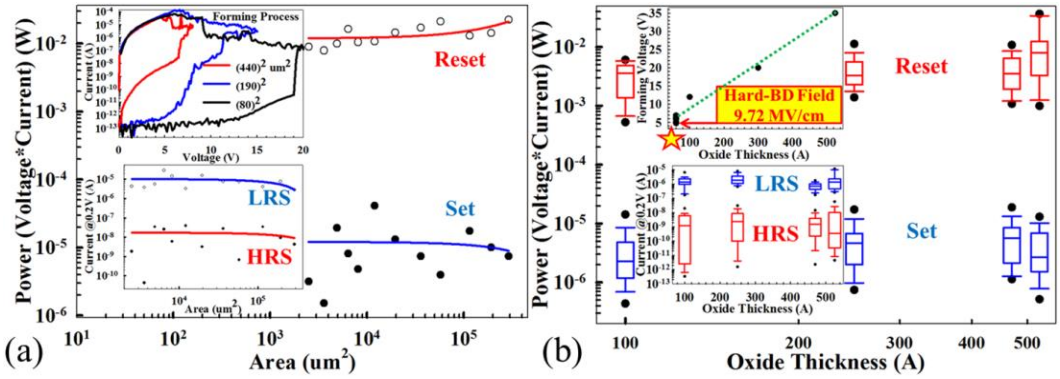

Figure 2.7. (a) The electroforming process, average of switching powers, and HRS and LRS as a function of device size. (b) The forming voltage, statistics of switching powers, and HRS and LRS as a function of SiO_x thickness.

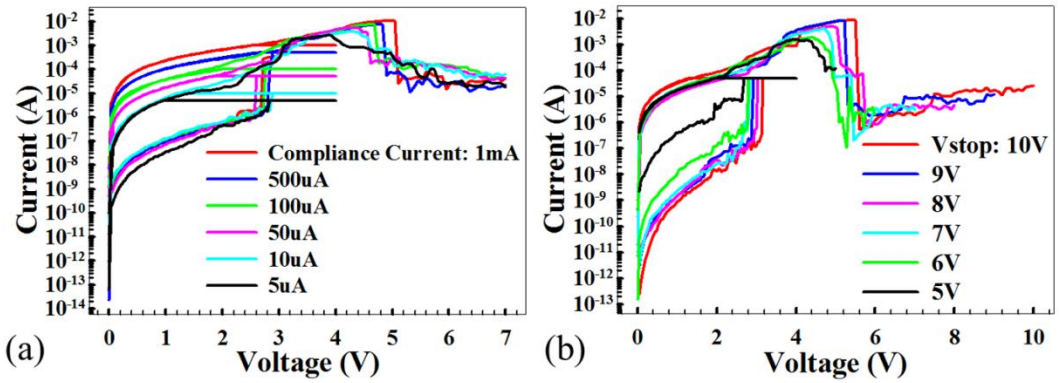

Figure 2.8. Continuous unipolar switching behaviors (a) under a series of compliance current and (b) under a series of stopped voltage.

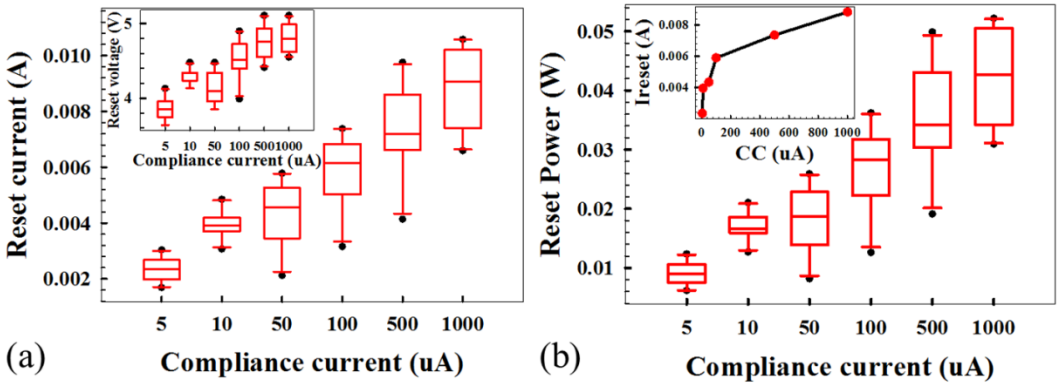

Figure 2.9. (a) Statistics plots of RESET current, voltage, and (b) RESET power as a function of compliance current. The inset shows the average RESET current under a series of compliance current.

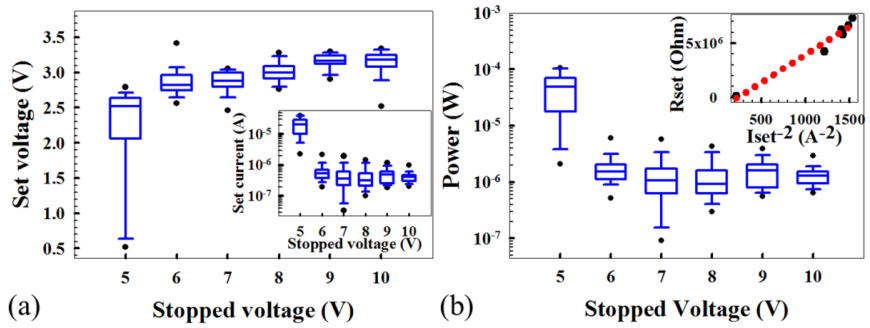

Figure 2.10. (a) Statistics plots of SET current and voltage as a function of stopped voltage. (b) Statistics plots of SET power as a function of stopped voltage.

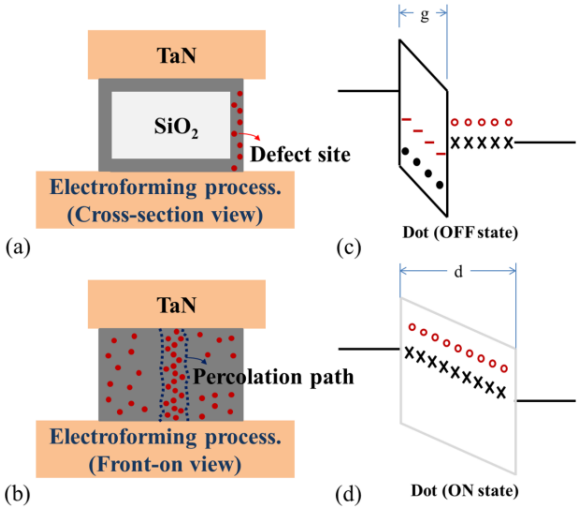

Figure 2.11. Schematic pictures of (a) showing the filament near the sidewall and (b) a front-view of the filaments. The band diagrams of sidewall-devices (c) HRS and (d) LRS states.

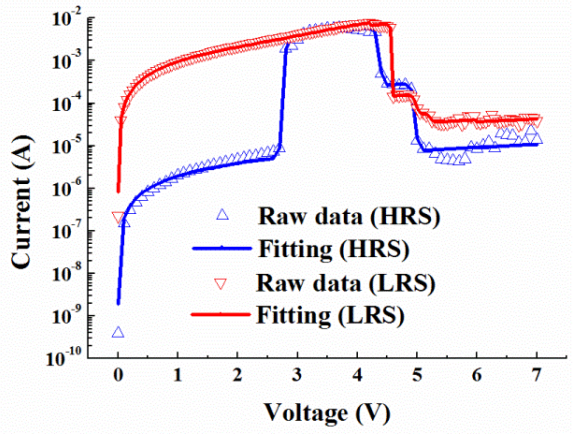

Figure 2.12. The simulated fitting curve from HRS and LRS in resistive switching behaviors.

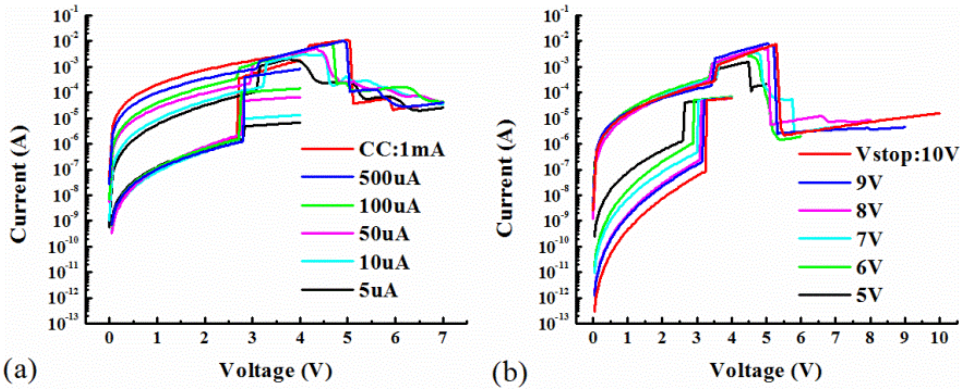

Figure 2.13. The simulated curve in (a) compliance current effect and (b) stopped voltage effect.

2.3. OXYGEN-INDUCED BI-MODAL FAILURE PHENOMENON (AMBIENT EFFECT) [49]

Figure 2.14 (a) and (b) show *I-V* characteristics of 30 switching cycles for samples (60 nm-thick SiO_x layer, device area 100×100 μm^2) in vacuum and pure N_2 ambient, respectively. Voltage was applied to the top electrode with bottom electrode at ground. The compliance current limit was set to 1 mA during each 4 V forward/reverse sweep used to program the device to the LRS. Unipolar switching is observed for both ambient conditions. By sweeping the voltage to 8 V, the current begins to decrease at V_{reset} and the device is programmed into a HRS. During the subsequent 4 V forward/reverse sweep, the current increases suddenly at V_{set} and sets the device to a LRS. The HRS/LRS resistance ratios for both are at least ~10^2 at 0.2 V, which satisfies sensing requirements. Before switching cycle measurements, a one-time electroforming process is performed, where leakage current fluctuations are observed with increasing bias, as shown in the insets of Figure 2.14 (a) and (b). The required forming voltage to achieve current fluctuations of about 1 μA is larger for the sample in N_2 ambient (20 V)

than for the sample in vacuum (8 V). The electroforming process is completed during the backward voltage sweep from forming voltage to 0 V, resulting in a LRS. In these devices, the RESET voltage is always larger than the SET voltage, which is unique as compared to other material systems. The RESET voltage is possibly larger than SET voltage due to series resistance or external parasitic resistance during the measurement. Metal filament formation, for example a Ta filament resulting from metal atoms diffusing into the SiO_x layer, can be ruled-out in this case since the *I-V* response maintains the characteristic response for SiO_x materials where $|V_{set}| < |V_{reset}|$.

The average values of key operating parameters for 30 resistive switching cycles are shown in Figure 2.15 as a function of N_2 pressure. Figure 2.15 (a) shows that the SET and RESET power (voltage × current) have little dependence on N_2 pressure, illustrating that reversible switching is not affected by N_2 exposure and devices operate without degradation as comparison to an oxygen-containing ambient (as will be shown later). Both LRS and HRS currents increase with N_2 pressure when the devices are operated for several switching cycles at each N_2 pressure, as shown by the open symbols in Figure 2.15 (b). However, when devices are first set ON or OFF in vacuum at 10^{-4} Torr, and then simply read at 0.2 V without performing any switching cycles (a "non-destructive read" operation), the measured current is stable across all N_2 pressures (filled symbols in Figure 2.15 (b)). As compared to devices tested with the non-destructive read, the current in actively-switched ON- and OFF-state devices increased by 13X and 160X, respectively. To further characterize and confirm the switching-induced current increases in N_2 ambient, *I-V* data from 0 – 2 V were fit to the Frenkel-Poole characteristic, $I_{pf} = G \times$

$\exp(\beta V^{-1/2})$, and charge transport parameters G and β were extracted. As shown in the Figure 2.15 (a) inset, the apparent relative permittivity, calculated from the β parameter, increases substantially for both ON- and OFF-state devices. Based on our previous current fitting results and normalized conductance method, the current transport behavior from 0 to 2 V for both LRS and HRS can be accurately fit to Frenkel-Poole emission, where the apparent relative permittivity values of LRS and HRS can be controlled using compliance current and reset voltage. Furthermore, the apparent relative permittivity of LRS and HRS both increase with N_2 pressure, suggesting that the dielectric properties near the conductive filament are changed and tend to increase the apparent polarization as compared to operation in vacuum (Figure 2.15 (a) inset). Syu et. al. have suggested that a N-doped switching layer may help control oxygen vacancy defects and stabilize switching performance due to nitrogen having high electronegativity when introduced into SiO_x-based materials. Localized Joule heat is often considered to drive the RESET process in filamentary devices, suggesting that, as N_2 pressure is increased, more nitrogen may incorporate into the active switching region during repeated switching cycles as the result of a Joule heat-assisted process, essentially resulting in a N-doped switching layer.

In contrast to a N_2 ambient, a 20% O_2-N_2 mix limits the resistive switching range to $\leq$ 1 Torr, with device functionality becoming severely degraded at 10 Torr, as shown in Figure 2.16 (a). Interestingly, reversible switching can be re-established by performing a sweep from 0 to 8 V in vacuum, where resistive switching recovers to initial vacuum conditions (see inset of Figure 2.16 (a)). The statistical distribution of switching voltage as a function of 20% O_2-N_2 pressure is summarized in Figure 2.16 (b). Two operating

modes are observed: (1) for pressures ≤ 1 Torr, resistive switching is not degraded and follows normal operating characteristics; and (2) at pressures at or above 10 Torr, resistive switching fails where V_{set} becomes < 1 V and V_{reset} increases to > 7 V. Our working hypothesis to explain these results is that the defects responsible for resistive switching (and current transport) are hydrogen-passivated in both the LRS (H-bridge) and HRS (H-doublet), thus protecting them from oxidation when biased up to 2V in 1 atm of air; however, when bias is increased above ~2.5 V, a switching event occurs and hydrogen passivation is temporarily lost, thereby allowing ambient O_2 to react with the defect and disable switching. Figure 2.17 (a) and (b) show the cumulative distribution function (CDF) of set and reset voltages at 10 and 100 Torr for 20% O_2-N_2 ambient. By using the bi-modal Monte Carlo simulation (repeated random sampling) and weakest link approximation, the oxygen-induced failure mode can be modeled for failure analysis. The weakest link approximation applies when multiple elements are in series where failure of the first element causes failure of the device, leading to $F_N(t) = 1 - (1 - F_1(t))^N$, where N is the number of elements in the series and $F_1(t)$ is the CDF for single elements. The failure percentage values for set and reset processes are found to be 0.146 % and 0.3 %, respectively, which indicates that, for the same ambient conditions, the failure mechanism may be dominate during the RESET process (HRS) due to the larger percentage of the weak failure mode. In other words, the effect of oxidation during defect-level transformations, especially when forming the H-doublet, severely suppresses resistive switching behavior. The simulation not only characterizes the failure mode information in detail, but also provides additional insights into the critical oxygen content

levels necessary for development of a possible oxygen sensor and the packaging requirements for oxygen detection when using SiO_x-based resistive switching devices.

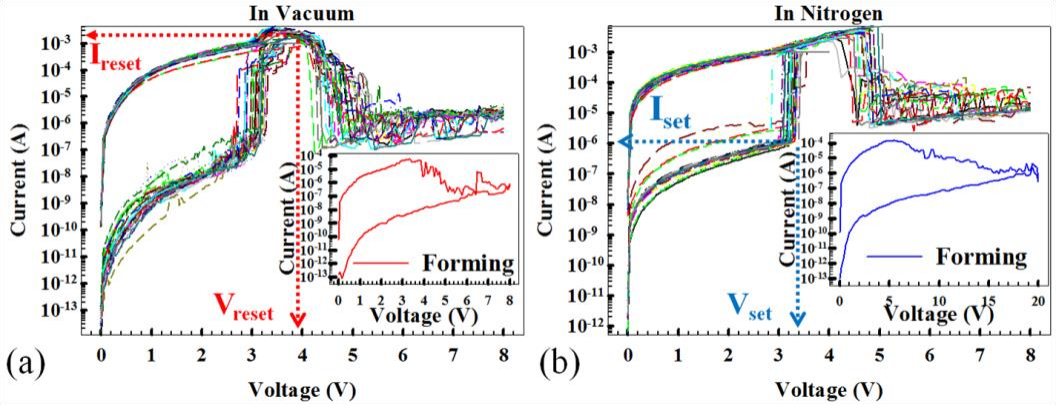

Figure 2.14. The resistive switching behaviors and forming process (insets) in (a) vacuum and (b) N_2 ambient.

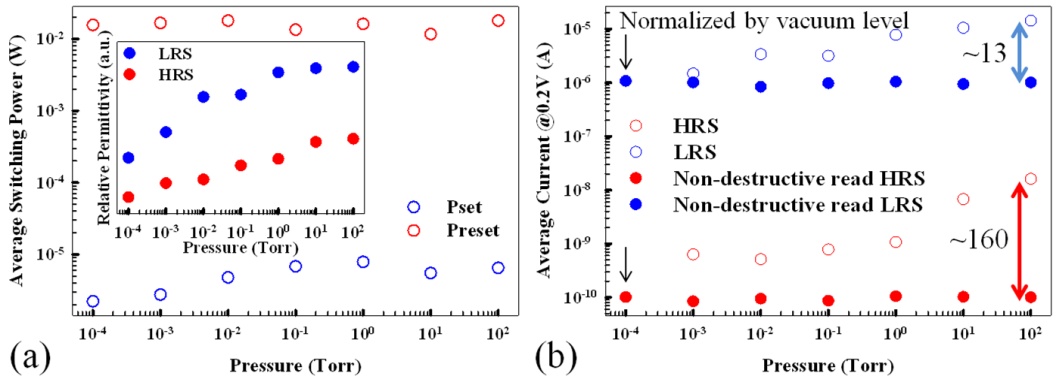

Figure 2.15. (a) Average of switching powers, relative permittivity values for LRS and HRS by Frenkel-Poole fitting (inset), and (b) LRS and HRS as a function of N_2 pressure.

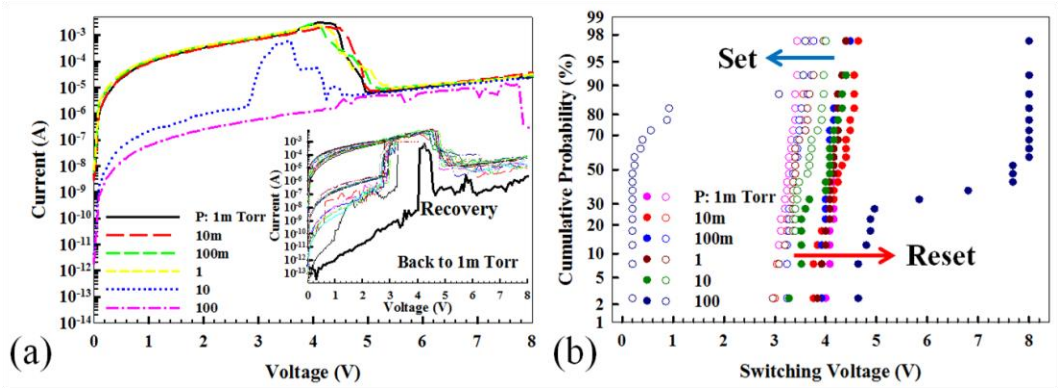

Figure 2.16. (a) Average current for 20 SET/RESET cycles for different 20% O_2-N_2 pressures and recovery process in vacuum (inset). (b) Cumulative probability of switching voltage as function of 20% O_2-N_2 pressure.

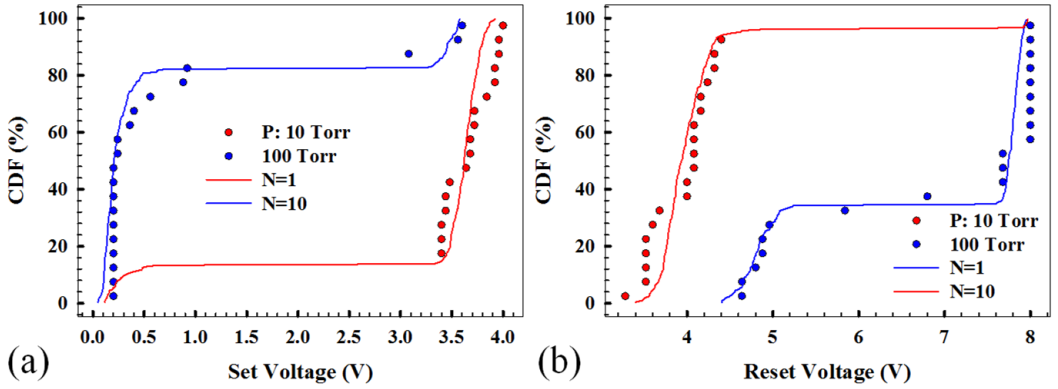

Figure 2.17. Initiation of resistive switching failures above 10 Torr of 20% O_2-N_2 mixture showing the cumulative distribution function (CDF) using bi-modal Monte Carlo simulation fitting for (a) SET and (b) RESET voltage.

Chapter 3: Resistive Switching Mechanism and Modeling

In our previous studies, SiO_x-based RRAM using $TaN/SiO_x/n^{++}Si$ and $TiW/SiO_x/TiW$ devices were demonstrated using a simple fabrication process compatible with conventional CMOS manufacturing to allow precise control over stack composition, improved cycling stability and good device yield for potential nonvolatile memory applications. Previous work has shown that anneal in H_2 and D_2 significantly reduces electroforming voltage, suggesting that SiH and $(SiH)_2$ may act as effective electroformation precursors, and we have proposed that the hydrogen bridge defect, Si-H-Si, may provide a low-energy pathway for oxygen reduction reactions during electroforming. The proposed unipolar resistive switching mechanism involves the transformation between a Si-H-Si defect in the LRS and a hydrogen doublet $(SiH)_2$ defect in the HRS, driven by proton (H^+) exchange reactions in the "GAP" region where switching occurs. Also, we have demonstrated high-density, wafer-scale 1D-1R nano-pillar SiO_x-based ReRAM fabricated by nano-sphere lithography, which can provide a fast and economical solution for wafer-scale manufacturing of high-density 1D-1R RRAM arrays (shown in Chapter 4). Despite these advances, multilevel operation and the resistive switching mechanisms leading to the distinctive unipolar switching characteristics of SiO_x materials are not well understood.

In this study, the unique unipolar operation of SiO_x-based ReRAM has been investigated by controlling the external resistance using a series transistor (1T) and monitoring resistive switching characteristics. A non-edge SiO_x device demonstrates that resistive switching can occur in bulk SiO_x materials and provides additional fabrication

flexibility. Thermal anneal of bulk devices improves device performance by hydrogen incorporation. An unusual backward-scan effect, which means a state is determined by the duration of the reverse sweep in switching process, is examined by DC and AC pulse measurements, which quantifies the requirements for programming duration during the reset process. The switching behavior of the backward-scan effect is incorporated into Verilog-A simulations to characterize integration strategies for future circuit-level applications. In addition, we analyze the effects of device structure, electrode material, SiO_x thickness and device area on electrical characteristics and confirm that RS occurs in a localized region along a conductive filament (CF) in detail. A physical model consistent with the observed RS I-V response is proposed. Our RS model differs from most conventional models by considering that the defects responsible for RS may remain localized within the switching region so that RS occurs when a collection of defects are driven between conductive and non-conductive forms. Based on the reported electrical and structural properties of known SiO_x defects, we further describe how proton exchange reactions can dramatically alter the conductivity of specific defects, leading to a model where the LRS has a large concentration of conductive defects within the switching region, and, conversely, when the device is programed to the HRS, most of the defects are converted to their non-conductive form. The electrically-conductive hydrogen bridge (Si-H-Si) is viewed as the most likely defect responsible for the LRS. Electrochemical reactions that form the non-conductive $(SiH)_2$ defect are discussed as potential mechanisms that enable localized switching without incorporating ion diffusion or drift mechanisms into the model. We also report the effects of varying the stoichiometry of a SiO_xN_y switching layer, where both device yield and electroforming voltage are found to improve for materials with higher oxygen content and less nitrogen incorporation. Characterizing the effects of external series resistance on the SET and

RESET transitions in the current-voltage (*I-V*) response shows that the program window (RESET-SET voltage) can be optimized for improved immunity to program/erase disturbance in circuit-level applications. The results indicate that both SET and RESET transitions have strong voltage dependence. As described in further detail in this chapter, we model the SET transition as being initiated by hydrogen desorption from $(SiH)_2$ to form Si-H-Si, and the RESET transition is modeled as electron injection into a fixed positive-charge defect that induces proton release and an electrochemical reaction with Si-H-Si to re-form $(SiH)_2$. High-temperature data retention testing for over 10^4 seconds on devices programmed to the low-resistance state (LRS) and the high-resistance state (HRS) demonstrate the robust nonvolatile nature of the device. Our experimental results and RS model provide insights into device electrical characteristics and charge transport, and may help identify localized, defect-driven switching mechanisms in SiO_x-based RRAM devices.

3.1. EDGE AND BULK DEVICE STRUCTURES, AND BACKWARD-SCAN EFFECT [50]

The SiO_x-based ReRAM devices are compatible with many different electrode materials. Figure 3.1 (a) and (b) show scanning electron microscopy (SEM) cross-section and tilted-view images of a metal-insulator-metal (MIM) edge-device architecture fabricated at Tronics MEMS Inc. The planarized TiW metal (M1) electrode is formed by first depositing 1 μm SiO_2 and 100nm Si_3N_4 as a polish-stop layer onto Si substrate using low-pressure chemical vapor deposition (LPCVD), etching 350nm-deep trenches into the dielectric stack using photolithography and reactive ion etch (RIE), sputter depositing TiW, and using chemical mechanical planarization (CMP). A 60 nm-thick SiO_x layer was

deposited using plasma-enhanced chemical vapor deposition (PECVD) with $SiH_4/N_2O/N_2/NH_3$ chemistry, followed by a 350 °C densification anneal in N_2 for 30 minutes. Via openings in the SiO_x layer were patterned using photolithography and buffered oxide etch (BOE). A top metal (M2) electrode comprised of 120 nm of TiW and 900 nm of Al was sputter-deposited, patterned and etched using standard Al and TiW wet etchants. A fourth photolithography module formed a SiO_x sidewall in some regions where M2 overlaps M1. The planarized TiW M1 and top TiW/Al M2 electrodes terminate at probe pads for electrical test using an Agilent B1500A semiconductor device analyzer and a Lake Shore Cryotronics vacuum probe chamber at < 1 mTorr.

Figure 3.1 (c) shows averaged *I-V* curves of 10 switching cycles for an MIM device without (1R) and with a series external transistor (w/ 1T). For the 1R configuration, voltage was applied to the top electrode with bottom electrode at ground; for w/ 1T configuration, the 1R device is connected to the 1T drain with voltage sweep on the top electrode and a constant gate bias (2.4 V in this case) to control the channel resistance (source and body are grounded). The compliance current limit was set to 1 mA during each 4 V forward/reverse sweep used to program the device to the LRS. Unipolar switching is observed for both cases, but V_{reset} in the 1R case is smaller than in the external 1T-1R configuration. By sweeping the voltage to 8 V, the current begins to decrease at V_{reset} and the device is programmed into a HRS. During the subsequent 4 V forward/reverse sweep, the current increases suddenly at V_{set} and sets the device to a LRS. The HRS/LRS resistance ratios for both cases are at least ~10^3 at 0.2 V. Before switching cycle measurements, a one-time electroforming process is performed, where

leakage current fluctuations to ~ 1 μA are observed with increasing bias. The electroforming process is completed during the backward voltage sweep from forming voltage (about 15 V - 18 V with 84 % device yield) to 0 V, resulting in a LRS (discussed further below). In Figure 3.1 (c) inset, switching voltage parameters V_{reset} and V_{set} are examined in detail by varying gate voltage V_g to control the channel resistance of the external transistor. The mean value and standard deviation of V_{reset} increase with channel resistance, from 2.31 V to 3.74 V and from 0.11 to 0.78, respectively. V_{set} is independent of V_g. In our previous reports, V_{reset} was always larger than V_{set}, which may have resulted from high contact or interfacial resistance resulting from the choice of electrode material. Metal filament formation, for example a filament resulting from metal atoms diffusing into the SiO_x layer, can be ruled-out in this case since the *I-V* response maintains the characteristic response for SiO_x materials and since switching only occurs in non-oxidizing ambient.

Figure 3.2 (a) and (b) show SEM cross-sectional and tilted-view images of a metal-insulator-semiconductor (MIS) device without an etched sidewall in the SiO_x layer that is typically used to enhance electroformation. The simple, capacitor-like MIS device structure is described in previous reports. In addition to the absence of a sidewall (resulting in the so-called "bulk" device, specifically shown in Figure 3.2 (b)), the only other fabrication difference is that the top TaN electrode was deposited using a lift-off process so that there was no plasma-induced damage or etching of the SiO_x layer (as for an "edge" device). Figure 3.2 (c) shows *I-V* characteristics for 50 switching cycles in a bulk device. No compliance current limit was used during the 4 V forward/reverse

sweeps. The HRS/LRS resistance ratio at 0.2 V is reduced to only one order of magnitude for these programming conditions, much lower as compared with the TiW device (Figure 3.1 (c)). The TaN bulk device electroforming voltage (typically above 25 V) was also higher than that for the TiW edge device (typically below 18 V). Device yield and electroforming voltage for different anneal ambients at 500 ^{o}C/2 minutes were also examined (Figure 3.2 (c) inset). The electroforming voltage and device yield of bulk devices are improved by incorporating hydrogen or deuterium into the SiO_x layer, as reported previously for edge devices, although the reduction in electroforming voltage was not as dramatic for the bulk devices. Successful electroformation and switching in the bulk device demonstrate that etching a sidewall into the SiO_x layer is not required, and that reversible switching can also occur in bulk SiO_x regions. In addition, doping with hydrogen or deuterium reduces formation energy and produces more stable filaments without a large change in switching parameters, but may result in a lower HRS/LRS resistance ratio.

Another unusual electrical characteristic of SiO_x-based ReRAM (regardless of an edge or bulk structure) is the backward-scan effect where the duration of the reverse sweep during electroforming or RESET determines whether a state change occurs, as illustrated by the DC and AC pulse response in Figure 3.3 (a) and Figure 3.3 (b), respectively. As mentioned above, during the forward sweep in the electroforming process, current fluctuations occur at about 1 μA followed by a backward sweep that forms a switchable filament, even if the electroforming process is momentarily stopped (see step 1 to step 3 in Figure 3.3 (a) where the backward sweep was stopped at 8 V in

the electroforming process, the state was checked at 1 V followed by a SET process). The backward-scan effect can also be observed in the RESET process, where the device changes from HRS to LRS if the backward scan is done slowly (step 4 in Figure 3.3 (a)). The dependence of the backward-scan effect on AC pulse falling time as a function of temperature is shown in Figure 3.3 (b). The SET voltage in all cases is fixed at 4 V DC with 1 mA compliance current limit to get a repeatable LRS prior to RESET pulse. The 8 V AC pulse used for the RESET process has a fixed rising time of 10 ns and pulse width of 100 μs but different falling times were used. At room temperature (RT) devices are RESET to the HRS for falling times less than 4 μs, but for longer falling times device RESET fails and the device remains in the LRS. As temperature is decreased, the transition point in falling time increases from 4 μs to 100 μs (RT to 250 K). Based on the above discussion, SiO_x-based ReRAM devices have the following properties that are typically not observed in conventional filament models: (1) Switching requires a non-oxidizing ambient; (2) unipolar operation with tunable reset transition voltage (Figure 3.1 (c)); and (3) a temperature-dependent backward-scan effect. Recently, we have proposed a resistive switching model involving the transformation between a hydrogen bridge (Si-H-Si) defect in the LRS and a hydrogen doublet $(Si\text{-}H)_2$ defect in the HRS driven by proton (H^+) transfer. Passivation by H is thought to stabilize device state at low applied voltage (< 2 V) in air, but when H-passivation is lost during a switching event, O_2 can disable switching. In this model, electron de-trapping from $(Si\text{-}H)_2$ initiates H^+ emission to form Si-H-Si during the SET process. This may explain the temperature dependence of the backward scan effect. This is since electron de-trapping rate is expected to increase as

temperature increases, the SET transition occurs at shorter falling times at RT as compared to lower temperatures (Figure 3.3 (b)). The RESET switching process may be driven either by Joule heat or an electrochemical reaction. Additional investigation into reversible switching is ongoing and will be described in future reports.

A Verilog-A model was developed in order to incorporate the backward-scan effect and resistive switching behaviors into circuit-level simulations (Figure 3.4). Three voltage thresholds are used to define the device-programming window: SET, Upper SET and RESET, as shown in Figure 3.4 (a). The LRS programming window (ON) is defined as the voltage range from SET threshold to Upper SET threshold, while the HRS programming window (OFF) is the voltage range greater than the RESET threshold. Once the applied voltage across the device enters a programming window, a state change may occur depending on how long the voltage remains in the programming window. Device measurements using fast and slow voltage sweeps (Figure 3.3 (b)) are used to determine the required duration for state transition. Figure 3.4 (b) explains the method used in the Verilog-A model to determine whether the programming time is able to switch the device. The backward-scan effect occurs when the reverse voltage sweep is too slow so that the device switches from OFF to ON. This is implemented by using digital timing signals in the model (Figure 3.4 (b)). When the voltage enters the ON programming window, digital signal *crossed_on* goes from 0 to 1, and when it leaves the ON window the *crossed_on* signal goes back from 1 to 0. The timing for digital signal *vcrosson* is delayed from the *crossed_on* signal by a fixed amount. The fixed delay is a user-defined parameter in the model to accommodate devices that may have different

switching speeds. If the voltage leaves the ON programming window and the two digital signals are both 1, the device will switch from OFF to ON (backward-scan effect), whereas, if *vcrosson* is still 0 the device switches OFF. Examples of fast (red line) and slow (blue line) backward voltage sweeps are shown in Figure 3.4 (a) and (b). The slow sweep causes the device to switch back to the ON state while the fast sweep only spends a short time in the ON programming window so that the two digital signals do not overlap and the device remains OFF. Based on previous work, the device *I-V* response can be modeled using $I = G_m V e^{B_m \sqrt{V}}$, or $R = 1/G_m e^{B_m \sqrt{V}}$, where R is device resistance and G_m and B_m are variables that can be extracted for a number of different device states (m), with m = 1, 2 and 3 describing the initial, ON (low-resistive) and OFF (high-resistive) states, respectively. The backward-scan effect is simulated by applying a periodic 8V triangular voltage signal, as shown in the bottom of Figure 3.4 (c). Both the rising and falling time of the triangular voltage waveform are 80 μs, which allows the voltage to remain in the ON and OFF programming windows much longer than the device switching speed. As shown by the current and resistance plots in Figure 3.4 (c), the device initially switches from OFF to ON during the leading edge of the first triangular sweep, and then begins to turn OFF when the voltage rises above the RESET threshold. However, since the falling edge of the sweep is too slow, the device turns back ON and subsequent sweeps are unable to turn the device OFF, thus demonstrating the backward-scan effect. As a result, during the RESET process it is very important to control the falling time of AC signals to avoid the backward-scan effect and achieve device RESET.

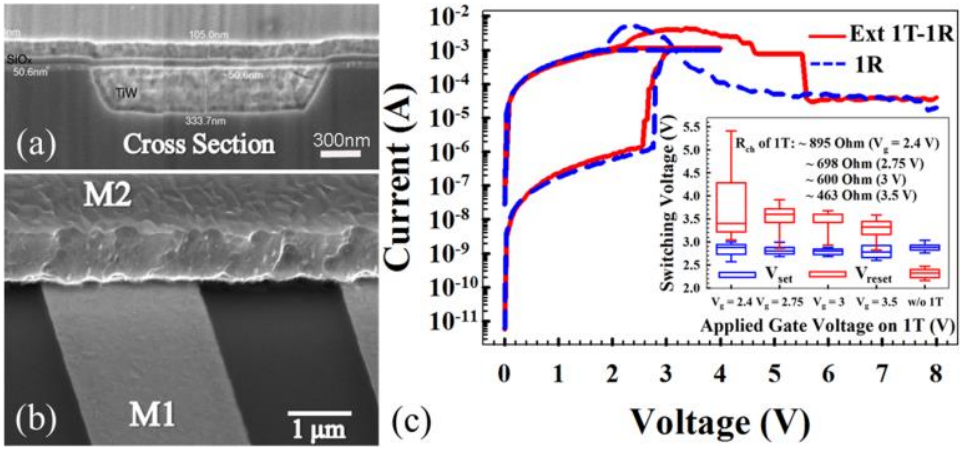

Figure 3.1. (a) Cross-sectional and (b) tilted-view SEM images of MIM edge-device, and (c) resistive switching behaviors with and without an external 1T-1R configuration.

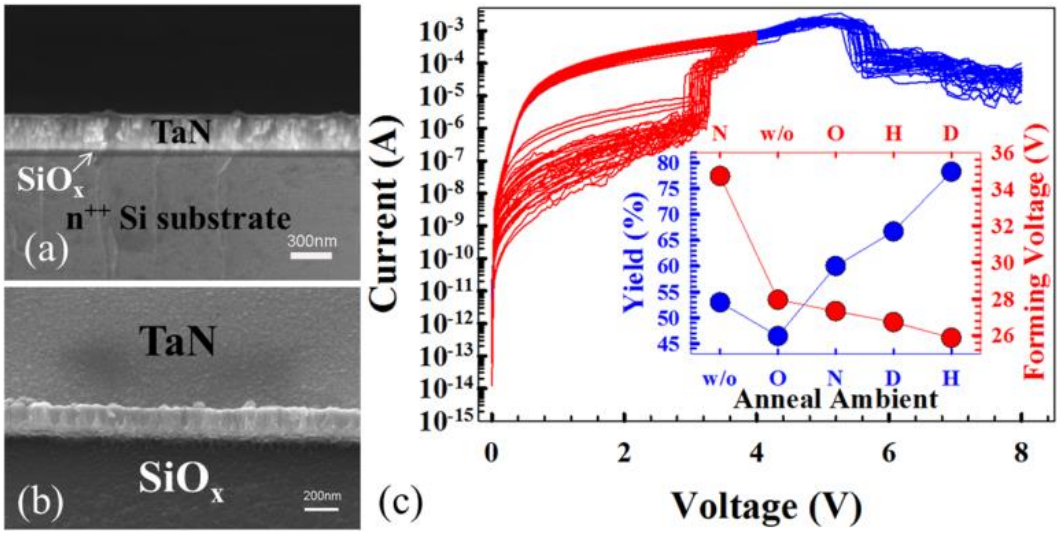

Figure 3.2. (a) Cross-sectional and (b) tilted-view SEM images of MIS bulk-device, and (c) resistive switching behaviors.

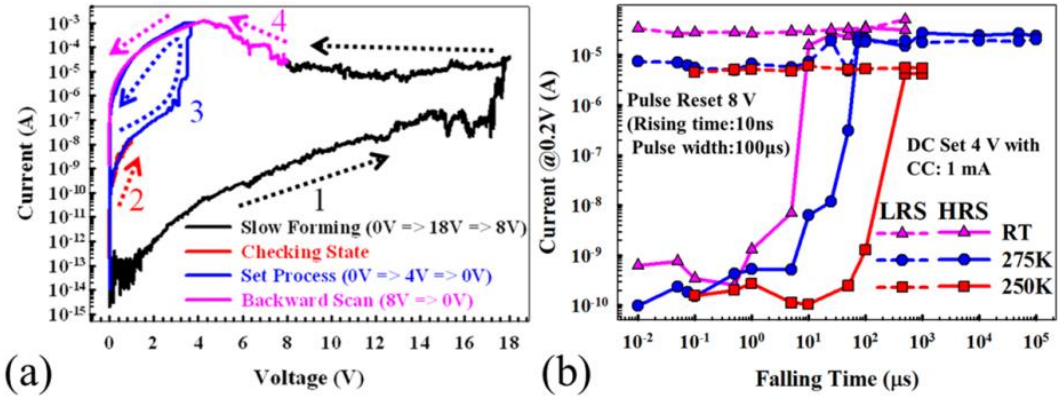

Figure 3.3. (a) The backward-scan effect in DC sweep. (b) The backward-scan effect using AC pulses with controlled falling times versus temperature.

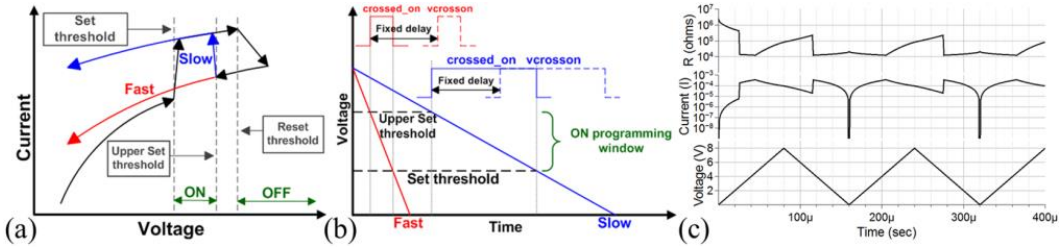

Figure 3.4. The fast (red) and slow (blue) backward voltage sweeps plotted in (a) I-V and (b) V-t form. (c) Resistance (R), current (I) and voltage (V) simulation results from OFF to ON state.

3.2. Oxide Stoichiometry Effects and Program Window Optimization [51]

The Three types of SiO_x RRAM device structures were fabricated for comparison: (1) metal-insulator-metal (MIM); (2) metal-insulator-semiconductor with an exposed SiO_x edge (MIS-edge); and (3) metal-insulator-semiconductor bulk (MIS-bulk) devices having a continuous SiO_x layer. The detailed fabrication process flow for $TaN/SiO_x/n^{++}$ Si MIS devices (Figure 3.5 (a), top panel) has been reported previously. The MIM devices (Figure 3.5 (a), bottom panel) were fabricated at Tronics MEMS Inc. in a crossbar architecture using a planarized bottom TiW electrode formed by etching trenches into a SiO_2 isolation layer, TiW sputter deposition and chemical mechanical planarization.

Before measuring switching characteristics, an electroforming process is performed under vacuum or N_2 ambient conditions, as shown in inset of Figure 3.5 (b), typically by applying a forward/reverse voltage sweep to a voltage level where current fluctuations of ~ 1 μA are induced and a negative resistance characteristic is observed during the reverse portion of the sweep. Electroforming voltage varies significantly depending on device structure, oxide deposition method, and thermal anneal conditions. The forming voltage is typically larger for MIS-bulk devices (~ 30 V) as compared to MIM and MIS devices with an exposed edge (< 18 V) [inset of Figure 3.5 (b)], most likely due to a higher concentration of defects (induced by non-stoichiometric composition, dangling-bond or oxygen vacancies) and potential leakage current pathways at the exposed sidewall surface in edge devices, whereas such high defect concentrations in bulk oxide regions are purposely avoided in materials commonly used in the industry. The MIS-edge devices were processed using RIE to pattern the top TaN electrode, but any defects created in the oxide by plasma-induced damage during RIE are removed by the subsequent BOE. However, electroforming voltage has been shown to decrease substantially after exposure to an additional Ar plasma treatment done after BOE, which is attributed to the electrical stress on the oxide layer as a result of the voltage induced across the oxide layer during the plasma treatment, and forming voltage also decreases after deuterium or hydrogen anneal. In general, we have found that electroforming occurs more readily (i.e. at lower voltage) in oxide materials with high as-deposited defect concentrations such as those deposited by electron-beam evaporation, PECVD and reactive sputtering. The possibility that metal filaments are formed within the SiO_x layer

is ruled-out based on TEM observations and since switching only occurs in non-oxidizing ambients. The nature of filament formation in SiO_x-based RRAM is expected to involve localized increases in Si content and the release of O^{2-} ions, most likely driven by high-energy electron impacts and the associated Joule heating. As discussed in more detail below, these findings make it clear that the oxide defect concentration is a critical parameter that must be controlled in order to optimize the electroforming process by lowering electroforming voltage, reducing variability and increasing yield. Electroforming is a one-time process that results in a LRS when using the forward/reverse sweeping method.

Figure 3.5 (a) and (b) show scanning electron microscopy (SEM) cross-section images of MIM and MIS structures, and *I-V* plots of 30 switching cycles for MIM, MIS-edge and MIS-bulk devices. The simple, capacitor-like MIS structures are described in previous reports. In each case, voltage was applied to the top electrode with bottom electrode grounded. For the MIM and MIS-edge *I-V* plots shown in Figure 3.5 (b), a compliance current limit of 1 mA was used during each 4 V forward/reverse sweep to program the device to the LRS. No compliance current limit was used for the MIS-bulk device due to the distinctive self-compliant current behavior of the SiO_x device (discussed in more detail below). The use of a compliance current during the SET process is not required, but can be used to help characterize the SET transition. Unipolar switching is observed for all device structures. During the RESET sweep to 8 V, current begins to decrease at V_{reset} and the device is programmed to a HRS. During the subsequent 4 V forward/reverse sweep, current increases suddenly at V_{set} and sets the

device to a LRS. In contrast to the other two device structures, the MIS-Bulk device shown in Figure 3.5 (b) exhibits a HRS/LRS resistance ratio of only about one order of magnitude under these programming conditions. Although this can satisfy minimum sensing requirements, the ratio for the MIS-bulk device can be increased by simply increasing the RESET program voltage to above 8V.

After extensive characterization of multiple devices with each structure, we find that MIM devices generally have higher overall yield than MIS-edge and MIS-bulk devices, where overall yield takes into account electroforming yield and short-term cycling yield. The simple crossbar design and the PECVD oxide layer used in the MIM architecture provide RRAM devices with good yield (at this stage of development), low electroforming voltage, and low series resistance that allows a tunable programing window (as discuss further below), all of which are highly-desirable for practical circuit-level applications. The effects of switching layer stoichiometry on electroforming voltage and device yield are discussed further below.

As shown in Figure 3.5 (b), the RESET transition can depend dramatically on device structure, where average V_{reset} values ranged from 2.72 V to 5.04 V in MIM and MIS-bulk devices, respectively, and the I-V response above V_{reset} was either gradual, as in the MIM device, or steep, as in MIS devices. In contrast, V_{set} is largely independent of device structure owing to the voltage-triggered process and is possibly independent of current or Joule heating (as discussed below in more detail). In our previous reports, similar behavior was observed in MIM devices when varying the gate voltage of a MOSFET in series with the RS device in order to control the external resistance of the

circuit. For MIS-edge and MIS-bulk devices, contact resistance between the probe and TaN top electrode can be relatively large (~ 250 – 350 Ohms, as determined by independent measurements of series resistance) due to the high hardness of the TaN material (leading to a small contact area with the probe), and the n^{++} Si substrate further increases the external series resistance (as estimated below). In contrast, MIM devices have low contact resistance due to the softer Al probe pads and typically less than ~ 250 Ohm series resistance in the TiW metal interconnect line. As a result, there is a larger voltage drop across the series resistance in the MIS devices as compared to the MIM device, and therefore the MIS devices require higher applied voltage to initiate the RESET process, leading to larger V_{reset} values in the raw *I-V* data. External series resistance does not affect the SET transition because the current is several orders of magnitude smaller in the HRS and the voltage drop across the external resistance is negligible.

The V_{reset} values in the MIS-edge device are typically lower than in the MIS-bulk device, perhaps as a result of higher defect concentration at the oxide sidewall (etched by using BOE) in the MIS-edge device, which may lead to higher surface conduction during the electroforming process and formation of a more robust, lower-resistance conductive filament. A possible explanation for higher resistance in the MIS-bulk device is that removing O^{2-} ions from the bulk oxide material during the vacuum electroforming process may be more difficult as compared to the MIS-edge device, where O^{2-} ions can more easily escape into the vacuum. Electroforming is thought to involve oxygen reduction reactions, consistent with oxide breakdown mechanisms where high-energy

electron injection breaks Si-O bonds and releases O^{2-} ions. We speculate that a higher concentration of O^{2-} ions may become trapped within the bulk oxide layer of the MIS-bulk device and may inhibit electroforming by re-oxidizing portions of the filament as it is being formed, thereby leading to higher internal filament resistance and enhancing the self-compliant current behavior in MIS-bulk devices. As a result, the larger defect concentration in MIS-edge devices may lead to lower electroforming voltage and a more robust conductive filament having larger cross-sectional area and overall lower resistance, whereas lower defect concentrations and the potential for larger O^{2-} concentrations in MIS-bulk devices will lead to higher filament resistance, increased V_{RESET} and steeper RESET transitions in the *I-V* response.

Figure 3.6 shows electrode material and device structure effects on SET and RESET switching voltages, where dependencies are observed primarily for V_{reset}. The MIM device has the lowest switching voltages, whereas the MIS-bulk structures have V_{reset} values ranging from 5.5 V to 9 V, more than twice as large as the MIM device with V_{reset} = 3.5 +/- 0.3 V. Nickel was found to have the highest bulk electroforming yield (about 90%) and auto-forming process (< 10V); Ni may act as an effective oxygen getter to help remove liberated O^{2-} ions from the filament as it is being formed. Other important parameters measured for each electrode combination include forming voltage and device yield, which show some dependence on device structure. For example, MIS-edge devices typically exhibit 15 - 18 V electroforming voltage with 70 % yield, and MIS-bulk devices have 30 – 35 V electroforming voltage with about 65 % yield, similar to the yield results shown in Figure 3.5 (b). The fabrication approach with the highest MIS-bulk electrical

yield uses e-beam-deposited SiO_2 and a lift-off process to fabricate the top electrode. In the lift-off process, photoresist is patterned to form openings that expose the SiO_2 layer to the developer chemical and de-ionized H_2O rinse prior to metal deposition and photoresist removal. This suggests that the high porosity of the e-beam SiO_2 material and the additional exposure to H_2O during the lift-off process may be important reasons why the combination of lift-off process and e-beam material successfully yields working bulk devices. The lower density of e-beam SiO_2 may allow any O^{2-} ions generated during the electroforming process to readily diffuse away from the filament or drift to an electrode where the ions can react and be neutralized. In addition, porous e-beam SiO_2 may have a high density of "pinholes," which are thread-like, low-density defects known to increase oxide leakage current. In this case the pinhole (or other defective region) with the highest initial leakage current will lead to conductive filament formation in bulk devices. Furthermore, metal electrode deposition in the lift-off process is done at low temperature (to protect the photoresist) after exposure of the SiO_2 layer to H_2O during photoresist development, the combination of which is likely to result in a large amount of H_2O-related defects at the metal/SiO_2 interface. Although hydrogen in SiO_x might be considered to be an extrinsic impurity, it is so common in SiO_x materials that it is often considered to be intrinsic. We speculate that pinhole defects may act similar to a surface where OH, protons and other H_2O-related defects can diffuse deep into the SiO_2 bulk, thus providing a source to form additional reactive species during the electroforming process that lead directly to the defects responsible for reversible switching.

The effects of SiO_x thickness and device area on operating performance of MIS-edge devices are shown in Figure 3.7. It is found that LRS and HRS current, as well as the SET and RESET voltages, are all independent of device area and SiO_x thickness, illustrating that charge transport and resistive switching occur in a localized region along a conductive filament. The electroforming voltage was previously found to decrease with SiO_x thickness until hard breakdown and loss of switching occurs at ~ 6 nm SiO_x thickness, whereas 10 nm-thick samples could be electroformed but exhibited lower yield and less-stable switching performance than thicker samples, suggesting that the effective length of the switching region in the filament may be in the range from 6 nm to 10 nm. Kim *et. al*. have reported that the localized "switchable filament" is about 3-10 nm in size and is located near the interface between the insulating layer and anode electrode for devices using TiO_2 materials. Our previous studies have suggested that resistive switching in SiO_x materials may occur at the cathode side rather than the anode side due to oxygen vacancy clustering and asymmetrical thermal dissipation at the two electrodes, which can potentially result in the polarity dependence observed in RESET switching parameters. Together, these findings clearly indicate that switching occurs in a small region along the filament rather than throughout the entire bulk SiO_x layer, so that two distinct regions can be defined in the conductive filament: a first filament region that is formed during electroforming and remains intact during reversible switching; and a second "GAP" region that is responsible for the SET and RESET switching operations. The device *I-V* response remains essentially unchanged for a large range of SiO_2 thicknesses and electrode areas, indicating that resistive switching in

SiO_x-based devices follows a filament-type of characteristic rather than interface-type resistive switching.

Based on our previous work summarized above and a review of the reported electrochemical reaction dynamics and energetics of common SiO_x defects, a localized switching model involving proton exchange reactions is proposed. Figure 3.8 (a) shows a schematic representation of the CF similar to models used to describe stress-induced leakage current and breakdown in SiO_x materials, where defect concentration increases as a result of electrical stress to the point where percolation pathways capable of conducting appreciable current (> 1 μA) are formed. The region along the filament with minimum cross-sectional area is defined as the switching region, or "GAP," consistent with similar models used to characterize HfO_2, $Ge_2Sb_2Te_5$ and TiO_2 RS materials where oxygen vacancies are found to be the electron traps most likely involved in switching. The maximum GAP length occurs when the device is programed with high voltage to achieve a HRS with maximum resistance. Our hypothesis is that electrically-active defects within the GAP remain localized, and are converted between conductive and non-conductive forms by electrochemical reactions that occur during the switching transitions. In the LRS, most all defects in the switching region are in the conductive form, whereas, in a HRS, a significant fraction of defects have been converted to their non-conductive form. This modeling approach allows the resistance of the GAP region to vary uniformly with the concentration of conductive defects to account for all intermediate-resistance states between the LRS and the maximum-resistance HRS. Several studies have documented the presence of Si nanocrystals within the CF using TEM, although it is not yet clear

whether RS is the result of an overall increase in nanocrystal size or whether switching occurs at locations in between the nanocrystals. Our model can accommodate both viewpoints where on the one hand the conductance GAP can be viewed as increasing in length when nanocrystal size decreases or, on the other hand, the GAP may be viewed as the result of a uniform decrease in conductive defect concentration.

Most models of RRAM switching involve drift or diffusion of oxygen vacancy defects, Si-Si, (or equivalently, O^{2-} ions), but these models cannot explain the unipolar I-V response or the robust nonvolatile data retention properties of the SiO_x device. As found in a previous study, the CF is directly exposed to O_2 whenever a (unpassivated) device is exposed to air. The reaction of O_2 with Si-Si defects in amorphous SiO_2 occurs immediately at room temperature without an activation energy barrier to form Si-O-O^{+}Si. Also, H_2O vapor in the air would eventually diffuse into the switching region and react with Si-Si defects when the device is biased above ~ 1.3 V, which corresponds to the activation energy of the electrochemical reaction. Both of these reactions would be expected to alter programed data if Si-Si defects were present, but this is not observed in our experiments or those of others where programed states remain nonvolatile after many months of air exposure. Furthermore, a switching model based on Si-Si creation/annihilation driven by O^{2-} ion drift cannot account for the unipolar operating characteristics because the O^{2-} ions will drift in the same direction during both SET and RESET programing events, making it very difficult to explain where the O^{2-} ions go and how they return to the switching region. As a result, the instability of Si-Si oxygen

vacancy defects with regards to reactions with O_2 and H_2O, and the incompatibility with unipolar operation make it unlikely that these defects are involved in switching.

Attempting to switch devices in 20% O_2/N_2 ambient at 1 atm pressure is found to disable switching, and yet programed states in unpassivated devices are nonvolatile under 1 V constant bias for several hours at 150 °C in 1 atm air. Our working hypothesis to explain these results is that the defects involved in RS are H-passivated and are therefore inert to reactions with O_2 and H_2O in the air under low bias, but, when bias is increased to $> \sim 2.5$ V so that a switching event occurs, the defects are temporarily un-passivated and O_2 or H_2O in the air can react with the defects to disable switching. Oxide materials deposited at low temperatures such as those used here are typically rather porous and susceptible to moisture uptake when unpassivated and exposed to air. There have been many reports over several decades documenting that residual H_2O in electrically-stressed metal-oxide semiconductor (MOS) devices introduces H^+ and OH^- into the oxide layer, which drift in the applied field towards the cathode and anode, respectively. One H_2O decomposition pathway is reaction with Si-Si to form SiH + SiOH, so that SiO_2 materials with high as-deposited Si-Si concentrations are expected to form these species more readily than high-quality materials with few defects such as thermal oxide. Using a new dissociative water potential, recent molecular dynamics simulations of H_2O adsorption onto SiO_2 surfaces reveals a new mechanism for dissociative chemisorption involving the formation of H_3O^+ as a reaction intermediate leading to silanol (Si-OH) formation in the near-surface region, where Si-OH density is estimated to approach 3.8 molecules/nm^2. All of these reported results make it reasonable to assume that ample H_2O-related defects

are present near the SiO_x sidewall which provide a source of hydrogen as the CF forms during the high-field electroformation process. Support for this assumption is provided by previous results showing that anneal in H_2-containing ambient significantly reduces electroforming voltage by over 50%. Anneal in H_2 is expected to form a high concentration of $(SiH)_2$, which can then directly form electrically-conductive Si-H-Si by emitting a proton. In this way the energy required to electroform the CF could be significantly reduced, in-line with the experimental observations.

Based on the reported electrical and structural properties of known SiO_x defects, it is clear that small changes in defect composition can dramatically alter the defect's conductivity. We view the electrically-conductive hydrogen bridge (Si-H-Si) as the most likely defect in the LRS for the same reasons that it is considered the most likely candidate for stress-induced leakage current (SILC) in MOS devices, including the small separation of ~ 1.2 – 2.6 eV between switching charge-state energy levels and a thermodynamic energy level near the Si mid-gap energy so that trapped electrons are loosely-held and charge is easily exchanged with the electrodes. As shown schematically in Figure 3.8 (b), in our model proton capture by Si-H-Si defects forms non-conductive $(Si-H)_2$ defects in the HRS, which are known to trap electrons in a stable, shallow energy level near the amorphous SiO_2 valence band-edge and about 2.7 eV below the Si mid-gap energy level. This concept directly raises the questions of where the proton goes when it is released from the $(SiH)_2$ defect during the SET transition and how the proton comes back to the Si-H-Si defect during the RESET transition.

Proton uptake and release by a water molecule is viewed as a potential mechanism that enables localized switching, where the water molecule acts as both a reservoir and source for the proton. In the 1990s, E. H. Poindexter developed a hydrogen physical chemistry model to investigate the potential reactions of H_2O in SiO_2, leading him to postulate the reaction $2H_2O \rightarrow H_3O^+ + OH^-$.This reaction was verified in 2002 using first-principles density functional theory (DFT) calculations finding that $2H_2O$ in "bigger voids" react to form a mobile OH^- ion (that can easily be removed from the void by ~ 0.3 eV) and a *localized* H_3O^+ ion that may contribute to positive fixed-charge in as-deposited SiO_2 materials. The energy barrier for the reaction is ~ 1.5 eV and involves a total energy of only 0.4 eV. The H_3O^+ attaches to an O atom in the Si-O-Si network to form Si_2=O-H_3O^+. Formation of H_3O^+ has long been established in weak ionic solutions such as HF and H_2O, where the reversible reaction $HF + H_2O \leftrightarrow F^- + H_3O^+$ is known to occur. Since SiO_2 is also a weak ionic medium, it is reasonable to expect that H^+ uptake by H_2O to form H_3O^+ will occur in SiO_2. In fact, DFT calculations have established that H^+ uptake by interstitial H_2O can form H_3O^+ near Si/SiO_2 interfaces when interfacial Si-H and a hole are present, which proceeds with only a ~ 0.8 eV reaction barrier and ~ 0 eV forward energy. Experimental data link trace amounts of H_2O in thermal oxides to bias-temperature instability (BTI) in MOS devices as a result of this mechanism. These findings make it reasonable to expect that similar proton exchange reactions will occur in bulk SiO_2 materials, especially near SiO_2 surfaces previously exposed to water vapor. Therefore, as a stable, localized, positive fixed-charge, the H_3O^+ ion is a very good candidate for being involved in reversible switching since it can potentially release a H^+

to leave a H_2O molecule that is then available for H^+ uptake in a reversible reaction that depends on the local charge environment.

Our resulting hypothesis is that proton exchange reactions between the defect complex shown in Figure 3.8 (b) can support reversible switching in SiO_2 materials, where proton emission from $(Si\text{-}H)_2$ and uptake by chemisorbed water $(Si\text{-}OH)_2$ forms the conductive defect Si-H-Si and fixed positive charge H_3O^+ in the LRS. In the reverse reaction, injection of two electrons induces H^+ release from H_3O^+ and charges the Si-H-Si defect negative, which leads to the exothermic reaction $H^+ + Si\text{-}H^-\text{-}Si \rightarrow (Si\text{-}H)_2$ that releases ~ 3 eV of energy. As discussed in more detail in Part II, electrons are not able to access the H_3O^+ defect at low voltage since the energy levels of the H_3O^+ are expected to be high in the SiO_2 bandgap and at least ~ 2.5 eV higher than the energy levels of the Si-H-Si defect. Although perhaps many other defect complexes could perform essentially the same electrochemical operations, the proposed complex provides a straightforward description of reversible switching in SiO_2 materials that is consistent with the established energetics of well-characterized defects. To provide deeper insights regarding the feasibility of the proposed switching reactions, future work plans include DFT calculations investigating proton uptake by $(Si\text{-}OH)_2$ and the stability of the dipole (potentially) formed by the $Si\text{-}H\text{-}Si^-/H_3O^+$ complex in the LRS. In Part II of this paper, we investigate charge transport mechanisms for their role in reversible switching and correlate specific defect energy levels to the RS transitions in the I-V response, where we find that the energy levels of the proposed defects are well-matched to transitions in the I-V response and the measured electron energy barriers in the HRS and LRS.

Figure 3.9 shows XPS analysis results for the O-1s and Si-2p binding energies in thermal oxide grown by low-pressure chemical vapor deposition (LPCVD), sputtered oxide with PDA, and PECVD oxide. The existence of stoichiometric SiO_2 can be observed in all samples (binding energy Si: 103.2 eV; O: 532.5 eV), especially for the thermal oxide with essentially no sub-oxide bonding (SiO_x with $x < 2$) being detected. Based on our previous reports, thermal oxide devices are in general difficult to electroform, require high electroforming voltage ~ 30 V, and have relatively poor RS performance as compared to oxides deposited at lower temperatures. In contrast, the sputtered oxide with PDA and the PECVD oxide devices are readily electroformed and consistently show good RS performance, which may result from the non-stoichiometric SiO_x ($x < 2$) composition in the switching layer, as indicated by the peak binding energies in the XPS spectra (Si: 530.5 eV; O: 101.9 eV and 100.9 eV). It has been reported that both nitrogen- and hydrogen-passivation of Si bonds may exist within the PECVD SiO_x layer, specifically by observing the Si 1p signal in XPS measurement. For the O 1s signal, the cooperated hydrogen and nitrogen are difficult to distinguish because their peaks are quite close to the SiO_2 bonding energy, but the sub-oxide (SiO_x) component can still be estimated. The characteristic peaks for Si_3N_4 and $SiN_{0.91}$ in the Si 1p XPS spectrum are located at 101.9 eV and 100.85 eV, respectively, and the NH_3 peak in Si is also located at similar binding energies (100.9 eV and 101.8 eV). These results suggest that we cannot rule out the possibility for nitrogen- or hydrogen-passivation in our SiO_x layers. It may be noted that PECVD oxide showed the largest degree of non-stoichiometry out of the three oxide materials tested, and we speculate that the associated

sub-oxide defects may promote higher leakage current during the electroforming process that leads to the low electroforming voltages and "autoforming" characteristics observed in PECVD oxides.

Figure 3.10 (a) shows several electroforming *I-V* plots for devices using SiO_xN_y switching layers with varying stoichiometry (as verified by refractive index measurements). The *I-V* plots are unusual because they exhibit autoforming characteristics, where fresh devices begin the electroforming process with high leakage current as if they were already in a LRS, followed by a sudden current decrease to a HRS at low voltage ~ 6 V. During the reverse portion of the electroforming sweep, the devices switch to the LRS at 4 – 5 V. Devices showing such autoforming capability can have electroforming voltages as low as V_{RESET}.

Figure 3.10 (b) plots electroforming yield and average forming voltage versus refractive index (n @ 600 nm) of the SiO_xN_y layer as measured by spectroscopic ellipsometry. The devices were fabricated with a MIS-edge structure having 50 nm-thick SiO_xN_y. The refractive index depends on the N_2O/SiH_4 flow rate ratio used during the PECVD process. The flow rates and corresponding n values measured in this experiment were: $SiH_4/N_2O/N_2/NH_3$ = 77/Y/100/6 sccm, where Y = 80 (n = 1.540), 60 (n = 1.578), 40 (n = 1.642), 20 (n = 1.770), 0 (n = 1.905)). The difference in refractive index values demonstrates that the SiO_xN_y composition is changed by controlling the N_2O flow rate, where "oxygen-rich" devices deposited at higher N_2O flow rates have n closer to 1.46 consistent with a near-stoichiometric SiO_2 material, and "nitrogen-rich" devices deposited at low N_2O flow rates have n = 1.9 indicating an SiO_xN_y layer approaching

Si_3N_4 (n = 2.05). Figure 3.10 (b) shows that electroforming voltage decreases with decreasing refractive index (increasing N_2O flow rate). Electroforming voltage decreased to 10 V and yield increased to ~ 90 % for the oxygen-rich deposition conditions of $SiH_4/N_2O/N_2/NH_3$ = 77/80/100/6 sccm, clearly indicating that materials closer to stoichiometric SiO_2 perform much better than materials with significant nitrogen content. These results may imply that the high as-deposited defect concentration normally present in PECVD SiO_x materials is significantly reduced by nitrogen and hydrogen incorporation. The reduction in electroforming voltage may be related to the binding energies of Si-N (355 kJ/mol), Si-H (318 kJ/mol), and even Si-Si (222 kJ/mol) being weaker than Si-O (452 kJ/mol). The passivation of SiO_x dangling bonds during the PECVD deposition process can reduce the as-deposited defect concentration, but the weak bonding energy of non-SiO_2 bonds can potentially lower the forming energy. In addition, the choice of gas sources (for example NH_3) may lower electroforming voltage for our devices, as compared with robust thermal oxide materials. The proposed model of Figure 3.8 (b) can further potentially explain why significantly lower electroforming voltage is measured in PECVD SiO_x materials. During plasma-enhanced deposition, H is incorporated into the SiO_x layer from the gas sources (NH_3 or SiH_4), which may lead to formation of $(Si\text{-}H)_2$. As described above, proton emission from the $(Si\text{-}H)_2$ defect provides a low-energy (~ 2.5 eV) pathway to directly form Si-H-Si. In contrast, materials without H-incorporation and low Si-Si concentration must form Si-H-Si via multiple interactions involving hot electrons and water-related defects. For example, in high-quality oxides, hot electrons must first generate Si-Si defects (requiring > 9 eV), and then

water-related defects such as OH^- and H^+ must diffuse or drift to the Si-Si defects and react to form Si-H-Si (requiring a total energy of ~ 5 eV). The overall energy required to electroform is therefore substantially reduced in H-incorporated SiO_x materials with high as-deposited defect concentrations since H^+ emission from $(Si\text{-}H)_2$ provides a direct, low-energy pathway to form Si-H-Si. Band diagrams based on the specific energy levels of $(Si\text{-}H)_2$ and Si-H-Si defects are found to be consistent with the measured LRS and HRS electron energy barriers and switching transition voltages observed in the I-V response, providing additional support for the proposed localized switching model of Figure 3.8.

Figure 3.11 shows averaged *I-V* curves for a MIM device with and without an external series transistor (shown as a resistor in the circuit schematics). By controlling the gate voltage to vary the channel resistance of the external transistor, V_{reset} was observed to increase as external series resistance increased. Also, the RESET *I-V* transition above V_{reset} changed from having a gradual fall-off in current to having a steep reduction in current as external series resistance increased. However, V_{set} is found to be independent of series resistance, which suggests that the SET process is primarily a voltage-triggered mechanism largely independent of current or Joule heating. We estimate that the local filament temperature increase due to Joule heating in the HRS is only about 60 ^oC at 2 V bias, making Joule heating an unlikely driver of the SET process. The results also make it clear that the different program window ($V_{reset} - V_{set}$) characteristics observed for different device structures (Figure 3.5 (b)) may be due to the parasitic series resistance in each device structure (MIM, MIS-edge and MIS-bulk). Figure 3.12 further illustrates the program window dependence on series resistance. The

linear fit to MIM raw data was extrapolated and the measured program windows for MIS-edge (1.4 V) and MIS-bulk (2.0 V) devices were used to estimate an effective series resistance of 1400 Ω in the MIS-edge device and about 2100 Ω in the MIS-bulk device. It may be noted that the effective series resistance may include contact resistances between probes and electrodes, the n^{++} Si substrate and top electrode resistance, the resistance of the intact portion of the conductive filament, as well as any voltage drops at the two filament/electrode interfaces that may be caused by energy band misalignments. The y-intercept of the linear fit in Figure 3.12 is 0.17 V, suggesting that the intrinsic switching voltages for both SET and RESET processes are essentially equal so that $V_{reset} \sim V_{set}$, as observed for the MIM device in Figure 3.5 (b) and in Figure 3.11 for the device with smallest series resistance. This is consistent with the proposed switching mechanisms being driven by a reversible electrochemical reaction that requires the same energy in both directions. The larger program window in MIS devices may result from the series resistance of the n^{++} Si bulk substrate and the larger program window in MIS-bulk structures relative to MIS-edge structures may involve formation of a more tenuous, less-robust conductive filament as a result of lower defect concentrations in bulk devices. In any event, the data clearly demonstrate that series resistance affects RESET *I-V* characteristics (gradual versus steep transitions) and leads to a larger program window as series resistance increases. The controllable program window demonstrated here can potentially be used to improve the program/erase disturbance immunity of the device in circuit-level applications.

Figure 3.13 shows high temperature (85 ^{o}C) static data retention performance of

MIM and MIS-edge devices programed to the LRS and HRS in vacuum. The four devices were electroformed and cycled by applying a 4 V forward/reverse SET sweep with 1 mA compliance current limit and an 8 V RESET sweep. Then, the LRS and HRS current was measured at 0.2 V after every decade of time in MIM and MIS-edge devices. In Figure 3.12, the retention reliability test for both device structures and states are stable with a resistance ratio of at least three orders of magnitude and no significant degradation is observed for more than 10^4 sec, further confirming the excellent nonvolatile properties of the SiO_x-based resistive switching device.

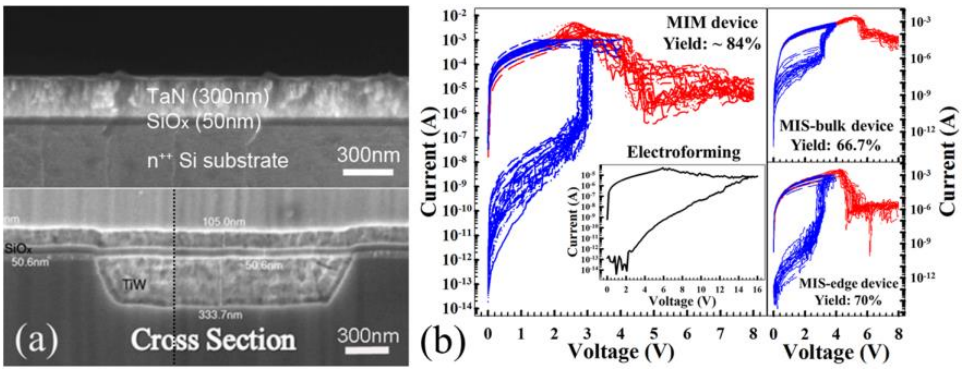

Figure 3.5. (a) SEM images of MIS and MIM structures. (b) 30 cycles of I-V plots for MIM, MIS-bulk and MIS-edge devices with corresponding yield labeled.

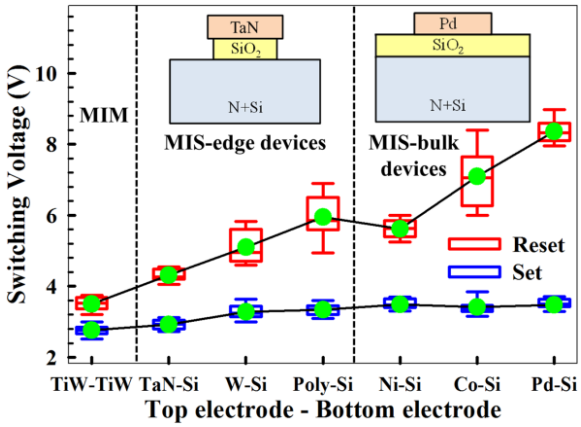

Figure 3.6. Effects of electrode material on SET and RESET switching voltages in MIM, MIS-edge and MIS-bulk devices.

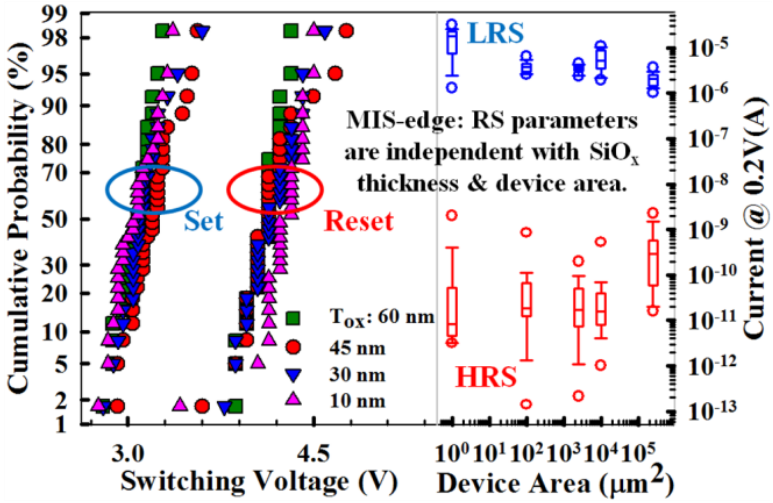

Figure 3.7. RS parameter dependence on SiO_x thickness and device area in MIS-edge devices.

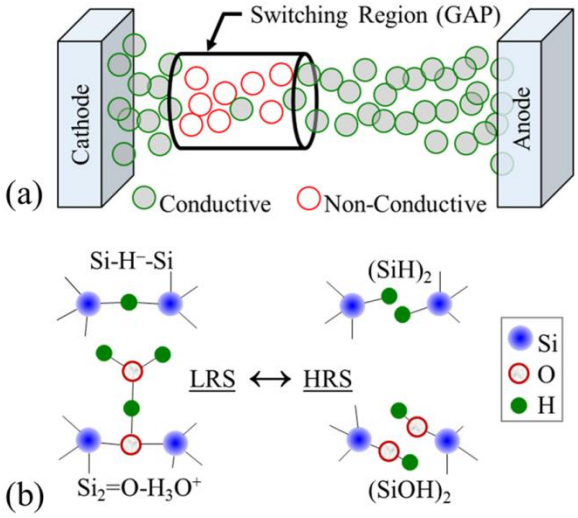

Figure 3.8. (a) Physical representation of conductive filament with switching region. (b) Hypothesized defect complex in LRS and HRS.

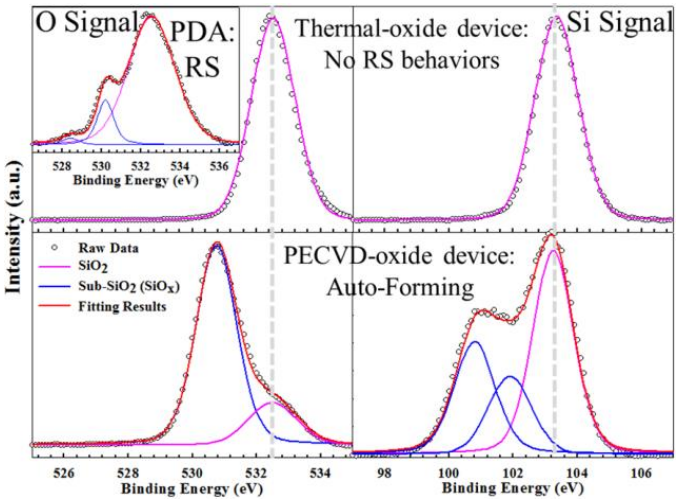

Figure 3.9. XPS spectra and fitting results for LPCVD thermal oxide, sputtered oxide with PDA treatment, and PECVD oxide.

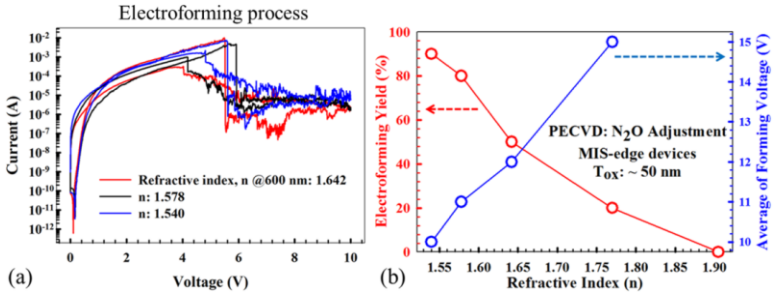

Figure 3.10. (a) I-V plots for SiO_xN_y-based devices, demonstrating autoforming capability. (b) Device yield and forming voltage versus refraction index.

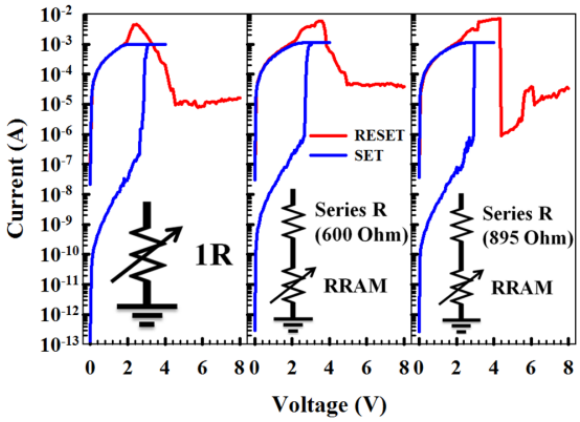

Figure 3.11. RS characteristics of MIM device with and without an external series transistor.

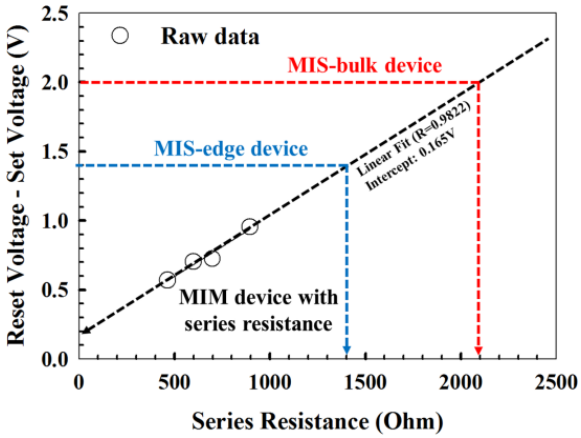

Figure 3.12. Program voltage window ($V_{reset} - V_{set}$) dependence of MIM structure versus external series resistance.

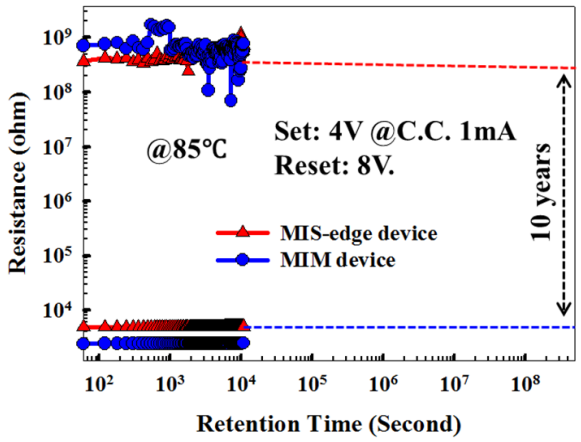

Figure 3.13. Static data retention test at 85 ^{o}C for MIM and MIS-edge devices programed to the HRS and LRS.

3.3. MULTILEVEL, TEMPERATURE EFFECT AND BAND DIAGRAM MODELING [52]

Figure 3.14 (a) and (b) show the unipolar resistive switching response for MIS and MIM devices, and the effects of varying CCL from 10 µA to 3 mA during the SET process while keeping RESET voltage fixed at 7 V. The CCL was only applied during the 4 V forward/reverse sweep to SET the device to a LRS. Figure 3.14 shows the RESET sweeps to 7 V that programs the device to the HRS. In the low-voltage region <

2 V, one can see that the resistive states of SiO_x-based RRAM can be programed by varying the CCL to achieve intermediate states between the LRS and HRS. For the programing cycles that used small CCL values (10 – 500 μA), SET transitions are clearly observed at 2 – 3 V. The SET transition voltage has been found to range from 2.5 – 3.5 V in MIM devices, and from 3.5 – 4 V in MIS devices, both depending on the magnitude of the previous RESET programing pulse, as discussed further below. Current continues to increase in the 3.5 to 5 V range and there is a clear "programing window" in between the SET and RESET transitions in the MIS device (Figure 3.14 (a)), whereas decreasing current is observed in the MIM device beginning at 3 V and the program window is very small. We have described in Part I how the series resistance of the circuit leads to the larger program window in MIS devices. The charge transport mechanisms corresponding to each region in the I-V response and device switching transitions are discussed in more detail below.

Figure 3.15 shows that multiple states in the MIM device can be programed by controlling the RESET stopped voltage magnitude. This device was SET using a forward sweep from 0 – 4 V, and these I-V curves are used to measure the device HRS in the low-voltage region and the SET transition to the LRS in the range from 2.5 to 3.5 V. Very large programed resistance can be achieved using this method, where LRS/HRS current ratios up to 10^8 can potentially be achieved. The programing range observed in the Figure 3.15 plot is ~ 5 orders of magnitude, which corresponds to the ratio of the LRS current of ~ 10^{-4} A at 1V to the highest-resistance state programed using RESET stopped voltage of 12 V and having current of ~ 10^{-9} A.

We also investigated programing the device to intermediate LRS values by controlling the CCL. Figure 3.16 (a) shows detailed results of the CCL effect on LRS current for the MIM and MIS devices shown in Figure 3.14. The LRS current levels at 0.2 V increase in both devices by roughly 1-2 orders of magnitude as CCL is increased from 10^{-5} A to 3 mA. The roughly 1 order-of-magnitude range in the measured values at each CCL setting leads to the inability to clearly distinguish the programed states for adjacent CCL settings. However, it may be possible to program two distinguishable states using CCL values of 3 mA and 10 μA. Despite the large available programing range, the variability observed in programed states, which typically increases with programed resistance, continues to hinder the demonstration of more than three clearly-distinguishable programed states, and methods are needed to reduce the within-device and device-to-device variability so that a viable multistate device with four or more states can be achieved.

SET transition voltage is plotted versus RESET stopped voltage in Figure 3.16 (b), where an increasing trend is observed for both MIM and MIS devices. The overall larger SET transition voltages in MIS relative to MIM devices may be the result of an additional electron energy barrier at the interface between the n^{++}Si cathode and the conductive filament in the MIS device, as will be investigated in future reports. As described further below, we attribute the SET process to electron tunneling through $(SiH)_2$ defects in the switching region. The increasing SET voltage trend with RESET stopped voltage is discussed further below with the aid of a band diagram, where the

asymmetrical effective bandgap of $(SiH)_2$ and the larger tunneling distance in the HRS combine to limit tunneling probability and thus increase SET voltage.

To investigate charge transport mechanisms, *I-V* data were analyzed by fitting to common insulator charge transport expressions. Table I lists the voltage dependence of current and normalized conductance G_N for the five insulator charge transport expressions investigated, where $G_N = G_d/G$, with dynamic conductance G_d being given by $G_d = \partial I/\partial V$ and static conductance being $G = I/V$.

Charge Transport	I	G_N	Linear Fitting Plots
Poole-Frenkel	$gVe^{\beta\sqrt{V}}$	$1+\beta\sqrt{V}/2$	$\ln(I/V)$ vs $V^{1/2}$
Fowler-Nordheim	$AV^2e^{-B/V}$	$2 + B/V$	$\ln(I/V^2)$ vs $1/V$
Schottky	$I_oe^{\rho\sqrt{V}}$	$\rho\sqrt{V}/2$	$\ln(I)$ vs $V^{1/2}$
Hopping	KVe^{LV}	$1+LV$	$\ln(I/V)$ vs V
Power Law	MV^p	p	$\ln(I)$ vs $\ln(V)$

Tabel 3.1. Voltage dependence of current (I) and normalized conductance (G_N), and the axes used for linear fitting are listed for common insulator charge transport expressions.

Analyzing plots of G_N can help identify the active charge transport mechanism and the voltages where a change in charge transport occurs. As shown in Figure 3.17, there is no temperature dependence, CCL effect or device structure dependence observed in the G_N plots for MIM and MIS devices, thus verifying that the fundamental charge transport mechanisms are unaffected by these variables under all programing conditions. There is a clear increase in slope and variability in the HRS plots; however, the G_N plots

in all cases have an intercept near unity, which indicates either ohmic transport, ionic transport, Poole-Frenkel emission, or hopping conduction, as opposed to Schottky thermionic emission (where the intercept would be close to 0 according to Table 3.1) or space-charge-limited current according to Child's Law (where I is proportional to V^2 so that the intercept would be 2). We rule out ohmic and ionic transport since these mechanisms would have $p = 1$ in Table 1 but zero slope in a plot of G_N versus V, whereas there is instead a clear slope in G_N data observed in Figure 3.17. Thus we are left with Poole-Frenkel emission and hopping conduction as possible charge transport mechanisms for current in the low-voltage region from 0 – 2 V. These two transport mechanisms are known to be quite similar when electron-trapping defects are involved. The slight transition in the LRS G_N plots at ~ 0.5 V may be associated with trap-filling mechanisms that depend on electron emission from the cathode into charge-trapping defects in the filament as the bias is swept from 0 V to 0.5 V.

Based on the above discussion, we focus the low-voltage analysis on the Poole-Frenkel (P-F) and hopping conduction mechanisms. Figure 3.18 shows the temperature-dependence of P-F fitting results for HRS and LRS in MIM and MIS devices. The P-F emission formula is:

$$\textbf{Poole-Frenkel emission}: \quad J = BV \exp\left(\frac{-q(\phi_t - \sqrt{qV / \pi\varepsilon_r\varepsilon_0 d})}{kT} \right) \qquad (1)$$

where B is a constant, q is the elementary charge, ϕ_t is the energy barrier that must be overcome by the electron, ε_r is relative permittivity of the RS medium, d is SiO_x thickness, k is the Boltzmann constant and T is local filament temperature. Figure 3.18

indicates that the electron energy barrier is 0.6 eV in the HRS and 0.1 eV in the LRS as V approaches 0. As described above, the intermediate states between LRS and HRS can be controlled by CCL and RESET stopped voltage magnitude. Conceptually, the resistance states can be characterized as a change in defect concentration for a collection of defects within the switching region. We also must consider that each individual defect may have more than one conductance state to account for the scenario where reversible switching could simply be the result of electrically-altering the defects between conductive and non-conductive forms. Writing the total defect concentration as $n = n_1 + n_2$, where n_1 denotes the conductive defect concentration and n_2 denotes the non-conductive concentration, allows us to account for two possible conductance states for the defects in the switching region. In the LRS state, $n_1 >> n_2$ so that high current flows through conductive defects and the electrons encounter a small energy barrier of 0.1 eV, whereas, when a large fraction of the n defects are converted to their non-conductive form so that $n_2 >> n_1$, the barrier increases to 0.6 eV and the device is in a HRS.

Hydrogen (H) is so common in SiO_x materials that it is typically considered an intrinsic defect, so that a comprehensive investigation into potential defect-driven switching mechanisms must include H-related defects. In Section 3.2, we proposed that proton exchange reactions could be driving the defects in the switching region between a conductive Si-H-Si form and a non-conductive $(SiH)_2$ form. A companion defect that acts as both a proton reservoir and proton source was postulated to be the Si_2=O-H_3O^+ defect in the LRS and the $(SiOH)_2$ defect in the HRS. Additional support for this model is based on recently-reported electroluminescence measurements, TEM studies and the reported

density functional theory (DFT) calculations for defects in SiO_2, as discussed further below.

We also analyzed low-voltage current transport using the fixed-range hopping expression, as shown in Figure 3.19 (a). The hopping conduction formula is

$$\textbf{Hopping conduction}: \quad J = qnav_0 \exp\left[-\frac{q\left(\phi_t - aV/2d\right)}{kT}\right] \qquad (2)$$

where n, a, ϕ_t, v_o, and d are concentration of space charge, mean of hopping distance, electron barrier height for hopping, intrinsic vibration frequency, and SiO_x thickness, respectively.[57] As shown in the Figure 3.19 (a) inset, the electron barrier height is determined from the slope of a linear plot of ln(I) versus 1/T at each V condition so that the activation energy $E_a = q(\phi_t - aV/2d)$ is determined as a function of voltage, as shown in Figure 3.19 (a). The intercept with the vertical axis represents the electron energy barrier to hopping transport and the slope allows the hopping distance to be calculated if the film thickness is known. Typical values for the hopping barrier and distance are listed in Figure 3.19 (a) for MIM and MIS devices in the LRS. The values do not differ significantly for the two device structures, where the electron barriers are 88.6 meV and 98.2 meV, while the hopping distances are 1.32 nm and 1.61 nm for the MIS and MIM devices, respectively. However, both hopping barrier and distance are a strong function of programed resistance, as shown in Figure 3.19 (b), where both the barrier height and hopping distance increase substantially as resistance increases. Overall, the temperature dependence data indicate that the defects responsible for charge transport have an average hopping distance of ~ 1 nm in the LRS, and the energy barrier to electron hopping is

quite small ~ 0.1 eV. In the HRS, the barrier height is observed to approach 0.6 eV for high-resistance states and the calculated defect spacing is significantly larger (6 – 12 nm). The P-F and hopping results are consistent in that they both predict similar electron barriers across the entire programing range of the device. The result of a 0.6 eV barrier in the HRS is consistent with historical measurements of the barrier height in SiO_2 materials deposited using CVD, thus demonstrating that charge transport in the HRS is similar to transport in SiO_2. The results are also consistent with the reported energy barriers in Si-rich SiO_x devices, where the LRS barrier was reported to be 0.086 eV and the HRS barrier was 0.52 – 0.66 eV. In extrinsic Cu/SiO_2 materials, the reported energy barrier is 0.63 eV and the hopping distance is 1.3 nm, both of which are very similar to our results for intrinsic SiO_2.

Current in the moderate-voltage region (3 – 5 V) shows no CCL effects and exhibits different characteristics than current in the low-voltage region, as observed in the Figure 3.14 (a) I-V plots. Transport in this voltage range is found to fit well to the Fowler-Nordheim (F-N) tunneling expression:

Fowler-Nordheim tunneling: $$J = \frac{q^2 \mathrm{E}^2}{16\pi^2 \hbar \phi_{ox}} \exp\left[\frac{-4\sqrt{2m^*}(q\phi_{ox})^{3/2}}{3\hbar q \mathrm{E}}\right] = C_4 \mathrm{E}^2 \exp\left(\frac{-C_5}{\mathrm{E}}\right) \quad (3)$$

where E is electric field (V/cm), q is the elementary charge, ϕ_{ox} is the energy barrier that must be overcome by the electron, m^* is electron mass in SiO_2, $\hbar$ is the reduced Planck constant, $C_4 = 9.63\times10^{-7}$ (A/V^2), and $C_5 = 2.77\times10^{8}$ (V/cm) is related to the energetics of the Si/SiO_2 system as reported by Yao et. al and Sze. As shown in Figure 3.20, using an acceptance criteria of 99 % linearity, data fitting to the F-N expression led to an extracted

electron barrier height of 0.1 eV in devices with film thickness d = 60 nm (MIM), and the result was independent of temperature (inset of Figure 3.20). Each of the three transport mechanisms that were investigated in detail resulted in the same estimate of 0.1 eV for the LRS electron barrier, suggesting that useful information regarding device physical parameters can be obtained from all three analyses. An accurate fit to the F-N expression is often viewed as an indicator of trap-assisted tunneling, and has been used to identify TAT as a predominant current transport mechanism in Si-rich SiO_x (x ~ 0.9) RRAM devices. The LRS I-V response is plotted on a linear scale in Figure 3.21 to demonstrate how the F-N fit in the region from 2 – 3 V departs from the hopping conduction fit in the low-voltage region from 0 – 1.5 V. We refer to this departure from the low-voltage response as the "overshoot" region. The I-V data plotted in Figure 3.21 were corrected for the measured device series resistance of 235 Ω. A linear extrapolation of the data in the overshoot region to the V axis is used to estimate the threshold for overshoot, where we find V_{th} = 1.57 ± 0.15 with no dependence on RESET stopped voltage (inset of Figure 3.21). The overshoot region is clearly observed in Figure 3.14 (a) from 3.5 – 5 V for the MIS device, where series resistance effects in the MIS device cause stretch-out of the overshoot region and lead to the large program window.[14]

In order to further investigate the dielectric properties of the switching region, the relative permittivity was extracted and characterized. The P-F formula in (1) can be rearranged to give

$$\ln(J/V) \propto \left(const(\phi_t) + \frac{\sqrt{q^3 V/\pi\varepsilon_r\varepsilon_0 d}}{kT} \right), \qquad (4)$$

where the slope in data plotted versus $V^{1/2}$ is used to extract ε_r with: $q = 1.6\times10^{-19}$ C; $\varepsilon_0 = 8.854\times10^{-12}$ F/m; $d = 50\times10^{-9}$ m; and $k = 1.38\times10^{-23}$ J/K. For improved accuracy, the local filament temperature was first determined by analyzing the effects of temperature on device resistance. When voltage is applied and current flows through the filament, the local filament temperature T_{Local} can increase as a consequence of Joule heating. For a symmetric filament configuration, device electrodes will be at room temperature and maximum temperature will occur in the switching region. The *I-V* plots in Figure 3.22 show an increase in LRS current with temperature over the range from 300 to 375 K. The resistance decrease with increasing voltage is due to the exponential term in the P-F, or hopping conduction expression, and is markedly different than binary oxides based on metal filament formation and breakage that exhibit ohmic transport and increasing resistance with temperature. As shown in the inset of Figure 3.22, resistance decreases with temperature like in a semiconductor according to

$$R(T) = R_O \left[1+\alpha\left(T - T_O\right)\right] \tag{5}$$

with thermal coefficient α = -0.013 K^{-1} obtained from the linear fit. Once α was known, the resistance R_o was used as a thermometer to determine T_{Local} in the switching region as a function of V and ambient temperature T_o, as shown in Figure 3.23. The two plots in the left panel of Figure 3.23 show that both α and T_{Local} increase with current, presumably due to Joule heating. The LRS I-V plots in the center panel show that T_{Local} may approach 450 K when devices are biased with 2 V at room temperature, whereas T_{Local} only reaches ~ 360 K in the HRS due to the much higher resistance and less Joule heating (right panel

in Figure 3.23). Figure 3.24 shows the relative permittivity extraction method, where linear fits are made to devices programmed to the LRS, several intermediate states, and the HRS at T_o = 300 K (top panel). Extracted relative permittivity values are shown in the two lower panels, where the left panel plots the data assuming no increase in T_{Local} and the right panel shows the data corrected for T_{Local}. The uncorrected ε_r values are quite high at 200 – 300 for $I > 10^{-5}$ A, and there is a wide distribution of values when $I < 10^{-6}$ A. However, the data corrected for T_{Local} show two tight groupings for ε_r values, 70 ~ 80 for LRS with $I > 10^{-5}$ A, and ~ 4 for HRS with $I < 10^{-5}$ A. Very little permittivity temperature dependence was observed over the tested range from 300 – 375 K. In previous reports, we have proposed a RS model involving the transformation between Si-H-Si defects in the LRS and $(SiH)_2$ defects in the HRS, and have suggested that these transformations may be driven by proton transfer to and from a water molecule that forms Si-H-Si and H_3O^+ in the LRS. A stable dipole formed by this pair of defects could explain the large ε_r of ~ 80 in the LRS.

The localized reversible switching model presented in Part I and the energy band diagrams shown in Figure 3.25 and Figure 3.26 can be used to illustrate possible SET/RESET mechanisms and the electron energy barriers calculated in the above charge transport analyses. The band diagrams were constructed using the thermodynamic and switching charge-state energy levels of several electron-trapping defects as reported by Peter Blochl in 2000 and listed for reference in Table II. The unoccupied switching charge-state energy levels of closely-spaced defects are associated with an effective conduction band-edge, whereas the occupied levels are associated with an effective

valence band-edge, thus forming an effective bandgap. The small effective bandgap energy (E_G) of 1.70 eV for $Si*SiO(3)^+$ and 1.71 eV for Si-H-Si enable these two defects to conduct significant current in MOS devices. As described in Section 3.2, and discussed in more detail below, the defects involved in reversible switching may include Si-H-Si and $(SiH)_2$, where localized proton transfer drives a collection of defects in the switching region between conductive Si-H-Si and non-conductive $(SiH)_2$. In the proposed model, we account for the scenario where the defects remain at the same physical location within the switching region and their electrical conductivity is simply modified by proton release and capture. Our discussion below further identifies the specific hydrogen desorption and electrochemical reactions that may represent the fundamental mechanisms responsible for reversible switching in SiO_x materials.

Defect	–	**Charge-States**	E_C	E_{TH}	E_V	ΔE_G
Si-Si	–	+/0	-1.38	-3.03	-3.70	2.32
$(SiH)_2$	–	+/0	-1.07	-2.74	-3.67	2.60
$Si*SiO(3)^+$	–	+/0	0.68	-0.06	-1.02	1.70
Si-H-Si	–	0/-	1.58	0.74	-0.13	1.71
$SiH + SiSi(5)^-$	–	0/-	1.27	0.30	-1.85	3.12

Tabel 3.2. Defect switching charge-states, unoccupied switching charge-state energy level (E_C), thermodynamic energy level (E_{TH}), occupied switching charge-state energy level (E_V) and effective bandgap energy (ΔE_G).

The ideal band diagrams in Figure 3.25 and Figure 3.25 assume that both electrodes are TiW with Fermi level at the Si midgap energy. The hopping distance in the

LRS was estimated to be ~ 1 nm (Figure 3.19) based on data fitting to the hopping formula, which is only expected to estimate the distance between unoccupied defects (without a trapped electron) so that the actual physical spacing between defects may be ~ 1/2 the estimated hopping distance. As a result, a defect is placed every 1/2 nm in the energy band diagram to represent one filamentary current pathway through the switching region.

We have hypothesized that $(SiH)_2$ and $(SiOH)_2$ defects form a conductance "gap" within the switching region that is responsible for the low conductance in the HRS. To construct the HRS energy band diagram shown in Figure 3.25 (a), the switching region from 10 nm to 16 nm was filled with $(SiH)_2$ defects to form a conductance gap with length of l_{GAP} = 6 nm. The filament regions outside the switching region were filled with Si-H-Si, SiH + SiSi(5) and H_3O^+ to account for the low-resistance portions of the conductive filament. We place the energy level of H_3O^+ at 2.5 eV above the effective Si-H-Si conduction band-edge to match our findings that the fundamental RESET threshold is ~ 2.5 eV. This puts the H_3O^+ energy level 0.38 eV above the SiO_2 conduction band-edge, consistent with a fixed positive-charge defect.

To determine the relative band offsets in the Figure 3.25 and Figure 3.26 energy band diagrams, the standard methodology used for semiconductors was followed where each defect's thermodynamic energy level was aligned with the electrode Fermi levels at 0 V bias. This approach is consistent with Fermi-level pinning of the defects to near the Si midgap energy level, as expected for H-related defects. As shown in Figure 3.25 (b), after aligning the E_{TH} levels of the Si-H-Si and $(SiH)_2$ defects, a 0.83 eV electron energy

barrier is predicted as a result of the relative effective conduction band (E_C) offset between the two defects, which agrees reasonably well with the measured value of 0.6 eV (Figure 3.18 and Figure 3.19).

The Si-H-Si defect also has two interconversion products with modified bonding arrangements. The first is a positive-charged defect where the H atom and one Si atom form SiH and the other Si atom forms a 3-fold-coordinated bond with a network oxygen atom, $Si\text{-}O(3)^+$. The positive-charged oxygen atom can diffuse away to produce an isolated Si dangling bond, which we have proposed as a potential low-energy pathway that could lead directly to the Si-rich conductive filament during electroforming. The second interconversion product has stable neutral and negative charge states where one Si atom bonds to a network Si atom to make it 5-fold-coordinated, leading to $SiH + SiSi(5)^-$. Since Si-H-Si and $SiH + SiSi(5)^-$ are expected to form with approximately equal concentrations in amorphous SiO_2, we include both defects in the band diagrams using the energy levels listed in Table II. The difference in effective conduction band energy between the two defects is only 0.13 eV, with SiH + SiSi(5) being slightly higher in energy. As a result, the predicted electron energy barrier between $SiH + SiSi(5)^-$ and $(SiH)_2$ is ~ 0.70 eV in the HRS (see Figure 3.25 (b)), somewhat closer to our measured value of 0.6 eV.

The LRS band diagrams in Figure 3.26 were constructed as described above except that the switching region was filled with the conductive Si-H-Si and SiH + SiSi(5) defects and their corresponding H_3O^+ fixed positive charge. In Figure 3.26 (b), the small energy difference of 0.13 eV that exists between the effective conduction band-edges of

the Si-H-Si and SiH + SiSi(5) defects may lead to the ~ 0.1 eV energy barrier measured in the LRS (Figures. 18 – 20), where electrons hopping from trap-to-trap between the two defects would encounter the 0.13 eV energy barrier.

The Si nanocrystals observed using transmission electron microscopy (TEM) of SiO_x devices have been associated with reversible switching where they are thought to increase in size in the LRS, thus bringing neighboring crystals closer together and increasing conductivity, and where a transformation between amorphous and crystalline phases can occur within the nanocrystals. We view reversible switching as being related to defect transformations near the nanocrystal surfaces and in the regions between nanocrystals, similar to models described by Mehonic *et al*. for switching in Si-rich oxides. This line of reasoning is consistent with findings that charge transport occurs primarily along grain boundaries in HfO_2 and NiO memory materials, where oxygen vacancies are thought to be the electron traps most likely involved in reversible switching, and is also consistent with the "hour glass" model describing transport and switching as occurring at a narrowed "constriction" along the conductive filament.

In the LRS, the narrow constriction in the conductive filament results in higher resistance and an appreciable voltage drop across the switching region (Figure 3.26 (a)). As a result, the resistance of the switching region may dominate the filament resistance until the voltage increases above ~ 1.7 eV, where TAT through Si-H-Si defects effectively short-circuits the switching region, leading to the overshoot phenomenon and dramatic decrease in filament resistance observed in Figure 3.21. It is not clear what the relative concentrations should be for Si-H-Si and SiH + $SiSi(5)^-$ defects; however, of

these two defects, the TAT threshold at ~ 1.6 V observed in Figure 3.21 could only be associated with Si-H-Si since the effective bandgap is ~ 3.1 eV for SiH + $SiSi(5)^-$, much larger than that for Si-H-Si (1.7 eV), as listed in Table II and labeled in Figure 3.26 (a). This implies that any TAT through SiH + $SiSi(5)^-$ would show a threshold near 3.1 V, which is greater than the RESET threshold at ~ 2.5 V and therefore TAT through the SiH + SiSi(5) defect would never be observed. The only other well-characterized SiO_2 defect that could support TAT at ~ 1.6 V is the $Si^*SiO(3)^+$ defect, which is an oxygen vacancy defect known as the Eγ' charge center in amorphous SiO_2 that is formed by interconversion of the simple oxygen vacancy, Si-Si (Table II). As listed in Table II, the $Si^*SiO(3)^+$ defect has an effective bandgap of 1.7 eV; however, it is likely not involved in reversible switching due to the instability of oxygen vacancy defects in the presence of O_2 and H_2O, and the inability of an oxygen vacancy creation/annihilation mechanism to explain unipolar switching, as discussed in Section 3.2. In addition, the oxygen vacancy formation energy in SiO_2 is 0.9 eV, so that, if oxygen vacancy defects were involved in reversible switching, we would expect to see switching transitions at ~ 0.9 V. Since there are no such transitions in the I-V response, we have high confidence that oxygen vacancy defects are not involved in SiO_x reversible switching.

The band diagrams are consistent with recently-reported electroluminescence (EL) results with the LRS being associated with an EL peak of 1.6 eV, whereas the HRS emits light with a peak near 2.3 eV. The highest EL intensity was observed near the overshoot region of the I-V response, 3 – 7 V in the devices used in the EL study, which corresponds to the 3.5 – 5 V region in our MIS devices with moderate series resistance

that demonstrate good fits to the F-N tunneling characteristic (Figure 3.14 (a)). The series resistance in the EL study was not reported, so that it is not possible to directly compare the I-V response of the devices used in the EL study to those used here. Since the estimated overshoot threshold of 1.6 ± 0.2 V (Figure 3.21) corresponds to both the reported 1.6 eV EL peak and the theoretical effective bandgap of 1.7 eV for the Si-H-Si defect, we assign TAT as the charge transport mechanism responsible for the overshoot phenomenon in the LRS. The 1.6 eV EL peak has been attributed to electron-hole recombination, which would naturally occur during TAT through the Si-H-Si defect.

Based on the model described pictorially in Figure 3.8 of Section 3.2, we model the SET and RESET switching transitions as the overall reversible electrochemical reaction

$$Si\text{-}H\text{-}Si^{-} + Si_2{=}O\text{-}H_3O^{+} \leftrightarrow (SiH)_2 + (SiOH)_2 \qquad (6)$$

where (6) represents the state transitions given by LRS ↔ HRS for each defect complex.

Switching in the proposed complex is somewhat analogous to H activation/de-activation of thermal donor defects at SiO_2/Si interfaces, where the thermal donor is electrically active in an OHH configuration and inactive in an OHO configuration. In the proposed model, the defect complex is electrically active when the Si-H-Si defect is present, but electrically inactive when the complex contains the $(SiH)_2$ defect. During the SET transition, a proton is emitted from $(SiH)_2$ and the chemisorbed water molecule, or $(SiOH)_2$, uptakes the proton to form $Si_2{=}O\text{-}H_3O^{+}$. The stored proton can then be released when an electron is injected into the H_3O^{+} defect during the RESET transition. One interpretation of the defect complex is two H_2O molecules reacted with two oxygen

vacancy defects, while another view could be a chemisorbed H_2O molecule and a H_2 molecule reacted with a single oxygen vacancy. When the defect complex is in its conductive form, electrons trapped in Si-H-Si$^-$ cannot access H_3O^+ energy levels since they are high in the SiO_2 bandgap and at least ~ 2.5 eV above the Si-H-Si conduction band-edge. DFT calculations investigating proton uptake by $(SiOH)_2$ and the stability of the dipole formed by the Si-H-Si$^-$/H_3O^+ complex are slated for future work. Although perhaps there are many other defects that could perform essentially the same electrochemical operation, the proposed complex provides a straightforward, plausible description of reversible switching in SiO_2 materials.

The EL peak of 2.3 eV observed in HRS devices is consistent with TAT through the $(SiH)_2$ defect having an effective bandgap of 2.6 eV (Table II), which also corresponds well to the SET threshold at ~ 2.5 V. Our assignment for the 2.5 V SET threshold is hydrogen desorption from a SiH group within the $(SiH)_2$ defect, which is well-documented to have a desorption energy in the range of 2.5 – 2.9 eV at Si/SiO_2 interfaces in MOS devices. An increased probability for hydrogen release occurs when the $(SiH)_2$ defect is charged positive, which drives the two H atoms closer together and promotes H_2 dissociation. Positive charging of the $(SiH)_2$ defect requires that electrons be trapped and de-trapped by the defect, and so we assign TAT as the current transport mechanism that triggers hydrogen desorption to initiate the SET transition. Proton release is more favorable by ~ 0.5 eV over neutral H. The released proton is expected to react with chemisorbed (or interstitial) H_2O to form H_3O^+, as reported in both theoretical and experimental investigations of proton uptake by water near Si/SiO_2 interfaces, which

proceeds with a small reaction energy barrier of ~ 0.8 eV and ~ 0 eV forward energy when a hole is available for the reaction.

The HRS energy band diagrams in Figure 3.25 can potentially explain the increasing trend in SET voltage with RESET stopped voltage (Figure 3.16 (b)), which is also readily apparent in Figure 3.15. In the HRS, very little current flows and there is negligible voltage drop across the series resistance so that all applied voltage is dropped across the switching region. When the applied bias reaches ~ 2.6 V, TAT can occur through the $(SiH)_2$ defects in the switching region, as shown in Figure 3.25 (a). However, the tunneling probability is a strong function of tunneling distance x, with a functional dependence of $e^{-x/\lambda}$, where λ is a characteristic tunneling length. Hydrogen desorption from SiH depends on both V and I. As a result, when the device is programed with large RESET voltage, the length of the conductance gap may become larger than ~ 2λ so that TAT current is too low at 2.6 V bias to induce H desorption, resulting in the need to increase the voltage in order to increase TAT current and initiate the SET transition. In other words, for the 6 nm-long switching region shown in Figure 3.25, the electron tunneling distance x may be > λ at 2.6 V (Figure 3.25 (a)), but reduces to $x \sim \lambda$ as voltage is increased to ~ 3.4 V (Figure 3.25 (b)). This matches well with the measured SET voltage range of 2.6 – 3.4 V in MIM devices (Figure 3.16 (b)). It is also clear in Figure 3.25 (a) that, at 2.6 V bias, the asymmetric effective bandgap of the $(SiH)_2$ defect results in a longer electron tunneling distance for electron capture by the defect as compared to electron emission from the defect. However, when biased to 3.4 V as shown in Figure 3.25 (b), the tunneling distances for electron capture and emission become nearly equal,

thus maximizing tunneling probability and TAT current through the $(SiH)_2$ defects in order to induce H desorption and initiate the SET transition.

As shown in Figure 3.26 (b), our assignment for the RESET threshold, which approaches 2.5 V in devices with low series resistance, is F-N tunneling from the effective Si-H-Si conduction band into the H_3O^+ defect. This releases a H^+ that can react electrochemically with negative-charged Si-H-Si^- or SiH + $SiSi(5)^-$ to re-form $(SiH)_2$. The specific exothermic reaction described by Blochl involved a H^+ reacting with SiH + $SiSi(5)^-$, which was found to release ~ 3 eV. The localized H_3O^+ defect has been described as a fixed positive charge that attaches to the O atom in a Si-O-Si linkage in the SiO_2 network to form Si_2=O-H_3O^+. The exact energy levels of the H_3O^+ defect relative to SiO_2 band edges are to our knowledge unknown, but as a fixed positive charge, the energy levels would be located high in the SiO_2 energy bandgap near the conduction band-edge, consistent with our placement of H_3O^+ in the band diagrams (see Figure 3.26 (a)). The programed resistance of the device is a strong function of the applied RESET voltage, and so electron injection into a fixed positive charge defect would naturally explain the RESET stopped voltage effect (Figure 3.15) and the self-compliant behavior that appears to be specific to SiO_x materials. This is shown pictorially in Figure 3.26 (b) by the dashed arrows labeled with the voltage where F-N tunneling into the defect is allowed. As RESET voltage increases to above ~ 2.6 V, additional H_3O^+ defects become aligned with the Si-H-Si conduction band-edge so that electron tunneling through the triangular SiO_2 conduction band can convert H_3O^+ to H_2O and release a H^+. Therefore, as RESET voltage increases, a conductance gap with increasing length is formed, which of

course programs the device to a higher resistance at 1 V bias, as observed in Figure 3.15.

Consistent with TEM results showing Si nanocrystals in the conductive filament, switching in this model involves significant changes in O and H atomic positions that may result in an ordered morphology in the LRS, where closely-spaced defect clusters would align according to space-charge limitations due to the dipole formed by the Si-H-Si^{-}/H_3O^{+} complex. In contrast, the switching region in the HRS contains mostly neutral defects in the $(SiH)_2/(SiOH)_2$ complex without any space-charge effects, leading to what could be considered to be an amorphous phase. The proposed model is thus consistent with an in-situ study of reversible switching showing a more ordered morphology in the LRS, and a disordered, amorphous phase in the HRS. As noted in the study, TEM imaging with high-energy (200 keV) electrons resulted in the loss of programed states, and devices required re-electroforming after imaging. We speculate that exposure of the switching region to high-energy electrons will remove H and OH from the defects, perhaps leading to the observed loss of switching capability.

The energy band diagrams were constructed using the reported Si-H-Si and $(SiH)_2$ energy levels as determined by DFT calculations, and the good agreement between the electron energy barriers predicted by the band diagrams (0.7 – 0.83 eV in HRS and 0.13 eV in LRS) and the measured values (0.6 eV in HRS and ~ 0.1 eV in LRS) provides some level of confidence in the proposed switching mechanisms involving these defects. The band diagrams also naturally explain the reported EL results, where TAT through Si-H-Si defects with an effective bandgap of 1.7 eV corresponds to the 1.6 eV EL peak in the LRS, and TAT through $(SiH)_2$ defects with effective bandgap of 2.6 eV corresponds

to the 2.3 eV EL peak observed in the HRS. Our extracted relative permittivity value of ~ 80 in the LRS is consistent with the stable dipole potentially formed by the Si-H-Si^{-} /Si_2=O-H_3O^{+} complex. When the complex is in the inactive form $(SiH)_2$/$(SiOH)_2$, the extracted permittivity of ~ 4 is essentially that of SiO_2. Based on our charge transport analysis, the measured threshold of 1.6 +/- 0.2 V for the current overshoot phenomenon in the LRS is most likely due to TAT through the 1.7 eV effective bandgap of Si-H-Si defects. The RESET transition is assigned to F-N tunneling from the Si-H-Si effective conduction band into the H_3O^{+} defect, which was placed 2.5 eV above the Si-H-Si conduction band-edge in the energy band diagram according to the RESET threshold voltage of ~ 2.5 V reported in Section 3.2. F-N tunneling or electron injection into H_3O^{+} defects naturally explains the strong dependence of programed resistance on the RESET stopped voltage. In the HRS, TAT through the $(SiH)_2$ defects may directly initiate the SET switching transition by inducing H desorption and proton uptake by the $(SiOH)_2$ defect in the complex. As a result, the proposed switching mechanisms and the band diagrams based on the known energy levels of the Si-H-Si and $(SiH)_2$ defects provide a comprehensive, accurate model of operating performance and unipolar reversible switching in intrinsic SiO_x-based RRAM devices.

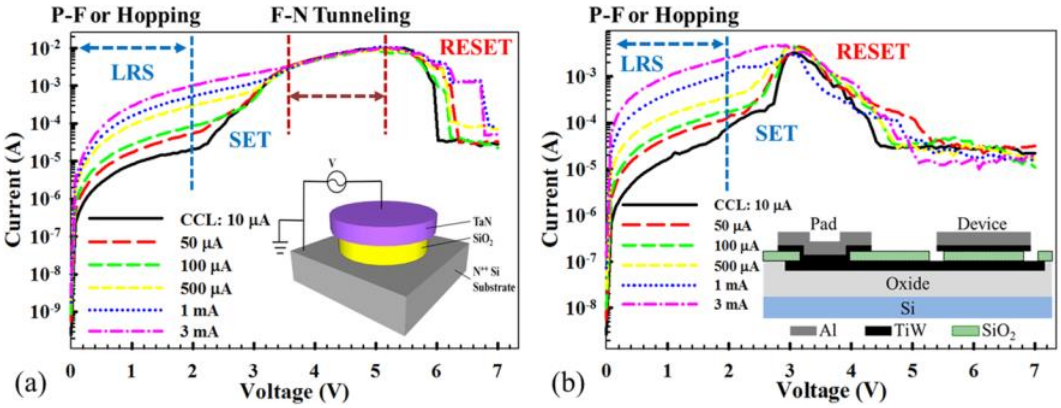

Figure 3.14. Current transport modeling in various voltage ranges with multi-level control by CCL in (a) MIS and (b) MIM structures.

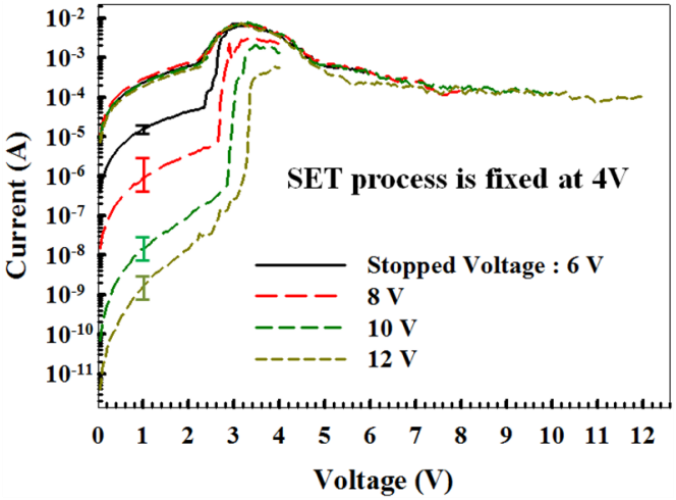

Figure 3.15. Switching behaviors and HRS curves for MIM device programed with a series of RESET stopped voltages.

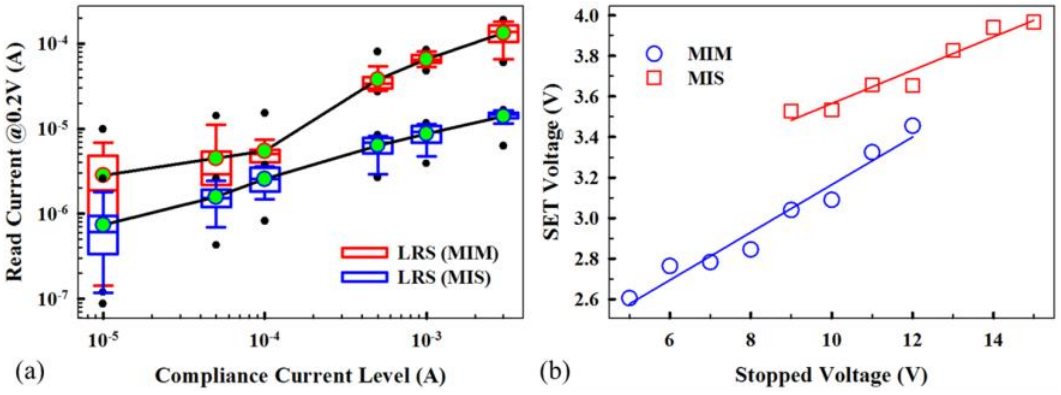

Figure 3.16. (a) LRS for MIM and MIS structures programed by controlling the CCL. (b) SET voltage versus RESET stopped voltage for MIM and MIS devices.

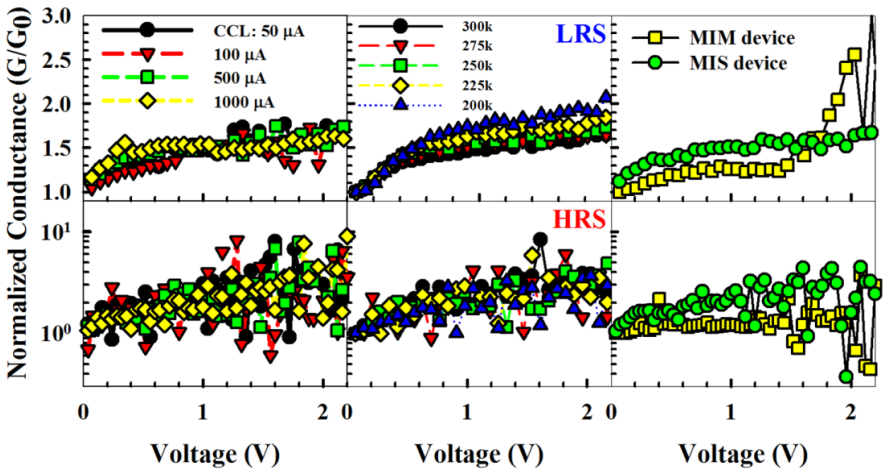

Figure 3.17. Normalized conductance of LRS/HRS as a function of CCL, ambient temperature, and MIM and MIS structure.

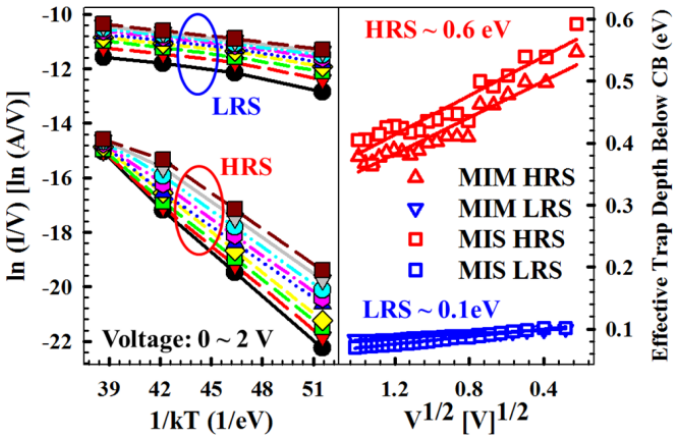

Figure 3.18. Poole-Frenkel emission analysis results in low voltage region and calculated energy barrier versus $V^{1/2}$ of LRS and HRS for MIM and MIS structures.

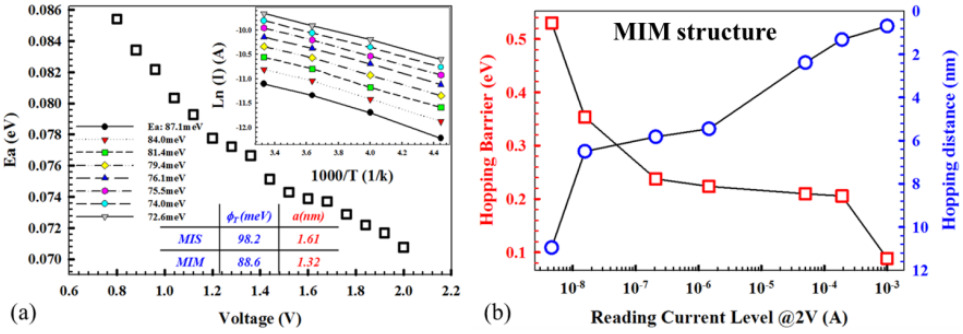

Figure 3.19. (a) Fixed-range hopping conduction of LRS in low voltage region for MIM and MIS structures. (b) Hopping barrier and hopping distance as a function of reading current level by CCL control.

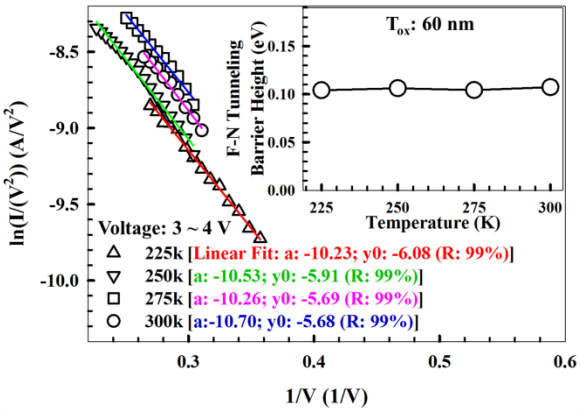

Figure 3.20. Fowler-Nordheim tunneling in MIS structure for the LRS in the moderate voltage region at 225 - 300 K.

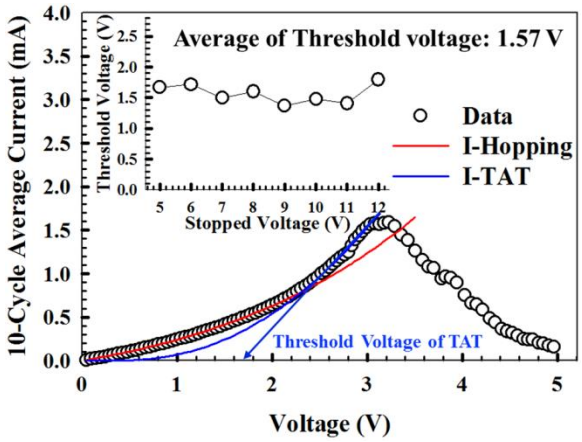

Figure 3.21. Linear I-V response for MIM device showing RESET voltage sweep. Data fits to hopping conduction and TAT are plotted, and the extrapolated TAT threshold voltage is labeled.

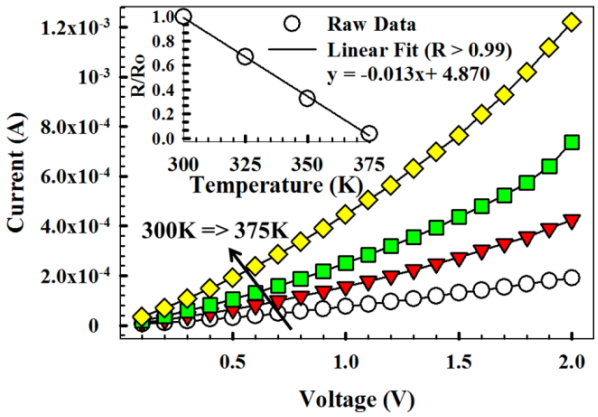

Figure 3.22. Measured *I -V* curves from 0 V to 2 V as a function of ambient temperature. Temperature coefficient was evaluated from the R - T plot in inset.

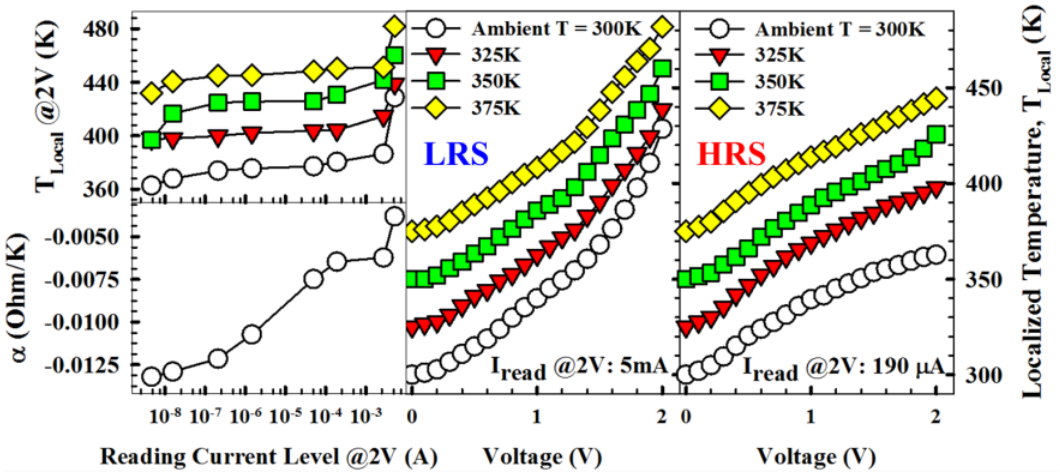

Figure 3.23. Extracted localized temperature and temperature coefficient for a series of ambient temperature ranges and intermediated states. Localized temperature versus voltage for LRS and HRS.

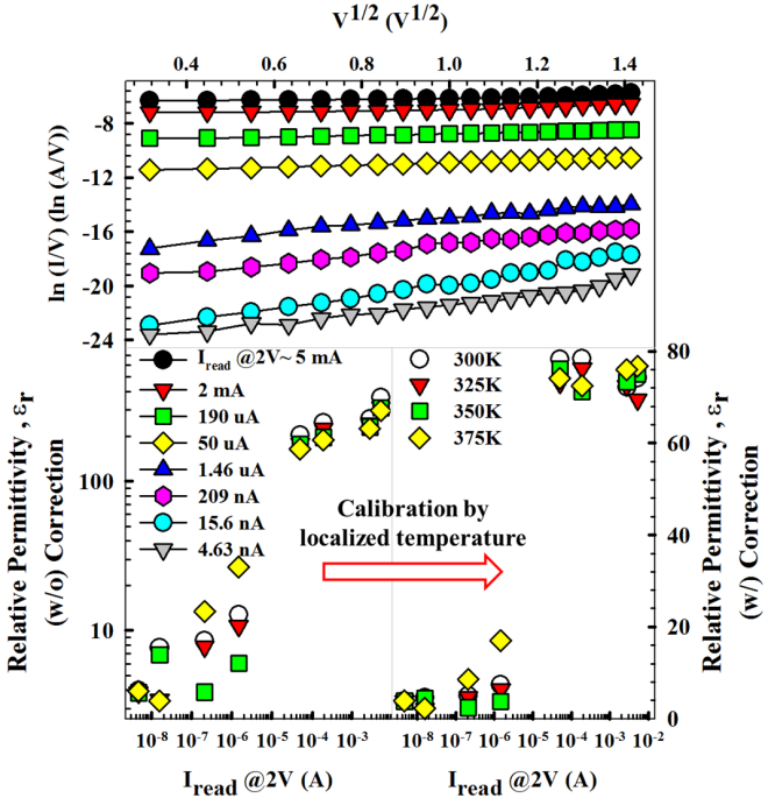

Figure 3.24. Relative permittivity extraction method and values as a function of ambient temperature range and intermediate states without and with localized temperature calibration.

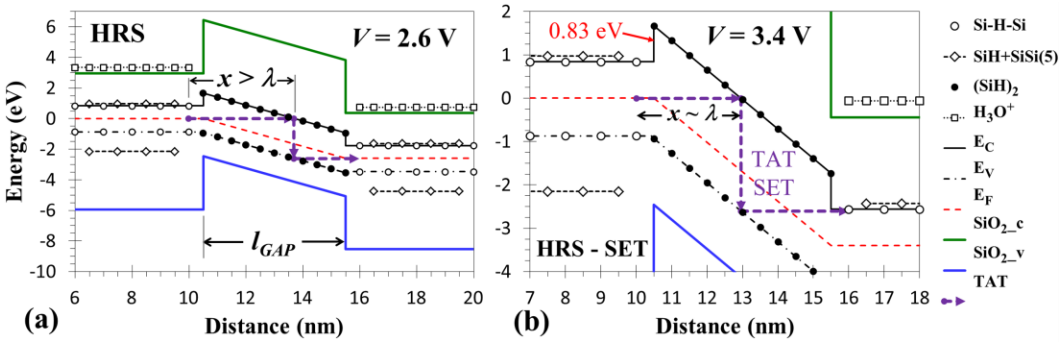

Figure 3.25. Energy band diagrams plotting electron potential energy versus distance along the conductive filament in the HRS.

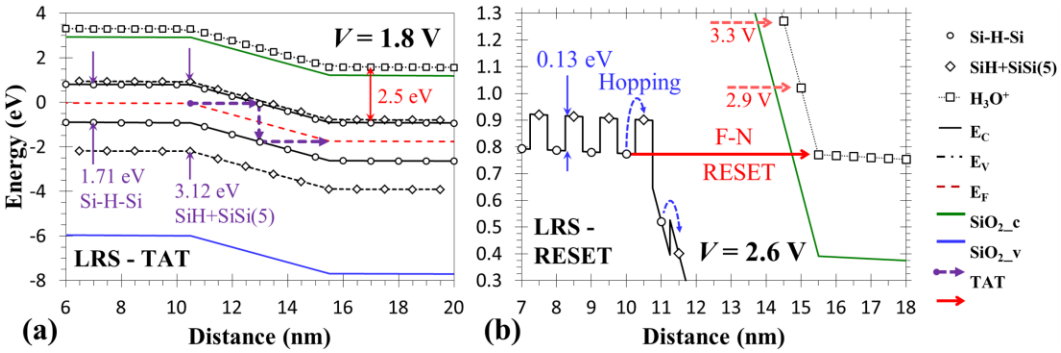

Figure 3.26. Energy band diagrams plotting electron potential energy versus distance along the conductive filament in the LRS.

Chapter 4: Integrated One Diode - One Resistor Architecture in Nano-Pillar SiO_x Resistive Switching Memory by Nano-Sphere Lithography

G. Wang *et al.* have reported an integrated Schottky diode-1R configuration that demonstrates high performance and low power in a 1k-bit array for potential circuit-level applications [53]. However, considering the static power consumption and sneak-path issues in large-scale, crossbar array designs [54-56], a Schottky-diode is not suitable for portable electronics due to its high reverse-bias leakage current and relatively low reverse-bias breakdown voltage as compare to a Si-based PN-diode or transistor [57-59]. For example, the reverse leakage current of Schottky diodes can increase dramatically with temperature to the point of a thermal-runaway situation [60], potentially resulting in instability issues and readout failures.

In this work, a Si diode (1D) with low reverse-bias current is integrated with a SiO_x-based memory element (1R) using nano-sphere lithography (NS lithography, or NSL) and deep-Si-etching (DES) to pattern a $P^{++}/N^{+}/N^{++}$ epitaxial Si wafer. The self-aligned process forms a high density, large-scale nano-pillar (NP) array architecture. Compared with conventional photolithography or direct-writing methods (such as electron beam lithography or focused ion beam milling), NSL has emerged as a low-cost (maskless), high-throughput alternative technique to pattern large areas [61-64]. The nanostructures fabricated using NSL can be well controlled in shape, size, and inter-pillar spacing through direct assembly of polymer nanospheres on the wafer-scale. Performance of 1R and 1D-1R structures are characterized and show that the integrated nano-pillar 1D-1R configuration offers low static-power for suppression of sneak-path issues [65].

The work reported here provides an efficient fabrication process and low reverse-bias current in a SiO_x-based 1D-1R configuration for potential use in future ultra-large-scale nonvolatile memory (NVM) applications.

4.1 SiO_X-BASED MEMORY ELEMENT (1R) FABRICATED BY NSL AND BASIC CHARACTERISTICS

Figure 4.1 illustrates the process flow for a 1R SiO_x-based ReRAM with sequential scanning electron microscope images (Zeiss Neon 40 SEM) of the evolving structures. The detailed procedure of 1R SiO_x-based ReRAM array fabrication begins with e-beam evaporation (PVD, CHA Industries) of 60 nm of SiO_x (measured by ellipsometer) on a N^{++} (100) Si substrate ($1\text{-}7\times10^{19}$ cm^{-3}, resistivity of 0.001-0.005 ohm-cm) used as a bottom electrode. The SiO_x acts as the 1R element and as a hardmask for self-aligned 1D nano-pillar fabrication (as describe further below). Next, the PVD-SiO_x layer is treated in an oxygen plasma reactor to obtain a hydrophilic surface. 18MΩ DI water and 200nm polystyrene nanosphere (Polysciences Inc.) were used for nanosphere mask preparation. 200nm nanosphere was chosen due to a trade-off between minimum feature size and larger-scale uniformity. Polystyrene nanosphere solution was dropped on top of microscope coverslips. This was then introduced to air-water interface in Petri dish filled with 18MΩ DI water. The polystyrene solution spread out at the air-water interface forming monolayer. Prior to monolayer formation, a prepared silicon substrate with SiO_x coating was immersed at the bottom of Petridish. The monolayer was then transferred to immersed substrate by slightly lifting the substrate. Then the sample was dried in air. The

diameter of each NS in the monolayer was reduced by reactive ion etching (Oxford 80 RIE) in oxygen-plasma (80 sccm O_2; power 60 W; pressure 100 mT; 1 minute). The power, partial pressure, and time of etching were optimized to obtain the desired size (Figure 4.1 (b)). The 1R array is formed by RIE (5 sccm Ar + 5 sccm O_2 + 80 sccm CF_4; Power 100 W; pressure: 200 mT) to transfer the treated NS pattern into the SiO_x layer (Figure 4.1 (c), with average diameter of about 150 nm). The NS layer was removed by bath sonication in water for 15 min. For 1D-1R structure, a $P^{++}/N^{+}/N^{++}$ epitaxial Si wafer is used as substrate (P^{++}: thickness 0.3 um, Boron (B), concentration 5×10^{19} cm^{-3}; N^{+}: thickness 0.6 um, Arsenic (As), concentration 5×10^{16} cm^{-3}; N^{++}: substrate, Phosphorus (P), concentration $1\text{-}7\times10^{19}$ cm^{-3}). Based on 1R array, nano-pillars are obtained via Bosch Deep Silicon Etch process (Versaline Deep Silicon Etch System, Plasma-Therm Inc.). A tungsten (W) probe tip (~10 um radius) was used as a top electrode, and a Lake Shore Cryotronics vacuum probe chamber (< 1 mTorr) and Agilent B1500A device analyzer were used for electrical test. *I-V* data were collected using AC pulse and forward/reverse DC sweeps: The SET process programs the device to a conductive, low-resistive state (LRS); The RESET process programs each device to a low-conductance, high-resistive state (HRS) having lower conductance as reset stop voltage is increased.

Figure 4.2 shows *I-V* characteristics of DC sweep and AC pulse response for SiO_x-based 1R array fabricated by NSL. Voltage was applied to the top electrode (W probe tip) with bottom electrode (N^{++} Si substrate) at ground. All testing was done in vacuum. To establish reversible switching in these devices, a two-step electroforming process was used: (1) a current-limited voltage sweep to induce soft breakdown; and (2) a

forward/backward voltage sweep to electroform the device. The soft-breakdown process is done by sweeping the voltage until current dramatically increases to a compliance current limit (CCL), typically 100 nA in this work. Generally, this process avoids hard breakdown and increases electroforming yield in most types of ReRAM devices. For the SiO_x-based ReRAM devices used here, a second electroforming step was done using a forward/backward voltage sweep (Figure 4.2 (a)), where current fluctuations are observed to increase to above the CCL during the forward voltage sweep. Electroforming is completed during the backward voltage sweep from the forming voltage (about 8 V - 18 V within 12 devices, inset of Figure 4.1 (b)) to 0 V, resulting in a LRS. After the electroformation, resistive switching performance is stabilized by cycling the device multiple times using voltage sweeps (Figure 4.2 (b)). The SET process is a 4 V forward/reverse sweep without any CCL to program the device to the LRS. The RESET process is done by sweeping the voltage to 8 V, where current decreases as the voltage is swept from about 5 V to 8 V; and the device is programmed into a HRS. The HRS/LRS resistance ratio is at least ~50 at 1 V reading, which satisfies sensing requirements. Figure 4.2 (c) demonstrates the AC pulse response for Set and Reset programming in the 50 ns regime where HRS and LRS resistance values are controlled by applied pulse height and pulse width, thus potentially enabling multilevel programming in a single memory cell. Figure 4.2 (d) shows HRS and LRS resistance values during 10^4 switching cycles. A resistance ratio of at least one order of magnitude is maintained, although soft-errors were observed during the first 100 cycles (inset of Figure 4.2 (d)). It may be noted that the electroforming voltages measured here (~ 12 V) are somewhat lower than those measured

in previous work on MOSCAP device architectures, and are near the voltage used in the RESET process (8 V). This could be due to creation of electrically active defects near the SiO_x sidewall during the RIE process that may lower the soft breakdown threshold and reduce the filament formation energy during the subsequent electroforming process. Also, the RESET voltage (i.e the voltage at which LRS current begins to decrease) is always greater than or equal to the SET voltage (where current increases sharply), which is a unique characteristic of SiO_x-based ReRAM as compared to other material systems. The difference between RESET and SET voltages can potentially be controlled by optimizing the series resistance in the circuit and choice of electrode materials.

4.2 1D-1R Architecture in Nano-Pillar SiO_X Resistive Switching Memory by Nano-Sphere Lithography

Figure 4.3 illustrates the 1D-1R NP fabrication process and shows SEM images of a NP array. Nano-pillars are formed and separated by the DSE process in Bosch mode (Versaline Deep Silicon Etch System, Plasma-Therm Inc.), which contains three steps: (1) Polymer deposition. (2) Polymer etching. (3) Si etching. The etch time and power in the Bosch process were optimized to reduce sidewall scalloping (Figure 4.3 (b)). Figure 4.3 (c) shows a 2-inch wafer used to demonstrate the 1D-1R fabrication process using an epitaxial 1D structure. Additional work is in progress to optimize the across-wafer uniformity of the NSL and DSE processes. The 1D-1R nano-pillar SiO_x ReRAM architecture was imaged using SEM (Figure 4.3 (d) – (f)). The average nano-pillar height and diameter are 1.3 μm and 130 nm, respectively.

Figure 4.4 (a) shows the I-V response of 100 voltage sweeps from -3 V to +3 V for a NP 1D configuration. The forward current can reach 100 mA at 3 V, which indicates a forward current level high enough to support the Reset process. The reverse current is below 1×10^{-12} A at -3 V. As mentioned previously, compared with schottky diodes, the advantages of Si-based PN diode are low reverse-current, high reverse-bias breakdown voltage, and fewer stability issues. The reverse current level is reduced by at least three-orders of magnitude compared with a previous report while maintaining good reliability. The simulation fitting results indicate that the defect concentration is about 1×10^{-15} cm^{-3} (using a simple assumption of mid-gap traps), which is expected due to the epitaxial quality of each layer. The quality of 1D stacked layers (epitaxy, diffusion or implantation) can dramatically affect diode reverse or forward current characteristics, as well as power consumption and readout margin issues (describe below). Also, the chosen $P^{++}/N^{+}/N^{++}$ configuration has high reverse breakdown voltage (> 30 V), which is important for SiO_x-based ReRAM operation. The concentration of each epitaxial layer strongly affects diode I-V characteristics due to the carrier injection characteristics, whereas NP height and diameter have minor effects. Figure 4.4 (b) shows *I-V* curves of 30 switching cycles for a SiO_x-based 1D-1R NP structure. The required forming voltage is similar to the 1R structure. However, the switching voltage values for Set and Reset processes in 1D-1R are larger than in 1R, and the current transition at the switching point is more gradual, possibly due to the series connection of 1D and 1R elements. By controlling the reset stop voltage, the HRS level can be controlled and the potential for multi-bit operation can be demonstrated for NP SiO_x-based ReRAM (inset of Figure 4.4 (b)). Compared to our previous studies, the HRS current here is significantly larger than in simple MOS (TaN-SiO_x-N^{++} Si wafer) structures, possibly due to plasma-etching-induced defect formation on resistive switching transformation. Plasma etching process

(RIE or DSE) can result in a more defective insulator causing increased leakage current in the 1R element. It should be emphasized that a W probe tip is used as the top electrode for the 1D-1R structures. As a result, the probe tip contacts ~ 7800 nano-pillars based on the deposited NS pitch (200 nm) and probe tip radius of 10 μm. Since we expect that only a single filament is activated during the electroforming process, the large HRS current is possibly due to the multiple parallel leakage paths in the NP array. Additional investigations by controlling RIE process, the oxygen content of SiO_x, and measuring an individual NP 1D-1R structure are ongoing and will be described in future reports. Changing the oxygen-content of the 1R element by controlling oxygen flow during sputtered deposition of the SiO_x layer can possibly enlarge the HRS/LRS ratio and stabilize switching characteristics. Figure 4.4 (c) shows multilevel retention performance of SiO_x-based 1D-1R NP arrays obtained by controlling the stop reset voltage from 8 V to 15 V. The readout current of LRS and HRS is measured at 1 V for every 60 second after each Set and Reset programming operation. The retention reliability test shows stable multilevel operation, and no degradation is observed for more than 10^4 sec, confirming the nonvolatile nature of the SiO_x-based 1D-1R NP devices. For circuit-level applications, low reverse current, larger HRS/LRS resistance ratio, and low readout current are desirable for large-scale ReRAM production. Low reverse-current can reduce the sneak-path leakage issue and provide larger readout margin, especially in large arrays. Large HRS/LRS ratio provides the potential for multi-bit operation with a small-footprint cell ($< 4F^2$) and reduces the chance for soft-errors. Nonlinear current response (ex. one selector and one resistor configuration, 1S-1R) is preferred for low-power applications. In our case, a 10% readout-margin can support a 1Gbit array due to the low reverse-biased diode current and large LRS/reverse-current ratio (Figure 4.4 (d)). The results

demonstrate here provide significant benefits by simplifying the ReRAM fabrication process and potentially enabling compatibility with high-volume CMOS manufacturing.

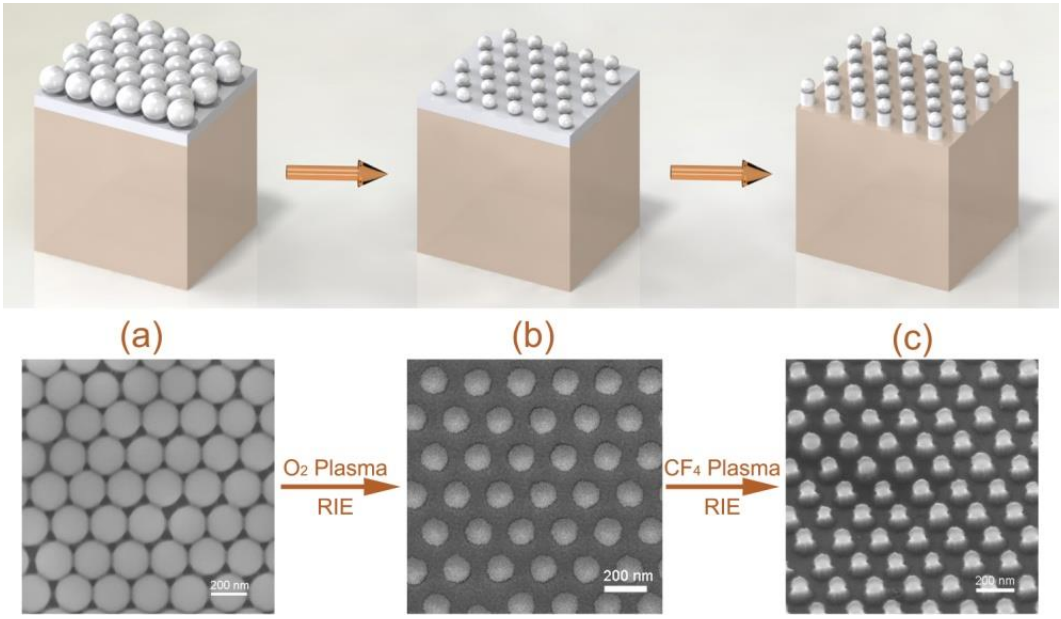

Figure 4.1 1R process flow using nano-sphere (NS) lithography.

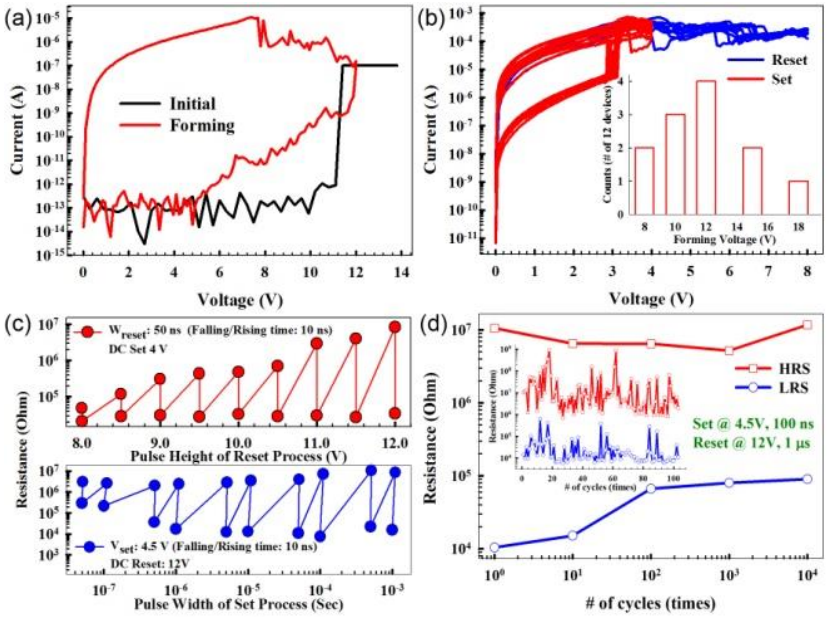

Figure 4.2 DC sweep resistive switching behaviors and AC pulsed response of 1R element.

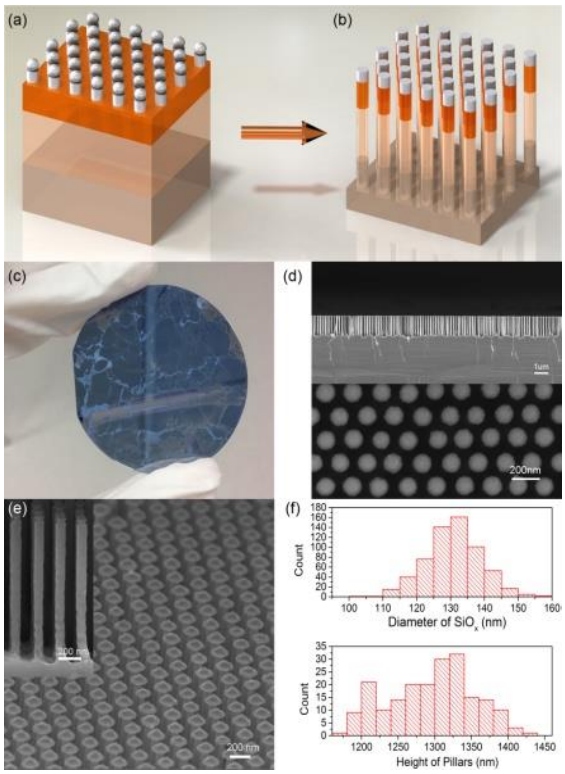

Figure 4.3 1D-1R fabrication procedure using DSE.

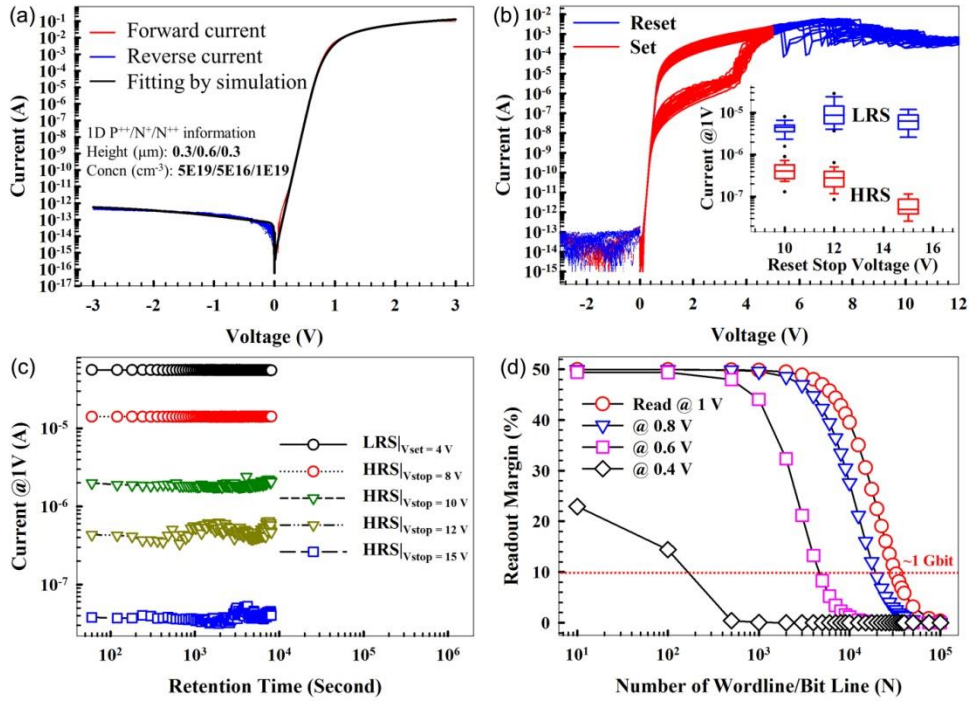

Figure 4.4 1D-1R electrical characteristics when using NSL and DSE.

Chapter 5: A Synaptic Device Built in 1D-1R Architecture with Intrinsic SiO_x-based ReRAM

Neuro-electronics and synaptic electronics are interesting applications for ReRAM that aim to build artificial synaptic devices that emulate the computations performed by biological synapses [66-70]. These emerging fields of research potentially have better efficiency in solving complex problems and outperform real-time processing of unstructured data than conventional von Neumann computational systems [71]. There have been many studies of binary metal oxide-based and perovskite oxide-based resistance switching characteristics for synapse-like electronic device development [72, 73], which can have operating instability issues due to difficulty in controlling stoichiometric compositions [74. 75]. Therefore, a simple process that is compatible with conventional complementary metal-oxide semiconductor (CMOS) fabrication allows multi-layer compositional engineering and provides good electrical stability and high yield, which are critical requirements for neuro-electronics realization [76]. Several recent reports describe using SiO_2 as the active switching medium in resistive switching memory devices [77-80]. We have further demonstrated a Si diode (1D) with low reverse-bias current integrated with a SiO_x-based memory element (1R) using nano-sphere lithography and deep Si etching to pattern a $P^{++}/N^{+}/N^{++}$ epitaxial Si wafer [65]. The above achievements for intrinsic SiO_x-based ReRAM indicate: 1) High device yield, forming-free operation, reduced operating voltage, excellent scalability (to dimensions < 40 nm in 1D-1R architectures without scarifying the device performance, such as the retention of multilevel states and endurance reliability) and good device stability; 2)

Pulsed programming in the 50 ns-regime and low reverse current with large rectification ratio to meet low-energy consumption criteria (> 10^6 for high-conductance states) for integrated 1D-1R nano-pillar architectures; and 3) wide programming resistance dynamic range (potentially up to 10^8), multi-level states, and excellent reliability. However, the resistive switching mechanisms in SiO_x are not well understood and use as an electronic synaptic device has not previously been demonstrated.

In this work, SiO_x-based resistive switching memory elements (1R) are integrated with Si diodes (1D) using conventional CMOS processing to demonstrate a 1D-1R device with synaptic behaviors. The Si diode provides low reverse-bias current and high power efficiency for future neuromorphic computing array architectures. Unlike other binary or complex metal oxide materials [81-84], SiO_x has been used in CMOS manufacturing for over 50 years due to its excellent electrical isolation properties, low-cost, high chemical stability, compatibility with mainstream integrated circuit materials, high-throughput processing and large-area production using chemical vapor deposition (CVD). A 1D-1R architecture fabricated at the wafer-scale using conventional CMOS processing can therefore be well-controlled in thickness, size, and electrical characteristics by precisely controlling the doping levels of the diode layers and the temperature and flow-rate of the oxide CVD process [85]. Synaptic device performance is characterized in a prototype 1D-1R array configuration. Robust biological synaptic behaviors such as long-term potentiation (LTP), long-term depression (LTD) and spike-timing dependent plasticity (STDP) are demonstrated with excellent uniformity, low operational variability and good suppression of static power consumption [81-84]. A bio-inspired proton exchange

resistive switching model is used to help characterize this novel application for SiO_x materials. The SET transition in the resistive switching memory is modeled as hydrogen (proton) release from the $(Si\text{-}H)_2$ defect to generate a conductive hydrogen bridge, and the RESET transition is modeled as an electrochemical reaction (proton capture) that re-forms non-conductive $(SiH)_2$. The synaptic behaviors exhibited by the 1D-1R device demonstrates good potential for using a simple and robust approach for large-scale integration of programmable neuromorphic chips using CMOS technology.

5.1 1D-1R Architecture Fabricated by Standard CMOS Process

Devices were fabricated at XFAB Inc. in Lubbock, TX. Secondary electron microscopy (SEM) images show a top-down view of a 1D-1R test structure (Figure 5.1 (a)), a tilted (45^o) view of the 1R device (Figure 5.1 (b)) and a cross-section image of the 1R device showing layer information (Figure 5.1 (c)). The 1R device was fabricated by implanting the Si substrate to form an n-type lower electrode. The active SiO_x memory layer was then deposited to a thickness of 40 nm using plasma-enhanced chemical vapor deposition (PECVD). This thickness is known to provide high electroforming yield and good memory endurance. An n-type polysilicon layer was deposited onto the SiO_x layer to form the top electrode. An opening in the polysilicon layer was made after all thermal oxidation and implant anneal steps are complete (Figure 5.1 (b)). A first dielectric layer was then deposited over the polysilicon top electrode. Tungsten plugs were used to make electrical contact to the n-type Si lower electrode and the polysilicon top electrode. After all the back-end dielectrics and a passivation layer were deposited, the back-end

dielectric layers were removed using reactive ion etch (RIE) to the Si substrate. This RIE step cleared-out the SiO_x layer inside the hole, and created a SiO_x sidewall where the memory device is formed (Figure 5.1 (c)). Polymer residue that remained after the post-RIE cleaning steps was removed by a 30-second buffered oxide etch (BOE). The pn diode used in the 1D-1R test structures was formed by an implanted p-well inside a deep n-well, and is a standard device available in the XFAB XC06 process with 40 V reverse-bias breakdown voltage, 1 nA reverse-bias leakage current and 0.5 V forward voltage. The active memory area of the 1R device is $2\times2\ \mu m^2$ and the overall size including metal interconnects is $21.9\times21.9\ \mu m^2$. The overall size of the 1D device is $41\times19\ \mu m^2$. A Lake Shore Cryotronics vacuum probe chamber (< 1 mTorr) and Agilent B1500A device analyzer were used to electroform devices and measure the DC/AC *I-V* response. The SET process programs the device to a conductive, low-resistance state (LRS). The RESET process programs each device to a low-conductance, high-resistance state (HRS). A Kratos Axis Ultra HSA X-ray Photoelectron Spectrometer (XPS) equipped with a monochromatized aluminum x-ray source was used to analyze several SiO_x materials deposited in our laboratory using different methods. Calibration of the binding energy scale was set by fixing the C-(C,H) peak at 284.4 eV. Figure 5.1 (d) shows XPS analysis results for the O-1s and Si-2p binding energies in thermal oxide grown by low-pressure chemical vapor deposition (LPCVD) and PECVD oxide. The existence of stoichiometric SiO_2 can be observed in thermal oxide (binding energy Si: 103.2 eV; O: 532.5 eV) with essentially no sub-oxide bonding being detected. In contrast, the PECVD oxide has non-stoichiometric SiO_x (x is about 1.6 based on the peak position and orbital valence)

composition in the switching layer, as indicated by the peak binding energies in the XPS spectra (Si: 530.5 eV; O: 101.9 eV and 100.9 eV) [86-88], which may promote low-energy defect generation during the electroforming process.

5.2 Basic Resistive Switching Behaviors in 1D-1R Architecture

Figure 5.2 (a)-(d) shows *I-V* characteristics for DC voltage sweeps applied to the SiO_x-based 1D-1R devices fabricated by the conventional CMOS process. Voltage was applied to the 1D top electrode (p-type Si) with bottom 1R electrode (n-type Si) at ground. All testing was done in vacuum. To establish reversible resistive switching in each SiO_x-based 1R ReRAM device, a forward/backward voltage sweep (Figure 5.2 (a)) was used to electroform a conductive filament, where current is observed to increase dramatically at 22.5 +/- 2.9 V during the forward voltage sweep. Electroforming is completed during the backward voltage sweep from the maximum sweeping voltage to 0 V, resulting in a LRS. After electroformation, resistive switching performance of 1D-1R is stabilized by cycling the device multiple times using voltage sweeps (Figure 5.2 (b)). The SET process is a 10 V forward/backward sweep without any compliance current limit (CCL) to program the device to the LRS. The RESET process is done by sweeping the voltage to 17 V, where current decreases as the voltage is swept from about 10 V to 17 V; and the device is programmed into a HRS. The HRS/LRS resistance ratio is at least ~10^3 at 1 V bias, which satisfies sensing requirements [89]. For diode characteristics, the forward current can reach 100 mA at 2 V, which indicates a forward current level high enough to support the RESET process. The reverse current is below 1×10^{-12} A at -5 V. Compared with

Schottky diodes, the advantages of Si-based PN diodes include low reverse-current, high reverse-bias breakdown voltage, and fewer stability issues. The quality of the Si-based PN diode can dramatically affect diode reverse or forward current characteristics, as well as power consumption (describe below). Also, the chosen Si-based PN diode configuration has high reverse breakdown voltage (> 40 V), which is important for SiO_x-based ReRAM operating in an array. Figure 5.2 (c) and (d) demonstrate the gradual change of resistive states by modulating the voltage sweep range during the SET and RESET process, respectively. Specifically, SET and RESET voltages were changed from 3.5 V to 9.5 V in 0.5 V increments and from 11 V to 18 V in 0.5 V decrements, respectively, thus potentially enabling multilevel programming in a single memory cell. It may be noted that the electroforming voltages measured here (~ 28 V) are somewhat higher than those measured in previous work on metal-oxide-semiconductor device architectures or nano-pillar type 1D-1R atchitectures, which may be due to fewer electrically-active defects being near the SiO_x sidewall as a result of the fabrication process. For example, several high temperature steps (> 650 °C) were done after PECVD SiO_2 deposition, namely: polysilicon deposition, thermal oxidation, and implant anneals, which might densify the SiO_2 layer, reduce the as-deposited defect levels, increase the soft breakdown threshold, and thus increase the filament formation energy during the subsequent electroforming process. Interestingly, the RESET voltage (the voltage at which LRS current begins to decrease) has been found to be greater than or equal to the SET voltage (where HRS current increases sharply), which is a unique characteristic of the SiO_x-based ReRAM as compared to other materials systems [90]. The difference

between RESET and SET voltages can potentially be controlled by optimizing the series resistance in the circuit and choice of electrode materials [91]. The switching voltage is largely independent of device size and SiO_x thickness. Figure 5.2 (e) shows multilevel retention performance of SiO_x-based 1D-1R devices obtained by controlling the maximum SET voltage from 3 V to 9 V. The readout current of LRS and HRS is measured at 1 V every 60 seconds after each programming operation. The retention reliability test demonstrates multilevel operation by using different SET voltages, and no degradation is observed for more than 10^3 sec, thus confirming the stable, nonvolatile nature of the SiO_x-based 1D-1R devices. In recent studies, a possible proton-exchange model consistent with the observed resistive switching *I-V* response has been proposed, as shown in Figure 5.2 (f) [91, 92]. Several studies have used transmission electron microscopy (TEM) to document the presence of Si nanocrystals within the CF [93, 94], but it is not yet clear whether resistive switching (RS) is the result of an overall increase in nanocrystal size or whether switching occurs in "GAP" regions in between nanocrystals. Most models of ReRAM switching involve the drift or diffusion of O^{2-} ions (or oxygen vacancy defects), but these models cannot explain the *I-V* response (such as the backward scan effect, as shown in Figure 5.2 (a)) or the ambient effects on resistive switching observed in the SiO_x device [95, 96]. The models used to describe the possible SiO_x-based RS mechanisms differ from most conventional models by considering that the defects responsible for RS may remain localized within the switching region so that resistive switching occurs when a collection of defects are driven between conductive and non-conductive forms [96]. A thorough review of the reported electrical and structural

properties of known SiO_x defects [91] has identified possible proton exchange reactions that can dramatically alter the conductivity of specific defects, leading to a model where the LRS has a large concentration of conductive defects within the switching region, and, conversely, when the device is programmed to the HRS, most of the defects are converted to their non-conductive form. The electrically-conductive hydrogen bridge (Si-H-Si) is viewed as the most likely defect responsible for the LRS due to the location of its energy levels relative to the oxide conduction band and its small effective bandgap energy [91, 92]. Adding a proton to Si-H-Si forms the non-conductive $(SiH)_2$ defect and proton desorption from $(SiH)_2$ re-forms Si-H-Si, which are well-understood electrochemical reactions that could enable localized switching without incorporating ion diffusion or drift mechanisms into the model. The SET transition voltage from HRS to LRS occurs at ~ 2.5 V in the I-V response, and is very near the activation energy for proton desorption from SiH (~ 2.5 eV), thus making the defect transformation from $(SiH)_2$ to Si-H-Si a logical assignment for the SET transition [91, 92]. In this model, the proton that is lost from $(SiH)_2$ reacts electrochemically with $(SiOH)_2$, which is simply chemisorbed H_2O, to form the fixed positive charged H_3O^+ defect. The transition from LRS to HRS is modeled as being initiated by electron injection into H_3O^+ that induces proton release and electrochemical reaction with Si-H-Si to re-form $(SiH)_2$. The localized proton exchange switching model can thus be written as $(SiH)_2 + (SiOH)_2 \leftrightarrow$ Si-H-Si + H_3O^+, where a voltage drop of ~ 2.5 V across the switching is required to drive the reversible reaction. The RS model not only provides insights into multilevel operational characteristics but also implies a possible biomimetic chemical reaction similar to

reactive oxygen species (ROS–like) production for future device characterizations [97-99].

5.3 Pulse Mapping and Long-Term Potentiation (LTP) and Long-Term Depression (LTD) Synaptic Behaviors

Figure 5.3 (a) - (h) show contour plots of the current-change ratio achieved by modulating the AC pulse height and pulse width applied to 1D-1R devices for both SET and RESET switching events, leading to optimized waveform designs for a biological synaptic device. The current-change ratio is defined as $\log_{10}$ ($I_{FINAL}/I_{INITIAL}$), where $I_{INITIAL}$ and I_{FINAL} are the currents measured at 1 V before and after applying the programing waveform, respectively. The SET switching events (S) increase current through the device, leading to positive current change ratios, whereas RESET switching events (R) decrease device current and lead to negative current change ratios. The pulse mappings are generated using the Agilent B1500A device analyzer in a three-step process: (1) Initial states are programmed using a fixed DC voltage before the pulse waveform is applied; (2) The pulse waveform is applied; and (3) Device state is read by measuring the current at 1 V before and after each pulsed switching event. One can observe by inspecting the contour lines in Figure 5.3 that when larger pulse heights (higher voltages) are applied to the device, shorter pulse widths are needed to achieve a similar current-change ratio. In general, we find that a single 1R device operates at higher speed and requires lower programming voltages as compared to a 1D-1R device [100]. The higher operating voltages and lower operating speed of the integrated 1D-1R device

may result from higher parasitic resistance in the Si electrodes, their contacts and the diode, as well as higher parasitic capacitance in the diode, all of which can act to degrade the pulse mapping results shown in Figure 5.3 (a) and (b). It should be noted that current sneak-path issues in arrays of 1R devices would cause misread problems and substantially increase standby power consumption. The 1D-1R devices are used to suppress sneak-path currents, and perform much better than 1R devices in an array architecture. From Figure 5.3 (a) and (b), it can be calculated that the switching energies to achieve at least a one-order-of-magnitude change in resistance in the 1D-1R architecture are about 0.01 pJ for SET and 1.54 nJ for RESET operations. However, due to the suppression of sneak-path current, the standby power during a 1 V read operation can be dramatically reduced in 1D-1R devices (1 pW) as compared to 1R devices (1 μW). Minimizing the total power consumption due to sneak-path current is as crucial as reducing the synaptic dissipation.

Most importantly, the pulse mapping results not only demonstrate the potential for multilevel programming by properly designing the pulse waveforms for SET and RESET operations, but also demonstrate the potential to realize biological synaptic behaviors. Figure 5.3 (c) – (h) demonstrate the optimization waveform design for biological synaptic behaviors in 1D-1R SiO_x-based resistive switching memories. The long-term potentiation (LTP)/long-term depression (LTD) are a long-lasting enhancement/reduction in signal transmission between two neurons, which can be realized by designing the SET and RESET pulse waveform to use either identical (fixed pulse width and pulse height, as shown in Figure 5.3 (c) – (f)) or non-identical (variable pulse width or pulse height, as

shown in Figure 5.3 (g) and (h)) pulsing methods. Both methods can be used to demonstrate a SiO_x-based synaptic device. It may be noted that when the dynamic range was evaluated in detail and the trade-offs between high dynamic range and gradual multilevel programming performance (Figure 5.3 (e) – (h)) were considered, it was found that non-identical pulse waveform methods may have certain advantages. (Dynamic range is defined as the maximum achievable resistance of the HRS divided by the minimum resistance of the LRS.) Although non-identical pulsing might require a more complex neuromorphic circuit, our results show that this approach enables more efficient programming to target states while maintaining a larger dynamic range (Figure 5.3 (g) – (h)). The use of non-identical pulse heights ranging from 4 V to 10 V in 0.3 V increments (for LTP) and ranging from 11 V to 17 V in 0.3 V decrements (for LTD) allow the dynamic range to be mapped for pulse widths ranging from 100 ns to 1 ms, thereby realizing biological synapse behaviors in the SiO_x-based 1D-1R architecture (Figure 5.3 (g) – (h)). The switching energy is defined as $I \times V \times \delta t$, where δt is the pulse width. For δt = 100 ns, the smallest switching energies are ~6 fJ and ~130 pJ for LTP and LTD, respectively. The larger energy for LTD is mainly due to the lower resistance of the LRS (~ 93 kΩ) compared to the HRS (~ 260 MΩ), which results in higher switching current (118.28 μA) for the RESET process than for the SET process (15.38 nA). In order to minimize synaptic energy consumption all three components—programming current (~nA level switching), pulse amplitude (< 1 V) and programming time (< 10 ns)—need to be minimized. In SiO_x-based ReRAM and in other material systems, an exponential voltage–time relationship is commonly observed [101, 102]. A small increase in

programming voltage will decrease programming time exponentially. Hence, low programming energy is obtained by minimizing the programming time (traded off by increasing the pulse amplitude slightly) for ReRAM. Further decreases in synaptic energy consumption during the switching process to fJ levels will be challenging but important to build very large-scale systems.

5.4 Spike-Timing-Dependent Plasticity (STDP) in the SiO_x-based 1D-1R architecture

Such flexible artificial control built with synaptic devices could provide a suitable platform for a broad range of computing applications, as shown Figure 5.4. Some of the advantages that SiO_x-based synaptic devices provide over other resistive switching materials include a higher dynamic range ($\sim 10^4$) and the potential to achieve as many as 60 multi-level states in both LTP and LTD by changing the increment/decrement of the voltage step, as shown in Figure 5.4 (a). These advantages may arise as the result of there being a large number of defects within the switching region of the memory device. Switching is modeled as a change in conductivity of a group of defects within the switching region. In this framework, defects are not created or destroyed, but are simply driven between conductive and non-conductive forms by proton exchange reactions that are known to occur in SiO_x materials (Figure 5.2 (f)) [92, 103]. The SET and RESET switching transitions can be described in more detail with the aid of the electron energy band diagrams shown in Figure 5.4 (b), which were constructed using the thermodynamic and switching charge-state energy levels reported by Peter Blochl in 2000 [104]. The

ideal energy band diagrams in Figure 5.4 (b) represent only a single electron pathway through the memory device, whereas in reality there are likely many such percolation pathways in parallel. The SET transition is modeled as being the result of trap-assisted electron tunneling through $(SiH)_2$ defects that stimulates H desorption and reaction of H^+ with absorbed water $(SiOH)_2$ to form conductive Si-H-Si and H_3O^+ (Figure 5.2 (f)). Trap-assisted tunneling can only occur when the bias across the switching region is $\geq$ 2.6 V, which is the effective band gap of the $(SiH)_2$ defect and compares well with the observed minimum SET voltage of ~ 2.5 V in the *I-V* response [91, 92]. The RESET transition is modeled as being the result of Fowler-Nordheim electron tunneling into the H_3O^+ defect to stimulate proton release and electrochemical reactions that re-form $(SiH)_2$ and $(SiOH)_2$ (Figure 5.2 (f)). The band diagrams shown in Figure 5.4 (b) are found to be consistent with measured electron energy barriers and electroluminescence results reported for similar devices [92, 94].

Figure 5.4 (c) – (f) demonstrates spike-timing-dependent plasticity (STDP) in the SiO_x-based 1D-1R architecture, which is a biological process that adjusts the strength of connections between two neurons in a synapse gap junction region that is an electrically conductive link between the pre- and post-synaptic neurons. Two pulse generator sources are built to simulate the pre- and post-synaptic neurons, which provide the pulse waveforms using the non-identical pulse method for demonstration of spike-timing-dependent plasticity (STDP). By design of pre-neuron and post-neuron spikes in neuromorphic circuits, the strength of the conductance change can be modulated based on the delta spike timing (Δt) between the two neurons (Figure 5.4 (c) – (d)). Figure 5.4 (e) –

(f) demonstrates a total of 10 different states of STDP biological behavior for depression and potentiation with n = 2, 4, 6, 8, 10 and as a function of spike width modulation, ranging from 100 ns to 1 ms. For example, the depression of conductance change strength can be achieved by using multi-step spike heights from -4 V to 0 V in the pre-neuron state and a single spike height fixed at 13 V in the post-neuron state, with both neurons having a fixed pulse width of 10 μs and a firing period of 20 μs, as shown in Figure 5.4 (e) – (f). When the time delay difference is -10 × (n-1) μs, where n is an even number, the total spike waveform (post-neuron spike minus pre-neuron spike) applied to the synapse gap junction region can adjust the conductance ratio between two neurons over the range from 10^{-3} to 0.1 in the depression direction (RESET process) as compared with the initial LRS conductance (Figure 5.4 (f)). Similarly, the potentiation of conductance change strength can be achieved by using multi-step spike heights from 4 V to 8 V in the pre-neuron state and a single spike height also fixed at 13 V in the post-neuron state, with both neurons having a fixed pulse width of 10 μs and a firing period of 20 μs. When the time delay difference is 10 × (n-1) μs, where n is an even number, the total spike waveform (post-neuron spike minus pre-neuron spike) applied to the synapse gap junction region can in this case adjust the conductance ratio between neurons over the range from 10^{3} to 0.01 in the potentiation direction (SET process) as compared with the initial HRS conductance (Figure 5.4 (e)). It may be noted that the 1D-1R architecture not only avoids sneak-path issues and lowers standby power consumption, but also helps to realize STDP behaviors. Without the 1D rectification characteristics in reverse-bias polarity, the above spiking forms cannot be implemented due to the unipolar nature of the

1R device, specifically in the potentiation behaviors under negative bias. In the 1R case, an applied voltage above the RESET threshold voltage (for example, -9 V) can trigger the RESET process and induce depression behaviors instead of potentiation behaviors. Also, for depression behaviors, when the time delay difference is smaller than the spiking width, the remaining 4 V spike height in this case would not fire the synapse towards a LRS in the depression direction (see Figure 5.3 (h)). Therefore, by carefully designing the firing pulses between neurons in the neuromorphic circuit, a biological synapse behavior can be demonstrated with 1D-1R SiO_x-based resistive switching memories.

Figure 5.5 shows robust electrical reliability and low variation in a 1D-1R-array structure that can potentially be used in future neuromorphic computing applications. Figure 5.5 (a) shows a portion of a test chip containing a 16x16 bit cell array. Each bit cell is comprised of a Si PN diode isolation element and a SiO_2-based resistive memory element. Electroforming yield of the 256 bit cells in the array was 98%. Of these yielding devices, 100% passed a quick, 10-cycle switching performance test without failure. Figure 5.5 (b) shows the average and ± 3-sigma variation of resistive switching behaviors in the 16x16 bit cell array cycled using a 10 V double-sweep for SET and 20 V single-sweep for RESET. In this case, the 3-sigma LRS/HRS current ratio at 1 V read bias, was at least 6×10^3. A gradual change in the SET transition is observed over the voltage range from 3.5 V to 6 V, thus allowing programming of the multilevel states that are required for a robust neuromorphic circuit design, and which are accompanied by excellent sub-µs transitions with at least 10X resistance ratio after 10^5 cycles (Figure 5.5 (c)). A 2×2 array of integrated 1D-1R bit cells with unipolar programming strategy shows excellent write/read disturbance immunity after 10^6 pulses for unselected devices and a clear

programming window > 100 (Figure 5.5 (d)). In addition to 1D-1R device arrays, the hybrid CMOS/synaptic device architecture shown in Figure 5.5 (e) has been successfully demonstrated as shown in Figure 5.5 (f) by the *I-V* resistive switching plots. The 1D-1R architecture with SiO_x-based resistance switching devices and the structure of artificial neural networks map naturally onto hybrid CMOS/synapse circuits that can be designed on a single chip to provide predictable results with an ultimate scaling potential of CMOS technology to the sub-10-nm level, which could possibly challenge the complexity and connectivity of the human brain.

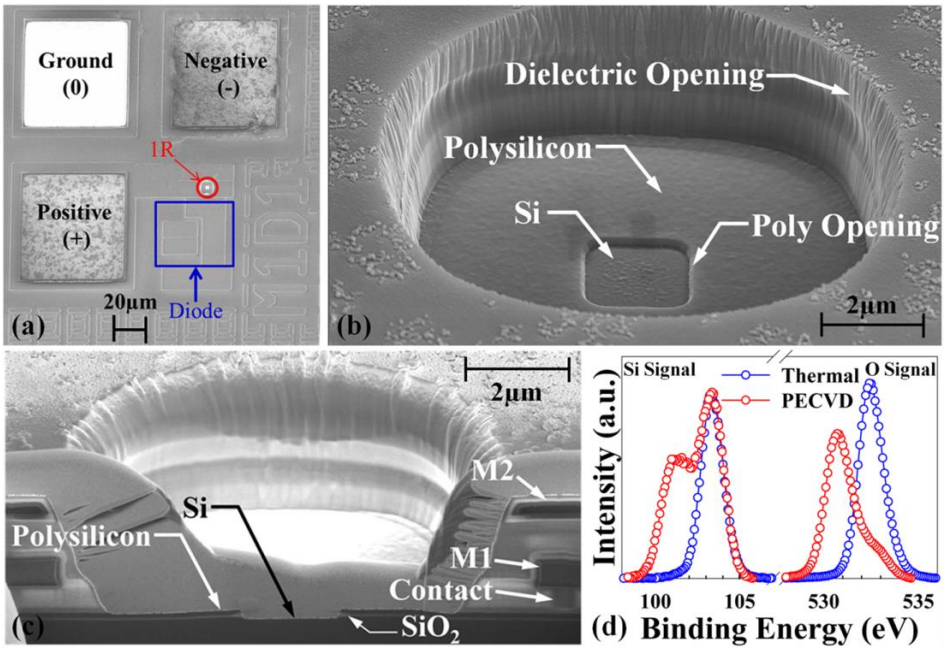

Figure 5.1. SEM images of 1D-1R architecture, and Si-$2p_{2/3}$ and O-1s XPS spectra for PECVD oxide and thermal oxide.

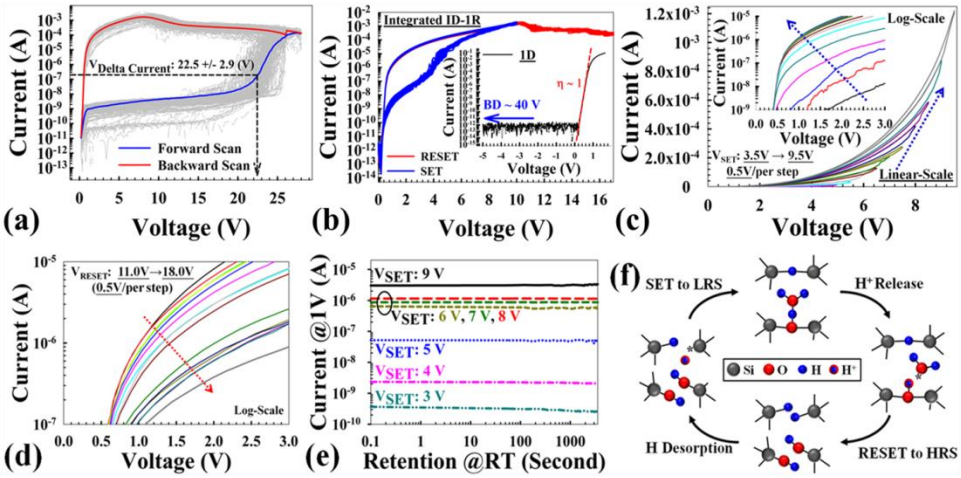

Figure 5.2. DC sweep resistive switching behaviors of 1D-1R architecture.

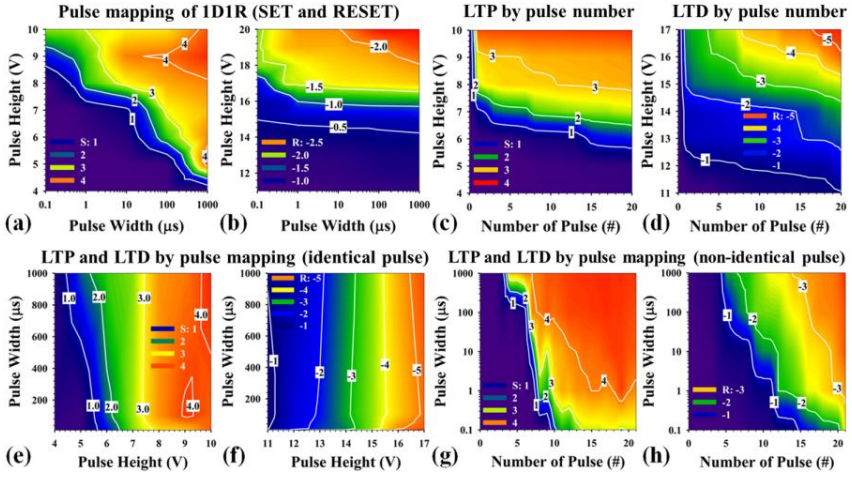

Figure 5.3. AC pulse mapping plots of current-change ratio by modulating pulse height and pulse width to demonstrate synaptic behaviors.

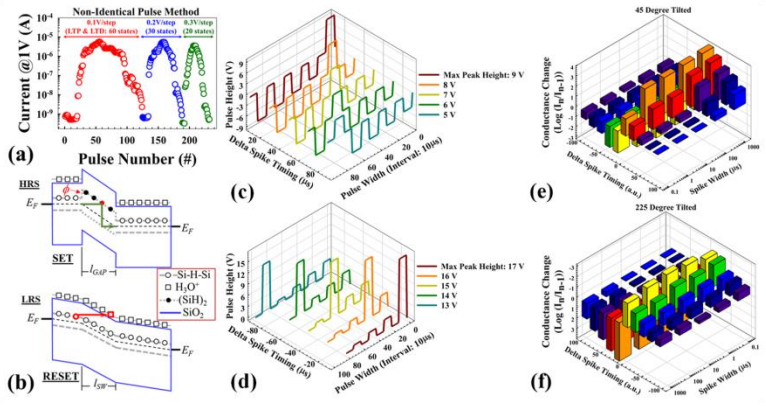

Figure 5.4. Demonstration of a SiO_x–based synaptic device.

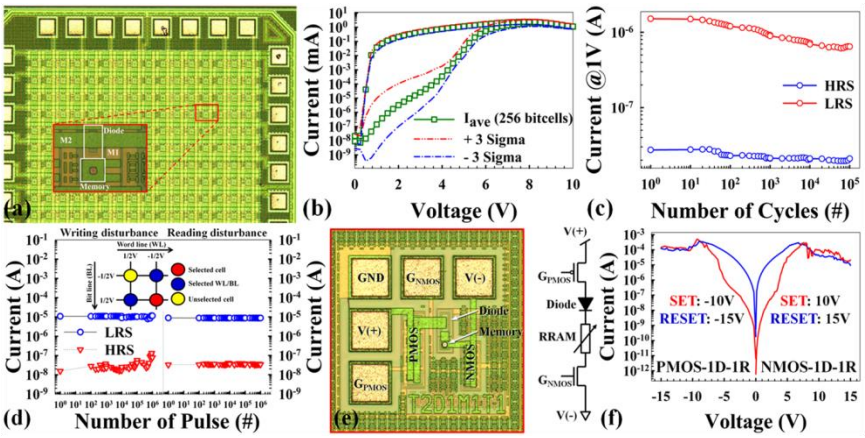

Figure 5.5. Electrical variation and reliability results for array structure for potential use in future neuromorphic computing applications.

Chapter 6: Conclusion and Future Work

6.1. CONCLUSION

At the time of finishing up this dissertation, Samsung's 3D V-NAND technology on FG structure has already been launched for around a year. 16nm technology node is also approaching the end of development phase with 3D NAND structure still on FG structure. Research is pushing into 10 nm and 7 nm technology node with new concepts on material and structure – binary metal oxide materials, 2D material, ReRAM, carbon nanotube, MRAM, and SiO_x. This research work looks at SiO_x materials in explicit in next generation nonvolatile application, aims at advancing their device performance through novel device structures and better fabrication techniques.

First, device structure, materials and electrical controlling for SiO_x-based ReRAM were investigated. MIS architecture was fabricated with various post-deposition anneal using rapid thermal annealing. Polarity effects of resistive switching characteristics and RESET process were studied. Horizontal and vertical device structure designs, and composition optimization (SiO_x, $x < 2$) by sputtering process have been fabricated in MIS architecture. Device characteristics including SET/RESET voltage, high/low resistive state (HRS/LRS), forming process and electrical controlling characterizations with various compliance current limitations and stopped voltage values have been compared. Effect of ambient dependence in SiO_x-based ReRAM has also been examined.

Second, further understanding the resistive switching mechanism for SiO_x-based ReRAM, edge and bulk device structures have been applied. An unusual backward-scan effect with DC and AC electrical response were studied. The switching behavior of the backward-scan effect is incorporated into Verilog-A simulations to characterize integration strategies for future circuit-level applications. Oxide stoichiometry effects by PECVD process on reversible switching and program window optimization has been

fabricated and examined to achieve autoforming process. Different electrode materials have also been applied into SiO_x-based ReRAM to achieve flexible manufacturing process. Modeling of resistive switching mechanism, including temperature effect, pulse response and carrier transport behaviors are performed, to develop a compact model in energy diagram, trap-level information, dipole polarization in SiO_x resistive switching layer, even for computer-aided design (CAD) in very-large-scale integration (VLSI) design.

Third, we have demonstrated high-density, wafer-scale 1D-1R nano-pillar SiO_x-based ReRAM fabricated by nano-sphere lithography. Excellent resistive switching characteristics and reliability are observed, the AC pulsed switching speed is in the 50 ns regime and multi-bit operation is demonstrated. The Si-based epitaxial 1D NP structure was formed by using a deep-Si-etch process. Low reverse-bias diode current and nonlinear I-V characteristics help reduce sneak-path issues and further improve the readout margin in practical large-scale array designs up to 1 Gbit in size. The demonstrated technology has great potential not only for maskless electronics, but also provides a fast and economical solution for wafer-scale manufacturing of high-density 1D-1R ReRAM arrays.

Last, we have demonstrated potentiation, depression and spike timing dependent plasticity in a synaptic device built using a SiO_x-based 1D-1R architecture. Proton-induced resistive switching behaviors in the SiO_x memory element were discussed. The electrical results demonstrate that the technology has good potential for providing a simple and robust approach for large-scale integration of programmable neuromorphic chips using CMOS technology, and represent a critical milestone regarding the potential use of SiO_2–based resistive memory as a synaptic device in future synthetic biological computing applications.

6.2. FUTURE WORK

6.2.1. Frequency Response and Internal Filament Modeling

Continue addressing resistive switching mechanism and self-compliance characteristics in intrinsic unipolar SiO_x-based ReRAMs are one of the interesting works for future topics. Adding external resistance is found to dramatically affect the voltage of the RESET process, providing insight into the unique unipolar operation. Resistive switching (RS) parameters for a range of external series resistance values indicate that RESET voltage can be controlled by series resistance; however, SET voltage is independent of series resistance. This suggests that the SET process is due to a voltage-triggered mechanism and that the program window (RESET-SET voltage) can be optimized for program/erase disturbance immunity in circuit-level applications. The SET and RESET transitions were also characterized using a dynamic conductivity method, which distinguishes the self-compliance behavior of SiO_x-based ReRAM (Figure 6.1). By using a conceptual "filament/GAP" model of the conductive filament and making reasonable assumptions, the internal filament resistance and GAP resistance can be estimated for high- and low-resistance states (HRS and LRS), and are found to be independent to external series resistance. Also, the hopping mechanism with temperature-dependence polaron effect and conductance with frequency response, or we called corner-frequency characteristics (transition frequency for defects and modeling) will be studied in detail (Figure 6.2). The experimental results not only provide insights into potential reliability issues, but also help clarify the switching mechanisms and device operating characteristics of SiO_x-based ReRAM.

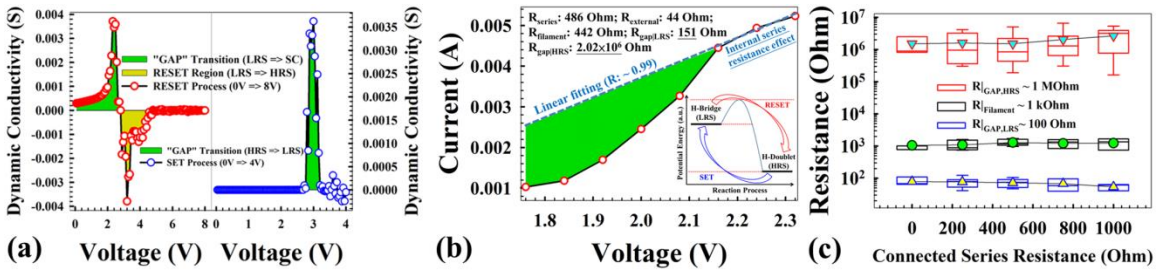

Figure 6.1. (a) ∂I/∂V characteristics for RESET and SET processes. (b) Calculated resistance values of filament, HRS, and LRS, and (c) for 10 cycles versus external series resistance.

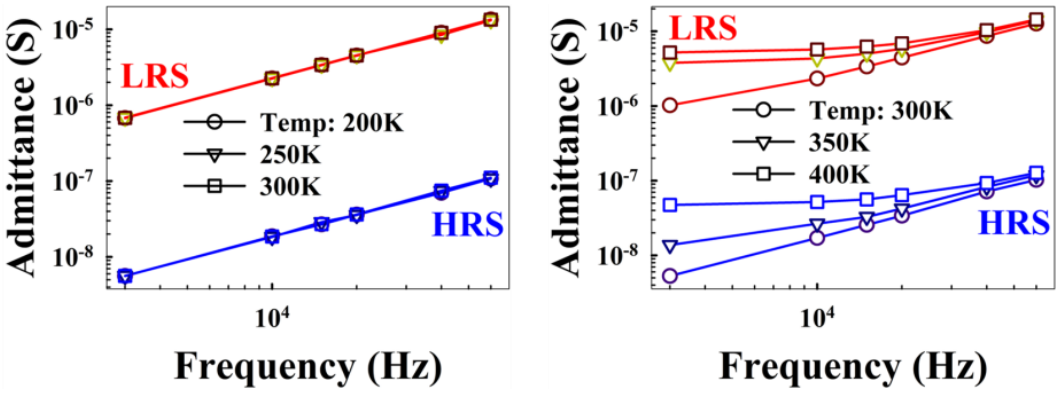

Figure 6.2. Admittance versus AC frequency between LRS and HRS (a) at low temperature range and (b) at high temperature range.

6.2.2. Stacking Engineering of SiO_x/HfO_x

Vertical Three different MIS device types have been fabricated to study the effects of the bi-layer dielectric structure (NP: 30nm-SiO_x; T1~T10: 1~10nm-HfO_x on top of SiO_x; and B1~B10: 1~10nm-HfO_x on bottom of SiO_x) (Figure 6.3 (a)). The results show that with HfO_x (> 3nm) on bottom, MIS exhibits resistive switching at low voltage (< 2V) and operation in air atmosphere without passivation. The added hafnium layer apparently provides the source of proton exchange reaction with conduction bandgap offset reduction for low-voltage (< 2V) RS (Figure 6.3 (b)). Clearly, SiO_x/HfO_x stacking optimization not only maintains the RS behaviors even in air environment without any

programming window degradation, but also further reduces the switching voltage below 2V.

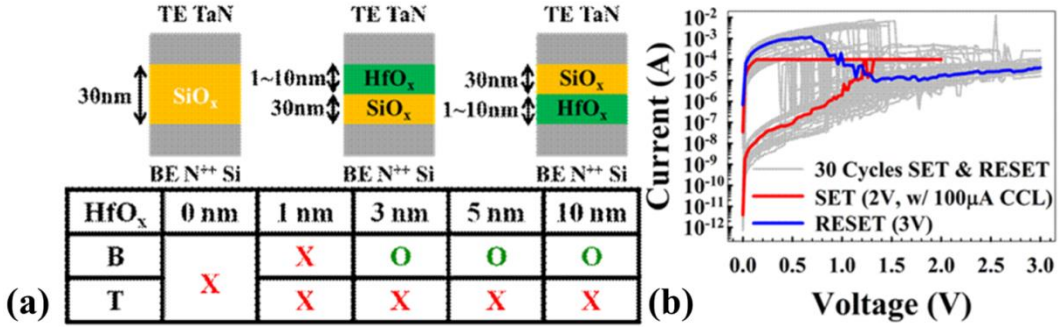

Figure 6.3. (a) Schematic description of vertical stacks of SiO_x/HfO_x layers (scales and layer position). (b) Thirty I-V SET and RESET curves in air with low voltage (< 2V) switching.

6.2.3. Bio-Inspiration from Mitochondrion: Reactive Oxygen Species Biomimetics in Electronics Device

Interest in mitochondria has risen and fallen over the past century in the quest to describe the fundamental processes of the cell. The mitochondria are the energy machinery of the cell, mainly producing adenosine triphosphate (ATP) as a major source to drive cellular processes necessary for its function. The process of oxidative phosphorylation in the mitochondrial respiratory chain also generates the major byproduct of superoxide, which is relatively short-lived and its usual fate is rapid dismutation to hydrogen peroxide (H_2O_2) by the mitochondrial superoxide dismutase (SOD). Other partially reduced or activated derivatives of oxygen (O_2^1, O^{2-}, and HO^-) may also accompany with highly reactive and toxic, and can lead to the oxidative destruction of cells in invertebrates and plants by radiation, toxic chemicals and drugs, which exert their detrimental effects via oxidation of essential molecules such as enzymes and cytoskeletal proteins. Excessive ROS are associated with several pathologies, such as

decreased performance in cognitive tasks, increase of tumor cell proliferation, and induce apoptosis (programmed cell death). During normal physiological aging, ROS production increases and antioxidant defenses decline; hence, ROS levels increase dramatically, resulting in hundreds of pathological conditions that promote oxidative stress, including neuro-degenerative diseases such Alzheimer's disease and Parkinson's disease. Therefore, the amounts of ROS need to keep in check by an elaborate antioxidant system, such as (1) composed of a multitude of enzymes, including superoxide dismutase (SOD), catalase, and peroxidases, (2) redox-active metals, such as iron catalyzing, and (3) radical-scavenging antioxidants (e.g., vitamin E). Recently, a range of assays, such as fluorescent dyes and redox-sensitive genetic reporters, have been developed to measure end points of mitochondrial oxidative damage and ROS flux in isolated mitochondria, cell culture and in vivo. This is thought to be a very specific application where specific cells produced what can only be described as toxic agents in order to kill invading microorganisms, so that we can better understand the roles and functions of mitochondrial ROS production in redox signaling and oxidative damage. In my proposal work, for the first time, we simulate a biomimetic reactive oxygen species (ROS–like) production and regulation systems by silicon dioxide (SiO_x) based electrical devices. Our studies are modeled the resistive switching mechanism as hydrogen (H)-related molecular transformations based on the theoretical energy-level calculation and polarization coupling with carrier transport behaviors. Two states, hydrogen bridge (Si-H-Si) and hydrogen doublet $(SiH)_2$, are modeled the SET transition as being initiated by hydrogen desorption from $(SiH)_2$ to form Si-H-Si, and the RESET transition is modeled as electron injection into a fixed positive-charge defect that induces proton release and an electrochemical reaction with Si-H-Si to re-form $(SiH)_2$. The switching event occurs at enough bias applied, however, not for oxygen-content environment. The H-passivation is

temporarily lost due to the oxygen-induced biomimetic reactive oxygen species (ROS–like) substance so that RS fails in ambients containing O_2. The recovery of RS process can be done when device backs to non-oxygen-content environment or integrating a hermetic passivation layer to avoid ROS–like substance production. Furthermore, by using the one diode – one memory element (1D-1R) architecture, it can offer low static-power for suppression of sneak-path issues and reduces peripheral circuit design, and, also realize a synapse behaviors, including spike-timing-dependent plasticity (STDP) for neuromorphic computing regulation system. This work not only provides the concept of biomimetic ROS-like production and regulation systems in electrical device applications, but also could have huge therapeutic potential in treating redox-related disease for time-reduction and accuracy incensement.

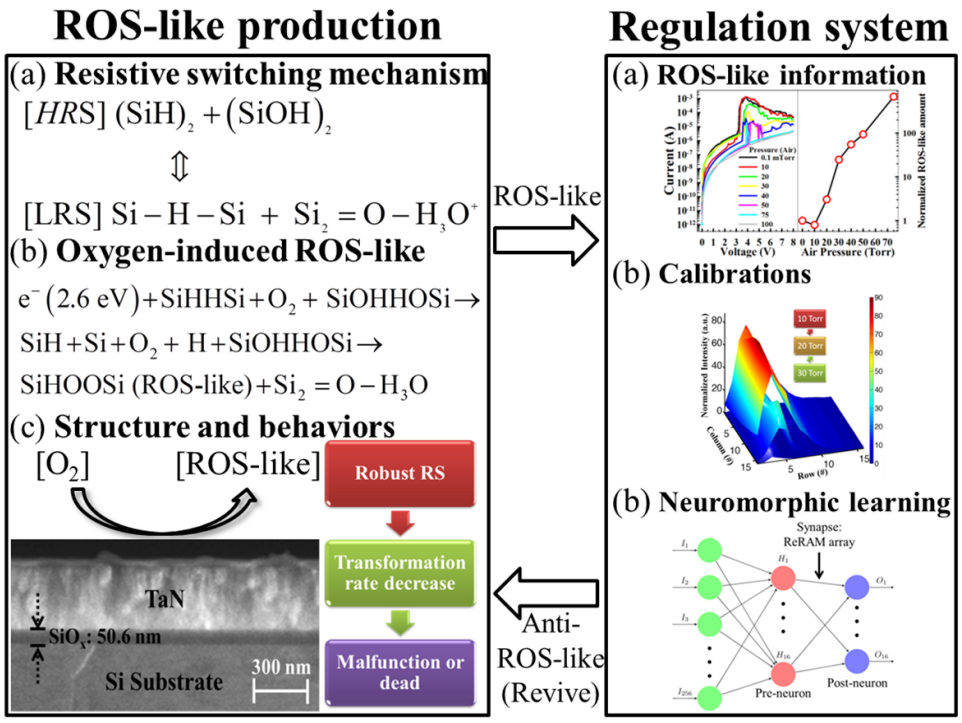

Figure 6.4. The ROS-like production and regulation system in biomimetics electrics devices.

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Vita

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