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Roll-to-Roll Nanofabrication Process for Flexible Cu Metal Mesh Transparent Conducting Electrodes

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Roll-to-Roll Nanofabrication Process for Flexible Cu Metal Mesh Transparent Conducting Electrodes

by

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Dedication

To my family and beloved friends.

Thank you for your endless encouragement and all the opportunities I have had in this life.

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The work described herein is by no means an individual effort and would not be possible without the help of many people. I would like to especially thank Dr. Ovadia Abed for having patience with me during every step of this remarkable journey and for sharing his extensive knowledge and humor. I would also like to acknowledge Dr. Michael Watts for his invaluable expertise and helpful suggestions during process development. I also appreciate Dr. Shrawan Singhal for performing the imprint lithography needed for this work. Thank you to all the members of the Scalable Nanotechnologies Lab (SNL) for their countless advice, assistance and friendship since starting my graduate career. I would like to specifically thank Brian Gawlik for his help with running simulations and taking optical measurements. Thank you to the staff at the University of Texas Microelectronics Research Center (UT-MRC) for providing the training and equipment necessary for experimentation. I would also like to thank the donors of the Cockrell School of Engineering Graduate Fellowship Program which partially supported my graduate work at UT Austin. This work was supported by the National Science Foundation Nanosystems Engineering Research Center on Nanomanufacturing Systems for Mobile Computing and Mobile Energy Technologies, NSF EEC under Grant No. 1160494.

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Abstract

Roll-to-Roll Nanofabrication Process for Flexible Cu Metal Mesh Transparent Conducting Electrodes

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Transparent conducting electrodes (TCEs) are essential components in many optoelectronic and display technologies including light-emitting diodes, photovoltaics, and display touch screen panels. Transparent conducting oxides, specifically indium-doped tin oxide (ITO), are currently the industry standard TCE material due to their high electrical conductance and optical transparency. However, conventional ITO electrodes are intrinsically brittle, require high-temperature vacuum processing and suffer from fluctuating material costs making them undesirable for future generation optoelectronic and display devices and incompatible for flexible devices. As a result, many alternative TCEs have garnered significant research interest over the past few decades. Metal mesh-based electrodes have recently appeared as the most pragmatic solution to replace ITO for future flexible devices due to their highly tunable electrical and optical properties, low material cost and inherent mechanical robustness. However, metal mesh TCEs require high-resolution, ultra-large area nanoscale patterning on flexible polymer substrates which is beyond the capabilities of optical lithography. Moreover, commercial metal mesh

electrodes will depend upon high throughput, scalable roll-to-roll (R2R) processing in order to meet the cost needs of the projected markets.

In this work, nanoscale Cu metal mesh electrodes on flexible polycarbonate substrates and rigid quartz substrates are demonstrated using a novel R2R compatible fabrication process employing jet-and-flash nanoimprint lithography (J-FIL), linear ion source etching (LIS) and selective electroless Cu metallization (ECu) using a Pd seed layer. Process step verification details are provided including a morphological study of ECu deposition. Cu grain size is found to be independent of Pd seed layer thickness and plating time in solution, and resistivity of ECu deposited thin films was found to be about 8 times higher than bulk Cu at 13 μΩ cm. Rectangular cross-section trench patterns arranged in a square grid geometry embedded in UV cured imprint resist define the fabricated Cu metal meshes. Two trench dimensions were explored in this work: (i) height of 100 nm, linewidths of 300 nm and pitch of 3 μm, and (ii) height of 100 nm, linewidths of 500 nm and pitch of 5 μm. The most conductive flexible metal mesh sample achieved sheet resistance as low as 3.4 Ω/sq. and average transmittances of all samples was roughly 50% in the visible spectrum with significant potential for optimization. Comparison of measured spectral transmittance and simulations showed a reduction in broadband transmittance up to 40% due to the sputter-coated 3 nm thick Pd seed layer required to reliably catalyze the ECu reaction. The focus of the experimental work was to use existing J-FIL templates to establish the R2R compatible nanofabrication process. The optimum mesh design to maximize transmission while minimizing sheet resistance was not the focus of experiments. In order to further improve metal mesh TCE performance, a preliminary optimization strategy has been proposed to identify optimum mesh geometry given a target application. Optimization results tend towards a pitch to linewidth ratio of about 100 and maximize grid line aspect ratio for high transmittance while minimizing for sheet

resistance. Simulation and process development insights incorporated in this thesis provide guidance for future research to further refine the proposed R2R compatible fabrication process for and design of flexible metal mesh TCEs.

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Chapter 1: Introduction and Motivation

Transparent conducting thin-film electrodes (TCEs) are essential components in many optoelectronic devices such organic photovoltaic cells (OPVs), organic light-emitting diodes (OLEDs), liquid crystal displays (LCDs) and touch screen panels (TSPs) [1]–[4]. TCEs provide electrical contact to active layers of these devices while allowing light to enter or exit them i.e. electrically conductive and optically transparent. In order to accomplish this critical function, TCEs must possess high charge carrier (electron or hole) mobility and concentration while counterintuitively supporting the transmission of photons through the film. Therefore, the in-plane DC electrical sheet resistance (R_s) and optical transmittance in the visible spectrum (typically represented by the transmittance at 550nm wavelength, T_{550nm}) are two key parameters which characterize performance of TCE films [5]. Recall, sheet resistance is a measure of resistance of a thin film with uniform thickness (t), and is written as

$$R_s = \frac{\rho}{t}$$

Equation 1: Sheet resistance of a uniform thin film

where ρ is resistivity of the material. Optical transmittance is the ratio of intensity of total light transmitted through the film (I) to the intensity of incident light (I_o) at a given wavelength, and is expressed by Equation 2 for 550nm.

$$T_{550nm} = \frac{I}{I_0}$$

Equation 2: Optical transmittance though a thin film

Note, 550nm wavelength light is of prime interest in transmittance measurements since it corresponds to the peak solar spectrum visual sensitivity in humans [6]. Ideally, electrical conductivity should be maximized while retaining high broadband transmittance

throughout the visible spectrum. For displays applications, another important consideration of TCE films is optical haze or scattering of light. Haze is defined as the ratio of forward scattered light intensity (I_s) outside of a cone with half angle 2.5° subtended at the center of the surface of the film [7] to the intensity of total forward transmitted light through the film, and is expressed by Equation 3 [8].

$$Haze = \frac{I_s}{I}$$

Equation 3: Haze through a thin film

Figure 1 shows the basic device structure and components of an LCD, OLED and OPV cell. TFT-LCDs employ two separate transparent electrodes, the common and pixel electrode, in order to induce a local electric field and control the alignment of the liquid crystal molecules between two orthogonally oriented polarizing films. Light enters the LCD device from a backlight unit and must pass through both electrodes and substrate materials before exiting. OLEDs and OPVs, in contrast, generate photons or charge in the active layer due to charge recombination or separation, respectively. TCEs must readily be able to inject or collect charge from the active layers in OLED and OPV devices, respectively, for efficient performance of these devices.

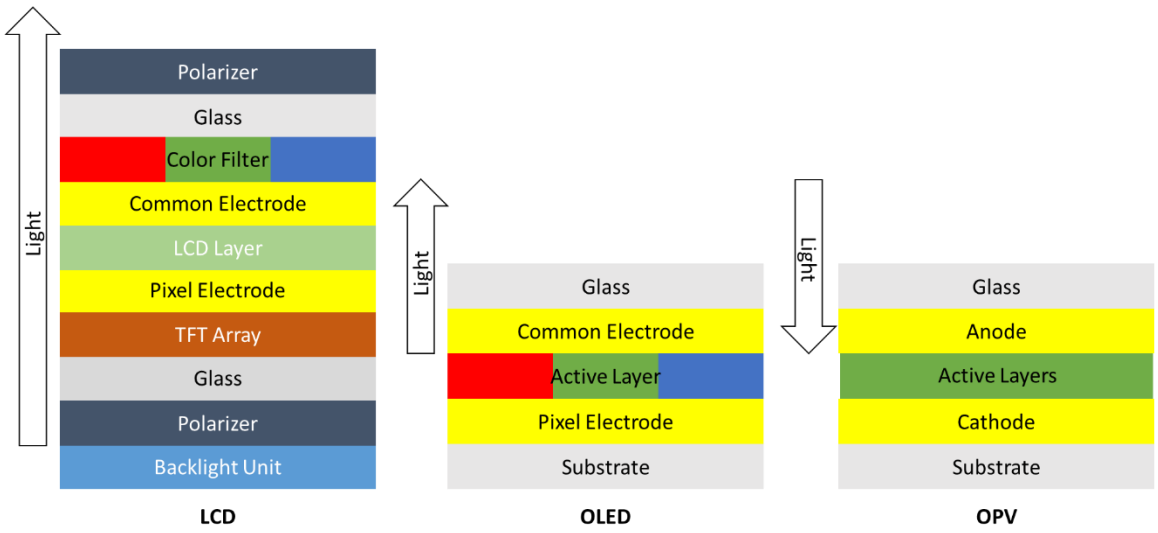

Figure 1: Schematic illustration of basic LCD, OLED and OPV device architecture

Specific performance and material property requirements of TCEs in application are unique to device type and position of the electrode in the device architecture. Typical LCD and organic optoelectronic applications require TCE sheet resistance under 10 Ω/sq. and transmittance above 90%, whereas, TSPs may only require sheet resistance of 100-300 Ω/sq. at a similar transmittance [9], [10]. Moreover, the interface between the electrode and active layer strongly affects overall device performance. Various electrode properties such as surface roughness, work function and processability highly influence electrical properties of this interface. As device footprints continue to increase, TCEs need to be able to scale accordingly and correspond with lower sheet resistance values in order to preserve device performance and efficiency. Growing demand in recent years for flexible and wearable devices now requires compliant TCE films which retain their optical and electrical properties under large and repeated strain induced by bending.

Discovered in the mid-20th century [11], doped metal-oxide films or transparent conductive oxides (TCOs) are the industry's incumbent technology for TCEs in optoelectronic applications. Indium doped tin-oxide (ITO) is the ubiquitous TCO for use as a TCE due to its excellent balance of optical and electrical properties. There exists an intrinsic trade-off between Rs and T550nm where increasing thickness of the TCO layer

results in higher electrical conductivity at the expense of lower optical transmittance and vice versa. Commercial ITO films vary in thickness between 80-300nm with sheet resistances below 20 Ω/sq. and optical transmittance of 85-90% within the visual spectrum (λ from 400nm to 700nm). Essentially, electrical properties of ITO are a function of the film's dopant concentration which makes them highly tunable. Developed alongside the semiconductor industry, various techniques exist to grow ITO films on a substrate in the form of physical vapor deposition (PVD) i.e. magnetron sputtering and evaporation [12], [13]. However, these deposition methods are limited in scale and applicability due to high temperature vacuum processing conditions required which can damage organic active layers. Furthermore, the naturally brittle mechanical behavior of TCOs coupled with scarce indium resources and wasteful manufacturing make the use of ITO in future flexible applications either highly undesirable or unacceptable [14]. Next generation devices require TCEs that not only balance electrical and optical properties but must also be inexpensive, flexible and compatible with cost-effective scalable manufacturing methods i.e. roll-to-roll (R2R) fabrication.

STATE OF THE ART IN ALTERNATIVE TRANSPARENT CONDUCTING ELECTRODES

To address the need for a flexible TCE film, researchers have investigated a variety of ITO alternatives over the past few decades. Research efforts in alternative TCEs include three main categories: 1) conducting polymers, 2) carbon-based materials and 3) metallic transparent electrodes. The following sections provide a brief overview of each type and their place in this rich research ecosystem beginning with polymeric transparent electrodes then graphene and carbon nanotube (CNT) networks followed by metal nanowire (MNW) networks and finally patterned thin-films metal mesh grids.

Transparent Conducting Polymers

Since gaining prominence in the later 1980s, transparent conducting polymers have attracted attention as alternative TCEs due to their high transparency, compatibility with scalable solution-based processing and intrinsic flexibility [15]. Conductive polymers achieve high conductivity through a process of chemical doping, and post treatments can further improve electrical characteristics [16]. Amongst this type of TCE, poly(3,4-ethylenedioxythiophene): poly(styrenesulfonic acid) (PEDOT:PSS) is one of the most important and widely used conductive polymer for optoelectronic applications to date. Due to its relatively high work function, PEDOT:PSS often serves as an interfacial layer in OLEDs and OPVs between the active layer and ITO to overcome the energy barrier for injection/collection of charge and effectively smooth ITO surface roughness [17]. While Mochizuki et al. and Zhang et al. demonstrated TSPs and OPVs using PEDOT:PSS as stand-alone TCEs, respectively, further improvement in PEDOT:PSS conductivity is needed for it to be a suitable replacement for ITO [16], [18], [19]. Conductive polymers also exhibit significant performance degradation from exposure to high levels of humidity, temperature and UV light [20], [21]. Environmental and operational instability are key technological challenges limiting conducting polymers and must be addressed to meet the needs for next generation TCEs.

Graphene

Graphene is a two-dimensional material consisting of a single atomic monolayer of carbon atoms connected by sp^2 bonds in a honeycomb crystal lattice [22]. This structure gives graphene extremely high in-plane conductance since all valance electrons are delocalized over the entire sheet and travel freely with negligible scattering [23]. Based on this unique electronic structure, graphene has a theoretical optical transmittance of 97.7% per layer [24]. In addition to remarkable electrical and optical properties, defect-free single

layer graphene is arguably the most mechanically resilient material ever studied [25] and possesses excellent thermal and chemical integrity [26].

By all merits, graphene is an ideal candidate material to replace ITO as a flexible TCE, however, the inability to achieve large-scale synthesis of high-quality graphene currently hinders it application in commercial devices. Mechanical exfoliation of monolayers of graphene from bulk graphite using an adhesive is the basic method for academic research, but this method is both low-yield and throughput i.e. produces highly defective graphene flakes rather than continuous sheets [22]. Chemical vapor deposition (CVD) of graphene followed by thermal post-processing steps has successfully yielded large area graphene films [27], [28]. However, both the peeled graphene and chemically derived methods induce structural defects in the graphene monolayer and considerably increase its sheet resistance in excess of ITO at comparable transmittance values [29]. Introducing dopants into graphene sheets may improve electrical properties, but this increases processing complexity. Therefore, graphene is unable to replace ITO since no scalable fabrication process capable of producing high-quality graphene sheets currently exists.

Carbon Nanotube Networks

Similar to graphene, CNT networks have gained extensive interest and continue to be a promising research topic due to their unique combination of electrical, optical, mechanical properties and solution processability. Single-walled CNTs are a 1D material consisting of a single layer of graphene rolled into a hollow cylindrical shape. Individual CNTs exhibit remarkable electrical conductivity and high charge mobilities [30], [31]. However, thin film counterparts consisting of dispersed CNT networks fail to reproduce such properties due to contact resistance between adjacent CNTs and a lack of percolating electrical pathways through the film [9]. Processing of CNT networks requires the suspension of individual CNTs in solvent or aqueous media and techniques such as spin-

coatings with which to dispense a thin layer of the CNT containing solution on to a substrate. The electrical and optical properties of these films are highly dependent on the concentration and degree of dispersion of CNTs in the prepared solution [32]. Due to challenges associated with CNT synthesis, these solutions have yet to achieve the CNT concentration levels required to surpass the electrical percolation density threshold for large-scale fabrication [33]. Moreover, CNT solutions include surfactants to promote disperse suspension and prevent aggregation of individual CNTs. These additional species act as impurities in solid CNT networks films and contribute to CNT junction resistance lowering conductivity of prepared films [34]. As shown in Figure 2, CNTs in these networks settle in a random arrangement resulting in a film with excessive surface roughness. The irregular surface of these networks leads to poor electrical contact with active layers and lowers overall device performance. While post-processing steps can reduce surface roughness of fabricated CNT network TCEs [35], current challenges with scalable production of CNTs obstructs the wide spread adoption of this technology for next generation flexible electrodes.

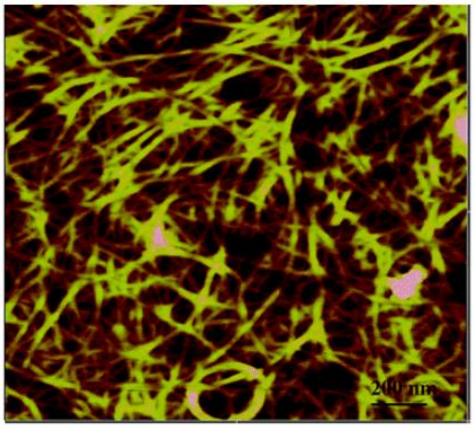

Figure 2: AFM image of CNT network on PET substrate [36]

Metal Nanowire Networks

Researchers have also studied arranged and random networks consisting of metal nanowires (MNWs) for next generation TCEs due to their superior electrical properties and

solution-based processing [37]. MNWs typically constitute Cu, Au, or Ag due to their high bulk conductivities and relative ease of synthesis. Physical dimensions of individual MNWs range in diameter between 20-40 nm and length up to 20 μm depending on wire material and chemistry [6], [38]. Similar to CNT networks, the performance MNW thin-film networks is a function of MNW type/geometry, interaction between MNWs and density/dispersion of MNWs in the film. In practice, Ag NW networks are the most common type since their synthesis is the best understood, but Cu NWs are less susceptible to corrosion. Increasing the diameter and length of individual NWs increases conductivity of MNW networks by permitting more electrical pathways. However, increasing cross-sectional area of MNWs negatively affects transmittance of light through the network and induces significant scattering [39]. Scattering of light translates to increased haze which is especially deleterious in display applications where image clarity is a primary concern [8].

As shown in Figure 3, fabricated optoelectronic devices employing percolating random networks of Ag NWs as TCEs demonstrate comparable performance to ITO while being flexible i.e. transmittance above 90% and sheet resistance of ~20 Ω/sq. [40]. Nonetheless, several key technology challenges need solutions in order for MNW networks to be a viable next generation TCE. The main concerns associated with MNWs network TCEs are atmospheric corrosion and electrical breakdown which catastrophically increase sheet resistance and degrade device performance [41], [42]. Corrosion such as oxidation in NMWs due to exposure to atmospheric conditions in operation are akin to their bulk material counterparts. Electrical breakdown in NMW networks results from electromigration of charge within individual NWs causing void formations and eventual breakage of the wire [43]. Additionally, deposited MNW films exhibit poor adhesion to substrates and high surface roughness resulting in poor electrical contact with functional layers of organic optoelectronics often requiring an interfacial layer such as PEDOT:PSS. Post-process steps such as thermal annealing, laser sintering and mechanical pressing have

shown to reduce surface roughness and wire-to-wire junction resistance, but these measures contribute to fabrication complexity, lower throughput and increased cost.

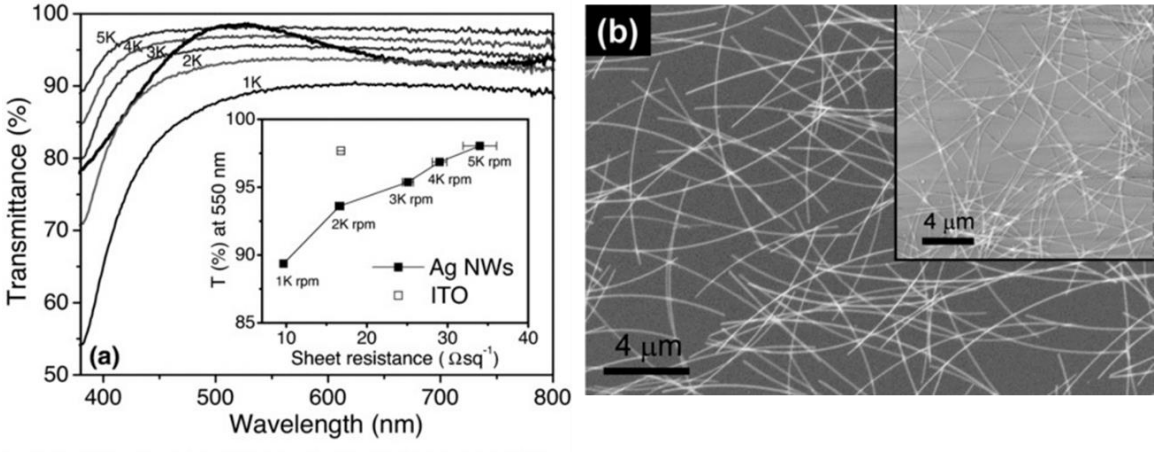

Figure 3: Measured spectral transmittance of Ag NW network on glass deposited at different spin-coater speeds compared to commercial ITO coating (bold line). The insert compares transmittance to sheet resistance. b) SEM & AFM images for a prepared Ag NW network [40]

METAL MESH TRANSPARENT CONDUCTING ELECTRODES

One of the most promising candidates to replace ITO for future flexible optoelectronic applications are TCEs based on patterned metal mesh grids (MMGs). As their name suggests, MMGs are patterned thin metal films with thru-hole transmissive windows in a periodically repeating lattice creating a very fine, interconnected network of repeating metal lines. MMGs typically employ submicron wide grid lines to ensure invisibility to the human eye and provide for adequate transparency in the visible spectrum [44]. While macro-scale MMGs exist, this thesis focuses on metal nano-mesh grids for practicality in high-end TCE applications. Figure 4 provides an example of a typical metal nano-mesh TCE on a glass substrate where the raised orthogonal lines constitute the patterned grid.

MMGs possess several advantages over ITO and other alternative TCE technologies making them attract candidates as TCEs for future devices. For example, MMGs have the potential to increase OPV efficiency by exploiting the light trapping

phenomenon of subwavelength grating structures [45], [46]. Unlike CNT and MNW networks, metal mesh grids do no suffer from a lack of percolating electrical pathways nor junction resistance between metal lines since the entire network is a contiguous metal mesh and can achieve extremely low sheet resistances [9]. Furthermore, metal mesh TCEs are naturally compatible with future flexible devices due to the intrinsic ductility of metals. Choice of material for MMGs is virtually limitless due to the relative ease of depositing thin metal films on a substrate, and literature on the topic reports on MMGs TCEs consisting of Au [47], Cu [48], Al [49] and Ag [50]. This freedom in material compatibility allows for simple tuning of electrode work function for optimum device performance [51].

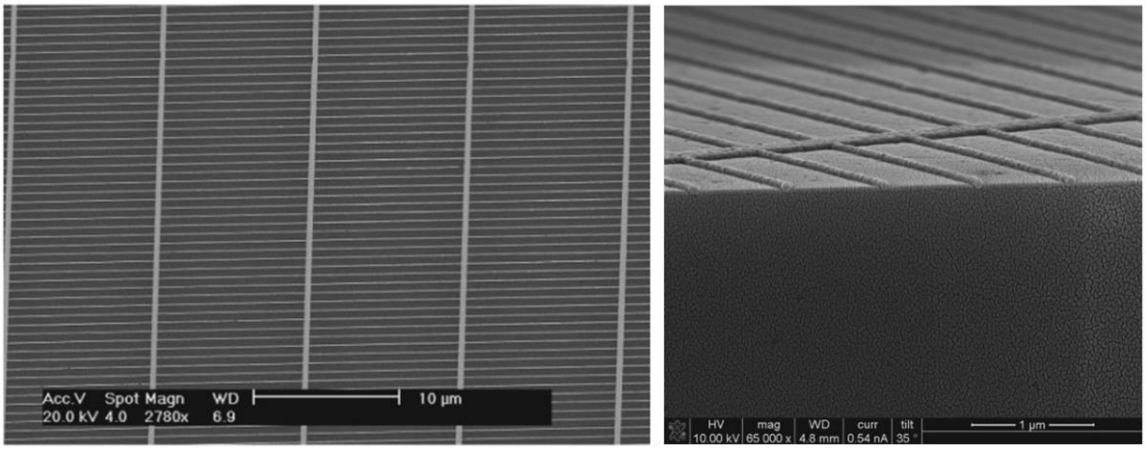

Figure 4: Left) SEM image of an metal mesh electrode on glass; Right) Perspective image of the same electrode [52]

The geometry of the metal layer highly influences the optical, electrical and mechanical properties of metal mesh grids. For instance, the shape of the MMG pattern can take different forms such as square or honeycomb as shown in Figure 5, and this aids in avoiding the presence of moiré phenomenon on the surface of the MMG film. Kwon et al. also report the shape of the metal grid pattern effects the flexibility and durability of MMG TCEs under both static and cyclic strain [53]. Furthermore, hierarchical structures consisting of multiple pattern geometries benefit by combining properties corresponding to each pattern into a single film [54]. Geometric parameters linewidth (w), line-height (h)

and pitch (p), as depicted in Figure 6, define the fill factor (f_F) of the grid or the ratio of area covered by metal verses the open aperture area in the center of the unit cell for a given pattern geometry i.e. the shaded area [55].

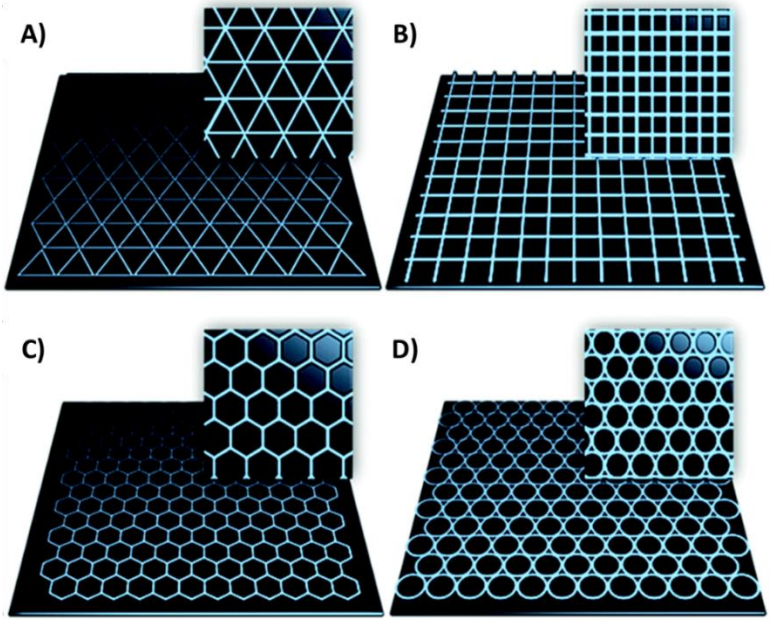

Figure 5: Schematics illustrating different metal mesh electrode patterns: A) triangular, B) square, C) honeycomb and D) circular [6]

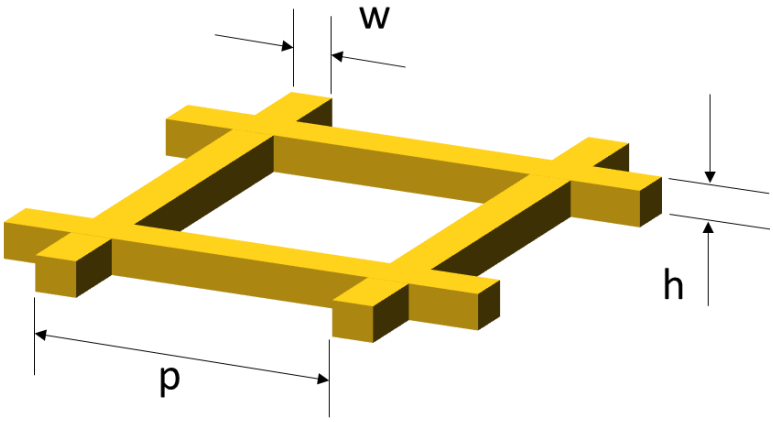

Figure 6: Schematic depicting linewidth (w), line-height (h) and pitch (p) of a square grid

Therefore, fill factor is an exemplary indicator of optical transmittance and sheet resistance of MMG TCEs and is discussed in greater detail later in Chapter 2. Not that

expressions for fill factor are unique to a particular pattern shape and should be modified accordingly e.g. Equation 4 defines fill factor for a square grid similar to that depicted in Figure 6, whereas Equation 5 defines fill factor for a regular hexagon or honeycomb pattern.

$$f_F = \frac{2pw - w^2}{p^2} = 1 - \frac{(p-w)^2}{p^2}$$

Equation 4: Fill factor for a square grid

$$f_F = 1 - \frac{\left(a - \frac{w\sqrt{3}}{3}\right)^2}{a^2}$$

Equation 5: Fill factor for a honeycomb grid where a is the side length of the regular hexagon

MMGs are either embossed on a substrate or embedded depending on the fabrication process. Positioning of the grid relative to the supporting substrate is an important consideration when evaluating surface roughness. As mentioned, low surface roughness allows for improved electrical contact with active layers of devices especially OLEDs and OPVs. Embedment in a substrate material significantly reduces surface roughness of MMGs, and post-processing such as chemical-mechanical polishing (CMP) may further planarize the film in some cases. Furthermore, embedded grids are less likely to delaminate from substrates due to the increased contact area for adhesion.

Since Gao et al originally reported metal mesh TCEs realized by nano-imprint lithography (NIL), researchers have studied MMGs extensively, and there exists a large body of knowledge on this subject [49], [52]. Table 1 tabulates reported transmittance and sheet resistance values of fabricated metal mesh TCEs along with several key design parameters. Analyzing Table 1 reveals strong evidence metal mesh-based electrodes have progressed steadily and are now at a level matching or exceeding ITO in terms of optical

and electrical performance [56]. Moreover, various fabrication methods compatible with flexible substrates including lift-off, etch, transfer printing, blading/sintering of conductive inks, selective metallization and electrohydrodynamic printing have demonstrated realized metal mesh grids.

Table 1: Reported values and features of various metal mesh TCEs

Reported Values			Device Design							Ref.
T_{Avg}	Rs [Ω/sq.]	Haze	Pattern	Linewidth [μm]	Line height [μm]	Pitch [μm]	Material	Substrate	Packaging	
95%	<5	5%	Square	0.3	0.5	30	Al	Glass	Embossed	[57]
96%	6.3	-	Square	>0.6*	2	50	Ag Paste	PET	Embedded	[58]
80%	90	-	Square	5	.180*	25	Ag NW	Glass	Embossed	[59]
96%	0.5	-	Square	5	8	800	Cu	PDMS	Embedded	[60]
89%	100	-	Square*	0.04	0.015	1.14	Pt ink	Glass	Embossed	[61]
94%	0.43	5%	Square	0.9	0.8	26	Ag	PUA	Embedded	[62]
83%	9.8	-	Square*	7.5(.21)	0.018	150(5)	Cr/Ag	PET	Embossed	[54]
84%	14	-	Hexagon	3.5	3	74*	Cu/Sn ink	PET	Embedded	[63]
89%	2.1	-	Hexagon	2.4	3	74*	Ag/Ni	PET	Embedded	[64]
80%	5	15%	Square	0.13	0.03	1	Ag	Glass	Embossed	[65]
94%	1	-	Square	0.9	1.8	50	Cu	COC	Embedded	[56]
75%	74.5	-	Square	0.065	0.05	0.5	Au	SiO_2/Si	Embossed	[66]
91%	10	-	Square	0.5	1.5	20	Au	Glass	Embossed	[67]
85%	17	10%	Square	0.7	0.1	10	Ag	PET	Embedded	[68]
63%	15	-	Hexagon	3	0.03	10	Au	Glass	Embossed	[47]
92%	97	5%	Square	4.5	0.09	150	Au	PET	Embossed	[69]
88%	49.2	-	Square	0.15	0.06	3.2	Ag	Glass	Embossed	[70]
83%	20	-	Hexagon*	0.3	0.25	10*	Ag	PET	Embossed	[50]
91%	38.7	-	Square	0.045	0.06	1	Ag	SiO_2	Embossed	[71]

Patterning of metal mesh TCEs, however, requires nanometer resolution and is the crux of the problems in terms of throughput, yield, and expense for MMGs for use as next generation TCEs. There currently exists a need to identify a scalable method for producing metal nano-mesh TCEs in order to demonstrate their commercial competitiveness as a replacement for ITO. Patterning of metal mesh grids utilizing conventional photolithography is the most common method, but it is prohibitively costly, complex to scale, and incompatible with flexible substrates [72]. Rolling mask lithography (RML) developed by Metamaterial Technologies - formally Rolith - offers a method to perform photon based patterning in a R2R fashion, but due to fabrication complexity associated with cylindrical photomasks, this method is limited in substrate width and lacking in resolution/anisotropy of etch [57], [73]. Electron beam lithography offers class-leading resolution at the cost of throughput, and cannot be considered a realistic technique for industrial fabrication due to its serial information transfer nature.

One possible solution comes in the form of NIL, specifically Jet and Flash Imprint Lithography (J-FIL), due to its excellent resolution, scalability, compatibility with R2R processing and ability to produce high aspect ratio (AR) features [74]–[77]. NIL mechanically transfers a pattern onto a substrate and is well-suited for large-area continuous printing. J-FIL is a mature technology deployed commercially in the semiconductor industry [78], [79] and offers an excellent platform to realize scalable metal mesh electrodes. Figure 7 depicts the basic process steps of J-FIL.

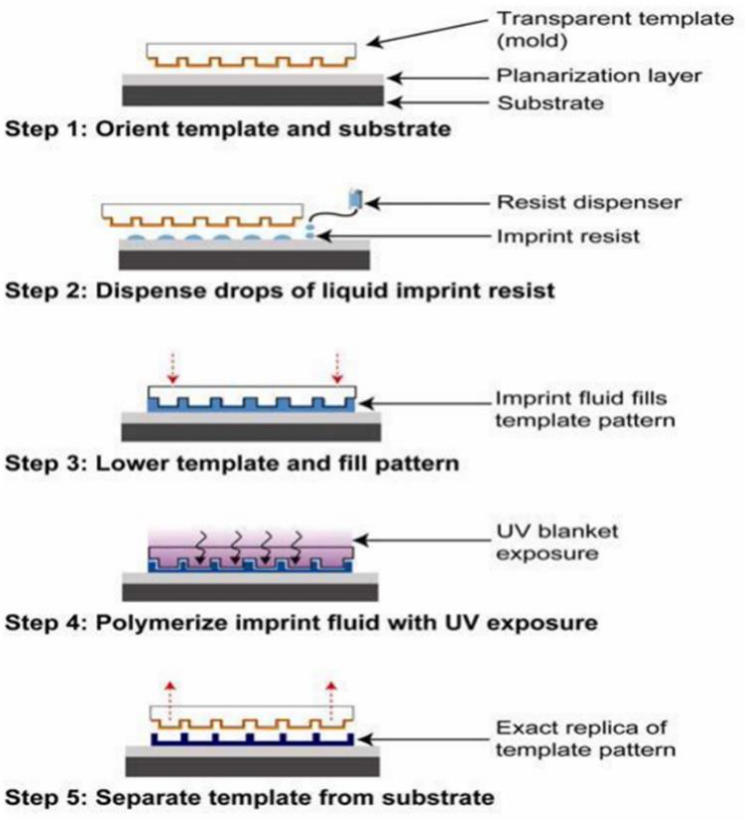

Figure 7: Schematic of J-FIL process [80]

First, spin coating or ink-jet printing dispenses a layer of liquid UV-sensitive imprint resist on a planarized substrate. Next, a transparent template or mold etched with the inverse of the desired pattern lowers on to the substrate surface, and the liquid resist fills cavities in the template mold by capillary action. Then, UV light exposure through the transparent template polymerizes the previously liquid imprint resist. Finally, the template rises and separates from the substrate leaving behind an exact negative replica of the template pattern in the UV cured resist.

RESEARCH OBJECTIVES

This thesis presents an engineering effort to develop a nanofabrication process scheme utilizing only roll-to-roll compatible unit steps to realize Cu metal nano-mesh

transparent conducting electrodes on polymer substrate for flexible display applications. Cu is selected as the material of choice for this purpose, as opposed to Ag or Au, due to its low material cost, excellent electrical conductivity, and solution-processability. The main goal of this research consists of two objectives. The first objective entails accurate modeling of metal mesh TCE electrical and optical properties for the purposes of optimization. The second objective is to demonstrate a viable method to fabricate any arbitrary geometry metal mesh such that optimized designs can be created in an inexpensive, scalable and high-throughput R2R fashion.

Chapter 2 discusses the underlying physics of the optical and electrical properties metal mesh electrodes and methods to predict device performance. Theoretical understanding informs modeling of transmission and sheet resistance values of MMGs. Following model verification, the chapter concludes with a simple preliminary design optimization approach for designing MMG TCEs.

Chapter 3 captures process development and experimentation towards identifying a feasible fabrication process for embedded Cu metal mesh electrodes. This is divided into three main fronts and chronicles major learning items from each.

Finally, chapter 4 contains a summary of work, main conclusions and recommendations for future work.

Chapter 2: Design of Metal Mesh Transparent Conducting Electrodes

PREDICTIVE MODELS FOR METAL MESH PERFORMANCE

On a scale greater than the pitch (p) of grid lines, geometry of the mesh structure dominates the overall in-plane current distribution, and therefore sheet resistance, of the MMG electrode [55]. By way of Kirchhoff's rules, Van de Groep et al. showed that R_S of a square grid network consisting of N x N wires can be approximated by Equation 6 with good agreement to empirical data [71].

$$R_s = \frac{N}{N+1}\left(\frac{\rho p}{wh}\right)$$

Equation 6: Expression to calculate sheet resistance of square grid metal mesh electrode

As the number of lines in the network increases, the first term in Equation 6 approaches unity, and sheet resistance becomes a linear function with respect to network pitch for a given linewidth and height. Note, resistivity (ρ) here may not be equivalent to bulk resistivity (ρ_{bulk}) and should be confirmed experimentally. Nonetheless, for an arbitrary grid geometer, applying Kirchhoff's rules may become prohibitively complicated. Ghosh et al. proposed another expression to calculate R_s of a metal mesh given by Equation 7.

$$R_s = \xi\left(\frac{\rho}{h}\right)\left(\frac{1}{f_F}\right)$$

Equation 7: Expression to calculate sheet resistance of an arbitrary geometry metal mesh electrode

This expression assumes sheet resistance of a patterned metal mesh is proportional to that of a continuous thin-film of the same metal of equal thickness divided by the fill factor of the grid geometry. The correction factor (ξ) accounts for discrepancies between

ideal grids and actual fabricated grids due to defects and/or processing, and is defined empirically.

If the thickness of the metal grid is sufficiently larger than the skin depth of the material, the following simplifying assumption holds true: grid lines are optically thick or completely opaque and the space between the lines allow for 100% transmission. Therefore, the light which directly passes through the gaps between grid lines minus light reflected or absorbed by the areas covered by metal should, in principle, dominate the optical transmittance through a metal mesh electrode. Fresnel reflection losses at interfaces as light passes through the substrate which supports the grid and any subsequent material layers in the TCE stack also affect total transmission through the film. According to this simplifying assumption, theoretical transmittance of a metal mesh TCEs is given by [81]:

$$T_{550nm} = \left[\prod_{i=1}^{n}(1 - R_i)^2\right](1 - f_F) = T_{layers}(1 - f_F)$$

Equation 8: Theoretical transmittance through metal mesh grid electrode where n is the number of materials in device stack.

The product term in the Equation 8 accounts for reflection losses of all material layers in the device stack. Fresnel reflection loss (R_i) is defined by Equation 9.

$$R = \frac{(n_1 - n_2)^2}{(n_1 + n_2)^2}$$

Equation 9: Fresnel reflection loss at material interface where n_i represents refractive indices of corresponding materials at interface

Jang et al. report good agreement between these models and measured values of Ag grids prepared by EHD printing for both electrical resistance and optical transmittance as shown in Figure 8.

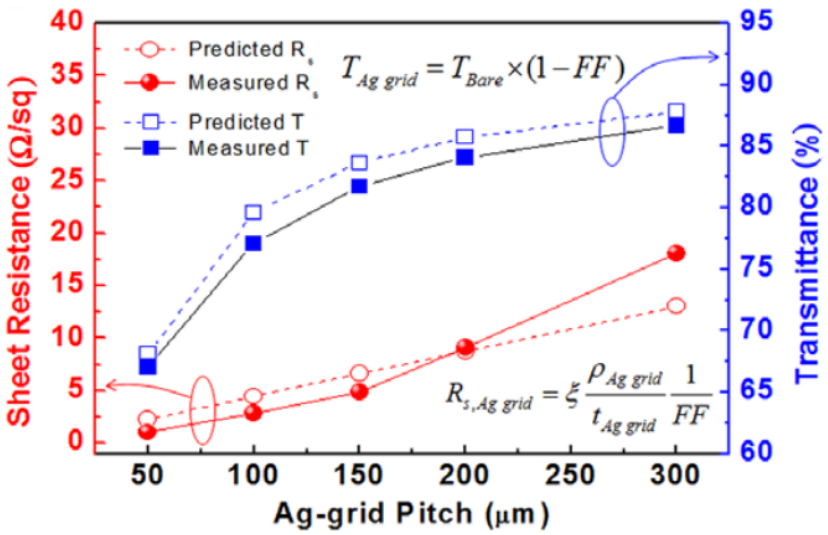

Figure 8: Theoretical vs. empirical sheet resistance and transmittance of Ag metal mesh TCE as a function of grid pitch. FF denotes fill factor (f_F) [82].

Nanophotonic Phenomena

As previously mentioned, it is necessary to pattern metal mesh electrodes such that the linewidth of the constitute grid is submicron in dimension for many optoelectronic device applications and, in the case of photovoltaics and displays, subwavelength (<400nm) to ensure adequate transmission and haze. While the models introduced in the preceding section are able to reasonably predict performance in the micro- and macro-scales, simple geometric optics do not hold at the nano-scale. Efforts to elucidate underlying physics of general metal nano-mesh TCEs reveal an interesting and complex interaction of scattering, reflection, local surface plasmon resonances (LSPR) and surface plasmon polariton (SPP) phenomena which influence transmittance through the structure [66], [83].

Van de Groep et al. conducted an intensive study of nanophotonic phenomena of metal mesh grids in the subwavelength domain [71]. Their analysis concludes there exist

4 main scattering mechanisms which govern transmittance through a 2D network of Ag square grid pattern metal mesh electrode as depicted in Figure 9.

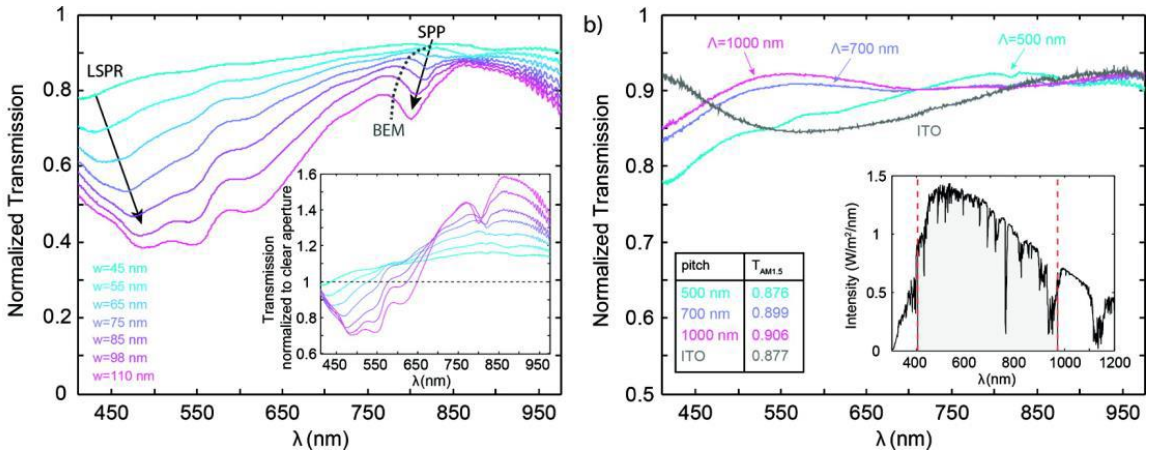

Figure 9: a) Spectral transmittance measurements through Ag grid with p=500nm & h=60nm for different linewidths (w). Insert shows same transmittance data normalized to glass reference; b) Spectral transmittance data through metal mesh networks with w=45nm & h=60 and 80nm thick ITO on glass [71]

First, Fano type constructive and destructive interference occurs between directly transmitted light in the space between lines and scattered light in the near-field of the grid lines due to the excitation of LSPR within the metal conductor. This scattering mechanism is shown in Figure 9a in the spectral range 450-550nm and blueshifts with increasing aspect ratio (AR) of the lines. Secondly, there is a step increase in transmittance at the wavelength roughly equal to the pitch of the grids (550nm). This behavior is attributed to the Rayleigh anomaly wherein the ±1 diffraction orders are directed in-plane of the grid and couple into scattering losses due to LSPR at wavelengths below the grid pitch. For wavelengths greater than the pitch, these same diffractions order point out of plane and contribute to increased transmittance, and hence, the greater than unity transmission observed in the insert in Figure 9a. Third, transmittance gradually decreases for wavelengths beyond 750nm due to the decay of the primary transverse electric (TE) mode in the metal-insulator-metal waveguide created by the grid lines and space between them. This type of loss is

exaggerated for thicker or taller grids since the TE mode becomes increasingly more evanescent with path length. Finally, strong absorption losses occur due to the excitation of SPP modes at the metal interface of the grid at wavelengths around 800nm. SPP are effectively red-shifted out of the spectrum of interest for increased grid pitch as seen in Figure 9b.

TRANSMISSION SIMULATIONS USING THE FDTD METHOD

Clearly, more sophisticated modeling than geometric optics is needed to accurately capture transmittance through nanoscale metal mesh electrodes. The finite-difference time domain (FDTD) method is a particularly well suited analysis tool for this type of problem [84], [85]. This section presents transmittance simulation setup and validation followed by a demonstration of a proposed preliminary procedure for optimizing metal mesh electrode geometry. This study exclusively analyzed square grid metal mesh electrodes due to their modeling simplicity and prevalence in reported literature.

Model Setup and Validation

The simulation model consists of a single unit lattice of metal grid lines embossed on a semi-infinite substrate centered at the origin and orthogonally oriented parallel to the axes on the XY plane. Figure 10 shows a schematic of the model configuration.

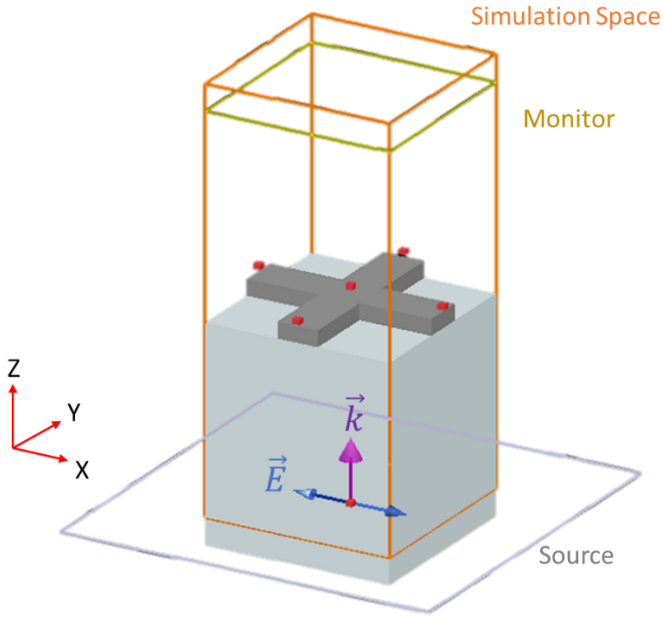

Figure 10: Schematic of FDTD simulation setup

Position of the light source is 700 nm below the substrate-air interface at normal incidence to the grid. The light source itself consists of a broad spectrum ($\lambda = 400$ - 700nm) plane wave with TE polarization along the x-direction. One power monitor located 700 nm above the surface of the grid lines monitors the Poynting vector of transmitted light. Anti-symmetric and symmetric boundary layer conditions in the x and y directions, respectively, exploit symmetry of the model in order to reduce simulation space and computational expense. Model setup employs perfectly matched layer (PML) boundary conditions in the z-directions, and all material optical constants are from Palik [86]. Conformal meshing is employed with default mesh resolution set to a minimum step size of 0.25nm for grids with pitch less than 10um. For geometries with pitch greater than 10um, the memory requirement to run the simulation and converge to a solution scales by the cubed power and exceeds available computational resources. Therefore, minimum mesh step size for

large pitch grids was set to one-tenth of the shortest wavelength of light in the most absorptive media i.e. metal.

Validation of the FDTD model entailed polling several fabricated metal mesh electrodes from reported literature and faithfully reconstructing the grid designs in the modeling software using closest matching material optical constants. Next, average and spectral transmittance results from simulation outputs were compared to corresponding measured values from literature. When selecting designs from literature for comparison, grids fabricated using high-resolution and repeatable methods were given preference in order to reduce the influence of defects and line-edge roughness from idealized geometry i.e. photolithography, NIL, e-beam lithography, EHD printing etc. Table 2 tabulates average transmittance data from literature against results from comparative simulations. Note, reported transmittance values have been normalized to air where appropriate in order for direct comparison. Values for simulated average transmittance (T_{Avg}) over the spectrum λ=400-700nm are within error of 5% of report data in most cases tested. Item 2 in Table 2 accounts for the largest error between simulation and actual transmittance, however, this may be due unique solution-processing wherein ordered Ag nanowires serve as grid lines instead of solid cross-section metal as assumed by the simulation.

Table 2: Reported average transmittance verse simulated average transmittance for various metal mesh designs

item	Reported Values	Simulation Result	Device Design						Ref.
	T_{Avg}	T_{Avg}	Linewidth [um]	Line height [um]	Pitch [um]	Material	Substrate	Packaging	
1	95%	94.3%	0.3	0.5	30	Al	Glass	Embossed	[57]
2	74%	63.0%	5	0.04	25	AgNW	Glass	Embossed	[59]
3	89%	90.0%	0.04	0.015	1.14	Pt ink	Glass	Embossed	[61]
4	68%	65.0%	0.67	0.015	2.87				
5	80%	74.9%	0.104	0.03	1	Ag	Glass	Embossed	[65]
6	78%	67.9%	0.119	0.03	1				
7	70%	62.6%	0.148	0.03	1				
8	75%	75.0%	0.065	0.05	0.5	Au	SiO2	Embossed	[66]
9	70%	75.0%	0.06	0.05	0.5				
10	57%	55.0%	0.1	0.05	0.5				
11	91%	89.0%	0.5	1.5	20	Au	Glass	Embossed	[67]
12	88%	84.3%	0.15	0.06	3.2	Ag	Glass	Embossed	[70]
13	76%	72.6%	0.15	0.06	1.6				
14	63%	59.6%	0.15	0.06	1				
15	87%	90.1%	0.045	0.06	1	Ag	SiO2	Embossed	[71]
16	86%	86.0%	0.045	0.06	0.7				

Spectral transmittance is also compared to reported values from fabricated metal meshes to analyze the ability of the simulation to capture nanophotonic phenomena. Figure 11 shows transmittance spectra for Ag metal mesh grids on glass substrates for three different pitch values and FDTD simulated transmittance for equivalent model designs. This simulation model is able to accurately reproduce optical performance of real-life metal nano-mesh grids with only minor error. Again, discrepancies between reported data and simulation results are mainly an artifact of manufacturing defects in as-fabricated grids which is not captured in modeling i.e. surface roughness and rounding of edges at line intersections. Based on these results, this simulation model shows good agreement with empirical data and is assumed validated.

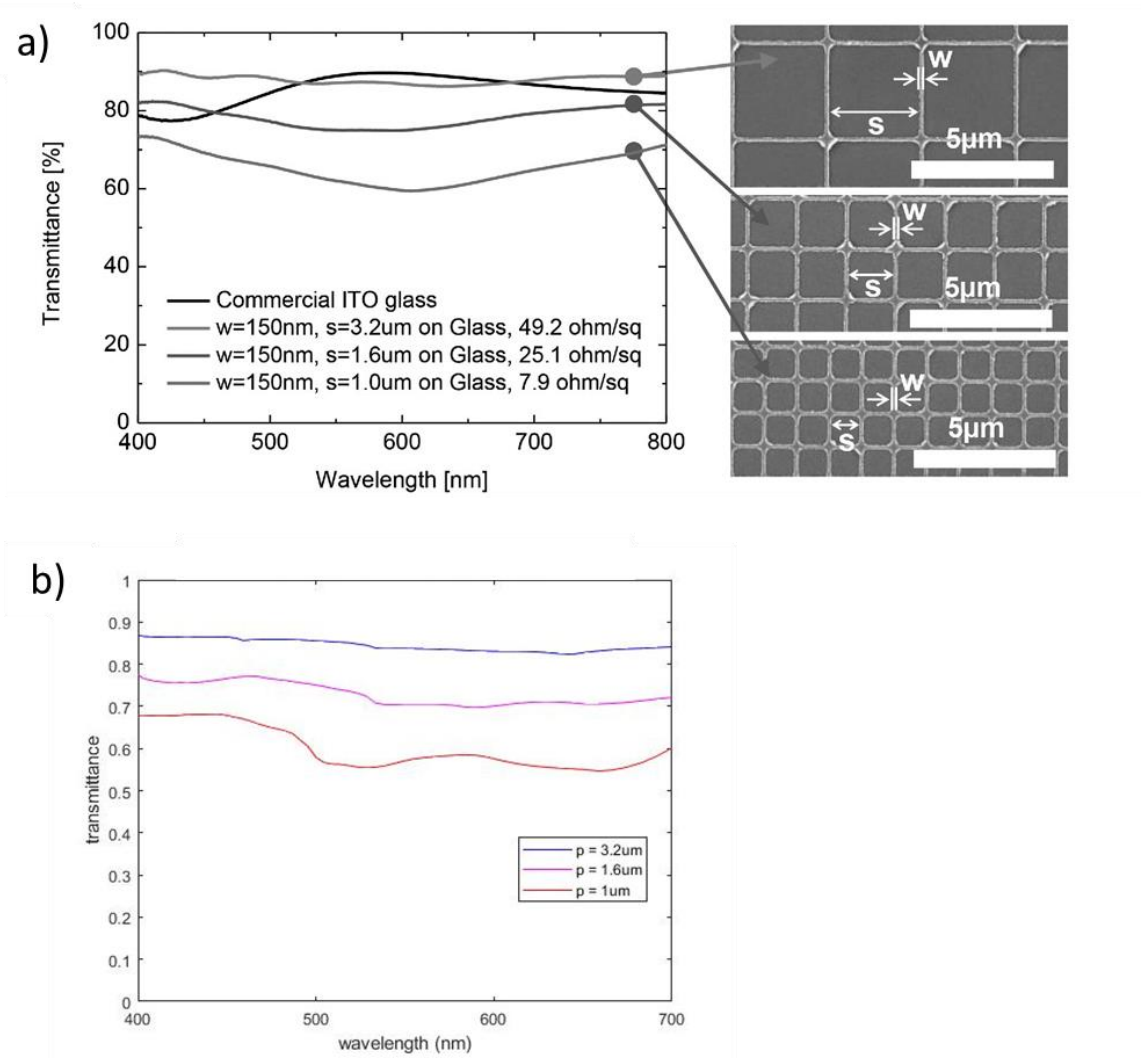

Figure 11: a) Transmittance spectra and FE-SEM images of 60nm thick Ag nano-mesh patterns [70]; b) Simulated spectral transmittance for equivalent metal mesh structures

Preliminary Design Optimization Procedure

This section introduces a simple optimization procedure to identify an optimal mesh geometry for a particular application i.e. $T_{500nm} - R_S$ tradeoff. The algorithm first utilizes geometric approximations to efficiently and quickly find an ideal mesh configuration, and then, FDTD transmittance analysis based on this output provides a rigorous study of the optical behavior of the metal mesh electrode. The optimization is a single-objective, multi-

variant, nonlinearly constrained problem which employs a gradient-based sequential quadratic programming (SQP) algorithm to minimize the objective function. The objective function in this case is a commonly used Figure of Merit term for TCEs based on the relationship between DC conductivity (σ_{dc}) and optical conductivity at 550nm wavelength (σ_{opt}) defined by Equation 10 [6], [87].

$$\frac{\sigma_{dc}}{\sigma_{opt}} = \frac{188.5}{R_s\left(T_{550nm}^{-\frac{1}{2}} - 1\right)}$$

Equation 10: Figure of Merit for TCEs as a function of sheet resistance and transmittance at 550nm wavelength

Design variable inputs include linewidth (w), thickness or height (h) and grid pitch (p). Nonlinear constraints include minimum acceptable transmittance, sheet resistance and aspect ratio (AR) of grid line. Resolution limit of common fabrication techniques and target application requirements inform values for bounds and constraints.

For demonstration purposes, consider the case of an ideal Cu square metal nano-mesh embossed on a SiO_2 substrate as a TCE for display applications. Transmittance and sheet resistance are found by Equation 8 and Equation 6, respectively, where resistively is equal to bulk Cu for simplicity. Table 3 tabulates design variable bounds and constraints employed to identify two candidate designs.

Table 3: Optimization criteria for Cu metal mesh example

	Test Case 1			Test Case 2		
	Linewidth	Line Height	Pitch	Linewidth	Line Height	Pitch
Lower Bound	25nm	0	0	25nm	0	0
Upper Bound	150nm	Inf	Inf	50nm	Inf	Inf
Transmittance Constraint	≥90%			≥90%		
Sheet Resistance Constraint	≤5 Ω/sq.			≤5 Ω/sq.		
Aspect Ratio Constraint	≤3			≤5		

Table 4 summarizes the output of the optimization algorithm including optimum geometry and performance metrics calculated by geometric approximations. In both test cases, the algorithm maximizes linewidth and aspect ratio within the specified bounds/constraints. The tendency to maximize AR corresponds to findings by Kang et al. which state increasing AR benefits sheet resistance while minimally affecting transmittance [49]. Furthermore, the optimization settles to a pitch-to-linewidth ratio of 100 or pitch roughly two orders of magnitude greater than linewidth for optimum transmittance.

Table 4: Optimization results for test case 1 and 2 with corresponding transmittance and sheet resistance values calculated by geometric approximations

	W*	H*	P*	AR	T_{550nm}	R_S
Test Case 1	150nm	450nm	14um	3	94%	3.5
Test Case 2	50nm	225nm	3um	4.5	93%	4.6

Figure 12 shows the transmittance spectra of optimized geometry for test case 1 and 2. Due to the micron scale pitch of the both grids, SPP absorption losses do not appear in the wavelengths simulated. Furthermore, the large pitch-to-linewidth ratio removes transmittance losses associated with Rayleigh's anomaly and decay of the primary TM mode through the aperture of the grid. The relatively small oscillations in the transmittance spectra for both test cases are likely due to interference caused by excitations of LSPR in

the grid lines. However, light is not able to effectively couple in LSPR modes due to the large AR resulting in only a relatively small drop in transmission. The difference in AR is the reason for the larger amplitude of LSPR induced oscillations in test case 1 verses test case 2. Note, the presence of LSPR in test case 2 resulting in average transmittance of about 89.5% or 3% lower than transmittance based on Equation 8.

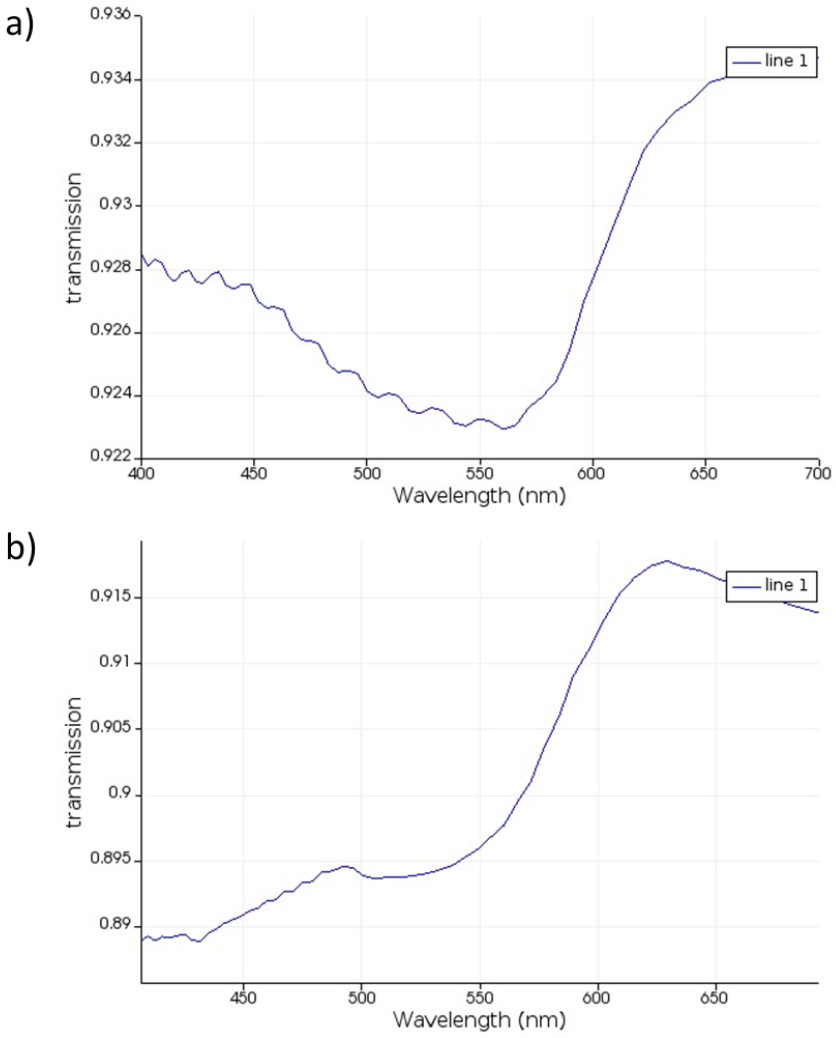

Figure 12: a) Simulated transmittance spectra for test case 1; b) Transmittances spectra for test case 2

While this is a simplified case, the optimization procedure presented is able to identify optimal mesh geometries which satisfy the desired performance specifications, and demonstrates the only known rapid yet rigorous optimization method for designing metal mesh grids for any arbitrary application to the author's best knowledge.

Chapter 3: R2R Nanofabrication Process Development & Experimentation

This section chronicles experimental work and learnings towards development of a R2R compatible fabrication process for realizing Cu metal nano-mesh TCEs on flexible substrates. First, we describe the process flow schemes studied and methodology used to achieve the objectives of this research. Then, subsequent sections review major process steps in detail and outcomes from experimentation on electroless Cu metallization, glancing angle deposition (GLAD) and residual layer etching by linear ion source (LIS) plasma treatment.

PROCESS OPTION SELECTION

A multitude of possible processes flows may yield metal mesh geometries with nanoscale resolution in a R2R fashion i.e. direct printing [61], hybrid printing [60], [64], transfer printing [56], lift-off [57], [62], [65] etc. However, many of these processes struggle in terms of either scalability or low-yield. For example, lift-off entails selective removal of one material usually by chemically etching a sacrificial underlying layer when immersed in etchant, but lifted-off material tends to redeposit elsewhere on the surface of the substrate resulting in defects and poor-quality devices. In order to identify the best suited process scheme for the goals of this research, a systematic comparison of different process flows and their individual steps is required. Figure 13 provides a concise graphical summary of candidate process flows considered for this study and risks inherent in each individual step which comprise them. Unit steps shaded in red denote high risk, yellow denotes relatively-low risk and items shaded in black do not pose significant risk. Risk is defined in terms technology research and development uncertainty or likelihood of unsuccessful integration into existing commercial systems based on literature review, professional expertise and best-practices in industry. Note, this section provides reasoning

behind the decision of a fabrication process, and ensuring sections discuss details of relevant process steps.

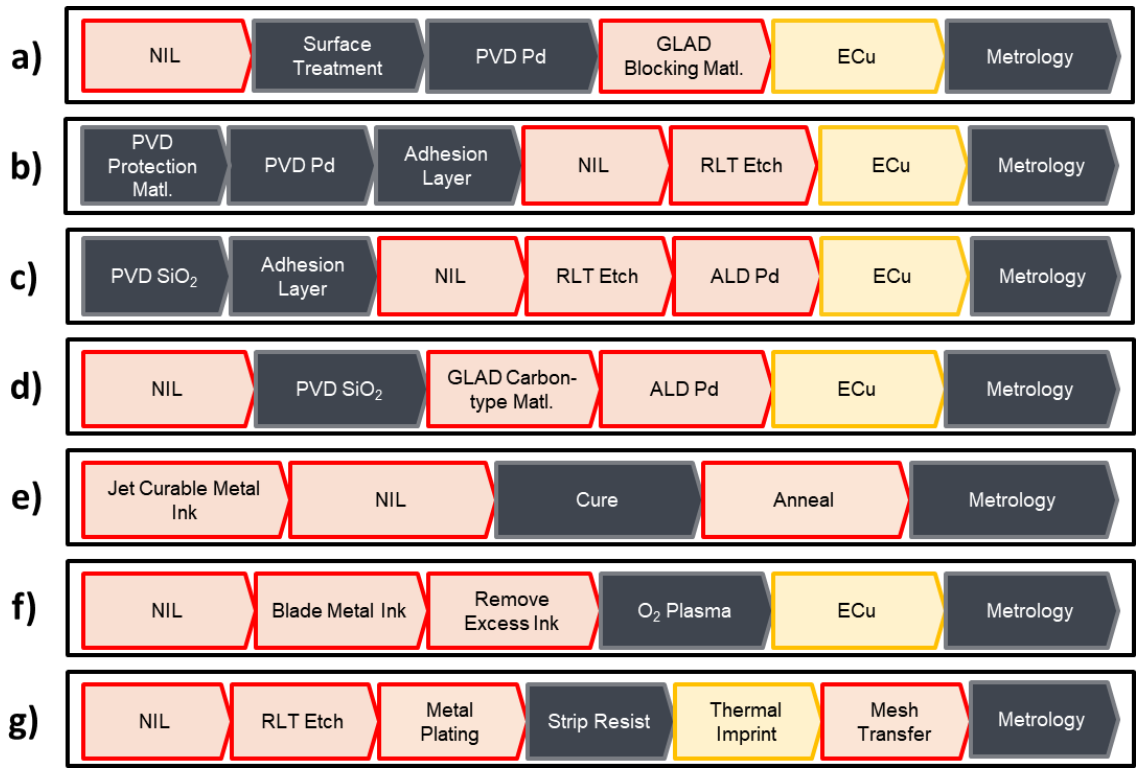

Figure 13: Graphical summary of candidate process flows with constitute unit steps. a) Glancing angle deposition flow; b) Etch-expose flow; c) Selective ALD flow; d) GLAD/ALD combination flow; e) Directing printing flow; f) Hybrid blading conductive ink flow; g) Transfer printing flow.

All processes in the figure above are referred to by their defining unit step as is common practice. NIL is the patterning method of choice for all candidate process options due to its advantages over photolithography mentioned earlier. However, high-fidelity R2R NIL processing based on the J-FIL method is still in the early stages of research. Therefore, the NIL pattern step is denoted as high-risk, and negatively affects the attractiveness of all options evenly.

Many of the candidate processes also employ electroless Cu metallization (ECu) in order to grow the conductor within the grid lines of metal mesh electrode. ECu offers a low

temperature vacuum-free solution-based processing method to selectively deposit Cu without the need of a conductive substrate and external current source as in the case of Cu electroplating. Furthermore, since plating rate is not dependent on current distribution within the substrate, ECu deposits uniformly across the entire face of an activated substrate once the metal layer is contiguous. ECu is a well-studied technique commonly used for through-hole plating for printed circuit boards (PCBs), and can be adapted for R2R processing relatively easily due to its compatibility with plastic substrates. For these reasons, ECu plating is considered an ideal process for selectively metallizing flexible substrates in this research. However, in the case of subwavelength nano-mesh TCEs, the critical feature dimensions of extremely thin gridlines (<50 nm) are similar in order of magnitude as the nominal grain size of electroless grown Cu and may result in a poor-quality, low-conductivity films [88]. Thus, the ECu step possesses intrinsic risk and necessitates morphology and electrical characterization.

Comparison of all options in Figure 13 reveals Glancing Angle Deposition (GLAD) and Etch process options (Figure 13a and b, respectively) possess the least inherent technology risk. As a result, this thesis focuses on using these two candidate process flow schemes to accomplish said research objective defined in section 1.3. The GLAD process flow consists of 6 unit steps including patterning (J-FIL), surface cleaning treatment, deposition of Pd to seed ECu deposition, GLAD of blocking oxide, ECu and metrology. The GLAD operation is essential for selective ECu and is a major contributor of risk in this candidate process as its feasibility is unknown and requires investigation. The etch process scheme requires 7 unit steps including deposition of a protective material layer to isolate the bare PC substrate, PVD of Pd, dispensing of an adhesion promoter, patterning by NIL, residual layer thickness (RLT) etch or descum, ECu plating and metrology. The RLT or expose etch step employs a novel R2R ion milling process and is critical for selective ECu.

Thus, RLT etch is a main source of risk in this approach due to its novelty and must be validated.

METHODOLOGY

The methodology of this process development study adopts a pragmatic framework consisting of wafer-scale experimentation, metrology /characterization and process integration illustrated by Figure 14.

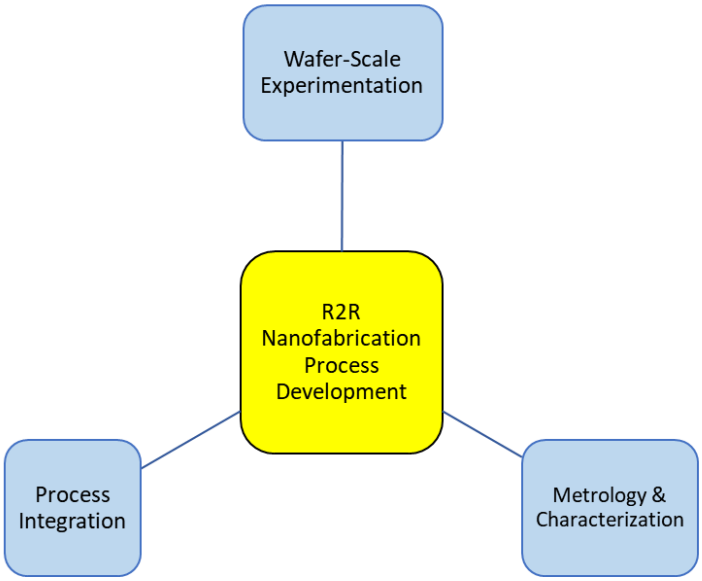

Figure 14: Framework of R2R nanofabrication process development

In the experimentation branch of this framework, individual unit process steps are evaluated on feasibility and compatibility with R2R processing by first qualifying them on wafer-scale with flexible polycarbonate (PC) substrates. This approach has a two-fold benefit: 1) existing semiconductor wafer-scale equipment can provide the capability to evaluate individual process steps such as material deposition i.e. magnetron sputter, electron beam evaporation and spin coating; 2) wafer-scale processing allows for rapid prototyping and fine tuning of process parameters in highly isolated environments. To

serve flexible device applications, PC wafers with nominal thickness of 500 μm are the substrates selected to support the Cu metal nano-mesh TCE in this research. PC is highly transparent with a low refractive index close to imprint resist (n_{PC}=~1.59 @ 550nm) [89], and PC is proven to be compatible with J-FIL technology unlike polyethylene terephthalate (PET) [90]. Furthermore, the surface of sourced PC wafers is highly planer and considered negligible during experimentation.

The imprint template used in this research to pattern metal mesh electrodes contains two separate 15x15mm fields which create trench features of rectangular cross-section and 100 nm in depth in polymerized imprint resist in a 2D square grid pattern. Trenches allow for an embedded metal grid which is preferred over an embossed structure due to the advantages mentioned in Chapter 1. Figure 15 shows a diagram of the patterned imprint resist on a substrate after successful pattern transfer. Note the residual imprint resist thickness (RLT) at the bottom of the trenches.

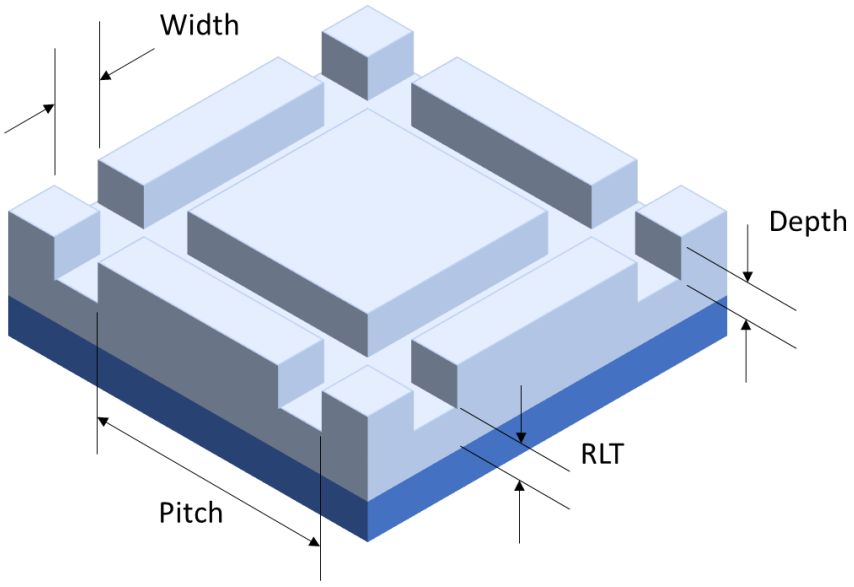

Figure 15: Diagram of trench pattern in imprint resist representative of patterns used in wafer-scale experimentation. The dark blue layer here represents the substrate (PC or glass etc.)

The finer geometry of the two patterned fields imprints 300 nm wide trenches with pitch of 3 μm (fine grid), and the coarser geometry imprints 500 nm wide trenches with pitch of 5 μm (coarse grid). The area surrounding the patterned fields contains no features and creates a planar resist layer of constant thickness. The simple subwavelength geometries of these template patterns are arbitrary selected for the primary purpose of evaluating fabrication processes for metal nano-mesh electrodes, and are not optimized for any particular application.

Next, nanoscale metrology and functional characterization inform understanding of process behavior and material properties. Film thickness measurements entailed optical profilometry (Dektak 150) and ellipsometry (J.A. Woollam M-2000). Imaging included both scanning electron (SEM Zeiss Neon 40) and optical microscopy. Electrical characterization consists of sheet resistance measurements using a Guardian SRM-232 surface resistivity meter (4-point probe). Optical characterization involves measuring of transmittance spectra through prepared electrode films using an Ocean Optics spectrometer and a custom imaging spectrophotometer setup for transmittance measurements [91].

Finally, the process integration branch entails combining all R2R compatible unit steps in sequential order to realize a Cu metal mesh on flexible PC substrates. This front is tailored for the modules and capabilities of the Emerson & Renwick GENESIS series R2R pilot platform which contains inline sputtering, e-beam evaporation and a linear ion source (LIS) [92]. The following sections systematically describe major learning outcomes of process development efforts gained by this methodology framework.

ELECTROLESS COPPER METALLIZATION

Electroless Cu (ECu) deposition is a redox reaction consisting of an oxidation reaction of a reducing agent and a reduction reaction of Cu ions from solution onto a catalytically activated surface. While ECu plating is an energetically favorable process, it

requires a catalyst species deposited on a surface in order to reduce the activation energy of the reaction and initiate spontaneous decomposition of Cu. Therefore, ECu deposits nucleate at the sites of catalytic seed material, and films selectively grow on activated surfaces only where there is exposed catalyst to the solution.

The basic chemical reaction of ECu plating solutions based on formaldehyde as the reducing agent and ethylenediaminetetraacetic (EDTA) as the complexing agent is described by Equation 11 [93], [94].

$$[CuEDTA]^{2-} + 2HCHO + 4OH^{-} \rightarrow Cu + 2HCOO^{-} + 2H_2O + H_2 + EDTA^{4-}$$

Equation 11: Overall reaction of electroless Cu deposition

Plating rate of ECu is largely a function of species concentrations, pH levels and bath temperature. Increased plating rate is accompanied by increased production of hydrogen which tends to create pressurized voids containing hydrogen gas in the Cu film. The presence of voids in the film results in higher dislocation density and resistivity of the film. Surfactants can be added to the ECu solution to help control plating rate and prevent inclusion of hydrogen in Cu deposits. Pd is the catalyst of choice in most practical applications and in this research. Note, the effectiveness of the catalyst layer is highly susceptible to oxidation and contamination.

The electroless Cu solution used in this work is formaldehyde based and is sourced from Transene Company, INC. (PC Electroless Copper). Figure 16 provides a schematic of the process steps this research uses to perform electroless Cu deposition on an arbitrary substrate. First, sputtering of a Pd seed layer catalytically activates the substrate's surface which is followed by electroless Cu deposition by immersion of the Pd coated sample in plating solution. Sputtering is selected as the method of coating due to its proven compatibility with R2R fabrication and reduced process complexity compared to wet

solution-based surface activation techniques. A hot plate and water bath maintain plating solution temperature between 35 – 40°C during testing, and plating was performed according to the manufacturer's directions. At these bath conditions, the manufacture quoted nominal plating rate of the sourced ECu solution is 0.2 mil/hour or about 85 nm/min. Preparation of virgin plating solution occurred periodically during experimentation to reduce influence of particle contaminants in solution after multiple plating runs. Immediately after ECu plating, all samples are purged in a DI water bath then dried by high-velocity house N_2 gas.

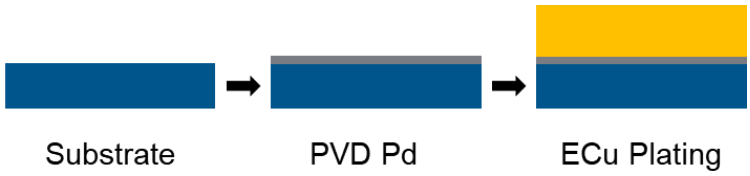

Figure 16: Schematic of dry surface activation process for electroless Cu plating

To assess the appropriateness of ECu metallization in a R2R nanofabrication process for metal nano-mesh TCEs, this study investigated the quality of ECu films grown with different Pd seed layer thicknesses. The investigation then made efforts to understand the growth of ECu films and quantified the electrical properties of ECu grown thin films.

Palladium Seed Layer Deposition and Film Quality

The minimum Pd seed layer thickness required to reliably deposit ECu films was tested by sputtering 0.5 nm, 1 nm, 2 nm and 3nm thick layers of Pd catalyst on bare PC wafers. Coupons cut from the coated PC wafers were subsequently immersed in plating solution for 2 min. Visual inspection of the sample surfaces confirmed the presence of ECu deposits and assessed plating quality. Figure 17 shows experimental results of ECu plating for each Pd seed layer thickness tested.

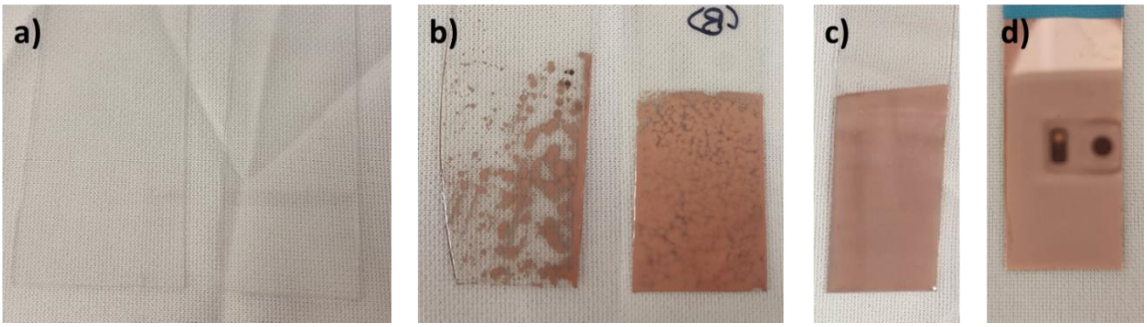

Figure 17: Photographs of ECu film deposition results on bare PC substrate coupons with a) 0.5 nm, b) 1 nm, c) 2nm and d) 3 nm thick Pd seed layers after immersion in plating solution for 2 min. Note, the dark spots in image d) are due to the reflection of the camera off of the film surface

For samples with Pd seed layer thicknesses of 0.5 nm, ECu plating did not initiate and completely failed to deposit a Cu film on the substrate surface. At Pd seed thickness of 1 nm, ECu deposition did initiate, however, film quality was inconsistent between similar samples, and plating occurred in a discontinuous fashion at random locations on the substrate surface as shown in Figure 17b. This highly nonuniform nature of ECu plating suggests that the Pd seed layer does not form a continuous film at 1 nm thickness, but instead, is comprised of isolated islands of catalyst where Cu ions are able to nucleate and initiate growth. Pd seed layer thicknesses greater than 2 nm repeatedly produced uniform, continuous ECu films with a highly reflective surface finish after 2 min immersion time in plating solution. Based on these results, all further testing in this work adopt a baseline minimum Pd seed layer thickness of 3 nm to ensure reliable ECu plating.

A peel test using standard scotch tape tested the adhesion of the Pd seed layer and plated ECu films to PC substrates as shown in Figure 18. 3 nm thick sputtered Pd seed layer remained virtually unaffected by the application and removal of tape which suggests excellent adhesion to the PC substrate. The resilience of the seed layer in the adhesion peel test may be explained in part as a result of the sputtering deposition technique which

embeds Pd molecules into PC mechanically fixing them to the substrate surface. Similarly, ECu deposited films exhibited strong adhesion to the PC substrate.

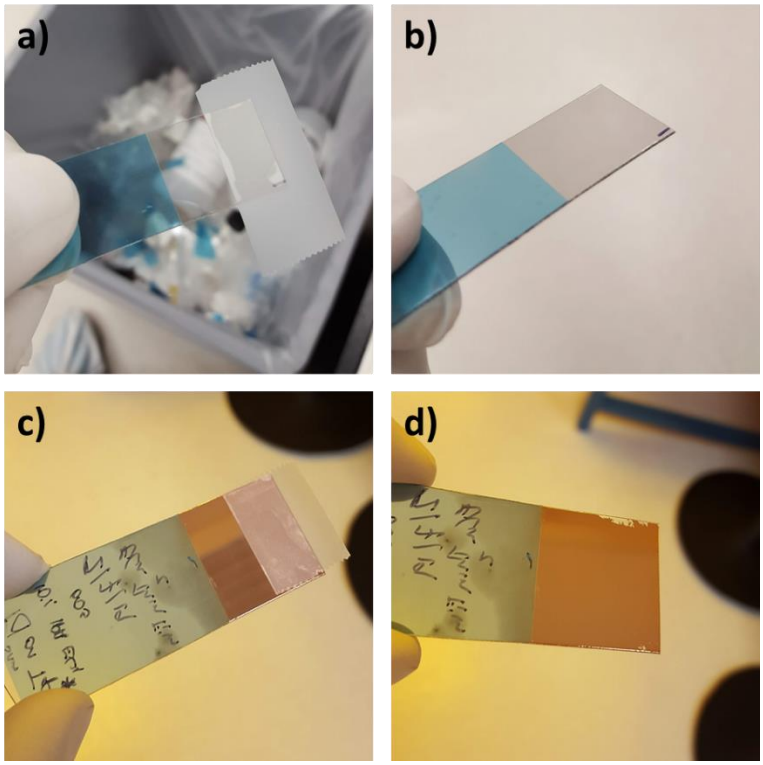

Figure 18: Results of Pd seed layer and ECu film adhesion to PC substrates experiments. a) Placing tape on top of 3nm Pd seed layer on PC & b) Pd seed layer on top of PC after removal of tape. The Pd layer stays intact; c) Application of tape on top of 1 min ECu plated PC surface on top of 3nm Pd seed layer & d) The ECu plated film on top of 3nm Pd layer on PC after removal of tape. The Ecu layer is virtually intact.

Next, the minimal Pd thickness required to form a uniform seed layer was empirically determined by sputtering 5 nm, 10 nm and 20 nm thick Pd layers on bare PC wafers then spin coating a liquid adhesion promoting polymer containing strong PC solvents onto the coated wafer. By visually observing whether or not the PC solvent is able to reach the surface of underlying PC substrate and proceed to cause immediate chemical dissolution, the uniformity of the Pd layer could be ascertained without time-consuming

SEM imaging. In other words, the Pd layer is assumed to be continuous at a particular thickness if no chemical attach is observed on the PC substrate after application of the adhesion promoting polymeric material. Figure 19 is a picture of the three PC wafers tested after sputtering of Pd and spin coating of the adhesion material.

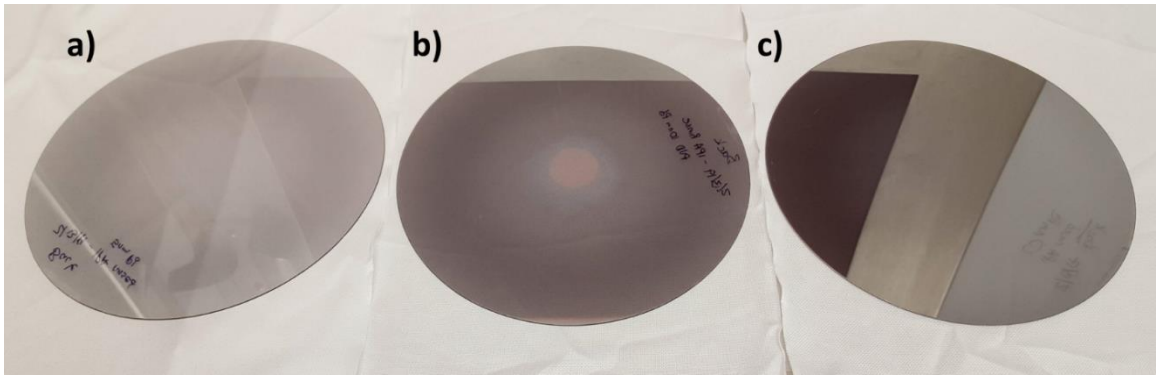

Figure 19: Results of minimum uniform Pd layer thickness experiment. a) 5nm Pd thickness wafer, b) 10nm Pd thickness wafer, c) 20 nm Pd thickness wafer. All wafers have adhesion promoter solution spin coated on them. Note, reflections off the surface of wafers should be ignored

In both the 5 nm and 10 nm Pd thickness cases, the solvent in the adhesion promoter solution is able to reach the PC substrate through the metal layer and chemically attack the surface. This is observable in the Figure 19 a & b above as the lighter white areas in the center of the wafers with increased opaqueness. In contrast, the PC wafer coated with a 20 nm thick layer of Pd shows no such signs of chemical attack and serves as evidence for the formation of uniform continuous metal layer. Note, the chemical attack is highly localized near the center of the wafers in the 5 nm and 10 nm Pd thickness cases since droplets of adhesion promoter solution are first dispensed over this location and collect as a pool for a few seconds before the spin cycle is engaged. Figure 20 below shows an SEM image of 20 nm thick Pd layer on PC before the application of the adhesion promoter solution and confirms uniformity. The dark line in the SEM image is the only feature found which

provided contrast needed to focus the lens, and the area around the line is characteristic of the high planarity of the film.

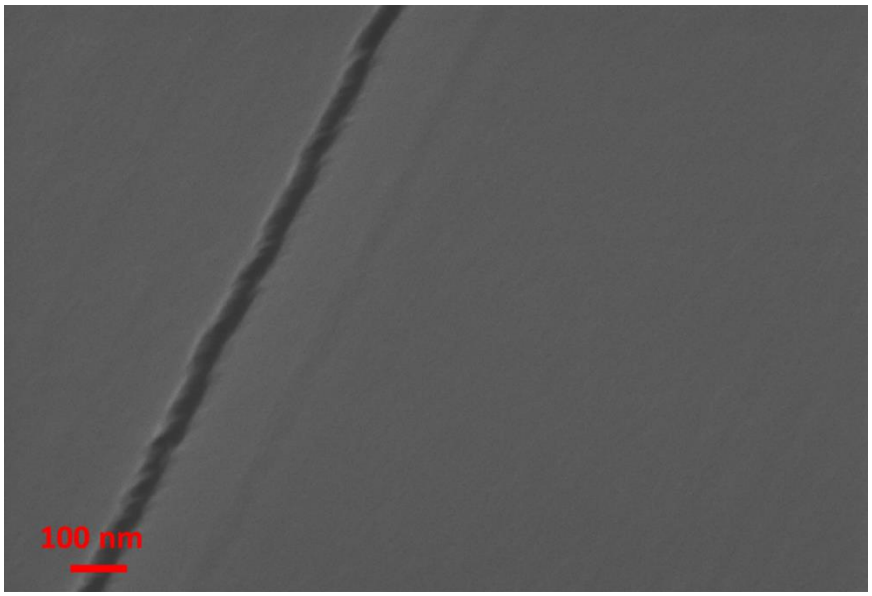

Figure 20: Top down SEM image of 20 nm thick Pd layer sputtered on PC

Microstructure Evolution and Growth of Electroless Cu Films

Grain sizes of electroless deposited Cu films differ from bulk Cu, and required characterization in order to determine the feasibility of this plating technique in a R2R fabrication process for subwavelength metal nano-mesh TCEs To better understand growth mechanisms of electroless Cu films, an extensive morphological study is presented which investigated ECu film development as a function of immersion time in plating solution and Pd seed layer thickness.

Figure 21 shows SEM images of ECu deposited films on PC substrates for different immersion times and Pd seed layer thicknesses. Cu particles first appear on PC substrates seeded with 3 nm of Pd within roughly 30s of immersion in the plating solution. The Cu particles are initially arranged in distinct bands of a high-density Cu crystallites and in large clusters of aggregated grains. It is theorized Pd particles in the underlying 3 nm thick seed

layer exhibits this structure post sputter coating, and therefore, Cu grains also form a similar pattern since they preferentially deposit around the Pd catalyst particles. As immersion time increases, the bands of high-density Cu grains and the blob-like clusters expand laterally and begin to merge with one another. Beyond immersion time of 120s in the plating solution, distinct bands and large clusters of Cu grains vanish having merged to form a continuous film of consistent grain density.

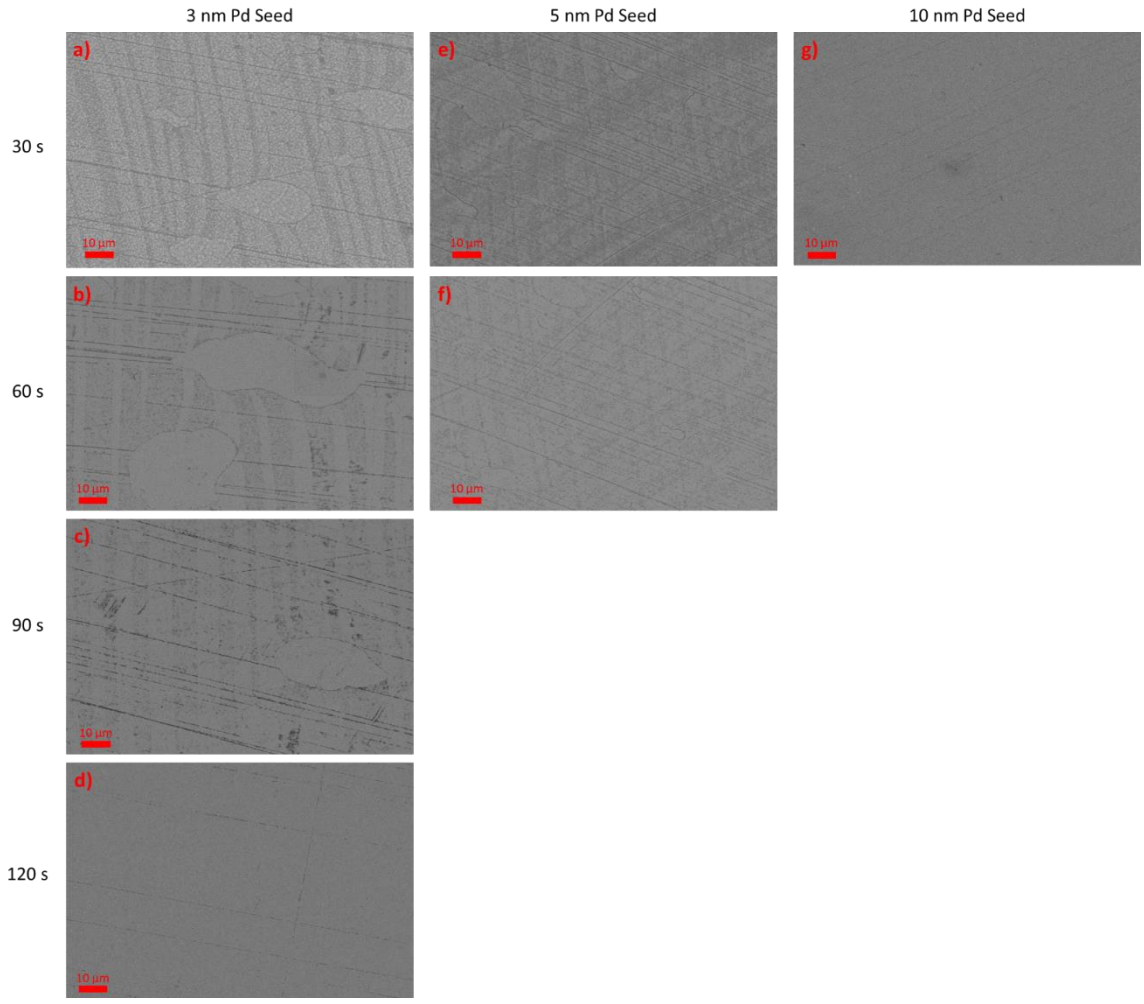

Figure 21: SEM images of ECu film deposits for different plating times and Pd seed layer thicknesses. 3 nm Pd seed for a) 30s, b) 60s, c) 90s and d) 120s. 5nm Pd seed for e) 30s and f) 60s. 10 nm Pd seed for g) 30s

PC substrates coated with 5 nm thick Pd seed layers exhibit a similar microstructure evolution, but coalescences of bands and clusters occurs at a shorter immersion time of 60s. For PC substrates seeded with 10 nm thick Pd layer or greater, bands and clusters of Cu grains are not observed. A continuous ECu film develops within 30s of immersion time in the plating bath due to the increased number of Pd catalyst sites.

Essentially, the spacing between neighboring Pd islands decreases for thicker seed layers, so the Cu particles which agglomerate at these Pd islands nucleate in closer vicinity

to each other. Hence, less plating time is required for the Cu particles to grow and impinge on each other to form a continuous film. To better understand electroless Cu film growth, consider the diagram in Figure 22 below.

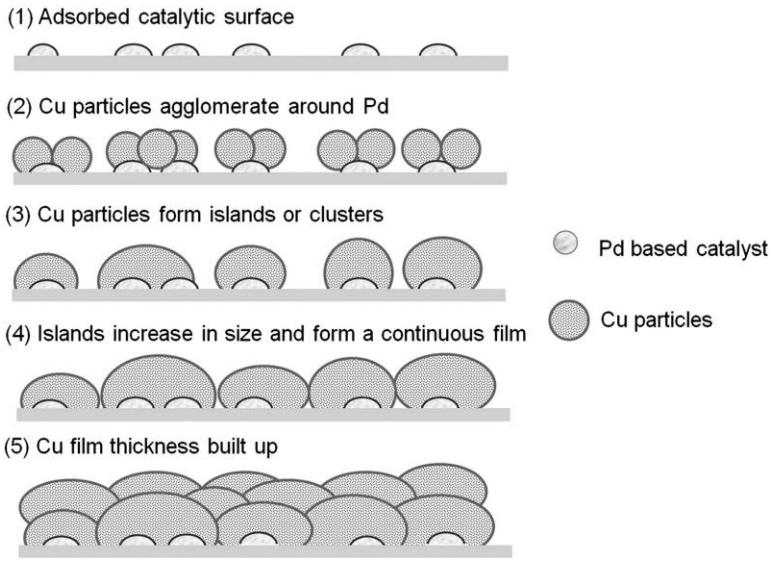

Figure 22: Diagram of Cu film growth with Pd catalyst surface activation [88]

Cu grain size of electroless deposited films is observed to be independent of both plating time (<3 min) and Pd seed layer thickness. Figure 23 shows high-magnification SEM images of ECu films for different immersion times and Pd seed thicknesses. Average Cu grain size of all samples tests is 43.8 nm with a relatively narrow sample standard deviation of 19.8 nm. These observations agree well with data in literature for electroless plated Cu films with thickness below 150 nm [88]. Based on data presented in this section, electroless Cu plating is confirmed to produce sufficiently small Cu grains for metallizing subwavelength metal nano-mesh TCEs.

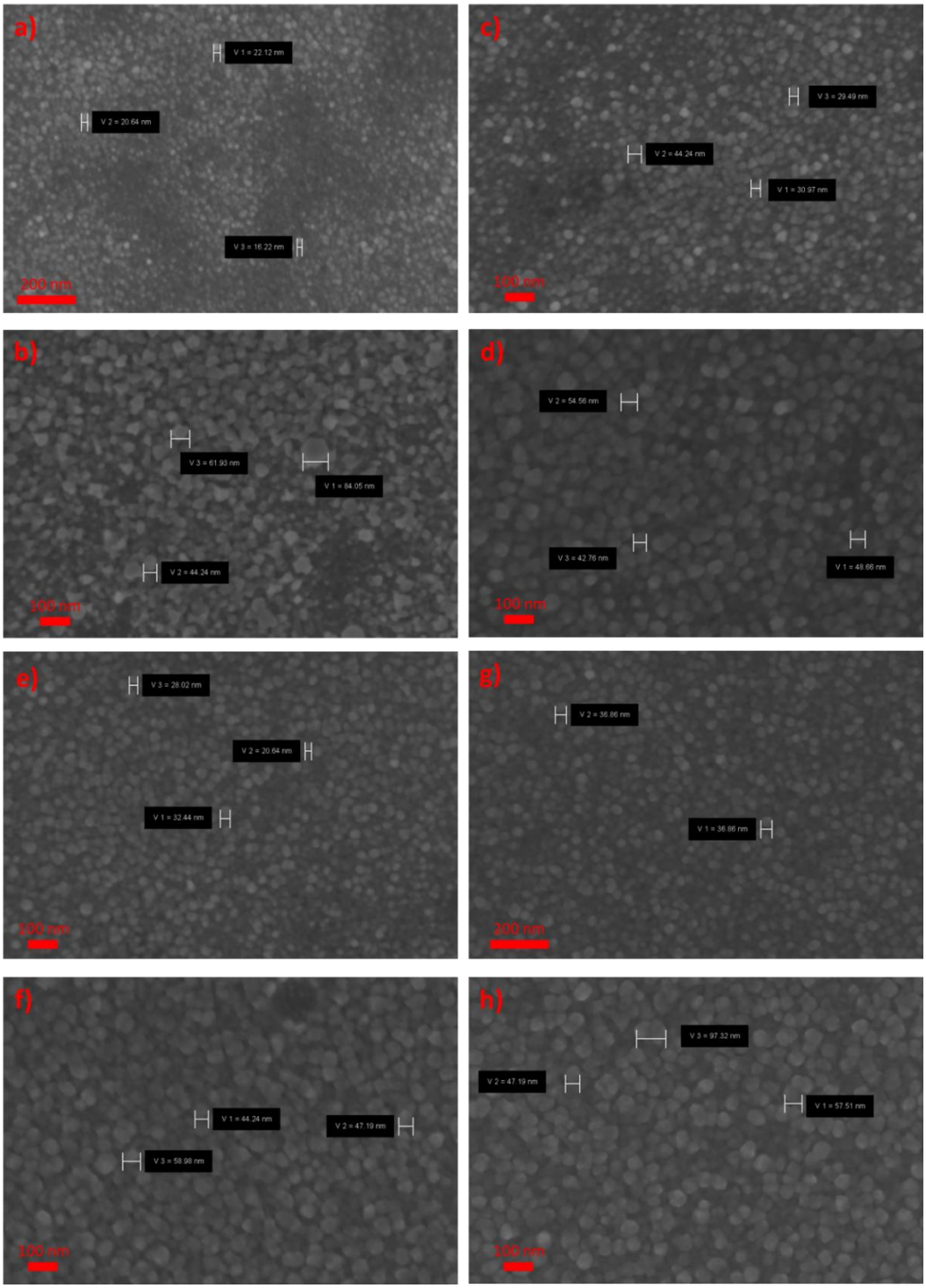

Figure 23: SEM images of ECu films for different Pd seed layer thicknesses and immersion times in plating solution. 3 nm Pd seed thickness immersed for a) 30s and b) 90s. 5 nm Pd for c) 30s and d) 90s. 10 nm Pd for e) 30s and f) 90s. 20 nm Pd for g) 30s and h) 90s

Figure 24 shows step height of ECu deposited films seeded with a 3 nm thick layer of Pd on bare PC as a function of immersion time in plating solution. Cu particles rapidly nucleate within the initial 30s of immersion similar to the SEM micrography in Figure 21a. Next, vertical plating rate slows down during the Cu granular merging phase between 30s to 90s immersion in solution. Finally, uniform film growth proceeds at a constant rate of ~80 nm/min beyond 90s of immersion in the plating solution. The measured deposition rate matches manufacturer specifications, and is assumed to be the nominal plating rate for further characterization due to the difficulty of film thickness measurements on PC substrates.

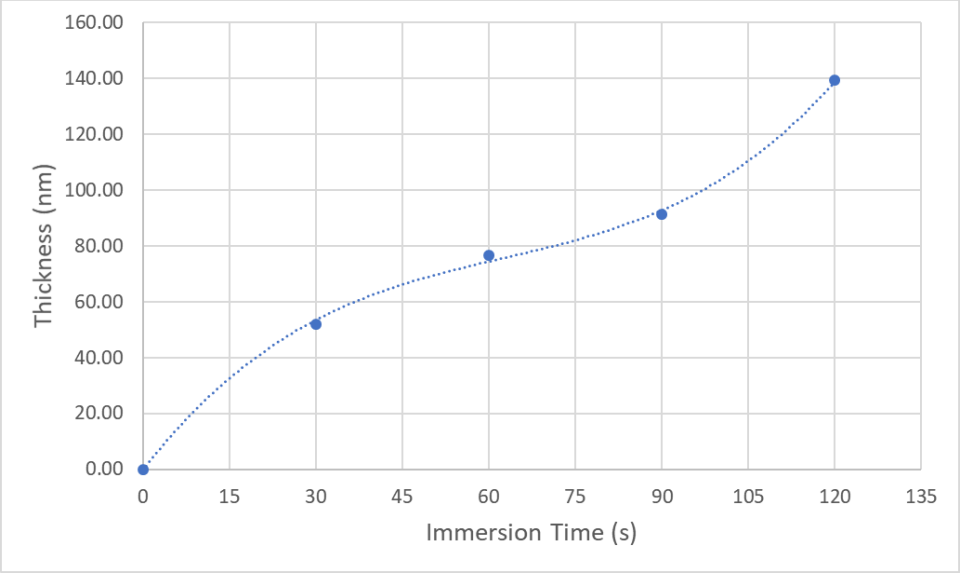

Figure 24: Thickness of ECu deposited films with 3 nm Pd seed layer thickness on bare PC substrates as a function of immersion time in plating solution

Electrical Characterization of Electroless Cu Films

Electrical characterization of ECu films included measuring sheet resistance of deposited films for various immersion times in plating solution and calculating resistivity of film by assuming the nominal plating rate identified in the preceding section. Figure 25 presents sheet resistance of ECu deposited films as a function of immersion time for seed

layer thicknesses of 3 nm, 5 nm, 10 nm and 20 nm. Sheet resistance is initially large but rapidly drops between 30s to 90s of immersion in the plating solution for all seed layer thicknesses. Sheet resistances beyond 90s of immersion time asymptotically level out to a common value below 2 Ω/sq. for all seed layer thickness. The sharp decrease in sheet resistance corresponds to the granular merging phase of discontinuous islands of Cu particles on the substrate surface as noted earlier. As Cu islands develop and coalesce for longer immersion times, film resistance drops due to increasing number of contacts between individual grains allowing for a greater number of electrical pathways and an increase in electron mobility [95].

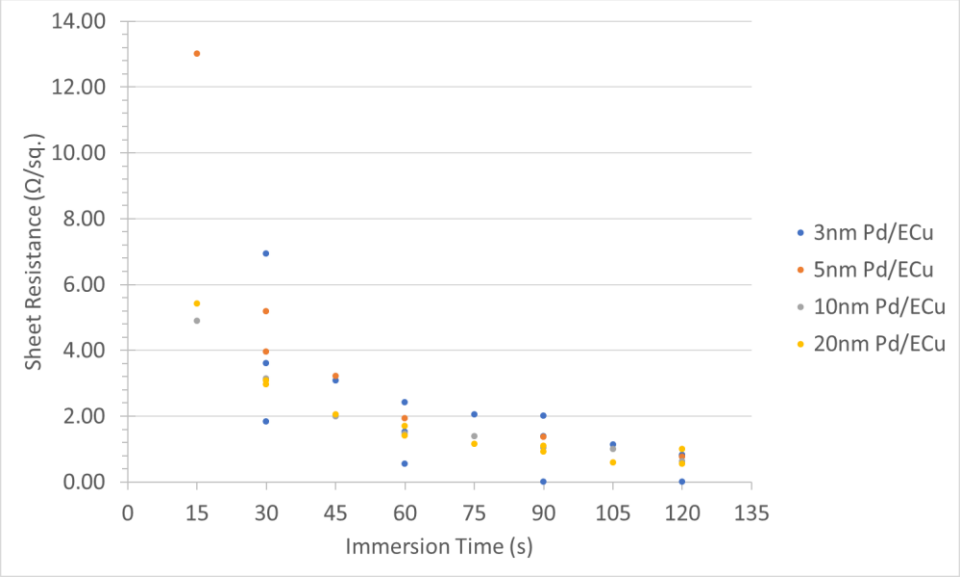

Figure 25: Sheet resistance of ECu films as a function of immersion time in plating solution for various Pd seed layer thicknesses

Figure 26 shows resistivity of ECu deposited films with 3 nm thick Pd seed layers solved for by Equation 1 as a function of immersion time assuming the nominal plating rate. Resistivity exhibits a large variance for immersion times shorter than 60s as expected due to the disperse stochastic nucleation of Cu particles on the substrate surface prior to coalescence. Resistivity eventually converges to a value of ~13 μΩ cm. at immersion time

of 120s which is roughly 8 times greater than resistivity of bulk Cu. This resistivity of electroless Cu matches findings by Radoeva et al. [96].

Substituting the resistivity value of 13 μΩ cm into Equation 7 and solving for the fine and coarse grid template yields predicted R_S values of 6.84 Ω/sq. for both metal mesh geometries i.e. fill factors are equivalent in both cases. These metal mesh sheet resistance values are within the required performance specifications for TCEs in display applications, and therefore, confirm ECu plating is capable of producing sufficiently high-quality Cu films for use in proposed nanofabrication processes.

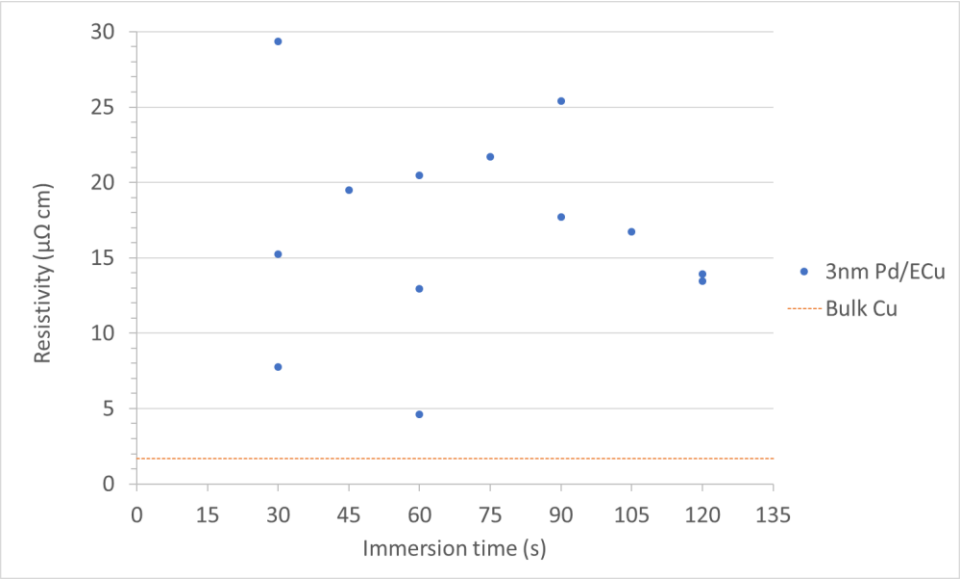

Figure 26: Resistivity of ECu deposited films with 3 nm Pd seed thickness as a function of immersion time in plating solution. Resistivity of bulk Cu is shown for comparison

Summary

This section presented series of exploratory experiments which capture the knowledge gained on how to successfully deposit electroless Cu films on PC using the process depicted in Figure 16. Based on these results ECu is deemed suitable for use in a

R2R nanofabrication process for Cu metal nano-mesh TCEs. The bulleted list below tabulates major learning items.

- 2 - 3 nm thick Pd seed layer is needed for reliable ECu deposition of high-quality
- Pd seed layer and ECu films exhibit good adhesion to PC substrates
- Pd layer is continuous for thicknesses equal to and greater than 20 nm
- ECu films begin as isolated islands and coalesce to form a continuous layer in three distinct phases of growth: nucleation, granular merging and uniform film
- Average grain size of ECu is 43.8 nm with sample standard deviation of 19.8 nm
- Grain size is independent of plating time and seed layer thickness
- Deposition rate of ECu films beyond 60s immersion time is close to 80 nm/min
- Resistivity of electroless deposited copper is ~13 μΩ cm.

GLANCING ANGLE DEPOSITION (GLAD) PROCESS APPROACH

The GLAD process approach relies on the principle that electroless plating is only able to deposit Cu where Pd catalyst is exposed to the solution. Therefore, selective ECu plating is achievable if certain areas of a catalytically activated surface are coated by an inert blocking layer material such that the underlying seed catalyst is locally isolated from coming in contact with the ECu solution. In other words, electroless Cu is expected to deposit only were Pd is not covered by the blocking layer material. The key advantage of the GLAD process approach is that it does not require etching of materials to attain selectivity in metallization. Etching steps in a candidate fabrication process should be carefully evaluated since they tend to increase processing complexity. Hence why this research first explores the GLAD process approach verses the Etch process scheme.

The glancing angle deposition technique entails evaporating material at an oblique deposition angle (α) between the substrate normal and incident vapor trajectory direction. Additionally, rotation of the substrate by angle (θ) orients features on the substrate surface

relative to the incident vapors. Note, the trajectories of evaporated material vapors are accurately described by rays parallel to one another originating from the source material at the center of the crucible. Figure 27 illustrates how the GLAD technique was performed during wafer scale experimentation in this thesis.

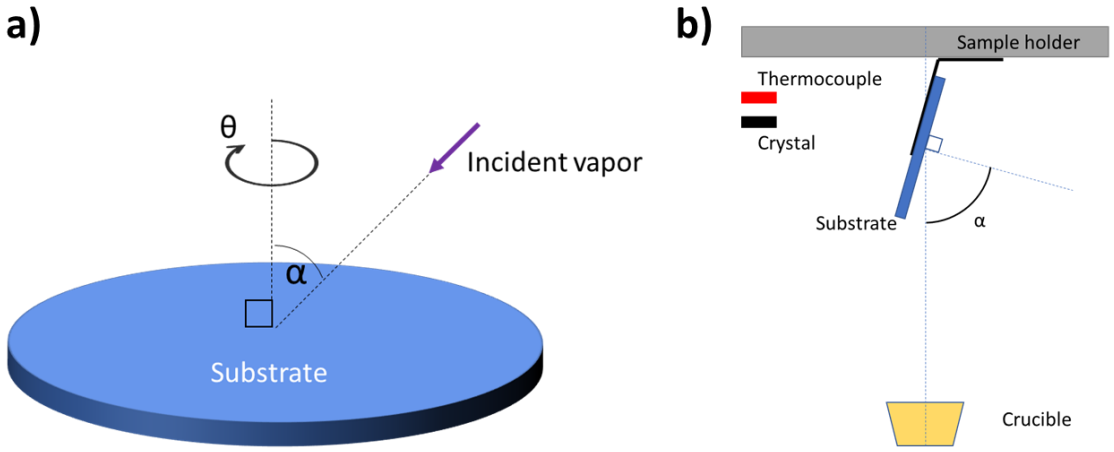

Figure 27: Diagram on GLAD technique. a) Definition of oblique deposition angle (α) and substrate rotation angle (θ). b) Arrangement of sample substrate in electron beam evaporation tool relative to source material in crucible during GLAD.

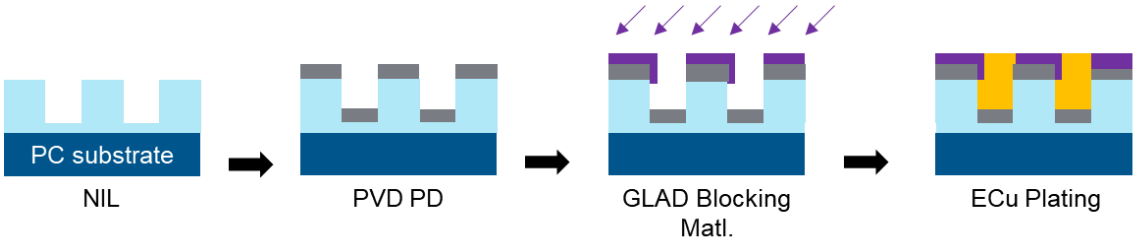

Figure 28: Schematic diagram of GLAD process steps

Figure 28 provides a schematic of the process steps in the glancing angle deposition approach. First, NIL (J-FIL) transfers a pattern of trenches arranged in a 2D square grid in UV cured imprint resist onto a PC substrate as depicted in Figure 15 . Although not depicted in Figure 28, patterned PC substrates then undergo a surface treatment consisting

of a solvent rinse to clean the resist surface and promote adhesion. Next, PVD sputtering is used to deposit a 3 nm thick Pd seed layer which catalytically activates the entire surface of the resist layer for subsequent electroless Cu plating. After surface activation, the glancing angle deposition technique is used to selectively grow blocking layer material only on the raised planar areas between trenches leaving Pd catalyst at the bottom of the trenches exposed. The blocking layer material does not deposit in the trenches of the pattern due to line of site shadowing of incident vapor by the trench sidewalls at appropriate values for both α and θ for a given pattern geometry. Figure 29 shows an example of this shadow-dependent deposition on the fine grid (300nm width and 3μm pitch) imprint pattern of trenches after GLAD of Ta_2O_5. In actual practice, some sidewall coverage will occur since the deposition angle (α) is limited to <90°. The final step in the GLAD process is immersion of the sample in ECu plating solution for selective metallization insides of trenches to form an electrically conductive embedded Cu metal mesh grid.

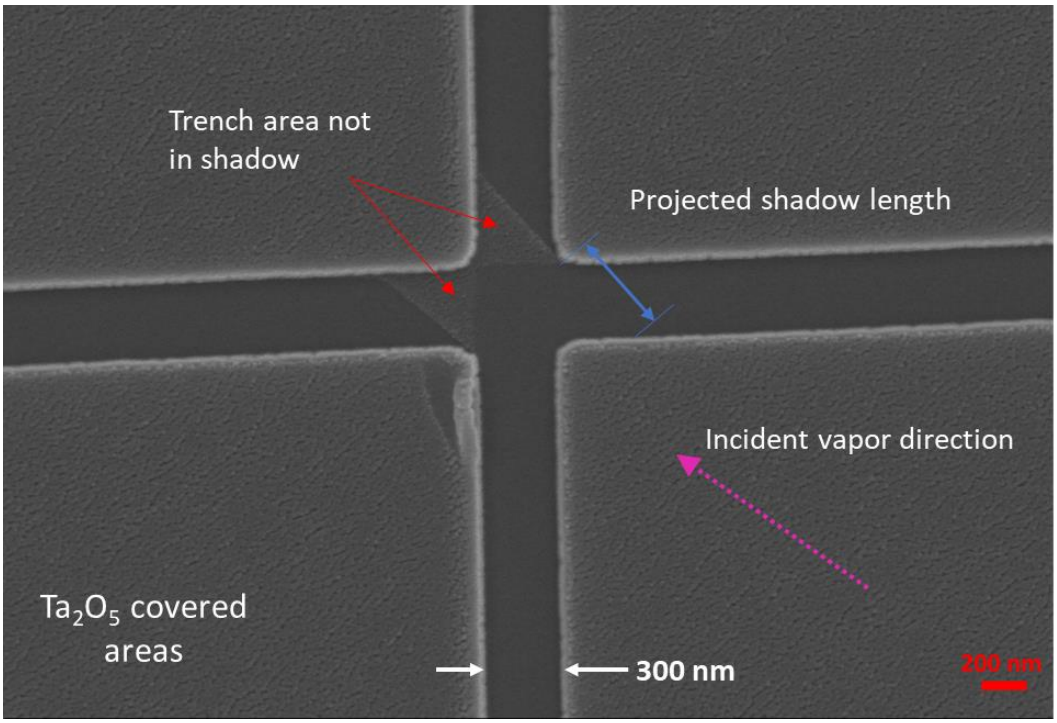

Figure 29: Top-down SEM image of fine grid trench pattern after GLAD of 50nm Ta_2O_5 at $\alpha = 75°$ and $\theta = 45°$

Identifying a Suitable Blocking Layer Material

In order to effectively seal the Pd seed layer from communication with ECu plating solution when immersed, candidate materials for the blocking layer must meet the follow requirements.

1. Material must be compatible with evaporative PVD process i.e. electron beam or thermal evaporation
2. Material refractive index must be relatively low to limit reflection losses at material interfaces
3. Material must not be soluble in ECu plating solution
4. Material must not act as an ECu catalyst itself
5. Material must form continuous layer at necessary oblique deposition angles

6. Boiling temperature of material must not be excessively high to protect PC substrate during depositions
7. Material should not adversely affect wetting properties of patterned surface such that ECu solution does not reach Pd at the both of imprinted trenches

Requirement 1 above eliminates polymers from consideration, and similarly, requirements 2 and 4 prevent the use of conductors i.e. metals. Based on the above requirements, metal-oxides were considered as the best suited candidate materials for the blocking layer.

Materials selected for testing include SiO_2, HfO_2, Ta_2O_5 and SnO_2 since they all meet requirements 1 and 2 based on prior knowledge. Experimentation explored whether any candidate material simultaneously satisfied requirements 3 – 7. Testing of selected candidate materials consisted of performing metrology after each process step shown in Figure 28 at varying process parameters on PC wafers for all candidate metal-oxides individually. Table 5 summarizes findings from experiments performed with each candidate material according to the blocking layer requirement noted above. Note, GLAD did not occur in a partial O_2 environment, and actual metal to oxide stochiometric ratios of deposited film may differ from target material.

Table 5: Results from Blocking Layer Material Test Experiments

Requirement	SiO_2	HfO_2	Ta_2O_5	SnO_2
Refractive index (n_{PC} = ~1.58)	Good (1.46)	Acceptable (2.12)	Acceptable (2.14)	Acceptable (2.01)
Prevents ECu Plating	No (Soluble in ECu Solution)	TBD	No (Plating in pinholes)	No (Soluble in ECu Solution)
Forms uniform layer (α>45°)	TBD	-	No	TBD
Boiling Temperature	Good (1025°C)	High (~2500°C)	High (1920°C)	Good (~1000°C)
Wetting Properties	TBD	-	Good	TBD

Of all materials tested, only Ta_2O_5 was observed to be chemically resistant in the ECu plating solution but failed to prevent Cu deposition at necessary oblique angles. Figure 30 shows performing GLAD of Ta_2O_5 at $\alpha > 45°$ results in the formation of a discontinuous film allowing Cu grains to nucleate in gaps between neighboring deposits of Ta_2O_5. This is a limitation associated with the GLAD technique rather than a property of the material, and is discussed in greater detail in the following section. Dissolution of blocking layer materials other thanTa_2O_5 exposed the underlying Pd catalyst to the plating solution and allowed plating to occur everywhere. A pH dip test revealed the pH level of the ECu solution to be roughly 14. This hot alkaline nature of the plating solution may explain why neither SiO_2 or SnO_2 are able to survive immersion. Moreover, stoichiometry of deposited metal-oxides may differ from target material resulting in changes to chemical properties. The high boiling temperature of Ta_2O_5 also caused temperatures to quickly rise during deposition in the evaporation chamber and consequently the PC substrate. The largest thickness Ta_2O_5 layer deposited during the course of experimentation was <50 nm before substrate temperature approached the glass transition (T_g) temperature of PC. HfO_2 has an

even higher boiling temperate than Ta_2O_5 and attempts to deposit the material resulted in damage to the PC substrate. At the time of writing this thesis, no suitable blocking layer material has been identified to achieve highly-selective ECu plating by GLAD. Further testing is required to address concerns of current candidate metal-oxides or explore alternative materials.

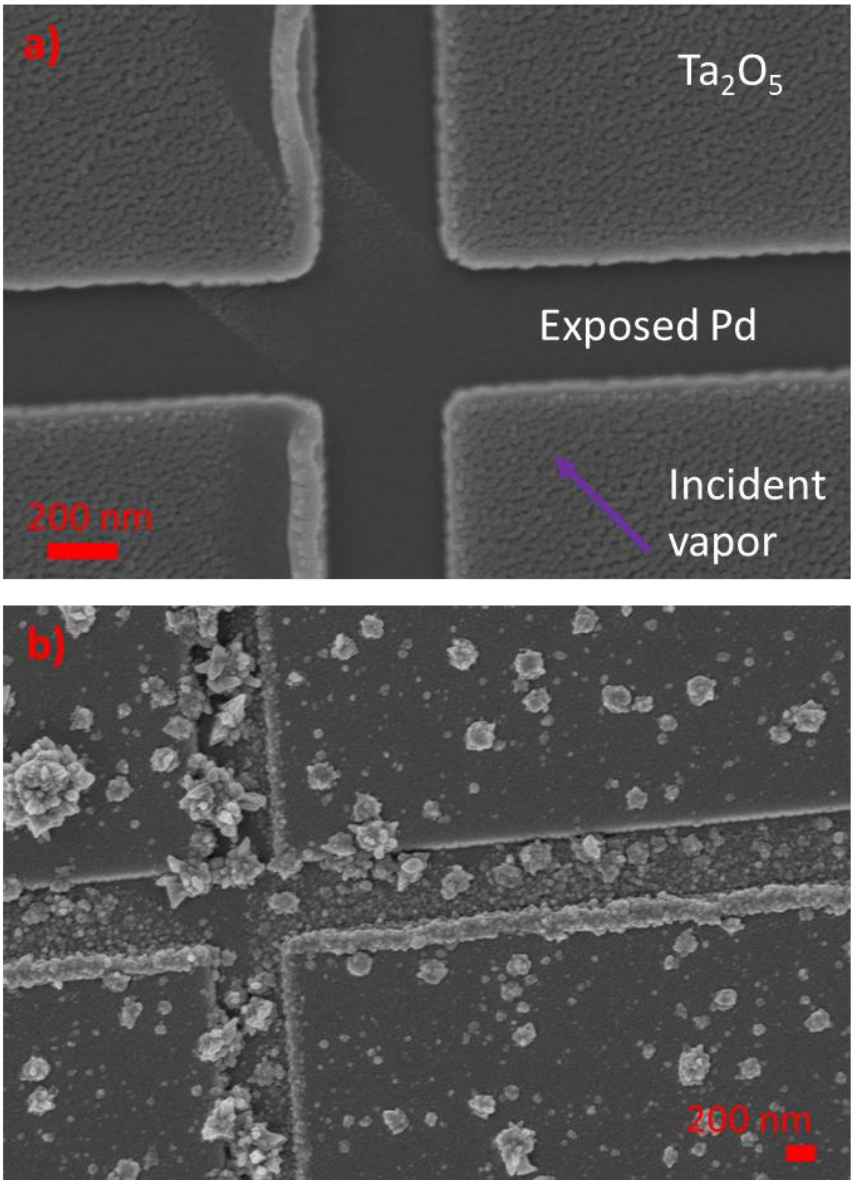

Figure 30: Top-down SEM images of GLAD 30 nm of Ta2O5 at $\alpha = 75$ and $\theta = 45$ a) before ECu plating and b) after 30s immersion in ECu plating bath. Cu is able to nucleate in Ta_2O_5

Limitations of GLAD Process

Regardless of blocking material choice, the GLAD technique has several caveats discovered through experimentation which limit is applicability in a R2R fabrication process for metal mesh grids. In terms of geometry, shadows cast by trench sidewalls are

unable to span the entirety of the trench width at line intersection even at large deposition angles as see in Figure 29 and Figure 30. Insufficient shadowing of blocking layer material will result in disconnected gridlines at every intersection and lower overall conductivity of the grid. This shadowing issue becomes more problematic for grid geometries where intersecting lines are not orthogonal to each other e.g. honeycomb. One solution is simply to increase the deposition angle (α) to produce long enough shadows such that they cover the whole of the bottom of the trench at line intersections.

However, increasing α exacerbates the problem of discontinuous deposited blocking layer films mentioned in the previous sections. Consider the diagram in Figure 31. During GLAD of an arbitrary material, the initial nuclei which condense on the substrate surface also cast their own shadow in the immediately surrounding area. These local shadows in turn restrict further deposition to the tops of the nuclei. As deposition proceeds, this phenomenon results in the formation of a micro-columnar structure of the blocking layer material which is unable to completely isolate the underlying Pd seed from reacting with the ECu plating solution.

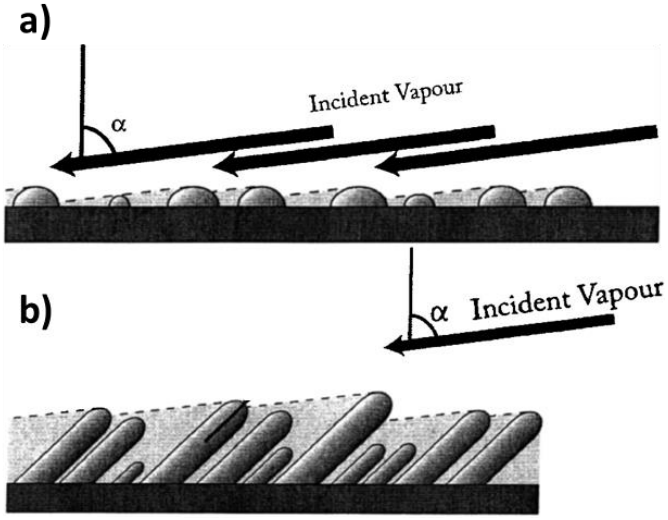

Figure 31: a) Initial nucleation of GLAD material showing localized ballistic shadowing. b) Collimation of film as deposition continues [97]

Columniation of GLAD deposited films can occur for α values as low as 25° and becomes more prominent as deposition angle increases [97]. Furthermore, throughput is reduced since the incident vapor flux of the target material normal to the substrate becomes a product with the sine of deposition angle. At larger α, the incident vapor flux is significantly diminished reducing actual blocking layer deposition rate and allowing more time for the substrate to heat up.

Summary

The GLAD process approach is an attractive option in theory, but significant challenges associated with this scheme in practice impede successful selective ECu plating. All materials tested as potential candidates for the blocking layer in the GLAD step failed to simultaneously satisfy all blocking layers requirements. Only Ta_2O_5 exhibited chemical compatibility with the ECu solution while SiO_2 and SnO_2 were observed to be soluble. However, at the deposition angles required to cast sufficiently long shadows for the geometries of current imprint trench patterns, Ta_2O_5 develops a discontinuous columnar

film microstructure unable to effectively block the Pd seed layer from contacting the plating solution. Additionally, larger oblique deposition angles negatively affect throughput using GLAD and worsen substrate heating. Based these outcomes, it is concluded the GLAD process is incompatible as an option for R2R fabrication of metal nano-mesh TCEs, and focus of this research is now directed to the Etch process option.

ETCH PROCESS APPROACH

Similar to the GLAD approach, the basic premise of the Etch process scheme is to achieve selective ECu metallization by isolating certain areas of an activated surface from interacting with the plating solution. An important distinction of the Etch process is patterned imprint resist acts as the blocking layer material rather than a metal-oxide grown using the GLAD technique. UV irradiated polymerized imprint resist exhibits remarkable chemical resilience and is known to be insoluble in ECu plating solution. Moreover, the Etch process does not suffer from the geometric and microstructure limitations related to shadow-dependent oblique angle deposition like in the GLAD process flow However, this process employs an adhesion primary layer and etch step to perform pattern transfer and remove the RLT of imprinted resist to expose the underlying Pd catalyst, respectively. These additional process steps risk corrupting the Pd catalyst by inducing oxidation resulting in poor-quality ECu deposition or failure to plate entirely. Therefore, experimentation is necessary to evaluate the feasibly of this fabrication method.

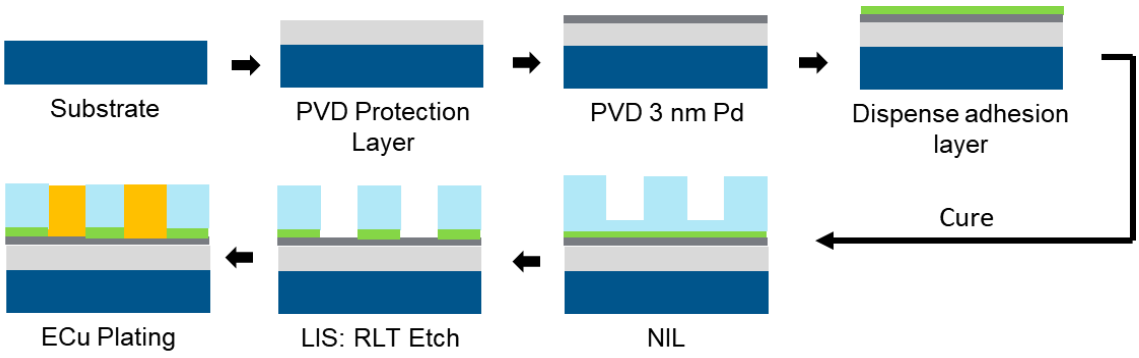

Figure 32: Schematic of Etch process steps

Figure 32 shows the required sequence of steps involved in the Etch process. The flow begins with the PVD of a protection layer material on PC substrates which acts as a barrier between the PC and a polymeric adhesion promoting material containing strong solvent later in the process scheme [98]. Next, sputtering 3 nm of Pd is used to catalytically activate the surface of the protection layer for subsequent ECu plating. A polymeric adhesion promoting layer is then dispensed in order to successfully perform NIL on the Pd coated protection layer surface. The adhesion layer ensures UV cured imprint resist separates from the imprint template rather than the substrate surface during the last step in J-FIL. In wafer-scale experimentation, dispersion of the adhesion layer is completed by spin-coating, but slot-die coating can accomplish the same task for R2R processing. Adhesion layer coated samples are then cured at temperatures below T_g of PC to evaporate off solvents. Afterwards, NIL is used to transfer trench patterns on to the substrate surface. Then, samples undergo exposure to the linear ion source (LIS) equipped in the Emerson & Renwick GENESIS series tool platform in order to etch the RLT of the imprint resist layer. The LIS works by bombarding a mixture of Ar and O_2 ions towards the substrate to allow oxidation of organics and also physically mill away material. Therefore, the Pd and protection layers should function as an etch stop in the Etch process scheme The LIS etch exposes Pd catalyst only at the bottom of trenches in imprint resist allowing for selective

ECu deposition. Finally, samples are immersed in plating solution to metallize trenches and form an interconnect embedded metal mesh electrode.

Proof of Process Concept Experimentation

This section presents results of initial proof of concept experiments demonstrating ability of the Etch process to achieve highly selective ECu plating and fabricate metal mesh grids. Before devoting research resources to identify a viable protection layer material, preliminary testing assessed the likelihood of success and capabilities of the etch process in general. In these initial versions of exploratory experiments, thick Pd layers act simultaneously as the seed for ECu catalysis and barrier between the PC and the adhesion layer polymer. Recall, the morphology study of catalyst seeding showed 20 nm PVD of Pd forms a continuous, highly planar layer. Figure 33 shows the modified etch process step in proof of concept testing.

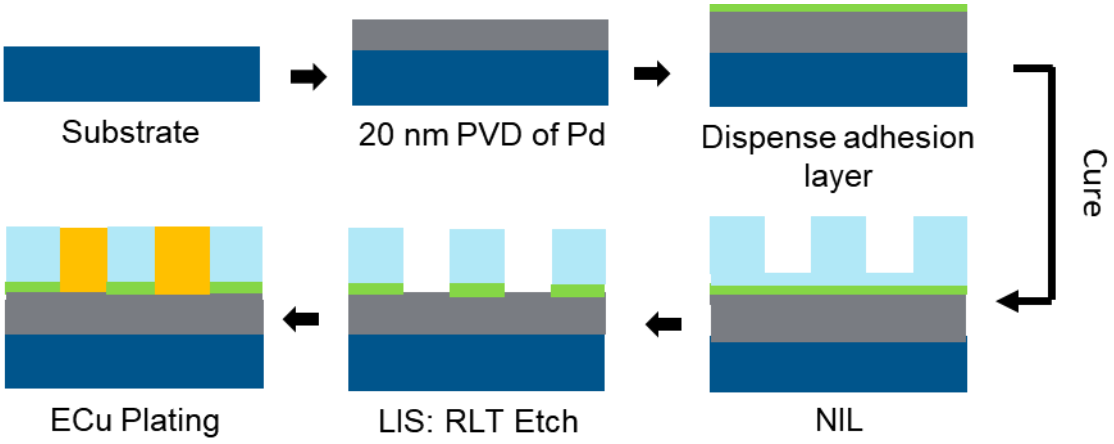

Figure 33: Schematic of modified Etch process steps for proof of concept testing

Figure 34 shows results from an etch approach proof of concept experiment after all process steps in Figure 33 have been performed on the sample. Despite adhesion concerns related to imprinting on Pd coated substrate, high quality pattern transfer is demonstrated. For both the fine and course grid pattern geometry, ECu plating occurred

highly selectively within trenches and formed a well-defined continuous network of grid lines. Figure 34d shows incomplete filling of trenches for the immersion time of 105s in plating solution, but this may be a result of the relatively short time in solution. However, observable Cu plating occurs preferentially at the trench sidewalls and is highly localized to large granules within the width of trenches. The sizes of Cu granules range between 60 – 200nm which is significantly larger than the average Cu size previously observed on planar PC substrates. In addition, trench width for the course grid pattern widened by ~200nm post exposure to LIS which is evident of isotropic etching. These results suggest there are interactions occurring amongst the RLT etch and different process steps which affect the quality of ECu plating and necessitate further investigation.

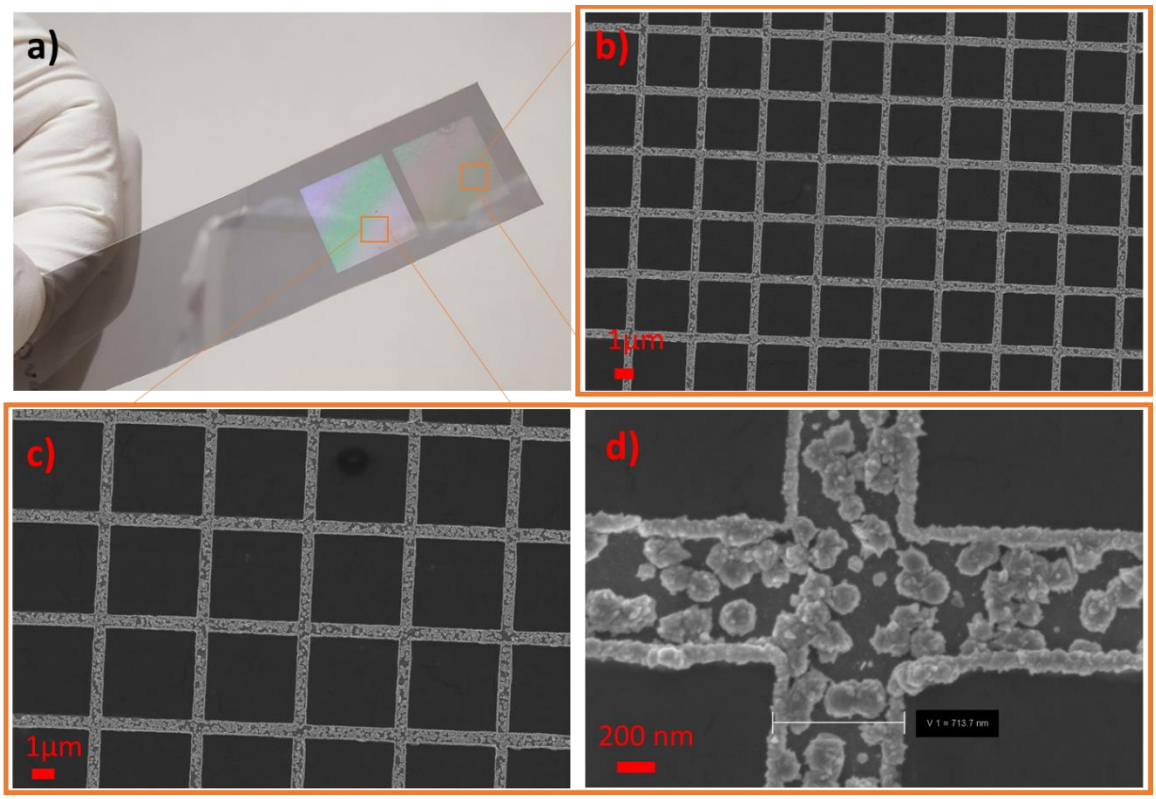

Figure 34: Example of results from proof of concept testing using the Etch fabrication process. a) photograph of a PC coupon showing fields with grid patterns after ECu plating, b) SEM image of fine grid pattern after 105s in plating solution, c) & d) SEM images of course grid pattern after 105s in ECu plating

To study the effect of the LIS on the Pd seed layer, bare PC samples were prepared according to Etch process flow (Figure 32) up to electroless Cu metallization step but not immersed in plating solution. 100 nm of SiO_2 comprised the protection layer since it is known to be compatible with both the adhesion promoting polymer and imprint resist. Figure 35 provides a comparison between PC coupons cut from the same 3 nm Pd coated wafer where one section was subjected to LIS treatment and the other was not.

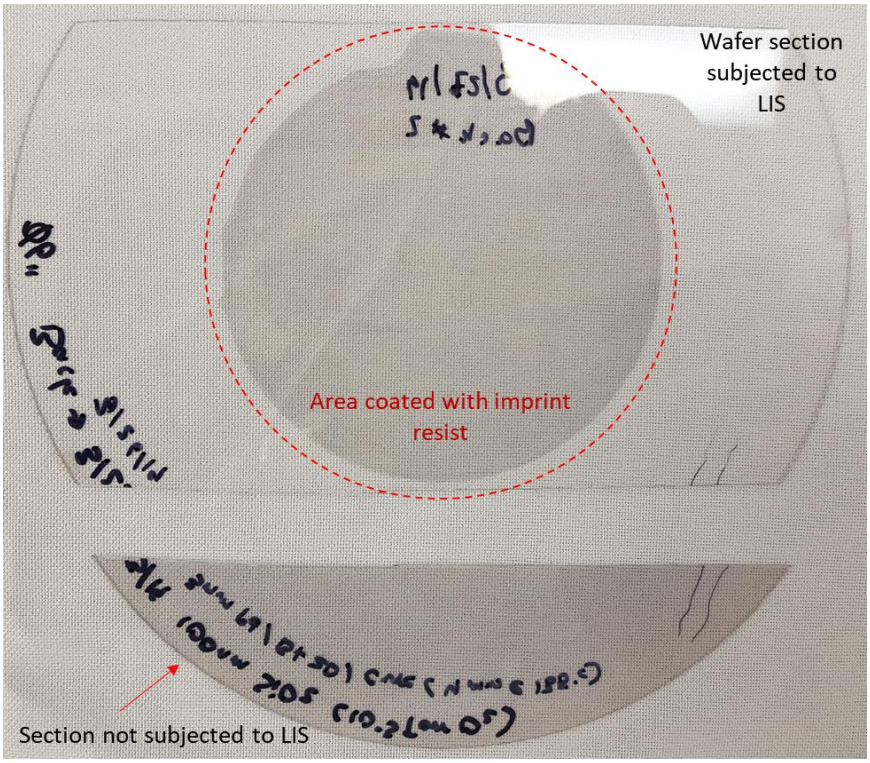

Figure 35: Picture of PC wafer prepped using the Etch process flow showing the effect of LIS exposure on the Pd seed layer

Visual comparison of both sections of the PC wafer clearly reveals a change in tint between areas not protected by an addition layer of imprint resist after exposure to the LIS. This change in shading is indicative of less Pd remaining on the surface of the wafer post LIS etch than originally deposited by sputtering. In other words, the LIS plasma is milling the Pd seed layer off of the wafer in addition to etching imprint resist. The milling of Pd seed catalyst may also explain the preferential deposition of electroless Cu on the trench sidewalls and discontinuous granularity at the bottom of trenches shown in Figure 34d. Consider Figure 36 which illustrates the ejection of Pd atoms from the seed layer due to kinetic energy transfer from incident ions. The emitted Pd atoms at the bottom of the trenches have a high probability of redeposition along the sidewalls of the trenches creating nucleation sites for Cu grains during ECu plating. Conversely, ejection of Pd atoms at the

bottom of the trench results in less catalyst sites causing nucleation to occur in isolated islands rather than uniformly. Excessive milling caused by prolonged exposure to LIS results in partial filling of trenches during ECu plating and increased surface roughness due to the formation of large granules.

Undoubtedly, the LIS etch step requires fine tuning to minimize milling of the Pd seed layer to improve metal mesh quality. Nonetheless, exploratory testing was able to fabricate a metal mesh grid with only minor modification to the process steps proving the Etch process approach is able to achieve highly selective ECu plating. These positive results suggest the Etch process is capable of fabricating any arbitrary grid geometry and signify progress towards overall goals of this research.

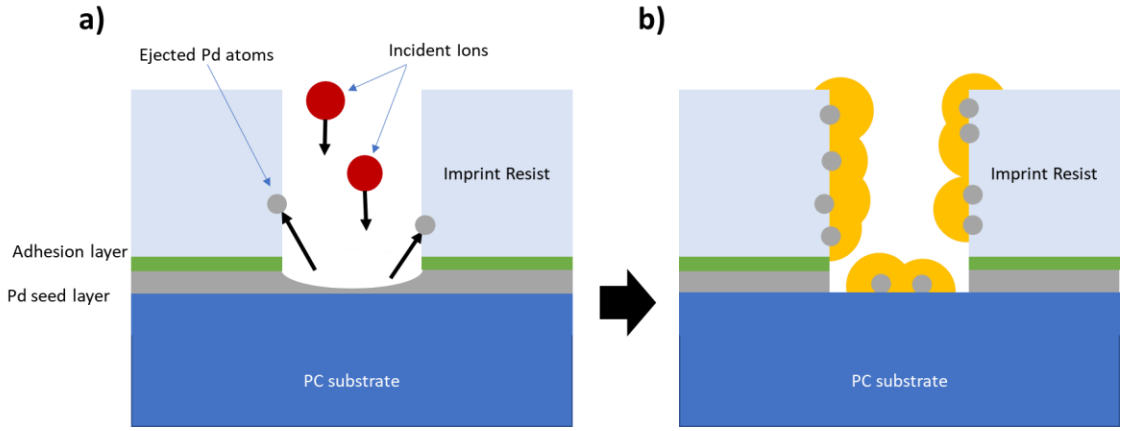

Figure 36: a) Illustration depicting redeposition of ejected Pd atom along trench sidewalls during LIS etching, b) Discontinuous electroless Cu deposition at the sites of Pd catalyst along

Fabricated Metal Mesh on Quartz

Although the modified LIS etch process (Figure 33) demonstrates the feasibility of selective ECu plating by the LIS RLT etch scheme, the 20 nm thick Pd seed layer used for proof of concept testing is not appropriate for fabricating actual metal nano-mesh TCEs. Transmittance of light in the visible spectrum through a 20 nm thick film of Pd is <30%

alone, and scaling any process which requires significant amounts of Pd for large-scale production would be prohibitively expensive. Therefore, a candidate material for the protection layer is required to reduce Pd seed layer thickness per process steps in Figure 32.

Building on knowledge gained during experimentation for a candidate material as the blocking layer in the GLAD process approach, metal-oxides are considered once again. However, most are incompatible with the ECu solution due to chemical solubility. Nonstoichiometric chemistry and amorphous microstructure of evaporated SiO_2 films may explain why they did not previously exhibit the same inert behavior as their crystalline counterpart, quartz. To evaluate the merit of this theory, metal mesh grids are demonstrated on a quartz substrate by employing the Etch process in Figure 32 i.e. the substrate and protection layer are the same material in this case.

Figure 37 shows results of the fabricated metal mesh on a quartz substrate using an reduced LIS exposure time and immersion in ECu plating solution for 60s. Slight Cu deposits seen around the edge of the patterned quartz wafer in Figure 37a are expected since Pd seed was sputtered over the entire face of the wafer but was mostly removed under exposure to the LIS. In both the fine and coarse grid geometries, high-quality selective ECu plating is observed and is continuous throughout the trenches. Defect density and total number of defects is extremely low exemplifying the robustness of the Etch process approach. Furthermore, average Cu grain size is on par with other electroless plating films i.e. ~45 nm. Continuous ECu plating here is directly a result of improved LIS exposure time discovered through multiple iterations of testing. Note, preferential Cu plating along the sidewalls still exists suggesting further refinement of the LIS etch step is required (this can also be inferred form the fact there is virtually not Cu plating outside of imprint resist coated area). Important to process development is the fact fabricated metal mesh grid show

good adhesion to the substrate which is strong evidence quartz, and therefore crystalline SiO_2, is resilient to dissolution by ECu plating solution.

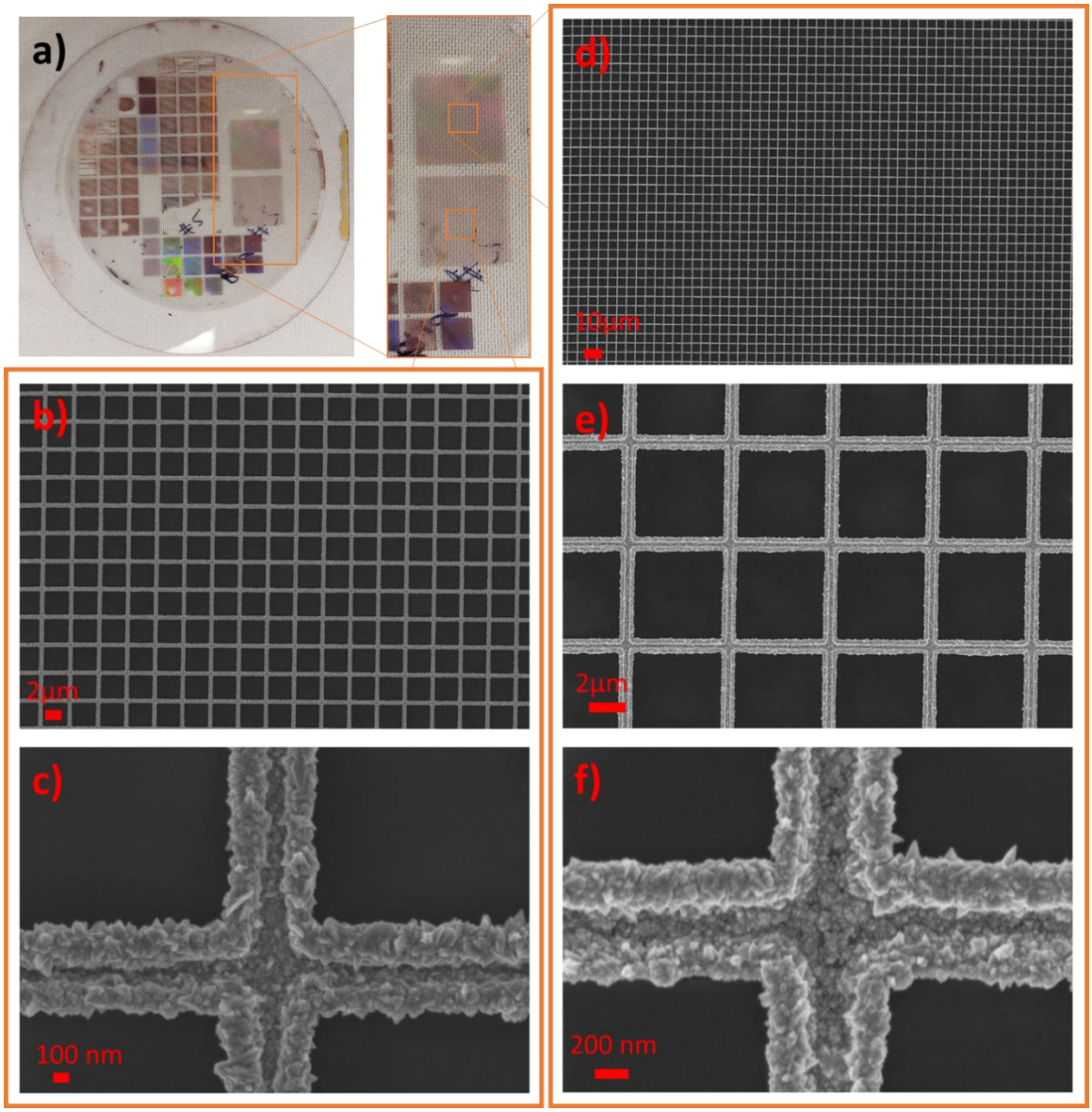

Figure 37: Fabricated metal mesh on quartz wafer. a) image of patterned quartz (insert is of fields consisting of trench grids), b) & c) SEM images of the fine grid pattern, d-f) SEM images of coarse grid pattern post 60s ECu plating

Measured sheet resistance values for the Cu metal grids shown in Figure 37 were 2.8 Ω/sq. and 3.3 Ω/sq. for the fine grid and coarse grid geometries, respectively. Measures

R_s values are less than half of predicted values using Equation 7. The discrepancy between measured and predicted sheet resistances is most likely due to the larger cross-section of plated Cu lines within the trenches of the imprint resist pattern due to anisotropic etching and over plating of Cu.

Figure 38 shows the measured and simulated transmittance spectra normalized to air through both metal mesh patterned fields. In order to study the influence of the Pd seed layer on transmission through the metal mesh TCE, results of simulated transmittance with and without the 3nm Pd layer are provided. Note, modeling employs poly(methyl methacrylate) (PMMA) to represent UV cured imprint resist and the adhesion promoter polymer based on material optical data from Kasarova et al. [99]. Measured T_{550nm} for the fine and coarse grid is 45% and 53%, respectively, however, simulated T_{550nm} with 3 nm Pd seed layer for the fine and course grid is 34% and 36%, respectively.

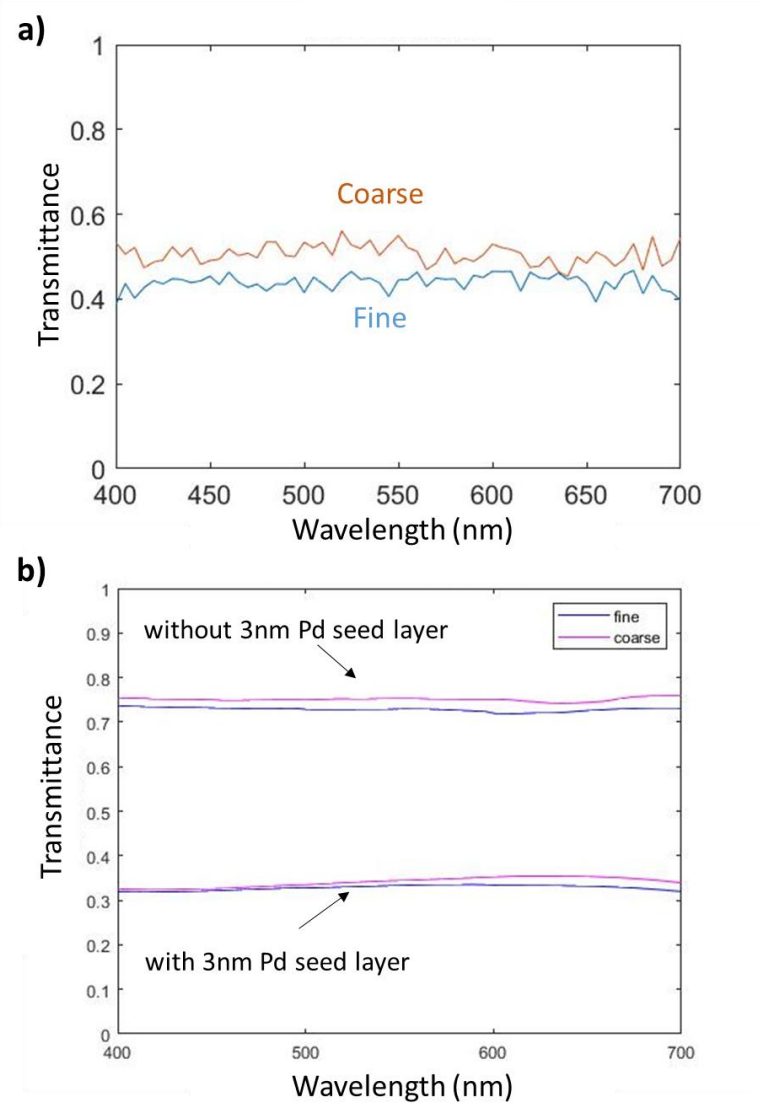

Figure 38: a) Measured transmittance as a function of wavelength through fine and coarse metal mesh grid electrodes fabricated on quartz substrate by the Etch process approach, b) simulated spectral transmittance as a function of wavelength through both fine and coarse grids with and without 3nm Pd seed layer on quartz substrates

The discrepancy between measured and simulated transmittance may be due to one of several factors. To fully understand this problem, a combination of simulation studies involving perturbation of ideal parameters along with careful complementary experiments

are needed. These studies are a topic for future research. Among the factors to consider are:

- The seed layer is assumed to be exactly 3 nm thick and perfectly continuous in simulation, whereas, in experiments, sputtering 3 nm of Pd creates disperse islands of metal deposits rather than a uniform film which may allow increased transmission of light compared to a contiguous layer.
- There is uncertainty in the refractive index of the materials in the film stack including the imprint resist and adhesion promoter polymer layers.
- The measurement precision and uniformity of the various films including the remaining imprint resist after the LIS RLT etch, and the variation in the Pd seed layer.

Future work should include making unpatterned stacks of the various films employed on representative substrates to estimate the optical properties and film thicknesses that need to be incorporated into simulations. Also, introducing quantified uncertainty in the simulation models and performing careful sensitivity analyses will help identify the dominant factors that are causing the discrepancy between simulations and measured results.

Separately, it is imperative to reduce the thickness of the Pd seed layer while still allowing for reliable electroless Cu deposition. Comparison of simulated transmittance with and without the 3nm Pd seed layer in Figure 38b shows nearly a 40% reduction in broadband transmittance due to the presence of the thin metal film. Recommendations for future work address this issue by suggesting a possible solution in the form of selective atomic layer deposition (ALD) of Pd in the trenches before ECu plating.

Fabricated Metal Mesh on Polycarbonate

Based on the successful fabrication of metal mesh grids on quartz substrates, SiO_2 was considered as a candidate material for the protection layer in the Etch process scheme. To assess whether SiO_2 is a suitable material choice, Cu metal mesh grids were realized on PC wafers with 100 nm thick SiO_2 layers functioning as the protective barrier between the substrate and solvent containing adhesion promoter polymer. E-beam evaporative deposition of SiO_2 occurred in an environment with partial pressure of O_2 at 2e-5 Torr to ensure correct metal-to-oxide stoichiometry [100], [101]. RLT etch by LIS exposure was performed at identical process conditions to metal mesh grids fabricated on quartz substrates presented in the preceding section. Figure 39 shows results of a Cu metal mesh fabricated on a PC substrate with SiO_2 protection layer after immersion in ECu plating solution for 45s. Even on a flexible substrate, the Etch process is able to again achieve high-quality selective ECu plating within the trenches of both fine and coarse grid patterns. Cu grains are close to the average size of ECu deposition, and plating covers the bottom of the trenches entirely. However, sidewall preferential plating is still evident as expected.

Measured sheet resistance values for the Cu metal grids shown in Figure 39 were 3.4 Ω/sq. and 3.6 Ω/sq. for the fine grid and coarse grid geometries, respectively. Sheet resistance values are once again about half of predicted values but slightly higher than equivalent grids on quartz substrates. The difference in R_S between fabricated Cu metal mesh grids on quartz and PC is due to the shorter ECu plating time for samples on PC wafers i.e. less Cu deposited in trenches.

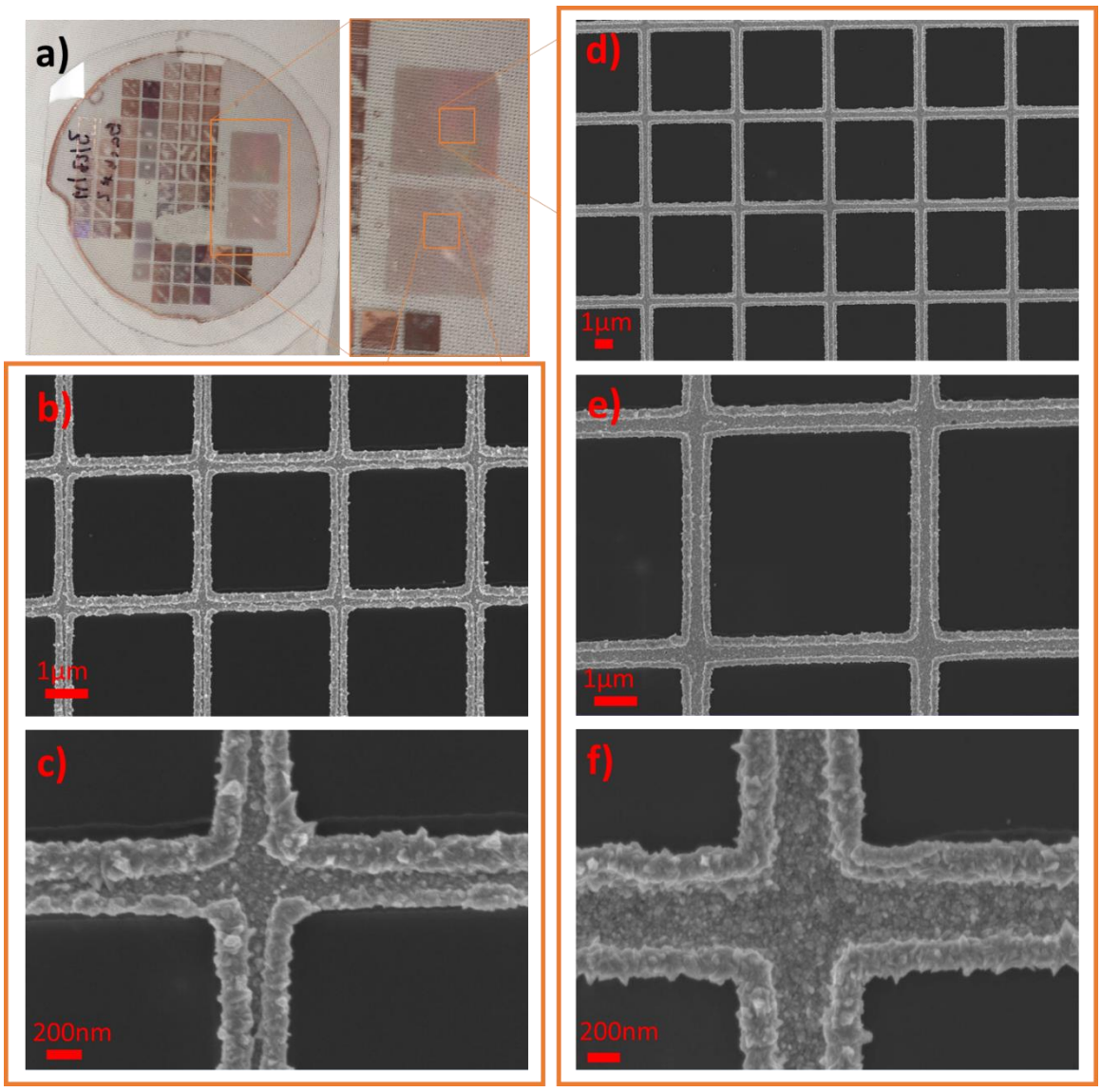

Figure 39: Fabricated metal mesh on PC wafer. a) image of patterns on PC (insert is of fields consisting of trench grids), b) & c) SEM images of the fine grid pattern, d-f) SEM images of coarse grid pattern post 45s ECu plating

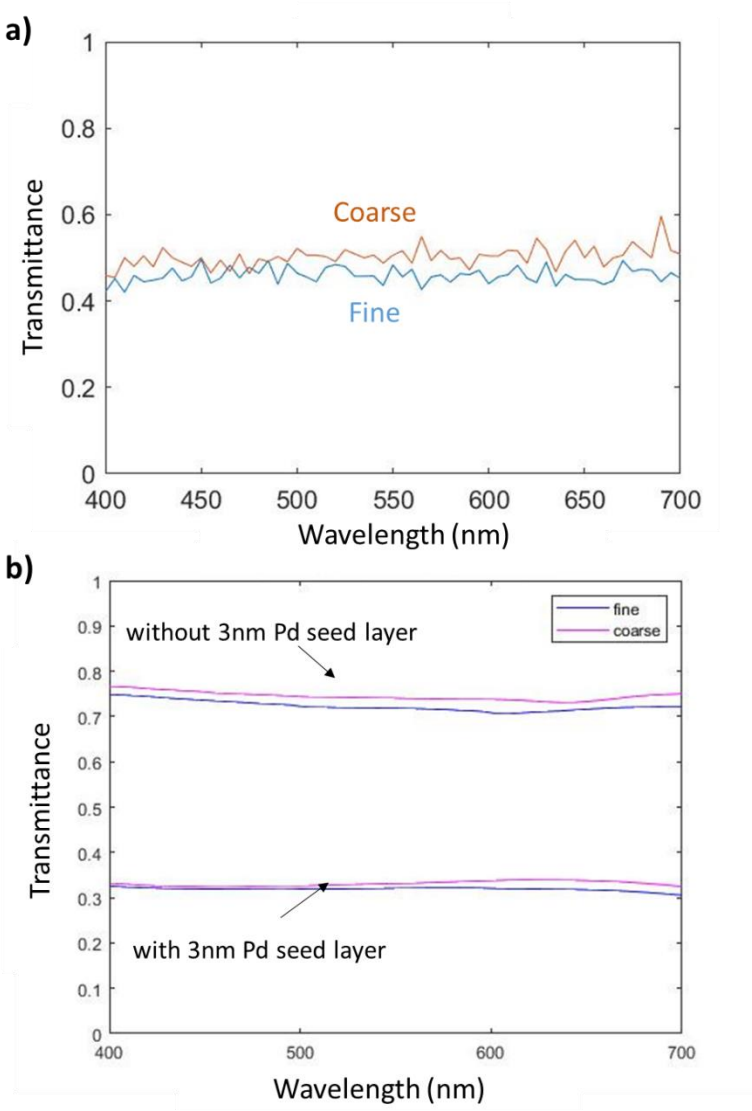

Figure 40: a) Measured transmittance as a function of wavelength through fine and coarse metal mesh grid electrodes fabricated on PC substrate with 100 nm thick SiO_2 protection layer, b) simulated spectral transmittance as a function of wavelength through both fine and coarse grids with and without 3nm Pd seed layer on PC substrates with 100 nm thick SiO_2 protection layer

Figure 40 shows the measured and simulated transmittance spectra normalized to air through both metal mesh patterned fields on PC substrates. Simulated transmittance with and without the 3nm Pd layer on PC substrates is provided once again to illustrate effect of the Pd seed layer on transmission through material stack. Modelling employs

material optical data for PC from Sultanova et al. [102]. Measured T_{550nm} for the fine and coarse grid is 44% and 51%, respectively. Measured transmittance of grids fabricated on PC substrates is similar to those fabricated on quartz which is expected since quartz and PC have closely matching refractive indices. Simulated T_{550nm} for the fine and coarse grid is 33% and 34%, respectively. Differences in the simulation results and the corresponding experimental results are speculated to be caused by several factors as discussed in the first full paragraph starting on page 71. Similarly, the presence of the 3 nm Pd seed layer results in the roughly 40% reduction in broadband transmittance of both grids.

Judging from results shown in Figure 39, SiO_2 does not allow the adhesion promoter material to penetrate and cause damage to the underlying PC substrate. However, catastrophic delamination of the metal mesh patterned fields is observed beyond 45s immersion time in the plating solution as shown by Figure 41.

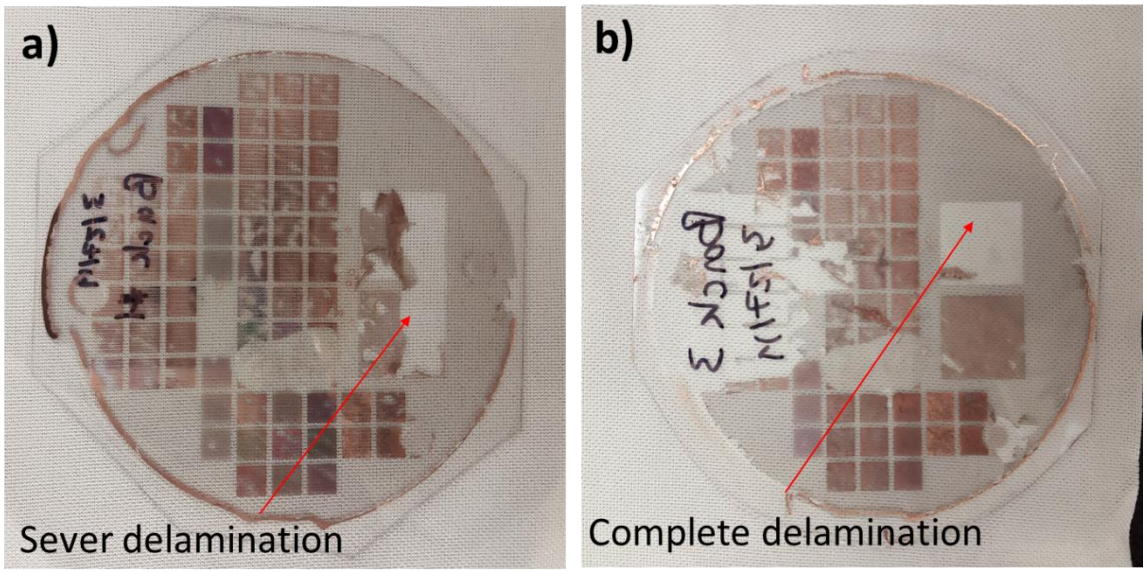

Figure 41: Images of delamination of metal mesh fields from PC substrate due to dissolution of SiO_2 protection layer. a) PC wafer immersed in ECu plating solution for 60s, b) another PC wafer immersed for 60s

Further investigation into the occurrence of delamination revealed that a continuous layer of SiO_2 is still present on the substrate surface after immersion in plating solution for 60s. These results show the protection layer is chemically failing at the interface between SiO_2 and the Pd seed layer as depicted by Figure 42. Hence, all materials deposited on top of the protection layer lift-off due to adhesion failure once enough of the SiO_2 is dissolved by the plating solution. Moreover, this experiment shows crystallography of SiO_2 is the key factor, not stoichiometry, in regards to its chemical compatibility. For this reason, SiO_2 is not a suitable protection layer material and an alternative must be identified.

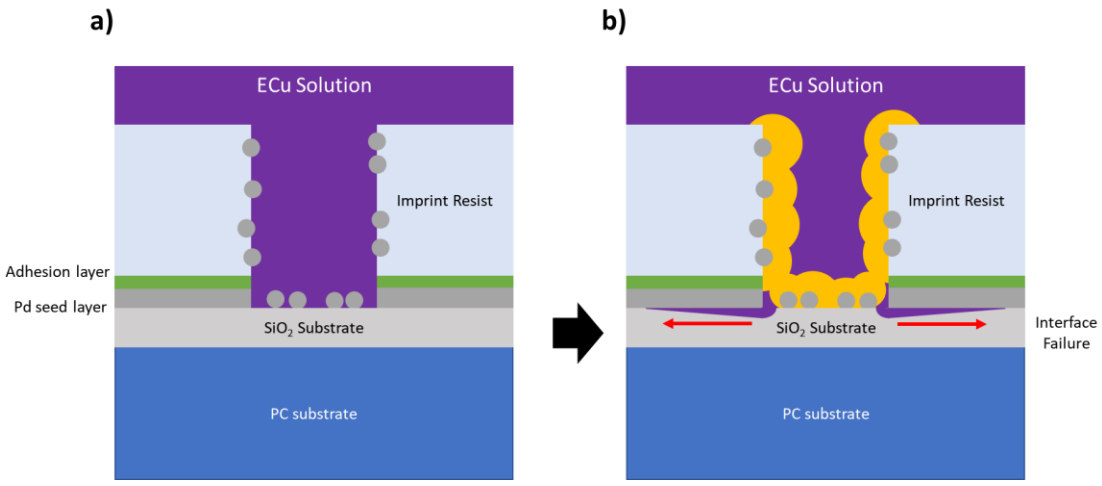

Figure 42: Illustration of adhesion failure at the SiO_2 protection layer and Pd seed layer interface. a) imprinted sample structure upon initially being immersed in the ECu plating solution, b) dissolution of SiO_2 protection layer surface by ECu solution under Pd seed layer leading to adhesion failure and delamination of subsequently deposited layers

Summary

The LIS etch process approach successfully demonstrated selective electroless Cu deposition of high quality and uniformity within subwavelength trench geometries. Cu metal nano-mesh grids with remarkably low defect densities were fabrication on stiff and flexible (quartz and PC) substrates using the Etch process. Moreover, measured sheet resistances of fabricated grids were superior than predicted values using the empirically determined resistivity of electroless Cu. While results of early experimentation of this process are extremely promising for a R2R nanofabrication, additional process development work is needed for scalable, inexpensive high-through production of metal mesh TCEs. Firstly, an appropriate protection layer material should be identified to prevent delamination of patterned films in ECu solution. One auspicious metal-oxide candidate is Al_2O_3. Second, the process parameters of the RLT etch step using LIS exposure need further optimizing to reduce milling of the Pd layer and sidewall metallization. Finally, an investigation to reduce the Pd seed layer thickness and improve transmittance though the

film is needed before the Etch process approach is mature enough for commercial TCE application. The bulleted list below tabulates major learning items from experimental work using the Etch process approach.

- Pd catalyst is not corrupted by application of adhesion promoting polymeric material and subsequent RLT etch by LIS exposure
- Etch process flow is capable of high-quality selective electroless Cu plating within trenches
- LIS exposure mills Pd seed layer in addition to organic resist and adhesion promoter layers. Timed exposure requires further tuning.
- LIS etch is anisotropic in the vertical and horizontal directions
- 3 nm thick Pd seed layer can reduce transmittance through the material stack by up to 40%. Therefore, Pd seed layer thickness must be reduced.
- Amorphous SiO_2 is soluble in ECu plating solution and incompatible as a protection layer material

Chapter 4: Conclusions

This work demonstrates for the first time an imprint, etch and electroless plating process for fabricating nanoscale metal mesh TCEs on flexible PC substrates suitable for R2R processing. Performance of fabricated metal mesh electrodes using the proposed nanofabrication process surpasses predictive models for transmittance and conductivity with significant opportunity for optimization.

First, this thesis provides a detailed review of the current state-of-the-art in the field of TCEs and the physics informing metal mesh TCE film performance. Next, a method for simulating the optical behavior of metal mesh grids using the FDTD method was presented. Comparison of the FDTD simulation results to reported data validated its ability to capture nanophotonic phenomena and showed simulated transmittance to be within 5% of measured values. Next, a demonstration of a simple preliminary optimization procedure illustrated the use of geometric approximations to effectively identify optimum values for design parameters given a target TCE application. Combining results of FDTD simulations with optimization established a technical grounding for the competitiveness of metal mesh grids over ITO for use as TCEs.

Process development efforts towards a scalable R2R nanofabrication process to realize Cu metal mesh grids constitutes the second half of this thesis. This work successfully developed practical understanding of nanopatterning, pattern transfer and electroless Cu (ECu) deposition, its microstructure growth mechanisms and characterized electrical properties of ECu grown films. Knowledge gained then informed decisions pertaining to process flow options which incorporate techniques such as R2R GLAD and R2R Linear Ion Source (LIS) etching. Extensive experimentation identified the limitations of fabricating metal mesh electrodes using the GLAD approach, but went on to prove the viability of the LIS etch process method with promising results. The main objectives of the

research were successfully met and significant progress towards the research goal was demonstrated.

FUTURE WORK

Several avenues of research are available to expand upon the work presented here. This section briefly discusses such ideas for future research and offers recommendations for addressing each one.

Expansion of Modeling & Design Optimization Strategy

Haze is a critical property of TCEs especially for display applications, but is often ignored in literature due to the difficulty of its measurement and modeling. On possible method to predict its value is by interpolating results from near-field transmittance simulations and projecting the data to the far-field. Additionally, the optimization strategy presented in this thesis can be expanded to incorporate results from FDTD modeling with the aid of metamodeling. Integrating FDTD simulation results into a multi-objective genetic algorithm (MOGA) lends itself well to this design problem and should be explored as future work. Potential MOGA objective functions can include transmittance, sheet resistance and haze.

Identification of Protection Layer Material

As noted in Chapter 3, SiO2 is soluble in ECu plating solution due to its amorphous structure. Heat treatment to modify its crystalline structure is incompatible with flexible substrates because of the excessively high temperatures required. Alternative materials for the protection layer must, therefore, exhibit chemically resistance to the hot alkali nature of the ECu plating solution in the amorphous state. Al_2O_3 has been known to exhibit stability in aqueous alkaline media and has a relatively low boiling temperature compared to other alkali resilient metal-oxides [103]. Experimentation of the LIS etch process

approach employing Al2O3 as the protection layer should be sufficient to identify the feasibility of the material in fabrication. An alternative to using a protection layer is replacing the solvent containing adhesion promoter with a PC compatible polymer which may be a vapor-based treatment such as the one reported in Section 4.04.3.2.2 of reference [104]. Thus, the need for protection layer would be eliminated if the alternative promoter layer material allows for successful NIL directly on Pd coated PC.

Demonstration of Etch Process on R2R Scale

The problem of protection layer material is foreseeably the last major technical obstacle remaining in order for compatibility of the Etch process with scalable R2R fabrication. Translating and integrating individual process step to continuous inline processing on flexible substrates is, however, a significant undertaking. Accomplishment of this task should mark a milestone in fabrication of flexible electronics in general. Each individual process step will require revalidation and process parameter tuning using a similar methodology employed by this thesis. Exploratory testing is necessary to understand the differences of similar process steps between wafer-scale and R2R processing. Furthermore, morphological investigation should confirm any changes in ECu deposited film microstructure and plating selectivity using similar techniques but in the R2R version. Finally, Cu metal nano-mesh TCEs need demonstration and device performance and life-cycle testing to ensure their broad acceptance over ITO.

Modification of Etch Process for Selective Atomic Layer Deposition of Pd

Reducing the thickness of the Pd seed layer is essential to minimizing optical losses through the metal mesh TCE film. However, reducing the thickness of below 2 nm was shown to interfere with the ability to reliable initial electroless Cu deposition. One solution may be selective atomic layer deposition (ALD) of Pd only at the bottom of trenches where

metal-oxide is exposed. This has been demonstrated on many metal-oxide surfaces [105] and more recently on Al_2O_3 surfaces [106], [107]. If Al_2O_3 is suitable as the protection layer material, the integration of selective ALD of Pd would offer a solution for simultaneously improved transmittance and reliable ECu plating for low sheet resistance.

Bibliography

[1] B. Geffroy, P. le Roy, and C. Prat, "Organic light-emitting diode (OLED) technology: materials, devices and display technologies," *Polym. Int.*, vol. 55, no. 6, pp. 572–582, Jun. 2006.

[2] H. Hoppe and N. S. Sariciftci, "Organic solar cells: An overview," *J. Mater. Res.*, vol. 19, no. 7, pp. 1924–1945, Jul. 2004.

[3] "TFT-LCD manufacturing technology — current status and future prospect —," in *2007 International Workshop on Physics of Semiconductor Devices*, 2007, pp. 29–34.

[4] D.-J. Kim, H.-J. Kim, K.-W. Seo, K.-H. Kim, T.-W. Kim, and H.-K. Kim, "Indium-free, highly transparent, flexible $Cu_2O/Cu/Cu_2O$ mesh electrodes for flexible touch screen panels," *Sci. Rep.*, vol. 5, p. 16838, Nov. 2015.

[5] L. He and S. C. Tjong, "Nanostructured transparent conductive films: Fabrication, characterization and applications," *Mater. Sci. Eng. R Rep.*, vol. 109, pp. 1–101, Nov. 2016.

[6] H. B. Lee, W.-Y. Jin, M. M. Ovhal, N. Kumar, and J.-W. Kang, "Flexible Transparent Conducting Electrodes Based on Metal Mesh for Organic Optoelectronic Device Applications: A Review," *J. Mater. Chem. C*, Dec. 2018.

[7] D20 Committee, "Test Method for Haze and Luminous Transmittance of Transparent Plastics," ASTM International.

[8] C. Preston, Y. Xu, X. Han, J. N. Munday, and L. Hu, "Optical haze of transparent and conductive silver nanowire films," *Nano Res.*, vol. 6, no. 7, pp. 461–468, Jul. 2013.

[9] D. S. Hecht, L. Hu, and G. Irvin, "Emerging Transparent Electrodes Based on Thin Films of Carbon Nanotubes, Graphene, and Metallic Nanostructures," *Adv. Mater.*, vol. 23, no. 13, pp. 1482–1513, Apr. 2011.

[10] S. Bae, S. J. Kim, D. Shin, J.-H. Ahn, and B. H. Hong, "Towards industrial applications of graphene electrodes," *Phys. Scr.*, vol. 2012, no. T146, p. 014024, 2012.

[11] J. Gao, K. Kempa, M. Giersig, E. M. Akinoglu, B. Han, and R. Li, "Physics of transparent conductors," *Adv. Phys.*, vol. 65, no. 6, pp. 553–617, Nov. 2016.

[12] H. Kim *et al.*, "Electrical, optical, and structural properties of indium–tin–oxide thin films for organic light-emitting devices," *J. Appl. Phys.*, vol. 86, no. 11, pp. 6451–6461, Nov. 1999.

[13] S. D. Nehate, A. Prakash, P. D. Mani, and K. B. Sundaram, "Work Function Extraction of Indium Tin Oxide Films from MOSFET Devices," *ECS J. Solid State Sci. Technol.*, vol. 7, no. 3, pp. P87–P90, 2018.

[14] A. Kumar and C. Zhou, “The Race To Replace Tin-Doped Indium Oxide: Which Material Will Win?,” *ACS Nano*, vol. 4, no. 1, pp. 11–14, Jan. 2010.

[15] C.-K. Cho, W.-J. Hwang, K. Eun, S.-H. Choa, S.-I. Na, and H.-K. Kim, “Mechanical flexibility of transparent PEDOT:PSS electrodes prepared by gravure printing for flexible organic solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 12, pp. 3269–3275, Dec. 2011.

[16] H. Shi, C. Liu, Q. Jiang, and J. Xu, “Effective Approaches to Improve the Electrical Conductivity of PEDOT:PSS: A Review,” *Adv. Electron. Mater.*, vol. 1, no. 4, p. 1500017, Apr. 2015.

[17] R. Po, C. Carbonera, A. Bernardi, and N. Camaioni, “The role of buffer layers in polymer solar cells,” *Energy Env. Sci*, vol. 4, no. 2, pp. 285–310, 2011.

[18] X. Zhang *et al.*, “Highly conductive PEDOT:PSS transparent electrode prepared by a post-spin-rinsing method for efficient ITO-free polymer solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 144, pp. 143–149, Jan. 2016.

[19] T. Mochizuki, Y. Takigami, T. Kondo, and H. Okuzaki, “Fabrication of flexible transparent electrodes using PEDOT:PSS and application to resistive touch screen panels,” *J. Appl. Polym. Sci.*, vol. 135, no. 10, p. 45972, 2018.

[20] A. M. Nardes, M. Kemerink, M. M. de Kok, E. Vinken, K. Maturova, and R. A. J. Janssen, “Conductivity, work function, and environmental stability of PEDOT:PSS thin films treated with sorbitol,” *Org. Electron.*, vol. 9, no. 5, pp. 727–734, Oct. 2008.

[21] E. Vitoratos *et al.*, “Thermal degradation mechanisms of PEDOT:PSS,” *Org. Electron.*, vol. 10, no. 1, pp. 61–66, Feb. 2009.

[22] M. J. Allen, V. C. Tung, and R. B. Kaner, “Honeycomb Carbon: A Review of Graphene,” *Chem. Rev.*, vol. 110, no. 1, pp. 132–145, Jan. 2010.

[23] J. Wu *et al.*, “Organic Light-Emitting Diodes on Solution-Processed Graphene Transparent Electrodes,” *ACS Nano*, vol. 4, no. 1, pp. 43–48, Jan. 2010.

[24] R. R. Nair *et al.*, “Fine Structure Constant Defines Visual Transparency of Graphene,” *Science*, vol. 320, no. 5881, pp. 1308–1308, Jun. 2008.

[25] C. Lee, X. Wei, J. W. Kysar, and J. Hone, “Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene,” *Science*, vol. 321, no. 5887, pp. 385–388, Jul. 2008.

[26] S. Pang, Y. Hernandez, X. Feng, and K. Müllen, “Graphene as Transparent Electrode Material for Organic Electronics,” *Adv. Mater.*, vol. 23, no. 25, pp. 2779–2795, Jul. 2011.

[27] S. Bae *et al.*, “Roll-to-roll production of 30-inch graphene films for transparent electrodes,” *Nat. Nanotechnol.*, vol. 5, no. 8, pp. 574–578, Aug. 2010.

[28] H. Park, J. A. Rowehl, K. K. Kim, V. Bulovic, and J. Kong, "Doped graphene electrodes for organic solar cells," *Nanotechnology*, vol. 21, no. 50, p. 505204, Dec. 2010.

[29] K. S. Kim *et al.*, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature*, vol. 457, no. 7230, pp. 706–710, Feb. 2009.

[30] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, no. 6348, pp. 56–58, Nov. 1991.

[31] B. S. Shim, Z. Tang, M. P. Morabito, A. Agarwal, H. Hong, and N. A. Kotov, "Integration of Conductivity, Transparency, and Mechanical Strength into Highly Homogeneous Layer-by-Layer Composites of Single-Walled Carbon Nanotubes for Optoelectronics," *Chem. Mater.*, vol. 19, no. 23, pp. 5467–5474, Nov. 2007.

[32] J. L. Bahr, E. T. Mickelson, M. J. Bronikowski, R. E. Smalley, and J. M. Tour, "Dissolution of small diameter single-wall carbon nanotubes in organic solvents?," *Chem. Commun.*, no. 2, pp. 193–194, 2001.

[33] H. T. Ham, Y. S. Choi, and I. J. Chung, "An explanation of dispersion states of single-walled carbon nanotubes in solvents and aqueous surfactant solutions using solubility parameters," *J. Colloid Interface Sci.*, vol. 286, no. 1, pp. 216–223, Jun. 2005.

[34] H.-Z. Geng, D. S. Lee, K. K. Kim, G. H. Han, H. K. Park, and Y. H. Lee, "Absorption spectroscopy of surfactant-dispersed carbon nanotube film: Modulation of electronic structures," *Chem. Phys. Lett.*, vol. 455, no. 4–6, pp. 275–278, Apr. 2008.

[35] R. C. Tenent *et al.*, "Ultrasmooth, Large-Area, High-Uniformity, Conductive Transparent Single-Walled-Carbon-Nanotube Films for Photovoltaics Produced by Ultrasonic Spraying," *Adv. Mater.*, vol. 21, no. 31, pp. 3210–3216, Aug. 2009.

[36] J. Li, L. Hu, L. Wang, Y. Zhou, G. Grüner, and T. J. Marks, "Organic Light-Emitting Diodes Having Carbon Nanotube Anodes," *Nano Lett.*, vol. 6, no. 11, pp. 2472–2477, Nov. 2006.

[37] T. Sannicolo, M. Lagrange, A. Cabos, C. Celle, J.-P. Simonato, and D. Bellet, "Metallic Nanowire-Based Transparent Electrodes for Next Generation Flexible Devices: a Review," *Small*, vol. 12, no. 44, pp. 6052–6075, Nov. 2016.

[38] W. Cao, J. Li, H. Chen, and J. Xue, "Transparent electrodes for organic optoelectronic devices: a review," *J. Photonics Energy*, vol. 4, no. 1, p. 040990, Oct. 2014.

[39] S. M. Bergin, Y.-H. Chen, A. R. Rathmell, P. Charbonneau, Z.-Y. Li, and B. J. Wiley, "The effect of nanowire length and diameter on the properties of transparent, conducting nanowire films," *Nanoscale*, vol. 4, no. 6, pp. 1996–2004, Mar. 2012.

[40] D.-S. Leem, A. Edwards, M. Faist, J. Nelson, D. D. C. Bradley, and J. C. de Mello, "Efficient Organic Solar Cells with Solution-Processed Silver Nanowire Electrodes," *Adv. Mater.*, vol. 23, no. 38, pp. 4371–4375, 2011.

[41] J. Zhao, H. Sun, S. Dai, Y. Wang, and J. Zhu, "Electrical Breakdown of Nanowires," *Nano Lett.*, vol. 11, no. 11, pp. 4647–4651, Nov. 2011.

[42] J. L. Elechiguerra, L. Larios-Lopez, C. Liu, D. Garcia-Gutierrez, A. Camacho-Bragado, and M. J. Yacaman, "Corrosion at the Nanoscale: The Case of Silver Nanowires and Nanoparticles," *Chem. Mater.*, vol. 17, no. 24, pp. 6042–6052, Nov. 2005.

[43] B. Stahlmecke, F.-J. Meyer zu Heringdorf, L. I. Chelaru, M. Horn-von Hoegen, G. Dumpich, and K. R. Roos, "Electromigration in self-organized single-crystalline silver nanowires," *Appl. Phys. Lett.*, vol. 88, no. 5, p. 053122, Jan. 2006.

[44] L. Hu, H. Wu, and Y. Cui, "Metal nanogrids, nanowires, and nanofibers for transparent electrodes," *MRS Bull.*, vol. 36, no. 10, pp. 760–765, Oct. 2011.

[45] C. Cocoyer *et al.*, "Implementation of submicrometric periodic surface structures toward improvement of organic-solar-cell performances," *Appl. Phys. Lett.*, vol. 88, no. 13, p. 133108, Mar. 2006.

[46] C. Min, J. Li, G. Veronis, J.-Y. Lee, S. Fan, and P. Peumans, "Enhancement of optical absorption in thin-film organic solar cells through the excitation of plasmonic modes in metallic gratings," *Appl. Phys. Lett.*, vol. 96, no. 13, p. 133302, Mar. 2010.

[47] F. L. M. Sam, C. A. Mills, L. J. Rozanski, and S. R. P. Silva, "Thin film hexagonal gold grids as transparent conducting electrodes in organic light emitting diodes," *Laser Photonics Rev.*, vol. 8, no. 1, pp. 172–179, 2014.

[48] W.-K. Kim *et al.*, "Cu Mesh for Flexible Transparent Conductive Electrodes," *Sci. Rep.*, vol. 5, p. 10715, Jun. 2015.

[49] M.-G. Kang and L. J. Guo, "Nanoimprinted Semitransparent Metal Electrodes and Their Application in Organic Light-Emitting Diodes," *Adv. Mater.*, vol. 19, no. 10, pp. 1391–1396, May 2007.

[50] N. Kwon, K. Kim, S. Sung, I. Yi, and I. Chung, "Highly conductive and transparent Ag honeycomb mesh fabricated using a monolayer of polystyrene spheres," *Nanotechnology*, vol. 24, no. 23, p. 235205, 2013.

[51] M. Kang, H. J. Park, S. H. Ahn, T. Xu, and L. J. Guo, "Toward Low-Cost, High-Efficiency, and Scalable Organic Solar Cells with Transparent Metal Electrode and Improved Domain Morphology," *IEEE J. Sel. Top. Quantum Electron.*, vol. 16, no. 6, pp. 1807–1820, Nov. 2010.

[52] M.-G. Kang, M.-S. Kim, J. Kim, and L. J. Guo, "Organic Solar Cells Using Nanoimprinted Transparent Metal Electrodes," *Adv. Mater.*, vol. 20, no. 23, pp. 4408–4413, Dec. 2008.

[53] O. Y. Kwon, Y. S. Lee, W. J. Lee, Y. M. Jang, and S.-H. Choa, "The Effects of Grid Shape on Flexibility and Durability of Flexible Transparent Metal Grid Films," *J. Korean Soc. Precis. Eng.*, vol. 35, no. 5, pp. 551–559, May 2018.

[54] L. Li *et al.*, "Fabrication of Flexible Transparent Electrode with Enhanced Conductivity from Hierarchical Metal Grids," *ACS Appl. Mater. Interfaces*, vol. 9, no. 45, pp. 39110–39115, Nov. 2017.

[55] D. S. Ghosh, T. L. Chen, and V. Pruneri, "High figure-of-merit ultrathin metal transparent electrodes incorporating a conductive grid," *Appl. Phys. Lett.*, vol. 96, no. 4, p. 041109, Jan. 2010.

[56] A. Khan *et al.*, "High-Performance Flexible Transparent Electrode with an Embedded Metal Mesh Fabricated by Cost-Effective Solution Process," *Small*, vol. 12, no. 22, pp. 3021–3030, Jun. 2016.

[57] M. Aryal, J. Geddes, O. Seitz, J. Wassei, I. McMackin, and B. Kobrin, "16.1: Sub-Micron Transparent Metal Mesh Conductor for Touch Screen Displays," *SID Symp. Dig. Tech. Pap.*, vol. 45, no. 1, pp. 194–196, 2014.

[58] S.-I. Chung, P. K. Kim, T.-G. Ha, and J. T. Han, "High-performance flexible transparent nanomesh electrodes," *Nanotechnology*, Jan. 2019.

[59] D. Li, T. Han, and H. Ruan, "Solution-Assembled Ordered Grids Constructed with Silver Nanowires as Transparent Conductive Electrodes," *ACS Omega*, vol. 3, no. 7, pp. 7191–7195, Jul. 2018.

[60] S. Han *et al.*, "High-performance solution-processable flexible and transparent conducting electrodes with embedded Cu mesh," *J. Mater. Chem. C*, vol. 6, no. 16, pp. 4389–4395, 2018.

[61] F. M. Wisser, K. Eckhardt, W. Nickel, W. Böhlmann, S. Kaskel, and J. Grothe, "Highly transparent metal electrodes via direct printing processes," *Mater. Res. Bull.*, vol. 98, pp. 231–234, Feb. 2018.

[62] S. Yu *et al.*, "Area-Selective Lift-Off Mechanism Based on Dual-Triggered Interfacial Adhesion Switching: Highly Facile Fabrication of Flexible Nanomesh Electrode," *ACS Nano*, vol. 11, no. 4, pp. 3506–3516, Apr. 2017.

[63] X. Chen *et al.*, "Hybrid Printing Metal-mesh Transparent Conductive Films with Lower Energy Photonically Sintered Copper/tin Ink," *Sci. Rep.*, vol. 7, no. 1, p. 13239, Oct. 2017.

[64] X. Chen *et al.*, "Embedded Ag/Ni Metal-Mesh with Low Surface Roughness As Transparent Conductive Electrode for Optoelectronic Applications," *ACS Appl. Mater. Interfaces*, vol. 9, no. 42, pp. 37048–37054, Oct. 2017.

[65] B. Sciacca, J. van de Groep, A. Polman, and E. C. Garnett, "Solution-Grown Silver Nanowire Ordered Arrays as Transparent Electrodes," *Adv. Mater. Deerfield Beach Fla*, vol. 28, no. 5, pp. 905–909, Feb. 2016.

[66] G. Yang, B. Liu, K. Cheng, and Z. Du, “Modulation of optical transmittance and conductivity by the period, linewidth and height of Au square mesh electrodes,” *Opt. Express*, vol. 23, no. 3, pp. A62–A70, Feb. 2015.

[67] J. Schneider, P. Rohner, D. Thureja, M. Schmid, P. Galliker, and D. Poulikakos, “Electrohydrodynamic NanoDrip Printing of High Aspect Ratio Metal Grid Transparent Electrodes,” *Adv. Funct. Mater.*, vol. 26, no. 6, pp. 833–840, 2015.

[68] H.-J. Choi, S. Choo, P.-H. Jung, J.-H. Shin, Y.-D. Kim, and H. Lee, “Uniformly embedded silver nanomesh as highly bendable transparent conducting electrode,” *Nanotechnology*, vol. 26, no. 5, p. 055305, 2015.

[69] J. H. Park *et al.*, “Flexible and Transparent Metallic Grid Electrodes Prepared by Evaporative Assembly,” *ACS Appl. Mater. Interfaces*, vol. 6, no. 15, pp. 12380–12387, Aug. 2014.

[70] H.-J. Kim *et al.*, “High-Durable AgNi Nanomesh Film for a Transparent Conducting Electrode,” *Small*, vol. 10, no. 18, pp. 3767–3774, 2014.

[71] J. van de Groep, P. Spinelli, and A. Polman, “Transparent Conducting Silver Nanowire Networks,” *Nano Lett.*, vol. 12, no. 6, pp. 3138–3144, Jun. 2012.

[72] D. J. Resnick *et al.*, “Imprint lithography: lab curiosity or the real NGL,” in *Emerging Lithographic Technologies VII*, 2003, vol. 5037, pp. 12–24.

[73] B. Kobrin, E. S. Barnard, M. L. Brongersma, M. K. Kwak, and L. J. Guo, “Rolling mask nanolithography: the pathway to large area and low cost nanofabrication,” in *Advanced Fabrication Technologies for Micro/Nano Optics and Photonics V*, 2012, vol. 8249, p. 82490O.

[74] S. H. Ahn and L. J. Guo, “Large-Area Roll-to-Roll and Roll-to-Plate Nanoimprint Lithography: A Step toward High-Throughput Application of Continuous Nanoimprinting,” *ACS Nano*, vol. 3, no. 8, pp. 2304–2310, Aug. 2009.

[75] S. H. Ahn and L. J. Guo, “High-Speed Roll-to-Roll Nanoimprint Lithography on Flexible Plastic Substrates,” *Adv. Mater.*, vol. 20, no. 11, pp. 2044–2049, 2008.

[76] S. V. Sreenivasan, “Nanoscale Manufacturing Enabled by Imprint Lithography,” *MRS Bull.*, vol. 33, no. 9, pp. 854–863, Sep. 2008.

[77] D. J. Resnick, S. V. Sreenivasan, and C. G. Willson, “Step & flash imprint lithography,” *Mater. Today*, vol. 8, no. 2, pp. 34–42, Feb. 2005.

[78] “Canon Nanotechnologies,” *Canon Nanotechnologies*. [Online]. Available: http://cnt.canon.com/. [Accessed: 18-Apr-2019].

[79] S. V. Sreenivasan, “Nanoimprint lithography steppers for volume fabrication of leading-edge semiconductor integrated circuits,” *Microsyst. Nanoeng.*, vol. 3, p. 17075, Sep. 2017.

[80] I. McMackin *et al.*, “Step and Repeat UV nanoimprint lithography tools and processes,” in *Emerging Lithographic Technologies VIII*, 2004, vol. 5374, pp. 222–232.

[81] J. Hautcoeur *et al.*, “Transparency and electrical properties of meshed metal films,” *Thin Solid Films*, vol. 519, no. 11, pp. 3851–3858, Mar. 2011.

[82] Y. Jang, J. Kim, and D. Byun, “Invisible metal-grid transparent electrode prepared by electrohydrodynamic (EHD) jet printing,” *J. Phys. Appl. Phys.*, vol. 46, no. 15, p. 155103, 2013.

[83] P. B. Catrysse and S. Fan, “Nanopatterned Metallic Films for Use As Transparent Conductive Electrodes in Optoelectronic Devices,” *Nano Lett.*, vol. 10, no. 8, pp. 2944–2949, Aug. 2010.

[84] “High-Performance Nanophotonic Simulation Software,” *Lumerical*. [Online]. Available: https://www.lumerical.com/. [Accessed: 13-Apr-2019].

[85] “Understanding the FDTD Method.” [Online]. Available: https://www.eecs.wsu.edu/~schneidj/ufdtd/. [Accessed: 26-Jan-2019].

[86] E. D. Palik, E. D. Palik, and E. D. Palik, *Handbook of Optical Constants of Solids*. San Diego, UNITED STATES: Elsevier Science & Technology, 1998.

[87] M. Dressel and G. Grüner, *Electrodynamics of Solids : Optical Properties of Electrons in Matter*. Cambridge: Cambridge University Press, 2002.

[88] X. Cui, D. A. Hutt, and P. P. Conway, “Evolution of microstructure and electrical conductivity of electroless copper deposits on a glass substrate,” *Thin Solid Films*, vol. 520, no. 19, pp. 6095–6099, Jul. 2012.

[89] “Refractive index of (C16H14O3)n (Polycarbonate, PC) - Sultanova.” [Online]. Available: https://refractiveindex.info/?shelf=organic&book=polycarbonate&page=Sultanova. [Accessed: 16-Apr-2019].

[90] M. I. Inc, “World Class Touch Sensor Performance For Displays Achieved Using Molecular Imprints’ J-FIL® Technology.” [Online]. Available: https://www.prnewswire.com/news-releases/world-class-touch-sensor-performance-for-displays-achieved-using-molecular-imprints-j-fil-technology-281506191.html. [Accessed: 16-Apr-2019].

[91] B. M. Gawlik *et al.*, “Structural coloration with hourglass-shaped vertical silicon nanopillar arrays,” *Opt. Express*, vol. 26, no. 23, pp. 30952–30968, Nov. 2018.

[92] wkm, “Coating & Laminating Vacuum Pilot,” *Emerson and Renwick*. .

[93] V. M. Dubin, Y. Shacham-Diamand, B. Zhao, P. K. Vasudev, and C. H. Ting, “Selective and Blanket Electroless Copper Deposition for Ultralarge Scale Integration,” *J. Electrochem. Soc.*, vol. 144, no. 3, pp. 898–908, Mar. 1997.

[94] Y. Shacham-Diamand, V. Dubin, and M. Angyal, “Electroless copper deposition for ULSI,” *Thin Solid Films*, vol. 262, no. 1, pp. 93–103, Jun. 1995.

[95] H.-D. Liu, Y.-P. Zhao, G. Ramanath, S. P. Murarka, and G.-C. Wang, “Thickness dependent electrical resistivity of ultrathin (<40 nm) Cu films,” *Thin Solid Films*, vol. 384, no. 1, pp. 151–156, Mar. 2001.

[96] M. Radoeva and B. Radoev, “Ohm resistivity of electroless copper layers as a function of their thicknesses,” *J. Mater. Sci.*, vol. 30, no. 9, pp. 2215–2219, May 1995.

[97] M. M. Hawkeye and M. J. Brett, “Glancing angle deposition: Fabrication, properties, and applications of micro- and nanostructured thin films,” *J. Vac. Sci. Technol. A*, vol. 25, no. 5, pp. 1317–1335, Jul. 2007.

[98] F. Y. Xu, S. V. Sreenivasan, and E. B. Fletcher, “United States Patent: 8808808 - Method for imprint lithography utilizing an adhesion primer layer,” 8808808, 19-Aug-2014.

[99] S. N. Kasarova, N. G. Sultanova, C. D. Ivanov, and I. D. Nikolov, “Analysis of the dispersion of optical plastic materials,” *Opt. Mater.*, vol. 29, no. 11, pp. 1481–1490, Jul. 2007.

[100] S. M. Baumann, C. C. Martner, D. W. Martin, R. J. Blattner, and A. J. Braundmeier, “A study of electron beam evaporated SiO2, TiO2, and Al2O2 films using RBS, HFS, and SIMS,” *Nucl. Instrum. Methods Phys. Res. Sect. B Beam Interact. Mater. At.*, vol. 45, no. 1, pp. 664–668, Jan. 1990.

[101] “Kurt J. Lesker Company | Silicon Dioxide SiO2 Pieces Evaporation Materials | Vacuum Science Is Our Business.” [Online]. Available: https://www.lesker.com/newweb/deposition_materials/depositionmaterials_evaporationmaterials_1.cfm?pgid=si2. [Accessed: 22-Mar-2019].

[102] N. Sultanova, S. Kasarova, and I. Nikolov, “Dispersion Properties of Optical Polymers,” *Acta Phys. Pol. A*, vol. 116, no. 4, pp. 585–587, Oct. 2009.

[103] “Alkali-Resistant Materials,” *TheFreeDictionary.com*. [Online]. Available: https://encyclopedia2.thefreedictionary.com/Alkali-Resistant+Materials. [Accessed: 23-Apr-2019].

[104] T. Singh, S. V. Sreenivasan, J. Choi, P. Schumaker, and F. Xu, “Status of UV Imprint Lithography for Nanoscale Manufacturing,” in *Reference Module in Materials Science and Materials Engineering*, Elsevier, 2017.

[105] G. A. Ten Eyck, S. Pimanpang, H. Bakhru, T.-M. Lu, and G.-C. Wang, “Atomic Layer Deposition of Pd on an Oxidized Metal Substrate,” *Chem. Vap. Depos.*, vol. 12, no. 5, pp. 290–294, 2006.

[106] J. W. Elam *et al.*, “Atomic layer deposition of palladium films on Al2O3 surfaces,” *Thin Solid Films*, vol. 515, no. 4, pp. 1664–1673, Dec. 2006.

[107] D. N. Goldstein and S. M. George, “Surface poisoning in the nucleation and growth of palladium atomic layer deposition with Pd(hfac)2 and formalin,” *Thin Solid Films*, vol. 519, no. 16, pp. 5339–5347, Jun. 2011.

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