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Epitaxial Germanium via Ge:C and its use in Non-classical Semiconductor Devices

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Epitaxial Germanium via Ge:C and its use in Non-classical Semiconductor Devices

by

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Dedication

To my family.

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Epitaxial Germanium via Ge:C and its use in Non-classical Semiconductor Devices

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The microelectronics industry has been using Silicon (Si) as the primary material for complementary metal-oxide-semiconductor (CMOS) chip fabrication for more than six decades. Throughout this time, these CMOS devices have gotten exponentially smaller, faster, and cheaper. While new materials and fabrication processes have been slowly added over the years, the CMOS device of today is largely the same as it was decades ago. However, field-effect transistors (FETs) have now scaled so far that Si is approaching physical limits. Thus, new channel materials and new fundamental device structures are being investigated to replace traditional CMOS.

Germanium is one of the prime candidates to replace Si in the FET channel, with its increased electron and hole mobilities compared to Si. Perhaps more importantly, it is compatible with the existing Si manufacturing techniques by epitaxially growing thin layers of Ge crystal on the starting Si wafer. Because these two crystals do not share a

lattice constant, there will inevitably be crystal defects in the thin Ge layer that can be catastrophic for device functionality. Several approaches have been introduced to reduce defects, but most of them are wastefully thick ($> 1\mu m$) or require complex manufacturing methods. In this work, we utilize an extremely thin ($\sim 10nm$) buffer layer of carbon-doped Ge (Ge:C) to grow Ge and SiGe layers for FET and virtual substrate applications with improved crystalline quality and reduced surface roughnesses.

These thin Ge layers not only offer new pathways for MOSFETs, but can also be used in non-classical structures. Semiconductor nanowires (NWs) and tunnel-FETs (TFETs) are two of the most promising device architectures, and both can be used with Ge. This dissertation presents a simulated Si/Ge heterostructure interface TFET that can be fabricated on a virtual substrate made with the Ge:C buffer layer. Detailed analysis on device operation is given. Also in this work is the fabrication process for individually addressable Ge NW-FETs. The NWs offer excellent electrostatic gate control through reduced dimensions and offer another potential pathway for Ge in a post-CMOS world.

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CHAPTER I

Introduction

1.1 Moore's Law and CMOS Scaling

Since the advent of the mass produced microchip in the semiconductor industry, the primary metric for improvement has been to scale the transistors to smaller dimensions while simultaneously achieving higher performance. In the mid-1960s, Gordon Moore of Fairchild Semiconductor made the observation that the number of transistors fabricated on a chip could be increased exponentially, and that was the metric that industry continued to strive for [1]. Now coined "Moore's Law", we have witnessed transistor count approximately doubling every ~two years for several decades, enabling faster speeds and lower costs at each node. Dennard's scaling theory [2] showed that by maintaining a constant electric field in the gate dielectric, a reduction in lateral physical dimensions would improve performance while not affecting power density. By simultaneously reducing operating voltages,

reductions in power density could even be achieved. Combined with Moore's Law, the semiconductor industry was able to increase chip performance while decreasing costs via scaling for the next several decades.

Naturally, this scaling cannot continue indefinitely. Physical limitations really became clear as gate lengths decreased and approached the $100nm$ range. Slowly but surely, the materials used for the many 'pieces' of the microchip were replaced. Copper replaced Al for back end-of-line (BEOL) interconnects. Also in the BEOL, low dielectric (low-κ) materials have replaced SiO_2 to separate the Cu lines. In the front end-of-line (FEOL), the $45nm$ node first introduced the high-κ - metal gate stack. This solved two problems that were detrimental for scaling. First, the SiO_2 gate oxide had become so small (sub-$2nm$) that current was tunneling directly from the gate to the channel and introducing wasted power consumption. The high-κ oxide HfO_2 was introduced as a way to allow a physically thicker gate oxide that still provided channel control via the electronic coupling of a high dielectric constant material. Secondly, the metal gate was introduced to solve the problem of poly-Si depletion at the interface causing lower inversion currents. Another place that materials changed is in the source and drain regions, where SiGe and various silicides (ex: NiSi) have been used to reduce parasitic resistances. Despite all of these changes, the core piece of the microchip — the Si channel of the MOSFET — has remained the same.

The only real deviation from standard Si has been to change it by applying mechanical strain. At the $90nm$ node, Intel introduced the first use of strained Si. By using a tensile strain of ~1%, created via a SiN encapsulation layer, a boost of more than ~10% could be achieved in drain current (I_D) in nMOS devices [3]. On the other hand, pMOS devices require a compressive stress in the channel to boost I_D. For this, Intel utilized heavily doped SiGe:B source/drains. In addition to the lower resistivity provided by the SiGe:B for

lowering contact parasitic resistances, the larger Ge atoms had the effect of compressing the Si channel in the middle and resulted in a surprising ~30% boost in I_D [3]. This was particularly beneficial for CMOS, since pMOS devices are physically larger to compensate for smaller I_D, making CMOS slightly more symmetric with Ge.

Yet again, however, further scaling is causing problems — these strain performance benefits are becoming less pronounced as transistor period decreases, and new methods for increasing performance must be considered. It appears that it is finally time to look beyond Si in our efforts to continue performance improvements in planar CMOS. Germanium is one of the primary candidates for such replacement.

1.2 Germanium — a Silicon CMOS Replacement

The first experimentally demonstrated transistor was a point-contact transistor created using a Ge crystal at Bell Labs in the 1940s. Despite this immediate head start for Ge, Si has always been the center of the CMOS world due primarily to its terrific native oxide, SiO_2. As scaling has pushed us into the sub-$100nm$ regime, this primary benefit has been lost as the industry moved to high-κ dielectrics. Thus, new materials that provide performance enhancements, such as Ge, are being actively pursued.

Germanium exhibits higher electron (μ_e ~2x) and hole (μ_h ~4x) mobilities compared to Si, which is key to providing faster performance. Mobility is shown to directly relate to source injection velocity (ν_{inj}), which in highly scaled devices is critical for achieving high I_D [4]. Germanium has the highest known μ_h for known semiconductor materials and provides the most symmetry between μ_e and μ_h. A comparison of material properties of Ge and other common semiconductors is provided in table 1.1.

Table 1.1: Properties of common semiconductors ($T = 300K$).

Semiconductor	$\mu_e(cm^2/Vs)$	$\mu_h(cm^2/Vs)$	$E_g(eV)$	a(Å)
Si	1500	450	1.12	5.431
Ge	3900	1900	0.67	5.658
GaAs	8500	400	1.42	5.653
InP	5400	200	1.34	5.869
InAs	40000	500	0.36	6.058
InSb	77000	850	0.17	6.479

Another benefit of Ge is the smaller bandgap of 0.67 eV. As physical dimensions of transistors have shrunk, so have the operating voltages. As operating voltages have hit 1.3 V and below, it becomes somewhat difficult to invert a highly doped Si device with a bandgap of 1.1 eV. Having a smaller bandgap allows a lower gate voltage to invert the channel. That being said, there are disadvantages as well. For instance, band-to-band tunneling (BTBT) currents will increase with a smaller bandgap, since for a given amount of band bending, the conduction and valence bands are energetically closer. Similarly, the smaller barrier leads to increased other short channel effects like drain-induced barrier lowering (DIBL). The challenge of the future will be to lower the operating voltages to suppress these effects while still providing sufficient on-state current for high performance.

1.3 Germanium Challenges

Naturally there are several challenges accompanying the use of Ge in high volume manufacturing (HVM). Germanium is more brittle than Si, and would thus need either extra care during processing or extra wafer thicknesses to make up for the fragility. Since Ge is already far more expensive than Si, making it thicker would just compound the cost

problem. Another aspect that is worse for Ge is thermal conductivity. High performance Si chips already exhibit thermal design challenges that must be met. At a minimum, heat sinks and air-forced cooling are required to keep modern CPUs in proper operating environments. Unfortunately, this problem would only get worse with a Ge substrate chip, since the thermal conductivity of Ge is lower than that of Si.

One way to get around both of these problems is to use chemical vapor deposition (CVD) to epitaxially grow a thin Ge layer atop a Si substrate. This provides the mechanical strength and thermal properties of the Si with the performance boost of Ge, since the functional area for transistors is at the surface of the crystal.

1.3.1 Germanium Integration on Silicon

Chemically, Ge shares many properties with Si. Both are column IV semiconductors with 4 valence shell electrons forming a diamond lattice. Each atom shares these four electrons with its nearest neighbors in a tetrahedral orientation, and this arrangement is the basis for the observed similarities. As such, Si and Ge can be completely alloyed together in the form of Si_xGe_{x-1}, with $0 \leq x \leq 1$, and pure Ge can be grown heteroepitaxially on Si via the CVD method.

Figure 1.1 shows the very simple process used to heteroepitaxially grow Ge on Si. Elevated temperatures ($\geq 330°$C) and exposure to a Ge-containing precursor gas (usually GeH_4) cause a Ge crystal to grow atop a Si seed crystal (wafer). For any heteroepitaxial system, growth will proceed in one of three ways, as outlined in Fig. 1.3. Germanium heteroepitaxy on Si follows the S-K growth mode, where there is initial layer coverage that switches to islanded growth.

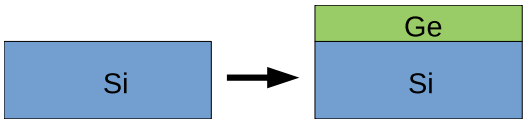

Figure 1.1: Process flow for Ge heteroepitaxy. Germane gas decomposes at elevated temperatures on the Si crystal to 'grow' a Ge layer.

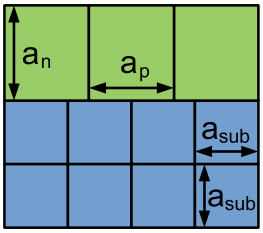

Figure 1.2: Diagram showing heteroepitaxial lattice mismatch between relaxed Ge (a_n=a_p) and underlying Si. Lines represent atomic bonds. Strained Ge growth yields $a_n > a_p \approx a_{sub}$.

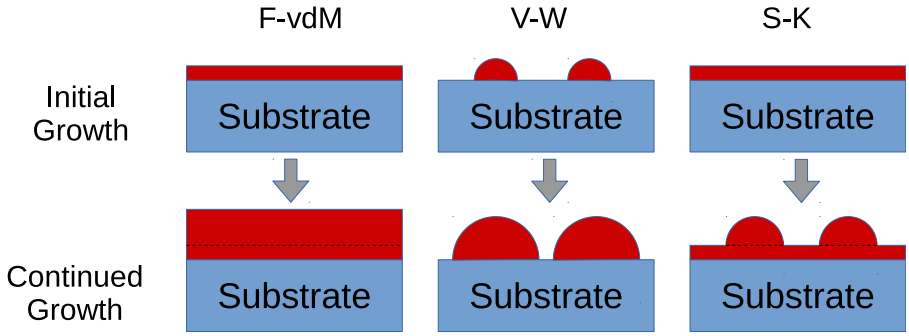

Figure 1.3: The three primary growth modes for heteroepitaxy: (1) Frank - van der Merwe (F-vdM), (2) Volmer-Weber (V-W), and Stranski-Krastanow (S-K).

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Ideally the substrate and new Ge layer would be contiguous and single crystal, but in reality there are many defects created due to the lattice mismatch between the materials, as $a_{Ge} > a_{Si}$. Figure 1.2 shows the combined releaxed Si and Ge layers. During growth, initially the Ge and Si atoms align, yielding $a_{n,Ge} > a_{p,Ge} = a_{Si}$. After the film thickness surpasses the critical thickness, t_C, the Ge film partially relaxes via defect formation and $a_n > a_p \approx a_{sub}$. For high-T Ge growth, the energetically preferred defect formation is the islanding of the S-K growth mode. If temperatures are kept very low during growth ($\leq$ ~350°C), slow layer-by-layer F-vdM growth can occur, where the relaxation mechanism

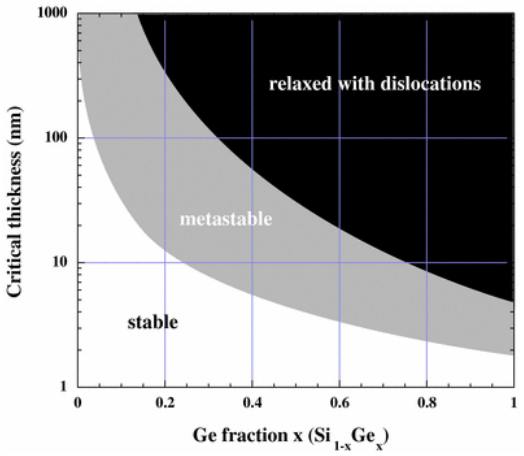

Figure 1.4: A map of the critical thickness of $Si_{1-x}Ge_x$ layers heteroepitaxially grown on Si. Pure Ge shows a t_C of just a few monolayers before metastable conditions set in [5].

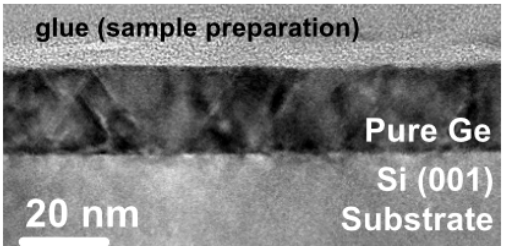

Figure 1.5: A cross sectional TEM image of a ~$20nm$ Ge heteroepitaxial layer. A multitude of defects can be observed due to the lattice mismatch [6].

is typically threading dislocations. Much of the UHV-CVD growth in our system is of this low-T variety. Figure 1.4 shows the transition between fully strained and partially relaxed states, and 1.5 showcases potential defects in the epitaxial layer.

These defects are a considerable problem for planar CMOS. Typical threading dislocation densities (T_{DD}) for Ge layers grown on Si range from sub 10^8 to more than $10^{11}cm^{-2}$ [7]. Even for the better cases, this leaves an average of ~1 defect per 100 transistors at the $32nm$ node. Considering that modern processors contain more than a billion transistors, it is easy to see that at a minimum there will be serious power leakage, and at a maximum complete CPU failure. These defects propogate to the surface and cause surface roughness which causes additional scattering mechanisms and reduces mobility in the channel. Reducing these defect levels and forming smoother surfaces is critical for Ge adoption for channel materials. Section 2.3 discusses one method to reduce surface roughness for Ge thin films.

Many approaches have been introduced to achieve high-quality Ge heteroepitaxy on Si. Perhaps the most common, and also frequently used in our UHV-CVD chamber, is the 2-step low-temperature (LT) high-temperature (HT) approach. First introduced by Colace et. al. at Stanford, it first employs a LT Ge film of ~50 nm, and after this the T is raised to ~600°C before growth continues (at faster growth rates) [8]. It is often accompanied by H_2 cyclic annealing to reduce threading dislocation density (TDD) [9]. However, this method favors lower TDD at the surface and leaves high defect densities near the interface (see Fig. 1.6). Other methods used by researchers include graded buffers [9], surfactant mediated [10], Ge condensation [11], and aspect ratio trapping [12]. All of these methods require either wasteful thick films, complex processing, or a combination thereof.

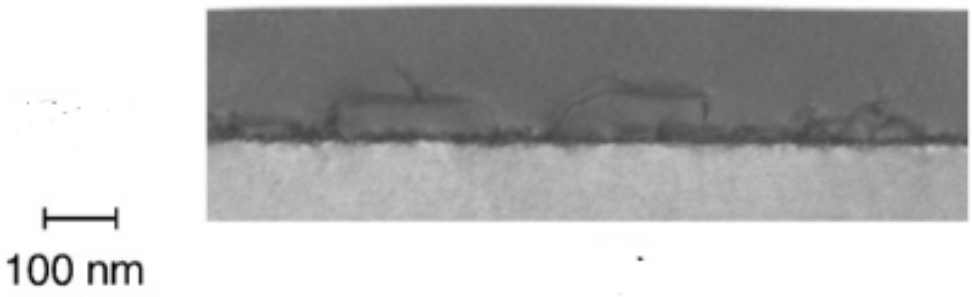

Figure 1.6: XTEM image showing the high concentration of defects near the heterointerface, but less near the Ge surface for LT+HT (+Anneal) Ge-on-Si samples. From [13].

1.3.2 Germanium nMOSFET Challenges

One of the largest challenges for Ge lies with n-channel MOSFETs. While pMOSFETs have experimentally demonstrated extremely high mobilites both in bulk and quantum well

devices (QWFETs) [14][15], Ge nMOSFETs have generally underperformed relative to their intrinsic electron mobility [16] and only recently have they surpassed the universal silicon mobility [17]. One of the primary causes of the diminished performance is the poor quality of Ge n^+/p junctions.

Table 1.2: Solid Solubilites (SS) of Dopants in Ge and Si [18].

Dopant	Dopant Type	SS in Ge (cm^{-3})	SS in Si (cm^{-3})
P	n	2.0×10^{20}	1.3×10^{21}
As	n	8.1×10^{19}	1.5×10^{21}
Sb	n	1.2×10^{19}	7.0×10^{19}
B	p	5.5×10^{18}	4.1×10^{20}
Ga	p	4.9×10^{20}	4.0×10^{19}

The n^+/p junctions in Ge FETs cause problems for a few reasons. First, n-type dopants exhibit comparatively low solid solubility levels and even lower activation levels compared to Si (Table 1.2) [19]. This results in high source/drain (S/D) series resistances that limit drive current in the devices. Coupled with this is the fact that the n-type dopants diffuse rapidly in Ge. This makes ultra-shallow junctions difficult to form and forces the use of fabrication processes with low thermal budgets (which is also detrimental to getting higher dopant activation). Another downfall for Ge n^+/p jucntions is that ion implantation is the predominant method for S/D junction formation in both production and research environments. Because of the low thermal budget and fast dopant diffusion mentioned above, implantation end-of-range (EOR) defects are not thermally annihilated and this may be cause for high off-state currents observed in Ge nFETs [19] [20]. Besides EOR damage, some n-type dopants (Sb in particular) can cause significant voiding if the implant dose is too high as shown in Fig. 1.7 [21] [13]. In an effort to avoid these pitfalls of Ge n^+/p junctions, other doping methods are actively being researched. Solid source diffusion [22],

gas-phase doping [23], and in-situ epitaxial doping [24] are among the candidates for future devices.

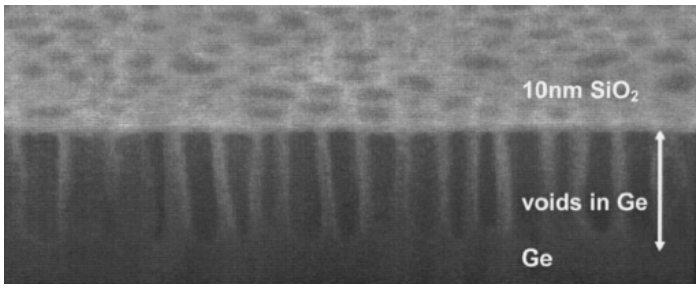

Figure 1.7: SEM image showing voids in Ge caused by high dose anneals of Sb ($1 \times 10^{15} cm^{-2}$ at 70 keV). From [13].

1.4 The Call for New Transistor Geometries

1.4.1 Short Channel Effects and Gate-All-Around Nanowires

As devices have continued to shrink, we have approached the point where the channel lengths are now of similar sizes to depletion layer widths of the source and drain junctions. As a result, 'short channel effects' (SCE), have become a large concern due to their effect on threshold voltage (V_t) and drift characteristics. In a sufficiently short channel, V_t is lowered due to this set of SCEs, which increases off-state leakage currents, reduce subthreshold swing (SS), and negatively impacts electrostatic control of the gate voltage.

One of the key SCEs is drain-induced barrier lowering (DIBL). In long channel devices, there exists an energy barrier between the source and drain inside the channel that retards current until a gate bias is applied to invert the channel. In a short-channel device, however, this barrier is lowered slightly near the source end because of the large lateral

field. Colinge $et.al.$ calculated the natural length scales for traditional single gate, dual gate, and gate-all-around structures for SOI samples, and the results are shown in table 1.3 [25]. The important conclusion from this work was that SCEs can be minimized for gate lengths much larger than this natural length. Comparing the three equations, the gate-all-around architecture allows for the best electrostatic gate control and thus the best means for controlling SCEs. Sufficiently narrow NWs naturally offer the best gate-control over the channel, because the NW can be made so thin that the entirety of the Si (or Ge) is electrostatically controlled.

Another key benefit for top-down NW devices is the vertical transport. Rather than take up valuable Si planar real estate, a top-down NW only needs the diameter of the NW plus a few thin ($\sim 10nm$) films radially around it. The S/D contacts can be made below and above the FET, minimizing areal impact.

Table 1.3: Natural length in SOI devices with various gate geometries for SOI MOSFETs. t_{Si} is the thickness of the SOI layer (or NW in case of 1.3). From [25].

Geometry	Natural length (nm)	
Single-Gate	$\sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} t_{ox}}$	(1.1)
Dual-gate	$\sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} t_{Si} t_{ox}}$	(1.2)
Circular Gate-all-around	$\sqrt{\frac{2\epsilon_{Si} t_{Si}^2 ln(1+\frac{2t_{ox}}{t_{Si}}) + \epsilon_{ox} t_{Si}^2}{16\epsilon_{ox}}}$	(1.3)

1.4.2 Tunnel-FETs

In addition to the NW, the Tunnel-FET (TFET) is one of the more exciting MOSFET replacements currently under investigation [26][27][28]. Rather than using carrier inversion in the channel, it uses band-to-band tunneling (BTBT) — similar to a zener diode in reverse breakdown. Figure 1.8 shows the cross section of TFET. The overall structure is similar to a MOSFET, with the major exception that the source and drain are oppositely doped. There is still a gate modulating the channel, and current still flows from source to drain.

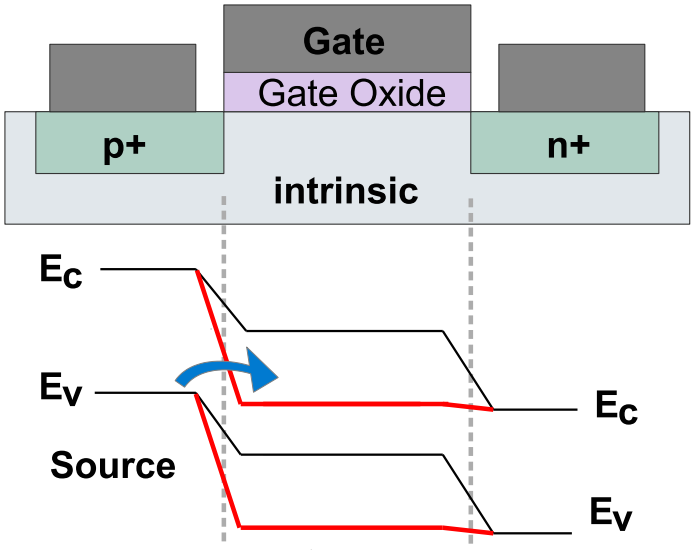

Figure 1.8: A cross section of a traditional n-type TFET. Below is the band diagram in the semiconductor immediately below the dielectric, for both no-bias (black) and positive bias (red) cases.

When a gate voltage is applied, the bandstructure is modulated in the channel uniformly (laterally) under the gate. On the source side (p^+), the gate has strong control of the channel immediately under the dielectric and to the right of the source doping, creaing a very strong lateral electric field. The red line in the band diagram (Fig. 1.8) shows the sharp slope of the band diagram and shows where tunneling can occur with a blue arrow

by electrons (which are plentiful in the p^+ source) that can quantum=mechanically tunnel into the now-free states of the channel. The lateral V_{DS} pulls the electrons out at the drain terminal.

The real advantage to the TFET lies in its ability to break the $60mV/dec$ thermionic limit inherent in MOSFETs. Equation 1.4 shows the subthreshold slope of a MOSFET, where kT/q is the thermionic energy divided by the charge of an electron, C_d is the depletion layer capacitance, and C_{ox} is the gate-oxide capacitance. As $C_{ox} \rightarrow \infty$, SS ~60 mV/dec at room temperature. Tunnel FETs do not have this thermionic limitation, and have been simulated to be able to achieve sub ~40 mV/dec [29][30]. A small SS enables transistor inversion with minimal applied bias, which is extremely beneficial for power reduction, but also has the advantange of faster switching speeds, as the time delay between consecutive logic states is (for MOSFETs), $\tau \sim CV/I$.

$$SS = \frac{1}{ln(10)\frac{kT}{q}(1 + \frac{C_d}{C_{ox}})} \tag{1.4}$$

For TFETs to really be competetive with MOSFETs, however, higher drive currents are necessary. While SS slopes are low and operating voltages are low, the drive current is substantially reduced. New designs have been put forth to boost current, including heterostructure devices and gate-normal tunneling, and one such approach is discussed in section 2.5.3, utilzing Si and Ge.

1.5 Chapter Organization

This chapter has introduced some of the key issues related to Ge MOSFETs, both some of its shortcomings and where it may surpass Si. Chapter 2 briefly introduces Si and Ge epitaxy in the UHV environment and continues to showcase the C doping of Ge to form Ge:C. A thin buffer layer of this Ge:C can be used as to grow thin or thick highly relaxed and high quality $Si_{1-x}Ge_x$ or Ge epitaxial films starting from a Si substrate. One of the more promising applications for relaxed 'virtual' substrates is for use in Si/Ge (strained) TFETs, and chapter 3 runs through some theoretical devices via self-consistent simulations. Chapter 4 sidesteps to introduce a new method for n-type doping of Ge that offers a simple method with high dopant activation and sharp (albeit deep) profiles. Chapter 5 introduces the design of Ge NW FETs via a top-down etching method, which can ustilize the doping method of chapter 4. 1-D band structure simulations are run to design the FETs, and a fabrication method is explained with initial results. A conclusion is given in chapter 6.

CHAPTER II

Heteroepitaxy of Group IV elements in UHV-CVD

2.1 The UHV-CVD System

2.1.1 UHV-CVD Hardware and Software

The UHV chamber used for our epitaxy experiments is a custom- built, cold-wall system that houses 4 inch wafers. Starting from the top of Fig. 2.1, the growth chamber is pumped

Some of the work in this chapter has also been published elsewhere. The Ge on Ge:C work was reported in "Ultra-smooth epitaxial Ge grown on Si(001) utilizing a thin C-doped Ge buffer layer" by J. Mantey, W. Hsu, J. James, E.U. Onyegam, S. Guchhait, and S.K. Banerjee in Applied Physics Letters 102, 192111 (2013). J. Mantey fabricated the films and performed characterization. W. Hsu, J. James, and E.U. Onyegam contributed to UHV equipment maintenance, S. Guchhait assisted with resistivity measurements, and S.K. Banerjee advised. The SiGe on Ge:C work was reported in "Thin, relaxed $Si_{1-x}Ge_x$ virtual substrates on Si grown using C-doped Ge buffers" by W. Hsu, J. Mantey, C.C. Hsieh, A. Roy, and S.K. Banerjee in Applied Physics Letters 105, 152107 (2014). W. Hsu fabricated and characeterized the films. J. Mantey assisted with fabrication and characterization. C.C. Hsieh and A. Roy helped characterize, and S.K. Banerjee advised.

to the mTorr range by a dry mechanical pump. After this is achieved, a turbo-molecular pump (TMP) can be activated to lower the chamber pressure to $\sim 1 \times 10^{-7}$ Torr. After performing a system water bake-out, in which the temperature of the entire system is brought over $100°C$ (usually $\sim 120°C$+) to evaporate water molecules clinging to the chamber's interior surfaces, we can achieve a base pressure of $\sim 1 \times 10^{-10}$ Torr. This pressure is measured by a set of hot-filament (aka hot-cathode) and cold-cathode pressure gauges. Below the main growth chamber is the load lock which is also baked-out and kept under vacuum. It can be vented with N_2 gas, and quickly pumped down via LN_2 sorption pumps. Samples are loaded in the N_2-purged glove box that the load lock opens to (on the right side of the figure).

Epitaxial growth in the chamber is performed primarily by three input variables: (1) gas flow rates (measured in standard cubic centimeters per minute, or sccm), (2) substrate temperature, and (3) growth pressure (measured in Torr). Each of these variables will be very briefly discussed.

Table 2.1: Available source gases in the UHV-CVD system.

Source Gas	Notes	Desired Adatoms	Max Flow Rate
Si_2H_6	liquid, 100 %	Si	20 sccm
GeH_4	40%, He balance	Ge	20 sccm
H_3GeCH_3	10%, He balance	C, Ge	10 sccm
PH_3	10-1000 ppm in He	P	10 sccm
B_2H_6	10-1000 ppm in He	B	10 sccm

The first mentioned variable for growth is that of precursor gas flow. Table 2.1 shows the available gases to our UHV system. Each of our input gases is controlled by a mass-flow controller (MFC) and several electronically controlled valves. The MFCs control gas flow with a percentage input of the rated flow rate — for instance, a 20 sccm

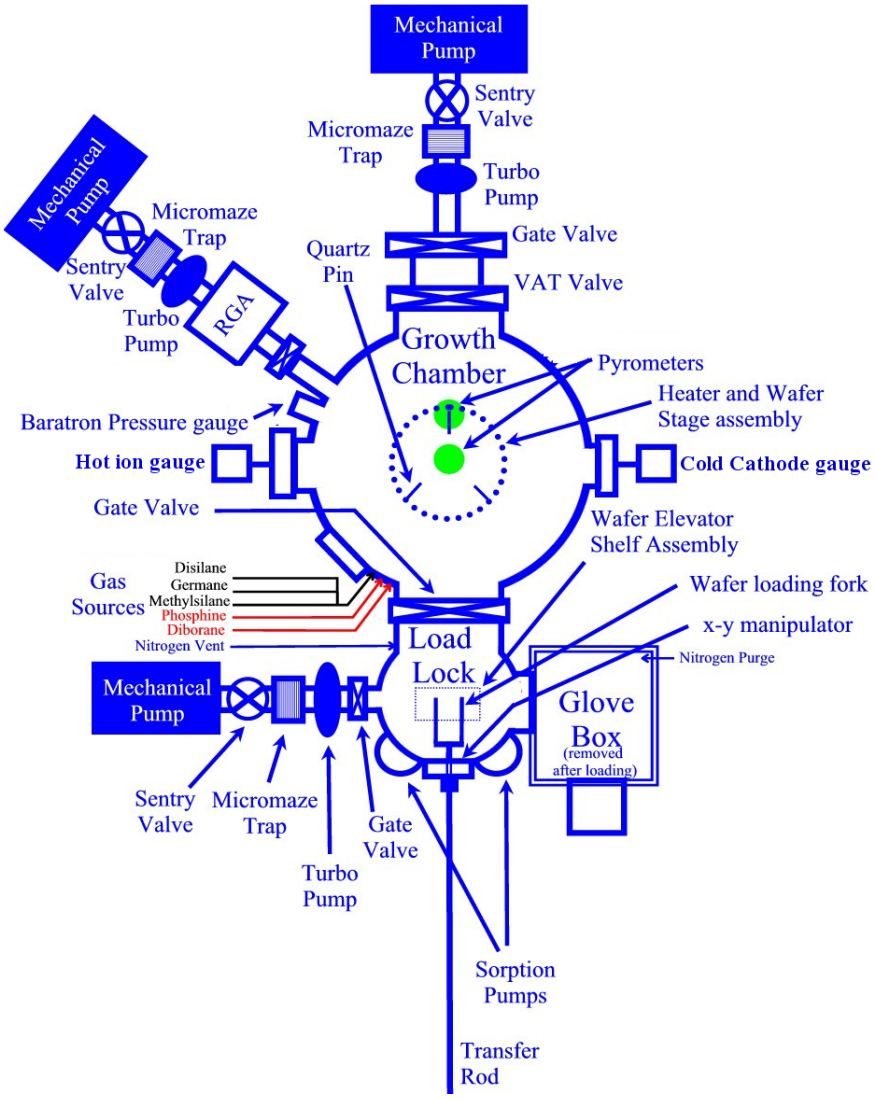

Figure 2.1: Schematic Diagram of the UHV-CVD system and its components. The three critical parts of the CVD chamber are the input gas sources (left, source of epitaxial atoms), the heater (center, source of heat), and the pump (top, source of system pressure).

controller set at 10% would flow 2 sccm of the designated gas. Multiple gases can be inputted to the chamber simultaneously. In the source-limited regime of epitaxy, lower flow rates yield slower growth rates. Generally, however, UHV-CVD growth conditions are set in the temperature limited regime, where flow has comparatively minor effects.

The next major variable in CVD epitaxy is growth temperature, where growth rates are exponentially dependent on growth temperature (in K) so long as there is sufficient gas flow to remain in the temperature limited regime. Past students working with the UHV-CVD tool used infrared lamps to control the wafer temperature, which was unstable with time due to ever-changing deposition on the lamps. A graphite cup heater was used as a replacement heat source to combat the growth inconsistencies and reduce system down-time for lamp replacement. The heater contains three-zones (one center zone and two outer zones on opposite sides) and enables us to control temperature uniformly over the wafer surface more effectively. A direct current is applied to each of the three zones of graphite conductor sandwiched between two boro-nitride insulating layers as depicted in Figs. 2.2, 2.3, and 2.4. Maximum temperatures at the wafer surface are approximately 700-750°C, with poor uniformity. Lower temperatures of ~600°C are significantly more uniform. Based on expected growth rates taken from Arrhenius plots, the temperature variation can be controlled to a few °C. Thick Ge films grown with the 2-step process (350°C + 600°C) can yield thickness uniformities of $< 5\%$. Since growth rate is exponentially dependent on temperature, the temperature variations across the wafer are expected to be very small.

The third primary variable is chamber pressure. For most processes (though not with Ge:C — see section 2.3), an increase of pressure will yield an increase of growth rate. Naturally with higher growth rates, there can be additional defects, so careful attention must

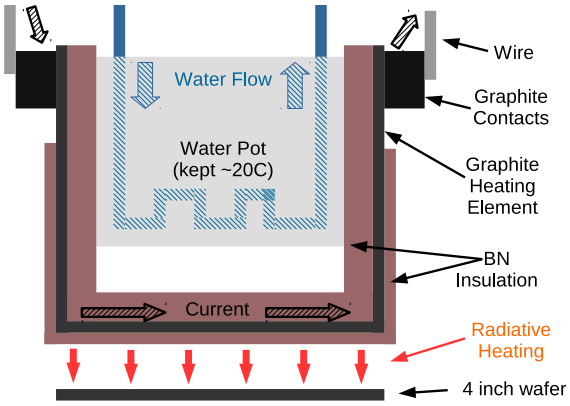

Figure 2.2: The heat source for the UHV-CVD system. It's a cup-shaped heater with graphitic heating elements sandwiched between two layers of boro-nitride insulation. A water pot is used to prevent deposition on and around the contacts which would cause short path outside the heater.

be made. Our chamber controls pressure using a electronically controlled variable VAT valve in conjunction with a Baraton capacitance manometer pressure gauge. A pressure is set via computer between ~1 mTorr and 100 mTorr and the variable valve opens and closes based on the feedback given from the Baratron gauge. Naturally, this method only controls the total pressure. To control partial pressures, one must change the ratios of the input gases.

On the software side, a LabView program is utilized to control the aforementioned hardware. Both automated (recipe-based) and manual controls are available to the user. Due to the change in heater hardware, new modules were developed to control the DC power supplies. Recipes have been written to use a slow ramp-up in temperature (~10°C per minute until 150-200°C for the cup heater to eliminate thermal shock to the heater. Upon recipe completion, a ramp down is often used, but not required, as the natural decay of temperature is slowly changing already. The slow ramp-up does not affect the H-passivation on the surface, as H doesn't desorb until ~450-500°C [31]. Pressure, gas flow rates, and

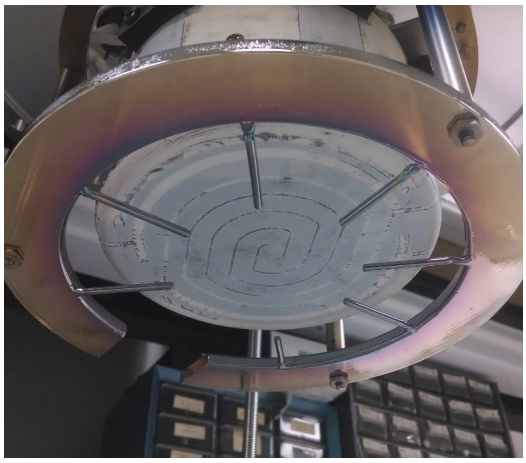

Figure 2.3: The underside of the installed cup heater. The graphite heating element is winding around, providing uniform heat over the 4 inch wafer size. The (coated) quartz pins of the holder assembly are visible in front of (beneath) and circling the heater.

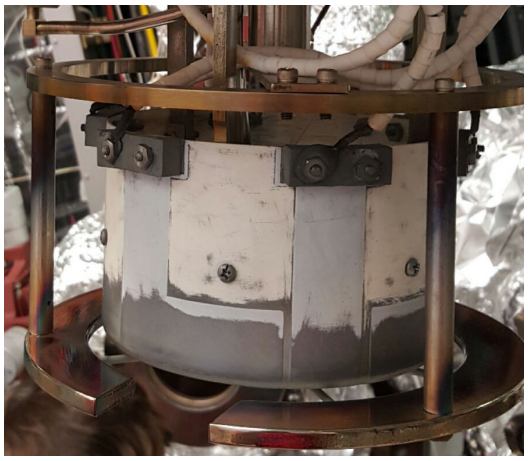

Figure 2.4: Side view of the installed cup heater. Apparent is the graphite contact pads, and sandwiched graphite that goes to the bottom of the cup. The bottom third of the cup has significant Si/Ge deposition, the top two thirds has been sanded off after a water pot failure caused despostion everywhere.

temperature (indirectly controlled through DC current output) are all controlled via this LabView code. Temperature feedback is obtained via reading type-C thermocouples and pyrometers and is recorded in data logs during the recipes.

2.1.2 Substrate Preparation and Loading

Prior to epitaxy in the UHV-CVD system, one must properly clean and prepare the wafers before loading into the chamber. Four inch Si wafers are placed in a piranha solution (2:1 or 3:1 H_2SO_4 (97%) : H_2O_2 (30%)) for ~7-8 minutes to clean organics off the surface. Because this is a strong oxidizing solution, the resulting wafers have a thin oxide layer remaining and are hydrophillic (due to the many -OH bonds on the surface). After an

organic clean, the typical industrial procedure is to follow with an ionic clean (e.g. RCA SC-2) to reduce metal contamination. We often skip this step since our epitaxy will cover this surface effectively. After the piranha clean, the wafers are rinsed in water and dipped into a dilute HF acid solution (40:1 H_2O:HF (49%)) to remove the native oxide. This ratio delivers an SiO_2 etch rate of $\sim 1/s$. The wafers remain in the solution until de-wetting occurs (typically $60-90s$), indicating a clean, hydrogen terminated surface. The wafers are briefly spin-dried (2000 RPM, 120s, N_2 ambient) and quickly carried into the N_2 purge-box attached to the outside of the UHV-CVD chamber load lock.

After using a glove to insert the wafers into the load lock, the pressure is quickly reduced via a liquid N_2-cooled sorption pump, taking the load lock from atmospheric pressure (ATM) to sub-100 mTorr pressures. Next, the sorption pump is closed off and a dedicated turbo-molecular pump (TMP) is opened, pulling the pressures in the load lock to the 10^{-7} Torr range over the course of 20-60 minutes. Now the wafers can be loaded into the growth chamber, sequentially, for epitaxial growth.

It is important to note why the rapid HF-dip-to-load process is critical in our system. In many Si-growth chambers, H_2 cleans are performed in-situ to remove the native oxide and yield H-terminated surfaces. This is not possible in our chamber for two reasons. First, as mentioned earlier, the maximum temperature of the wafer in the UHV system is ~700-800°C due to power supply limitations. Hydrogen annealing is typically performed at high temperatures, typically 800°C or higher [32]. Secondly, the chamber currently does not possess a H_2 gas source, so modifications would need to be made. For most growths, as a result, we simply do Si homoepitaxy first to bury any surface contamination that may exist.

2.2 Silicon and Germanium Epitaxy via Disilane and Germane

2.2.1 Silicon Epitaxy via Disilane

There are several Si precursors that can be used for Si epitaxy, the most common of which are $SiCl_4$, $SiHCl_3$, SiH_2Cl_2 (DCS), SiH_4, and Si_2H_6. The chlorine-based precursors (the most common of which is DCS, which has been studied since the 1980s [33] enable selective epitaxy, as the byproduct Cl_2 gas etches Si preferentially (over SiO_2). As long as external Cl_2 is not introduced to the system (i.e. just the byproducts of the precursor are present), the Si growth rate will be faster than the Cl-based Si etching, and a positive net growth rate will be achieved. Any Si that does deposit on the SiO_2 is etched quickly before further epitaxy proceeds.

In systems that do not require selective epitaxy, silane gas (SiH_4) is often preferred as the growth rates are substantially higher than that of the Cl-based precursors in the temperature-limited regime (a.k.a. surface-kinetics limited or reaction-limited), which is generally the regime used for UHVCVD processing. Figure 2.5 compares the Arrhenius plots of the two gases and shows the relative increase in growth kinetics. In an Arrhenius plot, the right side of the figure (towards increasing 1/T or decreasing T) has a slope (on a log-linear scale) that shows the activation energy (E_a) for the chemical reaction. While E_a is higher for DCS, the growth rate is significantly higher at the temperatures of interest (~550°C to 1000°C).

Disilane gas (Si_2H_6) has an even higher growth rate at low temperatures, and was

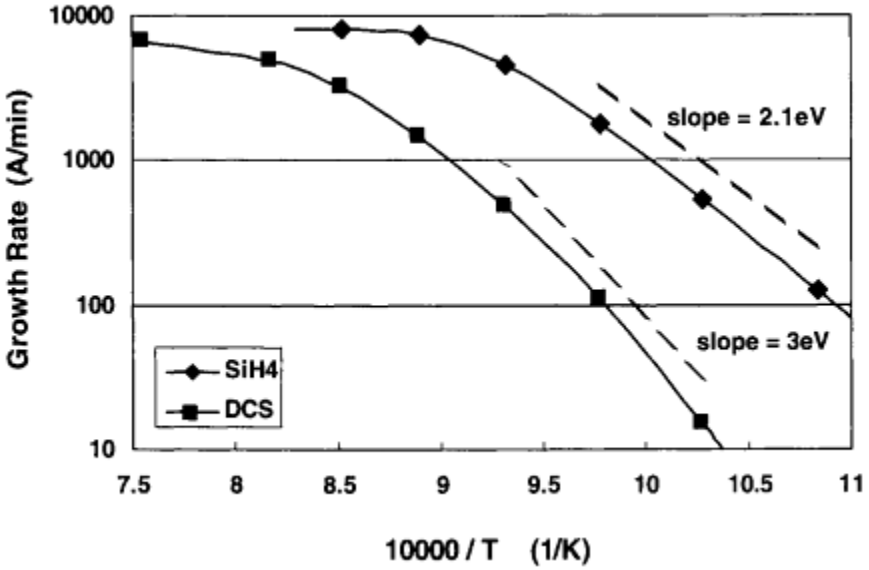

Figure 2.5: Comparison of the Arrhenius plots of silane and DCS gases for similar growth conditions. For the temperature (reaction) limited regime, an increase of growth rate of more than one order of magnitude can be seen. From [34].

thus chosen as the Si precursor for our UHVCVD system. In a UHV system, conditions are generally set to minimize contamination at all costs in order to achieve the best epitaxy with the lowest number of defects. Higher temperatures, while enabling faster growth rates, increase thermal budgets and introduce unwanted contaminants from unlikely sources — such as those evaporated or sublimated from chamber walls or internal components. Through efforts such as water-cooling of the chamber and proper precursor selection, thin film quality (or at least purity) will improve.

For all of these Si precursors, reaction-limited growth is the key mechanism in the UHV environment. Here, the epitaxial growth is facilitated through available dangling bonds (DBs) on the crystal surface [35]. For a clean H-terminated Si surface, DBs are formed by the thermal desorption of H_2 (or optical, plasma-enhanced, etc. desorption).

The density of DBs depends exponentially on T, shown by E_a, and thus the growth rate varies rapidly — so the choice to use Si_2H_6 is corroborated. A comparison between the growth rates of Si_2H_6 and SiH_4 is shown in Fig. 2.6, where the reaction-limited regime shows a clear increase in GR for Si_2H_6.

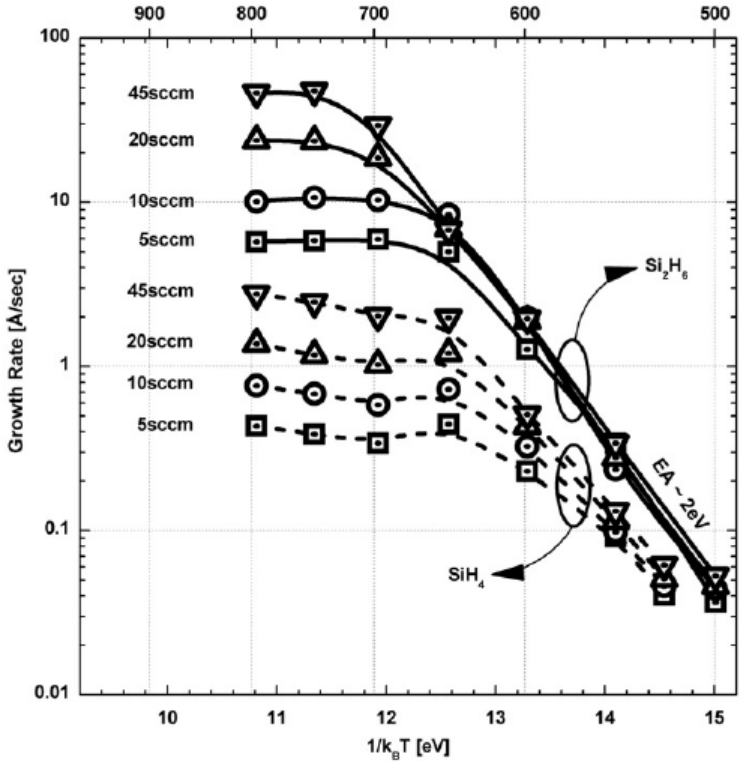

Figure 2.6: Comparison of the Arrhenius plots of silane and disilane gases for different gas flow rates. For the temperature limited regime, an increase of growth rate is observed for Si_2H_6. From [36].

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The net reactions for both SiH_4 and Si_2H_6 are quite simple if we ignore the (important) intermediary reactions: the Si atoms become adatoms, and the H atoms become H-passivation or H_2 gas. For information about the intermediary reactions, one is referred to Refs. [34], [37], and [38]). In the case of Si_2H_6 grown on Si(100) surfaces, the Si_2H_6 first

dissociatively chemisorbs onto DB sites, with two SiH_3 fragments on nearby sites that can proceed to decompose into SiH_2 + H [39] [40] [38]. Initially, this yields a (2×1) dihydride surface, which will eventually (through a slower process than the initial Si_2H_6 adsorption) form bonds between adajacent Si atoms, emitting H_2 and forming a (2×1) monohydride surface, where epitaxial growth continues [41].

Typical growth conditions used in the UHVCVD system are shown in table 2.2. First, the temperature in the chamber is slowly (~10°C/sec) ramped to ~200°C to reduce initial thermal shock to the cup-heater. The corresponding cup-heater current levels for 200°C are ~1.0 and 1.4 A for the center and edge zones, respectively. The currents is then set to ~4.2 and 5.7 A to achieve T ~600C at the wafer surface. Disilane gas is then flown at 10-20 standard cubic cm per min (sccm) into the chamber. For these conditions (see Tab. 2.2), typical growth rates are on the order of ~1 Å/s for Si homoepitaxy. This value matches closely with the Arrhenius plot (Fig. 2.6) shown in literature. Gas flow rates can be adjusted, but have minimal effect (as we are in a reaction-limited regime). While it is more wasteful, higher flow rates are often chosen to help minimize any contamination from the gas lines — either internally or externally. Since our Si growths are typically short in duration (~5-10 min.), this is an acceptable compromise.

Table 2.2: Typical Si epitaxial growth conditions in the UHVCVD.

Parameter	Typical Values	Notes
Pressure	~1 mTorr	TMP open; No pressure control
Gas Flow Rate	50%	20 sccm MFC, source = 100% Si_2H_6
Temperature	~600°C	
Growth Rate	~1 Å/sec	

Unless otherwise stated, the thickness of all films grown in the UHV-CVD is mea-

sured by a J.A. Woollam M-2000 DI Ellipsometer. Software models exist for most of the materials grown in the UHV-CVD (Si, $Si_{x-1}Ge_x$, and Ge), which describe how polarized lights of varying wavelengths behave in the material. The Ge:C material to be discussed in Sec. 2.3 is optically comparable to Ge, so the Ge model can be used [42]. Cross-sectional transmission electron microscopy (XTEM) was used to validate the Ge:C thickness values outputted by the ellipsometer software. For the heteroepitaxial samples, the film thickness is easily measured using a model with an Si substrate. For Si homoepitaxial samples, a thin $Si_{x-1}Ge_x$ layer is grown, followed by a Si layer to calibrate the growth rate (GR) of Si at the given conditions (atop of the low Ge concentration $Si_{x-1}Ge_x$). While the thickness of the Si homoepitaxial samples are not directly measured, the approximation from this calibration run is adequate for our purposes.

While there are potential projects for Si homoepitaxy in the UHV-CVD system, the primary use of Si in our system has ben for creating a chemically pure Si surface for alternative materials like SiGe, Ge, and Ge:C. Depending on the desired use (material vs. electrical characterization), a typical Si starting film will range in thickness from ~10-100 nm, at conditions similar to those shown in table 2.2. Figure 2.7 shows an example of a Si/Ge superstructure that was grown in the UHV-CVD system. An example recipe is available in the appendix.

2.2.2 Germanium Epitaxy via Germane

There is a drive in the microelectronics industry to move to new materials for superior electrical transport. Germanium is one material that offers many benefits — one of which being that one can heteroepitaxially grow it on a Si substrate as introduced in section 1.2.

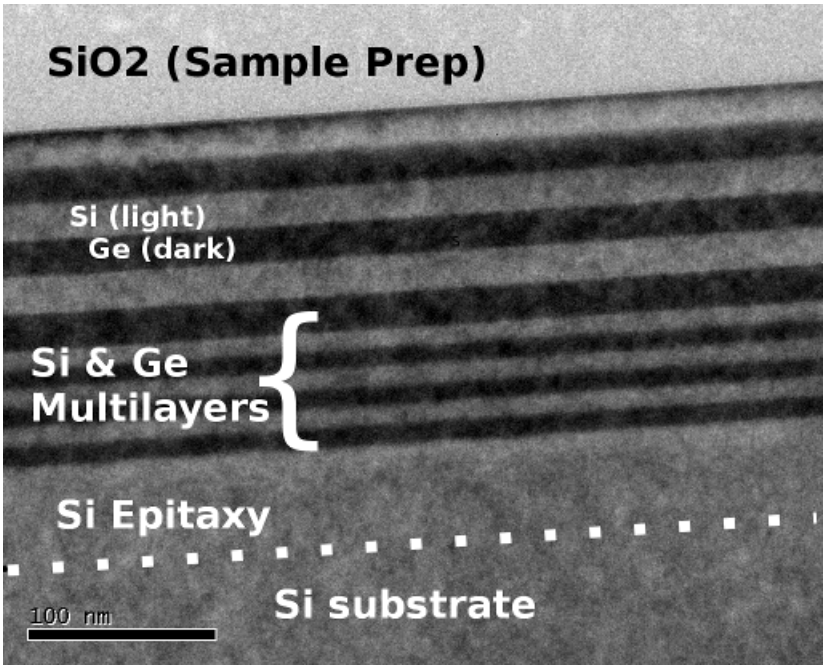

Figure 2.7: Si/Ge superlattice grown in the UHV-CVD system is a clear visual indication of Si epitaxy. The initial epitaxy is difficult to distinguish from the underlying substrate (approximately at the dotted line).

After growing the initial ~50 nm Si buffer as already described, the chamber temperature is lowered to the desired Ge growth temperature of ~330-350°C. After stabilization, germane gas (40%, He balance) is flown into the chamber, and a variable valve is set to control pressure (~5-30 mTorr typically) for the duration of the (low-T) growth.

The process above yields low growth rates of ~1 nm/min. Because of the exponential dependence on temperature, temperatures lower than 330°C are uneconomical. Higher temperatures promote S-K growth, which drastically increases surface roughness (R_{RMS}) and thus is detrimental to planar device performance. While thin films are useful, it is sometimes necessary to grow thicker ($\pm 1 \mu m$) films. In the UHV-CVD, our best choice is the 2-step method (based on Ref. [8]). Here, after ~30-50 nm of initial LT Ge growth, the

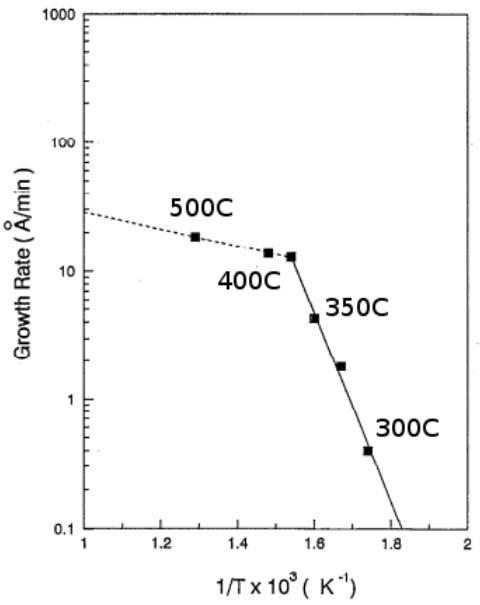

Figure 2.8: Arrhenius curve for Ge homoepitaxial growth in UHV conditions. From [43].

temperature is raised to ~600°C and additional HT epitaxy is performed at a much higher growth rate. Temperatures lower than ~570°C for the second step result in rough, cloudy growths in the UHV system. Figure 2.9 shows the 2-D AFM image (RMS roughness = 0.33 nm) of a 460 nm thick Ge film grown in the UHV-CVD tool via the 2 step method. For planar surface devices, this approach can be adequate, as the surface is smooth with few defects. Compare this to Fig. 2.10 where a thick Ge film grown at high-T was grown without a low-T buffer resulting in R_{RMS} of > 20 nm.

Figure 2.8 shows the Arrhenius relationship for Ge growth via GeH_4 in UHV conditions. It is important to note that these curves represent Ge homoepitaxy rather than heteroepitaxy, since with Ge heteroepitaxy there is often an incubation time where the initial few monolayers (MLs) take additional time to form due to the immediate change of lattice size and interface [44]. In our chamber, this incubation time can be as long as 15

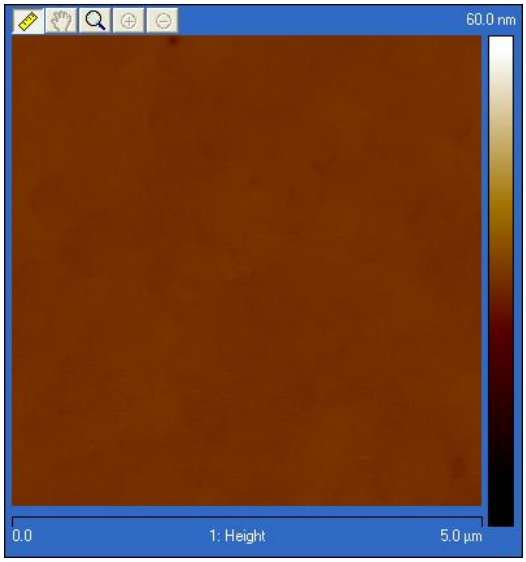

Figure 2.9: A 460nm thick Ge film grown in the UHV-CVD system via the 2-step process. Final RMS surface roughness is 0.33 nm in a 10×10 μm^2 area.

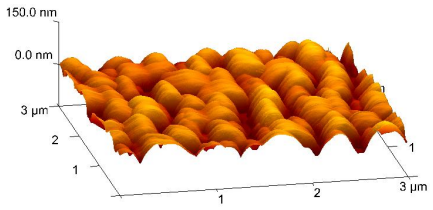

Figure 2.10: A ~~300 nm growth of Ge at higher T without initial low-T step promotes S-K growth and a high R_{RMS} of ~20 nm.

minutes for low-T, low-P conditions. Higher T and P will reduce this time (but will also degrade epitaxial quality, so compromises must be made).

The growth procedure for Ge heteroepitaxial growth begins the same as a recipe for Si homoepitaxy above. A thin (~10-100 nm) of Si is grown. While still under vacuum, T is set to 330-350°C, and GeH_4 is introduced into the chamber. To ensure the system is not source limited, high gas flow rates and a relatively high pressure are usually used. See table 2.3 for typical growth conditions. The resulting growth rate for LT conditions will be $\leq$ ~1 nm/min to prevent island formation. For subsequent HT steps, GR increases by over an order of magnitude to 10-20 nm/min.

Table 2.3: Typical Ge epitaxial growth conditions in the UHV-CVD. Note that first we grow a thin Si buffer layer as shown in Tab. 2.2 prior to this Ge growth.

Parameter	Typical Values	Notes
Pressure	10-15 mTorr	
Gas Flow Rate	50-100%	GeH_4, 20 sccm MFC, source gas is 40% balanced in He
Temperature	330-350°C	used for thin layers and LT buffer of 2-step growth mode
	600°C	used for HT step of 2-step growth mode
Growth Rate	1 nm/min	for LT mode
	15-20 nm/min	for HT mode

2.3 Germanium:Carbon

2.3.1 Germanium:Carbon Epitaxial Growth

Much research has been poured into minimizing the defect density for Ge thin films grown on Si. Section 1.3 mentions several methods used by various research groups in attempts to improve the Ge crystalline quality, especially near the surface where FET devices are utilized. One of these methods is to incorporate relatively high amounts of C (~few atomic %) in the film, which was first demonstrated by molecular beam epitaxy (MBE) [45] and later done via CVD at Arizona State University [46]. This Ge-C approach mitigated the use of extremely thick layers (often several μm) or complex processing to give a simple method to producing a thin layer of Ge. The ASU team used a novel precursor for CVD Ge epitaxy — a mixure of germane (GeH_4) and methylgermane (H_3GeCH_3). If concentrations of C got too high (using higher H_3GeCH_3:GeH_4 ratios), defective epitaxy occured — primarily giving {111} stacking faults and microtwins. However, using low concentrations of C (~2 at.%), the resulting Ge layers were highly crystalline. Electron energy loss

spectroscopy (EELS) data shows that the C was largely substitutional in nature and yielded sp^3 hybridized bonding with the lattice. To perfectly lattice match a Si crystal, Vegard's law (Eqn. 2.1) shows that a ~10% concentration is necessary in a Ge_xC_{1-x} to match the underlying Si substrate lattice parameter, which thus far has been unachievable in CVD processes. It is already remarkable that one can achieve a few at. % C in Ge, considering that the solid solubility (SS) is $< 10^{10}$ cm^{-3} at room temperature [47]. Table 2.4 shows typical growth conditions for Ge:C on a Si substrate. Germanium:Carbon requires higher processing temperatures compared to Ge, and has a slower growth rate. The details behind this will be discussed in detail in Sec. 2.4.

$$a_{Ge_{1-x}C_x} = (1-x)a_{Ge} + xa_C \tag{2.1}$$

The Banerjee group at the University of Texas was the first group to use CVD Ge:C as a means to create electronic grade Ge films [6]. David Kelly et. al. fabricated long-channel ring-FET devices on UHV-CVD grown Ge:C (Fig. 2.11), and compared results to Si control samples. It was determined that the Ge:C pMOSFETs outperformed their Si counterparts in drive current and hole mobility and that the C had minimal impact on device performance relative to other Ge heteroepitaxy literature. Importantly, The surface roughness (R_q) of the Ge:C film is substantially lower than that of pure Ge, where islanding due to strain relaxation is usually encountered from S-K growth. This reduces scattering for FET devices, and subsequently increases mobility. Based on etch pit density tests of the new films, they estimated a defect density on the order of 3×10^5 cm^{-3} for the Ge:C films, compared to 2×10^8 for the Ge control sample [6], further corroborating the epitaxial quality of the Ge:C layers.

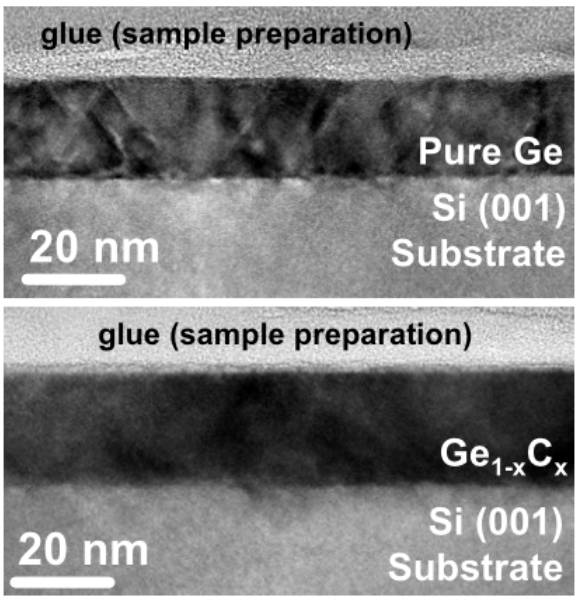

Figure 2.11: Comparison of growths of Ge and Ge:C heteroepitaxial films. Notice the defects in the Ge sample. From [6].

One important and interesting aspect of Ge:C growth is the relationship between GR and growth pressure. Chemical vapor deposition is typically a thermally activated process. The precursors need thermal energy to crack or force surface reactions on the crystal surface. Particularly for rate-limited growth, an increase in precursor partial pressure in the chamber will cause an increase in GR, as there is additional available source material able to chemically react with the surface. For Ge:C growth, a mixture of GeH_4 and H_3GeCH_3 is used. Obviously, changing the ratio of these two gasses will affect GR in different directions. Higher ratios of GeH_4:H_3GeCH_3 will increase the GR, and reducing the ratio will decrease the GR. The higher T used for Ge: growth (relative to Ge growth) positively allows the GeH_4 to decompose on the surface, which explains the increase of GR. What is interesting about Ge:C growth is that at a given T and gas flow ratio, increasing total P will reduce the growth rate rather than increase (or stay the same, in the case of reaction-

Table 2.4: Typical Ge:C epitaxial growth conditions in the UHV-CVD. Note that first we grow a thin Si buffer layer as shown in Tab. 2.2 prior to this Ge:C growth.

Parameter	Typical Values	Notes
Pressure	5-10 mTorr	GR inversely proportional to P, see Sec. 2.4
Gas Flow Rates	100%	GeH_4, 20 sccm MFC, source gas is 40%, balanced in He
	7%	H_3GeCH_3, 10 sccm MFC, source gas is 10%, balanced in He
Temperature	430-450°C	
Growth Rate	~0.4 nm/min	GR reported by Kelly in [6]. This turned out to be incorrect as will be shown in Sec. 2.4.

limited growth). Figure 2.12 shows the effect of an increase in total pressure on the GR for a Ge:C film. It is worth noting that the slower GR at higher P does have a positive effect on surface roughness (R_q reduced), but the drastic decrease in GR is cumbersome for reasonable film thicknesses ($\geq 20nm$). If low R_q is required, a lower growth temperature with lower pressure is suggested. Kelly et. al. did report on the temperature-vs-R_q relationship, which shows that lower T growth yields smaller surface roughnesses (but also slower growth rates) — this is expected from Ge heteroepitaxy and can be seen in Fig. 2.13. For additional relationships between gas flow ratios, temperatures, and pressures, one is referred to D. Kelly's thesis [42].

While the Ge:C films did compare favorably to Si in Kelly's work, there are also some negative aspects to this method. Firstly, in order to achieve the desired (low) surface roughness that Ge:C can provide, the temperature is kept low and the GR is thus very low compared to Ge epitaxy. Thus, both cost and time will be major factors on the feasibility of Ge:C. Furthermore, small amounts of substitutional (or interstitial) C introduces neutral impurity scattering, so we expect lower mobility for Ge:C compared to Ge. For these

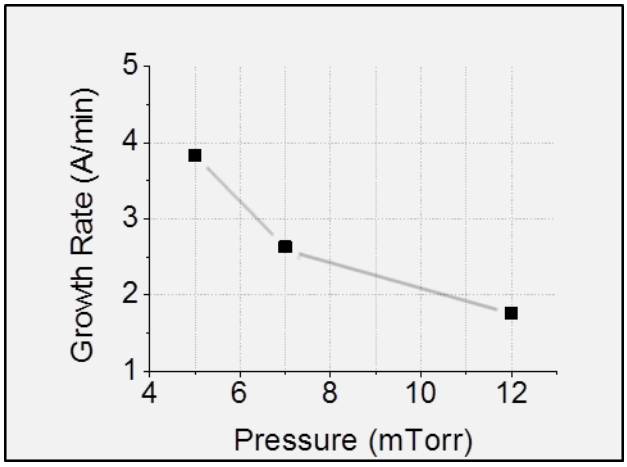

Figure 2.12: The effect of total pressure on GR for a 30 minute Ge:C growth. The wafer temperature and GeH_4:H_3GeCH_3 (=20:0.7 sccm) ratio are kept constant. The effective GR after a 30 minute growth is significantly reduced at higher P, which is counter-intuitive in a CVD process.

reasons, it is preferable to have a pure Ge crystal if possible. Section 2.4 discusses using Ge:C as a buffer layer to grow Ge on Si. In addition to these issues, it turns out that the already slow GR of Ge:C is not constant, exacerbating the issue. The following section discusses the non-linearity of Ge:C growth.

2.3.2 Further Analysis of Ge:C Growth Evolution and Inconsistencies

Germanium with C incorporation was shown to be a good method for forming smooth Ge surfaces on Si substrates. It was discovered, however, that growing thick layers of Ge:C is not possible at these standard conditions. Despite maintaining constant UHV-CVD chamber conditions — temperature, pressure, and gas flows — the growth rate of Ge:C is not constant with time, but instead decreases drastically after a short period of time. Figure 2.14 shows the effective growth rate of a Ge:C film over the course of a two hour growth (rates taken as slope of piecewise linear function of total growth thickness vs time). Ini-

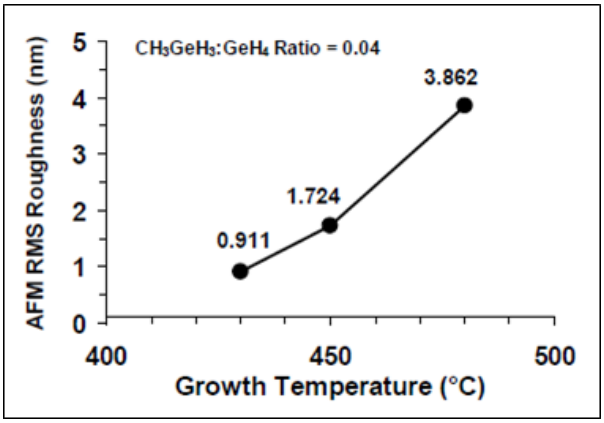

Figure 2.13: The effect of surface roughness with changing T for Ge:C films as shown in [42]. Note that lower GR and lower R_q are generally correlated. For additonal relationships between gas flow, T, and P for Ge:C films, one is referred to [42]

tially, The film proceeds to grow between 3 and 4 Å/min. After ~30 minutes of growth, however, this value begins to drop. At the two hour mark, there is effectively no additional growth, despite the constant settings of the system. The process varies slightly with temperature, where lower T (~430°C) sees a maximum thickness of ~20 nm and higher T (~450°C) sees a maximum thickness of closer to 30nm. The following section investigates the cause of this changing GR.

Because of the decreasing GR with time, it is impossible to have thick ($> 30 - 50nm$ or so) high quality Ge films utilizing the low R_q results of the Ge:C layer. As such, we became interested in potential Ge grown on a thin Ge:C buffer layer. Here, one would expect that the Ge:C buffer layer will allow for strain relaxation at the interface due to the addition of C atoms. When GR slows down, a change can be made to use Ge 'homoepitaxy' on the Ge:C buffer, where GR is much higher and less resource intense. At the same temperature, following the Arrhenius relationship of Fig. 2.8, we expect a GR nearly an order of magnitude higher by using simply GeH_4 (~0.3Å/s for Ge:C vs ~20Å/min

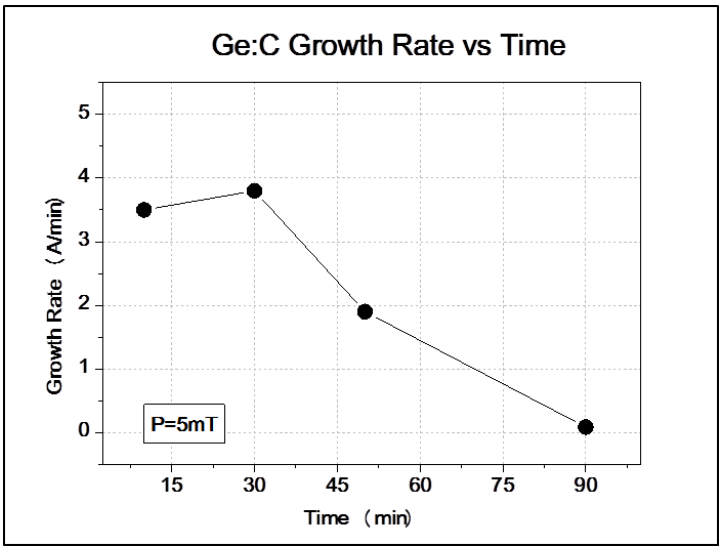

Figure 2.14: The non-linear GR of Ge:C grown heteroepitaxially on Si. For this sample, T = 430°C, P = 5 mTorr, gas flow = 20 sccm : 0.7 sccm GeH_4 : H_3GeCH_3. After ~2 hours of growth, growth stops

for Ge).

2.4 Germanium on Germanium:Carbon Buffer Layers

2.4.1 Growth Rates of Germanium Grown on Thin, Ge:C Buffer

The first attempts to grow Ge on Ge:C buffer were performed at similar conditions to what is typically used for Ge heteroepitaxy in our UHV-CVD system. First, a thin Si layer (Sec. 2.2) is grown to ensure a clean surface. Next, T is lowered to 430°C, and a thin ($\leq$ 10 nm) Ge:C layer (Sec. 2.3) is grown to confine defects at the interface and relax the new film, promoting a subsequent high quality Ge growth. Temperature is again lowered to ~330°C, where Ge growth is attempted (Sec. 2.2). Interestingly, at this stage, no further Ge growth is observed, and only after increasing the T by almost 100°C to 435°C— a significant

change in processing temperature — is additional growth even seen. For instance, a 30 minute growth of Ge at 330°C is expected to yield ~25 nm, yet no change in film thickness occurs. At T ~435°C, growth begins, but — as in the case of Ge:C — is not constant in time. Figure 2.15 shows the increasing growth rate vs. time (left hand axis), while T and P remains constant in the chamber. In order to identify the cause of the growth rate deviations, several experiments were performed, as explained in the next sections.

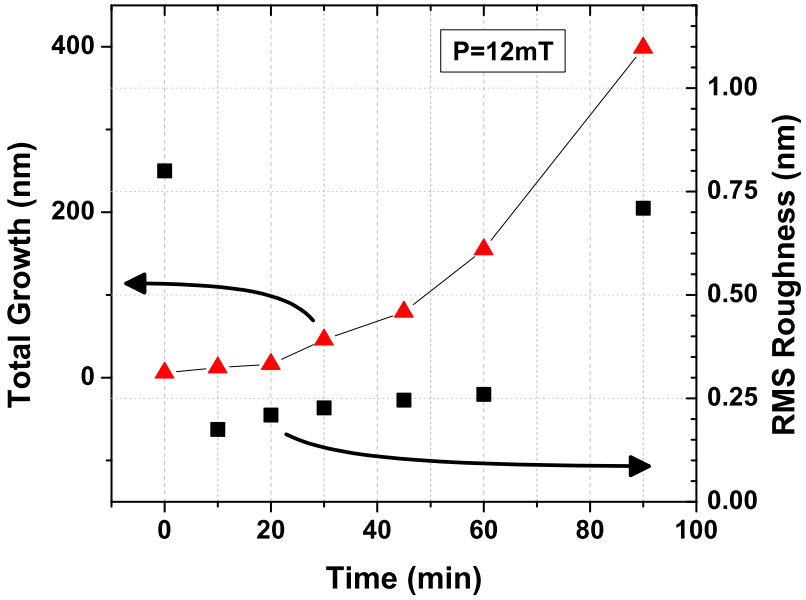

Figure 2.15: Total growth and R_q for a Ge film grown on a thin Ge:C buffer. $P = 12$mTorr and $T = 435$°C.

2.4.2 Atomic Force Microscopy Analysis of Surface Roughness

It is useful to analyze the evolving surface roughness of the Ge:C to determine whether changes in R_q affect the GR of the Ge layer. For surface roughness measurements, a Digital

Instruments Nanoscope V Veeco is used in tapping mode to generate surface topography on a $3 \times 3\mu m^2$ or $10 \times 10\mu m^2$ areas. Figure 2.16 shows the surfaces of the Ge film as it grows from the Ge:C buffer (a) to become a 400 nm film (e). The GR is clearly non-linear (refer to Fig. 2.15) over time, with an exponential-type dependence.

The first surface roughness data point is especially interesting. Despite Kelly et. al. (and our own data) showing that Ge:C growth is low-RMS, our very thin Ge:C layer (~5-7 nm) is actually islanded, with a comparably rough $R_q = 0.80$nm RMS film. Figures 2.17 and 2.18 show the islanding in higher resolution scans, where islands of ~50 nm in diameter and 1-2 nm in height are visible. The shape of the islanding is rectangular in nature, which is frequently reported in literature for Ge heteroepitaxy as a stress-relaxation mechanism during the initial states of growth.

Despite this initial 'rough' film, after 10 minutes of Ge growth at 435°C, R_q decreases from 0.80 nm RMS to 0.18 nm RMS — a value comparable to the starting Si surface (before any epitaxy), and far lower than anything reported by Kelly or ASU. From 10 min to 60 minutes, the R_q doesn't change significantly (0.18 to 0.26 nm RMS), but the GR (and total growth) change substantially (~10 nm to 140 nm). Surface roughness can be ruled out as not having a significant impact on GR in the Ge film.

2.4.3 Strain Extraction from X-ray Diffraction Reciprocal Space Maps

Another possiblity for the unexpected rise of GR is changing strain in the film. Perhaps initially, due to the lattice mismatch, there would be significant strain. As the film relaxes during additional epitaxy and the lattice parameter approaches a_{Ge}, the GR could increase.

To analyze strain in a semiconductor thin-film, we use a Philips PANanalytical

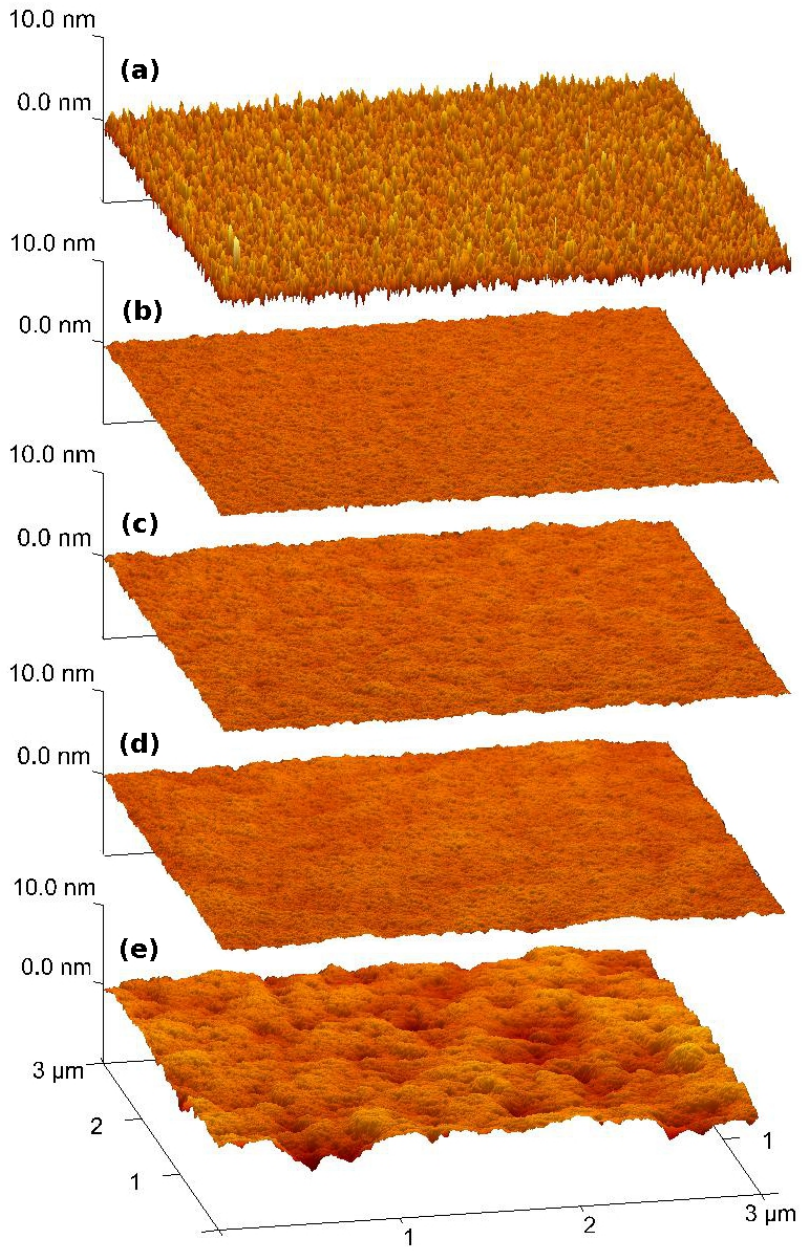

Figure 2.16: The evolution of surface roughness for Ge grown on a thin Ge:C buffer layer of 7 nm. $P = 12$ mTorr, and $T = 435$°C. (a) R_q of Ge:C buffer, (b)-(e) are after 10, 30, 60, and 90 min of Ge epitaxy after the Ge:C buffer. These and additional data points can be seen in Fig. 2.15

.

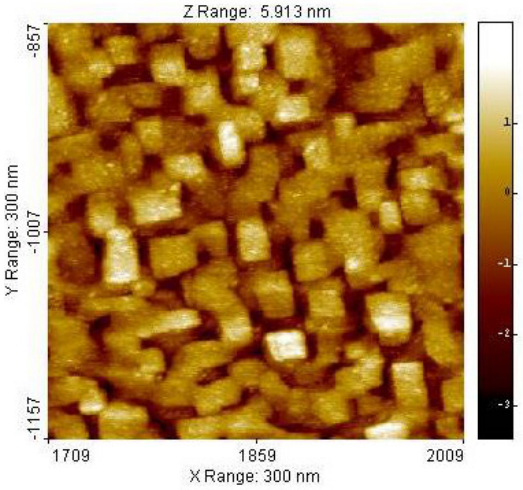

Figure 2.17: A $3 \times 3\mu m$ STM area scan of a thin 5-7 nm Ge:C buffer layer. Islanding is visible.

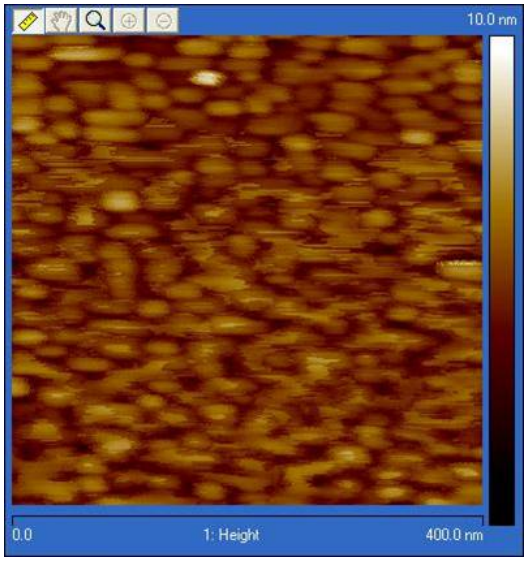

Figure 2.18: A $4 \times 4\mu m$ AFM area scan of a thin 5-7 nm Ge:C buffer layer. Islanding is visible, and qualitatively similar to the STM image.

X'PERT Pro MRD diffractometer. All $\omega - 2\theta$ scans in the XRD system were measured using a 1 mm slit. For reciprocal space maps (RSMs), a three-bounce Ge analyzer crystal was placed in front of the detector. Both, symmetric (004) and asymmetric (224) scans were performed on the epitaxial sample to extract the in-plane ($a_{\|}$) and out-of-plane ($a_{\perp}$) lattice parameters (also known as a_p and a_n, respectively).

Figures 2.19 and 2.20 shows an example of the reciprocal space maps from the (004) and (224) symmetric and asymmetric scans. The output given by the X'PERT software is the intensity measured for the real-space values of various ω and 2θ angles. These values can be converted to reciprocal lattice units (Å^{-1}) by the relationships given in Eq. 2.2, as shown by [48].

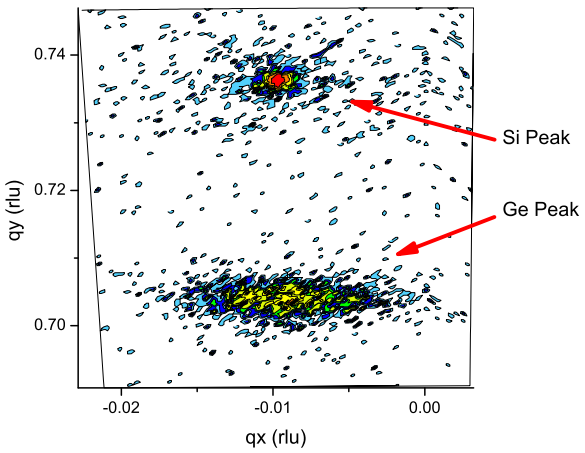

Figure 2.19: The 004 symmetrical scan of a 41 nm Ge-on-Ge:C sample. The Peaks for both Si and Ge are visible.

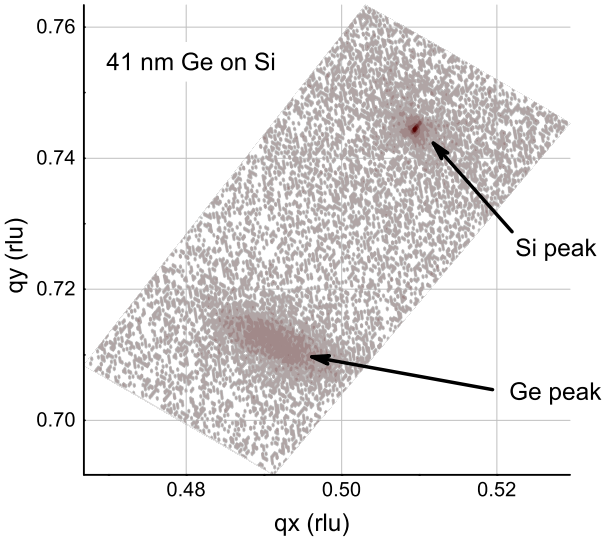

Figure 2.20: The 224 symmetrical scan of a 41 nm Ge-on-Ge:C sample. The Peaks for both Si and Ge are visible. One may notice that the Ge peak is slightly off-center, indicating strain in the film.

$$
\begin{aligned}
q_x &= \frac{cos(\omega) - cos(2\theta - \omega)}{\lambda} \\
q_z &= \frac{sin(\omega) + sin(2\theta - \omega)}{\lambda} \\
\Delta q_x &= \frac{2}{\lambda} sin(\theta + \Delta\theta) sin(\Delta\omega - \Delta\theta) \\
\Delta q_z &= \frac{2}{\lambda} [sin(\theta + \Delta\theta) cos(\Delta\omega - \Delta\theta) - sin(\theta)]
\end{aligned}
\tag{2.2}
$$

From the reciprocal lattice units, we can determine the lattice parameters of the thin film. First, the symmetric (004) RSM data is used to correct for tilt, by determining the amount of rotation, α, required to align the experimental Δq_x from calculated Δq_x [48]. After the (004) and (224) RSMs are tilt-corrected, the (004) map can be used to find a_n of the thin film by measuring the distance between the substrate (Si) and epitaxial (Ge) peaks [49]. Similarly, the (224) asymmetric data is used to calculate $a_{p,Ge}$ by measuring the offset from the no-strain line (the line connecting the origin of the (224) map to the Si peak). After a_n and a_p are extracted, the lattice mismatches (f_z , f_{xy}, and f_{total}) and degree of relaxation, R. Equation 2.3 shows the calculations for relaxation, where Ge and Si have constants $\nu = 0.273$ and 0.277, respectively.

$$
\begin{aligned}
f_z &= \frac{a_{n,Ge} - a_{Si}}{a_{Si}} \\
f_{xy} &= \frac{a_{p,Ge} - a_{Si}}{a_{Si}} \\
f_{total} &= \frac{1 - \nu}{1 + \nu} (f_z - f_{xy}) + f_{xy} \\
R &= \frac{f_{xy}}{f}
\end{aligned}
\tag{2.3}
$$

Table 2.5 shows how the lattice mismatch and degree of relaxation change as a function of film thickness for the samples of Ge grown on Ge:C buffer in Fig. 2.15. Even for thinner films, close to ~40 nm, the degree of relaxation in the film is quite high, at ~88% relaxed. As the film gets thicker, extending to 111 nm, there is not much difference in R — now at 92%. In this same range of film thickness, however, the growth rate is nowhere near constant (refer back to Fig. 2.15), but instead is still in the process of exponentially increasing towards expected (Fig.2.8) values. Based on this, it is safe to dissociate strain effects on the growth rate changes observed in the Ge film.

Table 2.5: Strain Relaxation Parameters for Ge on Ge:C samples. Note: $a_{Ge}/\ a_{Si} = 5.658$ Å$/5.431$ Å$= 1.042$. For a graphical representation of a_n and a_p refer back to Fig. 1.2.

Ge Thickness (nm)	a_n (Å)	a_p (Å)	f_{xy} (%)	f_z (%)	Relaxation (%)
41	5.6811	5.6311	1.046	1.037	87.5
58	5.6750	5.6320	1.045	1.037	89.2
111	5.6688	5.6362	1.044	1.038	91.7

It is now verified that neither surface roughness nor strain effects are responsible for the increasing growth rate in the Ge film on the Ge:C buffer. Next we discuss the presence of C in the Ge:C and Ge films, and the role it plays in growth rate.

2.4.4 Carbon Distribution via Secondary Ion Mass Spectroscopy

Since we are growing a thin Ge:C film and purposefully incorporating C, it is useful to observe the distribution of C within the film. Samples were sent to Evans Analytical for secondary ion mass spectroscopy (SIMS) to analyze the distribution of C in our films. Figure 2.21 shows the SIMS analysis for a 85 nm Ge-on-Ge:C sample (heteroepitaxially grown on Si). The left side of the figure is the surface of the sample. Immediately at the

left we see a large tail of C that attenuates into the sample. This is adventitious C from atomspheric conditions that adhered to the surface before analysis, and is not of interest (in fact — it makes analysis more difficult). At the 85 nm depth, we see a clear bump in the C concentration, peaking near 0.1 atomic %, or 2×10^{19}cm^3. This is not enough C to compensate for the larger Ge atoms, but is still significantly higher than the solid solubility. Deeper than 85 nm we see the C concentration reduce in the epitaxially grown Si, before another large peak is observed near 125 nm. This is also adventitious C that was not removed during surface cleans prior to loading the wafer into the UHV-CVD chamber. This is clear evidence that a Si homoepitaxy layer is desired to ensure a clean Si-terminated surface.

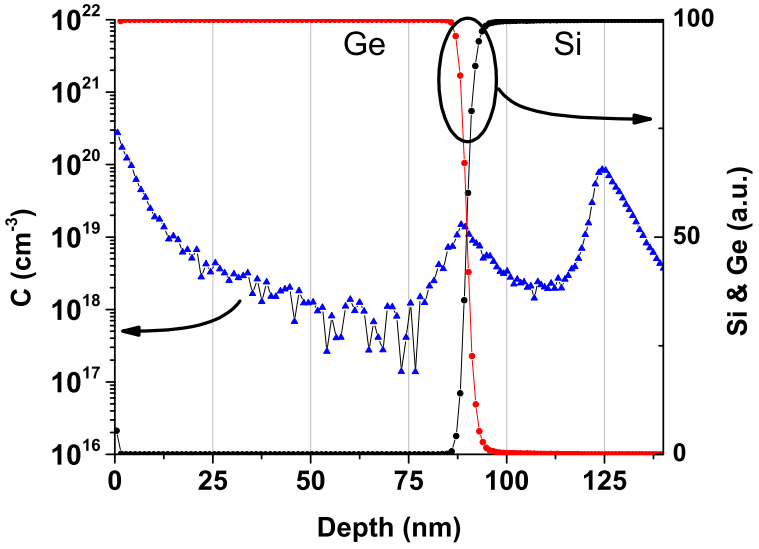

Figure 2.21: Secondary ion mass spectroscopy plot showing C concentration as a function of depth in a 85 nm Ge-on-Ge:C-on-Si sample.

The tails decreasing in depth (towards the right) in the SIMS plot are an unfortunate side-effect of the SIMS process, where the surface is sputtered away. The beam doing the

sputtering is larger than a single point, and the deeper that SIMS needs to go, the larger the area of the surface that is accidentally analyzed. The tails that decrease towards the surface, however, are more indicative of an actual decrease in C concentration. Of particular interest is the tail from the Ge:C buffer layer towards the surface. The slope is lower than that of the slope near ~125 nm, where the adventitious Si is immediately burried, showing that there is a slower decrease in C concentration in this area. This leads us to believe that there is an oversaturation of C on the surface during growth, which has the effect of retarding Ge epitaxy. While Kelly did show that some of the C in a Ge:C film is in fact sp^3 bonding [42], it is also likely that there is a buildup of interstitial C that slowly gets burried during growth. As growth continues, more C is buried, and GR can increase to expected level. Corroborating this idea is the evidence that increasing growth pressure during Ge:C growth will decrease GRs (recall Fig. 2.12). An increase in pressure yields more C on the surface, which retards growth rather than promotes it.

Cross-sectional TEMs of the Ge-on-Ge:C samples can be viewed in Fig. 2.22. Compared to the pure Ge film (a), the density of threading dislocations in the Ge-on-Ge:C (b) is greatly reduced and are more difficult to identify. The Ge:C buffer is difficult to see (C concentration is $< 1\%$), but is approximately shown by the white arrows. Part (c) of the figure shows a separate sample with just the Ge:C buffer layer grown. A few dislocations are visible (arrow), and the surface islands can even be identified. In fact, more dislocations are seen in (c) than in (b), suggesting that the defects get pinned near the interface.

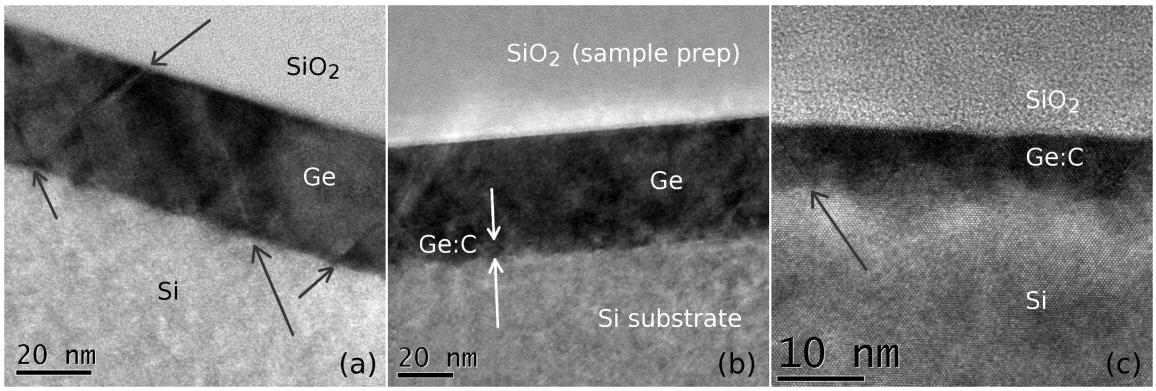

Figure 2.22: Cross sectional TEM images of (a) Ge-only, (b) Ge on Ge:C, and (c) Ge:C buffer only. Fewer defects are observed in the Ge on buffer sample (see arrows).

2.4.5 Hall Mobility of Germanium on Ge:C layers

Initial electrical analysis was performed by fabricating a Van-Der-Pauw (VDP) Hall structure. In these samples, n-type Si wafers were used to grow a 125 nm p-type Ge with 7 nm Ge:C buffer. The alternate carrier type creates an internal space-charge region at the interface to remove the influence of trap and defect-generated electron-hole pairs on mobility measurements. Diborane gas was flown during the Ge growth phase, and the incorporated B did not significantly affect the low R_q of the films. Using a VDP measurement with **B**=9T magnetic field, a carrier concentration of $\sim 1.5 \times 10^{18}$cm^{-3} was determined — a value comparable to that of state-of-the-art short-channel FETs. A control sample of 126 nm p-type Ge was used for comparison, and results are shown in Fig. 2.23. The sample with Ge:C buffer exhibited over 2x the mobility of the control Ge device, most likely due to its smoother surface and reduced defect density.

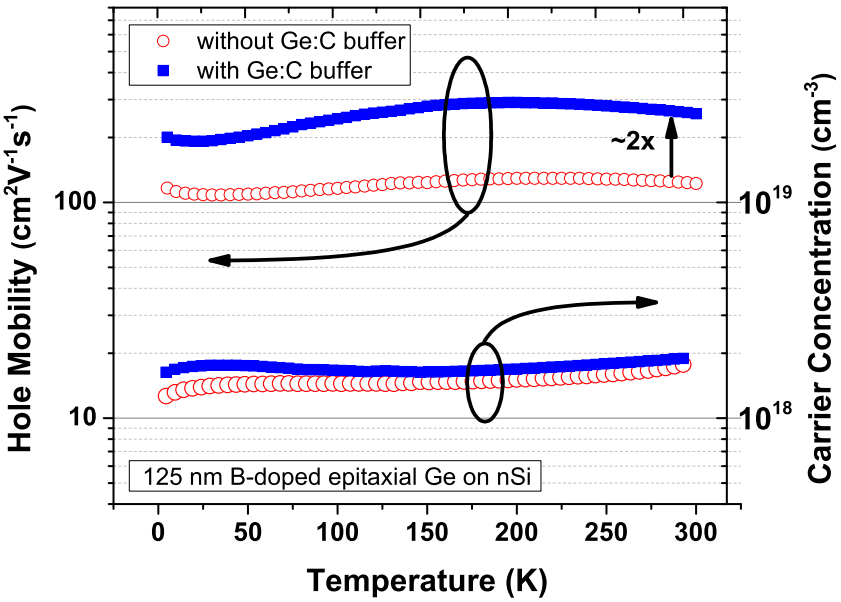

Figure 2.23: Carrier Hall mobility and carrier concentration as a function of temperature taken from a Van Der Pauw structure (**B**=9T).

2.5 Silicon-Germanium on Germanium:Carbon Buffer Layer

Silicon-germanium has been used in semiconductor research and industry for decades. Certainly one of the primary uses during this time has been strain and bandgap engineering for Si and Ge, and these SiGe layers have been necessarily grown on bulk Si for industry compatibility. Much effort has been made to create 'virtual substrates' of strain relaxed SiGe that sit atop a Si substrate, for much the same reasons that Ge heteroepitaxy is of interest as mentioned in 1.2. These virtual substrates can provide a wide range of lattice constants from which future strained layers can be grown.

2.5.1 Silicon-Germanium Epitaxy on Germanium:Carbon Buffer Layers

Generally, $Si_{1-x}Ge_x$ epitaxy using Si_2H_6 and GeH_4 allows for a wide range of growth conditions despending on the desired film properties [50]. While less common than SiH_4/GeH_4 systems [51] [52], this gas combination allows for lower temperature growth (sub-500°C). For otherwise similar $Si_{1-x}Ge_x$ growth conditions, higher T will yield lower Ge concentrations. Using the Ge:C buffer as described in Sec. 2.3, $Si_{1-x}Ge_x$ can be grown epitaxially to the effect of greatly reduced strain in the film, leading towards a simple method for virtual substrate formation.

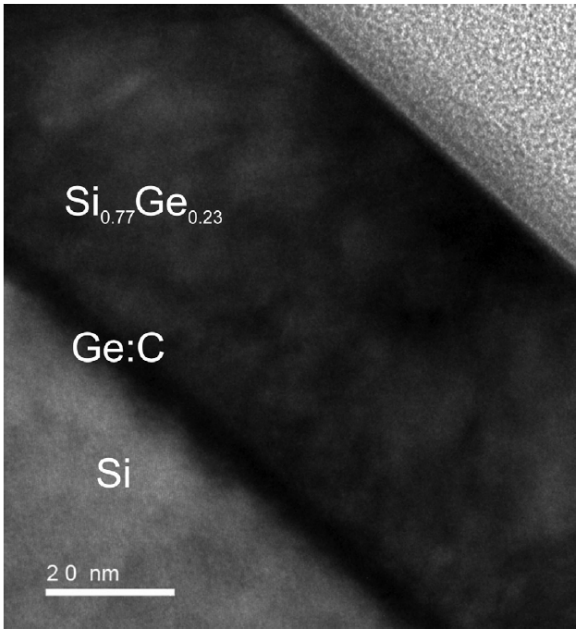

Figure 2.24: A XTEM image of a 50 nm $Si_{0.77}Ge_{0.23}$ layer grown on a thin Ge:C buffer.

Figure 2.24 shows a XTEM image of a 50 nm $Si_{0.77}Ge_{0.23}$ film grown on a Ge:C buffer. Virtually no defects are visible in the film, and a low R_q of 0.28 nm RMS was

measured. Of interest is the growth time required for the $Si_{1-x}Ge_x$ film on Ge:C. An additional ~5 min of growth at 550°C was necessary to achieve similar thickness (~10 vs 15 min) to the control SiGe film without Ge:C. The assumption is the same that existed for Ge — that surface C is interfering with the epitaxy and that an effective incubation time is needed to bury the C before GR increases.

2.5.2 Strain Extraction of SiGe films on Germanium:Carbon

The lattice constants and relaxation of the $Si_{1-x}Ge_x$ films grown both with and without Ge:C buffer layers were also extracted from XRD RSMs. A comparison between two 50 nm $Si_{0.77}Ge_{0.23}$ samples — both with and without a Ge:C buffer — is seen in Fig. 2.25. Notice that the SiGe peak in the sample with the Ge:C buffer (left) is in line with the origin, meaning the film is at least partially relaxed. The right images (without Ge:C), however, has a SiGe peak located directly beneath the Si substrate peak, indicating a fully strained layer. The pendellösung finges are also observed in the strained sample immediately above and below the SiGe peak, indicating pseudomorphic growth. The relaxation of the $Si_{0.77}Ge_{0.23}$ films are determined to be 107% and 0.3% for the buffered and non-buffered samples, respectively, illustrating that even a thin ($t < t_C$), otherwise fully-strained SiGe film can achieve a high level of relaxation with the insertion of a thin Ge:C layer.

A wide variety of Ge concentrations were grown to evaluate the effect of concentration on relaxation, as seen in Tab. 2.6. While $Si_{1-x}Ge_x$ films of high Ge concentration ($x > 50\%$) are possible in SiH_4/GeH_4 systems [53], x tends to be limited to ~30% or less in Si_2H_6/GeH_4 scenarios at typical UHV-CVD growth conditions. With the addition of the Ge:C buffer, however, we were able to achieve concentrations of up to $Si_{0.35}Ge_{0.65}$, all of

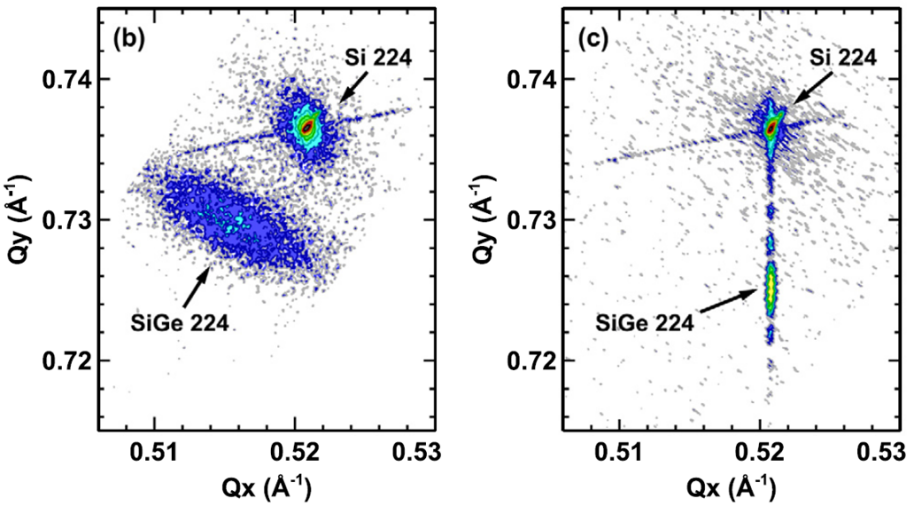

Figure 2.25: Asymmetric (224) XRD RSMs of 50 nm $Si_{0.77}Ge_{0.23}$ epitxial layers with (left) and without (right) a Ge:C buffer. The Ge:C buffer enables a nearly relaxed $Si_{0.77}Ge_{0.23}$ film.

which had a high $R > 90\%$, demonstrating the effectiveness of the Ge:C buffer at forming virtual $Si_{1-x}Ge_x$ substrates. For all of these films, AFM roughness data showed smooth films, with $R_q < 0.4$ nm RMS.

Table 2.6: The surface roughness and degree of relaxation for samples of varying Ge concentration, as measured by XRD RSMs. AFM data included as well.

Ge Mole Fraction	Ge:C Buffer	Growth T (°C)	R (%)	R_q (nm)
0.23	no	550	0.3	0.14
0.23	yes	550	107	0.28
0.38	yes	550	103	0.39
0.50	yes	500	98	0.37
0.65	yes	450	96	0.33
1.0	yes	435	91	0.24

2.5.3 Defect Density Extaction via Etch-Pit Density Test

In an attempt to quantify the defect density of the virtual substrates, etch pit density (EPD) tests were performed on thick 500 nm $Si_{0.77}Ge_{0.23}$ samples. The extra thickness is required, as the samples were dipped into a dilute Secco etch ($K_2Cr_2O_7$:HF:H_2O=1:2:6) (250 nm etch), where SiGe defects and dislocations are preferentially etched. A cross-hatching pattern as seen in Fig. 2.26 arises because of the relaxation mechanism that happens during thick ($t > t_C$) SiGe film grown — a network of threading dislocations in a cross-hatch pattern [54]. On the other hand, Fig. 2.27 shows that a SiGe film grown with a Ge:C layer does not contain the cross-hatch pattern, but yields an occasional single-point defect. This supports the idea that the film is highly crystalline and contains few defects. Threading dislocation densities (TDDs) of the two films were calculated to be $\sim 1 \times 10^9$ and 2×10^4 cm^{-2}, respectively. Further corroboration of the improved crystalline quality comes from the etch rate of the surface of the two films (targeted at 250 nm). The buffered sample etched at ~1.7 nm/min, while the buffer-less sample etched at a much faster ~2.5 nm/min, hinting towards a superior film.

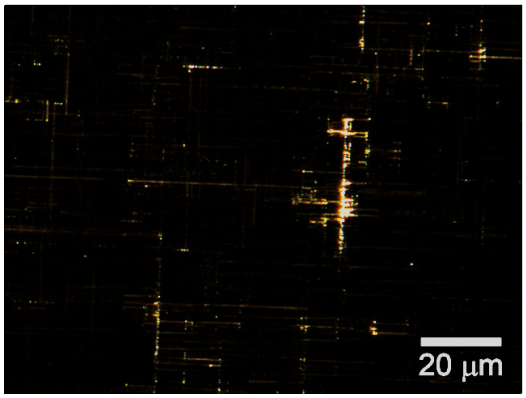

Figure 2.26: Optical microscope images of an EPD test on a 500 nm $Si_{0.77}Ge_{0.23}$ film without Ge:C buffer layer. Cross-hatch patterns are visible indicating high levels of threading defects. TDD ~10^9 cm^{-2}.

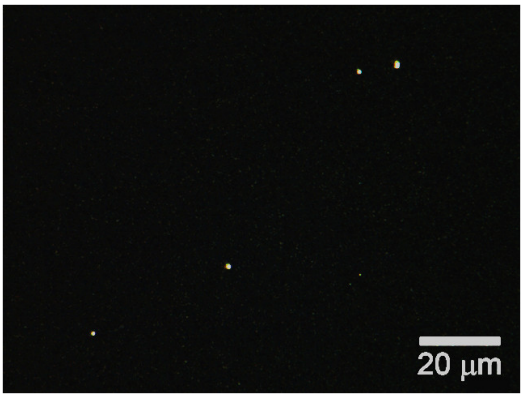

Figure 2.27: Optical microscope images of an EPD test on a 500 nm $Si_{0.77}Ge_{0.23}$ film with Ge:C buffer. Etch areas are visible, but no cross-hatch patterns are visible. TDD ~2×10^4 cm^{-2}.

CHAPTER III

Simulated Tunnel-FETs Utilizing Silicon-Germanium Virtual Substrates

Section 1.4 introduced Tunnel Field Effect Transistors (TFETs) as a means to replace conventional MOSFETs for future devices, particularly for enabling lower supply voltages (V_{DD}) and generally reducing power consumption via a steeper subthreshold slope (SS). Further power reductions can be attained by using heterostructures with different bandgaps, particularly a type-II interface (see Fig. 3.1) where the staggered-gap allows the conduction band (CB or E_c) of one side to lie very close in energy and real space to the valence band (VB or E_v) of the other when a voltage is applied to shift the bands [28]. If sufficiently thin films are used, strain and quantum confinement can raise the energy bands away from E_c

Some of the work in this chapter has also been published elsewhere. The TFET simulations were published in "Strained-Si/strained-Ge type-II staggered heterojunction gate-normal-tunneling field-effect transistor" by W. Hsu, J. Mantey, L.F. Register, and S.K. Banerjee in Applied Physics Letters 103, 093501 (2013). W. Hsu performed the simulations, J. Mantey assisted in TFET design, and L.F. Register and S.K. Banerjee advised.

and E_v, further separating the energy levels, having the effect of reducing OFF current.

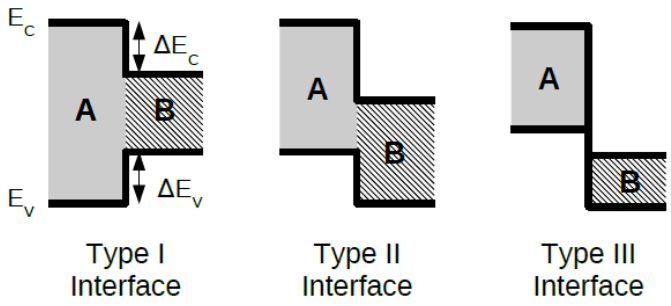

Figure 3.1: The types of possible interfaces created when two different semiconcutors are brought into contact. In a type-I interface, one gap lies completely within the second. Type-II is a staggered interface, where the VB (or CB) lies within the gap of the other, but not the CB (VB). Type-III interfaces (rare) has one band completely above the other.

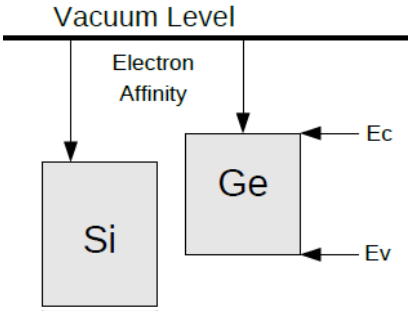

Figure 3.2: Figure showing the type-II interface of Si and Ge. Both E_c and E_v of Si lie below those of Ge's E_c and E_v. SiGe alloys lie in between (not linearly). Refer to Tab. 3.1 for the numerical details.

3.1 Gate-Normal Heterojunction TFET with Silicon and Germanium

When Si and Ge are put in contact, a type-II interface is created (Fig. 3.2. Based on the electron affinities, one would expect a ~$50meV$ E_c offset, and a larger E_v offset of ~$240meV$. In reality, due to strain caused by the lattice mismatch, these numbers will vary. Compressive (tensile) hydrostatic strain will increase (decrease) the energy gap, and uniaxial strain will lift the degeneracy of the bands. This is particularly important in an n-type Si/Ge TFET that tunnels from the source (E_v) of the p-type Ge to E_c of the n-type Si. The compressive strain in the Ge layer will increase its E_g, and the tensile-strained Si layer will lower in energy, allowing $E_{c,Si}$ and $E_{v,Ge}$ to get very close. In the traditional

TFET structure, heterostructures are difficult to fabricate, as two different semiconductors are required to be laterally in contact where the tunneling occurs, though it has been done [55]. However, non-classical structures, such as nanowire axial TFETs and gate-normal TFETs with their non-traditional geometries are able to overcome this fabrication difficulty [56] [57] [58].

Table 3.1: Silicon and Germanium Band Alignment. Silicon-Germanium alloys lie in between (not linearly, as the band gap changes from Δ to valley minimum).

Property	Silicon	Germanium
Electron Affinity	4.05 eV	4.0 eV
E_g	1.12 eV	0.67 eV
Valley of $E_{c,min}$	Δ	L
ΔE_c	56.2 meV	
ΔE_v	237.2 meV	

As alluded to in the introduction, one of the biggest problems facing the TFET is the comparatively low drive currents that can be achieved. Fischetti et. al. showed that in order for sub-$60\mu m$ devices to replace or compete with the MOSFET, drive currents need to be on the order of ~1-10 $\mu A/\mu m$ [59]. Because TFET devices have often have either high I_D or steep SS (but not both), it was difficult to compare various research that offer devices with either high currents or steep SS values. A figure of merit (FOM), the I_{60}, was created that takes into account both the SS and the ON-current, so more apt comparisons could be made across devices. Since SS is not constant in a TFET, but instead degrades at both low and high V_D, the I_{60} FOM tells the ON-current when the degradation is equal to 60 mV/dec. Typical drive currents in homojunction TFETs reported in literature are significantly lower than this — on the order of $10^{-4} - 10^{-3}\mu A/\mu m$, compared to MOSFETs that can reach $100\mu A/\mu m$.

The gate-normal SiGe TFET alleviates some of the concern regarding low I_D. First, the gate-normal TFET contains a vastly increased tunneling area since the entire area under the gate contributes to tunneling. The traditional TFET, on the other hand, focuses tunneling at the source/gate boundary in the semiconductor and only scales with width. Scaling concerns are addressed in [60]. In the gate-normal orientation, tunneling is also assisted by the gate-source potential, since the direction of the electric field is the same as the direction of tunnel transport, which can also further reduce SS [61][62]. The staggered gap gate greatly improves injection efficiency, and also significantly contributes to higher ON-currents [61].

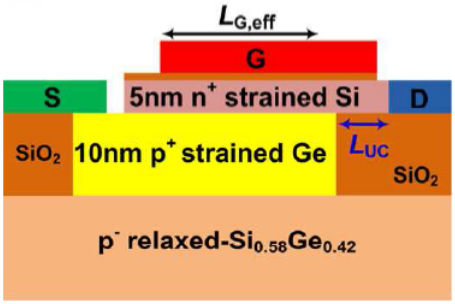

Figure 3.3: The cross section of the simulated TFET. Parameters as follows: $EOT = 0.6nm$, $L_{UC} = 10nm$, and $L_{G,eff} = 50nm$.

The structure considered in the following work is shown in Fig. 3.3. The starting substrate is a relaxed p-type ($10^{16}cm^{-3}$) $Si_{0.58}Ge_{0.42}$ film. The Ge:C buffered SiGe films of Sec. 2.5 can be used for this purpose, as a film of this Ge ratio is expected to be nearly perfectly relaxed (see Fig. 2.6) based on XRD-RSMs of similar films. Additionally, Ref. [63] calculated the band offsets for strained Si/Ge films with this mole fraction, and we utilize these values in our analysis. Atop this layer is a 10 nm (compressively) strained layer of p^+ Ge ($10^{19}cm^{-3}$), bounded by dielectric on either side. The source electrode makes ohmic contact with this layer, and this is the layer that will inject electrons through

the tunnel. The next layer is a 5 nm n^+ tensile strained Si layer ($10^{18}cm^{-3}$), which is connected to an ohmic drain contact above one of the sidewall dielectrics. As such, the film would need to be laterally overgrown, which is feasible in CVD chambers. Above this is the low-EOT gate dielectric (0.6 nm) and gate metal (work function 4.46 eV). While larger devices can be fabricated to further improve ON-current, $L_{G,eff}$ is set at 50 nm to better approximate in low dimension sizes required for todays devices. The undercut (L_{UC}) is set to 10 nm.

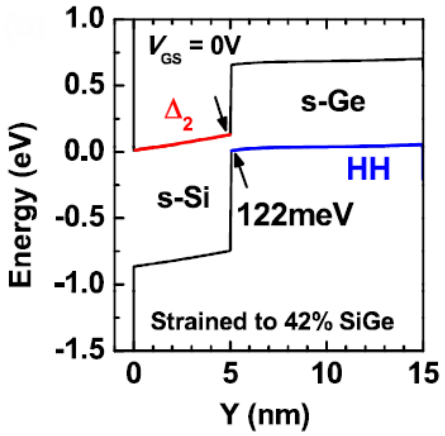

Figure 3.4: The band diagram for the device shown in Fig. 3.3 with no applied V_{GS}. $V_{DS} = 0.3V$ and $V_{GS} = 0$. $E_{c,min(Si)}$ is the Δ_2 split valley. Offsets taken from [63].

The energy-band diagram for the same device is shown in Fig. 3.4 and is taken from [63]. There is an effective bandgap of 122 meV between $E_{c,s-Si}$ and $E_{v,s-Ge}$ due to the band splitting induced by stress in the film. The splitting is so large ($> 3k_BT$) that only the Δ_2 band is considered for the s-Si drain in these simulations for the density of states (DOS) mass for electrons in $E_{c,Si}$. Similarly, only the heavy hole (HH) band is considered in the $E_{v,s-Ge}$, whose DOS effective mass uses the value for unstrained Ge HH band ($0.33m_0$). The 2-D self consistent simulation, were run in the commercial Sen-

taurus Device software. A Wentzel-Kramer-Brillouin based dynamic nonlocal path model for tunneling is used for BTBT across the Si/Ge interface. Fermi-dirac statistics, doping-dependent mobility, hydrodynamic transport, velocity saturation, and Schockly-Read-Hall (SRH) generation and recombination are included in the model. Quantum correction (via density gradient (DG) model) was also used, though it should be noted that this model does not properly account for the details of the band structure, but should be adequate for a first order approximation to quantum effects.

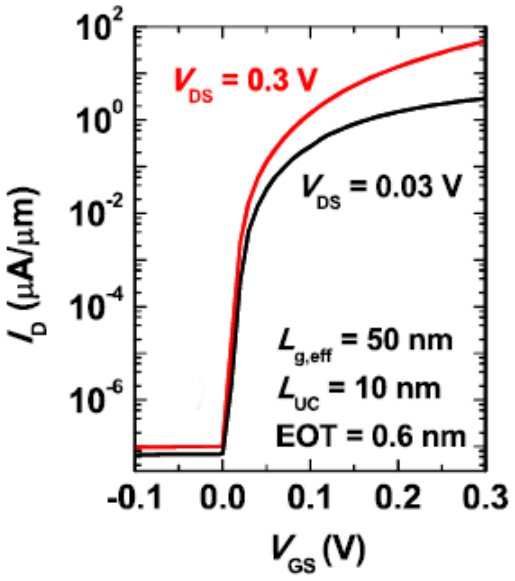

Figure 3.5: Transfer curve for the gate-normal Si/Ge TFET. High (10^8) ON/OFF ratio is observed and a sub-60 mV/dec SS (see Sec. 3.2) at low V_{GS}.

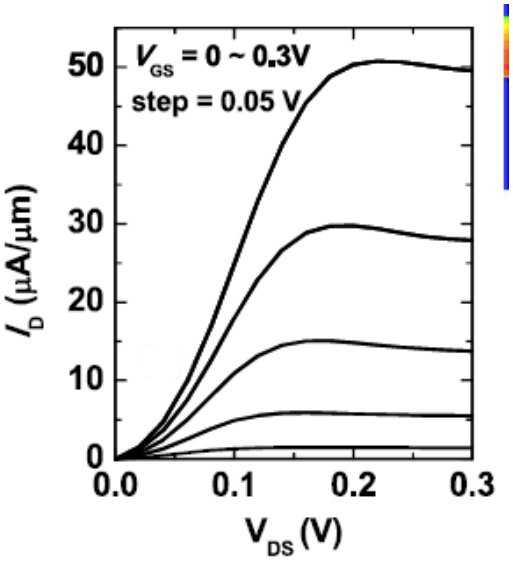

Figure 3.6: Drain output current for the gate-normal Si/Ge TFET. Negative differential output is observed, though minimal.

The results of the simulation are shown in figures 3.5 and 3.6. For both $V_{DS} = 0.03$ and $0.3V$, we see excellent gate control of the tunneling current. An I_{ON}/I_{OFF} ratio of 10^8 is achieved for $V_{DS} = 0.3V$. Threshold voltage is ~80 mV/V (using a constant-current, $I_D = 0.1\mu A/\mu m$ defined V_t). Peak current at $V_{DS} = 0.3V$ is ~$5 \times 10^1 \mu A/\mu m$. Looking

at the I_D output curves of 3.6, one does notice the slight negative differential for higher V_{GS} values after saturation. This phenomenon is widely observed and is due to charge pile-up in the s-Si channel and thus higher quantum-corrected potential which acts to reduce tunneling [59].

To obtain I_{60}, SS is plotted against I_{DS} as shown in Fig. 3.7 (and data taken from Fig. 3.5), where we find that $I_{60} = 0.8\mu A/\mu m$ — nearly in the $1 - 10\mu A/\mu m$ range that is necessary for competetive devices. The figure to the right of that (3.8) shows that doping in the s-Si layer only minimally affects the I_{60} value for a given doping in the s-Ge layer. The very slight decrease (at lower N_d) is primarily due to the increase of channel resistance to pull the charge out of the drain terminal.

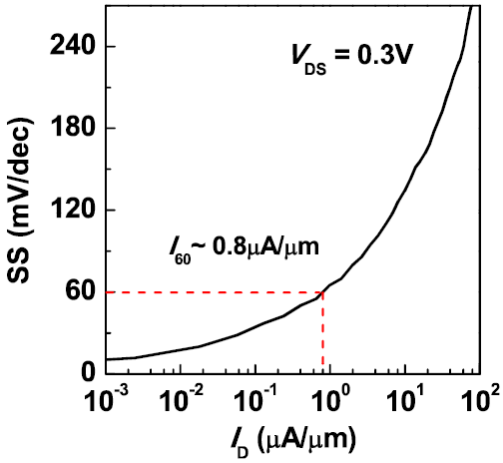

Figure 3.7: The SS vs I_D at $V_{DS} = 0.3V$. $I_{60} = 0.8\mu A/\mu m$ with $L_{G,eff} = 50nm$

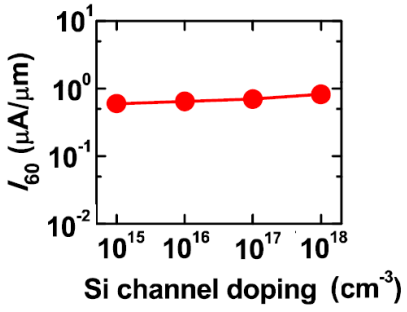

Figure 3.8: The role of doping in the s-Si layer for a fixed dopant density in the s-Ge layer. Almost no change is observed.

3.2 Deeper analysis of the Gate-Normal Si/Ge TFET

It is useful to get a better understanding of the underlying mechanisms behind this device and the effects of various parameters on the output curves shown in 3.5 and 3.6. We start by showing the generation of electrons in the TFET to analyze where the current is coming from. Figure 3.9 shows the BTBT electron generation rate for the 2-D cross section of the device, showing where electrons in the s-Si come from and how they contribute to the current. Part (a) shows the device at $V_{GS} = 0V$ and $V_{DS} = 0.3V$, in the off-state before we see any (significant) current at the drain. At the Si/Ge interface, we do not observe any BTBT, as we would expect due to the significant effective bandgap between $E_{v,Si}$ and $E_{c,Ge}$ states. The only generation that contributes to current exists in the s-Si film directly adjacent to the drain terminal. The cause of this is the short-channel related drain-induced barrier modulation (DIBM), which has the effect of lowering V_t and increasing SS at increased V_{DS}.

The effect of the undercut length, L_{UC}, is one of the primary contributers to DIBM in our device. As L_{UC} decreases from $15nm$ to $5nm$, I_{DS} in the off-state is increased dramatically as tunneling can exist diagonally from s-Ge towards the ohmic drain contact area. It is clear from Fig. 3.10 that significant undesired tunneling occurs for $L_{UC} < 7.5nm$. At lower $V_{DS} = 0.03V$, L_{UC} of even $5nm$ showed no subthreshold leakage issues. The choice of L_{UC} for simulation was thus chosen to be $10nm$ to avoid this DIBM.

Part (b) of Fig. 3.9 shows the device in the subthreshold region. At a gate bias $V_{GS} = 0.06V$, $E_{v,Si}$ and $E_{c,Ge}$ are close enough for occasional tunneling to occur. While the diagonal tunneling towards the drain has increased, the vast majority of the current ($> 10^5$ higher) comes from BTBT at the s-Si/s-Ge interface. Notice that the generation

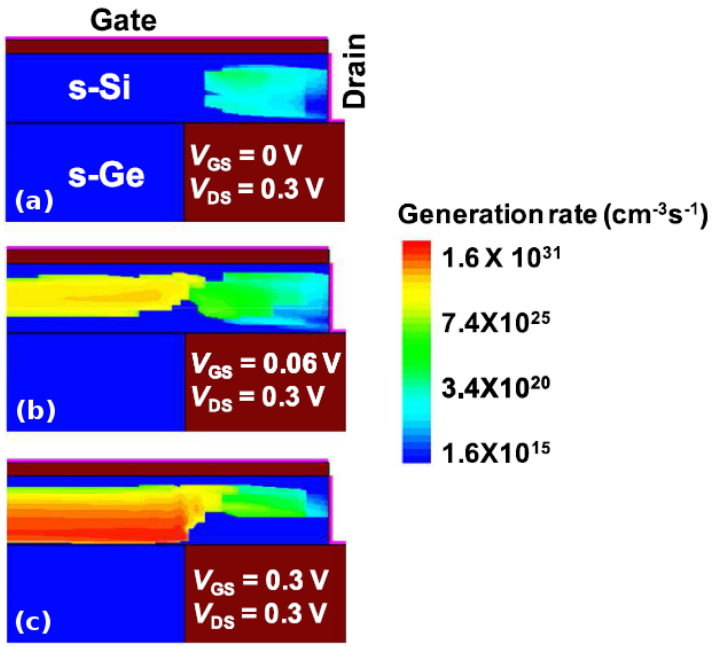

Figure 3.9: The generated electrons found in the s-Si in the device for (a) $V_{GS} = 0$ (OFF), (b) $V_{GS} = 0.06V$ (subthreshold), and (c) $V_{GS} = 0.3V$ (ON).

rate occurs towards the center of the s-Si layer, because the slope of the band due to V_{GS} yields lower energy closer to the gate, which is the area that tunneling first begins (with longer tunnel distances and lower probabilities). Continuing to increase the gate bias to the on-state ($V_{GS} = 0.3V$, see part (c)) continues this trend of increased BTBT at the interface, where the two energy levels are now similar, and the majority of the BTBT occurs right at the interface.

One can see the positive effect that strain plays in our simulated device in figures 3.11 and 3.11, which show the transfer and output characteristics of the device using valley-splitting (solid line) and artificially ignoring it (dashed line). In the two energy valley (Δ_2) mode, a ~$280meV$ degeneracy breaking is observed in the tensile strained Si, with the other four effectively not participating in conduction. In the $I_{DS} - V_{GS}$ curve, V_t is clearly

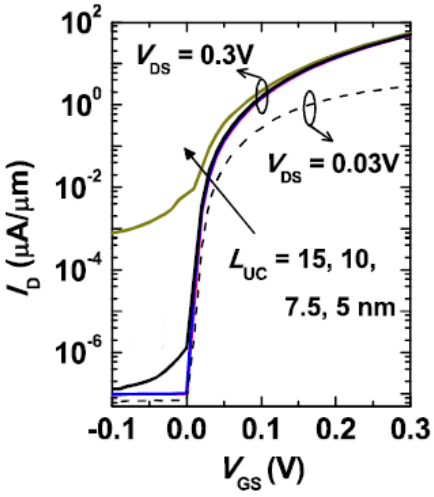

Figure 3.10: The effect that undercut length has on leakage current in the off-state. Reasonable I_{OFF} requires ~$L_{UC} > 7.5nm$.

observed to be lowered due to the splitting, as expected since $E_{c,Si}$ would start closer to $E_{v,Ge}$. The DIBM unrelated to the short-channel effects is minimal in this simulation due to the valley splitting of the s-Si, preventing unwanted BTBT. It is possible that a CVD-grown s-Si layer that is laterally overgrown as needed in this structure may not retain such valley splitting that we simulate here. The s-Ge underneath the Si is what causes the strain, since the crystal will extend upwards continuously. The overgrown portion will have an oxide underneath that does not encourage strain as much, so it's possible that the overgrowth will have less strain than desired. The two valley model achieves less V_t shift (~$80mV/V$ vs ~$220mV/V$) and higher I_{ON} in the $V_{DS} = 0.03V$ case, which allows greater conduction before saturation in the output curves of Fig. 3.12.

The I_{60} FOM was introduced for the traditional TFET layout, where tunneling occurs in a 1-D line in the semiconductor near the source/gated interface. Thus, I_{60} does not account for a gate-normal TFET as used in this work. Naturally, we can increase I_{60}

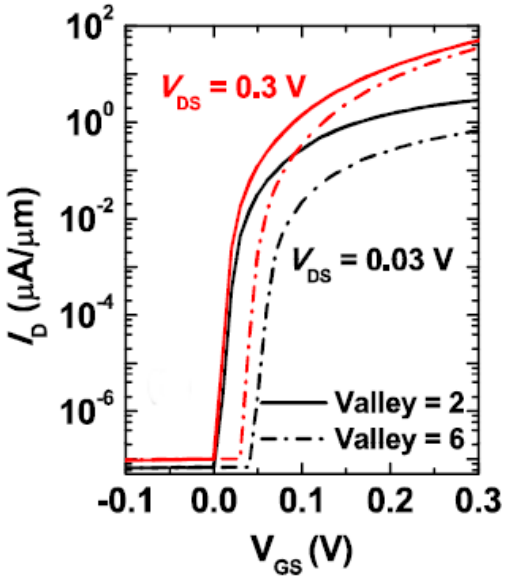

Figure 3.11: Transfer curves showing the benefits of strain-induced band splitting, compared to artificially degenerate Δ valleys in the Si layer.

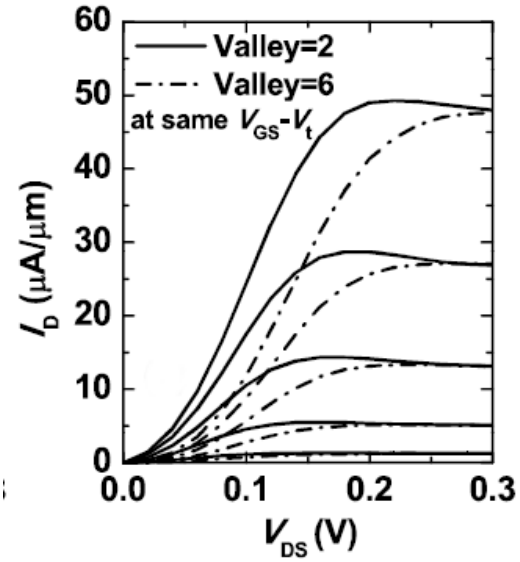

Figure 3.12: Output characteristics for two and six (artificially) degenerate Δ valleys in the Si layer E_c.

by increasing the gated area of our device, as shown in the inset of Fig. 3.13. There is an approximately linear relationship with $L_{G,eff}$ (and thus, area) and I_{60}, as more tunneling can occur. The rest of Fig. 3.13 shows the $I_{DS} - V_{GS}$ transfer relationship for $25nm \leq L_{G,eff} \leq 100nm$, where the drain current increases with effective gate length. One must keep in mind that despite the ability to increase I_{DS} with increased area, it will take additional charge to switch logic states, which would thus require more current.

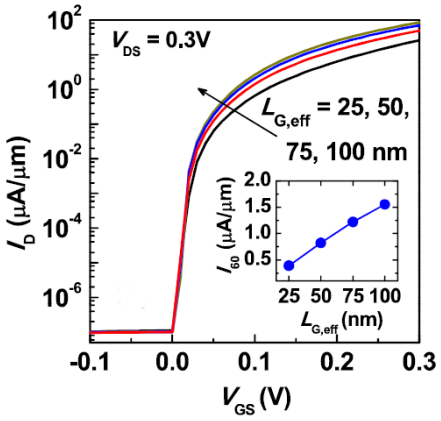

Figure 3.13: Output current and I_{60} metrics and their dependence on TFET gate area.

CHAPTER IV

Source-Drain Formation Via Spin-on Dopants for Germanium nMOSFETs

4.1 Advanced Doping Profiles in Germanium

Germanium nanowire transistors (to be discussed in Chap. 4.3) utilize a transistor structure with a cross section similar to that of the traditional MOSFET. The obvious difference being that the 'substrate' is measured in nm, and contains a gate that wraps around its entirety. Because of this, it is useful to discuss some of the issues facing Ge MOSFETs before moving on to Ge NW-MOSFETs.

Some of the work in this chapter has also been published elsewhere. The SOD devices were published in "High-Performance Ge nMOSFETs With n^+-p Junctions Formed by "Spin-On Dopant"", by M. Jamil, J. Mantey, E.U. Onyegam, G.D. Carpenter, E. Tutuc, and S.K. Banerjee in IEEE Electron Device Letters, Vol. 32, No. 9, pp. 1203-1205 (2011). M. Jamil and J. Mantey fabricated and characterized the SOD devices, E.U. Onyegam introduced the SOD process flow, and G.D. Carpenter, E. Tutuc, and S.K. Banerjee advised.

Modern Ge p-MOS devices have been suitable as Si replacements for some time now in planar devices. Germanium has the largest semiconductor hole mobility (~$4\times$ that of Si), which leads to improved source injection velocity (ν_{inj}) and thus a higher saturation drive current, I_{ON} — even nearing the ballistic limit [64]. The improved I_{ON} has has been experimentally observed demonstrating the feasibility of Ge pMOS [65] [64]. Mobility can even be further improved by using compressive strain [66] and quantum well structures [67][68]. In addition to the improved hole mobility of Ge, high concentration acceptor doping of Ge is comparatively easy with low thermal budgets (as low as ~$400°C$ [69]). Silicon can be introduced to form $Si_{1-x}Ge_x$, which allows for exceptionally high ($> 10^{21}$) source/drain activations (with the side benefit of free compressive strain with an Si channel to further improve mobility) [70]. This provides great ohmic contacts to the source and drains of Ge pFETs. If this was not enough, point defects in Ge lie energetically close to the valence band [71], which creates acceptor-like states. When inverting a n-type Ge channel, the inadvertent surface states that can pin the fermi energy near the valence band only help conduction

It is much more difficult to fully activate high concentrations of donors in Ge, however. One of the key difficulties in achieving a completely Ge CMOS world is the formation of good n+/p junctions at the source and drains of Ge nFETs. Particularly, the junctions need to be shallow, with low amounts of diffusion during activation, and have high levels of activation ($> 1 \times 10^{20}$ cm^{-3}). Unfortunately, these conditions are not easily met for Ge n^+/p junctions.

The first problem is the low activation level of P in Ge. Despite a high solid solubility of P in Ge of ~$2 \times 10^{20} cm^{-3}$, P has trouble activaing over ~$1 \times 10^{19} cm^{-3}$, which is less than desired for modern scaled FET devices [72]. Secondly, high activation temperaturs

are required to achieve those values, and at these temperatures P rapidly diffuses, so sharp, thin profiles are a challenge. Outdiffusion of P during annealing is also observed, lowering the effective surface concentration. Perhaps the largest obstacle that needs to be tackled, however, is the acceptor-like defect levels in Ge pinning the fermi level near the valence band which creates a schottky contact at the source and drain. This is all in addition to the ion implantation EOR damage mentioned in Sec. 1.3 that exacerbates the fermi pinning issue.

To tackle these concerns, Ge n^+/p junctions were formed using a P-containing spin-on dopant (SOD) which is driven in via a rapid thermal anneal (RTA). In principle, the process is similar to other solid-source diffusion methods, but is an attractive low-cost and simple method that lacks the defects that otherwise occur during implantation. The SOD is applied to the wafer in a method similar to photoresist, and is rotated at high RPMs to form a uniformly thin later. The samples are then annealed via RTA to drive in the dopants and the SOD is removed via a dilute HF solution, resulting in an a n+/p junction. Due to the simplicity of the method, it is easily integrated with modern fabrication processes. The process flow for SOD implementation is shown in Fig. 4.1.

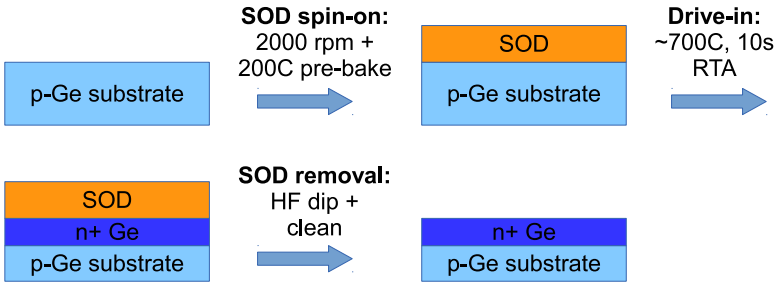

Figure 4.1: Process flow used for spin-on-dopant incorporation.

The SOD solution used in our n^+/p junctions is a commercially available product

from Filmtronics, Inc. The P507 solution was found to be the most compatible with Ge due to more similar coefficients of thermal expansion (CTE) [73]. Other solutions with higher and lower concentrations of P showed more cracking during the RTA step, due to the larger difference in CTE. The cracks primarily formed in the SOD film (though the Ge film was affected), but even in this case nonuniform dopant drive-in could occur. The typical process conditions for forming the n^+/p junction are shown in Fig. 4.1.

4.2 Material Analysis of Resulting Ge After SOD

Since SOD doesn't require physical implantation and instead relies on diffusion , there is no end-of-range damage. This limits the amount of acceptor-like defect levels deep in the implant range. For use in vertical Ge NW structures, deep implants would be required because it is not a planar surface device, instead needs to be implanted deeper, causing damage from implants such as that seen in Fig. 4.2. Additionally and perhaps more importantly, implants necessarily have concentration tails during implant, which would lead to a non-abrupt drain/channel interface and potentially EOR defects in the channel. We use Raman spectroscopy ($\lambda = 532nm$) to qualitatively determine the crystalline quality before and after SOD and ion implantation. Figure 4.3 shows the Raman data for the three

Table 4.1: Steps to form an n^+/p junction in Ge via SOD.

Step	Step Name	Typical Conditions
1	Surface prep	>100 C hotplate to remove adsorbed H_2O
2	SOD spin-on	2000 RPM for 30 s, 500 RPM ramp rate
3	Solvent Removal	Hotplate ramped from $90 - 200$°C (~20 min ramp)
4	RTA Drive in	650-750°C for 10 s, slow ramp-up of ~5 °C/s
5	Remove SOD	Dilute HF dip (~1%) for 120 s, Acetone, IPA, H_2O

cases. The lower intensity of the implanted case infers that there are fewer Ge-Ge phonon interactions with the laser and that the crystal quality is lower. The SOD peak is higher, but still lower than the bulk starting Ge.

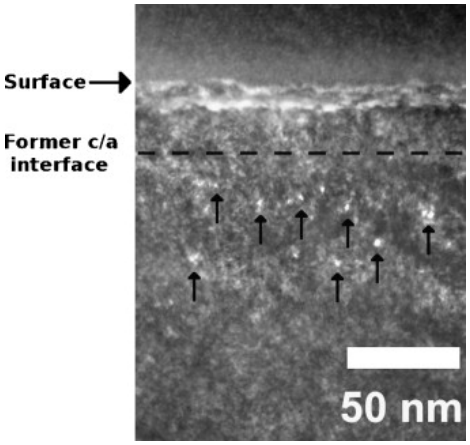

Figure 4.2: End-of-range damage of P-implanted Ge (Conditions: $15keV$, $1 \times 10^{15}cm^{-2}$ dose, $550°C$ anneal). From [74].

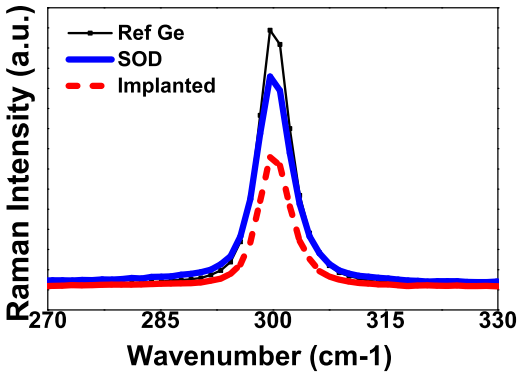

Figure 4.3: Raman spectra of P-implanted and P-containing SOD Ge samples.

4.3 Electrical Analysis of Resulting Ge After SOD

Diodes demonstrate superior electrical characterisitics for junctions with fewer defects in the space-charge region, and we can use this to analyze the SOD junctions. Figure 4.4 shows the electrical characterisitcs of two Ge n^+/p diodes, an SOD doped sample and an implanted control sample with dose of $1.5 \times 10^{15}cm^{-2}$ at $50keV$. Peak concentration was targeted to be the SS limit of P in Ge ($2 \times 10^{20}cm^{-3}$). A 550°C activation anneal was performed. The SOD process flow is shown in Tab. 4.1. Three immediate comparison points can be made. First the on-state currents are nearly the same, with the implanted

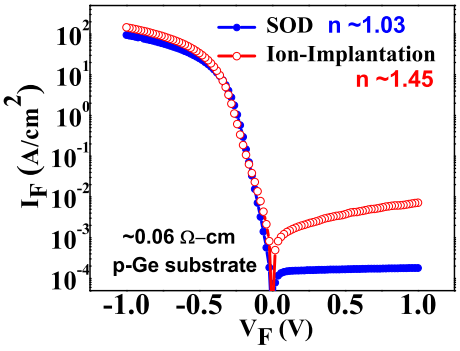

Figure 4.4: Diode characteristics from n+/p Ge diodes fabricated using SOD. Note the high I_{on}/I_{off} ratios.

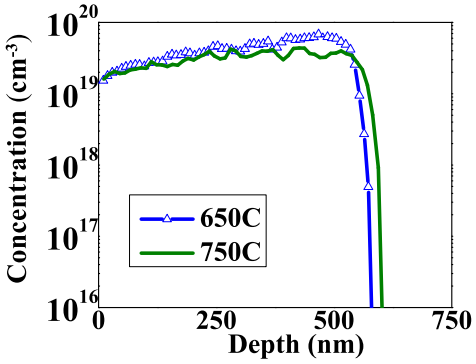

Figure 4.5: SRP measurements for n+/p Ge diodes fabricated via SOD. Note the peak activation near $10^{20}cm^{-3}$.

samples slightly superior. This could be due to series resistance if the SOD was not removed properly, leaving a barrier film interfering with the metal contacts. Secondly, the off-state currents are significantly improved in the SOD sample — two orders of magnitude improvement. The third quick observation is the far superior diode ideality factor (η) of the SOD sample ($\eta \approx 1$ vs $\eta \approx 2$). This shows the slope of the curve during on-off transistion in log scale governed by Eq. 4.1. The lower η of the SOD sample indicates more diffusion current, compared to the higher recombination current of the implanted sample [75]. Temperature measurements were also performed and found an activation energy E_A of ~0.67 eV. This matches the bandgap of Ge, thus corroborating evidence of a diffusion dominated device.

$$J_F \propto exp\left(\frac{qV}{\eta kT}\right) \tag{4.1}$$

Next we look at the spreading resistance probe (SRP) measurements of the SOD sample. As we see in Fig. 4.5, the peak activation level is approximately $7 \times 10^{19}cm^{-3}$.

This result surpasses the results of Chi On Chui (~$5 \times 10^{19} cm^{-3}$ [72]), which is one of the highest reported activation levels for P ion implantation. We observe a sharp box-like profile due to the concentration dependent diffusivity that is observed with P dopants in Ge [76]. Generally in highly scale devices, a sharp profile is desired, and an etch-back process could yield concentrated shallow and sharp P profiles in Ge. Germanium top-down nanowires (Chap. 4.3) is one case where a shallow junction is not necessary — though you lose the box-like profile for extremely deep junctions. While other methods — such as P + Sb co-implantation [77] or laser spike annealing[78] — can produce n^+ doping profiles in Ge of ~$10^{20} cm^{-3}$, SOD is both cost effective and provides nearly comparable results to these other methods.

A SOD process was also used to make MOSFET devices to analyze the difference between implanted and SOD-formed S/D junctions. Bulk Ge (100) 1-10 $\Omega - cm$ p-type wafers were used in a gate-last process for long-channel devices ($2\mu m < L < 100\mu m$) with a GeO_2 / Al_2O_3 / TaN ($2nm/10nm/200nm$) gate stack. The GeO_2 was formed via RTA in an O_2 ambient to better passivate the Ge surface, and the gate-last process was used to maintain the integrity of the GeO_2 layer, since $T > 450°C$ causes unstable GeO to form and degrades the passivation [79]. The Al_2O_3 was formed in a Cambridge NanoTech Fiji atomic layer deposition (ALD), and gate metal was formed via sputtered Ta in N_2 plasma. Source and drain contacts were made via a lift-off procedure consisting of a $5nm$ Ti $+50nm$ Ni e-beam evaporated metal stack.

Figures 4.6 and 4.7 show the I_D-V_G and I_D-V_D curves, respectively. The SOD devices are shown with the blue curve. In the I_D-V_G curve, we notice good gate control with an I_{on}/I_{off} ratio of ~$10^4 - 10^5$ and low off-state leakage of ~$3 \times 10^{-10} A/\mu m$. A SS of 111 mV/decade translates to a D_{it} of ~$2 \times 10^{12} cm^{-2}$ and is comparable to the midgap

D_{it} value found via quasi-static C-V (QSCV) of ~$9 \times 10^{11} cm^{-2}$. The implanted samples suffer from worse gate induced drain leakage (GIDL), which we attribute to lower defect density in the gate-drain overlap area that can cause trap-assisted tunneling. In the I_D-V_D curves, a ~30% enhancement in drive current is observed, and using (111) substrates gives an additional ~33% improvement is seen (not shown). Drive currents of ~$12 \mu A/\mu m$ at $V_G - V_t = 2V$ and $V_D = 1.5V$ are seen for a $L = 20 \mu m$ device.

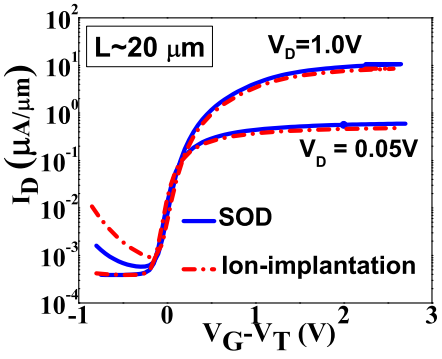

Figure 4.6: Transfer curves of Ge nFET with SOD and implantation. Good I_{on}/I_{off} ratios are seen for both, with reduced GIDL in the SOD sample.

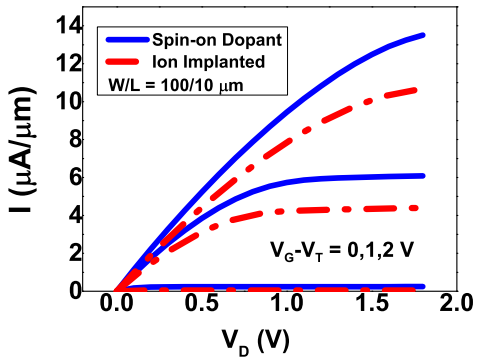

Figure 4.7: Drive current of Ge nFETs with SOD-formed source and drains.

Mobility data is extracted from linear $I_D - V_G$ and split $C - V$ curves and then corrected for series resistance and channel length via the total resistance-slope method [80]. Resulting high effective mobilities of 679 $cm^2/V^{-1}s^{-1}$ were found for the SOD devices, which represents a ~15% boost. We conclude that this is likely due to reduced charge trapping near the S/D junctions of the channel [81]. The (111) devices see even higher mobility (as expected) — nearly 50% higher and surpass the Si universal curve.

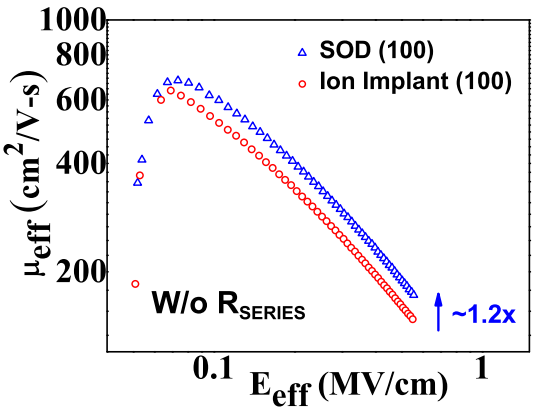

Figure 4.8: Effective mobility of SOD and implanted Ge nFETs with RTO GeO_2 + ALD Al_2O_3 dielectric stack and TaN metal gate.

CHAPTER V

Germanium Nanowire Field Effect Transistors

Nanowire MOSFET devices are one of the most promising MOSFET end-of-roadmap devices due to their tight gate control. Horizontal devices would yield good control, but would take up valuable real estate on a chip. Instead, using top-down vertical transport NWs could take up very little space while still providing the great transport.

Because of the high-density possibilities for top-down RIE etched NW devices, one potential application is use in DRAM, where a very high density of FETs is required. Using gate-lines and drain lines as word and bit lines, vertical transport DRAM MOSFETs could

Some of the work in this chapter has also been published elsewhere. This work modifies and improves a process flow that was introduced in "High-Performance Vertical Gate-All-Around Silicon Nanowire FET With High-κ Metal Gate" by Y. Zhai, L. Mathew, R. Rao, M. Palard, S. Chopra, J.G. Ekerdt, L.F. Register, and S.K. Banerjee in IEEE Transactions on Electron Devices, vol. 61, no. 11, pp. 3896-3900 (2014). Y. Zhai fabricated and characterized the devices, S. Chopra helped with fabrication, L. Mathew, R. Rao, M. Palard, J.G. Ekerdt, L.F. Register, and S.K. Banerjee advised.

be very dense. If additional drive current is required, several devices could be connected in parallel while maintaining tremendous OFF-currents due to the great electrostatic control.

5.1 Heteroepitaxial Design of Vertical Ge NW-FETs

Incorporating Ge with the preexisting Si infrastructure will be one of the key enablers for Ge microelectronics. Using the epitaxial growth methods of Sec. 2.4, thick high-quality Ge can be grown directly on Si. Using in-situ doping, which is commonplace in Si and Ge CVD epitaxy systems, it is trivial to create vertical $n^+/p^-/n^+$ or $p^+/n^-/p^+$ stacks that act as source/channel/drain structures in vertical transistors. Using electron-beam lithography, small circular dots can be patterned to act as a mask for dry etching NW structures into the epitaxial layer, as shown in Fig. 5.1.

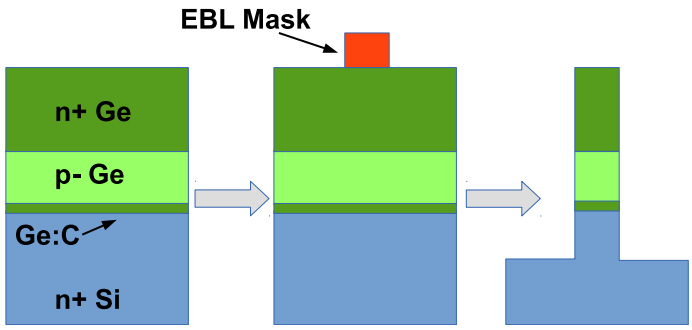

Figure 5.1: Nanowire fabrication process for a UHV-CVD grown Ge layer. E-beam lithography is used to pattern the nanowire diameter, which is dry-etched to form vertical Ge NW FETs. A $n^+/p^-/n^+$ stack is shown, but a $p^+/n^-/p^+$ stack is equally achievable.

The addition of the Ge:C buffer layer is optional in this configuration, since the goal of Ge:C is to create ultra-smooth surfaes by forcing defects to be confined to the buffer. Since NWs require vertical etching, and the FET surface will be vertical, the resulting epitaxy roughness is a secondary factor. However, in one specific scenario, the Ge:C plays

a critical role: in order to utilize the sharp step-like profile of a SOD-formed n^+ drain, we need to use temperatures of $\sim 700^\circ C$. At these temperatures — even for short time periods — Si and Ge intermix in a traditional Si/Ge heterointerface [82]. The addition of C in a Si/Ge system minimizes this interdiffusion [83]. Thus, by growing a Ge film of ~700-800 nm, one can use a SOD-formed 600 nm drain to consistently get channel lengths of ~100-200 nm. This can later be etched back if desired while maintaining the box profile.

It is equally possible to use ion implantation for long-channel NW devices. Due to the nature of ion implantation, there is a statistical distribution of implanted atoms in the crystal, modeled by the fitting of four moments (the Pearson IV distribution, see Sze's text [75]). There necessarily a tail of this distribution that limits the ability to form sharp drain/channel doping interfaces which forces the use of long-channel vertical architectures, since short-channel situations will exhibit punch-through, high ion-scattering, high series resistance, or a combination thereof. However, the modern use of source/drain extensions in planar FETs is effectively built-in to the drain side if the tail of the implant can be controlled appropriately.

A second issue with implanted drains and channels are the end-of-range defects briefly introduced in Sec. 4.1. In the traditional planar FET, these defects lie at the interface between drain and substrate far away from the action of the channel. While these defects can cause inadvertent leakage current via trap-assisted electron hole generation or recombination, this leakage mechanism is generally more benign than other short-channel effects of modern processes and are of less concern. In a NW architecture, however, the EOR defects will be present under the drain implant area — and right in the channel of the transistor. Considering that one of the main draws of the NW design is the excellent gate control and low off-state leakage, any defects created in this area would be catastrophic.

Using the SOD system gives both the sharp profile and eliminates EOR defects.

One may have initial hesitation to use the Ge:C buffer layer near the channel of the FET, since we are effectively using the C to force defects to this region so that the subsequent Ge layer has fewer. We can calculate that for research purposes, this fear is unfounded. For an individually addressable NW array, each NW has a small area, $A_{NW} = \pi r^2$, for $25nm < r < 100nm$, or $2.0 \times 10^{-11} cm^2 < A_{NW} < 3.1 \times 10^{-10} cm^2$. Qualitatively, TEM images show significantly fewer defects in the Ge-on-Ge:C-on-Si system at the interface compared to the Ge-on-Si system (see Sec. 2.4), but perhaps not so within the buffer layer itself. Typically reported TDDs for direct Ge heteroepitaxy in CVD are on the order of $10^7 cm^{-2}$ [84] [85]. Since threading dislocations propogate to the surface, we can estimate that each defect 'runs through' ~5 NW widths ($r = 100nm, t_{Ge} = 1\mu m$), so our effective density is $5 \times 10^7 cm^{-2}$. This calculates out to $5 \times 10^7 / cm^2 \times A_{NW} \approx 0.02$ defects per NW. Using a 10×10 array, we estimate a few NW to be defective at any point within the $1\mu m$ height, let alone just within the channel of the device. Thus, even if TDD in the buffer is an order of magnitude higher (qualitatively not the case), acceptable yields can be attained. It is understood that such methodology is adequate in research environments, but HVM would obviously require quantitative analysis of acceptable defects levels and empirical evidence of reduced TDD in the buffered samples.

5.2 Design Optimization for UHV-CVD Grown Ge NWs

Whether designing the NWs for implant or SOD processes, one must consider the channel conditions and scaling potential for the NWs. A series of simulations were performed via 1-D self-consistent Poisson and Schrodinger solvers to calculate the band diagrams in a

Si/Ge heterojunction NW system. The software used can be downloaded from Dr. Gregory Snider's (Notre Dame) website found in Ref. [86]. The tool is primarily aimed at III-V materials, so material properties for Ge were manually added. Figures 5.2 and 5.3 show a sample band diagram for both pMOS and nMOS NW stacks, using a fairly low-doped channels. It is apparent from these diagrams that for short channel devices, higher channel doping will be required. That said, for a NW, adding NW vertical space has a lower relative cost compared to long-channel planar devices, since the 2-D planar area stays the same regardless of depth. However, smaller total NW height will reduce cost and also make NW etching significantly easier due to the very high aspect ratios required. In our research devices, NWs higher than ~$1\mu m$ became significantly more difficult to maintain yield and cylindrical shape.

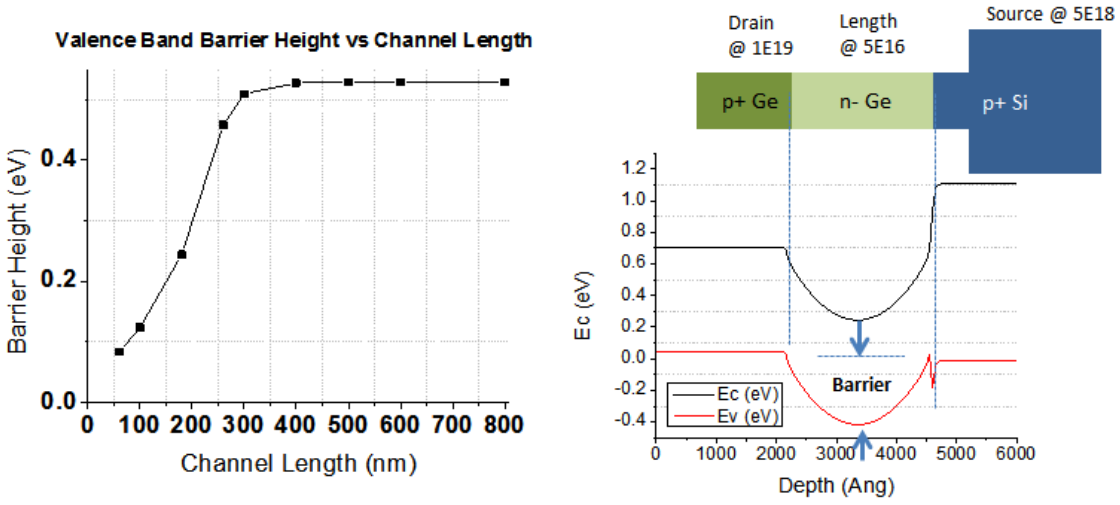

Figure 5.2: (a) Function of Band Offset vs Channel length for a $1 \times 10^{19}/5 \times 10^{16}/5 \times 10^{18} cm^{-3}$ Ge epitaxail $p^+/n^-/p^+$ NW stack. (b) Band Diagram for the 250 nm case. Note the lower relative drain doping and higher relative channel doping compared to Fig. 5.3, and how the curve shifted to the left (lower channel lengths required to keep high barriers).

All of the values used for these simulations are achievable in the UHV-CVD system. Based on SRP data of doped Ge grown in our system (not shown), Doping values on

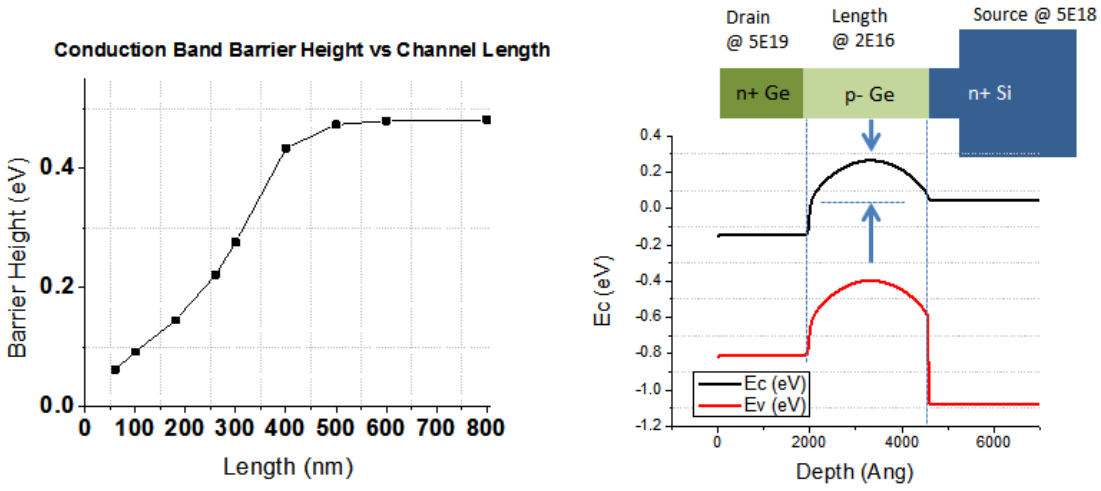

Figure 5.3: (a) Function of Band Offset vs Channel length for a $5 \times 10^{19}/2 \times 10^{16}/5 \times 10^{18} cm^{-3}$ Ge epitaxial $n^+/p^-/n^+$ NW stack. (b) Band Diagram for the 250 nm case.

the order of ~5×10^{18} can be achieved with high flow of high concentration ($100-1000 ppm$ B_2H_6 or PH_3) gases. At lower temperatures or with higher dopant concentration gases, ~$1 \times 10^{19} cm^{-3}$ should be feasible. On the low end, it is possible to achieve doping of ~10^{16} for both n and p-type Ge, but care must be taken as there is often memory-like conditions in the chamber, where particularly phosphine gas will continue to contribute to epitaxial layers for some time after its use. Luckily, low-dose conditions are unncessary in a Ge NW device, as we see in Fig. 5.4), where channel doping lower than $1 \times 10^{16} cm^{-3}$ or higher than ~$10^{18} cm^{-3}$ offer leakage mechanisms and would result in poor inversion-mode devices.

The final design chosen for epitaxial Ge NW device fabrication is shown in Tab. 5.1 and Fig. 5.5. Starting with a commonly available n^+ Si wafer, Ge is epitaxially growth (with or without Ge:C buffer) with a 200 nm channel and 600 nm drain height. This drain height is chosen based on SOD drive-in conditions, so if implant is utilized, this number

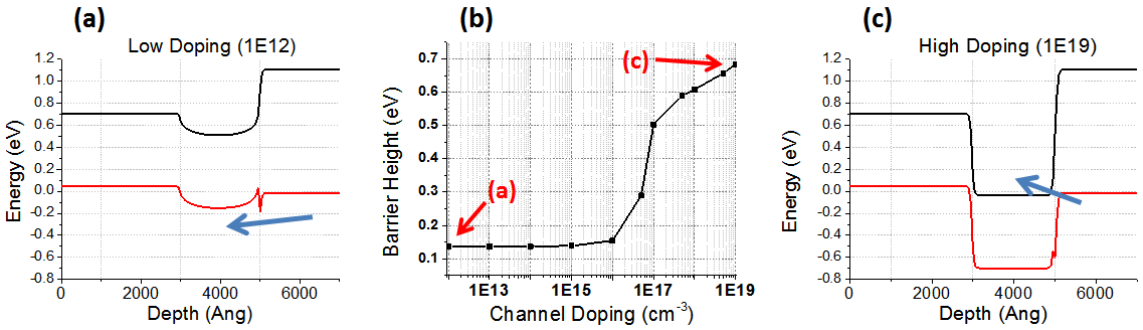

Figure 5.4: The effect of channel doping on a 200 nm NW Ge epitaxial pMOSFET. Drain and source doping are set at 1×10^{19} and $5 \times 10^{18} cm^{-3}$. (a) shows the band diagram at low doping, where there is effectively no barrier for holes to enter the channel. (c) shows the same with a highly doped channel, which can cause BTBT due to the sharp profile. Optimized doping levels will be in between.

can be reduced. The doping levels are set such that there is a high barrier ($\sim 500 meV$) and no overlap between E_c and E_v that could cause unintended tunneling ($> 100 meV$).

5.3 Germanium NW-FET Fabrication Process

Table 5.2 and Fig. 5.6 give a high level overview of the proposed fabrication process for individually addressable Ge NW FETs. Most of the steps will be described and further discussed in the following subsections. Any process details left out can be viewed in Appendix G.

5.3.1 Nanowire Formation

After UHV-CVD growth of the Ge n^-/p^+ or p^-/n^+ stacks (and perhaps the Ge:C buffer — see Fig. 5.1 for the desired result), a NW-diameter sized mask must be utilized for

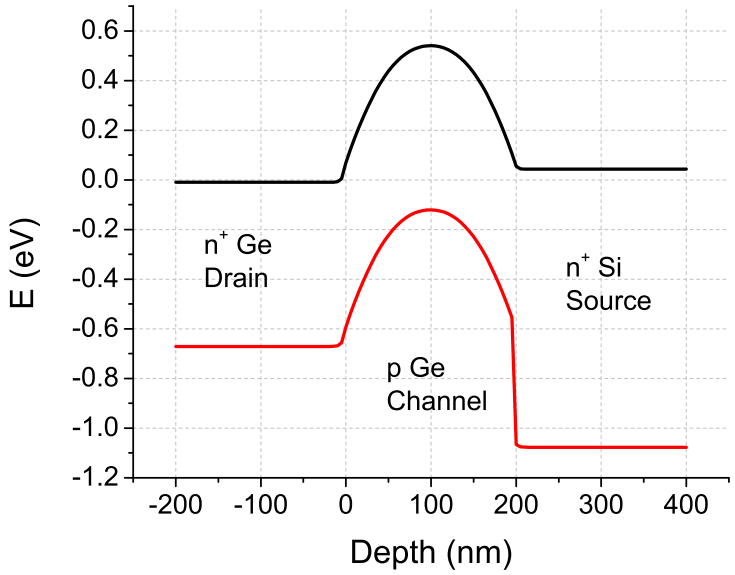

Figure 5.5: An optimized nMOS NW design. Same data as in Tab. 5.1. For a $200nm$ channel, a diameter of $< 75nm$ should be used.

dry-etching the NW vertically. The Jeol 6000 FSE was used to pattern circular dots of 50-200 nm diameters (among other structures, including fins) on positive e-beam resist. The resulting holes were blanketed by e-beam evaporated Ti/Ni layers and lifted off, leaving the Ti/Ni stack in only the patterned areas. After cleaning the resist off, the samples are loaded into an RTA furnace and annealed at $300°C$, a minimum needed to form NiGe [87]. This NiGe layer is used as the hard mask for deep-Si etching (DSE) via the Bosch process (or deep-Ge etching in this case), as introduced by the Robert Bosch corporation [88]. This method utilizes alternating deposition of polymer and strong etch steps for high aspect ratio dry etching of Si. The polymer that is deposited on sidewalls is not etched as effectively as the polymer on the planar surface, and it thus protects the sidewalls from additional etching. Since Ge is generally receptive to similar dry etch chemistries as Si (but generally etches at faster rates), the Bosch process can be similarly used for Ge etching.

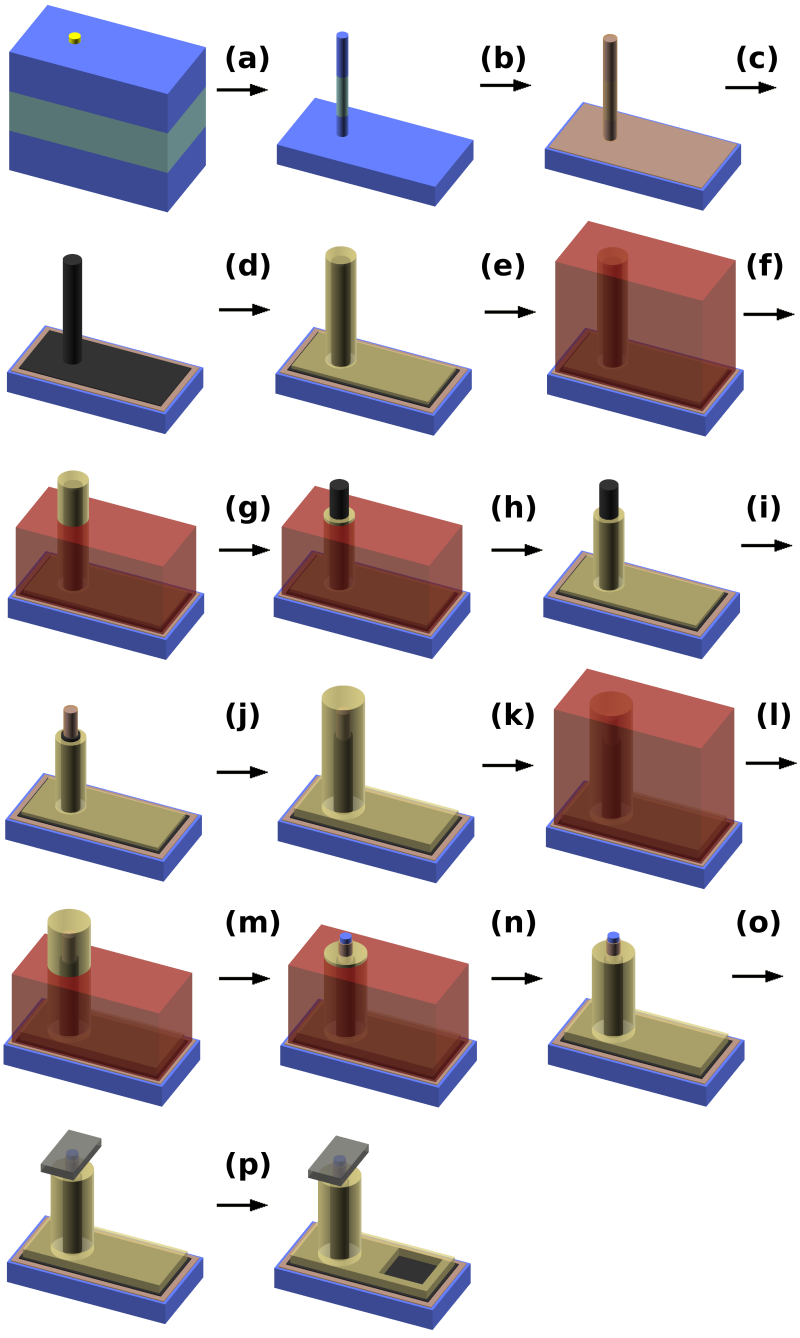

Figure 5.6: Process flow for vertical NW fabrication. See Tab. 5.2 for details.

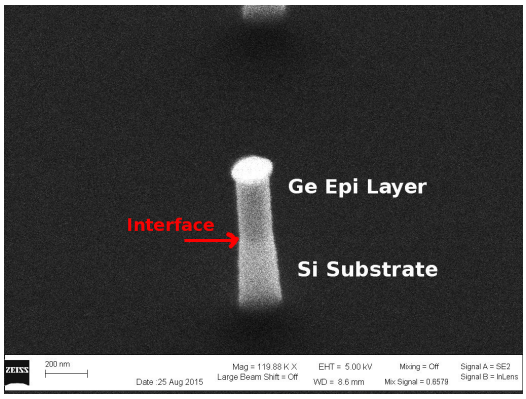

Figure 5.7: Remaining NW after DSE step. Images has been enhanced to show the interface of Si/Ge, with a Ge thickness of ~450 nm. Top NiGe layer is clearly visible.

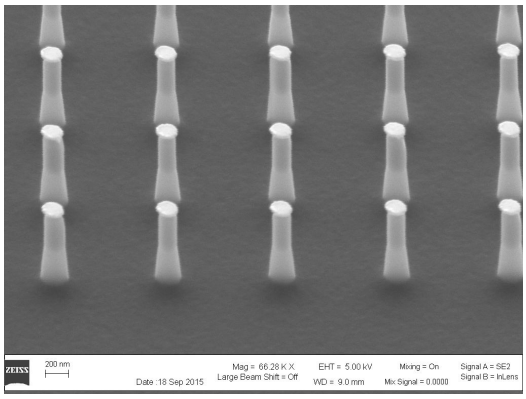

Figure 5.8: Unenhanced Ge-on-Si NW array.

Figures 5.7 and 5.8 shows the resulting NW after Bosch etch. In addition to the interface, one also observes the shape change throughout the NW. The Ge side is fairly cylindrical while the Si portion begins to broaden at the base. This is indicative of the slower-etching Si requiring different etch/deposition parameters. While this sample was over-etched, an optimally etched device (~100 nm below the Si/Ge interface would suffice) would not require such deep etching in the underlying substrate. The largest first-order variable for adjusting the shape of the NW is the ratio of etch and deposition times, as shown in Si by a previous student [89]. For the Ge NW devices, a deposition : etch ratio of $0.5s$: $1.2s$ yields a vertical profile for nearly $1\mu m$ worth of etching for a 200 nm diameter wire. Longer times with equal ratio yields visible scalloping along the NW edge.

The mask system that was designed for the NW project contains several zones, including individually addressable (via photolithography lines0, large arrays, and Fins). During optimization of the DSE etch, the large arrays were used for analysis of the etch

processes, as higher numbers of NWs gave a more uniform and better statistical idea of the effects of the DSE variables (etch and depositoin times, gas flows, and pressures). While excellent results could be achieved with the large arrays (see Fig. 5.9 and 5.10 imaged from the same etch), it was found that there was severe microloading effects taking place for the individually addressable NWs (spacing on the order of ~$10 - 20\mu m$ between consecutive devices). An example of this is observed in Fig. 5.10, where the NiGe layers disappear and the NW is etched nonuniformly (probably as the NiGe is removed) and at higher rates than the arrays.

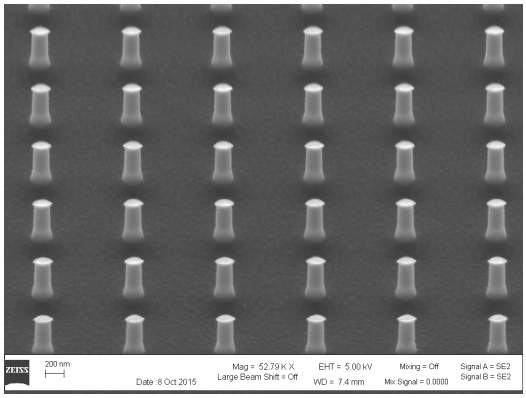

Figure 5.9: Large array of NWs ($200nm$ diameter, spacing of ~$0.5 - 1.0\mu m$) has high yield of excellent-shaped NWs.

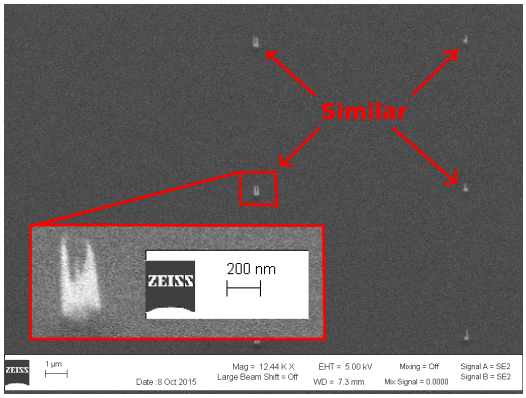

Figure 5.10: Single NWs ($200nm$ diameter, spacing of $\geq$ ~$10\mu m$) exhibit loading effects that etch the NiGe (and NW) faster than desired.

This microloading can be limited by reducing the RF Bias power during the thigh-power etch steps from $450W$ to ~$300W$. This has the negative effect of slowing etches (and reducing mask effectiveness), but because Ge etches quite fast relative to Si (~$2 - 4\times$ depending on the process), this is an acceptable compromise. When lowering the RF power, it is also important to note that the surface prep (cleans) are critical prior to etch. A systematic cleaning method should be used to eliminate variables at the surface. The best

cleans achieved for the Ge NWs after RTA NiGe anneal was an acetone/IPA/H_2O clean after short, low power O_2 plasma clean ($100W$, 2 min, in the Marsh Asher tool). Despite this optimization, in general one must choose to either optimize the array structures (great visibility and less variability) or the single NW structures (better for devices, harder to image, more variability).

5.3.2 Gate Stack Formation and Patterning

After the NWs are formed, a surface clean is performed followed by the gate stack deposition, which consists of a ~$15nm$ Al_2O_3 dielectric and a $\geq 30nm$ TiN Gate metal both of which are conformal ALD processes that can be done sequentially in-situ. For the conformal TiN in the Fiji ALD, either a thermal process (via TMAH + NH_3) or a plasma-enhanced (TMAH + N_2) can be used. The N_2 plasma process gives lower resistivity (per thickness) and slower wet-etching resistance compared to the Ammonium based thermal process, but requires longer growth times due to the plasma power cycling. In fact, for a given deposition time, the total areal resistivities of the two films are remarkably similar — one must just choose whether they desire the thicker film or the lower resistivity (but thinner) film. One is referred to Ref. [89] for details about the ALD TiN parameters.

The new gate metal must now be patterned. For the single-addressable NWs for DRAM use, the gate metal is used as a word line while the drain metal can be used as a bit line. As such, the gate metal must be patterned lengthwise to several NW in a row. Additionally, to make drain contacts to the top of the NW, the gate metal must be removed from this portion of the device. Because we want to minimize gate-drain overlap and undesired processing leakage, it is beneficial to perform a wet-etch of the TiN rather than a

dry etch. Perhaps equally importantly, dry-etching processes for TiN are moderately slow and may require thick masking, which is less desirable for small NW-sized features.).

The RCA Standard-Clean 1 (SC-1) (5:1:1 of H_2O:NH_4OH:H_2O_2) can be used for this purpose, since it attacks the Ti in the TiN film. While SC-1 is often performed at elevated ($\sim 70-80^{\circ}C$) T, a room temperature clean can be used for controlled, slow etching which is ideal for gate metal etching. In the concentrations above, SC-1 etches TiN at a rate of $\sim 2nm/min$ for the plasma N_2 TiN, and $\sim 3-4\times$ faster for the NH_3 version. This process is first masked off by a plasma-enhanced CVD (PECVD) SIO_2 layer of $\sim 30nm$, which is unaffected by the SC-1. The SiO_2 is removed in the desired locations by a combination of photoresist (PR) with lithography and an etch-back processes, as shown in Fig. 5.6(g) and Fig. 5.11. After etch-back, the sample is dipped in a buffered-HF acid (BOE) solution to remove the PECVD SiO_2 in the selected areas. The PR is stripped off, and samples proceed to the SC-1 steps as outlined above. Result after SC-1 is shown in Fig. 5.12. While not shown in the SEM image, the thicknesses of the TiN and SiO_2 layers can be verified. A reduced magnification view is seen in Fig. 5.13

5.3.3 Drain and Gate Metal Contacts

With gate metal lines etched as needed, we can proceed to pattern the drain metal and make contact holes for the gate pads. An additional layer of $\sim 100nm$ PECVD is deposited to separate the gate and drain. In a similar process to the previous etch-back step, PR is applied and patterned to open the gate contact hole. The PR is etched back to yield just the tips of the NW ($< 50nm$). Then, the samples are dipped in BOE to remove the newly-deposited PECVD in addition to the high-κ Al_2O_3 at the exposed NW tips. An SEM of

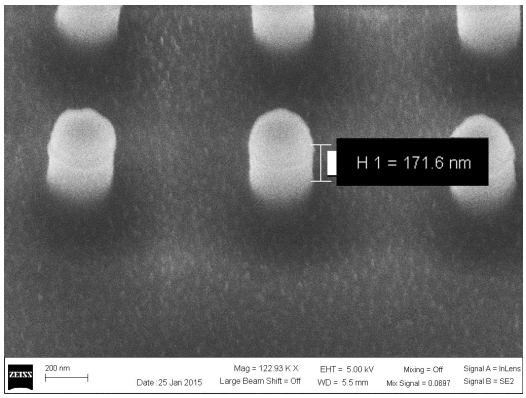

Figure 5.11: Etch-back exposure of NW tips (which have hi-κ + TiN + SiO_2). Approximately $200nm$ is exposed.

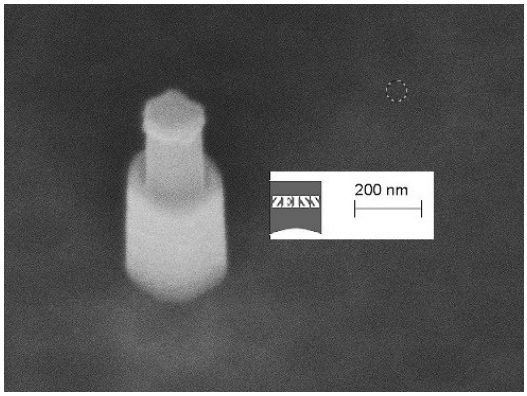

Figure 5.12: After SC-1, the TiN is etched away from the drain region (PECVD SIO_2 and TiN both etch away in this image).

the tip is shown in Fig. 5.14 during the etch back. Once all dielectrics are removed, PR is stripped, reapplied, and patterned in a lift-off pattern for drain-metal deposition. A $5/50nm$ Ti/Ni stack is e-beam evaporated and lifted-off with Baker PRS-3000 (acetone can work for this liftoff process, but is slower and requires sonication frequently). The resulting structure is shown in Fig. 5.15, showing both gate and drain contacts that individually address a single NW. A reduced magnification image shows the entire 4×4 addressable array including contact pads

This initial process flow yielded devices with effectively short-circuits between the gate and drain terminals. This was primarily due to an additional Al_2O_3 film that was placed atop the PECVD SiO_2 layer to slow down the etch rate for the drain contact. Because the sandwiched PECVD SiO_2 etched significantly faster in BOE compared to the capping and gate dielectric regions. there existed an air-gap between the gate metal and the newly-exposed NW tip (for drain contact). The metal liftoff process used deposited metal that short circuited the two terminals, so unfortunately electrical characterization has not

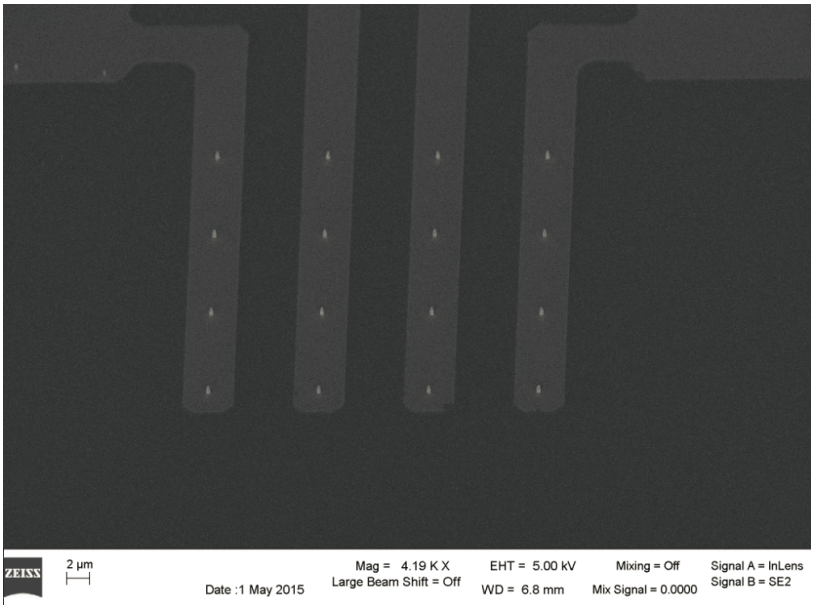

Figure 5.13: Reduced Mag view of the individually addressable 4×4 NW array, with the gate lines visible.

yet been performed. The Al_2O_3 capping layer was removed from the process flow listed above, and should eliminate this issue.

The process flow is completed and has had many trial runs (particularly for the initial steps) and should enable new students to quickly get results. In addition to the NW process that was carefully explained, the EBL pattern includes FinFET structures that generally did not exhibit the loading-effects experienced with the NWs and should perform admirably as well. Sufficiently small fins maintain most of the tight gate control that NWs do, with likely improvement in drive current.

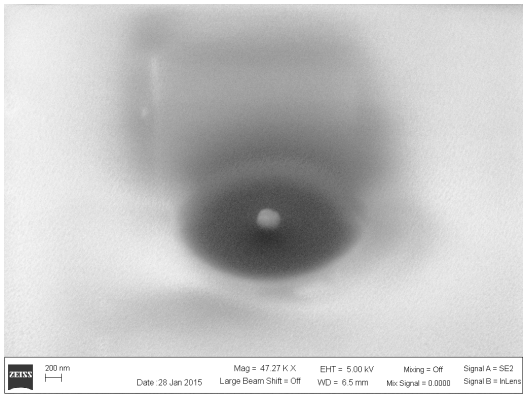

Figure 5.14: A second etch-back process to remove the oxides at the very tip of the NW for Drain contact. $\sim 80nm$ of NW tip is exposed (measured, not shown). The dark area above the NW is charging introduced during SEM. It is subsequently etched away.

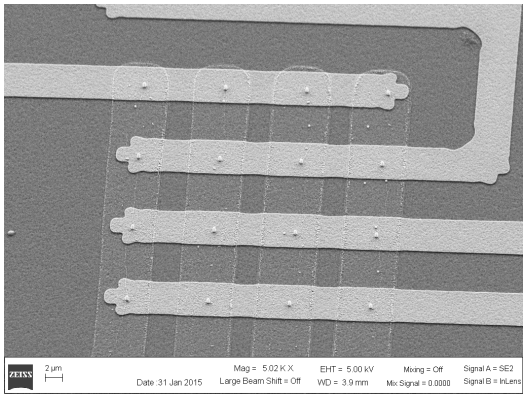

Figure 5.15: Final view of the individually addressable NWs with both gate (fainter) and drain (brighter) lines visible.

Table 5.1: Final design of the epitaxial nMOS NW device to be used in fabrication. Similar values for pMOS devices are found (but not shown).

Zone	Length	Type	Doping	Notes
Source	N/A	n^+ Si	$5 \times 10^{18} cm^{-3}$	Commonly available substrate with 0.001 $\Omega - cm$ resistivity
Chan.	$200nm$	p^- Ge	$1 \times 10^{17} cm^{-3}$	High barrier without E_c and E_v overlap ($> 100meV$ offset). $200nm$ length is sufficient for both SOD and DSE etching steps.
Drain	$600nm$	n^+ Ge	$5 \times 10^{18} cm^{-3}$	Enough depth for SOD process, or can be reduced for Implantation process. High enough doping for low R_{series}, yet low enough for achievable in-situ CVD-doping.

Table 5.2: Process overview for individually addressable Ge NW FETs. Visual overview for step letters can be found in Fig. 5.2.

Step	Details
Starting	Epitaxial NW stack is formed, and EBL is used to pattern NW diameter Ti/Ni stacks via e-beam evaporation and liftoff. Samples are annealed to form germanide dots with same diameter as desired NW for use as both DSE mask and germanide metal contact
(a)	DSE, ~800-1000 nm
(b)	10 nm ALD high-k (Al_2O_3) deposition
(c)	30-50 nm ALD TiN Gate Metal deposition
(d)	50 nm PECVD SiO_2
(e)	Photoresist (PR)
(f)	Etch-back to expose tip (most of drain exposed)
(g)	HF etch to remove PECVD SiO_2
(h)	Remove PR
(i)	SC-1 TiN etch to remove gate metal over drain and pattern gate pads
(j)	30 nm PECVD SiO_2
(k)	PR deposition
(l)	Etch-back to expose just the NW tip for Drain contact
(m)	HF etch to remove PECVD SiO_2 and ALD Al_2O_3
(n)	Remove PR
(o)	Pattern drain contact via Metal Liftoff
(p)	Open gate metal contact holes

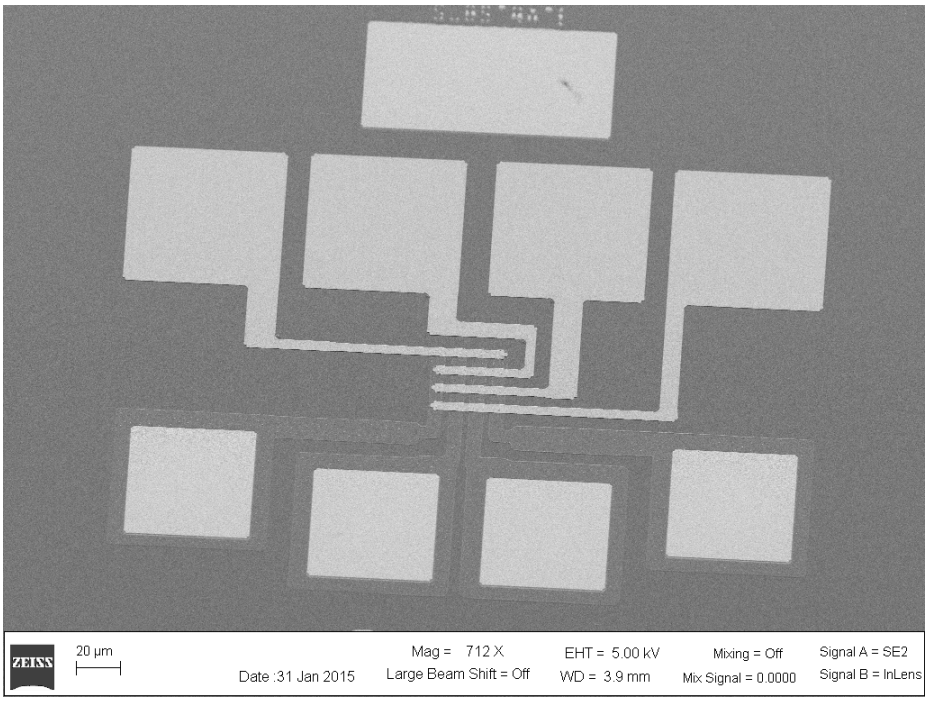

Figure 5.16: Reduced magnification view of the final structure for the individually addressable 4×4 NW array, including gate (bottom 4 pads) and drain (top 4) contact pads.

CHAPTER VI

Conclusions

6.1 Summary and Conclusions

With Moore's Law pushing into uncertain territory, researchers are investigating new materials and device architectures that can improve device performance (either in reducing power consumption or increasing speed and performance). In this, we have explored how Ge can fit into this new world. Because of the smaller bandgap and higher mobilities compared to Si, Ge is one of the few materials that has potential to replace or supplement Si.

In addition to the exciting possiblities available for Ge, the potential use for Ge:C buffer layers was considered. Using a $\sim 5 - 10nm$ buffer, ultra smooth films of Ge or $Si_{1-x}Ge_x$ can be easily incorporated atop a Si substrate, giving reduced defect densities and high degrees of relaxatin which can be used in virtual substrate applications. These thin buffers offer pathways to Si/Ge gate-normal TFETs and to thick Ge films for use with

vertial NW etching.

Beyond planar devices, we looked at how Ge can be used in these novel architectures like gate-normal TFET devices or vertical top-down nanowire FETs. These new structures enable exceptional gate-control (NW) or energy level misalignment (TFET) to provide the reduced OFF-state leakage currents that can push microelectronics forward into ultra-low power environments. In addition to the low power uses, our work has shown that Ge can at least be competitive with Si in TFET applications, and higher mobilities could drive competition on the performance front as well.

6.2 Recommendations for Future Work

It is an excellent time to be researching microelectronic devices. The potential switch from traditional planar MOSFETs to novel structures is exciting and could potentially lead to one of the greatest changes in the MOSFET IC since it was first invented.

The above works outlined the process flow for top-down Ge NW fabrication. While the initial run forced the discovery of a fabrication design flaw, this error has been corrected in the text above and should enable another user to quickly fabricate additional devices and proceed with characterization of single NW devices. In the same mask set, there is parallel arrays to enable higher ON-currents with arrays ranging from 4×4 to 100×100, and fin structures for vertical transport with similar goals. To further demonstrate the capabilities of the NWs, other channel materials or a denser construction via EBL gate and drain metal patterns could be used.

The TFET work showed promise in simulations, and naturally the next step is to fabricate the devices to empirically measure them. Perhaps the largest challenge will be

the controlled lateral overgrowth required to separate the drain and tunnel region, though lateral overgrowth has been researched [90], though often in MBE type environments. In CVD systems, often higher growth T or P is required for overgrowth, so an investigation on whether these process conditions affect the resulting films or their ability to laterally grow over oxide. Most Si/Ge TFET structures utizilze strain and rely in virtual substrates, so Ge:C buffer layers can be used in many of these cases.

APPENDICES

APPENDIX A
Abbreviations

Abbreviation	Full Name
a	Lattice parameter (Å)
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
bHF	Buffered HF acid (~6:1 $H_2O : HF$)
CB	Conduction Band
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DB	Dangling Bond
DIBL	Drain-induced Barrier Lowering (MOSFET)
DIBM	Drain-induced Barrier Modification (TFET)
DOS	Density of states
EBL	Electon-Beam Lithography
E_A	Activation Energy
E_c	Conduction band (level of energy)
EELS	Electron Energy Loss Spectroscopy
EOR	End-of-Range (Defects from Implantation)
EOT	Effective Oxide Thickness (nm)
EPD	Etch Pit Density
E_v	Valence band (level of energy)
FET	Field-Effect Transistor
FOM	Figure of Merit
F-vdM	Frank - van der Merwe (epitaxial growth mode)

Abbreviation	Full Name
GIDL	Gate-Induced Drain Leakage
GR	Growth Rate
HH	Heavy Hole (band)
HVM	High Volume Manufacturing
IR	Image Reversal (PR)
LN_2	Liquid Nitrogen
m_0	mass of an electron
μ_e	electron mobility (cm^2/Vs)
μ_h	hole mobility (cm^2/Vs)
MBE	Molecular Beam Epitaxy
ML	Monolayer
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
ν_{inj}	Source Injection velocity (cm/s)
N_a	acceptor concentration in a (p-type) semiconductor (cm^{-3})
N_d	donor concentration in a (n-type) semiconductor (cm^{-3})
nMOS	n-channel MOS(FET)
P	Pressure
PECVD	Plasma-Enhanced CVD
pMOS	p-channel MOS(FET)
PR	Photoresist
RIE	Reactive Ion Etch
R_q	See R_{RMS}
R_{RMS}	Root mean square surface roughness
RSM	Reciprocal Space Map (type of XRD Analysis)
SC-1	RCA (company) Standard clean 1
sccm	Standard Cubic cm/min (gas flow rate)
SCE	Short Channel Effects (of MOSFET)
SEM	Scanning Electron Microscope (or Microscopy)
SIMS	Secondary Ion Mass Spectroscopy
S-K	Stranski-Krastanov (epitaxial growth mode)
SOD	Spin-on Dopant
SRP	Spreading Resistance Probe (Measurement)
SS	Solid Solubility (cm^{-3})
STM	Scanning Tunneling Microscope (or Microscopy)

Abbreviation	Full Name
T	Temperature
t_C	critical thickness (nm)
TDD	Threading Dislocation Density (cm^{-2})
TEM	Transmission Electron Microscope (or Microscopy)
TFET	Tunnel-FET
TMAH	Tetrakis(dimethylamido)titanium(IV) (ALD Precursor)
TMP	Turbo-molecular Pump
UHV	Ultra-high Vacuum
UHV-CVD	Ultra-high Vacuum Chemical Vapor Deposition
VB	Valence Band
V_{DD}	Positive supply voltage
VDP	Van Der Pauw (Hall structure)
V_{SS}	Negative supply voltage
V_t	Threshold voltage
V-W	Volmer-Weber (epitaxial growth mode)
XRD	X-ray Diffraction
XTEM	Cross-sectional TEM

APPENDIX B
Example UHVCVD Ge Heteroepitaxy Recipe

22			VAT Commands		Disilane				Germane				Methylsilane				Manifold
Step Time (s)	C. Power	E. Power	Command	Value	Flow	V1	V2	EN	Flow	V1	V2	EN	Flow	V1	V2	EN	Manifold
300	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.1	0.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.2	0.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.3	0.6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.4	0.8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.5	0.9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.6	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.7	1.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.8	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.9	1.3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
90	1.8	2.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
140	4.6	6.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	4.2	5.7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
300	4.2	5.7	0	0	40	1	1	1	0	0	0	0	0	0	0	0	1
30	4.2	5.7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
20	2.3	3.15	5	0	0	0	0	0	0	0	0	1	0	0	0	0	0
90	1	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6.1: Recipe for Si homoepitaxy.

C(enter) and E(dge) Power are DC current values (Amps) sent to the cup heater C and E zones, respectively. VAT commands are commands sent to the pressure controller as follows: (0) No command. (1) Set pressure to <next column value (mTorr)>. (5) Open valve 100%. Gas flows are percentage of MFC. V1 and V2 are valves allowing gas access to the UHV-CVD system. E(nable) allows valves to be operated. Manifold is another valve for the gas lines.

APPENDIX C
Example UHVCVD Ge Heteroepitaxy Recipe

24			VAT Commands		Disilane				Germane				Methylsilane				Manifold
Step Time (s)	C. Power	E. Power	Command	Value	Flow	V1	V2	EN	Flow	V1	V2	EN	Flow	V1	V2	EN	Manifold
60	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.1	0.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.2	0.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.3	0.6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.4	0.8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.5	0.9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.6	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.7	1.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.8	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.9	1.3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
90	1.8	2.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
140	5.4	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
300	4.05	5.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
120	4.05	5.5	0	0	40	1	1	1	0	0	0	0	0	0	0	0	1
60	1.2	2.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
60	1.8	2.6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1200	2.3	3.4	1	12	0	0	0	0	50	1	1	1	0	0	0	0	1
20	2	3	5	0	0	0	0	0	0	0	1	1	0	0	0	0	1
90	1	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
30	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6.2: Example recipe for Ge heteroepitaxy.

See Appendix B for notes regarding the abbreviations of the recipe columns.

APPENDIX D
Example UHVCVD Ge:C Heteroepitaxy Recipe

26			VAT Commands		Disilane				Germane				Methylgermane				Manifold
Step Time (s)	C. Power	E. Power	Command	Value	Flow	V1	V2	EN	Flow	V1	V2	EN	Flow	V1	V2	EN	Manifold
600	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.1	0.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.2	0.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.3	0.6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.4	0.8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.5	0.9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.6	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.7	1.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.8	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.9	1.3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
90	1.8	2.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
140	5.4	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
300	4.05	5.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
240	4.05	5.5	0	0	40	1	1	1	0	0	0	0	0	0	0	0	1
60	1.2	2.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
70	2.9	3.7	1	10	0	0	0	0	0	0	0	0	7	1	1	1	1
600	2.7	3.7	1	10	0	0	0	0	100	1	1	1	7	1	1	1	1
600	2.7	3.7	1	5	0	0	0	0	100	1	1	1	7	1	1	1	1
30	2.7	3.7	5	0	0	0	0	0	0	0	0	1	7	1	1	1	1
20	2.3	3.15	5	0	0	0	0	0	0	0	1	1	0	0	0	0	1
90	1	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
30	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6.3: Example recipe for Ge:C heteroepitaxy.

See Appendix B for notes regarding the abbreviations of the recipe columns.

APPENDIX E
Example UHVCVD Ge-on-Ge:C Heteroepitaxy Recipe

30			VAT Commands		Disilane				Germane				Methylgermane				Manifold
Step Time (s)	C. Power	E. Power	Command	Value	Flow	V1	V2	EN	Flow	V1	V2	EN	Flow	V1	V2	EN	Manifold
600	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.1	0.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.2	0.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.3	0.6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.4	0.8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.5	0.9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.6	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.7	1.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.8	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.9	1.3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
90	1.8	2.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
140	5.4	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
300	4.05	5.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
240	4.05	5.5	0	0	40	1	1	1	0	0	0	0	0	0	0	0	1
60	1.2	2.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
70	2.9	3.7	1	10	0	0	0	0	0	0	0	0	7	1	1	1	1
600	2.7	3.7	1	10	0	0	0	0	100	1	1	1	7	1	1	1	1
600	2.7	3.7	1	5	0	0	0	0	100	1	1	1	7	1	1	1	1
30	2.7	3.7	5	0	0	0	0	0	0	0	0	1	7	1	1	1	1
30	2	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
600	2.7	3.7	1	12	0	0	0	0	50	1	1	1	0	0	0	0	1
600	2.65	3.65	1	12	0	0	0	0	50	1	1	1	0	0	0	0	1
600	2.6	3.6	1	12	0	0	0	0	50	1	1	1	0	0	0	0	1
20	2.3	3.15	5	0	0	0	0	0	0	0	1	1	0	0	0	0	1
90	1	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
30	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6.4: Example recipe for Ge-on-Ge:C heteroepitaxy.

See Appendix B for notes regarding the abbreviations of the recipe columns.

APPENDIX F
Example UHVCVD SiGe-on-Ge:C Heteroepitaxy Recipe

29			VAT Commands		Disilane				Germane				Methylsilane				Manifold
Step Time (s)	C. Power	E. Power	Command	Value	Flow	V1	V2	EN	Flow	V1	V2	EN	Flow	V1	V2	EN	Manifold
600	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.1	0.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.2	0.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.3	0.6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
50	0.4	0.8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.5	0.9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.6	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.7	1.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.8	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	0.9	1.3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
60	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	1	1.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
90	1.8	2.5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
140	4.5	6.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	4.05	5.65	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
300	4.05	5.65	0	0	40	1	1	1	0	0	0	0	0	0	0	0	1
60	1.2	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
70	2.5	4.15	1	10	0	0	0	0	0	0	0	0	7	1	1	1	1
600	2.4	4.13	1	10	0	0	0	0	100	1	1	1	7	1	1	1	1
600	2.45	4.2	1	10	0	0	0	0	100	1	1	1	7	1	1	1	1
600	2.45	4.2	1	3	0	0	0	0	100	1	1	1	7	1	1	1	1
10	2.45	4.2	5	0	10	1	1	1	80	1	1	1	7	1	1	1	1
60	3.2	4.95	0	0	10	1	1	1	80	1	1	1	0	0	0	0	1
1800	3.2	4.95	0	0	10	1	1	1	80	1	1	1	0	0	0	0	1
20	2.3	3.15	5	0	0	0	0	0	0	0	0	1	0	0	0	0	0
90	1	1.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30	0	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6.5: Example recipe for SiGe-on-Ge:C heteroepitaxy.

See Appendix B for notes regarding the abbreviations of the recipe columns.

APPENDIX G
Germanium Nanowire Process Flow

Step	Details
UHV-CVD Growth	• Covered in Detail in Secs. 2.4 and Appendix E
PL Mask 1 — EBL Align Mk	• HMDS Oven, 2 min prime • AZ5124E, 3500 RPM (for IR Process) • 90°C pre-bake on hotplate • 3.5s I-line exposure at 7.5 mW/cm^2 (Karl Suss MA6) • 45s 120°C hotplate (critical step) • 40s I-line flood exposure • 60s develop AZ 726 MIF
EBL Align Marks	• CHA 5 nm Ti + 50 nm Pt (limit temp) • Liftoff in PRS 3000 (or Acetone). Sonication and heat may be required
EBL	• ZEP 520 : ZEP 520A = 1:1, 4000 RPM, 40s • hotplate bake 180°C, 2 min • Nominal Jeol Exposure: 500 μC/cm^2 for 100pA current • Develop 2 min 3:1 IPA:MIBK • Rinse IPA
Deposit NW Metal	• CHA Ti 20 nm + Ni 20 nm • Liftoff with Acetone or Remover PG
Germanide Anneal	• AET RTA N_2 350C 60s to form NiGe
Deep Si etch	• DSE Etch Tool. Approximately 30 cycles of Dep/Etch = 0.5/1.2 sec, 125/40 C_4F_8 flow, 10 sccm Ar flow, 50 sccm SF_6 flow, 10/450W RF Power, No Morph, 20 mTorr. Yields ~600 nm etched

Step (Continued)	**Details**
Clean	• Acetone, IPA, H_2O, HF dip
Gate Stack	• Optional: GeO_2 RTO in AET, 600°C 10s in O_2 • ALD Al_2O_3, 10 nm (~100 cycles of thermal TMA+H_2O) • ALD TiN (thermal or plasma recipe ok). ~300 cycles for 15-22 nm depending on recipe • ALD Al_2O_3, few nm (protects TiN) • PE-CVD SiO_2 (45 nm, 90 s of recipe YJ-SiO02 in Plasmatherm I)
PL Mask 2 - Gate	• AZ MiR 703 Positive PR, 3500 RPM • 90°C pre-bake on hotplate • 6s I-line exposure at 7.5 mW/cm^2 (Karl Suss MA6) • 60s develop AZ 726 MIF • Etchback PR to expose 200 nm of NW. Use recipe YJ-O2-2 in plasmatherm 2 to etch ~143 nm/min in the O_2 plasma.
Etch Gate	• 15 sec BOE to remove PE-CVD SiO_2 • Remove PR (Aceteone, etc) • SC-1 at room temperature for ~15 min depending on TiN thickness (very slow etch)
Prepare for Drain	• PE-CVD SiO_2 (45 nm, 90 s of recipe YJ-SiO02 in Plasmatherm I) • AZ MiR 703 Positive PR, 3500 RPM • Etchback with YJ-O2-2 to expose < 100 nm NW for Drain contact • BOE etch PE-CVD + Al_2O_3 (~15sec). Be careful not to over etch here.

Step (Continued)	**Details**
PL Mask 3 — Drain	• HMDS Oven, 2 min prime • AZ5124E, 3500 RPM (for IR Process) • 90°C pre-bake on hotplate • 3.5s I-line exposure at 7.5 mW/cm^2 (Karl Suss MA6) • 45s 120°C hotplate (critical step) • 40s I-line flood exposure • 60s develop AZ 726 MIF
Deposit Drain Metal	• CHA Ti 5 nm + Ni 50 nm Liftoff with PRS 3000 or acetone Optional here: Metalization anneals
PL Mask 4 — Gate access	• HMDS Oven, 2 min prime • AZ5124E, 3500 RPM (for IR Process) • 90°C pre-bake on hotplate • 3.5s I-line exposure at 7.5 mW/cm^2 (Karl Suss MA6) • 45s 120°C hotplate (critical step) • 40s I-line flood exposure • 60s develop AZ 726 MIF
Open Gate Pad	BOE etch for combined PE-CVD SiO_2 and Al_2O_3.

Note that in between many of these steps, one must analyze the status of the samples via SEM, optical microscopy, ellipsometry, etc.

Bibliography

[1] G. Moore, "Progess in digital integrated electronics," in *International Electron Device Meeting*, pp. 11–13, 1975.

[2] R. Dennard, F. Gaensslen, H. Yu, L. Rideout, E. Bassous, and A. LeBlanc, "Design of Ion-implanted MOSFETs with Very Small Physical Dimensions," *IEEE J. Solid State Circuits*, vol. SC-9, pp. 256–268, 1974.

[3] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C.-H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, "A 90-nm logic technology featuring strained-silicon," *IEEE Transactions on Electron Devices*, vol. 51, no. 11, pp. 1790–1797, 2004.

[4] A. Khakifirooz and D. Antoniadis, "Transistor performance scaling: The role of virtual source velocity and its mobility dependence," in *IEDM Tech. Dig.*, pp. 667–670, 2006.

[5] J. Mathews and A. Blakeslee, "Defects in epitaxial multilayers: III. Preparation of almost perfect multilayers," *J. Cryst. Growth*, vol. 32, p. 265, 1976.

[6] D. Kelly, I. Wiedmann, J. Donnelly, S. Joshi, S. Dey, S. Banerjee, D. Garcia-Gutierrez, and M. JosÃ©-YacamÃ¡n, "Thin germanium-carbon alloy layers grown directly on silicon for metal-oxide-semiconductor device applications," *Applied Physics Letters*, vol. 88, pp. 152101–152104, 2006.

[7] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, and F. Evangelisti, "Ge/Si (001) Photodetector for Near Infrared Light," *Solid State phenomina*, vol. 54, pp. 55–58, 1997.

[8] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange, and F. Evangelisti, "Metal-semiconductor-metal near-infrared light detector based on epitaxial ge/si," *Applied Physics Letters*, vol. 72, no. 24, pp. 3175–3177, 1998.

[9] A. Nayfeh, C. O. Chui, K. Saraswat, and T. Yonehara, "Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: Surface roughness and electrical quality," *Applied Physics Letters*, vol. 85, no. 14, pp. 2815–2817, 2004.

[10] M. Horn-von Hoegen, M. Copel, J. C. Tsang, M. C. Reuter, and R. M. Tromp, "Surfactant-mediated growth of ge on si(111)," *Phys. Rev. B*, vol. 50, pp. 10811–10822, Oct 1994.

[11] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S.-i. Takagi, "Characterization of 7-nm-thick strained ge-on-insulator layer fabricated by ge-condensation technique," *Applied Physics Letters*, vol. 83, no. 17, pp. 3516–3518, 2003.

[12] J.-S. Park, M. Curtin, J. M. Hydrick, J. Bai, J.-T. Li, Z. Cheng, M. Carroll, J. G. Fiorenza, and A. Lochtefeld, "Low-defect-density ge epitaxy on si(001) using aspect ratio trapping and epitaxial lateral overgrowth," *Electrochemical and Solid-State Letters*, vol. 12, no. 4, pp. H142–H144, 2009.

[13] T. Janssens, C. Huyghebaert, D. Vanhaeren, G. Winderickx, A. Satta, M. Meuris, and W. Vandervorst, "Heavy ion implantation in Ge: Dramatic radiation induced morphology in Ge," *Journal of Vacuum Science and Technology B*, vol. 24, pp. 510–514, 2006.

[14] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "High mobility Ge pMOSFETs with 1nm thin EOT using Al2O3-GeOx-Ge gate stacks fabricated by plasma post oxidation," *Tech. Digest Papers Symp. VLSI Technol.*, pp. 55–56, 2011.

[15] L. Gomez, N. Chleirigh, P. Hashemi, and J. Hoyt, "Enhanced hole mobility in high Ge content asymmetrically strained-SiGe p-MOSFETs," *IEEE Elec. Dev. Lett.*, vol. 31, pp. 782–784, 2010.

[16] C. Chao-Ching, C. Chao-Hsin, L. Guang-Li, L. Ching-Lun, C. Hung-Sen, L. Jun-Cheng, K. Chi-Chung, H. Chien-Nan, and C.-Y. C., "Junction and Device Characteristics of Gate-Last Ge p- and n-MOSFETs With ALD- Al2O3 Gate Dielectric," *IEEE Transactions on Electron Devices*, vol. 56, pp. 1681–1689, 2009.

[17] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. Pianetta, H.-S. Wong, and K. Saraswat, "Experimental demonstration of high mobility Ge NMOS," in *IEEE Electon Device Meeting*, pp. 1–4, 2009.

[18] F. Trumbore and E. Porbansky, "Solvent evaporation technique for the growth of arsenic doped germanium single crystals for esaki diodes," *Journal of Applied Physics*, vol. 31, p. 2068, 1960.

[19] D. P. Brunco, B. D. Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. V. Steenbergen, P. W. Mertens, M. Meuris, and M. M. Heyns, "Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance," *Journal of The Electrochemical Society*, vol. 155, pp. H552–H561, 2008.

[20] C. Yu-Lin and J. Woo, "Germanium n+/p Diodes: A Dilemma Between Shallow Junction Formation and Reverse Leakage Current Control," *IEEE Transactions on Electron Devices*, vol. 57, pp. 665–670, 2010.

[21] M. Razali, *Phosphorus Activation and Diffusion in Germanium*. PhD thesis, University of Surrey, U.K., 2014.

[22] C. Chi-On, K. Hyoungsub, P. McIntyre, and K. C. Saraswat, "A germanium NMOSFET process integrating metal gate and improved hi-Î° dielectrics," in *IEEE Electon Device Meeting*, pp. 18.3.1–18.3.4, 2003.

[23] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High-performance GeO2/Ge nMOSFETs With Source/Drain Junctions Formed by Gas-Phase Doping," *IEEE Electron Device Letters*, vol. 31, pp. 1092–1094, 2010.

[24] Y. Hyun-Yong, Y. Nishi, K. Saraswat, C. Szu-Lin, and P. B. Griffin, "Germanium In Situ Doped Epitaxial Growth on Si for High-Performance n+/p-Junction Diode," *IEEE Electron Device Letters*, vol. 30, pp. 1002–1004, 2009.

[25] J.-P. Colinge, "Multiple-gate soi mosfets," *Solid-State Electronics*, vol. 48, no. 6, pp. 897 – 905, 2004. Silicon On Insulator Technology and Devices.

[26] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, "A new three-terminal tunnel device," *Electron Device Letters, IEEE*, vol. 8, pp. 347–349, Aug 1987.

[27] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond cmos logic," *Proceedings of the IEEE*, vol. 98, pp. 2095–2110, Dec 2010.

[28] L. Register, M. Hasan, and S. K. Banerjee, "Stepped broken-gap heterobarrier tunneling field-effect transistor for ultralow power and high speed," *Electron Device Letters, IEEE*, vol. 32, pp. 743–745, June 2011.

[29] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond cmos logic," *Proceedings of the IEEE*, vol. 98, pp. 2095–2110, Dec 2010.

[30] W. Cao, D. Sarkar, Y. Khatami, J. Kang, and K. Banerjee, "Subthreshold-swing physics of tunnel field-effect transistors," *AIP Advances*, vol. 4, no. 6, pp. –, 2014.

[31] S. H. Wolff, S. Wagner, J. C. Bean, R. Hull, and J. M. Gibson, "Hydrogen surface coverage: Raising the silicon epitaxial growth temperature," *Applied Physics Letters*, vol. 55, no. 19, pp. 2017–2019, 1989.

[32] B. S. Meyerson, K. J. Uram, and F. K. LeGoues, "Cooperative growth phenomena in silicon germanium low temperature epitaxy," *Appl. Phys. Lett.*, vol. 53, pp. 2555–2557, 1988.

[33] J. F. Gibbons, C. M. Gronet, and K. E. Williams, "Limited reaction processing: Silicon epitaxy," *Applied Physics Letters*, vol. 47, no. 7, pp. 721–723, 1985.

[34] D. Crippa, D. L. Rode, and M. Masi, *Silicon Epitaxy*. Academic Press, 2001.

[35] A. M. Beers and J. Bloem, "Temperature dependence of the growth rate of silicon prepared through chemical vapor deposition from silane," *Applied Physics Letters*, vol. 41, no. 2, pp. 153–155, 1982.

[36] T. Adam, S. Bedell, A. Reznicek, D. Sadana, A. Venkateshan, T. Tsunoda, T. Seino, J. Nakatsuru, and S. Shinde, "Low-Temperature growth of epitaxial (100) silicon based on silane and disilane in a 300 mm UHV/CVD cold-wall reactor," *J. Crystal Growth*, vol. 312, pp. 3473–3478, 2010.

[37] D. Lubben, R. Tsu, T. R. Bramblett, and J. Greene, "Mechanisms and kinetics of si atomic layer epitaxy on si(001)2x1 from si2h6," *Journal of Vacuum Science and Technology A*, vol. 9, no. 6, pp. 3003–3011, 1991.

[38] Y. Suda, D. Lubben, T. Maotooka, and J. Greene, "Adsorption and thermal dissociation of disilane (si2h6) on si(100) 2x1," *Journal of Vacuum Science and Technology A*, vol. 8, no. 1, pp. 61–67, 1990.

[39] J. J. Boland, "Role of hydrogen desorption in the chemical-vapor deposition of si(100) epitaxial films using disilane," *Phys. Rev. B*, vol. 44, pp. 1383–1386, Jul 1991.

[40] F. Bozso and P. Avouris, "Thermal and electron-beam-induced reaction of disilane on si(100)-(2x1)," *Phys. Rev. B*, vol. 38, pp. 3943–3947, Aug 1988.

[41] S. M. Gates, C. M. Greenlief, and D. B. Beach, "Decomposition of silane on si(111)-(7x7) and si(100)-(2x1) surfaces below 500c," *Journal of Chem. Phys.*, vol. 93, p. 7493, 1990.

[42] D. Q. Kelly, *Metal-Oxide-Semiconductor Devices Based on Epitaxial Germanium-Carbon Layers Grown Directly on Silicon Substrates by Ultra-High-Vacuum Chemical Vapor Deposition*. PhD thesis, The University of Texas at Austin, 2006.

[43] B. Cunningham, J. O. Chu, and S. Akbar, "Heteroepitaxial growth of ge on (100) si by ultrahigh vacuum, chemical vapor deposition," *Applied Physics Letters*, vol. 59, no. 27, pp. 3574–3576, 1991.

[44] M. Halbwax, V. Yam, C. Clerc, Y. Zheng, D. Debarre, H. Nguyena, and D. Bouchier, "Kinetics of the heteroepitaxial growth of ge layer at low temperature on si(001) in uhv-cvd," *Phys. Stat.Sol.*, vol. 201, no. 2, p. 329, 2004.

[45] J. Kolodzey, P. ONeil, S. Zhang, and S. Shah, "Growth of germanium carbon alloys on silicon substrates by molecular beam epitaxy," *Applied Physics Letters*, vol. 67, pp. 1865–1867, 1995.

[46] J. Kouvetakis, D. Nesting, and D. Smith, "Synthesis and Atomic and Electronic Structure of New Si-Ge-C Alloys and Compounds," *Chemistry of Materials*, vol. 10, p. 2935, 1998.

[47] R. I. Scace and G. A. Slack, "Solubility of carbon in silicon and germanium," *The Journal of Chemical Physics*, vol. 30, no. 6, pp. 1551–1555, 1959.

[48] J.-M. Chauveau, Y. Androussi, A. Lefebvre, J. Di Persio, and Y. Cordier, "Indium content measurements in metamorphic high electron mobility transistor structures by combination of x-ray reciprocal space mapping and transmission electron microscopy," *Journal of Applied Physics*, vol. 93, no. 7, pp. 4219–4225, 2003.

[49] E. Koppensteiner, G. Bauer, H. Kibbel, and E. Kasper, "Investigation of strain-symmetrized and pseudomorphic si(m)ge(n) superlattices by x-ray reciprocal space mapping," *Journal of Applied Physics*, vol. 76, no. 6, pp. 3489–3501, 1994.

[50] R. Malik, E. Gulari, S. H. Li, and P. K. Bhattacharya, "Modeling growth of si(1-x)ge(x) epitaxial films from disilane and germane," *Journal of Applied Physics*, vol. 73, no. 10, pp. 5193–5196, 1993.

[51] B. M. H. Ning and J. E. Crowell, "Investigation on the growth rate enhancement by ge during sige alloy deposition by chemical vapor deposition," *Applied Physics Letters*, vol. 60, no. 23, pp. 2914–2916, 1992.

[52] L. T. Vinh, V. Aubry-Fortuna, Y. Zheng, D. Bouchier, C. Guedj, and G. Hincelin, "Uhv-cvd heteroepitaxial growth of si(1-x)ge(x) alloys on si(100) using silane and germane," *Thin Solid Films*, vol. 294, pp. 59 – 63, 1997.

[53] A. Y. Hikavyy, E. Rosseel, S. K. Dhayalan, L. Witters, H. Mertens, H. Bender, P. Favia, and R. Loo, "(invited) high ge content sige thin films: Growth, properties and integration," *Meeting Abstracts*, vol. MA2014-02, no. 35, p. 1847, 2014.

[54] H. Chen, Y. K. Li, C. S. Peng, H. F. Liu, Y. L. Liu, Q. Huang, J. M. Zhou, and Q.-K. Xue, "Crosshatching on a sige film grown on a si(001) substrate studied by raman mapping and atomic force microscopy," *Phys. Rev. B*, vol. 65, p. 233303, May 2002.

[55] E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, "Device physics and guiding principles for the design of double-gate tunneling field effect transistor with silicon-germanium source heterojunction," *Applied Physics Letters*, vol. 91, no. 24, pp. –, 2007.

[56] G. Zhou, Y. Lu, R. Li, Q. Zhang, W. Sik Hwang, Q. Liu, T. Vasen, C. Chen, H. Zhu, J. ming Kuo, S. Koswatta, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "Vertical ingaas/inp tunnel fets with tunneling normal to the gate," *Electron Device Letters, IEEE*, vol. 32, pp. 1516–1518, Nov 2011.

[57] J. Nah, E.-S. Liu, K. Varahramyan, and E. Tutuc, "Ge-si core-shell nanowire tunneling field-effect transistors," *Electron Devices, IEEE Transactions on*, vol. 57, pp. 1883–1888, Aug 2010.

[58] G. Zhou, Y. Lu, R. Li, Q. Zhang, W. Sik Hwang, Q. Liu, T. Vasen, C. Chen, H. Zhu, J. ming Kuo, S. Koswatta, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "Vertical ingaas/inp tunnel fets with tunneling normal to the gate," *Electron Device Letters, IEEE*, vol. 32, pp. 1516–1518, Nov 2011.

[59] W. G. Vandenberge, A. S. Verhulst, and M. V. Fischetti, "Figure of merit for and identification of sub-60 mv/decade devices," *Applied Physics Letters*, vol. 102, 2013.

[60] T. Nirschl, S. Henzler, J. Fischer, M. Fulde, A. Bargagli-Stoffi, M. Sterkel, J. Sedlmeir, C. Weber, R. Heinrich, U. Schaper, J. Einfeld, R. Neubert, U. Feldmann, K. Stahrenberg, E. Ruderer, G. Georgakos, A. Huber, R. Kakoschke, W. Hansch, and D. Schmitt-Landsiedel, "Scaling properties of the tunneling field effect transistor (tfet): Device and circuit," *Solid-State Electronics*, vol. 50, no. 1, pp. 44 – 51, 2006. Special Issue: Papers selected from the 2005 {ULIS} Conference.

[61] Y. Lu, G. Zhou, R. Li, Q. Liu, Q. Zhang, T. Vasen, S. Doo Chae, T. Kosel, M. Wistey, H. Xing, A. Seabaugh, and P. Fay, "Performance of algasb/inas tfets with gate electric field and tunneling direction aligned," *Electron Device Letters, IEEE*, vol. 33, pp. 655–657, May 2012.

[62] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *Electron Device Letters, IEEE*, vol. 27, pp. 297–300, April 2006.

[63] J. T. Teherani, W. Chern, D. A. Antoniadis, J. L. Hoyt, L. Ruiz, C. D. Poweleit, and J. Menéndez, "Extraction of large valence-band energy offsets and comparison to

theoretical values for strained-si/strained-ge type-ii heterostructures on relaxed sige substrates," *Phys. Rev. B*, vol. 85, p. 205308, May 2012.

[64] M. Kobayashi, J. Mitard, T. Irisawa, T. Hoffmann, M. Meuris, K. Saraswat, Y. Nishi, and M. Heyns, "On the high-field transport and uniaxial stress effect in ge pfets," *Electron Devices, IEEE Transactions on*, vol. 58, pp. 384–391, Feb 2011.

[65] R. Xie, T. Phung, M. Yu, and C. Zhu, "Interface-Engineered High-Mobility High-k/Ge pMOSFETs with 1-nm Equivalent Oxide Thickness," *IEEE Trans. Electron Devices*, vol. 56, pp. 1330–1337, 2009.

[66] M. Bollani, S. Signoretti, C. Beeli, G. Isella, M. Kummer, and H. Kanel, "Compressively Strained Ge channels on Relaxed SiGe Buffer Layers," *Mater. Sci. Engg. B*, vol. 101, pp. 102–105, 2003.

[67] R. Pillarisetty, "High mobility strained p-channel germanium quantum well field effect transistor for low power (Vcc=0.5V) III-V CMOS applications," in *Device Research Conference*, pp. 231–232, 2011.

[68] A. Dobbie, M. Myronov, R. Morris, and A. Hassan, "Ultra-high hole mobility exceeding one million in a strained germanium quantum well," *Applied Physics Letters*, vol. 101, pp. 172108–172112, 2012.

[69] Y. Suh, M. Carroll, R. Levy, and G. Bisognin, "Implantation and Activation of high concentrations of boron in Germanium," *IEEE Trans. Electron Devices*, vol. 52, pp. 2416–2421, 2005.

[70] L. Horng-Chih, J. Tze-Guei, L. Hsiao-Yi, and L. Tan-Fu, "Deposition and device applications of in situ boron-doped polycrystalline SiGe films grown at low temperature," *J. Applied Physics*, vol. 74, no. 9, pp. 5395–5401, 1993.

[71] A. Dimoulas, P. Tsipas, and A. Sotiropoulos, "Fermi-level pinning and charge neutrality level in germanium," *Applied Physics Letters*, vol. 89, p. 252110, 2006.

[72] C. O. Chui, L. Kulig, J. Moran, W. Tsai, and K. C. Saraswat, "Germanium n-type shallow junction activation dependences," *Appl. Phys. Lett.*, vol. 87, p. 091909, 2005.

[73] J. Van Der Heide, *Cost-efficient thermophotovoltaic cells based on germanium*. PhD thesis, University of Leuven, Belgium, 2009.

[74] S. Koffela, P. Scheiblina, A. Claverieb, and V. Mazzocchia, "Doping of germanium by phosphorus implantation: Prediction of diffused profiles with simulation," *Mat. Sci. Engg. B.*, vol. 154-155, pp. 60–63, 2008.

[75] S. M. Sze and K. N. Kwok, *Physics of Semiconductor Devices*. Wiley Interscience, 2007.

[76] C. O. Chui, K. Gopalakrishnan, P. B. Griffin, J. D. Plummer, and K. C. Saraswat, "Activation and diffusion studies of ion-implanted p and n dopants in germanium," *Appl. Phys. Lett.*, vol. 83, pp. 3275–3277, 2003.

[77] J. Kim, S. W. Bedell, S. L. Maurer, and R. Loesing, "Activation of implanted n-type dopants in Ge over the active concentration of 1E20 cm-3 using coimplantation of Sb and P," *Electrochem. and Solid-State Lett.*, vol. 13, pp. H12–H15, 2005.

[78] G. Thareja, J. Liang, and Y. Nishi, "High performance germanium n-MOSFET with antimony and dopant activation beyond 1E20 cm-3," in *IEDM Tech. Dig.*, pp. 245–248, 2010.

[79] M. Jamil, J. Oh, M. Ramon, S. Kaur, P. Majhi, E. Tutuc, and S. K. Banerjee, "High-Mobility TaN/Al2O3/Ge(111) n-MOSFETs With RTO-Grown Passivation Layer," *IEEE Elect. Dev. Lett.*, vol. 31, pp. 1208–1210, 2010.

[80] G. Niu, J. Cressler, S. Mathew, and S. Subbana, "A total resistance slope-based effective channel mobility extraction method for deep sub-micrometer CMOS technlogy," *IEEE Trans. Electron Devices*, vol. 46, no. 9, pp. 1912–1914, 1999.

[81] C. Dupre, T. Ernst, J. Hartmann, F. Andrieu, J. Barnes, P. Rivallin, O. Faynot, S. Deleonibus, P. Fazzini, A. Claverie, S. Cristoloveanu, G. Ghibaudo, and F. Cristiano, "Carrier mobility degradation due to high dose implantation in ultrathin unstrained and strained silicon-on-insulator films," *Journal of Applied Physics*, vol. 102, no. 10, p. 104505, 2007.

[82] X. R. Qin, B. S. Swartzentruber, and M. G. Lagally, "Scanning tunneling microscopy identification of atomic-scale intermixing on si(100) at submonolayer ge coverages," *Phys. Rev. Lett.*, vol. 84, pp. 4645–4648, May 2000.

[83] H. RÃŒcker and B. Heinemann, "Tailoring dopant diffusion for advanced sige:c heterojunction bipolar transistors," *Solid-State Electronics*, vol. 44, no. 5, pp. 783 – 789, 2000.

[84] Y. Tan and C. Tan, "Growth and characterization of germanium epitaxial film on silicon (001) using reduced pressure chemical vapor deposition," *Thin Solid Films*, vol. 520, no. 7, pp. 2711 – 2716, 2012.

[85] H.-Y. Yu, M. Ishibashi, J.-H. Park, M. Kobayashi, and K. Saraswat, "p-channel ge mosfet by selectively heteroepitaxially grown ge on si," *Electron Device Letters, IEEE*, vol. 30, pp. 675–677, June 2009.

[86] G. Snider, "1-d poisson solver." http://www3.nd.edu/~gsnider/. [Online; accessed 01-Aug-2015].

[87] K. Lee and X. Pan, "Formation and morphology evolution of nickel germanides on ge (100) under rapid thermal annealing," in *Symposium C - Silicon Front-End Junction Formation Physics and Technology*, 2004.

[88] F. Laermer and A. Schilp, "Method of anisotropically etching silicon." http://www.freepatentsonline.com/5501893.html. [Patent number 5501893, March 1996].

[89] Y. Zhai, *Novel 3-D IC Technology*. PhD thesis, University of Texas at Austin, 2013.

[90] J. H. Nam, T. Fuse, Y. Nishi, and K. C. Saraswat, "Germanium on insulator (goi) structure using hetero-epitaxial lateral overgrowth on silicon," *ECS Transactions*, vol. 45, no. 4, pp. 203–208, 2012.