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Nanostructuring Approaches to Altering and Enhancing Performance Characteristics of Thin-Film Transistors

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Nanostructuring Approaches to Altering and Enhancing Performance Characteristics of Thin-Film Transistors

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Abstract

Nanostructuring Approaches to Altering and Enhancing Performance Characteristics of Thin-Film Transistors

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Nanostructured thin-film transistor (TFT) designs and approaches in this work have been shown to enhance transistor characteristics across many semiconductor materials. We highlight two nanostructuring approaches, including nanostripe patterning of the transistor channel and nanospike patterning of the source and drain electrodes. Both nanostructuring techniques are shown to alter and improve transistor performance by (i) enhancing gate control which improves subthreshold characteristics, (ii) enhancing electric fields and carrier concentrations near the source contact to improve carrier injection, and (iii) redistributing the carrier concentrations within the channel resulting in enhanced concentrations in narrow channels designated as charge nanoribbons.

Nanostripe-patterning of semiconductor channels was studied with technology computer-assisted design (TCAD) software and shown to enhance transistor drive currents over unpatterned channels by greater than a factor of 11 and showed that the nanostripe patterning of the semiconductor channel resulted in reduced short channel effects and significantly improved gate control. The advantages of nanostripe channel patterning were

also demonstrated experimentally and showed enhancement of carrier mobility by a factor of 2.

Nanospike-patterning of the metal source and drain electrode TFTs were also explored and shown, through experimental studies and simulation studies, to substantially improve the performance of TFTs, especially at short channel lengths and also below threshold. Inspired by field emission contacts and our nanostripe work, the sharp tip of the nanospike electrodes focus electric fields and produces field-emission enhanced carrier injection from the nanospike source and drain contacts, leading to higher drive currents, carrier densities, and carrier velocities. Nanospike electrodes also facilitate quasi-three-dimensional gate control, especially at low gate voltage conditions. This leads to significantly improved subthreshold characteristics and reduced subthreshold dependence on drain voltage, especially at short channel lengths. While nanospike electrode TFTs do not have physically patterned semiconductor regions as nanostripe TFTs, nanospike electrode TFTs also form charge nanoribbons at high drain voltages which similarly facilitates superior gate control over the full channel.

Both nanostripe semiconductor TFTs and nanospike electrode TFTs are promising approaches that are compatible with many thin-film semiconductor materials, fabrication methods, and design strategies. These nanostructuring strategies can improve processing speed and performance while reducing power consumption when applied to flexible electronic systems or in back-end-of-the-line circuits.

Table of Contents

List of Tables

List of Figures

BACKGROUND

In this dissertation, we present new transistor designs and strategies that can greatly improve the performance of thin-film transistors (TFTs). We will first provide a brief overview of key topics that are important to TFTs. However, each major section will provide an introduction and background information as needed. This Background section can be treated as a preface.

Chapter 1: Introduction to Thin Film Transistors

Thin film transistors (TFTs) are transistors that feature thin-film semiconductors rather than the current industry standard of transistors fabricated from crystalline silicon wafers. Unlike traditional silicon transistors that operate in inversion mode, TFTs typically operate in accumulation mode, where the doping of the semiconductor is the majority carrier for the transistor. There are many options of semiconductor material families that can make TFTs, which will be discussed in a later section. TFTs are desirable not only for their potential to realize flexible and transparent electronics, but also for their potential for large-area, high throughput manufacturing and their potential for their versatility in applications and customization. In this chapter, we will discuss the TFT applications that are already commercially implemented, how device fabrication scales up, and where the technology needs to advance to next.

TFTs in Commercial Products

TFTs are already found in many display products on the commercial market today, primarily as active-matrix pixel drivers. Liquid crystal displays (LCDs) initially began

using TFT active-matrix pixel drivers in the 1990s and were typically made using amorphous silicon (a-Si) or less commonly polycrystalline silicon (poly-Si). More recently, display technology shifted to focus on active-matrix organic light emitting diodes (AMOLEDs) displays which outperform LCDs with lower power consumption, higher display contrast, faster display response times. AMOLED displays feature TFTs made from a combination of both a-Si and poly-Si, though some commercial AMOLED displays have also used organic TFTs or amorphous metal oxide TFTs. For display applications, TFTs need to operate at dozens of Hz for the human eye to not notice image flicker. High resolution displays for electronics have pixel densities as high as 458 PPI and continually increase each year. Even with a high resolution of 458 PPI, a pixel takes approximately 60 μm with both switching and driving TFTs sized on the order of a few microns. And one of the most recent developments in display technology is the flexible display, which features flexible LEDs along with a flexible diving and switching TFTs.

In comparison to specifications for TFTs for display applications, specification for TFTs for processing applications demand higher frequencies of operation and ideally higher device density. Commercial production of flexible TFT processors would seem like a natural next step, since TFTs have been in commercial production for decades for displays and the infrastructure for manufacturing them on a large scale is available and accessible. However, TFT performance has not attained the specifications needed to build processors for electronic systems yet.

SCALING-UP TFTS AND MANUFACTURING STRATEGIES

Since the fabrication of TFTs not limited to methods compatible with rigid silicon substrate, TFTs can be manufactured with a wide array of solution-based and low temperature techniques that are both compatible with large area processing and compatible

with the lower thermal budget of flexible substrates. Unlike traditional silicon manufacturing, TFT manufacturing can be understood as a more additive manufacturing process where the TFT is built on top of a substrate, rather than a transformative process like silicon processing where the silicon substrate is also the primary semiconductor that is then processed on to become the transistor. Here we will briefly discuss processes used for depositing material for and patterning TFTs.

For the patterning of TFT layers, we will discuss both resist patterning techniques and direct material patterning techniques. Commercial TFTs still use photolithography for resist patterning of layers, where patterns are transferred using optical masks and photoreactive polymer solutions, just like traditional silicon process patterning. In addition to photolithography, the pattern TFT layers have been made with additive processes such as inkjet printing, screen printing, and other large-area, solution-based patterning methods compatible with flexible substrates. These methods can not only deposit patterned resist layers for patterning TFTs, these solution-based methods can also directly print active TFT materials (such as the semiconductor, the insulator, and even metals).

One method for large scale and high throughput solution processing is nanoimprint lithography, which uses a hard, physical mask with the desired pattern etched in, to imprint solution-based materials onto various substrates, including both flexible and rigid substrates. Nanoimprint lithography also requires a curing or annealing step for the printed resist or material. And for most implementations, nanoimprint lithography benefits from a descum step which removes residual and unwanted material outside of the patterned area. Work on these nanoimprint tools have shown successful and consistent printing of line resolutions down to 20 nm or smaller on flexible substrates, and below 10 nm for rigid substrates. These methods are discussed further in later sections as is applicable to the corresponding TFT device design of the section.

Chapter 2: Introduction to Disordered Semiconductors

One class of semiconductor materials commonly used in TFTs is disordered semiconductors, where "disordered" refers to the lack of long-range crystalline structure in these semiconductors. Disordered semiconductors include semiconductors that have structures that range from polycrystalline to completely amorphous. Materials with high crystallinity are brittle and very easily fracture along the lines of crystalline symmetry. This is especially true with thick crystalline materials. When crystalline materials are thin enough, they can become more resilient to flexing. But these thin crystalline materials are usually difficult to make or fabricate on. Disordered semiconductors do not have long range order or brittle symmetries are more resilient to mechanical flexing which retaining semiconducting electronic behavior. But for the same reason they can be mechanically flexible, the disorder of the material introduces trap states within the bandgap of the semiconductor, which presents challenges to electronic transport and transistor performance. In this chapter, we will be providing a background of disordered semiconductor physics as well as discuss common challenges disordered semiconductor TFTs face.

DEVICE PHYSICS OF DISORDERED SEMICONDUCTORS: TRAP-DOMINATED TRANSPORT

In high-mobility polymers as well as in amorphous metal oxides, the multiple trap and release (MTR) model for change transport has been shown to work well [1]–[3]. The essential physics of MTR type transport of charge in this polymer is modeled as a linearly carrier concentration dependent mobility system. Similar models have been described in previous publications [4], [5]. The linear carrier concentration dependent mobility relationship can be derived from the multiple trap and release transport model for mobilities [6], [7], which is exponentially dependent on temperature, T,

$$\mu_p = \mu_o \cdot \alpha \cdot e^{-(E_t - E_v)/kT}\,, \tag{1}$$

where μ_p is the hole mobility, μ_o is the mobility in the transport band, α is a constant depending on the ratio of carriers in the band and total carriers, E_t is the trap state energy level, and E_v is the valence band energy level. Given that mobility is scaled by the ratio of free carrier density to total carrier density, the effective mobility can also be expressed as follows:

$$\mu_p = \mu_o \cdot \left(\frac{p_v}{p_t + p_v}\right), \tag{2}$$

where p_v is the density of free holes experiencing band transport in the valence band and p_t is the density of trapped carriers. Note that we assume that $p_t + p_v$ is approximately the total carrier density, p. For polymer material systems which have activation energies much higher than kT, we can use the Boltzmann approximation to estimate the free hole ($p_v = N_v \cdot e^{-(E_f - E_v)/kT}$) and trapped carrier densities ($p_t = N_t \cdot e^{-(E_f - E_t)/kT}$). This means that this model is no longer accurate when the device operation pushes the Fermi level close to or into the valence band, where the mobility is expected to saturate. Using the Boltzmann expressions and combining with Eqs. 1 and 2, we can approximate that

$$\mu_p = \mu_o \cdot \left(\frac{1}{1 + \frac{N_t(E)}{N_v} \cdot e^{-(E_t - E_v)/kT}}\right) \cong \mu_o \cdot \frac{N_t(E)}{N_v} \cdot e^{-(E_t - E_v)/kT}, \tag{3}$$

where E_f is the Fermi level, N_v is the valence band density of states and $N_t(E)$ is trap density of states as a function of energy. Assuming a large number of trapped carriers (when $p \approx p_t$) and an exponential band tail distribution, we can approximate p with a Fermi-Dirac occupation probability, which can now be written as

$$p = \int_{E_f}^{\infty} \frac{N_{t0}}{kT_0} \cdot e^{-\frac{E - E_v}{kT_0}} \cdot f(E) \cdot dE\,, \tag{4}$$

where N_{t0} is the total density of trap states, T_0 is the characteristic width of the density distribution, $f(E)$ and is the Fermi-Dirac function. Under lower temperature

operating conditions, $f(E)$ can be approximated as a step function and the evaluation of the definite integral results in

$$p = N_{t0} \cdot e^{-(E_f - E_v)/kT_0} \ . \tag{5}$$

Rearranging the expression after integration will give

$$\left(E_f - E_v\right) = kT_0 \cdot ln(\frac{p}{N_{t0}}) \ . \tag{6}$$

Given Eq. 6, we can rewrite the Boltzmann expression for p_v as

$$p_v = N_v \cdot e^{-\left(\frac{T_0}{T}\right) ln(\frac{p}{N_{t0}})} \ . \tag{7}$$

Eq. 2 can now be written as

$$\mu_p = \mu_0 \cdot \frac{N_v}{N_{t0}} \cdot (\frac{p}{N_{t0}})^{(\frac{T_0}{T} - 1)}. \tag{8}$$

where typical T_0 values for TFT materials approach 600 K [4], confirming the observed behavior where hole mobilities display approximately linear carrier concentration dependence.

We then simplify the unipolar carrier concentration dependent hole mobility model is of the form $\mu_p(p) = \mu_{min} + \mu_o\ (N_V/N_{to}^2) \times p$, where μ_p is the hole mobility, μ_{min} is the minimum hole mobility, μ_o is the band transport hole mobility, N_V is the valence band density of states, N_{to} is the total trap density, and $p(r)$ is the hole concentration as a function of the spatial coordinate. It is also important to note that the process of fabricating stripes could introduce trap states at the sidewall edges. These edge trap states are not included in the simulation. However, given substantial carrier density enhancement, these trap states can be quickly filled and nanostripe devices retain their advantage over unpatterned films. This linear carrier concentration dependence of carrier mobility is commonly seen in many classes of TFT semiconductor materials, and the TFT designs presented in this dissertation capitalize this property to enhance the transistor performance.

COMMON SEMICONDUCTORS FOR TFTS

A few of the most desirable material properties for semiconductors to be used in TFTs include mechanical flexibility and optical transparency, low temperature processing, and good carrier transport. These requirements preclude bulk crystalline materials, as they are mechanically rigid and brittle and typically require high temperature processing. Semiconductors that meet these basic material specifications for TFTs can be divided up into two major material categories: non-crystalline, disordered semiconductors or thin crystalline semiconductors. In this dissertation, we focus on presenting solutions for non-crystalline and disordered semiconductors, though we believe our innovative TFT designs should also benefit thin-crystalline semiconductors, such as transition metal dichalcogenides, graphene-based semiconductors, and thin-silicon. Non-crystalline and disordered semiconductors are semiconductors with no long-range crystalline molecular order. Within disordered semiconductors, there are various levels of disorder. Amorphous semiconductors have no long-range or short-range crystalline order. Examples of such materials include amorphous metal oxides (AMO) and amorphous silicon (a-Si). Poly-crystalline semiconductors are materials with short-range crystalline order, but no long-range crystalline order. These include many polymers and organic small molecule semiconductors as well as polycrystalline silicon (poly-Si). Poly-crystalline materials can be even more finely classified by specifying the size of the crystalline regions, such as micro-crystalline for materials with micrometer-sized crystal grains, or nano-crystalline for materials with nanometer-sized crystal grains.

This dissertation will describe multiple device architectures and demonstrate the advantages of these architectures using multiple disordered semiconductor materials. For each section and topic, important material properties will be provided within the section for clarity. Key materials used for this work include amorphous metal oxides such as zinc

tin oxide (ZTO) and indium gallium zinc oxide (IGZO), polymers such as diketopyrrolopyrrole-naphthalene (PDPP-TNT), and small organic molecules such as pentacene.

NANOSTRIPE THIN-FILM TRANSISTORS[1]

Abstract: We analyze the operation of thin-film transistor (TFT) devices where the active semiconductor is patterned into nanostripes. It is shown that using relatively large separations between stripes can improve current drive capability by more than a factor of 13 for many of the important material families of disordered and solution-processable TFTs. When comparing nanostripe TFTs to unpatterned TFTs under the same operating conditions, nanostripe devices show enhancements in peak carrier density and conductivity along the edges of the stripe. In addition to increasing the drive current, these carrier density enhancements are large enough to potentially lower the contact resistance. Short channel effects are also greatly reduced, allowing the possibility of scaling down channel lengths for improved operation at high frequencies. This architecture will work especially well for TFT materials in which the mobility increases with carrier density, a common feature in many organic, polymer, and amorphous metal oxide semiconductors. The results of our analysis on nanostripe TFTs not only makes TFTs considerably more attractive for existing optoelectronic applications, but nanostripe patterning may also provide TFTs an opportunity to expand into new higher-frequency and higher-performance applications.

Chapter 1: Introduction to Thin-Film Transistor Channel Patterning

In recent years, there have been an increasing number of reports on thin-film transistors (TFTs) where the active semiconductor layer has been patterned or textured into stripes. In some cases, the TFTs are composed of disconnected stripes that are micron-sized

[1] K. Liang *et al.*, "Nanospike electrodes and charge nanoribbons: A new design for nanoscale thin-film transistors," *Sci. Adv.*, vol. 8, no. 4, Jan. 2022, doi: 10.1126/SCIADV.ABM1154.

[8], while in others, the individual stripes are of sub-micron or smaller widths [9]. In other cases, the TFTs are composed of patterned stripes which form nanogrooves on the dielectric surface [10], [11], randomly striated surfaces [12]–[14], or FinFET like structures [15], [16]. A variety of semiconductor materials have been used in these reports including poly-Si [16], polymers [9], [11], [13], organics [10], and amorphous metal oxide [8], [15]. In each of these cases, patterning and texturing of the devices improve the performance, which have been attributed to a wide variety of morphological, electrostatic, and device physics factors. While these effects have been explored experimentally, there has yet to be a detailed study on the device physics and design optimization of such TFTs. It is the aim of this section to describe these advantages. With the aid of simulations based on experimental data, we demonstrate the many advantages and characteristics of nanostripe TFTs and describe how these advantages scale with stripe dimensions, channel length, and other device parameters.

Nanostripe pattering is the most advantageous when the semiconductor is disordered and has a mobility that increases with carrier density. This is the case in many polymer/organic, amorphous metal oxide, and other disordered semiconductor TFTs [2], [17], [18], and these materials will be the focus of our discussion. We show that the use of a set of parallel semiconducting stripes helps focus the gate electric field on the edges of the stripes, vastly improving the transport properties along the edges, which greatly improves the overall performance of the TFT. Even with the loss in cross-sectional area of the device, the improvements in carrier mobility along the edges are sufficiently large that the total current flowing between source and drain is greater than in planar unpatterned devices, even when the stripes are loosely spaced. This enhancement in on-current is an advantage of nanostripe patterning unique to semiconductor materials whose mobility increases with carrier density. In addition to the improvements in on-currents, the sub-

threshold characteristics and gate control are improved, and this improvement is seen for most materials regardless of mobility dependence. The improved gate control leads to lower off-currents and reduced short-channel characteristics. We present a case for reduced contact resistance in such devices, which in conjunction with improved gate control and sub-threshold response will be beneficial for small channel length TFTs and faster switching TFTs. Thus, this device architecture may offer a way to improve TFT frequency response which has thus far been curtailed by high contact resistance in most TFTs [19]. Fabrication of such devices has been expectedly more complicated. In recent years, the advent of scalable nanomanufacturing methods such as nanoimprint lithography [10], [15], [16], [20] will enable the relatively facile fabrication/manufacture of such devices with high throughput and process control [21]–[23].

DEVICE PHYSICS—CARRIER MOBILITY AND CARRIER CONCENTRATION.

Several semiconductors used in TFTs are amorphous or polycrystalline. The disorder in these semiconductors introduces trap states—or states that are in the forbidden gap, which generally reduce carrier mobility and complicate charge transport. Electronic transport in the presence of these traps is often described by variable range hopping (VRH), multiple trap-and-release (MTR), or a combination of both models. Both methods of transport heavily depend on the electronic carrier density where the higher the carrier density in the disordered material, the greater the mobility of the carrier at that location. At room temperature, both models of trap-dominated transport reduce to an approximately linear dependence of carrier mobility on carrier concentration. In this section, we focus on modeling with MTR transport, since our semiconductor, diketopyrrolopyrrole-naphthalene (PDPP-TNT), is a high mobility polymer known to be MTR-dominant. This linear relationship between mobility and carrier concentration for MTR systems at room

temperature is reported in many papers [1]–[3], and it is one of the unique properties of disordered materials which makes nanostripes uniquely advantageous for TFT design. **Fig. 1** shows the mobility as a function of gate voltage for a polymer TFT [2] and also an amorphous metal oxide TFT [3] reported previously by our group. The derivation of the linear dependance of mobility on carrier concentration is shown in the Appendix of this section, along with additional information about VRH and MTR. We also note that in some TFTs, the mobility increases sub-linearly with carrier density [24]; in such systems many of the advantages we discuss in the following sections still apply qualitatively.

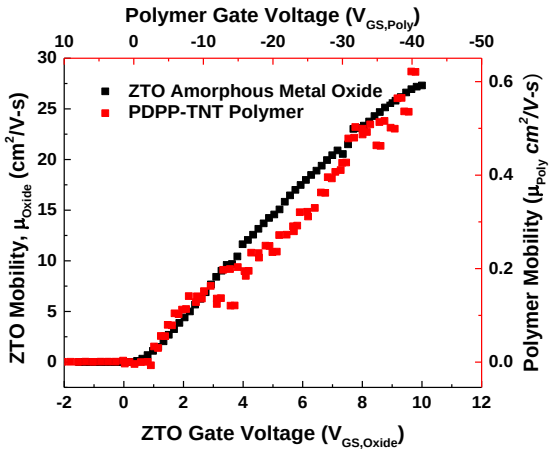

Fig. 1 *Gate voltage dependence of mobility in two disordered semiconductor TFTs at room temperature. The mobility increases approximately linearly with increasing gate voltage. This data has been previously reported for a polymer TFT [10] and an amorphous metal oxide TFT [11].*

Chapter 2: Nanostripe TFTs

We present a new methodology for designing TFTs which is centered on optimizing nanostripe geometries to improve transistor performance. There are three main origins of nanostripe enhancement—first is improved morphological order of the disordered materials especially polymers, as previously reported by several groups [9], [12], [13];

second is greatly enhanced induced carrier densities along the edges of the stripe which, as mentioned in the previous section, and is especially advantageous for disordered semiconductors; third is improved gate control, similar to FinFET schemes seen in silicon and other semiconductor transistors. With the combined effects of all three, nanostripe devices can expect substantially improved drive currents and gate control over their unpatterned thin-film counterparts. This chapter will focus on the latter two sources of nanostripe enhancement since they are more broadly applied to all disordered semiconductor systems. The nanostripe geometry is suited for optimizing the densities of carriers induced by the gate, especially when compared to unpatterned devices of the same dimension and operating condition. Our proposed approach of designing the nanostripe devices consists of reducing semiconductor stripe widths to the nanometer-scale, where stripes spaced far from each other and filled with either air or low permittivity dielectric, as illustrated in **Fig. 2**. This geometry allows the electric field from the gate to focus on the stripe, thereby inducing a much higher carrier concentration along the edges of the stripes. While the device performance improvements are already significant, we also show that it is possible to overcome the micron short channel bottleneck. By first scaling down the channel width of TFT devices into arrays of nanostripes, we have found a means of scaling down the channel length while retaining transistor performance.

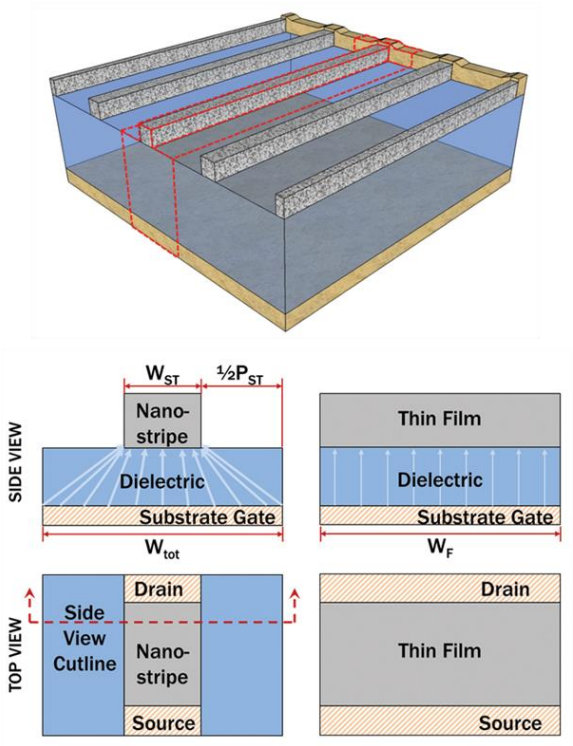

Fig. 2 *Geometry and electric fields of nanostripe TFTs. (a) The nanostripe architecture features narrow semiconductor stripes atop a gate dielectric with air or a low permittivity dielectric between each stripe. A nanostripe TFT device features multiple strips with a common gate and common source and drain contacts. (b) Key device geometry parameters include nanostripe widths, W_{ST}, and nanostripe pitches, P_{ST}, defined as shown. The pitch-to-width ratios, R_{PW}, is defined as P_{ST}/W_{ST}.*

NANOSTRIPE TCAD SIMULATION

To quantify the potential advantages of designing TFTs with nanostripes, we extensively studied the nanostripe design space by developing a TCAD model using Silvaco ATLAS™ to simulate polymer TFTs. In addition to drift-diffusion, current continuity, and Poisson's equations, an additional transport model is required to capture the physics of trap states for the high-mobility and p-type, diketopyrrolopyrrole-naphthalene (PDPP-TNT) co-polymer [25]. This solution-deposited polymer film, like most disordered films used in TFTs, shows a mobility that is linearly dependent on the

carrier concentration [1], [3]. The unipolar carrier concentration dependent hole mobility model is of the form $\mu_p(p) = \mu_{min} + \mu_o (N_V/N_{to}^2) \times p(r)$, where μ_p is the hole mobility, μ_{min} is the minimum hole mobility, μ_o is the band transport hole mobility, N_V is the valence band density of states, N_{to} is the total trap density, and $p(r)$ is the hole concentration as a function of the spatial coordinate. This mobility model is derived from standard multiple trap-and-release (MTR) models and is shown in the Appendix of this section. These simulated TFT devices also show very high carrier densities; therefore, the model must use Fermi-Dirac carrier statistics. **Table I** shows the complete list of simulation parameters used for all devices in this chapter. This means that we use the same material model even when comparing the nanostripe patterned devices to the unpatterned devices, though previous publications have shown that patterning polymers into stripes greatly improves crystallinity and thus transport properties [9], [12], [13]. Therefore, this simulation underestimates the relative advantage of nanostripes over unpatterned thin films regarding to the semiconductor material transport property improvements. Even without adjusting the material properties to reflect improved crystallinity, the benefits from the electric field coupling with increased gate area and the resulting increase in induced charge are apparent. The important device design parameters are depicted in **Fig. 2b**. Pitch here is defined as the distance between stripes, rather than the pitch being defined as the full period of a pattern as is done so as convention in many optical devices. The simulation confirms the intuition that under the same electrical biasing conditions, nanostripe device channels have much stronger gate control and larger induced carrier densities than their unpatterned device channel counterparts, shown in **Fig. 3**.

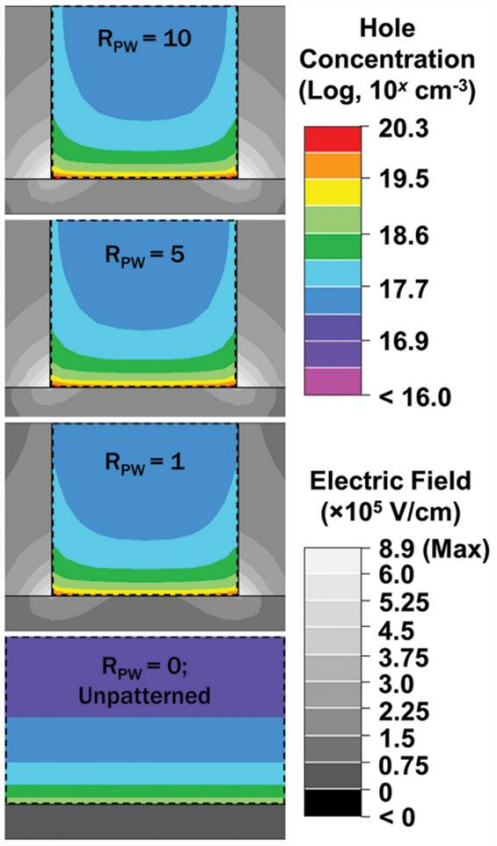

Fig. 3. *The cross-section profiles comparing the hole density and electric field strength of unpatterned film with nanostripes at various R_{PW} shows the focusing of the gate's electric field on the edges of the nanostripes. The semiconductor is outlined in black dashed lines for clarity, and all devices are operated at V_{GS} = -2 V and V_{DS} = -1 V, have W_{ST} = 20 nm, and have a channel length of 2 µm.*

To help the study of nanostripe device design, all material and most device design parameters were kept constant. All devices are bottom gate and top-contact thin-film transistors, and each device has a 20 nm thick polymer semiconductor and a 180 nm thick zirconium dioxide (ZrO_2) gate dielectric. We simulated 20 nm wide stripes because it is one of the smallest dimensions that current nanoimprint lithography tools can reliably print on flexible substrates [20]. For all the results described in the section, the semiconductor film thickness has been kept constant. We have separately verified that varying the film

thickness in the range 15-640 nm has little impact on the TFT currents. Thicknesses from 90 nm to 35 nm of solution-deposited ZrO_2 has been regularly used and reported by our group for many amorphous metal oxide and carbon nanotube semiconductor TFTs [26]. This makes 180 nm a practical and achievable gate dielectric thickness for these simulations. Simulated nanostripe devices (schematic shown in **Fig. 2b**) have also been simplified to one stripe of width, W_{ST}, centered over the gate that is W_{tot} wide, where $W_{tot} = W_{ST} + P_{ST}$. Using one stripe allows a reduction in the volume of the simulation (which, for a full device, would include an entire array of stripes), enabling the use of finer mesh points in areas of highly varying carrier concentrations and electric fields for increased simulation accuracy. These individual stripes have perfectly symmetrical geometries reflected across the axis cleaving the device along the channel, splitting the channel width in half. We use a Neumann boundary condition along these axes of high symmetry, and for our specific geometry, this is equivalent to using a periodic boundary condition. This means we can interpret our single stripe TFT setup as if it is a single stripe situated in an infinite array of periodic Simulations also used Fermi-Dirac statistics, since the extremely high carrier densities requires such a model. Meshes were mapped hexahedron meshes. For all devices, the mesh density at the semiconductor-dielectric interface in the *y*-direction was a constant 400 points/μm. For all nanostripe devices, the mesh spacing at the edge of the stripe devices in the *x*-direction was a constant 1000 points/μm.

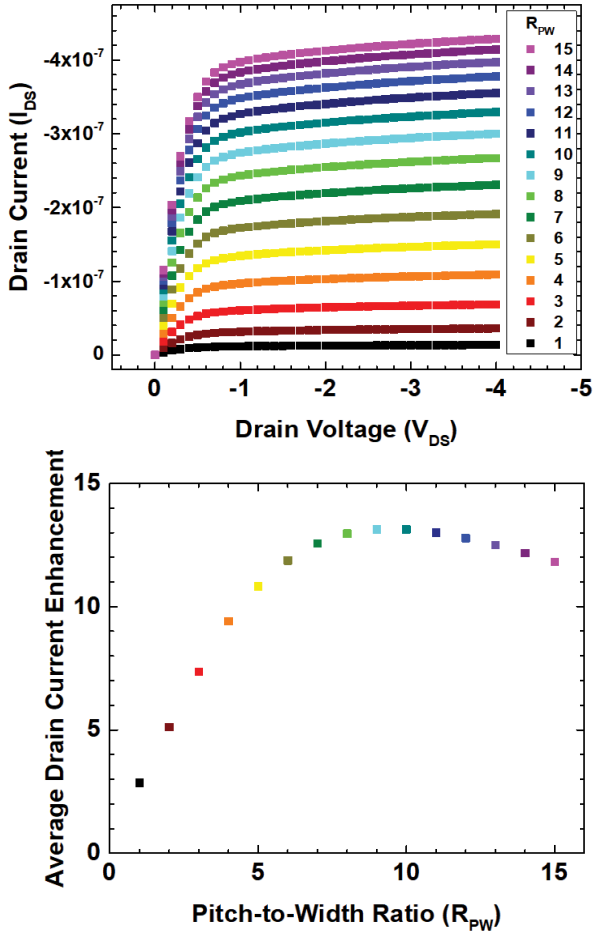

Fig. 4 *(a) Drain currents of nanostripe devices with a fixed width of 20 nm at various R_{PW}. All devices are operating at V_{GS} = -2 V. Increasing R_{PW} increases the drain and saturation current, though at higher R_{PW}, the improvement in currents becomes less pronounced. (b) Drain current enhancement of nanostripe devices compared to equivalently sized unpatterned devices*

SIMULATION RESULTS AND DEMONSTRATION OF ENHANCEMENTS

The geometry of the nanostripe devices in this dissertationare parameterized by three key variables: the stripe width (W_{ST}), the pitch to width ratio (R_{PW}), which is defined as $R_{PW} = P_{ST}/W_{ST}$, and channel length (L). All other device dimensions, such as gate dielectric thickness, are the same for all devices and listed in **Table I**.

Symbol	Quantity	Value	Unit
Semiconductor		*PDPP-TNT*	
$\epsilon_{r,s}$	Permittivity	3	
N_A	P-Type Doping	7×10^{14}	cm^{-3}
E_g	Bandgap	1.99	eV
χ_s	Electron Affinity	3.3	eV
N_C, N_V	Density of States (Conduction and Valance)	1×10^{21}	cm^{-3}/eV
v_s	Saturation Velocity	1×10^{6}	cm/s
τ	Carrier Lifetime	1×10^{-5}	s
Carrier Concentration Dependent Mobility			
μ_0	Minimum Mobility	1×10^{-4}	cm^2/V-s
α	Concentration Prefactor	1.2×10^{-3}	
Gate Dielectric		*ZrO_2*	
$\epsilon_{r,di}$	Permittivity	23	
T_{die}	Dielectric Thickness	180	nm
Device			
χ_{SD}	Metal Contact Work Function	5.29	eV
L_{reg}	Regular Channel Length	2	um
L_{short}	Short Channel Length	150	nm
T_0	Device Operation Temperature	300	K

Table I. *Parameters and values used for PDPP-TNT in TCAD simulations.*

Variation of Nanostripe Pitch

In **Fig. 3**, the cross sections of the nanostripes at the midpoint of the channel length are shown for varying R_{PW} with a fixed stripe width (W_{ST}) of 20 nm. While maintaining the same biasing conditions and only increasing R_{PW}, the intensity of the electric field at the edge of the stripe is greatly enhanced. Effectively, nanostripe patterning focuses the electric field of the gate and can be viewed as the TFT equivalent to a silicon FinFET transistor without needing a complicated wrap-around gate structure. Compared to silicon

FinFET transistors, nanostripe TFTs not only improve the overall gate control to lower off-currents, but also features a design that focuses on locally enhancing electric field, and in turn, locally enhancing the carrier concentration at the edges. By focusing the carrier concentration enhancement locally, nanostripes take advantage of the carrier concentration dependent mobility and create very conductive stripe edges. The resulting device performance enhancement can be seen in the output curves in **Fig. 4a**, where increasing the R_{PW} increases the drain on-current and the saturation current, even when the W_{ST} is a fixed 20 nm. The on-current is a key figure of merit in display TFTs which allows the TFT to drive higher current loads and enables the scale down of TFT area, leading to higher aperture ratios in displays. To make a fair comparison between nanostripe and unpatterned film devices, we evaluate drain current enhancement by comparing the currents of a nanostripe to their "equivalently sized" unpatterned thin film devices. An "equivalently sized" thin film device has a width that is equal to the nanostripe device's total width, W_{tot}, as illustrated in **Fig. 2b**. Plotting the on-current enhancement of nanostripe devices to their equivalently sized unpatterned devices in **Fig. 4b** shows that the maximum enhancement for these devices with W_{ST} = 20 nm occurs at R_{PW} = 10 with a current enhancement of a factor of more than 13. The drain current enhancement reaches a maximum because the absolute drain current will saturate with increasing R_{PW}, as shown in **Fig. 4(a)**; however, the response of the unpatterned device will continue to increase linearly with W_{TOT}. This leads to the decrease in relative enhancement, shown in **Fig. 4(b)**. The optimum R_{PW} will change with different device geometries and semiconductor materials. This significant enhancement can be attributed in part to the carrier concentration dependent nature of the carrier mobility. The field effect mobilities of these simulated devices with varying R_{PW} plotted in **Fig. 5** also show a linear trend typical of reported TFT devices [1], [3]. It is important to note that for these extracted mobilities, the capacitance is overestimated and

assumed to be an unpatterned film capacitance. The overestimation of the capacitance leads to a more conservative and underestimated extraction of field effect mobility.

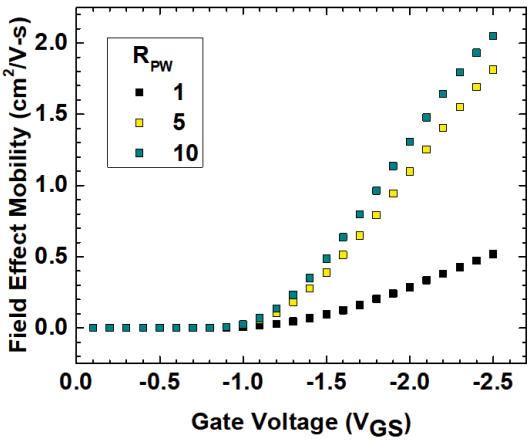

Fig. 5. *Linear hole mobility with respect to gate voltage (V_{GS}). The simulated TFT's field effect mobility follows the linear behavior of previously reported TFTs. While the material itself remains unchanged, the apparent field effect mobility improves with increased R_{PW} due to enhancements on transport from the nanostripe pattern. Note that the simulated device is operating at V_{DS} = -1 V, which is a much lower drain bias than experimental papers typically show for field effect mobility. W_{ST} = 20 nm.*

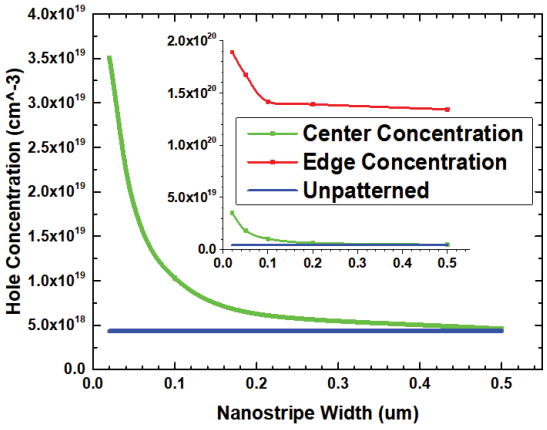

Fig. 6. *Induced carrier concentration at various locations in the nanostripe. The carrier concentration at the center of the stripe is highly dependent on W_{ST}. As the stripe becomes wider, the hole concentration at the center approaches that of the hole concentration of an unpatterned film. As seen in the inset, the hole concentrations at the edge of the device consistently see large enhancements compared to the unpatterned film.*

Variation of Nanostripe Width

In addition to tuning the R_{PW} to increase the enhancement at the edges of the stripes, modifying W_{ST} can tune the percentage of the channel that experiences the enhancement due to nanostripe patterning. Most striped TFT devices that have been reported have been wider than 200 nm, and **Fig. 6** shows that at 200 nm, the nanostripes already have enhanced carrier densities at the edges, but most of the channel behaves just as a channel in an unpatterned device. However, further narrowing W_{ST} causes enhancement of hole concentration to dominate the behavior of channel and not just as an isolated effect at the edges.

While obtaining improved on-currents is one very noticeable advantage of using nanostripe devices, another important consequence of increased carrier concentrations is greatly improved conductivities in the channel of the TFT. The increases in overall drain current and conductivity we observe are predominantly a consequence of the spatial redistribution of carriers in the nanostripe devices, creating local regions with high volume carrier density and hence conductivity. With enhancement of both the hole mobilities and increased hole concentrations in nanostripe devices, the conductivity—which is directly proportion to the product of the mobility and carrier concentration [27], drastically increases compared to unpatterned devices under the same operating conditions. High conductivities caused by high gate voltages have been shown to reduce contact resistance in TFTs [28], [29], a problem that has the scaling down of channel lengths in TFTs [30], [31]. From the simulation results seen in **Fig. 7**, conductivities in a nanostripe can also exceed 100 S/cm along the edges of the stripe, a conductivity threshold that is approximately at the transition between insulating and metallic behavior [32]. Such metallic behavior has been reported by our group in amorphous zinc tin oxide TFTs [3] and has been reported in polymers using ion gel gated devices [33], but has yet to be shown

for semiconducting polymer devices that are electrostatically gated. Now, the nanostripe device is a strong contender for attaining metallic behavior in conventionally gated polymer FETs.

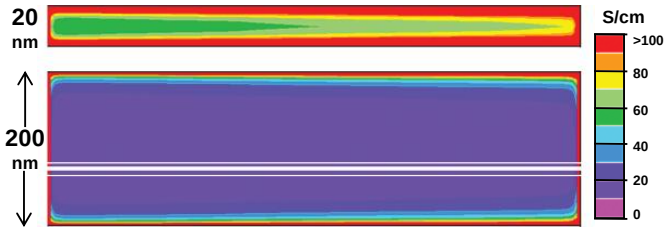

Fig. 7. *Conductivity profiles at the nanostripe-dielectric interface. Local conductivity plot of a narrow nanostripe and a wider nanostripe width. When conductivities are greater than 100 S/cm, the semiconductor is in the metallic state. The upper bound of this conductivity plot, shown in red, is set to 100 S/cm. (Stripe width to length not to scale.)*

SHORT CHANNEL ADVANTAGES OF NANOSTRIPE TFTS

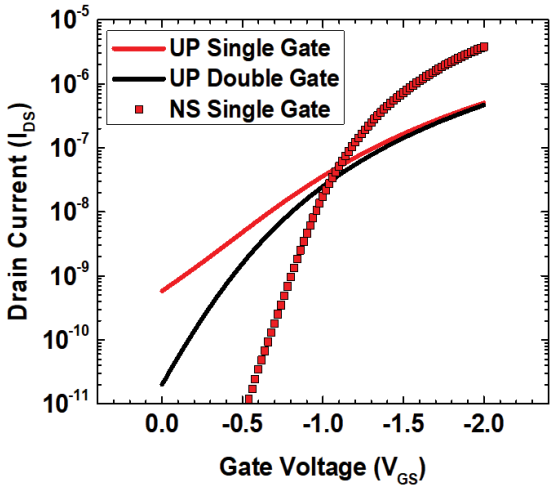

Fig. 8. *Nanostripe (NS) and unpatterned (UP) 50 nm short-channel devices with W_{ST} = 20 nm. Nanostripe patterning of short channel devices more effectively reduces the off-current and increases the on-current compared to adding a second gate for TFTs with carrier concentration dependent mobilities.*

Beyond helping TFTs improve on-currents and lower contact resistance, the nanostripe device geometry also mitigates short channel effects, which are seen when the source-drain bias competes with and dominates the gate control of the channel. Nanostripe TFTs offer a promising opportunity to shorten the channel lengths which can increase the operation frequencies of TFT devices [34], which have hitherto been the bane of most TFT technologies and have prevented their use in RF circuits and systems [35]. Previous attempts to create nanoscale polymer TFTs resulted in devices with severe short channel effects that did not saturate and showed diode-like behavior for output currents [36]. Nanostripe patterning can significantly reduce short channel effects more than just adding a second gate to a TFT. **Fig. 8** shows three equivalently sized and 50 nm long TFTs. While adding a second gate (an identical thin ZrO_2 top gate) does improve the sub-threshold swing and reduce the off-current some, nanostripe patterning lowers the off-current and improves the sub-threshold swing even better while also significantly enhancing the drive current.

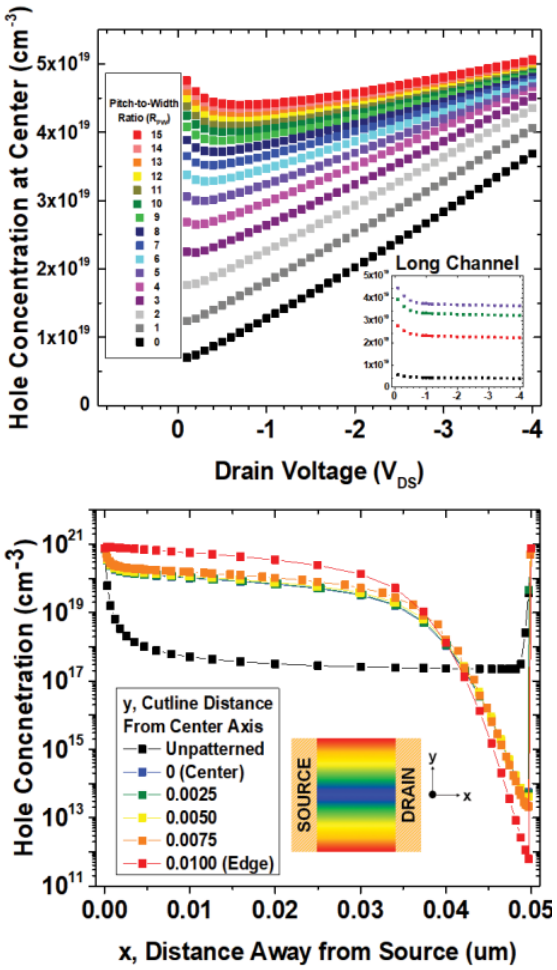

Fig. 9. *Hole concentration profiles. (a) Constant mobility TFTs still show significant short channel effect reduction. Nanostripe devices reduce the influence of VDS on carrier concentrations at the center of the channel. (b) Hole concentration profile across the channel length of an unpatterned device (black) and a nanostripe device with RPW = 15. Both devices biased in saturation region, the unpatterned device does not exhibit pinch-off behavior because of short channel effects while the nanostripe device does.*

In much of the above discussion, we have assumed that the mobility increases linearly with carrier density, as has been observed in several materials [1]–[3]. However, even for materials that do not have carrier concentration dependent mobilities [4], [5], this structure still can improve device performance and reduce short channel effects. This is

evident in **Fig. 9a** where we show the effect of changing drain voltage on the hole concentration at the center of the stripe along the semiconductor-dielectric interface. For an unpatterned thin film device, the drain voltage directly impacts the hole concentration because of short channel effects. But as the pitch-to-width ratio is increased, the impact of the drain voltage becomes reduced on the hole concentration and the behavior of the hole concentration at the center approaches the behavior of long channel devices. To further illustrate the reduction in short channel effects for constant mobility TFTs, the hole concentration along the channel length of an equivalently sized unpatterned and nanostripe device are compared in **Fig. 9b**. Both devices are operating under the same saturation mode bias, but the nanostripe device shows distinct pinch off regions all along the width of the stripe. On the other hand, the unpatterned device does not have a pinch off region at all. The additional patterning of disordered semiconductors into nanostripes can open the door to greatly reducing channel lengths while retaining good transistor operating characteristics.

PRELIMINARY EXPERIMENTAL RESULTS

With the wealth of TCAD simulation evidence, we sought to demonstrate these advantages of nanostripe patterning in a fabricated device. Nanostrip patterned zinc tin oxide (ZTO) transistors were made. The zinc tin oxide was deposited from solution that was made in an oxygen- and moisture-suppressed glovebox environment with 0.24 M of $Zn(NO_3)_2$ and 0.22 M of $SnCl_2$ dissolved in acetonitrile. The gate dielectric for this TFT was made from solution-based zirconium oxide (ZrO2) which was also made in a glovebox environment and used 0.5 M of zirconium chloride ($ZrCl_4$) and 0.5 M of zirconium isopropoxide isopropanol complex {$Zr[OCH(CH_3)_2]_4$ $(CH_3)_2CHOH$} dissolved in 2-methoxyethanol. The ZTO-ZrO_2 TFT device was fabricated on a doped silicon wafer with

native oxide which was approximately 1-3 nm thick. The bulk silicon substrate also acted at a global back-gate electrode. Once the silicon wafer was cleaned with sonicated solvent baths with acetone, methanol, and isopropyl alcohol, the substrate was treated under an ultraviolet ozone lamp with the chuck heated to 120ºC for 10 min to both clean the substrate and modify the surface energy to promote the wetting of the ZrO_2 solution. The sample was then transferred into the glovebox for solution deposition. The ZrO_2 solution was spincoated onto the substrate at 2000 rpm for 30s and then underwent a solvent bake off in the glovebox at 100ºC for 1 hour. The sample was then transferred out of the glovebox for the oxidation anneal which was an anneal in an O_2 rich environment at 500ºC for 1 hour that formed the ZrO_2 film. A second layer of ZrO_2 would be deposited immediately after the oxidation anneal finished. The same steps and spin speed would be used to also deposit the single ZTO layer on top of the double ZrO_2 layer. It is important to note that no cleaning steps were performed in between the deposition of each solution layer. Once the ZrO_2 and the ZTO layers were deposited and formed, the nanostripes needed to be patterned. PMMA was spincoated on and the pattern was written by electron-beam (e-beam) using Raith eLine lithography tool and then developed in a MIBK:IPA (1:4) solution bath. The sample was then etched using a dry, reactive ion etch (RIE) with 20 sccm of CHF_3 and 5 sccm of O_2 at a pressure of 40 mTorr and at a power of 100 W. Once the nanostripes were etched, the remaining PMMA was lifted off in an acetone bath, and then aluminum contacts were deposited with thermal evaporation in pressures $<1.0\times10^{-6}$ Torr. Atomic force microscopy images and optical images of the stripe patterning are shown in **Fig. 10**. Stripes were formed, and the resulting nanostripes were about 100 nm tall and about 420 nm wide for the 500 nm wide stripe-pattern, and about 50 nm tall and 180 nm wide for the 250 nm wide stripe-pattern, showing that the stripes were over-etched. Even with the slight over-etching

of the stripe pattern, these nanostripe patterned TFTs worked and demonstrated enhancement in both the drive current and the mobility of as seen in **Fig. 11**.

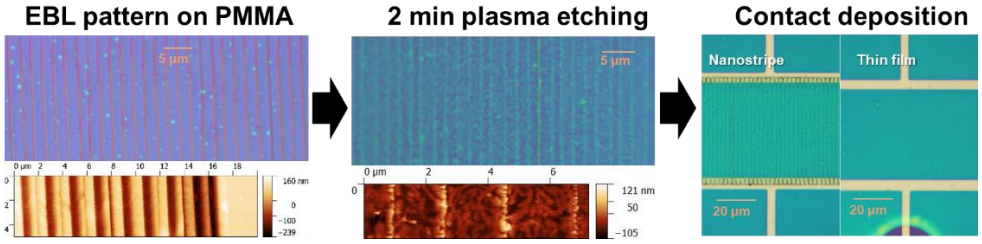

Fig. 10. *Optical and AFM images of various steps in the fabrication of nanostripe TFTs. From left to right: (Left) PMMA patterned by e-beam lithography into 250 nm wide stripes with 750 nm wide spacing and after development; top image is optical and bottom image is AFM. (Middle) Nanostripe channel after 2 min of reactive ion etching and an acetone liftoff bath; top image is optical and bottom image is AFM. (Right) Optical image showing the nanostripe TFT and the unpatterned thin film TFT after contact deposition.*

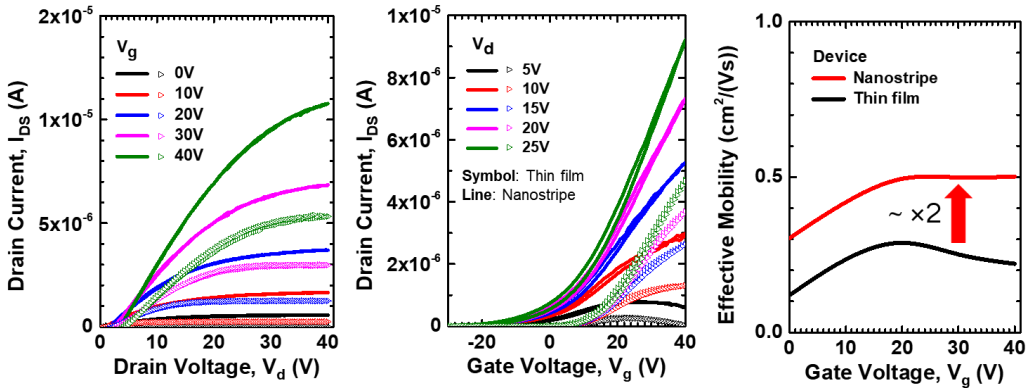

Fig. 11. *Transistor characteristics of the nanostripe TFT compared to the thin film TFT. Nanostripe device was 180 nm wide stripes, and both TFTs were 70 um wide with a channel length of 45 um. From left to right: (Left) Output characteristics showing the nanostripe device with higher drive current than the thin film device. (Middle) Transfer characteristics in linear scale showing the nanostripe device with a lower VTH and therefore a lower operating voltage than the thin film device. (Right) Carrier mobility showing a factor of two enhancement of the nanostripe TFT over the thin film TFT.*

Chapter 3: Nanostripe Conclusion

In summary, we have demonstrated the considerable advantages that accrue for TFT performance in device architectures where the active semiconductor is patterned into nanostripes. We have shown that nanostripe patterning of TFTs can enhance the on-current of TFTs by up to a factor of 13 when comparing the on-current of a nanostripe TFT and its equivalently sized unpatterned thin-film TFT. The carrier densities and conductivity in the channel are both enhanced with this architecture and additional enhancement in the on-current can be seen if the semiconductor has carrier density dependent mobility. Short-channel effects are mitigated, suggesting the possibility of making small channel length devices that push the maximum frequencies of operation even higher. Nanostripe devices were fabricated and demonstrated to enhance the carrier mobility and current levels by a factor of approximately 2. Such architectures can potentially improve the frequency response of TFTs and open new applications. The advantages of this approach will apply to all TFT materials systems while it will be especially useful for polymer, organic, and amorphous metal oxide TFTs.

Chapter 4: Appendix

In high-mobility polymers as well as in amorphous metal oxides, the multiple trap and release (MTR) model for change transport has been shown to work well [1]–[3]. The essential physics of MTR type transport of charge in this polymer is modeled as a linearly carrier concentration dependent mobility system. Similar models have been described in previous publications [4], [5]. The linear carrier concentration dependent mobility relationship can be derived from the multiple trap and release transport model for mobilities [6], [7], which is exponentially dependent on temperature, T,

$$\mu_p = \mu_o \cdot \alpha \cdot e^{-(E_t - E_v)/kT} , \qquad (1)$$

where μ_p is the hole mobility, μ_o is the mobility in the transport band, α is a constant depending on the ratio of carriers in the band and total carriers, E_t is the trap state energy level, and E_v is the valence band energy level. Given that mobility is scaled by the ratio of free carrier density to total carrier density, the effective mobility can also be expressed as follows:

$$\mu_p = \mu_o \cdot \left(\frac{p_v}{p_t + p_v}\right), \tag{2}$$

where p_v is the density of free holes experiencing band transport in the valence band and p_t is the density of trapped carriers. Note that we assume that $p_t + p_v$ is approximately the total carrier density, p. For polymer material systems which have activation energies much higher than kT, we can use the Boltzmann approximation to estimate the free hole ($p_v = N_v \cdot e^{-(E_f - E_v)/kT}$) and trapped carrier densities ($p_t = N_t \cdot e^{-(E_f - E_t)/kT}$). This means that this model is no longer accurate when the device operation pushes the Fermi level close to or into the valence band, where the mobility is expected to saturate. Using the Boltzmann expressions and combining with Eqs. 1 and 2, we can approximate that

$$\mu_p = \mu_o \cdot \left(\frac{1}{1 + \frac{N_t(E)}{N_v} \cdot e^{-(E_t - E_v)/kT}}\right) \cong \mu_o \cdot \frac{N_t(E)}{N_v} \cdot e^{-(E_t - E_v)/kT}, \tag{3}$$

where E_f is the Fermi level, N_v is the valence band density of states and $N_t(E)$ is trap density of states as a function of energy. Assuming a large number of trapped carriers (when $p \approx p_t$) and an exponential band tail distribution, we can approximate p with a Fermi-Dirac occupation probability, which can now be written as

$$p = \int_{E_f}^{\infty} \frac{N_{t0}}{kT_0} \cdot e^{-\frac{E - E_v}{kT_0}} \cdot f(E) \cdot dE\ , \tag{4}$$

where N_{t0} is the total density of trap states, T_0 is the characteristic width of the density distribution, $f(E)$ and is the Fermi-Dirac function. Under lower temperature

operating conditions, $f(E)$ can be approximated as a step function and the evaluation of the definite integral results in

$$p = N_{t0} \cdot e^{-(E_f - E_v)/kT_0} \ . \tag{5}$$

Rearranging the expression after integration will give

$$\left(E_f - E_v\right) = kT_0 \cdot ln(\frac{p}{N_{t0}}) \ . \tag{6}$$

Given Eq. 6, we can rewrite the Boltzmann expression for p_v as

$$p_v = N_v \cdot e^{-\left(\frac{T_0}{T}\right) ln(\frac{p}{N_{t0}})} \ . \tag{7}$$

Eq. 2 can now be written as

$$\mu_p = \mu_0 \cdot \frac{N_v}{N_{t0}} \cdot (\frac{p}{N_{t0}})^{(\frac{T_0}{T} - 1)}. \tag{8}$$

where typical T_0 values for TFT materials approach 600 K [4], confirming the observed behavior where hole mobilities display approximately linear carrier concentration dependence.

We then simplify the unipolar carrier concentration dependent hole mobility model is of the form $\mu_p(p) = \mu_{min} + \mu_o\ (N_V/N_{to}^2) \times p$, where μ_p is the hole mobility, μ_{min} is the minimum hole mobility, μ_o is the band transport hole mobility, N_V is the valence band density of states, N_{to} is the total trap density, and $p(r)$ is the hole concentration as a function of the spatial coordinate. It is also important to note that the process of fabricating stripes could introduce trap states at the sidewall edges. These edge trap states are not included in the simulation. However, given substantial carrier density enhancement, these trap states can be quickly filled and nanostripe devices retain their advantage over unpatterned films. Simulations used Fermi-Dirac statistics, since the extremely high carrier densities requires such a model. Meshes were mapped hexahedron meshes. For all devices, the mesh density at the semiconductor-dielectric interface in the *y*-direction was a constant 400 points/μm. For all nanostripe devices, the mesh spacing at the edge of the stripe devices in the *x*-direction was a constant 1000 points/μm.

NANOSPIKE ELECTRODE TFTS

Abstract: To scale down thin film transistor (TFT) channel lengths for accessing higher levels of speed and performance, a redesign of the basic device structure is necessary. While the nanostripe patterning has the potential to make great strides towards this goal, nanostripe TFTs require patterning the active material, which depending on the process flow, could introduce damage to the semiconductor material and reduce carrier transport properties. However, with nanospike-shaped electrodes, the active material can remain untouched while the metal contacts are instead shaped to produce many of the advantages of nanostripe patterning. Patterning the source and drain electrode into tens-of-nanometers wide stripes with sharp tips induces field emission effects at the sharp tips. One of the advantages resulting from these field emission effects is that the higher local electric field at the nanospike tips can assist charge injection from the electrodes into a short-channel (sub-200 nm) TFT, as we demonstrate for amorphous oxide and organic TFTs. These designs also can result in the formation of charge nanoribbons at low gate biases that greatly improve sub-threshold and turn-off characteristics. This new design paradigm, in which the TFT can operate with a gate electric field less than the source-drain field, is proposed and demonstrated, and is a promising solution for boosting TFT performance through charge focusing and charge nanoribbon formation in flexible/printed electronics applications by combining small channel lengths and thick gate dielectrics. Data from indium gallium zinc oxide (IGZO) TFTs and the organic semiconductor (pentacene) TFTs are used to demonstrate the effects, showing that they are not confined to a single material system and can benefit many materials systems.

Chapter 1: Introduction to Short Channel TFT Challenges

In more demanding applications of thin-film transistors (TFTs), scaling down the channel length [27], [37] is problematic due to increasing contact resistance and short-channel effects [38]–[40]. When contact resistance is high, it can dominate TFT performance at short channel lengths. Contact resistance and short channel effects can both be seen in amorphous oxide semiconductors, organic/polymer semiconductors, and 2D semiconductors such as MoS_2 [41]–[43], and various approaches have been tried to overcome these problems [43], [44].

SUBTHRESHOLD OPERATION

As the channel length of TFTs decrease, the influence of the drain bias over the channel can increase until the gate loses the ability to turn off the channel. This phenomenon is captured in part by the concept of drain-induced barrier lowering (DIBL). DIBL occurs when the drain bias, which controls the lateral electric field, lowers the barrier for carrier injection at the source even while the gate is biased the turn the channel off. In other words, the vertical electric field, which is controlled by the gate, no longer retains dominant influence over the energy barrier to carrier injection from the source contact. When looking at transistor characteristics, some hallmarks of DIBL short channel effects include degraded subthreshold swing, drain-bias dependent subthreshold swing, drain-bias dependent threshold voltage, and in the most extreme cases, inability for the gate to turn the transistor off. A common approach to improving the subthreshold performance of a TFT is a combination of decreasing the dielectric thickness and choosing a dielectric material that is higher-k, or a material with a larger dielectric constant. This approach is essentially increasing the gate dielectric capacitance. However, for flexible electronics, the strategy of thinner and higher-k dielectrics is in direct opposition of what is required for

dielectrics for reliable flexible performance and to meet the low thermal budget of flexible substrates. We are left with the task of identifying a method to increase the gate control of the short TFT channel in a way that is compatible with the strict specifications for flexible electronics.

CONTACT RESISTANCE

Contact resistance is present in any metal-semiconductor junction that is a Schottky barrier and is not inherently a problem. Contact resistance negatively begins impacting the performance of transistors when the resistance of electrode injecting carriers into the semiconductor is comparable to the resistance of the channel. At longer channel lengths for most TFTs, the channel resistance is greater than the contact resistance, and contact resistance does not heavily impact the transistor characteristics. As the channel decreases, by Ohm's law, the channel resistance decreases proportionally. The shrinking of the channel length and the lowering of the channel resistance is desirable and increases many of the key performance metrics of transistors, including increasing speed of transistor operation and increasing the drive current. However, once the channel resistance decreases to the point that it is comparable with the contact resistance, the overall device resistance is limited by contact resistance and further channel length scaling does not lower the overall device resistance effectively. Contact resistance limits the enhancement of transistor characteristics as the TFT's channel length scales down. One hallmark of contact resistance can be seen in the linear region of output characteristics. A transistor with negligible contact resistance will have a clear linear drain current turn on. A transistor with noticeable contact resistance will exhibit a more exponential drain current turn on, as the injection of carriers through a Schottky barrier is exponentially dependent on the bias.

The ability to reduce or lower contact resistance in a TFT allows the device a longer runway to continue scaling down to reduce the device resistance and improve the overall performance of the transistor. Increasing the overall operating speeds and drive currents of our flexible transistors for flexible electronic systems critically depends on finding strategies to lower contact resistance in TFTs.

Chapter 2: Nanospike Electrode Thin Film Transistor Basics[2,3]

The nanospike electrode TFT design addresses both contact resistance and short-channel effect problems in multiple classes of semiconductors with channel lengths below 200 nm. Charge injection is facilitated due to a combination of field-emission and enhanced charge carrier density near the source electrode. Simultaneously, and sub-threshold swings are much steeper and off-currents are kept low at short channel lengths. Nanospike electrode TFTs facilitate a new mode of TFT operation where the spatial distribution of charges in the channel changes, such that charges are expected to form one or more narrow channels in sub-threshold and near turn-off conditions (we designate these narrow regions of charge as "charge nanoribbons").

[2] Ch 2-5: K. Liang *et al.*, "Field-Emission Enhanced Contacts for Disordered Semiconductor based Thin-Film Transistors," *2021 Device Res. Conf.*, pp. 1–2, Jun. 2021, doi: 10.1109/DRC52342.2021.9467233.

[3] Ch 2-5: K. Liang *et al.*, "Nanospike electrodes and charge nanoribbons: A new design for nanoscale thin-film transistors," *Sci. Adv.*, vol. 8, no. 4, Jan. 2022, doi: 10.1126/SCIADV.ABM1154.

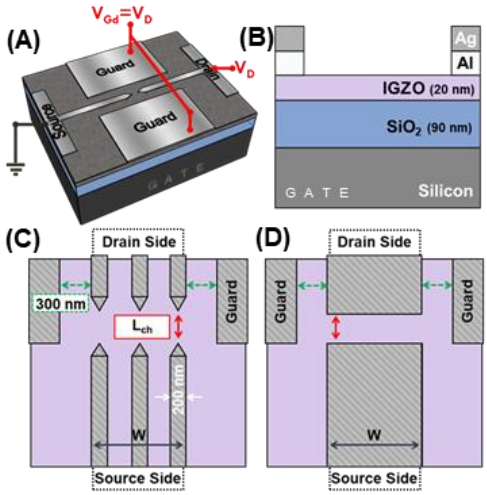

Fig. 12. *Nanospike electrode TFT design and characteristics. (A) Device schematic of a TFT with side-guard electrodes. (B) Cross section showing the materials and layer thicknesses. (C), (D) Design and dimensions of nanospike array (multispike) electrode TFTs with equivalently sized flat electrode TFTs.*

NANOSPIKE ELECTRODE DESIGN AND IMPLEMENTATION

The basic device design of a nanospike TFT with IGZO is shown in **Fig. 12**, where both the source and drain electrodes are nanospike-shaped. Such electrodes are analogous to field emission tips used in vacuum electronics and in conducting scanning probe microscopes, both of which take advantage of shaping metal tips to sharp points to achieve local field enhancement for facile emission of electrons into the vacuum energy level [45]. In TFTs, nanospike shaped tips similarly focus electric fields at the source and/or drain contact tips. Far from the active channel (>1000 μm), the width of electrode lines is increased substantially to both reduce the resistance of the electrodes leading to the contact pads and increase yield and prevent line breaks from occurring in the metal lines. For comparison, conventional flat edge electrodes (or flat TFTs) are also fabricated alongside with the same channel length. For accurate channel current measurements and to avoid collecting spreading currents, separate side guard electrodes are employed, and they are biased to the same potential as the drain.

IGZO thin-film fabrication and measurement

The indium gallium zinc oxide (IGZO) TFTs were fabricated as bottom gate, top contact transistors. The substrate used is a silicon wafer with 90 nm of thermally grown SiO_2, where the highly doped silicon wafer acted as a global bottom gate and the SiO_2as the gate dielectric. 20 nm of IGZO was then sputtered on the sample using a 1:1:1 target for In:Ga:Zn respectively, and at a RF power of 150 W, a pressure 5 mTorr, and at 7% O_2 in Ar. The IGZO film was annealed at 450 °C for 1 hour in air to complete the film formation. For the TFT data shown in **Fig. 4**, the IGZO material was sputtered using a target with a composition of Ga_2O_3:In_2O_3:ZnO at a ratio of 1:2:2 respectively. The sputtering conditions were the same as previously stated.

All devices reported in this chapterwere fabricated in this manner, unless otherwise noted. For the 200 nm short channel devices, JOEL electron beam patterning was for the metal contact patterning to prototype various source drain designs and geometries, processing details listed below. For long channel devices, all layers up to and including IGZO were the same as the short channel devices. To deposit the contact metals, 500 nm of Al was deposited through a shadow mask. Device dimensions of the long channel devices include channel lengths ranging from 50-150 um with all W/L = 20. The sputtered IGZO material is very uniform and consistent with previous reports of low variation of film quality [46]. Both long and short channel devices were tested and analyzed under vacuum, unless otherwise noted, in a probe station at pressures $<1\times10^{-3}$ Torr and at room temperature.

Scanning electron microscope (SEM) images were taken of the resulting pattern using a ZEISS NEON 40 SEM. Micrographs of TFTs with an array of 5-spike electrode pairs shown in **Fig. 13**.

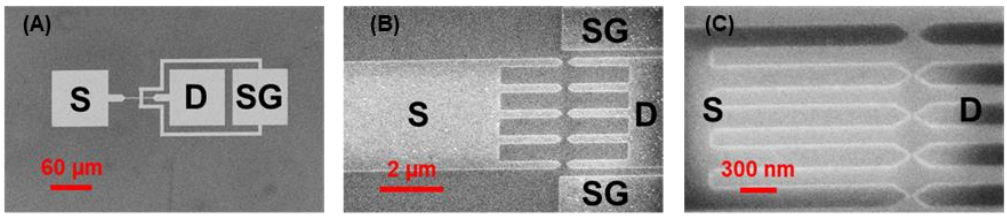

Fig. 13. *SEM images of nanospike electrodes. (A) SEM image of TFT design featuring a side-guard electrode. (B) Nanospike electrode TFT channel with 5-spikes for the source and the drain, with ~300 nm gap between side-guard electrodes and drain electrode. (C) Nanospike TFT with 1:3 spacing.*

E-beam lithography of nanospike contacts

The nanospike pattern was fabricated using a JEOL 6000 FSE Electron Beam (e-beam) lithography tool. A solution of ZEP-520A:Anisole::1:2 was used as the e-beam resist. The resist was deposited onto the prepared IGZO samples with a plastic syringe through a 0.2 µm PTFE filter and spin coated for 2000 RPM for sixty seconds and annealed at 180° C for 2 min. The resulting film is ~140 nm thick, as measured using an Ellipsometer J.A. Woollam M-2000 DI.

The writing of the pattern was done at 50 keV with an exposure current of 100 pA using Exposure Mode 7, the fine feature aperture, and 5th lens of the JEOL 6000 system. Development was done using a bath of Amyl Acetate for 15 seconds followed by a rinse in DI water.

The resulting patterned resist was used as a mask to create metal contacts through a metal deposition and lift-off process. 30 nm of aluminum and 30 nm of silver was deposited onto the resist using a Kurt J. Lesker Thermal Evaporator tool. Aluminum was used as the contact layer, while silver is primarily used to help with SEM imaging of the metal features. Lift-off was conducted by soaking the sample in a 4-hour bath of Remover PG at 80° C followed by 2 seconds of ultrasonication, and then a rinse using DI water.

TFT Isolation Method and Measurement

While most of the TFTs presented in this section were made on substrates where the semiconductor film was uniform and continuous on the entire substrate, the currents measured from these devices required a post-processing step to subtract out leakage, as described in the next section. To increase the fidelity of the characteristics measured, we introduced semiconductor film isolation as a processing step. Each device was isolated by removing a ring of the semiconductor film surrounding each TFT device. For IGZO, isolation was achieved with electron beam patterning and a wet etch. For organics, isolation was achieved by using probes to scratch around each device.

To isolate individual devices, the IGZO film was etched into islands, where the etch pattern is conformal to the devices. The etch areas were patterned using Raith eLine Electron Beam (e-beam) lithography tool. The e-beam resist consisted of 4 wt% PMMA in anisole and was spun onto the IGZO samples at 3000 RPM for 60 seconds. The substrate was then annealed at 180°C for 2 minutes. The writing of the pattern was done with 20 kV EHT and a 120 μm aperture. The sample was developed with a solution consisting of 10 mL of MIBK and 15 mL of IPA for 10 seconds followed by a rinse in IPA. The patterned devices were then wet etched in an HCl solution diluted in water (1:6, respectively), followed by a water rinse. After the etch, the remaining PMMA was lifted-off in acetone. The measurement of these isolated TFTs were taken in air at atmosphere and at room temperature.

LEAKAGE CURRENT SUBTRACTION METHOD

The small negative current at low drain high gate bias is due to the global gate pinhole leakages. Due to the measurement setup, the measured drain current at the drain side of the device not only includes the current through the TFT, but also the leakage

current from the gate. Clearly, the leakage current is dependent on the difference of the drain voltage and the gate voltage. The leakage current is large when the gate voltage is a lot greater than the applied drain voltage. It becomes smaller when drain voltage is close to gate voltage and it is negligible when drain voltage is larger than the gate voltage. To get a clean output curve, it is necessary to get rid of the leakage current. Below gives the method of how to remove the negative leakage current in the output characteristics. It must be emphasized that gate leakage present in these devices not intrinsic and is a result of fabrication and material handling conditions which can be improved to reduce gate leakage current.

To subtract out the gate leakage current from the drain current, the first step is to get the leakage current characteristics dependent on gate drain voltage difference. The transfer curve (drain current I_d) is measured when both drain end and source end are grounded (V_d = 0 V, V_s = 0 V) for the device under test. The gate voltage (V_g) is swept from -30 V to +30 V, while the drain end current was picked by the parameter analyzer. **Fig. 14(A)** shows the drain current Id as a function of V_g when V_d=0. Apparently, this is the leakage current that is picked up at the drain end, since there is no voltage applied at the drain end. Assuming that the leakage current is only dependent on the voltage difference between gate and drain (V_{dg}), the leakage current as a function of V_{dg} (V_{dg}=V_d-V_g) is obtained as shown in **Fig. 14(B)**.

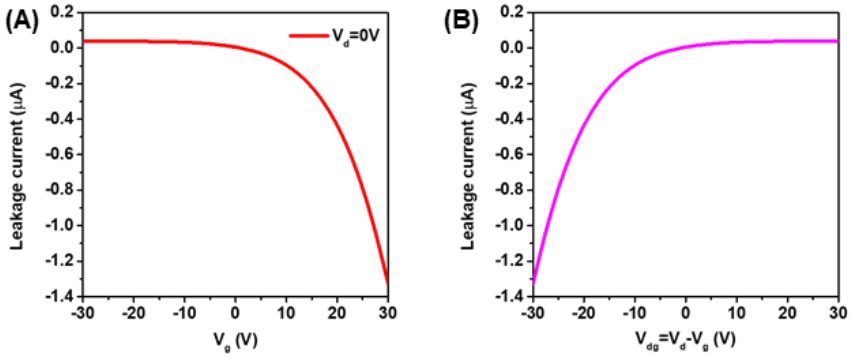

Fig. 14. *Leakage current estimation for leakage current processing. (A) leakage current as a function of gate voltage V_g when V_d = 0 V. (B) leakage current as a function of drain-gate voltage difference.*

The second step is to remove the leakage current from the output curves. Now that the V_{dg} dependent leakage current characteristic is obtained, the leakage current at a certain operating condition (a given V_d and V_g) can be accurately estimated. Subtracting the measured drain current by the leakage current at given operating condition, the actual drain current through the TFT channel under this operating condition can be obtained. Doing the subtraction for each current point, the true output characteristics of device can be recovered. **Fig. 15** shows the output current before **(A)** and after **(B)** correction. It may be noted that the biggest differences are at small drain voltages. The differences become very small, almost negligible, at larger drain voltages.

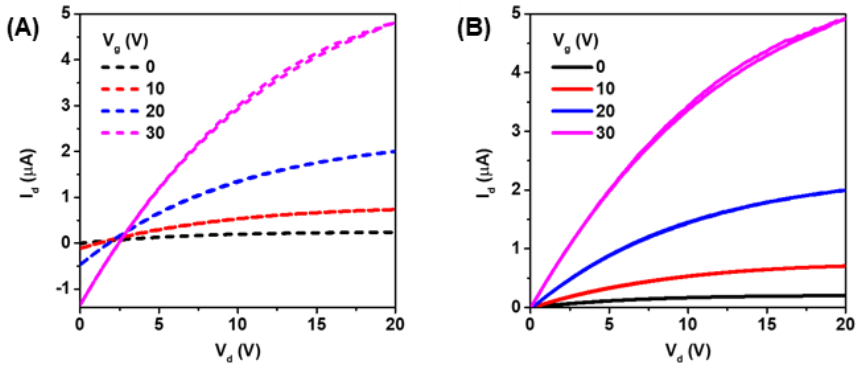

Fig. 15. *Example unprocessed and processed output characteristics. (A) output current before leakage current correction. (B) output current after leakage current correction.*

The following are figures from the main text which use this leakage current processing. The raw data plots are shown below the leakage current processed plots.

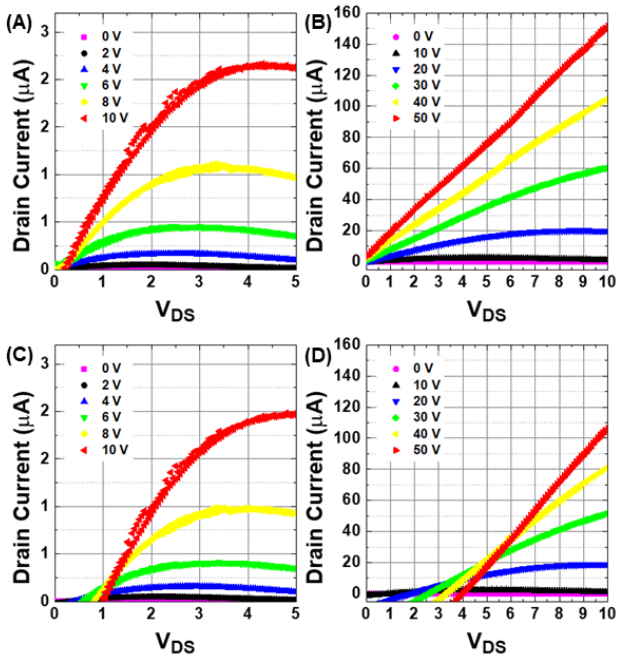

Fig. 16. *Single spike output characteristics from Fig. 1, processed and unprocessed. Single spike, 50 nm channel length. Top row processed; bottom row unprocessed.*

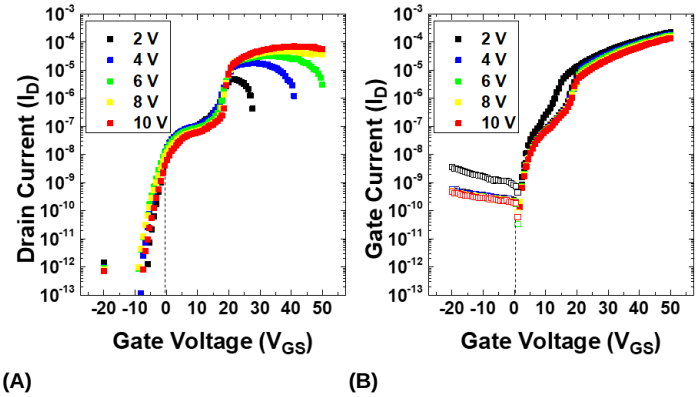

Fig. 17. *Measured gate leakage current of nanospike TFT. 5-spike, 150 nm channel length. (A) Total drain current without leakage processing. (B) Measured gate leakage current, exhibiting a bend as the device turns on.*

Chapter 3: Single-spike Tip Nanospike TFT Characteristics

To quantify the impact of shaping electrodes into nanospikes, we first explored the electrode design featuring only one spike at the source side and one spike at the drain side, referred to from now on as a single-spike electrode. The single-spike electrode TFT also featured guard electrodes and were fabricated on the same substrate stack of a silicon wafer, doped and used as a back gate, and 90 nm of thermally grown silicon dioxide. The nanospike TFT has a channel length (L_{CH}) of 200 nm, the nanospike width at the base is 200 nm, the nanospike tip radius is ~10 nm, and the offset between the source-drain contact and the guard contact is 300 nm.

TRANSISTOR CHARACTERISTICS OF SINGLE-SPIKE TFTS

As seen in **Figure 18**, the single-nanospike TFT has higher current density, steeper subthreshold swing, and lower voltage operation than the flat electrode TFT with the same channel length. The flat TFT also has a channel length of 200 nm, a channel width of 1000 nm, and the same offset between the source-drain contact and the guard contact of 300 nm. The single-nanospike TFTs and the flat TFTs were processed on the same substrate and underwent the same fabrication procedure.

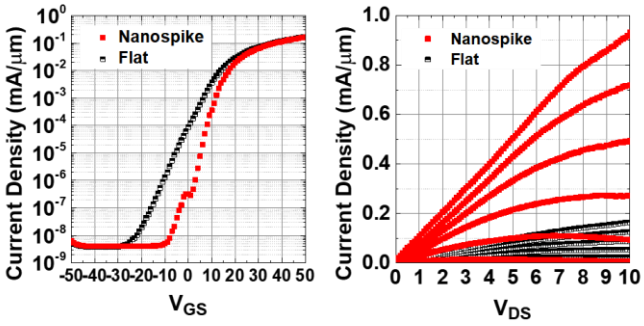

Fig. 18. *Output characteristics comparing a single-NS electrode TFT with a flat electrode TFT with the width normalized current density. (B) Transfer characteristics comparing the two TFTs showing the NS has both improved subthreshold swing and a much lower $|V_{ON}|$ than the flat.*

To analyze and compare the threshold voltage, V_{th}, between nanospike and flat electrode TFTs, we used the following V_{th} extraction method, developed by Emily Zhou. To obtain V_{th}, the slope of the square root of the drain current, $\sqrt{I_d}$, transfer curve needs to be calculated. V_{th} is extracted using the most linear portion of the $\sqrt{I_d}$ curve, so to identify the linear region, we have developed an algorithm in MATLAB. The algorithm divides the data set into smaller subsets and then calculates the slope and correlation coefficient R^2 for each voltage subset. The data was then divided into subsets with smaller V_{GS} ranges and then analyzed to identify the linear region of operation. Each subset of data was calculated for the linear slope, g_d, and the correlation coefficient, R^2, of the slope. To identify the linear region, only data subsets with the highest g_d (top 10%) were considered. Then the data subset with the largest R^2value was determined as the linear region. After the algorithm finds and fits the linear region, it then finds the x-intercept of the linear fit of that region, which is approximated to be the V_{th}. In this chapter, the threshold voltages used in the calculation were extracted from devices with identical dimensions. For 200 nm channel length TFTs, the V_{th} is summarized in **Table II**.

V_{DS}	Flat	Spike
2 *V*	10.29 *V*	2.91 *V*
4 *V*	13.24 *V*	6.39 *V*
6 *V*	14.89 *V*	8.67 *V*
8 *V*	16.36 *V*	10.48 *V*
10 *V*	16.96 *V*	12.27 *V*

Table II. *V_{th} values for nanospike v. flat TFTs.*

In **Fig. 19** is lateral electric field distribution in a nanospike and flat TFT geometry. This TCAD simulation uses and electrostatic approximation, where there are no free carriers in the semiconductor and acts as a dielectric, and the metal is a perfect conductor. The lateral electric field is defined as the component of the electric field that is parallel to

the vector of the source tip to drain tip. The color scale used in the simulation figure is on a logarithmic scale and the scale is capped at 1.05×10^8 V/m to more clearly depict the lateral electric field enhancement seen at the spike tip. Actual maximum electric field of this nanospike tip is $>2\times10^8$ V/m. Due to field enhancement at the spike tip, the field in the rest of the channel is lower for the nanospike TFT compared to the flat TFT. This can potentially translate into smaller velocities and currents for the nanospike TFT. But at small channel lengths, the reduction in velocities and currents does not happen for two reasons. First, there is a dissipative ohmic drop at the metal-semiconductor interfaces in the flat electrode TFTs that are not evident from the idealistic simulations shown. The second reason is that in such small channel length TFTs, carrier velocities are likely already saturated.

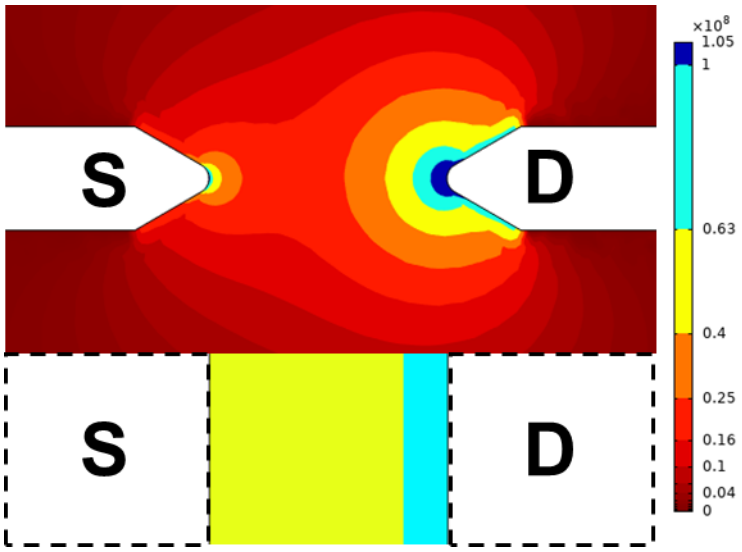

Fig. 19. *Electric field comparison of nanospike and flat electrodes. Electric field simulation comparison of spike and flat electrode. Comparing the x-component field (V/m) distribution between source to drain at V_{GS} = 2 V and V_{DS} = 10 V. Nanospike electrode width is 100 nm, flat electrode width simulated is 500 nm.*

Nanospike TFTs also lower the contact resistance. In **Fig. 20**, we see a comparison the overall device resistance between an IGZO nanospike TFT and a IGZO flat TFT where the nanospike TFT has lower total resistance. The electric field enhancement of the nanospike tip has two driving advantages. The higher electric field induced by the nanospike tip lowers contact resistance by lowering the energy barrier for injection and enhancing the carrier concentration at the tip once carriers have been injected, which further reduces the contact resistance.

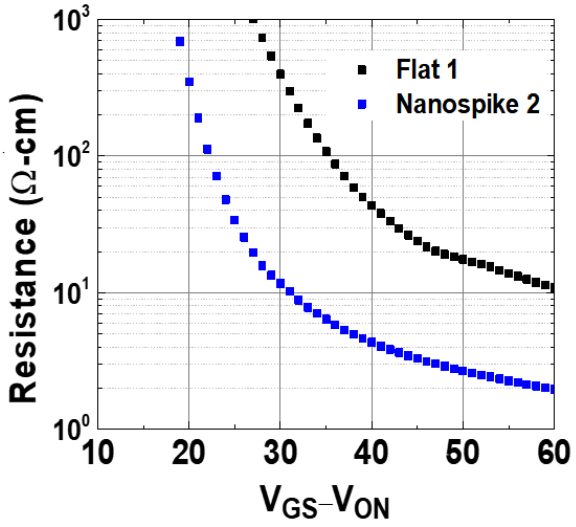

Fig. 20. *Total device resistance comparison of a NS and a flat electrode IGZO TFT with a channel length of 200 nm.*

SHORT CHANNEL SINGLE-SPIKE TFT

Nanospike TFTs not only are an effective solution for enhancing subthreshold swing while boosting current density at a 200 nm channel length, nanospike TFTs are also very effective at reducing short channel effects down to at least 50 nm. **Figure 21 (A)-(B)** show the measured characteristics of a 50 nm channel length single nanospike IGZO TFT. The characteristics show excellent drain current modulation with gate voltage despite the

physical gate dielectric thickness being almost twice the channel length. At low gate voltages in the sub-threshold region, drain currents do not change significantly with increasing drain voltage. This is evidence that short channel DIBL-like effects have been suppressed, which is different from what is typically observed in TFTs below 100 nm, especially at this thick of a gate dielectric. The output characteristics in **Fig. 21(B)** show linear and saturation behavior in the expected voltage regions. The gate leakage current, which flows from the drain contact through the insulator, was subtracted from these characteristics to arrive at more accurate drain currents.

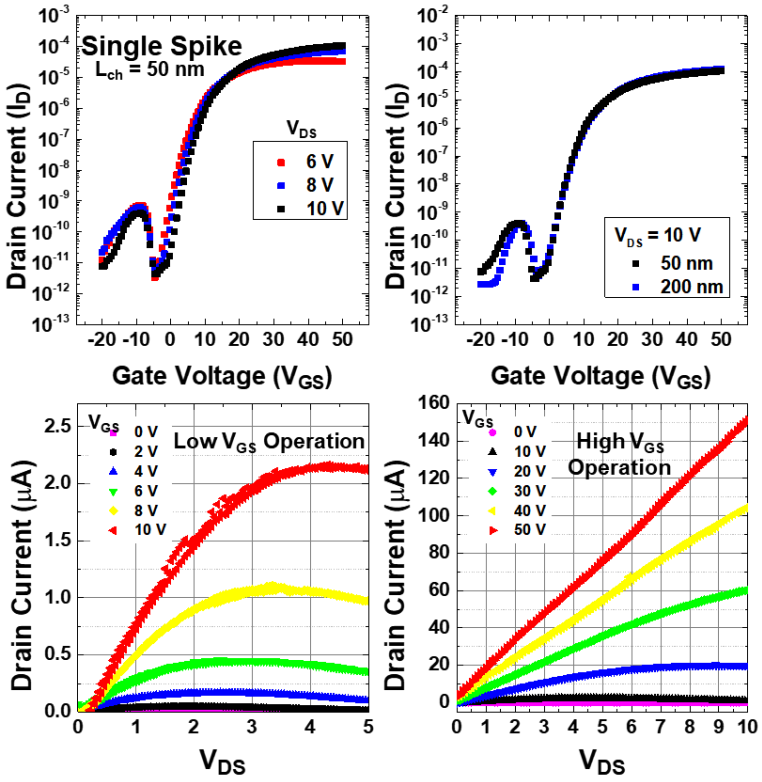

Fig. 21. *(A) Transfer characteristics of 50 nm channel length single spike TFT at various V_{DS}. Characteristics include both forward and reverse sweeps which are nearly identical, showing little hysteresis. (B) Transfer curve at V_{DS} = 10 V for two different channel lengths. (C) Output characteristics at low V_{GS} operation, showing minimum contact effects for a 50 nm channel length device. (D) Output characteristics at high V_{GS} operation, showing minimum contact effects for a 50 nm channel length device.*

RELIABILITY AND STATISTICS OF SINGLE-SPIKE TFTS

With these impressive improvements in the performance of nanospike TFTs over flat TFTs, we wanted to provide some information on variability in the performance of these single-spike TFTs. Reported below is data summarizing the statistics and variation of V_{th} in **Table S3** and drive current in **Fig. S6** for 7 identical nanospike devices. These nanospike TFTs were 200 nm channel length single spike electrode TFTs.

V_{DS}	Std. Dev. (σ)	Avg.	% σ	Min.	Max.
2 *V*	1.81 *V*	10.36 *V*	17%	7.85 *V*	13.47 *V*
4 *V*	1.36 *V*	9.25 *V*	15%	7.47 *V*	11.42 *V*
6 *V*	1.31 *V*	10.89 *V*	12%	9.14 *V*	13.07 *V*
8 *V*	1.40 *V*	12.56 *V*	11%	10.61 *V*	15.06 *V*
10 *V*	1.40 *V*	14.41 *V*	10%	12.62 *V*	17.11 *V*

Table III. *V_{th} statistics for single spike 200 nm channel length TFTs.*

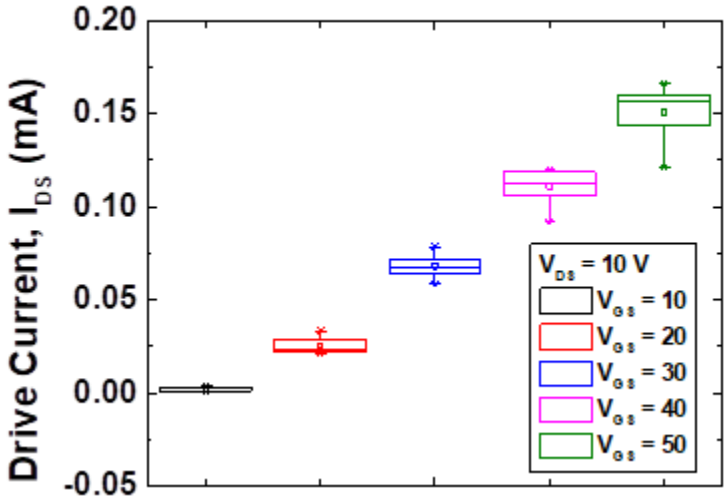

Fig. 22. *Drive current statistics of nanospike TFTs. Statistical variation and distribution of drive currents for single spike 200 nm channel length TFTs.*

Chapter 4: Multispike Tip Nanospike TFT Performance and Parameters

SPIKE SPACING STUDY

To increase drive current in a spike electrode TFT, a line array of nanospikes can be employed. Three different spacings between individual nanospikes were studied. Output characteristics are shown in **Fig. 23(A)** for TFTs with spike width to spike spacing ratios of 1:0 (in which the spikes are all coalesced), 1:1, and 1:3. The currents approximately scale with the overall device width. This is because the wider spacings between spikes correspond to a greater gate area and hence a greater number of channel electrons. Electrostatic electric field simulations in **Fig. 23(C)** were performed with COMSOL®. The magnitude of the enhancement of the electric field at the tips and the distribution of the field within the device channel are shown. As the spacing between individual nanospikes increases, so does the enhancement of the electric field at the nanospike tips and on the carriers within the channel. Given a tip radius of 20 nm for all devices, the maximum electric field of a 1:3 electrode is 2.58×10^6 V/cm, a 1:1 of 2.53×10^6 V/cm, a 1:0 of 2.45×10^6 V/cm. Increasing spike spacing also initiates the formation of individual charge conduction paths. The transfer characteristics in **Fig. 23(B)** also show greatly improved subthreshold characteristics with increased spacing between the nanospikes. This is again due to efficient charge focusing into nanoribbons in sub-threshold conditions. Indeed, at low gate voltages, when the source-drain electric field is greater in magnitude than the gate field, gate control can be considered quasi-3D. In several respects, the enhancement in gate control by the nanospike electrode TFTs make them the planar analog to silicon finFETs.

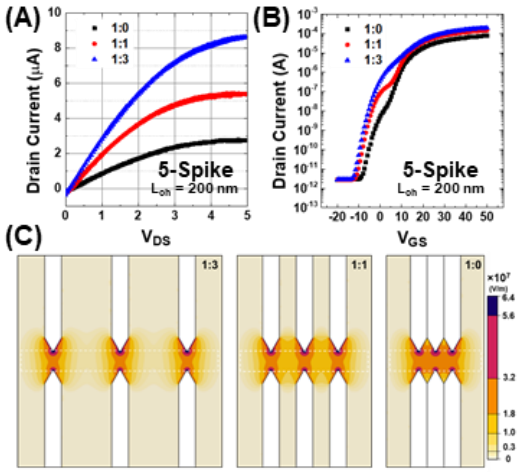

Fig. 23. *Nanospike electrode spacing. (A) Output characteristics at V_{GS} = 10 V of 5-spike electrode TFTs with 200 nm channel length at various spacings between individual spikes. (B) Transfer characteristics at various spacings showing improved subthreshold swing and improved drive currents with larger spacings between spikes. (C) Electric field simulations of multispike TFTs with various spike spacings; (left to right) 1:3, 1:1, and 1:0. V_{GS} = 4 V and V_{DS} = 10 V.*

SHORT CHANNEL AND CHANNEL LENGTH STUDY

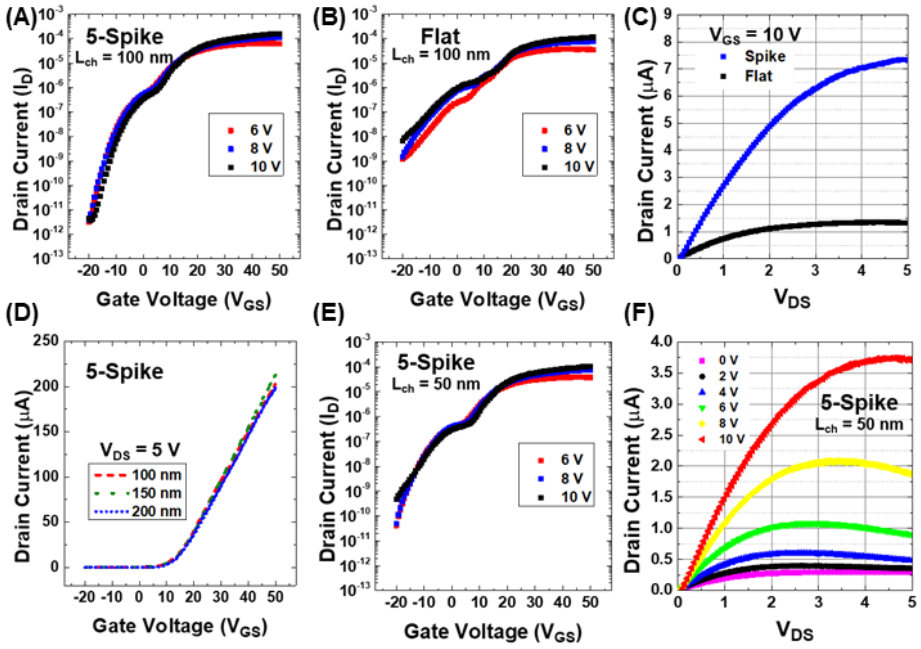

Fig. 24. *Short-channel nanospike TFTs. (A) Transfer characteristics of 100 nm channel length 5-spike electrode TFT with 1:1 spacing and (B) flat electrode TFT. (C) Output characteristic at V_{GS} = 10 V showing the 5-spike electrode TFT with nearly 5 times improvement in drive current. (D) Transfer characteristics on a linear scale at various channel lengths showing virtually identical responses. (E) Transfer characteristics of a 5-spike electrode TFT with 1:1 spacing and a 50 nm channel length that still retains gate control of the channel despite the channel length being less than the gate insulator thickness (90 nm thick SiO_2). (F) Output characteristics of the 50 nm channel length TFT in the linear and saturation regime.*

Figure 24 depicts the contrast between sub-threshold operation of multispike TFTs and flat electrode TFTs with the same channel length (100 nm) and width (1.8 μm). Sub-threshold swings are much better for the nanospike TFTs compared to flat TFTs, and the Off-current is much lower for the nanospike TFTs. Threshold conditions are reached at smaller gate voltages and the difference in drain current with respect to flat electrode TFTs near threshold is substantial, as shown in **Fig. 24(C)**. The nanospike TFT has better injection through field emission effects and increased volume carrier density at the source electrode because of charge nanoribbon formation, despite having a much smaller injection perimeter. The total number of charges induced by the gate is the approximately the same for the nanospike TFT and the flat TFT (since the channel width, channel length and gate area is the same). In the nanospike TFT, the high S-D electric field in the IGZO relative to the gate field causes charge nanoribbons to persist even in the on-state. Thus, the total channel charge is confined in a smaller surface area in the nanospike TFT compared to the flat TFT. The Fermi level is raised in the nanospike TFT resulting in increased volume carrier densities and lower contact resistance per unit channel width at the source. In IGZO and many other disordered semiconductors, multiple trap and release has been shown to be a dominant charge transport mechanism [41] and a higher carrier density generally translates to a higher mobility and carrier velocity. In **Fig. 24(D)**, it can be noticed that the currents are nearly identical in TFTs with multiple channel lengths, suggesting that the

carrier velocity is saturated. Saturation velocities, estimated from measured drain currents and the device geometry, are more than 1.5×10^6 cm/s, and are reduced in value from the theoretical saturation velocity of crystalline IGZO, which is > 8×10^6 cm/s. Such reduction in velocity from ideal values is due to trapping and has been described in detail in a theoretical study that was recently reported [41].

ETCH-ISOLATED NANOSPIKE ELECTRODE TFT

In order to reduce the gate leakage current further, a wet etch was performed to isolate individual IGZO TFT devices. **Fig. 25** shows the transfer and output characteristic of an isolated 100 nm channel 5-spike electrode TFT with a 4:1 spacing. With the isolation of individual devices, the gate leakage current is greatly reduced by more than a factor of 10^3. These devices are measured in air and the data presented is raw data with no leakage current processing. This data also shows both the forward and reverse measurement sweep, indicating negligible hysteresis. The output characteristics also show linear turn-on drain currents that are not visibly influenced by contact resistance and good saturation behavior.

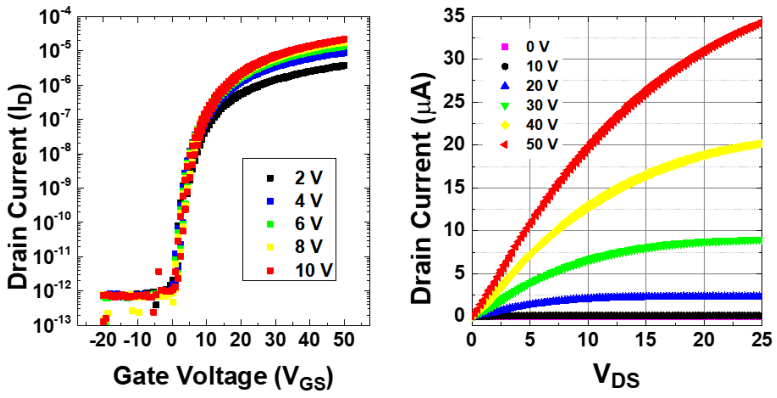

Fig. 25. *Nanospike electrode TFT with Isolated IGZO. 5-spike electrode TFT with the spike spacing of 5:1 and 100 nm channel length, measured in air. Data presented is raw and unprocessed. Gate leakage currents are greatly reduced. (A) Transfer characteristics and (B) output characteristics show a linear turn-on and good saturation.*

With the isolation etch, the transfer characteristics measured are less impacted by leakage currents compared to the previous TFTs with IGZO films that were not isolated. This means the subthreshold characteristics of these devices are much more reliable and we conducted further analysis. The subthreshold region of operation occurs before V_{TH}, which is the voltage that lies at the boundary of the ON-state and OFF-state of transistor operation. For these devices, the threshold voltage ranges from about V_{TH} = 5 V at V_{DS} = 2 V to V_{TH} = 8 V at V_{DS} = 25 V. When a TFT is in the subthreshold region, the drain current, I_D, is exponentially sensitive to changes by the gate voltage. This exponential sensitivity is captured in the figure of merit, subthreshold swing (SS), and is defined as $\max([d(V_{GS,1}) - d(V_{GS,0})] / [d(\log_{10}(I_{D,1})) - d(\log_{10}(I_{D,0}))])$ while $V_{GS} < V_{TH}$. While nanospike electrodes universally make these improvements in the subthreshold region, nanospike electrodes are especially effective at reducing the impact of short channel effects, helping to retain better SS and V_{DS} variability compared to unpatterned electrode devices. Initial subthreshold swing analysis can be seen in Fig. 26, where we show an approximation of subthreshold swing at V_{GS} = 1 V to V_{GS} = 1.7 V for various V_{DS}. Both for nanospike electrodes with 1:4 spacing and 1:1 spacing, the SS improves with increasing V_{DS}, indicating the increased responsivity to channel turn-on with the formation of nanoribbon channels.

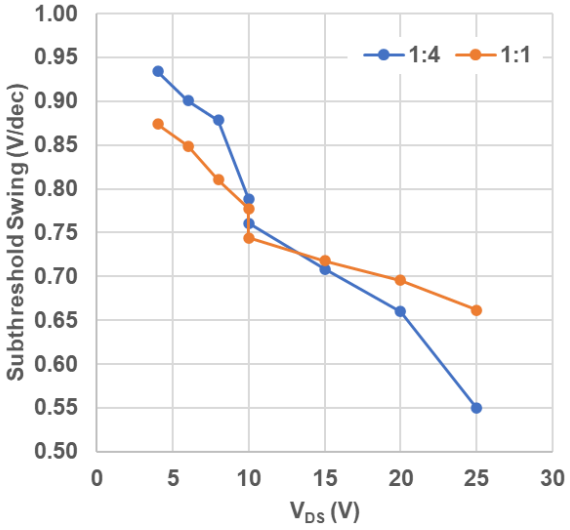

Fig. 26. *Subthreshold swing for isolation-etched nanospike electrode TFTs. The subthreshold swing is approximated from the drain currents at V_{GS} = 1 V and V_{GS} = 1.7 V. Both devices have improved subthreshold swing with increased V_{DS}.*

PENTACENE NANOSPIKE ELECTRODE TFTS

Moving beyond IGZO to a very different material system, data from pentacene TFTs with a channel length of ~20 nm is shown in **Fig. 27**. Similar TFTs were previously reported by our group in the context of short channel organic TFTs and chemical sensors [47]. However, many unique aspects of the characteristics of these TFTs were never mentioned in previous work. The maximum gate-source and gate-drain electric fields are lower than the maximum source-drain fields. The gate insulator is 100 nm thick, which is > 5 times more than the channel length. This is contrary to the design principle of all TFTs and even silicon field-effect transistors, in which the gate insulator is always designed to be much thinner than the channel length value.

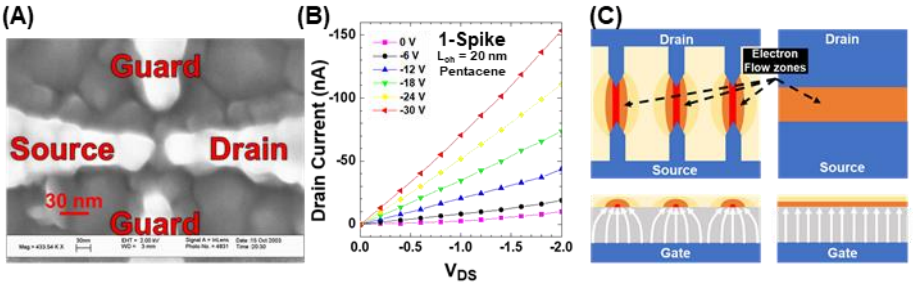

Fig. 27. *Pentacene nanospike TFTs. (A) SEM image of the ~20 nm channel length pentacene TFT with side guard electrodes. (B) Output characteristics at lower V_{DS} for V_{GS} as large as -30 V. Output characteristics show minimum contact effects at low V_{DS}. (C) Schematic demonstrating the formation of charge nanoribbons in the channel that focuses a larger area of gate electric field to a smaller channel area, allowing for better gate control as well as enhanced carrier concentrations in channel.*

Chapter 5: Nanospike Device Architecture TCAD Studies

When designing nanospike electrodes, there are several geometric parameters to consider. While it is possible to explore the parameterization of all the experimentally, it would be very time consuming to do so. Rather than explore the impact of changing various geometric parameters purely through experiments, we leveraged the insight provided by TCAD electrostatic simulations to get a better understanding of how changing parameters, such as spike tip radii and spike spacing, in conjunction with experimental verification, to both predict the qualitative design trends and parameterize the design space. In this section, we explore both simulations of different nanospike geometries and preview some TFT device architecture studies.

Electric Field Comparison of Nanospike and Flat Electrode TFTs

The nanospike electrode's proposed primary advantage is its ability to focus electric fields at its sharp tip. We first verified that the nanospike tip geometry does indeed focus electric fields better than the original flat electrode. We explored this concept with

COMSOL Multiphysics® with an electrostatic TCAD simulation. The electrostatic simulation does not include any free carriers with the model, therefore the semiconductor is approximated to be a dielectric. This reduces the computational intensity of the simulation, allowing us to increase the complexity of the geometry model and simulation a greater number of geometric and electronic instances.

Our initial comparison of a nanospike electrode and a flat electrode is shown in **Fig. 28.** We immediately see that the tips of our spike electrodes, even when rounded, still greatly enhance electric fields. All plots of the electrostatic simulations plot the x-component of the electric field, which is the vector component of the electric field which is begins at the source tip and travels to the drain tip.

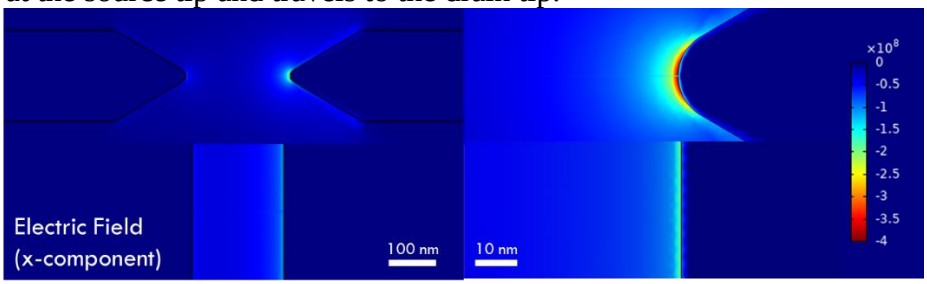

Fig. 28. *TCAD electrostatic simulation results of the x-component of electric field comparing a nanospike electrode and a flat electrode.*

NANOSPIKE TIP RADIUS OF CURVATURE STUDY

While we have explored many design parameters of nanospike electrodes in the previous chapter, such as spike spacing and TFT channel length, there are a few parameters that are difficult to control through fabrication, but essential to understanding the enhancement of nanospike electrode TFTs. One of these parameter is the nanospike tip radius, which is an artifact of the fabrication process rather than a design choice.

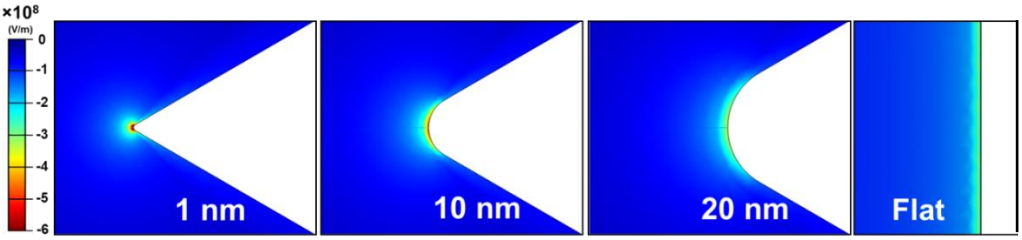

Fig. 29. *Electric field simulations of varying nanospike tip sharpness. Electric field (x-component, source to drain) simulations at various tip radii. Enhanced electric fields at tips with decreasing radii. Maximum electric fields of the tips for V_{GS} = 2 V and V_{DS} = 10 V are 14.7×10^6 V/cm in the 1 nm tip to 3.4×10^6 V/cm in the 20 nm tip.*

In **Fig. 29**, TCAD simulations show the electric field distributions at the nanospike source electrode in different conditions. The electric field strength at the tip is a function of tip radius, and while the change in field magnitudes appear small, the injection of carriers is exponentially dependent on the electric field magnitude. Even with wide spikes, if the tip radii are sufficiently small, there can still be TFT enhancements such as a reduced threshold voltage value and better subthreshold swing. In the experimental devices we made, when examined with the SEM we saw that the nanospike tips were typically fabricated at a tip radius of 15-25 nm. To approximate and track the electric field enhancement at different radii, we conducted further simulation analysis and looked at the cutline profile of the x-component of the electric field as a function of distance from the tip, as shown in **Fig. 30**. The increase in the tip radius does lower the maximum electric field seen at the metal-semiconductor interface when using this electrostatic approximation of nanospike TFTs. However, the enhancement even at larger radii is still significant and extends away from the tip laterally for several nanometers.

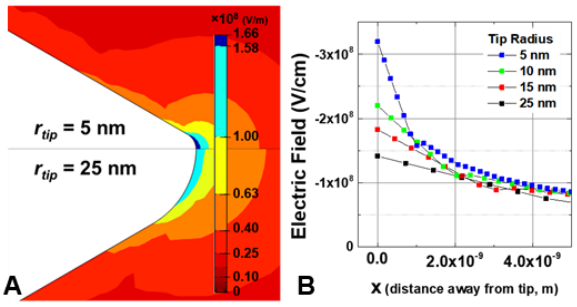

Fig. 30. *(A) Electrostatic field simulation of two NS source electrode tips with different tip radii of curvature. V_{GS} = 4 V and V_{DS} = 2 V. (B) Electric field strength with increasing distance away from NS tip at different radii of curvature. Note that the color scale is logarithmically spaced and not linearly spaced.*

Chapter 6: Nanospike TFTs for Flexible and Thick Dielectric Transistors[4]

Flexible electronics systems are sought for several applications and the field has made considerable progress in recent years [48], [49]. High-performance transistors have proved to be one of the most challenging components to fabricate with printing methods and/or on flexible substrates. Nevertheless, thin film transistors (TFTs) fabricated using printing and other methods well suited to flexible electronics have made significant strides in performance [50]–[52]. Several families of semiconductors have potential for use in large-area manufacturing on flexible substrates. These manufacturing-friendly semiconductors used for TFTs are typically disordered materials—or materials that have no long-range crystalline order—and include amorphous metal oxides (AMO) [53]–[62], polymers [63], [64], and small organic molecules [65]–[70]. AMO and polysilicon TFTs have already made their way into commercial products as display backplanes for high-end displays. Some of these systems are manufactured on flexible polyimide substrates [71].

[4] K. Liang, Y. Zhou, C. McCulley, X. Xu, and A. Dodabalapur, "High-performance thin-film transistor device architecture for flexible and printed electronics," *Flex. Print. Electron.*, Jul. 2022, doi: 10.1088/2058-8585/AC84EB.

However, such TFTs still struggle to operate at high enough speeds and low enough operating voltages to meet the specifications needed for flexible electronic systems such as internet-of-things (IoT) applications and advanced displays. TFTs made from disordered semiconductors have recently reached hundreds of MHz and even GHz frequency of operation [61], [72], [73]. High frequency demonstrations of these TFTs usually feature very thin and high-k gate dielectrics that typically require processing materials or methods that are sometimes difficult to combine with flexible substrates. Solution processed dielectrics are very compatible with the manufacturing and mechanical requirements for flexible electronics [74]. However, low-temperature solution processed dielectrics are usually lower-k dielectrics and are typically thick (to maintain acceptably low pinhole densities and gate leakage currents after being flexed). TFTs with such dielectrics may meet speed requirements to drive flexible displays, but may not be fast enough to meet more demanding specifications for processors [59]. Thick and low-k dielectrics have low capacitances per unit area, which leads to the operating voltages being high, which is very problematic in most applications. It is therefore very important to create device architectures that are more compatible for use with thicker gate insulators and low operating voltage while avoiding or mitigating a performance penalty. Nanospike-patterned source and/or drain electrodes can enable the realization of fast and flexible TFTs with comparatively thick gate dielectrics. This section presents the advantages of nanospike contact for flexible electronics applications with a combination of electric field simulations and experimental data.

MANUFACTURING CONSIDERATIONS FOR FLEXIBLE ELECTRONICS

Manufacturing methods that are being actively explored include patterning techniques such as roll-to-roll nanoimprint lithography, roll-to-roll photolithography, and

large-area printing methods such screen printing, inkjet printing, and coating methods such as slot-die coating [40], [75]. These methods and most other flexible electronics manufacturing methods heavily favor the use of solution based electronic materials. Solution-based materials and deposition techniques usually result in film thickness that are significantly larger than those typically attainable with rigid substrate-based manufacturing. Studies on flexible thin-films and devices fabricated with these solution-based methods typically require great effort to produce dielectric thicknesses < 100 nm [48], [74], [76], [77]. In TFTs, the gate dielectric must be pin hole free and for this reason dielectric thicknesses will tend to be high in high-yield manufacturing processes. Lateral dimension control down to the ~50 nm scale has been enabled by nanoimprint lithography. This is a very important development for flexible TFTs and multiple groups have reported on nanoimprinted TFT devices [21], [78]–[80]. In other recent work, amorphous oxide TFTs with 800 nm channel length with excellent properties have been fabricated with roll-to-roll photolithography and related methods [40].

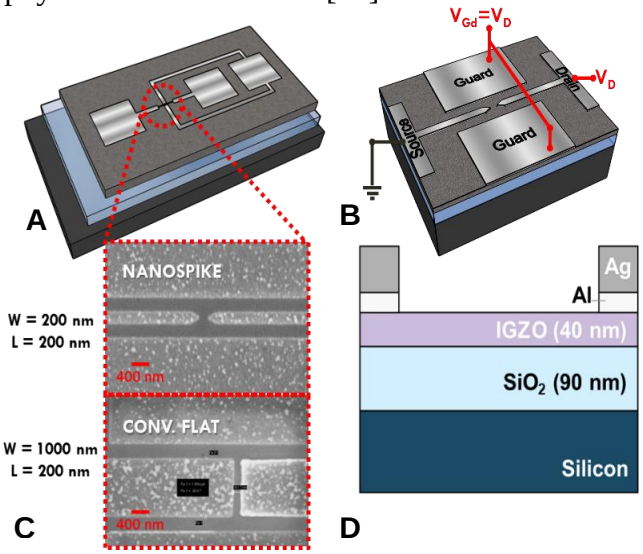

Fig. 31. *(A) Schematic of TFT device with a single pair of source and drain electrodes. Side guard electrodes biased at the same potential as the drain collect the spreading currents ensuring that the drain current is the current that flows in the channel. (B) Schematic demonstrating the measurement of TFTs with guard electrodes. (C) Scanning electron microscope image of active channel of a nanospike electrode TFT and a conventional flat electrode TFT used for comparison purposes. (D) Cross-sectional schematic of the layer structure of IGZO TFTs presented in this chapter.*

SIMULATION AND EXPERIMENTAL DESIGN

The nanospike device design presented in this work only requires one layer of high-resolution features and is robust enough to withstand coarser alignment between nanoimprinted layers. It is well suited for implementation on flexible substrates in combination with nanoimprint lithography or high-resolution photolithography, although results presented in this chapterutilized electron beam lithography. The nanospike electrode design is suitable for many families of thin-film semiconductor materials, including the two—amorphous metal oxide and organic semiconductors, that will be discussed here. Indium-gallium-zinc-oxide (IGZO) nanospike TFTs are shown in the device schematic and SEM images in **Fig. 31**. These bottom gate, top contact devices were fabricated on silicon wafers with 90 nm of thermally grown SiO_2, which has a capacitance of 3.83×10^{-4} F/m^2, in which the silicon functions as the back gate and the SiO_2 as the gate dielectric. The fabrication process has been described in more detail in Refs. [81], [82].

NANOSPIKE TFTS AT VARYING DIELECTRIC THICKNESSES

Nanospike electrode TFTs use electric field focusing, taking inspiration from the sharp tips in field emission tips and related fields [81], at the sharp tips and show improved gate control of the device over conventional flat electrode devices. **Fig. 32** shows TFTs with varying gate dielectric thicknesses simulated electrostatic field distributions of TFTs at zero gate voltage (nominally off state) done with COMSOL®. It is clearly seen that the

field magnitude close to the source is much lower in nanospike TFTs compared to flat TFTs at every thickness. This indicates better gate control and turn-off behavior in nanospike TFTs. The improved gate control in nanospike TFTs is seen in experimental data presented later as lower V_{TH} and improved subthreshold swing (SS). We have shown that these enhancements are scalable to much larger nanospike dimensions, such as the 800 nm scale, which has been realized on flexible substrates, using scalable manufacturing processes including photolithography [40].

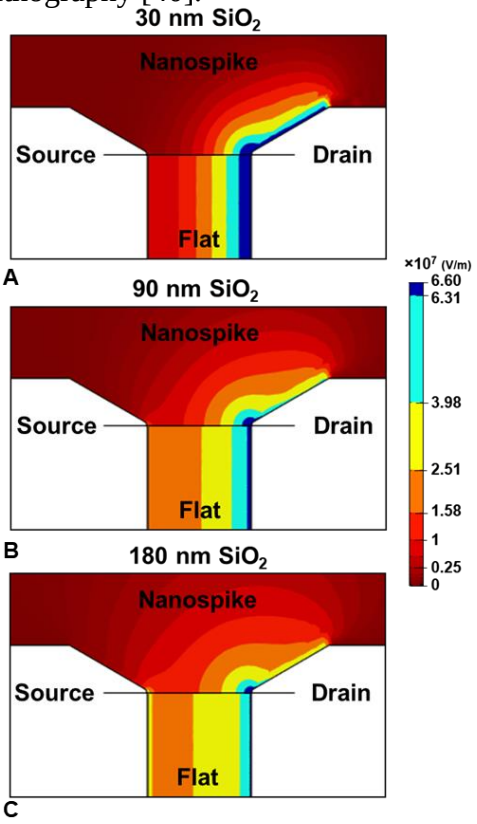

Fig. 32. *Lateral electric field simulations plots of 200 nm channel length TFTs at zero gate voltage with different gate dielectric thicknesses, (A) 30 nm, (B) 90 nm, and (C) 180 nm thick SiO_2. The lateral electric field strengths values are at the interface of the dielectric and the semiconductor, IGZO. Top side of each figure shows the field distributions in nanospike electrode TFTs and the bottom part of each figure shows the field distributions in flat electrode TFTs. V_{GS} = 0 V and V_{DS} = 6 V, in all the simulations.*

SHORT CHANNEL NANOSPIKE TFTS AT VARYING DIELECTRIC THICKNESSES

When shortening channel lengths of TFTs, improving gate control one of the first design challenges to overcome. The TCAD simulations in **Fig. 33** are in an off-state condition (V_{GS} = 0 V, V_{DS} = 6 V) and demonstrates significantly improved gate control of the nanospike TFT over the flat TFT at a short channel length of 50 nm. Since the gate is biased so the channel is off, the lateral electric field of a well-performing TFT should be very small to prevent drain induced barrier lowering (DIBL)-like effects. The nanospike TFT's gate control is superior and can be seen by lateral electric fields that are much lower in the nanospike TFT channel and throughout the thickness of the channel than the flat TFT channel. The nanospike TFT's gate control of the channel outperforms the flat electrode at every dielectric thickness, with the thickest dielectric nanospike TFT having better gate control than the thinnest flat TFT. With increasing dielectric thickness, the flat TFT's gate loses all control of the channel and experiences a uniform lateral electric field. However, the nanospike TFT's gate maintains at least partial influence over the channel, even at 180 nm thick dielectric, especially at the semiconductor-dielectric interface.

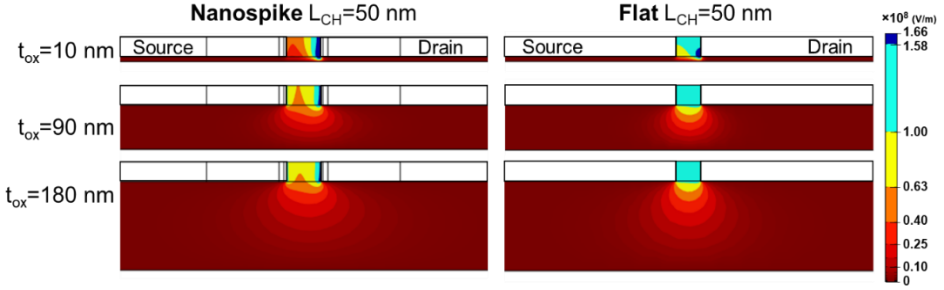

Fig. 33. *Electric field simulation plots of 50 nm channel length TFTs at varying dielectric thicknesses, from top to bottom, 10 nm, 90 nm, and 180 nm thick SiO_2. These plots show a cross-sectional view of the TFT. V_{GS} = 0 V and V_{DS} = 6 V.*

ORGANIC NANOSPIKE TFTS

Polymer and organic TFTs suffer more severely from contact resistance effects [65], [66], [69], [83], and the benefits of the nanospike electrode geometry are seen even more clearly in **Fig. 34**. These 800 nm channel length DNTT TFTs have a nanospike source electrode and a flat drain electrode, and these devices were fabricated and analyzed by Calla McCulley. Additional data on these devices can be found in the following citation, [82]. These results show that the nanospike electrode patterning of the source contacts of DNTT TFTs results in substantial improvements in regular transistor characteristics, showing improved drive current, better SS, lower V_{TH}, as well as significantly lowered device resistance and lowered contact resistance. These devices also feature 200 nm wide spikes with 800 nm wide spike spacing.

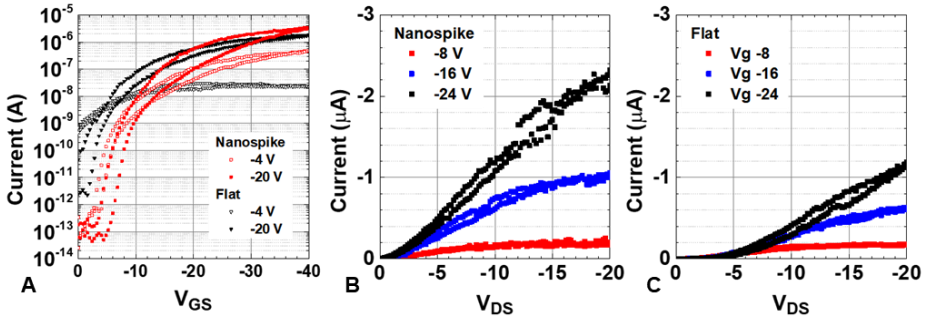

Fig. 34. *(A) Transfer characteristics of a DNTT nanospike-flat electrode TFT compared with a DNTT flat electrode TFT. The channel length is 800 nm for both TFTs. The nanospike-flat TFT features a nanospike source electrode consisting of an array of three spikes and a single flat drain electrode. The flat TFT has both flat source and drain electrodes. (B) Output characteristics of a DNTT nanospike-flat electrode TFT. (C) Output characteristics of a DNTT flat electrode TFT.*

CHARGE NANORIBBON FORMATION IN NANOSPIKE TFTS

The improved sub-threshold and turn-off characteristics in both amorphous oxide and organic nanospike TFTs are very likely a consequence of charge nanoribbon formation

which restricts the effective width of the channel to be more closely match the spike width. This behavior is more pronounced at large drain voltages and relatively small gate voltages. Due to the thick dielectric (~ 90 nm) and small channel length (200 nm), the lateral field is higher than the vertical gate field for sub-threshold conditions when the gate voltage is relatively small. This results in the charge flow regions to conform closely to the widths of the spikes with relatively little current flow in the space between the spikes. This ribbon-like channel geometry provides lateral gate control which reduces the off current. The restricted channel area below threshold also improves sub-threshold swing as fewer interface defects are active compared to a uniform channel in flat electrodes TFTs for which the effective channel area is larger. This will help reduce operating gate voltage to reach threshold and is especially beneficial for TFTs with thick gate insulators.

The principal advantages of nanospike TFTs can be thought of in the following terms: Charge focusing into nanoribbons implies that gate induced charge from a relatively large gate area is spatially concentrated in a smaller area. This leads to improved sub-threshold swings since a smaller number of interface states are active because of the reduced effective channel area. Above threshold, carrier mobilities are often enhanced due to the greater local carrier densities in semiconductors with multiple trap and release (MTR) or some types of hopping transport. The reduced contact resistance [82] also means that a greater fraction of the applied drain voltage is dropped across the channel, which also results in a larger drain current. These advantages can be used to increase the drive current density for a given set of operating voltages or they can be used to reduce the operating voltages to maintain a drive current density. The above comparisons are with respect to conventional flat edge electrode TFTs.

The demonstrated advantages of nanospike TFTs have been experimentally verified in multiple semiconductors and at channel lengths in the range 10-800 nm. Some

of these advantages will also apply for larger, micron scale, channel lengths. At such channel dimensions, electric field enhancements close to spike tips will continue to result in improved injection. Some of the advantages seen in smaller channel length TFTs will likely get weaker. The gate field will be much larger than lateral source-drain fields and hence charge nanoribboning will likely be absent, and the carrier density and current density will be more uniform (along the channel width direction) in the channel away from the source.

NANOSPIKES FOR FLEXIBLE ELECTRONICS SUMMARY

Nanospike electrodes provide a path for thick, solution-processed gate dielectric TFTs to perform at the speeds demanded by emerging applications for flexible electronics. By shaping source and/or drain electrodes of TFTs, we have demonstrated improvement of both subthreshold characteristics as well as above threshold characteristics. The geometry of the nanospike tip enhances electric fields which allows for both better gate control and increased carrier densities near the tip. In the subthreshold regime, nanospike electrode TFTs can have lower device operating voltages and a superior subthreshold response. In the above threshold regime, NS electrode TFTs show enhanced current densities despite have both a smaller carrier injection width and a longer effective channel. Nanospike electrodes reduce the impact of contact resistance on TFT operation, especially for short channel TFTs. The combination of improved gate control and reduced contact resistance provides a viable solution to achieving short channel flexible TFTs that operate at speeds > 1 GHz. While nanospike electrodes are particularly adept at enhancing the behavior of thick dielectric TFTs, the nanospike design is a general method that can be explored to enhance performance in TFTs .

Chapter 7: Subthreshold Advantage of Nanospike TFTs[5]

Nanospike TFTs have source and drain electrodes shaped in the form of an array of sharp spikes with gaps between individual spikes [81], [82], [84], [85]. Such TFTs have several advantages over conventional flat electrode TFTs, as reported by our group in very recent work [81], [82], [84]. These include reduced contact resistance [82], [84], increased on/off ratio, and improved sub-threshold swing. The nanospike electrode geometry is expected to be very useful in reducing the channel length of several TFTs with Schottky contacts to below 100 nm. In such TFTs, contact resistance is usually high and limits the scaling of channel length to increase speed and device density. It is expected to be particularly valuable in back-end-of-line (BEOL) applications such as memories, neuromorphic circuits, etc. that combine the advantages silicon CMOS circuits in the front-end with one or more levels of BEOL circuitry to improve functionality, density, speed, etc. [38], [39].

In this chapter, we describe another important property in nanospike TFTs with many technological benefits. The sub-threshold swing can improve substantially with increasing drain voltage. This leads to very high values for the magnitude intrinsic gain that exceed those of silicon FETs and previous TFTs [86] and also to negative output resistance and gain [87], [88]. Drain induced barrier lowering (DIBL), a common problem in short channel FETs and TFTs, can be greatly reduced through the use of nanospike electrodes. Many of these unusual properties have their origin the formation of charge nanoribbons, under suitable conditions, in nanospike TFTs. In this chapter, very short channel length (50-200 nm) indium gallium zinc oxide (IGZO) TFTs are described;

[5] K. Liang, Y. Zhou, X. Xu, and A. Dodabalapur, "Sub-threshold swing control and very high negative intrinsic gain due to charge nanoribbon formation in nanospike thin-film transistors," (*Submitted*).

however, the effects we describe are applicable to many other TFTs including organic/polymer TFTs and 2D FETs.

CHARGE NANORIBBONS IN NANOSPIKE AMORPHOUS INDIUM GALLIUM ZINC OXIDE TFTS

TFT devices with the schematic structure shown in **Fig. 35** have been fabricated and analyzed to demonstrate the considerable advantages of nanospike-electrode TFTs. These devices feature a global silicon back gate and 90 nm of dry thermal silicon dioxide as the back gate dielectric. Indium gallium zinc oxide (IGZO) has been shown to be an excellent semiconductor for TFTs [41], [53], [59], [60], [67]. IGZO from a target with a composition of Ga_2O_3:In_2O_3:ZnO at a ratio of 1:2:2 respectively was then sputtered followed by an anneal at 450 ºC for one hour, thus forming a 20 nm thick semiconductor layer. The nanospike electrode layer was then patterned using electron beam (e-beam) lithography, aluminum and silver deposited with thermal evaporation, and the e-beam resist lifted off to complete the nanospike electrode layer. E-beam patterning was then performed again to pattern an isolation etch of the IGZO. The IGZO was etched away using a hydrochloric acid (HCl) bath. Further fabrication details are described in Ref. [81]. The nanospike TFTs have channel lengths in the range 50-200 nm, and nearly all the discussion in the chapter is based on L = 100 nm TFTs. **Fig. 35(c)** and **(d)** show the plan view of nanospike TFTs with L = 100 nm and each device features pairs of nanospike source-drain electrodes where each electrode features a 5-spike array. Spreading currents are minimized using two methods: (i) by etching the IGZO along the external perimeter of the devices or (ii) by using side guard electrodes biased at the same potential as the drain electrode to collect spreading currents. Also, shown in **Fig 35(c)** is the schematic charge flow area under low gate voltage and high drain voltage operation indicating the spatial extent of

charge nanoribbons which define the charge flow zones. **Fig. 35(d)** also indicates the charge flow zones at high gate voltage and low drain voltage, when charge flow is more uniform across the entire channel and not restricted to the narrow ribbons as in **Fig. 35(c)**.

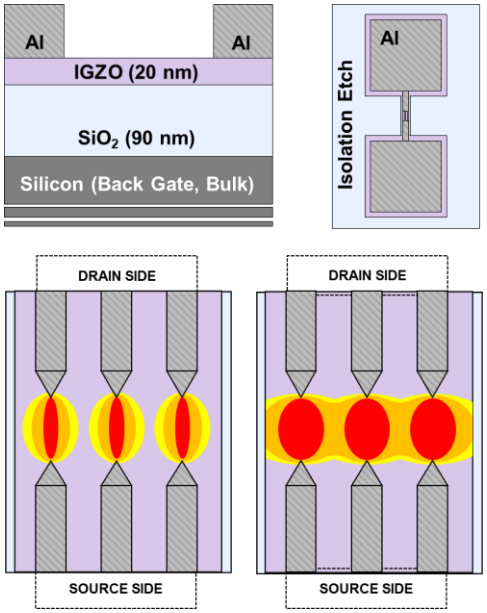

Fig. 35. *IGZO nanospike TFT device structure and schematic. (a) TFT device structure with a silicon back gate, silicon dioxide gate dielectric, IGZO semiconductor, and aluminum top contact electrodes. (b) Schematic of conformal isolation etch of IGZO TFTs to reduce spreading currents. Schematic of carrier concentration distribution of a nanospike TFTs at (c) low gate voltage operation and at (d) high gate voltage operation.*

Charge nanoribbons are expected to form in FETs in which the lateral source-drain electric field is greater than the vertical field due to the gate. The second requirement for charge nanoribbon formation is that charge injection should be restricted to specific regions along the width of the FET or TFT with gaps in between in which no injection takes place. The later condition exists in nanospike TFTs, in which charge injection occurs at and close to the tips of the nanospikes, as shown schematically in **Fig. 35(c)**, and not between the nanospikes. The electric field requirement for nanoribbon formation is met in short channel length TFTs, especially at low gate voltages and large drain voltages. It is also helpful to

have a high ***k*** gate dielectric so that the gate insulator thickness can be relatively large while maintaining a large enough induced charge density. In the TFTs we report, charge nanoribbons are expected for channel lengths of 50 nm and 100 nm as the gate insulator is 90 nm thick. These effects are strongest in the sub-threshold regime, in which gate voltages are small, and get weaker as the gate voltage is increased.

SUB-THRESHOLD SWING CONTROL

The sub-threshold swing in a TFT is given by the equation:

$$S = \frac{dV_G}{d(\log I_D)} \sim 2.3\frac{kT}{q}\ \left(\frac{q^2 N_{it}}{C_i}\right)$$

Where q is the element of charge, *k* is Boltzmann's constant, T is the temperature, N_{it} is the total number of interface traps per unit energy in the device, and C_i is the total insulator capacitance of the device. For uniform channels that do not change shape with bias, as in conventional field-effect transistors, N_{it} is usually replaced by D_{it}, the interface trap density per unit area per unit energy, and C_i is expressed in units of capacitance per unit area. In nanospike TFTs, the channel shape does change with bias, becoming narrower with increasing drain voltage due to charge nanoribbon formation, and the ratio $\frac{N_{it}}{C_i}$ is a function of gate and drain voltage values. As V_D is increased keeping V_G constant, the value of N_{it}, which is directly proportional to the active channel area, decreases as charge flow becomes restricted to nanoribbons between the nanospike electrodes. The value of C_i also decreases, but to a smaller extent. The decrease in C_i is because the gate capacitance changes from a parallel plate type capacitance (as in a conventional TFT) to a microstrip line type geometry when the charge ribbons form.

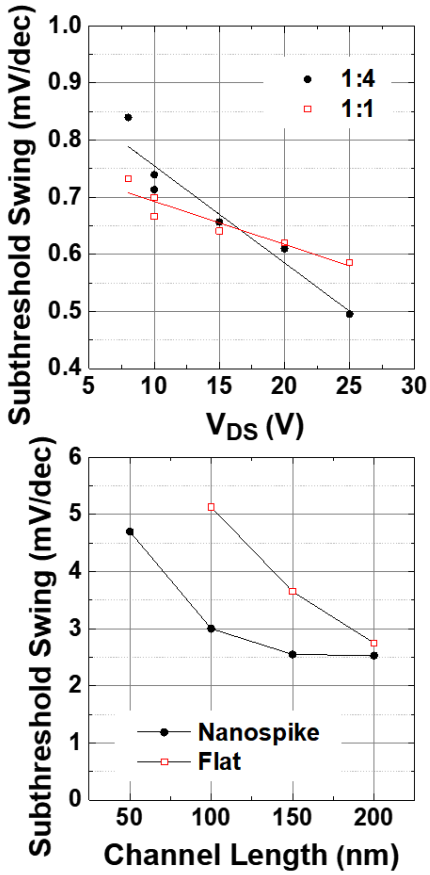

Fig. 36. *Subthreshold swing of various nanospike TFTs and flat TFTs. (a) Subthreshold swing at various VDS for a nanospike TFT with 1:4 spike spacing and 1:1 spike spacing. (b) Subthreshold swing at various channel lengths of a 1:4 nanospike TFT and a flat TFT.*

For the devices with channel length is 100 nm, the channel width per spike (the sum of spike electrode width and the space in between) is 200 nm + 800 nm = 1 µm for 1:4 spacing. For clarity, we will continue this comparison in the case of a single spike device and a flat device with the same gate area. Without charge nanoribbon formation, the value of the gate capacitance is given by the usual parallel plate capacitance formula and is equal to 2.8×10^{-17} F. With charge nanoribbon formation, and assuming that charge flow is along a 200 nm wide region over a gate area of 1 µm width x 100 nm length, the device

capacitance decreases to 1.54×10^{-17} F. These calculations assume that relative dielectric constant of SiO_2 is 3.9 and that a microstrip line model for the capacitance can be used. In this model, the bottom electrode dimensions are very large in comparison with the microstrip (which is a ribbon of charge in this TFT with dimensions 100 nm length x 200 nm width). In these TFTs, the bottom electrode dimensions are 100 nm length x 1 μm width for 1:4 TFTs and the above assumption is reasonable.

Assuming that only interface states in a narrow ribbon width of 200 nm and channel length of 100 nm contribute to the sub-threshold slope reduction, the ratio of N_{it} values for the nanospike geometry to the parallel place geometry is simply 0.2. Thus, the sub-threshold swing, which is given by Eq. 1, will increase by a factor of 2.78 as device operation transitions from purely nanospike mode to conventional parallel plate mode. The observed increase can be seen in **Fig. 36(a)** and is from 0.85 V/decade to 0.5 V/decade, which is an increase by a factor of 1.7, which is less than the theoretical maximum of 2.78 calculated above. This difference is due to the fact that the idealized limits and assumptions on which the calculation is based may not strictly apply. Nevertheless, the experimentally observed large change in sub-threshold swing with drain voltage is a very clear indication that charge nanoribbon effects are playing an important role in device operation. Improvements in sub-threshold swing with increasing drain voltage have never been previously reported for any conventional TFT or FET. Such behavior has been reported for negative capacitance FETs [39].

INTRINSIC GAIN AND OUTPUT RESISTANCE

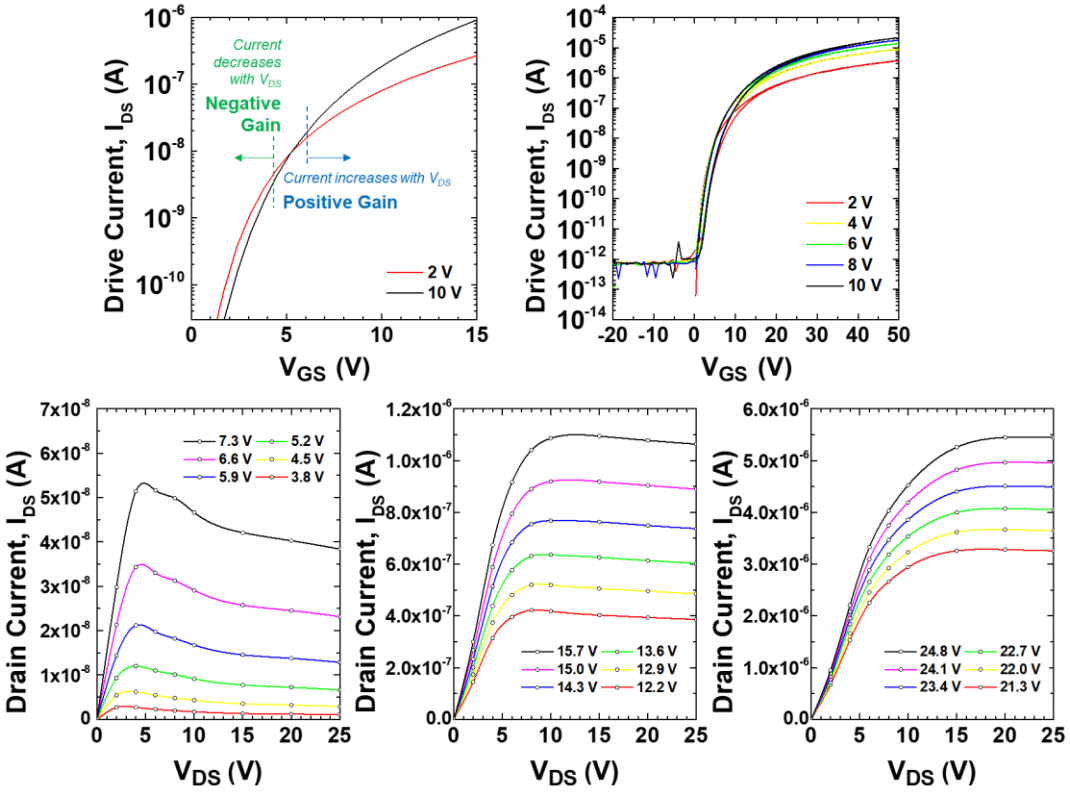

Fig. 37. *Output and transfer curves of 1:4 nanospike TFT. (a) Transfer characteristics showing regions of negative and positive gain. (b) Transfer characteristics of a nanospike TFT at low V_{DS}. (c)-(e) Output characteristics of a nanospike TFT demonstrating negative differential resistance, most visually prominent at low V_{GS}.*

The increase in sub-threshold swing with drain voltage will lead to transfer characteristics measured and shown in **Fig. 37(a)**. From the transfer characteristics, the transconductance, g_m, can be extracted by taking the derivative of the drain current with respect to V_{GS}, as seen in **Fig. 38** for a 1:4 and 1:1 spacing nanospike TFT. It can be seen from **Fig. 37(b)-(d)** that the drain current will decrease with increasing drain voltage when charge nanoribbon effects are significant. This will lead to negative output resistance, which is also observed in experimental data shown in **Fig. 39(a)**. The output resistance

remains negative throughout the sub-threshold region and above threshold, eventually becoming position at high enough gate voltage due to increasing vertical field leading to a widening of the channel dimensions.

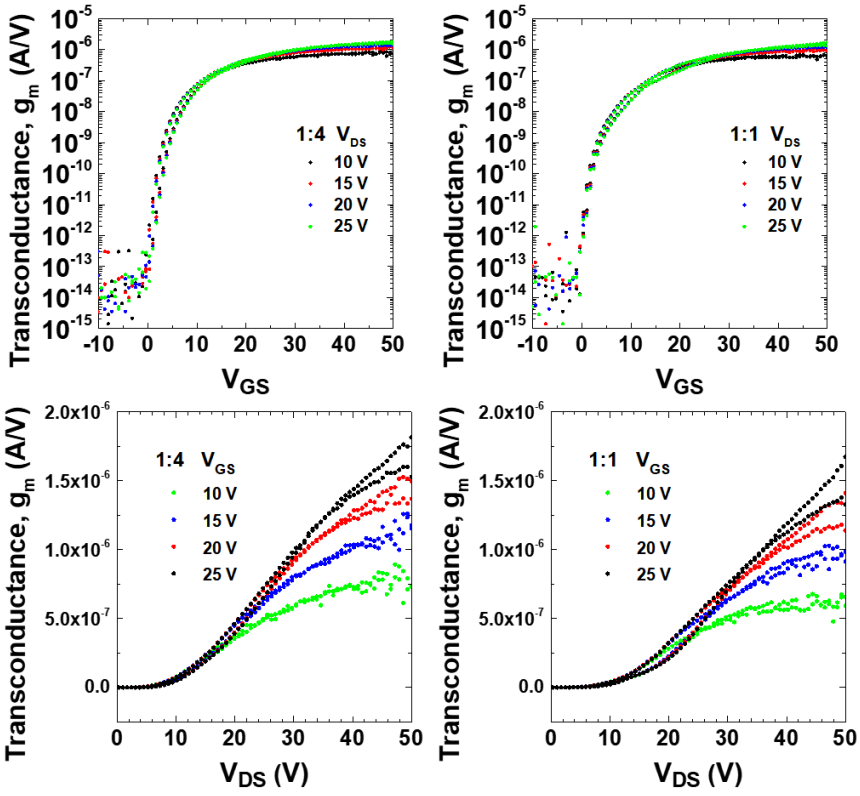

Fig. 38. *Transconductance of various nanospike TFTs. (a) Log-scale transconductance of a 1:4 spacing nanospike TFT. (b) Log-scale transconductance of a 1:1 spacing nanospike TFT. (c) Linear-scale transconductance of a 1:4 nanospike TFT. (d) Linear-scale transconductance of a 1:1 nanospike TFT.*

The ability to reduce DIBL to very low levels will lead to high output resistance values, even in the sub-threshold region. This will result in TFTs that have high intrinsic gain which operate in the sub-threshold region. This will be very useful for very low power circuits including neuromorphic circuits. The intrinsic gain is also very high above threshold and increases until it changes sign and become positive, as shown in **Fig. 39(b)**.

Negative output resistance and gain are very rarely observed in FETs. As noted above, it is only in negative capacitance transistors have been shown to have negative intrinsic gain and DIBL [21], [87]. Negative output resistance can persist even above threshold. In above threshold operation, the intrinsic gain can be very high leading to improved analog circuits and also better performing digital and neuromorphic circuits. The gain can be made positive as well. The device design parameters that control the gate voltage at which the negative gain become positive include the ratio of channel length to gate insulator thickness, the gate insulator dielectric constant (high ***k*** is better), and the spike width to spacing ratio.

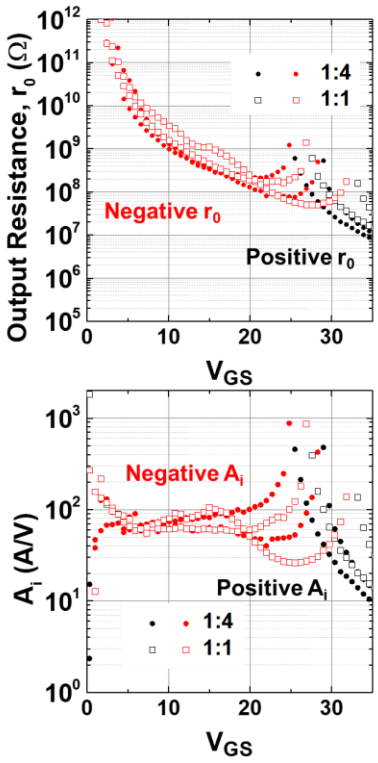

Fig. 39. *Output resistance and intrinsic gain of nanospike TFTs. (a) Output resistance, r_0, of a 1:4 and 1:1 spike spacing TFT at V_{DS} = 25 V, where r_0 transitions from negative to positive around V_{GS} = 30 V. (b) Intrinsic gain, A_i, of a 1:4 and 1:1 spike spacing TFT at V_{DS} = 25 V, where 1:1 has high A_i near V_{GS} = 0 V and both spacing TFTs retain relatively high negative A_i to V_{GS} = 20 V.*

The high intrinsic gain in the sub-threshold region is similar to the characteristics of source-gated TFTs which can possess very high intrinsic gains [88], usually at currents densities that are much lower than for conventional TFTs with the same dimensions and semiconductor [84]. At close to $V_G = 0$, the intrinsic gain magnitude is high and is ~ 200 and compares very well with the record value of 400 reported for L = 20 □m channel length Schottky Barrier (or source-gated) IGZO TFTs reported in the literature [86]. Above threshold, the intrinsic gain magnitude reaches ~ 1000 before the sign changes. In these TFTs, the sign change is triggered by the fact that the TFTs are approaching the linear regime at high V_G. With a thinner gate dielectric, it is possible to get such high intrinsic gains well into saturation and well above threshold. The intrinsic gain well above threshold is substantially higher than those of TFTs reported in Ref. [86].

SUBTHRESHOLD ADVANTAGE SUMMARY

Nanospike TFTs with IGZO active semiconductor layers and channel lengths near 100 nm have sub-threshold swings that change with drain voltage, becoming steeper with increasing drain voltage. This is contrary to most short channel length TFTs in which the subthreshold slope decreases with increasing drain voltage due to DIBL. The output resistance and intrinsic gain magnitudes are very high both in the sub-threshold region and above threshold. The intrinsic gain and output resistance are negative and become positive at high gate voltages well above threshold. Very high intrinsic gains close to 1000 have been measured above threshold. These unusual properties are related to the formation of narrow charge flow zones or change nanoribbons, which become especially important when the lateral electric field is greater than the vertical field, which is the case at high drain voltages and low gate voltages when the channel length and insulator thickness are comparable. These TFTs will be important in future BEOL and other applications.

Chapter 8: Nanospike Conclusion

Nanospike electrodes can be very useful in realizing high-performance TFTs, especially in applications with thick gate insulators deposited by printing and other fabrication methods compatible with flexible electronics. Charge focusing into nanoribbon arrays will enhance local carrier densities and will help achieve higher mobilities and velocities for a given operating voltage, notwithstanding the thicker gate insulator. The design of such a TFT is shown schematically in **Fig. 27(C)**. Compared to flat electrode TFTs, the proposed design will result in better contacts, and better device characteristics. The design will also improve speed by reducing overlap capacitance by increasing dielectric thickness while retaining the drive current and operating voltage. The overlap area and hence the capacitance is also reduced dupe to the spike geometry of the source and drain with gaps between spikes compared to continuous flat electrodes.

The TFT structures proposed in this work have some additional advantages and possible future uses. We have shown the reduction of DIBL-like variation of sub-threshold drain current with drain voltage. This has been hitherto difficult to achieve in short channel TFTs. Indeed, the slope of the sub-threshold region can be controlled by changing the spike width to spacing ratio. With a smaller spacing, or wider spikes, the TFTs will have sub-threshold behavior more similar to those of conventional TFTs with the same channel length. A very small DIBL-like effect means that the current gain in sub-threshold can be quite high, leading to sub-threshold circuits with high current gain and very low power dissipation. Further electric field tailoring of the charge distribution in the channel (for example by using two asymmetric gates) can lead to possible high density quasi-one-dimensional gated conductors.

The frequency response implications of this new TFT geometry needs to be explored. The reduced overlap capacitance (between gate-drain and gate-source) will likely

improve speeds while also providing greater tolerance to mismatches and alignment errors in fabrication. The reduced threshold will enable lower voltage (and lower power) operation. The combination of small channel lengths and relatively thick gate insulators (without short channel effects) will help the field of flexible/printable electronics in which thicker gate dielectrics are more common.

[81], [84], [85]

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