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**The Dissertation Committee for Jeffrey B. Hurst Certifies that this is the approved  
version of the following dissertation:**

**Molecular-Beam Epitaxial Growth of Low-Dark-Current  
Avalanche Photodiodes**

**Committee:**

---

Archie L. Holmes, Jr., Supervisor

---

Joe C. Campbell

---

Sanjay K. Banerjee

---

John G. Ekerdt

---

Leonard F. Register

**Molecular-Beam Epitaxial Growth of Low-Dark-Current  
Avalanche Photodiodes**

**by**

**Jeffrey Byron Hurst, B.S. E.E.; M.S. E.E.**

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## **Dedication**

To my wife, Molly.

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# **Molecular-Beam Epitaxial Growth of Low-Dark-Current Avalanche Photodiodes**

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Jeffrey Byron Hurst, Ph.D.

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Supervisor: Archie L. Holmes, Jr.

The quaternary material system  $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$  is an important material system for optoelectronic devices, specifically covering optimum fiber optic wavelengths. Among the limitations of using this material system concerning photodetector performance is generation of carriers due to material defects and impurities. This dissertation reports on the growth optimization of InGaAs using molecular-beam epitaxy for low-dark-current avalanche photodiodes through the study of the effects of the growth conditions on dark current. An optimum growth temperature of  $545^\circ\text{C}$  and arsenic beam equivalent pressure of  $2 \times 10^{-5}$  Torr was found for producing the lowest dark current density. Avalanche photodiodes were implemented with a dark current density  $80 \text{ mA/cm}^2$  at 90% of the breakdown voltage.

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# **Chapter 1**

## **Introduction**

Applications in optoelectronics for sensing are an important component of today's society. For communication systems, these system components are used for our ever increasing capacity to communicate with one another. In the receiver of an optical communication system, the function of a photodetector is to convert the optical signal sent over optic fiber into an electrical signal. Photodetectors play the same role in sensing and imaging applications for detecting incoming photons. In addition to fiberoptic receivers application for long-wavelength photodetector include low-light detector in 3-D imaging and eye-safe range where wavelengths greater than 1.4  $\mu\text{m}$  are required. Also, very sensitive detectors are needed in optical time-domain reflectometry (OTDR) for the detection of reflected light from faults in fiber optic cable and quantum cryptography where few or even single photons are detected.<sup>1</sup>

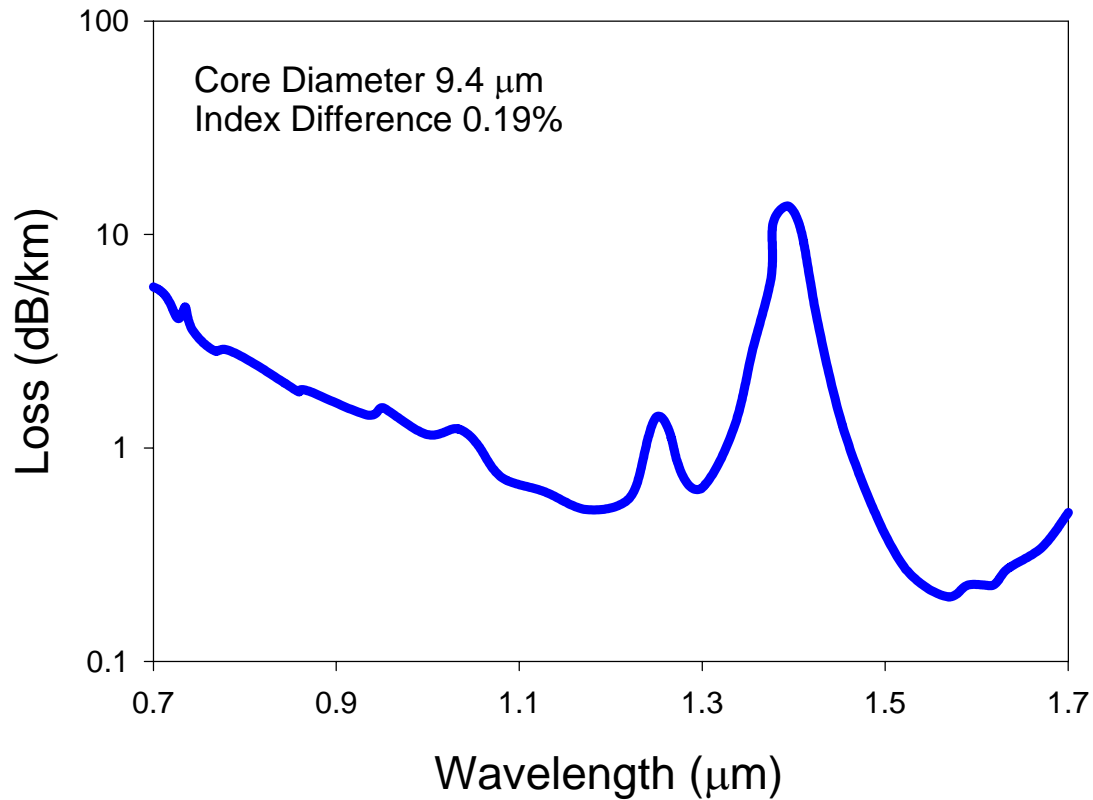
An important parameter in photodetector operation is the dark current which is the contribution to the device current in the absence of light. Dark current degrades the performance of photodetectors by contributing both to the noise of the device. A limit to the detection capability of a photodetector is the detector's noise. This addition noise due to dark current therefore reduces the devices sensitivity.

There are many epitaxy techniques for fabricating thin-film semiconductor materials used in photodetectors such as LPE, MOCVD, and MBE. This dissertation outlines my work

in reducing the dark current in  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  photodiodes. Two main effects have been studied. First, the influence of various MBE growths conditions on the dark current in photodiodes was studied in PIN photodiodes. Second, passivation techniques were studied for achieving low dark current PIN photodiodes by minimizing the dark current due to defect levels at the etched mesa interface. In addition to optimizing the growth and processing of photodiodes for low-dark-currents, separate absorption, charge, and multiplication (SACM) avalanche photodiodes (APD), where  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  is the absorbing layer, were implemented for low-dark-current applications.

## **1.1 PHOTODETECTORS: AN INTRODUCTION**

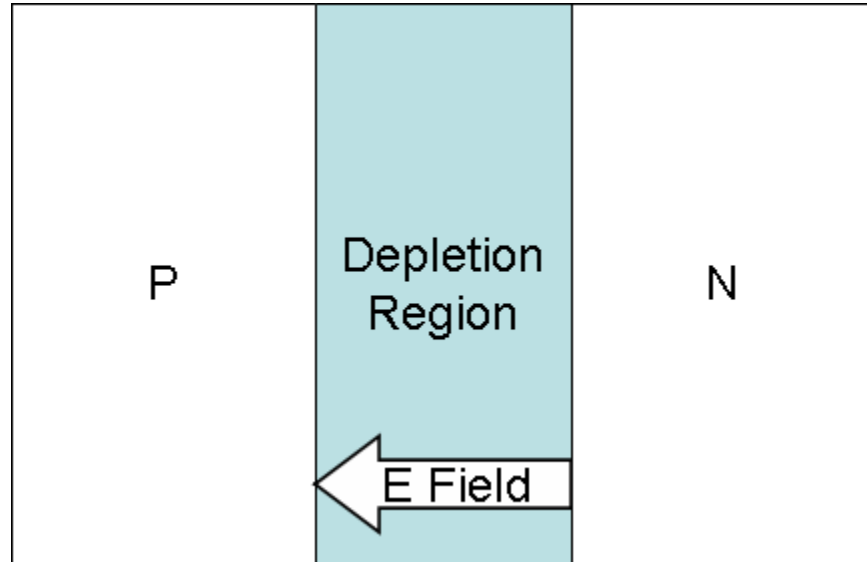
The  $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$  alloy system is important in long-wavelength photodetectors for the 1-2  $\mu\text{m}$  wavelength range. These materials can be grown lattice-matched to InP substrates. By varying the In and As mole fractions, the 1.1-1.6  $\mu\text{m}$  wavelength range can be covered. Especially important are the 1.3  $\mu\text{m}$  and 1.55  $\mu\text{m}$  wavelengths where the dispersion and attenuation minimums, respectively, are located in standard silica fibers, as shown in Figure 1-1.



**Figure 1-1.** Loss in single-mode silica fiber (Adapted from [1]).

A simple photodiode device can be fabricated using either a reverse-biased *pn*-junction or PIN structure as shown in Figure 1-2. In this structure a depletion region is due to the built-in electric field. In this depleted region, electron-hole pairs (EHPs) are created through the absorption of photons that are greater than the band gap generating electron-hole pairs (EHPs). Once EHPs are generated the applied electric field sweeps these carriers from the depletion region where they can be collected to provide a measurable current.

Where weak optical signal are involved and/or an enhanced detection capability is wanted, avalanche multiplication is employed. Additionally, in an APD, the “avalanche” multiplication process is used to provide gain to amplify the measured signal (further explain in section 2.2.1).



**Figure 1-2.** Simple  $p$ - $n$  junction.

## 1.2 SINGLE-PHOTON-DETECTORS: AN EXAMPLE

An example a device application where low dark current greatly affect device performance is in single-photon-detectors. Geiger-mode avalanche photodiodes (APD) allow for the detection of single photons.<sup>3</sup> Without very large gains, these signals cannot be measured. In photon counting APD's the devices are held above the breakdown voltage until an event occurs that results in avalanche breakdown. This event can be caused by either an electron/hole pair (EHP) created by absorbing a photon or by EHPs

generated in the device that contribute to the dark current. Dark count rates, representing the noise of the photon detector, are a measure of the false positives corresponding to avalanche breakdown in absence of light. Dark count rates have been found to be linearly related to the bulk dark current and is given by<sup>8</sup>

$$C_{dark} \approx (\frac{I_{dark,bulk}}{q})P_{ai} \quad (1-1)$$

where  $C_{dark}$  is the dark count rate,  $I_{dark,bulk}$  is the bulk dark current prior to breakdown,  $q$  is the electron charge, and  $P_{ai}$  is the probability that a single charge carrier will cause avalanche breakdown. In order to minimize dark counts it is important to be able to control the material quality to minimize the bulk dark current component.

### 1.3 DISSERTATION ORGANIZATION

This dissertation is organized as follows: Chapter 2 covers the basic theory of APDs including mechanisms responsible for dark current. In Chapter 3, the method for growing the materials used in the photodiodes, MBE, is covered. The measurement techniques employed following material growth for device characterization are then covered. The device fabrication process for mesa photodiodes and subsequent device characterization are then described. Chapter 4 covers the optimization of the MBE growth parameters for InGaAs lattice-matched to InP. The results from these measurements are explained by changes in the mid-gap trap concentrations and energies. Also, results from passivation experiments for minimizing the surface current contribution to the dark current are included. Chapter 5 presents APD device results for



low-dark-currents detectors. Chapter 6 contains a summary of this work as well as directions for future research.

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## **Chapter 2**

### **Theory of Dark Current in Avalanche Photodiodes**

#### **2.1 INTRODUCTION**

In this chapter the basic operation of avalanche photodiodes (APD) is covered including the impact ionization process, basic APD device operation, and components of the current. Following the basics of APD devices is a detailed discussion of deep-level traps, dark current, and trap-assisted generation currents. Finally, the separate absorption, charge, and multiplication (SACM) APD device structure is covered follow by important performance requirements for photodetectors.

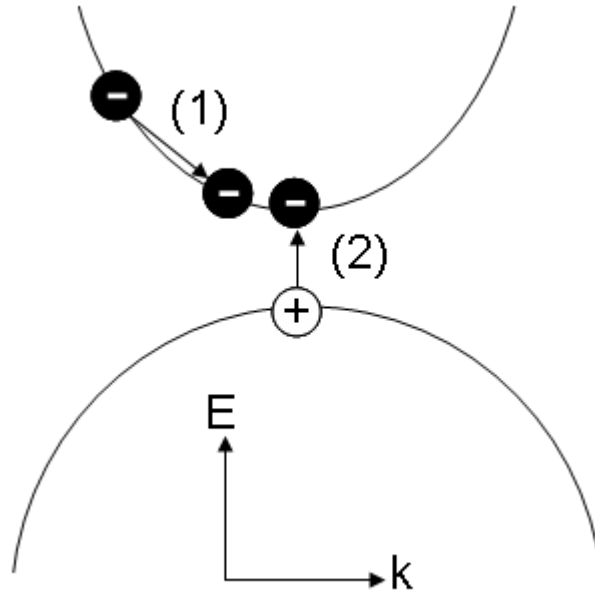
#### **2.2 BASIC OPERATION**

This section includes basic device operation of avalanche photodiodes including basic device characteristics.

##### **2.2.1 Avalanche Breakdown**

Avalanche photodetectors utilize the impact ionization process in order to provide internal gain. Impact-ionization was first studied in  $p$ - $n$  junctions in 1953.<sup>1</sup> Carriers thermally generated as well as those from light absorption can be multiplied by biasing the diode close to the breakdown voltage. Figure 2-1 shows a schematic of the impact ionization process in  $k$ -space. When event (2) occurs, primary carriers with high enough

energy scatter with the atoms in the crystal lattice (1) transferring energy into the formation of secondary carriers as free electron-hole pairs (EHPs, or (2)). This process can be repeated with the further scattering of the secondary carriers as they gain energy from the electric field building up the number of measurable carriers and providing a multiplication gain of the primary carrier current.



**Figure 2-1.** k-space diagram for impact ionization

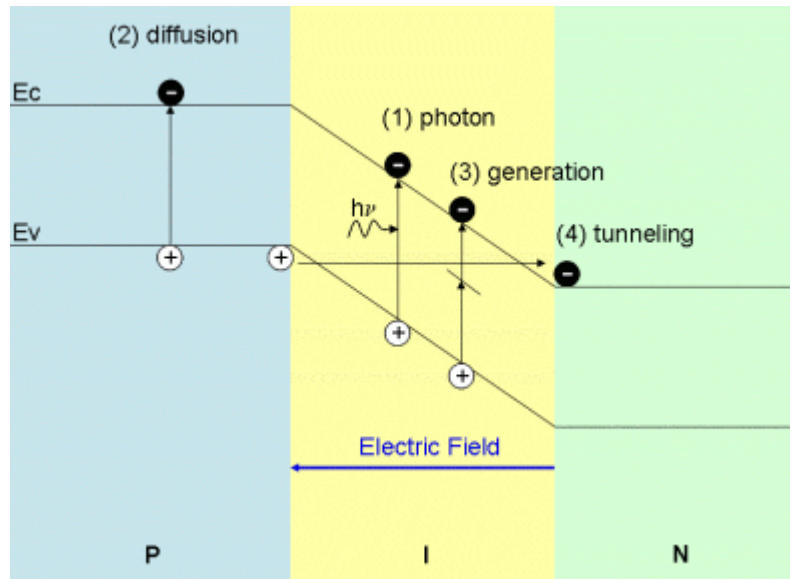
The avalanche gain measured from the device current at a particular bias voltage is given by the following expression,

$$M(V) = \frac{I_{total}(V) - I_{dark}(V)}{I_{total}(V_{unity}) - I_{dark}(V_{unity})} \quad (2-1)$$

Here, the avalanche gain,  $M$ , is expressed as the ratio of the difference of the total dark current and dark current at a particular voltage  $V$  to a voltage prior to the onset of multiplication,  $V_{\text{unity}}$ .

### 2.2.2 Current Components

In a reverse-biased  $p$ - $n$  junction, the four main contributions to the measured bulk current are (1) optical generation, (2) diffusion, (3) thermal generation, and (4) tunneling, as shown for the case of a PIN photodiode in figure 2-2. Electron-hole pairs (EHPs) can be generated by the absorption of a photon with sufficient energy and are quickly separated and collected due to the electric field across the depletion region. In addition to photo-generated carriers, other device current contributing mechanisms add to the total device current.



**Figure 2-2.** Overview of PIN photodiode current components.

Even in perfect crystal lattice broken bonds exist that provide thermally generated electron-hole pairs. Carriers thermally generated outside the depletion region can diffuse into the depletion region and can contribute to the total current. This diffusion current is negligible in well-designed  $p-n$  junctions since the anode and cathode are heavily doped (resulting in very small number of the minority carriers which can diffuse across the depletion region). However, thermally generated carriers within the depletion region are swept apart before they are able to recombine due to the applied electric field. This source of thermally generated carriers is caused by impurities or crystal defects that result in an energy level residing within band gap. This process will be discussed in detail in the next section. When the width of the depletion region is very thin and/or the band gap of the semiconductor is sufficiently small the carrier quasi-Fermi level can overlap. This results in some fraction of the carriers tunneling across the depletion region resulting in a tunneling current under reverse-bias. For InGaAs lattice-matched to InP, with a bandgap of 0.74 eV, tunneling currents dominate above  $\sim 150 \text{ kV/cm}^2$ .

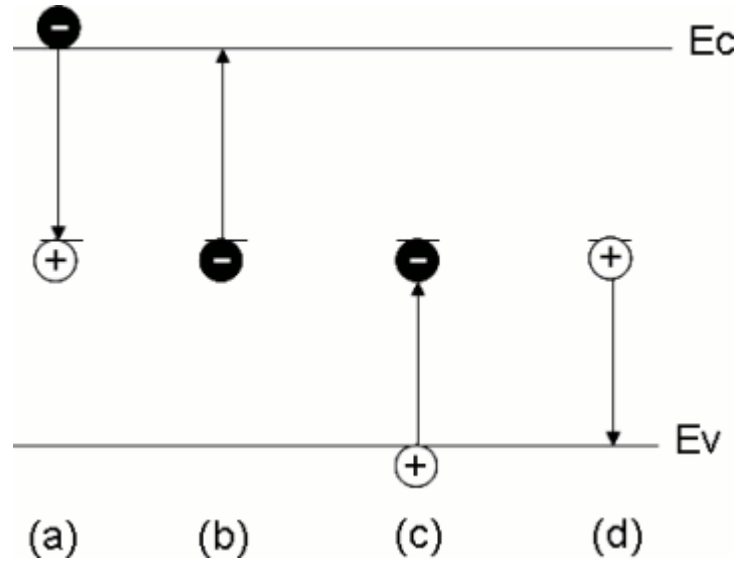
## **2.3 TRAPS AND DARK CURRENT**

The following section details the mechanisms contributing to dark current.

### **2.3.1 Deep-Level Traps**

In a perfect semiconductor no energy levels exist within the band gap. However, with the introduction of impurities and crystal defects, discrete energy levels can form in the band gap. Generally impurities/defects with energies near the middle of the band gap behave as generation-recombination centers while those close to the band edges act as traps. The

processes of electron/hole capture and emission are illustrated in Figure 2-3. Figure 2-3 (a) illustrates the capture of an electron from the conduction band. Once captured the electron can be emitted back to the conduction band (b), or the electron can recombine with a captured hole from the valence band (c). Figure 2-3 (d) shows the analogue to electron emission for holes. In a reverse biased  $p$ - $n$  junction generation process dominate due to the lack of available carriers for recombination in the depletion region.



**Figure 2-3.** Generation-recombination center processes.

Many studies of the  $\text{Ga}_x\text{In}_{1-x}\text{As}$  material system grown on both GaAs and InP substrates have reported a variety of deep level energies.<sup>2-22</sup> Table 2-1 lists reported values for important deep-level activation energies for  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  grown on InP. The traps can lead to generation currents that degrade photodetector performance. As will be seen in Chapter 4, the material quality can be optimized during crystal growth to reduce these effects. Later in this dissertation activation energies,  $E_a$ , are used as a metric for comparison with the trap level energies given in Table 2-1. The activation energies are

extracted from measuring dark currents at a chosen bias voltage and at varying device temperatures and are given by the following equation,

$$I = I_0 \exp(-Ea / 2kT) \quad (2-2)$$

Impurity/Defect	Ea (meV)
<b>Fe</b>	Ec – 300
	Ec – 340
	Ec – 370
	Ec – 440
<b>O-related</b>	490
<b>As<sub>Ga</sub></b>	390
<b>Ti</b>	Ev + 390
	Ev + 270

**Table 2-1.** Deep-levels in Ga<sub>0.47</sub>In<sub>0.53</sub>As. Taken from [3,14,16-18,20]

### 2.3.2 Dark Current Modeling

Dark current is the current measured under reverse bias under dark conditions. Dark current in photodetectors can be split into two primary sources: bulk and surface currents. Bulk dark current is defined by the material properties of the semiconductor material, and is used in this work to compare the material properties of devices from different growth conditions. Surface dark currents are greatly affected by the fabrication process and by how well surface states are passivated; this dark current component is also examined in this work. For mesa photodiodes, these quantities can be separated by their dependence on the etched device diameter,<sup>16</sup>

$$I_{dark} = (\pi d^2)J_{dark} + (4\pi d)K_{dark} \quad (2-3)$$



where  $d$  is the device diameter.  $J_{\text{dark}}$  represent the bulk current component (in units of  $\text{A}/\text{cm}^2$ ), and  $K_{\text{dark}}$  is the surface current component (given in units of  $\text{A}/\text{cm}$ ).

### **2.3.2.1 Bulk Dark Current**

In this work by Forrest et al.<sup>2,21</sup> it has been shown that the bulk dark current in  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  and  $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$  photodiodes has diffusion, generation, and tunneling components. As noted in the last section, diffusion currents are negligible under reverse bias and significant tunneling currents can be avoided by device design and operation. At low biases, generation is the dominant dark current mechanism and can occur from band-to-band and/or trap-assisted processes. The generation-recombination current is given by the following equation,<sup>18</sup>

$$I_{G-R} = (qn_iAW / \tau_{\text{eff}})[1 - \exp(-qV / 2k_B T)] \quad (2-4)$$

where  $n_i$  is the intrinsic carrier concentration,  $\tau_{\text{eff}}$  is the effective carrier lifetime,  $W$  is the depletion layer width, and  $V$  is the reverse bias voltage. This representation of the generation-recombination currents assumes thermally generated carriers assisted by recombination centers are located at mid-gap. Mid-gap traps are the most efficient recombination centers. From equation 2-4, we can identify several strategies for minimizing the dark current. First, reducing the depletion layer volume by reducing the device diameter and depletion thickness will result in a smaller generation current, but will also reduce the quantum efficiency. Second, dark current can be reduced by improving the material quality, which increases  $\tau_{\text{eff}}$ . Also, operating photodiodes at lower temperatures will lower the intrinsic carrier concentration which has the temperature dependence,<sup>22</sup>

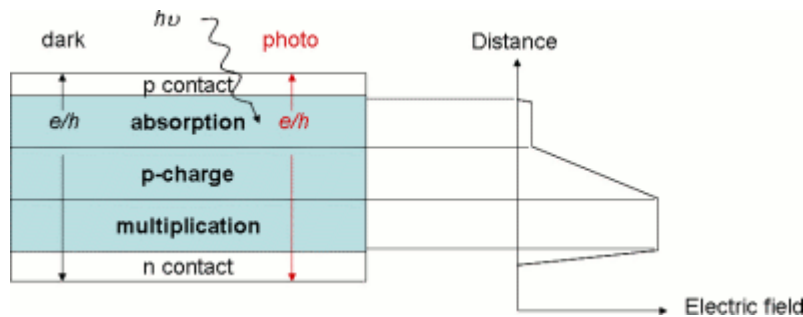
$$ni = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2} (m_n^* m_p^*)^{3/4} \exp\left(\frac{-E_g}{2kT}\right) \quad (2-5)$$

But lowering the device operating temperature results in added complexity of device design, such as the addition of TE cooling. Also, as can be seen from equation 2-5, using a larger band gap material will result in lower dark current. Because an increased band gap limits the lower detection wavelength of the detector, this method is limited by the working wavelength(s).

### 2.3.2.2 Surface Current

As stated earlier another source of dark current is surface recombination. In mesa diodes, the etched sidewalls contain dangling bonds which can act as generation-recombination sites for carriers. In order to minimize this current a passivation layer, such as SiO<sub>2</sub>, is typically deposited that reduces the number of dangling bonds. In order to separate the surface current contribution from the bulk, experimental data was fit with equation 2-3.

## 2.4 SACM DEVICE STRUCTURE



**Figure 2-4.** Basic SACM device Structure

For long-wavelength applications, the separate absorption, charge, and multiplication (SACM) device structure has been used widely.<sup>23</sup> Figure 2-4 shows a schematic of this structure along with a qualitative electric field profile. Tunneling is a concern for the small bandgap absorbing layer. For example, in InGaAs, tunneling currents dominate at relative low electric fields ( $\sim 190$  kV/cm) compared to typical multiplication layer breakdown field for AlInAs and InP,  $\sim 400$  kV/cm. In order to avoid tunneling, a charge layer is employed between the absorption and multiplication layers with a sufficient doping level to reduce the electric field in the absorption layer to avoid tunneling yet provide enough potential energy for the carriers to be injected into the multiplication region where avalanche gain is provided.

## **2.5 PERFORMANCE REQUIREMENTS**

There are several important parameters photodetectors have to meet given the device application. First is the operating wavelength. Because of the minimum in dispersion and attenuation at  $1.3\ \mu\text{m}$  and  $1.55\ \mu\text{m}$  in fiber optic cable, these wavelengths are standard for fiber optic communication systems. The quantum efficiency is a measure of how effective photons of a certain wavelength are collected by the device and can be improved by increasing the effective thickness of the absorption region. However, increasing the absorption region thickness also region in larger dark currents.

Speed is also an important parameter for photodetectors, and is related to how quickly carriers can be collected. Generally, small absorption layers thicknesses are used for high-speed devices where the time it takes for carriers to traverse the device is small in addition to reducing the RC time constant.<sup>23</sup>

A measure of the sensitivity of photodetectors is the responsivity, defined as the current generated by a unit incident optical power, given in A/W. Increasing the absorption layer thickness increases the number of photons absorbed and therefore increases the responsivity. Also unlike PIN photodiodes, APDs have an internal gain resulting from the extra carriers generated through impact ionization. This results in a greater sensitivity.<sup>24</sup>

Signal-to-noise is also an important parameter. In a PIN photodiode the noise consists of both shot noise, which arises from random arrival time of individual carriers, and thermal noise, due to the random motion of carriers across the equivalent receiver input resistance. In APD devices, additional noise is present resulting from the non-deterministic behavior of the avalanche process of which noise due to dark current is a component.<sup>25,26</sup>

Additionally, for single-photon-counting applications the dark count rate, a measurement of photon events in the absence of light, is also an important device parameter as described in section 1.2. Dark count rates depend on the operating conditions of the device and the material quality. Less generation current, primarily through mid-gap traps, result in lower dark count rates. Also, a larger excess bias over the breakdown voltage leads to an increased amount of dark counts.<sup>27</sup> For single-photon-counting application, dark count rates less than 100 cps are desired.<sup>28</sup>

## **2.6 SUMMARY**

In this chapter the basic device characteristics of APDs were covered as well as contributions to photodetector dark currents. Both the noise and sensitivity parameters of photodiodes can be improved by lowering the dark current. Dark current can be lowered through the optimization of the material quality, device operation, and device structure. Because dark current is a combination of bulk and surface currents, the bulk contribution is used in this dissertation as the target parameter for monitoring the effects of the growth conditions.

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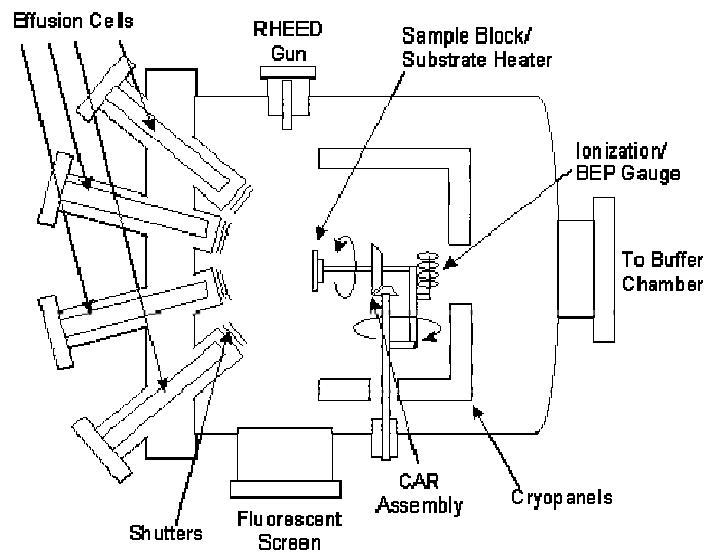
## **Chapter 3**

### **Experimental Methods**

#### **3.1 MBE GROWTH**

Molecular beam epitaxy (MBE) is a special evaporation technique developed by A.Y. Cho in the 1970's that precisely controls the beam fluxes and deposition conditions of materials under ultrahigh-vacuum conditions.<sup>1,2</sup> Low growth rates combined with shuttered sources allow extreme control of material composition and doping in layered structures and sharp hetero-junction interfaces. High quality semiconductor thin films can be grown using MBE, capable of controlling the composition at the atomic level. InP and GaAs based semiconductors are the most mature III-V material systems, with  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  being the most studied material system because of its use in heterostuctures lattice-matched to GaAs substrates. Fiber optic wavelength optoelectronics are primarily grown on InP substrates because of the In(Al, Ga, As)P material system with InGaAs grown lattice matched to InP substrates with a band gap of 0.75 eV.

### 3.1.1 System Overview



**Figure 3-1.** MBE Chamber schematic (copied from ref 3).

For this work, we used a Varian Gen II MBE system. The MBE system at the University of Texas at Austin (which we call the "Phosphide System") is equipped with three group-V valved crackers: two Applied EPI Mark IV arsenic and phosphorus 500cc valved crackers and an Applied EPI corrosive series antimony valved-cracker. Additionally, group-III sources consist of Al, Ga, and In 60cc Knudson effusion sources and a combo Be/Si dopant source for p-type and n-type doping, respectively. Also, the "Phosphide

System” consists of a load-lock (LL) chamber, buffer chamber, and growth chamber to maintain the integrity of the vacuum environment in the growth chamber.

### **3.1.2 Sample Preparation and Loading**

The following describes the normal operation for crystal growth on the “Phosphide System.” A careful procedure is used to maintain the integrity of the vacuum in the chamber by minimizing the introduction of impurities.

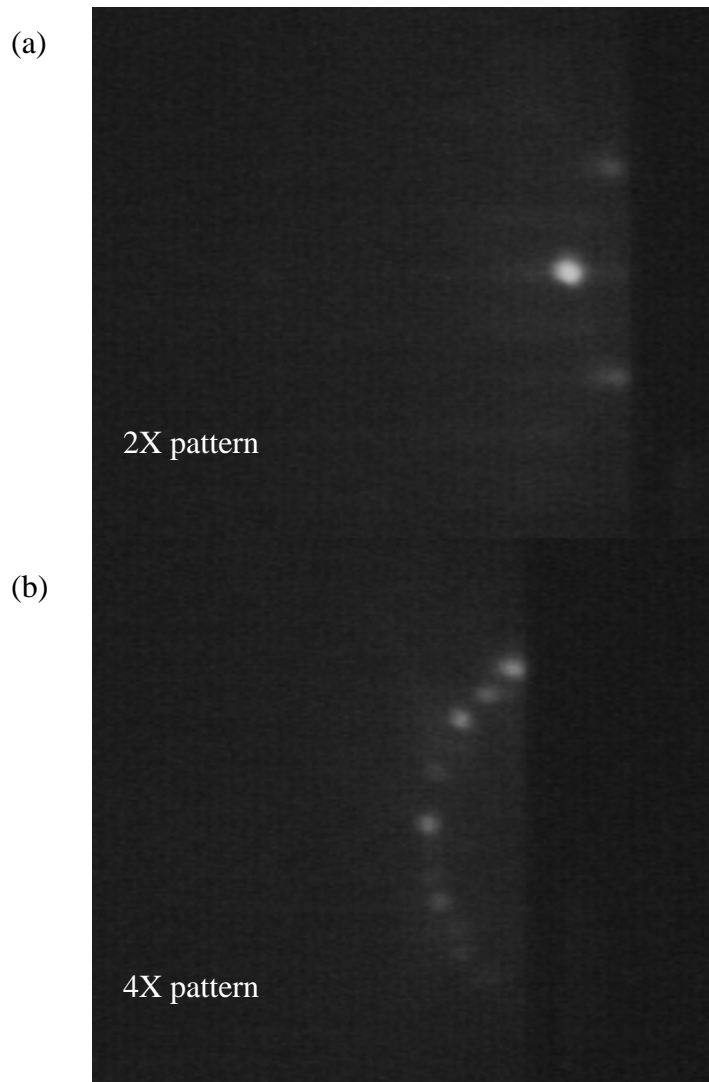
Wafers are first cleaved and then mounted onto molybdenum block using indium while heating on a hotplate. Next, the blocks are loaded into the LL where the samples are outgassed at 120°C while being pumped with a turbo-molecular pump. This is typically done the day before a growth is planned to ensure the sample have been thoroughly outgassed. Once the LL has reached  $1\text{-}2\times 10^{-8}$  Torr, the samples are transferred to the buffer chamber where further outgassing is performed by placing the block on a heater station while this chamber is pumped with an ion-pump. GaAs wafer are outgassed at ~400°C ,and InP are outgassed at ~300°C where the temperatures used are to ensure that As/P desorption is minimal. This step is performed until the buffer pressure falls below  $\sim 5\times 10^{-8}$  Torr.

After outgassing in the buffer chamber the sample are loaded into the growth chamber where the samples are placed on the continual azimuthal rotation (CAR) manipulator. On the CAR the samples are heated and rotated during crystal growth. An ion gauge located on the back of the CAR is used to measure the growth chamber pressure when pointed away from the sources and source beam equivalent pressure (BEP) when positioned facing the sources. Reflection high-energy electron diffraction (RHEED) is used to

calibrate the growth rates and monitor pattern transitions for removal of oxide (i.e., “de-ox”). A thermocouple on the CAR heater, along with optical pyrometry, is used to control the growth temperature. Computer controlled shutters and automated valve-positioners are used to control the fluxes from the sources during growth.

### **3.1.3 Growth Temperature Calibration**

Because temperature control of the substrates is an important parameter in this work, accurate temperature control is necessary. Temperature control of the substrates during growth is maintained by temperature measurements on a thermocouple mounted on the BN substrate heater. This temperature is typically 120°C hotter than the actual substrate temperature and varies ~10°C between calibration de-oxidations. The substrate temperature is measured using IRCON Modline 3 V3 infrared optical pyrometer capable of measuring temperatures down to 400°C. The emissivity of the pyrometer is set by a calibration de-oxidation during the careful monitoring of the removal of the surface oxide of GaAs epi-ready substrates such that the pyrometer temperature to 580°C.<sup>4</sup> GaAs oxide desorption is used as a temperature calibration point rather than InP because of the clear transition in RHEED from no pattern to observable 2X and 4X patterns. For InP substrates the removal of the surface oxide occurs at ~550°C under and arsenic overpressure.



**Figure 3-2.** (a) 2x and (b) 4x RHEED patterns on GaAs

GaAs substrate surface oxide removal is monitoring by RHEED. Before the surface oxide is removed the RHEED show a hazy pattern. The substrate temperature is slowly increased in 5°C increments with 5 min soaks close to “de-ox.” While heating the substrates the As BEP is set to  $6 \times 10^{-6}$  to prevent As-desorption. Once a distinguishable pattern observed the wafer is considered “de-oxed.” The wafers are then increased by 30

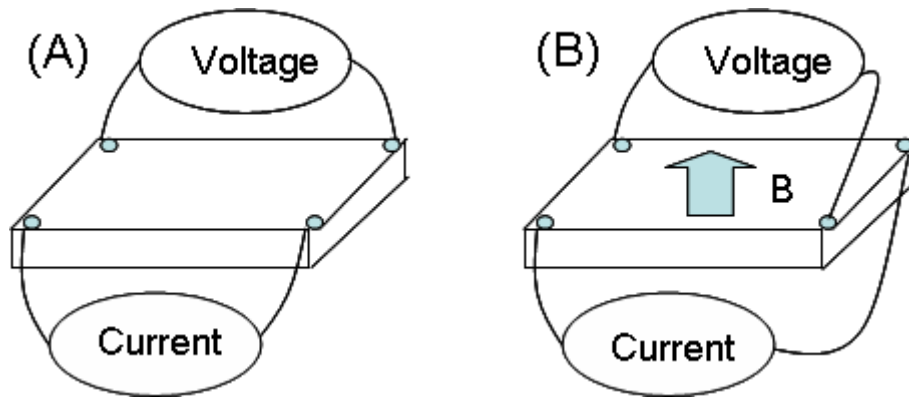
°C to ensure all of the surface oxide is removed. Once “de-oxed” the wafers show exhibit the 2X and 4X RHEED pattern (Figure 3-2).

For InP substrate the manufacturers, AXT, “de-ox” schedule is followed. The InP substrate are ramped from 400°C at 25°C until the 2X → 4X transition occurs. When “de-oxing” under an As-overpressure a BEP of  $1.5 \times 10^{-5}$  Torr is used and the transition occurs at ~550°C (for P-BEP,  $8 \times 10^{-6}$  Torr, 470°C). Once the “de-ox” temperature is reached the wafers are lowered to the growth temperatures.

### 3.2 MATERIAL CHARACTERIZATION

After MBE several characterization technique are used to characterize the material. The following sections describes the measurements used for this work.

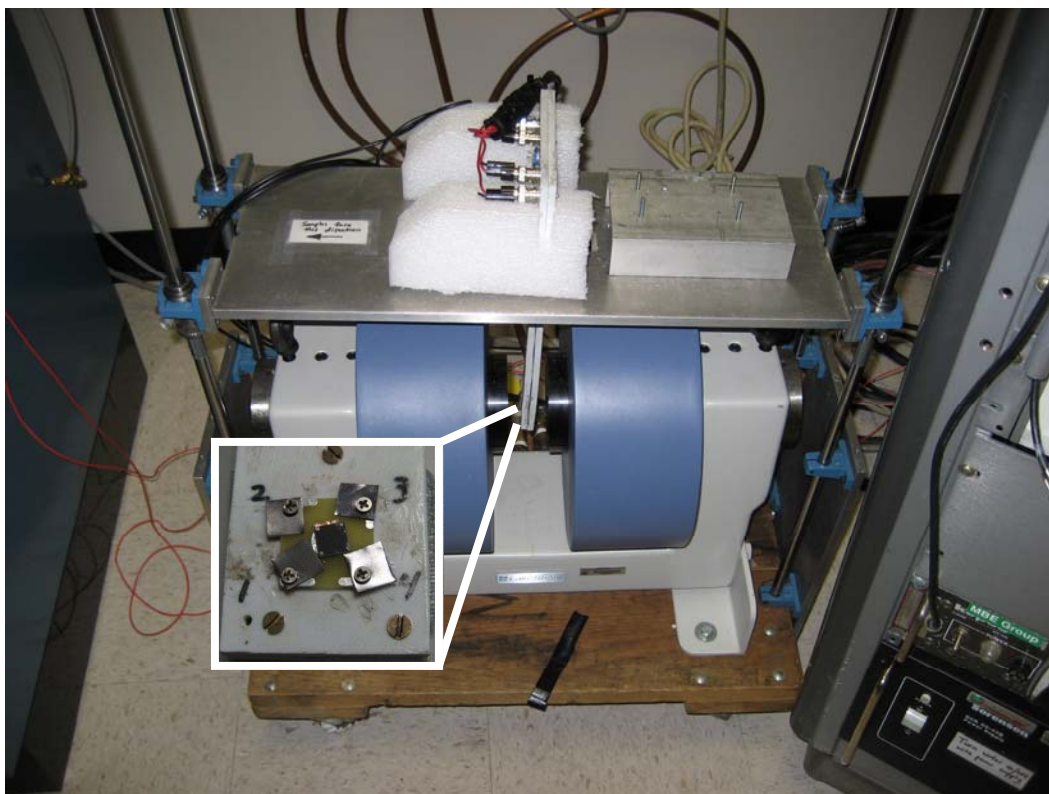
#### 3.2.1 Hall Effect



**Figure 3-3.** van der Pauw configuration showing (A) resistivity measurement and (B) Hall voltage measurement.

Hall measurements were used in this work as a method of determining dopant concentrations and can be used for determining material quality through the measurement of carrier densities and mobilities. Unintentionally doped layers include electrically active carrier concentrations due to impurities and lattice defects which also reduce the mobility of carriers through scattering mechanisms. These measurements used the van der Pauw configuration shown in Figure 3-3.<sup>5</sup> 1.5 cm x 1.5 cm samples were cleaved, and indium pieces were placed on the corners and annealed at 450°C for 30 sec to fabricate Ohmic contacts. Next, they are placed in a sample holder that positions the samples in a magnetic field (inset of Figure 3-4). Typical fields used for these experiments are 1-5 kGauss. Once measured the resistivity, activated carrier concentration, and Hall mobility are calculated given a sample thickness. For calibration of n- and p-type doping levels curves carrier concentration vs. dopant cell temperatures are measured. Typically after a set of data points have been measured for a dopant cell only one hall sample is grown periodically to calibrate any drift in doping levels. This is because the slope of doping concentrations versus cell temperature has been found to remain constant enough that only one measurement is needed periodically to update the doping curves.





**Figure 3-4.** Hall measurement setup.

### 3.2.2 X-Ray Diffraction (XRD)

XRD measurements were used along with RHEED oscillations to calibrate material composition and growth rates. Omega-2theta ( $\omega-2\theta$ ) scans were performed on a Phillips X'pert X-ray System. Figure 3-5 shows a standard layer structure grown for calibrating InGaAs and InAlAs, consisting a 3-layer calibration sample. RHEED oscillations were monitored to calculate the total growth rate for each layer, while XRD measurements provided compositional information. Bede RADS Mercury simulation software was used to model the growth structure. Composition results from x-ray simulations were then

used to adjust growth rates by changing cell temperatures to achieve the desired growth rate.

InGaAs
InAlAs
InGaAs

**Figure 3-5.** X-ray calibration structure.

### **3.2.3 Atomic Force Microscopy**

AFM measurements were performed on a Digital Instruments AFM with Sb-doped Si cantilevers. For determining surface roughness  $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$  scans were performed and were used as a possible method of correlating with material quality and dark current as reported by others.<sup>6</sup>

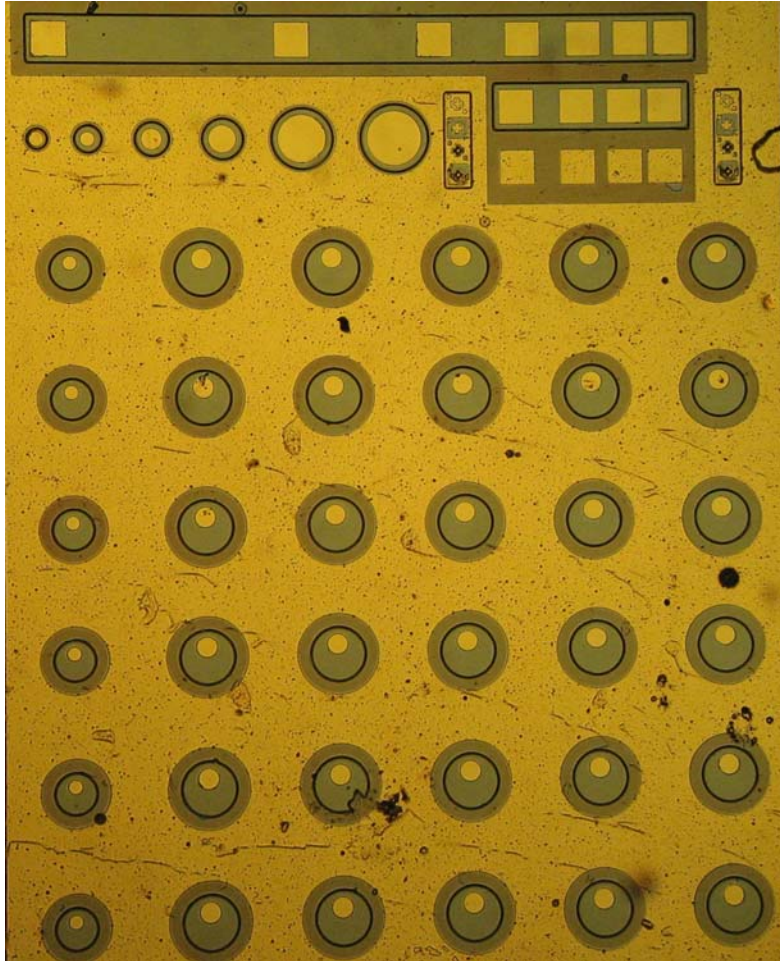
### **3.2.4 Photoluminescence**

Photoluminescence (PL) measurements were used both for verifying composition and for a metric for material quality. Typically, the lower the non-radiative recombination lifetimes the larger the intensity measured from PL. PL measurements were measured using a Coherent Sabre laser set a wavelength of 535 nm as a light source and LN cooled Ge detector located at the output of a spectrometer. The Triax-180 spectrometer contained a grating blazed for 1mm and was 600 grooves/mm.

### **3.3 DEVICE PROCESSING**

The “noise” mask set provides a basic mask set for the quick characterization of device. This set includes device of different diameters (60-200 mm) which were used for dark current measurements for the optimization of InGaAs MBE growth (Chapter 4). For processing small area devices, the “photon counting” mask was used which includes the use of air bridges for electrical contacts.

### 3.3.1 Basic mesa processing (Noise Mask)



**Figure 3-6.** Basic mesa devices after processing.

The following is the basic photodiode processing procedure follow for fabricated mesa devices from 60-200  $\mu\text{m}$  in diameter (Figure 3-6).

### *Step 1 Top Metal Contact*

The first step is a thorough cleaning in acetone/methanol/de-ionized (DI) water. Standard contact lithography is then used for patterning. This consisted of AZ5209 resist spun at 4 krpm for 40 sec. Then the wafers are soft-baked on a hotplate for 2 min at 90°C. Contact lithography on Karl Suss 579 is used to define the top contact, and then the sample is developed in AZ726 for ~30 sec. Before loading in the metal evaporation chamber, the wafer is dipped in buffer-oxide etchant (BOE) for 10 seconds to remove any surface oxide. For p-type top contacts, 20 nm Cr and 800 nm Au was deposited. After unloading the samples, they were submersed in acetone in then place in an ultrasonic agitator for metal liftoff and rinsed with methanol and DI water.

### *Step 2 Mesa Etching*

For InP-containing materials 200 nm of SiO<sub>2</sub> is first deposited as an etch mask in an Oxford PECVD chamber. Standard contact lithography is used again to define the device mesas. If an SiO<sub>2</sub> mask is used, an etch is performed with BOE for 1 min 15 sec, solvent clean, and then the mesas are etched in bromine/methonal at an etch rate of ~0.5 µm/min. Otherwise, after hard-baking the samples at 120°C for 20 min, an etchant of 1 H<sub>3</sub>PO<sub>4</sub> : 1 H<sub>2</sub>O<sub>2</sub> : 1 H<sub>2</sub>O is used to etch mesas at an etch rate of ~0.5 µm/min. Etch rates are monitored using a profilometer.

### *Step 3 Passivation*

Immediately after etching the mesas the PR is removed by an ultrasonic treatment followed by rinsing with methonal and DI water. If an oxide mask was used it is removed by etching in BOE for 1.5 min. Then the samples are quickly loaded into the

PECVD chamber where 200 nm of SiO<sub>2</sub> is deposited as a passivation layer. The conditions of deposition are 180 sccm N<sub>2</sub>O, 36 sccm SiH<sub>4</sub>, 900 mTorr, and 30 W.

#### *Step 4 Bottom Metal Contact (Optional)*

Standard contact lithography is again used for defining the bottom contact. After developing the PR, a BOE etch for ~1.5 min is performed to remove SiO<sub>2</sub>. Then 20 nm AuGe/ 10 nm Ni/ 80nm Au is deposited to for the bottom n-type contact.

### **3.3.2 Passivation Experiments**

When processing devices, impurities and defects are introduced by etching and other processing steps. Passivation is important to reduce surface recombination due to dangling bonds, impurities, and other defects on the mesa sidewalls. Passivation layers other than SiO<sub>2</sub> were investigated including polyimide, S-passivation with an H<sub>2</sub>SO<sub>4</sub> dip, and no passivation were investigated in addition using SiO<sub>2</sub>.

For passivating mesa sidewalls with polyimide, a process was developed to reliable pattern devices. The light sensitive components of polyimide are very sensitive to the chemical's age and instead of adjusting the development and exposure step, polyimide was patterning after curing step. The following recipe was used:

#### *Step 1 Top contact*

Standard lithography and metal lift-off for depositing the top contact.

#### *Step 2 Clean*

An ultrasonic clean in acetone is performed followed by acetone/methonal/DI water rinsing. Then the wafers are baked at 150°C for 2 min.

#### *Step 3 Polyimide spin and cure*

The wafer are coated with HD4000, at RT, first for 10 sec at 1000 rpm and then 60 sec at 5000 rpm. Then the wafers are baked on a hotplate 100°C for 2 min. The wafers are then loaded into a furnace and are cured at 350°C for 1 hr in a N<sub>2</sub> atmosphere. Then the wafers are loaded for metal deposition and are coated with 20 nm of Ti.

#### *Step 4 Mesa Lithograph*

Standard mesa definition and etch process.

#### *Step 5 Mesa etch*

After the mesa have been defined with PR the Ti is etched in BOE for ~1.5min. Next, an O<sub>2</sub> plasma etch is used to remove the polyimide (Oxford RIE, 100sccm, 200W, 40min). Finally, the wafers are cleaned is acetone/methonal/DI water, and then the remaining Ti is removed with a BOE etche for ~1.5 min.

#### *Step 6 Bottom Contact Metallization & Liftoff*

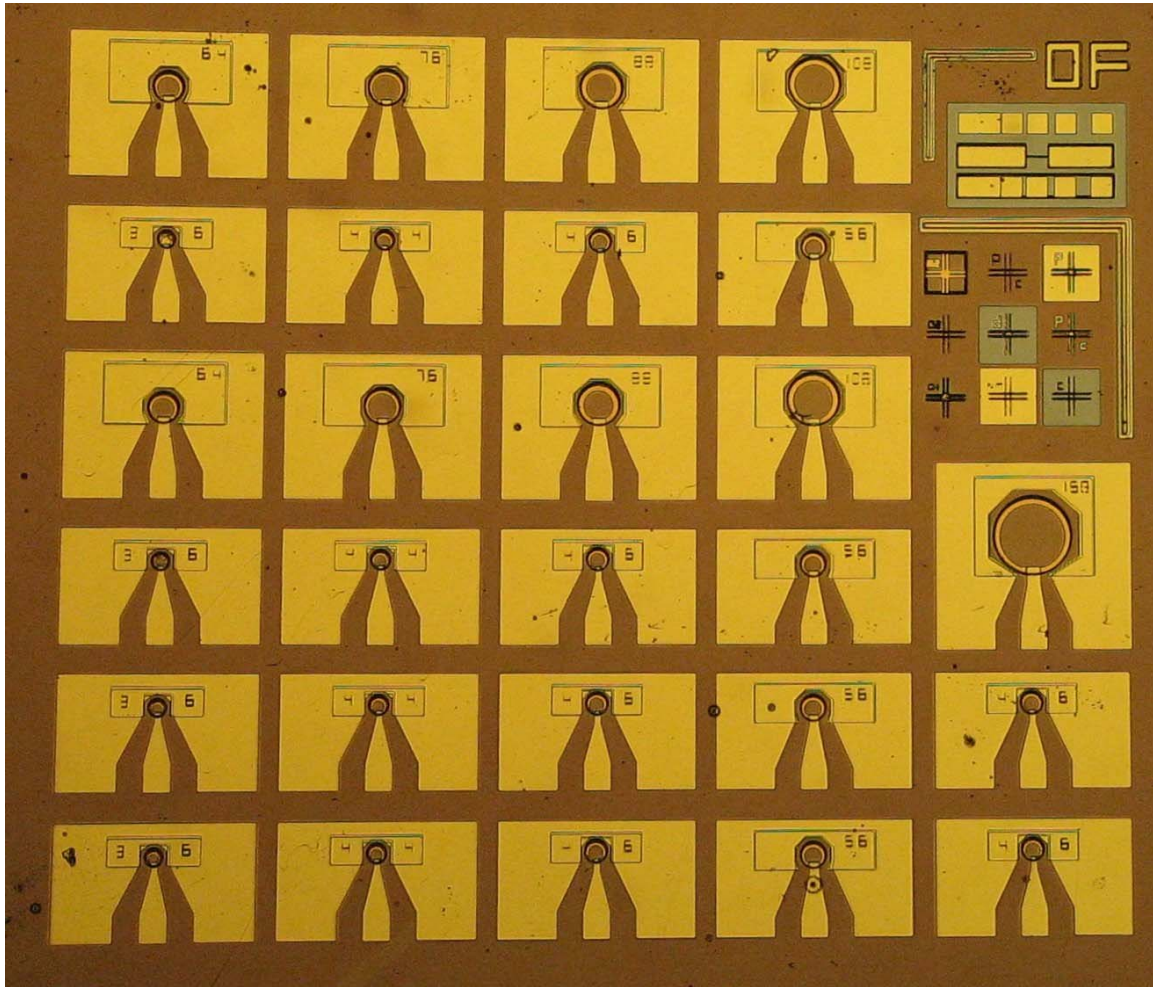
Standard contact formation is performed as described above.

### **3.3.3 Low-dark-current APD processing (Photon Counting Mask)**

In fabricating devices for photon counting, or other low-dark-current applications, smaller device diameters are used than those in the basic mesa mask set. The photon counting mask set consists of devices from 36-108 μm in diameter. Ring contacts are



used for the top contact, which allow the light to pass through the center of the device. These small contacts are too small to probe with conventional probe tips, so air bridges are used to provide a large top contact metal pad as show in Figure 3-7 below.



**Figure 3-7.** Devices patterned using the photon counting mask showing the n-contact pad (larger) and p-contact pad (smaller). The p-contact pad is connected to the top ring contact via air bridges.

The processing recipe used for the photon counting mask set is listed below, noting only deviations from the basic mesa processing recipe.



### *Step 1 Top Metal Contact*

Standard metallization process for defining and depositing the top metal layer is performed.

### *Step 2 Mesa Etching*

For device structures that cannot be etched with a wet etchant because of too large side-etching a dry etch was used. The etch was performed in a Oxford RIE chamber, and the conditions of the plasma were 20 sccm CH<sub>4</sub>, 70 sccm H<sub>2</sub>, 45 mTorr, and 150 W. The etch rate on this equipment was found to vary from day to day (0.015 – 0.4 μm/min), so before each etch a test wafer was used to calibrate the etch rate. After deposition, a polymer forms as a byproduct of the plasma, so an O<sub>2</sub> etch is performed for 5 min at 100 sccm, 100 W, and 50 mTorr to clean the chamber and wafer surface.

### *Step 3 Passivation*

Standard deposition of SiO<sub>2</sub> passivation layer.

### *Step 4 Open n and p Contacts*

After standard contact lithography, a BOE etch for ~1.5 min is performed to remove SiO<sub>2</sub> from the contact layers.

### *Step 5 Bottom Metal Contact*

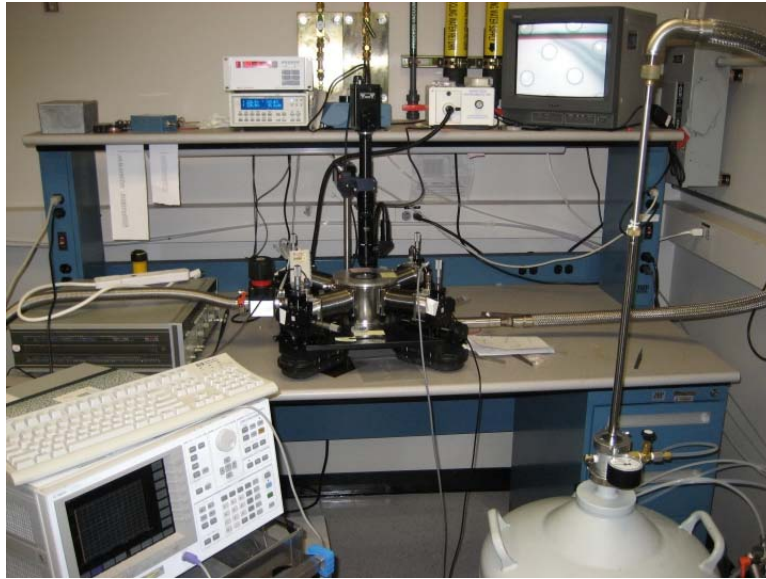
Same as for basic mesa processing except oxide removal using BOE was already performed in step 4.

### *Step 6 Air Bridge*

After defining the contact pad with standard contact lithography, 10 nm Ti and 40 nm Au is deposited. No metal lift-off step is performed before the next lithography step is used to define the air bridges. The sample is then submersed in Microfab AU-100 while heated on a hotplate to 80°C. Au-electroplating is performed for ~20 min using a current source at 2 mA/3 V limit, resulting in a ~2  $\mu\text{m}$  Au deposition. Finally, an ultrasonic clean with acetone is performed for metal liftoff.

## **3.4 DEVICE CHARACTERIZATION**

Room temperature IV measurements were taken using both HP 4145B and an Agilent 4155C semiconductor parameter analyzers. For low temperature IV characterization the wafer are loading into a cryoprobe station (from Desert Cryogenics) that is pumped to  $\sim 5 \times 10^{-4}$  Torr. Thermal contacts are made to the LN-cooled chuck with silicone thermal compound to ensure the device temperature was equal to the chuck temperature.



**Figure 3-8.** Cryoprobe station setup used for low temperature IV measurements.

CV measurements were performed on both an HP4275A LCR meter. These measurements were typically performed as another measurement to monitor charge layer doping and also to monitor the intrinsic layer thickness.

### **3.5 SUMMARY**

In this chapter, the techniques used for crystal growth and for device processing and characterization were covered. In order to quickly process and characterize material, the basic mesa process was followed. This process was also used as the basis for the growth condition experiments covered in the next chapter. Once material was characterized and smaller devices were to be fabricated, the single-photon-counting mask along with a slightly more complicated process flow was followed.

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## Chapter 4

### MBE Growth Optimization of InGaAs

#### 4.1 DEVICE STRUCTURE AND EXPERIMENTAL APPROACH

In order to investigate the effects of the growth conditions on measured dark current in InGaAs latticed-matched to InP, "test" PIN's were fabricated. The device structure consisted of 800 nm-thick intrinsic region InGaAs homojunction photodiode grown on n-InP substrates, shown in Figure 4-1. This simple photodiode structure was chosen so that the growth effects on dark current for InGaAs could be studied separately from other material influences.

<b>Cr/Au p-contact</b>
30nm p+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
500nm p $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
800nm u.d. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
800nm n+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
n-InP substrate
<b>AuGe/Ni/Au n-contact</b>

**Figure 4-1.** Test PIN structure.

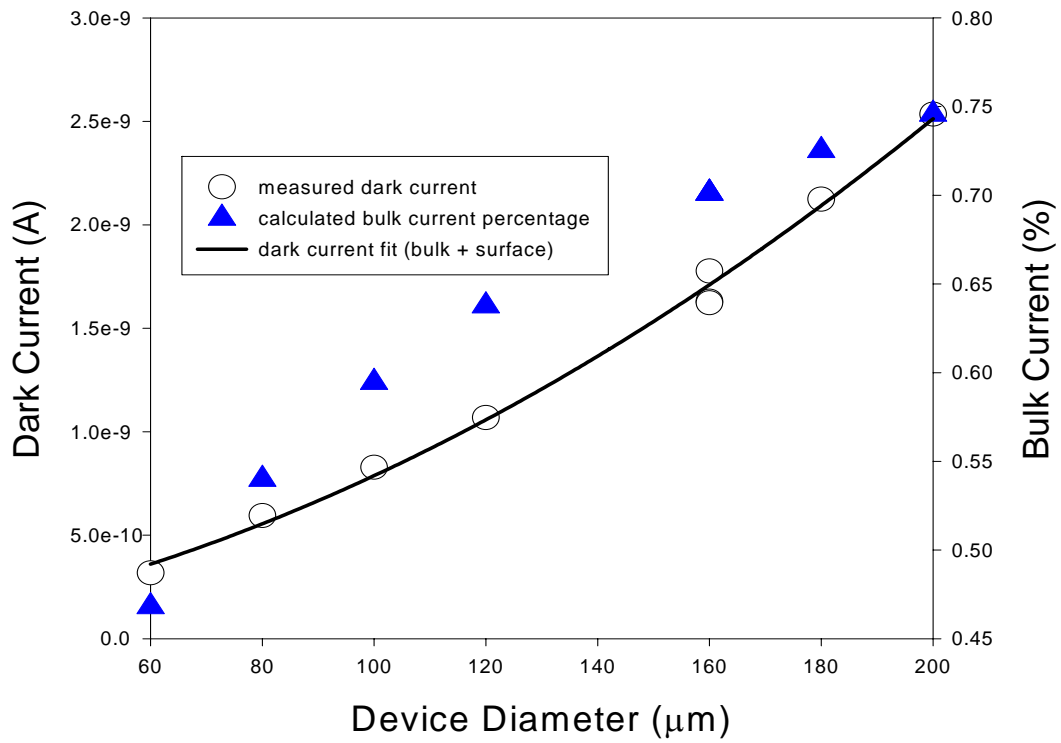
To investigate the effects of the growth conditions on dark current the following growth parameters were varied: growth temperature, arsenic BEP, and growth rate. Initial conditions were obtained for a fixed arsenic BEP of  $1 \times 10^{-5}$  Torr and growth temperatures ranging from 500°C to 560°C in addition to a fixed growth temperature of 530°C a arsenic BEPs fo  $8 \times 10^{-6}$  to  $3 \times 10^{-5}$  Torr. This initial data led to a matrix of experimental data, shown in Figure 4-2, at a growth rate of ~1 monolayer/sec. Additionally, a *P-I-N* was grown at a growth rate of 0.5 monolayers/sec at a growth temperature of 530°C and  $1.5 \times 10^{-5}$  Torr arsenic BEP.

	Growth Temperature (°C)				
Arsenic BEP (Torr)	500	515	530	545	560
$8.0 \times 10^{-6}$		X	X	X	
$1.0 \times 10^{-5}$		X	X	X	X
$1.5 \times 10^{-5}$	X	X	X	X	X
$2.0 \times 10^{-5}$		X	X	X	X
$3.0 \times 10^{-5}$		X	X	X	X

**Table 4-1.** InGaAs growth study data experimental data points for ~1 monolayer/sec where “X” denotes matrix element was grown.

In order to characterize the dark current components for different growth conditions, photodiodes were fabricated and measure for a range of device diameter (60-200  $\mu\text{m}$ ). Figure 4-3, below, shows the results of dark current measurements for a growth temperature of 530°C and Arsenic BEP of  $1 \times 10^{-5}$  Torr as an example. The dark current contribution that scales with the square of the device diameter is the bulk current

contribution. Equation 2-1 was used to separate the bulk current component from the surface current contribution. Here it can be seen as the device diameter decreases the bulk current percentage decreases due to the decrease in the device volume to surface ratio. Mesa photodiodes were fabricated, 160  $\mu\text{m}$  diameter, in order to compare the effect of the growth condition on measured dark current. Smaller device diameters would have led to lower dark currents.



**Figure 4-2.** Dark current measure for an InGaAs P-I-N ( $530^\circ\text{C}$ ,  $1 \times 10^{-5}$  Torr) showing total dark current measured (circles), fit of surface and bulk current components (line), and the extracted bulk current percentage (triangles) measured on 160  $\mu\text{m}$  diameter devices and applied electric field of 12.5 kV/cm.

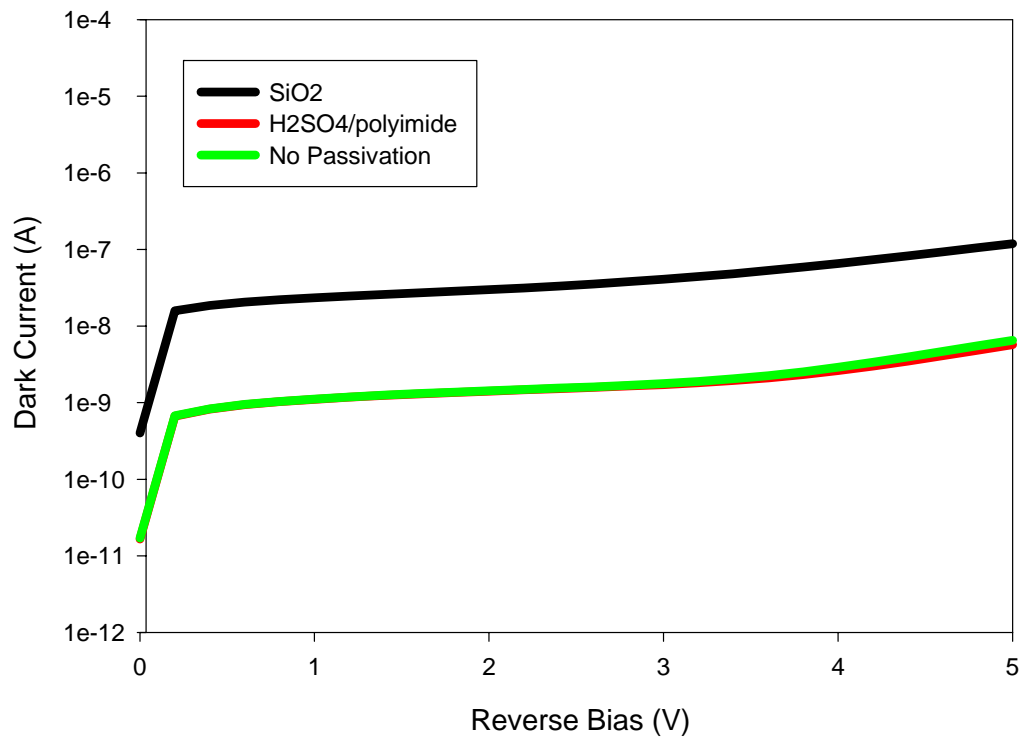
#### **4.1.1 Device processing**

The basic mesa process was used to fabricate the “test” P-I-N’s, as described in section 3.3. It was found that the most reliable way that in order to provide a suitable comparison of bulk dark current values that a reliable passivation was needed. Results from comparing passivation techniques are covered in the next section. Also, because the material for this study was grown on Indium-mounted blocks, the n-metallization was not necessary and the back of the wafer was used for the n-contact. Once the mesas were etched, the sample were cleaned in solvents and immediately taken to the cryoprobe station where the sample were loaded and pumped to  $\sim 5 \times 10^{-5}$  Torr. This was done because it was found that if the sample were left in the ambient air the devices exhibited very large dark currents as a result of large surface current contribution.

##### ***4.1.1.1 Passivation comparison***

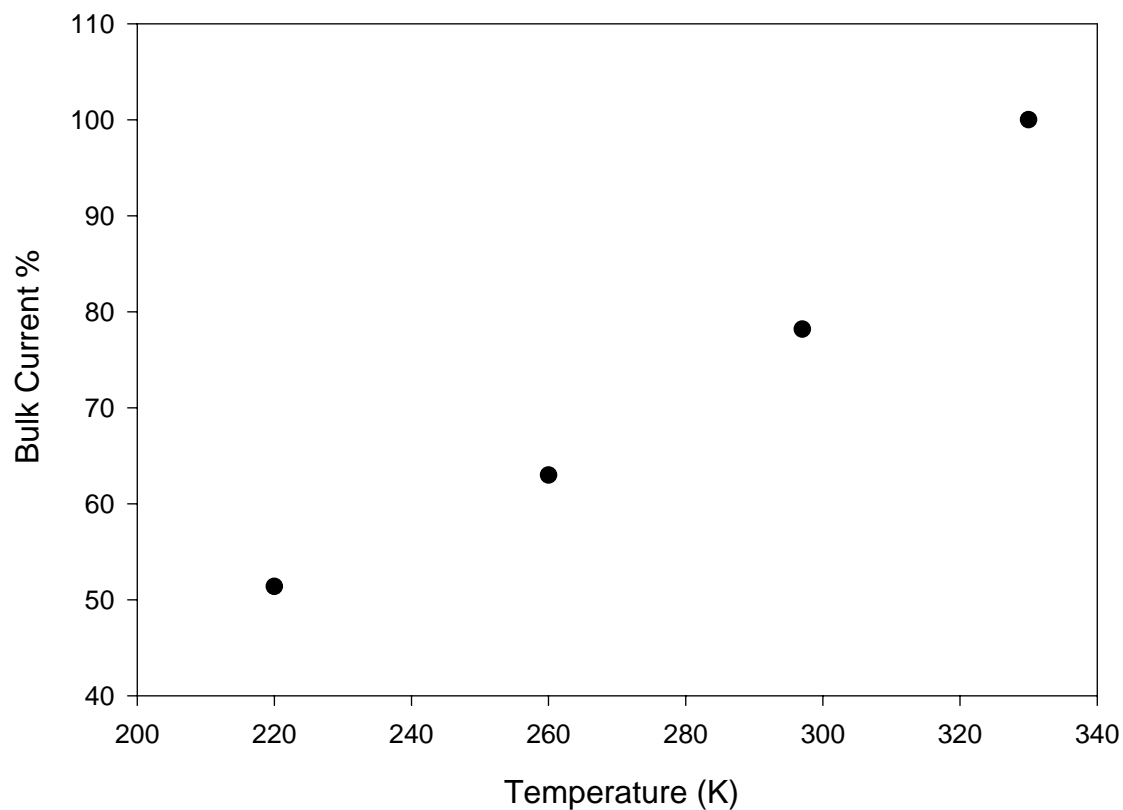
Figure 4-3 shows a comparison of the different passivation techniques investigated for InGaAs P-I-N’s.  $\text{SiO}_2$  was found to exhibit the largest dark current, and measurements of different device diameter revealed that the dark current was dominated by the surface current component. Both no passivation and using a  $\text{H}_2\text{SO}_4$  dip followed by a polyimide passivation coating provided the lowest dark currents where the bulk dark current contribution was  $> 80\%$  of the total dark current. Due to the difficulty in reliably passivating with the polyimide process, the easiest method for studying many PIN devices was first etching the mesas, and then transferring them directly to a vacuum chamber for IV measurements without using any passivation layer.





**Figure 4-3.** Comparison of passivation methods showing 300K IV measurements for 160  $\mu\text{m}$  diameter devices.

Also, the bulk current percentage was measured as a function of temperature as shown in Figure 4-4. Here it is seen that as the temperature decreases the amount of dark current from the bulk material decreases. This is due to large temperature dependence of the generation current on temperature (equation 2-2) and the relatively small surface current temperature dependence of surface recombination.



**Figure 4-4.** Bulk dark current contribution as a function of temperature (for no passivation) for a PIN device (545°C,  $1.5 \times 10^{-5}$  Torr).

## 4.2 SILICON CELL TEMPERATURE

The effects of the silicon cell temperature during the i-region layer growth were investigated. Two procedures in growing photodiode material were compared: (1) leaving silicon cell at the n-layer doping level temperature and (2) idling the silicon cell for some time after n-layer growth. These were simulated for Hall measurements by

heating of the cell and before growing unintentionally doped bulk layers. Material quality was compared using both Hall effect measurements and measured dark currents.

Hall measurements were performed at room temperature on approximately 1.5 cm x 1.5 cm pieces of 500 nm-thick bulk  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  samples using the van der Pauw measurement technique. In the course of these measurements it was found that because of the difficulty in fabricating ohmic contacts with low carrier concentration material there was a large variation in measured carrier concentrations from samples taken from the same wafer which resulted in large deviations in calculated carrier concentrations, but where adequate in comparing gross changes ( $>10\%$ ). Table 4-1 summarize Hall measurements where an order of magnitude change is observed. However, when comparing  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  samples grown with and without the silicon cell hot ( $1120^\circ\text{C}$  while hot,  $670^\circ\text{C}$  while idled), it was found that having the silicon cell hot resulted in approximately one order of a magnitude increase in measured carrier concentration (Table 4-2).

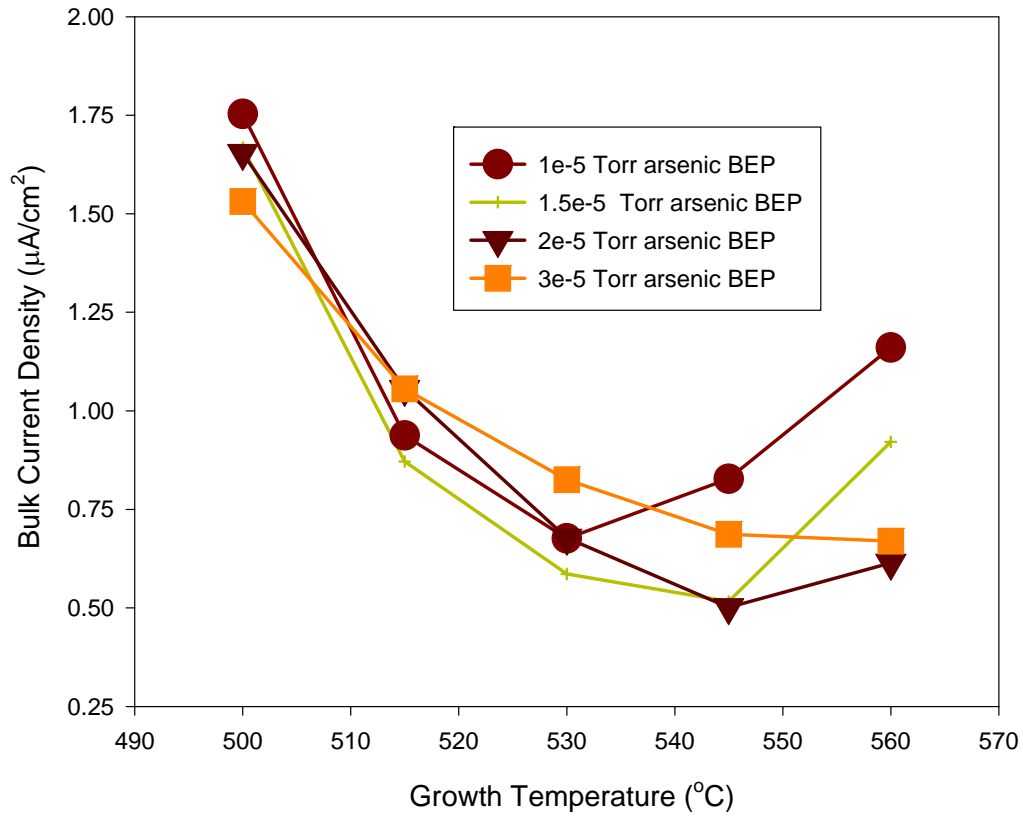
<b>Sample Description</b>	Hall carrier concentration [ $\text{cm}^{-3}$ ]
Silicon cell remaining hot	<b><math>1.2 \times 10^{14}</math></b>
Silicon cell idled for 5 min from hot	<b><math>1.1 \times 10^{14}</math></b>
<b>Silicon cell idled for 1 hr</b>	<b><math>1 \times 10^{13}</math></b>

**Table 4-2.** Hall measurement results for silicon cell hot and idled for different times.

PIN devices grown under the same growth conditions except for Silicon cell temperature during the intrinsic layer growth were measured. For 160  $\mu\text{m}$  diameter devices the bulk dark current was 1.5 nA and 0.5 nA, for Silicon at 1120°C and 670°C respectively.

#### **4.3 INFLUENCE OF AS BEP ON DARK CURRENT**

The arsenic BEP was varied from  $8 \times 10^{-6}$  -  $3 \times 10^{-5}$  Torr. For normal operating conditions the As sublimator temperature,  $\sim 390^\circ\text{C}$ , is maintained such that when the valve positions is halfway open the measure flux is  $\sim 1 \times 10^{-5}$  Torr. A higher sublimator temperature would allow higher As BEPS, but flux repeatability in the  $\sim 10^{-6}$  Torr range would be lost, hampering the growth of other material system grown in the same chamber. This limits the practical upper limit that can be achieved as well as faster depletion of the arsenic source material at the highest BEPs. Figure 4-5 below summarizes the measured bulk current with the variation of arsenic BEP under different growth temperatures.

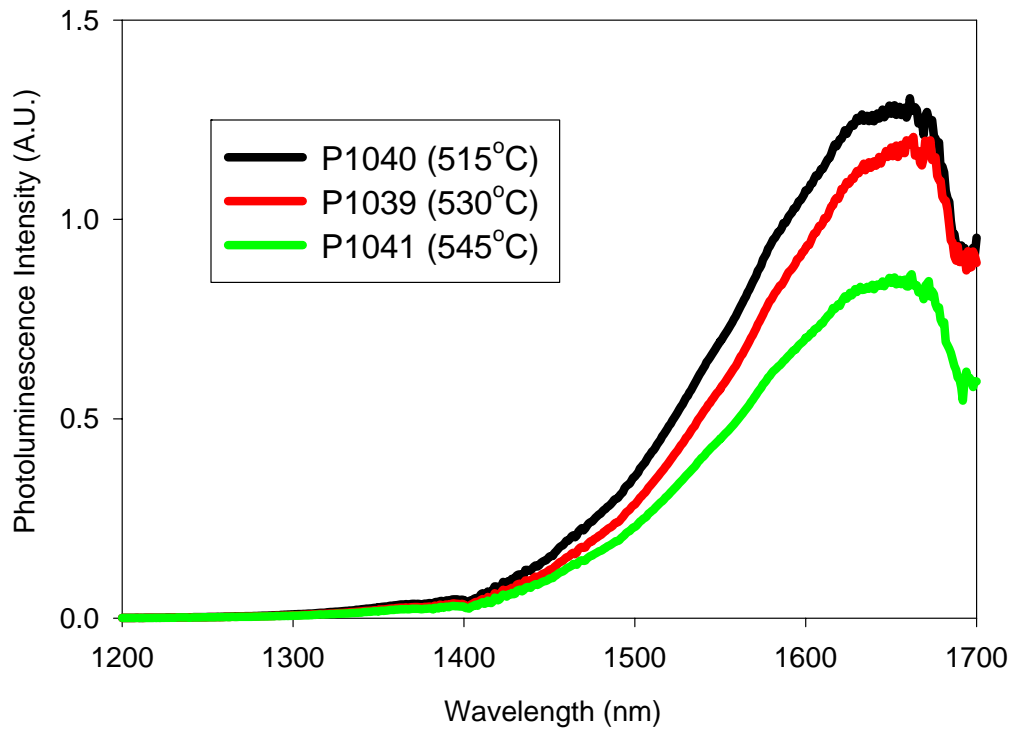


**Figure 4-5.** Bulk dark currents for InGaAs P-I-Ns grown with varying arsenic BEP and growth temperature at a growth rate of  $\sim 1$  monolayer/sec. Measured on  $160\ \mu\text{m}$  diameter devices with an applied electric field of  $12.5\ \text{kV/cm}$  ( $1\ \text{V}$  reverse bias).

The lowest measured dark current density was  $0.5\ \mu\text{A/cm}^2$  ( $0.1\ \text{nA}$  for a  $160\ \mu\text{m}$  diameter device) corresponding to an Arsenic BEP of  $2 \times 10^{-5}$  Torr for both  $545^\circ\text{C}$  and  $560^\circ\text{C}$ . A further discussion of the explanation of this trend in dark current is cover is section 4.6.

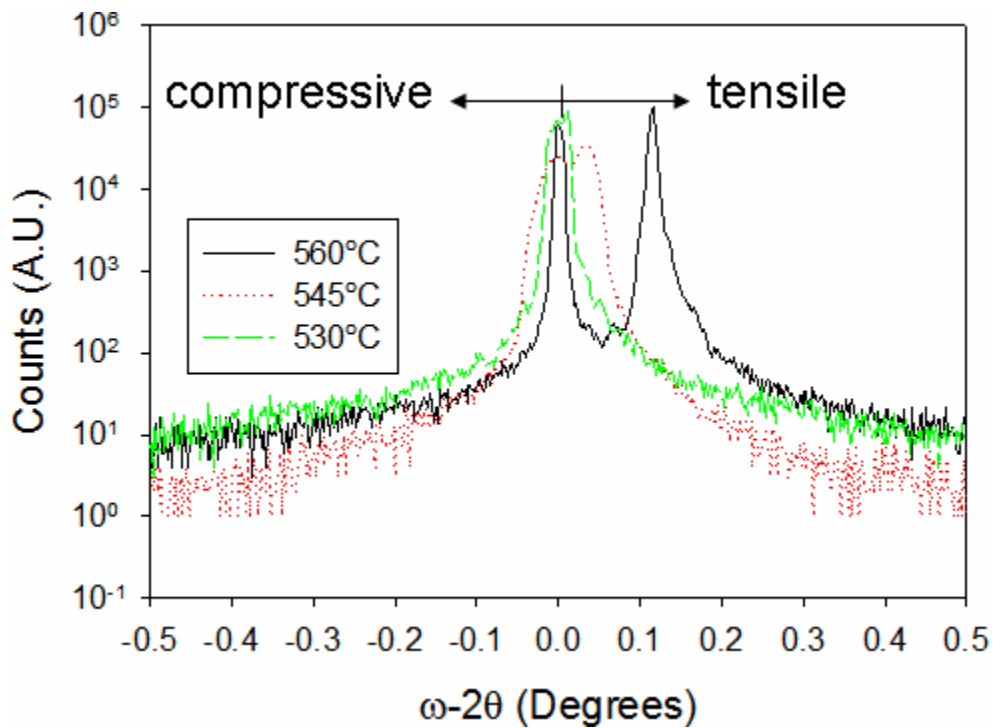
#### 4.4 INFLUENCE OF GROWTH TEMPERATURE ON DARK CURRENT

Photoluminescence (PL) measurements are widely used as a standard for determining material quality.<sup>1,2</sup> PL measurements were performed on 200 nm-thick  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  surrounded by 50 nm  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  confining layers. These were grown with an arsenic BEP of  $1.5 \times 10^{-5}$  Torr with growth temperatures of 515°C, 530°C, and 545°C. Figure 4-6 shows that as the temperature is increased, the PL intensity degrades.



**Figure 4-6.** PL measurements of InGaAs for different growth temperatures with an arsenic BEP of  $1 \times 10^{-5}$  Torr.

As seen in Figure 4-6, this trend in PL intensity does not follow the trend in measured dark current where an optimum temperature of 545°C was found for an Arsenic BEP of  $1 \times 10^{-5}$  Torr. From x-ray measurements, the upper limit in growth temperature was limited by the desorption of indium where a shift in the x-ray peaks indicated a slightly Ga-rich ( $\text{In}_{0.51}\text{Ga}_{0.49}\text{As}$ ) composition at 560°C and Arsenic BEP  $1.5 \times 10^{-5}$  Torr, as show in Figure 4-7. This explains the trend in measured dark current densities in Figure 4-5, where an increase in arsenic BEP is needed to stabilize the surface for higher growth temperatures.



**Figure 4-7.** X-ray diffraction showing Ga-rich InGaAs grown on InP at 560°C.

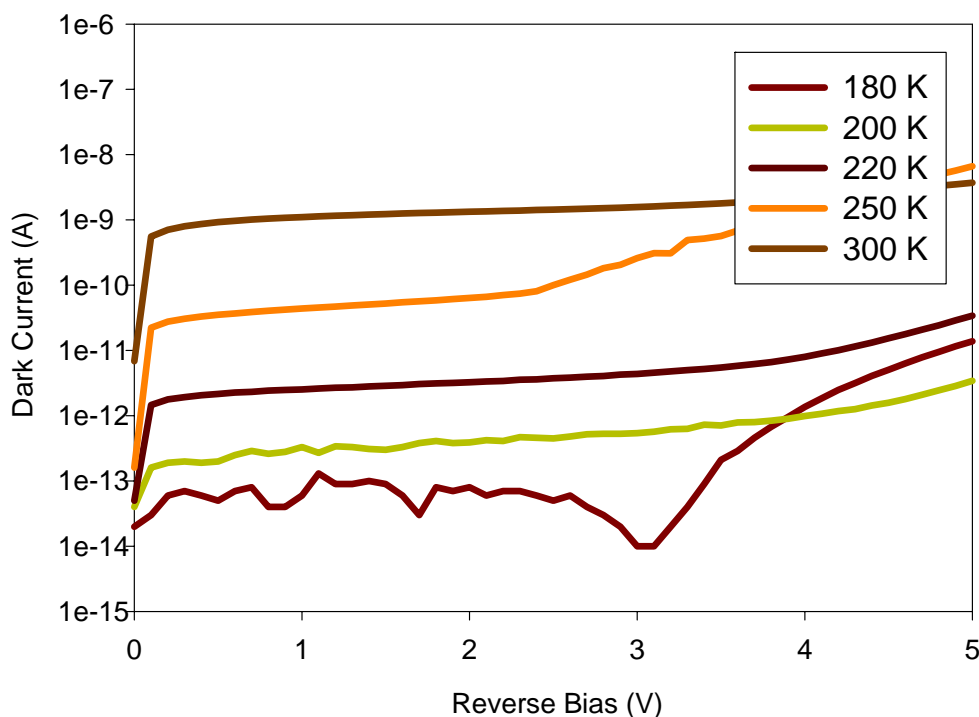
#### **4.5 INFLUENCE OF GROWTH RATE ON DARK CURRENT**

The previous growth rates for this study were all grown at  $\sim 1$  monolayers/sec. In order to investigate the role of growth rate in minimizing photodiode dark current a sample was grown at 0.5 monolayers/sec at an Arsenic BEP of  $1.5 \times 10^{-5}$  Torr and growth temperature of  $530^\circ\text{C}$ . The bulk dark current density was  $1.2 \mu\text{A}/\text{cm}$  with a calculated activation energy of 0.49 eV. These results were similar to measurements for an Arsenic BEP of  $3 \times 10^{-5}$  Torr ( $0.83 \mu\text{A}/\text{cm}^2$ , 0.47 eV) grown at the same growth temperature indicating that the deep-levels associated with an increase in dark current with Arsenic BEP also increase as with lower growth rate.

#### **4.6 ACTIVATION ENERGY ANALYSIS**

Activation energies for the measured dark currents were made for all of the PIN devices used for the MBE growth study in order to provide some insight into the impurity/defect levels responsible for the generation currents. Current-voltage measurements were made on photodiodes at different device temperatures (180-300 K). Equation 2-2 was used to calculate the activation energies. In interpreting the results of these measurements, an increase in dark current for the same activation energy corresponds to increase in a particular defect density. Also, a change in activation energy indicates that the source(s) of the deep level responsible changed. Figure 4-8 below shows the temperature dependence of a typical PIN device. At 180 K, the dark current measured is limited by the probe station setup.

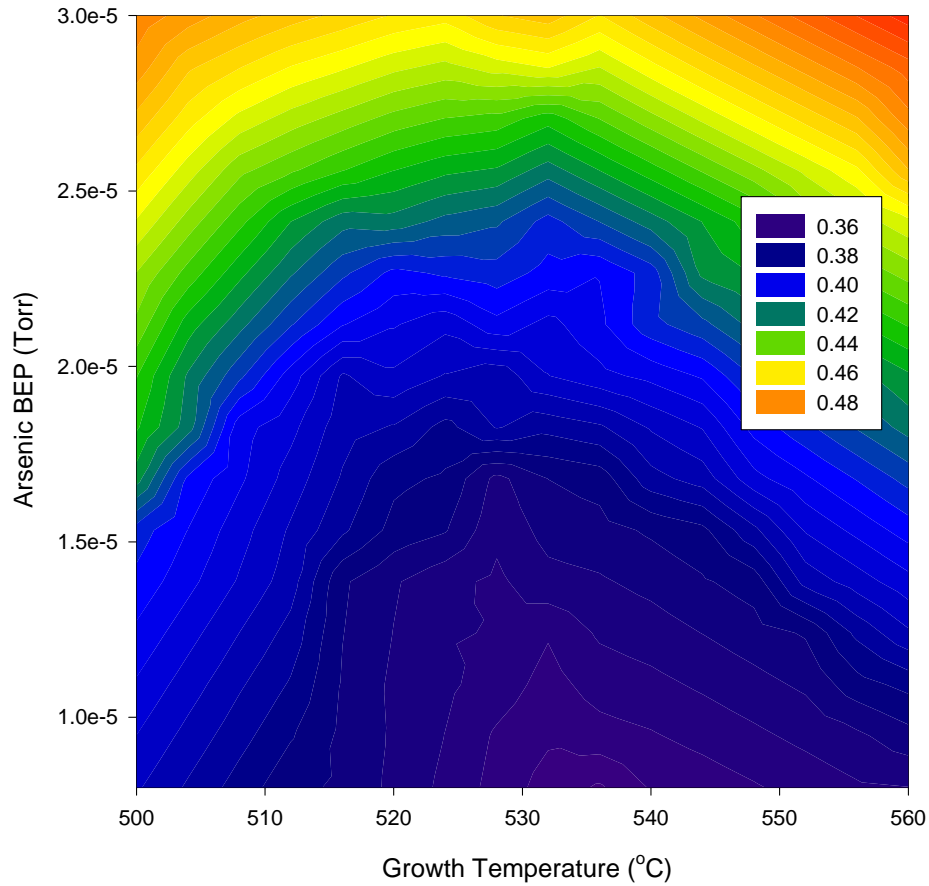




**Figure 4-8.** Temperature dependence of PIN current-voltage measurements.

Once activation energies (summarized in figure 4-9) were calculated from the temperature dependent IV measurements, a trend of increasing activation energies is found for the arsenic BEP ranges used from  $\sim 0.36$  eV at lower BEPs to  $\sim 0.48$  eV at BEPs of  $3 \times 10^{-5}$  Torr. This increase in energy levels indicates a change in the origin of the deep-level providing the majority of the generation current. A couple of changes in the growth environment are necessary when growing at elevated As BEPs. These include a larger group-V/III ratio and larger amount of impurities from the As source. Defects resulting from a larger group-V/III ratio would reduce the Ga surface mobility and provide an overabundance of As resulting in As-antisite formation. Also, since oxygen deep-levels have been reported to have an energy level of 0.48 eV and are present in As

source material, the increase in dark current with Arsenic BEP is attributed to an increase in oxygen rather than As-antisite formation.



**Figure 4-9.** Contour plot summarizing the activation energies dependence on growth temperature and arsenic BEP, given in eV for smoothed data.

At lower arsenic BEPs ( $0.8\text{--}1.5 \times 10^{-5}$  Torr), changes in growth temperature do not greatly affect the measured activation energies (mid-gap, 0.36-0.4 eV). Also, as was shown in figure 4-6, a minimum in measured dark current densities occurs ( $545^{\circ}\text{C}$  for As Bep of  $1.5 \times 10^{-5}$  Torr). At low temperatures the surface mobilities of the matrix elements are the lowest, which can cause As-antisite formation. As the temperature is

increased the density of As-antisite reduces. This can be extended as far as indium desorption allows which sets the upper temperature limit

#### **4.8 SUMMARY**

The influence of the arsenic BEP, growth temperature, and growth rate in the MBE growth of InGaAs photodiodes on dark current was studied. All three of these growth parameters need to be adjusted for the optimum (lowest) dark current. For a growth rate of  $\sim 1$  monolayer/sec, the lowest dark current was measured from PIN devices grown at a growth temperature of  $545^{\circ}\text{C}$ , and an arsenic BEP of  $2 \times 10^{-5}$  Torr. The trend in both dark current density and activation energy can be explained by defects/impurities reported elsewhere.

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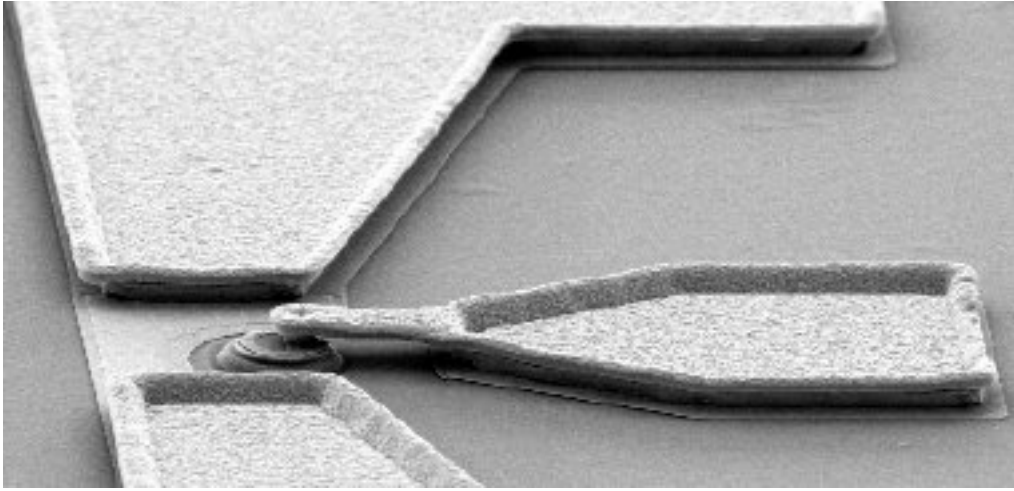
## **Chapter 5**

### **APD Device Results**

#### **5.1 OVERVIEW**

Various SACM APD device structures were grown for implementing low-dark-current devices. These structures were all grown utilizing InGaAs absorption layers. In SACM structures the charge layer doping is very critical for maintaining the desired electric field profile across the device. In addition, small variations in the MBE cell temperatures greatly affect the device characteristics. In designing these structures the breakdown voltage and punch-thru voltage are estimated by solving Poisson equation for the simplified electric field profiles corresponding to these voltages. Once approximate doping levels are found, device are grown, processed, and then measured. Adjustments to either doping concentration or charge layer thickness can then be made to fine tune the desired current-voltage characteristics.

In order to fabricate small area devices, lithography was performed using the photon counting mask which utilizes air-bridges to make contacts to ring contacts located on the top of the etched mesas. Figure 5-2 shows a SEM image of an air-bridge after metal liftoff.



**Figure 5-1.** SEM picture of air bridge after metal lift-off.

## 5.2 InGaAs-InAlAs SACM APD

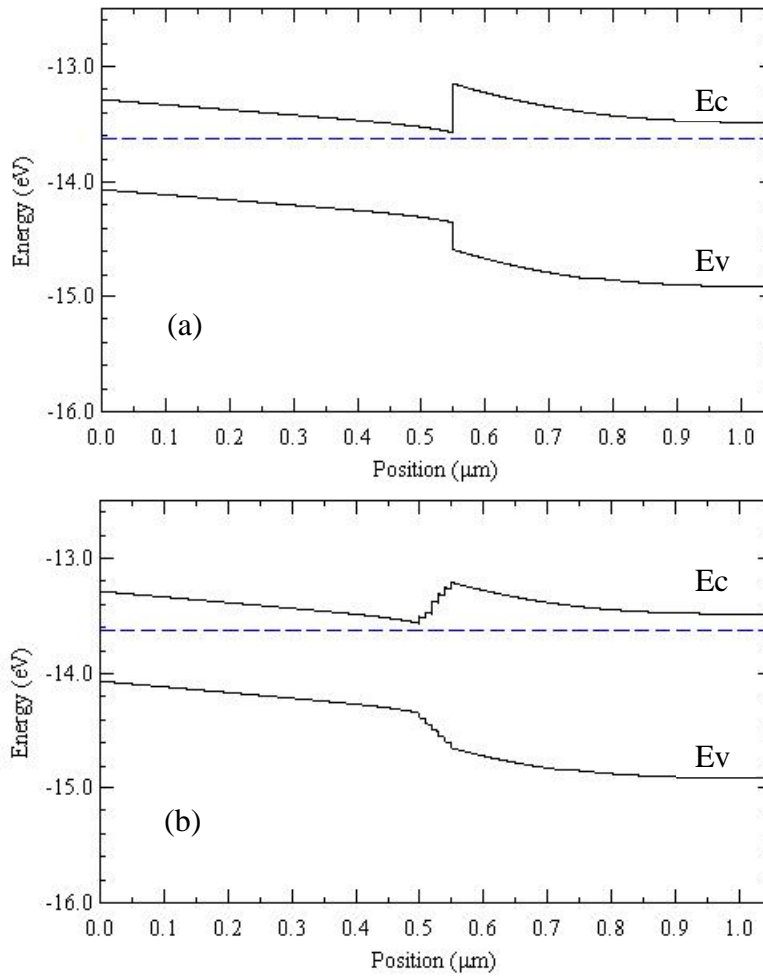
The following section describes the device structure of the implemented an InGaAs-InAlAs SACM APD, included design consideration and measurement results.

Ti/Pt/Au p-contact	
30nm p+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	
400nm p $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
50nm u.d. graded $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
1000nm u.d. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	
50nm u.d. graded $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
150nm p $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ $3 \times 10^{17} \text{ cm}^{-3}$	
800nm u.d. $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
800nm n+ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
n-InP substrate	
AuGe/Ni/Au n-contact	
	10nm p+ $\text{In}_{0.53}\text{Al}_{0.40}\text{Ga}_{0.06}\text{As}$ digital alloy
	10nm p+ $\text{In}_{0.53}\text{Al}_{0.32}\text{Ga}_{0.16}\text{As}$ digital alloy
	10nm p+ $\text{In}_{0.53}\text{Al}_{0.24}\text{Ga}_{0.24}\text{As}$ digital alloy
	10nm p+ $\text{In}_{0.53}\text{Al}_{0.16}\text{Ga}_{0.32}\text{As}$ digital alloy
	10nm p+ $\text{In}_{0.53}\text{Al}_{0.08}\text{Ga}_{0.40}\text{As}$ digital alloy

**Figure 5-2.** InGaAs-InAlAs SACM device structure.

### 5.2.1 Device Design

In this SACM structure an 800nm InAlAs multiplication region was used along with a 100nm InGaAs absorption region. On each side of the absorption region InAlGaAs was grown as a digital alloy to serve as a graded transition region to minimize carrier trapping at the interface. Figure 5-3 shows a comparison of simulated band profiles using a graded 50nm InAlGaAs layer between InGaAs and InAlAs layers.



**Figure 5-3.** Reduction of the interface discontinuity at the (a) InGaAs/InAlAs interface without a transition region and (b) using a 50 nm InAlGaAs transition region consisting of five 5 nm-thick grading layers.

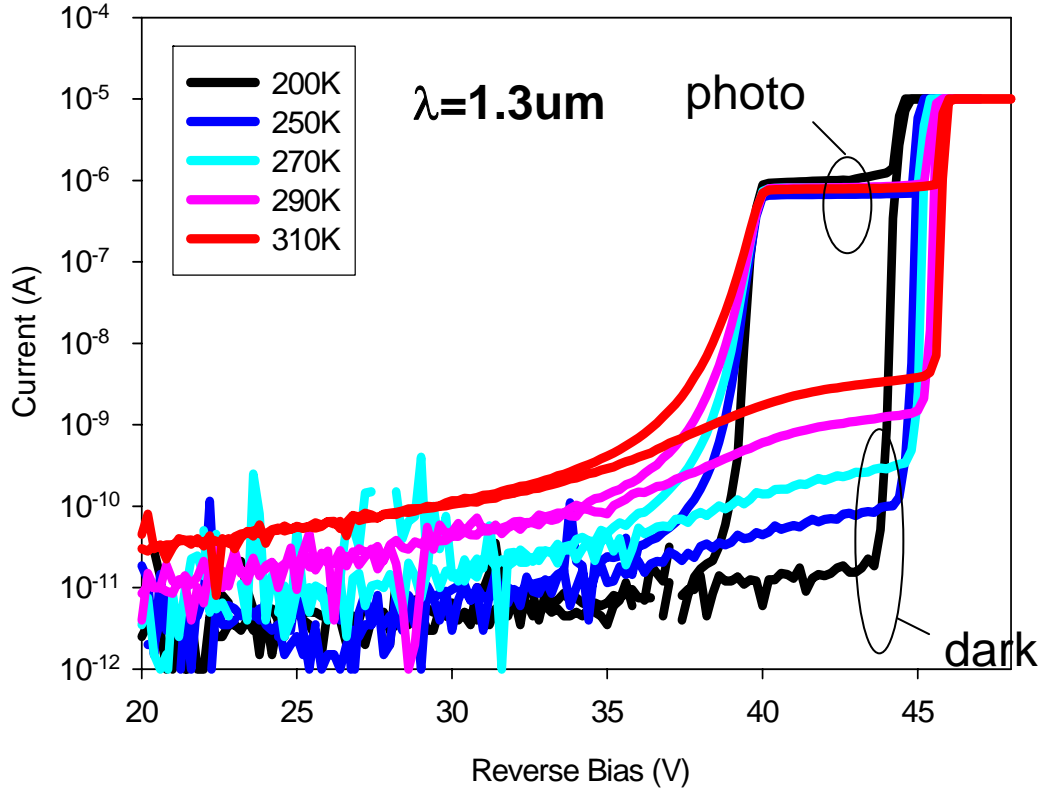
For these devices the charge layer doping concentration and charge layer thickness are critical parameters in determining the devices operating characteristics. A total charge layer charge amount that is too large results in avalanche breakdown occurring before punch-thru and hence no collection of optically generated carriers. Additionally, a charge layer that is too small results in a low punch-thru voltage (relative to breakdown) and a large dark current in the vicinity of the breakdown voltage, as shown in figure 5-4.

### 5.2.2 Device Characteristics

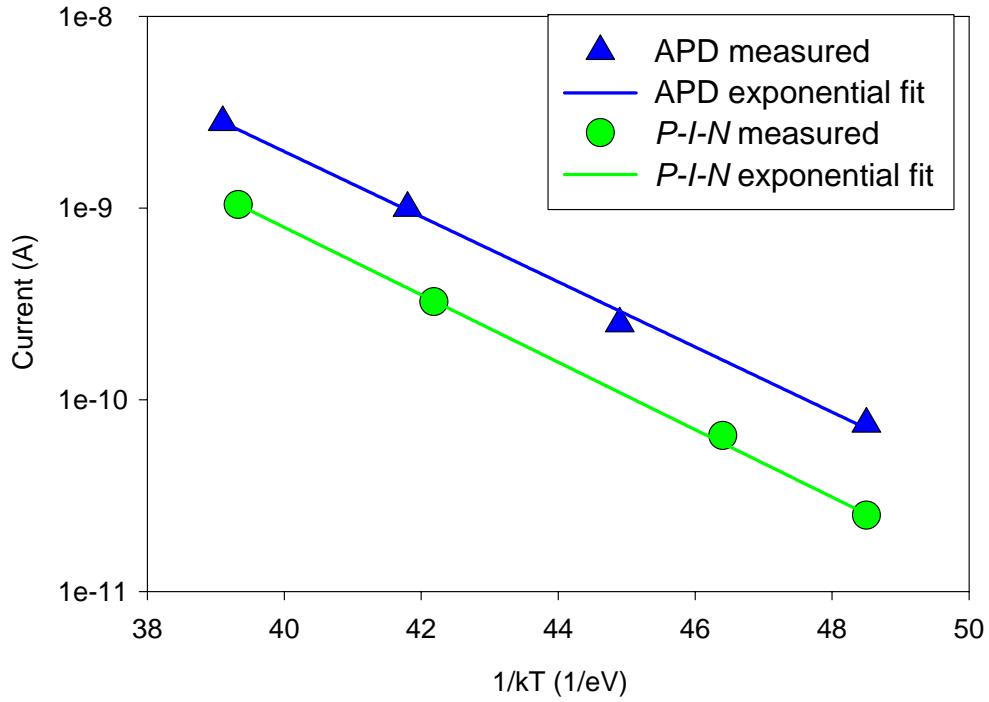
Measurements of the InGaAs-InAlAs APD were performed using  $1.3\ \mu\text{m}$  illumination, and dark currents were measured at various temperatures, as shown in figure 5-6 for a  $40\ \mu\text{m}$  diameter device. The breakdown voltage of these devices was 45 V at RT (13 mV/K temperature dependence) and the punch-thru voltage was located at 39 V. At 90% of the breakdown voltage the responsivity was measured at 0.8 A/W with a gain of 1.18. The dark currents and dark density was 1 nA and  $80\ \text{mA}/\text{cm}^2$  respectively. These dark current values are close to values found for devices manufactured by Epitaxx Ltd. (EPM239) where successful Geiger mode operation has been reported.<sup>1,2</sup> Photon counting measurements were performed G. Karve, procedure described elsewhere,<sup>3</sup> but photon counting was not achieved for these devices where the photon counts did not differ from the dark counts. Also, it was observed that the dark count rates increased with time as the device was operated. Because trap levels have been reported to be larger number of reported traps and greater concentrations in AlGaAs than GaAs,<sup>4,5</sup> and InAlAs could be



responsible for the change in dark count rate due to carrier trapping InAlAs layers were replaced with InP as a multiplication region material.



**Figure 5-5.** InGaAs-InAlAs APD IV characteristics at different temperatures for a 40  $\mu\text{m}$  diameter device and 1.3  $\mu\text{m}$  illumination.



**Figure 5-6.** Comparison of SACM and P-I-N dark current activation energies.

### 5.3 InGaAs-InP SACM APD

The following section describes the device structure of the implemented an InGaAs-InP SACM APD, included design consideration and measurement results.

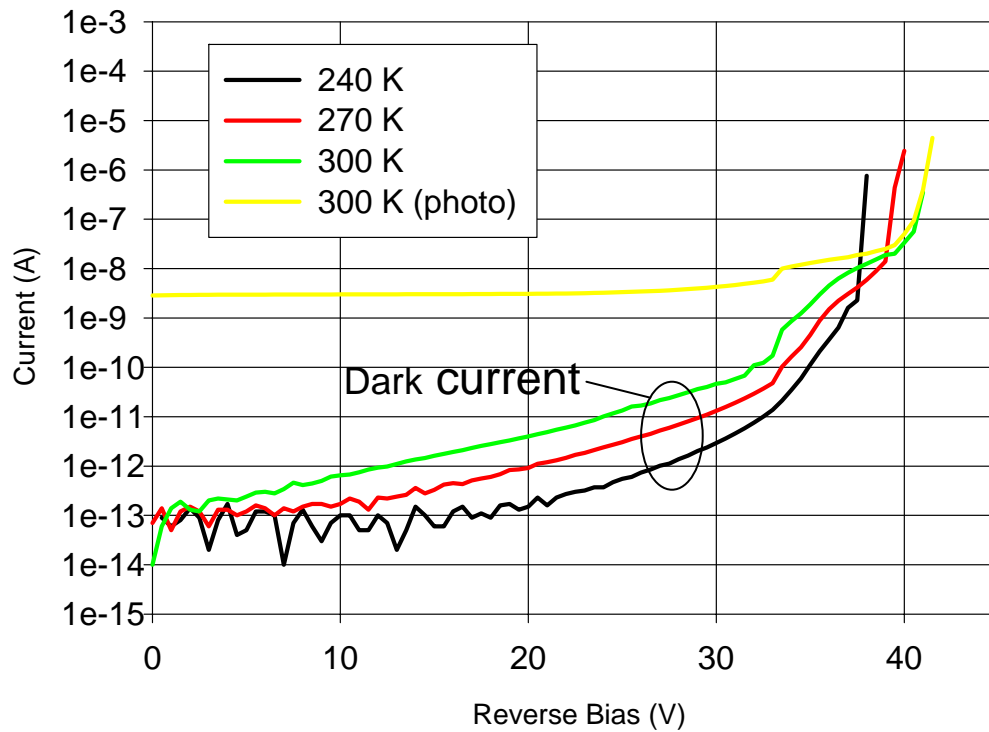
#### 5.3.1 Device design

In order to remove Al-containing layers from the devices InP was used as a multiplication region. As a result, only one grading layer was used,  $\text{In}_{0.72}\text{Ga}_{0.28}\text{As}_{0.61}\text{P}_{0.39}$ , to minimize

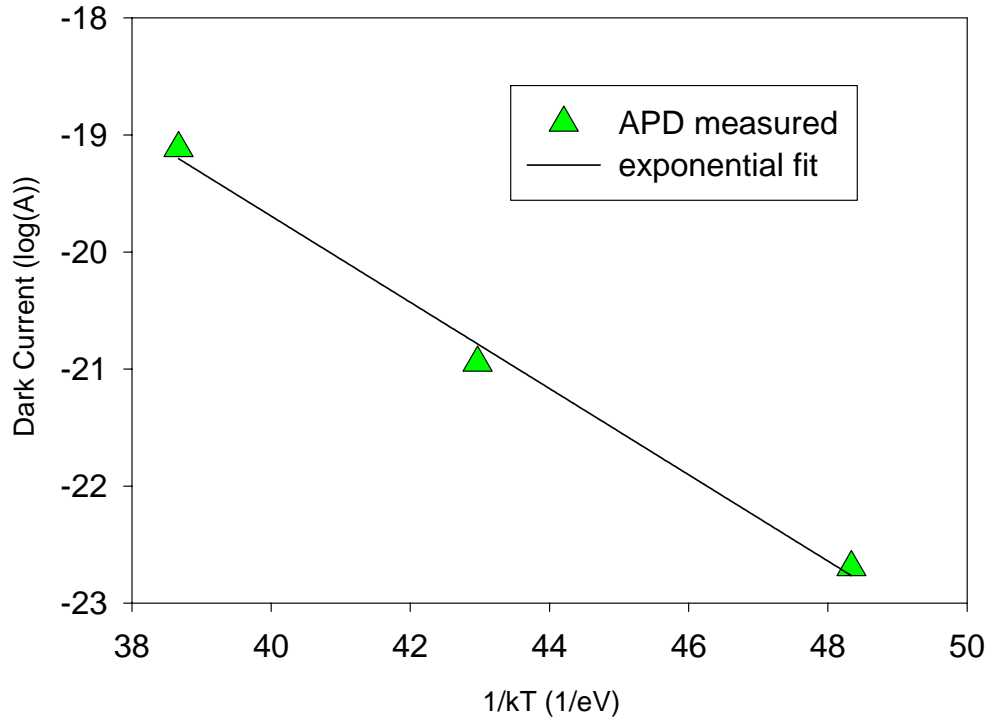
carrier trapping due to the smaller InGaAs/InP offset, and also due to the difficulty in growing a As/P-based digital alloy.

### 5.3.2 Device Characteristics

Figure 5-7 shows the IV characteristics measure at different bias voltages. These measurements were made on a 160  $\mu\text{m}$  diameter device. The photocurrent is shown only at 300K and the microscope light was used as a source. At 300K the breakdown voltage was at 42 V, and the punch-through voltage was at 33.5 V. The dark current measured at punch-through was 5 nA giving a dark current density of 10  $\mu\text{A}/\text{cm}^2$ .



**Figure 5-7.** InGaAs-InP SACM APD



**Figure 5-8.** InGaAs-InP SACM IV characteristics at different temperatures.

The activation energy calculated at punch-through was 0.37 eV, consistent with P-I-N activation energy under the same growth conditions (Figure 5-8). However, the large dark current density at punch-through indicates that the majority of dark current comes from surface current contributions due to the passivation layer.

## 5.4 SUMMARY

In this chapter two similar SACM APD device structures were implemented. Both InAlAs and InP were used a multiplication regions and exhibited dark currents at 90% breakdown, at 1 nA and 5 nA respectively, for 160  $\mu\text{m}$  diameter devices.

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## Chapter 6

### Summary and Future Work

#### 6.1 SUMMARY

In this dissertation, methods in reducing the dark current in  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  photodiodes were explored. Passivation options were explored as well as their limitations in practical use. S-passivation followed by polyimide deposition provided the lowest dark current through the reduction of surface currents. It was found that for low temperature operation and small device diameters the surface current can still provide a large portion of the dark current.

The optimization of the MBE growth parameters were explored in addition to device passivation. The growth temperature was found to be bound at high temperatures due to Indium desorption while being bound by the formation of deep-levels with a mid-gap activation energy most likely due As-antisite formation. Additionally, the Arsenic BEP was bound at low fluxes by the stabilization of In-desorption at  $T > 545^\circ\text{C}$  and was limited at high BEPs through defect-levels at 0.48 eV most likely due to increased oxygen impurity incorporation from the Arsenic source. It was also discovered that in a single shutter dopant cell geometry, the Si cell should be cooled during undoped layer growth to reduce the amount of unintentional Si doping even with the Si-shutter in the close position ( $\sim 1 \times 10^{14} \text{ cm}^{-3}$ ).

An InGaAs/InAlAs-InP APD structure was implemented that exhibited low dark currents at room temperature, but single photon counting wasn't achieved possibly due to Al-related defects.

## 6.2 FUTURE WORK

In the course of the research several experiments were proposed, but were not pursued to either time constraints and/or lack of measurement capability. Notably, two experiments are described below: (1) Deep Level Transient Spectroscopy and (2) utilization of the quaternary  $\text{In}_{0.72}\text{Ga}_{0.23}\text{As}_{0.61}\text{P}_{0.39}$  as the absorption region in a SACM APD device.

### 6.2.1 Deep Level Transient Spectroscopy

Deep level transient spectroscopy (DLTS) is a differential capacitance technique developed by Lang<sup>1,2</sup> that allows the analysis of non-radiative recombination centers in semiconductor materials. The DLTS technique can be used to quantify electrically active defect levels down to  $1 \times 10^{12} \text{ cm}^{-3}$  and measure energies from mid-gap to  $\sim 0.1 \text{ eV}$  of the conduction and valence bands.<sup>1,3</sup> The time constant for emission of trapped carriers from the depletion region of a Schottky barrier is given by the following expression,

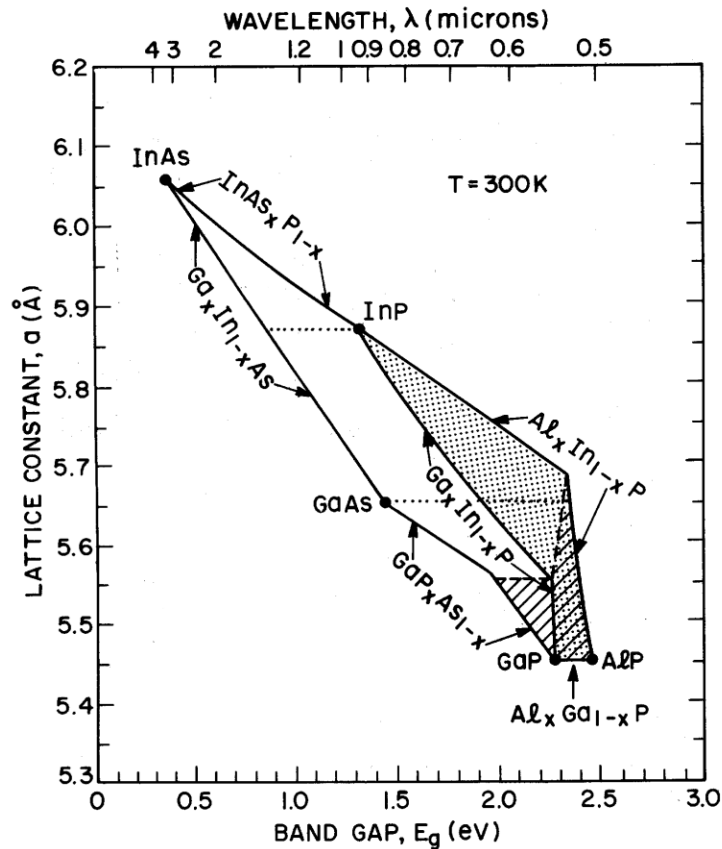
$$\tau = \frac{\exp(\Delta E - ET) / kT}{\gamma * \sigma * T^2} \quad (6-1)$$

Where  $\Delta E$  is the defect activation energy, and  $\sigma$  is the capture cross-section. By conducting DLTS measurements on the samples grown for this dissertation's dark current

study a quantitative description of the deep level energy levels and concentration can be made to verify the sources of defect/impurities.

### 6.2.2 InGaAsP Absorption Layers

For wavelengths shorter than the cutoff of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  grown on InP (1.65  $\mu\text{m}$ ), the quaternary material system  $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$  (Figure 6-1) can be used with a composition corresponding to the desired wavelength detection. The use of this quaternary allows the maximum band gap material to be used for the absorption region, which reduces the generation current (equation 2-2).



**Figure 6-1.** (Al, Ga, In)(As,P) material system. (Ref 1)



In order to grow material lattice-matched to InP, the following x and y mole fraction relationship is used,<sup>4</sup>

$$x = \frac{0.4526 * y}{1 - 0.031 * y}, \quad (6-2)$$

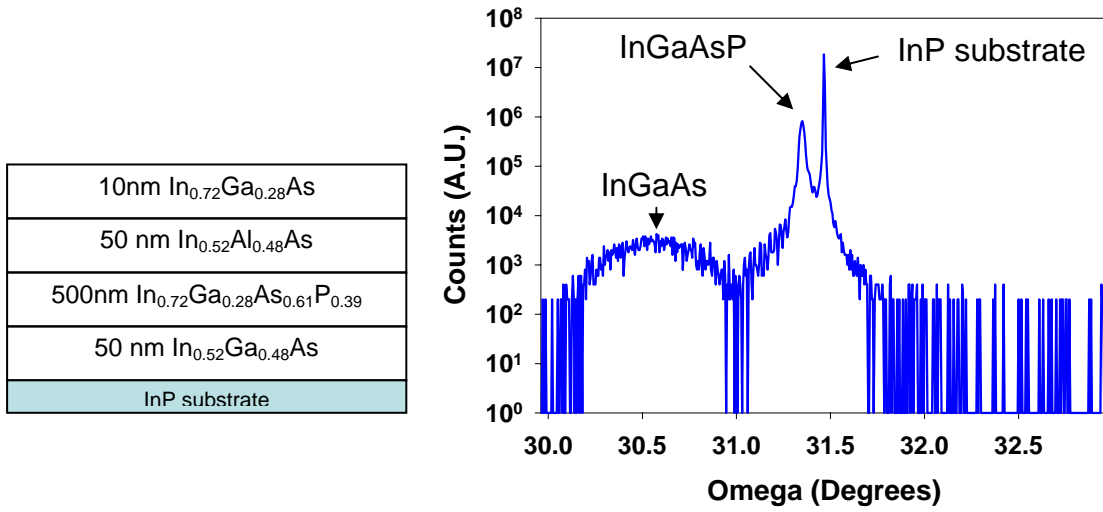
through the application of Vegard's Law to binary lattice constants. Additionally, the following band gap expression for material lattice-matched to InP derived from photoluminescence data can be used for tailoring the detection wavelengths,<sup>4,5</sup>

$$Eg(eV) = 1.35 - 0.72 * y + 0.12 * y^2 \quad (6-3)$$

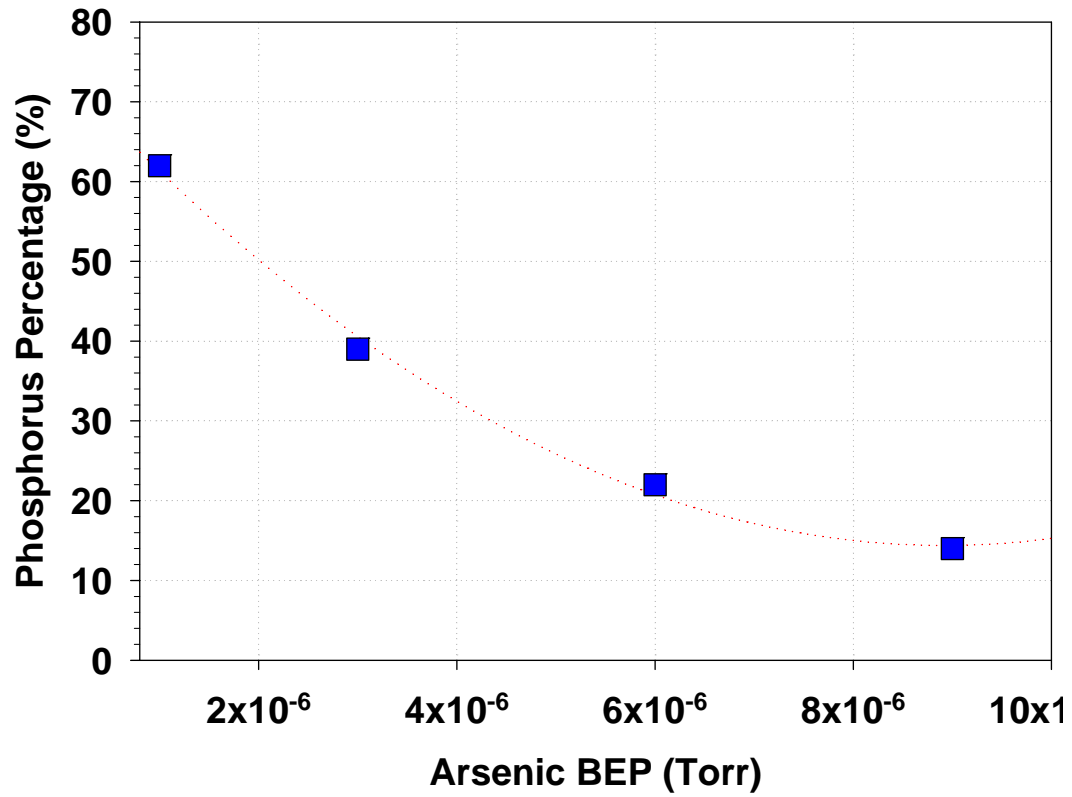
From equation 6-2 and 6-3, for 1.3  $\mu\text{m}$  wavelengths, the quaternary  $\text{In}_{0.72}\text{Ga}_{0.23}\text{As}_{0.61}\text{P}_{0.39}$  can be grown lattice-matched to InP.

### **6.2.2.1 Preliminary Work**

Preliminary results for the growths of these materials have been undertaken. In order to calibrate the composition, RHEED calibration were used to roughly measure In and Ga growth rates. To complete the calibration procedure an x-ray sample, as shown in Figure 6-2, was grown with both the quaternary and strained InGaAs in order to simultaneously measure each component. Photoluminescence measurements were taken for  $\text{In}_{0.72}\text{Ga}_{0.23}\text{As}_{0.61}\text{P}_{0.39}$ , where a growth temperature of 525°C produced the highest intensity. The dependence of the P mole fraction was measure with varying A-BEP at a P-BEP of  $6 \times 10^{-6}$  Torr.



**Figure 6-2.** InGaAsP x-ray calibration sample and x-ray rocking curve showing the strained InGaAs peak and InGaAsP closely latticed-match peak.



**Figure 6-3.** Dependence of phosphorus incorporation in InGaAsP with arsenic BEP at a phosphorus BEP of  $6 \times 10^{-6}$  Torr.

#### 6.2.2.2 Proposed Device Structure

The incorporation of the quaternary  $\text{In}_{0.72}\text{Ga}_{0.23}\text{As}_{0.61}\text{P}_{0.39}$  in the SACM structure as the absorption layer is proposed in the structure shown in Figure 6-4.

30nm p+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	
30nm p+ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	
400nm p $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
50nm u.d. graded $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
1000nm u.d. $\text{In}_{0.72}\text{Ga}_{0.28}\text{As}_{0.61}\text{P}_{0.39}$	
50nm u.d. graded $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
150nm p $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
800nm u.d. $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
800nm n+ $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$	
n-InP substrate	
AuGe/Ni,Au n-contact	

10nm p+ $\text{In}_{0.53}\text{Al}_{0.40}\text{Ga}_{0.08}\text{As}$ digital alloy
10nm p+ $\text{In}_{0.53}\text{Al}_{0.32}\text{Ga}_{0.16}\text{As}$ digital alloy
10nm p+ $\text{In}_{0.53}\text{Al}_{0.24}\text{Ga}_{0.24}\text{As}$ digital alloy
10nm p+ $\text{In}_{0.53}\text{Al}_{0.16}\text{Ga}_{0.32}\text{As}$ digital alloy
10nm p+ $\text{In}_{0.53}\text{Al}_{0.08}\text{Ga}_{0.40}\text{As}$ digital alloy

**Figure 6-2.** Proposed InGaAsP-InAlAs SACM APD structure.

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## **Vita**

Jeffrey Byron Hurst was born in Dallas, Texas on March 20, 1977, the son of Robert Byron Hurst and Dolores Laverne Hurst. After graduating from Duncanville High School he entered the University of Oklahoma in Norman, Oklahoma, where he received a Bachelor's degree in Electrical Engineering in May 1999. In August 1999 he entered the University of Texas at Austin, where he received a Master's degree in Electrical Engineering (Solid-State Electronics) in May 2001 and continued to pursue his Ph.D. in Electrical Engineering.

Permanent address: 2202 Corbin Way, Cedar Park, TX 78613

This dissertation was typed by Jeffrey B. Hurst