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Process Development, Characterization, Transient Relaxation, and Reliability Study of HfO_2 and $HfSi_xO_y$ Gate Oxide for 45nm Technology and Beyond

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Process Development, Characterization, Transient Relaxation, and Reliability Study of HfO_2 and $HfSi_xO_y$ Gate Oxide for 45nm Technology and Beyond

by

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Dissertation

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Dedication

To my wife, parents and my younger brother

Acknowledgements

Firstly, I would like to give honor to God who is always the head of my life. Through His undying and everlasting love for us, He has given me the desire, ability, and love to become motivated and inspired to reach the goals of my life.

I think if I honestly reflect on who I am, how I got here, what I think I might do well, and so forth, I discover a debt to my supervisor, Dr. Jack C. Lee for his constant supervision, encouragements, invaluable suggestion, timely assistance and guidance toward the completion of this work. His depth and breadth of knowledge in research inspired me to explore the world. His patience and calm guidance in the hard parts of my research work made me thankful to him. I would also like to thank Dr. Sanjay K. Banerjee, Dr. Paul Ho, Dr. Dodabalapur, and Dr. Frank Register for accepting to serve on my doctoral committee and spending their valuable time in guiding and suggesting in my work.

This is my opportunity to dedicate and share with the world, the in-depth love and compassion I have for you, my wife. What a powerful, dedicated, devoted, and loving woman you are, just only to me. May this work be a tribute to you, and not shame you in any manner. There are two other angels in my life that urged me on by way of their untiring support, all-time prayers and seemingly unlimited belief in me.

Thank you Abbu (Dad) and Ammu (Mom) for your moral support staying far and far away from me. Without your well-wishes, I would never reach such an extent. Thanks to my younger brother, Topu for his support and appreciation throughout my work.

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Process Development, Characterization, Transient Relaxation, and Reliability Study of HfO_2 and $HfSi_xO_y$ Gate Oxide for 45nm Technology and Beyond

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Silicon CMOS technology has been advancing along an exponential path of aggressively shrinking device dimensions, increasing density, increasing speed, and decreasing cost. Although providing huge benefits in microprocessor performances, advances in technology are accelerating the onset of causing enormous challenges in device integration and reliability. With device miniaturization, device design and process errors are shrinking, which in turn impact device characteristics and reliability. To keep pace with aggressive scaling, CMOS conventional SiO_2 gate oxide are facing tremendous challenges in power consumption and reliability. Aggressive scaling of SiO_2 pushed the technology down to the limit of direct tunneling regime, where the gate oxide leakage current increases exponentially as the thickness decreases. Thus the high

performance is coming from sacrificing both static and dynamic power of the circuits. Scaling up to 65nm technology node, use of SiO_2 and SiO_xN_y based dielectric barely met the ITRS roadmap. But keeping the same architecture with the same material we can't meet the 45nm technology gate oxide thickness and leakage current requirements. Therefore high-k dielectrics, of which HfO_2 and their silicates are most promising candidates, have attracted a great deal of attention recently. However, high-k dielectrics have also faced lots of integration challenges and issues that are needed to be resolved carefully before pushing it in production. For example, bulk charge trapping, interface states, degraded mobility, growth of interfacial layer, low crystallization temperature, dielectric phase separation, fermi pinning, soft optical phonon scattering, remote coulomb scattering, pre-existing traps are among those issues. In this research, process development, characterization and reliability study of HfO_2 and its silicate have been performed. It has been observed that both nitrogen (N) and chlorine (Cl) have significant effect in improving the device performances. Incorporation of nitrogen by NH_3 post-deposition anneal reduced EOT (effective oxide thickness), and improved device characteristics, like I_d-V_g, I_d-V_d characteristics, and mobility. On the other hand, surface nitridation using NH_3 was found to be an effective way to aggressively scale down the EOT. Moreover, Cl treatment using precursor, $HfCl_4$ pulse time variation in ALD (atomic layer deposition) HfO_2, and using HCl as high-k post deposition rinsing element, both mobility and bias instabilities of high-k oxides could be improved.

Reliability of Hf-based oxide could be improved by compositionally varying $HfSi_xO_y$ structure. Fabricating Hf-silicate with low composition of Si on top of Hf-

silicate with high composition of Si not only enhanced the device performance, but also improved the reliability characteristics. Furthermore, insertion of Si in the HfO_xN_y dielectric was found to be an effective way to improve device performance and reliability. At the end, a novel approach in understanding the breakdown mechanism of HfO_2 has been proposed by stress-anneal experiments. It was found that accumulation of holes is primarily responsible for breakdown of HfO_2 under substrate injection condition. An appropriate model has also been proposed along with supporting experimental data.

Considering all of the process development, characterization and reliability studies made in this research, it can successfully be asserted that high-k gate oxide can be proposed as a viable and promising candidate for 45nm technology and beyond. But still careful attention need to be taken to resolve remaining intrinsic and extrinsic issues in high-k gate oxide.

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Chapter 1

Introduction

Since the early 1970s, we have witnessed a relentless drive toward smaller features of CMOS transistors and hence higher functionality on semiconductor chips. The remarkable characteristic of transistors that fuels the rapid growth of the semiconductor industry is that their speed increases and their cost decreases as their size is reduced. To meet the requirement of high performance, high reliability, high package density along with low voltage and low power application for future CMOS technology nodes, device scaling has acted as the driving force. The ability to improve performance consistently while decreasing power consumption has made CMOS architecture the dominant technology for integrated circuits. The scaling of the CMOS transistor has been the primary factor driving improvements in microprocessor performance. The rapid device scaling is generally governed by Moore's law. It is important to understand the key principles underlying Moore's law, since these allow us to gain insight into the future. The observation made by Gordon Moore in 1965 was that the number of components on the most complex integrated circuit chip would double each year for the next 10 years [1]. Several forms of scaling like constant field scaling [2], constant voltage scaling, constant electrostatic scaling can be followed. Each of them has its own advantages and disadvantages. The basic premise of the Roadmap is that continued scaling of microelectronics will further reduce the cost per

function (historically, ~25%/year) and promote market growth for integrated circuits (averaging ~15%/year). Thus the Roadmap is put together in the spirit of a challenge- essentially: "What technical capabilities need to be developed for us to stay on Moore's Law?" During the 1980s and '90s, this challenge has become so formidable that more and more of the development effort has been shared in a pre-competitive environment including consortia and collaboration with suppliers. In this process, the roadmap serves as a guide to the principal technology needs. To keep track with the roadmap, rapid shrinking of feature size of transistor has forced the gate channel length and gate dielectric thickness as well to scale aggressively.

1.1. Basic Needs for Scaling

Followings are basic device scaling metrics as shown in fig. 1.1

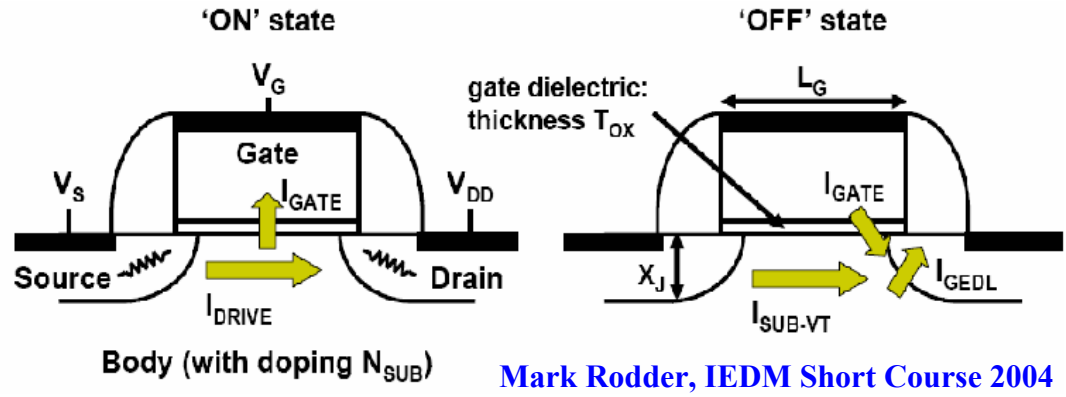


Fig. 1.1. Schematic representation leakage and drive current components of MOSFET devices at On and Off states.

a. Active Power = $(C_{TOTAL} \times V_{DD}^2 \times f) + (I_{GATE} \times V_{DD})$

b. Resistance, $V/I \alpha V_{DD} \times T_{OX}^{INV} / [(V_{DD}-I_D R_S-V_T) \times \mu_{eff}]$

c. Delay, $CV/I = C_{GATE} \times V_{DD}/I_D$

d. Static Power = $(I_{SUB} + I_{GATE} + I_{GIDL}) \times V_{DD}$

With scaling, L_{GATE} is decreasing. But delay can be written as

$CV/I = (C_{ox} \times A) \times V_{DD} / I_D$

$= (C_{ox} \times W \times L_{GATE}) \times V_{DD} / [(W/L_{GATE}) \times C_{ox} \times \mu_{eff} \times (V_{GATE}-V_{TH})^2]$

$= (L_{GATE}^2 \times V_{DD})/[\mu_{eff} \times (V_{GATE}-V_{TH})^2]$

Thus from the transistor point of view, gate delay reduces in proportion to the square of gate length, L_{GATE}. Moreover, to reduce gate delay or to increase speed of the device, operating voltage V_{DD} needs to be reduced as well. The other two parameters in the equation are effective mobility, μ_{eff} and threshold voltage, V_{TH}, which are needed to be enhanced and reduced respectively. Scaling has effect on speed mainly by an increase in the drive current, I_{Dsat} used both for logic and memory applications. Decreasing the channel length, gate oxide thickness or the threshold voltage can increase the drive current of a MOSFET. For logic applications, this means faster switching speeds while for memory applications like DRAM, it means faster write, erase and read cycles through the pass transistor. Thus, in short, scaling helps to increase the cheap density, reduce cost, enhance performance etc.

1.2 Scaling Challenges

As shown in the equation above, scaling of L_{GATE} needs to consider several other parameters for the device to function properly. The scaling challenges are as follows

a. L_{GATE} scaling needs the scaling of oxide thickness, T_{ox}, source/drain (S/D) junction depth, X_j, substrate concentration, $N_{SUB,}$ and operating voltage, V_{DD}

b. As N_{SUB} increases, μ_{eff} decreases due to increased channel scattering, and increase in gate oxide electric field

c. Short channel effects which reduces control of gate over the channel

d. Increase in I_{SUB}, I_{GIDL} current, which increases the static power

e. DIBL (drain induced barrier lowering), punch through, velocity saturation effects come into play

f. Increase in S/D resistance due to decrease in junction depth, X_j.

g. Since scaling boosts up speed, thus this frequency increase enhances active power

h. T_{ox} reduction increases gate leakage current, I_{GATE}, which increases the static power.

Hence it is seen that performance increase is achieved at the expense of active and static power.

1.3 Scaling Limitations in Current and Future Technology Nodes

As shown in fig. 1.2(a), scaling of L_{GATE} and T_{ox} is slowing with technology nodes. If the scaling of T_{ox} is slowed, it automatically slows down the scaling of L_{GATE} to keep pace with the short channel effects. Due to sluggishness of T_{ox} scaling, I_D<roadmap as shown in fig. 1.2(b). With this trend, it is difficult to meet the 45nm node target I_D if T_{ox} isn't scaled. For the same reason, V/I and CV/I are not at the roadmap targets for devices operating at low V_{DD} (fig. 1.2.c). On the other hand, the sub-threshold current, I_{SUB} exceeds roadmap targets as shown in fig. 1.3. Due to the increase in I_{SUB}, static power can exceed the active power as shown in fig. 1.4. To reduce the increase in active power, V_{DD} needs to be reduced as well. But as seen in fig. 1.5, V_{DD} is also falling behind the roadmap targets thus limiting the reduction of active power and increasing the electric field across the gate oxide, which decreases the reliability of gate oxides. Thus in short, it can be written that

a. Scaling of L_{GATE}, V_{DD}, and T_{ox} is already slowing from ITRS roadmap
b. It is difficult to meet 45nm node targets for V/I and CV/I without scaling of T_{ox}^{INV}
c. Leakage currents, I_{GATE}, I_{SUB} are already exceeding the roadmap
d. Due to increase in electric field across the gate oxide, effective mobility is decreasing too (fig. 1.6)
e. Performance is being achieved at the expense of power
f. Power is a problem

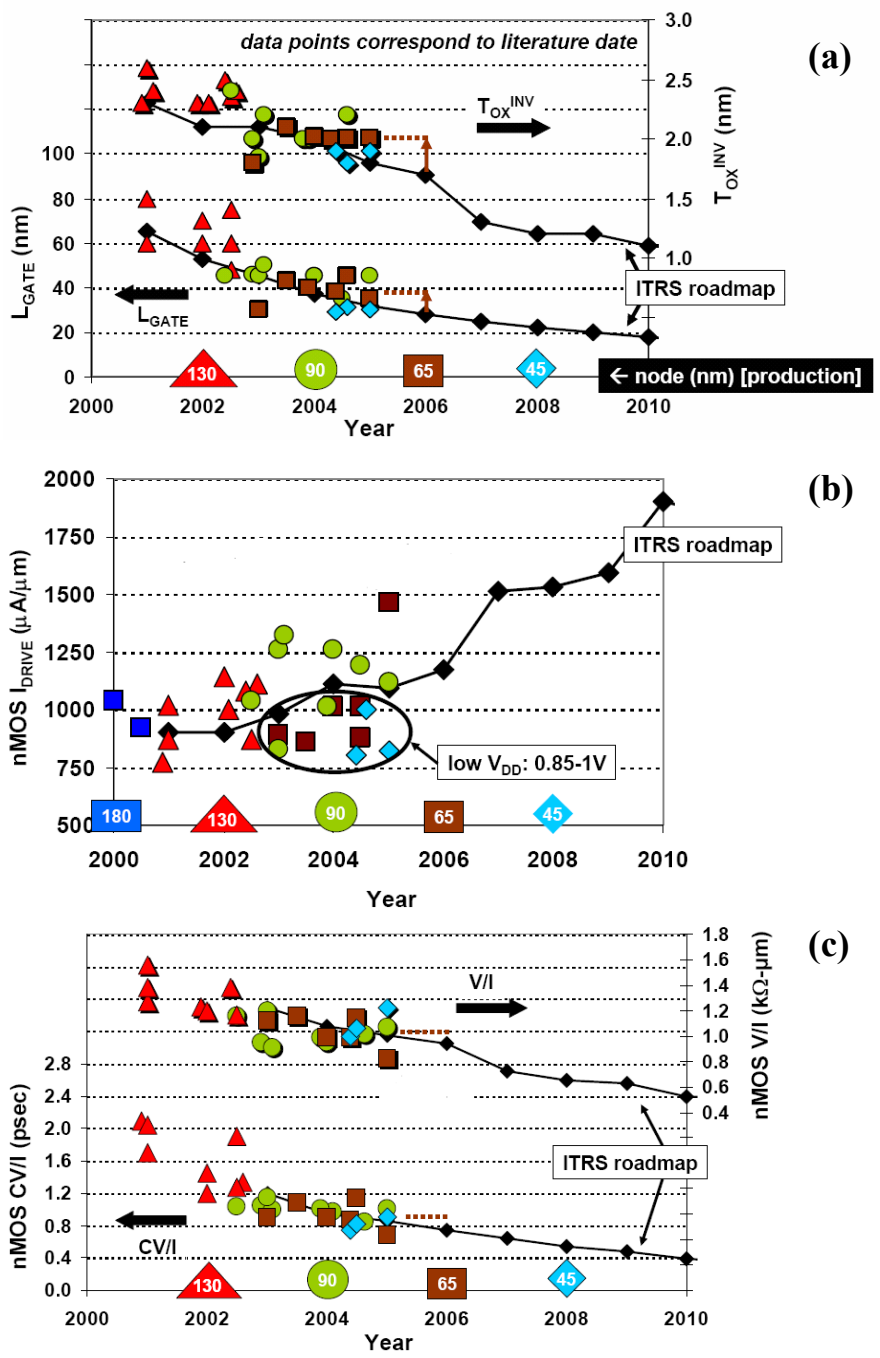


Fig. 1.2. For HP device, current scaling trend of (a) T_{ox} and L_{GATE}, (b) NMOS I_D, (c) V/I and CV/I with technology nodes (from Mark Rodder, IEDM short course 2004)

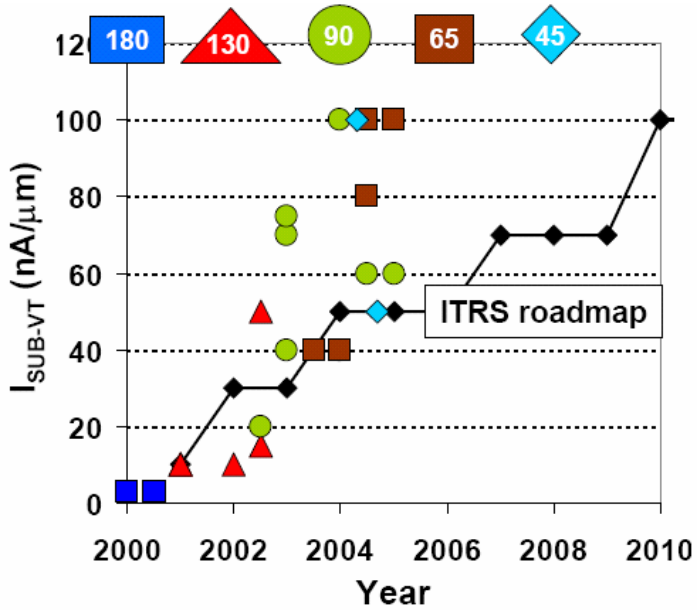


Fig. 1.3. Scaling of sub-threshold current with technology nodes [63]

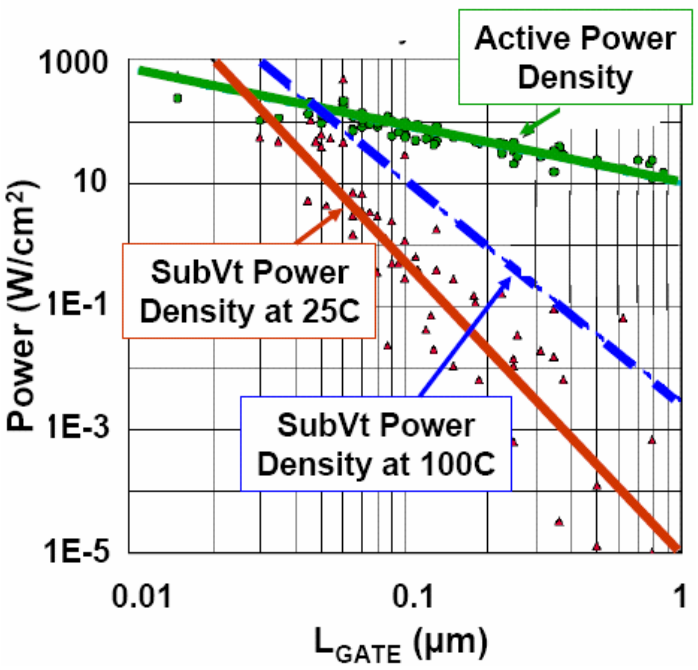


Fig. 1.4. Active and Static power increase with scaling of L_{GATE} [63].

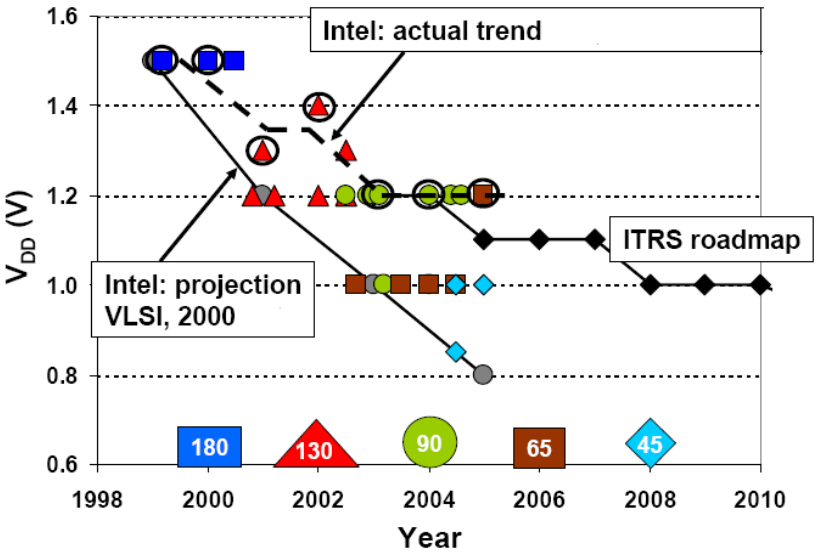


Fig. 1.5. Scaling of V_{DD} with technology nodes. V_{DD} scaling is below the targets, thus increasing the electric field in the oxides [63].

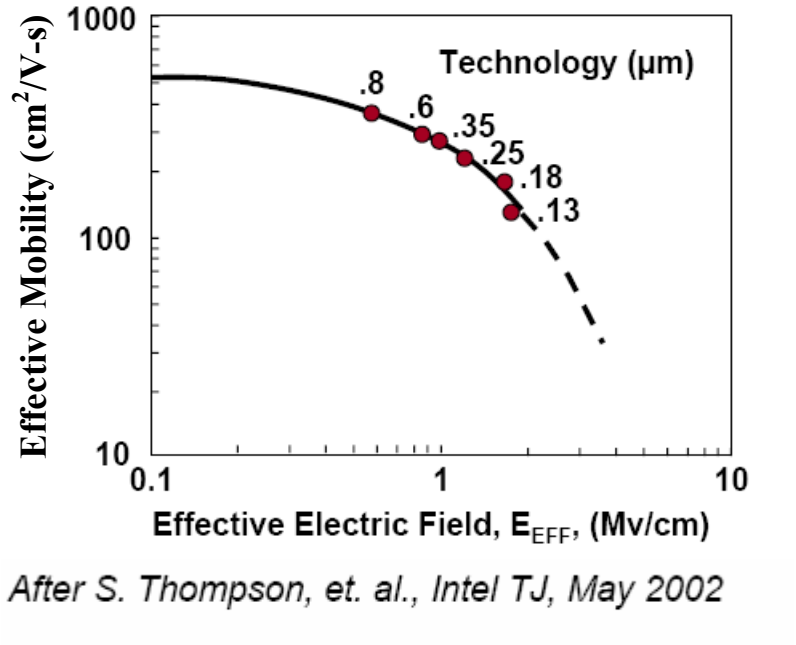


Fig. 1.6. Decreasing effective mobility trend with technology nodes due to the increase in effective electric field in the gate oxide.

The EOT requirement has set big challenge in reducing the dimension and demands for new technology and new materials. So there exists a trade off between device scaling and power. For example, scaling the horizontal device dimension has the adverse effect of "Short Channel" effect, which includes reduction of threshold voltage, DIBL, punch through and decrease in drive current improvement due to velocity saturation. On the other hand, though vertical scaling has the advantage of smaller channel depletion layer, controlled short channel effects [3], more control over channel and better subthreshold slop, it threatens mobility and reliability of the device.

So there are some of the fundamental scaling limits that need to be overcome:

- Scaling limit of SiO_2 gate dielectric
- Quantum Mechanical effect
- Poly depletion effect
- V_{th} non-scalability and fluctuation
- Mobility degradation
- Increase in S/D resistance
- I_{off} non-scalability

The first three limits demand a strong need for replacing conventional gate dielectrics with alternative high-k gate dielectric materials and will be discussed in detail. The last four limits however, are related to the transistor S/D structure and the device's fundamental limitation. For example, high S/D resistance is due to shallow

junction; mobility degradation is due to increased substrate doping concentration; and I_{off} non-scalability is due to non-scalable diffusion current.

1.4 Gate Oxide Scaling

Gate oxide thickness scaling has been instrumental in controlling short channel effects as MOS gate dimensions have been reduced from 10um to 0.1um. Gate oxide thickness must be approximately linearly scaled with channel length to maintain the same amount of gate control over the channel to ensure good short channel behavior. Fig. 1.7 plots the electrical channel length divided by gate oxide thickness for Intel's process technologies over the past 20 years. Each data point represents a process technology, developed approximately every three years, which was used to fabricate Intel's leading-edge microprocessors.

From fig. 1.8, a simple relationship between oxide thickness and the minimum channel length set by short channel effects is observed

$L_E = 45 * T_{OX}$

This relationship exists because the channel depletion layer is engineered to become smaller as the gate oxide thickness is decreased. In addition, short channel behavior is governed by the ratio of channel depletion layer thickness to channel length. The channel depletion layer is inversely proportional to the square root of the channel doping concentration. During device optimization, channel doping is increased as the

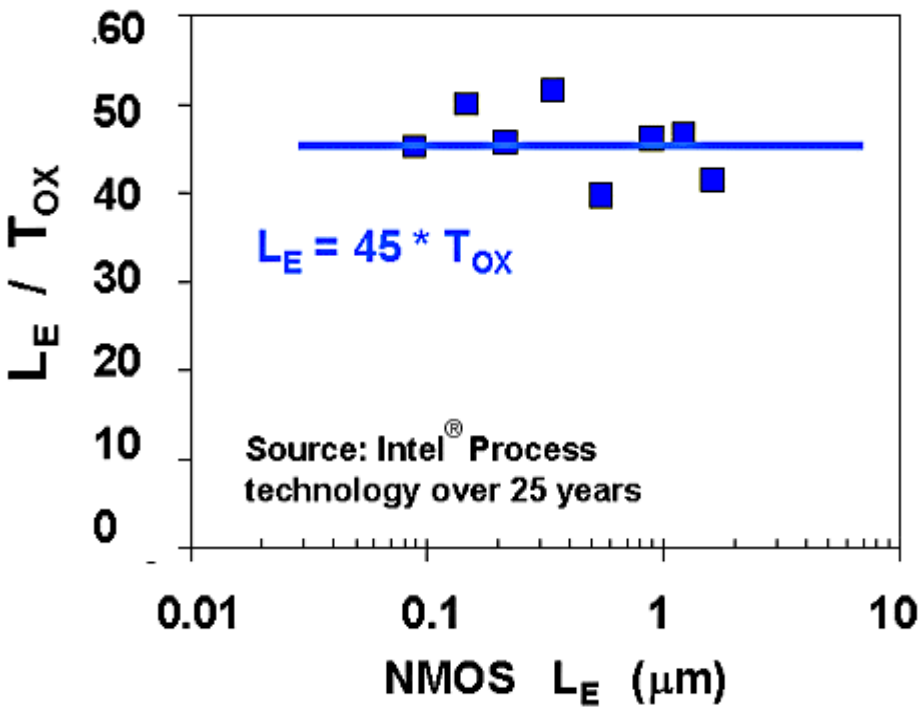


Fig. 1.7. Channel length divided by gate oxide thickness versus channel length

oxide is scaled to maintain approximately the same device threshold voltage. Fig. 1.8 illustrates this point. In Fig. 1.8, the thickness of the channel depletion layer for two devices with different oxide thickness is shown. Fig. 1.8(a) shows the depletion layer for a device with an oxide thickness of 4.5 nm while Figure 1.8(b) shows a device with an oxide thickness of 3.2 nm.

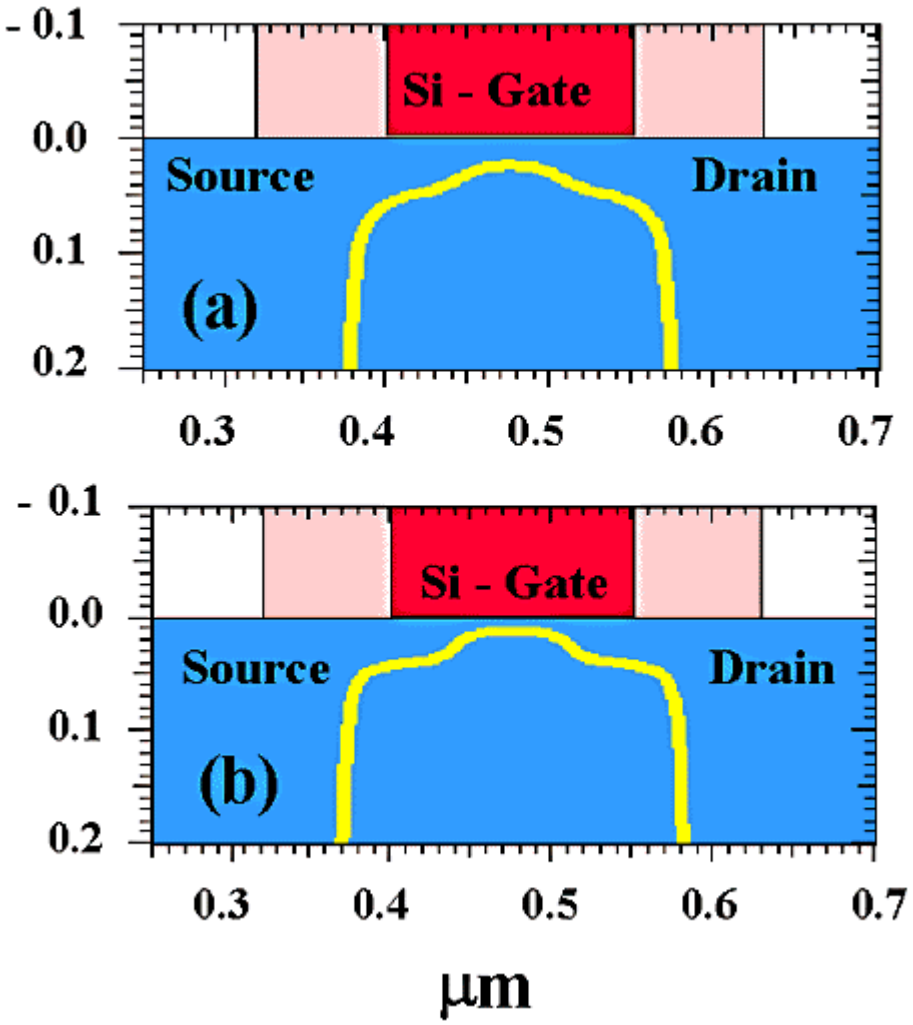


Fig. 1.8. Device simulations showing channel depletion layer thickness for devices with two oxide thicknesses: (a) 4.5 nm, (b) 3.2 nm

Both devices have the same off-state leakage. The device with the thinner oxide has a smaller channel depletion layer and hence improved short channel characteristics. The improved short channel effects can be taken advantage of by targeting a smaller channel length. Thus for continued MOS channel length scaling, the gate dielectric

thickness must continue to be scaled. Fig. 1.9 shows the Semiconductor Industry Association's (SIA) road map for gate dielectric thickness. This roadmap predicts that continued gate dielectric scaling will be required with a new gate dielectric material needed for the 2005-2012 time frames.

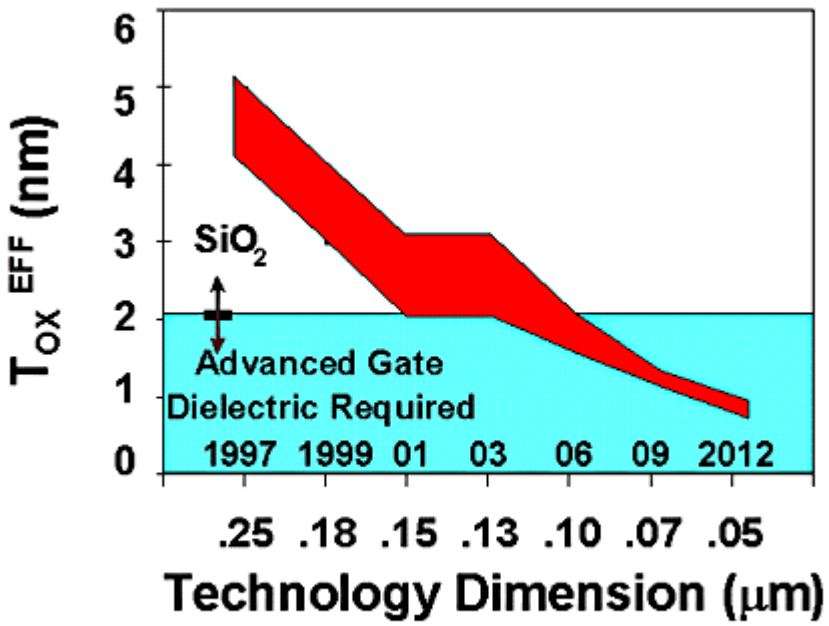


Fig. 1.9. SIA road map predicts that there is need for alternative material for gate oxde to meet the T_{ox}^{EFF} requirements.

1.5 Scaling Limitation for SiO_2

SiO_2 has been the gate dielectric used by the semiconductor industry for over 30 years. It has been used as primary gate dielectric material in field effect devices due to good interface, low leakage currents and excellent thermal stability at typical silicon process temperatures. SiO_2, which has been used since 1957, has been scaled down successfully with great effort towards current technologies of 0.13-0.18μm, but not without slight modifications. Over the last several years, silicon oxynitride, grown thermally or using rapid thermal annealing (RTA) and with EOT of around 18~25Å, has been used in manufacturing to replace conventional SiO_2. However further thickness scaling of SiO_2 or oxynitrides is necessary which faces serious challenges.

The thickness limit is the same for both materials and is not limited by manufacturing control. Today, it is technically feasible to manufacture 1.5 nm and thinner oxides on 200 mm wafers [4]. The thickness limit for SiO_2 is set instead by gate-to-channel tunneling leakage. Fig. 1.10 schematically shows the tunneling leakage process for an NMOS device biased in inversion.

As the thickness of the dielectric material decreases, direct tunneling of carriers through the potential barrier can occur. Because of the differences in height of barriers for electrons and holes, and because holes have a much lower tunneling probability in oxide than electrons, the tunneling leakage limit will be reached earlier for NMOS than PMOS devices. The SiO_2 thickness limit will be reached approximately when the gate

to channel tunneling current becomes equal to the off-state source to drain sub-threshold leakage (currently ~1nA/um).

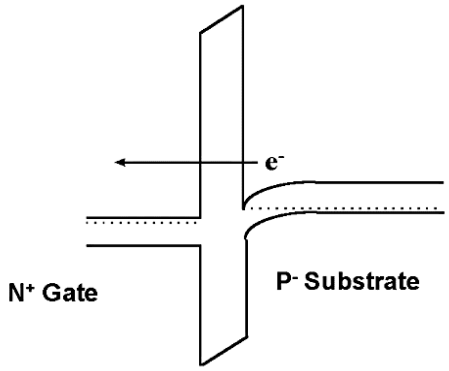


Fig. 1.10. Direct tunneling leakage current mechanism for thin SiO_2

Fig. 1.11 shows the area component of gate leakage current in A/cm^2 versus gate voltage. If we assume the gate leakage limit occurs for devices with 0.1um gate length designed for 1.0V operation, the SiO_2 thickness limit occurs at ~1.6 nm.

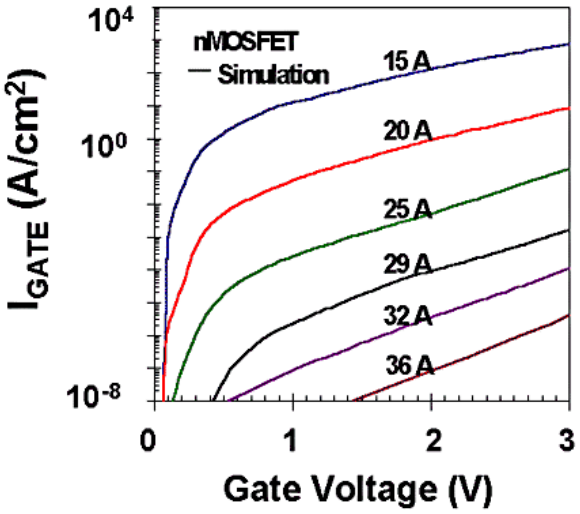


Fig. 1.11. Gate leakage vs. gate voltage for various oxide thicknesses [5]

Beyond this limit, it is unrealistic to use SiO_2 since the direct tunneling current is too high. The leakage current density will exceed the roadmap if we continue to scale down SiO_x based gate oxide (fig. 1.12). This is why T_{ox} decrease is slowing down (fig. 1.13).

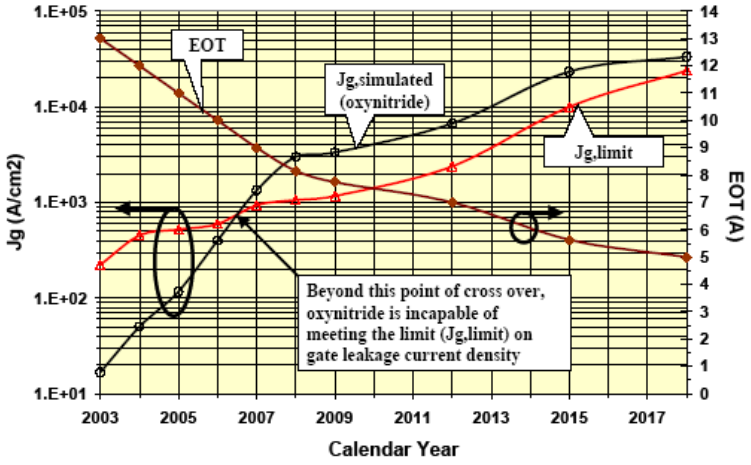


Fig. 1.12 ITRS 2004 (Updated) for leakage current density and EOT with technology nodes. There is a cross over point beyond which J_g will exceed the limit if we use oxinitride based gate oxide.

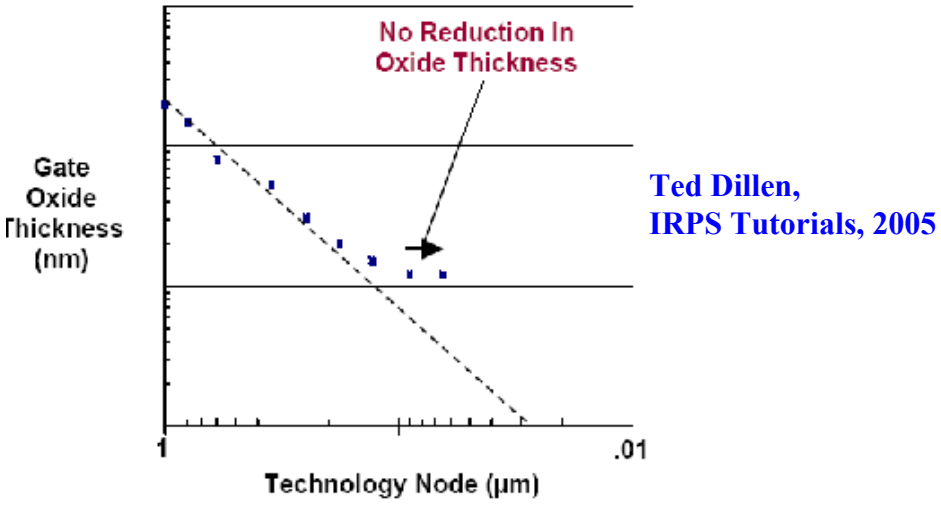


Fig. 1.13. Gate Oxide thickness scaling trend with technology nodes

We now have established that the thickness limit for SiO_2 is ~1.6 nm. However, due to quantum mechanical and poly-Si gate depletion effects, both the gate charge and inversion layer charge will be located at a finite distance from the SiO_2/Si interfaces with the charge location being a strong function of the bias applied to the gate. Fig. 1.14 shows the location of the inversion layer charge in the silicon substrate for a transistor with a typical bias when quantum mechanical effects are taken into account [6]. The centroid for the inversion charge is ~1.0 nm from the SiO_2/Si interface.

This increases the effective SiO_2 thickness (T_{OX}^{EFF}) by ~0.3 nm. By taking into account the charge distribution on both sides of the gate, the minimum effective oxide thickness for a MOS device bias in inversion (at voltages used in our 0.25 or 0.18um technologies) is increased by approximately 0.7 nm. Thus the 1.6 nm oxide tunneling limit results in an effective oxide thickness of approximately 2.3 nm.

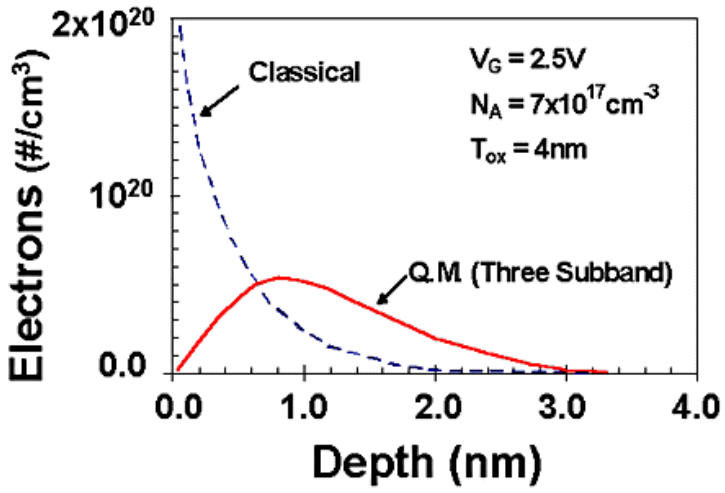


Fig. 1.14. Position of inversion channel charge versus depth of channel

On the other hand, tunneling current J increases exponentially with decreasing physical thickness of SiO_2 [8]. This degrades standby power dissipation and DRAM retention time, add to SRAM power consumption, offset designs for SRAM beta-ratio, reduce noise margin, and accelerate device degradation [9]. The standby power consumption of a CPU due to gate leakage is approaching to transistor off-state current (I_{off}) as the technology node shrinks (fig. 1.15) [10]. It has been shown that for T_{ox}<15Å, the leakage current densities of gate oxide are around 1-10A/cm^2 [11]. While this may still be tolerable for high performance applications such as microprocessors (requirement is < 1A/cm^2 [7]), they are orders of magnitude higher than acceptable leakage levels for low power applications such as wireless systems (which is of the order of 1mA/cm^2 [7]).

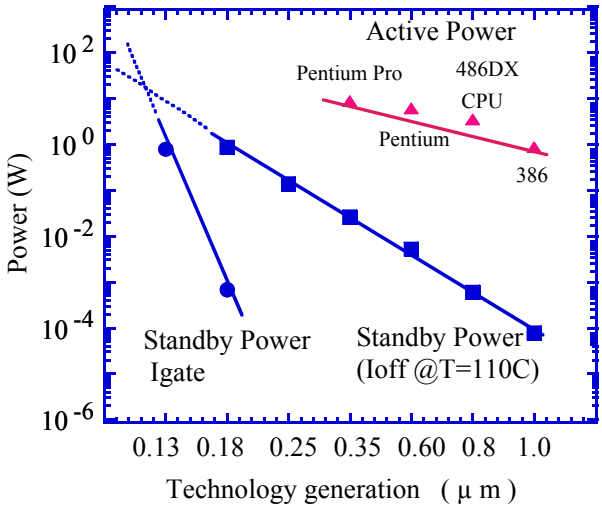


Fig. 1.15. Power consumption of CPU as a function of the technology nodes. The standby power is fast approaching due to I_{off}.

Another significant limitation to further scaling of the gate oxide is the thickness control and film quality. Considering for example that a 12Å SiO_2 would only be 3-4 monolayers of the oxide, the manufacturing implications of producing these films uniformly over 200 or a 300mm wafer is a substantial concern [12].

In addition to the above-mentioned problems, the issues of boron penetration [13] through the ultra-thin oxide and other reliability factors are a significant concern. A higher concentration of boron in the channel region causes severe V_t shifts and alters device properties in an unacceptable way [14]. As the oxide thickness reduces, lifetime prediction also becomes a serious issue.

Though polysilicon has been used successfully as a gate electrode due to its high thermal stability and compatibility, the issue of poly depletion effect has adverse effect on its suitability. With aggressive scaling, demand for shallow source and drain junction necessitates low thermal budget, which adversely reduces dopant activation temperature of polysilicon gate. The insufficient dopant activation at the poly and oxide interface results in a depletion layer due to inverted charges of the substrate. The depletion effect becomes more severe as the gate oxide becomes thinner by 3-5Å [15-16]. This depletion results in increased effective oxide thickness, increased V_t, degraded drive current, and also sensitivity to the doping concentration of the poly at the poly-oxide interface [17].

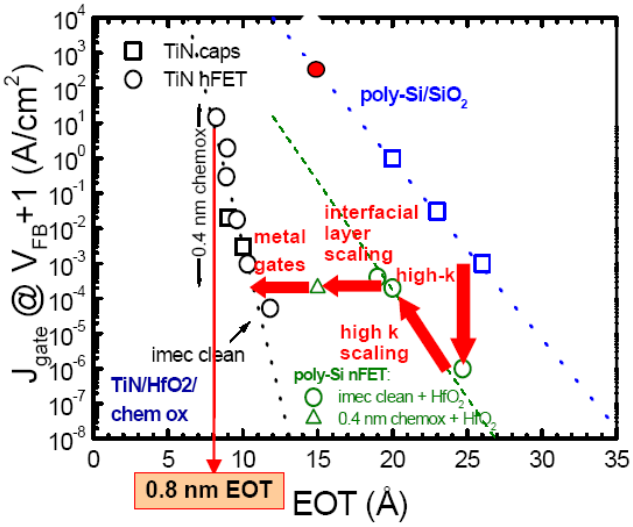
1.6 Motivation to High-k Gate Dielectrics

If we take a look at ITRS 2004 (updated) [7] in table 1.1, then we can find that the leakage current requirements for 45nm technology node (to be in production in 2007) and beyond can't be met with the existing SiO_xN_y based gate oxides with aggressive scaling of EOTs [7].

Calendar Year	2003	2004	2005	2006	2007	2008	2009
EOT	0.8	0.8	0.7	0.7	0.4	0.4	0.4
EOT (inv)	2.1	2	1.8	1.7	1.3	1.2	1.2
Jg (Amp/cm2)	2.50E+02	4.50E+02	5.20E+02	6.00E+02	9.30E+02	1.10E+03	1.20E+03
Idsat(mA/mm)	980	1110	1090	1170	1510	1530	1590
Mobility/Gm Imrov. factor	1	1.3	1.3	1.4	2	2	2

Table 1.1: ITRS 2004 (updated) for EOT, J_g and Mobility requirements.

As shown in fig. 1.16, with high-k dielectrics, leakage currents and EOT could be met using high-k dielectrics with metal gate electrodes.



Stefan De Gendt, IMEC IEDM Short course, 2004

Fig. 1.16. J_g vs. EOT curves showing scalability of high-k dielectrics with metal gates in comparison to SiO_2 with poly gates.

Thus high-k dielectrics are very critically important to meet the technology demands in near future. The following figure (fig. 1.17) shows the advantage of using high-k in reducing the leakage current of the devices.

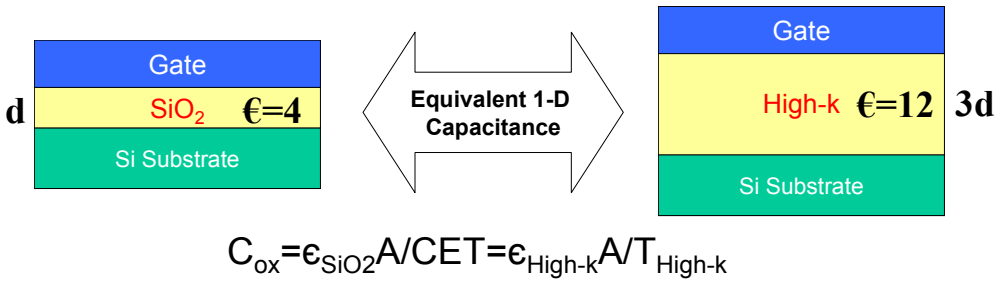


Fig. 1.17. Schematic Diagram showing SiO_2 and High-k based gate oxides. It could be made physically thicker for the same capacitance.

As shown, high-k dielectrics can be used to get the same equivalent thickness from a physically thicker film. The leakage current depends on the height and width of the barrier height. With high-k dielectrics, the width of the barrier height can be increased significantly reducing the leakage current with the same EOT. Due to thicker physical thickness, the reliability of the films may be improved.

1.7. Trade-Off between k-value Increase and E_g Decrease in High-k Dielectrics

Fig. 1.18 shows schematically why k-values are higher for high-k materials. High-k gate oxides are usually composed of high atomic number elements, typically transition metals. Dielectric constants come from polarizability of the material. Two components that contribute to polarization are electronic and ionic polarizability. Electronic polarizability is the ability to create charge dipole in electron cloud around atoms in material by applying external field. Ionic polarizability is the ability to shift ionic positions of the lattice.

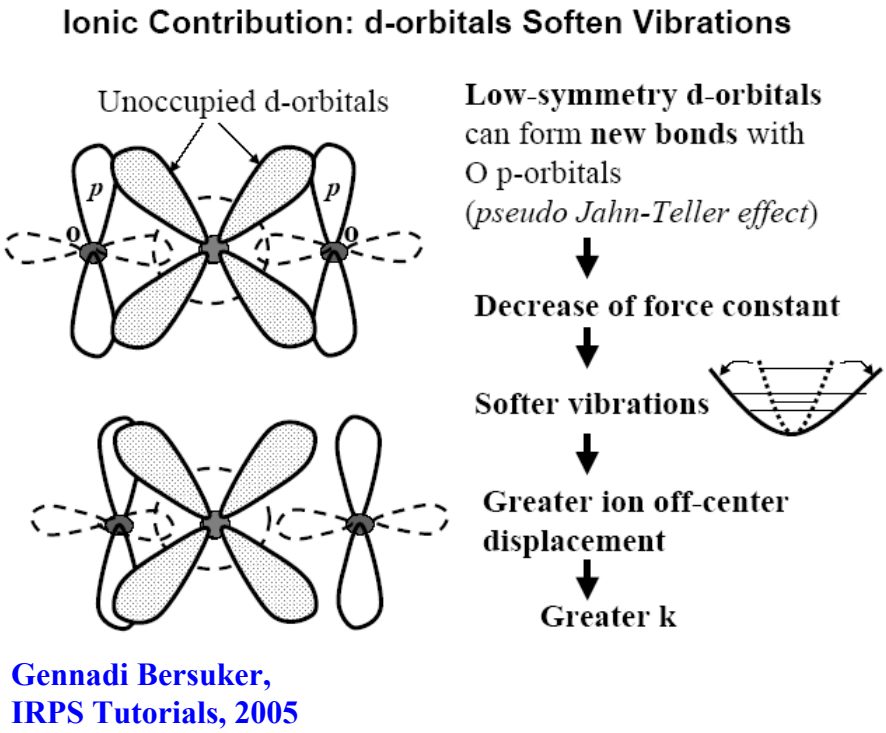
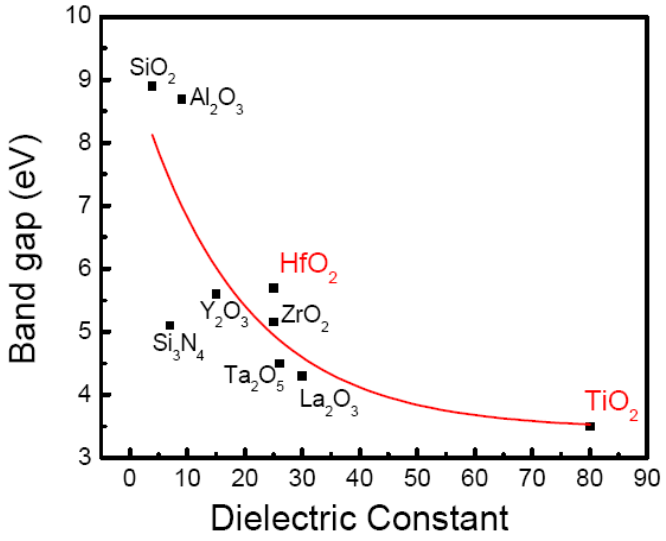


Fig. 1.18. Schematic representation of reasons behind high-k values in high-k materials

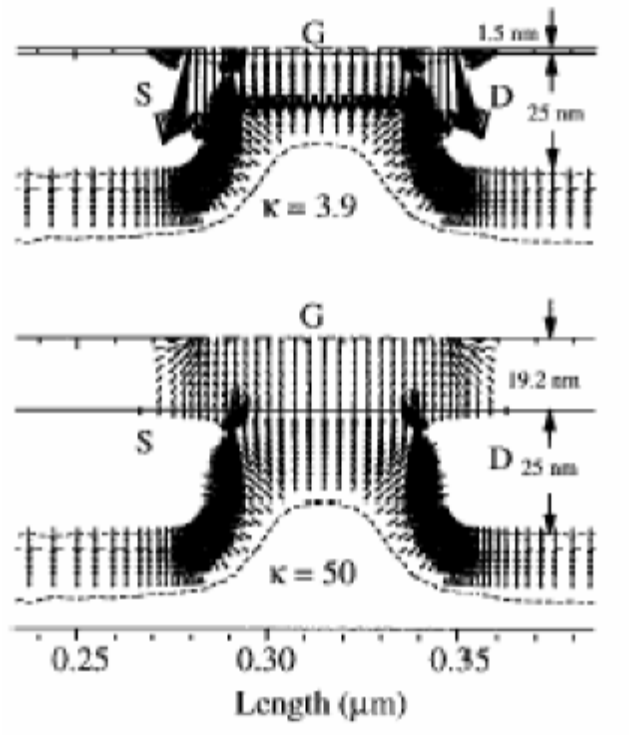
On the other hand, with the increase in k-values, the dielectric band gap, E_g (and so conduction band offsets) of high-k materials decreases as shown in fig. 1.19 [18].



G. D. Wilk et. al., JAP, vol. 89, pp. 5243

Fig. 1.19. Band gaps vs. dielectric constants of materials. Both band gaps and band offsets decreases as k-value increases.

As stated previously, high-k oxides mean using high atomic number elements (typically transition metals). Transition metals contain partially filled atomic d-orbitals which form levels with high density of states within the oxide band gap (between bonding and anti-bonding atomic energy levels). These d orbitals reduce band gap. So very high-k materials don't bring benefit in terms of leakage current reduction. Moreover, field induced barrier lowering also increases as k value increases (fig. 1.20). Fig. 1.21 summarizes energy gaps and band offsets of different potential high-k materials.



B. Chen et. al., Trans. Elec. Dev., vol. 46, pp. 1537 [17].

Fig. 1.20. FIBL (field induced barrier lowering) effect in very high-k materials due to fringing fields from the gate.

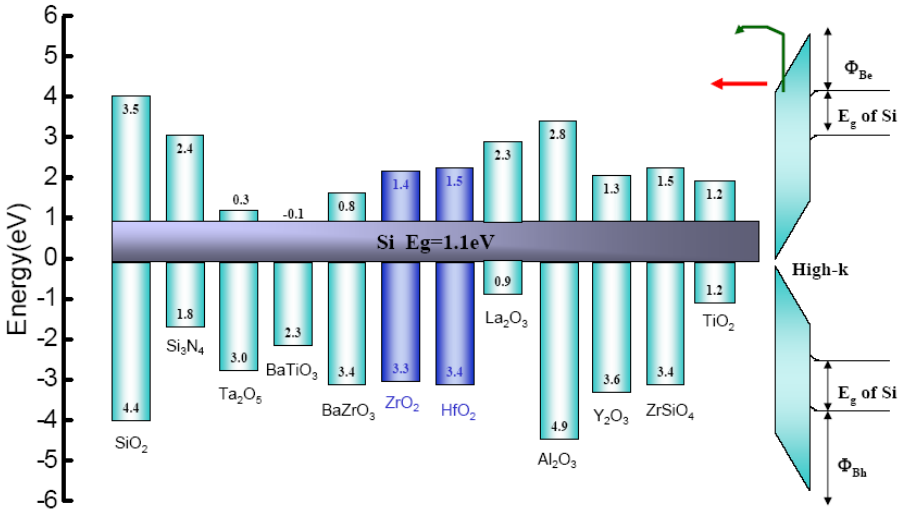


Fig. 1.21. E_g and band offsets of different potential high-k materials

1.8 Requirements for High-k Dielectrics

It has been proved that SiO_2 is the best material as an interface between Si-SiO_2 and good compatibility. So to be compatible with Si substrate, high-k dielectric should have possessed the following features:

Electrical Characteristics

- CMOS compatibility
- High enough dielectric constant, but not too high [17,18]
- High enough bang-gap and band offsets with silicon
- Good scalability
- Low leakage currents
- Reduced charge trapping characteristics and SILC (stress induced leakage current) as compared to SiO_2
- Very few electrically active trap sites (pre-existing charge traps) in the bulk and have good interface with silicon
- Small fixed charge at the Si/high-k interface as compared to SiO_2
- Negligible frequency dispersion and C-V hysteresis

- High drive current and mobility characteristics
- Good subthreshold characteristics
- No fermi pinning with poly-Si or metal electrode
- Uniform V_{th} for nMOS and pMOS (ie. Good V_{th} controllability)

- High reliability at operating conditions

Physical and Chemical Characteristics

- Thermodynamic and chemical stability in contact with Si
- High crystallization temperatures (>900°C)
- Low oxygen diffusivity in order to avoid formation of low-k interface layers
- Coefficient of thermal expansion similar to that of Si (for low mechanical stress)
- Low defect concentrations at the interfaces with Si
- Resistance to impurity and dopant diffusion at high temperatures
- Small process complexity
- Good adhesion property
- Easy etch capability
- No phase separation
- Smooth surface roughness

1.9 Researches on High-k Dielectrics

Several high-k dielectrics have been proposed as alternative to SiO_2 gate oxide such as Si_3N_4 [19], ferro-electric materials such as ferroelectric titanates ($Ba_xSr_{1-x}TiO_3$ and $SrTiO_3$) [20-21], metal oxides such as Ta_2O_5 [22-23], TiO_2 [24-24], Al_2O_3 [26-27], ZrO_2 [28-29], and HfO_2 [30-33]; and silicates such as $HfSi_xO_y$ and $ZrSi_xO_y$ [34-37]. N incorporation using NH_3, NO, N_2O has been studied extensively and they not only

raised the dielectric constant slightly (k ~ 5.5), depending on nitrogen content [38,39], but also had the added benefits of improved reliability, increased resistance to boron penetration, and better interfacial quality [40]. Unfortunately these dielectrics will only last a few generations due to limitations dictated by low power applications and scalability. Ta_2O_5, TiO_2 have high dielectric constant, but the band alignment is not favorable. For Ta_2O_5 it is 0.28eV and that of TiO_2 is 0.4eV. So it is difficult to reduce the leakage of these materials. Also interfacial layer thickness is large for those. Though Al_2O_3 has high band gap and band alignment, dielectric constant is low (<8) which offsets the advantage of high band-gap and ultimately resulting in higher leakage and leakage increases abruptly as EOT scales below 10Å. Y_2O_3 had drawn considerable attentions decades ago as alternative gate dielectrics to replace SiO_2. But with the gradual improvement of the quality of SiO_2 by incorporating N into the film, Y_2O_3 fell apart to compete with nitrided SiO_2 film. On the other hand Hubbard and Schlom [41] studied the thermal stability of several dielectrics in contact with Si using Gibbs free energy for silicidation and for dissociation to metals according to the equation

$$Si + MO_x \rightarrow M + SiO_2 \qquad \text{(dissociation)}$$

$$Si + MO_x \rightarrow MSi_z + SiO_2 \qquad \text{(silicide formation)}$$

The free energies of these reactions suggest that while Ta_2O_5 can dissociate into metallic Ta, TiO_2 forms a silicide. On the other hand, these reactions are not favorable

for oxides and silicates of Hf and Zr. Thus the candidate materials for alternative gate dielectric application have been narrowed down to HfO_2, ZrO_2 and their silicates film recently. Fig. 1.22 shows a comparative study of researches of promising high-k materials to date. HfO_2 and their silicates have been found to be the highest researched.

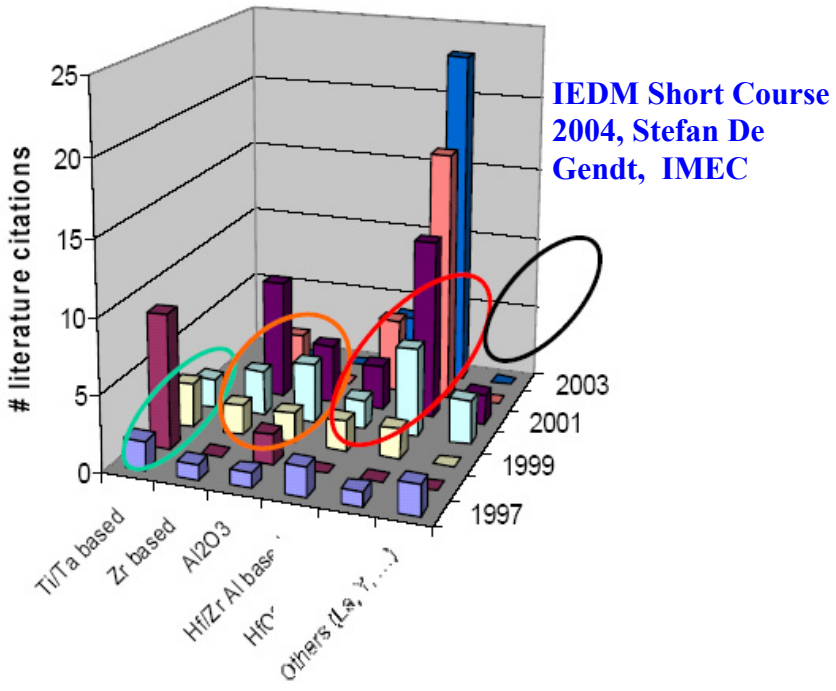


Fig. 1.22. Literatures on high-k researches. HfO_2 and their silicates are among the highest to date

1.10 Issues with HfO_2 and Hf-Silicate Dielectrics

Although extensive research has been done on the study many high-k materials, focus has been narrowed down to HfO_2, ZrO_2 and their silicates (fig. 1.22). Both Hf and

Zr are in column IV in periodic table, so they have almost similar chemical properties. Heat of formation is 271Kcal/mol for HfO_2 and 262Kcal/mole for ZrO_2 [42]. Band gap is 5.68eV [43] and 5.16eV [44] respectively, high enough to obtain sufficient barrier height. Despite some similarity between the two metal elements, HfO_2 is still a step ahead of ZrO_2 due to its compatibility with conventional polysilicon gate process. HfO_2 is thermodynamically stable with silicon substrate, high dielectric constant (~30), resistive to impurity diffusion because of its high density ($9.68g/cm^3$), lattice parameter similar to that of Si with a small lattice misfit (<5%) [45], low leakage, good reliability, good interface properties (D_{it}~10^{11} $ev^{-1}cm^{-2}$), with good lifetime (> 10 years). With some process modification, such as nitrogen incorporation on top [46], bottom [47] and throughout the film [48], showed much improved electrical properties in terms of scalability, thermal stability, reliability, and boron diffusivity etc.

However it has several drawbacks too. Low crystallization temperature (~600-700^0C) [49], large increase in EOT at high temperature due to interfacial layer growth [33], uncontrolled oxide formation at the Si/high-k interface, large hysteresis, fixed charge, charge trapping at the bulk, significant boron penetration, low channel mobility, and other reliability issues are the sources of serious concern [33, 50,51].

On the other hand SiO_2 is very well know for its compatibility with Si substrate due to excellent Si-SiO_2 bonding interface between Si and SiO_2. So to keep better interface properties and to resolve some of the above mentioned issues associated with HfO_2, recently research is being done on HfO_2 doped with Silicon, or $HfSi_xO_y$. By controlling the silicon composition carefully it has been shown that good electrical and

material properties could be obtained which solve some associated drawbacks with HfO_2. Briefly we can summarize some of the promising features of Hf-silicate ever explored

- Moderately high dielectric constant (13~25) [52, 56]. Its dielectric constant can be varied by controlling the composition of Si in the film.
- High Crystallization temperature, which is the most promising property of this film. With controlled Si composition it can go > 1000^0C [52, 56, 53] with smooth interface with Si substrate. Recently it has also been shown that by incorporating nitrogen in the film, this film remained stable up to 1100^oC [54, 55].
- Minimum interfacial layer, hysteresis in the range of 10-20mV, breakdown field E_{BD}~10MV/cm, mid-gap interface state density, D_{it}~10^{11} $eV^{-1}cm^{-2}$ [52,56].
- EOT as low as 13Å for polysilicon gate with nitrogen incorporated [54,55] and 10.8Å with TaN MOSCAP [57] with low leakage for both cases.
- Electron and hole mobilities ~80% of the universal curve at E_{eff}>0.8MV/cm and scalability to EOT<10Å (high leakage though) [55].
- Film remains amorphous and showed no phase separation even after a 950^oC dopant activation anneal [53].

Potentially large advantage for silicates is the similarity of bonding to SiO_2. Although there is very less information available on $HfSi_xO_y$ (especially when compared to $ZrSi_xO_y$), it is believed that Hf-silicate has a body-centered tetragonal

structure and is composed of parallel chains of HfO_2 and SiO_2 . This would mean that Hf silicate would possess properties similar to that of SiO_2. It is therefore expected that hafnium silicates would result in better electrical and reliability characteristics compared to HfO_2.

1.11 Motivation to Metal Gates

For gate electrode material, still polysilicon material is being used in industries due to several advantages over metal gates. It is compatible with the conventional self aligned process, which reduces complexity in processing and cost. It can withstand high processing temperature, work function is quite suitable to achieve low and symmetrical threshold voltages for both nMOS and pMOS, and better surface channel operation. The self aligned process makes sure that the gate S/D overlap is minimum and sufficient to ensure good gate control over the channel. Polysilicon/SiO_2 interface is extremely good and stable at high processing temperatures with low interface state density. Even with outstanding electrical and physical properties, it suffers from few problems, mainly poly depletion effect and boron penetration through the film during dopant activation of S/D region, and high resistivity. So to keep track with device scaling along with resolving the difficulties associated with poly gate, metal gates are being considered in industries now a days. Fig. 1.23 shows the CV behavior for metal and polysilicon gates [58]. No degradation in the inversion capacitance was observed in the case of metal gates.

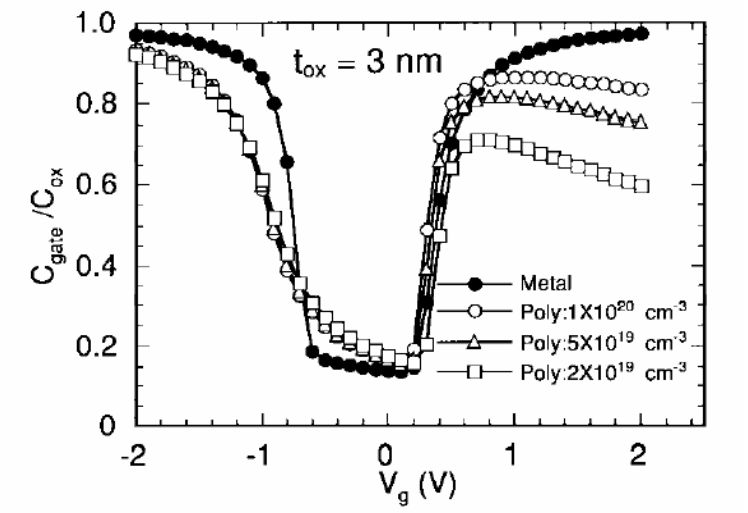


Fig.1.23. Normalized gate capacitance as a function of gate voltage for metal and polysilicon gate structures T_{ox}=3nm.

1.12 Requirements for Metal Gates

The following are the requirements for metal gates:

- Should be compatible with the conventional CMOS process
- Should have low resistivity
- High melting point
- Chemically and thermally compatible with high-k gate dielectric
- Easy to deposit and etch
- Should not penetrate into the film during deposition or subsequent high temperature annealing steps

- Low thermal coefficient to reduce mechanical stress during high temperature processing
- Low processing cost
- Band alignment should be appropriate to have optimum work function to achieve low and symmetrical threshold voltages for both nMOS and pMOS
- No fermi pinning with high-k dielectrics

1.13 Prevailing Challenges with High-k Dielectrics with Metal Gate Electrodes

Although high-k dielectrics are splendid solution to meet the EOT and leakage current requirement for the 45nm technology node and beyond, the CMOS compatibility with poly-Si gate electrode, bulk charge trappings, reduced mobility, threshold voltage non-uniformity and bias instabilities are among the prime concerns. Fig. 1.24 shows the possible location of charges which affects metal oxide (HfO_2) with poly gate electrode devices.

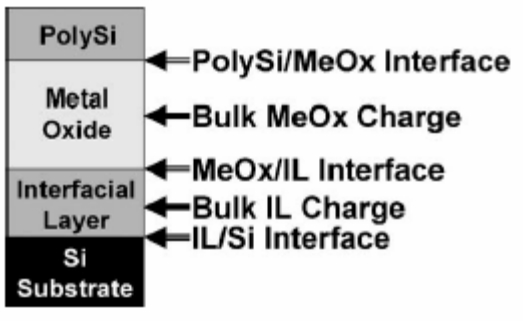


Fig. 1.24. Possible location of charges in metal oxide/poly-gate devices

These charges cause serious problems in integrating high-k dielectric in scaled devices. Fermi pinning with poly gate and poly gate depletion effect almost ruled out the possibility of integrating poly gate with high-k dielectric for future technology. Fig. 1.25 shows the effect of Fermi pinning in high-k dielectrics with poly-Si gate electrode in comparison to SiO_2/poly-gate electrode [59-61].

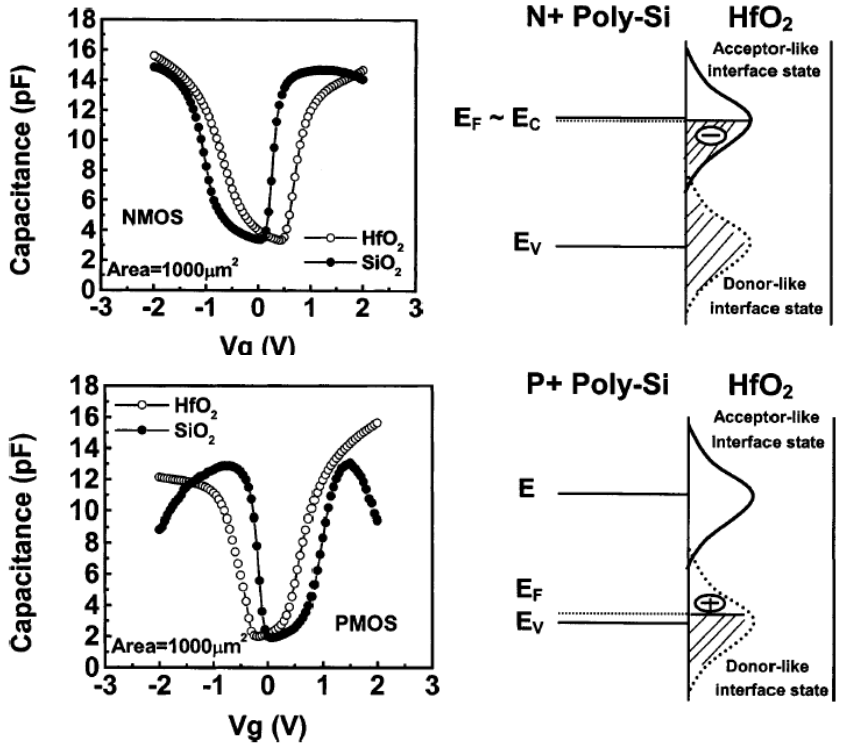


Fig. 1.25. Effect of Fermi pinning in HfO_2/poly-Si electrode. For both nMOS and pMOS fermi pinning is prominent [59].

Fermi pinning is more severe for pMOS than nMOS device with poly-gate electrode, since the pinning location is close to the poly gate conduction band as shown in fig.

1.26 [62]. Because of this dissymmetry, pMOS threshold voltage is higher than nMOS threshold voltage causing non-uniformity in V_{th} for CMOS application.

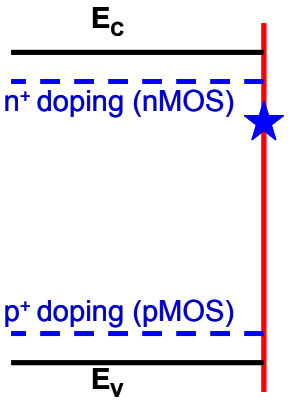


Fig. 1.26. Fermi pinning location of a HfO_2/poly-Si based structure [62]

With metal gate electrode, this non-uniformity in pMOS device could be reduced as shown in fig. 1.27, though it can't be eliminated completely [63].

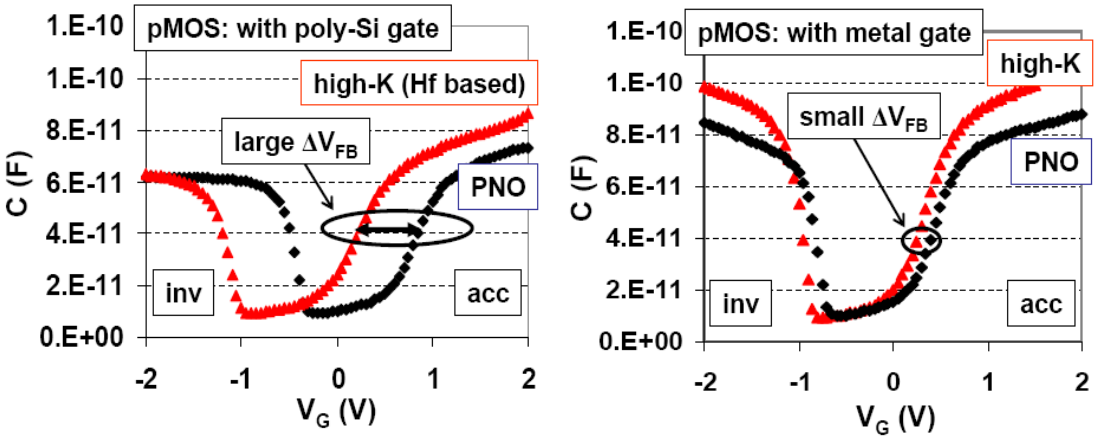


Fig. 1.27. Reduction of Fermi pinning using high-k/metal gate electrode.

Moreover, high-k with metal gate improves the degraded mobility obtained from high-k with poly gate electrode. As shown in fig. 1.28, mobility values are higher for metal gated devices in comparison to poly gated devices with varying inversion equivalent oxide thickness and interfacial layer thickness [64].

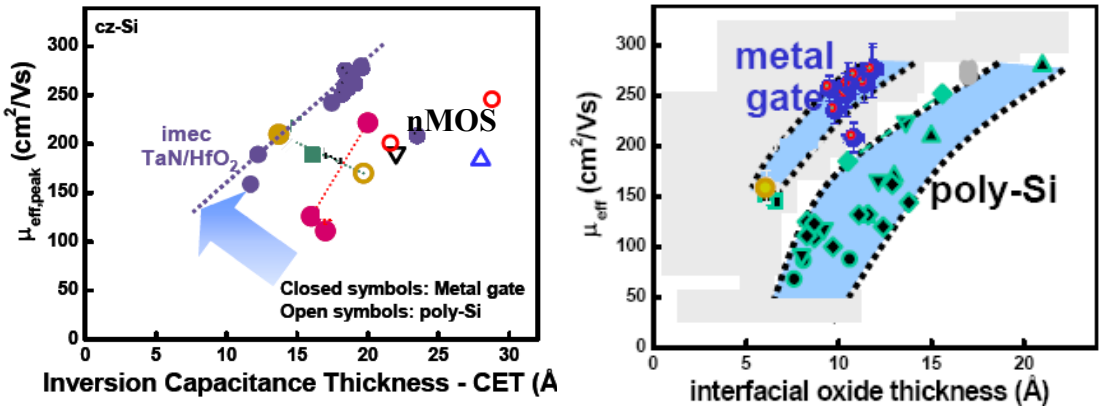


Fig. 1.28. Effective mobility value comparison of metal gated high-k dielectrics vs. poly gated high-k devices, varying inversion capacitance thickness and interfacial layer thickness.

But the most challenging problem with metal gate is its integration complexity in comparison to conventional self aligned CMOS process flow. For choosing metal gate, we need to choose different metals for both pMOS and nMOS devices with proper work function so that V_{th} for both devices could be uniform (fig. 1.29). So far, researches couldn't achieve perfect pair of metal electrodes for both nMOS and pMOS devices. On the other hand, most of the metals have tendency to migrate to mid-gap materials after high temperature process flows. Thus getting a good pair of metals with high-k dielectrics is a big challenge in current technological advances.

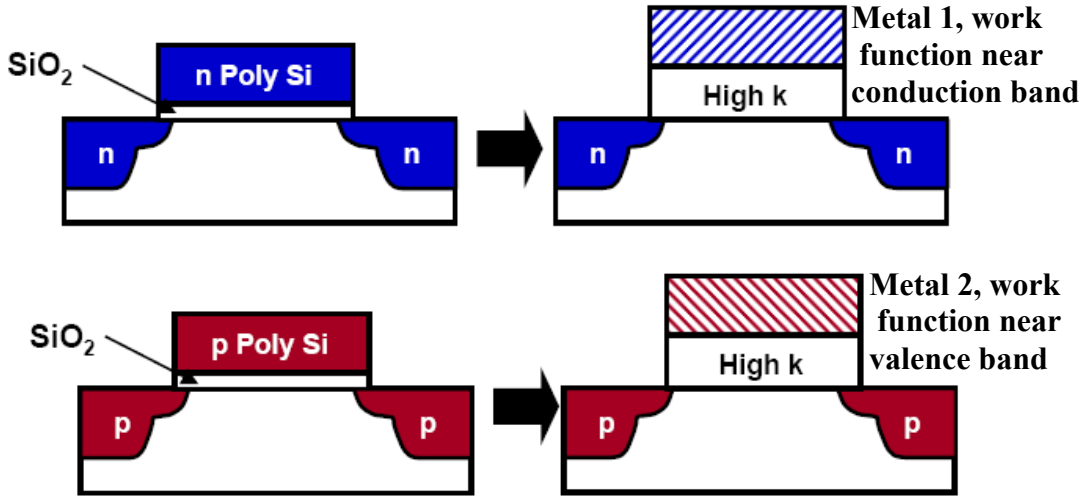


Fig. 1.29. Schematic representation of high-k with poly and metal gates for both nMOS and pMOS devices.

High-k dielectrics are also vulnerable to few intrinsic issues, such as soft optical phonon scattering [65-66], surface phonon scattering [67] which degrades the mobility of the channel. These intrinsic problems might not be overcome limiting application of high-k dielectrics for future CMOS devices.

1.14 Current Approaches to be in ITRS

Up to 65nm node, industries are still using conventional gate oxide with modification in the structure to improve device performance and reduce short channel effects. Intel's 90nm technology uses nitrided capping layer to improve nMOS performance, whereas pMOS performance has been improved by using SiGe S/D structure as shown in fig. 1.30 [68]. Nitrided capping layer enhanced tensile stress in

the channel and compressive stress in the channel was increased by using S/D SiGe regions. SiGe also reduces contact resistance, which increases drive current of nMOS devices.

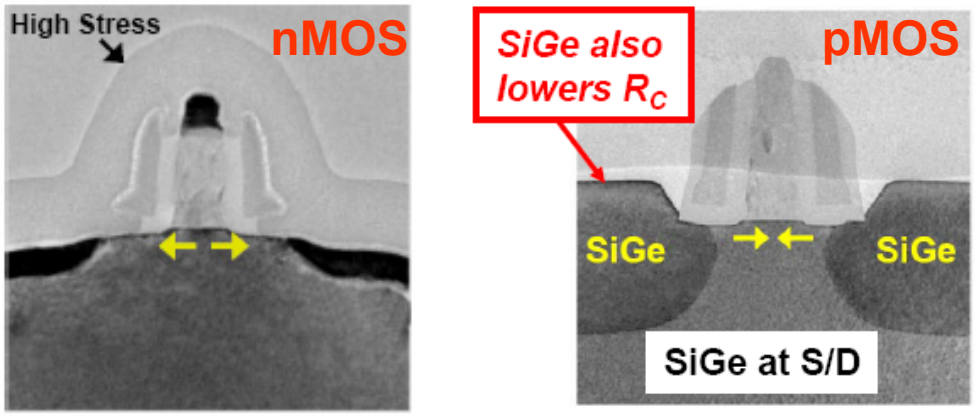


Fig. 1.30. Intel's 90nm nMOS and pMOS structure. SiGe S/D enhanced pMOS mobility, while nitride capping-layer enhanced nMOS mobility.

On the other hand, IBM is using SOI (silicon on insulator) technology to enhance CMOs performance. The SOI structure is shown in the fig. 1.31.

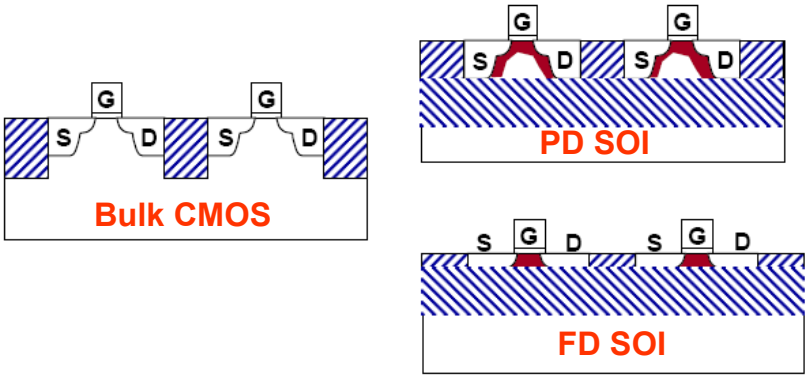


Fig. 1.31. Schematic representation of bulk, partially depleted SOI (PD SOI) and fully depleted SOI (FD SOI).

There are two main categories of SOI, partially depleted SOI (PD SOI) and fully depleted SOI (FD SOI). In FD SOI, Si layer gets partially depleted, (fig. 1.31), whereas PD SOI depletes the Si layer completely. IBM is using FD SOI for production of 65nm node to date. Fig. 1.32 shows the advantage of SOI (PD SOI) in improving sub-threshold characteristics in comparison to bulk SOI [63].

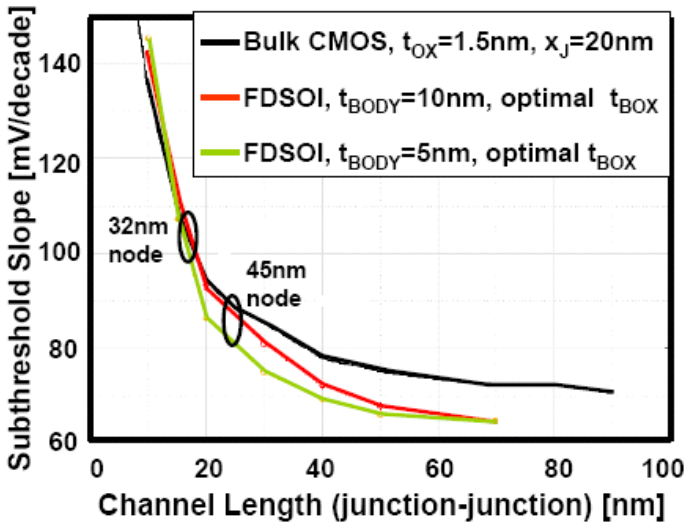


Fig. 1.32. Subthreshold characteristics improvement by using SOI technology in comparison to bulk CMOS

Researches are going on many other structures, for example, Double Gate Transistor, Tri-gate Transistor, Fin-Fet, Carbon Nano Tube Transistor etc to achieve the best performance. Every technique has its own advantages and difficulties in integration and process.

1.15 Outlines

Chapter 1 discusses a brief view of scaling of CMOS technology, needs for scaling, current scaling challenges, promises and issues of high-k dielectrics along with metal gate electrode in CMOS scaling for future technology nodes. It has been shown that high-k dielectrics is a very promising candidate to meet the 45nm and beyond technology nodes. Implementation of metal gate electrodes replacing conventional self aligned poly gate in obtaining optimized high performance device performance has also been discussed. Advantage and disadvantage of every alternative approach have been considered in this chapter. Other than using high-k materials, current approach of using SiGe source/drain and SOI (silicon on insulator) to improve CMOS performance has been touched up in brief.

Chapter 2 covers the effects of nitrogen in high-k dielectrics. This chapter is divided into two sections, first section of which discusses process optimization, development and characterization of NH_3 post-deposition annealed (PDA) Hf-silicate using TaN gate electrode. Hf-silicate film was deposited using DC magnetron sputtering using Hf and Si targets. NH_3 PDA was used to incorporate nitrogen into the dielectrics. It was shown in this section that NH_3 PDA HfSiON was superior to control HfSiO dielectric in terms of EOT scalability, leakage current reduction, C-V hysteresis, transistor I_d-V_g and I_d-V_d characteristics, and mobility. The lowest EOT obtained with this experiment was 9.2Å. Film composition was determined by XPS analysis. Ellipsometer was used to measure the film physical thickness. By surface nitridation using NH_3 pre-deposition anneal (pre-DA) prior to ALD (atomic layer deposition) HfO_2

deposition, the second section of this chapter describes the effect of nitrogen in reducing EOT down to 7.4Å with reasonable mobility. Furthermore, by increasing NH_3 pre-DA temperature up to 900^oC, bulk trapping in the dielectric of the device could be reduced due to the presence of nitrogen in the dielectric, though nitrogen pile-up at the interface degraded the mobility slightly.

Chapter 3 focuses on effects of chlorine (Cl) in the high-k dielectrics. This chapter has also been divided into two sections. The first section describes the incorporation of Cl atoms in ALD HfO_2 by varying ALD precursor, $HfCl_4$ pulse time variation. SIMS (secondary ion mass spectroscopy) analysis confirmed the presence and increase in Cl composition in HfO_2 by increasing precursor pulse time. It is shown that Cl incorporation into the high-k gate oxides helps to reduce the bulk trapping characteristics of the device. This observation was further supported by HCl post-rinsing treatment of MOCVD (metal organic chemical vapor deposition) HfSiO described in the second section of this chapter. In this section, HCl post-rinsing improved mobility and bias instabilities of the high-k gate oxides without affecting the bottom Si/high-k interface. The reduction of bulk trapping characteristics has been attributed to the observed mobility and bias instabilities improvements.

The transient relaxation effect, which has been addressed as an undesirable issue in high-k dielectrics, has been addressed in chapter 4. It is shown that devices relax after being stressed under substrate injection condition. This relaxation follows a unique behavior irrespective of device dimensions, device operating parameters and stress conditions up to certain limits. This study reveals the fact that bulk trapping in the oxide

is primarily responsible for device bias instabilities. The bulk trapping could be completely relaxable by applying pulses of opposite polarity to stress polarity. Bulk trapping has been found to be responsible for device degradation under substrate injection condition, whereas no significant interface degradation could be observed.

Chapter 5 discusses the reliability characteristics of high-k gate oxides. This chapter again is divided into three parts. The first part discusses the effect of compositionally varying HfSiO in enhancing the performance and reliability of the devices. The concept of bi-layer structure of HfSiO, of which top layer is composed of high composition Hf atoms on top of bottom layer composed of high composition Si atoms, has been proposed in enhancing device performance, reducing defect density and enhancing reliability of high-k gate oxides. The second part illustrates the effect of nitrogen profiling by inserting Si layer into HfON gate oxide in optimizing TDDB (time dependent dielectric breakdown) behavior of gate oxides. Reduction of bulk trapping density by inserting Si layer further away from the interface (i.e. trapping nitrogen atoms further away from the bottom interface) has been discussed. The third part of this chapter discusses a novel approach in understanding the breakdown mechanism of Hf-based gate oxides under substrate injection by using stress-anneal experiments to separate the role of injected holes and electrons in causing breakdown of the devices. The supporting experimental observations have been given to support the breakdown model proposed.

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Chapter 2

Effects of Nitrogen in High-k Gate Oxides

In conventional SiO_2 gate oxide, nitrogen (N) plays a significant role in enhancing the dielectric constant, thus providing a window to increase the physical thickness of the gate oxide keeping the EOT (effective oxide thickness) the same. Thus with technology nodes, semiconductor industries could be able to follow the ITRS even below 100nm gate length. The role of nitrogen in high-k gate oxides has extensively been investigated in recent years. Several mechanisms of nitrogen incorporation have been proposed, for example, nitridation at the top interface between high-k and gate electrode [1], at the Si/high-k bottom interface [2] and nitridation throughout the whole gate oxide [11]. Each of the processes has their own advantages and disadvantages. In this section of work, use of NH_3 as nitrogen source will be discussed in details and systematically.

2.1 Process Development and Characterization of NH_3 PDA PVD-HfSiON

2.1.1 Motivation to HfSiON

$HfSi_xO_y$ film as an alternative gate dielectric has gained considerable attention due to its promising material and electrical properties over HfO_2 film, specially in terms

of crystallization temperature, interface properties, thermal stability etc [3-9]. As nitrogen is playing a great role in HfO_2, ZrO_2 for scalability and thermal stability, $HfSi_xO_y$ film with reactive sputtered nitrogen incorporation has also been investigated so far. Scalability enhancement along with better crystallization has been obtained [10-11]. Apart from the above mentioned advantages of nitrogen incorporation, literature supports to minimize oxidation of the underlying Si and reduction of dopant diffusion [12]. Moreover, channel mobility higher than that reported for HfO_2 could be obtained for HfSiON film with poly gate.

This work focuses on N incorporation into the $HfSi_xO_y$ film using NH_3 as post deposition annealing ambient. Previous works on NH_3 PDA has been investigated on SiO_2 film mainly after reoxidation [13]. In most of the cases, NH_3 contributed to reduction of EOT and leakage and superior thermal stability at high temperatures. For high-k dielectric like ZrO_2, NH_3 has the effect of higher accumulation capacitance, lower leakage and better thermal stability and crystallization as compared to control ZrO_2 film [14], which is true for HfSiON film as well. Although EOT of less than 10Å could be obtained for HfSiON film [10], this incurs high leakage>10A/cm^2 at $V_g=V_{th}+1$. So to reduce EOT and at the same time to maintain lower leakage current along with other superior electrical and physical features, this work has investigated NH_3 annealing of as deposited Hf-Silicate film without any pre-reoxidation. The process condition and process parameters have been kept the same as done by previous works [15] except optimizing for NH_3 post deposition annealing for scalability and compatibility.

2.1.2 Process flow for MOSCAP and MOSFET Fabrication

MOSCAP and MOSFET process flow can be described as shown

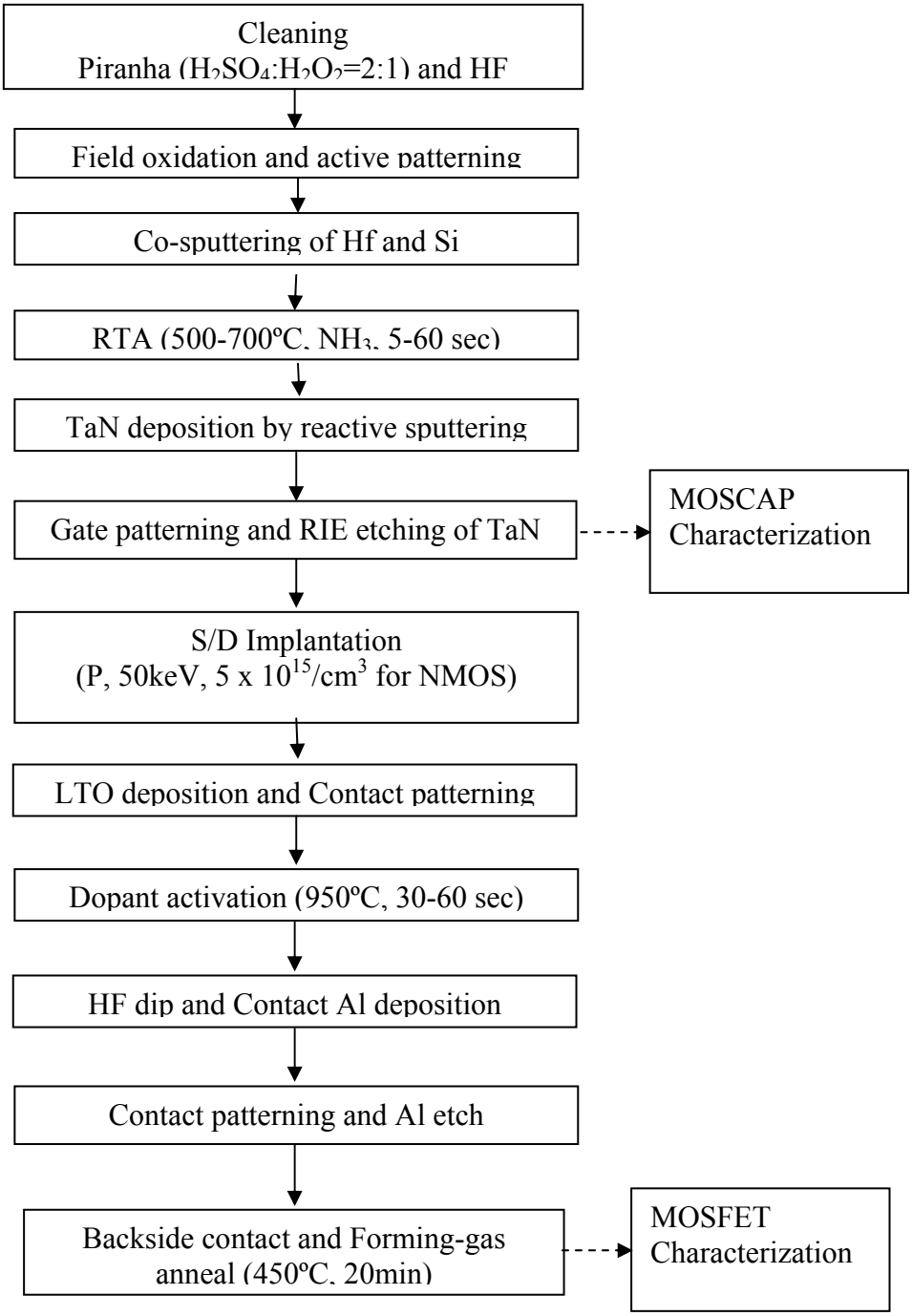

Fig. 2.1. Process flow for MOSCAP and self aligned MOSFET fabrication.

After rinsing several times, bare wafers were cleaned in piranha and HF solution consecutively. Piranha solution was made by mixing 800ml of H_2O_2 with 1600ml of H_2SO_4 solution. HF solution was prepared by 60ml of HF acid with 2400ml of H_2O. Then wafers were loaded in oxidation chamber for wet oxidation in 950^oC temperature for two hours to make 3500-4000Å thick field oxide layer. This process was followed by active patterning and BOE (Buffer oxide etching) of field oxide.

Before deposition of hafnium silicate layer, every time wafers were dipped in dilute HF solution. Hafnium silicate was deposited in a PVD system using co-sputtering of hafnium and silicon target at the same time (fig. 2.2). Deposition condition was as follows:

Hafnium Target Power	100-200 Watts
Silicon Target Power	100-200 Watts
Ar pressure	40 mTorr
Ar flow	20 sccm
Base Pressure	$<4x10^{-7}$ Torr
Film Thickness	38-42Å
Target position	Hf fixed, Si varied
Temperature	Room Temperature

Ar was used as ambient. Film thickness was estimated by ellipsometer with refractive index of 1.55. A schematic view of the co-sputtering hafnium silicate system can be shown in fig 2.2. The composition of the film was varied by changing the target power and also by changing the silicon target position maintaining the Hf position fixed.

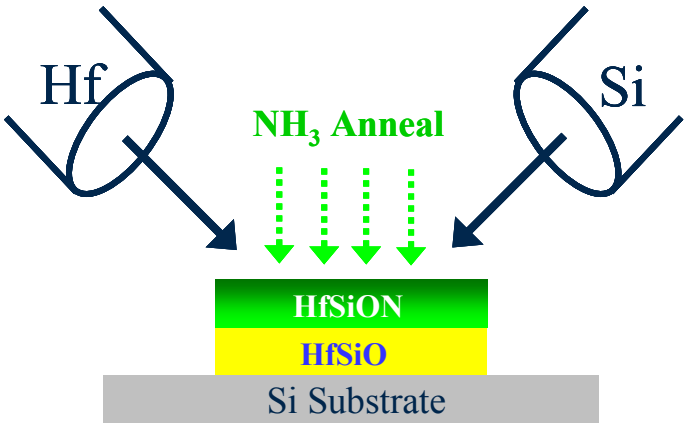

Fig. 2.2. Schematic of the PVD process for Hf-silicate deposition and NH_3 PDA HfSiON

The wafer was then transported to a rapid thermal annealing (RTA) chamber for NH_3 annealing. Different temperature and annealing time had been investigated for process optimization. The oxidation of the film was attributed to the residual oxygen in the annealing chamber, or atmospheric exposure into air, or oxygen content inherent to NH_3 gas due to its impurity. The flow rate for NH_3 was varied from 1 slm to 8 slm. Sufficient purging time before actual gas flow was kept 5 min to remove any oxygen content in the chamber. After that TaN gate was deposited onto the using same PVD system with the following condition.

Deposition Power	1100 Watts
Ar pressure	10 mTorr
Ar flow	20 sccm
N_2 flow	7 sccm
Base Pressure	$<4x10^{-7}$ Torr
Film Thickness	~2000Å (in 5 min)
Temperature	Room Temperature

The sheet resistance obtained with such a condition was found to be 10-15 ohm/sq. After gate patterning, the TaN was etched in RIE (Reactive Ion Etching) followed by photo resist removal by dipping in Acetone for 10 minutes. For only capacitor characteristics, the backside of the wafers was coated with Al using Al sputtering system. For Transistor fabrication, source/drain ion implantation was carried out followed by low temperature oxidation (LTO) step. After patterning for contact formation, S/D activation was done in 950^{o}C for 30s in RTA N_2 ambient. This was followed by HF dip and sputtered Al deposition for contact metal. After contact patterning sintering was done in forming gas in 450^{o}C for 20 minutes. Final back metal was carried out by Al sputtering technique.

Electrical characteristics were performed using HP4194 impedance analyzer for C-V and HP4156A semiconductor parameter analyzer for J-V and others. EOT was estimated from the accumulation capacitance of C-V measured at 1MHz, XPS (x-ray photoelectron spectroscopy) analysis was done to determine the composition and chemical bonding of the films. XRD was used to get the crystallization temperature.

2.1.3 Physical Characterization

XPS analysis has been performed on the samples to confirm the presence of nitrogen in the film. For analysis, samples were annealed in both N_2 (40s) and NH_3 ambient at 600^{o}C. NH_3 annealing has been done at 20s, and 40s. As shown in Hf4f spectra in fig. 2.3(a), Hf4f peak was shifted to lower binding energy with respect to Hf4f peak of the control sample. The shift is even higher to the lower binding energy,

as NH_3 annealing time is longer. This clearly indicates the presence of Hf-N bonds in the film.

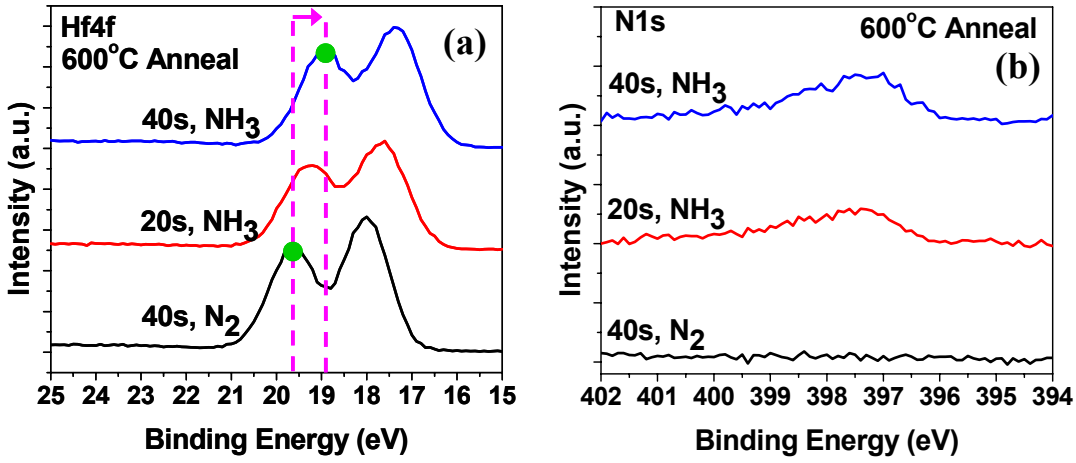

Fig 2.3. (a) Hf4f (b) N1s Spectra for Hf-Silicate and NH_3 PDA HfSiON

Initially the first peak was at 18 eV for control sample and then it shifted to 17.6 eV and 17.3 eV for 20s, and 40s NH_3 annealing respectively. The most interesting thing is that the difference between two Hf4f peaks is almost the same (~1.6eV). This means that the longer the annealing duration, the more is N incorporation in the film in the form of Hf-N bonds without changing the film morphology. For the case of HfO_xN_y, nitrogen incorporation results in lower shift of peaks in Hf4f spectra from HfO_2 to HfO_xN_y film [11-12]. So the lower shift in binding energy clearly indicates the presence of Hf-N. To further ensure the presence of nitrogen in the film, N1s spectra has been shown in fig. 2.3(b). No N1s peak for control sample has been observed, whereas clear peaks have been observed for both of the NH_3 annealing cases. Note that peak intensity

is a bit higher for 40s NH_3 annealing sample than for 20s annealing. This indicates higher nitrogen concentration for longer annealing duration.

2.1.4 Process Development and Optimization of Process Parameters

Process parameters such as EOT, J (leakage current density), C-V hysteresis etc are optimized using C-V and J-V curves for different process conditions. There are many processing parameters that need to be optimized, such as deposition time, pressure, temperatures of as deposited films, annealing temperatures, ambient and time, gate material etc. For control Hf-silicate films, optimization has already been done in [15]. In this work, process optimization using NH_3 annealing of as-deposited Hf-silicate in rapid thermal annealing (RTA) chamber has been discussed. The annealing condition for control sample is 600°C in N_2 ambient (RTA), 40 seconds.

2.1.5 Effect of NH_3 Annealing Temperature

Temperature plays a major role in proper film oxidization. Very low temperature sometimes results in incomplete oxidation, whereas very high temperature facilitates oxygen molecules to diffuse into the film resulting in interfacial layer. Interfacial layer increases EOT. Fig. 2.4 shows the effect of RTA annealing temperature in NH_3 ambient.

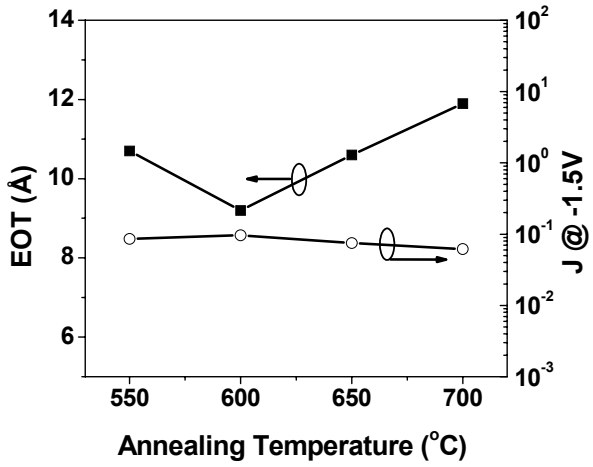

Fig. 2.4. EOT and J vs. different annealing temperature for NH_3 PDA

As shown, higher the temperature, higher the EOT due to thicker interfacial layer. Also at 550°C, EOT is large. The main purpose of NH_3 PDA is to incorporate nitrogen in the film that has the effect in increasing overall dielectric constant. But to break the binding energy of N-H bonds in NH_3, it requires enough temperature. So if we anneal the film at a lower temperature, it wouldn't break the bonds and this will result in small amount of nitrogen in the film. Thus 550°C is not sufficient to increase the dielectric constant, and so EOT was found higher than that at 600°C. So the optimum temperature for NH_3 annealing was set to be 600°C.

2.1.6 Effect of NH_3 Annealing Time

Figure 2.5 shows EOT-J values with the variation of NH_3 annealing time at 600°C in RTA.

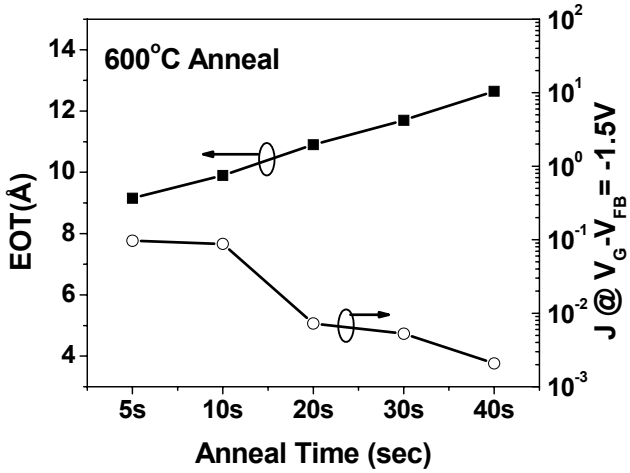

Fig. 2.5. EOT-J vs. 600°C NH_3 PDA time. EOT increases as annealing time increased due to growth of interfacial layer.

As shown, the lowest EOT obtained was 9.2Å for 5s annealing with a leakage current density, J~97 mA/cm^2. With the increase of annealing time, EOT increased while leakage current decreases. This observation is a bit contrary to what was found for NH_3 annealing in conventional gate dielectric [13]. Although longer annealing time incorporates more nitrogen in the film, NH_3 gas contained some impurity oxygen, which in turn causes oxygen penetration into the dielectric with annealing time. This may cause interfacial layer to be thicker. But the reduction of leakage compensates the increase in EOT as shown in fig. 2.5. On the other hand, residual oxygen in the annealing chamber is also responsible for this interfacial layer growth. Even then, EOT of 9.2Å with such a leakage value is still promising. To get a better leakage behavior

and at the same time low EOT value, pure NH_3 gas needs to be used. Figure 2.6 shows the typical well behaved C-V profile for 5s annealing time.

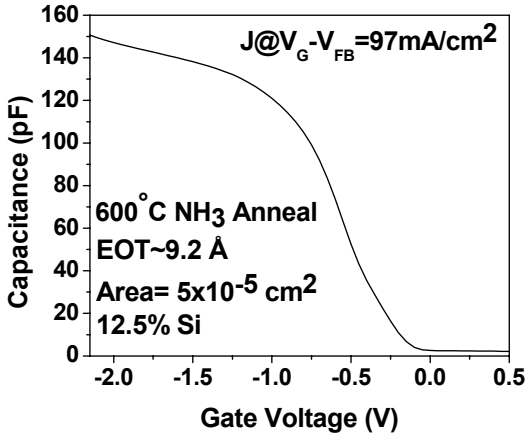

Fig. 2.6. Well behaved C-V profile for 600°C, 5s NH_3 PDA.

Finally EOT vs. J values for NH_3 annealed HfSiON has been plotted in fig. 2.7 below. The most promising part here is the possibility of scaling with NH_3 PDA.

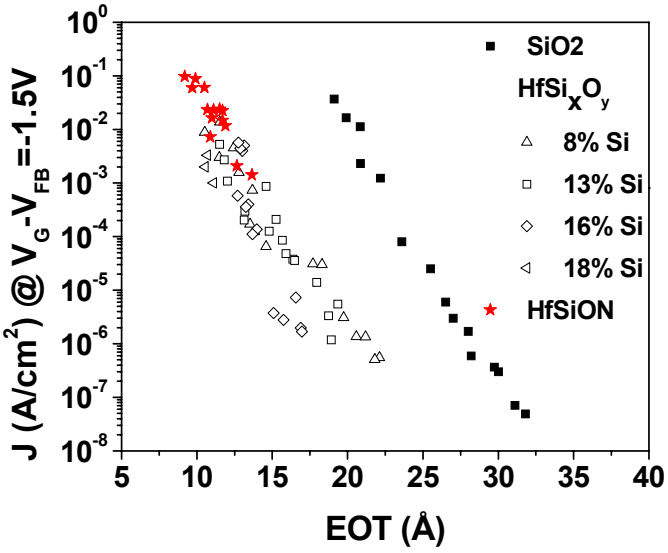

Fig. 2.7. J vs. EOT for SiO_2, Hf-silicate and NH_3 annealed HfSiON

2.1.7 Hf-silicate and NH_3 annealed HfSiON MOSCAP and MOSFET Comparison

Fig 2.8(a) and fig. 2.8(b) shows the C-V and J-V curves for control and NH_3 annealed (20s) sample respectively.

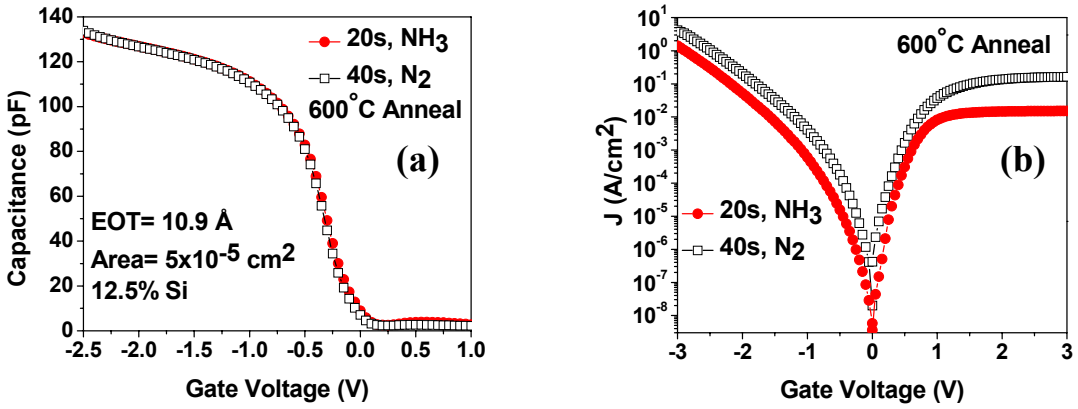

Fig. 2.8. (a) C-V and (b) J-V for control and NH_3 annealed devices

As shown, irrespective of annealing time and ambient, EOT for both devices is the same (fig. 2.8.a), but leakage is lower for NH_3 PDA sample (fig. 2.8.b). The decrease of leakage density is still not very clear. It has been reported that tunneling probability is qualitatively related to the area of the tunneling barrier associated with the oxide physical thickness and the oxide barrier height [16]. Obvious decrease in leakage current for NH_3 annealed hafnium silicate film indicates that this nitridation results in higher dielectric constant and allows larger physical thickness to suppress the increase in tunneling current while maintaining the same gate capacitance.

2.1.8 C-V Hysteresis

C-V hysteresis is a common phenomenon in high-k dielectric. It is believed that this is due to interfacial and bulk charge trapping as the gate voltage is swift [17]. Due to this, V_{FB} is different for positive and negative sweep of gate voltage. The difference in V_{FB} is due to the charge that has not been de-trapped after all the sweep cycles. In this experiment, V_{FB} difference after 4^{th} sweep has been taken. Figure 2.9 shows the C-V hysteresis data for control and NH_3 annealed sample just after capacitor process. As shown in the figure, hysteresis values are 114 mV and 150 mV for control and NH_3 annealed samples respectively. We know by high temperature treatment, hysteresis can be reduced as it anneals out the defects and H-species and makes the film denser. For these films, it has been observed that hysteresis could be reduced significantly just after LTO fabrication steps

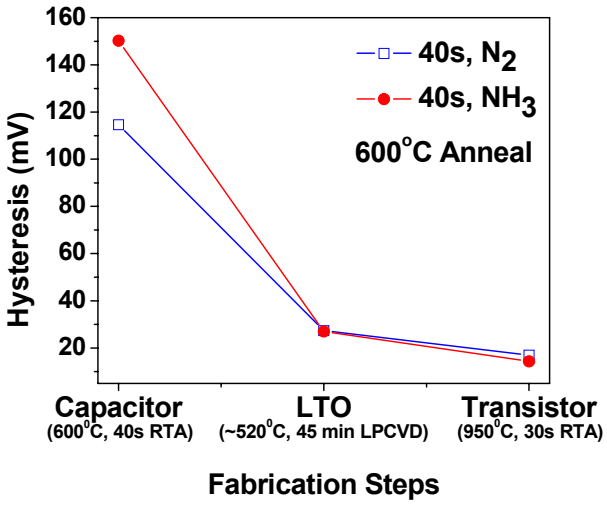

Fig. 2.9 Hysteresis for different fabrication steps of control and NH_3 annealed sample

2.1.9 Thermal Stability

One positive contribution of nitridation is the enhancement of thermal stability of the film. To ensure thermal stability of our HfSiON film, EOT and J values have been measured at different fabrication steps of conventional MOSFET process flow, i.e. after capacitor, LTO and transistor fabrication steps. LTO was deposited at ~520^{o}C for 45 minutes. As shown in fig. 2.10, both ΔEOT and J are lower for each of the high temperature process steps. This indicates higher immunity to high temperature thermal budgets in MOSFET process flow.

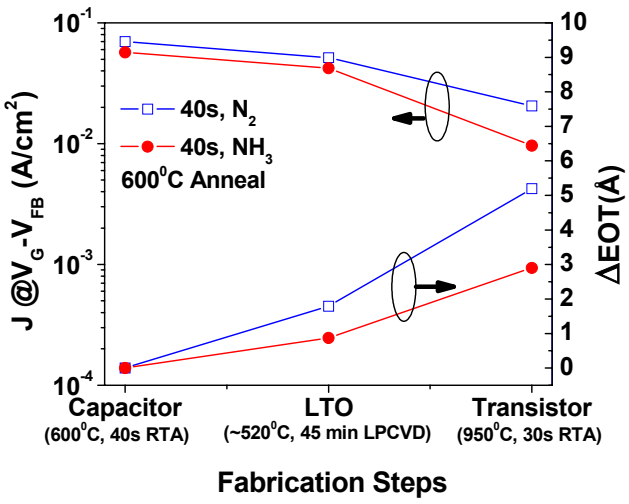

Fig. 2.10. Thermal stability of control and HfSiON devices for different fabrication steps.

2.1.10 SILC

During constant voltage stress, carrier traps are generated in the bulk of the dielectric due to energetic charge carriers (electrons) and these traps help to enhance

conduction through dielectric. We can define this enhancement of conduction as stress induced leakage current (SILC) [18-20]. In this work, SILC is defined as the difference in leakage current density (ΔJ) after stress from that of the fresh value, J_o divided by J_o. Thus SILC = $\Delta J/J_o$. Fig. 2.11 summarized the SILC at different stress times at a constant –2V stressing for control and NH_3 annealed samples respectively. For each of the stress condition SILC is lower for NH_3 case as is expected.

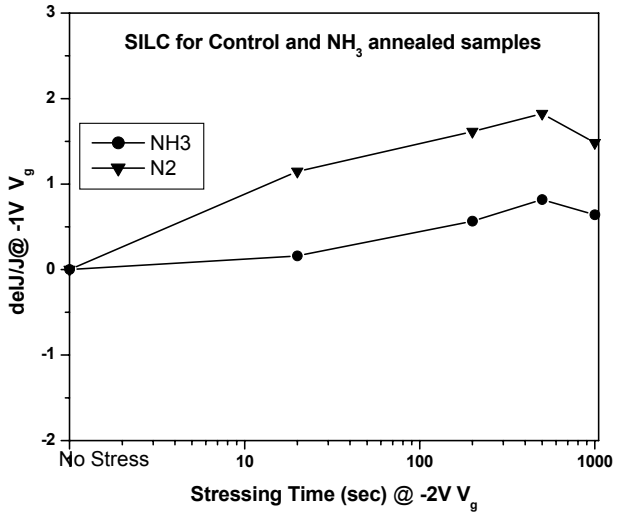

Fig. 2.11. SILC for Control and NH_3 annealed devices at V_g= –1V

2.1.11 MOSFET Characteristics

Fig 2.12 shows the C-V characteristic for control and NH_3 annealed MOSFET for both accumulation and inversion regions. As expected, due to better thermal stability, capacitance value is higher for NH_3 annealed MOSFET.

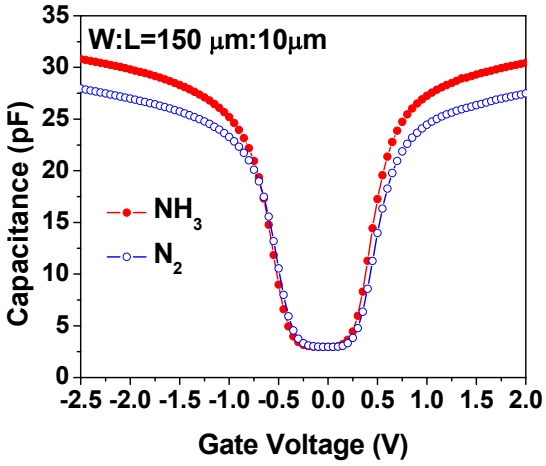

Fig. 2.12. C-V for control and NH_3 annealed MOSFET devices.

I_d-V_g and I_d-V_d characteristics have been measured for both cases as shown in fig 2.13 (a) and fig. 2.13(b) respectively. Unlike surface nitridation, no degradation of MOSFET behavior has been observed, rather it demonstrated slight improvement.

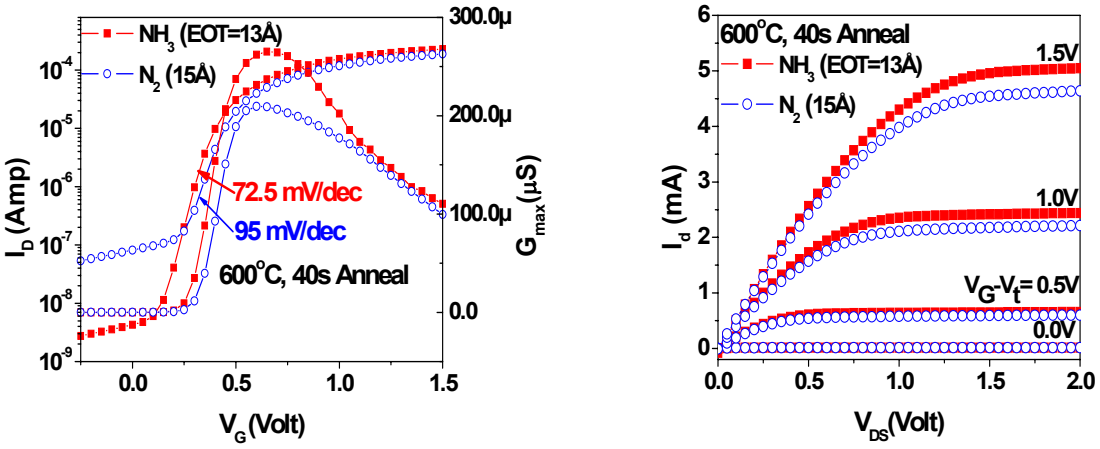

Fig. 2.13. (a) I_d-V_g and (b) I_d-V_d Characteristics of control and NH_3 PDA HfSiON

The subthreshold swings obtained were 95 mV/dec and 72.5 mV/dec for control and NH_3 annealed samples, respectively.

2.1.12. Mobility

Channel electron carrier mobility was measured by conventional split C-V techniques. This technique uses inversion C-V to calculate the inversion charge and uses I_d-V_g curves to calculate carrier mobility in the channel. Mobility values for control and NH_3 gives a fair comparison of the improvement in interface quality between the two samples. Mobility was even better in the case of HfSiON as shown in fig. 2.15. This observation also ensures the fact that nitrogen incorporation technique using NH_3 anneal at 600^{o}C doesn't pile up nitrogen atoms at the bottom dielectric/Si interface [21], which results in "radically induced reoxidation" effect in the film [13]. The outcome is the undesirable increase of EOT, transconductance degradation [13, 22], poor reliability and drive current reduction. Instead, this technique put nitrogen at the top portion of the dielectric increasing dielectric constant of the material.

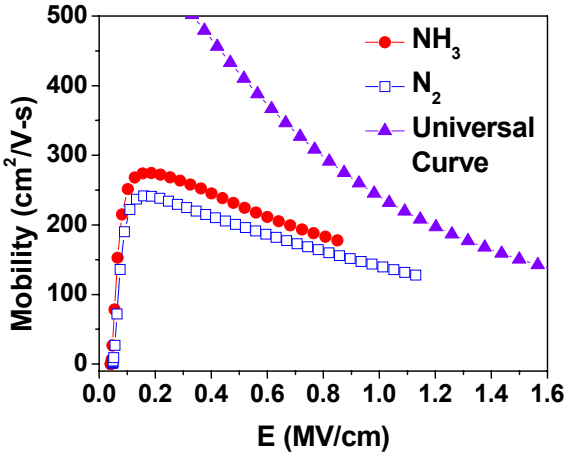

Fig. 2.15. Effective Mobility of control and NH_3 annealed MOSFETs

2.2 Effect of NH_3 Surface Nitridation Temperature in ultra-thin ALD HfO_2

The previous experiment of incorporating nitrogen into the dielectric was carried out by NH_3 post-deposition anneal in physically thick films (~40-45Å). This experiment was designed to observe the effect of surface nitridation in very thin high-k dielectric. It should be noted that most of the studies in the literature so far dealt with impact of nitridation at the bottom interface in EOT reduction, immunity to boron penetration and thermal stability of high-k gate oxides [23-24]. On the other hand, mobility is a very crucial parameter, which urges further attention to ultra-thin film devices. This work for the first time demonstrates the effect of NH_3 surface nitridation temperature in physically ultra-thin (~15-30Å) ALD (atomic layer deposition) HfO_2 on EOT, J (leakage current density) and mobility of MOSFET devices. Moreover, the

effect of temperature pre-treatment in bulk trapping and interface degradation has also been discussed.

2.2.1 Process Flow

The MOSFET process flow started with cleaning the active patterned (shallow trench isolation) wafer with dilute HF solution. The wafers then went through pre-DA (pre-deposition anneal) in NH_3 for 15 sec at temperatures ranging from 500^{o}C to 900^{o}C. Following this, ALD (atomic layer deposition) HfO_2 was deposited using precursor TEMA Hf with O_3 as oxidation ambient (300^{o}C, 1 Torr) at different thicknesses ranging from 15Å to 30Å. N_2 PDA at 700^{o}C, 60 sec was performed on those samples for complete oxidation. Then 10nm ALD TiN layer and 180nm amorphous silicon layer was deposited as a stack gate electrode. After gate patterning, high-k layer was removed with a wet etch process leaving a minimal damage in the extension region. A thin nitride layer (~5nm) was deposited followed by LDD (lightly doped drain) and halo dopant implantation to prevent the process induced damage through plasma process or oxygen diffusion [25]. After the thin nitride deposition, 100nm oxide spacer was formed and phosphorous was implanted to dope the source/drain regions (energy = 15KeV, dose = 4e15) followed by activation at 1000^{o}C, 10 sec rapid thermal anneal (RTA) in N_2 ambient. After the Ti-silicide formation, 700nm pre-metal dielectric (PMD) layer was formed. Then W plug with Ti/TiN liner was used to contact the source/drain and gate electrode regions and Al metal pad was patterned. Finally forming gas anneal was performed at 480^{o}C for 30 minutes.

Electrical characterizations were performed using HP 4284A impedance/gain phase analyzer and HP4156A semiconductor parameter analyzer. EOT was extracted from accumulation capacitance measured at 100 KHz, after accounting for quantum mechanical effects. The single pulse charge trapping measurements were done by Keithley Model 4200-SCS together with a switch matrix, and a pulse generator. Nitrogen concentration in the film was determined by SIMS (secondary ion mass spectroscopy) analysis

2.2.2 Chemical Analysis

By SIMS it was observed that increase in NH_3 Pre-DA temperature increased nitrogen concentration as shown in fig. 2.16, while oxygen concentration remains almost constant in the film. Fig. 2.17 shows the TEM (transmission electron microscopy) image of 500^oC and 700^oC NH_3 Pre-DA films respectively.

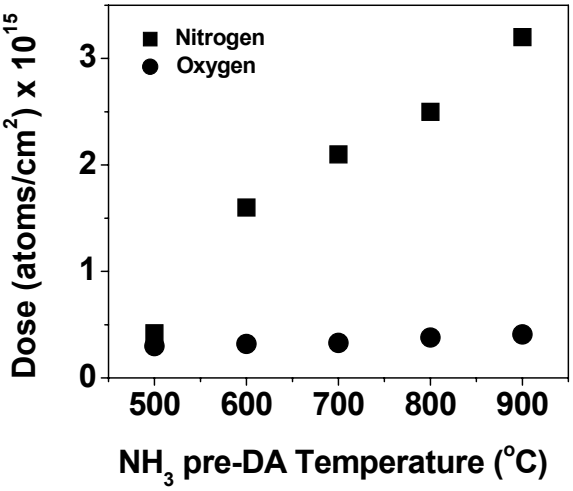

Fig. 2.16.. Nitrogen and oxygen composition after different NH_3 pre-DA temperature prior to ALD HfO_2 deposition.

Interfacial layer was seen slightly thicker (10Å) for 700°C Pre-DA sample as compared to 500°C one (9Å). On the other hand, total physical thickness of the film is almost the same (~28-29 Å).

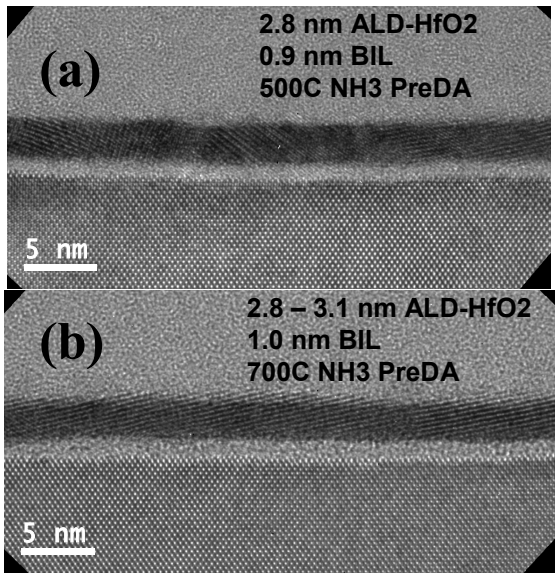

Fig. 2.17. TEM image of (a) 500°C and (b) 700°C NH_3 pre-treated samples.

The results show the fact that at the same physical thickness and almost at the same interfacial layer thickness, the amount of nitrogen incorporation could be varied by simply varying the pre-DA temperature, keeping the oxygen composition the same.

2.2.3 Electrical Characterization

Fig. 2.18 (a) shows the leakage current density (J) vs. EOT curve for different NH_3 pre-DA temperatures.

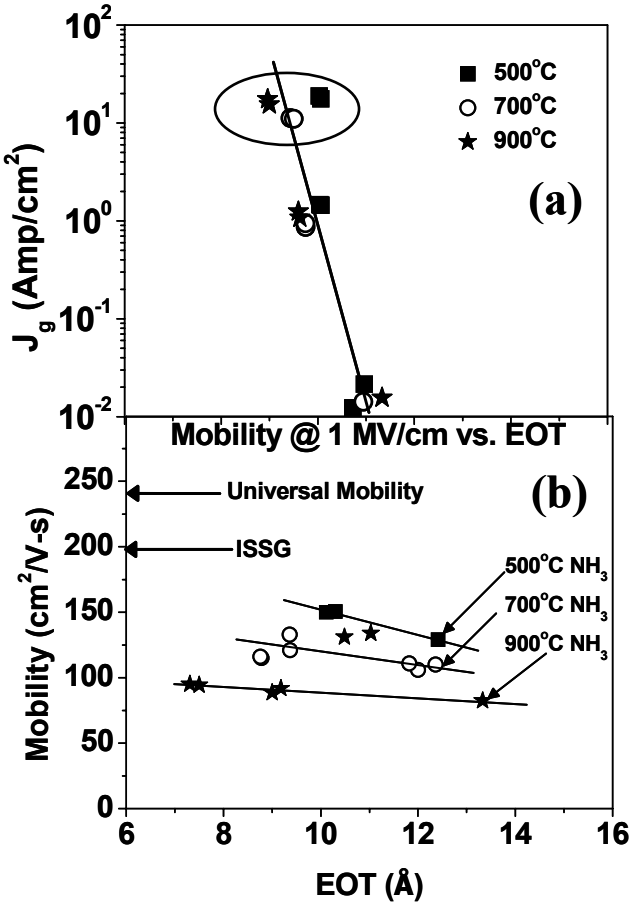

Fig. 2.18. (a) J vs. EOT and (b) mobility at 1 MV/cm vs. EOT plot for different NH_3 pre-DA temperatures with varying physical thicknesses (15Å to 30Å).

Therefore, as shown in fig. 2.18(a) [see circle], at the same physical thickness, reduction in EOT could be attributed to the increase in dielectric constant of the dielectric layer by nitrogen incorporation at high temperature NH_3 Pre-DA, though there was no apparent change in J. In fig. 2.18(a), physical thickness was reduced (from 30Å to 15Å) for a particular NH_3 pre-DA condition, thus reducing EOT, which was

accompanied by an increase in J. The EOT could be reduced down to ~7.4Å, one of the smallest values reported for ALD HfO_2. The most noted observation is the mobility trend with high temperature treatment. High temperature treatment reduced EOT for the same physical thickness, though it didn't have significant effect on mobility (at 1 MV/cm) reduction as shown in fig. 2.18(b). Mobility was the highest for 500°C NH_3 Pre-DA (75% of control SiO_2 shown), while it reduced for temperatures as high as 900°C (50% of control SiO_2). On the other hand, EOT could be reduced down to ~7.4Å for 900°C Pre-DA. So far this is one of the highest reported mobility values to date achieved for such a thin HfO_2 device. For comparison, mobility values for ISSG (in-situ steam gate oxide) and universal mobility at the same field are also given in the fig. 2.18(b).

To understand the role of bulk oxide in mobility degradation, bulk trapping characteristics were studied by short pulse I_d-V_g (drain current-gate voltage) measurements as shown in fig. 2.19 [26]. Inset of fig. 2.19(a) shows the shape of the pulse (rise time=fall time=5μs, width=125μs). I_d values were taken during the rise time by a digital oscilloscope. I_d degradation (ΔI_d) occurs in the device during the pulse width time, which is governed by charge trapping as shown in the figure. Due to charge trapping, I_d can't follow the same line as gate voltage sweeps back during pulse fall time. Hysteresis ΔV can be treated as an indirect measure of charge trapping since it includes the contribution from detrapping during the back and forth sweep. For fair comparison, all the devices were swept up to the same (V_g-V_t). The results show that both ΔI_d and ΔV were almost of the same magnitude for pre-DA treatment up to 700°C,

while these values are significantly lower for 900°C pre-DA treated devices as shown in fig. 2.19(b).

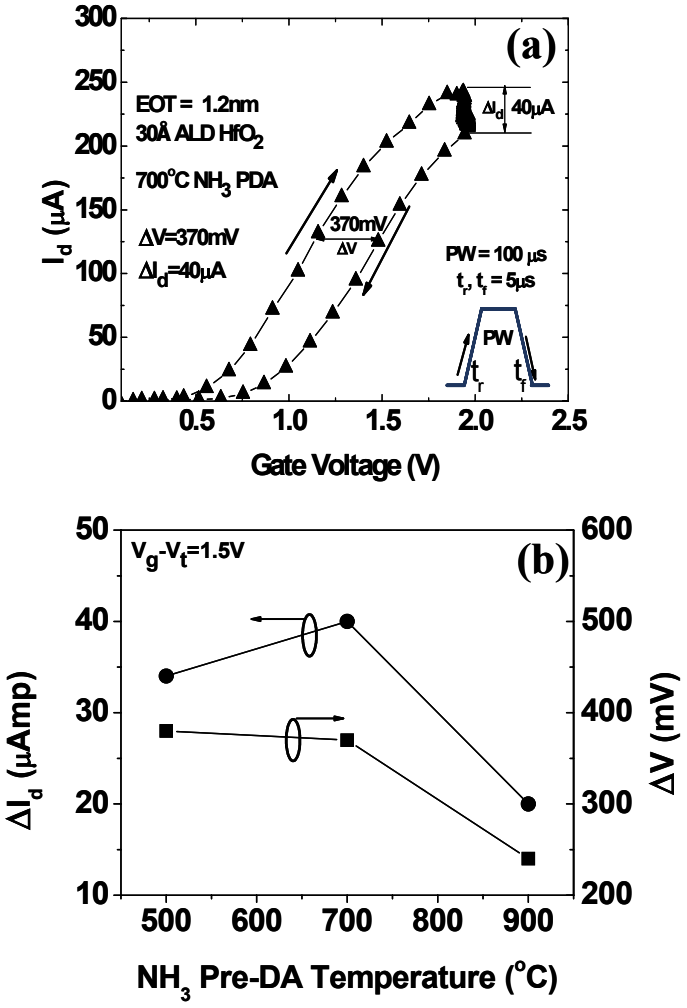

Figure 2.19. Bulk trapping characterization using single short pulse I_d-V_g measurement. (a) I_d-V_g up and down sweep during the short rise and fall time respectively (b) Comparison of I_d degradation (ΔI_d) and I_d-V_g up-down width (hysteresis ΔV) for NH_3 pre-DA at different temperatures.

Therefore, high temperature NH_3 pre-DA indeed helped to enhance bulk trapping immunity, though the reduction in mobility resulted from interface degradation as shown in fig. 2.20, in which the peak interface state density value, $(N_{it})_{max}$ was plotted as a function of pre-DA temperatures. Increase in interface state density with NH_3 pre-DA temperature (fig. 2.20) is due to nitrogen pile-up at the interface, resulting in mobility degradation.

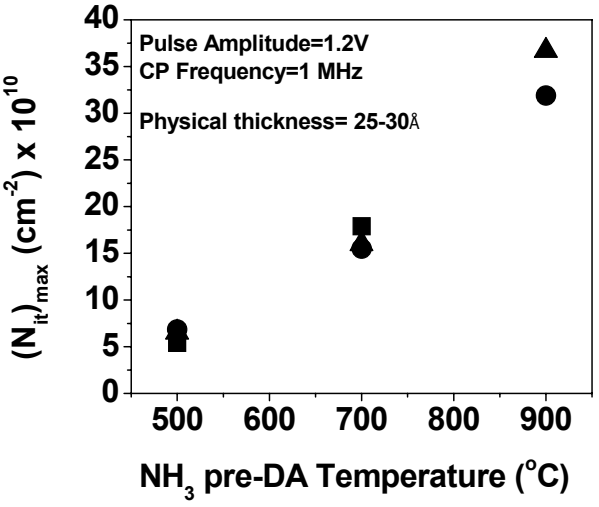

Figure 2.20. Plot of maximum interface states with NH_3 pre-DA temperatures. As expected, increase in interface states is prominent after high temperature treatment

2.3 Summary

In summary, it is confirmed that nitrogen incorporation into the high-k dielectric by NH_3 post-deposition anneal or NH_3 pre-deposition anneal both have positive attributes in decreasing EOT of the oxide. By subjecting as deposited Hf-silicate films to a NH_3 PDA, excellent electrical characteristics such as EOT scalability, leakage current density reduction, superior thermal stability, and negligible hysteresis have been obtained. This annealing remedies many of the bottlenecks associated with hafnium silicate dielectric. Unlike NH_3 surface nitridation, the proposed process does not seem to degrade the interface properties. Moreover, the temperature and anneal duration of NH_3 PDA technique has significant effect in film quality, so proper optimization of the film based on the desired electrical performance is the key issue. Therefore, HfSiON by NH_3 post-deposition anneal might be a promising alternative for future ultra-scaled MOS gate dielectric.

On the other hand, NH_3 pre-DA technique reduces EOT, though it degrades the mobility. Very thin EOT (~7.4Å) with reasonable mobility using high temperature NH_3 pre-deposition anneal (pre-DA) prior to ALD HfO_2 deposition could be demonstrated in this work. The pre-treatment improved bulk trapping characteristics, though it degraded the interface slightly. The mobility value obtained for such thin EOT dielectric is one of the highest reported to date. Therefore, high temperature (~900^{o}C) NH_3 pre-treated ALD HfO_2 could be regarded as potential candidate for ultra-thin alternate high-k gate oxide as well.

Although nitrogen treatment is an effective way of reducing EOT of the devices, the resulting decrease in mobility values due to nitrogen pile up at the interface is a critical concern to take care of. Considering the two approaches described in this work, NH_3 PDA HfSiON might be a better technique to reduce EOT keeping all other features in good standing. The only disadvantage is that the EOT scalability can't be as aggressive as can be done by surface nitridation technique.

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Chapter 3

Effects of Chlorine (Cl) in High-k Gate Oxides

Like nitrogen atoms, chorine atoms (Cl) in high-k gate oxides also play significant roles in electrical performance of the devices. So far, no systematic study of the effect of chlorine in high-k gate oxides has been done. For high-k deposition using ALD involves $HfCl_4$ as precursor, where Cl atoms present. This Cl can pile up at the interface degrading device characteristics [1]. On the other hand, this can affect the charge trapping characteristics of the gate oxide as well [2]. Moreover, optimization of Cl atoms in obtaining best performance of the device is critically important. This section of the work is devoted to detailed study of Cl atoms in electrical performance in both ALD and MOCVD high-k gate oxides.

3.1. Effect of Precursor Pulse Time on Charge Trapping and Mobility of ALD HfO_2

Among high-k dielectrics processing schemes, ALD HfO_2 showed promising attributes in terms of device electrical and chemical characteristics. The role of atomic layer deposition (ALD) deposition temperature on device characteristics and the role of processing in charge trapping-detrapping have been addressed recently [3-4]. However, the study of precursor pulse time in device performance has not been addressed yet.

This work demonstrates the precursor $HfCl_4$ pulse time's effect on device performance as well as bulk and interface characteristics.

3.1.1. Process Flow and Experiments

The MOSFET process flow started with cleaning the active patterned (shallow trench isolation) wafer with dilute HF solution. The wafers then went through pre-DA (pre-deposition anneal) in NH_3 for 15 sec at 700^{o}C temperature. Following this, 40 cycles of ALD (atomic layer deposition) HfO_2 was deposited using precursor $HfCl_4$ with O_3 as oxidation ambient (300^{o}C, 1 Torr). Precursor pulse time was varied at 150ms, 450ms and 1500ms respectively. 150ms pulse time is the standard (control) for control devices. N_2 post-deposition anneal (PDA) at 600^{o}C, 60 sec was performed on those samples for complete oxidation. Then 10nm ALD TiN layer and 180nm amorphous silicon layer was deposited as a stack gate electrode. After gate patterning, high-k layer was removed with a wet etch process leaving a minimal damage in the extension region. A thin nitride layer (~5nm) was deposited followed by LDD (lightly doped drain) and halo dopant implantation to prevent the process induced damage through plasma process or oxygen diffusion [5] After the thin nitride deposition, 100nm oxide spacer was formed and phosphorous was implanted to dope the source/drain regions (energy = 15KeV, dose = 4e15) followed by activation at 1000^{o}C, 10 sec rapid thermal anneal (RTA) in N_2 ambient. After the Ti-silicide formation, 700nm pre-metal dielectric (PMD) layer was formed. Then W plug with Ti/TiN liner was used to contact the

source/drain and gate electrode regions and Al metal pad was patterned. Finally forming gas anneal was performed at 480^{o}C for 30 minutes.

Electrical characterizations were performed using HP 4284A impedance/gain phase analyzer and HP4156A semiconductor parameter analyzer. EOT was extracted from accumulation capacitance measured at 100 KHz, after accounting for quantum mechanical effects. The single pulse charge trapping measurements were done by Keithley Model 4200-SCS together with a switch matrix and a pulse generator. The physical thickness of the film was measured by optical ellipsometer. The composition of different chemical elements in the films was determined by SIMS (secondary ion mass spectroscopy) analysis.

3.1.2 Electrical Characterization

Fig. 3.1(a) and Fig. 3.1(b) show the effect of precursor pulse time on EOT and leakage current characteristics of the devices. Increasing the precursor, $HfCl_4$ pulse time did not change EOT or leakage current (I_g) as shown, indicating that the total thickness of the samples was almost the same irrespective of pulse time variation. Only the 1500ms pulse showed slight increase in the leakage current value (fig. 3.1.b). The EOT on these samples were found to be around 7Å.

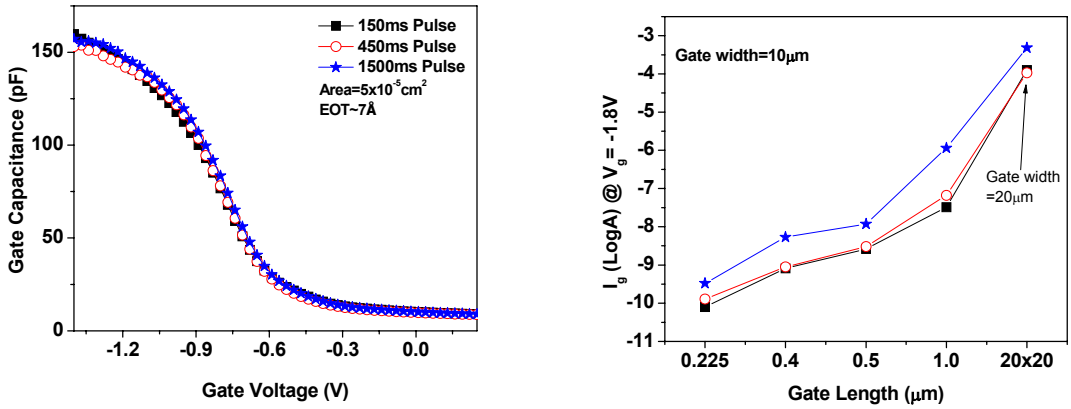

Fig. 3.1. (a) C-V characteristics with ALD precursor, $HfCl_4$ pulse time variation (b) Leakage current (I_g) vs. gate lengths for devices with different ALD precursor, $HfCl_4$ pulse times.

On the other hand, Fig. 3.2 shows the effect of precursor pulse time on mobility of the devices. Increasing the pulse time to 450ms enhanced the mobility slightly whereas 1500ms pulse negated the benefit.

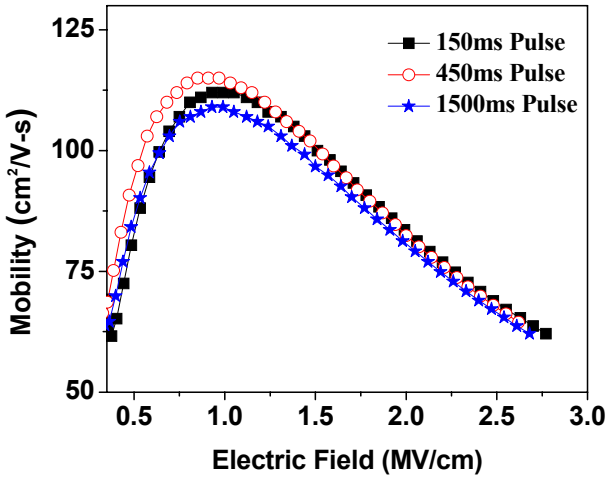

Fig. 3.2. Mobility plots of ALD HfO_2 with different precursor pulse times.

The bulk trapping characteristics of the devices with various pulse times were carried out by single-pulse I_d-V_g measurement and stressing the devices at different constant voltages. A significant reduction in bulk trapping was achieved with the 450ms pulse as shown in fig.3.3 (a). 1500ms pulse device showed less reduction as compared to that of 450ms pulse. Single pulse I_d-V_g measurement is shown if fig. 3.3(b). Inset of fig. 3.3(b) shows the shape of the pulse (rise time=fall time=5μs, width=100μs). I_d values were taken during the rise time by a digital oscilloscope. I_d degradation (ΔI_d) occurs in the device during the pulse width time, which is governed by charge trapping as shown in the figure. Due to charge trapping, I_d can't follow the same line as gate voltage sweeps back during pulse fall time. Hysteresis ΔV can be treated as an indirect measure of charge trapping since it includes the contribution from detrapping during the back and forth sweep. For fair comparison, all the devices were swept up to the same V_g-V_{th}. Thus fig. 3.3(b) also confirmed that the I_d degradation was much lower for 450ms pulse device as compared to control one, indicating that bulk trapping is reduced after increasing the pulse time.

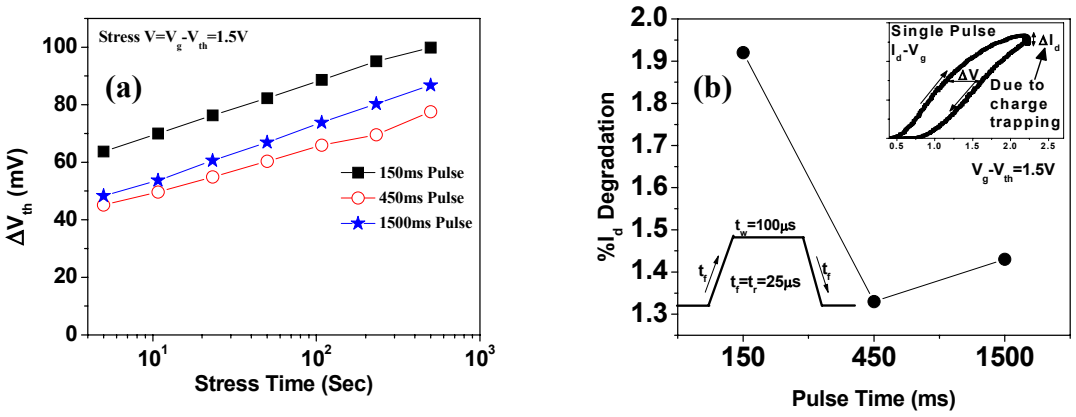

Fig. 3.3. (a) Shifts in V_{th} with stress times show that bulk trapping was reduced significantly for 450ms pulse device (b) I_d degradation after single-pulse I_d-V_g measurement for devices with different pulse times.

Furthermore, improvement in interface characteristics (interface states, N_{it}) was also observed with the 450ms pulse, compared to the control device as shown in fig. 3.4. In all the cases, the 1500ms pulse negated the improvement.

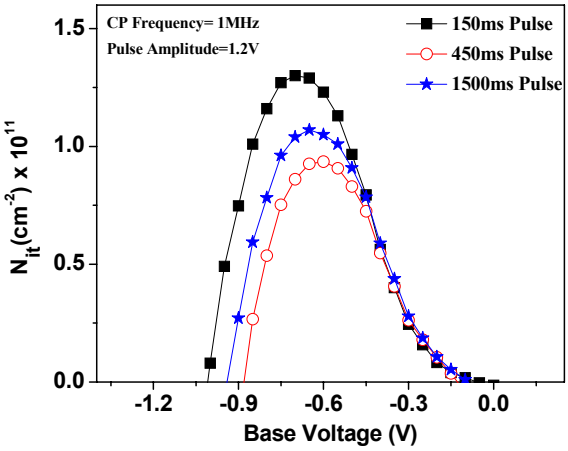

Fig. 3.4. Interfaces states, N_{it} with pulse time variation. The lowest N_{it} was observed for 450ms pulse devices.

3.1.3 Chemical Characterization

Considering the improvement in both bulk trapping and interface characteristics, it could be predicted that increase in pulse time might enhance Hf coverage and more Cl incorporation into the dielectric, which probably reduces trap vacancies in the oxide, forming bonds with Hf atoms and improving overall bond strength in the bulk of the oxide, thus enhancing bulk trapping immunity under stress. To better understand the physical mechanism, SIMS analysis was performed for the three devices as shown in fig. 3.5. From fig. 3.5(a), it is clear that increase in pulse time enhanced Cl incorporation into the dielectric. The peak of Cl composition was also sway from the interface. 600^{o}C N_2 anneal and subsequent source/drain high temperature activation treatment pushed Cl atoms into the TiN gate too. Moreover, Cl penetration into the Si substrate was also reduced. Hence Cl incorporation, which might form bonds with Hf atoms reducing the trap vacancies, might answer the underlying reason behind significant bulk trapping reduction. Fig. 3.5(b-c) shows shifts in N position in the form of HfN and SiN away from the Si substrate. Moreover, both peaks are higher than that in control devices, whereas almost no change in TiN composition throughout the bulk oxide was observed (fig. 3.5.d).

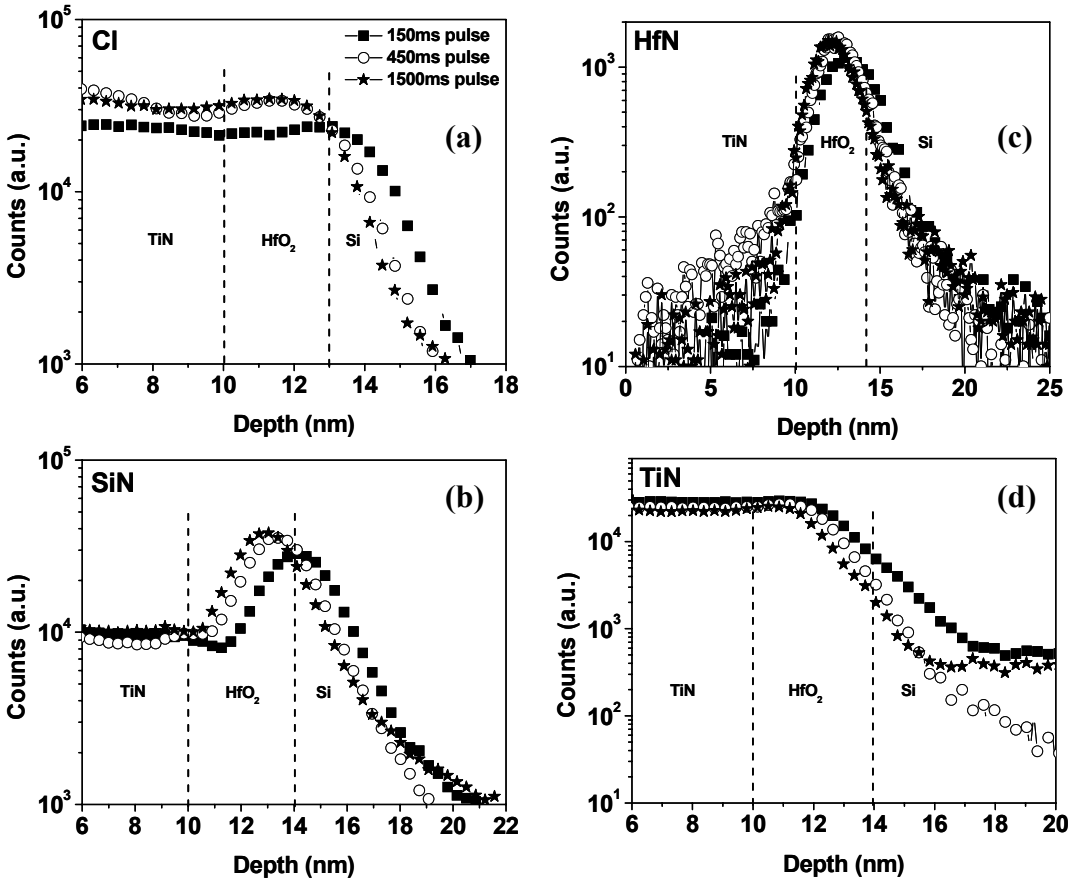

Fig. 3.5. SIMS profile of (a) Cl, (b) HfN, (c) SiN, and (d) TiN. Increase in pulse time shows more Cl incorporation and shifts of N position away from the Si/HfO_2 interface in the dielectric.

Thus the results demonstrate that increase in pulse time improved Hf coverage in the oxide and pushed N position away from the Si-interface, causing less N to pile up at the Si-interface and improving interface characteristics.

3.2 Effects of HCl Post-Deposition Rinsing in Improving CMOS Bias Instabilities and Mobility of MOCVD $HfSi_xO_y$

Previous experiments dealt with investigating the effect of Cl in ALD HfO_2. In this experiment it has been discussed that Cl atoms could also be incorporated into the high-k dielectric by HCl post-rinsing technique. To generalize the Cl effect in high-k, MOCVD $HfSi_xO_y$ has been chosen as the dielectric. It should be noted that HCl post-rinsing was carried out after high-k deposition.

3.2.1. Motivation behind HCl post rinsing

Successful integration of high-k dielectrics into the ultra-scaled devices demands tremendous challenges for below 65nm technology node. Moreover, shortcomings associated with poly gates (e.g. depletion effect, boron penetration, high resistivity and fermi-pinning) pose additional challenges in process integration [6]. Thus dual-metal-gate process would be needed for future CMOS technology. Several candidate metals for dual-metal-gate process have recently been proposed [7-12]. However, the ability of selective etching of first metal gate without affecting the underlying high-k gate oxides is critically important. Dry etching technique is expected to degrade the underlying gate-oxide, and thus degrading the device characteristics. C. S. Park et al [13] has proposed the use of very thin aluminum nitride (AlN_x) buffer layer between metal and gate-oxide to prevent it from being exposed to a metal etching

process. But the issues associated with wet etching of gate oxide without using any buffer layer in between and the consequent effects in device performance (degradation or improvement) haven't been addressed yet. In this work, we have investigated the effects of DI (de-ionized) water and dilute (500:1) HCl post-high-k deposition cleaning on the electrical characteristics of Poly-Si/Hf-silicate CMOS devices. It should be noted that HCl is a common chemical used as etch component in wet etching. It turns out to be the fact that presence of Cl as supplied by HCl post-rinsing has significant effect in electrical characteristics of device performance. Moreover, the effects of high pressure H_2 anneal on device electrical performance and bias instabilities have also been addressed systematically.

3.2.2 Process Flow and Experiments

The MOSFET process flow started with cleaning the active patterned (shallow trench isolation) wafer with dilute HF solution. Afterwards, the wafers went through pre-DA (pre-deposition anneal) in NH_3 for 15 sec at 700^{o}C. Following this, 35Å MOCVD Hf-Silicate was deposited. The devices were divided into three sets. The first set went through DI (de-ionized) water rinsing for 3 minutes, the second set went through dilute HCl (500:1) rinsing also for 3 minutes and the third set didn't have any post-deposition rinsing. NH_3 PDA, 60 sec at 700^{o}C was performed on those three sets for complete oxidation and nitridation as well. Then 200nm ALD amorphous poly-Si layer was deposited as a gate electrode. After gate patterning, high-k layer was removed with a wet etch process leaving a minimal damage in the extension region. A thin

nitride layer (~5nm) was deposited followed by LDD and halo dopant implantation to prevent the process induced damage through plasma process or oxygen diffusion. After the thin nitride deposition, 100nm oxide spacer was formed and phosphorous was implanted to dope the source/drain regions (energy = 15KeV, dose = 4e15) followed by activation at 1000^{o}C, 10 sec rapid thermal anneal (RTA). After the Ti-silicide formation, 700nm pre-metal dielectric (PMD) layer was formed. Then W plug with Ti/TiN liner is used to contact the source/drain and gate electrode regions and Al metal pad was patterned. Finally forming gas anneal was performed at 480^{o}C for 30 minutes.

Electrical characterizations were performed using HP 4284A impedance/gain phase analyzer and HP4156A semiconductor parameter analyzer. EOT was extracted from accumulation capacitance measured at 100 KHz, after accounting for quantum mechanical effects. The single pulse charge trapping measurements were done by Keithley Model 4200-SCS together with a switch matrix, and a pulse generator.

3.2.3 Electrical Characteristics and Bias Instabilities

Fig. 3.6 shows the leakage current and mobility characteristics as a function of EOT of Hf-silicate dielectric. EOT decreased which was accompanied by an increase in leakage current, while high field (@1 MV/cm) mobility improved after H_2O and HCl post-cleaning. The mobility improved further (4~6%), while EOT remained unchanged

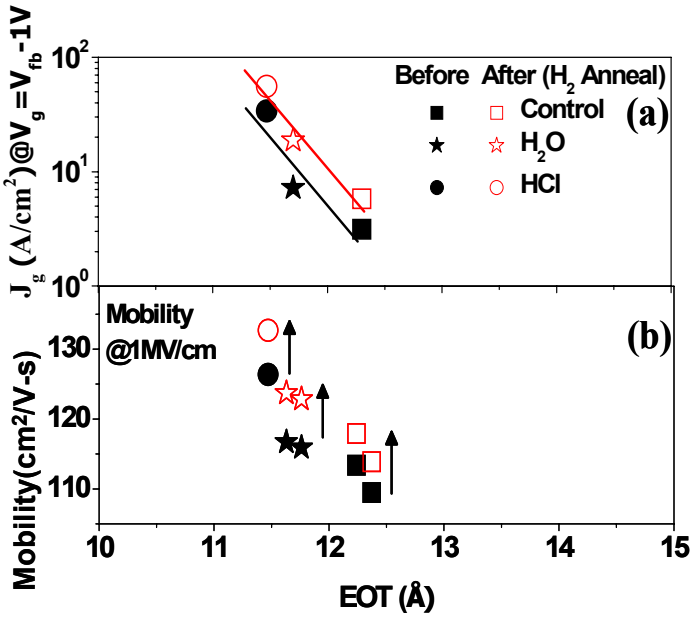

Fig. 3.6. (a) J_g-EOT and (b) Mobility-EOT plots. EOT decreased, while mobility increased after post-treatment. High-pressure H_2 anneal improved mobility, not EOT.

after high pressure H_2 anneal (fig.3.6.a). Mobility improvement for all three sets of samples came from the reduction of interface states, N_{it} (fig. 3.7).

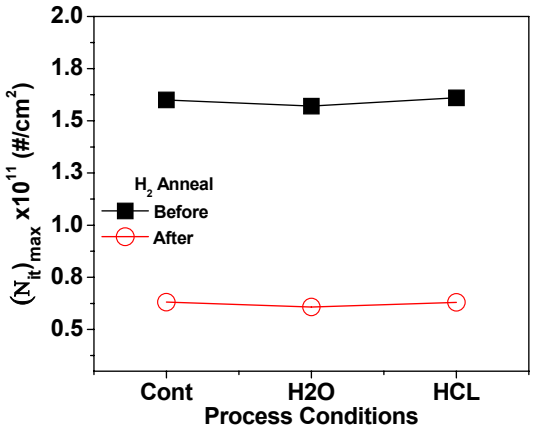

Fig. 3.7. No change in Nit after post cleaning. H_2 anneal improved N_{it}. (CP frequency=1.5MHz, Pulse Amplitude=1.2V)

It is interesting to note that N_{it} values for three sets of devices are almost the same. Thus mobility improvement after HCl rinsing didn't come from interface states reduction.

To further investigate the mechanism, nMOS and pMOS devices were stressed in inversion regions at the same (V_g-V_{th}) to figure out the bulk trapping characteristics under substrate (nMOS) and gate injection (pMOS). For nMOS, significance reduction in charge trapping has been observed in the HCl treated devices, in comparison to control and H_2O treated devices (fig. 3.8).

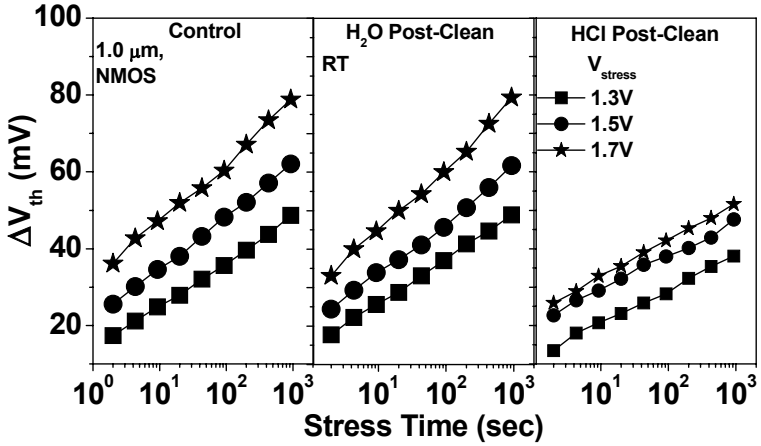

Fig. 3.8. ΔV_{th} vs. stress time. ΔV_{th} could be reduced significantly after HCl post-cleaning. $V_{stress}=V_g-V_{th}$

As shown in fig. 3.9, high pressure H_2 anneal didn't have any effect on bulk trapping characteristics in the devices. The results prove the fact that high pressure H_2 only improve mobility of the devices, it didn't change any bulk trapping behavior. Thus the improvement in bulk trapping characteristics completely came from HCl post-rinsing. Moreover, pMOS devices also showed similar bulk trapping improvement as nMOS devices (fig. 3.10)

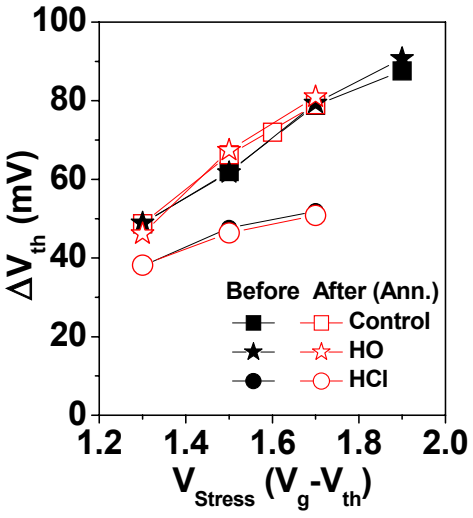

Fig. 3.9. No change in ΔV_{th} after H_2 anneal. Still HCl treatment showed lowest ΔV_{th}. (nMOS, 1μm, RT. T_{stress}=928s)

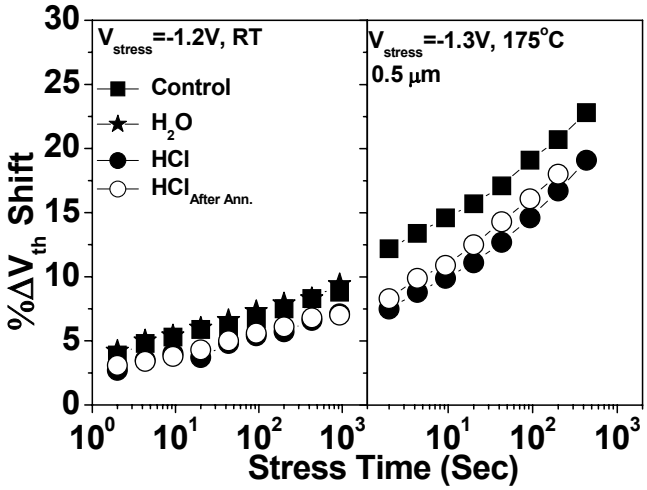

Fig. 3.10. ΔV_{th} for pMOS devices showed same trend as nMOS. The trend is true at high temperature. $V_{stress}=V_g-V_{th}$

Inversion SILC for nMOS, which is due to trap assisted tunneling, also indicated that the HCl treated devices exhibit reduced trap density (fig. 3.11).

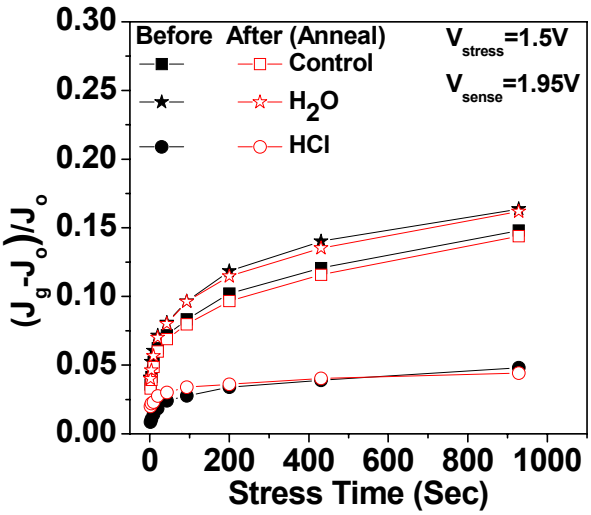

Fig. 3.11. Inversion SILC with stress time for substrate injection in nMOS showed significantly lower value for HCl treated devices. This trend is also true for pMOS (not shown). (The stress and sense voltage was $V_{stress}=V_g-V_{th}$ and $V_{sense}=V_g-V_{fb}$ respectively)

Moreover, single pulse I_d-V_g measurements on these three sets of devices further illustrated a significant bulk trapping reduction in HCl treated samples as shown in fig.3.12.

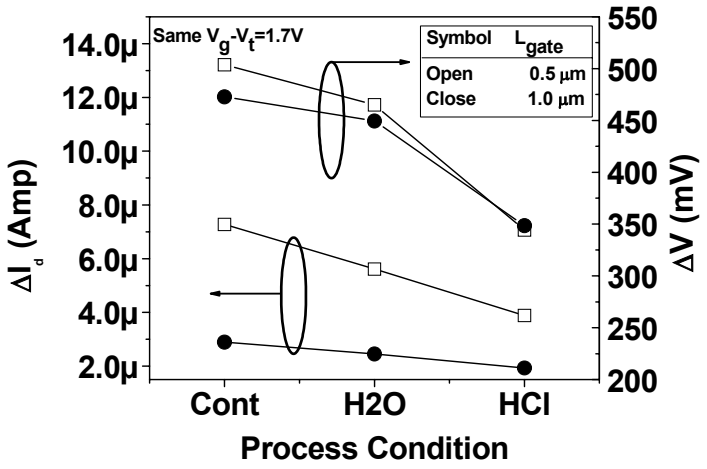

Fig. 3.12. Comparison of I_d degradation (ΔI_d) and I_d-V_g up-down width (ΔV) for different post-treated samples. Still HCl post treatment shows the highest improvement in bulk trapping immunity.

To investigate the interface properties of these devices, we performed charge pumping experiments at different frequencies with pulse amplitude of 1.2V (fig. 3.13.a) and at different pulse amplitude with 1MHz frequency (fig. 3.13.b). Only maximum interface states, $(N_{it})_{max}$ has been plotted for comparisons. The results show that no significant difference in $(N_{it})_{max}$ could be seen for those three sets of samples. This confirms that the improvement in HCl post-treated samples didn't come from any improvement in interface states, rather from the improvement in bulk trapping characteristics.

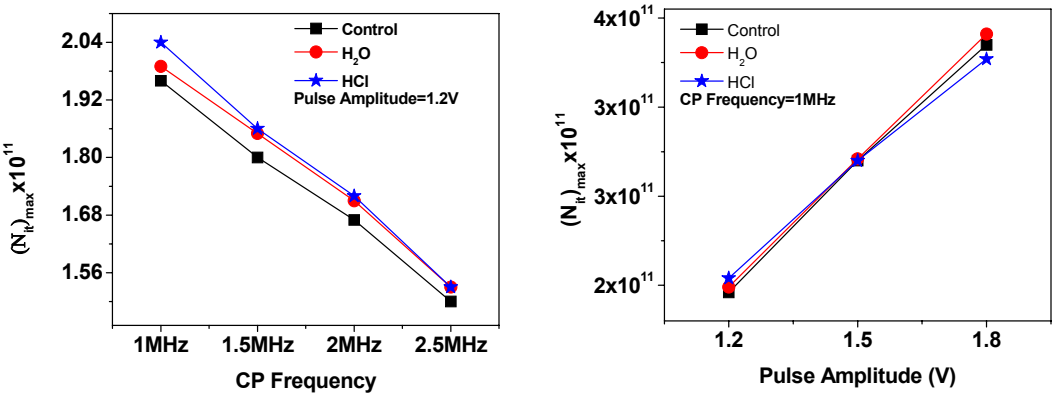

Fig. 3.13. Interface states for three sets of sample with (a) varying frequency (b) varying pulse amplitude. No significant difference could be observed.

Dilute HCl and H_2O post-treatment might have slight etch effect, which supports the results of EOT reduction (fig.3.6.a). It could be possible that Cl penetrates during post-HCl cleaning, and forms bonds with Hf/Si atoms, reducing trap vacancies into the bulk oxide, improving overall bond strength of bulk oxide, and thus enhancing bulk trapping immunity under stresses.

3.3 Summary

In summary, it can be asserted that Cl incorporation into high-k dielectrics has significant effect in electrical performance of the devices. For both of the cases of Cl treatments, bulk trapping immunity of the oxide has been improved.

For ALD HfO_2, it was found that precursor, $HfCl_4$ pulse time showed significant effect on its electrical and chemical characteristics. Improvement of bulk trapping immunity under stress and reduction of interface states after increase in pulse time was observed. Hence increase in the $HfCl_4$ pulse time appeared to lead to improved Hf coverage and comparatively larger Cl incorporation into the oxide, resulting in reduced vacancies in the oxide, which caused bulk trapping reduction. The improvement of interface characteristics with increase in pulse time has been attributed to shift in nitrogen peak position away from the bottom interface of the device. Optimization of pulse time can improve the device performance.

For MOCVD $HfSi_xO_y$, HCl post-deposition cleaning of high-k gate oxide has potential positive attributes to device characteristics. Dilute HCl post-cleaning showed the greatest improvement in both mobility and bias instabilities of the devices in comparison to control and H_2O post-treated samples. Improvement in bulk trapping immunity rather than in Si-interface properties has been attributed to the observed potential enhancement in electrical characteristics. It could be possible that Cl penetrates during post-HCl cleaning, and forms bonds with Hf/Si atoms reducing trap vacancies into the bulk oxide, improving overall bond strength of bulk oxide, and thus

enhancing bulk trapping immunity under stresses. High pressure H_2 anneal improved mobility further, but had no effect on bulk charge trapping characteristics and EOT.

3.4 References

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Chapter 4

Investigation of Transient Relaxation in HfO_2 Gate Oxides

To meet the requirement of 45nm technology node and below, high-k dielectric like HfO_2 has been evolved as a critical material to overcome the integration challenges associated with it. Along with the integration challenges, valid characterization techniques, and proper methodologies to study the reliability of Hf-based dielectric have been evolved as crucial issues [1-2]. Fast transient charging and discharging effect in Hf-based gate oxides are found to be the sources of various undesirable characteristics of high-k devices, such as threshold voltage (V_{th}) instability, frequency dependent mobility values, and C-V hysteresis [1-9]. These undesirable properties might lead to inaccurate characterization and wrong conclusions, which may obscure the proper optimization of high-k dielectrics. The transient charging has been addressed as the dominant mechanisms for device bias instabilities [10-13] and hot carrier instabilities [14-15]. Moreover, due to this transient effect, the dc I_d-V_g (drain current-gate voltage) and C-V (capacitance-voltage) measurement might result in erroneous results, which lead to inaccurate mobility values for high-k dielectrics [1]. Young et. al. [16] shows that using ultra fast single pulse (35ns) I_d-V_g measurement, the saturation current of high-k dielectric has increased by as much as ~40% at high V_g, encouraging the implementation of high-k dielectrics in high frequency and low duty cycle CMOS device circuits, where charge trapping is insignificant [17]. Polarity (substrate vs. gate

injection) and gate electrode (poly vs. metal) dependence of the transient trapping-detrapping have also been addressed in recent studies [7,9,18]. The relaxation effect has been observed in conventional gate oxides in terms of transistor bias instabilities [19-23], hot carrier instabilities [24-25] as well. Most of the studies in fast transient charge trapping suggest that the charge accumulation under substrate injection into the high-k gate oxide is recoverable and full recovery could be achieved when a negative pulse is applied following the positive stress [1,6,7,9,10,12,18]. The systematic study of the role of both bulk charge trappings and interface states' passivation effect on transient relaxation (TR), and their implication to high-k gate oxide's wear-out mechanism haven't been addressed yet. This work demonstrates transient relaxation behavior, the competing role of bulk and interface trapping in relaxation, the temperature effect on TR in high-k, and correlation of TR behavior with dielectrics' wear out characteristics. A simplified mathematical model has been proposed to understand the underlying physics behind the relaxation behavior.

4.1 Fabrication flow of Device under Test

The MOSFET process flow for control HfO_2 nMOS (n-channel metal-oxide-semiconductors) devices started with cleaning of the active patterned wafers in dilute HF solution followed by Hf deposition via DC magnetron sputtering (30 mTorr, Ar, room temperature) and rapid thermal annealing (RTA) of the deposited films at 600°C in N_2 ambient. Film thickness was ~50Å measured by ellipsometer. TaN gate was

deposited using DC sputtering (N_2+Ar, 10 mTorr, room temperature) followed by reactive ion etching (RIE) in Cl_2/He mixture for gate patterning. Phosphorous was implanted to dope the source and drain (S/D) regions (energy=50 KeV, dose=$5x10^{15}$ cm^{-2}). S/D dopant activation was done by RTA in N_2 ambient at 950°C for 1 min. Sputtered aluminum was used for both interconnect and backside metallization. The final sintering was done at 400°C in forming gas for 30 minutes. TaN/HfO_2/HfON/p-Si nMOS device was also fabricated using the sputtering technique, except that N_2 and Ar were flown during Hf sputtering for the bottom HfON stack, followed by Hf deposition in Ar ambient for the top HfO_2 stack. The combined stack was annealed as mentioned above.

4.2 Measurement Set-up and Stress Wave-Shape for Static and Dynamic Stressing

Stressing was performed at the gate terminals of devices using a DC source and pulse generator. The stress wave shape of voltage applied at the gate terminals is shown schematically in fig. 4.1. The corresponding shape of gate current is also shown schematically. Pre-stress-I_d (I_n) was measured at the base voltage, V_n=0.5V using 4156A semiconductor parameter analyzer (SPA). Post-stress I_d samplings with time [I(t)] were also monitored at the same V_n. Stress experiments were carried out at voltages ranging from 1.7V to 2.1V. Temperatures were varied from 25°C (RT) to 125°C.

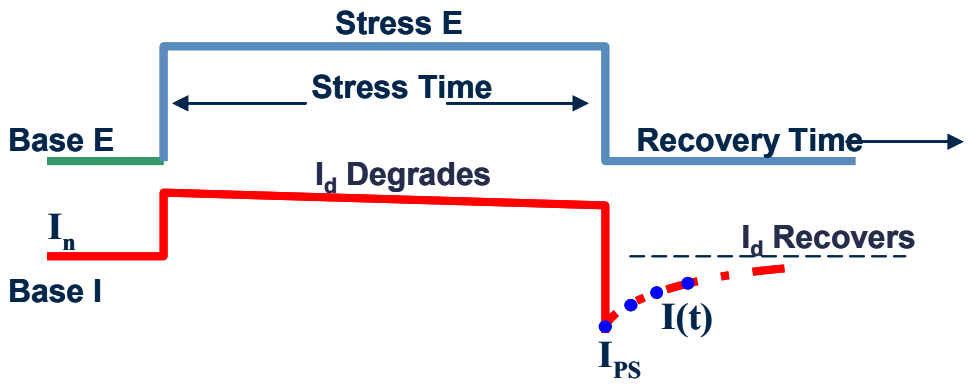
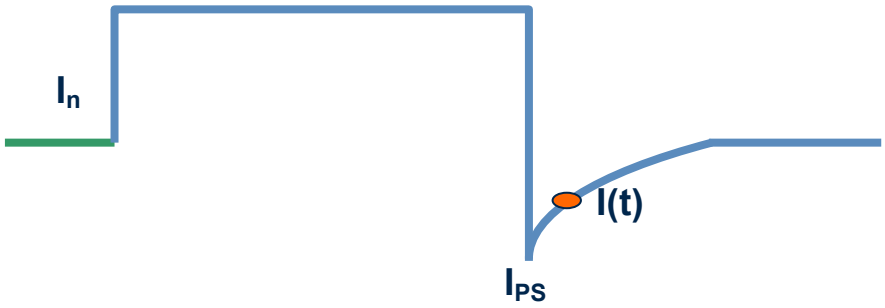


Fig. 4.1. Stress and current wave shape under stress and recovery

4.3 Definition of %Relaxation or %Recovery



$$\% \text{ Recovery} = [\{I(t)-I_{PS}\}/\{I_n-I_{PS}\}]*100$$

The %Recovery is simply percent of drain current recovered after degradation of time zero current due to stress. For measurement and analysis of the experimental data, the term %Relaxation or %Recovery has been used.

4.4 Effect of Sampling Interval of SPA 4156A in %Recovery

The sampling drain current immediately after stress is sampled by SPA 4156A used in this study. The interval time is very critical to get the first read-out of I_d immediately after stress. Fig. 4.2 shows the effect of sampling interval time on %Recovery (%R). As shown, the shorter is the interval, the faster is the %Recovery calculated using the equation discussed previously. For the limitation of the measurement system (SPA), the lowest sampling interval time of 560 μsec was chosen for I(t) samplings.

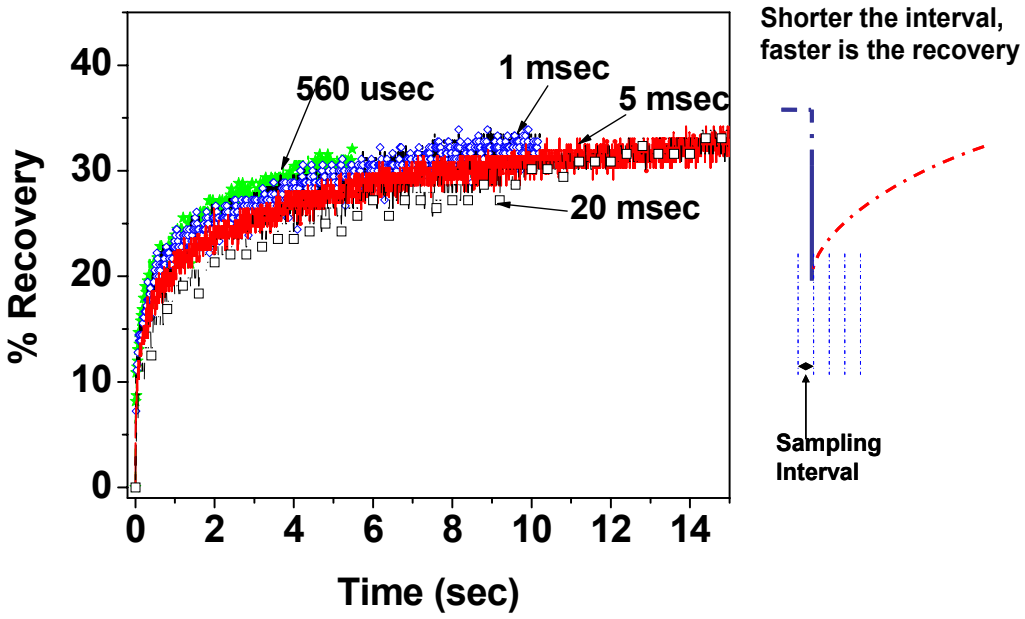


Fig. 4.2. Effect of sampling intervals on %Recovery. The shorter is the interval, the faster is the recovery rate. The shortest we could use was 560 μsec

4.5. Relaxation under Static and Dynamic Stress Conditions

Fig. 4.3(a) shows the I_d relaxation at 0.5V toward the pre-stress value (I_n) after being stressed by different constant voltage stress conditions shown. Inset of fig. 4.3(b) shows a schematic of the drain currents (I_d) mentioned. As shown, I_n was degraded upon stress. The first post-stress current (I_{PS}) is taken by the system immediately after stress. The sampled current read-outs with relaxation time, I(t) were monitored for various device dimensions and ΔI_d [$I(t)-I_{PS}$] is shown in fig. 4.3(a). With %Relaxation defined as $\%R=[\{I(t)-I_{PS}\}/\{I_n-I_{PS}\}]x100$, all the currents follow a unique curve up to certain stress limits (fig. 4.3.b). The stress limits are: stress voltages ranging from 1.7V to 2.1V, stress times ranging from 1000s to 1800s, and temperatures from 25^{o}C to 120^{o}C. Also the relaxation follows the unique line if re-stressed at the same voltages mentioned at the same times.

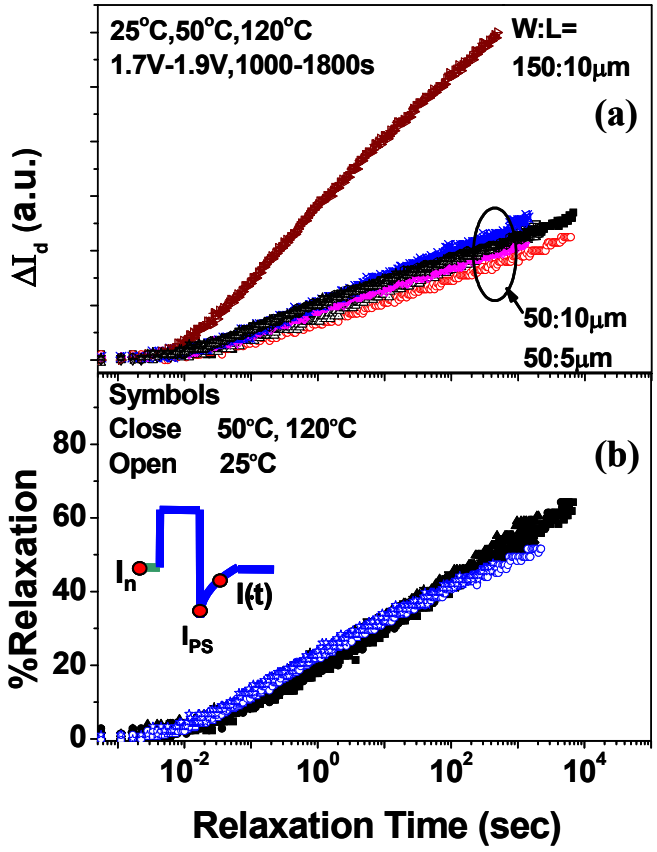


Fig. 4.3. (a) Relaxation of I_d (ΔI_d) for different device dimensions after various stress conditions shown. (b) %R, calculated by pre- and post-stress currents, lies in a unique line irrespective of stress conditions shown. Thus %R gives a simplified unique relaxation behavior if stressed up to certain stress limits.

Thus %R gives a simplified unique relaxation behavior up to certain stress levels mentioned above. The results reveal the fact that I_d degradations are different for

different stress conditions (different stress voltages or stress times), but the relaxation rate of the degraded current (I_n-I_{PS}) is the same if stressed up to certain limits. It is interesting to note that the temperature showed negligible effect on %R. Moreover, %R for devices stressed dynamically (50% duty unipolar stress, 0V to 1.9V) at RT followed the same unique line (fig. 4.4) irrespective of stress frequencies. This could be due to the fact that the characteristic time for bulk trapping (as it is believed that bulk trapping/detrapping is the dominant mechanism in transient relaxation [1,6,7,9,10,12,18]) is so small (even <100ns) that the stress frequency (up to 10MHz) didn't have any effect on bulk trapping characteristics of high-k devices. Thus $\%I_d$ relaxation followed the same line irrespective of stress frequency.

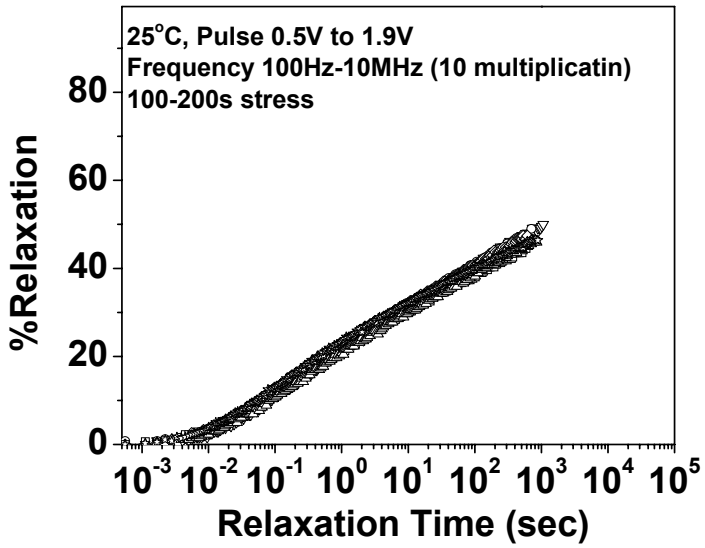


Fig. 4.4. %R for devices under dynamic stress at different frequencies. Still I_d relaxation follows a unique line irrespective of stress frequencies.

4.6 Background Mathematical Model and Interpretation

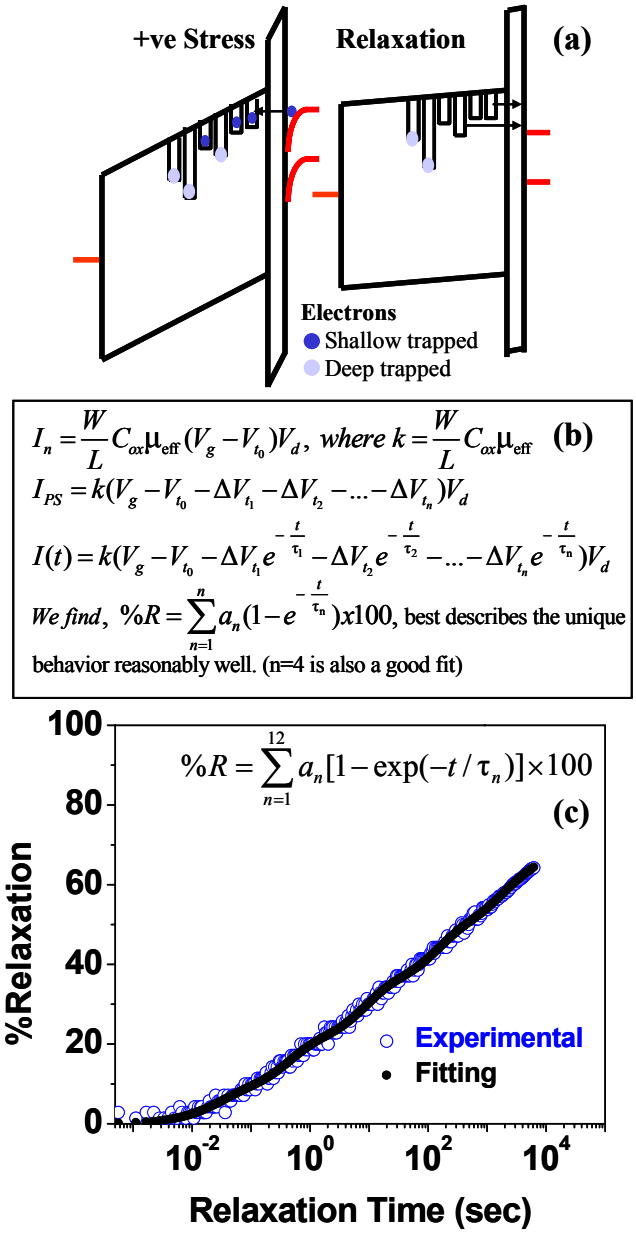


Fig. 4.5. (a) Schematic band diagram of high-k gate oxide during positive stress and relaxation period. (b) Calculation details of %R. (c) Fitting of mathematical model with experiments.

Upon positive stress, the electrons could be injected, distributed, and trapped as shown schematically in fig. 4.5(a). Carriers trapped in shallow potential can relax very fast (small characteristic detrapping time constant, τ) giving rise to fast transient relaxation, while deep-trapped carriers take significant time to relax (large τ). Thus taking V_d=50mV and writing the pre- and post-stress current components as shown in fig. 4.5(b), the simplified equation for %R best describes the observed experimental results (fig. 4.5.c). In this simplification, the effective mobility (μ_{eff}) has been assumed to be constant throughout the stress and relaxation periods for simplicity. Moreover, both bulk oxide and interface trapping/detrapping have been included in the threshold voltage (V_t) shift and V_t relaxation. It is interesting to note that the only dependence of this simplified equation of %R is the characteristic time,τ, and not any device parameter. This τ dependency of %R could explain the uniqueness of %R with relaxation time.

4.7 Stress Polarity Dependence

Device was stressed +1.9V and -2.3V for 30 min. Both ΔI_d (change in I_d) and ΔI_g (change in leakage current, I_g) was monitored at V_n=0.5V (fig. 4.6.a-b). Note that after the first initial transients, relaxation was gradual in time after positive bias, whereas it almost stopped with no apparent further relaxation after negative bias. The results suggest that the substrate injection incurs relaxable instabilities, while gate injection creates some permanent degradation in the oxide [18]. Recently Lu et al [26] reported for TiN/HfO_2 stack under gate injection that hole trapping from substrate is the

dominant trapping mechanism than electron trapping. Probably the injected holes from the substrate under gate injection get trapped permanently in the oxide and cause more degradation hindering the oxide to relax back to its original state with time, as shown schematically in fig. 4.7.

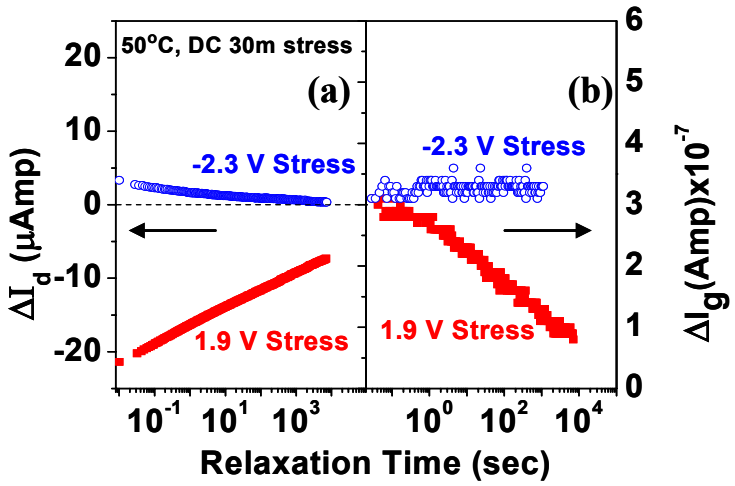


Fig. 4.6. (a) I_d and (b) I_g relaxation in magnitude under positive and negative stress voltages. nMOS positive stress (substrate injection) induced more relaxable trapping, while greater portion of non-relaxable trapping was created by gate injection.

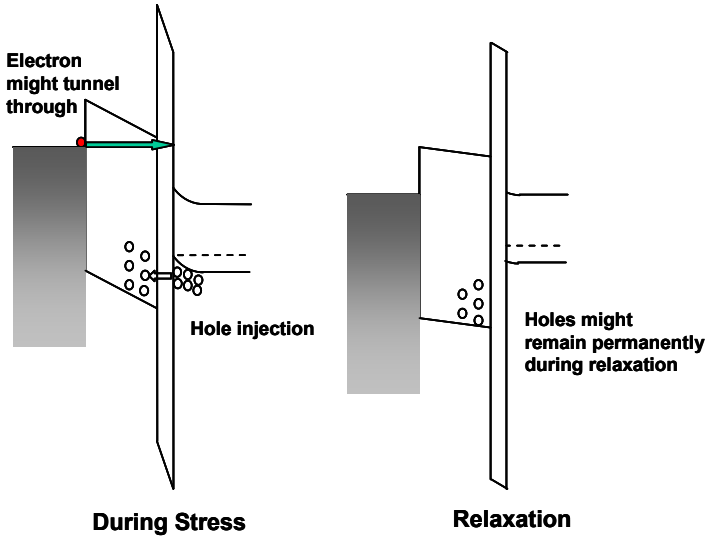


Fig. 4.7. Schematic energy diagram showing more probability of hole trapping than electron trapping under gate injection. During relaxation, the holes can't be detrapped quickly, rather most of them remains trapped, ausing permanent degradation in the devices.

4.8 Role of Bulk & Interface Trapping in Relaxation

Fig 4.8 shows the fast transient relaxation in charge pumping (CP) current, I_{cp} immediately after positive stress of 1.9V, 30min [27]. The initial fast transient relaxation in CP current includes both bulk and interface relaxation. To take the I_{cp} due to interface only, in the rest of the section, we took I_{cp} values after few seconds of initial transients to let the bulk trapping component of I_{cp} to decay down. The gradual decrease in I_{cp} values with times, as shown in fig. 4.8, indicates that interface also passivates with time after stress removal.

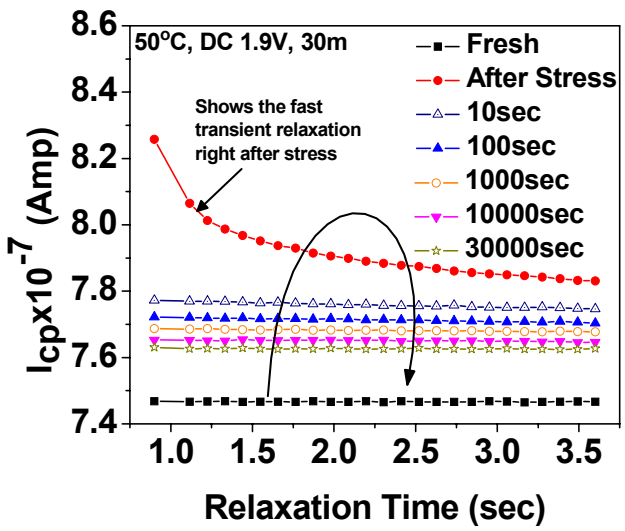


Fig. 4.8. Transient CP current, I_{cp} relaxation, indicating that interface trapping also relaxes after being stressed. The fast initial transient relaxation immediately after stress was due to bulk detrapping.

To investigate the role of bulk and interface trapping in transient relaxation, devices were stressed at 2V, 200s. ΔV_t and ΔI_{cp} were taken right after stress. Device was then allowed to relax for 10s, after which negative pulses of –0.25V to -1V were applied. ΔV_t and ΔI_{cp} measurements were carried out as usual. V_t recovered quickly with the increase of negative pulse voltages (fig. 4.9.a).

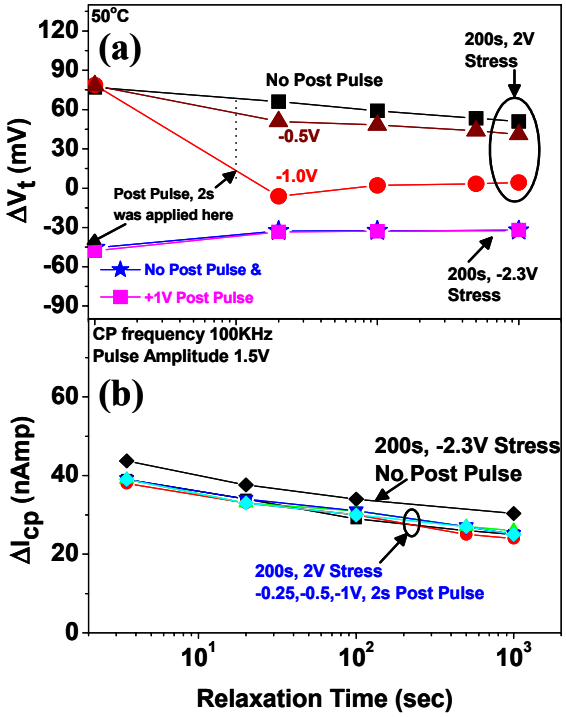


Figure 4.9. (a) V_t relaxation with or without post pulses after positive and negative stress voltages. Complete recovery could be obtained for devices under positive stress, while recovery is negligible for devices under negative stress. (b) I_{cp} relaxation after the same stress conditions coincides in the same line, indicating that post pulses don't have any effect on interface relaxation.

Interestingly, a complete recovery was obtained for negative pulse of –1V. On the other hand, for devices stressed at –2.3V, 200s, no significant relaxation was observed. Even –2.3V, 200s stress followed by 1V, 2s pulse had no effect in fast transient detrapping. These results indicate that negative charge trapping upon substrate injection can quickly

be relaxed by the application of negative pulses. But, for all of the cases, relaxation of interface states couldn't be altered by application of short negative pulses, rather they coincided on the same curve (fig. 4.9.b). Also note that, increase in I_{cp} after negative stress was slightly higher than that after positive stresses, but the passivation still follows the same trend. The results suggest that gate injection creates a greater portion of permanent degradation in the oxide. Hence it could be concluded that (a) both bulk oxide and interface trapping upon substrate injection show transient relaxation in high-k gate oxide, but bulk trapping is mostly relaxable, whereas interface trapping couldn't be relaxed/passivated completely, (b) mechanism of interface passivation remains the same irrespective of stress histories, (c) gate injection creates more interface degradation than substrate injection, but still passivation mechanism remains the same.

Now it has been shown that the bulk trapping causes device bias instabilities and is responsible for various undesirable characteristics in devices that manifested as PBTI (positive bias temperature instability), NBTI (negative bias temperature instability), TDDB (time dependent dielectric breakdown) etc. But question remains whether bulk trapping creates any permanent degradation in the oxide and, if so, how. To investigate further, nMOS devices were stressed at room temperature at 1.9V, for stress times 10-100s and 1000-1800s ranges (fig. 4.10). The reduction of %R for devices stressed longer

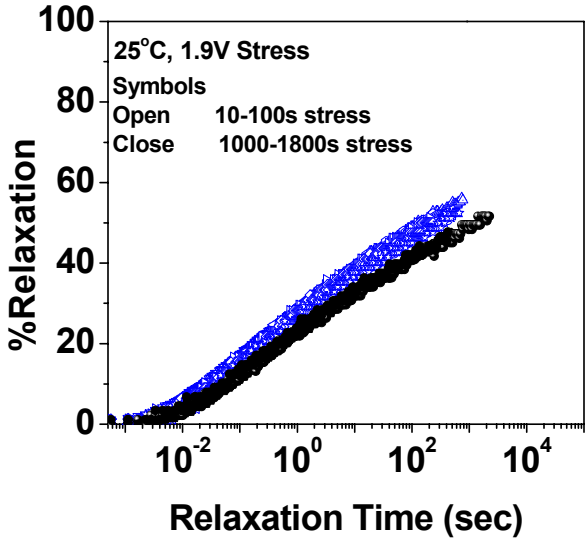


Fig. 4.10. %R comparison for devices stressed for short (10s-100s) and long (1000-1800) times. Slight difference in %R is possibly due to increase in oxide non-relaxable degradation, which increases characteristic time constants, τ.

times could be due to damage created by bulk trapping, which possibly increases the τ values of %R equation, thus reducing the relaxation rate (note that uniqueness of %R between two stress ranges are different). To answer this question more clearly, the devices were stressed from 1.5V to 4V, 10s. I_d relaxation (%R) diminishes with increasing stress voltages probably due to increase in bulk degradation (fig. 4.11). This is consistent with what Degraeve et al [28] reported stating that steep increase in HfO_2 bulk trap density for positive stress is likely to cause breakdown of the HfO_2 layer.

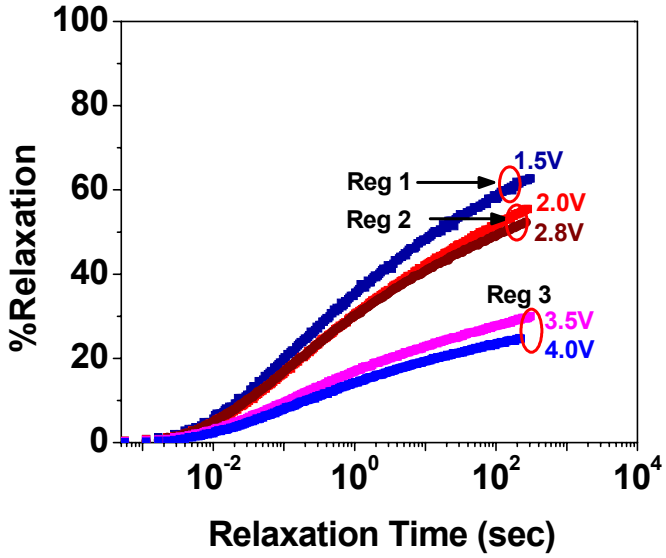


Fig. 4.11. I_d relaxation after increasing stress voltages. Significant decrease in %R was possibly due to dramatic increase in degradation due to bulk trapping.

4.9 Effect of τ in Different Dielectric Structures

Fig. 4.12(a) shows that %R of HfO_2-top/HfON-bottom structure has higher %R compared to HfO_2 (same electric field stress and same time). Fig. 4.12(b) indicates that the HfO_2-top/HfON-bottom dielectric shows significantly smaller ΔN_{ot} (change in oxide trapped charges) under the same stress conditions (same electric field, since the EOT was slightly different). N_{ot} was calculated as $\Delta N_{ot}=\Delta N_{tot}-\Delta N_{it}$, where N_{tot}=total oxide trapped charges calculated from V_t shifts under stress and N_{it}=interface states obtained by charge pumping measurement after each of the stress conditions. Thus it suggests that increase in %R could be due to increase in immunity to bulk trapping,

which reduced the number of deep trappings (with shorter τ values) facilitating faster transient relaxation.

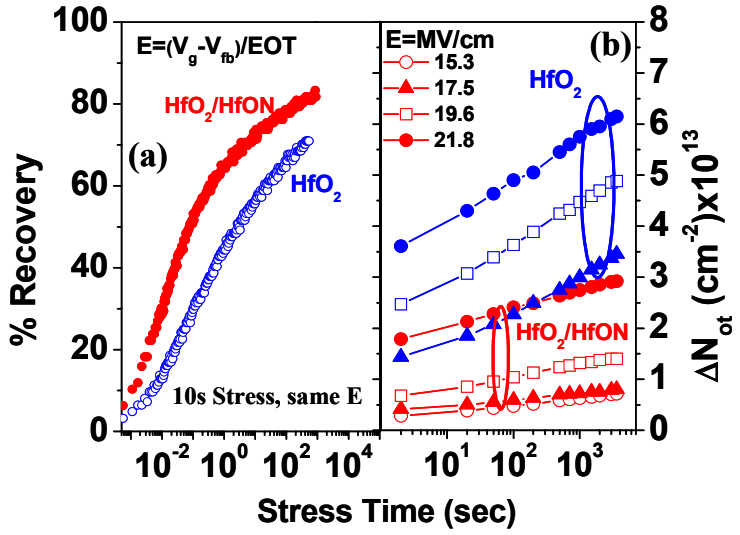


Fig. 4.12. (a) Comparison %R between two dielectric structures shown. One showed faster detrapping possibly due to smaller τ's compared to the other one. (b) Gate oxide stack with faster transient relaxation (HfO_2-top/HfON-bottom) showed higher trapping immunity, indicating that less number of electrons is likely to be trapped in deep potentials.

Single pulse I_d-V_g technique, which essentially probes the degradation due to the bulk trapping effect in high-k dielectrics, also showed the same bulk trapping immunity [16]. It should be noted that, the reduction in τ values primarily came from the reduced bulk trapping efficiency in HfO_2/HfON stack.

4.10 Effect of Dynamic Pulse Width in Transient Behavior

Fig. 4.13 shows the transient relaxation in each of the off-periods after dynamic unipolar stress for 10% and 90% duty (stress time, T_{on}=30s, 1Hz). It could be predicted from our model that for the same stress "on" time, higher duty cycle should induce less relaxable trapping (thus increasing τ values) compared to lower ones. Therefore, %R for low duty cycle showed faster recovery (see inset). Now application of train of pulses of very short width (~50ns) could eliminate or significantly reduce the bulk trappings in high-k oxide [16].

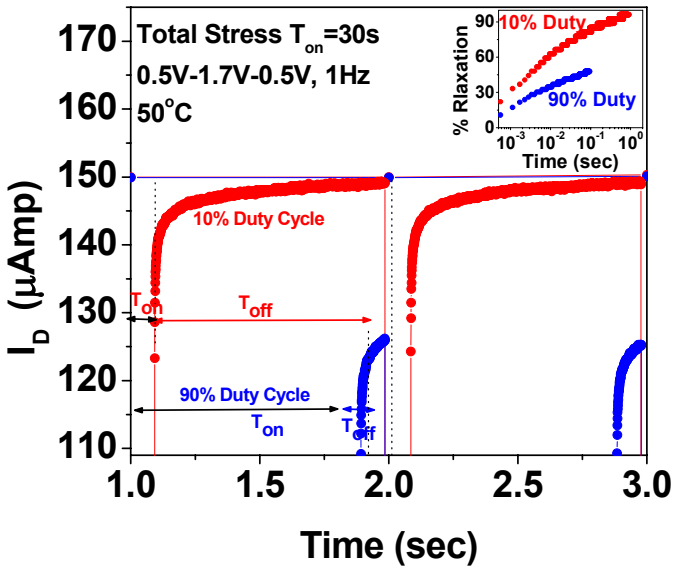


Fig. 4.13. Comparison of transient detrapping for device under dynamic stress of 10% and 90% duty (same T_{on}, 1Hz). Inset is %R for both cases. For the same stress "on" time, longer duty pulses in each of the pulse period might induce less relaxable trapping (thus increasing τ values) compared to shorter ones.

Fig. 4.14 shows comparison of I_d relaxation after being stressed for 9s ("on" time) by unipolar pulses of width 50ns (~0.1% duty) vs. 9950ns (~99,9% duty). As expected, short width makes the transient faster, possibly because of less deep trapping into the bulk oxide. Note that, the applied pulse amplitude is high (3V), so both devices degraded severely (as was observed in fig. 4.10), but the difference in I_d relaxation possibly came from reduced bulk trapping.

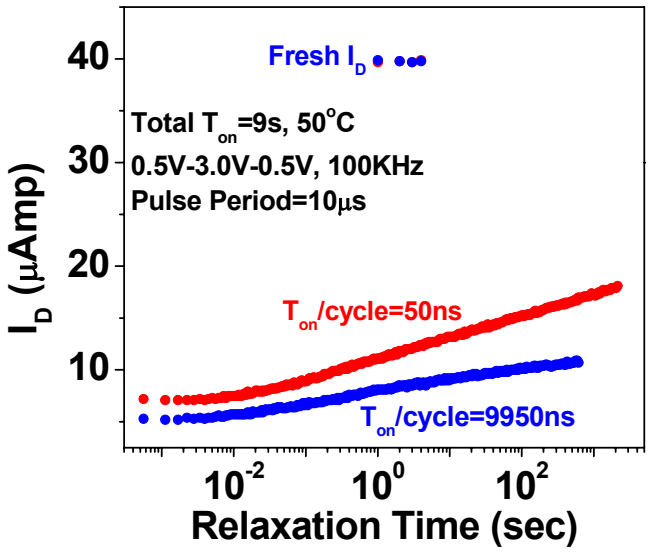


Fig. 4.14. I_d relaxation for devices stressed at the same frequency and T_{on} with ~0.1% duty and ~99% duty. Faster transient was seen for very short pulses, due to reduction in bulk trapping (thus reduction of τ values).

4.11 Effect of Temperature on Relaxation

It has been observed that temperature had no or negligible effect on %R (fig.1.b). To investigate it further, devices were stressed at 25°C, and relaxation was

monitored at 25°C, 75°C and 120°C, by turning the hot chuck "on" immediately after stress (fig. 4.15.a). Hot chuck took about 10s to ramp up as shown in the fig. 4.3(a). As shown %R increased with the increase in temperature applied during relaxation, but no increase in interface passivation was observed (fig. 4.15.b).

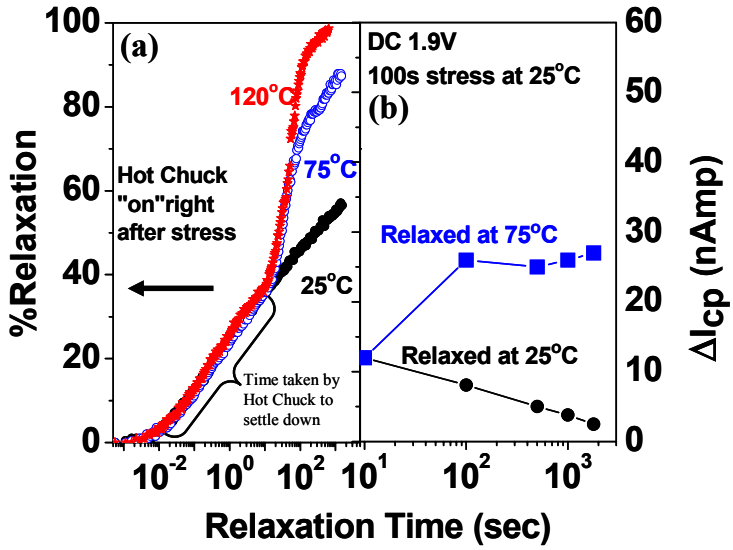


Fig. 4.15. (a) Effect of temperature on %R. Device was stressed at 25°C and relaxed at 25°C and higher temperatures shown. (b) ΔI_{cp} monitored at 25°C and 75°C. Increase in I_{cp} at 75°C indicates that dramatic %R increase wasn't due to temperature, rather due to V_t dependency on temperature.

Thus the increase in %R might be due to V_t dependence on temperature (since V_t decreases as temperature increases, and we already know that %R is coming from V_t relaxation after stress), and not due to any dependence of significant detrapping effect

on temperature in high-k gate oxides. The slight increase in %R at higher temperature than room temperature (fig. 4.3.b) could be due to slight τ dependence on temperature.

4.12 Summary

In summary, integration challenges and proper methodology of defining reliability of HfO_2 based high-k devices has to be taken into strong consideration. Transient relaxation is seen to be an undesirable issue in high-k gate oxides. Hf-based dielectrics show a unique relaxation behavior if stressed. HfO_2 bulk charge trappings, which play a major role in bias instabilities, are mostly relaxable, while interface degradation can't be passivated completely. Irrespective of stress history, interface passivation mechanism remains the same. Device with higher trapping immunity shows faster relaxation probably due to reduced bulk trapping efficiency which leads to faster relaxation. %Relaxation dependency of HfO_2 on temperature is insignificant. A good agreement of the proposed simple model with experimental results has been obtained. Under substrate injection device degradation is mainly triggered by bulk charge trapping in the oxide, so process issues of Hf-based oxides need to be investigated carefully to reduce pre-existing defects and bulk trapping in the oxides.

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Chapter 5

Reliability Study of Hf-based Gate Oxides

In this section, basically the reliability of Hf-based gate oxides, for example HfO_2, Hf-silicate, will be discussed. To estimate the viability and projected life time of high-k dielectrics, reliability study in terms of TDDB (time dependent dielectric breakdown), TZDB (time zero dielectric break down), charge trapping characteristics, PBTI (positive bias temperature instability), NBTI (negative bias temperature instability), hot carrier degradation in high-k MOSFET devices demand profound significance. The quality and reliability of Hf-based gate oxides could be affected by process conditions [1], crystallization of gate oxides, phase separation [2], gate oxide/gate electrode material combination, crystallinity of gate electrode, surface roughness of gate electrode/gate oxide interfaces etc. Existence of hydrogen related species in CVD technique, contamination from precursors in ALD process and plasma damage from PVD affect Hf-based gate oxides' reliability. So careful considerations of process parameters, choice of gate oxide and gate electrode materials are extremely necessary to obtain a reliable high-k gate oxide MOSFET device. Moreover, existence, quality and thickness of interfacial layer significantly affect bias instability and reliability of Hf-based gate oxides [3]. Intrinsic factors such as soft phonon [4], pre-existing traps, existence of di-poles between high-k gate oxides and gate electrode are critical parameters that affect oxide reliability. Charge trapping under electrical stress causes instability and affects reliability of gate oxides [5-9]. It is generally recognized

that Hf-based gate oxides have significantly large amount of charge traps in comparison to SiO_2. Thus reliability evaluation and requirements adopted from SiO_2 would give erroneous results, which might lead to inaccurate conclusion. Understanding of all of the intrinsic and extrinsic factors in high-k gate oxides, and then investigation of proper technique to evaluate the reliability of high-k are burning issues in current scaled technology. In this work, reliability, charge trapping-detrapping study, and break-down model investigation of Hf-silicate and HfO_2 have been investigated systematically.

5.1 Compositionally Varying Bi-layer Structure of PVD $HfSi_xO_y$ Dielectric

In comparison to HfO_2, Hf-silicate shows superior properties in terms of better crystallization temperature, higher mobility, higher charge trapping immunity under stress, and so better reliability [7, 10-11]. Since the dielectric constant of Hf-silicate is comparatively higher than that of HfO_2, the benefit came from sacrificing EOT of the device. T. Yamaguchi et al [12] found that increase in Zr concentration in Zr-silicate films decreases the effective mobility and current drivability of the device due to the dominant effect of coulomb scattering of bulk charges. Therefore, it is reasonable to expect that an increase in Si composition (thus decrease in Hf composition) close to the bottom interface of Hf-silicate dielectric would improve effective mobility, because of superior chemical similarity Hf-silicate/Si interface to SiO_2/Si interface and decrease in coulomb scattering originating from the bulk oxide. On the other hand, decrease in Hf

composition would lower the overall dielectric constant of the gate stack, which would eventually increase the equivalent oxide thickness (EOT). To take advantage of both the low and high composition of Hf, in this work we have proposed a bi-layer structure comprising of low Hf composition at the bottom stack, and high composition at the upper stack and have shown that this structure dramatically reduces leakage current density (J_g) and C-V hysteresis, while it improves the gate oxide reliability.

5.1.1 Process Flow and Experiments

The MOSFET process flow started with cleaning of the active patterned wafers (p-type) in diluted HF solution. Afterwards, Hf and Si were deposited via DC magnetron co-sputtering (40 mTorr, Ar, room temperature). Film composition, measured by x-ray photoelectron spectroscopy (XPS), was varied by adjusting the Si target position up and down. Three compositions; (a) Film-A: 19.5% Hf (b) Film-B: 24% Hf and (c) Film-C: 28.5% Hf and a bi-layer structure comprising of Film-A at the bottom and Film-C at the top were fabricated. Film thickness was measured by ellipsometer. All the deposited films were annealed in a rapid thermal anneal (RTA) chamber at 600°C in N_2 ambient. TaN gate was deposited using DC sputtering (N_2+Ar, 10 mTorr, room temperature) for a thickness of ~2000Å. After gate patterning, reactive ion etching (RIE) in Cl_2/He mixture was used to pattern the TaN gate material. Sputtered aluminum was used for backside metallization. Finally 450°C in forming gas anneal was carried out for 20 minutes.

Electrical characterizations were performed using HP4194 impedance/gain-phase analyzer and HP4156A semiconductor parameter analyzer. EOT (effective oxide thickness) was extracted from accumulation capacitance measured at 1 MHz, after accounting for quantum mechanical effects.

5.1.2 Electrical Characterization and Reliability Measurements

Fig. 5.1(a) shows the C-V curves of the three compositions along with the Bi-layer structure, whereas fig. 5.1(b) shows J_g (leakage current density) vs. EOT plot. As expected, EOT decreased with the percentage increase of Hf (%Hf={[Hf]/([Hf]+[Si]+[O])}x100) in the dielectric.

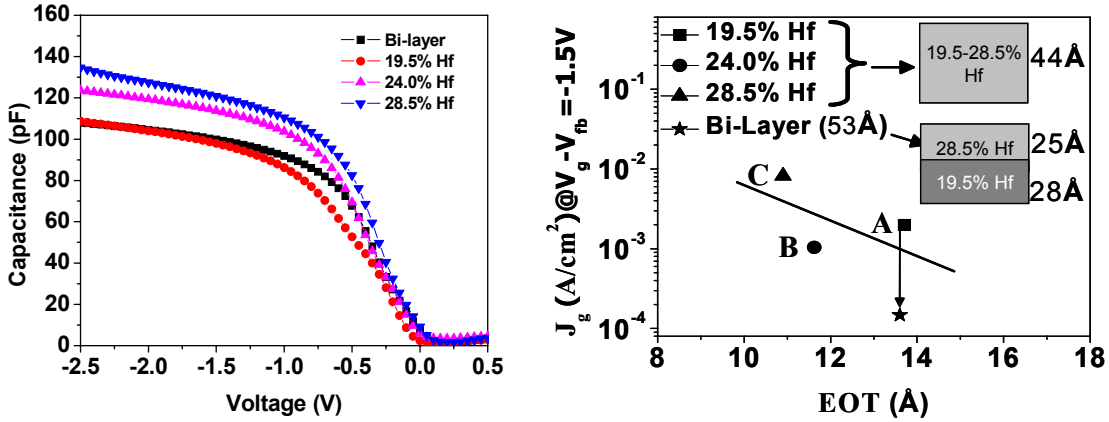

Fig. 5.1. (a) C-V curves and (b) J_g-EOT plots for Film-A (19.5% Hf), Film-B (24% Hf), Film-C (28.5% Hf) and Bi-layer structure with Film-A at the bottom and Film-C at the top. For the same EOT, leakage current of bi-layer structure could be dramatically reduced in comparison to Film-A as shown. Inset shows the schematic structure of the four films.

Irrespective of Hf composition, the J_g-EOT data lies almost in the same line as shown. This is consistent with our previous report, where J-EOT line lies almost in the same line irrespective of Si composition (fig. 2.7). At the same EOT, the bi-layer structure (see inset of fig. 5.1.b) showed an order of magnitude of lower leakage current as compared to Film-A. So by introducing the proposed bi-layer structure, we could obtain lower leakage (making the total thickness physically larger), while maintaining low EOT. The arrow line indicates the advantage of this structure over Film-A.

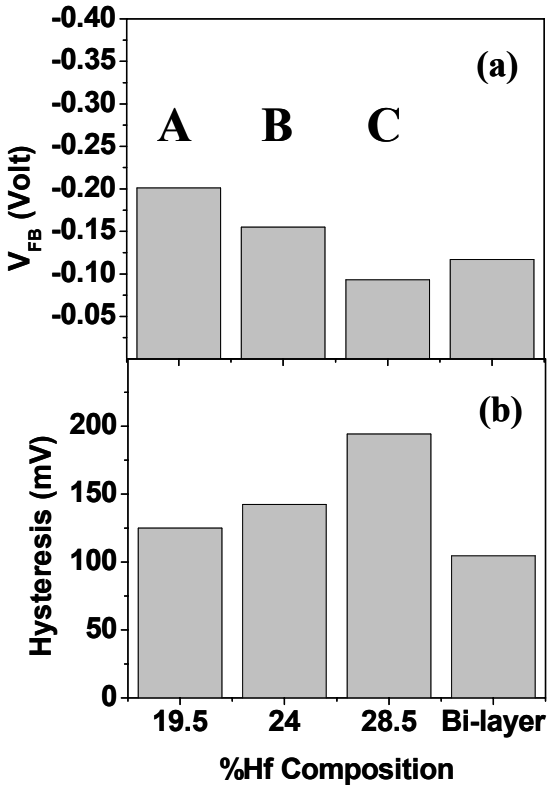

Fig. 5.2. Variation of (a) V_{fb} and (b) C-V Hysteresis for Film-A, -B, -C and bi-layer structure. Increase in %Hf composition increased negative fixed charges into the oxide. V_{fb} of bi-layer structure lied in between Film-A and –C. Hysteresis was also significantly reduced.

Fig. 5.2(a) shows the flat band voltage (V_{fb}) values as a function of %Hf in the dielectric. From the figure, it is clear that the increase in Hf concentration adds negative fixed charges into the dielectric, thus shifting V_{fb} in the positive direction. Similar phenomena has been reported for Zr-silicate and the additional coulomb scattering from the fixed charge was found to result in reduction of effective mobility for film with high %Zr [12]. It is interesting to note that Film-A and the bi-layer structure have almost the same EOT, while V_{fb} is different. The results indicate that putting Film-C on the top of Film-A introduces negative charge adjustment, thus resulting in an intermediate V_{fb} value. C-V (capacitance-voltage) hysteresis trend with %Hf composition is shown in fig. 5.2(b). Hysteresis is seen to increase with increase in %Hf composition, which is due to increase in bulk trapping and defect generation. The bi-layer structure was found to exhibit reduced C-V hysteresis compared to other three samples.

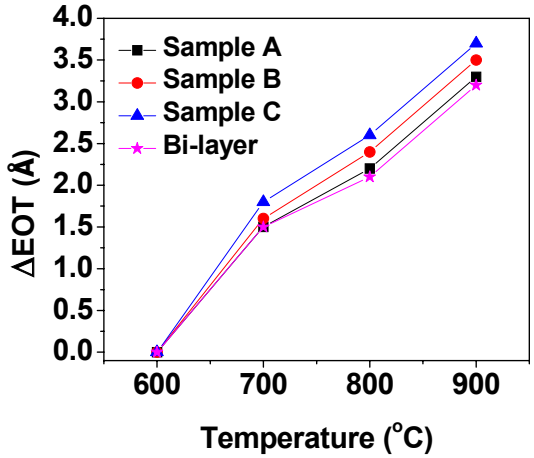

Fig. 5.3. Change in EOT (ΔEOT) with post-metal anneal temperature for Film-A, -B, -C and bi-layer structure.

It should be mentioned that thermal stability of bi-layer structure with post-metal anneal temperature could be retained smaller as compared other compositions as shown in fig. 5.3. Fig. 5.4 shows the SILC (stress induced leakage current) for the four different samples after the same stress voltage, V_{ox} (=V_g-V_{fb}). SILC is defined as difference in leakage current after stress from that of fresh current (J_o). The result shows that there was negligible SILC in the bi-layer structure due to negligible defect generation and bulk trapping under gate injection into the oxide. The charge trapping (ie. SILC and hysteresis) increases as %Hf increases. It should be pointed out that Film-A showed decrease in J_g initially followed by increase in leakage current with stress times. Thus the bulk charge trapping could significantly be reduced using bi-layer structure of Hf-silicate dielectric.

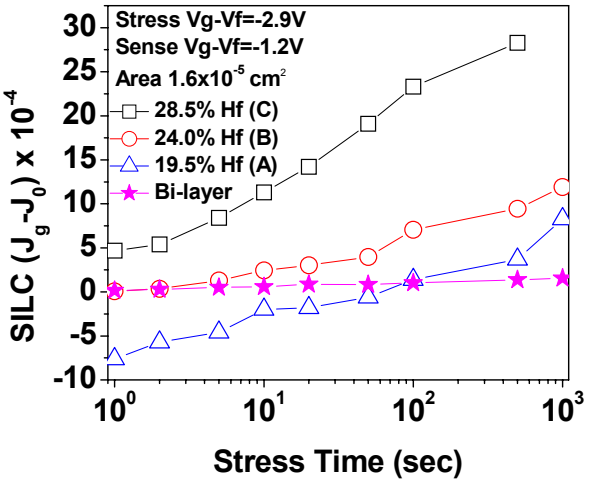

Fig. 5.4. SILC comparison for Film-A, -B, -C and bi-layer structure. Bulk trapping and defect generation could significantly be reduced by using bi-layer structure. Stress and sense voltage for SILC measurements were same for the four films

Fig. 5.5 shows the TZDB (time zero dielectric breakdown) of these four samples. Still Film-A shows better breakdown characteristics than the other two compositions, while bi-layer structure showed the highest breakdown voltage in comparison to all other devices. Therefore, reduction in bulk trapping by using bi-layer structure essentially improved the breakdown behavior, and thus reliability of the gate stack.

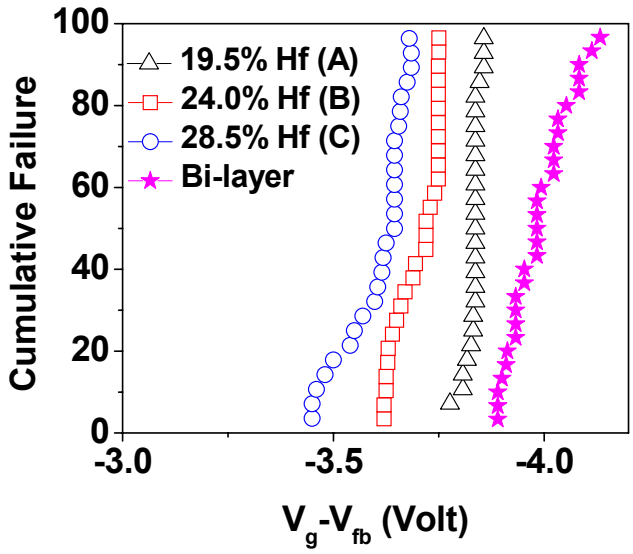

Fig. 5.5. TZDB (Time Zero Dielectric Breakdown) for Film-A, -B, -C and bi-layer structure. Bi-layer structure showed highest time zero breakdown characteristics in comparison to the other three structures.

5.2 TDDB Study of Si-Inserted HfO_xN_y with TaN Gate Electrode

TDDB (time dependent dielectric breakdown) study was carried out on nMOS capacitors being stressed at a constant voltage (CVS) in accumulation condition (gate injection). TDDB is a very important technique to determine the reliability of gate oxide. It is well known that high-k dielectrics are trap-rich material. Pre-existing traps, oxide defects, oxide impurities, surface roughness, oxide crystallinity, material quality, process conditions greatly influence high-k gate oxide reliability. Reliability becomes more critical for very thin oxides. Proper methodology to assess the accurate projection of gate oxide lifetime is also another challenge to be addressed. In this regard, percolation model was proposed to explain the thickness dependence of TDDB for SiO_2, which has been widely accepted [13-14]. In this concept, defects with a specific diameter, a_o are randomly generated inside the dielectric during TDDB stress. When these defects are accumulated and make an overlapping path between two electrodes, the path becomes conductive and the dielectric breaks down. The breakdown is a stochastic event and therefore has a distribution. The distribution due to the percolation model can be modeled with weibull distribution using the following equation;

$$F(x)=1-\exp[-(x/\alpha)^{\beta}]$$

where F is the cumulative failure probability, x is the time, α is the characteristic lifetime where 63.2% of samples fail, and β is the weibull slope parameter [14]. This β is a very important parameter in predicting lifetime distribution for gate oxides. According to the percolation model, the slope β is a function of the dielectric thickness.

For the SiO_2 based gate oxides, β becomes smaller as thickness decreases and approaches 1 as the thickness smaller than 30Å [14]. As β increases the distribution becomes tighter. A larger β is desirable from reliability point of view, since a fairly low failure rate is required for commercial devices.

Moreover, due to stochastic nature of the breakdown, TDDB has area dependence as well (ie. shorter TDDB for the larger capacitors), which can be expressed as follows,

$$\frac{\alpha'}{\alpha} = \left(\frac{A}{A'}\right)^{1/\beta}$$

where α and α' are the characteristic lifetime for the devices with different are A and A' respectively.

5.2.1 Soft and Hard Breakdown

As in SiO_2, high-k gate oxides also exhibit both soft and hard breakdown characteristics [15-16]. In general, soft breakdown is considered to result from a weak localized path between the gate electrode and the substrate. A critical number of electron traps generated in the gate dielectric layer and at the interface, which in turn form percolative clusters [13, 17-19]. The origin of soft breakdown in high-k could be quite different from SiO_2, since high-k is basically a bi-layer structure (an interfacial layer and a bulk high-k). For high-k dielectrics, soft breakdown has been predominantly observed as the first breakdown event. The sharp rise in gate current following soft breakdown is the hard breakdown as shown in fig. 5.6. Hard breakdown is the complete

breakdown of the gate oxide. In the case of SiO_2, the first breakdown could be either soft or hard breakdown, but both breakdown events have similar β values and thus a common origin in statistical characteristics [16]. However, the β values for high-k gate oxides for soft and hard breakdown events are quite different. It could be due to the difference in physical and chemical nature of interfacial layer and bulk high-k layer [3].

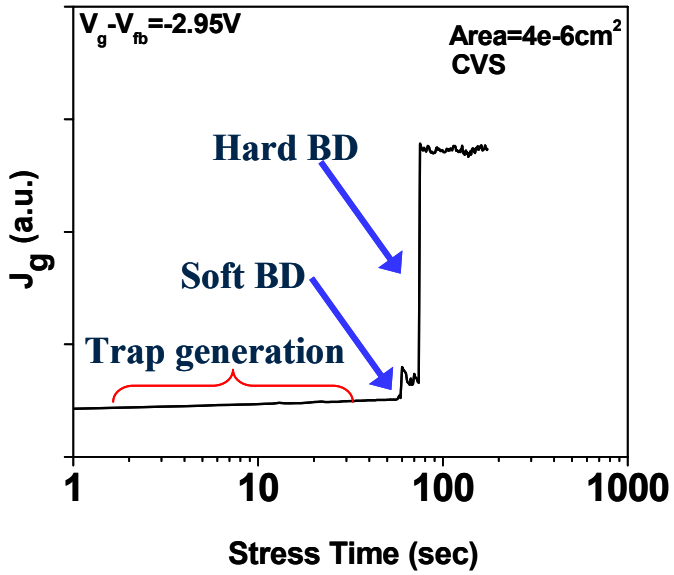

Fig. 5.6. Leakage current density with constant voltage stress time. Figure shows both soft and hard breakdown events in HfO_xN_y gate oxides including the trap generation phase with stress time.

5.2.2 Factors affecting β values in High-k Gate Oxides

Unlike SiO_2, β values for high-k gate oxides don't follow a common rule of thumb for all high-k materials. The defect generation rate, critical defect density to

breakdown, interfacial layer properties, nature of pre-existing traps all are different for different high-k materials. As the thickness increases, β values for HfO_2 also increases [3] as is seen for SiO_2. Kauerauf et al reported that based on the analysis of weibull slope for Al_2O_3 as a function of physical thickness, breakdown in high-k layer is dominated by an extrinsic mechanism [20]. A. Kerber et al. reported the thickness dependence of wear out properties of Al_2O_3 tend to support intrinsic breakdown mechanism [21]. ZrO_2, however, shows week thickness dependence [22]. Thus the thickness dependence of high-k dielectrics is not well understood. The polarity of stress also influences the charge trapping and defect generation in high-k gate oxides [21]. For substrate injection, it was proposed that the reliability is limited by electron trap generation in the bulk of Al_2O_3 rather than in the thin SiO_2 interfacial layer, thus strong thickness dependence of β values was observed, as expected from the percolation theory. For gate injection, on the other hand, it was also suggested that the breakdown of Al_2O_3 is determined by process induced defects causing weak spots in oxide [20]. It has also been reported that high voltage breakdown of thick Ta_2O_5/SiO_2 stack is completely determined by the interfacial SiO_2 layer due to high electric field at the interface. This causes Ta_2O_5 to breakdown immediately after interface degradation [23]. Thickness of interfacial layer and barrier height of the gate electrode material significantly influences β values of the HfO_2 materials [3]. The lower β values for HfO_2 in comparison to SiO_2 of same thickness might be explained by the factors such as defect density and defect size. In comparison to SiO_2, HfO_2 may have smaller defect density to breakdown and/or larger spacing between defects, where tunneling of a

trapped electron becomes probable. Moreover, the defects in high-k are more delocalized than SiO_2. Delocalized defects have larger sphere of influence. Thus there is no universal model which can explain all existing results for high-k reliability. In other words, high-k system may require considerations different from SiO_2, e.g. bimodal defect generations due to different physical nature of both interface layer and bulk layer, voltage drop as a function of interface layers, different charge fluences by different polarities, and critical defect density for breakdown which varies with thickness.

5.2.3. Process Details of Si-Inserted HfO_xN_y

The MOSFET process flow started with cleaning of the active patterned wafers (p-type) in diluted HF solution. Afterwards, HfO_2 was deposited via DC magnetron sputtering (30 mTorr, Ar, room temperature). All the deposited films were annealed in a rapid thermal anneal (RTA) chamber at 600°C in N_2 ambient. For HfO_xN_y, flow of N_2 was used during sputtering. For some samples, a thin Si layers (~6Å) was inserted according to the following schematic diagram shown in fig. 5.7.

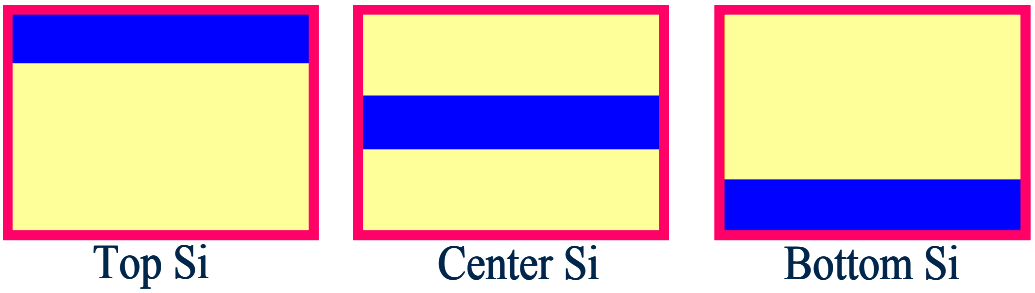

Fig. 5.7. Schematic Diagram showing Si-inseted HfO_xN_y dielectrics.

TaN gate was deposited using DC sputtering (N_2+Ar, 10 mTorr, room temperature) for a thickness of ~2000Å. After gate patterning, reactive ion etching (RIE) in Cl_2/He mixture was used to pattern the TaN gate material. Sputtered aluminum was used for backside metallization. Finally 450°C in forming gas anneal was carried out for 20 minutes. Fig. 5.8 shows the C-V profile of three structures of Si-insertion into the gate oxide. Top-Si insertion shows the lowest EOT, probably because of higher amount of nitrogen incorporation into the film as compared to the other two structures [24].

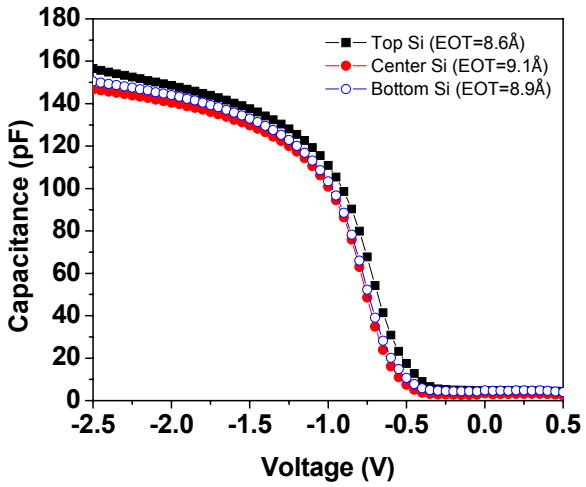

Fig. 5.8. C-V curves for the three structures. The Top Si-insertion show lowest EOT, because of higher percentage of nitrogen capture into the film.

5.2.4 TDDB Analysis

In this work, breakdown data only after hard breakdown have been taken for failure probability analysis. Before stressing, devices were screened by C-V and I-V measurements. Only devices with identical C-V and I-V were taken for stressing. For each set of data, almost 25-30 devices were stressed for statistical analysis purpose. Devices were stressed at constant voltage stress in accumulation until the devices break. For fair comparison, all the devices were stressed at the same V_g-V_{fb}. HP 4156A was used for stressing the gate terminals while all the other terminals of MOSFETs were kept grounded. Fig. 5.9 shows the weibull distribution of three dielectric structure stressed at different stress voltages. The slope of each distribution corresponds to β. The area was chosen to be $4x10^{-6}cm^2$. Fig. 5.10 shows the average β_{av} for the three stacks.

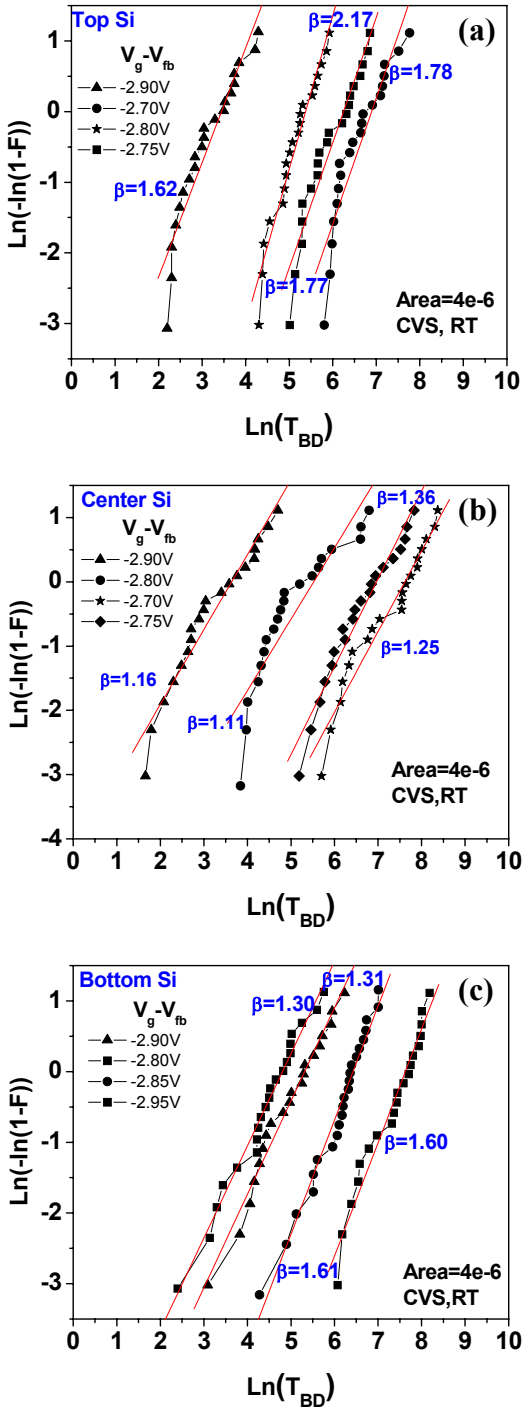

Fig. 5.9. Weibull distribution of (a) Top, (b) Center, and (c) Bottom Si-inserted HfO_xN_y dielectrics for various stress voltages.

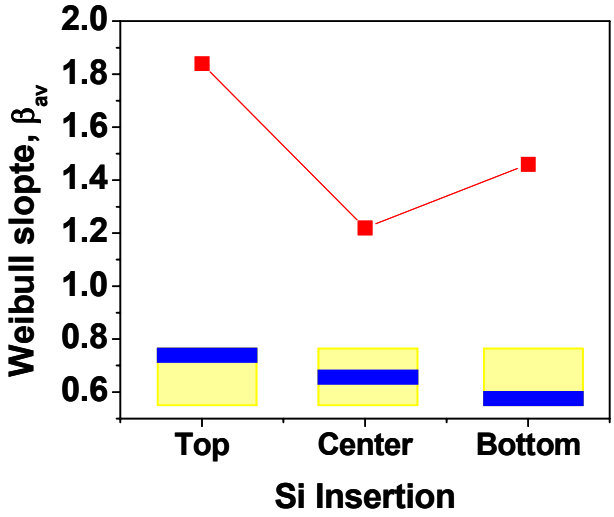

Fig. 5.10. Average β_{av} for the three stacks (Top Si, Center Si, and Bottom Si-insertion)

The results show that the β for top Si insertion has the highest value as compared to the other two structures. It should be mentioned that nitrogen capture by Si insertion was the highest for Top-Si structure. Thus it could be possible that Si insertion further away from the bottom interface is advantageous to reduce the defects and trapping sites in the oxide.

Fig. 5.11 shows the C-V hysteresis for the three structures. As shown, hysteresis was the smallest for the top Si-insertion. The similar results could be obtained from SILC study as shown in fig. 5.12. The SILC is defined here as $(J_g-J_o)/J_o$, where J_o is the fresh current density, and J_g is the current after stressing. For fair comparison, all the devices were stressed at the same (V_g-V_f). The stress and sense voltages were kept the same.

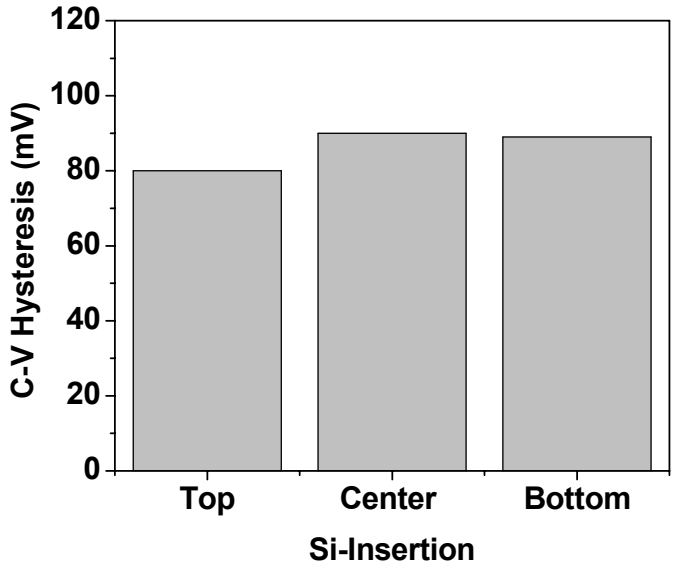

Fig. 5.11. C-V hysteresis for top, center, and bottom Si-insertion. Hysteresis was found to be lowest for top Si-insertion structure.

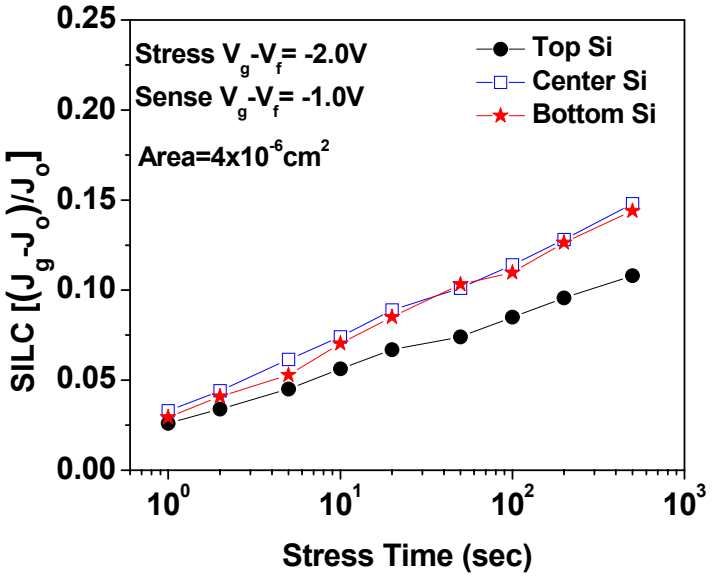

Fig. 5.12. SILC for top, center, and bottom Si-insertion. SILC was found to be lowest for top Si-insertion structure

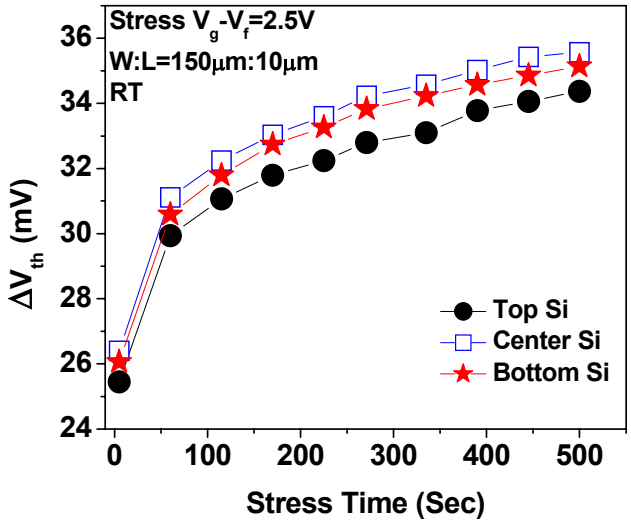

Fig. 5.13. Shifts in V_{th} for top, center, and bottom Si-insertion under constant voltage stress at the same (V_g-V_f). Top Si structure showed the lowest shift in V_{th}.

Fig. 5.13 shows the shifts in V_{th} for three structures stressed at constant voltage stress. As expected Top Si-insertion shows the lowest shifts indicating that stress induced bulk trapping is reduced by trapping the nitrogen further away from the bottom interface. The observations above could further be confirmed by charge pumping experiment [25]. The charge pumping current can be expressed by the following equation:

$$I_{CP} = 2q\overline{D_{it}}f \cdot A_G \cdot KT\left[\ln\left(v_{th}n_i\sqrt{\sigma_n\sigma_p}\right) + \ln\left(\frac{|V_{FB}-V_T|}{|V_{High}-V_{Low}|}\right) + \ln\left(\sqrt{t_f t_r}\right)\right](I)$$
$$+ qfA_G N_{BT}(V_G, f)(II) + \alpha f A_G C_{OX}(V_G - V_T)(III) + I_T\,(IV)$$

I. Interface Traps

II. Bulk Traps

III. Geometric Effect

IV. Leakage Current

Thus as the frequency is decreased, bulk traps play roles in charge pumping current. Moreover, to eliminate or reduce the geometric effect, the size of the transistor should not be too small or too large. If the device is leaky, then the leakage current would give erroneous results. In this experiment, we used 4.0-4.5nm thick device. Thus the effect of leakage current in I_{cp} is expected to be negligible. Now if we divide the equation by area, A and frequency, f, then we get pumped charge, Q_{cp} per unit area per cycle, expressed as $Q_{cp}=(I_{cp}/A*f)$. Fig. 5.14 shows the variation of Q_{cp} with frequency of charge pumping in a high-k device.

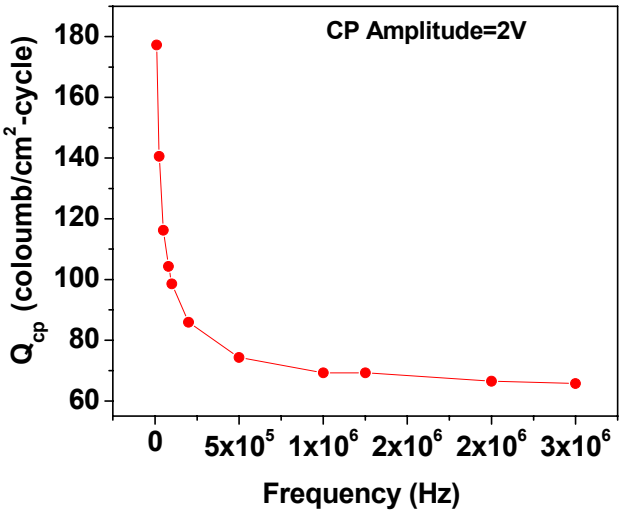

Fig. 5.14. Variation of Q_{cp} with CP frequency for a high-k device

As shown, Q_{cp} is high at low frequencies starting at 10KHz. As the frequency increases, the contribution from the bulk decreases. So CP technique measured at higher frequencies probes more into the interface between high-k and Si-substrate. But still this technique takes the bulk effect into consideration. Q_{cp} measurement by varying the rise time and fall time (t_r and t_f) gives more accurate results in estimating the interface traps. If we can vary the t_r and t_f, then we can eliminate the effect of 2nd, 3rd and 4th term in the above equation. Thus by varying t_r and t_f, and taking the slope of I_{cp} vs $\ln(t_r * t_f)^{0.5}$ plot, we can get the Q_{cp} resulting from the interface only as shown in fig. 5.15. In this way, we can separate the contribution of bulk traps and interface traps in charge pumping current.

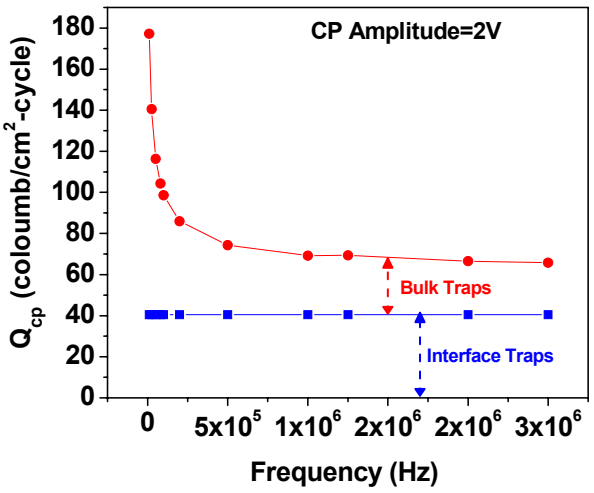

Fig. 5.15. Separation of bulk and interface Q_{cp} by meaureing I_{cp} varying CP frequency and varying rise-fall times.

If we integrate the area under the line, then we can get pumped charge per unit area in this frequency spectrum varying from 10KHz to 2.5MHz. Thus the area above the

interface line is the bulk traps, while area below is the interface traps. Using the same technique in determining the bulk traps in the oxide, it was found that Top Si-insertion still showed the lowest bulk traps compared to the other two structures as shown in fig. 5.16, while there was no significant different in interface traps as shown in fig. 5.17.

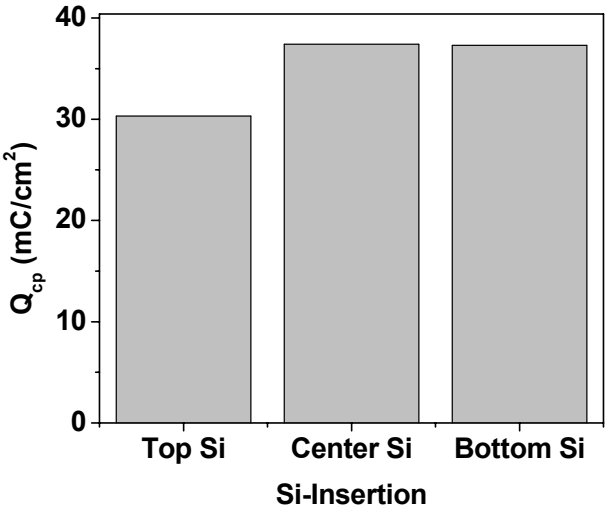

Fig. 5.16. Variation of Bulk-Q_{cp} with Si-insertion into the HfO_xN_y gate oxide. Top Si-insertion showed the lowest bulk trapping characteristics.

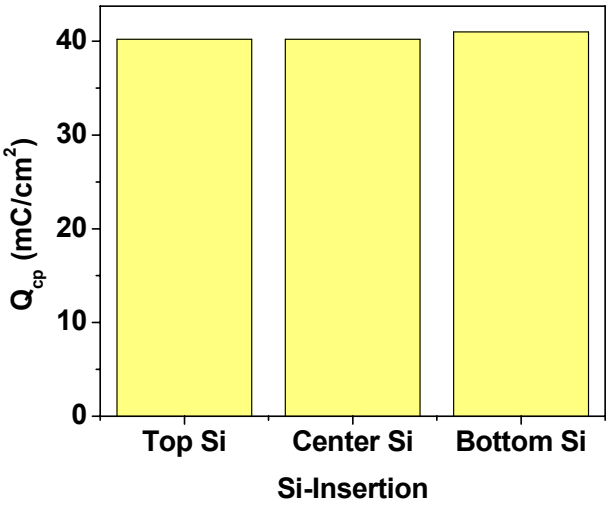

Fig. 5.16. Variation of Interface-Q_{cp} with Si-insertion.

There is little increase in interface Q_{cp} for the bottom Si-insertion structure, probably because of nitrogen pile up at the interface. Thus this technique confirms the fact that the improvement in β value for Top Si-insertion was due to reduction of bulk trapping in the high-k gate oxide. The results also demonstrate that nitrogen profiling using Si-insertion into the HfO_xN_y gate dielectric is an effective way to control the reliability of the device. Pushing the nitrogen location further away from the interface not only helps to reduce the EOT, but also improves the reliability of the oxide. It should be noted that under the unipolar stress condition, the values of β_{av} (i.e. β_{ac}) is smaller than those of β_{dc} for all of the Si-insertion structures as shown in fig. 5.17.

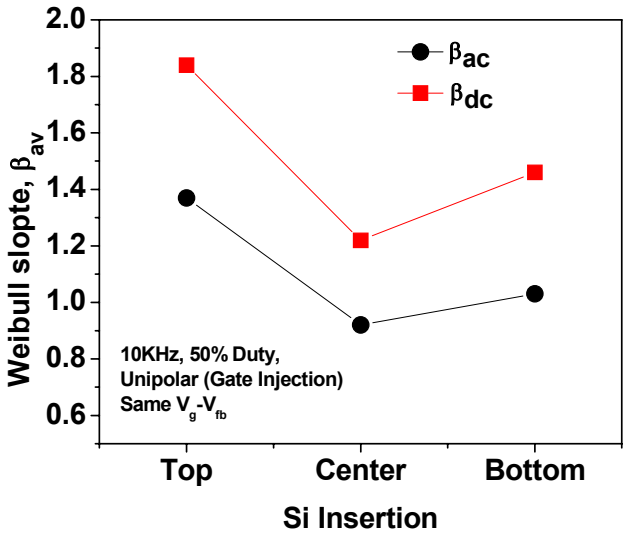

Fig. 5.17. Comparsion of β values for the three Si-insertion structures under static and dynamic (unipolar) stress conditions.

It is not clear why the β_{ac}'s are lower than β_{dc}'s. The rise time and fall time used for TDDB study under unipolar stress conditions were 5ns. Possibly fast rise and fall time

incurred additional displacement current effect due to high dV/dt overshoot effect during these rise and fall times. More study need to be done to understand these effects clearly.

5.3. A Novel Approach in Understanding the Breakdown Mechanism in HfO_2 Gate Dielectrics under Substrate Injection Condition

As discussed previously, the well accepted breakdown model for SiO_2 based gate oxide was percolation mode [13-14]. Several other models, for example, hole trapping model [26], modified hole trapping model [27], interface softening model [28] have been proposed to understand the underlying physics behind breakdown mechanisms in SiO_2 based oxides. But high-k dielectrics are known to be trap rich materials. Pre-existing traps, defects density, crystallization effect with temperature, grain size, dipole effects, all of them make the high-k dielectrics hard to come up with a unique breakdown model. On the other hand, the transient relaxation effects, which have been addressed as undesirable issues in high-k dielectrics, make the understanding further complicated [29-31]. Thus to achieve a unified model, careful attention need to be paid to consider all of the effects in breakdown. Recently, breakdown (BD) model involving grain boundary and field-assisted wear-out in high-k dielectrics has been proposed [32]. However, the role of electron and hole trapping in dielectric BD has not been addressed in detail. To systematically study the fundamental BD mechanism HfO_2 dielectrics, this work separates the role of electrons' transient charging and hole trapping by interrupting

the electrical stress and applying high temperature annealing for detrapping purpose. It has been reported that hole accumulation in the bulk of the Hf-based dielectrics is primarily responsible for dielectric breakdown under substrate injection, although both holes and electrons are trapped in the dielectrics. A model has been given supporting the experimental observations.

TiN/ALD HfO_2 (EOT of 1.2nm) and TaN/PVD HfO_2 (EOT of 1.4nm) nMOS devices were chosen for this study. Electrical stress under substrate injection was applied using HP 4156C. The single-pulse I_d-V_g measurements were done by Keithley Model 4200-SCS and a pulse generator. Post-stress furnace anneal was done in 20min.

5.3.1 Stress-Anneal Experiments

Three sets of ALD HfO_2 devices underwent a constant voltage stress (CVS) of 2.2V for 500s. Then set-1 and set-2 were annealed in forming gas (FG) and N_2 at 500^{o}C respectively, while set-3 was untouched for 90 hours. The same sets were stressed again while monitoring V_{th}. The stress-anneal cycle was repeated several times (fig. 5.18.a). The V_{th} shifts in each phase of stresses were almost identical, except that the initial V_{th}'s (post-anneal V_{th}) after each anneal was seen lower than the preceding one, irrespective of anneal ambient of FG or N_2 (fig.5.18.a-b, fig. 5.19). After 90 hours of no-anneal (set-3), device relaxed slightly, but V_{th} quickly jumped up after few stress intervals. Even leaving the devices untouched for another 190 hours followed by stress showed the same phenomena (fig. 5.18.c). To avoid any parametric effect due to anneal, ALD HfO_2 went through the same set of experiments except that the anneal was carried out at 400^{o}C (fig.

5.18.d). It showed the same decreasing trend of post-anneal V_{th}, irrespective of the anneal ambient (FG/N_2).

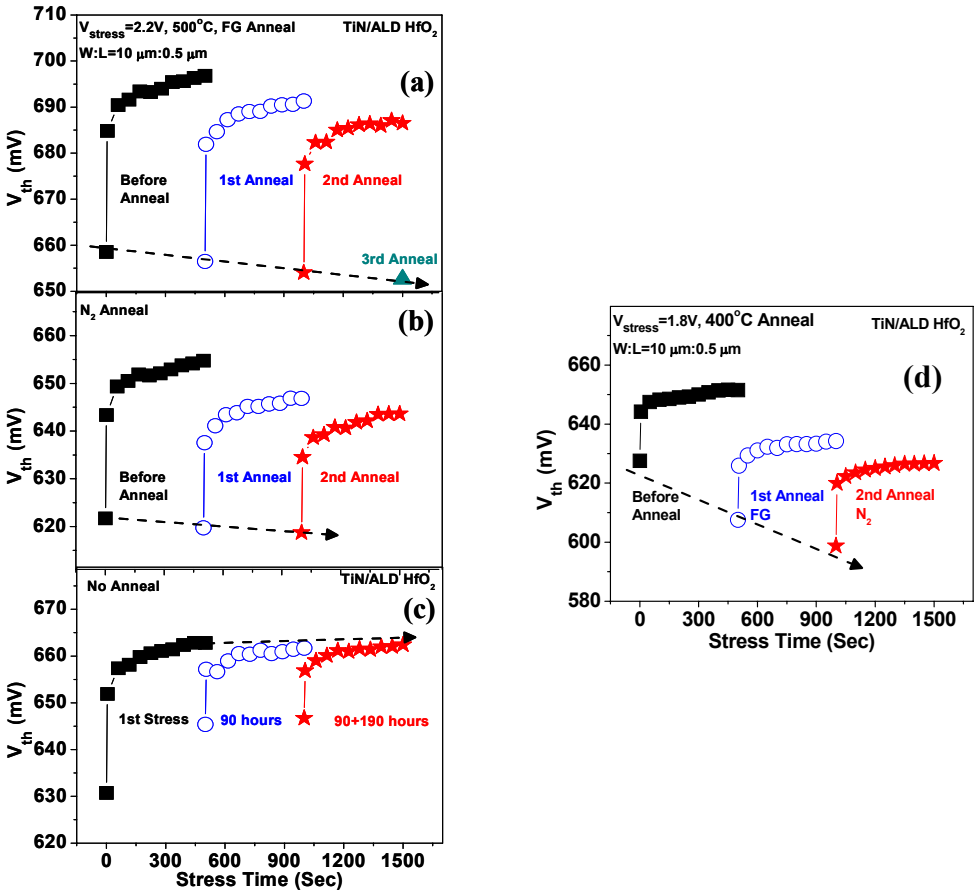

Fig. 5.18. V_{th} shifts in ALD TiN/HfO_2 vs. time with time-span of 500s. After each 500s, 500°C anneal was applied with (a) FG, (b) N_2 and (c) no anneal, (d) V_{th} shifts in ALD TiN/HfO_2 with post stress anneal at 400°C

5.3.2. Underlying Schematic Model

The schematic energy band diagram model could explain the above observations (fig. 5.20).

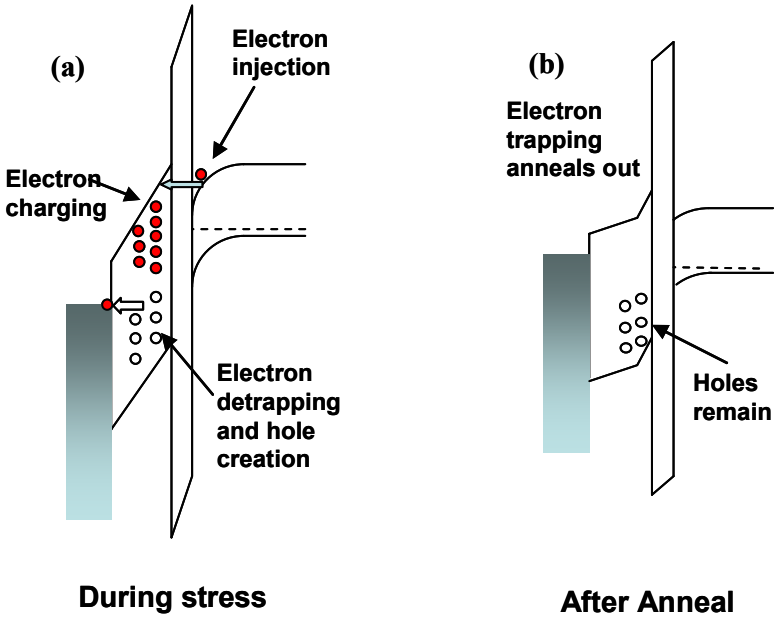

Fig. 5.20. Schematic energy band diagram (a) during substrate injection and (b) after high-temperature anneal. According to the model, breakdown of HfO_2 is triggered by conduction path caused by hole accumulation, not by electron charging.

Under substrate injection, electrons are injected from the substrate into the HfO_2 dielectrics, trapped and distributed in a region of shallow potential and closed to the interface between high-k/interfacial layer (IL). This electron charging causes V_{th} shifts in the positive direction. At the same time, some electrons (smaller in number than that

injected) at a deep potential could be detrapped leaving holes behind (fig. 5.20.a). After annealing, electron trappings are annealed out leaving holes. This resulted in the downward shift of initial V_{th} after anneal (fig. 5.20.b). Successive stresses cause an accumulation of holes, which couldn't be annealed out, pulling the initial V_{th} further downward.

5.3.3 Supporting Experimental Data

To confirm this observation, devices were stressed at different stress times and annealed at 500°C (fig. 5.21).

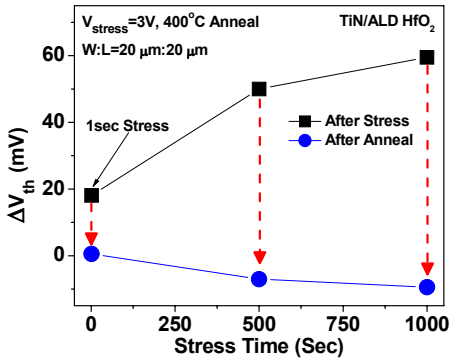

Fig. 5.21. V_{th} shifts at different stress times and corresponding post-anneal V_{th} reductions (shown dotted arrow) after 500°C FG anneals.

The corresponding post-anneal V_{th} is illustrated by the dotted lines. Interestingly, the longer stress time led to higher hole accumulation and larger post-anneal V_{th} reduction. Fig. 5.22 shows gradual and slight degradation of transconductance and subthreshold

slope as a function of time, indicating that holes are not accumulated at the Si interface and the interface characteristics aren't degraded much. A single-pulse I_d-V_g measurement was performed (fig. 5.23).

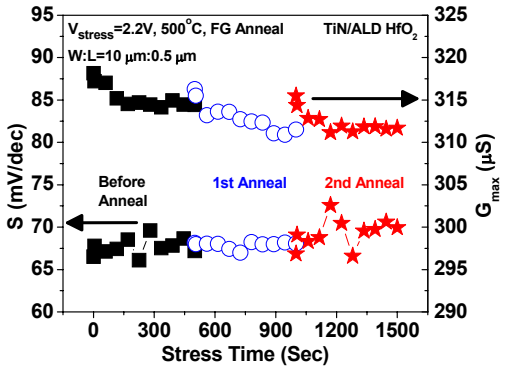

Fig. 5.22. Small decrease in G_{max} and small increase in sub-threshold swing (S) observed with stress times. The gradual trend was observed.

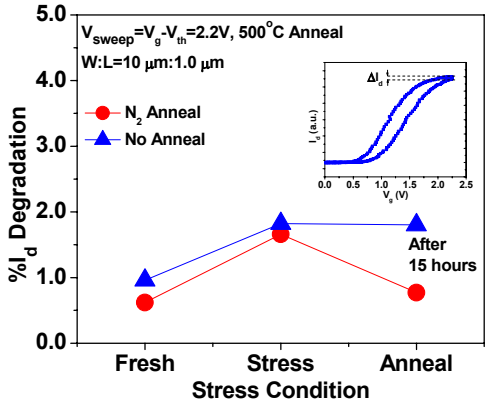

Fig.5.23. Reduction of bulk trapping after anneal of stressed devices. Significant reduction of bulk trapping indicates that electron trapping anneals out by temperature treatment. Inset shows up and down sweep in single pulse I_d-V_g.

I_d degradation (ΔI_d), which is primarily governed by bulk charge trapping, occurs during the pulse width time. Significant reduction in I_d degradation after N_2 anneal indicates that temperature treatment anneals out injected electron trapping. To further support our argument, leakage current of fresh sample and post-stress annealed sample has been compared (fig. 5.24). Existence of holes should reduce energy band diagram (as shown in fig. 5.20.b) at the hole locations, and should enhance leakage current of the post-stress annealed sample under substrate injection (fig. 5.24).

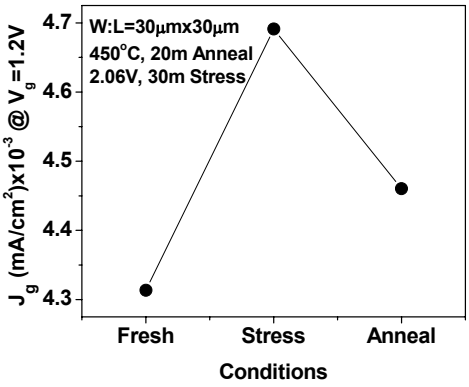

Fig. 5.24. J_g of the sample increased after annealing in comparison to fresh states, due to change in band diagram as shown if fig 5.20(b).

To investigate the hole accumulation BD (breakdown), two sets of NMOS capacitors with guard rings (to supply enough electron in inversion) were chosen. Set-1 went through CVS at 3.5V until the devices breakdown and the corresponding injected charges were monitored (Fig. 5.25.a-"$^1Q_{BD}$ without anneal" curve). Set-2 was stressed at the same 3.5V close to breakdown (fig. 5.25.a-"$^2Q_{inj}$ before anneal" curve) followed by

400°C N_2 anneal. This heat treatment annealed out the trapped electrons leaving holes behind. After annealing, set-2 was again stressed at 3.5V until the devices break. The summation of injected charges in two phases (before and after anneal) are plotted (fig. 5.25.a-"$^2Q_{BD}$ with intermediate anneal" curve).

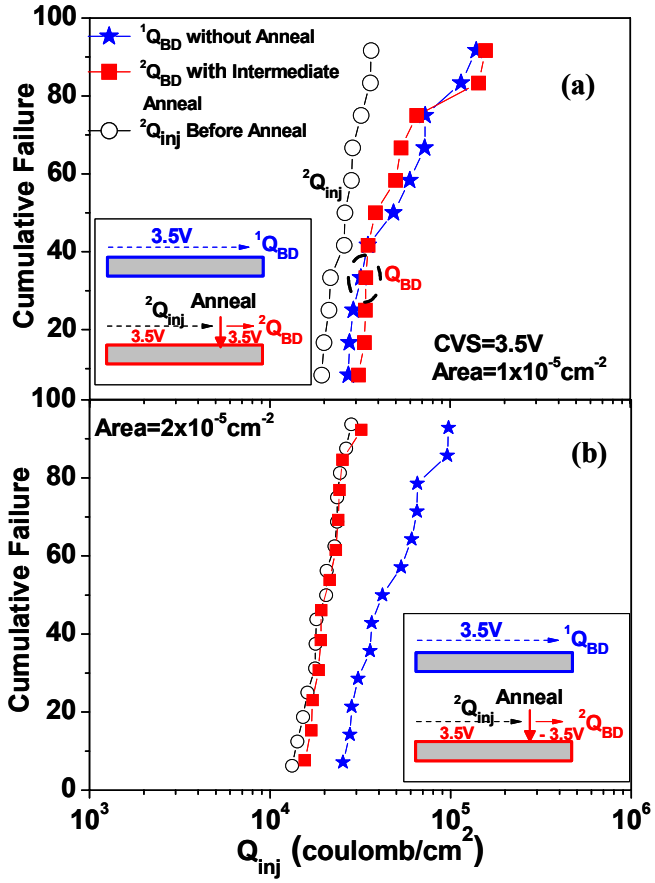

Fig. 5.25. Breakdown distribution (BD) of two sets of devices. Set-1 went through direct breakdown under CVS. Set-2 was stressed at 3.5V, close to breakdown and went through 400°C anneal. (a) BD of set-2 at 3.5V after anneal (b) BD of set-2 at -3.5V after anneal. Upper script in figures indicates set number.

As one can see, the BD distribution was almost the same as that of set-1. The results suggest that the rest of the amount of hole density to BD was generated by after-anneal additional substrate charge injection at 3.5V. If one changes the polarity to -3.5V (gate injection) after the intermediate anneal, BD occurs almost immediately (fig. 5.25.b). Under the gate injection polarity, major portion of injected carriers are holes (which causes V_{th} shift negatively) causing early breakdown (fig. 5.25.b). This further supports that it is the hole traps build-up that causes dielectric breakdown in high-k dielectrics.

5.4 Summary

In this chapter reliability of $HfSi_xO_y$, HfO_2 and HfO_xN_y has been discussed in terms of process issues, nitrogen effect and understanding the breakdown mechanism.

For compositionally varying $HfSi_xO_y$ bi-layer structure, the increase in Hf composition in Hf-silicate gate stack increases bulk trapping characteristics, which results in an increase in C-V hysteresis, mobility degradation, and oxide breakdown voltage reduction. On the other hand, the reduction of Hf composition essentially decreases the dielectric constant, thus resulting in an increase in EOT. Introduction of bi-layer structure with low percentage of Hf at the bottom stack, and high percentage of Hf at the top can effectively merge the positive attributes of the two compositions, thus enhancing overall electrical performance and oxide reliability.

For HfO_xN_y with Si-insertion structure, it was found that trapping of nitrogen atoms by incorporating Si into the dielectric further away from the interface helps to enhance the reliability of dielectrics. The weibull distributions get tighter with Top Si-insertion in comparison to Center and Bottom Si-insertion. Reduction of bulk trapping, and defect density in the bulk of the oxide have been attributed to the improvement. In comparison to dc stressing, β values for ac stressing were found to be smaller, possibly due to dV/dt transient effect in the oxide.

Furthermore, a model for understanding the breakdown mechanism in HfO_2 gate oxide has been proposed based on stress-anneal experiments to separate the effect of electrons and holes into the oxide. The model successfully confirms that hole accumulation in the HfO_2 is the primary reason of dielectric breakdown (BD) under

substrate injection. No significant interface degradation was observed. Thus the bulk of the HfO_2 plays a major role in degradation of high-k gate oxide devices. The better understanding of BD mechanism provides additional insights into high-k dielectric process optimization. The role of interface thickness still remains a question to be investigated its effect in breakdown of HfO_2. So further study might be needed to clarify the accurate breakdown mechanism.

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Vita

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