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Circuits and Architectures for Broadband Spectrum Channelizers with Sub-band Gain Control

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Circuits and Architectures for Broadband Spectrum Channelizers with Sub-band Gain Control

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To my beloved my wife and my daughters

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Circuits and Architectures for Broadband Spectrum Channelizers with Sub-band Gain Control

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Broadband receiver architectures for full-band or concurrent multi-band reception of signals are required in several applications. One approach to implementing such receivers is a spectrum channelizer that employs a frequency-folded analog-to-digital converter (FF-ADC). The design downconverts and channelizes a broadband input signal into multiple sub-bands at baseband by employing the harmonics of non-overlapping rectangular clocks. The downconverted and aliased baseband signal in each path is digitized by a baseband ADC, referred to as a sub-ADC below, that operates with a sampling rate that is lower than the Nyquist sampling rate set by the full bandwidth of the input signal. Sub-band separation is performed through digital harmonic rejection (HR) and image rejection (IR). The design operates similar to a time-interleaved ADC, except that it significantly reduces the bandwidth requirement of the samplers.

If rectangular pulse waveforms are used in the FF-ADC down-converter, all sub-bands experience nearly equal gain during frequency down-conversion. Since

all sub-bands are aliased to baseband before they are separated in the digital domain, a sub-band with large relative power can reduce the sub-ADC dynamic range that is available for other sub-bands, in addition to appearing as a blocker for other sub-bands. The research presented in this dissertation addresses approaches to overcome this issue, by embedding sub-band gain control within an FF-ADC.

Chapter 2 proposes an approach that employs pulse-width-modulated local oscillator (PWM-LO) waveforms in the polyphase paths of an FF-ADC for scaling individual sub-band signal levels at baseband before digitization. The PWM-LO waveforms, which directly drive switches in each path, can be used to vary the gain in each sub-band by varying the level of harmonics in the waveforms. This is achieved by controlling the pulse-widths of the PWM-LO waveforms. This design avoids the requirement for $N \times N$ switch matrices and variable transconductance cells in prior demonstrated approaches. The proposed architecture makes it possible to vary the spectral response of the FF-ADC with low signal-path complexity. Prediction of pulse widths for the desired harmonic, and hence the gain profile across all sub-bands, is performed using an off-chip supervised learning approach employing a neural network.

Chapter 3 presents the implementation of a spectrum channelizer employing the PWM-LO-based sub-band amplitude control. The design allows for scaling the relative gain of the sub-bands over a 20-dB range. This relaxes the compression performance of the channelizer baseband and the sub-ADC dynamic range in the presence of sub-bands with significantly higher signal levels. Gain control on individual sub-bands is performed by employing customized PWM-LO waveforms,

where the PWM-LO pulses are generated using delay-locked loops (DLLs). The off-chip neural-network based learning technique for estimating the PWM symbol pulse widths required for setting the desired LO harmonic levels is described. A 1.6 GS/s spectrum channelizer IC is implemented in a 65-nm CMOS process to verify the architecture. The measured channelizer gain is 51.6-56.5 dB without gain-scaling and provides a range of 37-59 dB with PWM-LO gain control. Gain-scaling at a specific harmonic improves blocker compression in an unattenuated sub-band from -34 dBm to -16 dBm. The in-band gain compression with gain-scaling also increases from -32 dBm to -17 dBm.

Chapter 4 describes a spectrum channelizer that uses voltage-mode downconversion. The approach requires a single voltage-mode input amplifier to drive the downconversion switches. Frequency-folding and sub-band gain control are achieved in a single signal path. This contrasts with the current-mode approach that requires a main FF-ADC path and a separate auxiliary path for sub-band gain control. By avoiding the requirement for an auxiliary input path, the approach presented here significantly simplifies the signal chain with identical gain-scaling capability.

The contributions of this research and scope for future related work are summarized in Chapter 5.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Overview

Several communication applications in recent years are experiencing a continuing demand for higher data rates. This is often being addressed through the use of new frequency bands, as shown in Fig. 1.1. Some of these applications may need to be integrated on to a single platform such as a computer or a mobile phone. Such implementations require receiver architectures that support multiple standards across a wide frequency range. For example, a single smartphone may be required to support several wireless standards that use different frequency bands, such as WCDMA, LTE, WIFI, Bluetooth, and GPS.

Separate ICs can be employed for receiving different frequency bands. However, this typically implies a large area and can lead to high cost. In order to implement a receiver on a single chip for multiple communication standards, a software-defined radio (SDR) architecture [1] that digitizes the broadband input bandwidth without frequency downconversion is an attractive approach to provide flexibility for the reception of multiple frequency bands. Signal analysis and demodulation are performed in the digital domain in an SDR.

In order to implement an SDR, direct sampling (DS) architectures that dig-

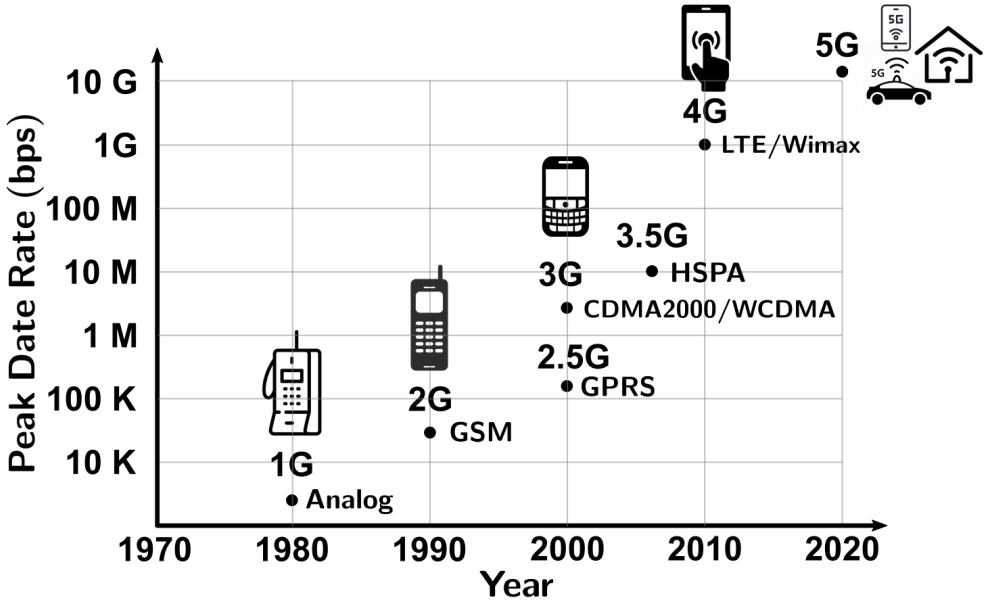


Figure 1.1: Evolution of mobile communication technology

itize the RF input bandwidth with a high-speed analog-to-digital converter (ADC) have been proposed [2, 3, 4, 5]. For high-speed sampling rates with good power efficiency, time-interleaved (TI) ADCs are often employed [6, 7, 8, 9]. TI-ADCs are implemented using multiple sub-ADCs that operate at a lower sampling rates.

In an environment with a large variation in the power level of various signals, the linear range of a TI-ADC gets limited by the largest signal incident on the receiver. This is the case because the receiver does not have frequency discrimination prior to digitization.

A frequency-folded ADC (FF-ADC)-based receiver with multiple sub-ADCs was introduced in [10]. The receiver downconverts and aliases a broadband input signal to baseband in multiple signal paths using N non-overlapping rectan-

gular clocks. Similar to TI-ADCs, a signal with a large power level can limit the linearity of the sub-ADCs.

A mixer-based channelizer can be employed to overcome the above limitation. A mixer-bank decomposes the broadband input spectrum into N contiguous sub-bands, which are bandlimited, and then digitized using N sub-ADCs [11]. Since channel separation is performed in the analog domain, the channels can be isolated such that channels with large signal levels do not limit the linear range in all receiver paths. This is done through the use of analog anti-aliasing filters at the ADC inputs in this type of channelizer. As described below, this type of receiver faces a significant limitation from the requirement for the synthesis of multiple LOs.

This research presents circuits and architectures for broadband channelizers with sub-band gain control, in the context of an FF-ADC. A spectrum channelizer that allows for scaling the relative gain of the sub-bands by using PWM-LO pulses is proposed, which relaxes the compression performance of the channelizer baseband and sub-ADC dynamic range in the presence of sub-bands with a significant signal. Off-chip learning employing a neural network can estimate the pulse widths of the PWM symbols that are required for setting the desired LO harmonics levels.

This chapter introduces broadband receiver architectures including direct sampling receivers, mixer-based channelizers and frequency-folded ADC-based receivers. Approaches for rejecting or selecting harmonic levels are also introduced.

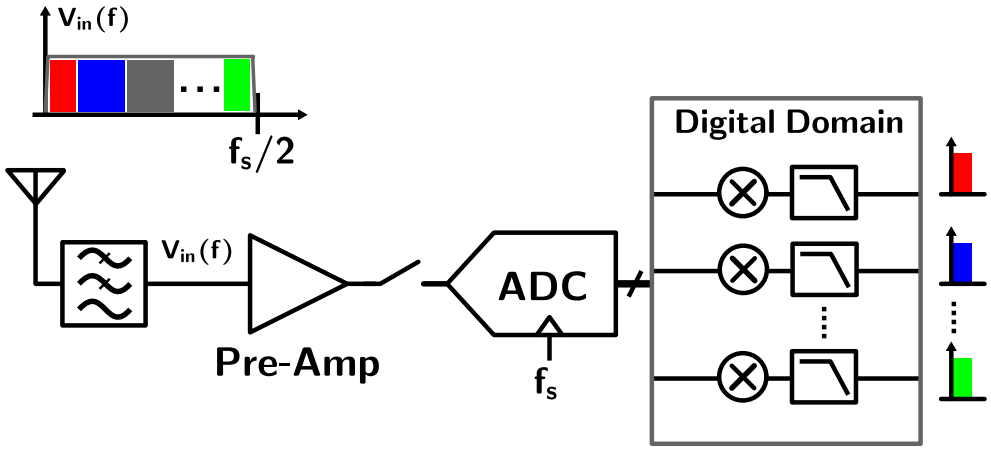


Figure 1.2: Block diagram of a direct sampling receiver

1.2 Broadband receiver architectures

Several architectures for the implementation of receivers that capture the full input spectrum have been previously introduced. The following section describes these broadband receiver architectures.

1.2.1 Direct sampling receiver

As the demand for increased data rates and more spectrum in communication standards has steadily grown, direct-sampling (DS) receivers that enable full-spectrum capture have become more attractive. Fig. 1.2 shows a simplified block diagram of a direct sampling receiver. The incident input signal is bandlimited to include the desired frequency bands by using a passive filter before a pre-amplifier. An ADC with sufficiently broad Nyquist bandwidth then digitizes the full input spectrum. A direct-sampling receiver does not suffer from analog non-idealities such as analog-domain noise and linearity limitation after digitization. Further,

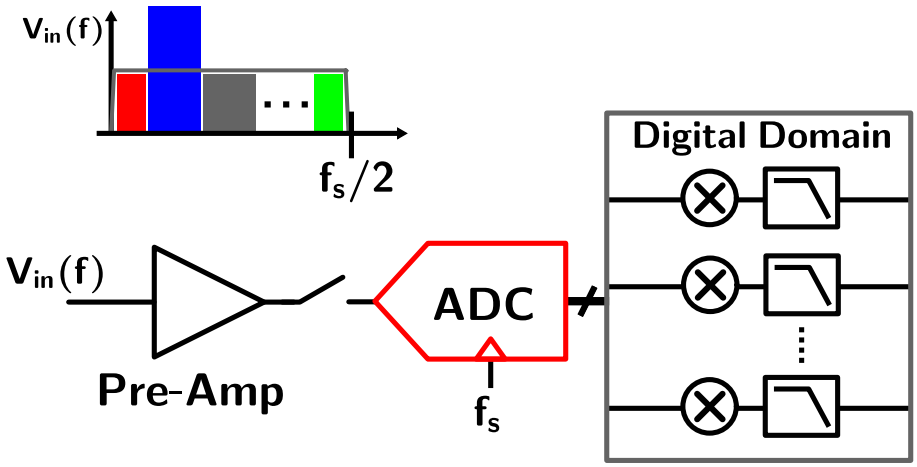


Figure 1.3: Degradation of ADC dynamic range for multiple sub-bands in the presence of a sub-band with a large signal

channel selection is performed in the digital domain, where highly precise filters can be implemented. A key advantage is that a fixed single-frequency PLL is employed for clocking the ADC instead of a tunable PLL.

A key challenge in a direct sampling receiver arises when the input spectrum has a considerable variation across all input sub-bands. For example, a specific sub-band with a significantly larger signal than others can degrade the ADC dynamic range for a small signal in other sub-bands (Fig. 1.3). The input stage of a direct sampling receiver must have a dynamic range that can be larger than the dynamic range of the input signal, which can be power-hungry.

1.2.2 Mixer-based channelizer

A second approach for implementing broadband receivers is based on a mixer-based channelizer. A simplified block diagram of the mixer-based channel-

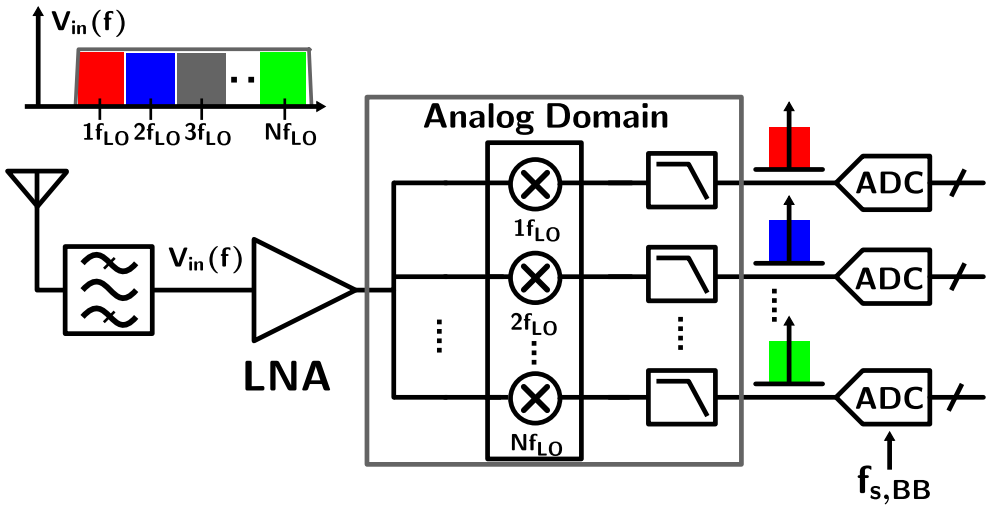


Figure 1.4: Block diagram of a mixer-based channelizer

izer is shown in Fig. 1.4. This channelizer consists of a parallel bank of mixers where each mixer (or a pair of quadrature mixers) is driven by an independent local frequency synthesizer and is followed by a low pass filter. The incident broadband input spectrum is downconverted through a mixer in each of the N paths. The input to each sub-ADC is selected and band-limited by filtering and then digitized by each sub-ADC, which can only see the sub-band of interest.

The sub-band signals are sampled at the baseband output with a lower sampling rate, relaxing the sampler bandwidth by N times compared to full-spectrum digitization [11, 12]. Such an approach also allows for scaling the amplitudes of signals in each sub-band to make the full sub-ADC range available to each sub-band. While the channelizer can be digitized with a lower sampling rate, multiple simultaneously operating local oscillators (LOs) are required. The concurrent use of multiple frequency synthesizers introduces practical challenges, such as injection-

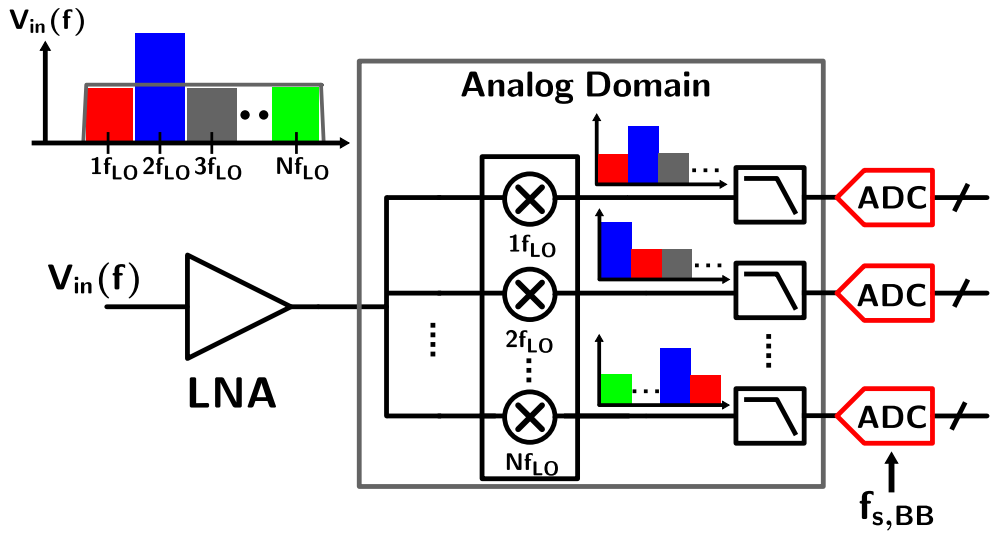


Figure 1.5: Linearity degradation in a channelizer caused by a sub-band with a large signal

locking, oscillator-pulling, and significant spurious signal levels [13]. Furthermore, a large signal in one sub-band at the input can interfere with other sub-bands in the mixer-based channelizer and degrade the linearity of the overall channelizer before it is filtered (Fig. 1.5). Such a large interferer must be attenuated at the earliest opportunity before any amplification in the receiver signal chain.

1.3 Review of prior research

The work described in this dissertation is based on an FF-ADC based receiver architecture, which channelizes the input spectrum in the frequency domain, while using a single primary clock. Key aspects of an FF-ADC [10] and prior related work are summarized below.

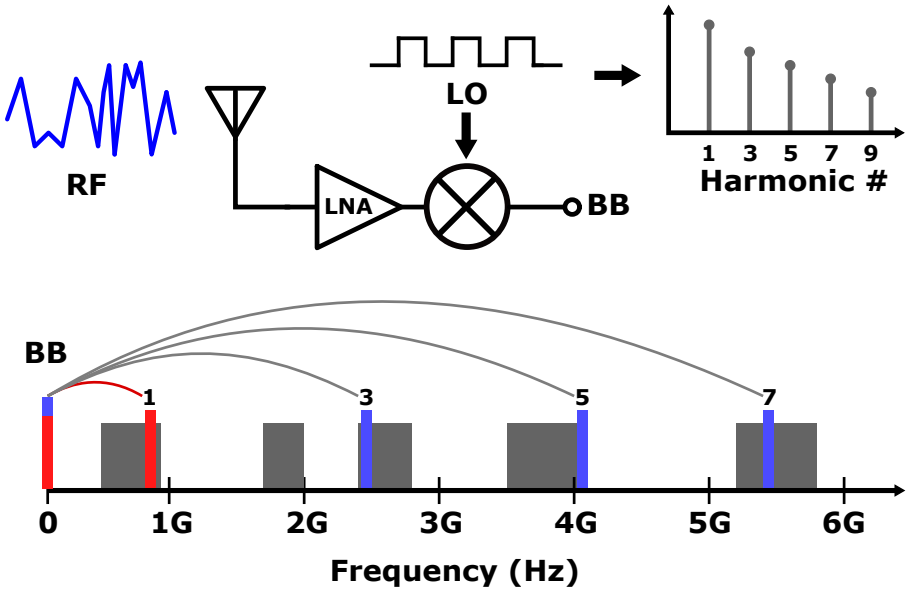


Figure 1.6: Harmonic mixing in a RF receiver

1.3.1 Harmonic rejection mixers

An RF receiver front-end generally comprises an antenna, an LNA, and a mixer (Fig. 1.6). The antenna receives the incoming RF signal, which is then amplified by the LNA. The amplified RF signal is downconverted to the baseband by the mixer. Switching mixers driven by a square wave are widely used for frequency downconversion since their noise and linearity performance are superior to analog multipliers. As this square-wave LO contains multiple harmonics of the LO frequency, f_{LO}, not only the desired signal at f_{LO} but also the potential interferers around the odd harmonics $(2k+1)f_{LO}$, where k is an integer, are downconverted simultaneously (Fig. 1.6). This can degrade the signal-to-noise (SNR) at the baseband. Therefore, a mixer design is required that avoids mixing with LO harmonics within the receiver.

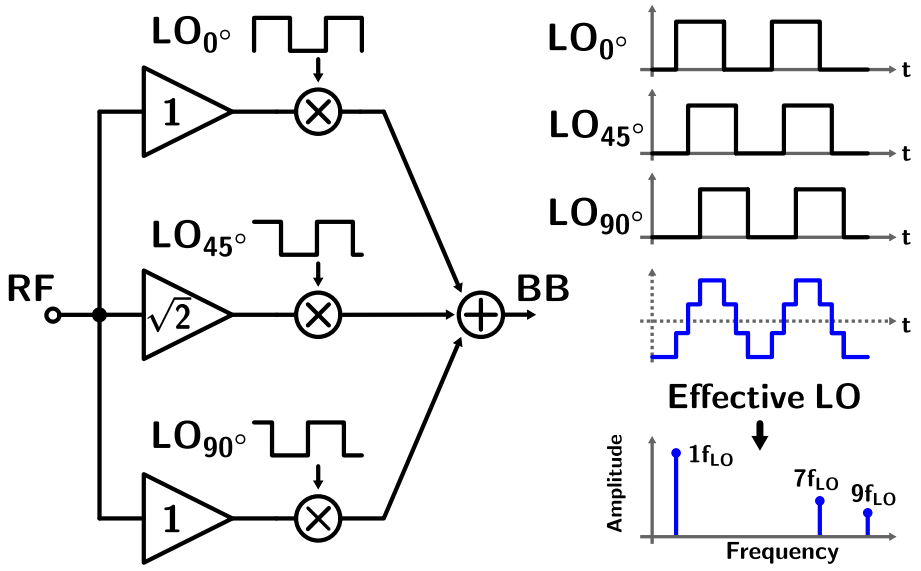


Figure 1.7: Harmonic reject mixer, its effective LO in the time-domain, and the LO frequency spectrum

Harmonic rejection mixers (HRMs) have been widely utilized in broadband receivers to suppress unwanted LO harmonics [14, 15, 16] while maintaining the advantages of switching mixers. These designs typically synthesize a discrete-amplitude approximation of a sinusoidal LO by applying a signal sequentially to gain coefficients that are proportional to samples of a sinusoid. A HRM implementation that employs three switching mixers in parallel is shown in Fig. 1.7 [14]. In this design, each path utilizes a 50% duty-cycle square-wave LO with a 45° relative phase shift. The three paths employ gains with a ratio of $1:\sqrt{2}:1$. The effective LO waveform is synthesized by summing the three switching-mixer outputs, and has harmonics at $(8m\pm 1)f_{LO}$ (where m is an integer). The harmonics at $3f_{LO}$ and $5f_{LO}$ are ideally rejected from the LO spectrum (Fig. 1.7).

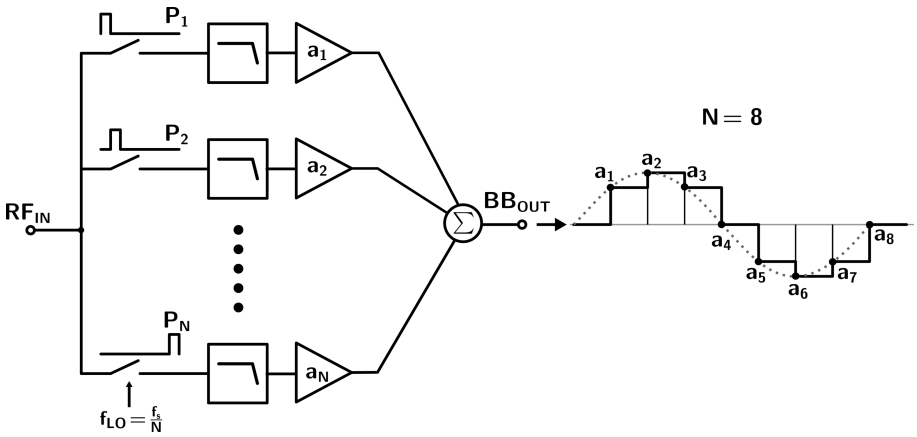


Figure 1.8: An N-phase harmonic rejection mixer using phase-shifted rectangular LOs with a duty cycle of $1/N$, with effective LO generation through time-sequencing of gain coefficients ($N = 8$)

1.3.2 Analog frequency synthesis harmonic rejection mixer

An HRM capable of analog frequency-synthesis (AFS-HRM) is employed in [17, 18]. This can generate multiple LO frequencies using a fixed primary clock, Nf_{LO}. Fig. 1.8 shows an N-phase HRM with N baseband gain coefficients [15]. An input signal is downconverted in N baseband paths by the phase-shifted rectangular LOs with a duty cycle of $1/N$ in each path. The gain coefficient applied to each path is derived from a sinusoid sampled N times per period, $1/(Nf_{LO})$. Thus, the gain coefficients are given by

$$a_k = sin(\frac{2nk\pi}{N}) \tag{1.1}$$

where k is the path number, and n is the harmonic selected for downconversion. Combining different baseband paths generates the effective LO, eliminating all har-

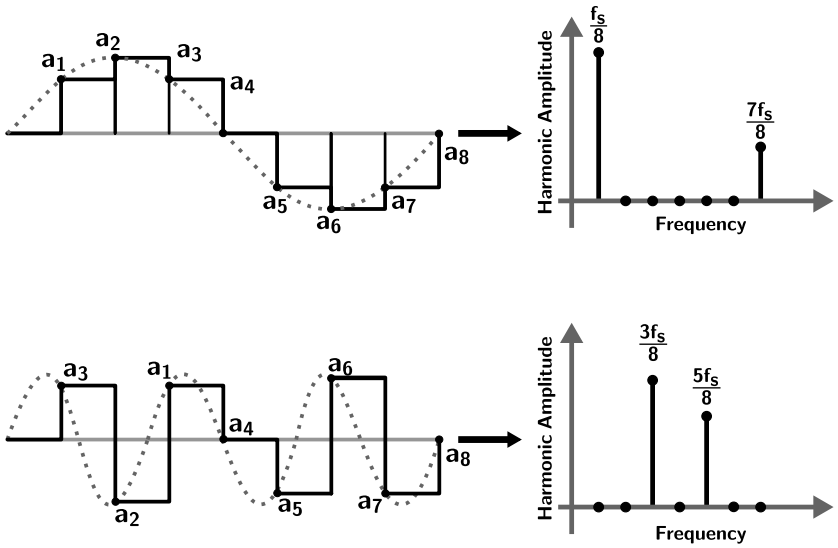


Figure 1.9: Effective generation of $1f_{LO}$ and $3f_{LO}$ by reordering gain coefficients and the resulting LO spectrum for $N = 8$

monics except for $(Nm \pm n)f_{LO}$, where m is any integer. An AFS-HRM can synthesize downconversion frequencies, qf_{LO}, $q \in [1 : N/2]$, if the appropriate coefficients, $\{a_k\}$, are applied. Fig. 1.9 shows the effective LO generation of $1f_{LO}$ and $3f_{LO}$ by reordering gain coefficients in the time-domain for $N = 8$. An AFS-HRM approach enables downconversion of the input spectrum around all individual harmonics of f_{LO} while using a single primary clock. This approach is based on a principle similar to direct digital frequency synthesis (DDFS) [19], while the implementation is performed in the analog domain.

1.3.3 Frequency-folded ADC based receiver

A frequency-folded ADC (FF-ADC) based receiver (Fig. 1.10) that employs a single primary clock, f_s, to channelize and digitize a broadband input was

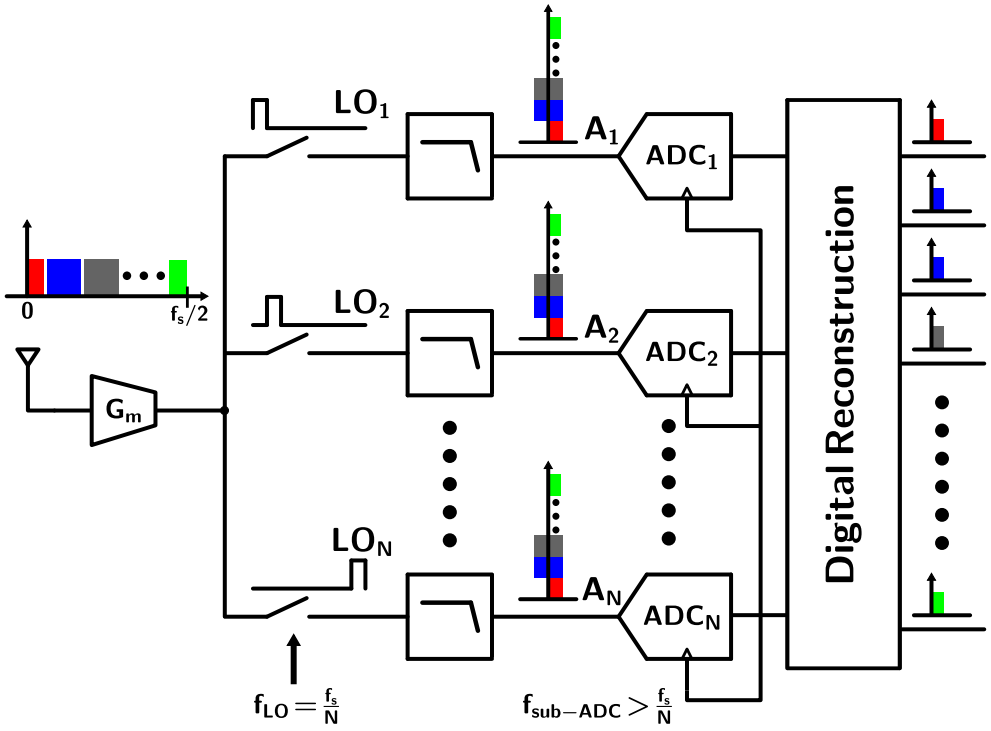


Figure 1.10: Block diagram of a frequency-folded ADC (FF-ADC)

introduced in [10]. Similar to an N-phase HRM in Section 1.3.2, the entire input spectrum is decomposed into multiple sub-bands and downconverted to the base-band by the harmonics of N non-overlapping rectangular pulses with a period of T_{LO} (Fig. 1.11). While the input signal's bandwidth is bandlimited to $Nf_{LO}/2$, the baseband signal at each analog output path is bandlimited to $f_{LO}/2$. Therefore, each sub-ADC can be operated at a lower sampling rate above f_S/N, but the overall effective sampling rate is f_s. The signal reconstruction for each sub-band is performed using digital-domain harmonic and image rejection. As shown in Fig. 1.12, the separation of sub-bands is completed by applying a set of both Cosine and Sine coefficients, $a_{i,k} = cos(\frac{2\pi n}{N}k)$ and $a_{q,k} = sin(\frac{2\pi n}{N}k)$, where k is the path number, and

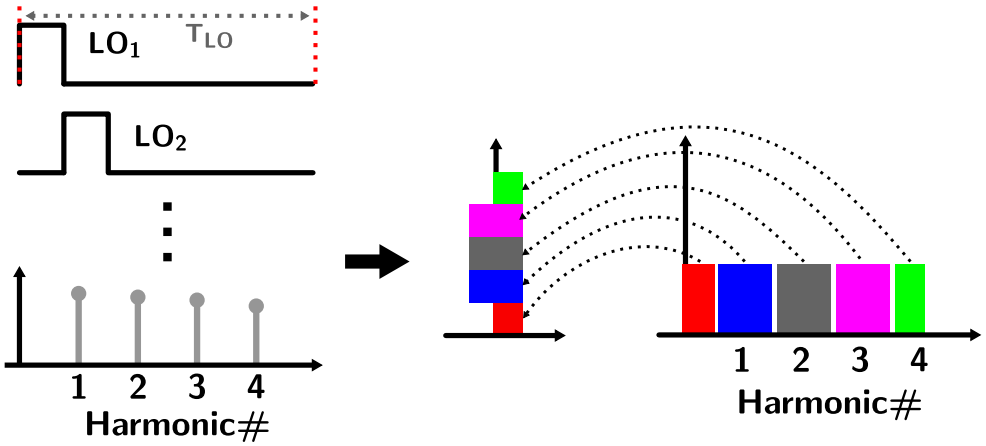


Figure 1.11: Folding of the input spectrum by N non-overlapping rectangular pulses for $N = 8$

n is the selected harmonic number, with a separate summation for each to achieve in-phase and quadrature mixing in the digital domain.

In this approach, the sampler bandwidth can be significantly relaxed because the bandwidth of the baseband signal in each path is smaller by a factor of N compared to the TI-ADC approach. In [10], a sixth-order anti-aliasing filter and 2x oversampling in each sub-ADC are employed to prevent aliasing when sub-ADCs sample the baseband signals. In order to relax the anti-aliasing filter requirement or the oversampling ratio in the sub-ADC, an approach based on digital equalization is introduced in [20].

A key challenge in this architecture originates from the potential for considerable variation in the sub-band signal level at the inputs of the sub-ADCs. Since the baseband signal at each sub-ADC's input is composed of a superposition of N downconverted sub-bands that are aliased by the harmonics of f_{LO}, a sub-band

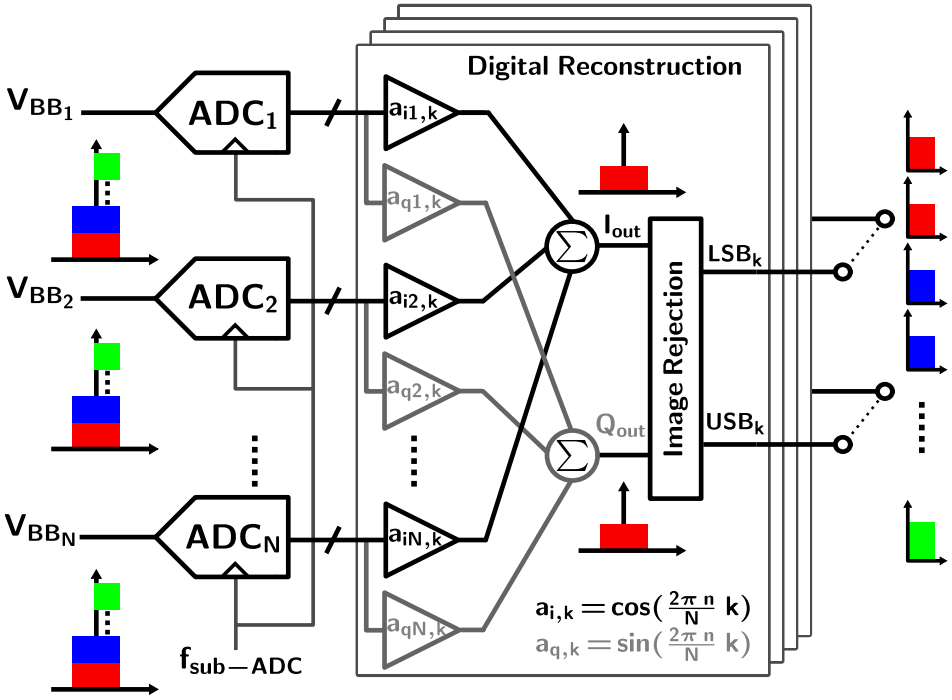


Figure 1.12: Separation of sub-bands by digital-domain harmonic and image rejection

with significant signal power can dominate the signal level in each of the baseband paths after frequency mixing. This large power can degrade the dynamic range that is available for sub-bands with small signal levels. This issue is also observed in time-interleaved ADCs. In order to avoid the dynamic range limitation arising from significant input signal variation, all sub-bands need to have a variable gain before the sub-ADCs.

1.3.4 Feedforward technique for sub-band suppression

A feedforward technique was introduced in [21] to avoid the dynamic range limitation of sub-ADCs in an FF-ADC arising from a large, spectrally local input

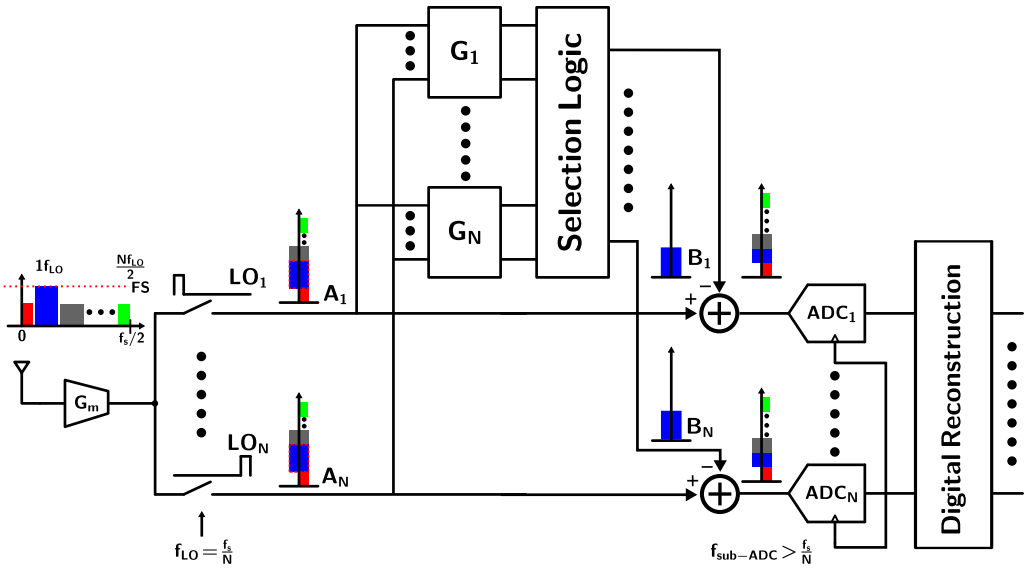


Figure 1.13: A feedforward technique in an FF-ADC to suppress the sub-band with a large signal

signal. As shown in the Fig. 1.13, the baseband AFS-HRM with frequency synthesis capability is in parallel with the FF-ADC paths for $N = 16$. This AFS-HRM provides downconversion using a single harmonic corresponding to the sub-band that has a large signal. Through proper weighting of gain coefficients, $G_1 - G_{16}$, this sub-band can be selected and subtracted at the sub-ADC input in each path. Therefore, the feedforward technique can suppress the sub-band with a large signal at the baseband before digitization. This sub-band suppression can also be implemented by a parallel AFS-HRM that uses RF gain coefficients, instead of baseband gain coefficients.

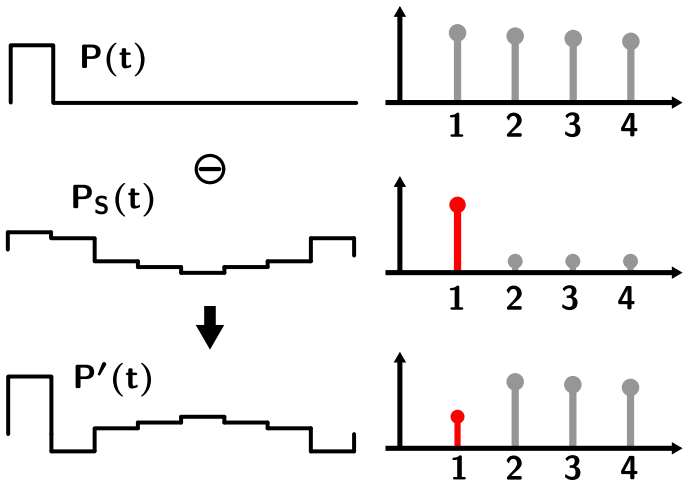


Figure 1.14: Effective LO waveforms, $P'(t)$, for gain scaling of $1 f_{LO}$

1.3.5 Sub-band gain scaling with variable RF gain coefficients

A technique using variable RF gain coefficients in an FF-ADC-based receiver was proposed in [22] for achieving sub-band gain scaling before digitization, which results in relaxing the dynamic range limitation for a specific sub-band with a large signal. Consider a single path in an FF-ADC. The rectangular pulse, $P(t)$, which has all harmonics from DC to $(N/2)f_{LO}$, downconverts and aliases the input sub-bands around harmonics of f_{LO} to baseband. In order to scale the signal power around a specific sub-band, an effective LO waveform, $P'(t)$, which can reduce the amplitude of the desired harmonic frequency, can be implemented by subtracting a discrete sinusoidal LO, $P_s(t)$, which has the desired level at the specific harmonic frequency. Fig. 1.14 indicates the resulting LO waveform, $P'(t)$.

Fig. 1.15 shows the implementation of the FF-ADC architecture using time-varying RF gain coefficients for sub-band gain control [22]. An HRM with fre-

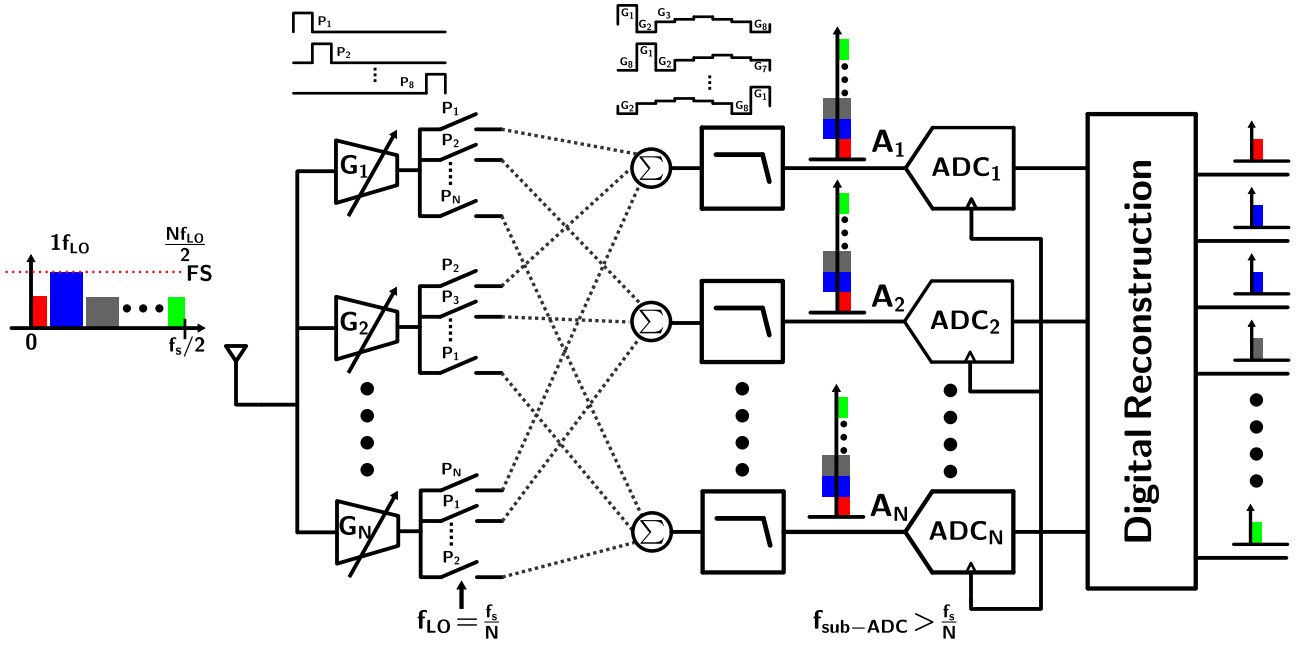


Figure 1.15: Implementation of FF-ADC architecture with sub-band gain control

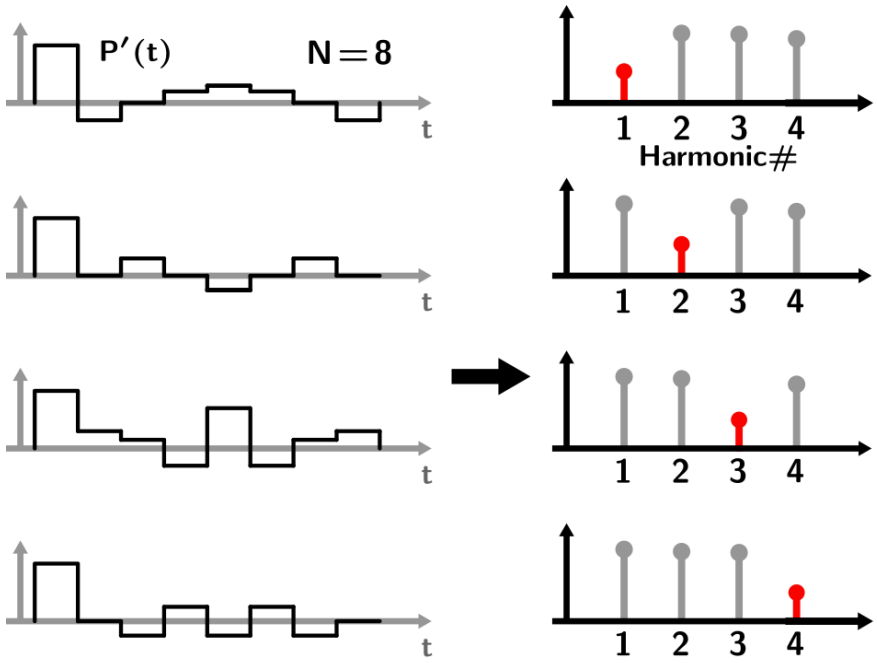


Figure 1.16: LO waveforms for single-harmonic gain scaling from $1f_{LO}$ to $4f_{LO}$

quency synthesis capability [17] is placed in parallel with the FF-ADC, using gain coefficients, G_m, $m \in \{1:N\}$, that are determined by the discrete levels that are required in $P'(t)$. N variable gm-cells implement these gain coefficients at the RF input stage. N parallel gm-cells, G_m, are connected to N switches which are driven by N non-overlapping rectangular pulses, $P_r(t)$, $r \in \{1:N\}$. Thus, the total number of switches required is $N \times N$.

Through a proper choice of gain coefficients in the HRM, the effective multiphase waveform, $P'_r(t)$, for gain control of the specific harmonic can be generated at each switch output. Fig. 1.16 shows the LO waveforms for single-harmonic gain scaling from $1f_{LO}$ to $4f_{LO}$ in an 8-path FF-ADC and corresponding time-domain waveforms $(T = 1)$. The technique can also be used for scaling the gains of all

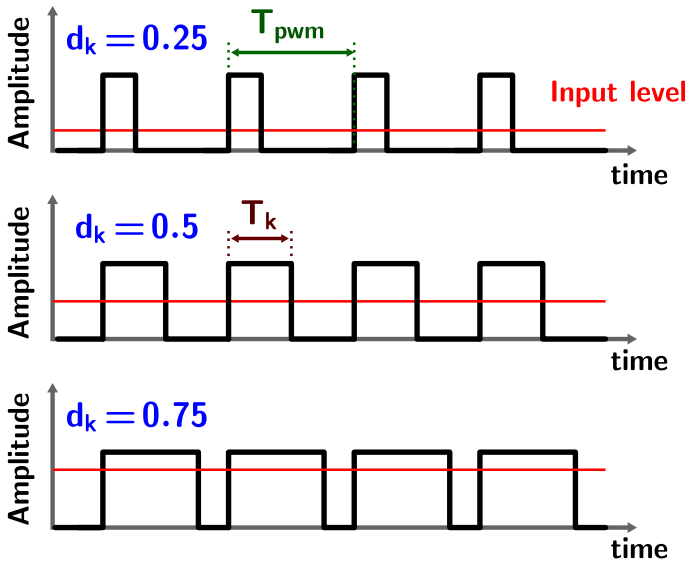


Figure 1.17: Pulse width modulation (PWM) signal

sub-bands by using the appropriate RF gain ratios.

1.4 Pulse width modulation

This section presents basic principles of pulse width modulation (PWM) in the context of sub-band gain control in the proposed spectrum channelizer. Pulse width modulation employs a periodic discrete level signal with a time period, T_{pwm} to represent the amplitude of an analog signal. The PWM signal, which has one rising edge followed by one falling edge, is generated at every time instant, kT_{pwm}. The duration for which the signal is high, is termed T_k. The duty cycle, d_k, is the ratio T_k/T_{pwm} (Fig. 1.17). In general, the implementation of PWM signals compares the input signal to a set of reference signals.

Fig. 1.18 shows various types of PWM signals [23]. In natural-sampling

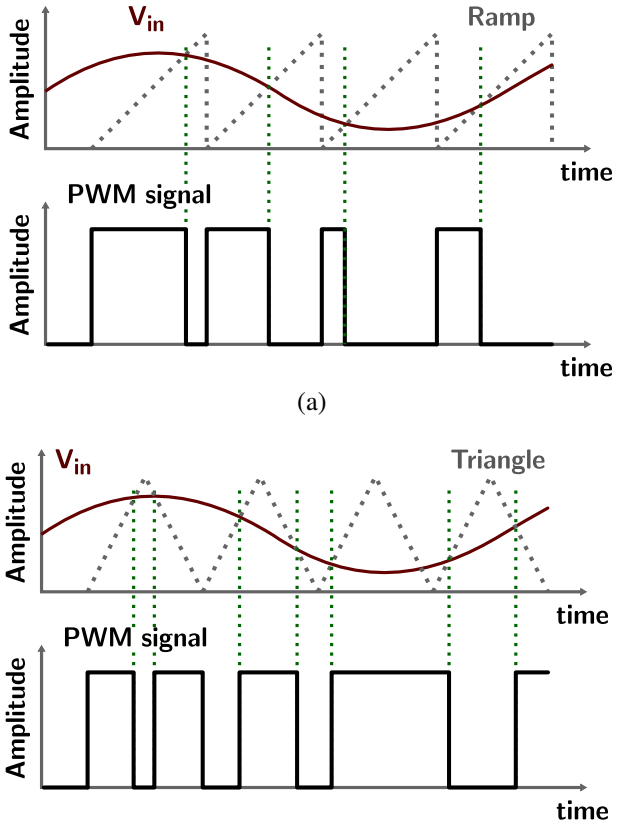
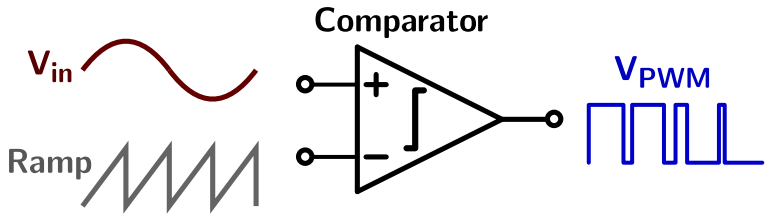


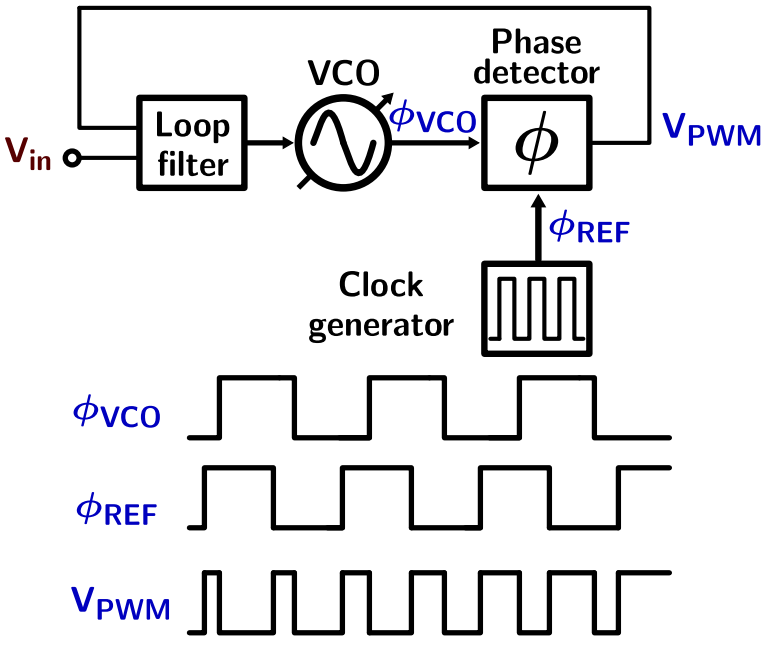
Figure 1.18: Different types of PWM (a) NTE-PWM (b) NDE-PWM

trailing-edge (NTE) PWM, the reference signal is a ramp waveform, and the rising edges appear at fixed time instants while the falling edges vary with the amplitude of the input (Fig. 1.18(a)). In natural-sampling dual-edge (NDE) PWM, the reference signal is a triangular waveform, and both edges vary with respect to the input signal (Fig. 1.18(b)).

A conventional approach for generating a PWM signal utilizes an analog comparator, which compares the input signal to a reference waveform such as a



(a)



(b)

Figure 1.19: PWM generation (a) Ramp-based architecture (b) PLL-based architecture

ramp or triangle waveform to produce the PWM signal (Fig. 1.19(a)). In a ramp-based PWM generator, the duty cycle, D_k, is proportional to the amplitude of the input signal. The reference can be implemented using analog techniques. For example, an integrator consisting of an operational amplifier, a capacitor and a resistor can be used to generate a triangular wave for dual-edge PWM. The use of an analog comparator for PWM generation has the benefit that there is no distortion since the input signal is not sampled. Due to this reason, combined with the simple circuit design requirement, this approach is often used for low-frequency applications such as audio amplifiers [24, 25, 26].

For high-frequency applications, comparator-based approaches may be challenging to employ. The operational amplifier and comparator require a higher unity-gain bandwidth than the PWM reference frequency, which can be severely challenging in current CMOS technologies, for frequencies exceeding several tens of MHz. Furthermore, a precise comparison of the input and reference signals is needed for the analog comparator. These design issues make it challenging to utilize ramp-based PWM generators for high-frequency applications.

Phase-locked loop (PLL)-based PWM generation [27, 28, 29] allows for high-frequency operation, by avoiding the requirement for an analog comparator and a linear ramp signal. As shown in Fig. 1.19(b), a phase detector generates the PWM signal by comparing the phase of the output signal of a voltage-controlled oscillator (VCO), φ_{VCO}, to that of the reference clock signal, φ_{ref}. This design requires a sufficiently high closed-loop bandwidth of the PLL for high-frequency PWM-LO generation. This requirement makes it challenging to generate the PWM-

LO required here using a PLL-based PWM generator.

A DLL-based PWM generator was demonstrated in [30], which does not require a ramp signal, a high-speed analog comparator, or have high loop gain-bandwidth requirement. This DLL-based PWM generation is used to synthesize the PWM-LOs for sub-band gain control in this work.

1.5 Dissertation organization

The remainder of this dissertation is organized as follows. Chapter 2 proposes a technique for sub-band gain scaling with the PWM-LO waveforms in an FF-ADC. The design can alleviate the dynamic range limitation arising from specific sub-bands with large signal power and relax the complexity of the signal path. Chapter 3 presents the implementation of a spectrum channelizer with PWM-LO-based sub-band gain control, which relaxes the compression performance of the channelizer and dynamic range limitation of sub-ADCs in the presence of sub-bands with large signals. The use of off-chip learning employing a neural network for determining the PWM symbol pulse widths that are required to achieve the desired harmonic levels, is also described. An alternative voltage-mode channelizer design for further architectural simplification is also proposed in Chapter 4. Conclusions and scope for future work are discussed in Chapter 5.

Chapter 2

Sub-band Gain Control in a Frequency-Folded ADC Based Spectrum Channelizer [1]

2.1 Introduction

A frequency-folded analog-to-digital converter (FF-ADC) that employs harmonic rejection (HR) downconversion for full-band spectrum channelization was demonstrated in [10]. In this approach, the input is multiplied in N paths by N non-overlapping rectangular LO pulses. Each LO pulse has a duty-cycle of $1/N$, such that its frequency domain representation is a comb, with a sinc-roll-off that is determined by N. The portions of the spectrum of the input signal that are coincident with harmonics of the rectangular LO pulses are downconverted to baseband, where they are bandlimited in low-pass filters and digitized in multiple sub-ADCs. The input is channelized into sub-bands by employing harmonic and image rejection in the digital domain.

The above architecture is similar to a time-interleaved ADC (TI-ADC), except that it decomposes the input in the frequency domain. In an FF-ADC, the

[1] This chapter is based on reference [31] (K. Y. Kim, H. Kang, V. S. Singh, and R. Gharpurey, "A broadband spectrum channelizer with PWM-LO based sub-band equalization," in 2018 IEEE 13th Dallas Circuits and Systems Conference (DCAS), pp. 1-4, Nov. 2018 ©2018 IEEE). Ki Yong Kim was responsible for the design and simulation of the channelizer architecture described in this publication.

sampler bandwidth requirement is determined by the sub-band bandwidth, instead of the full input signal bandwidth, and is smaller by approximately a factor of N. Similar to TI-ADCs, a large, spectrally-local signal can limit the dynamic range of the sub-ADCs that is available for other portions of the input spectrum.

A feedforward technique for alleviating the above dynamic range limitation of the sub-ADCs in an FF-ADC was proposed in [21], which employed analog harmonic rejection mixers (HRMs) with frequency synthesis capability in parallel with the FF-ADC paths in the analog domain. The HRMs provide a single-tone downconversion. The downconverted signal at the HRM outputs corresponding to the frequency of the tone, is subtracted in the analog domain within the FF-ADC, thus allowing for scaling the large signal in the specific sub-band before digitization. The approach requires a bank of $N \times N$ baseband gain coefficients. In [22], an approach is shown wherein, through the use of variable gain coefficients at RF, the amplitudes of the frequencies contributing to downconversion in the FF-ADC can be scaled as desired, thus allowing for amplitude scaling at baseband, at the input of the baseband sub-ADCs. The gain coefficients are implemented using RF transconductances, which are applied to the baseband through an $N \times N$ matrix of switches. The design requires (ideally) variable gain coefficients for achieving an arbitrarily variable spectrum in the FF-ADC downconversion. A receiver with non-overlapping LOs that can select the desired harmonics but reject other harmonics with sinusoidal weighting coefficients at baseband is demonstrated in [32].

In the proposed architecture, the use of PWM-LO waveforms for representing the above gain coefficients is described. The gain coefficients are effectively

determined by the pulse widths of the PWM-LO. The approach simplifies the signal path, as it does not require an $N \times N$ switch-matrix or bank of gain coefficients to achieve the desired spectral shaping, which is instead performed through control of pulse widths in the PWM waveforms.

In this chapter, Section 2.2 describes the FF-ADC. The approaches of [21] and [22] that allow for shaping the incident spectrum in an FF-ADC are described in Section 2.3. The use of PWM-LOs for this purpose is presented in Section 2.4.1, along with simulation results depicting multiple examples of spectral shaping and the corresponding PWM-LO waveforms employed in the design. An approach to generate the PWM-LO waveforms for sub-band gain control is also described in Section 2.4.1.

2.2 Frequency-folded ADC (FF-ADC) architecture

The FF-ADC architecture was introduced in Section 1.3.3. A detailed description of the architecture is provided here. The FF-ADC architecture (Fig. 2.1) [10] consists of an input transconductor that converts the input signal to current. The current is applied to N switches in sequence, which are driven by periodic rectangular clocks of period T and duty-cycle $1/N$.

The frequency components in the spectrum of the LO waveforms are spaced by $1/T$. The amplitudes of the harmonics are scaled by $sinc(f\frac{T}{N})$, which goes to zero for $f_s \equiv f = N/T$. The input is bandlimited to $f_s/2$, and, all components of the input spectrum around k/T, $k \in \mathbb{Z}$, are translated to the baseband, and to integer multiples of 1/T in the frequency domain. As described in [10], a sharp low-pass

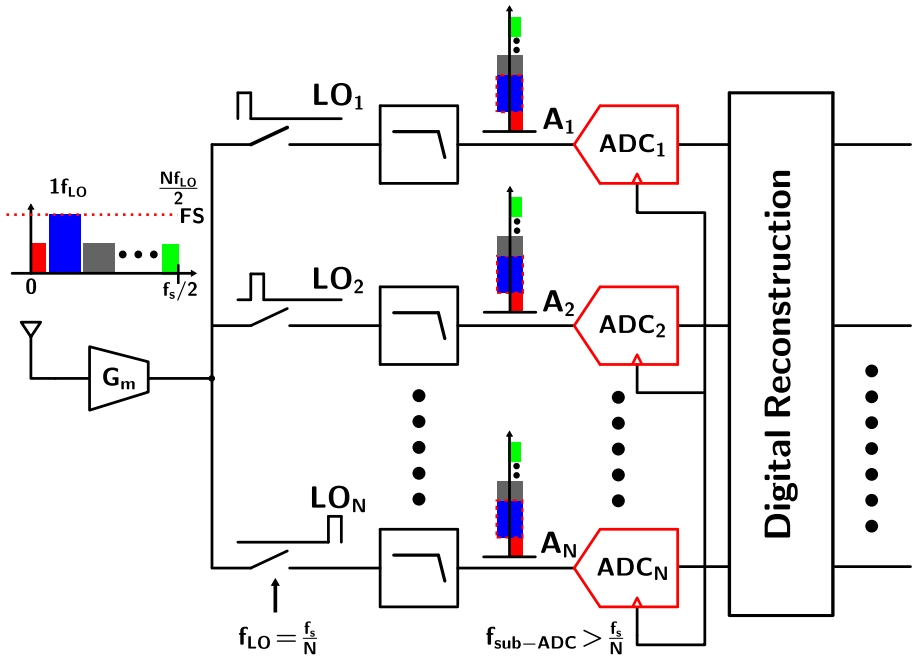


Figure 2.1: Degradation of sub-ADC dynamic range in an FF-ADC due to a single sub-band with a large signal

filter (LPF) of bandwidth $1/(2T)$ Hz can be applied in each path of the N paths. Each LPF output, which consists of aliased signal components from around k/T, is subsequently digitized using a sub-ADC. The LPF can also be used to provide gain, in order to amplify the baseband signal to the sub-ADC full-scale range. All N sub-ADCs sample at the same time instants, at a rate greater than 1/T.

The phase-shifted digitized signals after the sub-ADCs can be combined using the harmonic rejection principle to effectively downconvert a desired portion of the input spectrum. In the digital domain, if gain coefficients that are in proportion to the samples of a sinusoid, taken at N consecutive phase-steps of $2\pi/N$ over one period, are applied to the digitized inputs in the N paths, the sub-band at frequency

$f_{LO} \equiv 1/T$ is selected. By reconfiguring the sequence of application of the gain coefficients, all sub-bands with a bandwidth of $1/T$ each, corresponding to kf_{LO} for $k \in [0, N/2-1]$, can be isolated. Using image rejection, the sub-bands around kf_{LO} can be further resolved into upper and lower sidebands, each of bandwidth of $f_s/2$, where $f_s = Nf_{LO}$.

The sampling rate of the sub-ADCs needs to be greater than f_{LO}, similar to sub-ADCs employed in a time-interleaved ADC. However, the analog bandwidth of the sampler is also of the same order as f_{LO}, which is significantly relaxed compared to a time-interleaved ADC. Additional architectural comparisons are provided in [10].

The LPFs in each path need to be sufficiently sharp, such that the aliasing caused by the sampling in the sub-ADCs is reduced to an acceptable level. Band-limiting of the sub-bands is achieved in [10] by using 6^{th}-order anti-aliasing filtering. Aliasing in the sub-ADCs is further reduced by using 2x over-sampling in each sub-ADC. As described in [20], digital calibration can be employed to relax the order of the anti-aliasing LPFs.

2.3 Variable gain coefficients for sub-band gain control

As shown in Fig. 2.1, the baseband signals at the inputs of the sub-ADCs are scaled with the strength of the sub-bands at the transconductor input. The sub-bands with the larger power spectral density (PSD) therefore dominate the dynamic range of the sub-ADCs, thereby reducing the dynamic range available for other sub-bands with smaller power. This is a challenge in time-interleaved ADCs as well.

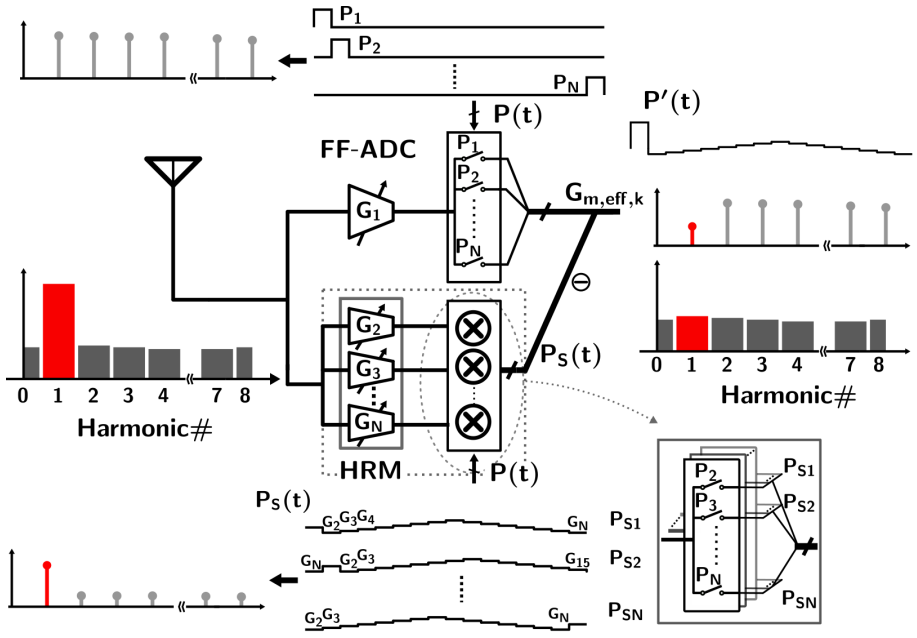


Figure 2.2: Implementation of effective LO waveforms with RF gain coefficients, $P''(t)$ ($N = 16$) for sub-band gain-scaling

A key benefit of the frequency-domain operation of this FF-ADC based architecture is that the sub-bands can be individually selected and scaled at the inputs of the sub-ADCs, as a consequence of which the amplitude of various sub-bands can be controlled as required, which makes it possible to optimize the dynamic range for any of the sub-bands.

Selection and scaling of individual sub-bands can be performed using a harmonic-rejection downconverter with an FF-ADC as described in [21, 22]. An intuitive description of the approach of [22] is shown in Fig. 2.2. By setting the magnitude of the gain coefficients in the HRM appropriately, specific sub-bands can be enhanced or attenuated, for example, by using gain steps from Fig. 2.3

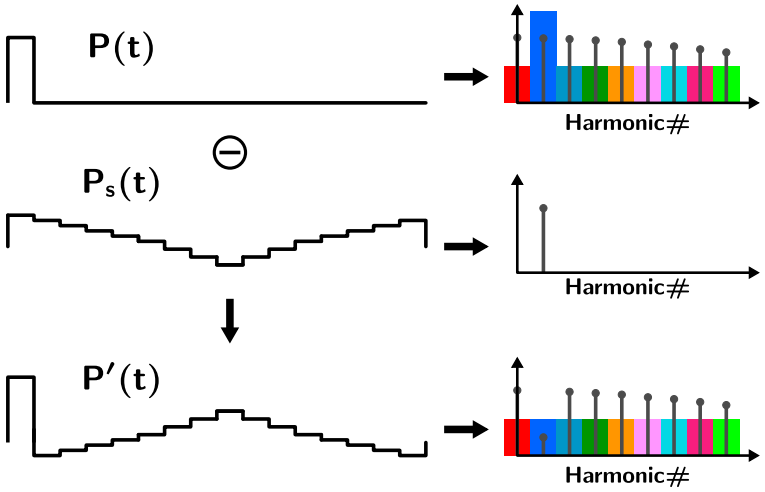


Figure 2.3: Mixing waveform to reject harmonic of $1f_{LO}$

($P_S(t)$), near-ideal rejection of $1f_{LO}$ is achieved at the sub-ADCs input. The FF-ADC and the HRM both employ 16 LO phases, and thus the useful input spectrum is up to the 8^{th} harmonic. For isolating all harmonics of the FF-ADC in the digital domain, all 16 phases of the waveform shown in Fig. 2.3 need to be implemented.

The waveform $P'(t)$ in Fig. 2.3 can be synthesized using baseband [21] or RF [22] gain coefficients. For implementing the discrete sinusoidal waveform of Fig. 2.3, in the approach of Fig. 2.2, 16 RF transconductance gain coefficients, $G_1 - G_{16}$, are employed in an FF-ADC and an HRM in [22]. A matrix of 16×16 switches is used to apply these gain coefficients in a cyclical manner in each of the 16 baseband paths. The HRM consisting of variable transconductances and switches is placed in parallel with the FF-ADC paths that use a transconductance G_1 to implement $P'(t)$. A discrete-level waveform, $P_S(t)$, which has the amplitude level for the desired harmonic scaling, can be achieved by using RF gain coefficients,

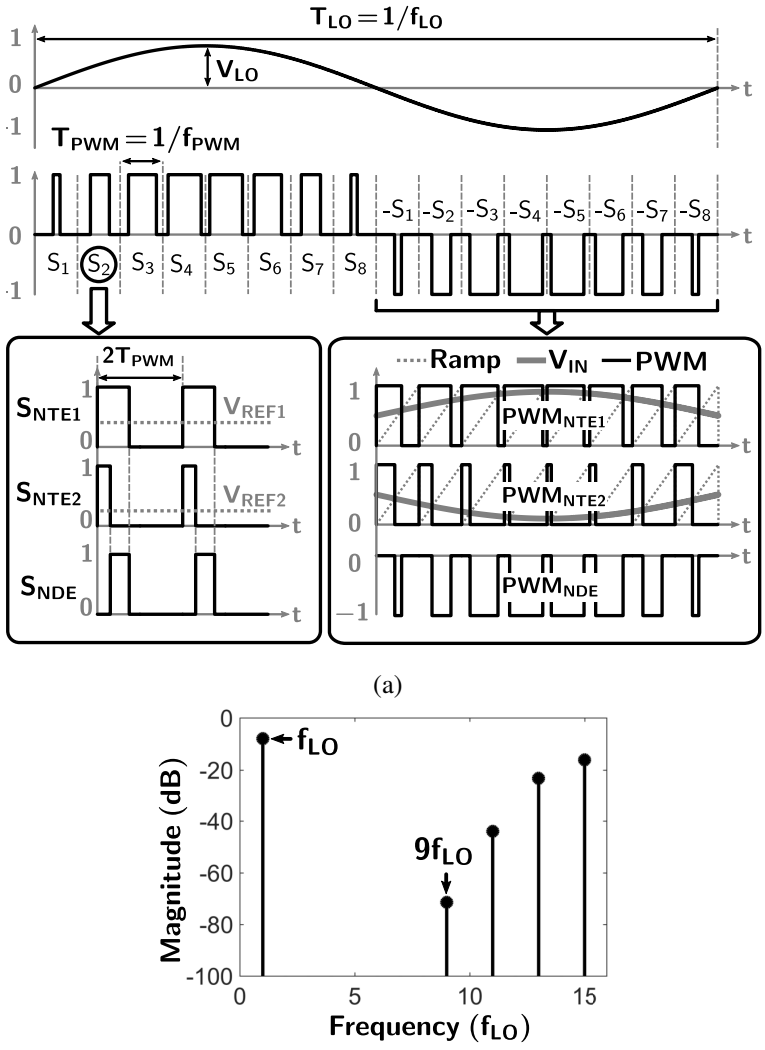
$G_2 - G_{16}$ in the HRM. The effective waveform, $P'(t)$, which enables attenuation of the desired harmonic, can be accomplished by subtracting $P(t)$ and $P_S(t)$.

Two sub-bands can be similarly scaled by placing two HRMs in shunt with the FF-ADC. Since the RF transconductor stages in each of the HRMs simply appear in parallel, in effect, scaling of two sub-bands also requires a configuration of 16 RF transconductors, as well as a matrix of 16×16 switches. In this manner, the input spectrum can be shaped as required while using an identical physical implementation, as long as the RF transconductance values are selected appropriately.

2.4 PWM-LO waveform in the FF-ADC for sub-band gain control

2.4.1 PWM-LO generation

In [30], an approach was demonstrated to implement a discrete-level representation of a sinusoidal LO employing natural-sampling pulse-width modulation (NS-PWM). The discrete-level waveform consists of a sequence of PWM pulses, with pulse widths that are equivalent to gain coefficients in an HRM. This is shown in Fig. 2.4, where a sine-wave is approximated using natural-sampling dual-edge (NDE) pulses. Each NDE-PWM pulse is synthesized using two natural-sampling trailing edge (NTE) PWM pulses in delay-locked loops (DLLs). The NDE-PWM waveform can be directly applied to a switch to achieve harmonic rejection mixing. Since the LO waveform uses discrete levels, the advantage of amplitude limiting is retained in the switches.



(a)

(b)

Figure 2.4: Differential 3-level NDE-PWM. (a) waveform, (b) spectrum

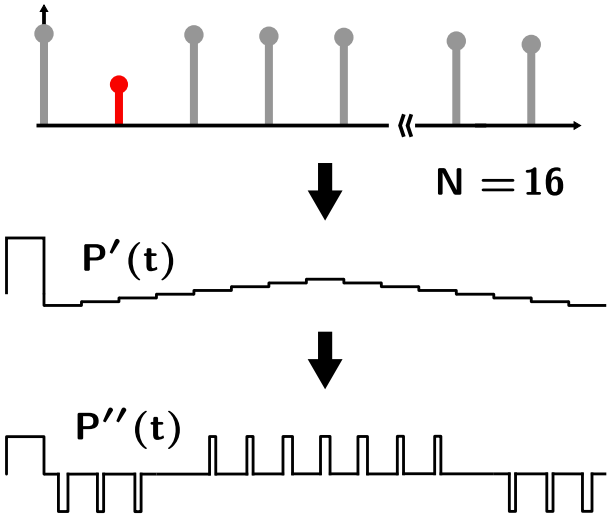


Figure 2.5: PWM-LO waveform for rejection of band-1 for $N = 16$

2.4.2 FF-ADC-based channelizer with PWM-LOs

In an HRM approach employing gain coefficients, as shown in Fig. 2.2, varying the spectral response requires variable transconductors $(g_{m,k})$. Instead of amplitude-based gain coefficients, as shown in Fig. 2.3, the approach of [30] can be employed, wherein the input is multiplied with a PWM-LO. A mixing waveform similar to that shown in Fig. 2.3, with its PWM equivalent, is shown in Fig. 2.5.

The PWM-LO waveform has a period T and consists of N pulse intervals. It is repeated in N paths with a time offset of T/N, which can easily be implemented through a delay circuit [30]. The architecture of the proposed approach is shown in Fig. 2.6. We note that the switching requirement is relaxed in the signal path since only one switch is required in series with each transconductor. Furthermore, changing the degree of suppression requires modification of the pulse widths in the time-domain while not varying the transconductance levels themselves. A

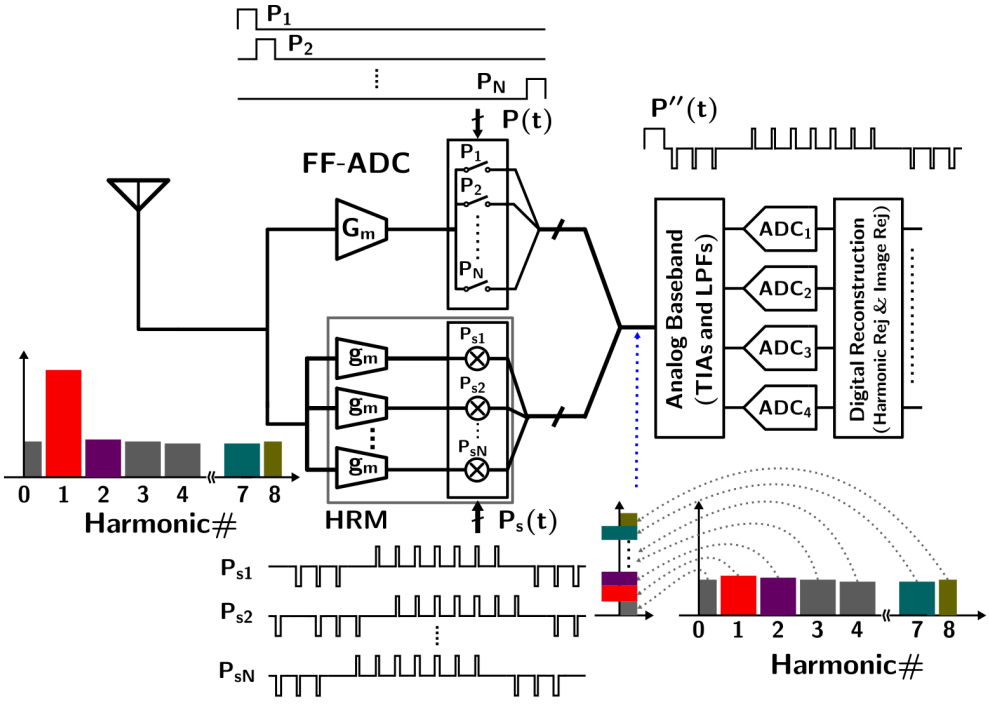


Figure 2.6: Block diagram of the FF-ADC Channelizer with PWM-LOs for sub-band gain control

rectangular pulse with a duty cycle of $1/N$ and a time period of T_{LO} has multiple harmonics whose gain is scaled down by the sinc-roll-off. In order to compensate for this, the LO waveform that corrects for this gain-reduction can be generated by using RF gain coefficients [22]. This sinc-roll-off compensation can be applied to harmonic gain scaling simultaneously. The spectra and corresponding time-domain sequences of the PWM-LOs that result in rejection of a single sub-band by 20-dB for sub-bands located at $1f_{LO}$ to $8f_{LO}$ in 16-path FF-ADC are shown in Fig. 2.7, with $T = 1$. The harmonic response of the PWM-LOs is observed to compensate for the sinc-roll-off gain reduction in Fig. 2.7.

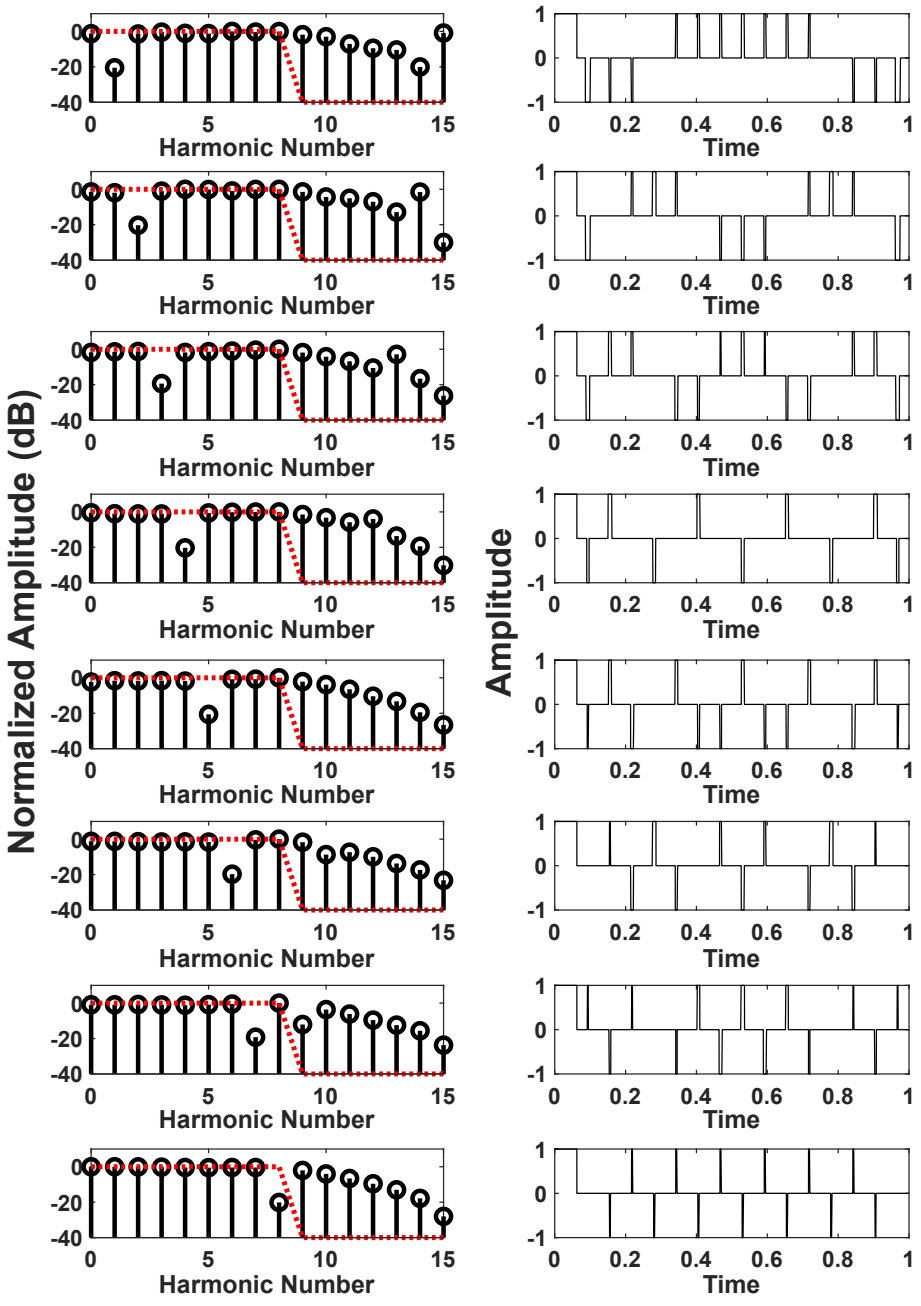


Figure 2.7: Rejection of sub-bands located at $1f_{LO}$ to $8f_{LO}$ for $N = 16$

The mapping of the gain coefficients to PWM-LO pulse widths, as shown in Fig. 2.5, is non-linear. Thus directly determining the pulse widths of the PWM-LO waveforms from the gain coefficients, e.g., through scaling the duty-cycle in proportion to the gain coefficient magnitude, does not provide accurate harmonic scaling. This is discussed further in Section 3.5. In order to enhance the mapping accuracy, a neural-network-based supervised learning technique is applied. The neural-network is trained using sets of Fourier coefficients and the time instants of the rising and falling edges of the pulses in the corresponding PWM-LO waveforms and is then used to predict the required PWM-LO pulse edges for a given spectrum. Examples of results of such mapping for arbitrary spectrum profiles are shown in Fig. 2.8. As can be observed, an accurate representation of the desired spectrum profile is achieved.

To alleviate the narrow-pulse width limitation of the PWM-LO waveform, the transconductances for the PWM-LO pulses can be designed with reduced values, relative to those used for the main-pulses with $1/N$ duty-cycle, in an architecture that is similar to what is shown in Fig. 2.2. The approach can also be combined with the design shown in Fig. 2.6, which uses smaller gains in the PWM-LO paths, to avoid narrow pulses. A wider pulse width of the PWM-LOs can compensate for this reduced value of transconductance.

Fig. 2.9 shows individual LO harmonics that effectively downconvert the input, for the PWM-LO waveform of Fig. 2.7, where the second harmonic is suppressed by 20 dB. These are derived through digital-domain separation employing harmonic rejection coefficients [10].

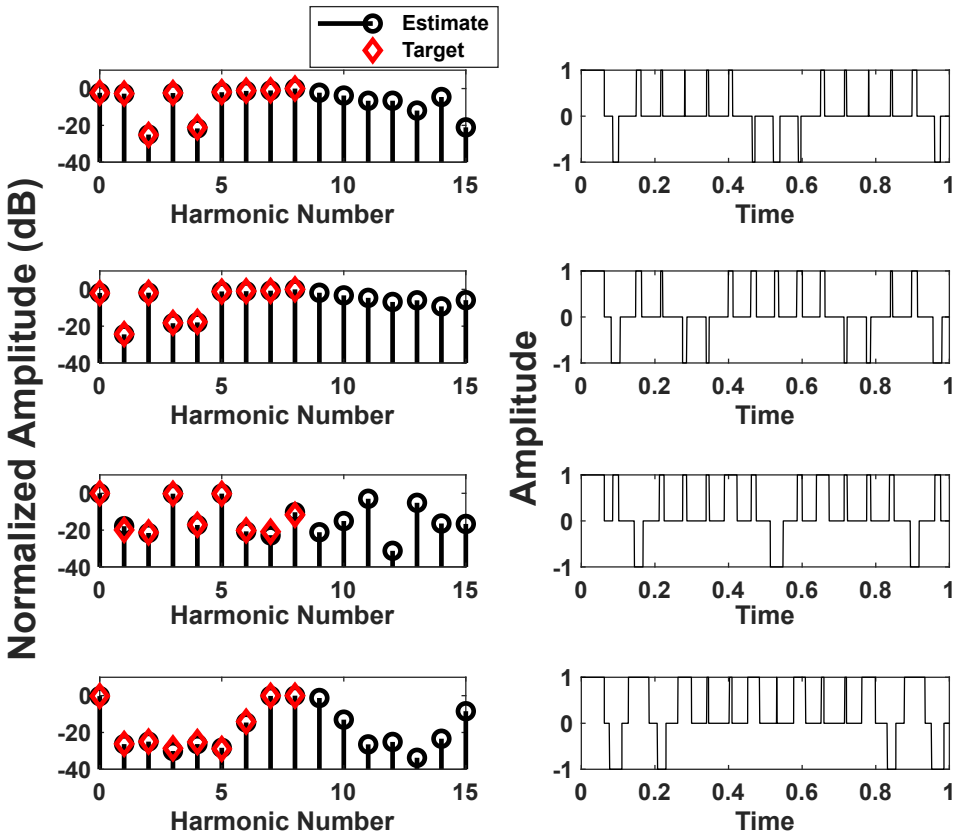


Figure 2.8: Examples of rejection of arbitrary sub-bands

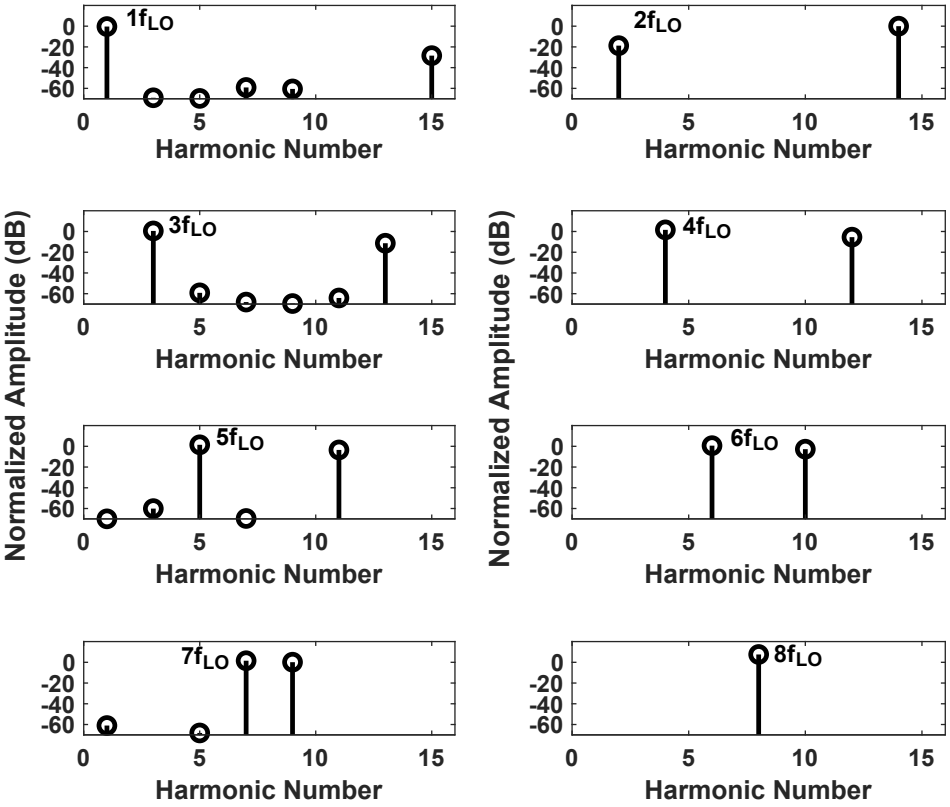


Figure 2.9: Effective LO harmonic response in the digital domain

2.5 Summary

An FF-ADC with customized PWM-LOs to shape the spectrum profile at baseband, in the analog domain, for optimizing the sub-ADC dynamic range available for each sub-band in the channelized system, was proposed. The use of PWM-LOs alleviates the complexity of the signal path. The PWM-LO waveforms for providing specific spectrum profiles are determined using a neural-network-based estimator.

Chapter 3

A 1.6 GS/s Spectrum Channelizer with PWM-LO Based Sub-Band Gain Control [1]

3.1 Introduction

Broadband receivers are required in a multitude of applications, such as communication receivers for broadband standards and those employing channel aggregation, as well as for spectrum analyzers, as noted in Chapter 1. One approach to implementing such a receiver is a direct sampling (DS) architecture that digitizes the entire input spectrum with a high-speed analog-to-digital converter (ADC) [2]. A direct sampling architecture does not experience analog-domain noise and linearity limitations after sampling and quantization, since mixing and filtering for channelization are performed in the digital domain. On the other hand, the analog sampler and the pre-amplifier require a sufficiently wide bandwidth to sample the broadband input spectrum directly. Furthermore, these need to be sufficiently linear, such that their dynamic range exceeds that of the complete receiver, which can lead to high power dissipation. An approach with multiple sub-ADCs to lower the sample rate of individual sub-ADCs is employed in time-interleaved (TI) ADCs [6, 8].

[1] This chapter is based on reference [33] (K. Y. Kim, D. Z. Pan, and R. Gharpurey, "A broadband spectrum channelizer with PWM-LO based sub-band gain control," IEEE J. Solid-State Circuits, vol. 5, pp. 1398-1410, March 2022, ©2022 IEEE). Ki Yong Kim was responsible for the design, implementation and measurement of the channelizer IC described in the publication.

The use of a TI-ADC in a DS receiver does not however alleviate the requirements for a high dynamic-range broadband front-end sampler and amplifier.

A frequency-folded ADC (FF-ADC) based receiver that employs multiple sub-ADCs, similar to a TI-ADC, was introduced in [10]. The architecture is described in Chapter 2, and reviewed here briefly. In an FF-ADC, a broadband input signal is downconverted and aliased to baseband in N signal paths using N non-overlapping rectangular clocks, with identical period T_{LO}. Each clock waveform consists of the fundamental frequency, $f_{LO} = 1/T_{LO}$, and its harmonics. All clocks are derived from a single primary square-wave clock at a frequency $f_s = Nf_{LO}$. Each signal path consists of a switch, a transimpedance amplifier (TIA), a low-pass filter (LPF), and a sub-ADC. The baseband signal at each analog output path is band-limited to $f_s/(2N)$ and digitized using a sub-ADC with a lower sampling rate in excess of f_s/N. The architecture provides an overall effective sampling rate of f_s. The signal after downconversion in each path consists of aliased sub-bands of the input spectrum, spaced by f_{LO}. After digitization, harmonic rejection (HR) and image rejection (IR) are performed in the digital domain to separate sub-bands. The sampler bandwidth requirement in an FF-ADC is set by the sub-band bandwidth instead of the entire input bandwidth.

The complete input signal is presented to each sub-ADC's input in an aliased form in the FF-ADC. In applications with considerable variation in the sub-band signal levels, a large signal in one sub-band at the input can limit the dynamic range for small signals in other sub-bands, similar to a TI-ADC. This issue can be avoided if the gains applied to each sub-band in the FF-ADC can be made variable. Sev-

eral techniques have been presented to allow for sub-band scaling. As discussed in Chapter 2, a feed-forward technique is described in [21] that employs an analog harmonic rejection mixer (HRM) [14, 16] with frequency synthesis capability to downconvert a single sub-band. Thus a sub-band with a relatively large power-level can be downconverted, and subtracted at baseband before digitization, to improve the dynamic range available to other sub-bands. In [22], an approach is described that employs variable RF gain coefficients to set different gains at individual sub-bands in order to attenuate sub-bands with large signal levels, allowing for amplitude scaling at the input of sub-ADCs. In [32], a receiver with non-overlapping LOs that can select an arbitrary number of harmonics, but reject other harmonics by applying sinusoidal gain coefficients at baseband is described. This approach employs N non-overlapping clocks for the implementation. Extracting k sub-bands in such an approach requires $k \times N$ variable transconductors.

In this chapter, a spectrum channelizer that employs pulse-width-modulated LOs (PWM-LOs) for sub-band gain-scaling is demonstrated [31, 34]. The pulse-widths of the PWM-LOs are used for gain control in each path of the FF-ADC, and similar to an FF-ADC, through the use of multi-phase LO paths, sub-bands are isolated after digitization using harmonic rejection and image rejection. The approach simplifies the signal path since it does not require an $N \times N$ matrix of switches or variable gm-cells for achieving the desired harmonic scaling. Estimation of pulse-widths for achieving a required gain profile is performed using an off-chip supervised learning approach employing a neural network.

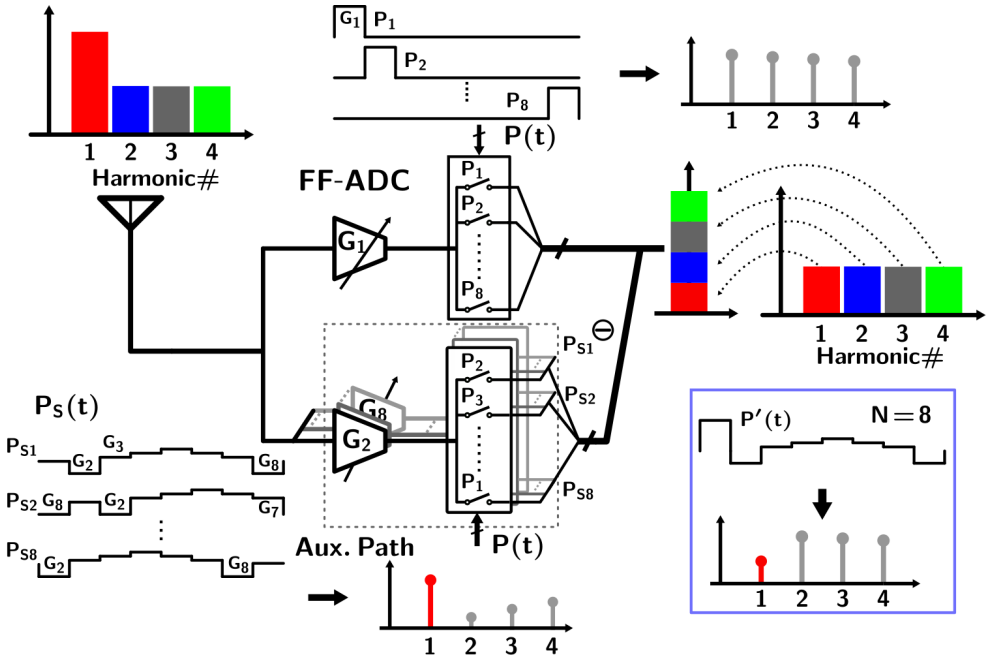


Figure 3.1: LO waveform synthesis with RF gain coefficients, $P'(t)$ for sub-band gain scaling ($N = 8$)

3.2 Receiver architecture

The techniques that enable sub-band gain control in an FF-ADC are described in detail in Chapter 2, while the implementation of each technique for a practical receiver design is presented in this section.

3.2.1 LO waveforms for sub-band gain-scaling

A sub-band equalization technique using RF gain coefficients in an FF-ADC architecture was introduced to allow harmonic scaling [22] and described in Section 2.3. Fig. 3.1 shows this approach with eight RF gain coefficients, $G_1 - G_8$. The LO waveforms required in eight paths for attenuating the fundamental LO component

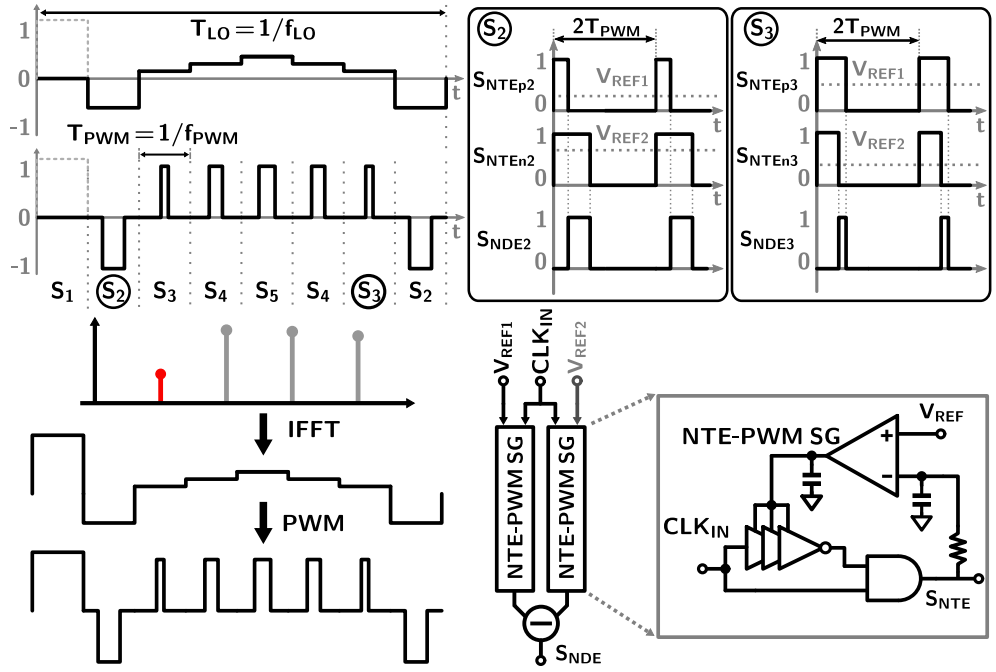


Figure 3.2: PWM-based LO waveforms for harmonic scaling for $N = 8$

at f_{LO} is shown in Fig. 3.1. The rectangular clocks, $P(t)$, used in the FF-ADC exhibit a $sin(n\pi/N)/(n\pi)$ roll-off, and have nearly equal harmonics up to $4f_{LO}$. The auxiliary path synthesizes a waveform, $P_S(t)$, which emphasizes the fundamental term at f_{LO} and attenuates all other harmonics. The effective LO waveform, $P'(t)$, which is achieved through the subtraction of $P(t)$ and $P_S(t)$, thus attenuates the $1f_{LO}$ term, thereby equalizing all sub-bands in the baseband paths.

3.2.2 PWM-LO based sub-band gain scaling

The use of PWM-LO waveforms consisting of Natural-Sampling Dual-Edge (NDE) PWM symbols to represent discrete sinusoidal LO waveforms in a harmonic rejection downconverter was shown in [30] (Fig. 3.2). The NDE-PWM waveform's

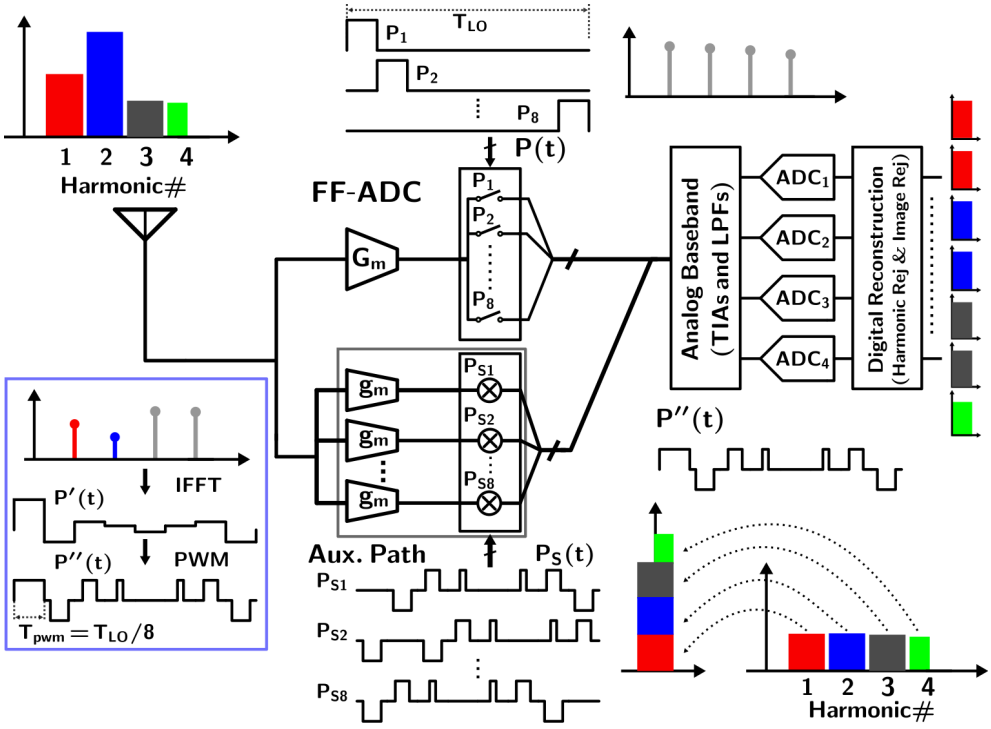


Figure 3.3: PWM-LO based gain-scaling applied to an FF-ADC downconverter for $N = 8$

pulse-width corresponds to a gain step in the effective LO waveform synthesized using g_m-cells in a harmonic rejection mixer. A PWM-LO consisting of a sequence of multiple NDE-PWM symbols can thus be used to achieve a desired harmonic response [31]. This can be contrasted with the approach of [22], which uses discrete gain steps for this purpose.

The spectrum channelizer employing PWM-LOs with an FF-ADC is shown in Fig. 3.3 [34]. The auxiliary downconverter employs the same number of PWM-LO phases as the rectangular LOs used in the FF-ADC. The architecture synthesizes an effective LO, $P''(t)$, by subtracting the PWM-LO waveform, $P_S(t)$, which

provides the desired harmonic scaling, from the rectangular pulse waveform, $P(t)$, which contains all harmonics of the fundamental, scaled by a $sin(n\pi/N)/(n\pi)$ factor, for the n^{th} harmonic, ($n \in [1,2,\cdots,N/2]$). The auxiliary downconverter paths use fixed transconductance values in individual paths, and are switched by PWM-LO waveforms. The PWM-LO waveform in any one path is simply a time-shifted version of the waveform in another path. This architecture can simplify the signal path as only one switch is used in series with each g_m-cell instead of an $N \times N$ switch matrix [22] since the multiphase PWM-LO waveforms are used to provide the harmonic gain control. The degree of suppression for single or multiple harmonics to achieve a desired sub-band gain profile is achieved through pulse-width control of the NDE-PWM pulses. The PWM-LO waveforms can also be used to compensate for the sinc-roll-off gain reduction similar to the approach in [22].

3.3 Circuit implementation

Fig. 3.4 shows the architecture of the 8-path PWM-LO based spectrum channelizer. A noise-canceling [35] differential main-path LNTA provides input impedance matching and converts the RF input signal to current. Current-mode passive mixers, driven by non-overlapping pulse LOs with a fundamental frequency of 200 MHz and duty cycle of 1/8, downconvert and alias the current to baseband in eight independent paths. The auxiliary path, which operates as an HRM, consists of eight identical LNTAs with switches which are driven by 8-phase PWM-LO waveforms to provide the desired gain-scaling. Each NDE-PWM symbol's pulse-width is determined by external reference voltages applied to the DLLs. The eight paths

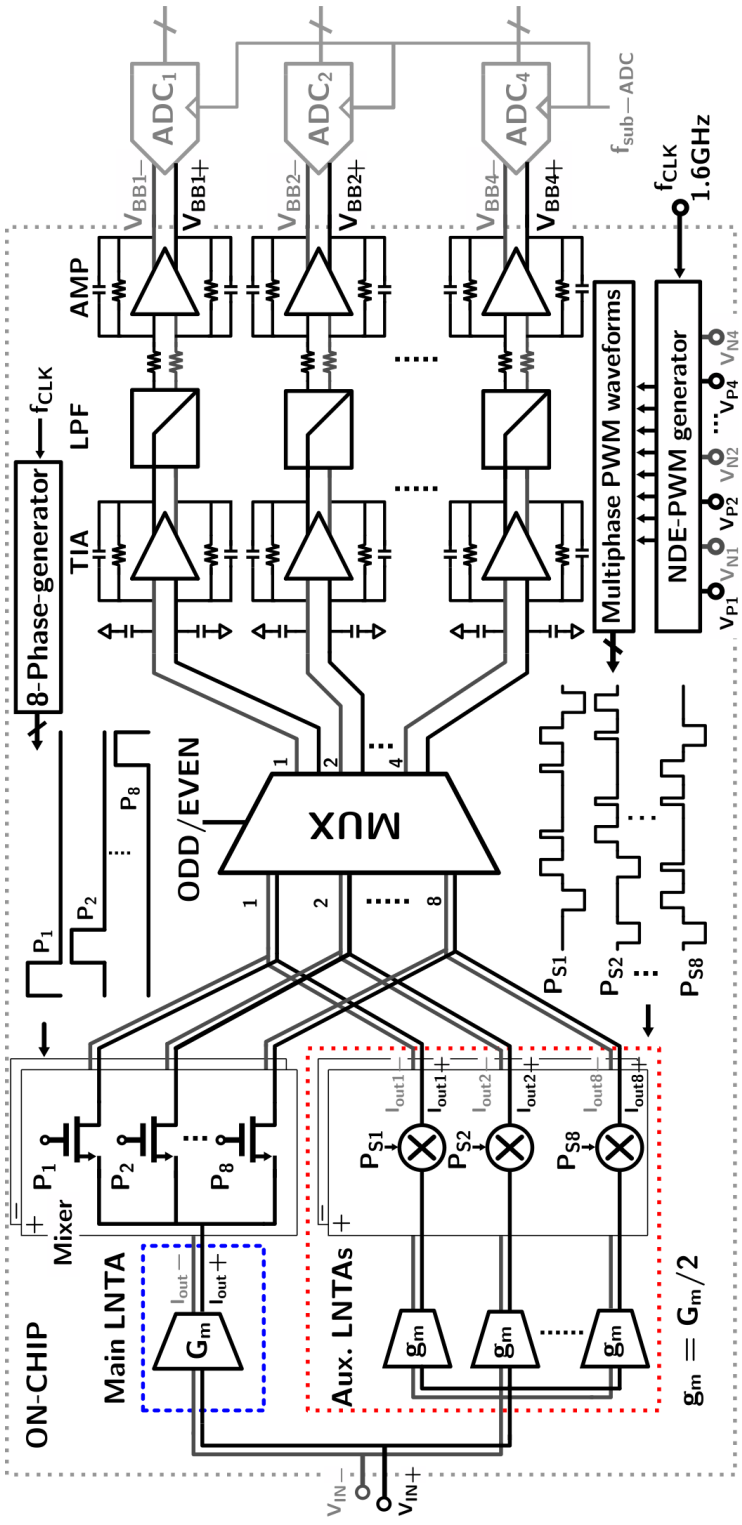


Figure 3.4: Block diagram of the spectrum channelizer with PWM-LOs for $N = 8$

are implemented with only four baseband paths after downconversion by exploiting the symmetry of the sinusoidal coefficients and using a multiplexer (MUX) in the signal path [10]. The downconverted current at the baseband is converted to voltages in a transimpedance amplifier (TIA). The TIAs are followed by 6^{th}-order low-pass filters (LPF) with 3-dB bandwidth of 100 MHz to band-limit the downconverted and aliased input sub-bands before the sub-ADCs. For scaling to the full-scale input range of the sub-ADCs, set at 1 Vpp, an amplifier follows each LPF. Analog baseband outputs interface to off-chip sub-ADCs with a sampling rate of 500 MS/s. The overall effective sampling rate is 1.6 GS/s. For signal reconstruction, harmonic-rejection and image-rejection are performed in the digital domain. This is performed in a frequency-domain equalizer which also provides calibration of relative baseband gain and phase errors [10].

3.3.1 Main & Auxiliary LNTA

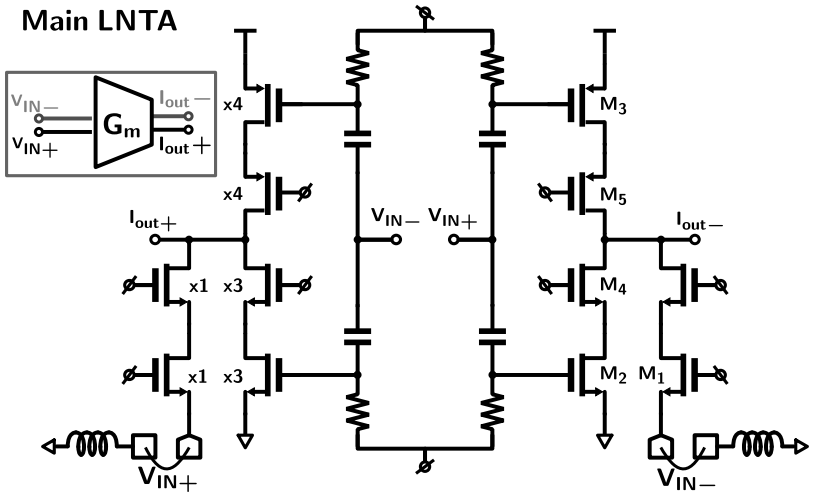
Fig. 3.5 shows the schematic of the main LNTA and auxiliary LNTAs. Considering a single-ended half-circuit of the main LNTA, a common-gate NMOS, M_1, provides input impedance matching with a 50-Ω source impedance, while an AC-coupled inverter-based amplifier, which consists of two common-source (CS) transistors is connected to the input node of opposite polarity [10, 16]. A cascode is used to desensitize the input matching to the transistor output resistance. The thermal noise of M_1 is canceled using the transconductance of M_2 and M_3. The half-circuit of each auxiliary LNTA consists of a current-reuse inverter-based amplifier, M_6 and M_7, connected to the input node. The CS devices in the main and auxiliary

path LNTAs are DC-biased using isolation resistors. The LNTAs are DC-coupled to the TIAs, and CMFB of the TIAs sets the DC level at the LNTA outputs.

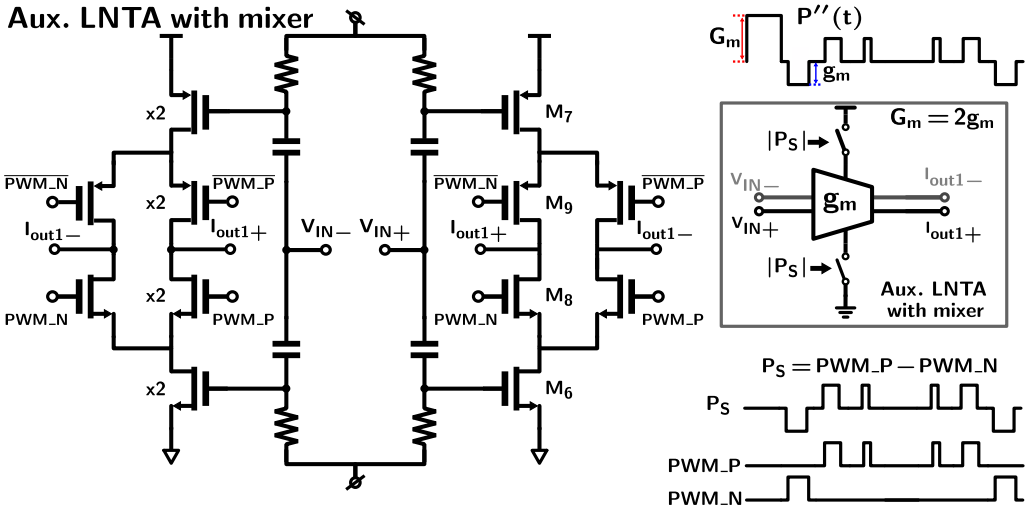
Cascode transistors, M_8 and M_9, in the auxiliary LNTAs are driven by the PWM-LOs, PWM_P and PWM_N, such that these LOs are not high in the same time-slot (Fig 3.5(b)). The current waveforms at the auxiliary LNTA outputs have the desired harmonic scaling used for sub-band gain-control. Auxiliary LNTAs operate only when the applied PWM-LO pulse is high. Thus, the total current consumption in auxiliary LNTAs is proportional to the PWM-LO duty cycle and varies with the degree of rejection or harmonic numbers because the duty cycle of the PWM-LO waveform can vary for different harmonic responses. By not employing static current in the transconductors, power dissipation is significantly reduced.

The achievable range of attenuation is determined by the minimum and maximum pulse-widths of the PWM symbols. The minimum pulse-width is set by the achievable pulse-width of a single symbol, while the maximum pulse-width is set by the minimum allowable time-gap between two adjacent symbols, at the mixer LO inputs.

In the design, the g_m of the auxiliary LNTAs is set to be half that of the main LNTA (Fig. 3.5(b)). This choice limits the minimum attenuation, for any combination of harmonics, to 5 dB, which corresponds to 1 bit of dynamic range of the sub-ADC, while placing a limit on the maximum attenuation to approximately 20 dB. Using the same transconductance in the auxiliary path as the main path would make the minimum achievable attenuation larger, and hence is not employed. Gain error between the auxiliary path and main path LNTAs is not critical since the



(a)



(b)

Figure 3.5: Schematics of (a) the main and (b) auxiliary low-noise transconductance amplifier (LNTA) with mixer

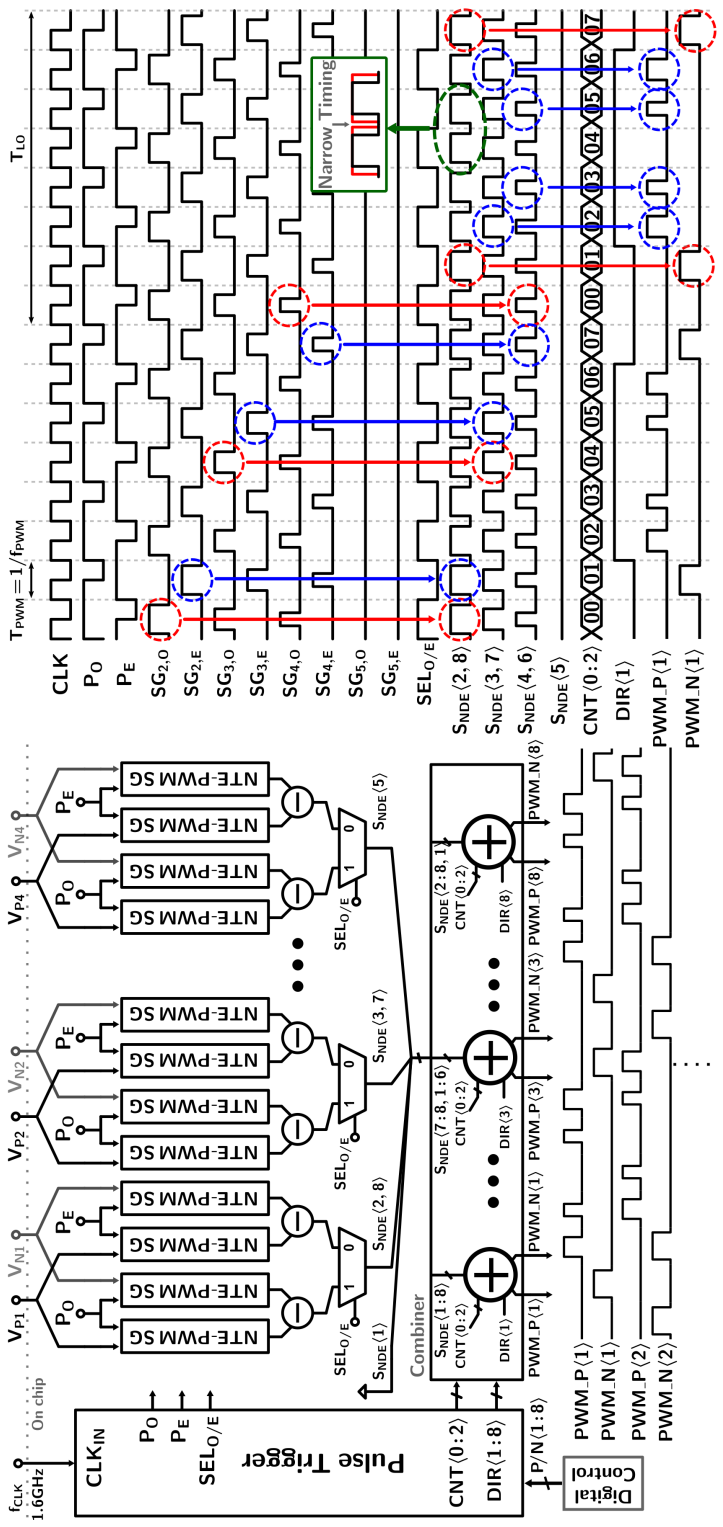


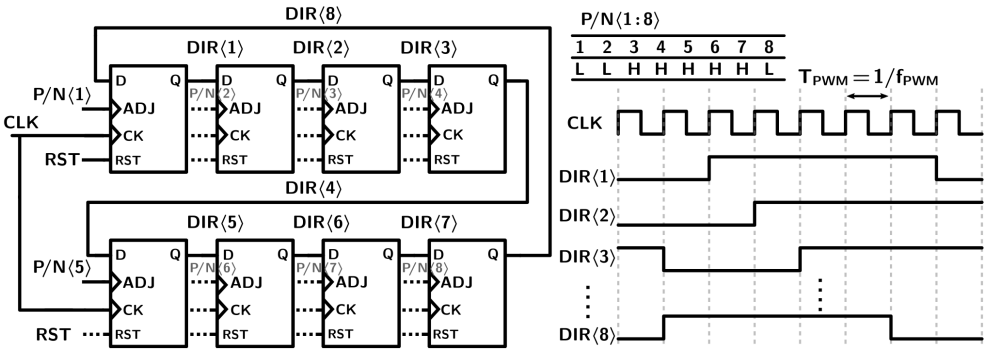
Figure 3.6: NDE-PWM generator, multi-phase PWM waveform synthesizer and PWM-LO timing diagram.

control of the PWM symbol pulse-widths (Fig. 3.6) can compensate for such error, to within the mismatch error range.

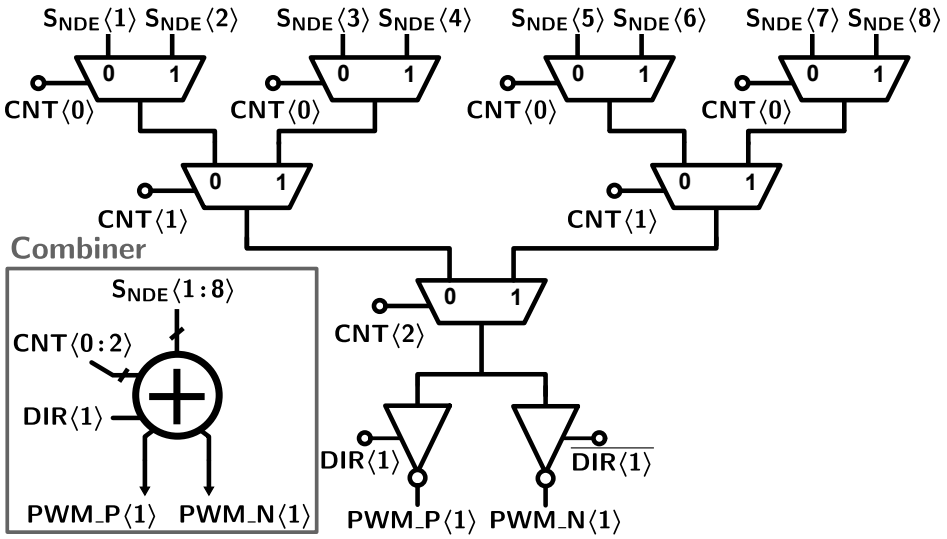
3.3.2 NDE-PWM generator and multi-phase PWM waveform synthesizer

NDE-PWM waveforms are employed to achieve the desired harmonic response in the auxiliary downconverter and are synthesized from two natural-sampling trailing-edge (NTE-PWM) signals generated in individual DLLs (Fig. 3.2) [30]. Only four NDE-PWM symbols are required for scaling a specific sub-band due to the symmetry of the PWM-LO pulses. A pair of reference voltages corresponding to the rising and falling edges of an NDE-PWM symbol (Fig. 3.6) is used to determine each NTE-PWM symbol's pulse-width. The DLL provides a linear relationship between the output pulse-width and the reference voltage. Thus four pairs of reference voltages, [V_{P1-4}, V_{N1-4}], are required for the synthesis of all the NDE-PWM symbols.

An NDE-PWM signal generator (NDE-PWM SG) consists of a pair of NTE signal generators (NTE-SG) and XOR gates, and provides an NDE-PWM symbol that has a pulse-width corresponding to the required gain coefficient (Fig. 3.2). Two half-rate NDE-PWM symbols ($SG_{k,O}$ and $SG_{k,E}$, $k \in \{2{:}5\}$) are employed to provide one full-rate NDE symbol (S_{NDE}) in order to avoid narrow timing between symbols, e.g., a harmonic profile may require a wide pulse-width, close to $T_{pwm} = 625ps$, which can lead to a narrow-pulse problem between consecutive symbols in the PWM generator. $SG_{k,O}$ and $SG_{k,E}$, which have a periodicity of $2T_{pwm}$ with a delay difference of T_{pwm}, are generated and merged by the multiplexer through



(a)



(b)

Figure 3.7: (a) DIR<1:8> generator (b) Combiner circuit for PWM_P<1> and PWM_N<1>.

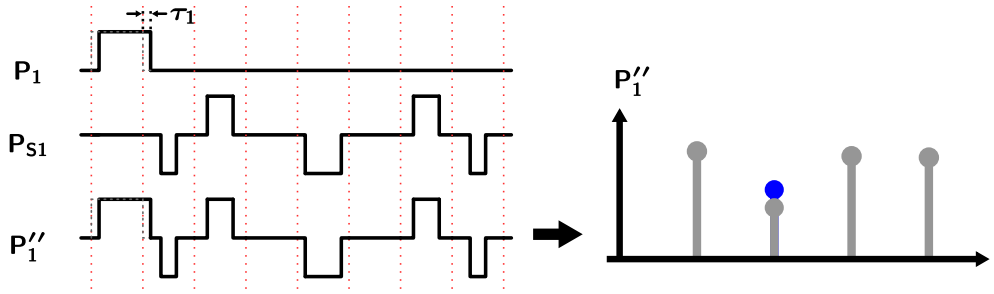


Figure 3.8: Phase error between the main rectangular waveform, $P(t)$, and the PWM-LO waveform, $P_s(t)$.

control line $SEL_{O/E}$ at a rate of $f_{pwm}/2$. Therefore, four pairs of NDE-PWM SGs generate seven NDE-PWM symbols, S_{NDE}<2:8>. S_{NDE}<1> is always low since this is the time-slot for the main pulse (P_{1-8} in Fig. 3.4).

The desired harmonic response is achieved through the sequence and timing of the NDE-symbols and their polarity. In the combiner, the signals CNT<0:2>, implemented by a 3-bit frequency counter, select the eight NDE-symbols, S_{NDE}<1:8>, corresponding to the eight paths, in sequence. The polarity of the symbols is determined by the signals DIR<1:8>. A shift register with eight flip-flops triggered by P/N<1:8> generates DIR<1:8> (Fig. 3.7(a)). The polarities of each NDE-PWM symbol, P/N<1:8>, are determined according to the desired harmonic scaling. Each combiner consists of seven multiplexers and two tri-state buffers (Fig. 3.7(b)). The eight combiners generate the final 8-phase PWM-LOs with a relative phase shift of 45° at the fundamental frequency between paths, PWM_P<1:8>, and PWM_N<1:8>, which are applied to auxiliary-path switches.

The effective LO waveform, P"(t), is implemented by combining the outputs of downconverters switched by pulse waveforms, P_{1-8}, and the PWM-LO

waveforms at baseband, for synthesizing the desired harmonic profile (Fig. 3.4). As shown in Fig. 3.8, phase error between the non-overlapping rectangular LOs, P_{1-8}, and the PWM-LOs, P_{S1-8}, can result in deviation from the desired harmonic response. This source of error is minimized at the design stage with proper layout matching and rigorous post-layout simulations. In addition, the phase error between P_1 and P_{S1} (Fig. 3.8) can be corrected with the control of reference voltages, which determine the pulse-width and position of the NDE-PWM symbols. Furthermore, a frequency-domain equalizer in the digital domain is also used to calibrate relative phase errors between multiple paths, through measurement of the undesired harmonic response.

3.3.3 Baseband design

Each baseband path is comprised of a transimpedance amplifier (TIA), a 6^{th}-order LPF, and a final gain-stage. Each TIA consists of an operational transconductance amplifier (OTA) with a single-pole RC filter. As shown in Fig. 3.4, the TIA combines the current-mode output of the main path and auxiliary path in each baseband path.

Maintaining a low input impedance of the TIA over the full sub-band bandwidth is necessary to minimize voltage swing at the input and output of the mixer switches. The OTA within the TIA thus needs to have a high gain and wide bandwidth to satisfy this requirement. An OTA with feed-forward compensation [36, 37] is employed due to its inherently wideband performance (Fig. 3.9). The first stage employs a telescopic transconductance stage to provide high gain. The second stage

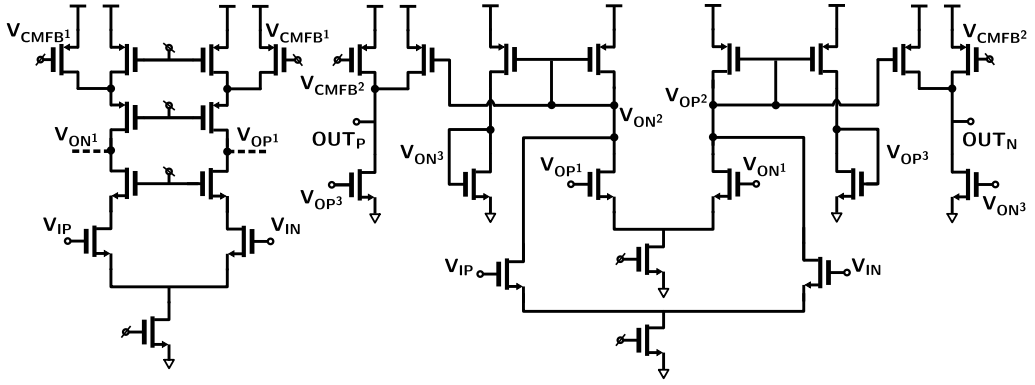


Figure 3.9: OTA with feed-forward compensation

is a current mirror transconductance, in combination with a class AB output stage. The feed-forward OTA provides 55 dB of open-loop gain and worst-case unity-gain frequency of 4 GHz over the process and voltage variation with a 1.3-V supply voltage, based on simulations.

A low pass filter (LPF) is used to obtain the desired signal-to-noise and distortion ratio (SNDR) by reducing the aliasing signal after sampling in the sub-ADCs. The LPF follows an implementation similar to that used in [10]. Three source-follower biquadratic cells [38] are employed to implement a 6^{th}-order response. These cells operate from a 2.5-V supply voltage to achieve high linearity. The source-follower based approach achieves good linearity due to its intrinsic feedback, and the positive feedback allows the synthesis of the complex pole through transconductance in the MOS device.

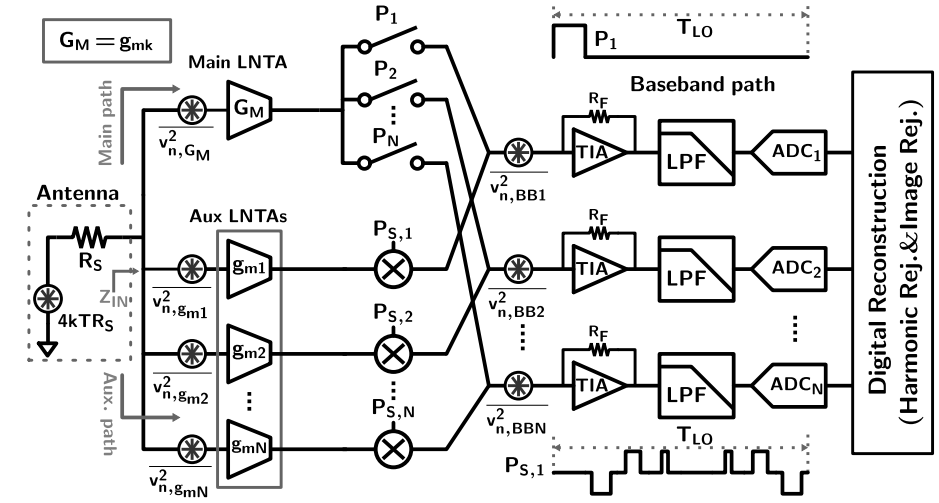
A buffer which also employs a source-follower is placed after the 6^{th}-order LPF to provide low output impedance and DC level-shift of the filter output voltage for driving the final gain-stage. The final gain-stage consists of an OTA with resis-

tive feedback, and operates from a 1.3 V supply to scale the output voltage range to match the input range of the sub-ADCs. The full-scale differential output voltage of the IC is 1 Vpp. The TIA and the final gain stage also have a low-pass frequency response due to a high-frequency pole.

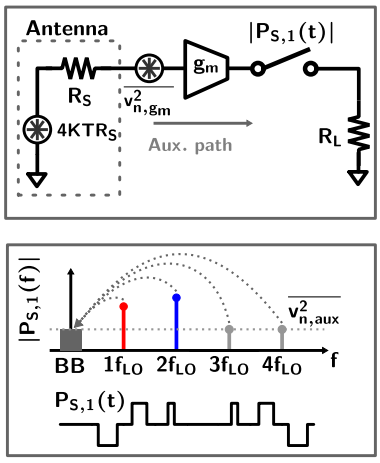
In this work, an oversampling ratio of 2.5 is used, as the bandwidth of each sub-band is 100 MHz, and the sampling rate of the external sub-ADCs is 500 MS/s. The simulated frequency response in the overall filter shows a 3-dB bandwidth of 100-MHz with 66 dB of rejection at 400 MHz. As pointed out in [20], the oversampling ratio, or the order of the filter can be significantly reduced by employing digital-domain calibration.

3.4 Noise analysis

The noise performance of the receiver is analyzed in this section. The analysis identifies the primary noise contributors, and highlights the noise variation that arises as a result of gain variation in the receiver, in response to the PWM-LO signals. The three major noise sources in the signal path include the noise of the main path, the auxiliary path, and the baseband path after mixing (Fig. 3.10(a)). The noise sources of the main-path LNTA and those of the auxiliary LNTAs are modeled by equivalent input-referred voltage sources, $\overline{v_{n,G_M}^2}$ and $\overline{v_{n,g_{mk}}^2}, k \in \{1,2,\cdots,N\}$, respectively. The baseband noise source in a single path, $\overline{v_{n,BB}^2}$, includes noise originating from noise sources in circuits after mixing and downconversion, such as the TIA, the LPF, and the baseband sub-ADC. The noise of the NDE-PWM generator is not explicitly analyzed, but is similar to that shown in [30].



(a)



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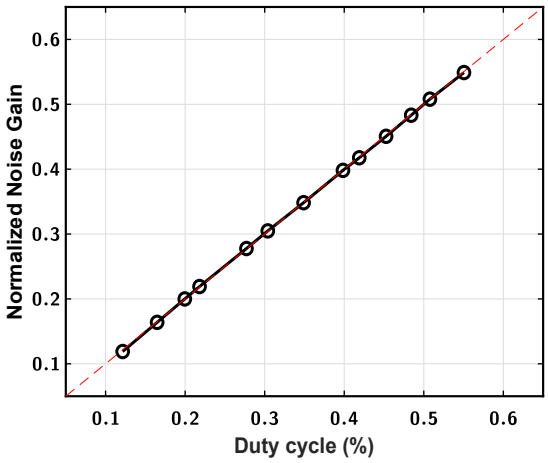


(c)

Figure 3.10: (a) Simplified noise sources in the spectrum channelizer. (b) Simplified single auxiliary path for noise analysis (c) Noise folding gain in single auxiliary path as a function of total on-state duty cycle of a PWM-LO waveform.

3.4.1 Main path noise

The noise of the main path, $\overline{v^2_{n,main}}$, (Fig. 3.10(a)), is modeled by the noise source, $\overline{v^2_{n,G_M}}$ which accounts for all noise sources within the main LNTA. The FF-ADC downconverts and aliases the input noise from around all LO harmonics of the non-overlapping multi-phase rectangular LOs, $P_q(t)$, to each baseband path. The LO waveforms are periodic with the time period, T_{LO}. The input spectrum of the pulse-train, $P_q(t)$, in each of the N paths, is given by

$$P_q(f) = \sum_{n=-\infty}^{\infty} \frac{sin(\frac{n\pi}{N})}{n\pi} \delta(f - nf_{LO}) e^{-j\left(\frac{n\pi}{N}(2q-1)\right)} \tag{3.1}$$

where q is the path number and n is the harmonic number. Therefore, the front-end noise around all LO harmonics is scaled by $sin(n\pi/N)/(n\pi)$ and is translated to each baseband path. Harmonic and image rejection in the digital domain is employed to extract specific sub-bands. This also rejects noise folding from other sub-bands to that sub-band after mixing. Thus the only noise in a selected sub-band originates from that sub-band and its aliased harmonics from around mNf_{LO}. The noise folding due to mixing then depends on the 3-dB bandwidth of the main LNTA's output and the selected downconversion harmonic number. The total noise power of multi-phase rectangular pulses, $P_q(t)$, at the channelizer output through the FF-ADC main path is given by [10],

$$\overline{v^2_{n,out,main}(n)} = \overline{v^2_{n,main}} T^2_{n,main}(n) \tag{3.2}$$

where the noise folding factor of the FF-ADC main path, $T_{n,main}$, is given by

$$T^2_{n,main}(n) = \left[\left| \frac{sinc(\frac{n\pi}{N})}{1+j\left(f_s n/N f_{FE,3dB}\right)} \right|^2 + \sum_{m=1}^{\infty} \left\{ \left| \frac{sinc\left(\frac{(Nm+n)\pi}{N}\right)}{1+j\left(\frac{f_s(Nm+n)}{N f_{FE,3dB}}\right)} \right|^2 + \left| \frac{sinc\left(\frac{(Nm-n)\pi}{N}\right)}{1+j\left(\frac{f_s(Nm-n)}{N f_{FE,3dB}}\right)} \right|^2 \right\} \right] \tag{3.3}$$

where n is the selected downconversion harmonic number and $f_{FE,3dB}$ is the 3-dB bandwidth of the LNTA output.

3.4.2 Auxiliary-path noise

The auxiliary path consists of N independent LNTAs with uncorrelated noise, unlike the main path, where the noise source of the main-path LNTA is steered through N switches. The noise of the k^{th} LNTA is modeled by an equivalent input-referred noise voltage source, $\overline{v^2_{n,g_{mk}}}$. The auxiliary LNTA noise is switched by a PWM-LO, whose spectral response is determined by the desired sub-band amplitude scaling.

Consider a single auxiliary path as shown in Fig. 3.10(b). The spectrum of the PWM-LO, $P_{s,q}(t)$, applied to the q^{th} auxiliary path switch, is given by

$$P_{s,q}(f) = \sum_{n=-\infty}^{\infty} p_n \delta(f - n f_{LO}) \tag{3.4}$$

where p_n is n^{th} Fourier series coefficient of the PWM-LO waveform, $P_{s,q}(t)$. The auxiliary-path noise, $\overline{v^2_{n,aux}}$, around the n^{th} harmonics of the PWM-LO is scaled by $|p_n|^2$ and translated to baseband. We assume that the PWM-LO waveform is

periodic with the time period, T_{LO}, and $P_{s,q}(t)$ ideally switches between "0" and "1". Ignoring the frequency response at the output of the auxiliary path LNTAs for simplicity, and applying Parseval's theorem, the noise power, $\overline{v^2_{n,BB,aux}}$, which is translated to baseband by the action of the PWM-LO in each of the N auxiliary paths, is given by

$$\overline{v^2_{n,BB,aux}} = \overline{v^2_{n,aux}} \sum_{n=-\infty}^{\infty} |p_n|^2 = \triangle \overline{v^2_{n,aux}} \tag{3.5}$$

where

$$\sum_{n=-\infty}^{\infty} |p_n|^2 = \frac{1}{T_{LO}} \int_0^{T_{LO}} p_s(t)^2 dt = \triangle$$

$\triangle$ is the total duty cycle of the PWM-LO, $P_{s,q}(t)$, that is the total fraction of time for which the PWM-LO is in a high state, regardless of the exact shape of the PWM-LO waveform. Since we ignore the frequency response at the LNTA output, the above expression for noise is an upper-bound. The impact of finite frequency response is considered below in Section 3.4.3. The simulated noise folding gain in a simplified single auxiliary path, for PWM-LO waveforms with various duty cycles for single or multiple harmonic gain scaling factors is plotted in Fig. 3.10(c), assuming the input impedance is matched ($R_S = 1/g_m$) and considering only the front-end noise sources ($4KTR_s$ and $\overline{v^2_{n,g_{mk}}}$). As shown, the noise-folding gain is linear with the total PWM-LO duty cycle as predicted by (3.5).

Since the noise from the multiple auxiliary paths is not correlated, each path's noise adds in power even after applying harmonic and image rejection after digitization. The noise arising due to combination of N auxiliary paths is scaled

by $N/2$ when considering harmonic rejection. Considering the noise from I and Q paths, due to image rejection, the total output noise power, when folded to baseband, from N auxiliary paths, is given by

$$\overline{v_{n,out,aux}^2} = \overline{v_{n,BB,aux}^2} \sum_{k=1}^{N} (a_{k,i}^2 + a_{k,q}^2) = N \triangle \overline{v_{n,aux}^2} \tag{3.6}$$

where the quadrature harmonic rejection coefficients are explicitly identified, and are given by $a_{k,i} = cos(\frac{2\pi kn}{N})$ and $a_{k,q} = sin(\frac{2\pi kn}{N})$, where n is the selected harmonic number and k is the path number.

3.4.3 Total noise

In the FF-ADC, each sub-band output in the digital domain results from a linear combination of the outputs of baseband paths and sub-ADCs after the mixer stage. Therefore, any noise originating from the mixer switches, baseband paths, and sub-ADCs must be considered. The noise of the mixer switches will not contribute significantly to the output noise since the output impedance of both the main and auxiliary LNTAs is high, and the mixer switches are current-mode.

In Fig. 3.10(a), a baseband input-referred voltage source, $\overline{v_{n,BB}^2}$, in each baseband path includes noise sources arising from the transimpedance amplifier (TIA), the LPF, and the sub-ADC. The baseband noise, $\overline{v_{n,BB}^2}$, is injected in each baseband path after the mixer stage and hence adds in power since noise in each of the N baseband paths is uncorrelated [10]. The total output noise power is given by

$$\begin{aligned}\overline{v_{n,out,tot}^2(n)} &= \overline{v_{n,out,main}^2(n)} + \overline{v_{n,out,aux}^2} + \overline{v_{n,out,BB}^2} \\ &= \overline{v_{n,main}^2} T_{n,main}^2(n) + \overline{v_{n,aux}^2} T_{n,aux}^2 + N\overline{v_{n,BB}^2}\end{aligned} \tag{3.7}$$

where the noise folding factor of the auxiliary paths, $T_{n,aux}$, is given by

$$T_{n,aux}^2 = N\left(\sum_{n=-\infty}^{\infty} \left|\frac{p_n}{1+j\left(n\frac{f_{LO}}{f_{FE,aux,3dB}}\right)}\right|^2\right) \tag{3.8}$$

where $f_{FE,aux,3dB}$ is the 3-dB bandwidth of the auxiliary LNTAs' outputs. The noise folding factors are dependent on the input LNTA's 3-dB bandwidth and the harmonic response of the PWM-LO for the chosen harmonic gain-scaling. In this work, the 3-dB bandwidths of the main and auxiliary LNTAs are estimated to be 1.5 GHz and 1.2 GHz, respectively, based on simulations. The front-end noise folding gain, $T_{n,main}^2 + T_{n,aux}^2$, of an 8-path channelizer with input LNTAs (main and auxiliary) with finite 3-dB bandwidth and identical transconductance ($G_M = g_{mk}$, $k \in [1:8]$) is plotted in Fig. 3.11(a). Since the filtering at the LNTA outputs reduces the noise folding from higher harmonics, the front-end noise from auxiliary paths that folds into the output is monotonically, but not linearly, dependent on the duty cycle of the PWM-LOs. Fig. 3.11(a) shows the comparison of noise folding gain due to PWM-LOs with different duty cycles for attenuation of 20-dB for a single harmonic from $1f_{LO}$ to $4f_{LO}$. Compared to no gain-scaling, noise impact from the auxiliary path increases with the total duty cycle of the PWM-LO.

Considering only the front-end gain, the conversion gain of the channelizer is given by

$$A_v(n) = g_m R_F \left(sinc\left(\frac{n\pi}{N}\right) + \kappa(n) \right) \tag{3.9}$$

where R_F is the feedback resistor at the TIA and $\kappa(n)$ is the total gain of the N auxiliary paths at baseband from harmonic n, and is proportional to p_n. $\kappa(n)$ can be positive or negative depending on the desired harmonic response of the PWM-LO. Fig. 3.11(b) shows the front-end conversion gain without gain-scaling and with gain-scaling of -20-dB at $1f_{LO}$ to $4f_{LO}$ normalized to the gain of sub-band 1 without gain-scaling. The conversion gain at the unattenuated sub-band with gain-scaling, that is with the PWM-LO turned on, is higher than without gain-scaling, that is with the auxiliary completely off, since the auxiliary downconverter can translate the signal from unattenuated sub-bands to baseband depending on harmonics of the PWM-LO with positive p_n and hence $\kappa(n)$. Assuming that the input impedance is matched, and considering only the front-end conversion gain, from (3.7)-(3.9), the double-sideband NF of the front-end in the n^{th} sub-band can be shown to be

$$\begin{aligned} \mathrm{NF}(n) &= \frac{SNR_i}{SNR_o} \\ &= 1 + \frac{(\frac{4kT\gamma}{g_m})(T_{n,main}^2(n) + T_{n,aux}^2) g_m^2 R_F^2}{2kTR_s A_v^2(n)} \\ &= 1 + \frac{(\frac{4kT\gamma}{g_m})(T_{n,main}^2(n) + T_{n,aux}^2)}{2kTR_s \left(sinc\left(\frac{n\pi}{N}\right) + \kappa(n) \right)^2}. \end{aligned} \tag{3.10}$$

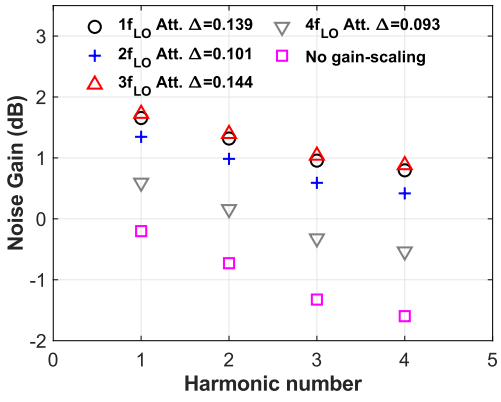
The noise figure (3.10) for $g_m = 20ms$, and $\gamma \approx 1$ is plotted in Fig. 3.11(c), without gain-scaling and with gain-scaling of -20 dB. The noise figure in the sub-bands with the attenuation increases significantly while the noise figure in the unat-

tenuated sub-bands with gain-scaling is lower (auxiliary path ON) than no gain-scaling (auxiliary path OFF) because the relative increase in the conversion gain is higher than the relative increase in the noise gain due to the auxiliary downconverter for the two cases, as shown in Fig.3.11(a)-(b).

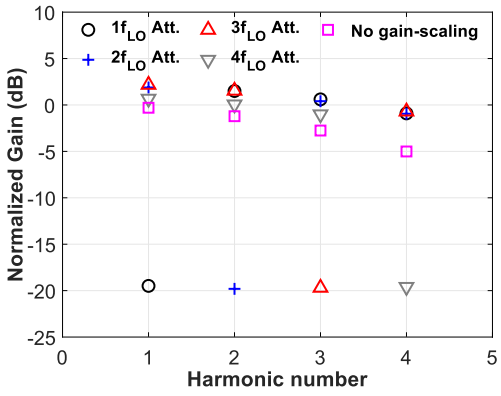
The above noise figure simulation is for purpose of highlighting the impact of $\kappa(n)$ on the noise figure. It assumes that the g_m of the auxiliary path devices, and hence the input referred noise, is identical to those of the main-path, and also ignores the baseband noise, which adds in a similar form to the auxiliary path noise.

3.5 Supervised learning for determination of NDE-PWM edges

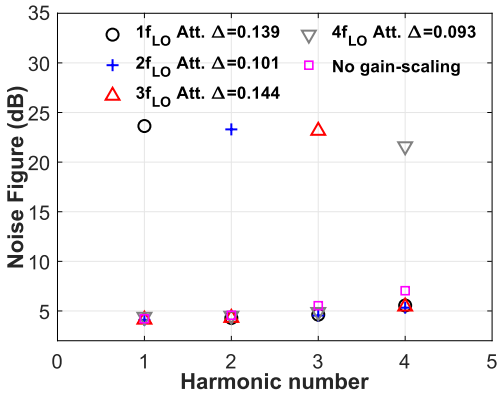
The rising and falling edges of the NDE-PWM waveforms determine the PWM-LO harmonic response. Estimating the NDE-PWM edges and duty-cycles through proportional scaling from the gain coefficients employed in [22] does not provide an accurate harmonic response. The function that relates harmonic amplitudes to the edges of the PWM-LO symbols is strongly non-linear, and the reverse function is non-trivial to derive. For example, Fig. 3.12 shows LO waveforms for single harmonic scaling from $1f_{LO}$ to $4f_{LO}$. Discrete-level waveforms that are synthesized using gain coefficients and provide 20 dB attenuation for a single harmonic, while providing equal gain at other harmonics are shown in Fig. 3.12(a). The gain coefficients are determined by applying an inverse FFT operation on the desired frequency-domain LO spectrum. PWM-LO waveforms are also shown, where the rising and falling edges and duty-cycles of the waveforms are set in proportion to the gain coefficients (Fig. 3.12(b)). However, it is observed that the LO



(a)



(b)



(c)

Figure 3.11: (a) Front-end noise folding with 3-dB bandwidth of LNTAs. (b) Normalized conversion gain and (c) Noise figure without gain-scaling and with single harmonic gain scaling from $1f_{LO}$ to $4f_{LO}$.

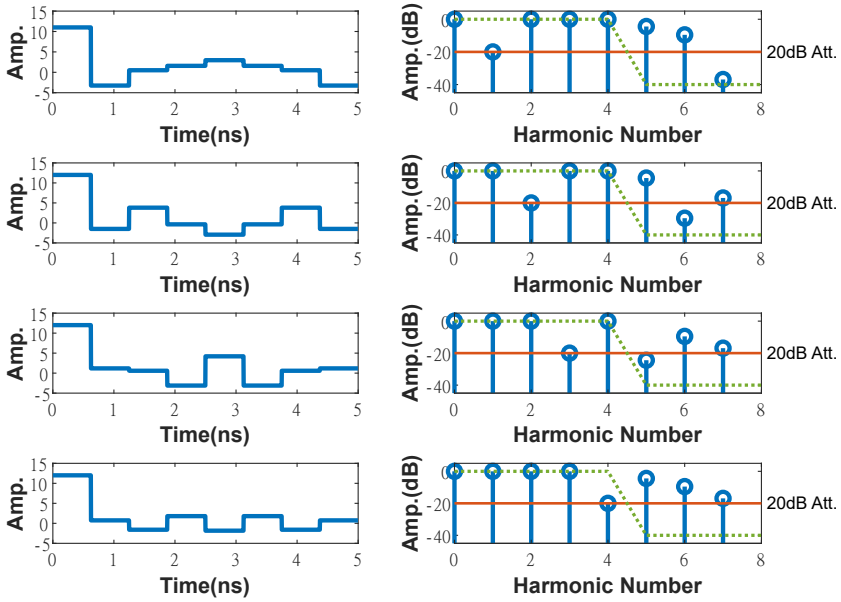
spectrum is different from that of Fig. 3.12(a). Further, the error across the different cases is inconsistent. To obtain an arbitrary desired harmonic response, analytically determining the PWM symbol's rising and falling edges is thus challenging. This work experimentally verifies a neural-network based supervised learning approach to rapidly estimate the rising and falling edges of the PWM-LO waveform for achieving specified harmonic responses (Fig. 3.13), as originally proposed in [31].

3.5.1 Neural networks based supervised learning

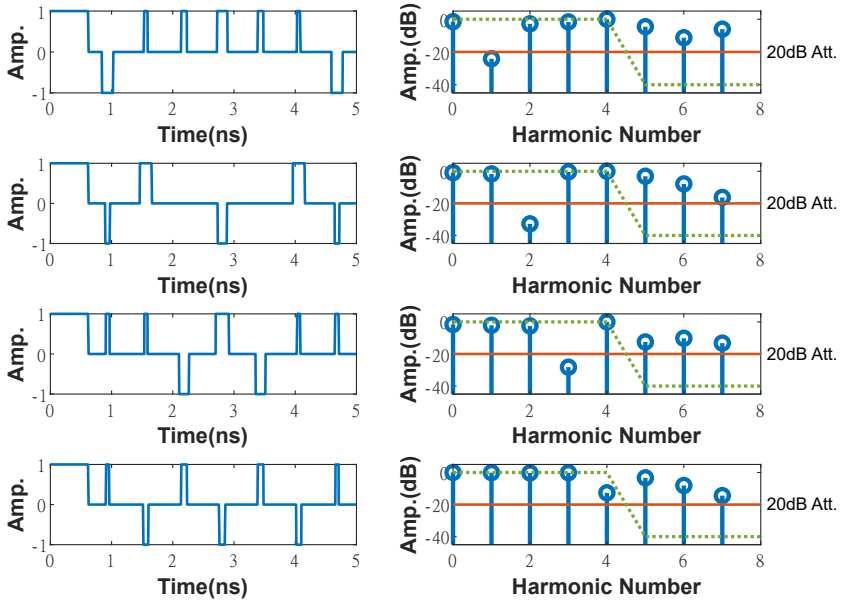
Supervised learning is a widely used machine learning algorithm. It produces a model to map a set of inputs to an output set by training neural networks with a known data set consisting of labeled examples, and the corresponding correct output set. The model created from the training data set can predict the output for an arbitrary input. Fig. 3.13 shows supervised learning for mapping from harmonic response to PWM symbols. For an arbitrary harmonic response, the effective LO waveform $P"(t)$, with the time period T_{LO}, is given by

$$P''(t) = \sum_{k=-\infty}^{\infty} C_k e^{jk\omega_o t} \tag{3.11}$$

where k is the harmonic number, and ω_o is $2\pi/T_{LO}$. The input data and the output data to the neural networks are amplitudes of harmonics, C_k, and the NDE-PWM symbol's transition edges (P_k, N_k) for the given harmonic amplitude, respectively. The index k varies from 1 to $N/2$ due to the symmetry of the PWM-LO pulses. The NN model mapping the input and output can be represented by



(a)



(b)

Figure 3.12: LO waveforms for single harmonic scaling from $1f_{LO}$ to $4f_{LO}$ ($N = 8, T_{LO} = 5ns$) (a) using a discrete-level waveform with gain coefficients (b) using PWM-LO with proportionally-scaled NDE-PWM edges and duty-cycles

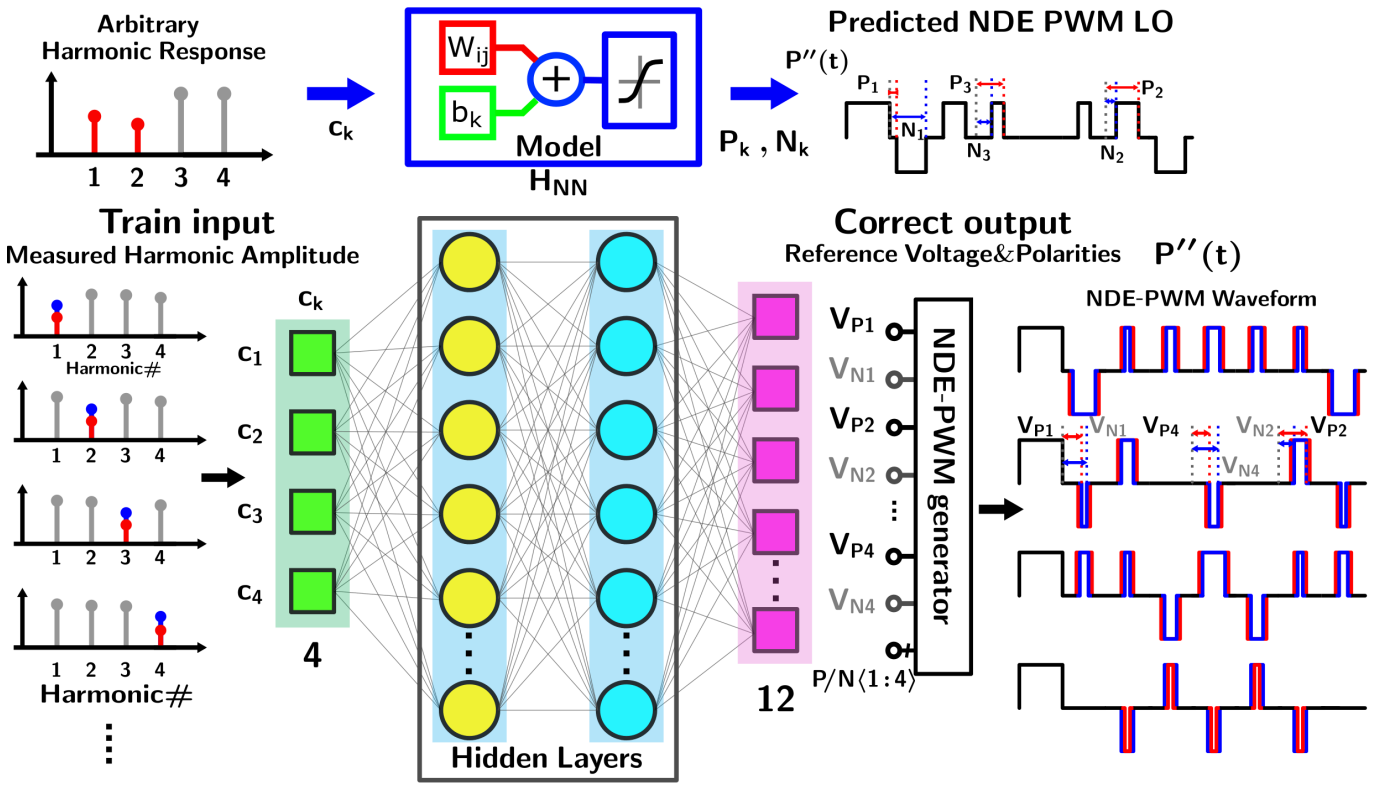


Figure 3.13: Supervised learning with neural networks for creating the mapping from harmonic levels to the PWM-LO waveform ($P''(t)$).

$$\{P_k, N_k\} = H_{NN}(C_k) \tag{3.12}$$

where $H_{NN}(\cdot)$ indicates the NN model. We employ feedforward neural networks (FFNN), which consists of 2 hidden layers with 12 neurons in each layer, as shown in Fig. 3.13. The NN model, can predict the NDE-PWM symbol's rising and falling edges after training for a desired LO harmonic amplitude.

3.5.2 Prediction of NDE-PWM edges with supervised learning

Each reference voltage applied to the DLLs indicates a rising or falling edge of an NDE-PWM symbol. PWM-LO waveforms with the desired harmonic response drive the auxiliary downconverter.

The datasets for training consist of the harmonic amplitudes from $1f_{LO}$ to $4f_{LO}$ at the output of the spectrum channelizer, and the corresponding 8 reference voltages $V_{P,k}$ and $V_{N,k}$ applied to the DLL and four polarities. Polarities $P/N(k)$ are determined by the difference of reference voltages, e.g., whether $V_P > V_N$ is high or $V_P < V_N$ is low. P/N<1:4> are employed in output datasets due to their symmetry (Fig. 3.7(b)). The NN model in (3.12) can be re-written as follows:

$$\{V_{P,k}, V_{N,k}, P/N(k)\} = H_{NN}(C_k), \qquad k \in [1 : N/2] \tag{3.13}$$

For off-chip learning, pre-determined sets of reference voltages and polarities, V_{P1-4}, V_{N1-4}, and P/N<1:4>, are applied to NDE-PWM SGs for single or multiple harmonic rejection cases. Input tones with the equal amplitudes are injected

at 10 MHz offset from each harmonic frequency, that is at 190 MHz, 390 MHz, 590 MHz, and 790 MHz. Harmonic amplitudes, C_k, are measured at each sub-band output. This is used to generate a training dataset for the neural network. The NN model can be iteratively optimized using backpropagation, while minimizing the mean-square-error (MSE) function.

For synthesis of a PWM-LO that provides a desired harmonic response, the harmonic amplitude levels are applied as inputs to the NN model that results from the above training. The NN provides as its output, the reference voltages and polarities that need to be applied to the NDE-PWM signal generators. The accuracy of the NN model using off-chip learning is shown in Section 3.6.

While off-chip learning is employed here, the neural network can be implemented on-chip as well, if required. In this case, the network can also be used to calibrate harmonic response with variations in supply voltage, bias currents and temperature. This work demonstrates the utility of neural networks in a signal processing application, where it is used as an interpolator. Future work in this area can include further optimization of the neural network architecture and parameter space, and comparison of computational complexity to other potential approaches for estimating the PWM waveforms.

3.6 Measurement results

The 1.6 GS/s channelizer is implemented in a 65-nm CMOS process, and has an active area of 0.5 mm^2 (Fig. 3.14). An external RF balun provides differential input to the LNTAs. The design includes the LNTAs, downconverters,

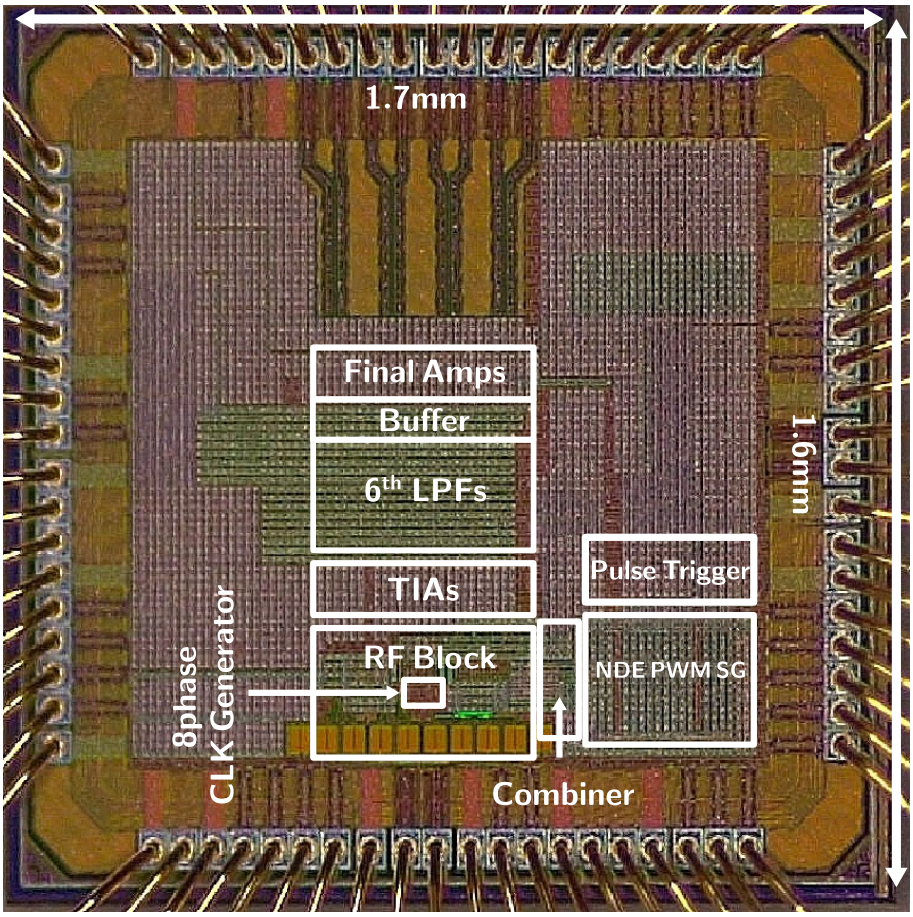


Figure 3.14: Microphotograph of the die.

baseband filters, TIAs, buffers, and the NDE-PWM generator. Four off-chip sub-ADCs digitize four analog outputs with 14-bit resolution, 64-dB SNR, and 75-dB spurious-free dynamic range (SFDR). After digitization, HR and IR are used to separate lower and upper sidebands around each harmonic. Amplitudes of 4 LO harmonics at 200*k MHz ($k \in [1:4]$) are controlled, and the channelizer spans 100 to 800 MHz, with a sub-band bandwidth of 100 MHz (Fig. 3.15). The measured S11 is lower than -10-dB from 100-800 MHz. The total power consumption is

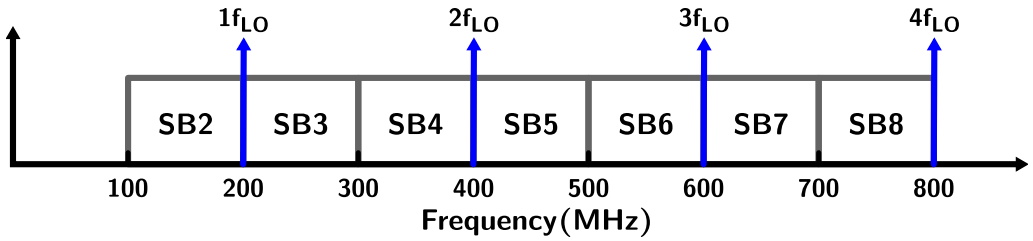


Figure 3.15: Channelization of the input spectrum.

Table 3.1: Current consumption breakdown

	Main LNTA	TIA+FG (a)	6^{th}LPF (a)	Aux. LNTAs	Digital (b)
Current (mA)	14	46	17	0 / 5-24(c)	10 / 22-32(c)
Supply (V)	1.3	1.3	2.5	1.3	1.3

(a) Total current for four baseband paths
(b) Includes the master clock input buffers and digital interface controls
(c) the minimum and maximum current consumption for single or multiple harmonic attenuation case

133.5 mW, without gain scaling, and up to 193.3 mW with gain-scaling, reflecting the variation in power consumption in the auxiliary LNTAs and the NDE-PWM SG with harmonic gain-scaling (Table 3.1). Higher current consumption is observed in the eight auxiliary LNTAs when gain-scaling is applied, since this requires wider PWM-LO pulse-widths. Likewise, the current consumption in the digital section varies with the number of NDE-PWM symbols for single or multiple harmonic attenuation.

Four pairs of external reference voltages, $V_{P,k}$ and $V_{N,k}$, which correspond to the desired harmonic scaling, are applied to the DLLs, and the multi-phase PWM-LOs generated in response are used to drive the auxiliary LNTAs. By controlling external analog reference voltages, LO harmonics for specific sub-bands can be controlled from -20 to -5 dB. Fig. 3.16 shows the gain and NF measurements with-

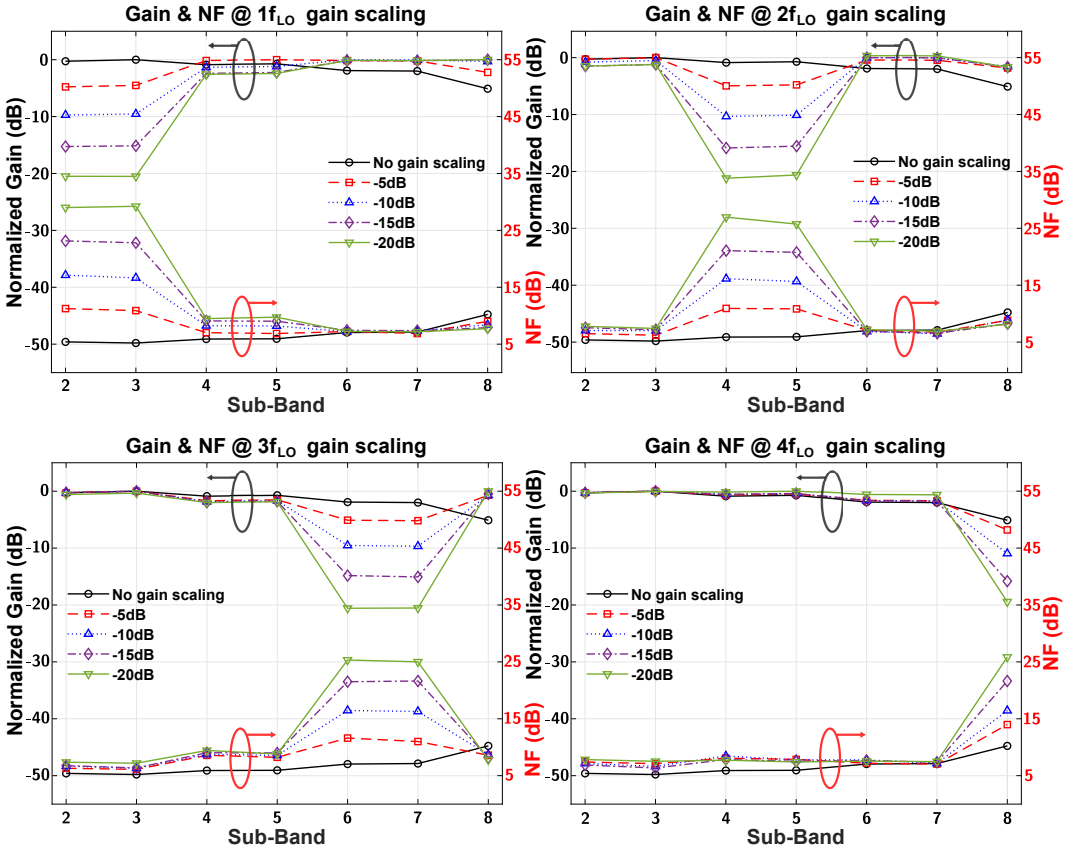
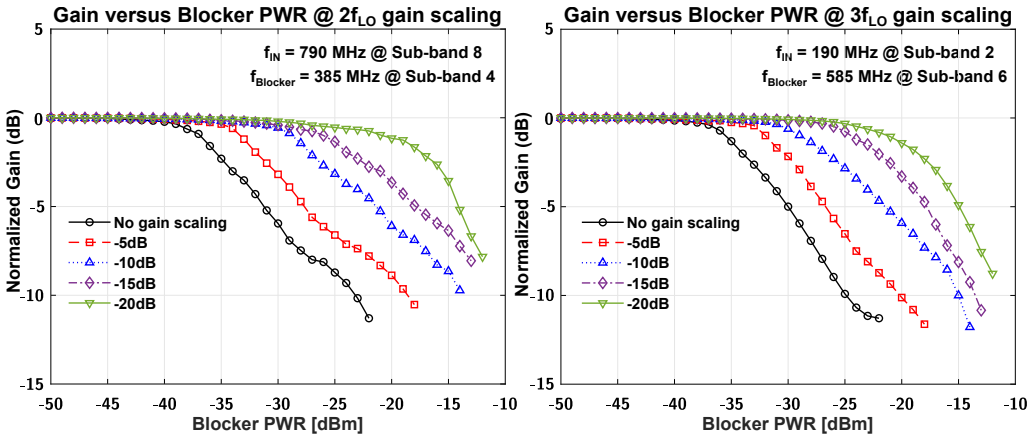


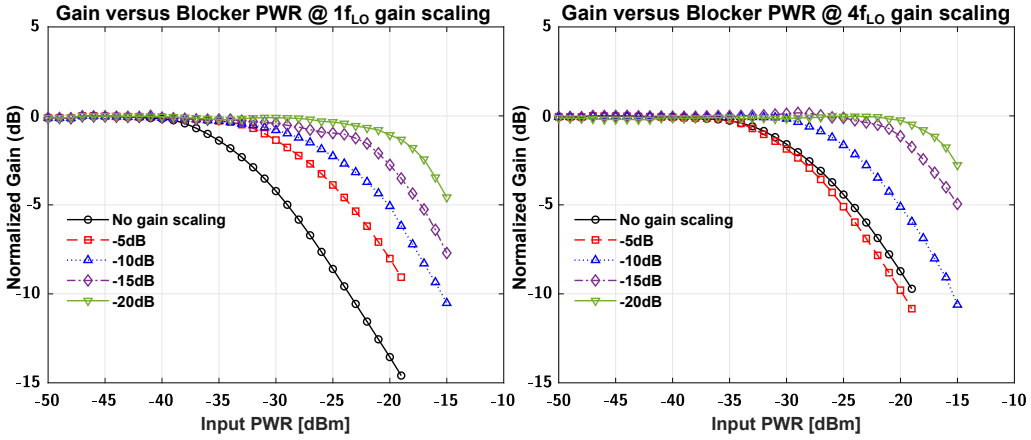
Figure 3.16: Measurement of gain and NF without gain-scaling and with single harmonic scaling from $1f_{LO}$ to $4f_{LO}$.

out gain-scaling and with single harmonic gain-scaling with 5 dB steps from $1f_{LO}$ to $4f_{LO}$. A voltage gain of 51.6-56.5 dB is measured without gain-scaling across sub-bands while voltage gain is 37-59 dB with single harmonic gain-scaling in all sub-bands (Table 3.2). The auxiliary paths are also employed for sinc-roll-off compensation, which increases the gain at higher harmonics.

The full-scale input-level of the spectrum channelizer was determined by the signal amplitude required for a 1 Vpp baseband output in sub-band 2. The



(a)



(b)

Figure 3.17: (a) Measured gain vs. blocker power with gain-scaling for $2f_{LO}$ and $3f_{LO}$ (f_{in} = 790 MHz and $f_{Blocker}$ = 385MHz; f_{in} = 190MHz and $f_{Blocker}$ = 585 MHz). (b) Gain compression in-band with gain-scaling for $1f_{LO}$ and $4f_{LO}$ (f_{in} = 190 MHz and f_{in} = 790 MHz).

noise figure is calculated in the digital domain by considering the noise floor after digitization, and application of HR and IR. NF of 5.2-10.3 dB is observed without gain-scaling. As explained in Section 3.4, noise impact from the auxiliary LNTAs is proportional to the duty cycle of the PWM-LOs and sinc-roll-off compensation increases gain at higher harmonics. The NF in unattenuated sub-bands varies from 6.1-9.7 dB while NF in the sub-bands increases with attenuation, e.g., to 29.2 dB with 20-dB attenuation in sub-band 2.

Fig. 3.17(a) shows the gain versus blocker power with 5 to 20-dB attenuation, respectively. Using the PWM-LOs, gain-scaling over this range at a specific harmonic improves the blocker compression in an unattenuated sub-band. With -20-dB gain-scaling of $2f_{LO}$, blocker compression in sub-band 8 improves from -34 dBm to -16 dBm, where the blocker is applied in the sub-band corresponding to $2f_{LO}$. With -20-dB gain-scaling of $3f_{LO}$, 16 dB improvement in sub-band 2 is observed for the blocker in the sub-band corresponding to $3f_{LO}$. Fig. 3.17(b) shows the in-band gain compression (P_{1dB}) with gain-scaling of -20 to -5 dB for $1f_{LO}$ and $4f_{LO}$. Due to gain-scaling, P_{1dB} increases from -36 dBm to -20 dBm, and from -32 dBm to -17 dBm at sub-band 2 and 8, respectively.

Off-chip learning employing a neural network is used to estimate the reference voltages and polarities (V_{P1}, V_{N1},$\cdots$, V_{P4}, V_{N4}, P/N<1:4> in Fig. 3.13), which are applied to the NDE PWM-LO signal generators for setting desired LO harmonic levels. Validation of the prediction accuracy of the NN model is performed through physical measurement of the harmonic spectrum at the output. Fig. 3.18 shows four examples of target and measured harmonic levels of the LO waveforms, generated

Table 3.2: Performance summary and comparison

	This work		JSSC'14	JSSC'19	JSSC'21	JSSC'18
	w/o gain-scaling	**with gain-scaling**	[10]	[32]	[39]	[8]
Freq (MHz)	**100 ~ 800**		125 ~ 1000	500 ~ 3000	300 ~ 1300	0 ~ 1000
Architectures	**FF-ADC based Channelizer**		FF-ADC	Harmonic Selective(1) Receiver	Carrier Aggregation(10) Receiver	Direct Sampling ADC
Gain (dB)	**56.5 ~ 51.6**	**59 ~ 37**[2]	43.3 ~ 38	42	46.7	0
f_S (GS/s)	**1.6**		2	-	-	1.6 / 3.2 / 6.4
Sub-band BW (MHz)	**100**		125	20[3]	7 ~ 33	-
NF (dB)	**5.2 ~ 10.3**	**6.1 ~ 29.2**	8.5 ~ 13.4	2.4 ~ 5	4.6 ~ 5.9[11]	-
IIP3 (dBm)	**-24 ~ -19**	**-21 ~ -10**[4]	-4.2 ~ +3.5	+4	-12.1	-
HR / IR (dB)	**>58 / >60**[5][9]	**>55 / > 57**[5][9]	>59 / >58[5]	>78[6] (HR)	>51.7[12]	>72.1 @ 1.6 GS/s (SFDR)
B_{cp} (dBm)[7]	**-34**	**-16**	-	-10	-8.4[11]	-
Power (mW)	**133.5**	**155.6 ~ 193.3**[8]	104	28 ~ 31	107.6[11]	40.7 / 120.6 / 225
Active area (mm^2)	**0.5**		0.35	1.2	1.8	0.9 @ 1.6 GS/s
Technology	**65 nm**		65 nm	28 nm	65 nm	65 nm

(1) Demonstration up to 3 sub-bands concurrently; (2) Maximum and minimum gain with single harmonic gain-scaling in all sub-bands; (3) Bandwidth for measuring receiver gain and NF; (4) IIP3 with gain-scaling for $1 f_{LO}$ of -5-dB with two tones, 189.5 MHz and 190.5 MHz / $4 f_{LO}$ of -20-dB with two tones, 789.5 MHz and 790.5 MHz; (5) HR, IR are harmonic rejection and image rejection in the digital domain; (6) With digital calibration; (7) Blocker 3-dB compression point; (8) Minimum and maximum power consumption with gain-scaling; (9) Limited by analog MUX; (10) Provides 2 band aggregation in high-sensitivity mode; (11) Dual-carrier-reception; (12) Sideband rejection with calibration.

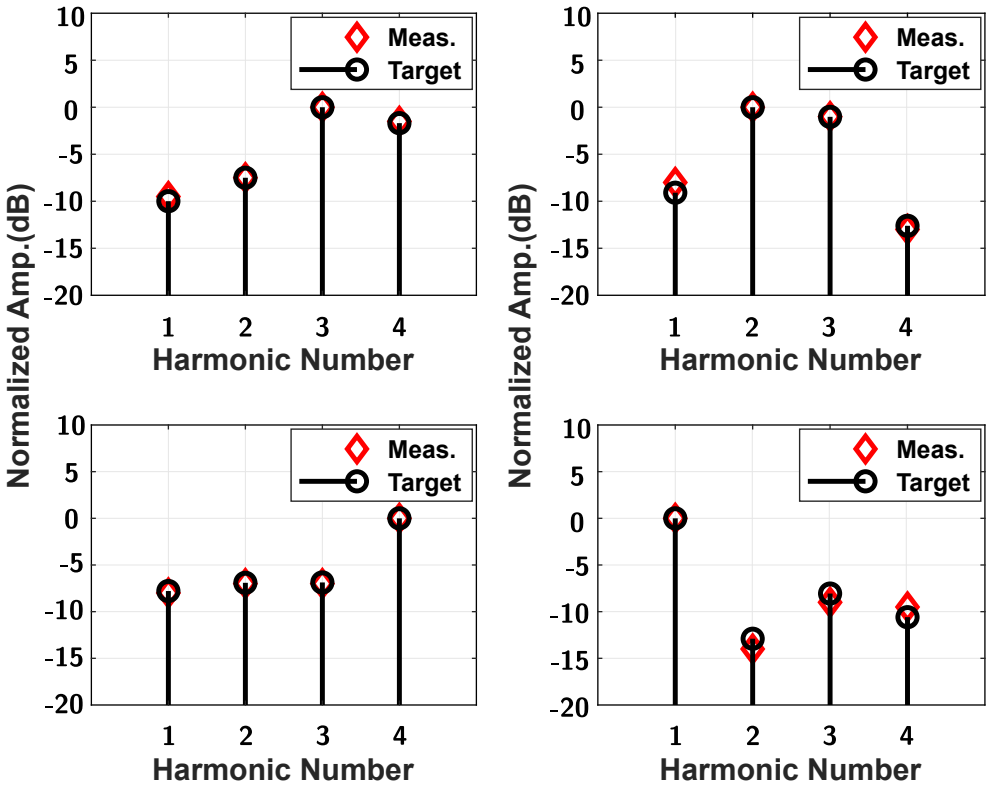


Figure 3.18: Four examples of target and measured harmonic levels employing neural networks predicting reference voltages and polarities.

by using the predicted reference voltages and polarities from the trained neural networks. Harmonic levels are measured at each sub-band with injected input tones at 10 MHz offset from each harmonic frequency. The NN model based on supervised learning can accurately predict the reference voltages and polarities for the desired harmonic response. Comparing the target and measured LO harmonic levels, the worst-case error is within 1.5 dB (Fig. 3.18).

Table 3.2 shows the performance summary and comparison to existing work [8, 10, 32, 39]. Compared to prior work on analog channelizing receivers for

concurrent multi-band reception, this work demonstrates full-band channelization, while including gain control in each sub-band. Compared to DS ADC-based approaches, the key advantage of this approach is that signal gain is already included, and sub-band scaling can be performed prior to digitization.

3.7 Summary

An 8-path spectrum channelizer with PWM-LO based sub-band gain control is described. The use of PWM-LO waveforms to achieve desired spectrum profiles can significantly simplify the signal path, while avoiding requirements for variable g_m-cells or switch matrices. For nominal scaled gain of 0 dB, relative gain in specific sub-bands can be controlled from -20 to -5 dB which can relax compression performance and the sub-ADC dynamic range limitation in the presence of a large local input signal. The harmonic response can be compensated for sinc roll-off as well. Supervised learning with neural networks is used to map from sets of harmonic responses to sets of reference voltages and polarities which are then applied to the NDE-PWM SG. This model makes it possible to predict the reference voltages and polarities for a given harmonic response. Further potential simplification of the architecture can be achieved by employing a fully voltage-mode design, wherein a single front-end LNA with low output impedance can be employed with 8-path PWM-LO waveforms, and is the subject of future work.

Chapter 4

A Voltage-Mode Design for a Spectrum Channelizer with PWM-LO Based Sub-band Gain Control [1]

4.1 Introduction

The architecture of [33] (Fig. 4.1) used a main path and an auxiliary path, whose outputs were combined in the current domain to enable gain scaling. The auxiliary path consists of N gm-cells and switches operating in parallel. In this work, an approach to implement a spectrum channelizer employing a single input stage is proposed for sub-band gain scaling, without the requirement for an auxiliary path, which significantly simplifies the signal path.

The architecture is described in Section 4.2. Noise performance of the proposed design is analyzed in Section 4.3, while simulation results are shown in Section 4.4. The design is verified through simulation in a 65-nm CMOS process.

[1] This chapter is based on reference [40] (K. Y. Kim, D. Z. Pan, and R. Gharpurey, "A voltage-mode design for a spectrum channelizer with PWM-LO based sub-band gain control," in Texas Symposium on Wireless and Microwave Circuits and Systems, (WMCS), pp. 1-5, Apr. 2022 ©2022 IEEE). Ki Yong Kim was responsible for the design and simulation of the channelizer architecture described in this publication.

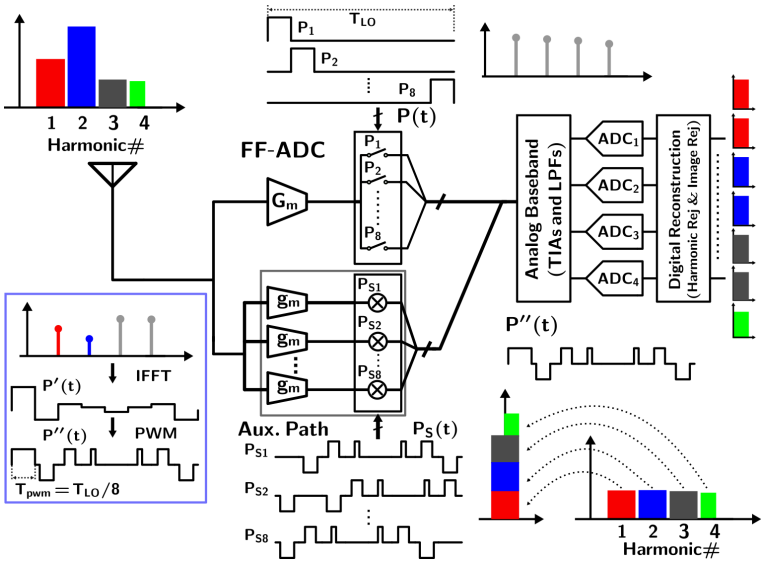


Figure 4.1: PWM-LO based gain-scaling in an FF-ADC channelizer for $N = 8$

4.2 Overview of the architecture

4.2.1 PWM-LO based sub-band gain scaling in the FF-ADC

Fig. 4.1 shows the architecture of the spectrum channelizer of [33]. The architecture is discussed in detail in Chapter 3, and briefly summarized here. The design employs an auxiliary downconverter, consisting of gm-cells and mixers, driven by PWM-LO waveforms, which are connected to individual baseband transimpedance amplifiers. The auxiliary downconverter is placed in parallel with the main-path FF-ADC downconverter and uses the same number of phases of the PWM-LO waveform as the non-overlapping rectangular LOs used in the main-path FF-ADC. The PWM-LO waveform, $P_S(t)$, that provides the desired harmonic response consists of a sequence of natural-sampling dual-edge (NDE) PWM symbols. The effective LO, $P''(t)$, which provides the net desired harmonic gain scal-

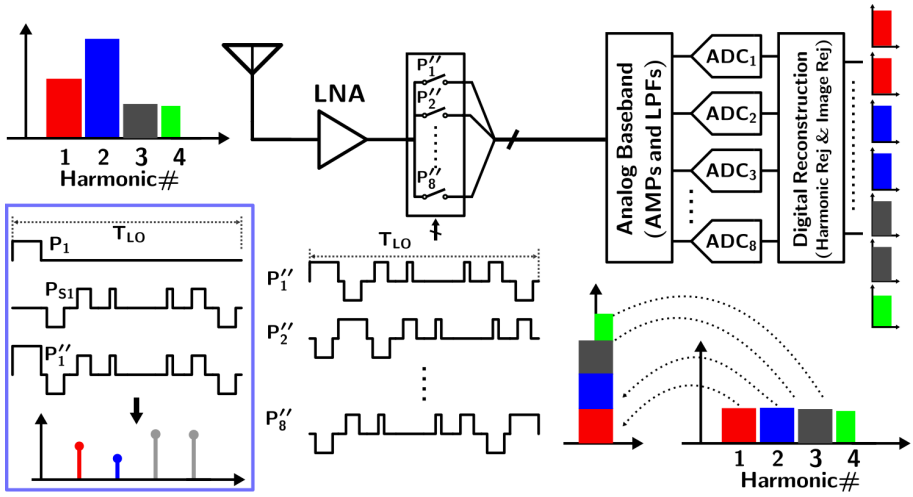


Figure 4.2: A voltage-mode design with PWM-LO based sub-band gain control for $N = 8$

ing, is synthesized by effectively subtracting a PWM-LO waveform, $P_S(t)$, from the rectangular waveform $P(t)$ that is applied to the main-path FF-ADC and contains all harmonics with a $sinc(f/f_s)$ scaling. This subtraction is performed in current-mode. The desired harmonic shaping is achieved by controlling each NDE-PWM symbol's pulse width, which can be easily implemented using delay-locked-loops (DLLs) [30].

4.2.2 A voltage-mode design with PWM-LO based sub-band gain control

Unlike the approach of [33], in this work, the effective PWM-LO waveform, $P''(t)$ is applied directly to the mixers that are connected to the output of a single low noise amplifier (LNA) stage in order to control the sub-band gain. This is made possible by the use of voltage-mode downconversion.

In [33], if a single input gm-cell were to be employed, the multi-phase wave-

forms $P''_{1-8}(t)$ would then drive switches connected to this gm-cell. In each period of the primary clock, f_s, multiple switches would be on simultaneously since the multi-phase waveforms overlap. This would lead to current sharing between multiple paths and scaling down the current amplitude translated to the baseband path by the NDE-PWM symbol. The current-shared waveform would not provide the desired harmonic response. Furthermore, the noise performance of such a design would be significantly worse because the baseband transimpedance amplifiers would not be isolated from each other due to waveform overlap between multiple paths.

Isolation of the baseband amplifiers, while driving them from a single input gm-cell requires the use of a high impedance level at the input to the baseband amplifier and a low impedance at the output of the input amplifier, which implies a voltage-mode design (Fig. 4.2). In this approach, a single front-end LNA with a low output impedance, instead of a low-noise transconductance amplifier (LNTA), is connected to the mixers directly driven by the multi-phase PWM-LO waveforms, $P''_k(t)$, $k \in [1:8]$, which are derived by combining the rectangular pulse waveforms, $P(t)$ and the PWM-LO, $P_S(t)$ used in the auxiliary path of [33]. The baseband transimpedance amplifiers are replaced with high input-impedance voltage amplifiers, which allows for sharing a single LNA output with other baseband paths. A sub-ADC in each path digitizes the baseband signal, and the digital harmonic and image rejection separate the individual sub-bands after digitization. By avoiding the requirement for an auxiliary path with multiple gm-cells, the voltage-mode design can reduce power consumption for the gm-cells, simplify the signal path, and

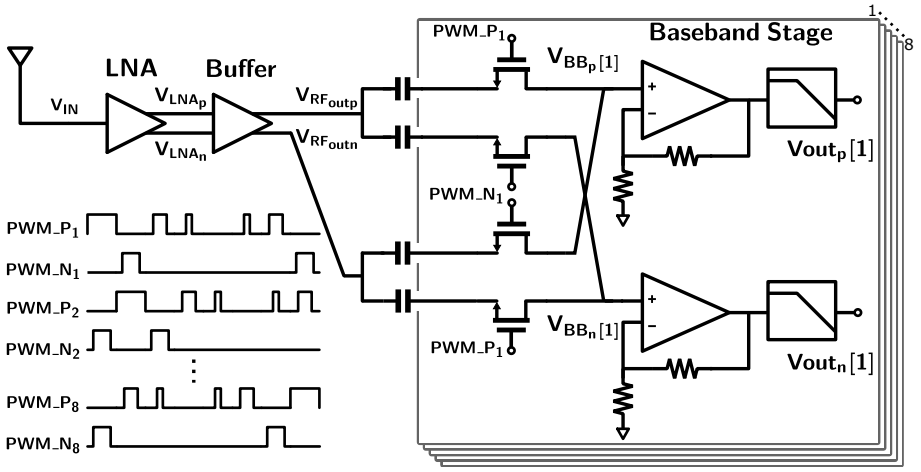


Figure 4.3: Implementation of the spectrum channelizer with a single input stage

remove the potential for gain mismatch between gm-cells on auxiliary paths, and phase mismatch between $P(t)$ and $P_S(t)$.

An eight-path spectrum channelizer that employs the voltage-mode design for sub-band gain control is shown in Fig. 4.3. A noise-canceling LNA provides input matching and implements single-ended input to differential output conversion by using a common-gate (CG) with common-source (CS) design [35]. A CG NMOS provides input matching. In order to equalize the output device sizes of the pseudo-differential CG/CS output, the approach of [41] can be employed. A pseudo-differential source-follower with cross-coupled capacitors is utilized between the LNA and mixer (Fig. 4.4(a)), to provide low output impedance in the LNA stage, and improve the differential balance.

Eight-path voltage-mode passive mixers driven by the multi-phase PWM-LO waveforms downconvert and alias the input voltage to the baseband. A double-

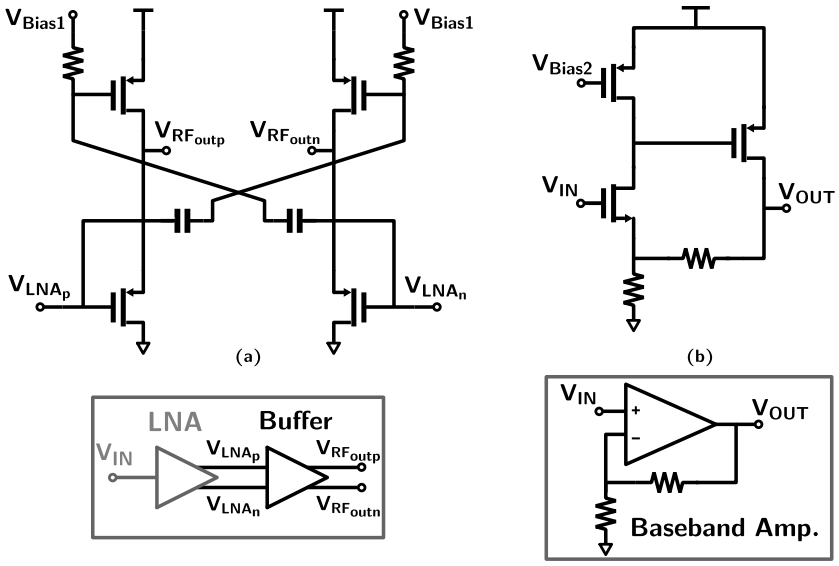


Figure 4.4: Schematics of (a) buffer and (b) baseband amplifier

balanced passive switching mixer consisting of two switches is used in each differential path (Fig. 4.3). Single-ended PWM-LO waveforms, PWM_P and PWM_N, are applied to each switch. Voltage amplifiers with series-shunt negative feedback are used in the baseband stage (Fig. 4.4(b)). The feedback amplifier consists of an input NMOS transistor with high input-impedance, that is loaded with a PMOS current-source. This is followed by a PMOS common-source stage whose output is fed back to the source of the NMOS input stage. Long channel transistors are used in the amplifier to reduce their noise contribution. In order to reduce aliasing after sampling in the sub-ADCs, a sixth-order low pass filter (LPF) using three source-follower biquadratic cells [38], which was used in [10, 33] is employed here as well.

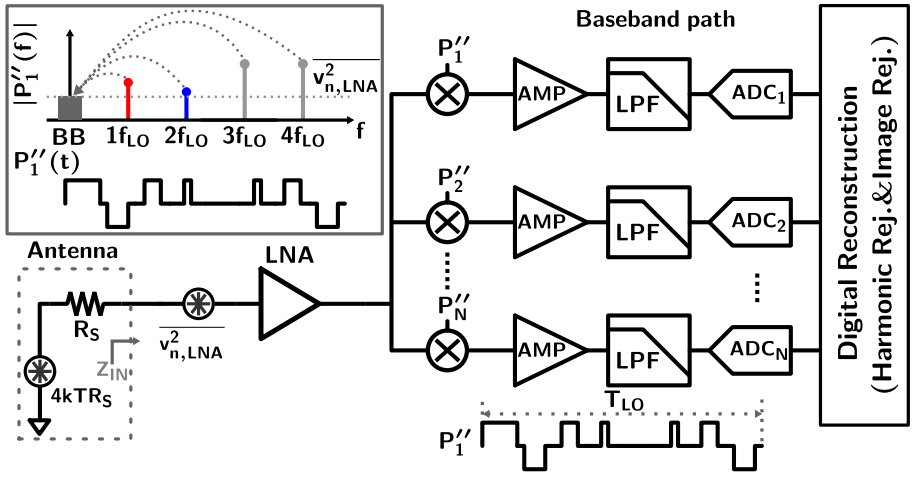


Figure 4.5: Input noise sources in the spectrum channelizer

4.3 Noise analysis

This section analyzes the noise performance of the proposed channelizer. The analysis identifies the noise arising from the front-end (Fig. 4.5). This design assumes voltage-mode mixers, where the output node of the LNA stage is shared by the mixer inputs in N paths. Since the noise from the front-end, including the LNA, is identical in all paths, the noise in each path is correlated, up to a relative phase shift between the paths.

Front-end path noise, $\overline{v^2_{n,FE}}$ is modeled by the noise source, $\overline{v^2_{n,LNA}}$ which includes all noise sources within the LNA before mixing. The input noise from around all harmonics of the effective PWM-LOs, $P_q''(t)$, with the time period of T_{LO}, is downconverted and aliased to baseband in each path (Fig. 4.5). The harmonic response of $P_q''(t)$ is determined by the desired sub-band gain scaling. The spectrum of the PWM-LO, $P_q''(t)$, applied to the q^{th}path, is given by

$$P_q^{''}(f) = \sum_{n=-\infty}^{\infty} p_n \delta(f - nf_{LO}) \tag{4.1}$$

where q is the path number, and p_n is the n^{th} Fourier series coefficient of the effective LO waveform, $P_q^{''}(t)$. The front-end noise components of $4KTR_S$ and $\overline{v_{n,LNA}^2}$ around the n^{th} harmonics of $P^{''}(t)$ are scaled by $|p_n^2|$ and translated to baseband in each path. HR and IR in the digital domain are performed to obtain individual sub-bands. This can also reject the noise folded to baseband after mixing from all harmonics except for the selected harmonic and its aliased harmonic frequencies around mNf_{LO}. The noise folding during mixing depends on the 3-dB bandwidth at the output of the LNA and the selected harmonic number at the final output. The total noise power of multi-phase PWM-LOs, $P_q^{''}(t)$, at the channelizer output through the front-end path is given by

$$\overline{v_{n,out,FE}^2(n)} = \overline{v_{n,FE}^2} T_{n,FE}^2(n) \tag{4.2}$$

where the noise folding factor of the front-end path, $T_{n,FE}^2(n)$, is given by

$$\begin{aligned} T_{n,FE}^2(n) = N^2 \Bigg[& \left| \frac{p_n}{1+j\left(f_s n / N f_{FE,3dB}\right)} \right|^2 \\ & + \sum_{m=1}^{\infty} \left\{ \left| \frac{p_{Nm+n}}{1+j\left(\frac{f_s(Nm+n)}{N f_{FE,3dB}}\right)} \right|^2 + \left| \frac{p_{Nm-n}}{1+j\left(\frac{f_s(Nm-n)}{N f_{FE,3dB}}\right)} \right|^2 \right\} \Bigg] \end{aligned} \tag{4.3}$$

where n is the selected harmonic number and $f_{FE,3dB}$ is the 3-dB bandwidth of the LNA's output.

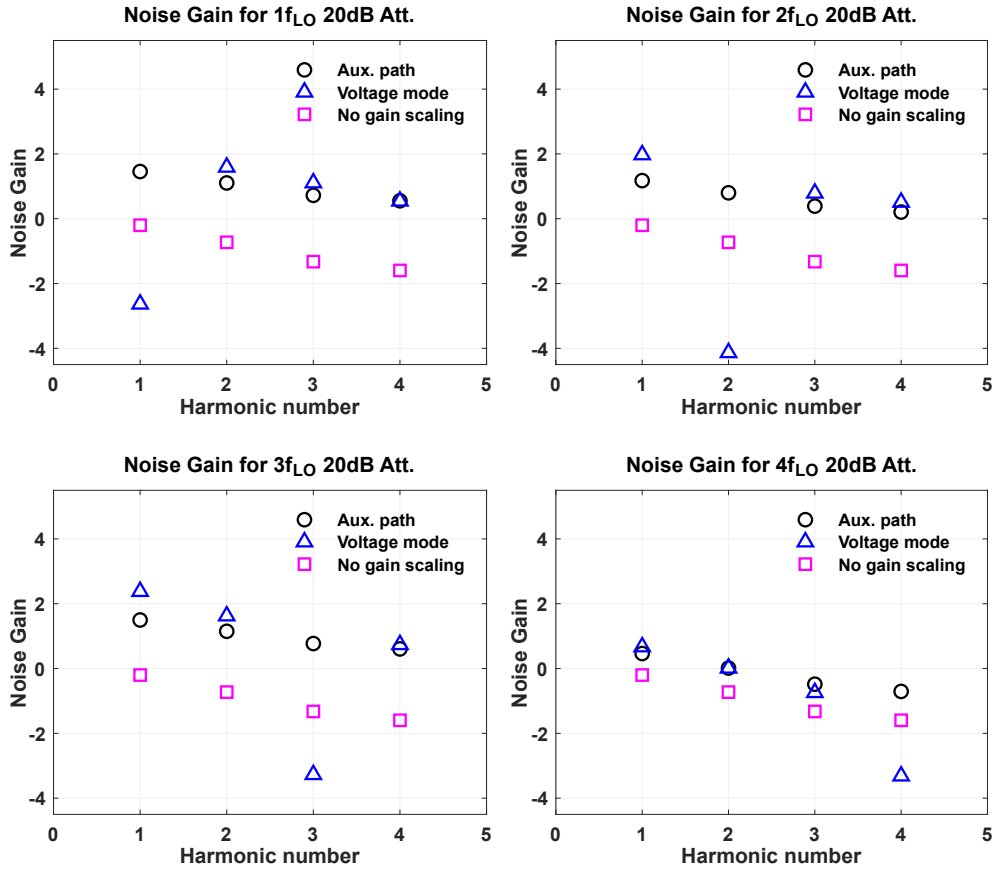


Figure 4.6: Front-end noise folding with 3-dB bandwidth of the input stage

The front-end noise-folding gain (3.3) is plotted along with $T^2_{n,main} + T^2_{n,aux}$ from [33], which is the sum of the noise-folding gains of the main and auxiliary path respectively, for an eight-path channelizer with finite input 3-dB bandwidth (Fig. 4.6). In this work, the 3-dB bandwidth of the LNA is estimated to be 1.5 GHz based on simulation. $P_s(t)$ is identical to the PWM-LO used in [33]. Fig. 4.6 compares the noise-folding gain between this design and the channelizer with the auxiliary path [33], assuming attenuation of 20-dB for a single harmonic from $1f_{LO}$ to $4f_{LO}$. As

can be observed, the front-end noise folding in the attenuated harmonic decreases with gain-scaling due to HR and IR. However, the noise impact on the unattenuated harmonic is higher than the case without gain-scaling since the harmonic amplitude of the PWM-LO, $P''(t)$, at the selected harmonic and unrejected harmonics is higher than the case without gain scaling with the rectangular pulse, $P(t)$. Compared to the impact of front-end noise in the channelizer employing the auxiliary path [33], for identical harmonic scaling, the noise impact for unattenuated harmonics is slightly higher. Unlike [33], the correlated front-end noise in each path adds in voltage after applying the digital reconstruction by HR and IR.

Considering only the front-end gain, the conversion gain of the channelizer is given by

$$A_v(n) = A_{LNA}\left(sinc\left(\frac{n\pi}{N}\right) + \kappa(n)\right) \tag{4.4}$$

where A_{LNA} is the voltage gain of the input LNA stage and $\kappa(n)$ is the scaled gain arising from the PWM-LO, $P_S(t)$ at baseband from harmonic number n. $\kappa(n)$ can be positive or negative according to the desired harmonic response of $P_S(t)$ and is proportional to n^{th} Fourier series coefficient of $P_S(t)$. The conversion gain at the attenuated sub-band is reduced with the PWM-LO $(P''(t))$ applied, while the conversion gain at the unattenuated sub-band is higher than the case with no gain-scaling, with only $P(t)$ applied. Assuming that the input impedance is matched and considering only the front-end conversion gain and noise-folding gain, from (3.3) and (4.4), the double-sideband noise figure (NF) of the front end in the n^{th} harmonic

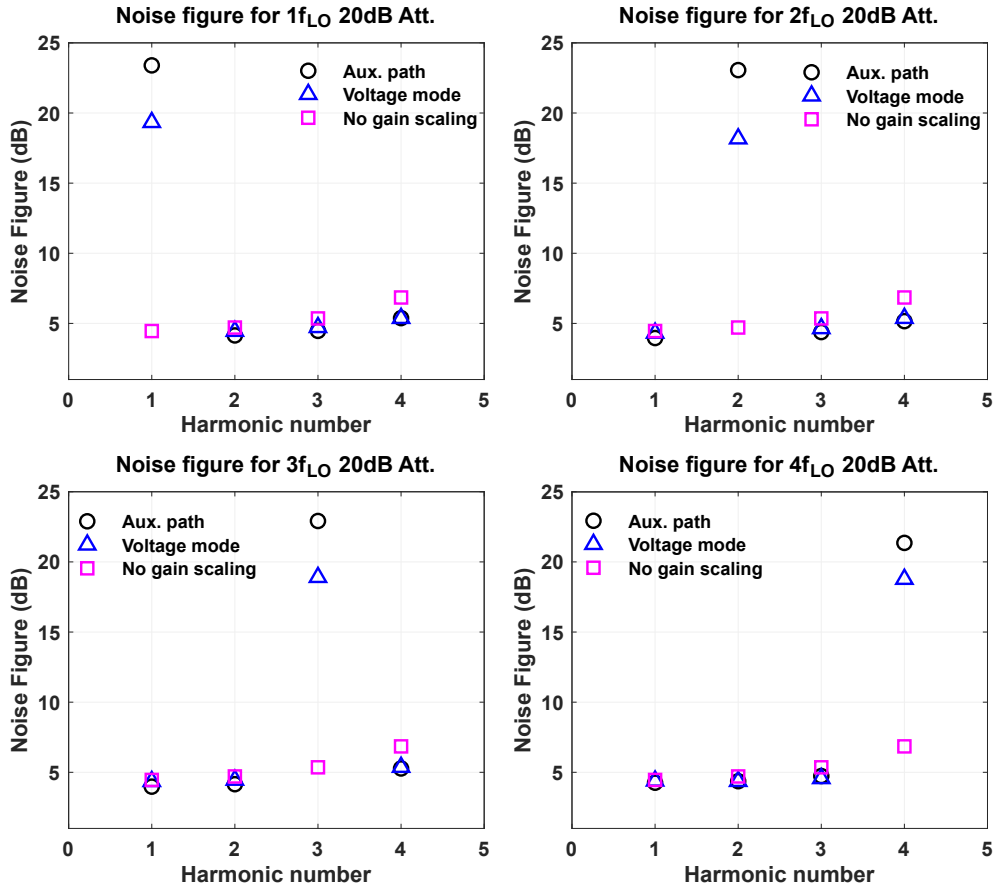


Figure 4.7: NF without gain scaling and with single-harmonic gain scaling from $1f_{LO}$ to $4f_{LO}$

can be calculated as

$$\begin{aligned} \mathrm{NF}(n) &= \frac{SNR_i}{SNR_o} \\ &= 1 + \frac{(\frac{4kT\gamma}{g_m})T_{n,FE}^2(n)A_{LNA}^2}{2kTR_sA_v^2(n)} \\ &= 1 + \frac{(\frac{4kT\gamma}{g_m})T_{n,FE}^2(n)}{2kTR_s\left(sinc\left(\frac{n\pi}{N}\right)+\kappa(n)\right)^2}. \end{aligned} \tag{4.5}$$

The comparison of the NF (4.5) with the NF (3.10) in Section 3.4.3 for $g_m =$ 20 ms and $\gamma \approx 1$ is plotted in Fig. 4.7, without gain-scaling and with gain attenuation of 20 dB. The NF in the harmonic with the attenuation increases significantly due to gain scaling. As can be observed, the NF at the unattenuated harmonics with gain-scaling is lower than without gain-scaling since the relative increase of the conversion gain in the unattenuated harmonic is higher than that in the noise folding gain from the PWM-LOs. Compared to the NF (3.10) in Section 3.4.3, the NF in the unattenuated harmonics with gain scaling is slightly higher due to the difference in noise folding gain, as shown in Fig. 4.6.

4.4 Simulation results

The simulated architecture includes the LNA, switch mixers, baseband amplifiers, and baseband filters and is designed using a 65-nm CMOS process. An 8-phase PWM-LO waveform with a frequency of 200 MHz is employed using an ideal clocking network in the simulation. In practice, the PWM-LO generators shown in [30, 33] can be employed. The design controls the amplitude of 4 LO harmonics at $200 * k$ MHz ($k \in [1:4]$) and spans a frequency-range from 100 MHz to 800 MHz with a sub-band bandwidth of 100 MHz. The harmonic and image rejection are performed in the digital domain to separate the sub-bands. This is simulated in MATLAB.

Fig. 4.8 shows the voltage gain without gain scaling and with gain scaling of -20 dB from $1 f_{LO}$ to $4 f_{LO}$. A voltage gain of 29-33.5 dB is observed without gain scaling across sub-bands, while the voltage gain is 31.5-35 dB with single harmonic

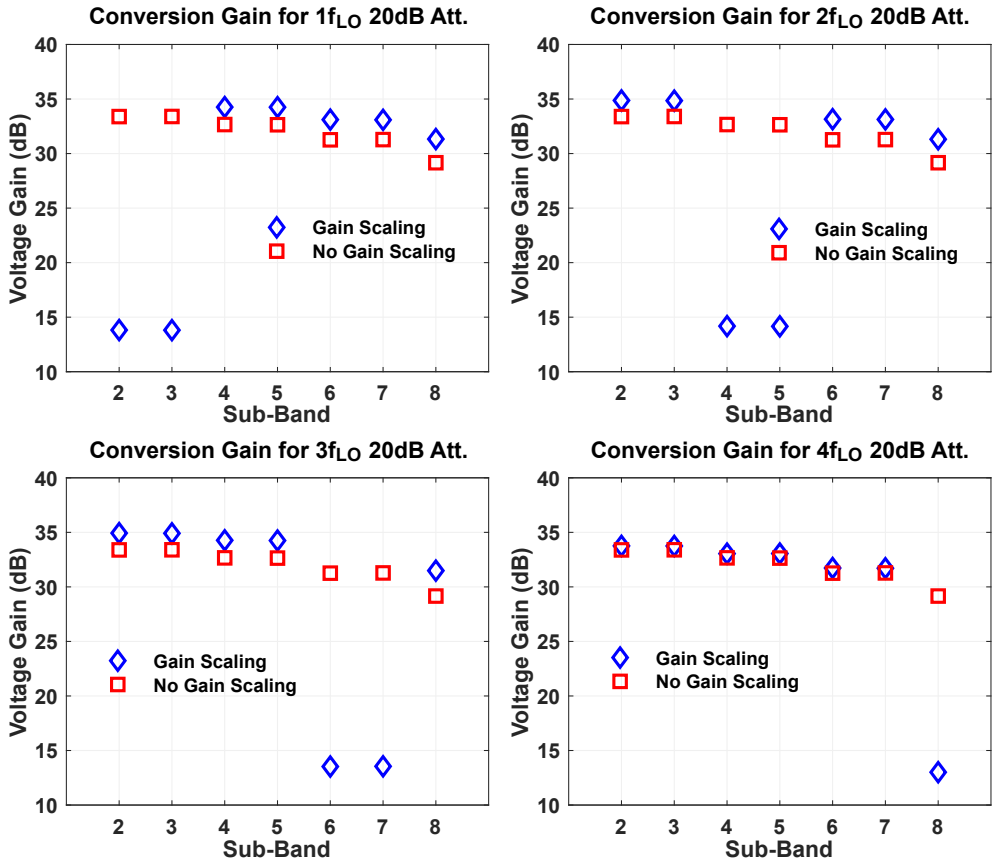


Figure 4.8: Simulated conversion gain without gain scaling and with single-harmonic gain scaling from $1f_{LO}$ to $4f_{LO}$

gain scaling in all sub-bands. As shown, the voltage gain in the desired attenuated sub-band is scaled by -20 dB compared to the unattenuated sub-band through the PWM-LOs applied to the switches.

Along with noise, linearity is a critical consideration in the design of the voltage-mode FF-ADC. The linearity requirement at the inputs of the sub-ADCs is identical in voltage and current-mode implementations. Thus the linearity requirements of the signal-path circuits in the voltage mode design are not expected to be

significantly different from the current-mode design. The primary circuit-level linearity consideration will arise from the input linearity of the baseband stage, since it is driven in the voltage mode. However, the signal levels at the input of the baseband stage will be lower than that at the input of the sub-ADCs by the gain ofthe baseband stage. In an optimized design, all critical circuit blocks, including the RF LNA, the baseband filters, and the baseband amplifier, would need to be designed for nearly identical dynamic range.

4.5 Summary

A broadband spectrum channelizer employing a voltage-mode design for sub-band gain control is proposed. The design uses a single LNA with a low output impedance, voltage-mode mixers, and baseband amplifiers with a high input impedance, and does not require an auxiliary downconverter for the desired sub-band gain scaling. This makes it possible to simplify the signal path and reduce power consumption, while this design also avoids the dynamic range limitation of the sub-ADCs which can arise in the presence of significant input signal variation across sub-bands. A noise analysis of the proposed channelizer is performed and compared to the previous work. Simulation results using 65-nm CMOS devices are presented.

Chapter 5

Conclusion

Time-domain digitization has been the primary approach for implementation of broadband receivers and spectrum analyzers. This approach offers the benefits of digital filtering and channel selection, which are immune from analog non-idealities. On the other hand, it places fundamental limits on the dynamic range, due to lack of spectral selectivity. Specifically, the dynamic range of the digitizer is dominated by the largest signals, thereby reducing the dynamic range available to smaller signals in other portions of the spectrum. In addition, the input driver for a time-domain digitizer needs to have a dynamic range in excess of the digitizer itself, which can imply significant power dissipation.

Frequency-domain approaches for implementing broadband receivers and spectrum analyzers based on RF receiver banks have also been proposed. However, in integrated applications these run into practical constraints arising from the requirement for synthesis of multiple LOs on a single IC, and potential performance degradation arising from harmonics and spurious LO coupling.

This thesis examines a mixed-signal approach that addresses the limitations of the above approaches. The requirement for multiple LO synthesis is avoided by using harmonics of a periodic rectangular clock. The design implicitly channel-

izes a broadband input by aliasing portions of the spectrum coincident with the LO harmonics to baseband, in the analog domain. The sub-bands are digitized using ADCs with a Nyquist rate corresponding to the sub-band bandwidth. Through the use of polyphase down-conversion, the LO harmonics are separated in the digital domain. Gain control is achieved in the analog domain by using pulse-width modulated clocks for downconversion. This allows for controlling the signal level of individual sub-bands that are applied to the baseband ADCs, and allows for balancing the dynamic range that is available across the spectrum, unlike a time-domain approach. The basic theory of the approach is described in Chapter 2.

A complete implementation of a current-domain design based on the above approach is presented in Chapter 3. The signal path consists of the RF transconductance amplifiers, the baseband filters and transimpedance amplifiers, and output buffers. The signal path is split into a main-path that downconverts the input signal using polyphase rectangular pulses with a fixed duty-cycle, and auxiliary paths, where polyphase PWM-LO clocks are applied for gain control. The outputs of the main and auxiliary paths are combined at baseband prior to the baseband ADCs. The baseband ADCs are off-chip. Harmonic and image rejection is performed in the digital domain employing an FPGA. The PWM-LO generator is included in the design. The full design is implemented in a 65-nm CMOS process.

A neural-network based interpolator is used to map the desired spectrum to PWM-LO timing information. The training used in the neural-network compensates for the non-linear mapping between spectrum amplitudes and PWM-LO pulse widths. The complete design and implementation are described in Chapter 3.

While a current-mode design is demonstrated, a voltage-mode approach that can potentially simplify the implementation is also proposed. The voltage-mode architecture avoids the requirement for an auxiliary path. The RF stage employs an LNA with a low output impedance, instead of an LNTA, and the baseband transimpedance amplifiers are replaced by baseband voltage amplifiers. These substitutions make it possible to apply the PWM-LO clocks for gain control within the main-path itself. This approach is described in Chapter 4.

The voltage-mode approach can be investigated as part of future work. Further work can consider the use of analog harmonic selection techniques at baseband within the FF-ADC, in combination with digital techniques, for resolving the aliases prior to the ADCs. This can help to further reduce the dynamic-range requirement of the ADCs.

A circuit that senses incoming signals could also be considered in future work, where an interference detector is used to rapidly determine the incoming frequency spectrum. In this case, on-chip learning implementation instead of off-chip learning is employed to control the desired harmonic response of the channelizer in real-time. This can help to quickly optimize each sub-band gain to avoid the ADCs dynamic-range limitation arising from the presence of multiple interferers.

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