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Predicting Performance Parameters of Analog and Mixed-Signal Circuits Using Built-In and Built-Off Self Test

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Predicting Performance Parameters of Analog and Mixed-Signal Circuits Using Built-In and Built-Off Self Test

by

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Dedicated to my family

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The widespread use of embedded mixed-signal cores in system-on-chip (SoC) or System-on-Package (SoP) design has been increasingly important in cost-effective manufacturing test for mixed-signal devices. A typical SoP encapsulates many of its internal functions, and its production test is performed by application of test signals to the SoP under control of external Automatic Test Equipment (ATE). However it is a problem that the external ATE does not have direct access to all the internal embedded functions of the SoP. Thus a classical test approach to SoP suffers from limited controllability and observability of its subsystems.

Built-in Self-Test (BIST) and Built-off Self-test (BOST) schemes have been suggested and developed to overcome the limitations of conventional test, such as limited test Input/Output (I/O) accessibility as well as high test cost. However most BIST/BOST approaches have limited test accuracy.

The focus of the dissertation is to develop a cost-effective performance-based test methodology based on BIST/BOST, while maintaining the same accuracy as conventional test. This dissertation proposes one BIST approach and two BOST schemes. Our BIST methodology presents a methodology for efficient prediction of circuit specifications with optimized signatures. The proposed Optimized Signature-Based Alternate Test (OSBAT) methodology accurately predicts the specifications of a Device Under Test (DUT) using a strong correlation mapping function. The approach overcomes the limitation that analytical expressions cannot precisely describe the nonlinear relationships between signatures and specifications. Our first BOST approach presents a practical methodology for effective prediction of individual dynamic performance parameters of differential devices with a cascaded Radio-Frequency (RF) transformer in loopback mode. The RF transformer produces differently weighted loopback responses, which are used to characterize the DUT dynamic performance. The approach overcomes the imbalance problem of Design for Test (DfT) circuitry on differential signaling, thereby accurately measuring the dynamic performance of differential mixed-signal circuits. The second BOST scheme is an efficient methodology for accurate prediction of aperture jitter using cost-effective loopback methodology. Aperture jitter is precisely separated from input and clock jitter as well as additive noise present in the DUT, by using an efficient loopback scheme. Hardware measurements were performed for all our approaches, and good results were obtained. This fact verifies that all approaches can be practically used for production test in industry.

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Chapter 1

Introduction

1.1 Motivation

The growing demand for multi-media, wireless communication, networking, and control systems has increased the importance of research in cost-effective manufacturing test for mixed-signal devices [29]. Most modern mixed-signal systems are of the 'big-D'-'small-A' (D-digital and A-analog) configuration. However, the 'small-A' takes up the majority of the production test time incurred in testing these devices [17], since it includes a large number of tests for analog circuit specifications. The extent of the problem can be gauged by the fact that the test cost is approaching 40% of the total manufacturing cost of these packages [5].

Also, analog test is a difficult task because of the necessity of dealing with the continuity of analog signal characteristics such as amplitude, frequency or phase of a voltage and since a tolerance is acceptable for the results. The analog specification for output of a non-faulty circuit can only be described within a tolerance margin as shown in Figure 1.1 [14, 49, 80]. Moreover, the ideal input waveform may not be applied to DUT, due to noise and tolerance specifications (or tolerances in the component values) of the circuit

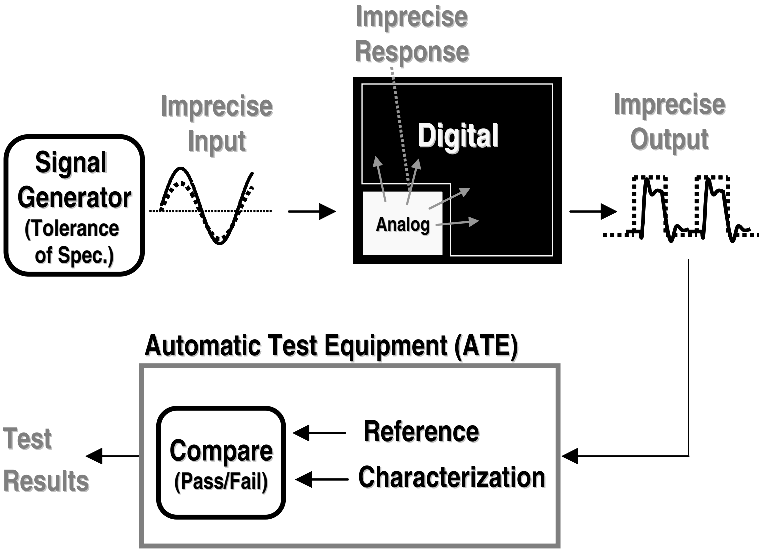


Figure 1.1: Issue of Conventional Test due to Design Tolerance

such as signal generator, voltage controlled oscillator (VCO) and crystal oscillator, which produces the waveform. Thus the noisy or distorted input can affect the response of the DUT.

The problem of analog circuit testing becomes more difficult due to the integration of analog circuits as parts of the core in SoCs or SoPs. A typical SoP encapsulates many of its internal functions, and its production test is performed by application of test signals to the SoP under control of external ATE. It is a problem that the external ATE does not have direct access to all the internal embedded functions of the SoP. It may be possible to route some of the internal electrical signals out of the package to the external tester; however, these internal signals operate at frequencies that cannot be observed directly by an external tester due to the frequency limitations of the

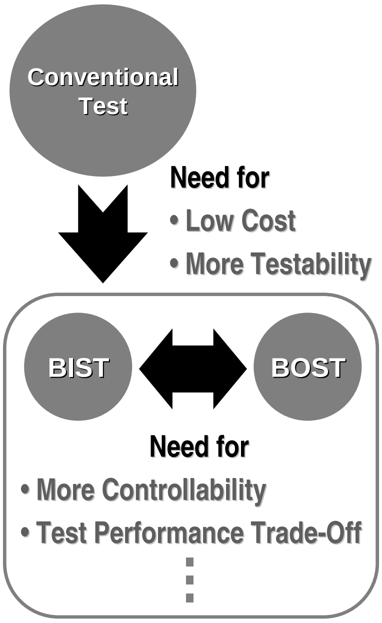
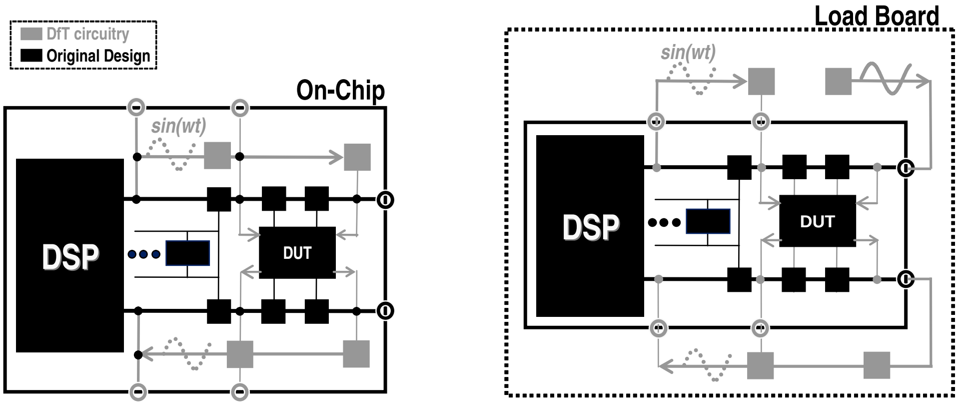


Figure 1.2: Need for BIST and BOST Schemes

encapsulating package and lower speed of external I/O. A similar speed and integrity concern is applicable to validating the subcomponents of the system. While traditional systems have test nodes to individually verify the operation of their subsystems, a classical test approach to SoP suffers from limited controllability and observability of its subsystems. Furthermore, the system specifications *guaranteed by design* depend on validation of associated subsystem specifications, which may no longer be accessible in a SoP configuration. This proposition is especially important for embedded passive components constituting a part of the package itself [5, 86].



Typical BIST Configuration

Typical BOST Configuration

Figure 1.3: Typical Configurations of Self Test

1.1.1 Need for New Solution

Consequently, the call for a testable SoP results in a conflict of interest between the degree of integration afforded by the design process and the level of testability achievable by an external tester. A viable solution is to place the ATE functionalities in close proximity of the SoP module to be tested. This improves the test-access speed, minimizes the test signal degradation by the cable parasitics of the external ATE, and increases controllability and observability of the signals internal to the DUT as shown in Figure 1.2. As widely accepted solutions, BIST [39, 53, 89] and BOST [5, 28] have been suggested and developed to allow test using much less expensive ATE as shown in Figure 1.3 [14].

A BIST scheme involves moving part of the required test resources (test stimuli generation, response evaluation, test control circuitry, etc.) from the

ATE to the chip. Basically BIST pushes the external tester functionality into the package and even into the bare dies wherever possible. Another alternative, BOST migrates test functions of the external tester to the load board as well as the bare dies. The additional DfT circuitry on the load board retains the ability to apply high-speed stimulus to the system under test, capture the test response or provide some weight on the DUT output for characterization. Moreover in BOST scheme, post-processing in the processor available in the SoP is performed to analyze the output response, such as histogram [42], sine wave fitting [71] and oscillation-based technique [68]. In these approaches, the device is modified to incorporate some additional functions within the chip by reusing components such as Analog-to-Digital (ADC) and Digital-to-Analog (DAC) converters already available at the system level. As a result, without BOST and BIST very high-performance SoPs may not be economically testable. The test economics is greatly improved by having test functions on the load board (BOST) or the SoP itself (BIST). This allows high performance systems to be tested with a low-cost ATE without loss of test quality.

Various methodologies based on a BIST/BOST scheme have been proposed to reduce the test cost compared to conventional test. Many approaches based on fault-based test have been proposed based on a BIST/BOST scheme [48, 75, 86]. Motivated by the popularity of fault-based production testing of digital circuits, many researchers tried applying the methodology to the analog and mixed-signal domains [75]. In fault-based testing, a list of physically realistic faults are derived from process information, defect statistics, and circuit layout. Tests are then developed to distinguish these faulty circuits from the fault-free circuit [81]. However the fault-based approach has limitations in testing analog and mixed-signal circuits.

- This approach requires DUT topology and the reference fault models [75]. It is hard to build the reference model of complicated circuits for the fault-based test. A poorly described model leads to lower test accuracy. Even though the method can increase fault coverage, the stimuli are targeted at detecting specific faults in specified components thereby covering selected faults.
- Secondly, although the methodologies can detect catastrophic faults effectively, such as open, short and bridge faults [76] resulting in reducing the test time and achieving a low-cost test as compared with a conventional performance-based test, they cannot detect parametric failures effectively. Furthermore even though it can detect parametric faults effectively by applying many sinusoidal signals, studying the steady state response of the DUTs is time consuming.
- Thirdly, analog circuits are tested for satisfying their specifications, not for faults [71]. Thus this type of test may not be a complete alternative to the existing performance-based test due to the lack of performance information.

In an attempt to overcome these drawbacks, many researchers have proposed performance-based test methodologies. In the performance-based test, short duration and optimized stimulus is applied to a DUT. The response is analyzed to characterize the performance parameter of the DUT, without the need for reference model for the DUT. As an example of the approach, the signature-based test methodology includes analyzing the DUT response to generate the intermediate performance parameter called *performance-based signature* [54, 65], which compresses or represents the output responses of a DUT. The signatures should be able to be easily found and strongly correlated with the DUT performance. Then the method involves deriving the relation between the signatures and the DUT performance [62]. The conventional test, which uses well-known Digital Signal Process (DSP) to characterize the specifications on the frequency domain, is also an example for the performance-based test. However this approach requires relatively long test time to analyze the output response for characterization of performance, and different instruments are sometimes needed for characterizing the specifications.

1.2 Contribution

This dissertation investigates efficient performance-based test methodologies based on BIST/BOST, without loss of test quality. The primary contributions of the dissertation are discussed in this section.

1.2.1 Development of Cost-Effective Methodology

CMOS and BI-CMOS technologies have made it possible to combine digital and analog circuits in a SoC and offer the possibility of designing high-

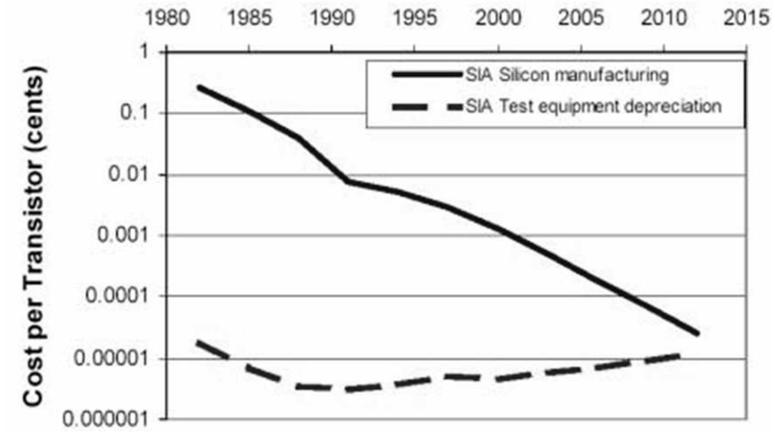


Figure 1.4: Test Cost and Manufacturing Cost (Semiconductor Industry Association [72])

quality analog circuits. Two factors dominate production costs in manufacturing of SoCs. These are the direct costs of test equipment and test time, and the indirect costs of test procedure development in conventional test [35]. Figure 1.4 shows that test cost approaches manufacturing cost as time goes by.

Analog signals are represented with much fewer parameters in this dissertation. Thus the acquisition of those parameters can be performed with simple DfT circuits. In addition the test response can be readily interpreted into performance parameters in a specification sheet. Thus it allows DUTs to be evaluated by comparing the measured performance directly against the specifications. As a result, our efficient approaches based on BIST/BOST architecture allow low-cost measurement without loss of test quality, thereby providing a complete alternative to the conventional mixed-signal test.

1.2.2 Improvement of Controllability and Observability

As mentioned in the previous section, while traditional systems have test nodes to individually verify the operation of their subsystems, a classical test approach to SoP suffers from limited controllability and observability of its subsystems [5, 86]. Consequently, the call for a testable SOP results in a conflict of interest between the degree of integration afforded by the design process and the level of testability achievable by an external tester.

DfT and self-test techniques have been proven to be very effective by the meaning of increasing the observability and the controllability of a DUT. Methodologies based on BIST and BOST schemes in this dissertation enhance the observability and controllability of mixed-signal circuits by splitting embedded analog and mixed-signal component into individual components using efficient DfT circuitry. Also high controllability and observability of the signals internal to the DUT are achieved for test stimulus application due to the fully digital generation method.

1.2.3 Overcoming Limitations of Conventional BIST Schemes

BIST pushes the tester functions into the DUT in order to overcome the issues of conventional test as mentioned previously. BIST of analog and mixed-signal electronics provides the following major merits.

- On-chip generation of high-speed test stimulus using low-cost hardware
- High-speed on-chip response acquisition followed by analysis or response

compaction

Although this approach addresses the tester cost and test access limitation problems, large silicon area-overhead taken by these circuits, especially in mixed-signal testing, may not be feasible for all applications, and the addition of BIST circuitry can degrade the performance of the circuit being tested [18]. Basically the introduction of test circuitry into the device may violate original design constraints, e.g., device matching, parasitic loading, etc., and, as a result, additional design iterations may be needed during system design. Consequently, BIST is feasible only when it can be integrated into the system design flow.

A performance-based test approach based on BOST is a viable solution. Even though a BOST scheme requires a load board and has the access limitation for test nodes, its advantages can overcome the limitations of BIST approach as follows.

- BOST can significantly reduce the on-chip area overhead taken by the DfT circuits in the package under test by pushing most DfT circuits onto the load board, resulting in lower design cost.
- This scheme is also effective when the used DfT device is very sensitive to the noise generated from other circuits.

The DfT device on the load board is not affected from noise generated by circuits in on-chip system, thereby improving test accuracy, since the DfT device can be installed physically more farther from other circuits. The DfT device sometimes needs to be characterized before it can be used to test DUTs. In such a case, the DfT device can be easily characterized on the load board. As mentioned before, BIST has the advantage to reuse devices already available at the system under test. It also means that if the needed DfT components are not available, the device should be carefully designed without affecting signal paths and the functionality of the original design in the system under test. This requires design efforts with the same quality as the original design. On the other hand, BOST uses the device as a DfT logic on the load board, which is commonly available for production test, resulting in lower test cost and no additional design efforts for DfT circuits. To summarize, BIST and BOST architectures are optimized for the different conditions of the ICs to be tested and DfT circuitry for the proposed approach. The broad range of different requirements of mixed-signal circuits can not be solved by BIST (or BOST) as a fixed unique solution. Careful selection of BIST and BOST schemes is needed to master the diversity of the problem. The approaches in this dissertation are performed based on efficient scheme to combine BIST and BOST features to overcome the limitations of conventional BIST.

1.2.4 Solutions to Challengeable Issues on High Speed Mixed-Signal Circuits

High-speed mixed-signal devices are designed using deep submicron process technologies, that generate a new class of defects and require faster, more accurate high-speed mixed-signal testing [19].

Many high-speed analog and mixed-signal circuits operate on a composite signal consisting of a differential signal pair. Most external test equipment used in conventional tests have single-ended I/O and use a coaxial cable to connect to the DUTs. However, no differential network device can avoid inherently the imbalance problem due to parasitic coupling capacitances in the differential terminals. The imbalance results in additional distortion or noise on the output of the DND. The distorted and noisy signal is delivered to the DUT input, thereby degrading the DUT performance [37].

Another challengeable issue of high-speed mixed-signal testing is the aperture jitter testing in high-speed ADC where aperture jitter is one of major limiting factors on the performance of mixed-signal circuits. Timing jitter introduced by sampling process is becoming a larger portion of the available timing margins, since it dramatically degrades the achievable Signal-to-Noise Ratio (SNR) of the data converters. Therefore this fact imposes stringent conditions on the allowable timing jitter in high-frequency signals. Thus jitter measurement is an important part in production testing of high-speed mixed-signal devices [84, 85].

However most mixed-signal BIST/BOST approaches have not been developed to deal with the issues in high-speed analog and mixed-signal testing due to the following reasons.

- The magnitude and phase imbalance introduced by DfT circuitry significantly degrades DUT performance parameters, thereby reducing test accuracy and fault coverage.

- Jitter-induced noise present in DUT affects performance of DfT circuitry as well as DUT output, thereby degrading DUT performance.
- Even if a self-test approach is developed to overcome the above issues, this could lead to greater complexity in DfT circuit implementation.

Efficient *Transformer-Coupled Loopback Test* characterizes individual mixed signal specifications on differential signaling to overcome the imbalance effect due to differential signaling and realize cost-effective test. The proposed method uses an existing device, the RF transformer commonly used in the conventional test. It means that the RF transformer does not need to be designed, and the test cost is reduced. Furthermore the RF transformer has inherently wide input bandwidth. Therefore reuse of the RF transformer is possible to apply various frequency input signal.

To improve prediction accuracy for aperture jitter, *Efficient Loopback Test for Aperture Uncertainty* in embedded mixed-signal circuits is proposed. The total six jitter components are present in DAC and ADC. Our efficient loopback test system allows us to characterize only three jitter components without the need for all the jitter components. As a result, our method allows us to predict aperture jitter of ADC using clock jittered-noisy DAC output. It further means that the proposed method replaces the need for expensive, low-jitter signal synthesizer to be essentially required in the conventional test.

1.3 Organization and Approach Overview

The rest of this dissertation is organized as follows. Chapter 2 discusses the hardware architecture of self test and ATE and various approaches based on BOST and BIST.

Chapter 3 explains an efficient methodology called Optimized Signature-Based Alternate Test (OSBAT), to improve the accuracy in prediction of specifications using strong correlation mapping and to reduce test time and cost. A sinusoidal signal is applied to a DUT and the resultant output signal is manipulated into the optimized signatures by using low-cost comparators and digital circuits. To predict the performance parameters of a DUT, the correlation functions which map the obtained signatures to the specifications are generated by a regression technique. This approach provides improved performance on the problems associated with representing the exact relationship between signatures and specifications due to nonlinear characteristics. The results of hardware measurement with DACs (AD9764) show error reductions of THD, SNR and SINAD as 1.4dB, 2.3dB, and 2.1dB compared with the TSR technique. In addition, we evaluated the sensitivities of this technique to common non-idealities, such as the variations of reference voltages and sampling rate of BIST circuits. The results from our method with low sensitivity indicate that our predictive accuracy is reliable and stable. Also another set of hardware measurements was performed with commercial DACs and ADCs (AD9764 and National Semiconductor ADC14L105) to evaluate the performance of the proposed method on the application for loopback mode. The results show that the proposed method deals with the fault masking problem in loopback tests, and produces lower errors when predicting specifications.

Chapter 4 discusses a BOST scheme based transformer-coupled loopback test for individual mixed signal specifications on differential signaling. A cascaded or double RF transformer used as the DfT circuit provides improved performance with regard to the imbalance, due to the reduction in parasitic capacitances. Using the characteristics of a cascaded RF transformer on the loopback signal path, we obtain differently weighted loopback responses. Then the spectral responses are used to characterize the characteristic parameters including imbalance caused by DUTs to provide the information about the nonlinear behavior of a DUT. The mapping function for the characterization is derived by a neural network algorithm. We test Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) to demonstrate our approach.

Chapter 5 explains efficient loopback test for aperture uncertainty in embedded mixed-signal circuits to improve prediction accuracy for aperture jitter and realize cost-effective test. A DUT is placed in a loopback mode that loops the output of one signal path back into the input of other signal path. Two tests are performed for the proposed method. In the first loopback test, a low frequency sinusoidal signal is applied to a DUT in loopback mode, and the spectral loopbacked response is characterized to find non-jitter related noise. Similarly in the second loopback test, a high frequency signal is applied and the resultant response is analyzed to find jitter induced-noise as well as non-jitter related noise. As a result, characteristic parameters are obtained from their spectral response, and spectral equations are derived to characterize jitters present in DUTs. For predicting the aperture jitter of a DUT, the equations are solved by precisely separating the aperture jitter from input and clock jitters, and additive noise based on low-cost and efficient loopback scheme.

Chapter 6 summarizes this dissertation and draws conclusions of the completed work.

Chapter 2

Review of Analog and Mixed-Signal Testing

This chapter analyzes hardware architecture of self test compared with that of a recent ATE model. The comparison helps to understand how the hardware of self test can provide a complete alternative to the ATE. In addition, BIST and BOST approaches, which have been recently developed, are analyzed based on the understanding of the hardware architecture.

2.1 Hardware Architecture of Self Test and ATE

A common architecture for a mixed-signal circuit is shown in Figure 2.1. It includes analog input components, which are connected to the digital core (e.g. RAM, ROM or DSP) through an ADC. The digital output of the digital

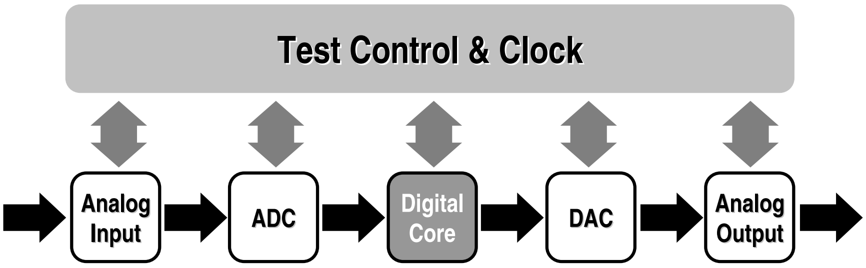


Figure 2.1: Simple Block Diagram of Mixed-Signal System

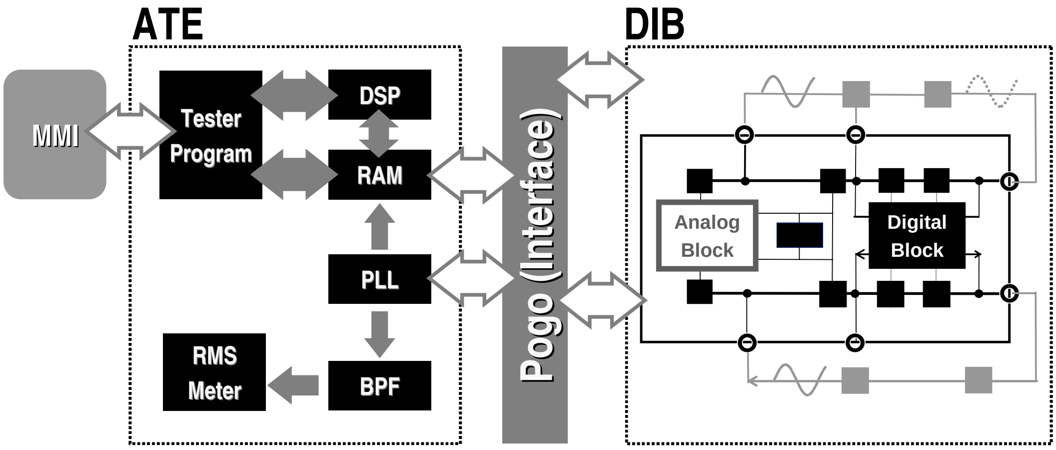


Figure 2.2: ATE Hardware Architecture

core is fed into a DAC, whose analog output is further transmitted to an analog output unit. By the transitional testing method, a ATE is applied and should provide both analog stimuli for the testing of analog parts (I/O blocks and ADC) and digital testing signals for the testing of digital components (DSP and DAC). Meanwhile, the ATE should be able to deal with the analog response as well as the digital response of the DUT. Such test environment is shown in Figure 2.2. The ATE is controlled through the tester program, and the tester hardware produces the testing analog and digital signals and feeds them into the DUT through pogo pins and Device Interface Board (DIB), which works as the interface between the ATE and the DUT. The digital response will be feed back directly into the load board and then returns to the ATE for further analyzing. The analog response is fed into the RMS meter on the ATE via a Band-Pass Filter (BPF) to get the testing parameters of the analog parts. The Phase Lock Loop (PLL) on the ATE provides the

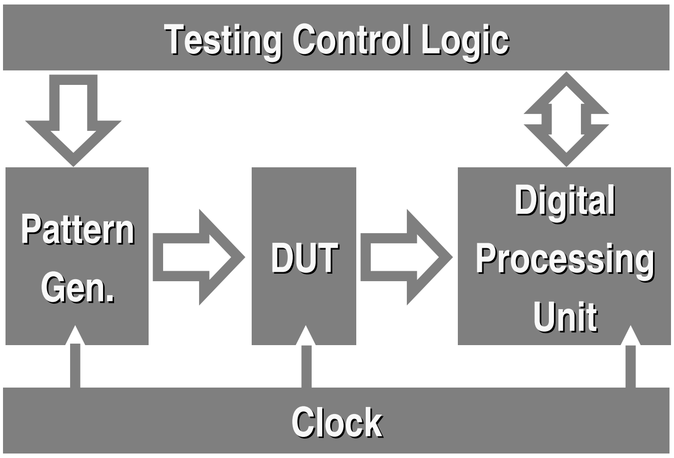


Figure 2.3: Block Diagram of Self Test Logic

primary clock for the ATE, the DIB and the DUT as well. The tester program can be modified through the Man-Machine-Interface (MMI) that is typically a workstation based on a UNIX or WINDOWS operating system so that the ATE can carry out different testing tasks as well as test different DUTs.

As an efficient alternative, self-test provides a convenient way to carry out the IC testing, whose architecture requires three additional components on chip, namely pattern generator, response processing unit, and testing controller as shown in Figure 2.3. Examples of pattern generators are a ROM with stored pattern or a chain of D-flip-flops. As a response processing unit, a comparator with a pre-set value or a linear feedback shift register (LFSR) is a typical implementation instance. A control unit is necessary to activate the test, manipulate the process and analyze the response. In general, several sub-tests can be carried out in one testing process. Sometimes the sampling rate of the DUT is different from that in other blocks. Hence the clock tree stimulated by a primary clock provides the clocks with different rates to the different blocks. It should be pointed out that self-test has some drawbacks yet: it needs overhead, power and additional circuits. Of course, it also needs some layout efforts. However, self-test does provide many advantages in reducing the testing cost. It can overcome many of the signal quality problems associated with the parasitic effects introduced by cables connecting the equipment to the device. Generally, deriving from its nature of on-chip performed test tasks, self-test has the following advantages.

- Costly external test equipment can be avoided.
- Parasitic effects introduced by cables connecting the equipment to the device can be avoided.
- Testing technology can be kept up-to-date with newer-generation integrated circuits.
- Reduction of test time through parallelization.
- Analog multiplexers to make the internal nodes accessible need not to be included in the design.

2.2 State of the Art for BIST and BOST approaches

Many performance-based test methodologies based on BIST and BOST solutions have been proposed for mixed-signal testing in order to reduce the costs associated with using testers and to enable testing of deeply embedded SoPs.

Azais [11]et al. presented a structure for the internal generation of a linear signal used with the histogram-based test technique. The structure is based on two highly linear ramp generators and a feedback control circuitry. In [33], the proposed BIST scheme in this work employs the delta-sigma modulation technique to generate the required linear ramp for testing the converters. Since they do not rely on the on-chip ADCs and DACs for stimulus generation and data conversion, the BIST strategy does not require the existence of both on-chip ADC and DAC, which makes it feasible for most mixed-signal IC's. However, a fundamental problem with these approaches is their need for a highly accurate signal to stimulate the DUT. Requirements for the stimulus input are typically substantially more precise than those of the DUT making the signal generator more challenging to design than the DUT itself and thereby raising the question of whether a test circuit is needed for the signal generator.

Several techniques [32, 59, 60, 83] have been published to generate on-chip linear ramps, but the results either depend largely on the accuracy of the additional components in the test circuitry, or have not been proven experimentally. An on-chip ramp generator can perform monotonicity and histogram tests of ADCs, yet the linearity of the on-chip ramp generator itself needs to be very high. A FFT approximation algorithm was developed for on-chip sinusoidal signal generation and analysis in; however, the area and power penalties associated with FFT calculations are large as indicated by the fact that the BIST approach was implemented in the largest Xilinx Virtex-II series Field Programmable Gate Array (FPGA).

In [31, 40], the authors attempt to test IP cores in an SoC by the embedded processor cores. The processor runs a test program that can deliver test patterns to the target IP cores via the PCI bus and then determine whether the chip is good or bad by verifying the test responses. This method mainly considers how to support scan testing using the system bus. One major problem with this method is that each core requires a buffer to hold the test data and a mechanism to convert the test data in each buffer into scan data for the associated core under test is needed. As a result, high area overhead is induced.

Simple and robust complete on-chip mixed-signal spectrum analyzers have been recently developed [47]. They performs the measurements in the analog domain, requiring small processing overhead. There is a special interest in the research community to look for solutions in the digital domain which aim to reduce the test cost and complexity. The advantage of this type of solutions are clear: robustness of digital circuitry, synthesis simplicity, reduced ATE requirements. However, the use of the approach is limited to low dynamic range applications.

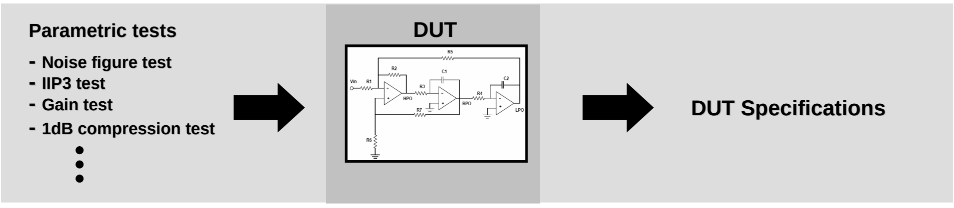
Hanai et al. introduced the BOST approach for testing the electrical characteristics of high resolution ADC/DAC unit statically. In order to achieve high measurement accuracy, this methodology reduces the noise from inside the tester by placing analog BOST on a performance board, and by placing a measuring circuit near the device to make the shortest length of wire. This minimizes the influence of external noise. Also the analog BOST includes the whole process from measuring to analyzing by self-control. The BOST is easily controlled by the circuitry implemented on the performance board and the processor installed in the tester. Therefore the test time can be reduced. However this approach requires the external conventional logic tester to generate noise caused by the characteristics of the long cable/wire between the performance board and the tester. Also the test cost is increased compared to on-chip test even though only fundamental functions of the conventional tester are used for the approach.

Chapter 3

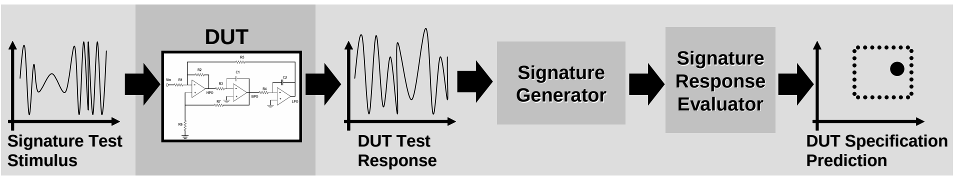
Prediction of Mixed-Signal Dynamic Performance Using Optimized Signature-Based Alternate Test

As mentioned in the previous chapters, short duration and optimized stimulus is applied to a DUT in the performance-based test. The response is analyzed to characterize the performance parameter of the DUT, without the need for a reference model for the DUT. Signature-based test is a common example of performance-based test. The signature test methodology includes applying a short duration test stimulus to the DUT and using the DUT response to estimate its performance as shown in Figure 3.1. Thus, compared to the conventional specification test, signature based test has the following advantages [62].

1. Multiple DUT specifications can be calculated using a single test response acquisition.
2. With conventional test, each specification test involves an overhead for setting up the instruments and the test configuration. On the other hand, the signature test approach uses a single test configuration and a single test stimulus, thereby reducing the overhead.



(a) Conventional Test



(b) Signature-Based Test

Figure 3.1: Signature-Based Test and Conventional Test

3. Finally, the instruments used to apply the signature test stimulus and measure the resulting response are much simpler and inexpensive, compared with the specialized instruments required for full specification test.

However there are several issues of the signature-based test as follows.

1. The analytical expressions using the signature resulting from the test cannot accurately represent the relationship between signatures and specifications.
2. The accuracy in the signature measurement is constrained by the BIST.
3. Unstable physical factors in the BIST circuitry can also cause signature values to be incorrect.

The Ternary Signal Representation (TSR) technique [89] improved the performance on the second problem mentioned above by using cost-effective BIST circuitry. However, the TSR technique still has the first and third problems. In short, if we use cost-effective BIST circuitry along with part of the TSR technique, the problems to be solved are the first and third problems.

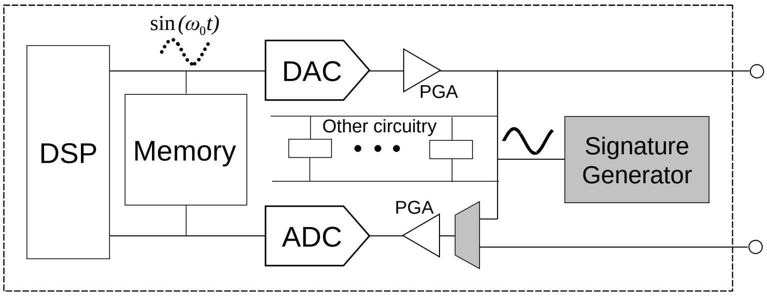
This chapter proposes a novel methodology called Optimized Signature-Based Alternate Test (OSBAT), to improve the accuracy in prediction of specifications using strong correlation mapping and to reduce test time and cost. The purpose of this proposed methodology is to generate correlations between parameters for prediction of specifications with the predictive accuracy of statistical alternate test [78]. This technique will then accurately predict specifications of a DUT by using the strong correlation. As a result, the proposed approach overcomes the first and third limitations above by predictive accuracy of statistical alternate test. The method has been evaluated using simulations in our previous work [38].

3.1 Motivation of Approach

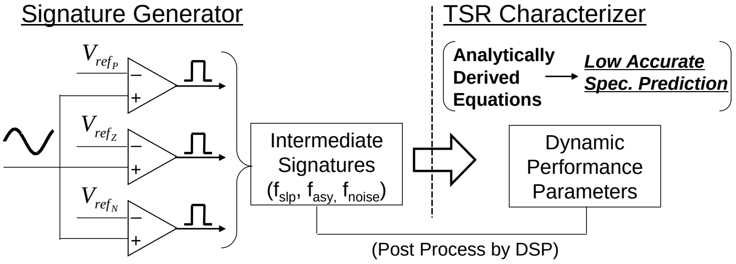
This section provides the overview of TSR technique as the motivation for the proposed methodology. The limitations of this technique are discussed.

3.1.1 Ternary Signal Representation (TSR)

The theory of the TSR methodology is discussed in detail in [89]. Due to its non-linear behavior, a ADC/DAC module generates harmonic distortion



(a) BIST Circuitry of TSR Technique



(b) Signature Generation and Specification Prediction of TSR

Figure 3.2: Overview of TSR Technique

and noise when a pure signal is applied to its input. The TSR signature generator (Figure 3.2) is used to analyze and predict the dynamic performance from the resultant output of a system.

An overview of the TSR technique is given using the DAC as an example in Figure 3.2. To predict the performance parameters of a DAC, a pure sine wave is applied to the input of the DAC and the resultant output signal is analyzed by the TSR signature generator.

The signature generator consists of three comparators with different reference voltages: positive, zero, and negative. The digital signals quantized by the three comparators are used to generate DC offset (f_{asy}), slope (f_{slp}), and noise (f_{noise}) of the fundamental signal by using the properties of harmonic distortion and noise. These intermediate signatures are discussed in Section 3.2.1 in detail. The TSR characterizer (Figure 3.2) then predicts the specifications of the DAC by using analytically derived equations with these signatures.

We define the *TSR technique* as the whole technique including the TSR signature generator and the TSR characterizer, and we assume that the *TSR signature generator* and the *TSR characterizer* are separate blocks.

3.1.2 Issues of TSR Technique

This section describes the solutions, which are provided by TSR technique, to overcome the limitations of signature-based test. The limitations of TSR technique are also discussed.

1. Conventional signature-based test cannot characterize accurate specifications of a DUT with signatures, because the correlation between them cannot be accurately derived due to lossy compression or high degree of dependence on mathematical relations. The TSR technique result shows a low error in prediction of specification [89]. However, the equations in the TSR characterizer cannot accurately describe the nonlinear relationship between the TSR signatures and the specifications, since the equations are analytically derived. Thus, there is a limit to the improvement of accuracy in measurement of specifications.

2. The accuracy in the signature measurement is constrained by the BIST. Methodologies minimizing the measurement error can lead to complexity in the BIST implementation. Thus, the measurement is limited by the BIST. This issue results in low accuracy measurement for signatures or specification parameters. The major advantages of using the TSR methodology are simple BIST circuitry and optimized signatures for cost-effective BIST. Thus, the TSR technique provides a solution to this problem [89].

3. Even though BIST circuitry is very simple, unstable physical factors in the BIST circuitry can result in errors in the signature value. The TSR technique generates three very optimized signatures (f_{slp}, f_{asy}, and f_{noise}) with simple BIST circuitry which consists of only three comparators as shown in Figure 3.2. However, even though the configuration

of TSR BIST circuitry is very simple, unstable physical factors in the BIST circuitry can result in incorrect signature values. For instance, the reference voltages of comparators can be unstable from unstable physical factors in the TSR BIST circuitry.

3.2 Optimized Signature-Based Test Methodology

This section shows the proposed OSBAT implementation for prediction of specifications using a strong mapping function.

3.2.1 Prediction of Performance Parameters with Optimized Signatures

If the output of the DAC/ADC shows nonlinear behavior, it generates noise and harmonic distortion when a pure input signal is applied to the system. The resultant system output can be expressed in the time domain as a sum of signals and noise as shown in Equation 3.1 [89].

$$\begin{aligned} f(t) = a_0 &- (a) \\ &+ \sum_{n=1}^{\infty} a_n \sin(n\omega_0 t) + \sum_{n=1}^{\infty} b_n \cos(n\omega_0 t) - (b) \\ &+ n(t) - (c) \end{aligned} \tag{3.1}$$

where (a) is DC bias, (b) is the fundamental input signal and harmonics, and (c) is the additive noise. ω_0 is the frequency of the fundamental signal. The harmonics, which are integer multiples of the tones present in the input signal, produce the distortion of the fundamental signal that is correlated with the tones, that is, odd-order harmonic distortion and even-order harmonic distortion. Odd-order distortion is produced by symmetrical non-linearities, and it is represented by shaping the resultant output to have sharper transitions at zero crossings in the fundamental signal without affecting the duty cycle of the resultant output. Even-order distortion is caused by asymmetrical non-linearities, such as unbalanced bias signals or faulty circuits and so on. The even-order harmonics change the duty cycle, and this results in destruction of the fundamental signal or DC offset.

Therefore, MARS model [22] is built based on the properties of these noise and harmonic distortion. We use this modeling approach for the accurate prediction of specifications. For demonstrating the proposed technique, a DAC is used as an example in Figure 3.3. The process consists of four steps.

Step1: Measurement of Actual Specifications

The N_s specifications, such as THD, SNR, and SINAD are actually measured from the output signal of the DAC. The measured specifications are used as a training set with which MARS generates correlation function.

Step2: Signature Generation

The output signal of the DAC is applied to the signature generator as shown in Figure 3.3. The signal is quantized by three comparators with different reference voltages into each of three digital data streams (f_{n_P}, f_{n_Z}, and f_{n_N}). The reference voltage for the positive portion (V_{ref_P}) can be any voltage between the maximum voltage and the average voltage of a given input signal,

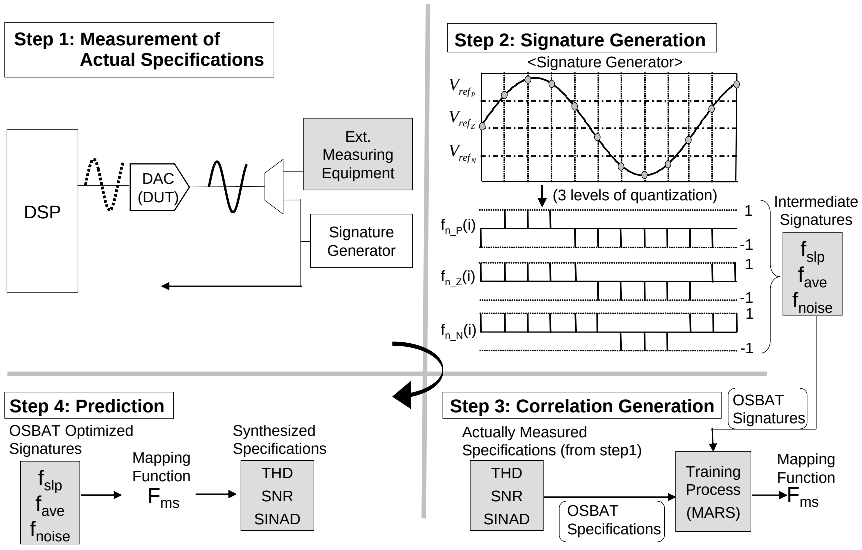


Figure 3.3: OSBAT Methodology

the reference voltage for the zero level (V_{ref_Z}) is the average voltage, and the reference voltage for the negative portion (V_{ref_N}) can be any voltage between the minimum voltage and the average voltage of a given input signal. The data streams are manipulated into three intermediate signatures f_{asy}, f_{slp}, and f_{noise} as followings. The signature generation details using properties of harmonics and noise are shown in Figure 3.4.

(i) Odd-Order Harmonic Distortion

If a DAC/ADC has non-linearities to cause odd-order harmonic distortion, and a single-tone sine waveform with zero DC bias is applied to the system, then Equation 3.1 can be rewritten as follows.

$$f(t) = \alpha_1 A \sin(\omega_0 t) + \alpha_3 A^3 \sin^3(\omega_0 t) + \alpha_5 A^5 \sin^5(\omega_0 t) + \cdots \qquad (3.2)$$

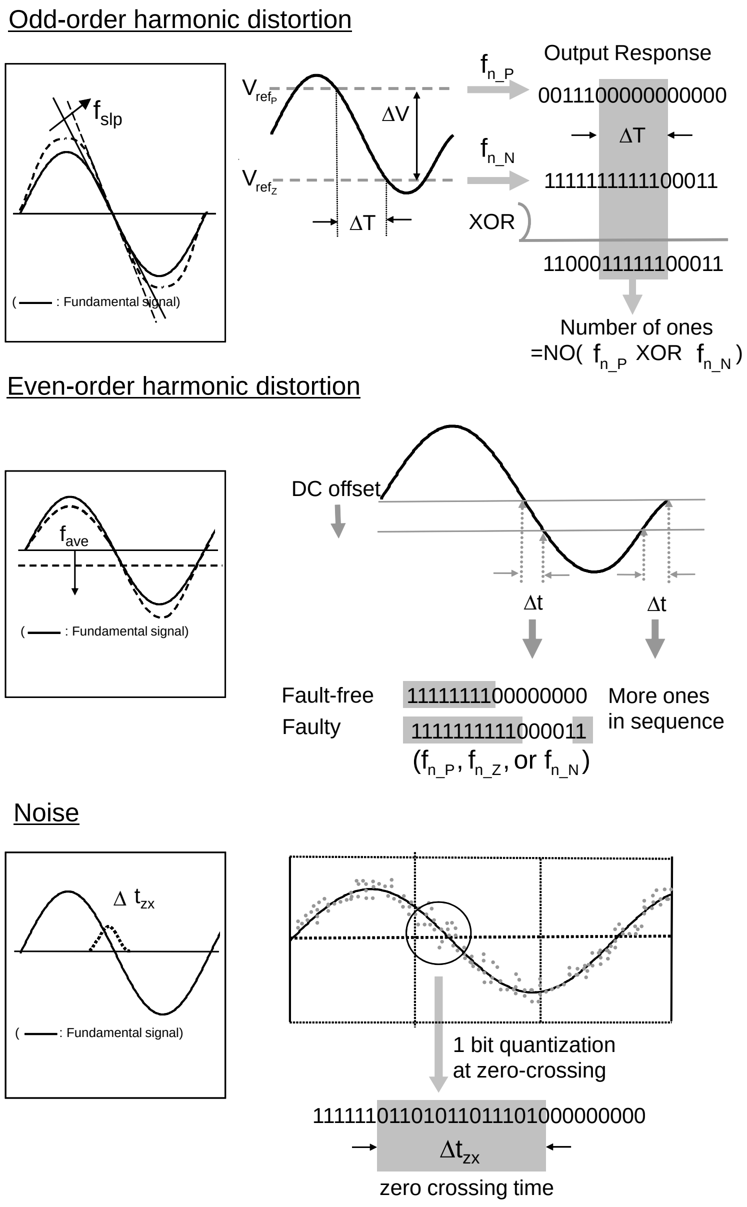


Figure 3.4: Properties of Harmonic/Noise and Signature Generation (Step2 Details in Figure 3.3)

where A is the amplitude of a fundamental signal, and α_1, α_3 and α_5 determine the amplitude of the harmonics. This produces a waveform that is wider at the top and bottom, and the waveform has sharper transitions at zero crossings maintaining the symmetry of the waveform as a square wave. For a sine waveform the highest slope of the signal occurs at the zero crossings. The slope (f_{slp}) is defined as the derivative.

$$\begin{aligned} f_{slp} &= \frac{\mathrm{d}f(t)}{\mathrm{d}t}|_{\omega_0 t = 2\pi n} \\ &\simeq (\alpha_1 A + 3\alpha_3 A^3 + \cdots)\omega_0 \end{aligned} \tag{3.3}$$

This slope can represent the degree of the harmonic distortions in the fundamental signal. Thus, the higher slope(f_{slp}) means more distortion as shown in Figure 3.4.

The slope at zero crossings is estimated using f_{n_P} exclusive-ORed with f_{n_N} and it is expressed as given in Equation 3.4.

$$f_{slp} = \frac{V_{ref_P} - V_{ref_N}}{NO(f_{n\_P}\ XOR\ f_{n\_N})T_s} \tag{3.4}$$

where NO is the number of ones in the sampling data and T_s is the sampling time.

(ii) Even-Order Harmonic Distortion

If a DAC/ADC has non-linearities causing even-order harmonic distortion and a single-tone sine waveform with zero DC bias is applied to the system, then Equation 3.1 can be rewritten by a Taylor expansion as follows.

$$f(t) = \alpha_1 A \sin(\omega_0 t) + \alpha_2 A^2 \sin^2(\omega_0 t) + \alpha_4 A^4 \sin^4(\omega_0 t) + \cdots \tag{3.5}$$

where A is the amplitude of an input signal and α_1, α_2, and α_4 determine the amplitude of the harmonics. This produces a waveform with a different duty cycle which is not symmetrical, and destroys the fundamental waveform. Thus a DC offset caused by this distortion is determined by the average value (f_{ave}) in the time domain as shown in Figure 3.4. and it can be calculated as the following equation.

$$f_{ave} = \frac{1}{T}\int_0^T f(t)\,\mathrm{d}t \tag{3.6}$$

where T is the period of the fundamental waveform. Therefore the data stream from signature generator for faulty circuits generates more ones in sequence by decreasing the DC offset as shown in Figure 3.4. The degree of the even-order harmonic distortion can be expressed using sum of the data streams(f_{n_P},f_{n_Z}, and f_{n_N}) as Equation 3.7.

$$f_{ave} = f_{slp}\frac{T_s}{2}\frac{\sum_i^{NS}(f_{n\_P}(i) + f_{n\_Z}(i) + f_{n\_N}(i))}{3} \tag{3.7}$$

where NS is the total number of samples and i is the sampling order. Then this change of DC offset results in the asymmetry in this distortion. The degree of asymmetry (f_{asy}) provides the ratio between the positive portion (PP) to the negative portion (NP) relative to DC offset in the waveform (Equation 3.8). Thus, the asymmetry more accurately describes the DC offset than the average value, and the degree of the asymmetry in this distortion can be estimated using the calculated average value (f_{asy}). We use the degree of the asymmetry to find the more exact effect of even-order harmonic distortion by the following equation.

$$f_{asy} = \frac{PP(f(t) - f_{ave})}{NP(f(t) - f_{ave})} \tag{3.8}$$

The degree of the asymmetry can better represent how even harmonics distort the fundamental signal. f_{asy} can be expressed using Equation 3.7 and 3.8 as follows.

$$\begin{aligned} f_{asy} = {} & \frac{\sum_i^{NS} PP(f_{n\_Z}(i))}{\sum_i^{NS} NP(f_{n\_Z}(i))} + \frac{\sum_i^{NS} PP(f_{n\_N}(i))}{\sum_i^{NS} NP(f_{n\_P}(i))} \\ & + \frac{\sum_i^{NS} PP(f_{n\_P}(i))}{\sum_i^{NS} NP(f_{n\_N}(i))} \end{aligned} \tag{3.9}$$

(iii) Noise Effect

If a DAC/ADC has additive noise ($n(t)$) and a single-tone sine waveform with zero DC bias is applied to the system, then Equation 3.1 can be rewritten as follows [16, 24, 27].

$$f(t) = a_1 \sin(\omega_0 t) + n(t) \tag{3.10}$$

where $n(t)$ represents zero-mean additive Gaussian noise having standard deviation, while $a_1 \sin(\omega_0 t)$ is the converter stimulus signal, and $f(t)$ is the converter output sequence. Notice that $n(t)$ models noise sources located inside the DAC/ADC under test, and the amplitude distributions are Gaussian. These noise values are superimposed on the fundamental signal. The resultant output waveform at a given amplitude also shows a Gaussian distribution. Then the width of the Gaussian distribution corresponds to the

RMS noise. The width of the Gaussian distribution can be represented by the standard deviation σ which corresponds to the half width of the peak at about 60% of the full height, as can be calculated from Equation 3.11.

$$P(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-0.5\left(\frac{x-\mu}{\sigma}\right)^2} \tag{3.11}$$

where μ and σ are the mean and standard deviation of the distribution. In the case of odd-order harmonic distortion and noise effects, we first estimate the zero crossing time (t_{zx}) of the fundamental signal. In fact, t_{zx} is the average value with a variance. The variance can be seen as noise effects if we assume that most noise is random and additive. In addition, the variance will occur in a similar way at any given voltage level of the fundamental signal. Thus RMS noise can expressed as the following equation.

$$n_{RMS} = \sqrt{\left(\frac{1}{2N}\sum_{i=1}^{2N}(t_{zx}(i) - t_{zx0})^2\right)} \tag{3.12}$$

where t_{zx0} is the average value of the fundamental signal. N is the number of cycles of the fundamental signal. Thus the noise effect (f_{noise}) can be estimated by zero crossing time variation (Δt_{zx}) as shown in Figure 3.4. Noise effects(f_{noise}) can be also expressed using Δt_{zx} as Equation 3.13. Therefore it represents the noise effects in the fundamental signal.

$$f_{noise} = \Delta t_{zx} \frac{f_{slp}}{2} \tag{3.13}$$

Step3: Correlation Generation

As explained in Step2, noise and distortion of the fundamental signal strongly

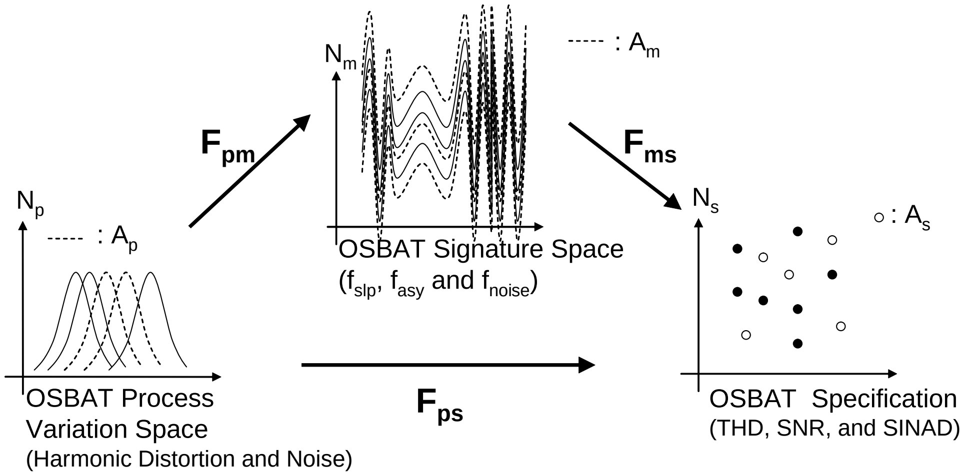


Figure 3.5: Signature Space and Specification Space for OSBAT Method

affect the intermediate signatures f_{asy}, f_{slp}, and f_{noise}. Therefore, noise and distortion in a DUT can be considered as the *OSBAT process variation space*, p and the intermediate signatures of TSR can be considered as the *OSBAT signature space*, m in Figure 3.5. Then, the measured specifications from Step1 can be considered as the specification space. We can then find the mapping function F_{ms} between the specifications and intermediate signatures of TSR. The intermediate signatures as OSBAT optimized signatures and the actually measured specifications are used as a training set for MARS, which generates the strong correlation mapping function F_{ms} with these training sets.

Step4: Prediction

We can then test numerous DUT ensembles with the mapping function generated from Step3. If the OSBAT signatures of many DUT ensembles are applied to the correlation function F_{ms} as input to be tested, the specifications accurately predicted by OSBAT methodology are finally generated, called synthesized specifications [78] such as THD, SNR and SINAD as shown in Figure 3.3. The synthesized specifications are used as pass or fail criteria for the DUTs.

3.2.2 Extended OSBAT Method for Loopback Test

Loopback test of mixed signal ICs provides a low-cost test solution. However this method suffers from fault masking caused by the uncorrelated interaction between non-functionally related components in loopback mode. In this section, we show how the proposed method can be applied to the loopback mode to remove the fault masking problem.

In Section 3.3.1, the strong correlation mapping function is generated between signatures and specifications in the example with a DAC. Equation 3.14 below describes the mapping function, $F_{ms\_DAC\_THD}$, generated for the characterization of THD in DAC channel (THD_{DAC}).

$$THD_{DAC} = F_{ms\_DAC\_THD}(f_{slp}, f_{asy}, f_{noise}) \tag{3.14}$$

$F_{ms\_DAC\_THD}$ is generated through the training process with the signatures and THD_{DAC} as shown in Equation 3.14.

For loopback mode as shown in Figure 3.6, the converted analog signal by the tested DAC is looped back to the ADC and digitized. As mentioned before, the loopback ADC output is the signal affected by noise and harmon-

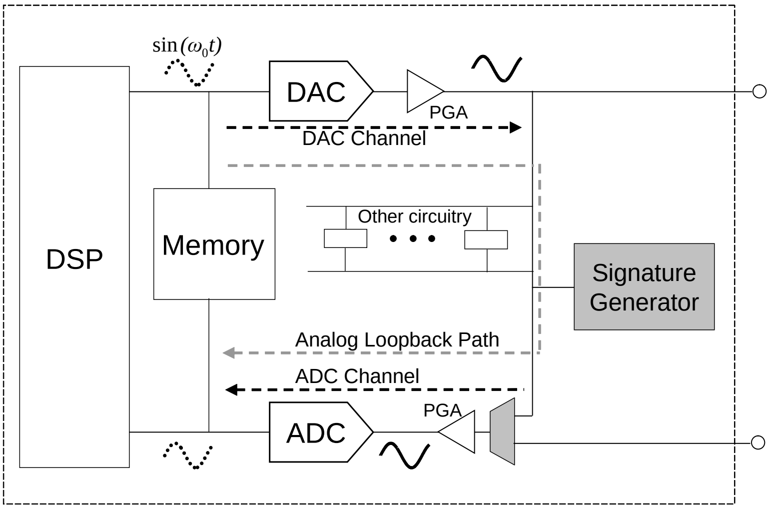


Figure 3.6: Loopback Test Scheme for OSBAT Methodology

ics from the DAC and ADC channel. Thus loop-backed specifications are expressed with the performance of DAC and ADC. The mapping function (Equation 3.15) is generated through the training process with the individual channel specifications and the loop-backed channel specifications.

$$THD_{loop} = F_{ms\_loop\_THD}(THD_{DAC}, THD_{ADC}) \tag{3.15}$$

where THD_{loop} and THD_{ADC} are respectively THD of analog loopback channel and ADC channel. THD_{loop} is calculated by applying Fast Fourier Transform (FFT) to the loop-backed signal. If THD_{loop} and THD_{ADC} are transposed, the mapping function can be expressed as

$$THD_{ADC} = \widetilde{F}_{ms\_loop\_THD}(THD_{DAC}, THD_{loop}) \tag{3.16}$$

Equation 3.16 can be re-written by Equation 3.14 as follows.

$$THD_{ADC} = \widetilde{F}_{ms\_loop\_THD}(F_{ms\_DAC\_THD}(f_{slp}, f_{asy}, f_{noise}), THD_{loop}) \qquad (3.17)$$

If we re-write the function, $\widetilde{F}_{ms\_loop\_THD}$, with the variables, THD_{DAC} and THD_{loop}, Equation 3.17 can be expressed as follows.

$$THD_{ADC} = \widetilde{\widetilde{F}}_{ms\_loop\_THD}(f_{slp}, f_{asy}, f_{noise}, THD_{loop}) \qquad (3.18)$$

Similarly, the mapping functions for the characterization of SNR and SINAD in ADC Channel can be expressed as follows.

$$SNR_{ADC} = \widetilde{\widetilde{F}}_{ms\_loop\_SNR}(f_{slp}, f_{asy}, f_{noise}, THD_{loop}) \qquad (3.19)$$

$$SINAD_{ADC} = \widetilde{\widetilde{F}}_{ms\_loop\_SINAD}(f_{slp}, f_{asy}, f_{noise}, THD_{loop}) \qquad (3.20)$$

Thus the mapping functions, $\widetilde{\widetilde{F}}_{ms\_loop\_THD}$, $\widetilde{\widetilde{F}}_{ms\_loop\_SNR}$ and $\widetilde{\widetilde{F}}_{ms\_loop\_SINAD}$, characterize the ADC specifications using the correlation with the signatures of the DAC channel and the performance parameters of loop-backed channel. In fact, these functions are generated based on the MARS modeling for loopback test as follows.

The signatures of the DAC and the loop-backed performance parameters can be considered as the *OSBAT signature space*, m in Figure 3.5. Also, noise and distortion in DUTs can be considered as the *OSBAT process variation space*, p. Then, the measured ADC specifications can be considered as the specification space, s. Similarly as discussed in Section 3.2.1, the signatures as OSBAT optimized signatures and the actually measured specifications are used as a training set for MARS. Thus, the correlation function expressed as Equation 3.18 is generated through the mapping process with the DAC signatures, the loop-backed performance parameters, and the performance parameters of the ADC. We will show hardware measurements to evaluate the performance of the proposed method in loopback mode in Section 3.3.3.

3.3 Experimental Results

In this section, we present hardware measurements to validate the proposed technique. Hardware measurements were performed on commercial ladder DACs (Analog Devices AD9764). Also, other hardware measurements were performed with commercial DACs and ADCs (AD9764 and National Semiconductor ADC14L105) to evaluate the performance of the proposed method on the application for loopback mode.

3.3.1 Hardware Results

Hardware measurements with a commercial converter (Analog Devices AD9764) [6] were performed to prove the validity of the method as shown in Figure 3.7.

3.3.1.1 Hardware Measurement Set-up

A converter board, AD9764EB, has a DAC (AD9764) with 14-bit resolution, which is the DUT. National Instruments (NI) digitizer, NI5620, was used for data acquisition of the output signal of AD9764EB. The digitizer

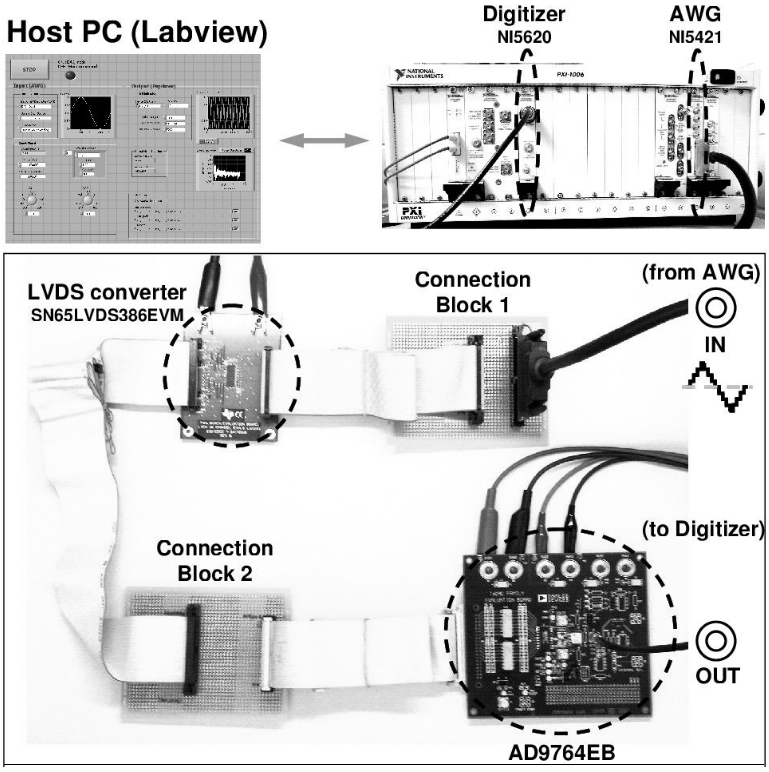


Figure 3.7: Hardware Measurement Setup

has 14-bit resolution and supports sampling rates up to 64 MSPS. NI Arbitrary Waveform Generator (AWG), NI5421, was used to generate a 125kHz sine waveform as an input stimulus to the AD9764EB and it supports sampling rates up to 100 MSPS and has 16-bit resolution. The oversampling ratio (OSR) was 256.

The Low-Voltage Differential Signaling (LVDS) converter converts a signal voltage level from LVDS to TTL. The host PC is connected to the backplane with the NI5620 and the NI5421 ports, and the data acquisition (DAQ) program on the host PC gets data from the ports.

3.3.1.2 Hardware Measurement Results

A 125 kHz single-tone sine waveform generated by AWG is applied to the input of AD9764EB. The output of a DAC was obtained by the digitizer. The post-processing on the host PC predicts the specifications with the signal. The Data Acquisition (DAQ) program based on the Labview distortion analysis library provides the actual value of the specifications to compare with the predicted specifications based on the proposed method. In order to inject a fault in the AD9764, we performed measurements under various stress conditions by sweeping the power supplies and the input amplitude/frequency, and reconfiguring the gain and by combining them. When the power supply is swept, transistors can be forced into various regions of operation and the transistors may be working beyond the acceptable specifications [34]. Therefore we have very carefully injected faults into a device through trial and error, in order to closely describe how an actual fault in the DUT affects the DUT output. Also the experiments evaluate the performance of our method in wide range of harmonic and noise values. Thus compared to noise level typically existing in faulty circuits, we have injected more faults by controlling amplitude/frequency and gain values.

We compared the performance of the OSBAT methodology with the TSR technique. For the training set, 52 DUTs were used and 52 DUTs were used in the validation set. The THD, SNR, and SINAD of a DAC were considered as the specification parameters for our hardware measurements.

(i) Classification Accuracy

The degree of misclassification is one of ways to represent the accuracy of the OSBAT methodology. The DUTs were classified by comparing synthesized performance parameters of the OSBAT methodology with the specification limits of the DUT. Table 4.3 shows the specification limits used for classification. The results of the DUT classifications using the actual and the predicted specification values are summarized in Table 5.4. The amount of misclassification, 4 (7.7%), indicates that the classification accuracy is very high.

(ii) Dynamic Performance Parameters

Figure 3.8 shows the comparison of predictive THD of the OSBAT technique with the TSR technique. The error of the OSBAT was reduced by 1.4dB compared with the THD error based on the TSR technique. Thus the pre-

Table 3.1: DUT Specification

Performance Parameter	**Specification Limits**
THD	-47.5[dB]
SNR	46.0[dB]
SINAD	46.0[dB]

Table 3.2: Classification Accuracy

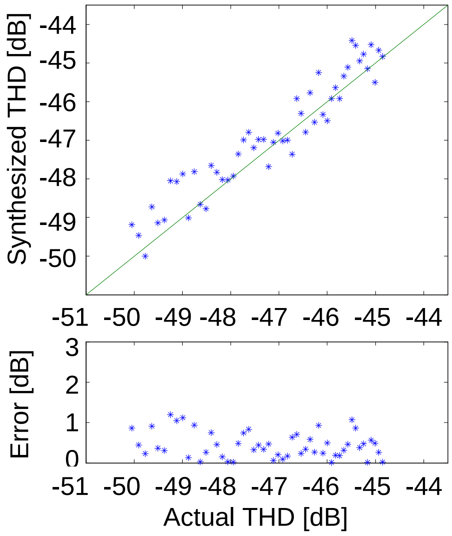
Performance Parameter	**Pass**	**Fail**
Actual Classification	24	28
Predicted Classification	20	32

dictive THD of the OSBAT technique is more accurate than that of the TSR technique.

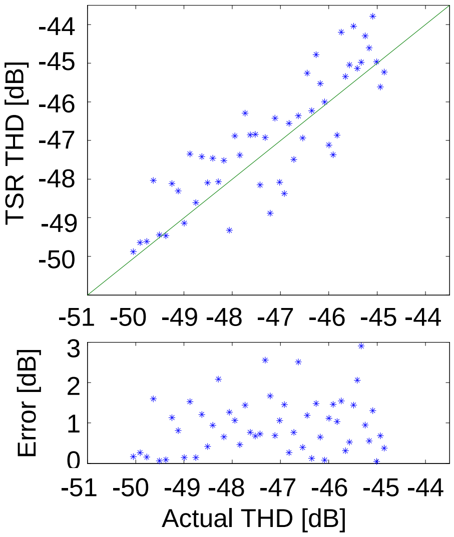
Consider the SNR in Figure 3.9. The SNR error distribution of the OSBAT methodology is generally stable compared with the SNR error of the TSR technique. As shown in Table 3.3, the error of the OSBAT was decreased by 2.3dB compared with the SNR error, based on the TSR technique.

For SINAD, the error of the OSBAT methodology was also reduced by 2.1dB compared with the SINAD error from the TSR technique. Table 3.3 summarizes the statistics of the predicted specification errors. The hardware measurements show that the prediction error is increased by approximately 1dB compared to the simulation results. This is primarily due to the measurements error, which we observed to be ±1dB.

Table 3.4 gives the correlation coefficients of specifications obtained using OSBAT and TSR techniques. The correlation coefficient of specifications is defined as the ratio between the RMS value of actual specification and the

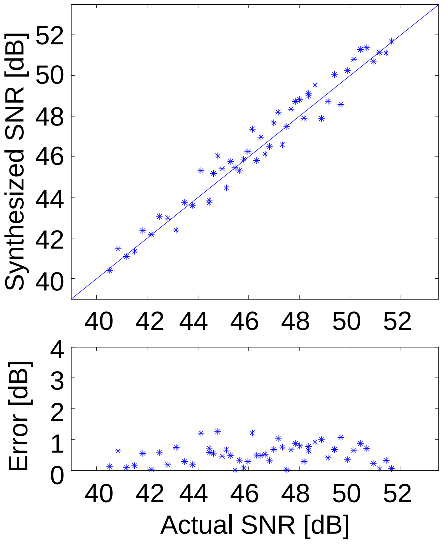


(a) THD based on proposed method

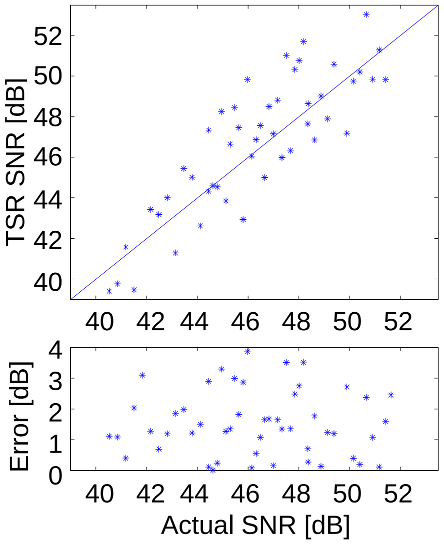


(b) THD based on TSR

Figure 3.8: THD Based on Proposed Method and TSR (Hardware Measurement Results)

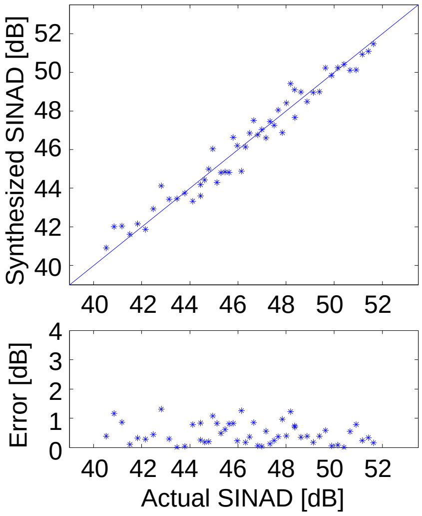


(a) SNR based on proposed method

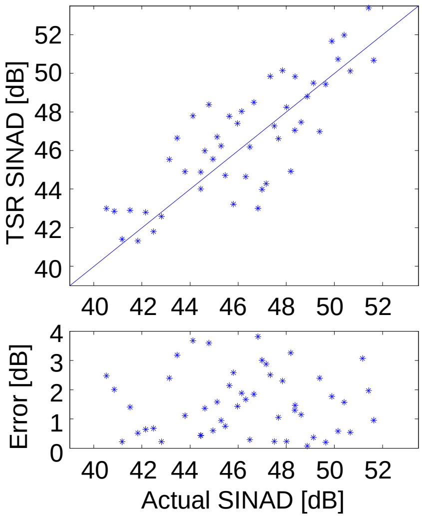


(b) SNR based on TSR

Figure 3.9: SNR Based on Proposed Method and TSR (Hardware Measurement Results)



(a) SINAD based on proposed method



(b) SINAD based on TSR

Figure 3.10: SINAD Based on Proposed Method and TSR (Hardware Measurement Results)

Table 3.3: Specification Errors of OSBAT and TSR Technique for Hardware Measurements

Spec.	**OSBAT**	**TSR**
THD	0.80±0.79[dB]	1.51±1.48[dB]
SNR	0.85±0.83[dB]	2.02±1.98[dB]
SINAD	0.88±0.85[dB]	1.91±1.88[dB]

Table 3.4: Correlation Coefficients between Actual and Predicted Values of Performance Parameters

Performance Parameter	**OSBAT**	**TSR**
THD	0.9736	0.9241
SNR	0.9576	0.8984
SINAD	0.9681	0.9073

RMS value of predicted specification. Thus, these coefficients being close to unity illustrate that the predictive accuracy of OSBAT method is very high.

3.3.2 Effect of Non-Idealities

The measurements obtained in various practical situations would be subject to the effects of various non-idealities. The sensitivities of the OSBAT technique to three common non-idealities are presented by results of the hardware measurements in this section.

3.3.2.1 Instability of Comparator in Signature Generator

The instabilities in each reference voltage of three comparators affect the correlation coefficient of predicted specifications. The post-process functions on the host PC collect the sine wave from AD9764EB. The functions quantize the signal to emulate the behavior of comparators used for our ap-

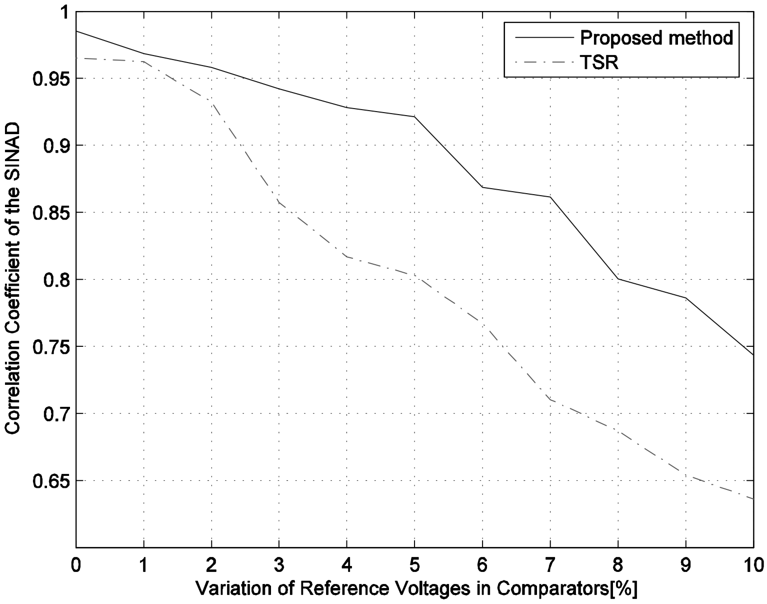


Figure 3.11: Effect of Instability of Comparator on Correlation Coefficients of SINAD

proach. We incorporated the variation in comparator reference voltages into the functions, in order to represent instability of the comparator in the signature generator.

Figure 3.11 shows the effect of instabilities of comparators on the predicted SINAD correlation coefficient based on the OSBAT technique and the TSR technique. It can be observed that the SINAD correlation coefficient based on the TSR technique decreases more sharply compared to using the OSBAT methodology in the variation range from 1% to 4%. While the correlation coefficient of SINAD based on the OSBAT technique remains more than 0.9 until the variation of 5%, the correlation coefficient of the TSR technique is already under 0.85 at 5%. A variation of 100% is defined as the voltage difference between zero reference voltage and positive or negative voltage.

The rate of decrease in correlation coefficients represents the sensitivity of the correlation coefficients with respect to the unstable reference voltages of the comparators. Lower sensitivity indicates relatively small change in predictive accuracy, and our method is less sensitive to the unstable reference voltage than the TSR technique. The results from our method with lower sensitivity indicate that the change in predictive accuracy of our method is relatively small compared with the TSR technique. As a result, we show that the proposed technique has improved performance on the third limitation of the TSR technique in Section 3.1.2.

3.3.2.2 Effect of Sampling Time of Signature Generator

This section shows how the performance of our method varies with an increase in the sampling time of the comparators. We varied the sampling time of the NI5620 in order to emulate the change in the sampling time of comparators.

The slope of the fundamental signal, f_{slp}, is measured at the zero crossing time. If the sampling time increases, the slope is measured as a lower value than the actual slope by the TSR signature generator. Figure 3.12 shows this effect of the change in sampling time on the correlation coefficient of SINAD for the TSR technique and the OSBAT methodology. In order to measure the slope, there should be at least two sampling points within a half period of in-

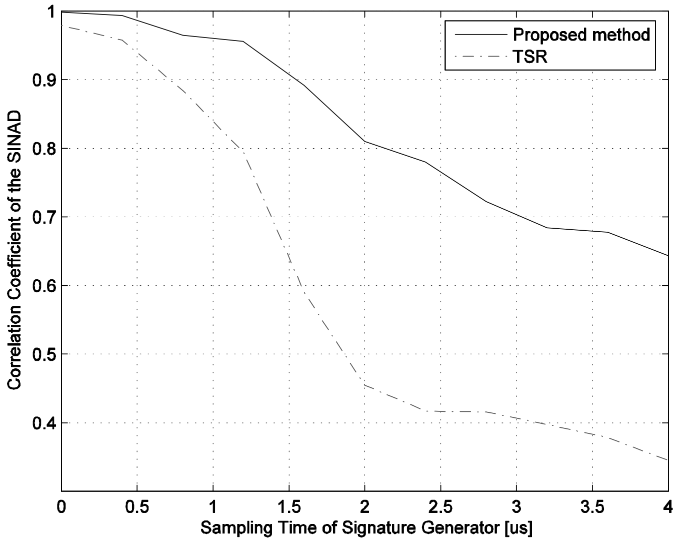


Figure 3.12: Effect of Sampling Time Variation to Correlation Coefficient of SINAD

put sine wave, which includes both the maximum and minimum peak voltages of the sine waveform. This means that the sampling time must be less than 4μsec to measure the slope.

For the TSR technique, the correlation coefficient of SINAD dramatically decreases as shown in Figure 3.12. Even though there are at least two points within a half period for the TSR technique, the analytically derived equations of the TSR cannot exactly measure the SINAD due to lower correlation between signatures and specifications.

On the other hand, the coefficient of the OSBAT technique decreases gradually. If there are at least two sampling points, the OSBAT method generates strong correlation with the specifications and the signatures. Thus, the OSBAT method reduces test costs, since lower frequency comparators can be used, when compared with the TSR technique.

3.3.2.3 Effect of Training Set Size

The effect of the training set size, which is used to derive the mapping function set, is evaluated for the accuracy of the OSBAT technique in this section. Training sets of different sizes were used to derive the mapping function set and then these functions were used to predict the performance parameters of 52 DUTs. Table 3.5 provides the prediction errors of OSBAT as the training set increases by 10. The results show that the predictive accuracy of our method generally improves with the size of the training set.

Table 3.5: OSBAT Prediction Errors for Difference Training Set Sizes

Training Set Size	**THD**	**SNR**	**SINAD**
12	0.8096[dB]	0.8546[dB]	0.8897[dB]
22	0.8644[dB]	0.7422[dB]	0.8041[dB]
32	0.6784[dB]	0.7925[dB]	0.6481[dB]
42	0.4876[dB]	0.5475[dB]	0.5134[dB]
52	0.4512[dB]	0.5067[dB]	0.4951[dB]

3.3.3 Hardware Measurements for Loopback Test

In order to evaluate the performance of the proposed method in the loopback mode, we will analyze the dynamic specification errors based on hardware measurements. Hardware measurements with the commercial converters (National Semiconductor ADC(ADC14L105) and Analog Devices DAC(AD9764)) were performed for loopback mode. ADC14L105 is a monolithic pipelined data

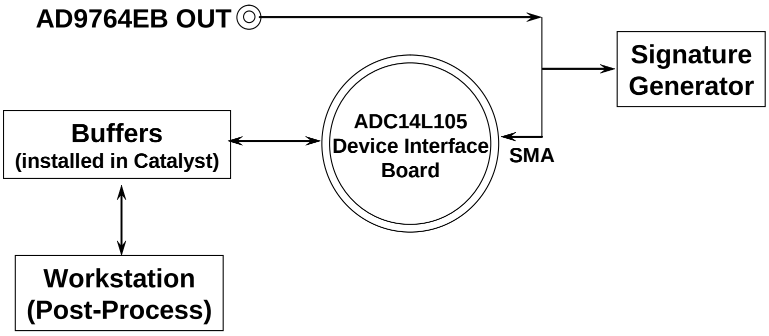


Figure 3.13: Hardware Measurement Setup for Loopback Test

converter with 14bit resolution and 105MSPS sampling speed. Also, the ADC device interface board was manufactured with input and output pins for testing and it was used for the connection between ADC and test equipments. The Teradyne Catalyst tester and the HP 8644B synthesizer were used to actually measure the ADC specifications. Also, an AWG and a digitizer installed in the tester were used for data acquisition.

The collected data from the signature generator were post-processed by workstation to generate the mapping function for testing a DAC on the AD9764EB. The signature generator was emulated by simulation on the workstation. As shown in Figure 3.13, the converted analog signal by the tested DAC is loop-backed to the ADC(ADC14L105) and digitized. The digitized data were transferred to the workstation through the buffers installed in Catalyst and the post-process was performed to generate the correlation function between the DAC signatures, the loop-backed performance parameters, and the ADC specifications. In order to inject a fault in the DAC and ADC, we performed measurements under various stress conditions by sweeping the power supplies, the input amplitude/frequency, and so on. 12 DUTs were used for the training set, and 18 DUTs were used for validation set. Figure 3.14, 3.15 and 3.16 show the predicted value of the performance parameters for 18 validation DUTs, and Table 4.2 summarizes the statistics of the prediction errors.

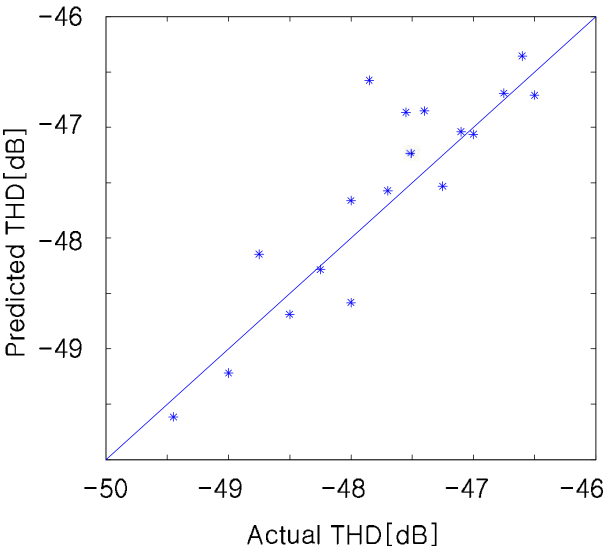
Table 3.6: Specification Errors of Hardware Measurements

Spec.	**DAC Channel**	**ADC Channel**
THD	0.79±0.77[dB]	0.89±0.87[dB]
SNR	0.81±0.78[dB]	1.19±1.16[dB]
SINAD	0.82±0.81[dB]	1.31±1.27[dB]

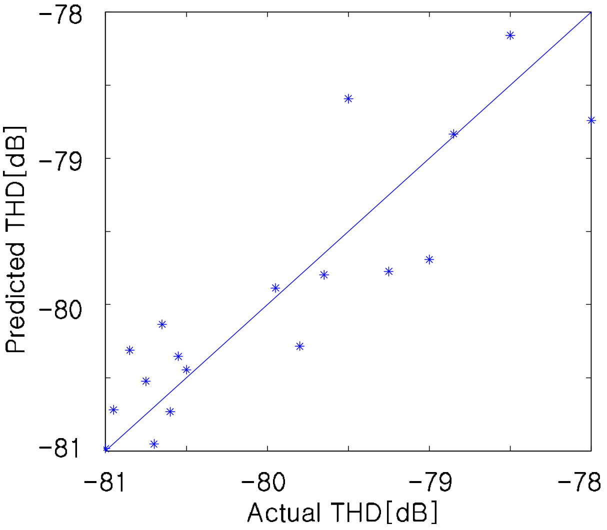
As shown in Table 4.2, the mean and standard deviation of prediction errors were less than 1.5dB. Also, the performance errors for the ADC channel are higher than those of the DAC channel by 0.1 to 0.5dB. This results from the fact that the calculation of specifications for the ADC depends on the signatures of the DAC which already has some errors, as can be seen from Equation 3.18.

3.4 Summary

In this chapter, we proposed a novel methodology for accurate predictions from optimized signatures. A sinusoidal signal is applied to a DUT and the resultant output signal is manipulated into the optimized signatures by using low-cost comparators and digital circuits. To predict the performance

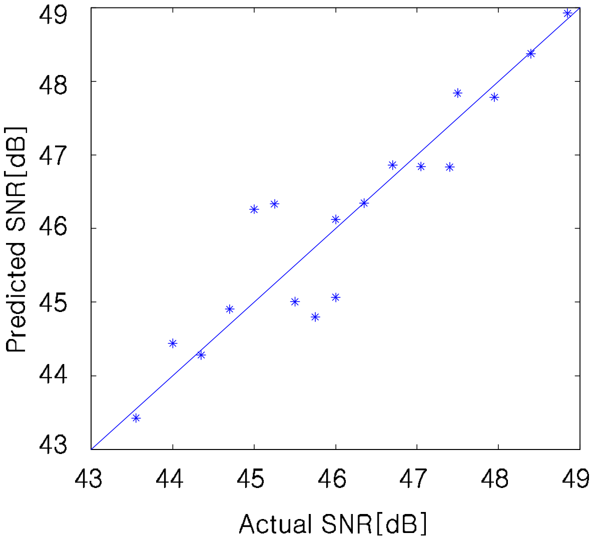


(a) THD of DAC Channel Based on Proposed Method and TSR

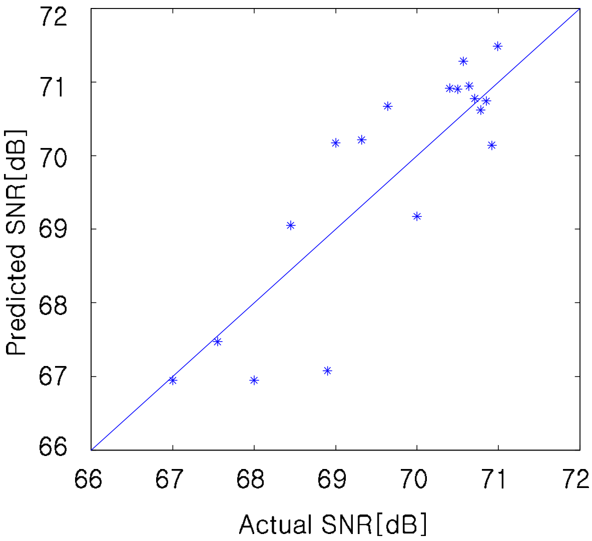


(b) THD of ADC Channel Based on Proposed Method and TSR

Figure 3.14: THD Results for Loopback Test (Hardware Measurement Result)

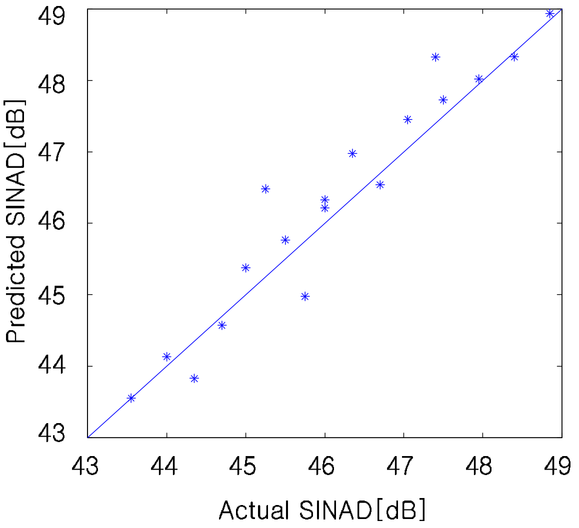


(a) SNR of DAC Channel Based on Proposed Method and TSR

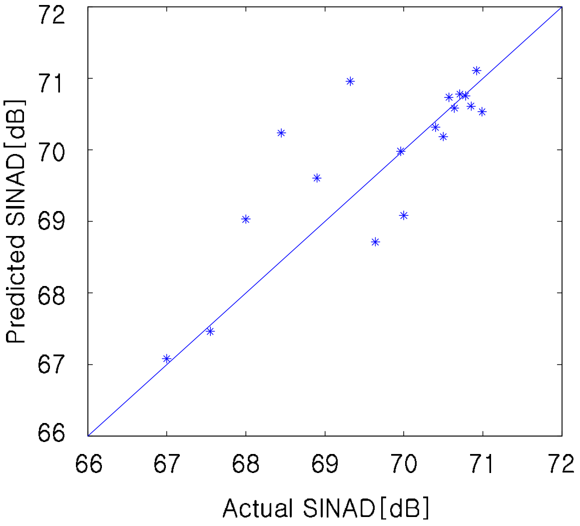


(b) SNR of ADC Channel Based on Proposed Method and TSR

Figure 3.15: THD Results for Loopback Test (Hardware Measurement Result)



(a) SINAD of DAC Channel Based on Proposed Method and TSR



(b) SINAD of ADC Channel Based on Proposed Method and TSR

Figure 3.16: THD Results for Loopback Test (Hardware Measurement Result)

parameters of a DUT, the correlation functions which map the obtained signatures to the specifications are generated by a regression technique. The proposed method provides improved performance on the problems associated with representing the exact relationship between signatures and specifications due to nonlinear characteristics. The results of hardware measurement with DACs (AD9764) show error reductions of THD, SNR and SINAD as 1.4dB, 2.3dB, and 2.1dB compared with the TSR technique. In addition, we evaluated the sensitivities of this technique to common non-idealities, such as the variations of reference voltages and sampling rate of BIST circuits. The results from our method with low sensitivity indicate that our predictive accuracy is reliable and stable. Also another set of hardware measurements was performed with commercial DACs and ADCs (AD9764 and National Semiconductor ADC14L105) to evaluate the performance of the proposed method on the application for loopback mode. The results show that the proposed method deals with the fault masking problem in loopback tests, and produces lower errors when predicting specifications.

Chapter 4

Transformer-Coupled Loopback Test for Differential Mixed-Signal Specifications

The previous chapter has explained the statistical alternative test methodology to characterize the dynamic performance using low-cost comparators. A low-cost comparator has limitations in the sampling performance of high frequency applications. High-speed mixed-signal devices are designed using deep submicron process technologies, that generate a new class of defects and require faster, more accurate high-speed mixed-signal testing [19]. This chapter discusses the test methodology for high-speed mixed-signal circuits.

Most high-performance, high-speed analog and mixed-signal components such as Low Noise Amplifiers (LNAs) and data converters are currently designed using differential signaling. Most external test equipments used in conventional tests have single-ended I/O and use a coaxial cable to connect to the DUTs.

However, no differential network device (DND) can avoid inherently the imbalance problem due to parasitic coupling capacitances in the differential terminals. The imbalance results in additional distortion or noise on the output of the DND. The distorted and noisy signal is delivered to the DUT input, thereby degrading the DUT performance [37].

BIST schemes have been suggested and developed to overcome the limitations of conventional test, such as limited test I/O accessibility as well as high test cost [25]. Among the various approaches for the implementation of BIST schemes, a loopback test method has been proposed as an efficient solution [26] [15], and various DfT circuits for loopback test schemes have been proposed [39, 53, 73, 89]. However most mixed-signal BIST approaches including loopback test have not been developed to deal with the issues in differential signaling due to the following reasons.

1. The magnitude and phase imbalance introduced by DfT circuitry significantly degrades DUT performance parameters, thereby reducing test accuracy and fault coverage.
2. Even if an analog self-test approach is developed to overcome the imbalance introduced by a DND, this could lead to greater complexity in DfT circuit implementation.

This chapter proposes a novel *Transformer-Coupled Loopback Test* for individual mixed signal specifications on differential signaling to overcome these limitations and realize cost-effective test.

4.1 Imbalance Issue of Differential Network Circuit and DUT Performance

This section shows how imbalance introduced by DND as a DfT circuit in loopback test affects the differential DUT performance. To better understand this imbalance effect, we use a single transformer as an example of a DND, and a differential ADC is used as a DUT. In fact, there are several parameters to represent the performance of a RF transformer, such as insertion loss, return loss, and magnitude and phase imbalance. We focus on magnitude and phase imbalance which are key factors to drive a differential DUT.

4.1.1 Imbalance Introduced by Single RF Transformer

A RF transformer with a high frequency signal input, has parasitic coupling capacitances (c_1 and c_2) between the primary and secondary side as shown in Figure 4.1. The difference between these capacitances introduces the imbalance of the RF transformer [37]. We discuss the imbalance of the RF transformer based on quantitative analysis in this section. For computational simplicity, we assume that a pure sinusoidal waveform is applied to the RF transformer input, and we use the t notation in digital domain, instead of using the conventional discrete time notation n.

The sinusoidal input $x(t)$ is applied to a single RF transformer, and is converted to a pair of signals, $y_p(t)$ and $y_n(t)$.

$$\begin{aligned} y_p(t) &= \kappa_p \cos(\omega t) \\ y_n(t) &= \kappa_n \cos(\omega t - \pi + \varphi) = -\kappa_n \cos(\omega t + \varphi) \end{aligned} \tag{4.1}$$

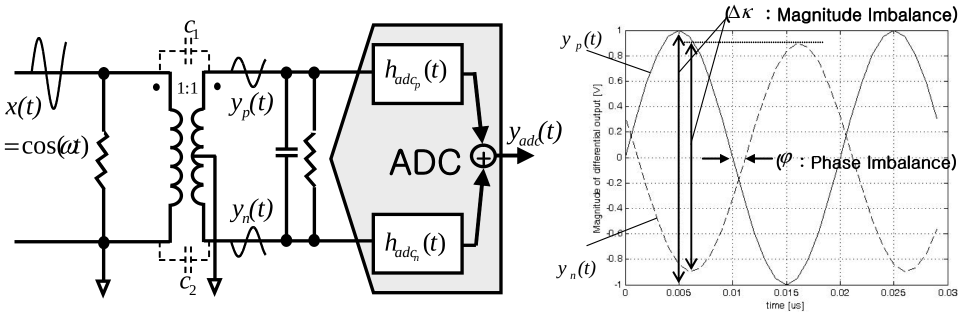


Figure 4.1: Single Transformer as DND

where φ represents the degree of the phase imbalance, and κ_p and κ_n are magnitudes of the differential output pair of the single RF transformer. The ADC is modeled as a symmetrical third-order transfer function, and harmonic distortion considered is up to the third order as follows.

$$h_{adc}(t) = a_0 + a_1 y(t) + a_2 y^2(t) + a_3 y^3(t) \tag{4.2}$$

where $y(t)$ is the one of differential input pair of the ADC.

$$\begin{aligned} y_{adc}(t) = a_1\{y_p(t) - y_n(t)\} + a_2\{{y_p}^2(t) - {y_n}^2(t)\} \\ + a_3\{{y_p}^3(t) - {y_n}^3(t)\} \end{aligned} \tag{4.3}$$

We examine the effect of the imbalance introduced by the single RF transformer.

4.1.1.1 Ideal Case (No Imbalance)

If y_p and y_n are perfectly balanced, they will have the same magnitude ($\kappa_p = \kappa_n := \kappa$) and will be exactly 180° out of phase ($\varphi = 0°$), and Equation 4.1

and 4.3 become

$$y_p(t) = \kappa \cos(\omega t), \quad y_n(t) = -\kappa \cos(\omega t) \tag{4.4}$$

$$y_{adc}(t) = \left(2a_1\kappa + \frac{3a_3}{2}\kappa^3\right)\cos(\omega t) + \left(\frac{a_3}{2}\kappa^3\right)\cos(3\omega t) \tag{4.5}$$

Even harmonics get canceled, while odd harmonics do not. We use total harmonic distortion (THD) as the key performance parameter of the ADC. Thus the THD in this ideal case can be compared with that of the imbalance cases to analyze the effect of the imbalances from a single RF transformer on the ADC performance.

$$THD = \frac{\left(\frac{1}{2}a_3\kappa^3\right)^2}{\left(2a_1\kappa + \frac{3}{2}a_3\kappa^3\right)^2} := \frac{\eta_h^2}{\eta_f^2} \tag{4.6}$$

where η_f and η_h are the coefficients of the fundamental frequency and harmonics, respectively.

4.1.1.2 Imbalance Case I (Magnitude)

If the two differential outputs, y_p and y_n, have a magnitude imbalance but no phase imbalance ($\varphi = 0°$), they will have different magnitudes ($\kappa_p \neq \kappa_n$) as follows.

$$y_p(t) = \kappa_p \cos(\omega t), \quad y_n(t) = -\kappa_n \cos(\omega t) \tag{4.7}$$

Similarly in the ideal case, we can obtain the response of ADC as follows.

$$\begin{aligned} y_{adc}(t) &= \frac{a_2(\kappa_p^2 - \kappa_n^2)}{2} \\ &+ \left\{ 2a_1 \frac{(\kappa_p + \kappa_n)}{2} + \frac{3}{2} a_3 \frac{(\kappa_p^3 + \kappa_n^3)}{2} \right\} \cos(\omega t) \\ &+ \left\{ a_2 \frac{(\kappa_p^2 - \kappa_n^2)}{2} \right\} \cos(2\omega t) + \left\{ \frac{1}{2} a_3 \frac{(\kappa_p^3 + \kappa_n^3)}{2} \right\} \cos(3\omega t) \end{aligned} \tag{4.8}$$

We assume that the difference between the squares of each magnitude, $\kappa_p^2 - \kappa_n^2$ may be ignored. Then similarly in the ideal case, THD in the magnitude imbalance case is as follows.

$$THD = \frac{\left\{ \frac{1}{2} a_3 \left(\frac{\kappa_p^3 + \kappa_n^3}{2} \right) \right\}^2}{\left\{ 2a_1 \left(\frac{\kappa_p + \kappa_n}{2} \right) + \frac{3}{2} a_3 \left(\frac{\kappa_p^3 + \kappa_n^3}{2} \right) \right\}^2} \tag{4.9}$$

4.1.1.3 Imbalance Case II (Phase)

Suppose that two signals have phase imbalance ($\varphi \neq 0°$) but no magnitude imbalance ($\kappa_p = \kappa_n := \kappa$), then we have

$$y_p(t) = \kappa \cos(\omega t), \quad y_n(t) = -\kappa \cos(\omega t + \varphi) \tag{4.10}$$

Similarly in other cases, we can obtain the response of ADC as follows.

$$
\begin{aligned}
y_{adc}(t) = \kappa_f & \left\{ \left(\frac{1+\cos(\varphi)}{2} \right) \cos(\omega t) - \left(\frac{\sin(\varphi)}{2} \right) \sin(\omega t) \right\} \\
& + \frac{a_2 k^2}{2} \left\{ (1-\cos(2\varphi)) \cos(2\omega t) + \sin(2\varphi) \sin(2\omega t) \right\} \\
& + \kappa_h^3 \left\{ \left(\frac{1+\cos(3\varphi)}{2} \right) \cos(3\omega t) - \left(\frac{\sin(3\varphi)}{2} \right) \sin(3\omega t) \right\}
\end{aligned}
\tag{4.11}
$$

Then, THD in the phase imbalance case is

$$
THD = \frac{\eta_h^2 \left(\frac{1+\cos(3\varphi)}{2} \right) + \frac{a_2^2 \kappa^4}{2} (1-\cos(2\varphi))}{\eta_f^2 \left(\frac{1+\cos(\varphi)}{2} \right)} \tag{4.12}
$$

4.1.2 Analysis of Imbalance Effect

Our analysis of the imbalance yields two facts.

1. Imbalance introduced by a DND can degrade DUT performance. Furthermore if another imbalance is introduced by the differential DUT itself, the imbalance problem affects DUT performance more seriously. Thus the DND cannot be used for a DfT circuit, and the loopback approach cannot address the issues in the differential signaling.

2. The phase imbalance effect on the ADC performance is dominant compared to the magnitude imbalance.

If we carefully observe Equation 4.6 and 4.12, we can see that the κ^4 term in Equation 4.12 significantly affects the THD of the ADC, compared to Equation 4.6.

On the other hand, if we compare Equation 4.6 with Equation 4.9, we can see that there are three average terms of magnitudes such as $\left(\frac{\kappa_p+\kappa_n}{2}\right)$ and $\left(\frac{\kappa_p^3+\kappa_n^3}{2}\right)$ in Equation 4.9, instead of κ_p and κ_n in Equation 4.6. Even if κ_p and κ_n are non-ignorably different, their averaged values in Equation 4.9 may not be quite different from the magnitudes (κ and κ^3) in Equation 4.6. Furthermore, these average terms are assigned in both numerator and denominator in Equation 4.9.

Thus the phase imbalance significantly contributes to the degradation of the ADC performance, compared with the magnitude imbalance. This analysis can be applied to any differential circuit including differential DUT and DND. Therefore we focus on the phase imbalance while ignoring the magnitude imbalance in our method.

4.2 Transformer-Coupled Loopback Test

This section describes the implementation of the proposed *Transformer-Coupled Loopback Test* for prediction of individual DUT specifications on differential signaling, using a cascaded RF transformer in loopback mode. We discussed the imbalance introduced by a single RF transformer in the Section 4.1. However if one more RF transformer is cascaded with the single RF transformer, the overall imbalance is significantly reduced. The theory is discussed in detail in [64].

Thus we determine the characteristic parameters including the imbalance introduced by DUTs, using a cascaded RF transformer as a DfT circuit.

4.2.1 Qualitative Analysis

This section gives an overview of the proposed approach based on qualitative analysis for better understanding. As shown in Figure 4.2, our proposed method has DAC and ADC as a DUT and three loopback paths (*Loopback I-III*) to be connected externally to the die on a loadboard [66].

The sinusoidal waveform is applied to the DAC, and the signal directly passes through the ADC by controlling analog multiplexer (Loopback I). Similarly the signals with the same frequency and magnitude pass through the *Loopback II* and *III*, respectively. These three loopbacked responses are each differently weighted by the characteristics of a single and a cascaded RF transformer. The single RF transformer detects the voltage difference between input terminals from output of the DAC and redistributes the voltage difference to the output terminals as shown in Figure 4.3. Ideally, even harmonic distortions are canceled out and the noise floor is reduced in this process, commonly used in differential mode.

In a practical situation, imbalance is introduced by an RF transformer; this makes the even harmonic power higher, and the fundamental signal and odd harmonic power lower. Furthermore the degree of the increase or decrease depends on how much imbalance is generated. Thus each spectral loopbacked response is different, depending on the degree of imbalance introduced by the RF transformers. Figure 4.3 shows how each signal in the loopback paths is weighted differently by the RF transformers. We carefully observe the power difference between the (*Loopback I*) path and the (*Loopback II*) path, and

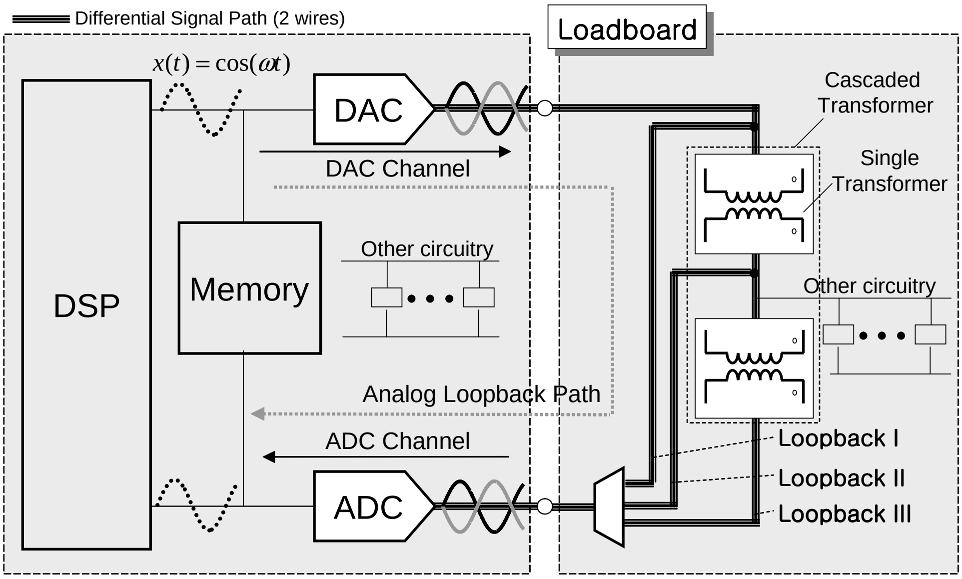


Figure 4.2: Proposed Loopback Test Scheme

the power difference from (*Loopback I*) path and the (*Loopback III*) path. Compared with the DAC output (*Loopback I*), even harmonic power on the *Loopback II* path is increased considerably more than that on the *Loopback III* path. That is because a cascaded RF transformer introduces less imbalance than a single RF transformer. Similarly the fundamental signal and the even harmonic power on the *Loopback III* path is decreased less than that on the *Loopback II* path. The same nonlinearity of the ADC is applied equally to the three loopback responses. The applied responses can be still seen as the differently weighted responses by the RF transformers. Therefore we can give a different weight to the signal on each loopback path. Also if we can find the degree of imbalance introduced by the RF transformers, we can use this

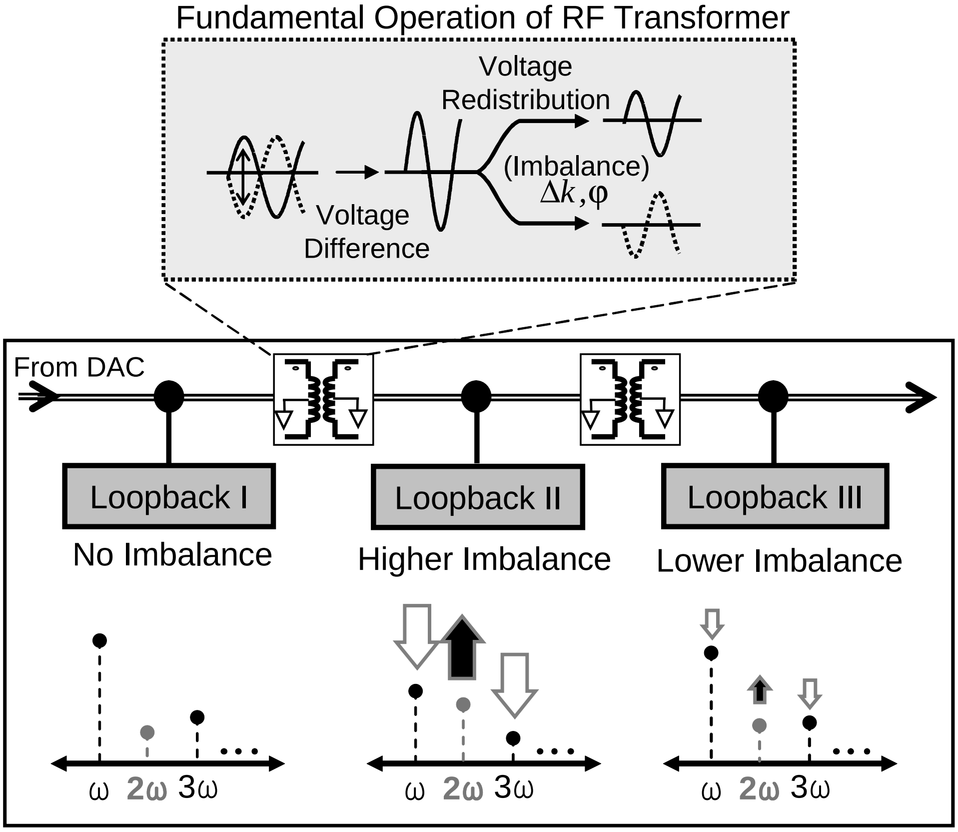


Figure 4.3: Characteristic of Cascaded RF Transformer on Loopback Paths

imbalance to characterize the specifications of the DUTs.

For accurate RF transformer modeling, we use the 4-port differential Hybrid (H)-parameter matrix [58]. Each H-parameter represents the RF transformer's gain weighted by the imbalance. Thus, the H-parameter can be seen as the weighting factor. We assume that H-parameters can be readily identified by the network analyzer, since it is implemented on the loadboard. Then we can derive the equations with the characteristic parameters and H-parameter matrix to describe the non-linear behavior of the DUTs. Finally we can get the spectral loopback responses and characterize the parameters by solving the equations. Neural Networks can be used to efficiently solve the non-linear equations.

Our method uses an RF transformer which is an existing device commonly used in conventional test. Furthermore the RF transformer has inherently wide input bandwidth, and it can be reused for our method to test DUTs with the quite different input frequencies from *kHz* to *GHz*.

4.2.2 Quantitative Analysis

We quantify the behavior of a differential test input pair in our proposed test scheme.

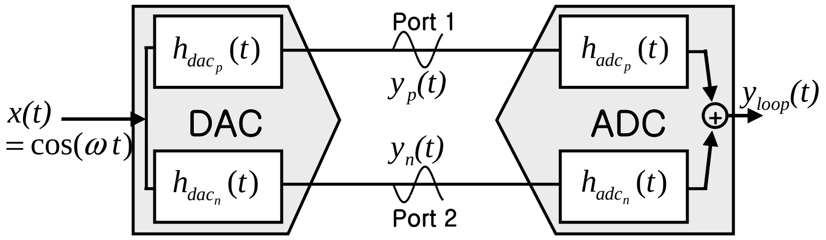
4.2.2.1 Characterization of Harmonic Distortion Parameter

Figure 4.4 and Figure 4.5 show the differential input signaling on each loopback path.

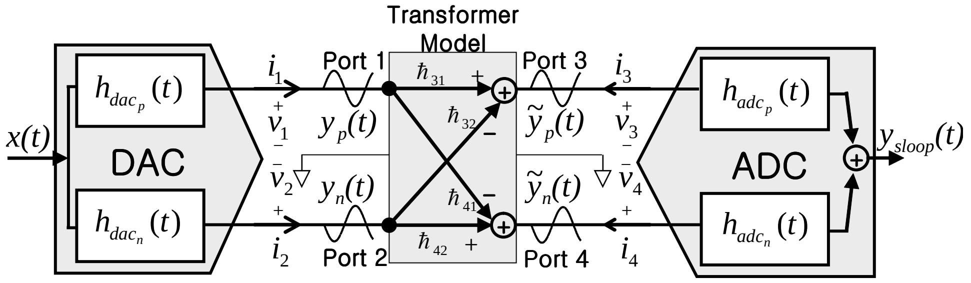
(i) Loopback I (Pure Loopback Path)

As we discussed in Section 4.1, the magnitude imbalance is ignored, and the phase imbalance between the differential output pair of DAC and ADC is considered. Thus, the differential DAC outputs can be expressed as

$$y_p(t) = \sum_i d_i \cos^i(\omega t) \qquad y_n(t) = \sum_i d_i \cos^i(\omega t - \pi + \varphi_d) \tag{4.13}$$



(a) Loopback I



(b) Loopback II

Figure 4.4: *Loopback I* and Cascaded Transformer Model on *Loopback II*

where d_i is the harmonic coefficient of the DAC channel and φ_d is the positive or the negative value for phase imbalance between the differential output pair, which is introduced by the DAC (Figure 4.4(a)). Also the differential DAC is modeled as a symmetrical transfer function by *Taylor* series as

$$h_{dac_p}(t) = \sum_i d_i x^i(t) \qquad h_{dac_n}(t) = \sum_i d_i x^i(t + \frac{-\pi + \varphi_d}{\omega}) \tag{4.14}$$

Similarly the ADC is modeled as Equation 4.15, and the loopbacked response is obtained as Equation 4.16.

$$h_{adc_p}(t) = \sum_i a_i y^i(t) \qquad h_{adc_n}(t) = \sum_i a_i y^i(t + \frac{\varphi_a}{\omega}) \tag{4.15}$$

$$y_{loop}(t) = \sum_i a_i({y_p}^i(t) - {y_n}^i(t + \frac{\varphi_a}{\omega})) \tag{4.16}$$

where a_i is the harmonic coefficient of the ADC channel, and φ_a is the positive or the negative value for the phase imbalance between the differential output pair, which is introduced by the ADC.

(ii) Loopback II (Single Transformer-Coupled Loopback Path)

A single RF transformer (winding ratio 1:1) is modeled with a differential 4-port H-parameter matrix as shown in Figure 4.4(b) [58]. The RF transformer behavior can be modeled by a set of 16 complex parameters to describe the imbalance as follows.

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} \hbar_{11} & \hbar_{12} & \hbar_{13} & \hbar_{14} \\ \hbar_{21} & \hbar_{22} & \hbar_{23} & \hbar_{24} \\ \hbar_{31} & \hbar_{32} & \hbar_{33} & \hbar_{34} \\ \hbar_{41} & \hbar_{42} & \hbar_{43} & \hbar_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \\ i_4 \end{bmatrix} \tag{4.17}$$

where $\hbar_{jk}$ is defined as the weighting parameter to the signal transmitted from port k to port j.

As mentioned in Section 4.1, we focus on the imbalance among several key parameters such as insertion loss and return loss of the RF transformer. H-parameters representing these losses are ignored. Then the H-parameter matrix for the single RF transformer can be re-written along with the differential DAC output as follows.

$$\begin{bmatrix} \tilde{y}_p(t) \\ \tilde{y}_n(t) \end{bmatrix} = \begin{bmatrix} \hbar_{31} & \hbar_{32} \\ \hbar_{41} & \hbar_{42} \end{bmatrix} \begin{bmatrix} y_p(t) \\ y_n(t) \end{bmatrix} \tag{4.18}$$

where $\tilde{y}_p$ and $\tilde{y}_n$ are the outputs of the single RF transformer. The *Loopback II* response is then expressed as

$$y_{sloop}(t) = \sum_i a_i(\tilde{y}_p^i(t) - \tilde{y}_n^i(t + \frac{\varphi_a}{\omega})) \tag{4.19}$$

(iii) Loopback III (Cascaded Transformer-Coupled Loopback Path)

As shown in Figure 4.5, two RF transformers are cascaded. The matrix describing the cascaded RF transformer is expressed as the multiplication of the matrices of the RF transformers, which is

$$\begin{bmatrix} \hbar_{53} & \hbar_{54} \\ \hbar_{63} & \hbar_{64} \end{bmatrix} \begin{bmatrix} \hbar_{31} & \hbar_{32} \\ \hbar_{41} & \hbar_{42} \end{bmatrix} = \begin{bmatrix} \hbar_{51} & \hbar_{52} \\ \hbar_{61} & \hbar_{62} \end{bmatrix} \tag{4.20}$$

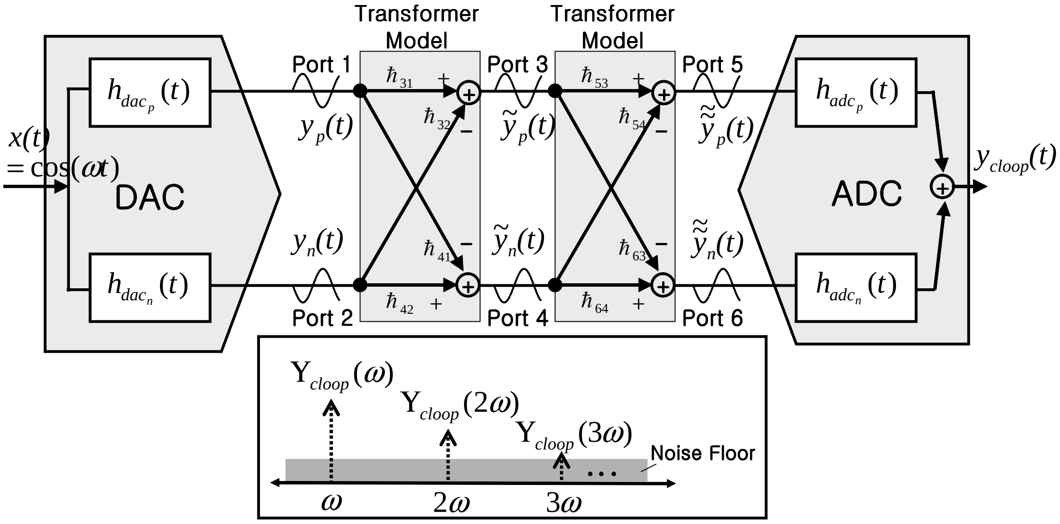


Figure 4.5: Cascaded RF Transformer Model and Frequency Response on *Loopback III*

The output of the cascaded RF transformer becomes

$$\begin{bmatrix} \tilde{\tilde{y}}_p(t) \\ \tilde{\tilde{y}}_n(t) \end{bmatrix} = \begin{bmatrix} \hbar_{51} & \hbar_{52} \\ \hbar_{61} & \hbar_{62} \end{bmatrix} \begin{bmatrix} y_p(t) \\ y_n(t) \end{bmatrix} \tag{4.21}$$

The ADC output can be expressed as

$$y_{cloop}(t) = \sum_i a_i(\tilde{\tilde{y}}_p{}^i(t) - \tilde{\tilde{y}}_n{}^i(t + \frac{\varphi_a}{\omega})) \tag{4.22}$$

(iv) Harmonic Coefficient Characterization

As mentioned in the previous section, each *Taylor* coefficient of the loop-backed response is identified in order to quantify the non-linearity of analog circuits [63]. Each harmonic coefficient in Equations 4.16, 4.19 and 4.22 is expressed as the spectral representation by *Fourier* Transformation as shown in

Equations 4.23, 4.24, and 4.25. We also obtain frequency loopback responses through the three loopback paths as Y_{loop}, Y_{sloop} and Y_{cloop} in Figure 4.5. Thus these spectral responses and H-parameters characterized are known values. Harmonic distortion considered is up to the third order, and $\hbar_{51}{}^2 - \hbar_{61}{}^2$ are ignored. Consequently each harmonic response can be expressed as

$$\begin{aligned} Y_{loop}(2\omega) &= (a_2 d_1^2)(1 - e^{j2\Phi})/4 \\ Y_{sloop}(2\omega) &= a_2^2 d_1 \hbar_{31} \hbar_{41} e^{j2\Phi} + d_1 \hbar_{32} \hbar_{42} \\ Y_{cloop}(2\omega) &= a_2 d_1 \hbar_{51} \hbar_{61} (1 - e^{j2\Phi}) + d_1 \hbar_{52} \hbar_{62} \end{aligned} \tag{4.23}$$

where $\Phi = \varphi_d + \varphi_a$. We first determine a_2, d_1 and Φ from Equation 4.23.

$$\begin{aligned} Y_{loop}(3\omega) &= (2a_2 d_1 + a_3 d_1^3)(1 - e^{j3\Phi})/4 \\ Y_{sloop}(3\omega) &= (a_3 + d_1{}^2/3)\{\hbar_{42}^3 e^{j3\varphi_a} + \hbar_{31}^2 \hbar_{41} (e^{j3\varphi_d} + e^{j3\Phi})\} \\ Y_{cloop}(3\omega) &= (a_3 d_1^3/6)\{\hbar_{51}^2 \hbar_{62} e^{j3\varphi_a} + \hbar_{61}^2 \hbar_{52} (e^{j3\varphi_d} + e^{j3\Phi})\} \end{aligned} \tag{4.24}$$

Then with these determined parameter values we find a_3, φ_a and φ_d using Equation 4.24.

$$
\begin{aligned}
Y_{loop}(\omega) &= \{a_1 d_1 + \frac{3}{4}(a_1 d_3 + 2a_2 d_1 d_2 + a_3 d_1^3)\}(1 - e^{j\Phi}) \\
Y_{sloop}(\omega) &= \{L_4(\hbar_{41} + \hbar_{31}) - L_5 \hbar_{32}\} e^{j\varphi_a} + \{L_1 \hbar_{42} \\
&\quad + L_2(2\hbar_{42}\hbar_{31} + \hbar_{32}^2) + L_3 \hbar_{41}\}(e^{j2\varphi_d} - e^{j2\Phi}) \\
Y_{cloop}(\omega) &= \{L_1 \hbar_{51} + L_2(2\hbar_{51}\hbar_{61}\hbar_{52} + \hbar_{51}^2 \hbar_{62})\}(1 + e^{j\varphi_a}) \\
&\quad + (L_4 \hbar_{51}\hbar_{62} - L_5)(1 - e^{j\varphi_a}) \\
&\quad + \hbar_{61}\{L_1 + L_2(2\hbar_{51}^2 + \hbar_{61}^2) + L_3\}(e^{j\varphi_d} + e^{j\Phi}) \\
&\quad - (L_4 \hbar_{61}\hbar_{52} - L_5)(e^{j\varphi_d} - e^{j\Phi})
\end{aligned}
\tag{4.25}
$$

where $L_1 = \frac{3}{4}a_1 d_3$, $L_2 = \frac{3}{4}a_3 d_1^3$, $L_3 = a_1 d_1$, $L_4 = \frac{3}{2}a_2 d_1 d_2$, and $L_5 = a_2 d_1 \hbar_{51}\hbar_{61} d_2$. Finally a_1, d_2 and d_3 are determined from Equation 4.25. Thus, all phase imbalance parameters (φ_d and φ_a) as well as the *Taylor* coefficients of the DAC and ADC channels are separately quantified.

4.2.2.2 Characterization of Noise Parameters

Noise is a key parameter in mixed-signal circuits in addition to harmonic distortion. Let $S_d(f)$ be the Power Spectral Density (PSD) of a pure noise input to the ADC channel, which is generated by the DAC channel, and $S_a(f)$ be the PSD of the ADC channel. Assume that the noise of the DAC and the ADC channel are uncorrelated. The output referred noise of *Loopback I* can be expressed as

$$
P_{loop} = \int_0^\infty \Gamma S_d(f) df + \int_0^\infty S_a(f) df \tag{4.26}
$$

where Γ is the overall gain of the DAC and the ADC channel, and P_{loop} is the total noise power of y_{loop}. Similarly the output referred noise of *Loopback III* can be expressed as

$$\begin{aligned} P_{cloop} = & \int_0^\infty \Gamma |H(f)|^2 |H(f)|^2 S_d(f) df \\ & + \int_0^\infty S_a(f) df + \int_0^\infty \Gamma S_t(f) df \end{aligned} \tag{4.27}$$

where $|H(f)|^2$ is the frequency response of the single RF transformer, $S_t(f)$ is the PSD of the cascaded RF transformer, and P_{cloop} is the total noise of y_{cloop}. We use the f notation rather than the ω notation for simplicity.

The integral in Equation 4.27 can be calculated within the *Nyquist* frequency. Thus P_{loop} and P_{cloop} are readily calculated from each measured loopback response. Finally given Γ, $|H(f)|$, and $\int_0^\infty S_t(f)df$, $\int_0^\infty S_a(f)df$ and $\int_0^\infty S_d(f)df$ can be determined.

4.2.2.3 Non-linear Regression

It is not trivial to analytically solve nonlinear equations. In fact the problem becomes more challenging if higher order harmonic distortion is considered. Therefore we use a neural network algorithm to solve the derived nonlinear equations. Harmonic power and noise power at frequency bins which are used in Equation 4.23, 4.24, 4.25, 4.26, and 4.27 are used as the training set to determine the *Taylor* coefficients, and the PSD of the DAC and the ADC.

4.3 Experimental Results

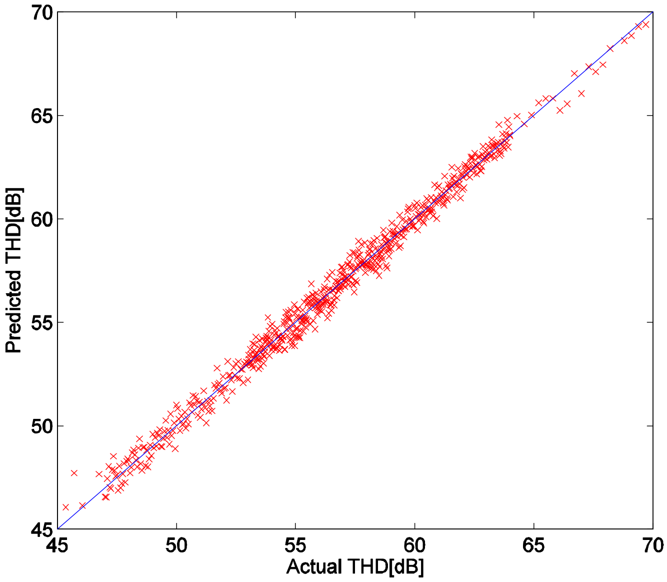
This section analyzes simulation results. In addition hardware measurements were performed on the commercial converters (National Semiconductor ADC(ADC14L105) and Analog Devices DAC(AD9764)) to evaluate the proposed method.

4.3.1 Simulation Results

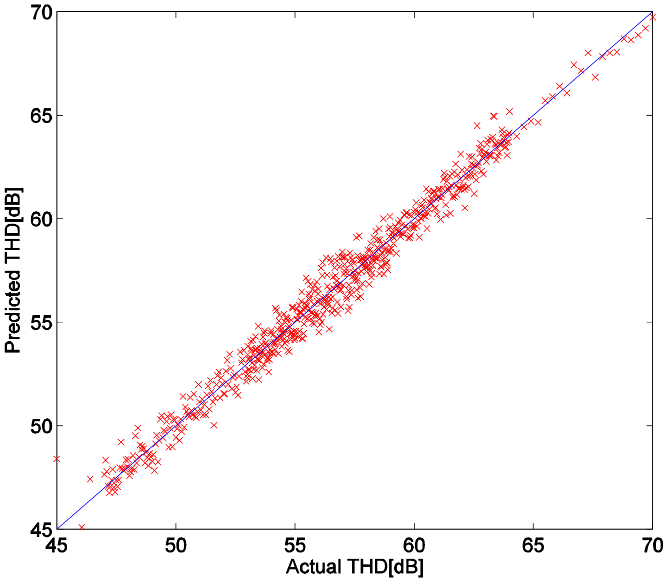
With HSPICE, on-chip converters and RF transformer were modeled and simulated using Matlab with SIMULINK. A sinusoidal wave digitized to 14 bit-codes was used as an input stimulus to the DAC and ADC. The simulation model consists of the first three harmonics to mimic the harmonic distortion. The combination of harmonics was determined by Monte Carlo simulation. In addition, random noise was added to the simulation model in order to include noise effects.

We performed the simulation of the proposed methodology using the same set of 1000 DUT ensembles. A set of 1000 DUT ensembles were generated assuming a 10% random deviation with normal distribution in noise of the fundamental signal. A new set of 100 ensembles is used as training data.

Figures 4.6, 4.7 and 4.8 show the predicted performance parameters such as THD, SNR and SINAD for the proposed method. Table 4.1 summarizes the prediction errors. The result indicates that the mean and standard deviation of prediction errors for both DAC and ADC were less than 0.7dB. Thus the predictive performance parameters of the proposed method provide

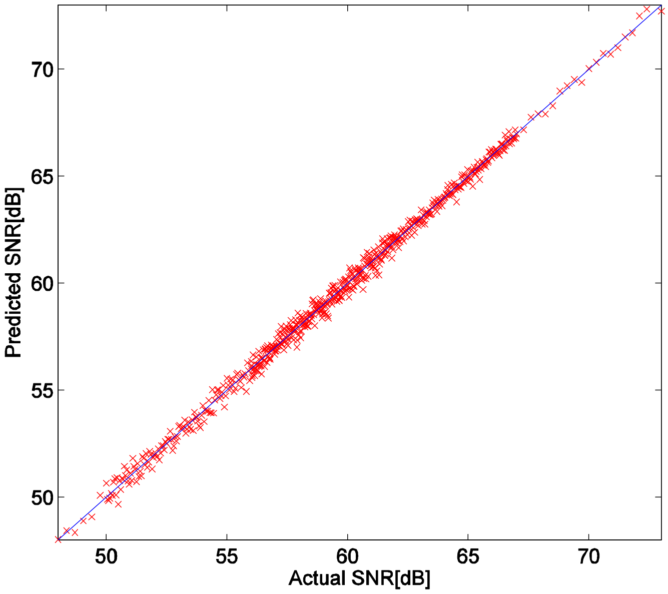


(a) THD of ADC channel

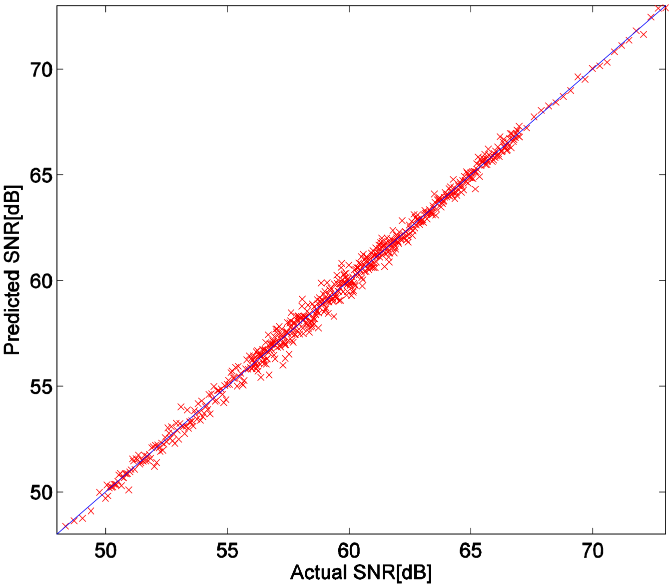


(b) THD of DAC channel

Figure 4.6: THD of DAC and ADC Channel (Simulation Results)

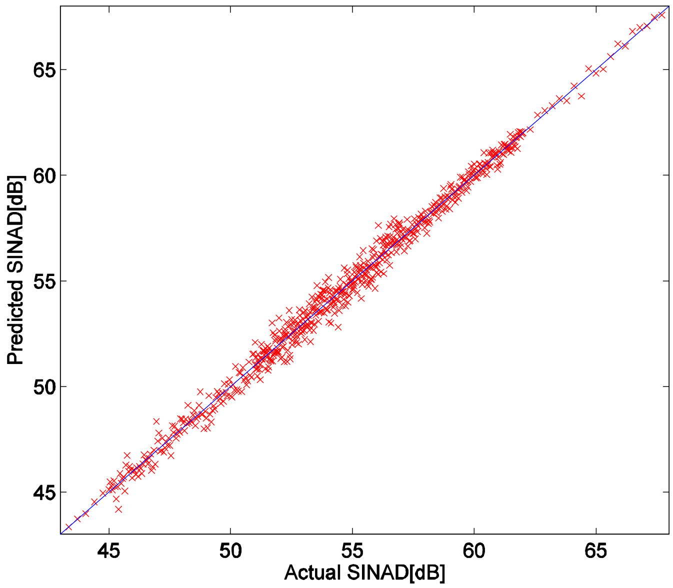


(a) SNR of ADC channel

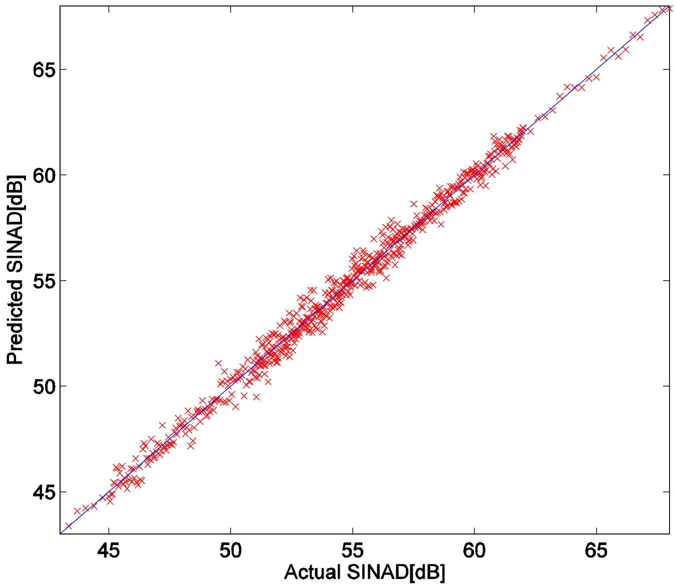


(b) SNR of DAC channel

Figure 4.7: SNR of DAC and ADC Channel (Simulation Results)



(a) SINAD of ADC channel



(b) SINAD of DAC channel

Figure 4.8: SINAD of DAC and ADC Channel (Simulation Results)

Table 4.1: Simulation Results for Specification Error

Parameter	**DAC channel**		**ADC channel**	
	Mean	**STD.**	**Mean**	**STD.**
THD	0.67dB	0.65dB	0.58dB	0.57dB
SNR	0.33dB	0.28dB	0.31dB	0.25dB
SINAD	0.35dB	0.31dB	0.42dB	0.40dB

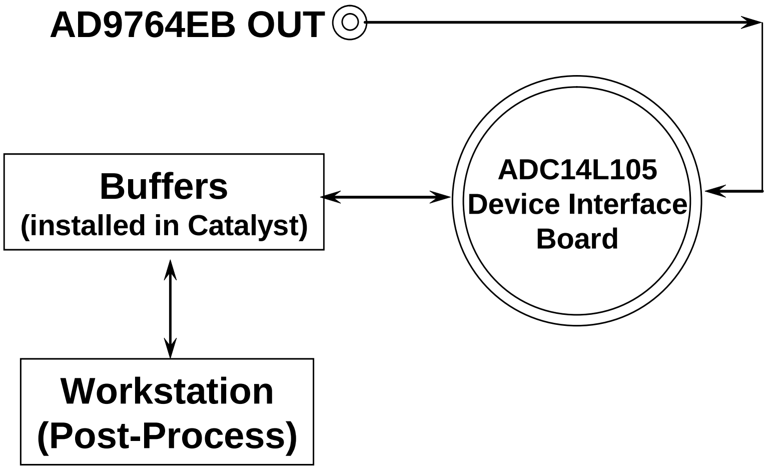


Figure 4.9: Hardware Measurement Setup

high accuracy.

4.3.2 Hardware Measurements

AD9764 has 14-bit resolution, 125MSPS sampling rate and differential current output. The ADC14L105 is a monolithic pipelined data converter with 14-bit resolution and 105MSPS sampling speed. A DIB for the ADC connection was manufactured, and an evaluation board was used for the DAC.

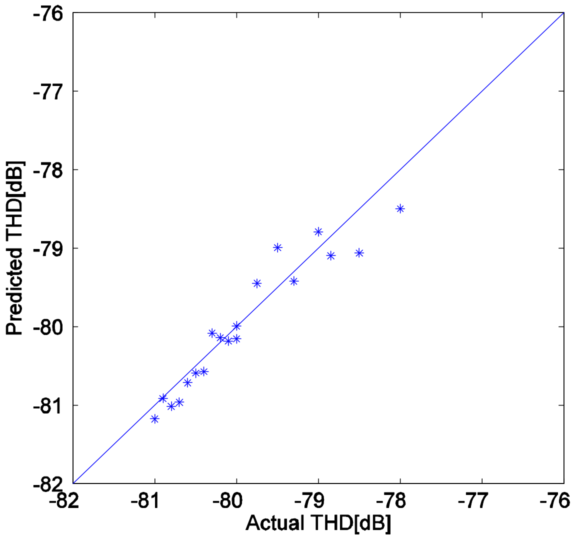
Table 4.2: Specification Errors of Hardware Measurements

Parameter	**DAC channel**		**ADC channel**	
	Mean	**STD.**	**Mean**	**STD.**
THD	0.33dB	0.31dB	0.24dB	0.22dB
SNR	0.87dB	0.70dB	0.36dB	0.31dB
SINAD	0.80dB	0.62dB	0.23dB	0.25dB

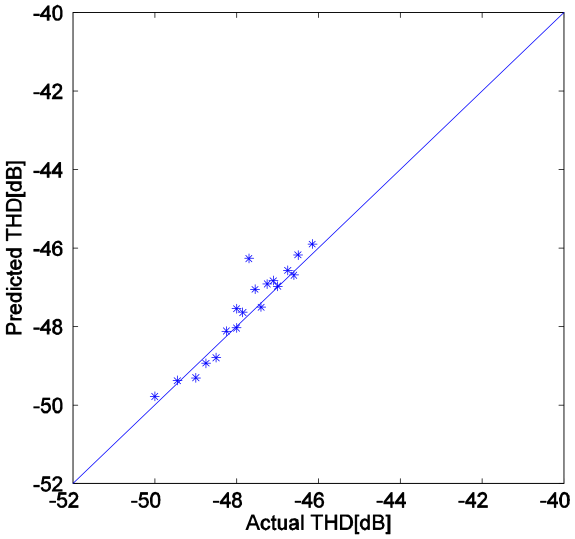
Cascaded RF transformers were installed on a separate connection board. In order to measure the actual DUT specifications, the *Teradyne Catalyst* tester and the HP 8644B synthesizer were used.

To implement the loopback scheme, the RF transformers were connected between the DAC on the evaluation board and the ADC on the DIB. As shown in Fig 4.9, the distorted and noisy analog signal at the output of the DAC was loopbacked to the ADC and digitized. The digitized data was transferred to the host computer through the buffers installed in the *Catalyst*, and post-processing was done to characterize the individual DUT specifications. In order to inject a fault in the DAC and the ADC, we performed measurements under various stress conditions by randomly changing the power supplies, and the input amplitude/frequency.

12 DUTs were used for the training set, and 18 DUTs were used for the validation set. Figure 4.10, 4.11 and 4.12 show the predicted value of the performance parameters for the validation set, and Table 4.2 summarizes the statistics of the prediction errors. The mean and standard deviation of prediction errors for the DAC and the ADC channel were both less than 1.0dB.

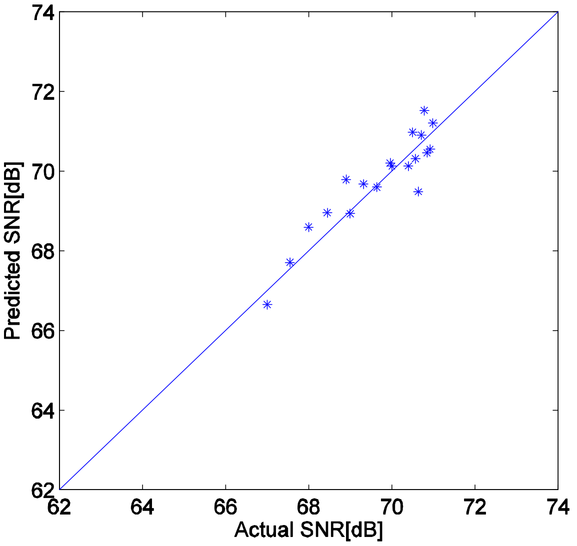


(a) THD of ADC channel

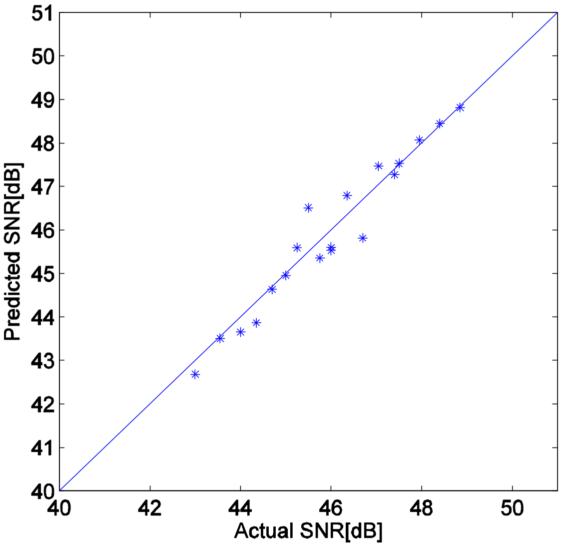


(b) THD of DAC channel

Figure 4.10: THD Results of DAC and ADC Channel

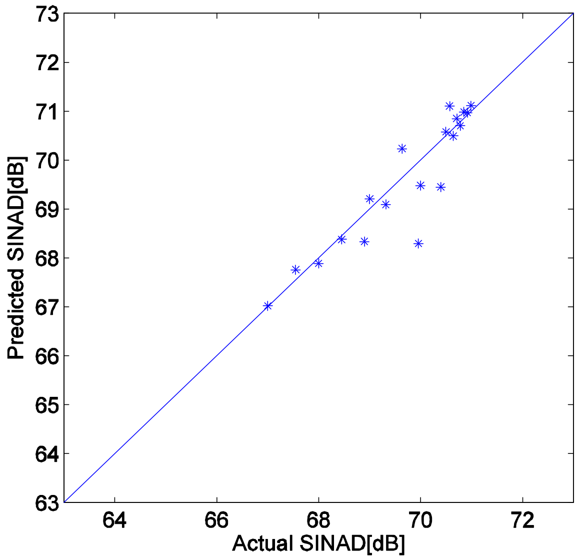


(a) SNR of ADC channel

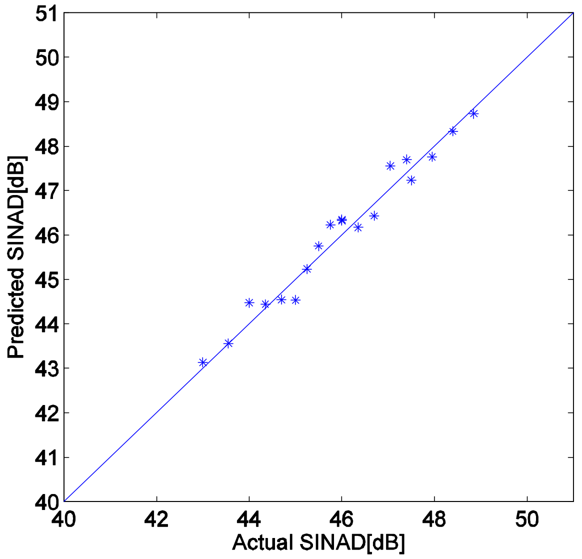


(b) SNR of DAC channel

Figure 4.11: SNR Results of DAC and ADC Channel



(a) SINAD of ADC channel



(b) SINAD of DAC channel

Figure 4.12: SINAD Results of DAC and ADC Channel

Table 4.3: DUT Specifications

Performance Parameter	**Specification Limits**	
	DAC	ADC
THD	-47.5[dB]	-61.0[dB]
SNR	45.5[dB]	70.5[dB]
SINAD	45.5[dB]	69.5[dB]

Table 4.4: Classification Accuracy

Performance Parameter	**Pass**	**Fail**
Actual Classification	10	8
Predicted Classification	10	8

4.3.2.1 Classification Accuracy

Misclassification is one of ways to represent the performance of the proposed methodology. The DUTs were classified by comparing synthesized performance parameters of the proposed method with its specification limits. Table 4.3 shows the specification limits used for classification. The results of the DUT classifications are summarized in Table 5.4, showing the very high classification accuracy.

4.4 Summary

This chapter proposed an efficient loopback test methodology utilizing the characteristics of the RF transformers on a loadboard. A sinusoidal signal was applied to DUTs in loopback mode, and the differently weighted loop-backed responses by a cascaded RF transformer were used to characterize the individual DUT specifications with the derived nonlinear DUT model. This method provides an efficient solution to the problems associated with characterizing differential DUT specifications under the imbalance introduced by differential DfT circuitry. The results of the hardware measurements on DACs (AD9764) and ADCs (ADC14L105) indicate low SINAD prediction errors of 1.4dB and 0.5dB respectively. The predictive accuracy of our method is reliable and stable. Thus, the method can be effectively used to predict the specifications of a mixed-signal circuit.

Chapter 5

Efficient Loopback Test for Aperture Jitter in Embedded Mixed-Signal Circuits

The previous chapter has discussed effective test methodology to characterize the dynamic performance for high speed mixed-signal circuits. Performance of a high-speed data converter is severely limited by technology dependent physical error effects, such as thermal circuits noise, comparator ambiguity, and timing jitter. Timing jitter introduced by the sampling process is essentially becoming a major portion of the available timing margins, since it dramatically degrades the achievable Signal-to-Noise Ratio (SNR) of the data converters. Therefore this imposes stringent conditions on the allowable timing jitter in high-frequency signals. Furthermore, since jitter involves measurement of time units that are much smaller than Unit Interval (UI) of the signal under consideration, extremely accurate timing measurements are required [18, 21]. For instance, a one Giga Sample Per Second (GSPS) state-of-the-art 8-bit converter claims a typical aperture jitter of 0.4 picoseconds (ps) [52]. Thus jitter measurement is an important part in production testing of high-speed mixed-signal devices [84, 85].

As is commonly known, the total timing jitter affecting the output of a data converter is given by the sum of three components: input signal jitter, clock jitter and aperture jitter [21, 45, 56]. Aperture jitter (otherwise called aperture uncertainty) is caused by broadband noise generated by data converter circuit itself, while other two jitter components are introduced by bench test setup [21, 56]. Thus only aperture jitter among these is a specification of data conversion quality, used to describe sampling fidelity in the data converter circuit [37, 50].

To measure the aperture jitter, it should be distinguished from the other two jitter components as well as from non-jitter related noise affecting the output signal of a data converter [37]. Conventional test uses expensive Automated Test Equipment (ATE), high-precision signal generator and digitizer to reduce input signal jitter and clock jitter, thereby performing accurate and tractable aperture jitter measurement [29, 37].

BIST schemes have been developed to overcome the limitations of conventional test, such as limited test I/O accessibility and high test cost [29]. A loopback test method among various BIST schemes has been proposed as an efficient solution [8, 9, 26, 39, 53, 73]. However BIST approaches have rarely been developed to deal with the particular issues of aperture jitter measurement due to the following reasons.

1. Jitter-induced noise present in the DUT affects the performance of DfT circuitry as well as the DUT, thereby reducing test accuracy and fault coverage.

2. Even if a self-test approach is developed to overcome the above problem, it could lead to greater complexity in DfT circuit implementation.

This paper proposes a novel *Efficient Loopback Test for Aperture Jitter* in embedded mixed-signal circuits to improve prediction accuracy for aperture jitter and realize cost-effective test.

5.1 Problems of Jitter Measurement in Mixed-Signal Circuits

In this section we present a mathematical analysis of the effect of timing jitter on the performance of mixed-signal devices. Issues relating to aperture jitter measurement are then discussed.

5.1.1 Effect of Jitter on Mixed-Signal Device

As mentioned in the previous section, high-speed mixed-signal devices suffer from three jitter components as shown in Fig.5.1-(a). Calculating the effects of these jitter components can become mathematically complicated in all but the simplest examples. One example first shows the analysis for the effects of aperture jitter on the samples obtained by an ADC. Then the analysis is extended for all three jitter components. *Aperture jitter* stands for the random sampling time variation in data converters, which is caused by broadband noise in the Sample/Hold Amplifier (SHA) in data converter [21]. It is specified as a Root-Mean-Square (RMS) time. We use continuous time notation t in the digital domain, instead of using the conventional discrete time notation n, for computational simplicity, and we assume that a unit magnitude, sinusoidal signal $\cos(\omega t)$ is applied to ADC with unit gain.

At first we focus on the effect of aperture jitter on ADC output. Without aperture jitter, the fundamental signal on ADC output response is

$$y_{adc}(t)|_{t=t_0} = \cos(\omega t_0) \tag{5.1}$$

where $y_{adc}(t)$ and t_0 are output response of the ADC and nominal sampling time of input sinusoidal waveform respectively. With aperture jitter present, the output of the ADC becomes

$$y_{adc}(t)|_{t=t_0+\varphi^{adc}} = \cos(\omega(t_0 + \varphi^{adc})) \tag{5.2}$$

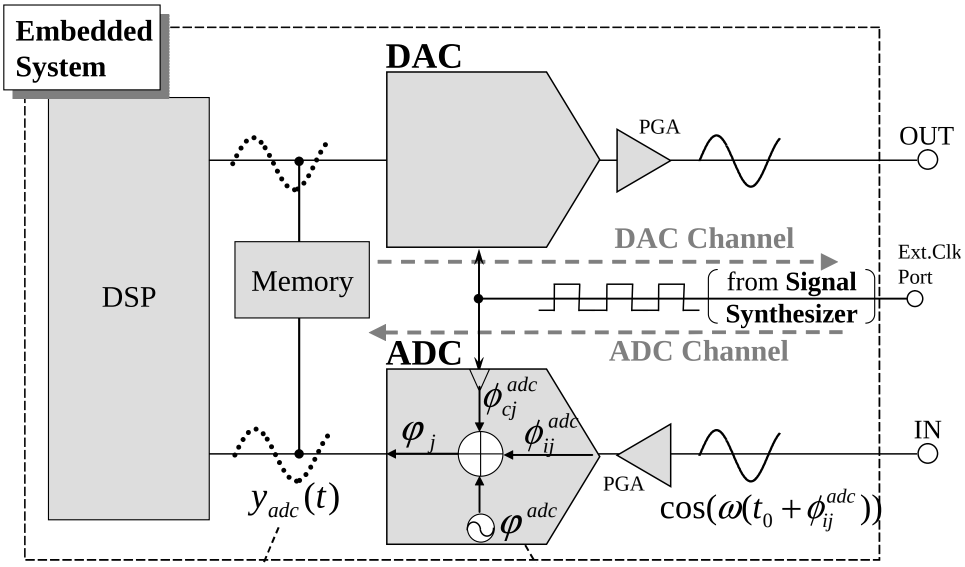
where φ^{adc} is the magnitude of aperture jitter introduced by ADC, and it is random variable. We can rewrite Equation 5.2 using the trigonometric identity as

$$y_{adc}(t) = \cos(\omega t_0)\cos(\omega\varphi^{adc}) - \sin(\omega t_0)\sin(\omega\varphi^{adc}) \tag{5.3}$$

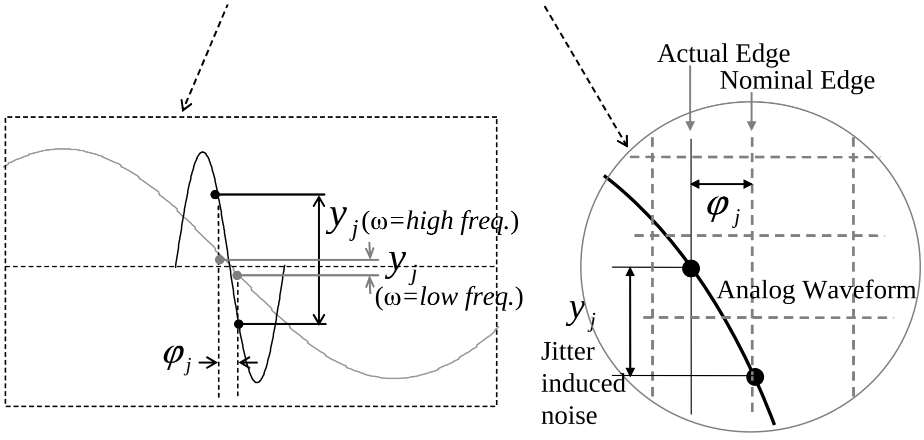
Since the magnitude of the aperture jitter φ^{adc} is assumed to be small compared to the Unit Interval (UI), we make use of the fact that when α is small, $\cos(\alpha) \simeq 1$ and $\sin(\alpha) \simeq \alpha$. Thus we can separate Equation 5.3 into two parts, fundamental signal term and jitter-induced error term.

$$y_{adc}(t) \simeq \cos(\omega t_0) - \omega\sin(\omega t_0)\varphi^{adc} \tag{5.4}$$

Thus the error due to aperture jitter in the ADC output, denoted as y_j, is



(a) Conventional Embedded Mixed-Signal Cirsuits



(b) Relationship between Jitter-Induced Noise and Signal Freq.

(c) Noise introduced by Jitter

Figure 5.1: Effect of Jitter on Conventional Embedded Mixed-Signal Device

$$y_j(t) \simeq -\omega \sin(\omega t_0)\varphi^{adc} = \left.\frac{dy_{adc}(t)}{dt}\right|_{t=t_0} \varphi^{adc} \tag{5.5}$$

Finally the jitter-induced error is written in terms of the magnitude of the jitter and the slope of the input signal at sample point as shown in Fig.5.1-(c). It means that a timing error will induce a larger sample error at the rapidly rising or falling points of a sine wave than its peak or trough as shown in Fig.5.1-(b). It further means that if input signal frequency is chosen to be sufficiently low, no errors or a negligible amount of error is induced by aperture jitter. Given input and clock jitter as well as aperture jitter, Equation 5.5 is rewritten as

$$y_j(t) \simeq \left.\frac{dy_{adc}(t)}{dt}\right|_{t=t_0} \left(\phi_{cj}^{adc} + \phi_{ij}^{adc} + \varphi^{adc}\right) \tag{5.6}$$

where ϕ_{cj}^{adc} and ϕ_{ij}^{adc} are clock and input jitter respectively, as shown in Fig.5.1-(a). We assume that the three jitter components are uncorrelated. It can be observed from Equation 5.6 that the value of φ^{adc} cannot be found using $y_j(t)$ obtained from ADC output, unless the values of ϕ_{cj}^{adc} and ϕ_{ij}^{adc} are exactly identified.

5.1.2 Previous Work

Rosing [61] has proposed an improved technique based on *double-beat and subtraction* [85] for measuring aperture jitter using an off-chip measurement platform. Based on coherent sampling, subtraction of the two essentially equal data sets obtained within low and high frequency input sessions removes all deterministic errors.

However, input jitter induced-noise and clock jitter induced-noise are not considered when the aperture jitter is measured. Therefore if the clock and input signals to the ADC have some jitter, this technique measures the sum of the aperture, the input and the clock jitter, instead of measuring aperture jitter separated from other jitters. In addition this technique does not separate aperture jitter from additive noise while assuming that aperture jitter is essentially dominant to additive noise by a significant amount. This is because the technique needs further modeling to precisely represent the relationship between aperture jitter and additive noise. Furthermore, when aperture jitter is not high enough to cause errors of several LSBs, this technique cannot find aperture jitter. Thus this technique can be applied only to high resolution ADCs.

5.2 Efficient Loopback Test for Aperture Jitter

To overcome the limitations on previous work as well as to develop a BIST scheme mentioned previously, we propose an *Efficient Loopback Test* methodology to accurately predict aperture jitter in embedded mixed-signal circuits.

5.2.1 Qualitative Analysis

We first discuss the proposed approach in a qualitative fashion prior to quantitative analysis. Our approach has a single loopback path to internally loop the output of the DAC back into the input of the ADC along with analog multiplexers as shown in Fig.5.2. The DAC and ADC are used as DUTs for our approach. It is assumed that clock source in the load board provides the clock signal for the DAC and ADC, and the clock source is synchronized with the pattern generator in DSP core.

As mentioned before, the total jitter affecting the performance of the DAC and ADC is given by the sum of three jitter components: $\phi_{ij}^{\{dac/adc\}}$, $\phi_{cj}^{\{dac/adc\}}$ and $\varphi^{\{dac/adc\}}$ which are the magnitudes of input signal jitter, clock jitter and aperture jitter of DAC and ADC respectively. It is assumed that the three jitter components are uncorrelated, and they are Gaussian random variables with zero means and the variations $\sigma_{ij}^{\{dac/adc\}}$, $\sigma_{cj}^{\{dac/adc\}}$ and $\sigma_{aj}^{\{dac/adc\}}$. Even though ϕ_{cj}^{dac} and ϕ_{cj}^{adc} are caused by the identified external clock jitter on the load board and they have the same distribution, they are uncorrelated for ADC circuit. This is because ϕ_{cj}^{dac} starts from the clock source, and it is applied to ADC input through DAC circuits and loopback path. This process requires some time. On the other hand, ϕ_{cj}^{adc} is directly applied to ADC clock input from clock source. This time difference makes them uncorrelated in ADC circuit, since it is assumed that they both have the random distribution.

The total jitter affecting the ADC output is given by the sum of ϕ_{ij}^{adc}, ϕ_{cj}^{adc} and φ^{adc} introduced by SHA circuit present in the ADC. On the other hand, input signal jitter of DAC ϕ_{ij}^{dac} present in the input source is only a problem in bench setups, and does not present a problem in on-chip systems [37, 51]. In addition DAC does not have specifications for aperture jitter φ_{aj}^{dac} since they have no internal SHA to cause aperture jitter. Aperture jitter is not measured or specified, since the external clock jitter is the dominant jitter source in DAC circuits [37]. Thus ϕ_{ij}^{dac} and φ^{dac} are ignored, and only clock jitter ϕ_{cj}^{dac} is considered as a jitter component degrading the performance of DAC in embedded system. Therefore our embedded loopback test is performed assuming that there are three jitter components of ADC (ϕ_{ij}^{adc}, ϕ_{cj}^{adc} and φ^{adc}), and clock jitter ϕ_{cj}^{dac} present in DAC output as shown in Fig. 5.2.

Based on these properties of the jitter components, our test procedure is performed based on coherent sampling as follows.

1. For the first loopback test, a low frequency sinusoidal waveform is applied to the DAC, and the output signal directly passes through the ADC using a controlling analog multiplexers in test mode. If this input frequency is chosen to be sufficiently low, a negligible error is introduced by the jitter components. However, quantization noise and additive noise still degrade the output of the ADC. Thus the ADC output is given by a commonly used theoretical model [23, 69] for DAC and ADC as follows.

   $$y_{loop}^{lf}(t) = \sum_i \kappa_i \cos^i(\omega t) + \varrho(t) + \alpha(t) \tag{5.7}$$

   where $\varrho(t)$, $\alpha(t)$ and κ_i represent quantization noise, additive noise and

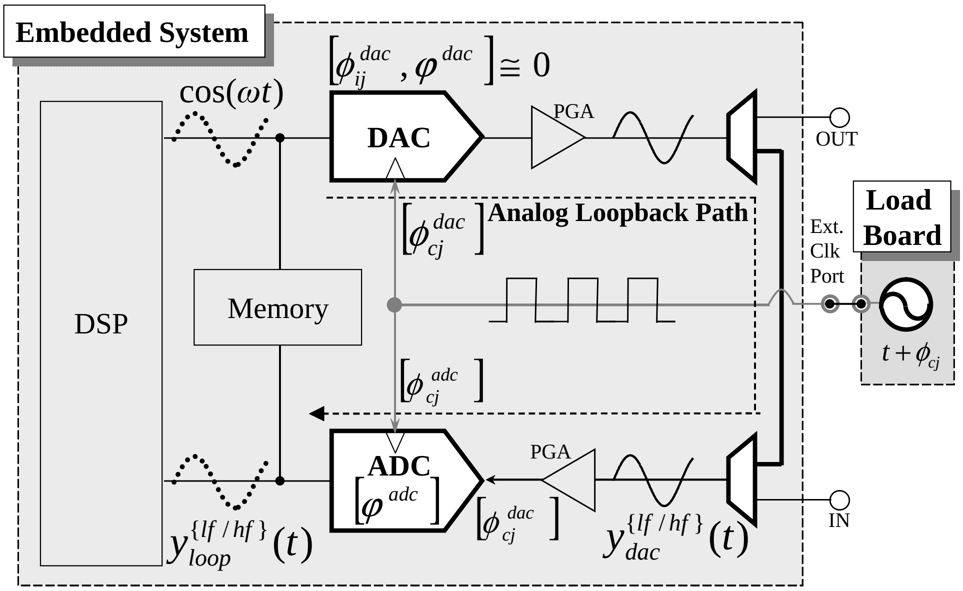


Figure 5.2: Proposed Loopback Scheme

harmonic coefficient introduced by the loopback path which includes the DAC and ADC channel.

2. Similarly a higher frequency input signal is applied to the DAC in the second loopback test. Clock jitter affecting the DAC performance becomes input jitter of the ADC as shown in Fig. 5.2, since the DAC output $y_{dac}^{hf}(t)$ is already affected by its clock jitter, and its output signal with jitter-induced noise is applied back to the ADC input as follows.

$$y_{loop}^{hf}(t) = \sum_i \hat{\kappa}_i \cos^i(\omega(t + \Psi(t))) + \hat{\varrho}(t) + \hat{\alpha}(t) \qquad (5.8)$$

where the random variable $\Psi(t)$ represents the contribution of the clock jitter of DAC ϕ_{cj}^{dac} and two jitter components present in ADC output

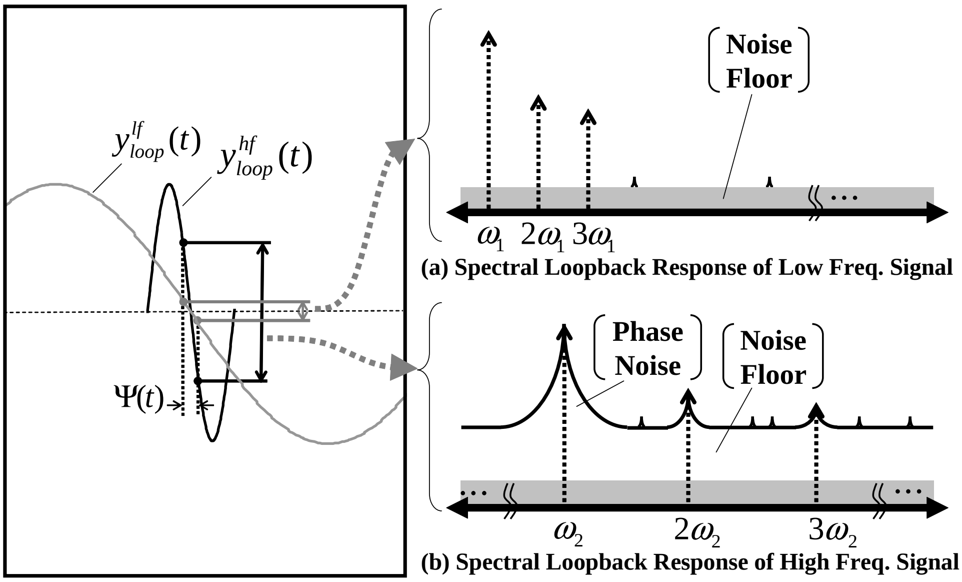
(ϕ_{cj}^{adc} and φ^{adc}). In addition $\hat{\varrho}(t)$, $\hat{\alpha}(t)$ and $\hat{\kappa}_i$ represent quantization noise, additive noise and the harmonic coefficient introduced by the loopback path when the high frequency signal is applied.

The relationship between Equation 5.7 and 5.8 can be analyzed by comparing the equations as follows.

It can be observed that effect of $\alpha(t)$ is almost the same as that of $\hat{\alpha}(t)$. Two different frequency input signals are sampled at the same sampling rate and sample size based on coherent sampling for our two loopback tests. Thus almost equal powers are consumed to sample each input signal in the two tests. The almost equal power dissipation leads to quite similar amount of thermal noise which is dominant in additive noise [37]. Thus the RMS values of random variables $\alpha(t)$ and $\hat{\alpha}(t)$ in Equation 5.7 and 5.8 have approximately same contribution on the spectral loopbacked response due to the very similar thermal noise in two loopback tests.

$\varrho(t)$ and $\hat{\varrho}(t)$ are determined by the resolution of the DAC and ADC in the loopback configuration, since quantization noise is determined by the resolution of the measurement [29, 37]. RMS values of $\varrho(t)$ and $\hat{\varrho}(t)$ give approximately the same contribution to the quantization noise power in the spectrum, since both the two different frequency signals are sampled at the same resolution of the DAC and ADC.

As a result, the contribution of the sum of $\varrho(t)$ and $\alpha(t)$ represents almost the same as that of the sum of $\hat{\varrho}(t)$ and $\hat{\alpha}(t)$ in the spectral response. As



(a) Spectral Loopback Response of Low Freq. Signal

(b) Spectral Loopback Response of High Freq. Signal

Figure 5.3: Contribution of Loopbacked Output on Spectral Response

shown in Fig.5.3-(a) and (b), the gray parts in the two plots indicate the noise floors with the same averaged power, and they represent the spectral response of $\varrho(t)$ and $\alpha(t)$, and the spectral response of $\hat{\varrho}(t)$ and $\hat{\alpha}(t)$, respectively.

On the other hand, the jitter-induced noise introduced by $\Psi(t)$ in Equation 5.8 makes a significant contribution to loopbacked spectral response as shown in Fig.5.3-(b). Basically higher noise floor and close-in phase noise shape due to jitters are superimposed on the gray noise floor.

External clock jitter can be readily identified by external equipment such as a spectrum analyzer, since a clock signal generator such as a crystal oscillator is implemented on the load board in Fig. 5.2. Thus the RMS value of ϕ_{cj}^{adc} and ϕ_{cj}^{dac} can be easily identified, thereby directly calculating $\Psi(t)$.

Finally characteristic parameters are obtained from spectral responses, and spectral equations are derived from Equation 5.7 and 5.8. Then the aperture jitter is identified by solving the spectral equations using the characteristic parameters and $\Psi(t)$.

To summarize, as shown in Fig.5.4, six jitter components are present in DAC and ADC. Our efficient loopback test system requires the characterization of only three jitter components in ADC channel. As a result, our method allows us to precisely predict aperture jitter of the ADC using DAC output with clock jitter-induced noise. It further means that our method replaces the need for an expensive, low-jitter signal synthesizer which is essential for conventional test.

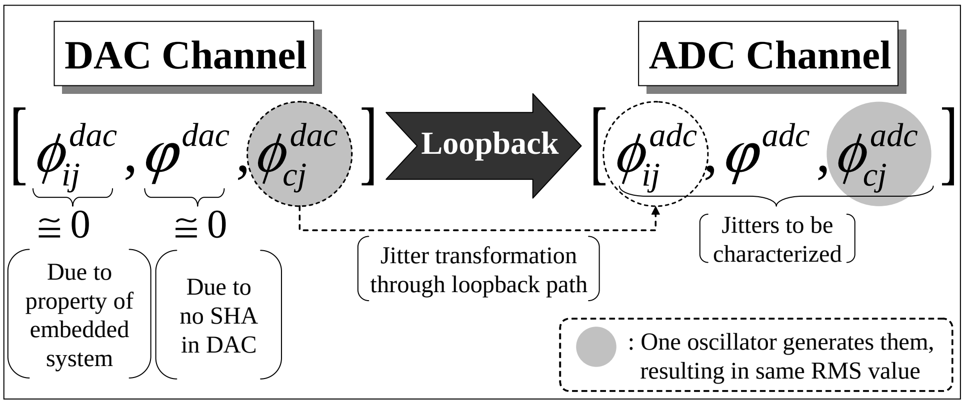


Figure 5.4: Relationship of Jitters in Our Loopback Scheme

Many approaches [23, 56, 61] ignore the jitter effects introduced by harmonics, and also additive noise is not considered to predict aperture jitter, since calculating these factors can make an approach so complicated, thereby increasing prediction error. However, our methodology considers additive noise for aperture jitter prediction, and also it calculates a magnitude of aperture jitter present in up to the third harmonic by an efficient analysis, resulting in a highly accurate measurement of aperture jitter.

5.2.2 Quantitative Analysis

We quantify the behavior of two different frequency input signals in order to characterize aperture jitter.

5.2.2.1 Loopback Test I

Harmonics and noise are characterized when low frequency signal is applied in loopback mode.

(i) Characterization of Harmonic Distortion Parameter: We assume that a unit magnitude, low frequency signal $\cos(w_1 t)$ is applied to a DAC, and jitter-induced noise is ignored as discussed in the previous section. Harmonic distortion is considered up to the third order. The DAC output response $y_{dac}^{lf}(t)$ can be expressed by a *Taylor* expansion as follows [63].

$$\begin{aligned} y_{dac}^{lf}(t) &= \sum_i d_i \cos^i(\omega_1 t) \\ &= \left(d_1 + \frac{3d_3}{4}\right)\cos(\omega_1 t) + \frac{d_2}{2}\cos(2\omega_1 t) + \frac{d_3}{4}\cos(3\omega_1 t) \end{aligned} \tag{5.9}$$

where d_1, d_2 and d_3 are the first, second and third harmonic coefficients of DAC channel respectively. As shown in Fig. 5.5, suppose the distorted and noisy analog signal $y_{dac}^{lf}(t)$ is loopbacked to the ADC channel, then the loopbacked response $y_{loop}^{lf}(t)$ can be expressed as

$$\begin{aligned} y_{loop}^{lf}(t) &= a_1 y_{dac}^{lf}(t) + a_2 \left(y_{dac}^{lf}(t)\right)^2 + a_3 \left(y_{dac}^{lf}(t)\right)^3 \\ &= (a_1 d_1)\cos(\omega_1 t) + (a_1 d_2 + a_2 {d_1}^2)\cos^2(\omega_1 t) \\ &\quad + (a_1 d_3 + 2a_2 d_1 d_2 + a_3 {d_1}^3)\cos^3(\omega_1 t) \end{aligned} \tag{5.10}$$

where a_1, a_2 and a_3 are the first, second and third harmonic coefficients of the ADC channel, respectively.

(ii) Characterization of Noise Parameter: In addition to harmonic distortion, quantization noise and additive noise are dominant in loopbacked response. Assume that the noise of the DAC and the ADC channel are uncorrelated. The output referred noise present in loopbacked response, P_{qa}^{loop} is calculated by performing *Fast Fourier Transformation* (FFT) on the experimentally measured loopback response.

5.2.2.2 Loopback Test II

In this section, harmonic distortion and noise are characterized to separate aperture jitter from other jitters, quantization noise and additive noise. ***(i) Characterization of Harmonic Distortion Parameter***: A unit magnitude, high frequency signal $\cos(w_2 t)$ is applied to the DAC in *Loopback Test II*. As derived in Equation 5.9 and 5.10, the DAC output $y_{dac}^{hf}(t)$ and loopbacked response $y^{hf}_{loop}(t)$ become

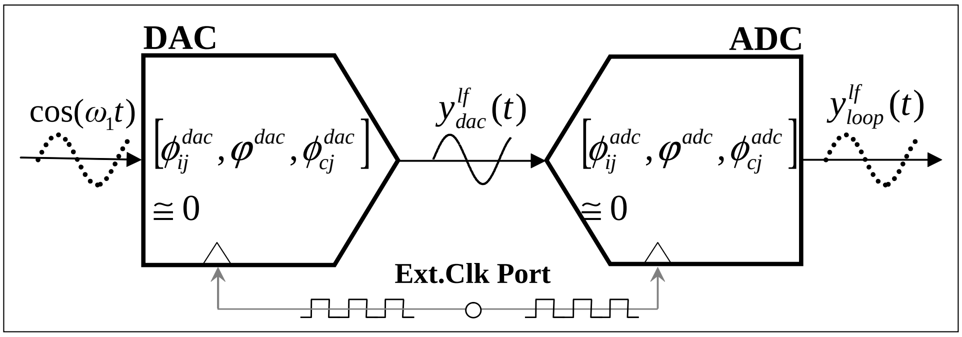
$$\begin{aligned}
y^{hf}_{dac}(t) &= \sum_i \hat{d}_i \cos^i(\omega_2(t+\phi^{dac}_{cj})) \\
y^{hf}_{loop}(t) &= (\hat{a}_1\hat{d}_1)\cos(\omega_2(t+\varphi^{adc}+\Phi)) \\
&\quad + (\hat{a}_1\hat{d}_2+\hat{a}_2\hat{d}_1^{\,2})\cos^2(\omega_2(t+\varphi^{adc}+\Phi)) \\
&\quad + (\hat{a}_1\hat{d}_3+2\hat{a}_2\hat{d}_1\hat{d}_2+\hat{a}_3\hat{d}_1^{\,3})\cos^3(\omega_2(t+\varphi^{adc}+\Phi)) \\
&= \left(\kappa_1+\frac{3}{4}\kappa_3\right)\cos(\omega_2(t+\varphi^{adc}+\Phi)) \\
&\quad + \frac{\kappa_2}{2}\cos(2\omega_2(t+\varphi^{adc}+\Phi)) \\
&\quad + \frac{\kappa_3}{4}\cos(3\omega_2(t+\varphi^{adc}+\Phi))
\end{aligned} \tag{5.11}$$

where $\hat{d}_i$ and $\hat{a}_i$ are the harmonic coefficients of the DAC and ADC channel respectively, and $\kappa_1 = \hat{a}_1\hat{d}_1$, $\kappa_2 = \hat{a}_1\hat{d}_2+\hat{a}_2\hat{d}_1^{\,2}$ and $\kappa_3 = \hat{a}_1\hat{d}_3+2\hat{a}_2\hat{d}_1\hat{d}_2+\hat{a}_3\hat{d}_1^{\,3}$, and $\Phi = \phi^{adc}_{cj} + \phi^{dac}_{cj}$. As discussed previously, clock jitter of the DAC ϕ^{dac}_{cj} becomes input jitter of the ADC ϕ^{adc}_{ij} as shown in Fig.5.5-(b). It allows us to easily find clock jitters of the DAC and ADC ($\phi^{dac}_{cj}(\equiv \phi^{adc}_{ij})$ and ϕ^{adc}_{cj}), since external clock jitter can be readily identified by external equipment. Thus Φ is directly identified.

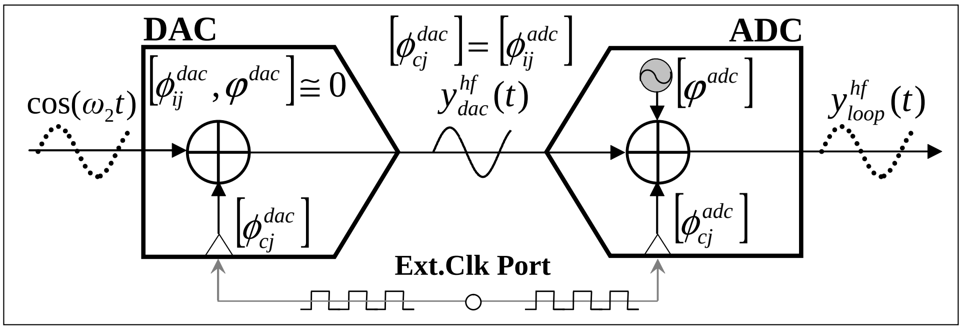
Equation 5.11 can be rewritten as

$$\begin{aligned}
y^{hf}_{loop}(t) = \Upsilon_1\cos(\omega_2(t+\varphi^{adc}+\Phi)) &\longrightarrow (a) \\
+ \Upsilon_2\cos(2\omega_2(t+\varphi^{adc}+\Phi)) &\longrightarrow (b) \\
+ \Upsilon_3\cos(3\omega_2(t+\varphi^{adc}+\Phi)) &\longrightarrow (c)
\end{aligned} \tag{5.12}$$

where $\Upsilon_1 = \left(\kappa_1+\frac{3}{4}\kappa_3\right)$, $\Upsilon_2 = \frac{\kappa_2}{2}$, $\Upsilon_3 = \frac{\kappa_3}{4}$. Aperture jitter can be separated in Equation 5.12 as derived in Equation 5.1∼5.5. At first the fundamental



(a) Scheme for Loopback Test I



(b) Scheme for Loopback Test II

Figure 5.5: Our Loopback Scheme for Quantitative Analysis

signal term $y^{hf}_{loop\_\omega_2}(t)$ (Equation 5.12-(a)) and its aperture jitter-induced error $y_{j\_\omega_2}(t)$ become

$$\begin{aligned} y^{hf}_{loop\_\omega_2}(t) &= \Upsilon_1\{\cos(\omega_2 t)\cos(\omega_2(\varphi^{adc}+\Phi)) \\ &\quad - \sin(\omega_2 t)\sin(\omega_2(\varphi^{adc}+\Phi))\} \\ y_{j\_\omega_2}(t) &= -\Upsilon_1(2\pi f)(\varphi^{adc}+\Phi)\sin(\omega_2 t) \end{aligned} \tag{5.13}$$

where f represents the input signal frequency. RMS value and power of the aperture jitter-induced error are derived as

$$\begin{aligned} y^{rms}_{j\_\omega_2} &= \sqrt{2}\pi f \Upsilon_1(\sigma^{adc}_{aj} + \sigma_\Phi) \\ P_{j\_\omega_2} &= 2\pi^2 f^2 {\Upsilon_1}^2(\sigma^{adc}_{aj} + \sigma_\Phi)^2 \end{aligned} \tag{5.14}$$

where $\sigma_\Phi = \sqrt{(\sigma^{dac}_{cj})^2 + (\sigma^{adc}_{cj})^2}$, and σ^{dac}_{cj} and σ^{adc}_{cj} are RMS values of ϕ^{dac}_{cj} and ϕ^{adc}_{cj}, respectively. Assume $\omega\varphi_{adc} \ll 1$.

Similarly jitter-induced noise powers introduced by the second and third harmonic components (Equation 5.12-(b) and (c)) are expressed by

$$\begin{aligned} P_{j\_2\omega_2} &= 8\pi^2 f^2 {\Upsilon_2}^2(\sigma^{adc}_{aj} + \sigma_\Phi)^2 \\ P_{j\_3\omega_2} &= 18\pi^2 f^2 {\Upsilon_3}^2(\sigma^{adc}_{aj} + \sigma_\Phi)^2 \end{aligned} \tag{5.15}$$

The power of total jitter P_{j_loop} becomes

$$P_{j\_loop} = 2\pi^2 f^2({\Upsilon_1}^2 + 4{\Upsilon_2}^2 + 9{\Upsilon_3}^2)(\sigma^{adc}_{aj} + \sigma_\Phi)^2 \tag{5.16}$$

Each harmonic coefficient in Equation 5.12 is expressed as the spectral representation by FFT as follows.

$$Y^{hf}_{loop}(i\omega_2) = \frac{\Upsilon_i}{2} \tag{5.17}$$

Consequently P_{j_loop} of Equation 5.16 can be rewritten as

$$\begin{aligned} P_{j\_loop} = \frac{\pi^2 f^2}{2} &\left\{ \left(Y^{hf}_{loop}(\omega_2)\right)^2 + 4\left(Y^{hf}_{loop}(2\omega_2)\right)^2 + 9\left(Y^{hf}_{loop}(3\omega_2)\right)^2 \right\} \\ &(\sigma^{adc}_{aj} + \sigma_\Phi)^2 \end{aligned} \tag{5.18}$$

Each harmonic coefficient $Y^{hf}_{loop}(i\omega_2)$ is calculated by performing FFT on the experimentally measured loopback response. Equation 5.18 is re-used for jitter characterization in the next chapter.

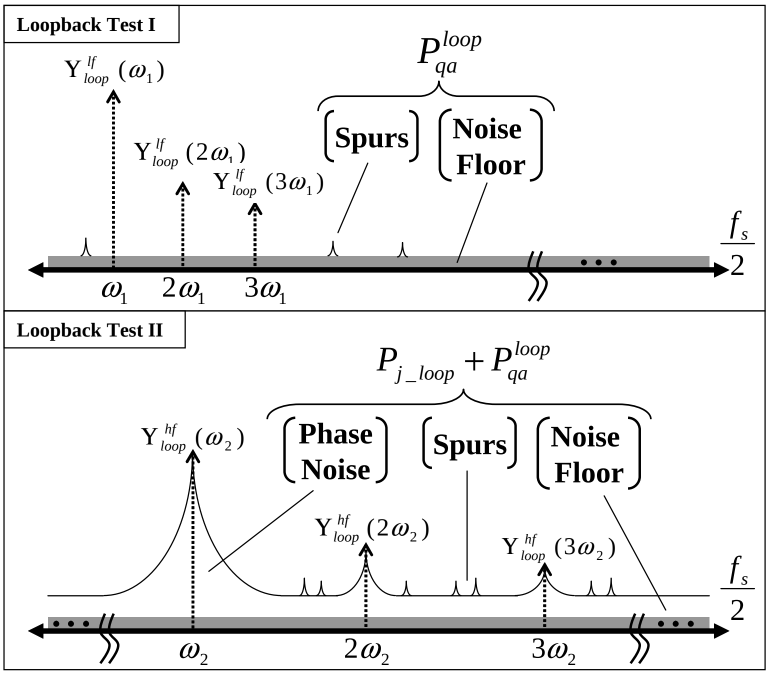


Figure 5.6: Loopbacked Spectral Response Based on Our Methodology

(ii) Characterization of Noise Parameter: P_{qa}^{loop}, which is the power of quantization and additive noise obtained in *Loopback Test I*, also represents the power of quantization and additive noise introduced by *Loopback Test II* as shown in gray parts of Fig.5.6-(a) and (b). In addition higher noise floor and close-in phase noise shape due to jitters are superimposed on the gray noise floor in *Loopback Test II.* Thus the total spectral noise power of *Loopback Test II* is given by the sum of total jitter induced-noise power P_{j_loop} and the power of quantization and additive noise P_{qa}^{loop}. P_{j_loop} is calculated by subtracting P_{qa}^{loop} from P_{total}^{hf} which is the total noise power integrated within

Nyquist frequency in *Loopback Test II* response.

$$P_{j\_loop} = P_{total}^{hf} - P_{loop}^{qa} \tag{5.19}$$

Since *Loopback Test I* and *II* are performed at same sampling rate, P_{total}^{hf} and P_{loop}^{qa} are the powers which are integrated within the same *Nyquist* frequency.

(iii) Characterization of Aperture Jitter: To summarize, each harmonic coefficient $Y_{loop}^{hf}(i\omega_2)$ and total jitter induced-noise power P_{j_loop} are calculated by Equation 5.17 and 5.19. In addition σ_Φ is directly identified by finding RMS value of Φ which is obtained previously.

Finally given $Y_{loop}^{hf}(i\omega_2)$, P_{j_loop} and σ_Φ, σ_{aj}^{adc} can be determined in Equation 5.18.

5.3 Experimental Results

Hardware measurements were performed on the commercial converters, Analog Devices DAC(AD9764) and National Semiconductor ADC(ADC14L105) to evaluate the proposed method.

5.3.1 Hardware Measurements

The ADC14L105 is a monolithic pipelined, 14-bit resolution and 105MSPS sampling rate ADC. The AD9764 is a 14-bit resolution, 125MSPS sampling rate and current output DAC. A Device Interface Board (DIB) for ADC inter-

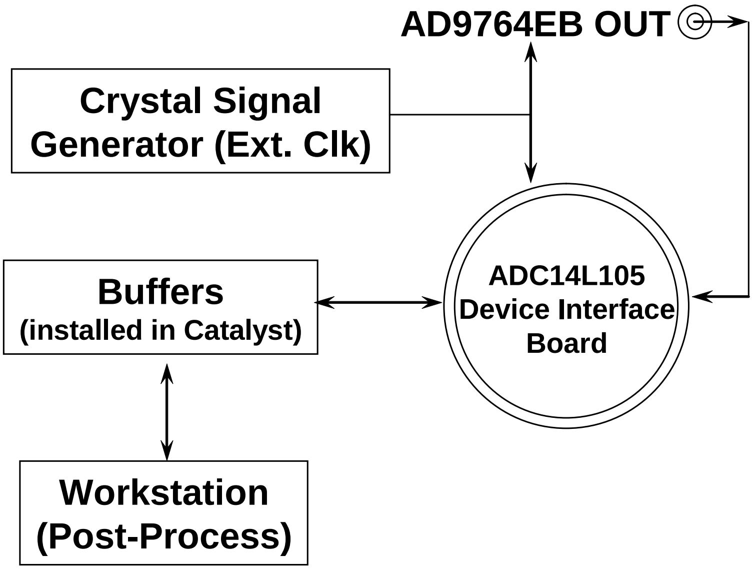


Figure 5.7: Experiment Setup

face was manufactured, and an evaluation board AD9764EB for DAC interface was used. As shown in Fig 5.7, the noisy analog signal at the output of the DAC board was loopbacked to the ADC using Sub-Miniature version A (SMA) cable. The digitized data was transferred to the host computer through the buffers installed in the *Catalyst*, and post-processing was then done to characterize the aperture jitter of the DUT.

The amplitude-controllable signal generator was manufactured to provide an external clock signal to the DAC and ADC as shown in Fig.5.8. 100MHz clock signal was used for running the DAC and ADC. Pads for two different footprints of crystal oscillators and four types of programmable attenuators (Unbalanced Tee, Balanced Tee, Unbalanced PI and Bridged Tee) were installed for the generator. Several crystal oscillators and different types of programmable attenuators were evaluated using the *Agilent* spectrum analyzer E4443A to determine a crystal with the best jitter performance and an attenuator to provide good attenuation. To measure actual RMS clock jitter, a standard phase noise conversion method [2] was performed using E4443A. Fig.5.9 shows phase noise in dBc/Hz of the external clock signal which is used to calculate RMS jitter based on the specified frequency range. To calculate RMS jitter, phase noise was integrated from 20Hz to 200MHz based on a standard jitter measurement procedure [2]. The best crystal was Crystek Crystal CCO-083-100 with 1.1ps RMS jitter. In addition each attenuator has the attenuation value from 0.1dB to 64.5dB in 0.1 dB increments.

High precision jitter measurement instrument *Timing Jitter Digitizer* (TJD) in the ATE *Catalyst* was used to measure actual RMS total jitter, σ_{tj}^{loop} in loopbacked response and actual input jitter due to bench test setup. Then the actual RMS aperture jitter was determined by subtracting $\left(\sigma_{ij}^{dac}\right)^2 + \left(\sigma_{cj}^{dac}\right)^2 + \left(\sigma_{cj}^{adc}\right)^2$ from $\left(\sigma_{tj}^{loop}\right)^2$ and performing the square-root of the subtraction result. Also σ_{ij}^{dac} was calculated since the experiments were performed in bench setup. The instrument provides more accurate measurement results than SNR based method [3]. Thus our results were compared to these ATE results as reference.

When 77.76MHz sine wave was applied to the ADC, σ_{tj}^{loop} and σ_{ij}^{dac} were measured using TJD, which were 1.587ps and 98.313fs, respectively. Aperture jitter was calculated as 0.301ps by the calculation which is mentioned above.

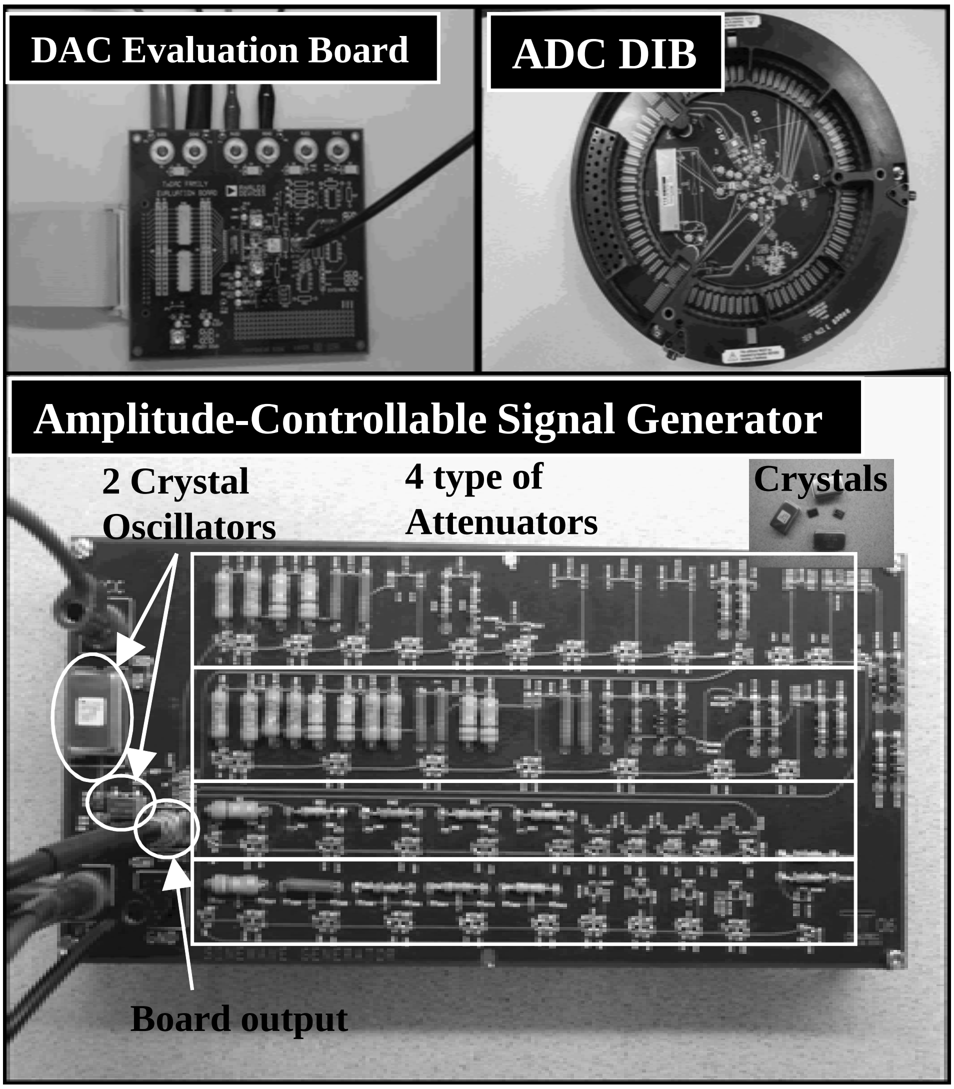


Figure 5.8: DAC Evaluation and ADC DIB, and Crystals Signal Generator

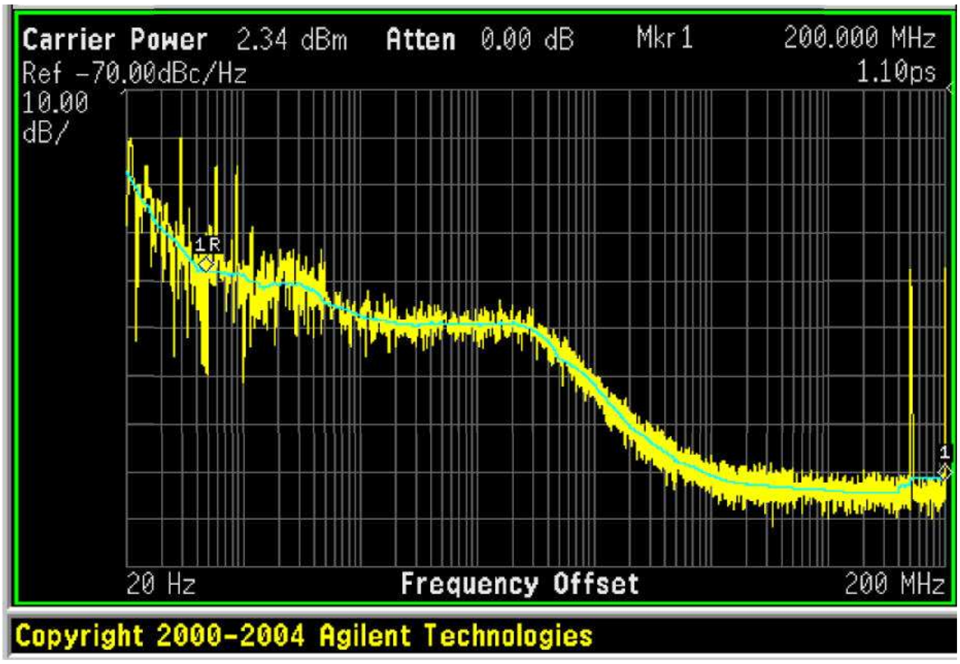


Figure 5.9: Phase Noise of Clock Signal for Clock Jitter Estimation

Table 5.1: Parameters Used for Hardware Measurements

Test1	**Test2**	**Test3**	**Test4**
12.96 MHz	38.88 MHz	58.32 MHz	77.76 MHz

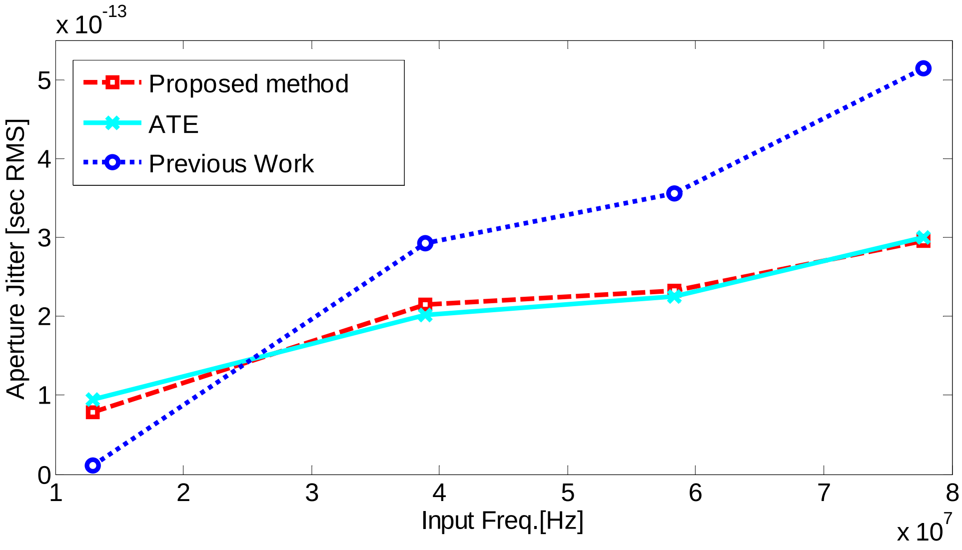


Figure 5.10: Comparison between Proposed Method and Previous Work [61]

Fig.5.10 shows the predicted values of the ADC aperture jitter based on our method as well as previous work [61], compared to ATE results. For the proposed method and previous work, 1 MHz sine wave was applied to ADC for the low frequency input signal. Four different frequency signals were used for high frequency input in each test as shown in Table 5.1. ATE results were obtained by TJD using the input signals as listed in Table 5.1. As shown in Fig.5.10, previous work almost does not detect aperture jitter in the *Test1*, compared to the proposed method and ATE results. This is because jitter-induced error with a positive value would be canceled by error with a negative value during subtraction in the time domain. Furthermore the magnitude of jitter-induced error is very small with low frequency signal. Thus the resultant values of subtraction become much smaller due to the cancellation. As the input signal frequency increased, the prediction error of previous method was increased, since the technique poorly separates jitter-induced noise from additive noise and clock jitter-induced noise. On the other hand, our method shows highly accurate results even when applying both low and high frequency input signals. Since the powers of additive noise and quantization noise are analytically removed from the spectral response, the aperture jitter-induced noise can be accurately calculated. The averaged error of the proposed method was 11fs, and previous work had 130fs for the averaged error.

5.3.2 Repeatability of Jitter Prediction

Table 5.2 shows the measurement setup for the repeatability of jitter prediction. The repeatability of the aperture jitter measurement was very good, as shown in Fig.5.11, where it can be seen that the aperture jitter is of the order of 0.3 ps, in good agreement with the ATE results. Table 5.3 summarizes the statistics of the repeatability. The standard deviation based on our approach was less than 50 fs.

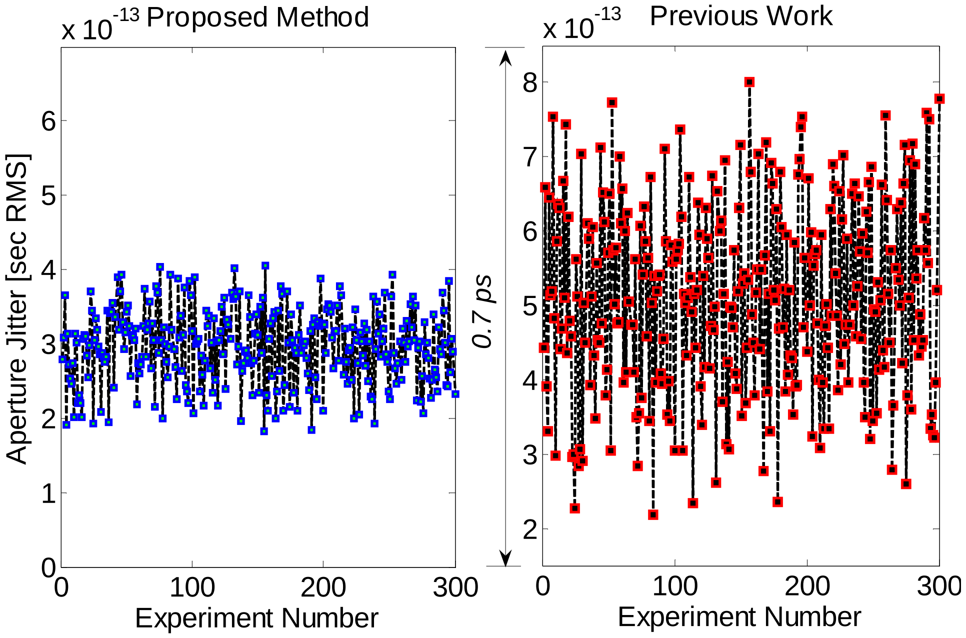


Figure 5.11: Repeatability of Proposed Method and Previous Work [61]

Table 5.2: Parameters Used for Repeatability

Low Freq. of Input	**High Freq. of Input**	**Clk.**
1 MHz	77.76 MHz	100 MHz

Table 5.3: Repeatability of Hardware Measurements

Approach	**Mean**	**STD.**	**Max.**	**Min.**
Proposed Method	0.295 ps	45.324 fs	0.399 ps	0.182 ps
Previous Work [61]	0.512 ps	126.682 fs	0.800 ps	0.218 ps

5.3.3 Classification Accuracy

Misclassification is one way to evaluate the performance of a proposed methodology. The 30 DUTs were classified by comparing predicted aperture jitter of the proposed method with its specification limit 0.5 ps. The results of the DUT classifications are summarized in Table 5.4, showing the very high classification accuracy. All the 23 DUTs, which were classified into *Pass* group in our method results, were the subset of 25 DUTs that were in *Pass* group in actual classification. In addition there were 2 DUTS which barely passed in actual classification. These 2 parts were misclassified due to measurement error, even though our results in Table 5.3 were great.

Table 5.4: Classification Accuracy

Performance Parameter	**Pass**	**Fail**
Actual Classification	25	5
Predicted Classification	23	7

5.4 Summary

In this paper, we proposed a novel methodology for accurate aperture jitter prediction using an efficient loopback test. Two tests are performed for our method. In the first loopback test, a low frequency sinusoidal signal is applied to the DUT in loopback mode, and the spectral loopbacked response is characterized to find non-jitter related noise. In the second loopback test, a high frequency signal is applied and the resultant response is analyzed to find jitter induced-noise as well as non-jitter related noise. As a result, characteristic parameters are obtained from their spectral response, and spectral equations of loopbacked response are derived by an efficient loopback analysis. The equations are solved using characteristic parameters, thereby accurately separating the aperture jitter from input and clock jitter, and quantization noise and additive noise based on low-cost and efficient loopback scheme. The proposed method provides an efficient solution on the problems associated with precisely separating aperture jitter component from other jitters and additive noise to predict aperture jitter. The results of hardware measurement with DACs (AD9764) and ADCs (ADC14L105) show reduction in the error of aperture jitter to be 11fs compared with a much higher value for previous work. The repeatability results from our method indicate that our predictive accuracy is reliable and stable. Thus our method can be effectively used to predict the aperture jitter of a mixed-signal circuit.

Chapter 6

Conclusion

We proposed a novel methodology for accurate predictions from optimized signatures in Chapter 3. A sinusoidal signal is applied to a DUT and the resultant output signal is manipulated into the optimized signatures by using low-cost comparators and digital circuits. To predict the performance parameters of a DUT, the correlation functions which map the obtained signatures to the specifications are generated by a regression technique. The proposed method provides improved performance on the problems associated with representing the exact relationship between signatures and specifications due to nonlinear characteristics. The results of hardware measurement with DACs (AD9764) show error reductions of THD, SNR and SINAD as 1.4dB, 2.3dB, and 2.1dB compared with the TSR technique. In addition, we evaluated the sensitivities of this technique to common non-idealities, such as the variations of reference voltages and sampling rate of BIST circuits. The results from our method with low sensitivity indicate that our predictive accuracy is reliable and stable. Also, other set of hardware measurements were performed with commercial DACs and ADCs (AD9764 and National Semiconductor ADC14L105) to evaluate the performance of the proposed method on the application for loopback mode. The results based on the proposed method provides improved performance on the fault masking problem in loopback test by low predictive specification errors. Thus, the proposed method can be used effectively to predict the specifications of a mixed-signal circuit.

In Chapter 4, we proposed an efficient loopback test methodology utilizing the characteristics of the RF transformers on a loadboard. The proposed method characterizes the performance parameters of individual channels in the loopback mode. A sinusoidal signal was applied to DUTs in the loopback mode, and the differently weighted loopbacked responses were obtained. The responses were used to characterize the individual DUT specifications with the derived nonlinear DUT model. The proposed method provides an efficient solution to the problems associated with characterizing the DUT specifications, due to the imbalance introduced by DfT circuitry to split the performance of the DUTs on the differential loopback path. The results of the hardware measurements on DACs (AD9764) and ADCs (ADC14L105) indicate low SINAD prediction errors of 1.4dB and 0.5dB respectively. The predictive accuracy of our method is reliable and stable. Thus, the proposed method can be effectively used to predict the specifications of a mixed-signal circuit.

Chapter 5 addresses a novel methodology for accurate aperture jitter prediction using efficient loopback test. Two tests are performed for our method. In the first loopback test, a low frequency sinusoidal signal is applied to a DUT in loopback mode, and the spectral loopbacked response is characterized to find non-jitter related noise. Similarly in the second loopback test, a high frequency signal is applied and the resultant response is analyzed to find jitter induced-noise as well as non-jitter related noise. As a result, characteristic parameters are obtained from their spectral response, and spectral equations are derived to characterize jitters present in a DUT. To predict the aperture jitter of a DUT, the equations are solved by accurately separating the aperture jitter from input and clock jitter, and quantization noise and additive noise based on low-cost and efficient loopback scheme. To more accurately measure aperture jitter, jitter model based on all jitter components present in mixed-signal circuit is used, and jitter components introduced by up to third harmonics are considered to predict aperture jitter. The proposed method provides an efficient solution on the problems associated with separating aperture jitter component from other jitters and random noise to predict aperture jitter. The results of hardware measurement with DACs (AD9764) and ADCs (ADC14L105) show error reductions of aperture jitter as 11 fs compared with the previous work. The results from our method with low sensitivity indicate that our predictive accuracy is reliable and stable. Thus, the proposed method can be effectively used to predict the aperture jitter of a mixed-signal circuit.

As mentioned above, the dissertation has proposed and examined new approaches for testing analog and mixed-signal circuits. The aim of this dissertation is to develop cost-effective performance-based test methodology based on BIST and BOST, without loss of test quality. Our research has laid the groundwork for further advancement in BIST and BOST schemes for the analog and mixed-signal cores in SoCs. In order to use the approach in wide band range, our statistical alternative test methodology can use a magnitude detector which is commonly used in RF testing, instead of using comparators. Furthermore the silicon implementation of the BIST scheme will show the more possibility that the test scheme can be used for production test. Our test approach on differential signaling can test high-speed mixed-signal device as well as base band applications. The methodology can therefore be applied to DfT logic to test the front-end components in RF circuits. For our methodology on aperture jitter measurement, the testability could be increased by applying oscillation-based techniques [7, 68]. BIST and BOST design will continue to be an important topic in the area of production test. The techniques proposed in this dissertation are demonstrated as an application for a couple of devices, and therefore have the potential of being further improved or expanded to meet the future demands.

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