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Energy-Efficient Data Converter Design in Scaled CMOS Technology

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Energy-Efficient Data Converter Design in Scaled CMOS Technology

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Dedicated to my parents.

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Energy-Efficient Data Converter Design in Scaled CMOS Technology

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Data converters bridge the physical and digital worlds. They have been the crucial building blocks in modern electronic systems, and are expected to have a growing significance in the booming era of Internet-of-Things (IoT) and 5G communications. The applications raise energy-efficiency requirements for both low-speed and high-speed converters since they are widely deployed in wireless sensor nodes and portable devices. To explore the solutions, the author worked on three directions: 1) techniques to improve the efficiency of the low-speed converters including the comparator; 2) techniques to develop high-speed data converters including the reference stabilization; 3) new architecture to improve the efficiency of the capacitance-to-digital converter (CDC).

In the first part, a power-efficient 10-bit SAR ADC featured with a gain-boosted dynamic comparator is presented. In energy-constrained applications, the converter is usually supplied with low supply voltage (e.g., 0.3

V-0.5 V), which reduces the comparator pre-amplifier (pre-amp) gain and results in higher noise. A novel comparator topology with a dynamic common-gate stage is proposed to increase the pre-amplification gain, thereby reducing noise and offset. Besides, statistical estimation and loading switching techniques are combined to further improve energy efficiency. A 40-nm CMOS prototype achieves a Walden FoM of 1.5 fJ/conversion-step while operating at 100-kS/s from a 0.5-V supply.

To further improve the energy-efficiency of the comparator, a novel dynamic pre-amp is proposed. By using an inverter-based input pair powered by a floating reservoir capacitor, the pre-amp realizes both current reuse and dynamic bias, thereby significantly boosting g_m/I_D and reducing noise. Moreover, it greatly reduces the influence of the input common-mode (CM) voltage on the comparator performance, including noise, offset, and delay. A prototype comparator in 180-nm achieves 46-μV input-referred noise while consuming only 1 pJ per comparison under 1.2-V supply, which represents greater than 7 times energy efficiency boost compared to that of a Strong-Arm (SA) latch.

The second part of this dissertation focuses on high-speed data converter techniques. A 10-bit high-speed two-stage loop-unrolled SAR ADC is presented. To reduce the SAR logic delay and power, each bit uses a dedicated comparator to store its output and generate an asynchronous clock for the next comparison. To suppress the comparator offset mismatch induced non-linearity, a shared pre-amp are employed in the second fine stage, which

is implemented by a dynamic latch to avoid static power consumption. The prototype ADC in 40-nm CMOS achieves 55-dB peak SNDR at 200-MS/s sampling rate without any calibration.

A key limiting factor for the SAR ADC to simultaneously achieve high speed and high resolution is the reference ripple settling problem caused by DAC switching. Unlike prior techniques that aim to minimize the reference ripple which requires large reference buffer power or on-chip decoupling capacitance area, this work proposes a new perspective: it provides an extra path for the full-sized reference ripple to couple to the comparator but with an opposite polarity, so that the effect of the reference ripple is canceled out, thus ensuring an accurate conversion result. The prototype 10-bit 120-MS/s SAR ADC is fabricated in 40-nm CMOS process and achieves an SNDR of 55 dB with only 3 pF reference decoupling capacitor.

Finally, this dissertation also presents the design of an incremental time-domain two-step CDC. Unlike the classic two-step CDC, this work replaces the OTA-based active-RC integrator with a VCO-based integrator and performs time domain (TD) $\Delta\Sigma$ modulation. The VCO is mostly digital and consumes low power. Featuring the infinite DC gain in phase domain and intrinsic spatial phase quantization, this TD$\Delta\Sigma$ enables a CDC design, achieving 85-dB SQNR by having only a 4-bit quantizer, a 1st-order loop and a low OSR of 15. The prototype fabricated in 40-nm CMOS achieves a resolution of 0.29 fF while dissipating only 0.083 nJ per conversion, which improves the energy efficiency by greater than 2 times comparing to that of state-of-the-art CDCs.

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Chapter 1

Introduction

The Internet-of-Things (IoT) is exploding, which spurs innovation across many industries and provides a platform enabling emerging technologies such as the ubiquitous sensing to become an integral part of our economy and lifestyle. A ubiquitous sensor network (USN) is one that connects all possible sensors in a given network or environment. It integrates wireless sensor nodes, data converters, built-in computational resources, and wireless transceivers. As the portal connecting the physical world to computational intelligence, the converters' performance is crucial in the USN. Primarily, these data converters must be low-power since they are widely deployed in the energy-constrained platforms, which are usually powered by coin batteries and/or energy harvesters. On the other side, device connectivity, including wireless transceivers and data links, provides communication ability and forms the foundation of IoT. Again, as the critical component, data converters here need to offer both high throughput and low energy consumption. In this dissertation, the author explores solutions for these two categories: 1) low-power data converters for the sensor front-end; 2) energy-efficient data converters for data links.

Successive approximation register (SAR) ADCs are becoming increas-

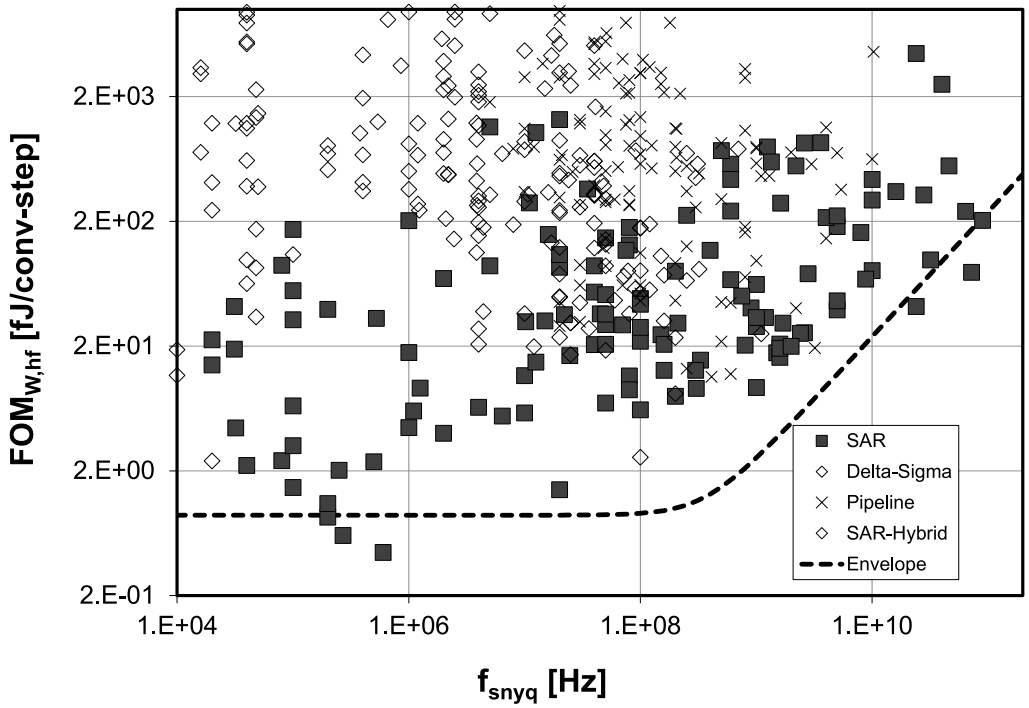


Figure 1.1: Prior ADC works plotted against conversion speed and energy efficiency.

ingly popular due to their scaling friendliness, which makes them highly power and area efficient in advanced CMOS process, as evidenced by the ADC survey in Fig. 1.1 [Murmann et al. [2019]]. There are two fundamental design specs for the ADCs which are f_{snyq} standing for the Nyquist sampling frequency and $ENOB$[1] representing effective number of bits of the converter. Besides, to characterize the energy efficiency of the ADC, the Walden figure of merit

[1]Effective Number of Bits. Calculated from signal to noise and distortion ratio (SNDR). $ENOB = \frac{SNDR-1.76}{6.02}$

(FoM_W[2]) is widely used. As can be seen, energy efficiencies of the SAR and SAR-hybrid architectures advance in all frequency bands. The main reason is that most circuits of a SAR ADC are digital, making it very amenable to technology scaling. Therefore, with the feature sizes of CMOS devices scaled down, SAR ADCs are becoming more and more efficient.

A standard SAR ADC is shown in Fig. 1.2 containing 4 main blocks: 1) a sample and hold circuit that acquires the input voltage V_{IN}; 2) a switched-capacitor (SC) digital-to-analog converter (DAC) array that outputs the feedback voltage V_{DAC} to successively approximate V_{IN} in a binary search fashion; 3) a comparator that compares V_{IN} with V_{DAC}; and 4) a SAR logic that takes the comparator output and reconfigures the DAC array.

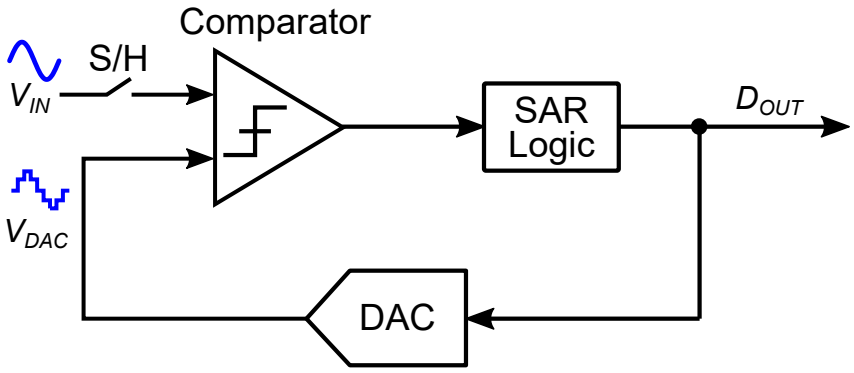


Figure 1.2: SAR ADC Architecture.

In SAR ADCs, the primary sources of power dissipation are the digital control circuit, comparator, and capacitive DAC network. Digital power consumption becomes lower with the advancement of technology. Various

[2] $FoM_W = \frac{P}{2^{ENOB} \cdot f_{snyq}}$

techniques have been proposed to lower the switching energy by 37% (split-capacitor method in [Chen and Brodersen [2006b]]), 56% (energy-saving method in [Ginsburg and Chandrakasan [2005]]), 81% (monotonic switching method in [Liu et al. [2010a]]), 88% (V_{cm}-based switching in [Hariprasath et al. [2010]]), and 98% (bi-directional single-side switching in [Sanyal and Sun [2013]]). However, the comparator power consumption becomes the bottleneck due to the fundamental thermal noise limitation. To address this issue, two techniques have been proposed to improve the energy-efficiency and performance of a dynamic comparator in a SAR ADC.

In a low-speed SAR ADC that embedded in sensor front-ends, a common technique to reduce power is to operate the ADC under a low-power supply voltage (e.g., 0.3 V-0.5 V). A key problem for the comparator to operate under such a low voltage is the reduced front-end pre-amp gain, leading to increased input referred noise and offset. To address this issue, a power-efficient 10-bit SAR ADC featured with a gain-boosted dynamic comparator is presented in the first part. A novel dynamic comparator topology with a common-gate stage is proposed to increase the pre-amplification gain, thereby reducing noise and offset. Besides, statistical estimation and loading switching techniques are combined to further improve energy efficiency. Moreover, the SAR sequencer and clock generator share only a single dynamic DFF chain to reduce the digital power. A 40-nm CMOS prototype achieves a Walden FoM of 1.5 fJ/conversion-step while operating at 100-kS/s from a 0.5-V supply.

To further improve the energy-efficiency of a comparator, a novel dy-

namic pre-amp is proposed. By using an inverter-based input pair powered by a floating reservoir capacitor, the pre-amp realizes both current reuse and dynamic bias, thereby significantly boosting g_m/I_D and reducing noise. Moreover, it greatly reduces the influence of the input CM voltage on the comparator performance, including noise, offset, and delay. A prototype comparator in 180-nm achieves 46-μV input-referred noise while consuming only 1 pJ per comparison under 1.2-V supply. This represents greater than 7 times energy efficiency boost compared to a classic Strong-Arm (SA) latch. It achieves the highest reported energy efficiency to authors' best knowledge.

The second part switches gear to explore the track of high-speed SAR ADCs which are widely-employed in device connectivity and communication systems. The main challenge becomes to increase the single-channel converter speed while maintaining the design efficiency. The limiting factor for a SAR ADC to achieve the higher throughput is its serial conversion algorithm, which usually requires N clock cycles for a N-bit data conversion. A few techniques have been proposed to reduce the conversion time[3]. Asynchronous operation is developed to reduce each conversion cycle time T_{clk} [Chen and Brodersen [2006b]]. Multi-bit per cycle is proposed to reduce the number of comparison cycles N, however at the cost of increased hardware and design complexity [Wei et al. [2012]]. Pipelining two-stage SAR ADCs can further increase the speed, but it suffers from inter-stage gain error and consumes large static power [Jeon et al. [2010]]. A loop-unrolled architecture [Jiang et al. [2012];

[3] $T_{conv} = T_{sample} + N \cdot T_{clk}$

Verbruggen et al. [2012]] incorporates multiple comparators to store its output and generate an asynchronous clock for the next comparison, which reduces critical cycle delay and boosts speed while requiring challenging and power consuming comparator offset mismatch calibration to prevent linearity degradation. To retrieve the simplicity and efficiency of the SAR architecture, a 10-bit fully-dynamic and calibration-free two-stage loop-unrolled SAR ADC is presented in this dissertation. To suppress the comparator offset mismatch induced non-linearity, a shared pre-amp are employed in the second fine stage, which is implemented using a dynamic latch to avoid static power consumption. The prototype ADC in 40-nm CMOS achieves 55-dB peak SNDR at 200-MS/s sampling rate without any calibration. It consumes 750 μW from 1.1-V power supply, leading to a Walden FoM of 8.6 fJ/conversion-step.

Benefited from the technology scaling, SAR ADCs have gone beyond 100MS/s with >10b resolution. With this core ADC performance advancing, to achieve high speed and high resolution simultaneously, exponentially elevated requirement has been put on the reference ripple settling caused by DAC switching. It is typically dominated by the package bond-wire LC resonance [Kapusta et al. [2013]; Chen et al. [2018]], which cannot benefit from technology scaling. A conventional solution requires either a wide-band buffer to ensure the fast ripple recovery while consuming large power(e.g., 4 times larger than the ADC core as in [Liu et al. [2016]]) or considerable on-chip decoupling capacitance (e.g., 200 times bigger decoupling capacitor than the CDAC in [Venca et al. [2016]]) to suppress the reference error amplitude to

be within 0.5 LSB. To tackle this issue, a novel ripple cancellation technique is proposed in this part. Unlike prior techniques that aim to minimize the reference ripple, this work proposes a new perspective: it provides an extra path for the full-sized reference ripple to couple to the comparator but with an opposite polarity, so that the effect of the reference ripple is canceled out, thus ensuring an accurate conversion result. The prototype 10-bit 120-MS/s SAR ADC is fabricated in 40-nm CMOS process and achieves an SNDR of 55 dB with only 3 pF reference decoupling capacitor. The proposed ripple cancellation technique improves the SNDR by 8 dB and reduces the worst-case INL/DNL by 10 times. Overall, the ADC achieves an SNDR of 55 dB with only 3 pF reference decoupling capacitor.

In the last part of this dissertation, the author explored the energy-efficient solution for capacitive sensor readout circuits by leveraging advanced ADC design techniques. Capacitive sensors are widely used to measure various physical quantities, including pressure, humidity, and displacement. Ultra-low-power capacitance-to-digital converters (CDCs) are required for sensors with limited battery capacity or powered by energy harvesters. A SAR CDC is simple to design and well-suited for low-to-medium resolution applications. However, to reach high resolution, it requires a low-noise comparator [Omran et al. [2016]] or OTA-based active charge transfer [Ha et al. [2014]], resulting in degraded power efficiency. The $\Delta\Sigma$ CDC is suitable for high-resolution applications [Tan et al. [2013]; Xia et al. [2012]], but it requires OTAs and repeated charging of the sensing capacitor, leading to high power consumption. This

dissertation presents the design of an incremental two-step CDC combining a coarse SAR CDC and a fine time-domain (TD) $\Delta\Sigma$ modulator implemented by a VCO-based converter. The VCO is mostly digital and consumes low power. Featuring the infinite DC gain in phase domain and intrinsic spatial phase quantization, this TD$\Delta\Sigma$M enables a CDC design achieving 85-dB SQNR by having only a 4-bit quantizer, a 1st-order loop and a low OSR of 15. The prototype fabricated in 40-nm CMOS achieves a capacitance resolution of 0.29 fF while dissipating only 0.083 nJ per conversion, which improves the energy efficiency by greater than 2 times comparing to the state-of-the-art.

In the subsequent five chapters, the details of these prototypes and their corresponding techniques will be presented and analyzed. Measurement results will also be discussed and compared to state-of-the-art statistics. Chapter 7 will conclude this dissertation.

Chapter 2

Low-Power SAR ADC with Gain-Boosted Dynamic Comparator

This chapter[1] presents an ultra-low power SAR ADC with 0.5-V supply voltage. It introduces a novel comparator topology with a dynamic common-gate stage which increases the pre-amplification gain, thereby reducing noise and offset. Statistical noise reduction technique is utilized to further reduce the noise in the converter. Loading switching technique is applied to improve the energy efficiency in the MSB comparisons. To reduce the digital power, the SAR sequencer and clock generator share only a single dynamic DFF chain. A 40-nm CMOS prototype achieves a Walden FoM of 1.5 fJ/conversion-step while operating at 100-kS/s and consuming only 69 nW under 0.5-V supply.

[1]This chapter is a partial reprint of the publication: X. Tang, L. Chen, J. Song, and N. Sun, "A 1.5fJ/Conv-step 10b 100kS/s SAR ADC with Gain-Boosted Dynamic Comparator," in *IEEE Asian Solid-State Circuits Conference (ASSCC)*, pp. 229-232. Dec. 2017. I am the main contributor in charge of circuit design, layout, and chip validations.

2.1 Introduction

Power-efficient ADCs are critical for energy-constraint applications, such as wireless sensors and biomedical implants. In these applications, low-speed and moderate-resolution ADCs are required to digitize the sensed signals. SAR ADC is preferred due to its simplicity and scaling compatibility [Liu et al. [2015b]; Tai et al. [2014]; Chen et al. [2015]; Harpe et al. [2013]; Ding et al. [2015]]. Since these sensors are often powered by batteries or energy harvesters, low power operation is critical.

The power consumption of state-of-the-art SAR ADCs is typically dominated by the comparator and digital circuits [Chen et al. [2015]; Tai et al. [2014]]. A common technique to reduce power is to operate the ADC under a low-power supply voltage (e.g., 0.5 V). A key problem for the comparator to operate under such a low voltage is the reduced front-end dynamic integrator gain, leading to increased input referred noise and offset. To boost the front-end gain, this work proposes a novel comparator topology with a dynamic common-gate stage inserted before the latch. This common-gate stage effectively increases the amplification gain so that the noise and offset are reduced but with little power cost.

To further reduce the comparator noise and power, this work synergically combines three other low-power techniques, including: 1) statistical estimation [Chen et al. [2015]], which reduces the comparator noise by estimating the ADC conversion residue from 4 repeated LSB comparisons; 2) CMOS input pair for bidirectional integration [Liu et al. [2015b]], which makes use of both

charging and discharging phases for amplification to halve the preamplifier power; and 3) load capacitance switching between MSB and LSB conversions [Ding et al. [2015]], which saves the comparator energy during MSB operations.

Moreover, to reduce the power of the digital circuits, this work uses only one shift register array for both SAR logic control and clock generation, which is different from classic designs that typically require two register arrays. All flip-flops (DFFs) are implemented with dynamic logics. Additionally, the strong-arm latch is used for data storage instead of DFFs to further reduce power.

This chapter is organized as follows. Section 2.2 describes the proposed SAR ADC architecture. Section 2.3 presents the circuit implementation. Section 2.4 shows measured results.

2.2 Proposed SAR ADC Architecture

Fig. 2.1 shows the architecture of the proposed 10-bit SAR ADC with 5 low-power techniques. This work proposes a novel 3-stage comparator with a dynamic common-gate stage. It reduces the comparator noise and offset by extending the integration time and increasing the pre-amplification gain. This is especially important under low supply voltage where the dynamic pre-amplification gain is very limited. The details are presented in Section 2.3.

The clock generator produces both the sampling clock and the data latch signal. A clock booster is used to ensure high sampling linearity under a

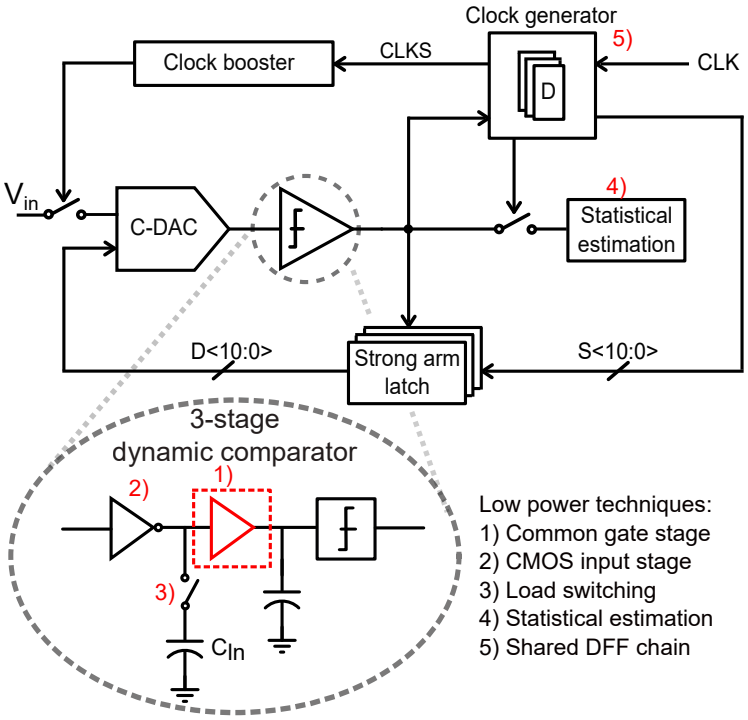


Figure 2.1: Proposed SAR ADC architecture

low supply voltage. The DACs are shown in Fig. 2.2. Custom designed 0.5-fF unit capacitor is adopted. A CMOS-input 3-stage dynamic comparator makes the decision. A Bayes estimation (BE) block performs statistical estimation based noise reduction.

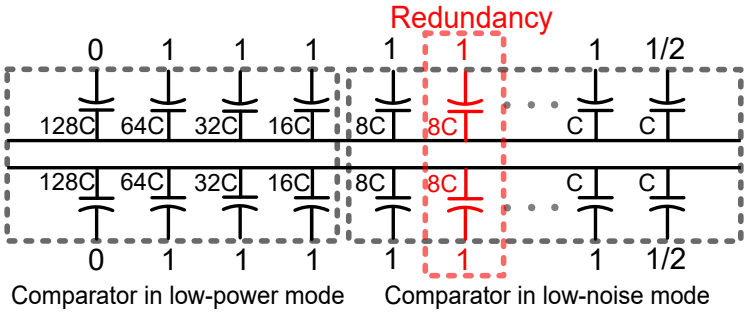


Figure 2.2: Proposed SAR ADC DAC array

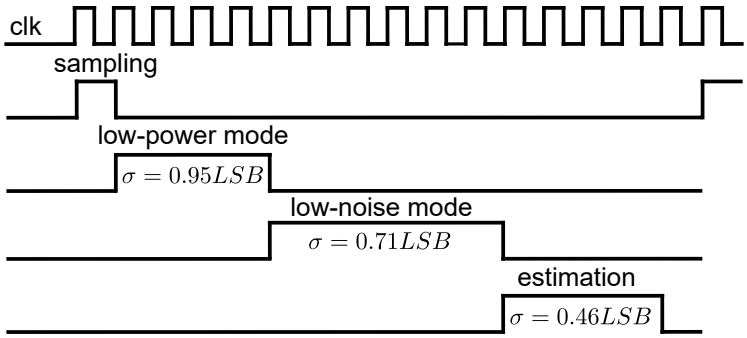


Figure 2.3: Proposed SAR ADC timing diagram

The timing diagram is shown in Fig. 2.3. In the sampling phase, the input is top-plate sampled onto the DAC. During the first 4-bit MSB conversions, the comparator operates in a low-power mode with a small load capacitor to save energy. The comparator rms noise is 0.9 LSB. The total ADC rms noise is 0.95 LSB including both comparator and quantization noise. During the next 7-bit LSB conversions including a redundant bit (8C), the comparator is configured in the low-noise mode with a large load capacitor to ensure accuracy. The comparator rms noise is reduced to 0.65 LSB, which results in the ADC rms noise reducing to 0.71 LSB. This load switching can cause comparator offset variation, but its induced error is fully absorbed by the redundancy (8C), which also absorbs any error caused by the large noise during the 4 MSB comparisons.

To further reduce noise but without a large power cost, the last LSB conversion is repeated by 4 times to perform Bayes estimation [Chen et al. [2015]], which exploits all the information embedded in the comparator outputs. The conversion residue voltage is estimated by examining the number

of '1's out of the repeated 4 comparison results, and is then subtracted out from the ADC output. This technique reduces both the comparator noise and the quantization error. The final ADC rms noise is reduced to 0.46 LSB after Bayes estimation.

2.3 Circuit Implementation

This low power SAR ADC requires judicious optimization to ensure high performance and power efficiency. Three design techniques are highlighted in this section.

2.3.1 Proposed 3-Stage Dynamic Comparator

As discussed earlier, a low power supply voltage (e.g., 0.5 V) reduces the comparator front-end dynamic integrator gain, leading to increased noise and offset. To boost the front-end gain while maintaining power efficiency, a CMOS-input 3-stage dynamic comparator is proposed. As shown in Fig. 2.4, it consists of a dynamic integrator for front-end amplification and a latch to provide positive feedback for regeneration. The integration stage includes a CMOS input pair followed by a PMOS common-gate stage.

As shown in Fig. 2.5, the integration can be divided into 3 phases. In ϕ_1, the NMOS input pair performs integration by discharging V_{xp}/V_{xn} from V_{DD}. After they drop below $V_{DD}/2$, ϕ_2 starts. The NMOS pair is disabled, and the PMOS pair integrates the input by charging V_{xp}/V_{xn} towards V_{DD}. Once V_{xp}/V_{xn} goes above the threshold voltage of the PMOS common-gate (CG)

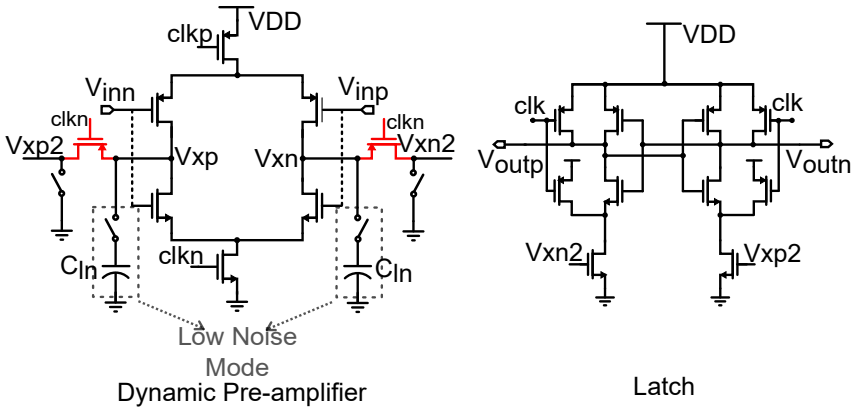


Figure 2.4: Proposed gain-boosted comparator architecture.

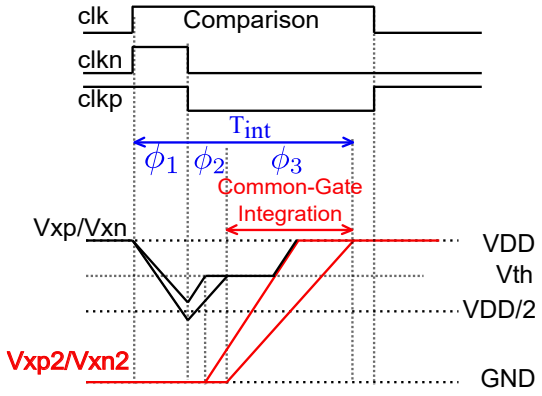


Figure 2.5: Proposed comparator operation.

transistors (marked in red), the CG integration phase ϕ_3 starts. The differential charges on V_{xp}/V_{xn} are transferred to V_{xp2}/V_{xn2}. Assuming large CG stage gain, the source nodes V_{xp}/V_{xn} are held still and the signal amplification continues on the new integration nodes V_{xp2}/V_{xn2}.

In the conventional strong-arm latch, the integrator output V_{cm} change is V_{DD}. This added CG stage extends the V_{cm} change by V_{th}, which effectively

elongates the integration time T_{int}. The total integration time becomes:

$$T_{int} \approx \frac{C}{I_D}\left(V_{DD} + V_{th}\right) \tag{2.1}$$

where I_D is the input pair current. We assume equal load C at V_{xp}/V_{xn} and V_{xp2}/V_{xn2} for simplicity. A longer T_{int} leads to a larger integration gain, which directly reduces the input-referred noise and offset from the latch. The integration gain A_{int} is given by [Razavi [2015]]:

$$A_{int} \approx \frac{g_m}{I_D}\left(V_{DD} + V_{th}\right) \tag{2.2}$$

Furthermore, the noise bandwidth of a dynamic integrator is inversely proportional to T_{int}, and thus, a longer T_{int} also reduces the noise from both the comparator input pair and the DAC. In addition to the benefits brought by the insertion of the CG stage, the use of the CMOS bidirectional integrator reduces the front-end integrator power by 2 times [Liu et al. [2015b]].

As discussed before, to further reduce the comparator power, load switching technique is employed. During MSB comparisons, the capacitor C_{ln} at integration node V_{xp}/V_{xn} is disconnected to save power. Only during the critical LSB comparisons, C_{ln} are connected to trade power for reduced comparator noise. C_{ln} is chosen to ensure that the comparator rms noise is 0.65 and 0.9 LSB with and without the loading of C_{ln}. The comparator power is 50% lower without the extra loading capacitor, and thus, load switching greatly reduces the MSB comparison power.

2.3.2 Statistical Estimation Based Noise Reduction

Statistical estimation is performed to reduce both the comparator noise and the quantization error [Chen et al. [2015]]. In a SAR ADC, the digital output can be expressed as:

$$D_{out} = V_{in} + n_s + V_{res} \tag{2.3}$$

where n_s is the sampling noise and V_{res} is the conversion residue at the comparator input. V_{res} includes the effects of both the comparator noise and the quantization error. The idea of statistical estimation based noise reduction is to form a digital estimator of V_{res}, denoted as V_{res}^*, and subtract it from D_{out} to enhance the overall ADC resolution.

The hardware cost for this statistical estimation technique is low. To obtain a target 4-dB ADC SNR improvement, we only need to repeat the ADC LSB comparisons by 4 times. We count the number of '1's from the comparator outputs and denote it as k. Depending on the value of k, we estimate the conversion residue and define V_{res}^*. Assuming the value of k is $\{0, 1, 2, 3, 4\}$, V_{res}^* is mapped to $\{-1, -0.5, 0, +0.5, +1\}$, respectively. Since only the LSB comparison is repeated by 4 times, the total comparator power is increased by only 30%. This is much more power efficient than the brute-force analog scaling, which requires 225% comparator power increase to obtain the same 4-dB ADC SNR improvement.

Comparing to the majority voting technique of [Harpe et al. [2013]], the merit of this statistical estimation technique is that *it makes full use of the*

statistical information, not just the majority information. Thus, it can provide finer steps of ±0.5 LSB, leading to a higher SNR enhancement. Simulations show that the overall SNR improvement is reduced by 2 dB if majority voting is used to determine the LSB. In addition, the proposed technique does not require an extra metastability detection circuit, which reduces the hardware complexity.

2.3.3 Low-Power SAR Logic Design

The digital circuit power can constitute a substantial portion of the overall SAR ADC power even in 40-nm CMOS. To reduce the digital power, a 0.5-V supply voltage is used. Furthermore, several design techniques are introduced. In a classic synchronous SAR logic design, a clock counter and a decoder forms a state machine triggered by the system clock *clk* to produce the sampling clock *clks* and the comparator clock *clkc*. A separate shift register array is required in the SAR logic to generate the data latch signal $S < 10 : 0 >$. By contrast, as shown in Fig. 2.6, the proposed clock generator only contains one shift register chain. It uses both system clock *clk* and comparator output ready signal. In this shift register chain, the first two DFF outputs generates sampling clock *clks* and the comparator clock *clkc*. The comparator output ready signal triggers the following DFFs in the chain, which produces the data latch signals. The last DFF's output resets the whole chain. In this way, the shift register chain serves as both the clock counter and the sequencer.

In the classic SAR, each comparison cycle triggers 1 DFF in the clock

counter, 1 DFF in the sequencer, and 1 data storage DFF. In this work, a strong-arm latch is used for data storage. The sequencer is merged with the clock generation block, as mentioned earlier. As a result, the SAR logic power is reduced by roughly 2 times: it only includes 1 DFF and 1 latch switching energy per bit. In addition, DFFs are implemented with dynamic logics to further reduce digital power.

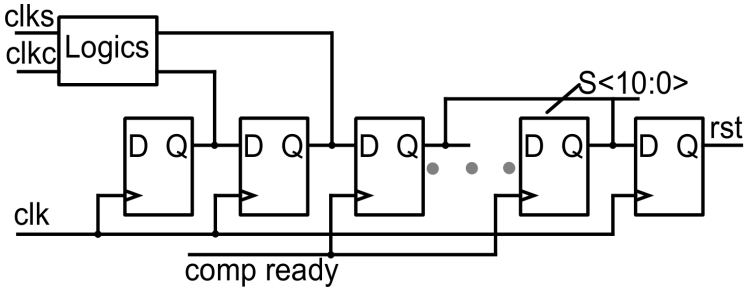


Figure 2.6: Proposed clock generator.

2.4 Measurement Results

The prototype ADC in 40-nm CMOS occupies an active area of 0.007 mm^2 as shown in Fig. 2.7. Fig. 2.8 shows the measured DNL and INL. DNL is $+1.26/-1$ LSB and INL is $+1.76/-1.15$ LSB. The DNL and INL errors are mainly caused by random mismatch among 0.5-fF unit capacitors.

The measured probability densities of D_{out} at $V_{in} = 0$ with and without Bayes estimation (BE) are shown in Fig. 2.9 together with fitted normal distributions. Before noise reduction, the standard deviation of D_{out} is 0.68 LSB, which is in agreement with SPICE simulation. After applying BE, the standard deviation of D_{out} is reduced to 0.45 LSB, which matches well with the

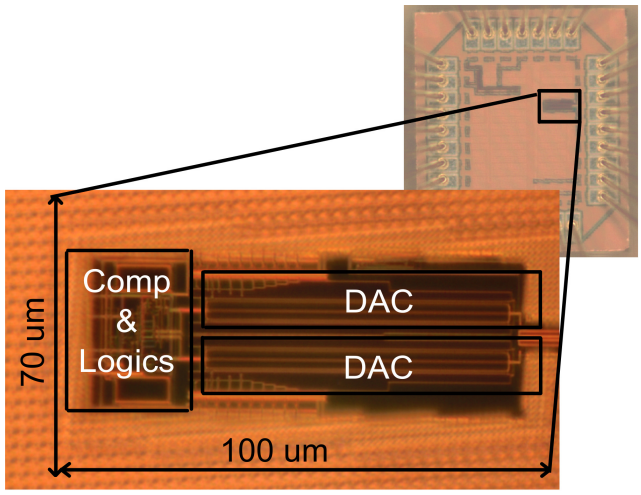


Figure 2.7: Die micrograph.

theoretical prediction. Overall, the ADC input referred noise is reduced by 3.5 dB after BE with only 30% increase in the total comparator power, which is much more efficient than brute-force analog scaling. If the conventional design approach is used, the comparator noise needs to be reduced to 0.35 LSB in order for the total ADC noise to be 0.45 LSB, which also includes the 0.29 LSB quantization noise. It would require 200% comparator power increase to get the same SNR improvement.

Fig. 2.10 shows the measured ADC output spectrum for a low frequency input and a Nyquist rate input with 100-kHz sampling rate. At low frequency input, 56.7-dB SNDR and 68.3-dB SFDR are achieved. With Nyquist rate input, 55.2-dB SNDR and 63.2-dB SFDR are achieved. Fig. 2.11 shows the SNDR with varying input amplitudes.

The ADC consumes 69 nW from a 0.5-V power supply. The power

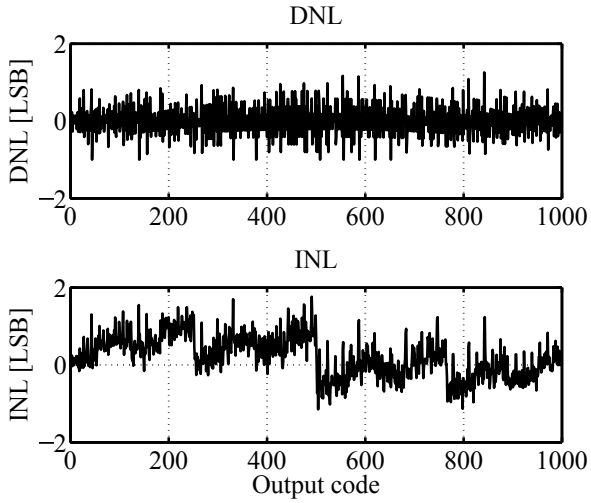


Figure 2.8: Measured DNL/INL.

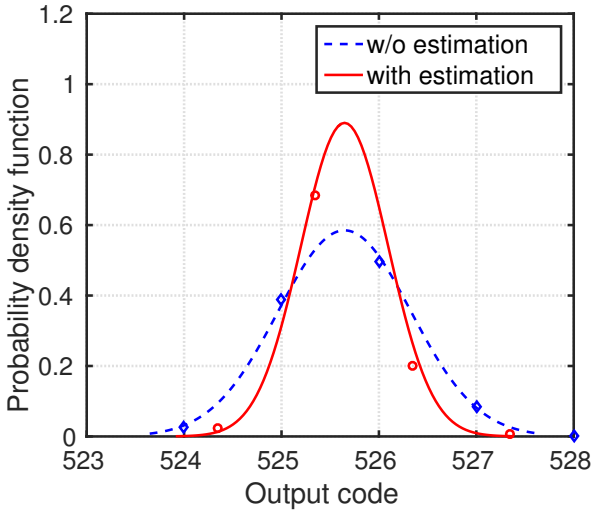


Figure 2.9: D_{out} distribution with and without estimation at $V_{in} = 0$.

breakdown is as follows: 24 nW for comparator, 36 nW for digital logics, and 9 nW for the reference. The measured Walden figure-of-merit (FOM) is 1.5 fJ/conversion-step. As shown in Table 2.1, the proposed ADC achieves the state-of-the-art performance.

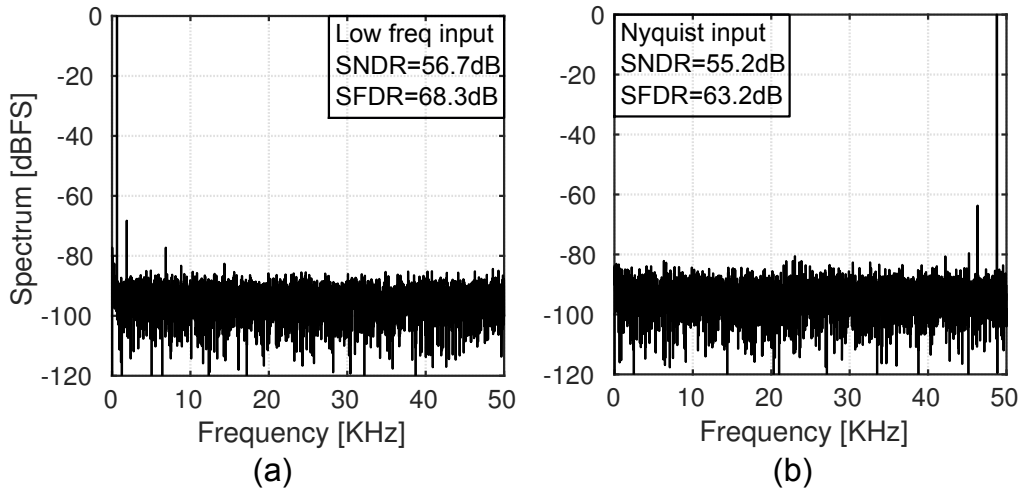


Figure 2.10: Measured FFT spectrum with low frequency input and Nyquist rate input with 100KHz sampling rate.

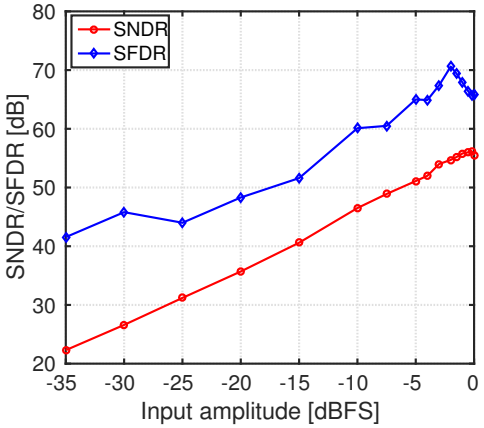


Figure 2.11: Measured SNDR versus input amplitudes.

Table 2.1: Performance Summary and Comparison with state-of-the-art low power SAR ADCs.

	[Liu et al. [2015b]]	[Tai et al. [2014]]	[Harpe et al. [2013]]	**This work**
Process [nm]	65	40	65	**40**
Supply Voltage [V]	0.6	0.45	0.8	**0.5**
Power [nW]	97	84	106	**69**
Active area [mm^2]	0.076	0.007	–	**0.007**
Sampling Rate [KS/s]	40	200	80	**100**
Resolution [bit]	12	10	10	**10**
Nyquist SNDR [dB]	62.5	55.6	56.6	**55.2**
Walden FoM [fJ/conv-step]	2.2	0.85	2.4	**1.5**

Chapter 3

Dynamic Comparator with Floating Inverter Pre-Amplifier

This chapter[1] presents an energy-efficient comparator with a novel dynamic pre-amp. By using an inverter-based input pair powered by a floating reservoir capacitor, the pre-amp realizes both current reuse and dynamic bias, thereby significantly boosting g_m/I_D and reducing noise. Moreover, it greatly reduces the influence of the input common-mode (CM) voltage on the comparator performance, including noise, offset, and delay. A prototype comparator in 180-nm achieves 46-μV input-referred noise while consuming only 1 pJ per comparison under 1.2-V supply. This represents greater than 7 times energy efficiency boost compared to a Strong-Arm (SA) latch. It achieves the highest reported energy efficiency to authors' best knowledge.

[1]This chapter is a partial reprint of the publication: Xiyuan Tang, Begum Kasap, Linxiao Shen, Xiangxing Yang, Wei Shi, and Nan Sun, "An Energy-Efficient Comparator with Dynamic Floating Inverter Pre-Amplifier," in *IEEE Symposium on VLSI Circuits (VLSI)*, pp. C140-C141, June 2019. I am the main contributor in charge of circuit design, layout, and chip validations.

3.1 Introduction

Comparator performs the core operation of an ADC. In various applications such as ubiquitous sensing and biomedical implants, a low-power and low-noise ADC is critical. As the technology scales down, the ADC power efficiency is significantly improved; especially, SAR ADCs benefit from mostly-digital architecture and achieve extremely low energy consumption [Hsieh and Hsieh [2018]; Tai et al. [2014]; Hsieh and Hsieh [2019]; Tang et al. [2017]]. Comparator becomes one of the major power contributors since it is bounded by the thermal noise limitation and does not benefit from the technology scaling. Besides the efficiency, another critical requirement raised for the comparator is the input common-mode insensitivity. In the sensor node applications, the environmental interferences may cause common-mode disturbance, thus degrading the system performance. Besides, advanced switching schemes in SAR ADCs [Liu et al. [2010a]; Sanyal and Sun [2013]; Tang et al. [2016]] also cause common-mode voltage variation, which limits the conversion linearity.

A comparator consists of a pre-amplifier followed by a latch. To save energy, dynamic comparators replaced the conventional static pre-amplifiers by dynamic ones, which remove static current. The Strong-Arm latch [Kobayashi et al. [1992]; Montanaro et al. [1996]], as shown in Fig. 3.1, is the first in the class and has been widely used over the years. The detailed operation and analysis are described in Section 3.2.1. With the embedded dynamic pre-amplifier followed by a regenerative latch, the Strong-Arm latch provides good energy-efficiency and achieves fast comparison speed, thus suiting well

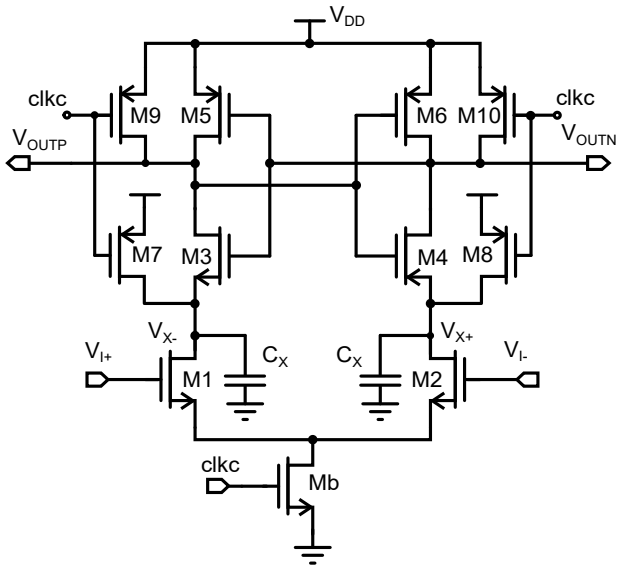


Figure 3.1: Classic Strong-Arm Latch.

for the energy-constraint applications. In a low-noise design, large integration capacitors C_X are required for good resolution. The complete discharge of C_X consumes fixed energy ($2{\cdot}C_X{\cdot}V_{DD}^2$) and limits the comparator energy-efficiency [Van Elzakker et al. [2010]; Schinkel et al. [2007]].

To prevent the full discharge of the integration capacitors, dynamically-biased integration is proposed in [Bindra et al. [2018]]. By providing a degeneration capacitor, the V_{GS} of the input pair keeps decreasing, and eventually the input pair is cut-off. It prevents fully discharging the load and boosts the g_m/I_D during the pre-amplification, thus resulting in a 3-times energy efficiency improvement. Another aspect to improve the efficiency is explored in [Liu et al. [2015b]], where the bi-directional integration realizes current reuse. However, the extra circuit cost limits the efficiency improvement to 1.5 times

compared to a Strong-Arm latch. A gain-boosted comparator is proposed in Chapter 2, where the dynamic integrator includes a CMOS input pair followed by a PMOS common-gate stage. Besides the current reuse, it further improves energy efficiency by increasing dynamic integrator gain. Yet, the efficiency is still limited by extra logics. In addition to relatively limited efficiency boost, none of the prior-arts addresses the input common-mode dependence problem.

This work presents an energy-efficient dynamic comparator with a floating inverter amplifier (FIA) based pre-amplifier. Its inverter-based input stage naturally realizes current reuse. By powering the FIA with a floating reservoir capacitor, it provides an isolated power domain and makes the amplification independent from the input common-mode voltage. The pre-amplifier output common-mode voltage is kept constant which elongates integration time and increases gain. In addition, the reservoir capacitor provides dynamic source degeneration that increases g_m/I_D and prevents full discharge of the integration capacitors. Overall, the proposed comparator achieves over 7 times energy-efficiency improvement compared to the Strong-Arm latch and provides input common-mode insensitivity.

This chapter is organized as follows. Section 3.2 reviews the conventional Strong-Arm latch and the dynamic bias technique. Section 3.3 presents the proposed FIA based pre-amplifier design. Section 3.4 describes the prototype comparator design. Section 3.5 shows the measured results.

3.2 Review of Prior-Arts

3.2.1 Strong-Arm Latch

The conventional Strong-Arm latch is shown in Fig. 3.1. The operation can be divided into two phases, the pre-amplification phase and the latch regeneration phase, with the turn-on of the PMOS cross-coupled pair separating two phases. During the pre-amplification phase, the PMOS cross-coupled pair is in cut-off, and the comparator works as a dynamic integrator. The comparator input voltage induces a differential drain current, which is integrated on the capacitors C_X and produces a differential integration voltage V_X that grows linearly with time. Once V_{X+}/V_{X-} reach $(V_{DD} - V_{THN})$, where V_{THN} is the threshold voltage of $M3/M4$, the cross-coupled NMOS pair is turned on, and the output nodes V_{OUTP}/V_{OUTN} starts to decrease. With the output nodes dropping below $(V_{DD} - V_{THP})$, where V_{THP} is the threshold voltage of $M5/M6$, the comparator enters the latch phase. The positive feedback provides the exponentially growing gain and dominates the behavior of the comparator during this phase. In a low-noise comparator design, large capacitors C_X are placed at the integration nodes, which are usually much larger than loading capacitors on the output nodes. As a result, the C_X integration process, whose simplified model is shown in Fig. 3.2(a), plays the dominant role in setting the comparator noise and power [Nuzzo et al. [2008]; Bindra et al. [2018]; Van Elzakker et al. [2010]]. The analyses [Razavi [2015]; Nuzzo et al. [2008]] show that the integration gain depends on the input transistor

g_m/I_D and the threshold voltage V_{THN}, which determines the integration time:

$$A_{int} \approx \frac{g_m}{I_D} \cdot V_{THN} \tag{3.1}$$

Computing circuit noise in the time domain is problem analogous to the Brownian motion, solvable by using stochastic differential equations (SDEs) [Øksendal [1998]; Nuzzo et al. [2008]; Sepke et al. [2008]; Bindra et al. [2018]]. Conventionally, the input transistors are biased in the strong-inversion region. The detailed analysis reveals that the input-referred comparator noise is dominated by the dynamic integrator, which is inversely-proportional to g_m/I_D and the loading capacitor C_X [Sepke et al. [2008]; Nuzzo et al. [2008]]:

$$\sigma^2_{n,int} \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{THN}C_X} \tag{3.2}$$

To reduce the thermal noise, we need a high g_m/I_D as well as a large loading capacitor C_X. The noise and offset contributed from the latch is attenuated by the integrator gain A_{int}:

$$\sigma_{n(os),in} \approx \sqrt{\sigma^2_{n(os),int} + \frac{\sigma^2_{n(os),latch}}{A^2_{int}}} \tag{3.3}$$

As can be seen, to design a low-noise comparator, it is desirable to have a large gain at the integrator output. Overall, this Strong-Arm latch saves energy by the elimination of static current and achieves high-speed thanks to the positive feedback in the latch phase. However, this conventional NMOS dynamic integrator based pre-amplifier suffers from several limitations: 1) the integration phase stops when V_{X+}/V_{X-} nodes reach $(V_{DD} - V_{THN})$, which

means that only this initial discharge of the loading capacitors contributes to the noise reduction; since C_X is usually large, it is a waste of energy to fully discharge the capacitors; 2) the integration gain is limited by bounded output common-mode drop, V_{THN}, resulting in a low dynamic integrator gain less than 10; 3) the comparator performance (e.g., noise, offset, and speed) depends strongly on the input common-mode voltage since the tail transistor works in the linear region.

3.2.2 Dynamically-Biased Integration

The dynamically-biased integration proposed in [Bindra et al. [2018]] increases the g_m/I_D of the input pair and prevents full discharge of the integration capacitors C_X, thus improving the energy efficiency. A comparison between the conventional NMOS integration model and the dynamically-biased integration model is presented in Fig. 3.2.

During the integration phase of a Strong-Arm latch, the overdrive voltage ($V_{GS} - V_{TH}$) of the input pair stays approximately constant, as shown in Fig. 3.2(c), which results in a constant g_m/I_D of 20 in this design. However, in a dynamically-biased integrator, thanks to the tail capacitor C_{TAIL}, the source voltage V_S is charged up, which results in the reduced overdrive voltage of the input pair. It brings two benefits to this pre-amplifier design. First, as the voltage V_S increases, the V_{GS} of $M1/M2$ reduces until the source voltage reaches the quenching point, $V_S = V_I - V_{TH}$, where V_{TH} is the threshold voltage of the transistors $M1/M2$. Then the input pair turns off, and the dynamic

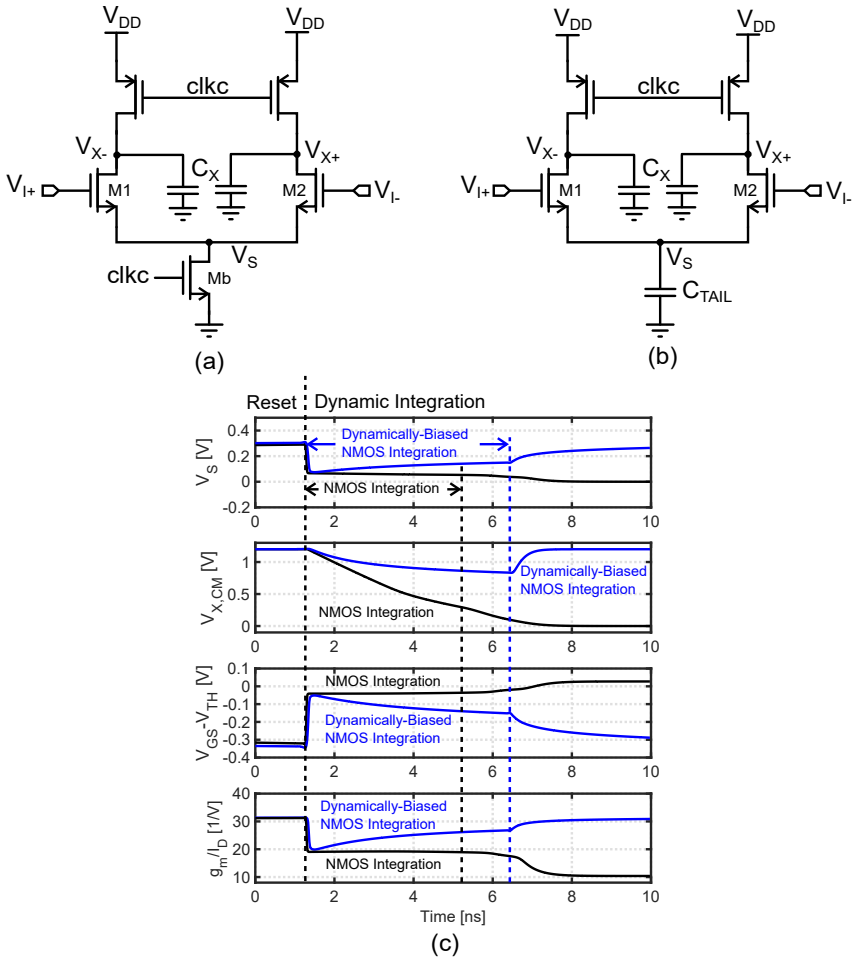


Figure 3.2: (a) Conventional NMOS integration pre-amplifier model, (b) dynamically-biased NMOS integration pre-amplifier model, and (c) simulated pre-amplifier behavior.

integration stops, which prevents the full discharge of the loading capacitors, as can been seen from the common-mode voltage behavior of the integration nodes $V_{X,CM}$. Second, a reduced overdrive voltage results in an increased g_m/I_D during the integration phase. Fig. 3.2(c) shows that the average g_m/I_D of the dynamically-biased integration is increased by 30% compared to that

of the conventional NMOS integration. The higher g_m/I_D of the pre-amplifier directly reduces input-referred noise of the dynamic integration phase, which is inversely-proportional to g_m/I_D, as shown in (3.2). It also brings higher integration gain, thus reducing the noise contribution of the latch as pointed out in (3.1) and (3.3). With the merits mentioned, the dynamically-biased integration based comparator [Bindra et al. [2018]] achieves 3 times energy efficiency improvement compared to the conventional dynamic comparator.

3.3 Proposed Floating Inverter Pre-Amplifier

3.3.1 CMOS Dynamically-Biased Integration Pre-Amplifier

To further improve the energy efficiency of the pre-amplifier, the CMOS dynamically-biased integration is proposed in this work. A differential integration model, including a CMOS input pair powered by two tail capacitors, is shown in Fig. 3.3(a). During the pre-amplification phase, the bottom source node V_{S-} increases while the the upper one V_{S+} decreases. It results in the decreased overdrive voltage ($V_{GS} - V_{TH}$) of both NMOS and PMOS input pairs. Let $G_m \equiv g_{m,n} + g_{m,p}$ represents the overall transconductance of the pre-amplifier, where $g_{m,n}$ and $g_{m,p}$ are the transconductance of NMOS and PMOS input pairs respectively. As shown in Fig. 3.3(c), at the beginning of the dynamic integration phase, the G_m/I_D of the pre-amplifier is twice of the one in Strong-Arm latch thanks to the current reuse. Throughout the integration, it keeps increasing and boosts the average G_m/I_D of the pre-amplifier by over 2.5 times, leading to a large improvement of the power efficiency.

In addition, during the pre-amplification phase, only the differential charge is integrated on the loading capacitors, and the common-mode voltage stays constant, which is 0.6 V with a 1.2-V supply. It prevents the full discharge of the C_X and removed the bounded common-mode drop limitation for the pre-amplifier gain.

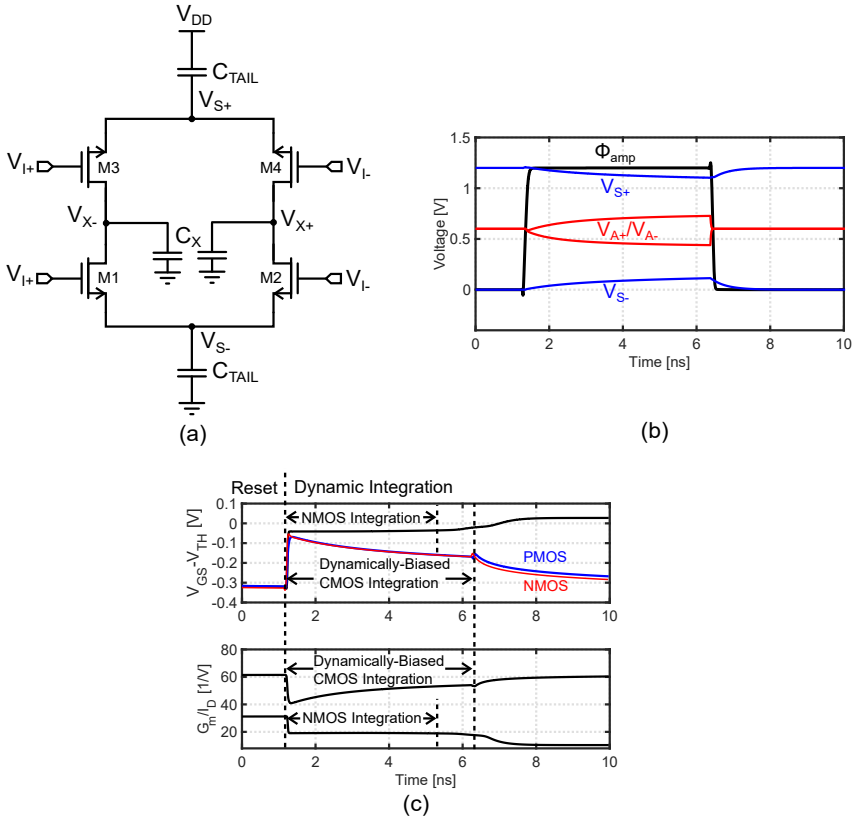


Figure 3.3: (a) Proposed CMOS dynamically-biased integration model, (b) simulated comparator behavior, and (c) comparison with Strong-Arm latch.

However, a caveat in this simple CMOS integration solution is the input common-mode and process corner sensitivity due to the lack of output common-mode feedback (CMFB). To ensure the CMOS integration function-

ality, the currents flowing through PMOS and NMOS input pairs should be equal. In the nominal corner, as shown in Fig. 3.3(b), the PMOS and NMOS transistors are well-balanced so that the current re-use is achieved and the integration performs well. However, in the extreme corners like SF, as shown in Fig. 3.4(a), where NMOS is in the slow corner while PMOS is in fast corner, the PMOS input transistor dominates the pre-amplification. The outputs are pulled to the supply resulting in the failure of the integration. Similarly, in the FS corner, the NMOS side dominates the amplifier operation and pulls the output to the ground. The failure mechanism is similar for the input common-mode voltage variations, as shown in Fig. 3.4(b). With lower input common-mode voltage, the PMOS input pair dominates the amplifier operation and vice versa. This drawback makes the simple CMOS dynamically-biased integration pre-amplifier approach infeasible.

3.3.2 Floating Inverter Pre-Amplifier with Reservoir Capacitor

To solve this problem and build a robust dynamic pre-amplifier against process corner and input common-mode variation, the FIA architecture is proposed, as shown in Fig. 3.5(a). By merging the two tail capacitors C_{TAIL} into single floating reservoir capacitor C_{RES}, it not only reduces the total capacitance size by 75% since $C_{RES} = \frac{1}{2} \cdot C_{TAIL}$, but also provides an isolated voltage domain for the pre-amplifier. A common-mode equivalent is shown in Fig. 3.5(b). Since the input and output currents from C_{RES} must be equal ($I_{AMP+} = I_{AMP-}$), the common-mode current flowing into the integration

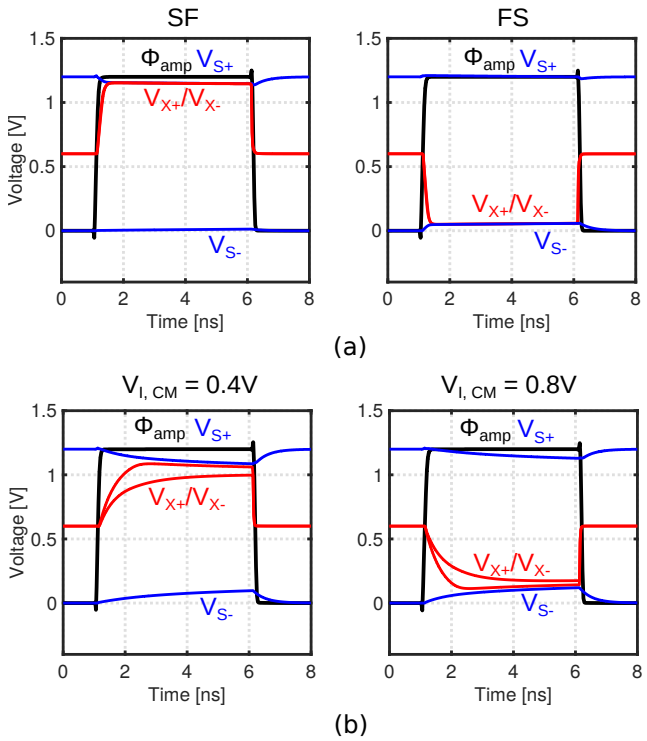


Figure 3.4: Pre-amplifier behavior simulation with (a) process corner variation and (b) input common-mode voltage variation.

capacitor $I_{X,CM}$ is forced to be 0, thus achieving a constant output common-mode voltage without a dedicated CMFB circuit [Akter et al. [2017]; Shen et al. [2019b]].

A behavioral simulation result with different process corners is shown in Fig. 3.6(a). In the fast PMOS (SF) corner, with the reduced PMOS V_{TH}, both the initial V_{S+} and V_{S-} reduced at the beginning of amplification phase. This down-shift of the isolated voltage domain results in a decreased V_{GS} for PMOS and an increased V_{GS} for NMOS, thus forcing the currents to be the same and maintaining the correct operation. In the fast NMOS (FS) corner,

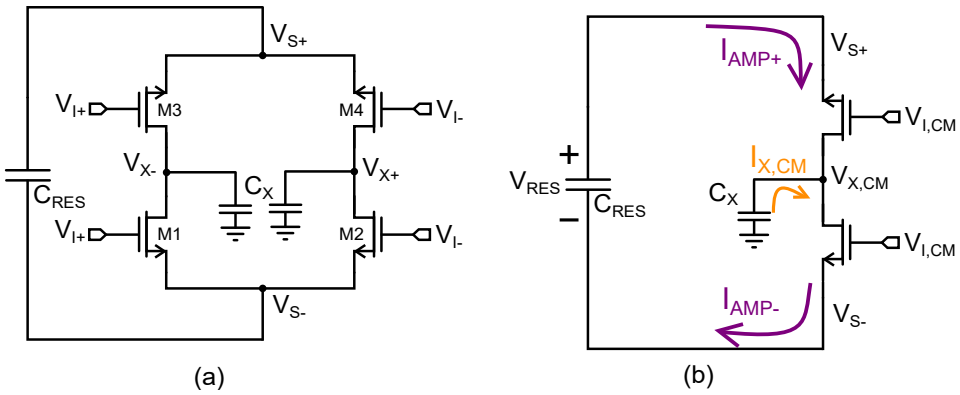


Figure 3.5: (a) Proposed FIA powered by a floating reservoir capacitor and (b) the common-mode equivalent of FIA operation.

both V_{S+} and V_{S-} are increased initially to maintain the correct integration.

The same mechanism also ensures the input common-mode insensitivity. The transistor strengths are balanced with 600-mV input common-mode voltage. If the input common-mode is decreased to 400 mV, to ensure the input/output current for C_{RES} to be the same, the isolated voltage domain will be automatically down-shifted by approximately 200 mV to balance the NMOS and PMOS overdrive voltages. Similarly, with 800-mV input common-mode voltage, the isolated voltage domain will be shifted up by about 200 mV, and as a result, the overall FIA operation is unaffected.

3.3.3 Pre-Amplifier Gain Analysis

In this design, with $V_{DD} = 1.2$ V and $V_{TH} \approx 0.55$ V in the typical corner, the input transistors $M1 - M4$ are biased in the vicinity of the weak-inversion region when the comparison starts. With the decrease of V_{GS} during

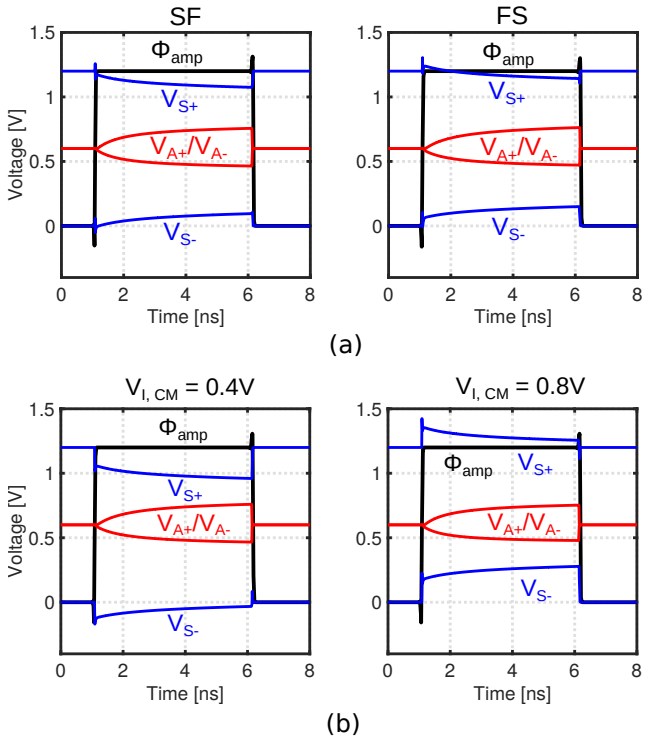


Figure 3.6: FIA behavioral simulation with (a) process corner variation and (b) input common-mode voltage variation.

the operation, the transistors are further pushed into the deep-subthreshold region. For simplicity of analysis, we assume the input transistors always work in the weak-inversion region, where the transconductance is expressed as [Razavi [2001]]:

$$g_m(t) \approx \frac{I_D(t)}{n \cdot U_T} = \frac{I_{AMP}(t)}{2 \cdot n \cdot U_T} \tag{3.4}$$

where $I_D(t)$ is the instantaneous current of the transistor, n is the weak-inversion slope factor, and U_T is the thermal voltage $= kT/q$. By ignoring the output impedance of the input transistors, the differential pre-amplifier

output voltage can be approximated as :

$$\begin{aligned}\Delta V_{X,DM}(t) &= \frac{\int_0^t \Delta V_{I,DM} \cdot G_m(\tau) d\tau}{C_X} \\ &\approx \frac{\Delta V_{I,DM} \int_0^t I_{AMP}(\tau) d\tau}{n \cdot U_T \cdot C_X}\end{aligned} \tag{3.5}$$

The tail current $I_{AMP}(t)$ can be calculated as follows:

$$I_{AMP}(t) = \frac{I_{AMP}(0^+)}{1 + \frac{I_{AMP}(0^+)}{n \cdot U_T \cdot C_{TAIL}} t} \tag{3.6}$$

where $I_{AMP}(0^+)$ is the tail current at the instant ($t = 0^+$) when the comparator starts. For a small differential input voltage, $I_D(t) \approx \frac{1}{2} I_{AMP}(t)$. The source voltage V_{S+}/V_{S-} change $\Delta V_S(t)$ can be shown as below:

$$\begin{aligned}\Delta V_S(t) &= \frac{\int_0^t I_{AMP}(\tau) d\tau}{C_{TAIL}} \\ &= n \cdot U_T \cdot \ln(1 + \frac{I_{AMP}(0^+)}{n \cdot U_T \cdot C_X} t)\end{aligned} \tag{3.7}$$

With $C_{TAIL} = 2 \cdot C_{RES}$ in the AC equivalent model, the integration gain is calculated as:

$$\begin{aligned}A_V(T_{INT}) &= \frac{\int_0^{T_{INT}} V_I \cdot G_m(\tau) d\tau}{V_I \cdot C_X} \\ &= \frac{2 \cdot C_{RES} \cdot \Delta V_S(T_{INT})}{n \cdot C_X \cdot U_T}\end{aligned} \tag{3.8}$$

In this design, C_{RES} is chosen to be 2 pF and C_X is approximated as 250 fF including the parasitics. With 1-mV differential input V_I, $\Delta V_S(T_{INT})$ is approximately 125 mV according to the simulation. The calculated $A_V(T_{INT})$ is approximately 60 while the simulated one is around 30 due to the finite output impedance of the input transistors $M1 - M4$.

3.3.4 Pre-Amplifier Noise Analysis

3.3.4.1 Conventional NMOS Integration Pre-amplifier

The noise analysis for the conventional NMOS integration pre-amplifier is presented in this part. The general expression of the dynamic integrator's output noise can be described as a convolution of the PSD $S_i(t)$ of the noise source and the magnitude squared impulse response from the noise source to the output voltage ($|h_n(t)|^2$) [Sepke et al. [2008]; Nuzzo et al. [2008]; Bindra et al. [2018]]:

$$\sigma_o^2(t) = \frac{1}{2}\int_0^t S_i(t-\tau)\cdot|h_n(\tau)|^2\,d\tau \tag{3.9}$$

where $S_i(t) = 4qI_D(t)$ is the input-referred single-side white noise PSD contributing from $M1 - M2$ biased in the weak-inversion region [Reimbold and Gentil [1982]]. Since $I_D(t)$ is relatively constant during the dynamic integration as shown in Fig. 3.2, $S_i(t)$ is independent of time. With the approximated impulse response $h_n(t) = \frac{1}{C_X}\cdot u(t)$, the mean square noise voltage at the the pre-amplifier output can be derived as:

$$\sigma_{o,SA}^2(t) = \frac{2nkT\cdot\Delta V_{X,CM}(t)}{C_X}\cdot\frac{g_m}{I_D} \tag{3.10}$$

Recall the integration gain from (3.1), the input-referred noise of the conventional NMOS integration pre-amplifier at the end of the integration phase T_{INT} can be expressed as:

$$\sigma_{in,SA}^2(T_{INT}) = \frac{2nkT}{V_{THN}\cdot C_X}\cdot\frac{I_D}{g_m} \tag{3.11}$$

3.3.4.2 Proposed FIA

In the proposed FIA design, $S_i(t) = 8qI_D(t)$ contributed from the differential CMOS input-pair $M1 - M4$. The mean square noise voltage generated across the pre-amplifier output is derived as:

$$\sigma^2_{o,FIA}(t) = \frac{4q \cdot C_{RES}}{C_X^2} \Delta V_S(t) \tag{3.12}$$

Given the voltage gain of the pre-amplifier in (3.8), the input-referred noise at the end of the integration time T_{INT} can be calculated as:

$$\sigma^2_{in,FIA}(T_{INT}) = \frac{2nkT}{C_{RES} \cdot \Delta V_S(T_{INT})} \cdot \frac{I_D}{G_m} \tag{3.13}$$

As can be seen, the input-referred noises in both conventional NMOS integration pre-amplifier and proposed FIA are inversely-proportional to G_m/I_D. In the proposed FIA, larger C_{RES} and $\Delta V_S(T_{INT})$ lead to larger integration gain, which reduces the input-referred noise.

3.3.5 Energy-Efficiency Analysis

In a low-noise comparator, the pre-amplifier dominates the power consumption as well as noise contribution, and thus the energy-efficiency of the pre-amplifier is critical. Due to the fundamental trade-off between power and thermal noise, a figure-of-merit (FoM) is defined as the product of the energy consumption and input-referred noise power:

$$FoM = Energy \cdot (NoisePower) \tag{3.14}$$

The lower the FoM, the higher energy efficiency the pre-amp achieves.

With the energy consumption per Strong-Arm latch conversion as $(2 \cdot C_X \cdot {V_{DD}}^2)$ and input-referred noise derived in (3.11), the FoM of the pre-amplifier in the classic Strong-Arm latch is:

$$FoM_{SA} = \frac{4nkT \cdot {V_{DD}}^2}{V_{THN}} \cdot \frac{I_D}{g_m} \tag{3.15}$$

The energy consumption for the FIA operation is $(2 \cdot C_{RES} \cdot \Delta V_S \cdot V_{DD})$, leading to the energy-efficiency representation as:

$$FoM_{FIA} = 4nkT \cdot V_{DD} \cdot \frac{I_D}{G_m} \tag{3.16}$$

The energy-efficiency improvement can be calculated as:

$$\frac{FoM_{SA}}{FoM_{FIA}} = \frac{V_{DD}}{V_{THN}} \cdot \frac{(G_m/I_D)_{FIA}}{(g_m/I_D)_{SA}} \tag{3.17}$$

Two major advantages of the proposed FIA are revealed in this equation. The coefficient (V_{DD}/V_{THN}) comes from the avoid of unnecessary fully-discharge of the loading capacitors in the proposed FIA operation. Besides, the energy-efficiency is proportional to G_m/I_D of the pre-amplifier, which is 2.5 times larger in the FIA as shown in Fig. 3.3(c). With $V_{DD} = 1.2$ V and $V_{TH} \approx 0.55$ V in the typical corner, this theoretical analysis predicts a greater than 5-times energy-efficiency improvement of the proposed FIA over the conventional NMOS dynamic integrator. Given the higher integration gain provided which attenuates the input-referred noise of the following latch, the proposed comparator can achieve an even larger overall energy-efficiency improvement.

3.3.6 Parasitic Capacitance Impact

When C_{RES} is a perfect capacitor without any parasitic, the FIA works in an isolated voltage domain, and thus ensures the robust integration. However, in reality, with the parasitic capacitances to the supply, it can cause a finite common-mode transfer function. To better analyze the parasitic effect on the common-mode behavior, a model is shown in Fig. 3.7. In the prototype design, C_{RES} is implemented as a symmetric MoM capacitor with equal parasitic capacitors on both plates.

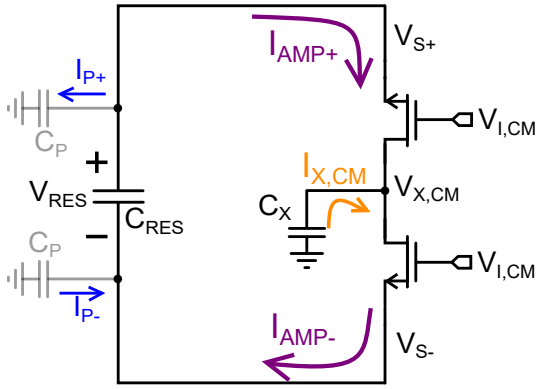


Figure 3.7: Common-mode operation model with parasitic capacitance.

The parasitic induced common-mode rejection degradation can be derived through the current equation:

$$I_{P+}(t) - I_{P-}(t) = I_{X,CM}(t) \tag{3.18}$$

It leads to a change in the output common-mode voltage:

$$\Delta V_{X,CM}(t) = -(\Delta V_{S+}(t) + \Delta V_{S-}(t)) \cdot \frac{C_P}{C_X} \tag{3.19}$$

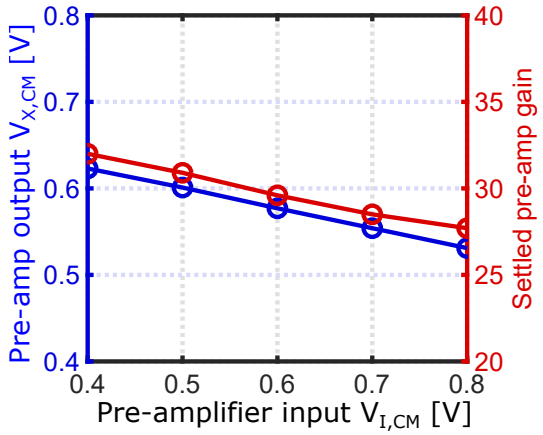


Figure 3.8: Simulated pre-amplifier output common-mode voltage and gain as a function of the input common-mode voltage.

Since the $\Delta V_{S+}/\Delta V_{S-}$ is proportional to the input common-mode voltage shift $\Delta V_{I,CM}$, the output common-mode voltage change can be estimated as:

$$\Delta V_{X,CM} \approx -2 \cdot \Delta V_{I,CM} \cdot \frac{C_P}{C_X} \tag{3.20}$$

With $C_P = 0$, there is no output common-mode voltage change as pointed out in Section 3.3.2. In this design, C_{RES} is implemented as a 2-pF MoM capacitor with the bottom layer of metal 2. The post-layout extracted parasitics including routing is 1.5%. With $C_X \approx 250$ fF including the integration node parasitics, the $\Delta V_{X,CM}$ is expected to be around 1/4 of the input common-mode voltage change. Comparing to the simple CMOS dynamically-biased integration pre-amplifier presented in Section 3.3.1, where the common-mode gain is around 20, the proposed FIA still achieves over 30-dB common-mode rejection improvement.

To verify the output common-mode behavior with the parasitic impact,

a post-layout simulation is shown in Fig. 3.8. With the input common-mode voltage varying from 0.4 to 0.8 V, the output common-mode has a variation below 100 mV, and the variation in the settled FIA gain is within 15%, which only has limited impact on the comparator performance as will be shown in the measurements.

3.4 Proposed Comparator Design

As shown in Fig. 3.9, the proposed comparator consists of an FIA stage and a standard Strong-Arm latch. During the reset phase ($clk = 0$), the reservoir capacitor C_{RES} is pre-charged to V_{DD}/G_{ND}, and the pre-amplifier output V_{X+}/V_{X-} is reset to $V_{CM} = V_{DD}/2$. When the comparison starts, the FIA performs dynamic integration ($\Phi_{amp} = 1$). Once the Strong-Arm latch resolves, the FIA is disabled to prevent the further discharge of C_{RES} to save energy ($\Phi_{amp} = 0$).

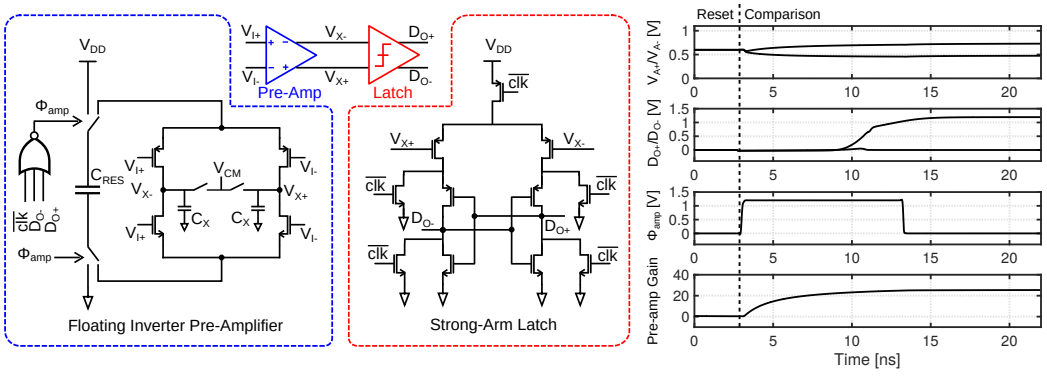


Figure 3.9: Schematic and operation of the proposed comparator with FIA.

As shown in the behavioral simulation, unlike the Strong-Arm latch, the

integration nodes V_{X+}/V_{X-} are only partially discharged, which saves considerable energy. Besides, it also removes the bounded common-mode limitation and can provide a sufficiently large gain. With a gain greater than 25, the noise contribution from the following Strong-Arm latch is negligible.

There are several considerations in choosing the value of C_{RES}. A simulated CLK-Q delay of the comparator versus C_{RES} is shown in Fig. 3.10(a), larger C_{RES} leads to faster pre-amplification which increases the comparator speed. Although the theoretical energy-efficiency (FoM) is independent of C_{RES} as indicated by (3.16), in reality, they are still correlated, as shown in Fig. 3.10(b). If C_{RES} is too small, the pre-amplification gain is not enough to suppress the latch stage noise, causing the degradation of comparator precision. While with larger C_{RES}, the dynamic bias effect is reduced, which diminishes the g_m/I_D boost. Given the area consumption, a 2-pF C_{RES} is adopted in this pre-amplifier design.

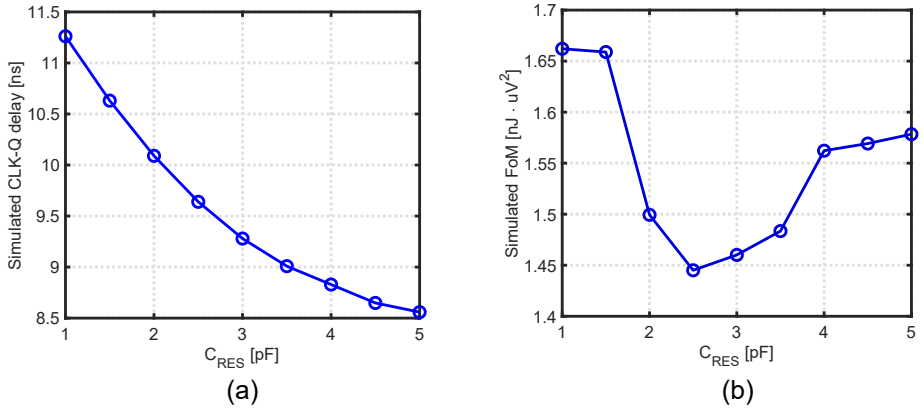


Figure 3.10: Simulated (a) CLK-Q delay with 1-mV differential input and (b) energy-efficiency of proposed comparator versus C_{RES} value.

The simulated CLK-Q delay versus the input common-mode voltage variation is shown in Fig. 3.11. With a low input common-mode, the current of Strong-Arm latch, I_D, reduces greatly, thus significantly increasing the delay of Strong-Arm latch. For instance, with the input common-mode voltage decreases from 0.6 V to 0.4 V, the simulated CLK-Q delay of Strong-Arm latch is increased by 10 times. By contrast, the proposed comparator only has a small variation of 15%, which again attests its insensitivity to the input common-mode variation.

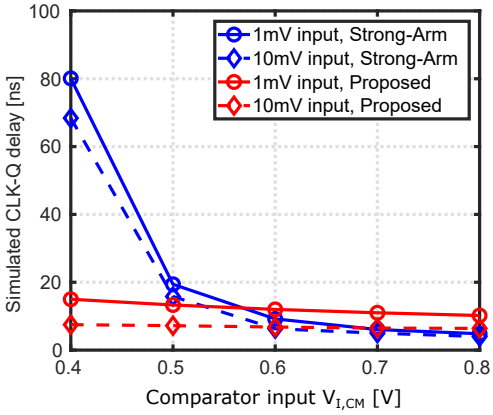


Figure 3.11: Simulated CLK-Q delay versus input common-mode voltage.

3.5 Measurement Results

The prototype is fabricated in 180-nm CMOS, as shown in Fig. 3.12. To form a better comparison, a standard Strong-Arm latch with 2-times NMOS input pair size is also fabricated, which shares the same initial G_m as the FIA. The proposed comparator occupies an area of 0.01 mm^2.

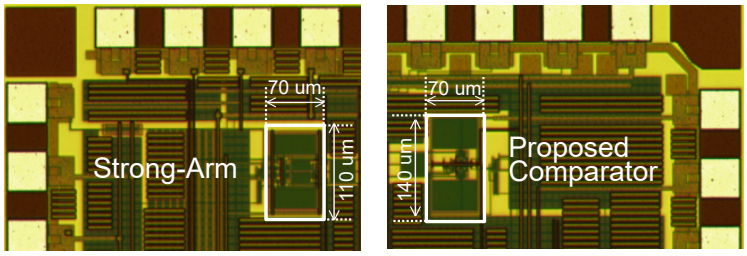


Figure 3.12: Die micrograph of the Strong-Arm latch and the proposed comparator.

To measure the input-referred noise of both comparators, a DC input voltage V_I is applied. By firing the comparator with a large number of times (e.g., 10^5), the output probability can be calculated. This process is repeated for small increments (5 μV) in V_I to measure the accurate cumulative distribution functions (CDFs), as shown in Fig. 3.13. Fitting the measurement results to a Gaussian CDF, the comparator performance can be extracted. The measured RMS input-referred noises are 62 μV for the Strong-Arm latch and 46 μV for the proposed comparator with FIA.

Fig. 3.14 shows the measured comparator noise versus input common-mode voltage. As for the Strong-Arm latch, with higher input V_{CM}, larger $(V_{GS} - V_{TH})$ results in lower g_m/I_D for the NMOS input pair. Since the input-referred noise is inversely-proportional to the g_m/I_D, as shown in (3.11), the noise is significantly larger with higher input common-mode voltage. By contrast, the input common-mode insensitive operation of FIA reduces the noise variation by 4 times. An input-referred offset measurement versus input common-mode voltage is performed in Fig. 3.15, where all parts are calibrated at 0.6-V input common-mode voltage. The Strong-Arm latch exhibits a 5.3-

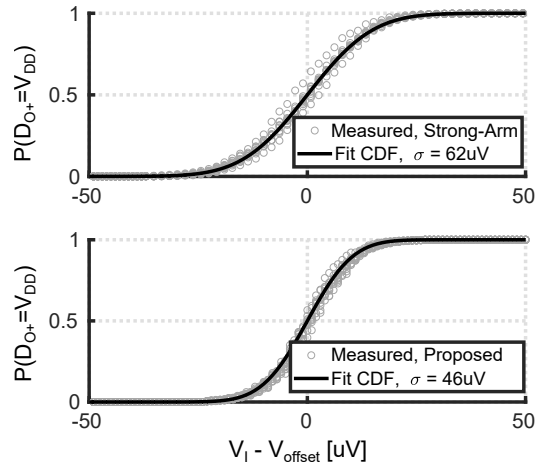


Figure 3.13: Measured cumulative probability density distribution and fit to Gaussian distribution for proposed comparator and Strong-Arm latch with 1.2-V supply and 0.6-V input common-mode voltage.

mV variation with 10 parts measured, while the proposed work reduces the variation by 4 times to 1.2-mV.

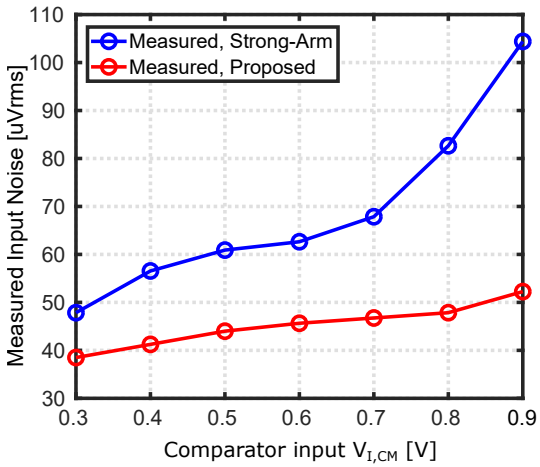


Figure 3.14: Measured input referred noise versus input common-mode voltage for the Strong-Arm latch and proposed comparator.

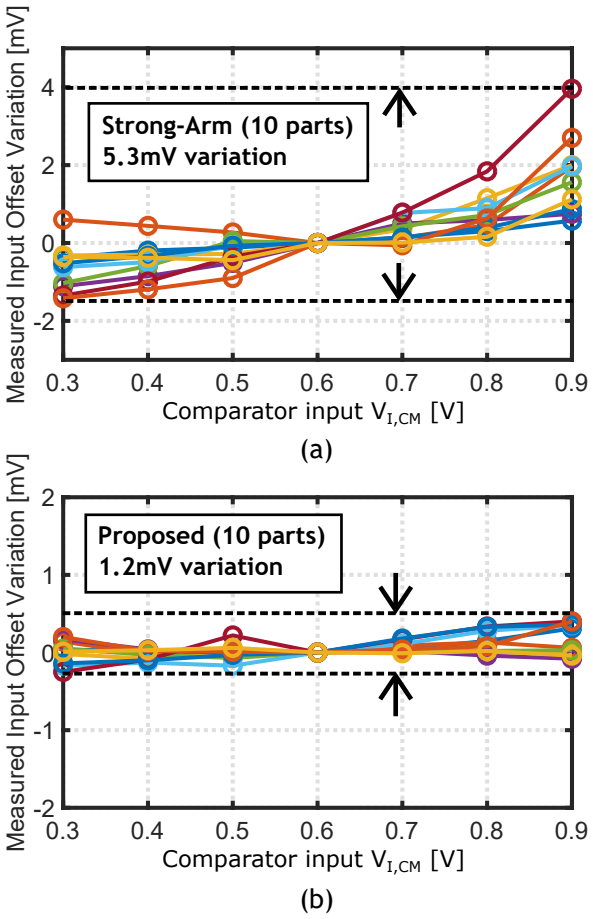


Figure 3.15: Measured 10 parts input-referred offset versus input CM voltage for (a) the Strong-Arm latch and (b) proposed comparator.

Fig. 3.16 shows the energy consumption versus input differential voltage, highlighting the reduction in overall energy consumption for various input common-mode voltages. The energy consumption per comparison for the proposed comparator is approximately 0.98 pJ per comparison, whereas it is 4.1 pJ per comparison for the Strong-Arm latch with 1-mV differential input at $V_{CM} = 0.6$ V. With the increase in the input common-mode voltage, the cur-

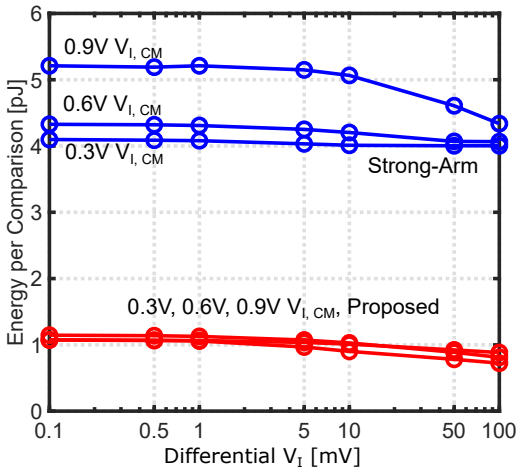


Figure 3.16: Measured energy consumption versus input voltage for the Strong-Arm latch and proposed comparator.

rent I_D in the Strong-Arm latch is raised, resulting in the increased energy consumption. Thanks to the input common-mode insensitive operation, the proposed comparator consistently achieves greater than 4 times energy reduction.

Table 3.1 summarizes the performance of the prototype design and compares it with other state-of-the-art dynamic comparators. All these comparators are operated under 1.2-V supply voltage, which forms fair comparisons of energy efficiency. The proposed comparator with FIA achieves greater than 7 times improvement over the classic Strong-Arm latch and greater than 2.5 times improvement over the 2nd best [Bindra et al. [2018]]. To authors' best knowledge, it is the most energy-efficient comparator reported to date. In addition, it has a reduced sensitivity to input common-mode voltage and process corner variation.

Table 3.1: Performance Summary and Comparison with state-of-the-art dynamic comparators.

	This Work		[Bindra et al. [2018]]		[Schinkel et al. [2007]]
Featured Architecture	**Proposed FIA+SA**	Standard SA	Dynamic Bias	Double-Tail [Van Elzakker et al. [2010]]	Double-Tail
Process [nm]	**180**	180	65	65	90
Supply [V]	**1.2**	1.2	1.2	1.2	1.2
Noise [uV]	**46**	62	400	450	1500
Energy [pJ]	**0.98**	4.1	0.034	0.088	0.113
FoM [nJ $\cdot \mu V^2$]	**2.07**	15.8	5.44	17.8	254
Insensitive to Input CM Voltage	**Yes**	No	No	No	No

Chapter 4

A Fully-Dynamic Calibration-Free High-Speed SAR ADC

This chapter[1] presents a 10-bit high-speed two-stage SAR ADC. Each bit uses a dedicated comparator to store its output and generate an asynchronous clock for the next comparison. By doing this, the SAR logic delay and power are significantly reduced. A modified bidirectional single-side switching technique is used to optimize the comparator speed and offset by controlling the input common mode voltage Vcm. To suppress the comparator offset mismatch induced non-linearity, redundancy and a shared pre-amplifier are employed in the second fine stage. The pre-amplifier is implemented using a dynamic latch to avoid static power consumption. The prototype ADC in 40-nm CMOS achieves 55-dB peak SNDR at 200-MS/s sampling rate without any calibration. It consumes 750 μW from 1.1-V power supply, leading to a Walden FOM of 8.6 fJ/conversion-step.

[1]This chapter is a partial reprint of the publication: Xiyuan Tang, Long Chen, Jeonggoo Song, and Nan Sun, "A 10-b 750uW 200MS/s Fully Dynamic Single-Channel SAR ADC in 40nm CMOS," in *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 413-416, Sept. 2016. I am the main contributor in charge of circuit design, layout, and chip validations.

4.1 Introduction

High-speed ADCs are widely used in measurement instruments, serial link transceivers, and wireless communication systems [Chen and Brodersen [2006b]; Wei et al. [2012]; Jiang et al. [2012]; Verbruggen et al. [2012]; Jeon et al. [2010]; Tripathi and Murmann [2013]; Liu et al. [2010b]]. Compared to flash and pipeline ADCs, SAR ADCs are more power efficient and scaling friendly due to their mostly digital architecture. Several high-speed SAR techniques have been proposed [Chen and Brodersen [2006b]; Wei et al. [2012]; Jiang et al. [2012]; Verbruggen et al. [2012]; Jeon et al. [2010]; Tripathi and Murmann [2013]; Liu et al. [2010b]]. Asynchronous operation is developed to reduce each conversion cycle time [Chen and Brodersen [2006b]]. Multi-bit per cycle is proposed to reduce the number of comparison cycles, however at the cost of increased hardware and design complexity [Wei et al. [2012]]. Pipelining two-stage SAR ADCs can further increase the speed, but it suffers from inter-stage gain error and consumes large static power [Jeon et al. [2010]]. Recently, the loop-unrolled architecture shows great potential for high-speed operation [Jiang et al. [2012]; Verbruggen et al. [2012]]. Its SAR logic is simple and fast. However, it cannot achieve good linearity due to offset mismatches among different comparators. To address this issue, complicated offset calibrations are required in [Verbruggen et al. [2012]; Jiang et al. [2012]].

This work proposes a calibration-free fully-dynamic SAR ADC. Loop-unrolled architecture is adopted to achieve high speed. Dedicated comparator is used for each bit to directly store the output and generate the asynchronous

clock. To solve the offset mismatch problem and achieve 10-bit resolution, the ADC is divided into two stages. The first stage is a 4-bit coarse loop-unrolled SAR ADC. The second stage is a 7-bit fine SAR ADC. A redundant bit is provided in the second stage to correct conversion errors due to comparator offset mismatches in the first stage. The second fine stage employs the same pre-amplifier for all comparators. By doing this, the input referred comparator offset is sufficiently attenuated by the pre-amp, so that the offset mismatch does not degrade the ADC linearity. The pre-amp is implemented using a dynamic latch to avoid any static power consumption. It can provide a large gain in a short amount of time due to positive feedback. In addition, a bidirectional single-side (BSS) switching technique of [Chen et al. [2014]] is applied jointly to optimize the comparator speed and offset by controlling its V_{cm}.

The proposed SAR ADC has several merits compared to prior works: 1) it is simple and fast, since the SAR logic delay is greatly reduced by using the loop unrolled architecture; 2) it is fully dynamic and can achieve high power efficiency. It does not consume any static power as in [Jeon et al. [2010]]; 3) thanks to the shared pre-amp in the second fine stage, it does not require any comparator offset calibration as in [Verbruggen et al. [2012]]; 4) it optimizes the comparator comparison speed and offset variation by controlling V_{cm} with the BSS switching technique. This is meaningful as the prior loop-unrolled architecture, such as [Verbruggen et al. [2012]], uses the monotonic switching technique which has large V_{cm} variation and offset mismatches [Chen et al. [2016b]]. A prototype ADC is implemented in 40-nm CMOS. It achieves 55-

dB peak SNDR at 200-MS/s sampling rate without any offset calibration, consuming only 750-μW power from 1.1-V power supply.

This chapter is organized as follows. Section 4.2 describes the proposed SAR ADC architecture. Section 4.3 presents the circuit implementation. Section 4.4 shows the measured results.

4.2 Proposed ADC Architecture

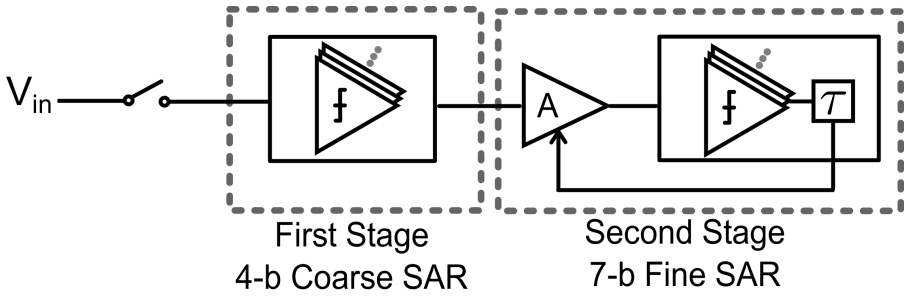


Figure 4.1: Proposed SAR ADC architecture

The architecture of the proposed two-stage SAR ADC is shown in Fig. 4.1. The detailed block diagram is shown in Fig. 4.2(a). The clock generator generates the required timing signals. The sampling switch S1 and S2 are bootstrapped to reach enough sampling accuracy at high frequency. A pair of always-off switch S3 and S4 are applied to cancel the differential mode feed-through during conversion phase. The DACs are implemented with binary weighted capacitors. 2 fF unit capacitor is adopted. A 4-bit coarse loop-unrolled SAR ADC including 4 comparators forms the first stage. The second stage is a 7-bit fine SAR ADC with a fully dynamic pre-amplifier. Dynamic logic gates with controlled delay are used to generate the asynchronous clocks.

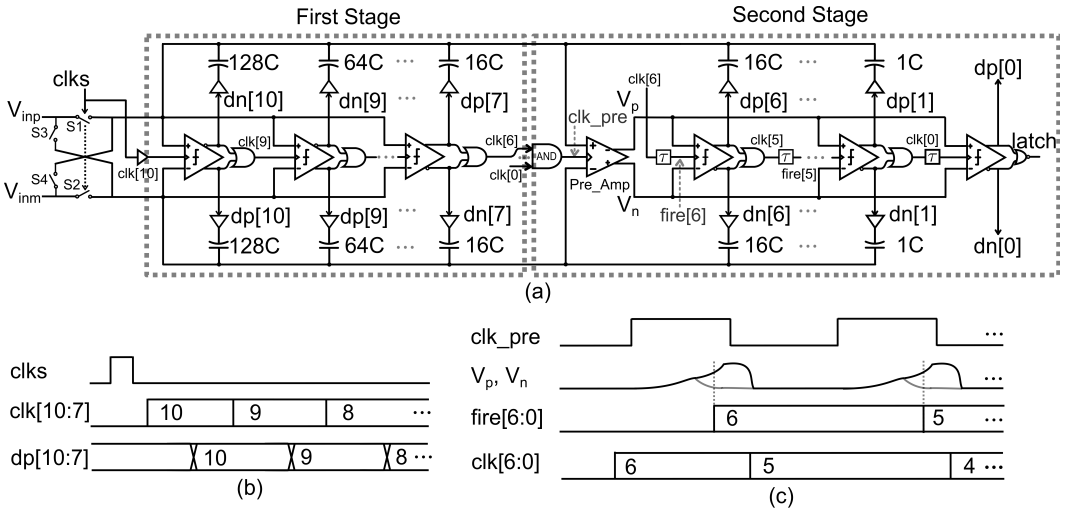


Figure 4.2: (a) Two stage architecture, (b) first stage timing diagram and (c) second stage timing diagram.

The detailed timing diagram of first stage loop-unrolled ADC is shown in Fig. 4.2(b). When *clks* is high, input signals are top-plate sampled on the capacitive DAC through bootstrapped switch S1 and S2. All comparators and internal timing control logics are reset by *clkse*. When conversion phase begins, *clk*[10] will be triggered with a delay from *clkse*. After the MSB comparison, *dp*[10] and *dn*[10] are generated and will be delivered to DAC directly. Thus, DAC begins to settle immediately after comparator resolves. *clk*[9] will also be generated after the MSB comparator resolves. After some controlled delay, the next bit comparator is fired. Due to the redundancy introduced in the second stage, there is no need to wait until the DAC fully settles. Since the first stage uses the loop-unrolled architecture, no extra logics and registers are required to generate the latch signal and store the data, resulting in greatly simplified logic and increased speed.

After the first stage finishes, *clk*[6] is triggered and delivered to the second stage, which is shown in Fig. 4.2(c). It first triggers the dynamic pre-amplifier. After certain delay for the pre-amp to generate a large enough signal at V_p and V_n, the corresponding comparator is fired by *fire*[6]. The signal *fire*[6] is generated by delaying the signal *clk*[6] by τ. The pre-amp will be reset after a carefully controlled delay in order to provide enough time for the comparator to resolve. After the comparator resolves, *clk*[5] triggers next conversion cycle. As long as we provide enough gain in the pre-amplifier, the input referred offsets in the second stage comparators are sufficiently attenuated, so that they do not degrade the ADC linearity. The first bit in the second stage ADC provides enough redundancy to recover the errors created by the first stage. After the last comparator resolves, the *latch* signal will be generated to indicate the finish of the entire conversion phase.

Compared to the conventional SAR ADC, a few advantages can help simplify SAR logic and reduce conversion time in the two-stage architecture while maintaining high power efficiency. First, thanks to the asynchronous nature, no sequencer is required in this ADC [Chen and Brodersen [2006b]]. The asynchronous clock can be easily generated by delay-controlled dynamic gate after the comparator. It also cuts unnecessary conversion time compared to a synchronous logic. Second, as dedicated comparators are used in each bit operation, separate storage registers are not needed. Comparator output controls DAC directly. It also moves the data storage time out of critical path, which further increases speed with almost no power penalty. Third, a

special designed bidirectional single-side switching technique (see Section 4.3) is applied to control the V_{cm} variation to maintain a good trade-off between comparator speed and accuracy. Fourth, comparators in first stage are triggered in a domino fashion. They will only be reset when conversion finishes. With this configuration, the comparator reset time is also removed from critical path. The optimized critical path expression for each comparison cycle in the first coarse stage can be represented as:

$$T_{coarse} = t_{comp} + \max\{t_{DAC}, t_{logic}\} \tag{4.1}$$

t_{comp} is optimized by the BSS switching scheme that we use. t_{DAC} is reduced by using a small DAC unit capacitor of 2 fF. Also, with the added redundancy, the DAC does not need to fully settle. t_{logic} is minimized by using the dynamic logic. All of these design features benefit both speed and power efficiency.

In the second stage operation, the DAC outputs are amplified by t_{preamp} before the comparison starts. In this case, comparators resolve very fast. As a result, there is no need to wait for the comparison finish signal before we reset the pre-amp. Therefore, t_{comp} and t_{DAC} overlap during the pre-amp reset phase. The optimized critical path delay for each comparison cycle in second fine stage is:

$$T_{fine} = t_{preamp} + \max\{t_{comp} + t_{DAC}, t_{reset}\} \tag{4.2}$$

4.3 Circuit Implementation

This two-stage SAR ADC design requires judicious optimization to ensure high speed and power efficiency. Two novel design techniques are highlighted in this section.

4.3.1 Modified bidirectional single-side switching technique

A modified bidirectional single-side switching scheme based on [Chen et al. [2014]] is applied in this design. This technique reduces the number of unit capacitors by 4 times compared to conventional SAR switching technique and 2 times compared to the monotonic switching technique [Verbruggen et al. [2012]]. Also, V_{cm} variation induced dynamic comparator offset is greatly reduced in this switching scheme. The chosen V_{cm} pattern is also a good trade-off between comparison speed and offset variation [Chen et al. [2016b]]. Fig. 4.3 shows the proposed DAC configuration during sampling phase. The DAC array associated with first-stage ADC includes [128C, 64C, 32C, 16C]. The second stage includes [16C, 8C, 4C, 2C, C, C]. The unit cap is 2 fF. During the sampling phase, the first two MSB capacitors are connected to ground. The last capacitor is connected to $V_{dd}/2$. All other capacitors are connected to V_{dd}. During the conversion phase, in first two MSB comparison cycles, one side will move from ground to V_{dd}, which leads V_{cm} moving from $0.5V_{dd}$ to $0.75V_{dd}$, then to $0.875V_{dd}$. After that, during each conversion cycle, one side of the DAC will switch from V_{dd} to ground, which lowers V_{cm} eventually to $0.75V_{dd}$. In this way, dynamic comparator offsets will not degrade linearity performance since

V_{cm} variation is reduced. Moreover, thanks to this V_{cm} range, the comparator has short decision time.

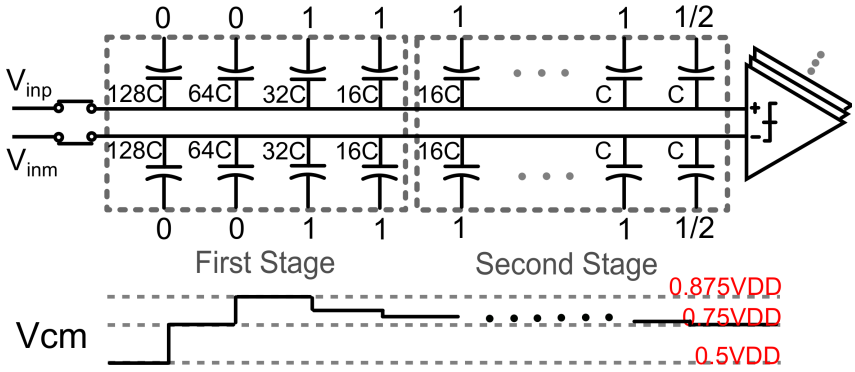


Figure 4.3: DAC configuration during the sampling phase.

4.3.2 Latch-based Dynamic Pre-amplifier

Fig. 4.4 shows a carefully designed strong-arm latch operating as the dynamic pre-amplifier in second stage fine ADC. This amplification includes two phases. First, input pair M1 and M2 begin to discharge integration node V_{x1} and V_{x2}. When V_{x1} and V_{x2} voltages are low enough to turn on M3 and M4, regeneration phase occurs. Due to the cross-coupled inverter, positive feedback provides large gain in a very short amount of time. V_{o1} and V_{o2} begin to regenerate very quickly. The output stage, M11∼M14, is highly skewed in order to make it working as an inverting amplifier when V_{o1} and V_{o2} are in the regeneration phase. In this case, after the triggering of the pre-amplifier, a large gain can be obtained at V_{outp} and V_{outn} with a very short delay. The simulated gain with 1 LSB input is shown in the figure. Then the small comparators in second stage is triggered to make the final decision. Because

V_{outp} and V_{outn} are growing exponentially, the following comparators will make the decision very quickly. Thus, the pre-amplifier can be reset immediately after the comparator is triggered. There is no need to wait for the comparator to resolve.

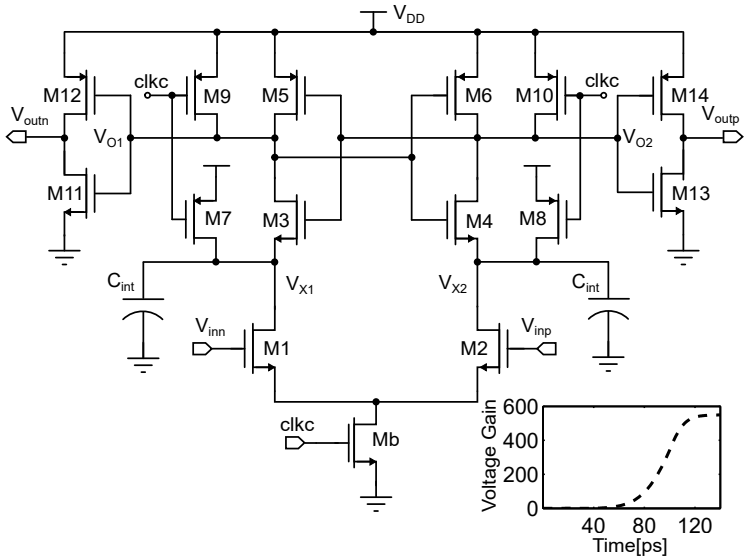


Figure 4.4: Schematic of the dynamic pre-amplifier.

4.4 Measurement Results

The prototype ADC in 40-nm CMOS occupies an active area of 0.023 mm^2, as shown in Fig. 4.5. In this design, comparators and corresponding SAR logic is placed between two capacitive DACs. This optimized routing benefits both speed and power consumption. The ADC output is decimated by 16 using 4 divide-by-2 flip-flops to simplify the measurement.

Fig. 4.6 shows the measured DNL and INL. DNL is $+1.13/-0.92$ LSB and INL is $+0.91/-0.96$ LSB. There exists a 1-LSB systematic mismatch be-

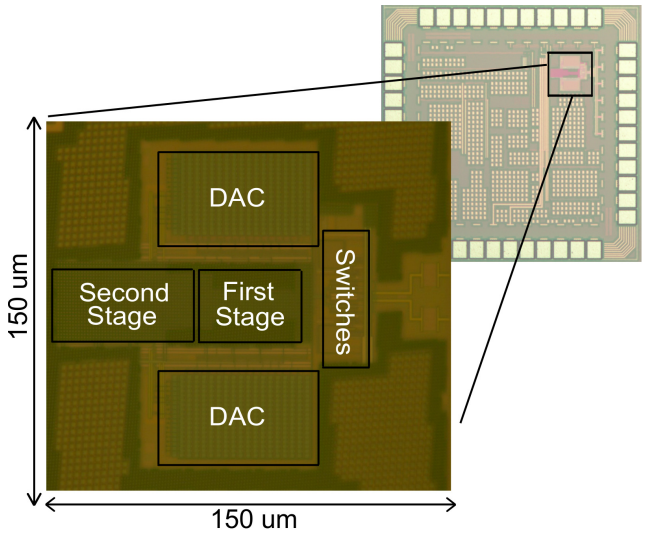


Figure 4.5: Die micrograph.

tween MSB and LSB capacitors, caused by the unmatched surrounding environment due to the segmented layout strategy and inaccurate parasitic extraction [Chen et al. [2014]].

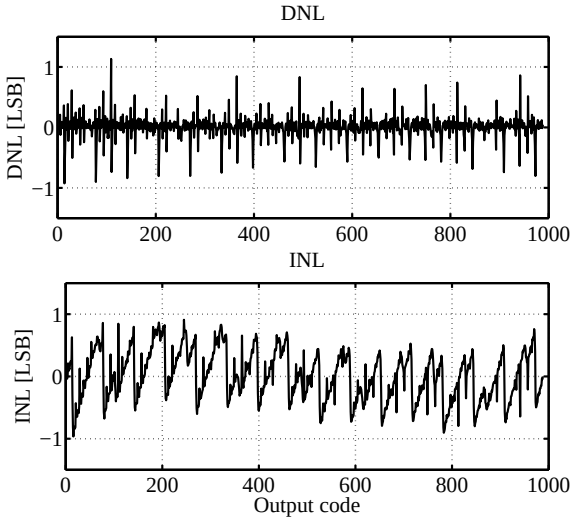


Figure 4.6: Measured DNL/INL.

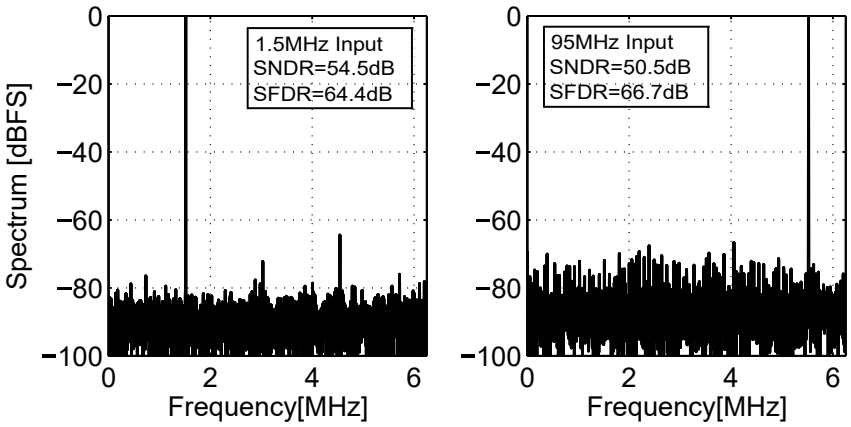


Figure 4.7: Measured FFT spectrum with 1.5-MHz input, 95-MHz input with 200-MHz sampling rate (output decimated by 16).

Fig. 4.7 shows the measured ADC output spectrum for a 1.5-MHz input and a 95-MHz input with 200-MHz sampling rate. At low input frequency, 54.5-dB SNDR and 64.4-dB SFDR are achieved. With Nyquist rate input, 50.5-dB SNDR and 66.7-dB SFDR are achieved. This degradation with a high frequency input mainly comes from the unsettled reference line bouncing. Fig. 4.8 shows the SNDR with varying input amplitudes.

The ADC consumes 750 μW from a 1.1-V power supply. The power breakdown is as follows: 320 μW for sampling and comparators, 280 μW for digital logics, and 150 μW for the reference. The measured Walden figure-of-merit (FoM) is 8.6 fJ/conversion-step. As shown in Table 4.1, the performance of the proposed ADC is comparable to other state-of-the-art works.

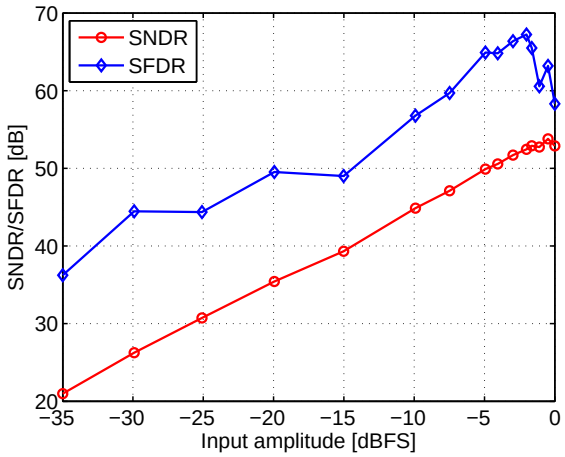


Figure 4.8: Measured SNR versus input amplitudes.

Table 4.1: Performance Summary and Comparison with state-of-the-art high speed single-channel SAR ADCs.

	[Wei et al. [2012]]	[Verbruggen et al. [2012]]	[Jeon et al. [2010]]	[Liu et al. [2010b]]	**This work**
Architecture	SAR	pipeline SAR	pipeline SAR	SAR	**SAR**
Process [nm]	65	40	65	65	**40**
Supply Voltage [V]	1	1.1	1.0	1.2	**1.1**
Sampling Rate [MS/s]	250	250	204	100	**200**
Resolution [bit]	8	11	10	10	**10**
Peak SNDR [dB]	46.7	58.7	55.2	59	**54.5**
FOM [fJ/conv-step]	42	9.7	95.4	15.5	**8.6**

Chapter 5

High-Speed SAR ADC with Reference Ripple Cancellation

This chapter[1] presents a reference ripple cancellation technique for high-speed SAR ADCs to address the reference voltage settling issue. Unlike prior techniques that aim to minimize the reference ripple, this work proposes a new perspective: it provides an extra path for the full-sized reference ripple to couple to the comparator but with an opposite polarity, so that the effect of the reference ripple is canceled out, thus ensuring an accurate conversion result. To verify the proposed technique, a prototype 10-bit 120-MS/s SAR ADC is fabricated in 40-nm CMOS process. The proposed ripple cancellation technique improves the SNDR by 8 dB and reduces the worst-case INL/DNL by 10 times. Overall, the ADC achieves an SNDR of 55 dB with only 3 pF reference decoupling capacitor.

[1]This chapter is a partial reprint of the publication: Xiyuan Tang, Yi Shen, Linxiao Shen, Wenda Zhao, Zhangming Zhu, Visvesh Sathe and Nan Sun, "A 10b 120MS/s SAR ADC with Reference Ripple Cancellation Technique," in *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, Apr. 2019. I am the main contributor in charge of circuit design, layout, and chip validations.

5.1 Introduction

Successive approximation register (SAR) ADCs are becoming increasingly popular due to their scaling friendliness, which makes them highly power and area efficient in advanced CMOS process. Nowadays, with technology scaling down, SAR ADCs can operate beyond 100-MS/s while requiring low power and small area [Tseng et al. [2016]; Tang et al. [2016]]. For SAR ADCs, a critical challenge for simultaneously achieving high speed and high resolution is the reference settling problem caused by DAC switching. For a SAR ADC without an on-chip reference buffer, the reference ripple is typically dominated by the package bond-wire LC resonance [Kapusta et al. [2013]; Chen et al. [2018]], which can lead to large conversion errors if left unaddressed.

There are two common ways to address this reference ripple problem. One way is to add an on-chip reference buffer as shown in Fig. 5.1(a). In this case, the ripple shows up as a sudden droop at the DAC switching moment. A wide-band reference buffer can ensure the droop is fully recovered before the next comparison. However, it consumes large power (e.g., 4 times larger than the ADC core as in [Liu et al. [2016]])]. The other approach is to place a large decoupling capacitor on the reference line to suppress the ripple amplitude to be well within 0.5 LSB, as shown in Fig. 5.1(b). Although this scheme does not consume additional power, it costs considerable area (e.g., 200 times bigger decoupling capacitor than the CDAC in [Venca et al. [2016]]).

Recently, to minimize the power and area cost, researchers have explored other directions to address the reference ripple problem. Since the

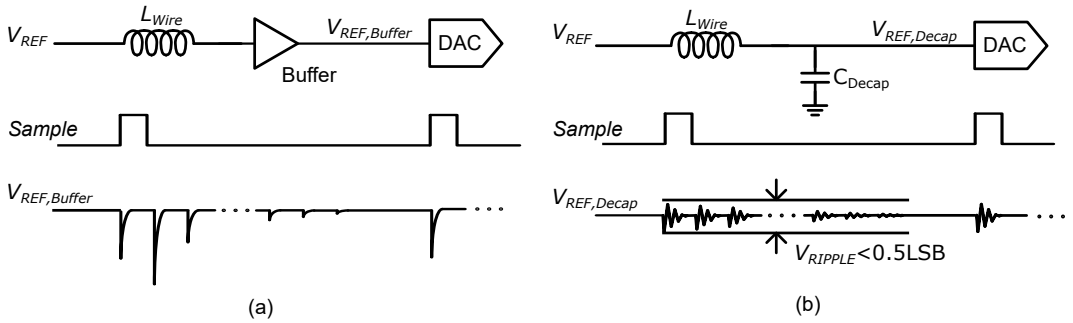


Figure 5.1: Reference voltage stabilized by (a) wide-band buffer and (b) large on-chip decoupling capacitor.

ripple amplitude is proportional to the DAC switching energy, one method is to use low-energy DAC switching techniques [Liu et al. [2010a]; Chen et al. [2014]; Hsieh and Hsieh [2018]]. Another widely adopted approach is to embed redundancy either inside the DAC [Liu et al. [2015a, 2010b]] or at the comparator [Chan et al. [2017]] to tolerate conversion errors due to large reference ripples during MSB transitions. Despite its effectiveness, this method increases the number of comparison cycles, and thus, slows down the ADC speed. In addition, it cannot tolerate any reference error after the last redundant bit. It requires the reference voltage to be completely clean during the LSB comparisons. An alternative approach is to use a pre-charged reservoir capacitor to supply the DAC switching energy [Martens et al. [2018]; Shen et al. [2018]; Kapusta et al. [2013]; Liu et al. [2019]; Chen et al. [2018]]. It isolates the DAC from the external reference, and thus, prevents the ripple generation. Nevertheless, the reservoir capacitor still has to be much larger (e.g., 80 times in [Kapusta et al. [2013]]) than the DAC to avoid significant voltage drop. Moreover, because the DAC takes nonlinear and signal depen-

dent charge, careful calibration is required to ensure high resolution and PVT robustness, leading to increased design complexity [Martens et al. [2018]; Shen et al. [2018]; Kapusta et al. [2013]; Chen et al. [2018]]. Recently, an auxiliary DAC is introduced in [Liu et al. [2019]] to compensate the signal-dependent non-binary DAC switching steps, but it still requires a reservoir capacitor that is 20 times larger than the DAC. Yet another approach proposed in [Lin et al. [2016]] is to use a switched capacitor (SC) circuit to neutralize the charge that the DAC takes in, and thus, relax the reference buffer requirement. However, it needs good matching between the DAC and the SC circuit. Also, it requires the supply voltage of the SC circuit to be clean, which is nontrivial to guarantee.

This chapter offers a new perspective to address the reference ripple problem. Different from prior techniques that focus on directly minimizing the ripple and preventing it from showing up at the comparator input, this work lets the full-sized ripple to reach the comparator input. To prevent the ripple from corrupting the comparator decision, it introduces an extra path for the ripple to reach the comparator input but with an opposite sign by inverting the polarity in a multi-input comparator, so that the effect of the ripple is canceled. The proposed technique can tolerate reference errors due to not only DAC switching but also other undesired interference, such as coupling from substrate or adjacent signal/clock wires. In addition, comparing to redundancy based techniques [Liu et al. [2015a, 2010b]; Chan et al. [2017]], it provides continued protection against the reference error after the last re-

dundant bit. Comparing to reservoir based techniques [Martens et al. [2018]; Shen et al. [2018]; Kapusta et al. [2013]; Liu et al. [2019]; Chen et al. [2018]], it does not require a large reservoir capacitor or calibration. To verify the proposed technique, a prototype 10-bit 120-MS/s SAR ADC is fabricated in 40-nm CMOS process. Measurement results show that the proposed ripple cancellation technique improves the SNDR by 8 dB and reduces the worst-case INL/DNL by 10 times. Overall, the prototype ADC achieves an SNDR of 55 dB with only 3 pF reference decoupling capacitor and without any on-chip reference buffer.

5.2 Proposed Reference Ripple Cancellation Technique

5.2.1 Basic Concept of Reference Ripple Cancellation

Fig. 5.2(a) shows the conceptual block diagram of a SAR ADC with the proposed reference ripple cancellation technique. In this simplified model, we focus only on the effect of the reference ripple, and ignore other non-idealities, such as the input sampling error, noise, comparator offset, DAC mismatch and incomplete settling. V_{DAC0} represents the ideal DAC output voltage in the absence of any reference ripple. V_{DAC0} is a direct mapping of the instantaneous conversion result D_{OUT} and gradually approaches V_{IN} during the SAR conversion process. In reality, the reference voltage V_{REF} is not completely clean, and can be represented as:

$$V_{REF} = V_{REF0} + V_{RPL} \tag{5.1}$$

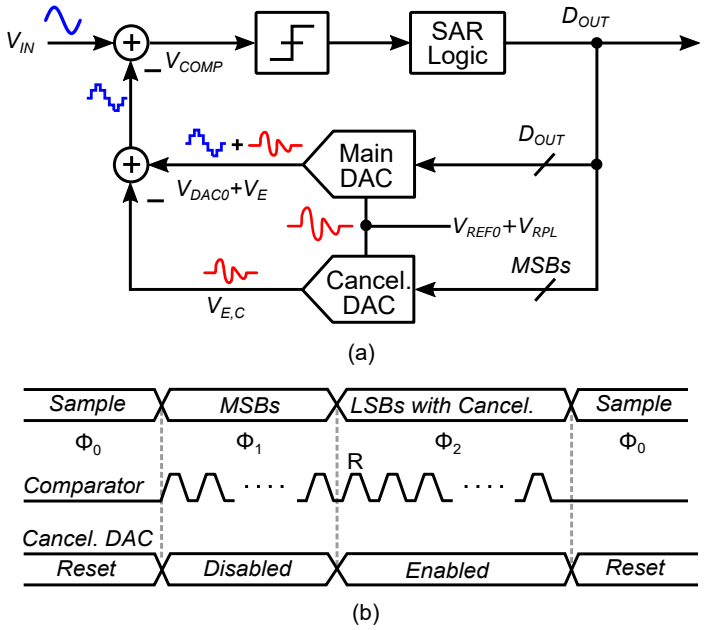


Figure 5.2: Proposed reference ripple cancellation technique and timing diagram.

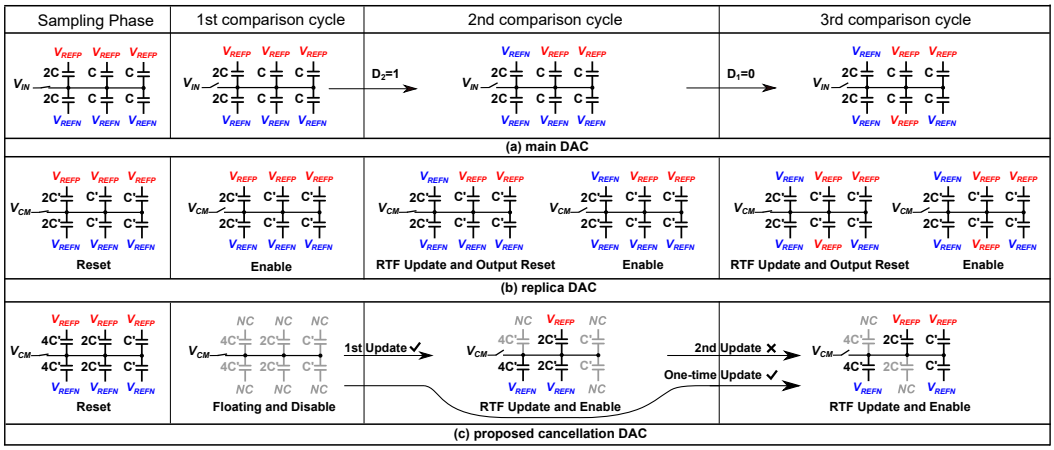


Figure 5.3: Example operations of (a) main DAC (b) replica DAC and (c) proposed cancellation DAC.

where V_{REF0} represents the ideal differential reference voltage, and V_{RPL} is the transient differential ripple. Due to the presence of V_{RPL}, the DAC output

carries an error term V_E. Their relationship can be captured in a ripple transfer function (RTF):

$$RTF(k) \equiv \frac{V_E(k)}{V_{RPL}(k)} = \frac{\sum_{i=1}^{k-1} C_{N-i} \times D_{N-i}}{\sum_{i=1}^{N} C_{N-i}} \tag{5.2}$$

where N is the total number of DAC capacitors, C_{N-i} is the DAC capacitor size (C_{N-1} is the MSB capacitor and C_0 is the LSB capacitor), and D_{N-i} is the i-th comparator decision result (it takes the value of ± 1 instead of 1 and 0). As shown in (5.2), $RTF(k)$ is not fixed, but depends on the capacitor size and prior $(k-1)$ comparator decision results.

V_E can cause a wrong comparator decision. To address this issue, this work uses a cancellation DAC to provide an extra path for the reference ripple V_{RPL} to show up at the comparator input but with an opposite polarity, so that the effect of the ripple is canceled out. With the cancellation DAC enabled, the effective differential voltage at the comparator input can be expressed as:

$$\begin{aligned} V_{COMP} &= V_{IN} - (V_{DAC0} + V_E) + V_{E,C} \\ &= V_{COMP0} - (RTF - RTF_C)\, V_{RPL} \end{aligned} \tag{5.3}$$

where V_{COMP0} is the ideal comparator input, and RTF_C is the RTF of the cancellation DAC. To eliminate the effect of V_{RPL}, $RTF_C(k)$ needs to match $RTF(k)$. Since $RTF(k)$ depends on prior bit-decision results as shown in (5.2), the cancellation DAC also needs the bit-decision information. Nevertheless, unlike the main DAC, the cancellation DAC should only produce the ripple, but not the signal component (i.e., V_{DAC0}) in order not to cause any

signal attenuation. In other words, although the bit decisions are sent to the cancellation DAC as input, they are not used to generate a proportional output; instead, they are used solely to guide the cancellation DAC to emulate the RTF of the main DAC.

Based on (5.2), $RTF(k)$ is primarily set by the MSB bits. The influence of the LSB bit decisions is small due to smaller capacitor weights. Hence, the variation of $RTF(k)$ during the LSB decisions is small and can be ignored. To simplify the implementation of the cancellation DAC, it only needs to take in the MSB decisions to update $RTF_C(k)$. This is sufficient to cancel out the majority of the ripples.

The timing diagram of the SAR ADC with the proposed ripple cancellation technique is illustrated in Fig. 5.2(b). During Φ_0, the main DAC is sampling the input signal while the cancellation DAC is reset. During Φ_1, the SAR performs the normal MSB decisions. At the beginning of Φ_2, a redundant bit is added to absorb MSB decision errors. During Φ_2, the cancellation DAC is enabled and uses the MSB decision results to emulate the main DAC RTF. This way, it ensures the majority of the reference ripples are canceled during the critical LSB comparisons, leading to an overall correct conversion result.

The proposed technique does not assume any prior knowledge of the shape or magnitude of V_{RPL}. This implies that it can tolerate reference voltage errors due to not only DAC switching, but also other unwanted couplings from power supply, substrate, or adjacent clock/signal wires.

5.2.2 Implementation of Cancellation DAC

The implementation of the cancellation DAC is at the heart of the proposed reference ripple cancellation technique. As shown in Fig. 5.2, it needs to pass the same amount of ripple as the main DAC by matching the RTF, but block any signal component from going through. Before presenting its design, let us take a look at how the main DAC configuration evolves using a 3-bit SAR ADC example shown in Fig. 5.3(a). For simplicity of illustration, only a single-ended DAC is shown but the implementation is assumed to be fully differential. Here, the DAC adopts the split capacitor switching scheme [Ginsburg and Chandrakasan [2007]] to minimize the switching energy and keep a constant output common-mode voltage. $V_{REF,P}$ and $V_{REF,N}$ represent the positive and negative DAC reference voltages, where $V_{REF,P} - V_{REF,N} = V_{REF}$. They carry ripples $V_{RPL,P}$ and $V_{RPL,N}$, respectively, where $V_{RPL,P} - V_{RPL,N} = V_{RPL}$. Fig. 5.3(a) clearly shows that the RTF depends on the bit decision and changes for every comparison cycle. For example, with the 1st MSB bit decision $D_2 = 1$, the individual RTFs for $V_{RPL,P}$ and $V_{RPL,N}$ are 1/4 and 3/4 respectively during the 2nd comparator decision. This corresponds to a differential $RTF(1) = 1/2$. With the 2nd bit decision $D_1 = 0$, the individual RTFs for $V_{RPL,P}$ and $V_{RPL,N}$ are updated to 3/8 and 5/8 during the 3rd comparator decision, leading to the differential $RTF(2) = 1/4$.

5.2.2.1 Replica DAC Implementation

To match the main DAC RTF, a straightforward idea to build the cancellation DAC is to replicate the main DAC, as shown in Fig. 5.3(b). However, just copying the main DAC and its operation means the signal component (i.e., V_{DAC0}) would also be produced at the cancellation DAC output, causing unwanted signal cancellation. To address this issue, the cancellation DAC output can be reset to V_{CM} after every DAC switching, as shown in Fig. 5.3(b). However, this method requires V_{REFP} and V_{REFN} to be accurate during this intermediate reset operation, which contradicts with the initial problem definition that reference voltages are not clean during the ADC conversion process. In the presence of reference ripples, the inaccurate reset operation introduces an error charge that can be expressed as:

$$Q_{RST}(k) = C_P(k) \cdot V'_{RPL,P}(k) + C_N(k) \cdot V'_{RPL,N}(k) \tag{5.4}$$

where $C_P(k)$ and $C_N(k)$ are the total capacitance connected to V_{REFP} and V_{REFN} respectively, $V'_{RPL,P}(k)$ and $V'_{RPL,N}(k)$ are reference ripple voltages during the k-th DAC reset. This error makes the replica DAC approach infeasible.

5.2.2.2 Proposed Cancellation DAC Implementation

By carefully examining the replica DAC method in Fig. 5.3(b), one can find that the need for intermediate reset is fundamentally due to the switching of the capacitor bottom-plate voltages. Thus, if we can match the RTF but without having charge redistribution, the need for reset can be obviated.

Following this train of the thought, a special cancellation DAC is designed, as shown in Fig. 5.3(c). The cancellation DAC is reset during the SAR ADC sampling phase. During the 1st MSB bit decision, it is disabled by making all capacitor bottom plates floating. There is no need to perform cancellation during the MSB decision, as the reference ripple shows up only as a common-mode signal at the comparator input. In the 2nd comparison cycle, the update of the cancellation DAC RTF is realized not by switching capacitor voltages, but by reconnecting appropriate capacitors. For example, with $D_2 = 1$, the MSB capacitor (in total $4C$) of the main DAC is connected to V_{REFN}. To match that, the bottom $4C'$ capacitor originally connected to V_{REFN} during the reset phase is re-enabled. At the same time, the 2nd MSB capacitors (two $2C'$) are also re-enabled. Since the re-enabled capacitors always connect to the same voltages as in the reset phase, there is no charge redistribution. As a result, the nominal output of the cancellation DAC remains at V_{CM}. No signal component is produced. Yet, if we discard the floating capacitors, the cancellation DAC indeed has the same configuration as the main DAC, leading to matched RTF.

With the 2nd bit decision of $D_1 = 0$, the cancellation DAC RTF can be updated in a similar fashion by appropriately disconnecting and re-connecting capacitors. Again, there is no charge distribution, thus obviating the need for the intermediate reset. However, this bit-by-bit RTF update introduces an update error. The reason is that when the bottom $2C'$ capacitor is disconnected, it takes away a charge that depends on V_{RPL}, causing the charge conservation

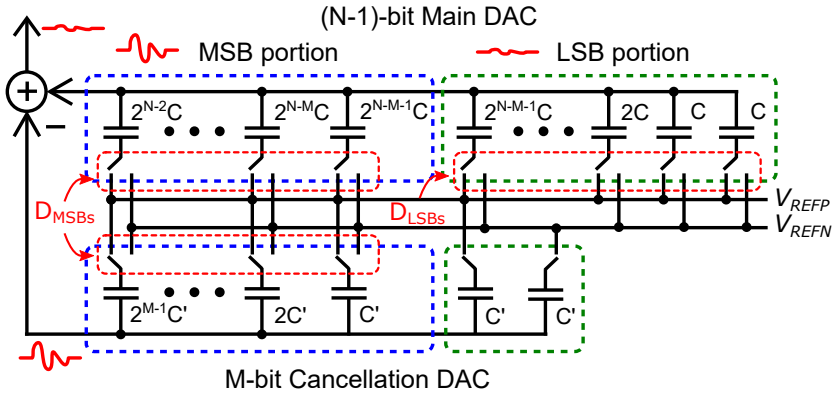


Figure 5.4: The DAC configuration during ripple cancellation phase.

at the cancellation DAC output to be broken. The moment before disconnecting the bottom $2C'$, the reference ripple at the cancellation DAC output is given by:

$$V_{E,C}(2) = 0.25 \cdot V'_{RPL,P}(2) + 0.75 \cdot V'_{RPL,N}(2) \tag{5.5}$$

By disconnecting this capacitor, an error charge is injected to the cancellation DAC:

$$Q_E(2) = [V_{E,C}(2) - V'_{RPL,N}(2)] \cdot 2C' \tag{5.6}$$

Q_E causes conversion error. Hence, no reconfiguration of the cancellation DAC is permitted. To address this limitation, as shown in Fig. 5.2, the cancellation DAC is disabled during the MSB bit decisions. It is configured only once at the end of the MSB bits. Even though no RTF update is allowed afterwards, the majority of the reference voltage errors are canceled because the RTF is mainly determined by the MSB bits, as explained in Section 5.2.1.

5.2.3 Reference Ripple Tolerance

This subsection analyzes the amount of reference ripple that can be tolerated without causing appreciable ADC performance loss. As discussed earlier, there are two mechanisms in the proposed ADC to mitigate the reference error. For MSB decisions, the tolerance comes from the redundancy. For LSB decisions, the tolerance comes from the ripple cancellation, which relies on the matching of the RTFs of the main DAC and the cancellation DAC. Since the cancellation DAC is configured only once and does not have any update during LSB decisions (see Fig. 5.2), the two RTFs will slightly differ, leading to non-perfect cancellation. Fig. 5.4 shows the configuration of the two DACs during the LSB comparisons for an N-bit SAR ADC that consists of an M-bit MSB portion and an LSB portion. The cancellation DAC is also M-bit, so that it can match the RTF of the MSB portion. For the first decision in the LSB section, because the two RTFs exactly match, theoretically speaking, the tolerance to the reference ripple can be infinity. Nevertheless, once the LSB bit decisions are loaded into the main DAC, the two RTFs no longer equal. The residue reference ripple, $V_{RES}(k)$, can be derived using (5.2) and (5.3):

$$\begin{aligned} V_{RES}(k) &= [RTF(k) - RTF_C(k)] \cdot V_{RPL}(k) \\ &= \frac{\sum_{i=M+2}^{k} 2^{N-i+1} \cdot D_{N-i+1}}{2^{N-1} + 2^{N-M-1}} \cdot V_{RPL}(k) \end{aligned} \tag{5.7}$$

The maximum error amplitude is reached when all D_i equal to $+1$ or -1:

$$|V_{RES,\max}(k)| = \frac{2 - 2^{M-k+2}}{2^M + 1} \cdot |V_{RPL}(k)| \tag{5.8}$$

Forcing it to be below half LSB size, we can solve the amount of ripple that can be tolerated. Overall, the amount of tolerable ripple, $V_{R,tol}(k)$, can be

summarized in the following expression:

$$\frac{V_{R,tol}(k)}{V_{LSB}} = \begin{cases} 2^{N-M}, & \text{for } k \leq M \\ \dfrac{2^M+1}{4-2^{M-k+3}}, & \text{for } k \geq M+1 \end{cases} \tag{5.9}$$

where V_{LSB} stands for the LSB voltage.

As can be seen from (5.9), for a fixed N, a larger M provides more error tolerance for LSB decisions due to more accurate RTF matching, but less error tolerance for MSB decisions due to smaller redundancy. In addition, a larger M also leads to increased cancellation DAC size. In a practical design, M has to be chosen judiciously to balance these trade-offs.

5.2.4 Effect of Path Gain Mismatch

So far we have assumed a perfect analog subtraction between the main DAC output and the cancellation DAC output. As will be shown later, this subtraction is embedded inside a dynamic comparator. Due to device mismatches and process variations, the two paths can have gain mismatch, causing error leakage and reducing ripple tolerance. Let $\Delta g \equiv 1 - g_2/g_1$ represents the gain mismatch, where g_1 and g_2 are the gains of the main DAC path and cancellation DAC path respectively. The maximum amplitude of the cancellation residue, $V_{RES}(k)$, can be re-derived as:

$$|V_{RES,\max}(k)| = \frac{\left|2 - 2^{M-k+2} + \Delta g(2^M - 1)\right|}{2^M + 1} \cdot |V_{RPL}(k)| \tag{5.10}$$

As can be seen from (5.10), the residue reference ripple increases with Δg. While the MSB ripple tolerance is set by redundancy and thus unaffected by

the path gain mismatch, the LSB ripple tolerance decreases in the presence of Δg:

$$\frac{V_{R,tol}(k)}{V_{LSB}} = \frac{2^M + 1}{|4 - 2^{M-k+3} + \Delta g(2^{M+1} - 2)|} \tag{5.11}$$

Thus, to ensure accurate ripple cancellation and large error tolerance, the path gain mismatch should be minimized via careful schematic and layout design.

5.3 Prototype SAR ADC Design

5.3.1 ADC Architecture

The schematic of the 10-bit prototype ADC is shown in Fig. 5.5(a). It consists of a main DAC, a cancellation DAC, a 4-input comparator, and an asynchronous SAR logic [Chen and Brodersen [2006a]]. As mentioned earlier, it adopts the split capacitor switching scheme [Ginsburg and Chandrakasan [2007]]. For the LSB, the single-side switching technique [Liu et al. [2010a]; Chen et al. [2014]] is used to halve the DAC size. The total capacitance of the 9-bit main DAC is 1056 fF with the unit capacitor size of 2 fF. The total capacitance of the 5-bit cancellation DAC is 528 fF with the unit capacitor size of 8 fF. These choices are made considering the matching and kT/C noise requirements. Dynamic logic is used to accelerate the SAR logic speed [Harpe et al. [2010]].

In this work, an extra pair of references, V_{REFP0}/V_{REFN0}, is introduced. They are used solely to reset the cancellation DAC during the ADC sampling phase. This way, the cancellation DAC and the main DAC are decoupled during the ADC sampling phase. In the prototype ADC design, the sam-

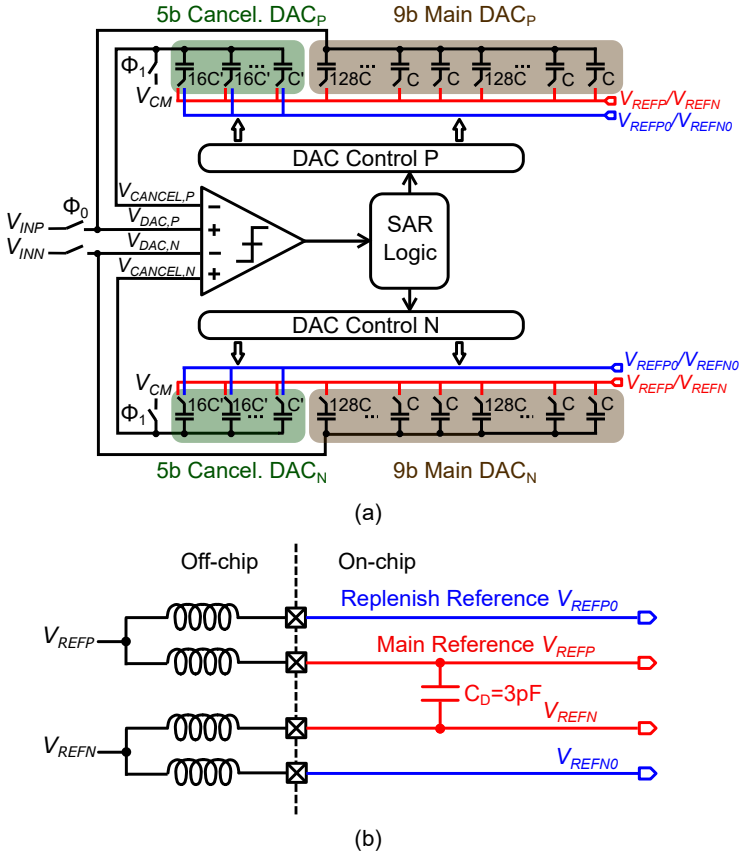


Figure 5.5: Architecture of the proposed SAR ADC.

pling phase takes 1 ns, which should be sufficient for the reference voltages V_{REFP}/V_{REFN} to completely settle. Having V_{REFP0}/V_{REFN0} provides extra assurance that even if V_{REFP}/V_{REFN} cannot fully settle during the ADC sampling phase, the cancellation DAC is still accurately reset. V_{REFP0}/V_{REFN0} and V_{REFP}/V_{REFN} are provided by four separate pads, but they are connected off-chip as shown in Fig. 5.5(b). The charge drawn from V_{REFP0}/V_{REFN0} is negligible as the cancellation DAC does not have any charge redistribution.

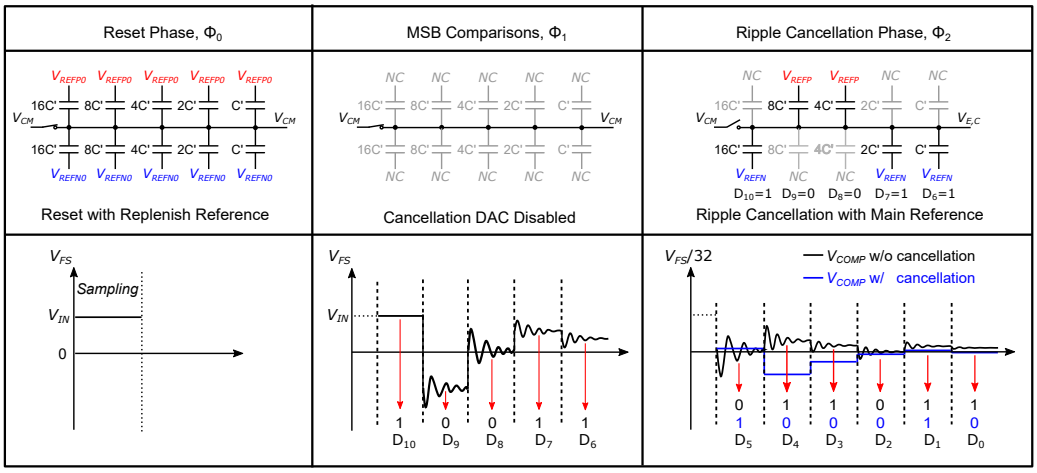


Figure 5.6: Cancellation DAC operation and signal behavior at the comparator input w/ and w/o cancellation.

Hence, V_{REFP0}/V_{REFN0} does not have any settling issue, and thus, does not need any decoupling capacitor. Thanks to the proposed reference ripple cancellation technique, only 3 pF on-chip decoupling capacitor is needed on the main references V_{REFP}/V_{REFN} to suppress the ripple to be within the tolerance range.

5.3.2 Cancellation DAC Operation

Fig. 5.6 shows the detailed operation of the cancellation DAC. During the ADC sampling Φ_0, the cancellation DAC is reset to V_{REFP0}/V_{REFN0}. During the first 5 MSB comparisons, the bottom plates are floating to prevent the comparator kick-back noise to interfere with the reference voltage. The top plates are always connected to V_{CM} during both Φ_0 and Φ_1. Once the 5 MSB comparisons are finished, $D_{OUT}[10:6]$ are loaded into the ripple cancellation DAC as described in Section 5.2.2. As illustrated in Fig. 5.6, without the rip-

ple cancellation technique, any reference error >0.5 LSB may cause a wrong comparison result. By contrast, with the cancellation technique, the equivalent ripples during the critical LSB decisions are significantly attenuated, leading to correct comparator decisions.

5.3.3 Ripple Cancellation Comparator

The ripple cancellation comparator adopts a Strong-Arm latch as its core. As shown in Fig. 5.7, an extra input pair (M_3 and M_4) is added to receive the cancellation DAC output. It has the same size as the main input pair (M_1 and M_2) to match the path gain, but with an opposite polarity. During the first 5 MSB comparisons, the gate voltages of M_3 and M_4 are always connected to V_{CM}, and thus, effectively disables this path. During the LSB comparisons when the cancellation DAC is enabled, the reference ripple is coupled through the cancellation DAC to the gates of M_3 and M_4, and thus, cancels out the reference ripple at the input of M_1 and M_2.

5.3.4 Choice of Cancellation DAC Resolution

This subsection aims to explain why the cancellation DAC is chosen to be 5-bit by analyzing the relationship among the reference ripple amplitude, the decoupling capacitor size, and the cancellation DAC resolution. The ripple amplitude depends on the DAC switching charge $\Delta Q(k)$ and the reference decoupling capacitor size C_D. The transient ripple amplitude caused by the

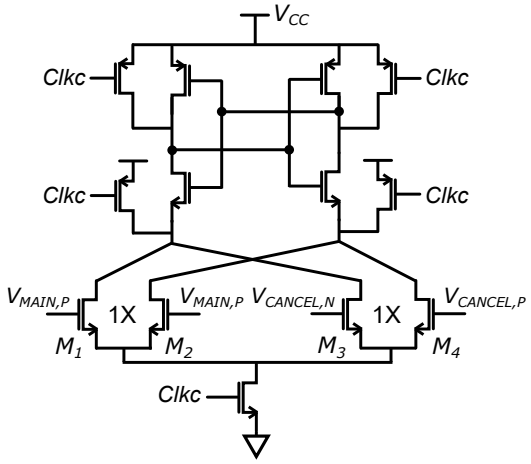


Figure 5.7: Ripple cancellation comparator.

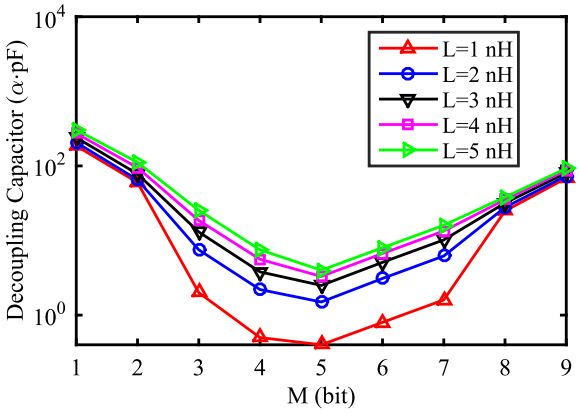


Figure 5.8: The required decoupling capacitor versus the resolution of the cancellation DAC for different L.

k-th DAC switching can be written as:

$$\frac{V_{RPL0}(k)}{V_{LSB}} = \alpha \cdot \frac{\Delta Q(k)}{C_D} \tag{5.12}$$

where the coefficient α is introduced to capture the linear relationship between the ripple amplitude and the switching charge. In a LC resonance limited settling system, a resistor R can be placed on-chip to reduce the quality factor

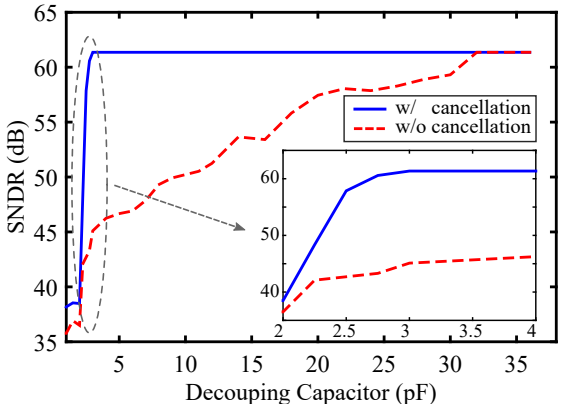


Figure 5.9: Simulated SNDR versus the decoupling capacitor.

of the resonance system. The reference ripple amplitude can be reduced by having large R, large C, or small L. Since L is package dependent and large R may cause non-linearity due to the RC settling error, a decoupling capacitor of suitable size is often chosen to suppress the reference ripple within error tolerance of each bit. When the decoupling capacitor is small, the ripple settling is dominated by the RLC resonance with the decay factor of $R/(2L)$. When the decoupling capacitor is large, the ripple settling is dominated by the RC response with the decay factor of $1/(RC)$. For simplicity, we use the decay function to approximate the ripple settling. With each SAR conversion cycle time of T, the reference ripple at the k-th comparison can be approximated using the following iterative equation:

$$V_{RPL}(k) = \begin{cases} V_{RPL0}(k-1)e^{\frac{-TR}{4L}} + V_{RPL}(k-1)e^{\frac{-TR}{2L}}, & \text{for } C_D < \frac{2L}{R^2} \\ V_{RPL0}(k-1)e^{\frac{-T}{2RC_D}} + V_{RPL}(k-1)e^{\frac{-T}{RC_D}}, & \text{for } C_D \geq \frac{2L}{R^2} \end{cases} \quad (5.13)$$

where $V_{RPL}(1) = 0$, as the MSB decision can be made without DAC switching for a top-plate sampled SAR ADC.

Using this simplified model, we can estimate the required decoupling capacitor size for different cancellation DAC resolution. The package bond-wire inductance is assumed to be less than 5 nH, and R is set to 20 Ω including the parasitic resistance. Fig. 5.8 shows that the minimum decoupling capacitance requirement is achieved when the cancellation DAC resolution $M = 5$. The trends for different inductors are similar. When M is too small, more reference decoupling capacitor is needed to handle the RTF mismatch during LSB decisions. By contrast, when M is too large, the redundancy is too small for MSB decisions, which also leads to increased decoupling capacitor size.

With the 5-nH bond-wire inductance and the 5-bit cancellation DAC, Fig. 5.9 shows the simulated SNDR versus the reference decoupling capacitor size. For simplicity, this simulation considers only the reference voltage error and the quantization error, but not capacitor mismatch and thermal noise. As can be seen, a small 3-pF decoupling capacitor is sufficient to meet the 10-bit accuracy with the proposed ripple cancellation technique. By contrast, for a conventional SAR ADC with the same redundancy at the 6-th bit comparison, a 10 times bigger 32-pF decoupling capacitor is needed. This result demonstrates the effectiveness of the proposed ripple cancellation technique.

5.3.5 Path Gain Mismatch Analyses

As mentioned in Section 5.2.4, the path gain mismatch affects the ripple cancellation effect. In the prototype ADC, there are three sources for the path gain mismatch Δg: 1) the DAC capacitor mismatch; 2) the DAC gain

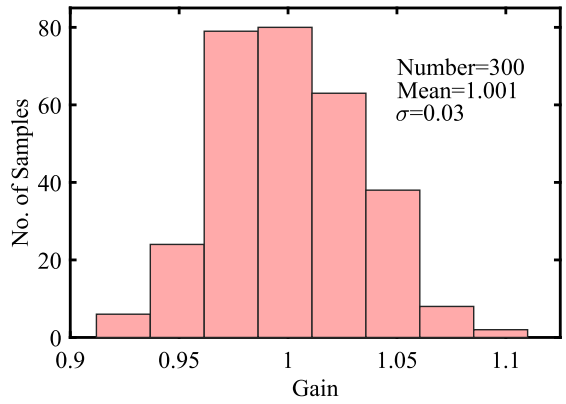


Figure 5.10: MC simulation result of path gain.

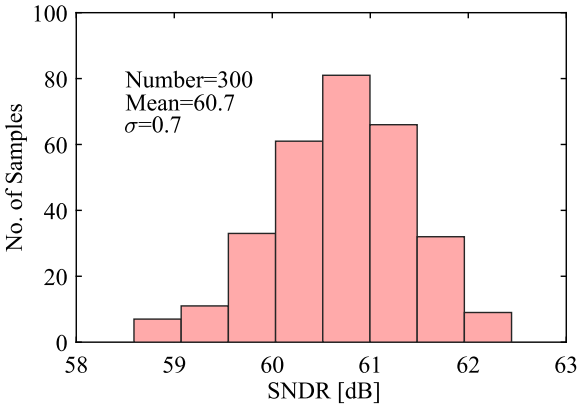


Figure 5.11: MC simulation result of the SNDR without thermal noise.

error due to the parasitic capacitance at the DAC output; 3) the mismatch between two comparator input pairs. In this work, the DAC matching is ensured by the chosen unit capacitor size and careful layout. As a result, the later two sources dominate the overall path gain mismatch. Based on post-layout simulation, the total parasitic capacitance, including the comparator input capacitance, switch capacitance, and routing capacitance, at the main DAC and the cancellation DAC outputs are estimated to be 65 fF and 29 fF,

respectively. The path gains of the main DAC and the cancellation DAC are 0.94 and 0.9, respectively, leading to a systematic gain mismatch of 4%. To evaluate the comparator gain mismatch, a 300-run Monte Carlo simulation is performed and the result is shown in Fig. 5.10. The standard deviation of comparator gain mismatch is 3%.

With these path gain mismatches included, a 300-run Monte Carlo simulation for the prototype ADC is performed. Fig. 5.11 shows the overall SNDR distributions. Here the SNDR considers all non-idealities except for noise. As can be seen, SNDR has a mean of 60.7 dB and a standard deviation of 0.7 dB. This result shows that even though there is a small path gain mismatch, the majority of the reference ripple is canceled out. The ADC performance is consistent. No path gain mismatch calibration is needed.

5.4 Measurement Results

The prototype ADC is fabricated in a 40-nm LP CMOS process. The die photo is shown in Fig. 5.12. The total active area is 0.023 mm^2. The reference decoupling capacitor occupies only 3% of the ADC core area. At the sampling rate of 120 MS/s, the ADC consumes in total 1.1 mW from a 1.2-V supply. The power breakdown is as follows: 0.41 mW for sampling and comparator, 0.38 mW for digital circuits, and 0.33 mW for DAC.

Fig. 5.13 shows the measured static performance. With the proposed ripple cancellation technique, the peak DNL and INL are reduced from $+5.9/-1$ LSB and $+6.1/-4.3$ LSB to $+0.59/-0.6$ LSB and $+0.7/-0.73$ LSB,

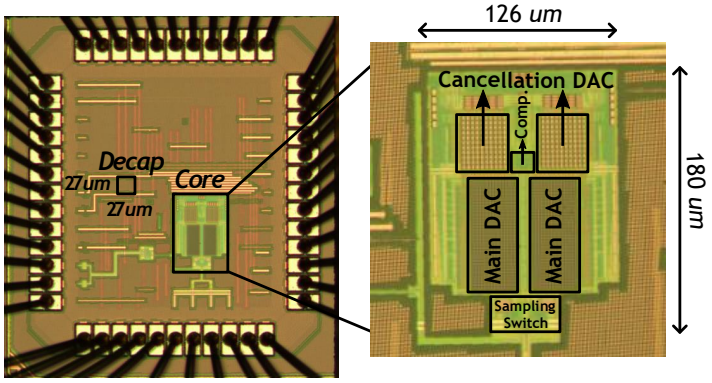


Figure 5.12: Die micrograph.

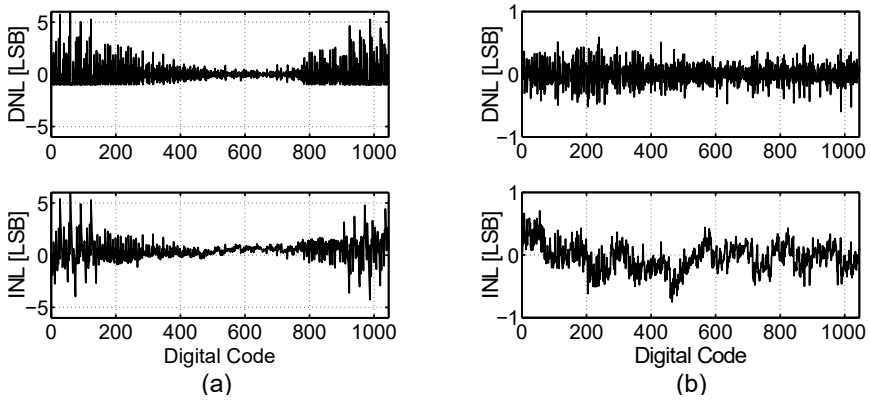


Figure 5.13: Measured DNL/INL (a) without and (b) with the proposed ripple cancellation technique.

respectively, which represents a 10 times worst-case improvement. Fig. 5.14 shows the measured SNDR and SFDR. At low input frequency, the SFDR/SNDR are improved by 16dB/10dB to 76.1dB/57.5dB, respectively. At Nyquist frequency, the SFDR/SNDR are improved by 9dB/8dB to 71.7dB/54.9dB, respectively. Appreciable performance improvements (>8dB) are observed across all frequencies ranges as shown in Fig. 5.15.

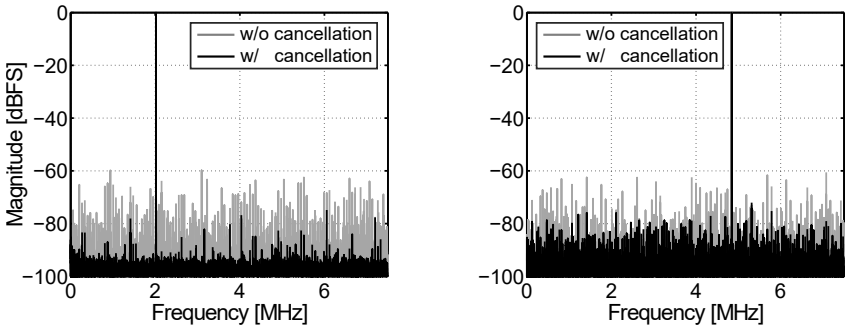


Figure 5.14: Measured spectra with low frequency and Nyquist frequency inputs at 120-MS/s sampling rate (output decimated by 8).

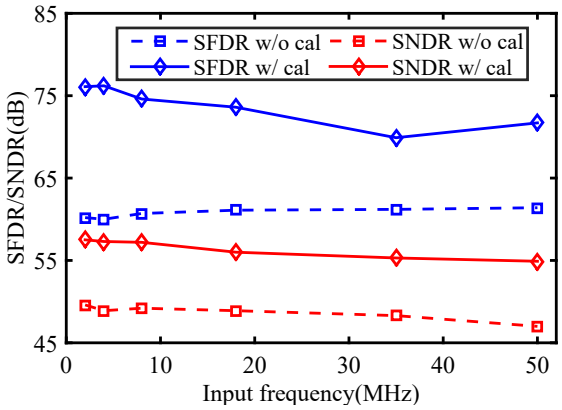


Figure 5.15: Measured SFDR and SNDR versus input frequency.

Table 5.1 summarizes the performance of the prototype ADC and compares it with other state-of-the-art ADCs. This work does not have an on-chip reference buffer; instead, it uses only a 3-pF decoupling capacitor, which is made possible by the proposed ripple cancellation technique. In contrast to [Chan et al. [2017]] which requires the reference to be completely clean during critical LSB conversions, this work provides continued error tolerance, which further relaxes the accuracy requirement on the reference voltage. The measured Walden figure-of-merit (FoM) is 20.5-fJ/conversion-step, which is in-line

Table 5.1: Performance Summary and Comparison with state-of-the-art high-speed SAR ADCs.

Specifications	JSSC-16 Tseng	JSSC-16 Venca	JSSC-17 Chan	JSSC-18 Martens	JSSC-19 Liu	JSSC-16 Zhu	**This work**	
Architecture	SAR	SAR-ΔΣ	SAR	Pipe-SAR	SAR	Pipe-SAR	**SAR**	
Technology [nm]	28	28	65	16	65	65	**40**	
Resolution [bit]	12	12	11	12	10	11	**10**	
Supply Voltage[V]	1.1/1.2	1.2/1.5	1.2	0.8	1.0/0.8	1.2	**1.2**	
Area [mm^2]	0.007	0.076	0.011	0.11	0.081	0.098	**0.023**	
Sample Rate [MS/s]	104	600	100	303	20	450	**120**	
No. of Channels	1	4	1	2	1	3	**1**	
De-cap/Reservoir [F]	N/A	20p	3p	50p	20p	300p	**3p**	
On-chip Ref. Buffer	Yes	Yes	No	No	No	No	**No**	
Ref. Ripple Cancel.	No	No	No	No	No	No	**No**	**Yes**
Peak SNDR [dB]	63	60.7	N/A	69.3	N/A	60.8	**47.4**	**57.5**
SNDR@Nyquist [dB]	N/A	58	59	63.9	55.4	56.2	**46.9**	**54.9**
Power [mW]	1.6	26.5	1.6	3.6	0.136	7.4	**1.04**	**1.12**
Peak FoM [fJ/c-s]	13.2	50	N/A	5.1	N/A	21	**45.3**	**15.2**
FoM@Nyquist [fJ/c-s]	N/A	68	21.9	9.2	13.3	32	**47.9**	**20.5**

with the state-of-the-art ADCs with above 100-MS/s sampling rate.

Chapter 6

Time-Domain Two-Step CDC

In the previous chapters, we have explored techniques to advance energy-efficiency of both low-power and high-speed converters. In this chapter, we will extend the techniques of ADC design into the capacitance readout circuits. This chapter[1] presents an incremental two-step CDC with a time-domain (TD) $\Delta\Sigma$M. Unlike the classic two-step CDCs, this work replaces the OTA-based active-RC integrator by a VCO-based integrator, which is mostly digital and consumes low power. Featuring the infinite DC gain in phase domain and intrinsic spatial phase quantization, this TD$\Delta\Sigma$M enables a CDC design, achieving 85-dB SQNR by having only a 4-bit quantizer, a 1st-order loop and a low OSR of 15. Fabricated in 40-nm CMOS technology, the prototype CDC achieves a resolution of 0.29 fF while dissipating only 0.083 nJ per conversion, which improves the energy efficiency by over 2 times comparing to that of state-of-the-art CDCs.

[1]This chapter is a partial reprint of the publication: Xiyuan Tang, Shaolan Li, Linxiao Shen, Wenda Zhao, Xiangxing Yang, Randy Williams, Jiaxin Liu, Zhichao Tan, Neal Hall, and Nan Sun, "A 16fJ/conversion-step Time-Domain Two-step Capacitance-to-Digital Converter," *in IEEE international Solid-State Circuits Conference (ISSCC)*, pp. 296-297, Feb. 2019. I am the main contributor in charge of circuit design, layout, and chip validations.

6.1 Introduction

Capacitive sensors are widely used to measure various physical quantities, including pressure, humidity [Tan et al. [2013]], and displacement [Xia et al. [2012]]. Ultra-low-power capacitance-to-digital converters (CDCs) are required for sensors with limited battery capacity or powered by energy harvesters. A SAR CDC is simple to design and well-suited for low-to-medium resolution applications. However, to reach high resolution, it requires a low-noise comparator [Omran et al. [2016]] or OTA-based active charge transfer [Ha et al. [2014]], resulting in degraded power efficiency. The $\Delta\Sigma$ CDC [Tan et al. [2013]] is suitable for high-resolution applications, but it requires OTAs and repeated charging of the sensing capacitor, leading to high power consumption. The zoom-CDC in [Oh et al. [2014]] achieves high resolution with only one-time charging, but its energy efficiency is still limited by power-hungry OTAs. The open-loop SAR-VCO CDC in [Sanyal and Sun [2017]] achieves low power consumption by eliminating the OTA; however, the VCO gain variation causes inter-stage gain error and requires background calibration, which increases the design complexity and makes it unsuitable for single-shot measurement in sensor node applications due to the long convergence time.

This work presents an incremental two-step CDC with a time-domain $\Delta\Sigma$M (TD$\Delta\Sigma$M) that achieves a resolution of 0.29 fF while dissipating only 0.083 nJ per conversion, which improves the energy efficiency by greater than 2 times comparing to that of state-of-the-art CDCs. This is achieved by performing $\Delta\Sigma$ modulation in the time domain. Unlike the classic zoom CDC

[Oh et al. [2014]], this work replaces the OTA-based active-RC integrator with a VCO-based integrator, which brings several merits: 1) the VCO is mostly digital and scaling friendly; it works well under low supply voltage and consumes low power; 2) it provides infinite DC gain in the phase domain, and thus is well-suited for high-precision applications that demand high DC loop gain; 3) it has intrinsic spatial phase quantization, and thus, enables a simple 4-bit quantization using only minimum-size DFFs; it obviates the need for an array of low-offset comparators. With a 4-bit quantizer, 85-dB SQNR can be achieved with a 1st-order loop and a low OSR of 15, which reduces the $\Delta\Sigma$M energy. Comparing to the open-loop VCO-based CDC [Sanyal and Sun [2017]], the proposed closed-loop TD$\Delta\Sigma$M CDC obviates the need for background calibration. Its closed-loop gain is set by capacitor ratio, which is precisely matched by merging the $\Delta\Sigma$ feedback DAC with the SAR DAC. Therefore, the VCO gain variation cannot change the feedback factor, and thus, has negligible impact on CDC performance ($\pm$20% VCO gain variation results in only 2 dB of SQNR change). By reusing the SAR comparator as the Gm stage of the VCO-based integrator, offsets in the SAR and the $\Delta\Sigma$M are inherently matched, which obviates the need for offset mismatch calibration.

6.2 Proposed CDC System Level Design

6.2.1 Conventional Two-Step Data Converter

The two-step CDC [Oh et al. [2014]; Xia et al. [2012]], also known as zoom-CDC, uses a SAR converter to coarsely quantize the sensing capacitance

C_X, followed by a $\Delta\Sigma$ modulator to perform fine quantization. Although the zoom-in nature restricts the converter to near-DC inputs [Chae et al. [2013]; Gonen et al. [2017]; Karmakar et al. [2018]], it is appropriate for sensor nodes where environmental parameters (e.g., capacitance) change very slowly.

To achieve high resolution, a high-order loop filter, as well as a large OSR, are required in zoom converters with a single-bit quantizer, which heavily increase the energy consumption. To address this limitation, multi-bit $\Delta\Sigma$ loop can be applied. However, to ensure loop linearity, dynamic element matching (DEM) block is usually required to address the feedback DAC mismatch issue, and calibration is needed to address comparator offset mismatches. With the constraints mentioned, the $\Delta\Sigma$M modulator power remains dominant and forms the energy-efficiency limitation of the zoom architecture.

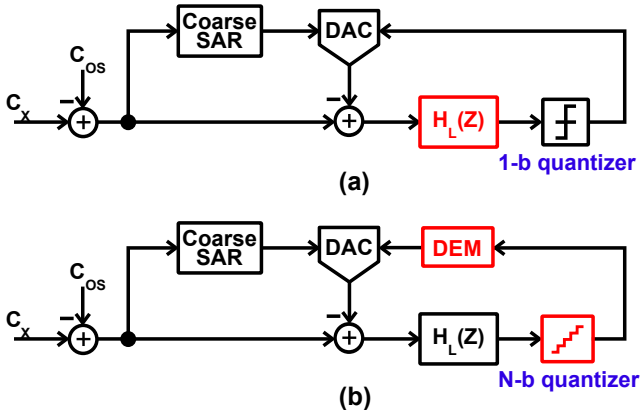


Figure 6.1: Conventional zoom converter design with (a) single-bit quantizer, and (b) multi-bit quantizer.

6.2.2 Proposed CDC Architecture

To break this limitation, a time-domain $\Delta\Sigma$ operation [Sanyal and Sun [2017]; Li et al. [2017]; Lee et al. [2015]] is employed in the proposed work. Fig. 6.2 shows the block and timing diagrams of the proposed CDC. During Φ_0, the bottom plates of sensor capacitor C_X and the offset capacitor C_{OS} are sampled to fixed reference voltages V_{refp}/V_{refn}. Once Φ_0 finishes, the bottom plate voltages are swapped, resulting in a signal charge proportional to the difference between C_X and C_{OS} transferred to the merged DAC array:

$$|Q_{DAC}| = |(C_X - C_{OS}) \cdot (V_{refp} - V_{refn})| \tag{6.1}$$

It is first quantized by a coarse 8-bit SAR in Φ_1. After that, an incremental 4-bit TD$\Delta\Sigma$M performs a fine quantization of the SAR conversion residue.

Fig.6.3 depicts the conceptual diagram of the proposed TD$\Delta\Sigma$M. The 7-stage ring VCO assumes the role of the loop filter. The ring VCO loop filter converts the residue voltage V_X into frequency variation at the VCO output while achieving phase integration. The integrated phase difference is subsequently detected by the PFD. As will be discussed in details in Section 6.3, the multi-PFD phase quantization scheme naturally transforms the phase information in every VCO stage to a tri-level output, which are then sampled and retimed through DFFs. The retimed digital output is readily a set of

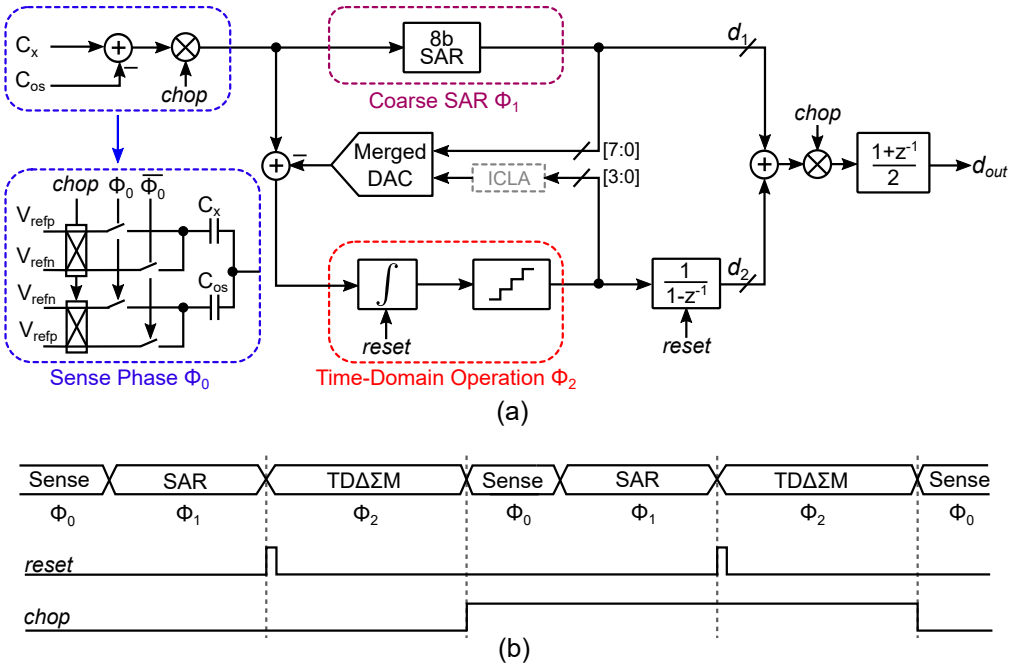


Figure 6.2: (a) Architectural diagram of the proposed CDC, and (b) the timing diagram.

thermometer codes for ΔΣM feedback DAC. The loop gain can be derived as:

$$\begin{aligned} Loop\ Gain &= K_{INT} \cdot K_{PFD} \cdot K_{DAC} \\ &= (K_{VCO} \cdot T_S \cdot 2\pi) \cdot (\frac{14}{4\pi}) \cdot (\beta \cdot \frac{2 \cdot V_{FS}}{14}) \end{aligned} \tag{6.2}$$

where K_{INT}, K_{PFD} and K_{DAC} represent the gain of phase integrator, PFD and feedback DAC, respectively. In the equation, the VCO tuning gain $K_{VCO} = G_m \cdot K_{CCO}$ consists of the transconductance of the Gm stage and the CCO current to frequency conversion gain. T_S is the period of the clock controlling the DFFs after the PFD array, i.e., the sampling period. β is the capacitive feedback factor of the loop and V_{FS} is the full swing of the CDAC reference voltage. With this 4-bit TDΔΣM and the 8-bit coarse SAR, the OSR is set

to 15 to achieve a 25-dB boost in SQNR, which gives the overall SQNR of 85 dB.

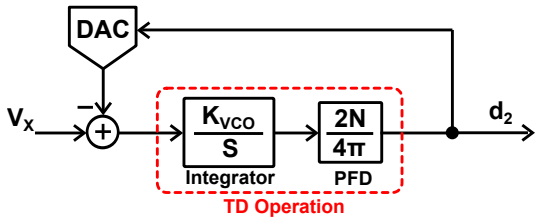


Figure 6.3: Simplified TDΔΣM model.

A decimation filter provides the digital output by filtering the TDΔΣM output d_2. For a thermal noise limited incremental modulator, a simple digital integrator provides sufficient thermal noise suppression [Steensgaard et al. [2008]]:

$$H(z) = \frac{1}{1 - Z^{-1}} \tag{6.3}$$

With an OSR of 15, it also provides notches at integer multiples of $f_s/15$, which provides suppression of periodic interferences.

To reduce the offset and flicker noise, the CDC is chopped at the system-level: the overall conversion is performed twice with swapped input polarities, and the two conversion results are averaged. Since CDC is limited by thermal noise, this technique also improves the overall SNR by 3 dB.

6.3 Detailed Implementation

6.3.1 Proposed CDC Schematic

Fig. 6.4 shows the simplified schematic. The circuit consists of two halves that are excited differentially. Only a single-ended circuit is shown in

the figure for illustration. The negative circuit includes another pair of C_X and C_{OS} that are connected through PADs to the replica of SAR and TD$\Delta\Sigma$M DAC arrays on chip. During Φ_0, the CDC is reset. When Φ_0 ends, by switching the bottom-plate voltages of C_X and C_{OS} between V_{refp} and V_{refn}, a differential voltage V_X proportional to $(C_X - C_{OS})$ is created at the comparator input. The SAR performs an 8-bit conversion of V_X. After that, the SAR comparator is reconfigured as a Gm stage and drives 2 current controlled oscillators (CCOs) to perform the phase-domain integration. The output of the 14-level phase quantizer is fed back to the DAC array to realize the $\Delta\Sigma$ modulation. With the 1st-order loop and 25% clock cycle retiming delay, this $\Delta\Sigma$M does not require any excess loop delay compensation.

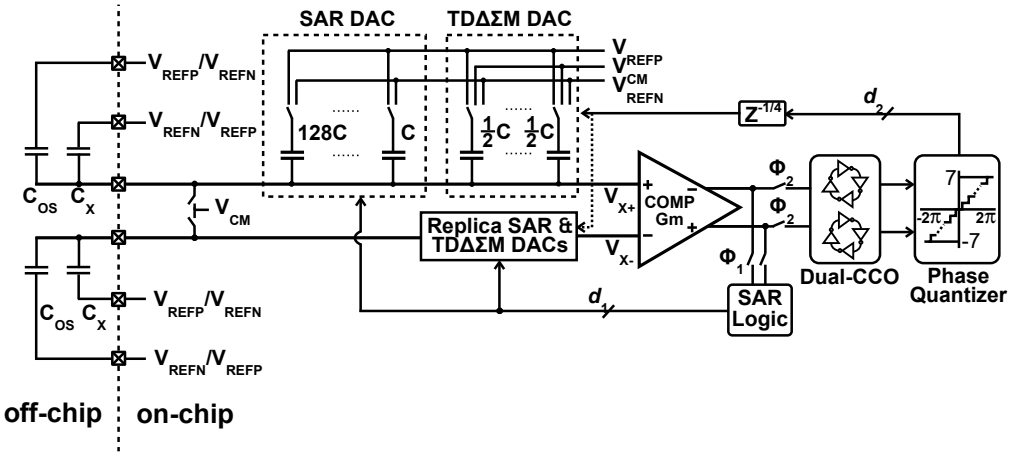


Figure 6.4: The simplified CDC schematic.

6.3.2 VCO-based Loop Filter Design

The VCO is implemented by a Gm-stage-driven CCO, as shown in Fig. 6.5. During Φ_0 and Φ_1, the two 7-stage CCOs are disabled. When Φ_2 arrives, the CCO rings are closed and start to oscillate with the same initial phase. To reduce the offsets between the SAR and TD$\Delta\Sigma$ stages, the comparator input pair $M1p, n$ and tail transistor Mb are reused as a Gm stage that converts residue V_X into current to drive the CCOs. As a result, the offset mismatch between the SAR and the VCO-based $\Delta\Sigma$M is minimized.

With the multi-phase PFD quantizer allowing lower VCO speed, the sub-μA CCO current results in low output swing (e.g., 0.25 V), thus level-shifting is needed between the VCO and the quantizer. To facilitate robust level-shifting [Drost et al. [2012b]], the CCO cell is made differential, as shown in Fig. 6.6(a), which also improves power supply rejection. In contrast to conventional CMOS cross-coupling [Li et al. [2017]], in this work, only PMOS cross-coupling is used to reduce the capacitive load, increase the VCO tuning gain, and reduce the CCO-contributed noise. Intuitively, in the CMOS-coupled design, the cross-coupled NMOS can be viewed as a common-source stage from the small-signal noise perspective. However, the cross-coupled PMOS essentially works as common-gate stage since the source node of the PMOS connects to the high-impedance Gm output instead of the supply. Therefore, the cross-coupled PMOS structure not only reduces the CCO cell loading to increase K_{CCO} but also contributes less noise comparing with the CMOS-coupled structure. The level-shifter [Drost et al. [2012a]] consumes no static

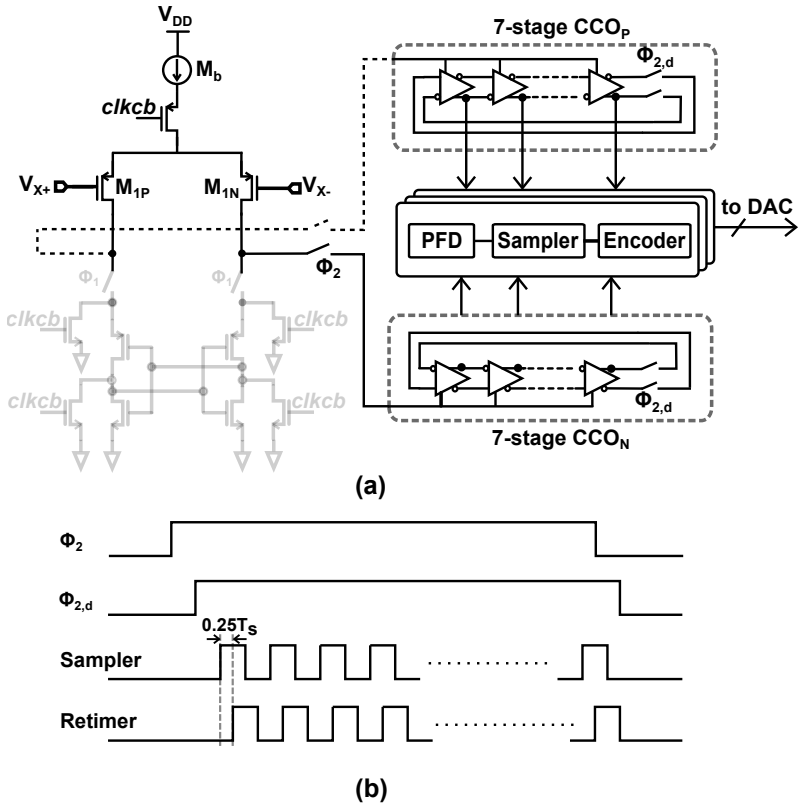
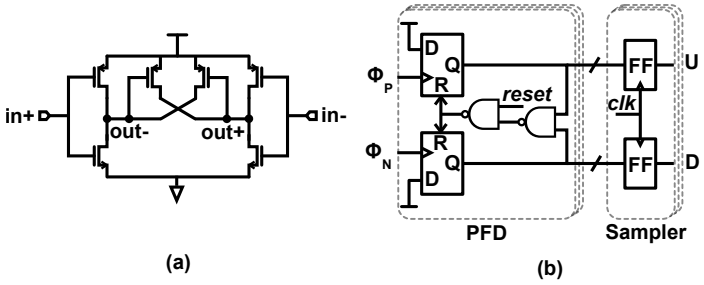


Figure 6.5: (a) Circuit schematic of the proposed VCO design, reusing the comparator as a Gm stage, and (b) the timing diagram of the TDΔΣM operation.

power and is designed to produce a sharp rising.



U	D	Encoder
1	0	1
0	0	0
0	1	-1

(c)

Figure 6.6: (a) CCO delay cell, (b) PFD design, and (c) Encoder mapping.

A phase frequency detector (PFD) is used to provide tri-level phase quantization. Comparing to an XOR gate that is widely used in VCO-based quantizers [Sanyal and Sun [2017]], the PFD doubles the quantizer resolution and quadruples the input phase range. The PFD output is retimed after 1/4 clock cycle delay. As shown in Fig. 6.6(c), the output of a quantizer slide (U, D) has three possible codes: 01, 00 and 10, which can be interpreted as (–1,0, +1) from a DAC control perspective. This tri-level signal naturally drives a tri-level DAC ($V_{refn}, V_{cm}, V_{refp}$). Note that V_{cm} does not need to be precise as it does not affect differential DAC outputs, which are $\pm(V_{refp} - V_{refn})$ and 0.

6.3.3 Redundancy Arrangement

The trade-off between resolution and redundancy is considered when choosing the unit capacitor size of the TDΔΣM DAC. In this work, a tri-level feedback DAC with C/2 unit capacitance is chosen to provide an inter-stage gain of 4. The full input range of the TDΔΣM is 14 LSB. With the 4-LSB SAR conversion residue, a ±5 LSB [(14 LSB - 4 LSB)/2] inter-stage redundancy range is provided to deal with the offset mismatches, which has already been minimized by reusing comparator as the Gm stage. There are two major offset contributors in the system including the cross-coupled pair in the comparator and the following ring-CCO. With 0.6-LSB (1 sigma) input-referred cross-coupled pair offset and 0.5-LSB (1 sigma) input-referred ring-CCO offset, an offset variation of 0.8 LSB is obtained in this system. With ±5 LSB inter-stage redundancy provided, greater than 6 sigma tolerance of offset mismatches is

achieved. Besides, if there is any SAR conversion error, it will also be absorbed by the above-mentioned redundancy.

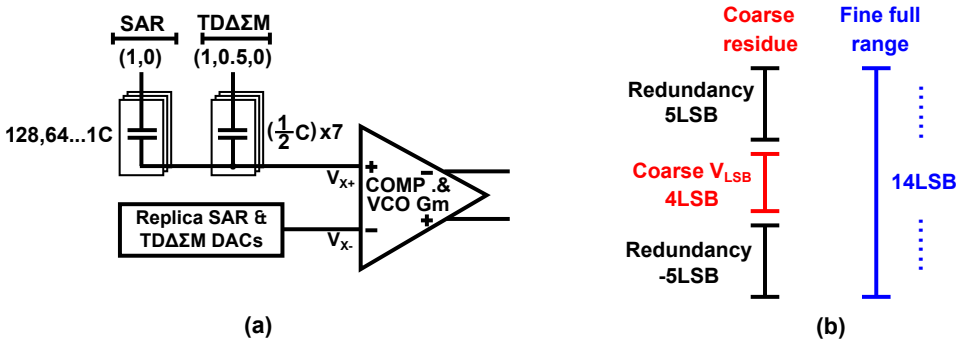


Figure 6.7: (a) Interfaces between coarse and fine converters and (b) voltage swing of the SAR's residue voltage, input range of TDΔΣM, and inter-stage redundancy.

6.3.4 Non-ideal effects in TDΔΣ CDC

As in any multi-bit ΔΣM, the DAC mismatch can cause non-linearity. This issue is typically addressed by having an explicit DEM circuit to scramble the DAC element selection pattern; however, it incurs additional power and area cost. In this work, the dual-VCO-based integrator brings intrinsic CLA (ICLA) capability [Li et al. [2017]], as shown in Fig. 6.8. As can be seen, the transition edge of the VCO is rotating at twice the VCO center frequency, which results in the same rotation frequency of the selected elements in the DAC array as $2f_{VCO}$. Hence, the mismatch errors are up-modulated to even-order harmonics of VCO center frequency and inherently suppressed by the decimation filter. As a result, greater than 85-dB linearity is ensured without an explicit DEM block.

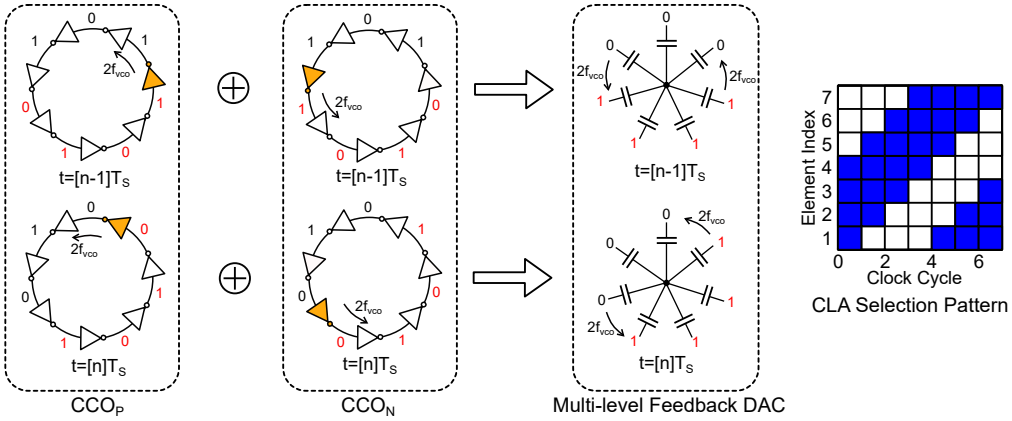


Figure 6.8: The illustration of Intrinsic CLA in the VCO-based ΔΣM.

One of the limitations of the conventional time-domain design [Sanyal and Sun [2017]] is the PVT-induced VCO gain variation, which changes the inter-stage gain, thus degrading conversion performance. In this work, the inter-stage gain between SAR and TDΔΣM is preciously defined as the capacitor-ratio and is independent of VCO gain. With high loop gain provided by the VCO integrator, this variation only has a limited impact on the system performance. To attest the robustness of the proposed architecture, a comparison between the previous open-loop design and the proposed closed-loop TDΔΣM is presented in Fig. 6.9. With ±20% VCO gain variation, the open-loop design has a significant performance degradation as 18 dB while our proposed work only has a 2.5-dB SQNR drop which has negligible impact to system SNR considering thermal noise.

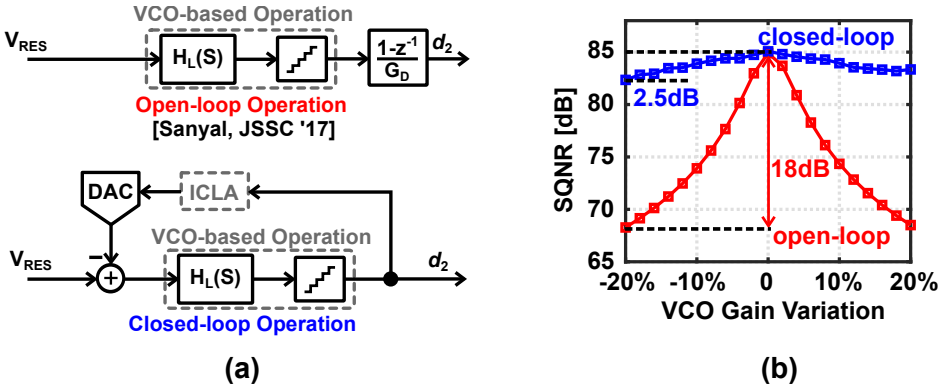


Figure 6.9: (a) Comparison between the proposed work and the previous time-domain design, and (b) performance degradation caused by VCO gain variation.

6.4 Measurement Results

The prototype CDC was fabricated in 40-nm CMOS technology with 20-fF SAR unit capacitor and 10-fF TD$\Delta\Sigma$M unit capacitor. It occupies an area of 0.06 mm^2, as shown in Fig. 6.10. The analog supply is 1.1 V, while the digital supply is reduced to 0.6 V to save power. With a measurement time of 12.5 μs, the CDC consumes 0.083 nJ per conversion, in which 0.044 nJ is consumed by the reference that charges the capacitors, 0.023 nJ is consumed by the VCO, and 0.016 nJ is consumed by digital logic.

A DC capacitance measurement is performed in Fig. 6.11. A series of DC capacitors ranging from 1 pF to 4 pF are measured. The measured code variation σ is within 0.012 which translates to a capacitance resolution of 0.24 fF.

To also evaluate the linearity, we reconfigured the sensing network to

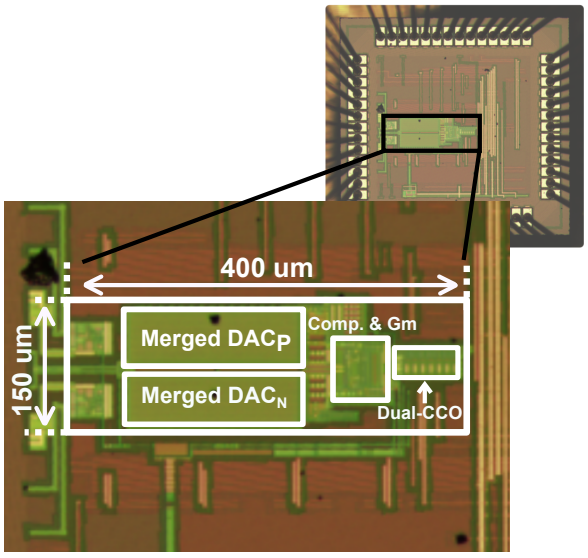


Figure 6.10: Die micrograph of proposed CDC design.

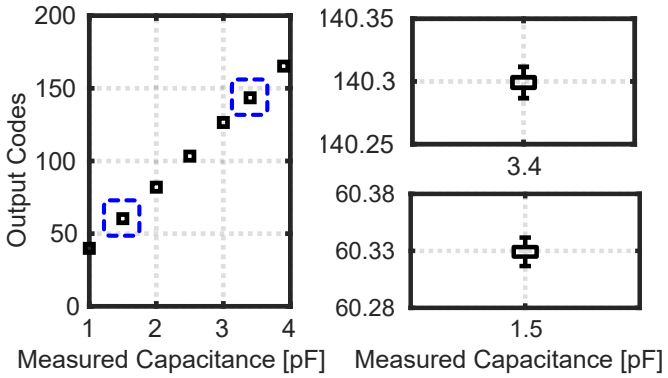


Figure 6.11: Measured DC capacitance performance.

the test mode. During the DC capacitance measurement, a fixed voltage (V_{refp}/V_{refn}) is sampled on C_X to observe the sensing capacitance change. In the test mode, a fixed 5-pF capacitor is connected as C_X, and a 1-kHz sine wave is applied as the sampling voltage to emulate the C_X change.

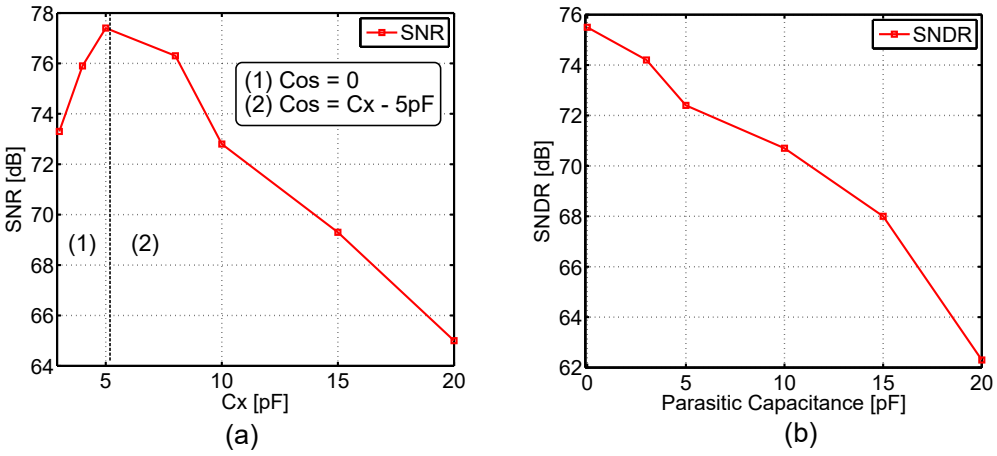


Figure 6.12: Measured SNDR versus (a) C_X and (b) parasitic capacitance.

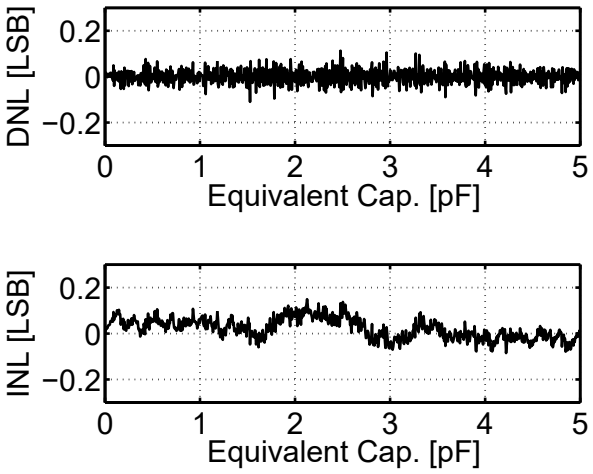


Figure 6.13: Measured DNL/INL plots.

Fig. 6.12(a) shows measured SNDR versus sensing capacitance. For $C_{OS} = 0$, the CDC supports an input range of 0–5 pF. The capacitance sensing range is extended by using a nonzero C_{OS}. Measured SNDR increases with C_X till 5 pF. Beyond 5 pF, as C_{OS} is combined with C_X, charge sharing is greatly increased, which increases the noise contribution from the CDC. This

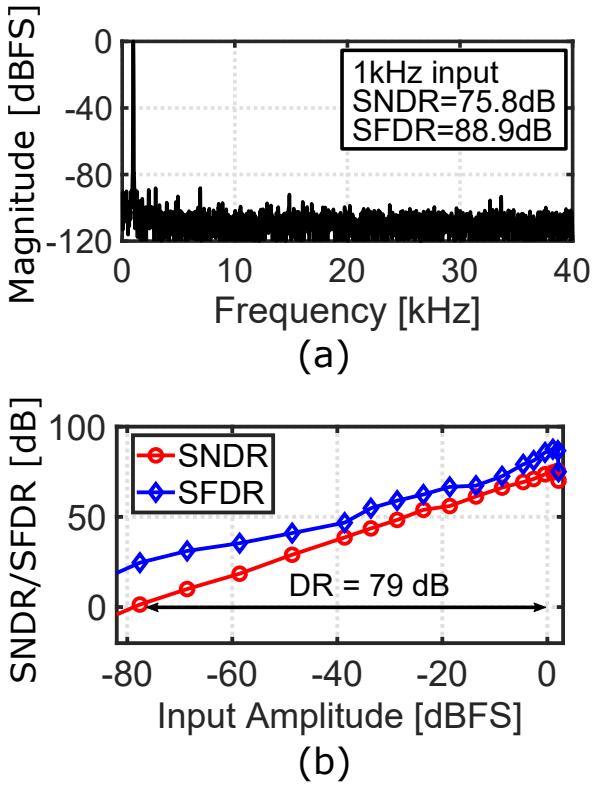


Figure 6.14: Measured (a) spectrum plot and (b) dynamic range plot.

leads to a decrease in SNDR beyond $C_X = 5$ pF. It should be noted here that for SNDR calculations beyond $C_X = 5$ pF, an effective full-scale capacitance range of $(C_X - C_{OS}) = 5$ pF is used. Fig. 6.12(b) shows the maximum SNDR achieved by the CDC as the parasitic capacitance is varied. As expected, CDC SNDR reduces as parasitic capacitance increases.

Fig. 6.13 shows the static performance of the CDC in the test mode. The measured DNL and INL are within ± 0.11 LSB and ± 0.15 LSB, respectively. The measured SNDR and SFDR are 75.8 dB and 88.9 dB, as shown in Fig. 6.14(a), respectively. The corresponding CDC resolution is 0.29 fF,

which includes both noise and non-linearities. The amplitude sweep, as shown in Fig. 6.14(b), demonstrates a dynamic range of 79 dB.

Fig. 6.15 compares figure of merit (FoM) versus ENOB of the proposed architecture with different CDC architectures. The FoM is calculated as $FoM = Energy/2^{resolution}$, which represents the energy required for each effective bit conversion. It can be seen that the proposed architecture compares favorably with the state-of-the-art and achieves highest energy efficiency.

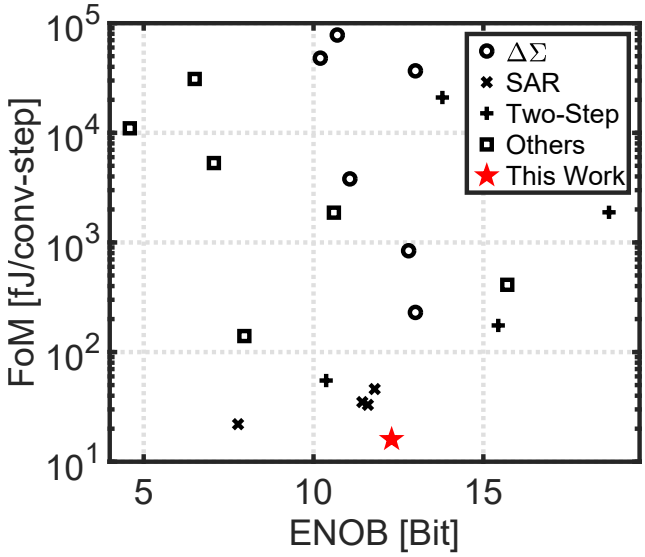


Figure 6.15: CDC energy-efficiency survey.

Table 6.1 summarizes the performance of this work and compares it with the state-of-the-art CDCs. This work is OTA-free; it uses a VCO to realize the TDΔΣM and also obviates the need for background calibration by operating the VCO in closed-loop. Overall, it achieves a CDC FoM of 16 fJ/conversion-step, which represents an over 2 times energy-efficiency improvement over the state-of-the-art.

Table 6.1: Performance Summary and Comparison with state-of-the-art CDCs.

	VLSI-16 Omran	ISSCC-14 Ha	VLSI-14 Oh	JSSC-17 Sanyal	JSSC-13 Tan	JSSC-15 Oh	ISSCC-15 Jung	**This work**
Process [nm]	180	180	180	40	160	180	40	**40**
Architecture	SAR	SAR	Zoom SAR+ ΔΣM	SAR+VCO	ΔΣM	Dual-Slope	Delay-Chain	**Zoom SAR+ TDΔΣM**
Measured Sensor	Dual	Single	Single	Single	Dual	Single	Single	**Dual**
Need Back. Cal.	NO	NO	NO	YES	NO	NO	NO	**NO**
OTA-Free	NO	YES	NO	YES	NO	NO	NO	**YES**
Input Range [pF]	0-12.66	2.5-75.3	0-24	0-5	0.54-1.06	5.3-30.7	0.7-10000	**0-5**
Meas. Time	16	4000	230	1	800	6400	19	**12.5**
Resolution [fF]	1.1	6	0.16	1.1	0.07	54.9	12.3	**0.29**
Energy [nJ]	0.12	0.64	7.75	0.075	8.24	0.704[4]	0.035[3]	**0.083**
SNDR[1] [dB]	70.6	81.8	94.7	64.2	68.4	44.2[4]	49.7[3]	**75.8**
FoM[2] [fJ/conv-step]	35	64	175	55	3800	5300[4]	140[3]	**16**

[1] $SNDR = 20 \cdot log_{10}(\frac{Capacitance\ range/\ 2/\sqrt{2}}{Capacitance\ resolution})$

[2] $FoM = \frac{Energy}{2^{(SNDR-1.76)/6.02}}$

[3] Measured with 11.3pF

[4] Calculated with one subrange

Chapter 7

Conclusion

This dissertation has proposed a set of techniques to improve the energy efficiency of data conversions in different application regimes. The major contributions are concluded in this session.

The first two techniques presented in Chapter 2 and Chapter 3 boost energy efficiency of dynamic comparator, which is the fundamental block in the data converters. Chapter 2 proposed a dynamic comparator with a common-gate stage to increase the pre-amplification gain, thereby improving low-power SAR ADC performance. Chapter 3 presents a dynamic comparator with a novel floating inverter pre-amp. It realizes current-reuse, boosts g_m/I_D, and prevents fully discharge of the integration capacitors by the CMOS dynamically-biased integration. Powered by the floating reservoir capacitor, this pre-amp achieves input CM insensitivity.

Chapter 4 addresses the comparator mismatch issue in loop-unrolled architecture. By employing a fully-dynamic pre-amplifier in the second stage operation, the comparator offset mismatches are alleviated without any calibration, thus ensuring the conversion linearity.

Chapter 5 proposes a new perspective to solve the reference settling

problem. Instead of minimizing reference ripple as in the conventional approaches, this work provides an extra path for the reference ripple to couple to the comparator but with an opposite polarity, so that the effect of the reference ripple is canceled out. This technique only requires a small on-chip decoupling capacitance, thus significantly reducing the reference stabilization cost.

Chapter 6 extends the energy-efficient design techniques to a capacitive sensor readout circuit. The design of an incremental two-step CDC including a time-domain $\Delta\Sigma$ modulator is presented. By operating fine conversion in the time-domain, this work greatly reduced $\Delta\Sigma$M power and improves the capacitance conversion efficiency.

All designs were validated through measurement on silicon prototypes, and demonstrated solid evidence on advancing cutting-edge performance. In summary, the energy-efficiency and simplicity of the proposed data converter techniques make them suitable candidates for future SoC, mobile, and especially IoT applications in advanced technology nodes.

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