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An evaluation of the electrical, material, and reliability characteristics and process viability of ZrO_2 and ZrO_xN_y for future generation MOS gate dielectric

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An evaluation of the electrical, material, and reliability characteristics and process viability of ZrO_2 and ZrO_xN_y for future generation MOS gate dielectric

by

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An evaluation of the electrical, material, and reliability characteristics and process viability of ZrO_2 and ZrO_xN_y for future generation MOS gate dielectric

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Over the past decades, continuing advancements in processes and tools and the introduction of new materials have facilitated the rapid downscaling of metal-oxide-semiconductor (MOS) technology. The 90 nm technology node and beyond will face one of the toughest challenges of the semiconductor industry – the replacement of conventional silicon dioxide (SiO_2) gate dielectric with a high-k dielectric material. SiO_2 has been used as the gate oxide since the inception of the MOSFET, but is reaching its physical scaling limits (~10-15Å) due to excessive gate leakage current and reliability issues. High-k materials are required to reduce leakage current while maintaining a low equivalent oxide thickness (EOT). However, the integration of high-k dielectrics into the MOS process will be a serious challenge.

One promising high-k candidate is zirconium oxide (ZrO_2) since it is has demonstrated thermal stability on Si, a dielectric constant ~20, a bandgap of 5.8 eV, low EOT (= 10Å), and low gate leakage. In this research, sputter-deposited ZrO_2 and

nitrogen-incorporated ZrO_2 (ZrO_xN_y) were evaluated in terms of electrical, material, and reliability characteristics to determine their viability as high-k gate dielectrics. Initially, platinum-gated MOS capacitors were studied to optimize the ZrO_2 deposition process and demonstrate low EOT (8.2Å) and low leakage. Unfortunately, both ZrO_2 and ZrO_xN_y were found to be incompatible with the polysilicon gate electrode process due to the formation of Zr-silicide and consequently, high leakage. However, dual metal gate electrodes will eventually replace polysilicon because of the polysilicon depletion effect.

Tantalum nitride (TaN) is a promising NMOS metal gate candidate due to its thermal stability and low resistivity. Both TaN-gated MOS capacitors and self-aligned transistors using ZrO_2 and ZrO_xN_y were fabricated to demonstrate process viability and characterized to yield low EOT (9.5Å), low leakage, negligible frequency dispersion, low C-V hysteresis, good thermal stability, and well behaved transistor characteristics. In addition, a high temperature (500-600ºC) forming gas anneal was found to improve mobility, subthreshold swing, and transconductance. Overall, ZrO_2 and ZrO_xN_y have demonstrated extremely promising electrical, material, and reliability characteristics as well as process viability and require further investigation as potential high-k gate dielectrics.

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CHAPTER 1

Introduction and Background

1.1 Challenges to Moore's law: 90 nm and beyond

The most crucial element in the success of the silicon semiconductor industry has been its continued ability to downscale transistor dimensions over the last few decades. Innovations in fabrication processes and the introduction of new materials and tools have allowed chipmakers to follow Moore's law each generation. Fig 1.1 illustrates how the number of metal oxide semiconductor field effect transistors (MOSFETs) in Intel processors has doubled with each technology generation as printed gate lengths have shrunk exponentially [1]. As gate lengths have been scaled to 90 nm and lower, new problems have arisen:

- SiO_2 minimum scaling limits
- Polysilicon depletion (PD) effect
- Quantum mechanical (QM) effects
- Non-scalability of threshold voltage (V_t)
- Mobility degradation
- Ultra-shallow Source/Drain junctions and S/D resistance
- Both adequate drive current and turn-off

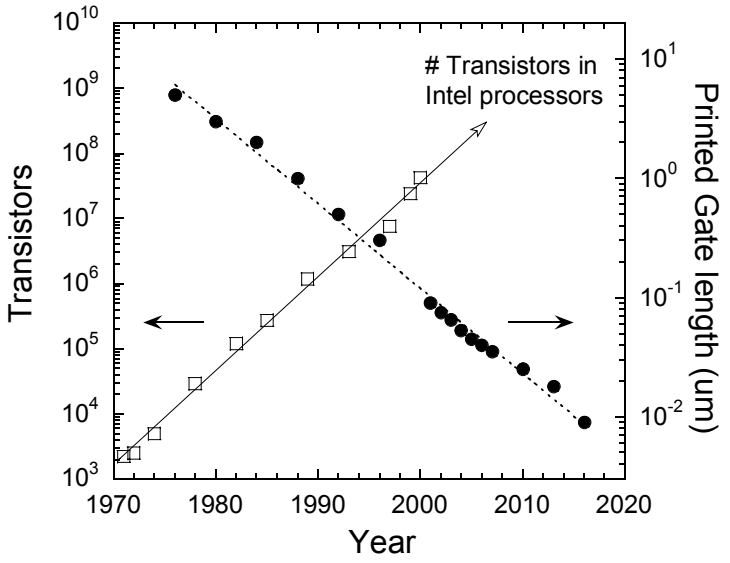

Figure 1.1 The number of transistors in Intel processors increases and transistor gate lengths decrease exponentially over the years [1].

The first three challenges – SiO_2 minimum scaling limits (section 1.2), the PD effect, and QM effects – will be discussed at length since they are the key motivations behind the need for high-k gate dielectrics.

Heavily doped polysilicon (poly) has been used as the gate electrode material since the 1970s. Poly gate electrodes have worked well in complementary metal oxide semiconductor (CMOS) processes for several reasons. First, the workfunction can be manipulated to be either p-type or n-type depending on the dopant and doping level. Additionally, poly gates lend themselves well to the self-aligned MOSFET process since they can be doped during the source/drain (S/D) implant, activated during S/D annealing, and can withstand the high temperatures required for CMOS processing.

The poly depletion (PD) effect is caused when the MOSFET is turned on and the poly gate electrode is depleted at the poly/SiO_2 interface. This thin depletion layer adds to the equivalent oxide thickness (EOT) and consequently, reduces the gate capacitance and drain current. Although PD only adds a 1-4 angstroms (Å) to the EOT, this represents a large percentage since EOT values will be less than 10Å by 2004 [2]. Additionally, PD has been reported to get worse as the gate length gets shorter ($\leq$ 35 nm) due to vertical fringing gate fields [3]. Increasing the poly doping can reduce PD, but achieving uniform doping is difficult due to the constraints of dopant (boron) diffusion into the gate oxide and maintaining the correct S/D junction depth and width during activation annealing [4]. Ultimately, PD will force the replacement of poly by dual metal gate electrodes.

Like PD, the quantum mechanical (QM) effect results in an increase in EOT. At gate lengths below 0.25 μm, the combination of high channel doping and thin gate oxides results in high electric fields at the Si surface. These high fields result in a splitting of the conduction band into discrete sub-bands, causing quantization of the carriers perpendicular to the SiO_2/Si interface [5,6]. As a result, carriers in the channel actually travel a few angstroms (Å) below the gate dielectric/silicon interface leaving a thin charge depletion region. This depletion region has a dielectric constant of Si (11.7) and thus reduces the gate stack capacitance, and the EOT is increased ~3-5Å [7]. Unfortunately, there is no known solution to avoid the EOT increase caused by QM.

1.2 Scaling limits of SiO_2

One of the industry's biggest scaling challenges – the replacement of silicon dioxide (SiO_2) as the MOSFET gate dielectric – must be addressed in order for the scaling to continue in the coming years. SiO_2 has been used as the gate dielectric material in MOS technology since the inception of the MOSFET in 1960. The ability to grow high-quality insulating oxide on silicon was one of the major reasons Si was chosen as the 'mainstream' semiconductor material. High temperature growth of the oxide directly from the silicon offered many desirable properties such as an excellent interface, thickness controllability, high thermal stability, and good reliability. Thus, replacement of SiO_2 with a deposited material that can offer comparable properties will prove to be a difficult challenge.

So, what is the driving force behind the replacement of SiO_2? The 2001 Edition of the International Technology Roadmap for Semiconductors (ITRS) predicts that the gate dielectric must have an equivalent oxide thickness (EOT) of 11-15Å in 2003 [2]. A SiO_2 layer of 11-15Å thick is only around 3-4 monolayers of SiO_2, which creates several problems.

First, a physical thickness of 11-15Å is so thin that electrons can directly tunnel through the SiO_2, resulting in excessively high gate leakage current. High leakage is a great concern, particularly for low power applications, and high performance applications as well. Figures 1.2a and 1.2b show the predicted gate

dielectric leakage limits and equivalent oxide thickness (EOT) range for in the coming years, respectively [2].

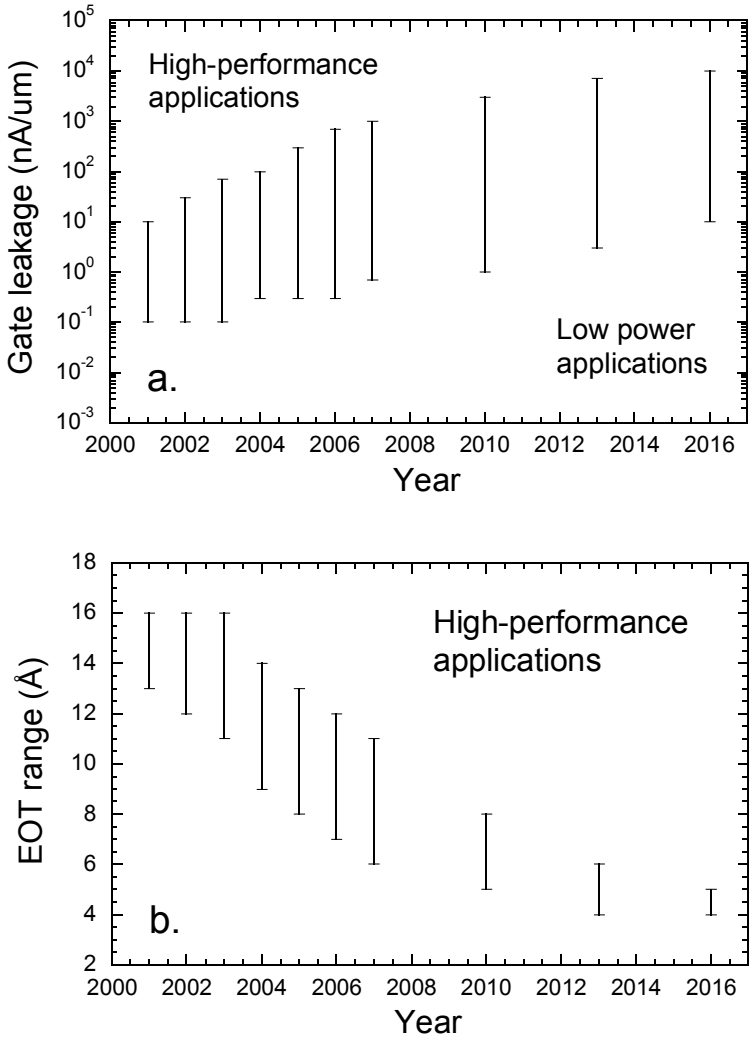

Figure 1.2 (a) The predicted range of acceptable gate leakage current over the years where the upper limit represents high performance and the lower limit represents low power applications [2].
(b) The range of EOT for high performance applications in the coming years [2].

Additionally, SiO_2 thickness uniformity across a 300 mm wafer becomes even more crucial for such a thin film, since even a monolayer difference in thickness represents a large percentage difference and thus can result in varying threshold voltage (V_t) across the wafer. Reliability also becomes a huge concern for such a thin SiO_2 dielectric.

1.3 Motivation for various high-k gate dielectric candidates

Materials with a dielectric constant higher than that of SiO_2, known as high-k dielectrics, have been under intense investigation in order to identify a SiO_2 replacement. High-k materials can provide the same capacitance as a very thin layer of SiO_2 although they are physically thicker as shown in equation 1.1 where C represents capacitance; k is dielectric constant; ε_o is the permittivity of free space - a constant; A is capacitor area, and t is dielectric thickness.

$$C = k\varepsilon_o \frac{A}{t} \qquad (1.1)$$

There is a wide range of high-k materials with a wide range of dielectric constants as shown in table 1.1.

	SiO_2	Si_3N_4	Al_2O_3	$ZrSiO_4$	$HfSiO_4$	ZrO_2	HfO_2	Ta_2O_5	TiO_2	BST
k	3.9	7	~10	~13	~15	~22	~25	~23	~80	~300

Table 1.1 Various gate dielectrics and their dielectric constants [8,9,10]

Materials at both ends of the spectrum will be discussed before concentrating more closely on the mid-range high-k materials.

1.3.1 Moderate high-k materials: Oxynitrides and Si_3N_4

Oxynitrides have been under investigation for gate dielectric application for over a decade. It was discovered that the introduction of nitrogen into SiO_2 via NO, N_2O, or NH_3 annealing, termed oxynitride, not only raised the dielectric constant slightly ($k \sim 5.5$, depending on nitrogen content [11,12]) but also had the added benefits of improved reliability, increased resistance to boron penetration, and better interfacial quality [13]. Nitride, Si_3N_4 ($k \sim 7$), has also been considered as a gate dielectric, and is attractive because it is already used in MOS technology. In addition, research on oxide/Si_3N_4 stack structures has demonstrated MOSFETs with 70 μm gate length [14].

Unfortunately, these oxynitrides, as well as oxide/Si_3N_4 stacks, and Si_3N_4 are still limited by their relatively low dielectric constants, and thus cannot be scaled much lower than 10Å. Consequently, these dielectrics will only last a few generations due to limitations dictated by low power applications and scalability.

1.3.2 Ultra high-k: Barium Strontium Titanate (BST)

Initial research into high-k MOS gate dielectrics focused on ultra high-k materials such as barium strontium titanate (BST) because it had already been

investigated for giga-bit DRAM applications [15,16,17]. EOT values of less than 1Å have been achieved with DRAM metal-insulator-metal (MIM) capacitors using BST [15]. However, researchers soon discovered that BST in metal-insulator-semiconductor (MIS) capacitors yielded much higher EOTs due to the formation of a relatively thick (~30Å) Si_xO_y interfacial layer between the BST and silicon substrate. The growth of this Si_xO_y layer resulted from reaction and interdiffusion between the BST and substrate [18], and it was concluded that BST was not thermodynamically stable in contact with silicon.

Various barrier layers and surface treatment techniques were used in an attempt to prevent this interfacial reaction. Barrier layers of Si_3N_4 [18], Ta_2O_5, TiO_2 [18], and ZrO_2 [19] did reduce the interfacial layer thickness, and thus the EOT, but not substantially enough to make BST a viable gate dielectric. Figure 1.3a shows the EOT reduction (~7Å) of Pt/BST/ZrO_2/Si capacitors as compared to Pt/BST/Si capacitors with the same BST thickness after various oxygen anneal temperatures [19]. Additionally, experiments using nitrogen (N_2) implantation into the Si substrate prior to BST deposition also resulted in reduced EOT values [20]. The nitrogen incorporated at the BST/Si interface served to decrease the interdiffusion and reaction between the BST and Si. As shown in figure 1.3b, the EOT decreased with increasing N_2 implant dose, but the drawback was that the leakage increased as a result of both lower EOT and increased implant damage with increasing dose [20].

Although the introduction of high-k barrier layers and the N_2 implantation technique did help scale the EOT of BST, they did not improve the scalability significantly enough to justify the added process complexity.

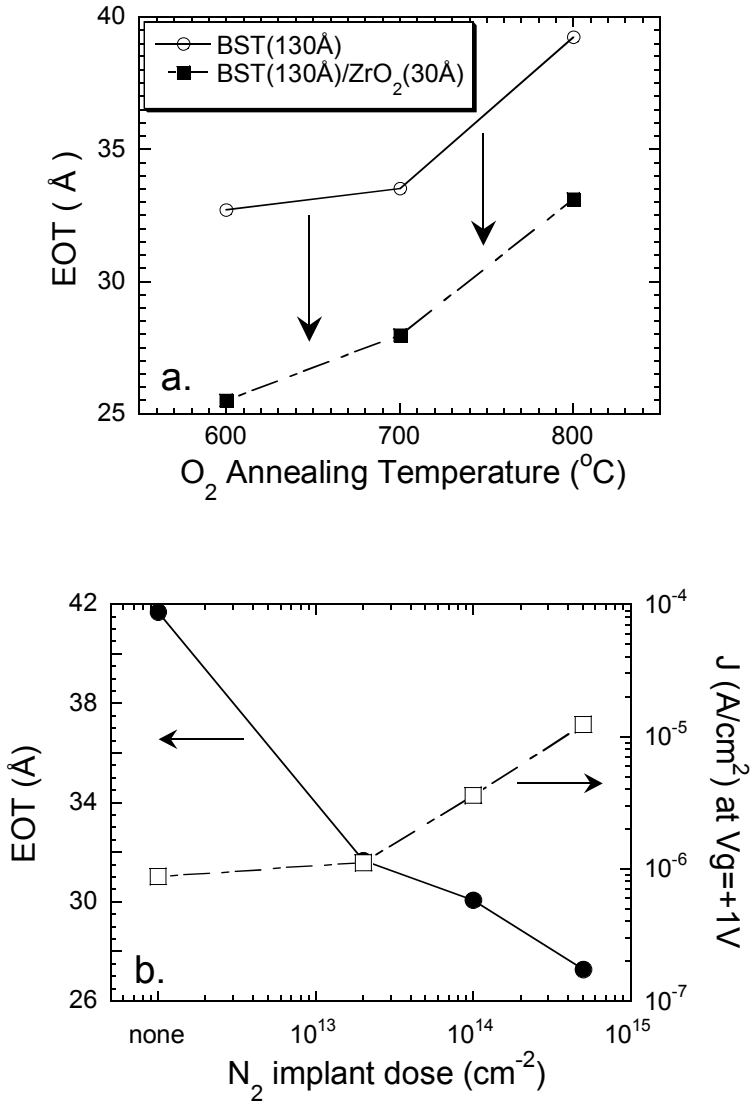

Figure 1.3 (a) EOT comparison of Pt/BST and Pt/BST/ZrO_2 stack structures for different oxygen annealing temperatures [19]. (b) EOT and leakage (J) dependence on N_2 implant dose of BST on N_2-implanted Si [20].

1.3.3 Mid-range high-k: Ta_2O_5, TiO_2, BeO, MgO, HfO_2, and ZrO_2

Of the mid-range high-k dielectrics, Ta_2O_5 and TiO_2 were initially studied, but were also found to have problems with interfacial layer formation between the high-k material and the silicon substrate. Focus was then shifted towards identifying high-k materials that were thermodynamically stable in contact with silicon.

In 1996, Hubbard and Schlom performed a thermodynamic analysis to determine which binary metal oxides were theoretically stable in contact with silicon up to temperatures ~700ºC [21]. Chemical equations were analyzed to determine the change in Gibbs free energy and thus the favored state of a system; if the Gibbs free energy was lowered for any of the equations, it was an indication of instability of the oxide with silicon. The chemical equations were as follows where MO_x represents the binary metal oxide [21]:

$$Si + MO_x \rightarrow M + SiO_2 \qquad (1.2)$$

$$Si + MO_x \rightarrow MSi_z + SiO_2 \qquad (1.3)$$

$$Si + MO_x \rightarrow MO_w + SiO_2 \qquad (1.4)$$

$$Si + MO_x \rightarrow MSi_z + MSi_xO_y \qquad (1.5)$$

$$Si + MO_x \rightarrow M + MSi_xO_y \qquad (1.6)$$

Equations 1.2 and 1.3 test for the formation of metal products (M) and silicides (MSi_z), respectively, with SiO_2. Equations 1.4-1.6 tested for the formation of other

binary oxides (MO_w) as well as ternary phases (MSi_xO_y). From these calculations, it was found that Ta_2O_5 was not thermodynamically stable, as it tended to dissociate into metallic Ta, thus failing equation 1.2. Furthermore, TiO_2 was also found to be unstable at temperatures around 700ºC because it tended to form a silicide, $TiSi_x$, thus failing equation 1.3.

Due to insufficient thermodynamic data, Hubbard and Schlom were not able to verify the thermal stability of HfO_2, although later studies have demonstrated stability via excellent device and materials characteristics [22,23]. HfO_2 is a promising candidate for high-k gate dielectric and will be mentioned periodically in chapters 3-5.

Hubbard and Schlom were able to verify the stability of three binary oxides: ZrO_2, BeO, and MgO. Since BeO and MgO have fairly low dielectric constants of 6.8 and 9.8 [8], respectively, they are of little interest as oxynitrides and oxide/nitride stack structures have comparable dielectric constants and are more well established processes. Because ZrO_2 has a reported dielectric value ranging from 17-27 [24,25] and was deemed thermally stable by Hubbard and Schlom, it has received much attention as a promising high-k gate dielectric candidate.

1.3.4 Requirements for high-k dielectrics [26,27]

As mentioned earlier, the replacement of thermally grown SiO_2 with a deposited high-k gate dielectric will be particularly difficult due to the excellent

interface properties between Si and SiO_2. Some of the required characteristics of high-k gate dielectrics are listed below.

Material characteristics and process compatibility:

- Thermal stability on Si (section 1.3.3)
- High dielectric constant ($\geq$ 15)
- Large bandgap and barrier heights
- High crystalline temperature (preferably amorphous phase)
- Compatibility with gate electrode material
- Resistant to interfacial layer growth (EOT increase) during thermal processing
- Low lattice mismatch and similar thermal expansion coefficient with Si
- High density to prevent impurity diffusion
- Etchability
- Mass production deposition process capability

Electrical and reliability characteristics:

- Scalable EOT < 10Å
- Low gate leakage current
- Negligible capacitance-voltage (C-V) hysteresis (< 20mV)
- Negligible frequency dispersion
- Density of interface states (D_{it}) comparable to SiO_2
- Mobility comparable to SiO_2 (80-90%)

- Good reliability (no charge trapping, high breakdown voltage, sufficient 10 year lifetime operating voltage, etc…)

1.4 Motivation for ZrO_2 gate dielectric

Past studies on ZrO_2 have focused on its use in optical and mechanical applications, and thus concentrated on a much thicker range of films than required for gate dielectric application (<100Å) [28,29]. Deposition techniques include chemical vapor deposition (CVD) [24,30,31], electron beam evaporation, pulsed laser deposition [32], atomic layer deposition (ALD) [33], RF sputtering, and DC sputtering [29]. More recent studies have focused on ZrO_2 for gate applications and have produced encouraging results, which will be discussed in detail in chapters 2-5.

1.4.1 ZrO_2 material properties

Many of ZrO_2 material properties make it an attractive MOS gate dielectric material as summarized in table 1.2. ZrO_2 has a sufficiently high dielectric constant of around 17-27 [24-25] and is stable in contact with Si [21], which should result in a scalable EOT. ZrO_2's hardness, chemically inert behavior, and durability [32] make it attractive for mechanical applications. Additionally, it has a reported refractive index ranging from 1.84-2.23 [34] and a fairly high density of 5.74 g/cm^3, which may help to prevent impurity diffusion. As for ZrO_2's energy bandgap, it is reportedly 5.8 eV with calculated band offsets of 1.4 eV for electrons and 3.3 eV for holes [35], which should be sufficiently large enough for low gate leakage current. It has a high

melting point of around 2950K. Finally, it was reported that ZrO_2 could be etched with dilute hydrofluoric (HF) solution, which is commonly used in current MOS processing to remove SiO_2 [25].

Material property	ZrO_2	SiO_2
Dielectric constant	17 - 22	3.9
Bandgap	5.8 eV	9.0 eV
Band offset for electrons	1.4 eV	3.5 eV
Band offset for holes	3.3 eV	4.4 eV
Refractive index	1.84 - 2.23	1.46
Density	5.74 g/cm^3	2.27 g/cm^3
Lattice mismatch with (100) Si	2.1%	–
Thermal expansion coefficient	1.2 x 10^{-5} K^{-1}	5.0 x $10^{-7}K^{-1}$
Melting point	~ 2677ºC	~ 1600ºC
Etchability	HF solution	HF solution

Table 1.2 Material properties of ZrO_2 and SiO_2

ZrO_2's lattice parameters a_o, b_o, and c_o are 5.148Å, 5.203Å, and 5.316Å, respectively, which correspond to a lattice mismatch of 5.2%, 4.2%, and 2.1% with silicon [25]. These values indicate that the lowest lattice mismatch, 2.1%, occurs in the (100) plane – the most common silicon orientation used in MOS processing today.

The thermal expansion coefficient of ZrO_2 is ~$1.2x10^{-5}$ K^{-1}, as compared to Si ($2.6x10^{-6}$ K^{-1}) and SiO_2 ($5.0x10^{-7}$ K^{-1}). Both the low lattice mismatch and comparable thermal expansion coefficient with Si will ensure low mechanical stress/strain between the films.

1.5 Outline

Chapter 1 has given an introduction to scaling challenges facing the semiconductor industry in the coming years. The combination of the limits to SiO_2 gate dielectric scaling, the poly depletion, and quantum mechanical effects will force the implementation of high-k gate dielectric materials. Of the high-k materials mentioned, ZrO_2 is a promising candidate since it possesses many of the material characteristics required by high-k gate dielectrics. Chapters 2-5 will investigate ZrO_2 in greater detail in terms of its electrical, material, and reliability characteristics as well as its compatibility with conventional CMOS processing.

Chapter 2 focuses on the process optimization and materials characterization of sputter deposited ZrO_2 films. Initially, platinum (Pt) electrodes are used to evaluate ZrO_2 MOS capacitor (MOSCAP) properties such as EOT scalability, frequency dispersion, C-V hysteresis, and gate leakage current. Interfacial layer composition is described as well.

Chapter 3 discusses the experiments performed on ZrO_2 and nitrogen-incorporated ZrO_2 (ZrO_xN_y) with polysilicon gate electrode. Despite numerous

attempts to optimize the MOSCAP fabrication process, it is discovered that the poly deposition process is not compatible with ZrO_2 or ZrO_xN_y. An explanation for this incompatibility is given.

Chapter 4 details the work performed on both MOSCAPs and MOSFETs using tantalum nitride (TaN) gate electrode. The motivation behind using TaN gate is presented along with MOSCAP and MOSFET characteristics such as C-V, frequency dispersion, C-V hysteresis, J-V, I_d-V_g, I_d-V_d, and mobility.

Chapter 5 investigates two types of nitrogen incorporation into the ZrO_2 gate dielectric: Si surface nitridation prior to ZrO_2 deposition and nitrogen-incorporated ZrO_2 (ZrO_xN_y). Both processes yield improvements such as improved thermal stability and higher breakdown voltage. TaN/ZrO_xN_y and TaN/ZrO_2 MOSFET characteristics such as I_d-V_g, I_d-V_d, and mobility are compared in addition to reliability tests such as time zero dielectric breakdown (tzdb), time dependent dielectric breakdown (tddb), and 10-year lifetime operating voltage. Finally, the effects of high temperature forming gas annealing on MOSCAP and MOSFET characteristics, including mobility, are investigated.

Finally, Chapter 6 summarizes the results yielded by the fabrication and the electrical, materials, and reliability characterization of these ZrO_2 and ZrO_xN_y MOSCAPs and MOSFETs. In addition, suggestions are given for possible future work on ZrO_2 and ZrO_xN_y gate dielectrics.

1.6 References

[1] S. Borkar, "Obeying Moore's Law beyond 0.18 micron," Proceedings of the 13th Annual IEEE International ASIC/SOC Conference, p. 26, 2000.

[2] International Technology Roadmap for Semiconductors, 2001 edition. Semiconductor Industry Association, 2001.

[3] C.-H. Choi, P.R. Chidambaram, R. Khamankar, C.F. Machala, Z. Yu, and R.W. Dutton, "Gate Length Dependent Polysilicon Depletion Effects," IEEE Electron Device Letters, vol. 23, no. 4, p. 224, 2002.

[4] R. Rios, N.D. Arora, and C.-L. Huang, "An Analytic Polysilicon Depletion Effect Model for MOSFET's," IEEE Electron Device Letters, vol. 15, no. 4, p. 129, 1994.

[5] R. Rios, N.D. Arora, C.-L. Huang, N. Khalil, J. Faricelli, and L. Gruber, "A Physical Compact MOSFET Model, Including Quantum Mechanical Effects, for Statistical Circuit Design Applications," International Electron Devices Meeting, IEDM Technical Digest, p. 937, 1995.

[6] R. Rios and N.D. Arora, "Determination of Ultra-thin Gate Oxide Thicknesses for CMOS Structures using Quantum Effects," International Electron Devices Meeting, IEDM Technical Digest, p. 613, 1994.

[7] K. Yang, Y.C. King, and C. Hu, "Quantum Effect in Oxide Thickness Determination from Capacitance Measurement," Technical Digest of Symposium on VLSI Technology, p. 77, 1999.

[8] R.D. Shannon, "Dielectric polarizabilities of ions in oxides and fluorides," Journal of Applied Physics, vol. 73, no. 1, p. 348, 1993.

[9] G.D. Wilk, R.M. Wallace, and J.M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics," Journal of Applied Physics, vol. 15, no. 1, p. 484, 2000.

[10] S. Ezhilvalavan and T. Tseng, "Conduction mechanisms in amorphous and crystalline Ta_2O_5 thin films," Journal of Applied Physics, vol. 83, no. 9, p. 4797, 1998.

[11] J. Vuillod, "Preparation and characterization of plasma enhanced chemical vapor deposited silicon nitride and oxynitride films," Journal of Vacuum Science & Technology A, vol. 5, no. 4, p. 1675, 1987.

[12] J.A. Diniz, P.J. Tatsch, and M.A.A. Pudenzi, "Oxynitride films formed by low energy NO^+ implantation into silicon," Applied Physics Letters, vol. 69, no. 15, p. 2214, 1996.

[13] H. Hwang, W. Ting, D.-L. Kwong, and J.C. Lee, "Electrical and reliability characteristics of ultrathin oxynitride gate dielectric prepared by rapid thermal processing in N_2O," International Electron Devices Meeting, IEDM Technical Digest, p. 421, 1990.

[14] A. Ono, K. Fukasaku, T. Fukuda, N. Ilezawa, K. Imai, and T. Horiuchu, "A 70μm Gate Length CMOS technology with 1.0V Operation," Technical Digest of Symposium on VLSI Technology, p. 14, 2000.

[15] N. Fukushima, K. Abe, M. Izuha, T. Schimizu, and T. Kawakubo, "Epitaxial (Ba,Sr)TiO_3 Capacitors with Extremely High Dielectric Constant for DRAM Applications," International Electron Devices Meeting, IEDM Technical Digest, p. 257, 1997.

[16] R.B. Khamankar, M.A. Kressley, M.R. Visokay, T. Moise, G. Xing, S. Nemoto, Y. Okuno, S.J. Fang, A.M. Wilson, J.F. Gaynor, T.Q. Hurd, D.L. Crenshaw, S. Summerfelt, and L. Colombo, "A Novel BST Storage Capacitor Node Technology Using Platinum Electrodes for Gbit DRAMs," International Electron Devices Meeting, IEDM Technical Digest, p. 245, 1997.

[17] T. Chen, D. Hadad, V. Balu, B. Jiang, S. Kuah, P.C. McIntyre, S.R. Summerfelt, J.M. Anthony, and J.C. Lee, "Ir-Electroded BST Thin Film Capacitors for 1 Giga-bit DRAM Application," International Electron Devices Meeting, IEDM Technical Digest, p. 679, 1996.

[18] Y. Jeon, B.H. Lee, K. Zawadski, W. Qi, A. Lucas, R. Nieh, and J.C. Lee, "Effect of Barrier Layer on the Electrical and Reliability Characteristics of High-k Gate Dielectric films," International Electron Devices Meeting, IEDM Technical Digest, p. 797, 1998.

[19] R. Nieh, "High-k Gate Dielectrics for Future MOS Technology," Master's Thesis. The University of Texas at Austin, 1999.

[20] R. Nieh, W.J. Qi, Y. Jeon, B.H. Lee, A. Lucas, L. Kang, J.C. Lee, M. Gardner, and M. Gilmer, "Nitrogen (N_2) implantation to suppress growth of interfacial oxide in MOCVD BST and sputtered BST films," Materials Research Society Symposium Proceedings Series, vol. 567, p. 521, 1999.

[21] K.J. Hubbard and D.G Schlom, "Thermodynamic stability of binary oxides in contact with silicon," Journal of Materials Research, vol. 11, no. 11, p. 2757, 1996.

[22] B.H. Lee, "Technology Development and Process Integration of Alternative Gate Dielectric Material; Hafnium Oxide," Ph.D. dissertation, The University of Texas at Austin, 2000.

[23] L. Kang, "Study of HfO_2 as a Future Gate Dielectric and Implementation of Polysilicon Electrodes for HfO_2 films," Ph.D. dissertation, The University of Texas at Austin, 2000.

[24] M. Balog, M. Schieber, M. Michman, and S. Patai, "The chemical vapour deposition and characterization of ZrO_2 films from organometallic compounds," Thin Solid Films, vol. 47, p. 109, 1977.

[25] C.S. Hwang and H.J. Kim, "Deposition and characterization of ZrO_2 thin films on silicon substrate by MOCVD," Journal of Materials Research, vol. 8, no. 6, p. 1361, 1993.

[26] G.D. Wilk, R.M. Wallace, and J.M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, vol. 89, no. 10, p. 5243, 2001.

[27] J.S. Suehle, E.M. Vogel, M.D. Edelstein, C.A. Richter, N.V. Nguyen, I. Levin, D.L. Kaiser, H. Wu, and J.B. Bernstein, "Challenges of High-k Gate Dielectrics for Future MOS Devices," 6th International Symposium on Plasma-Induced Damage, p. 90, 2001.

[28] M.A. Cameron and S.M. George, "ZrO_2 film growth by chemical vapor deposition using zirconium tetra-*tert*-butoxide," Thin Solid Films, vol. 348, p. 90, 1999.

[29] W.W. Davison and R.C. Buchanan, "ZrO_2 Thin Films for Packaging and Microelectronics Applications," Advances in Ceramics: Ceramic Substrates and Packages for Electronic Application, vol. 26, p. 513, 1989.

[30] M. Balog, M. Schieber, M. Michman, and S. Patai, "The Characteristics of Growth of Films of Zirconium and Hafnium Oxides (ZrO_2, HfO_2) by Thermal Decomposition of Zirconium and Hafnium β-Diketonate Complexes in the Presence and Absence of Oxygen," Journal of the Electrochemical Society: Solid-state Science and Technology, vol. 126, no. 7, p. 1203, 1979.

[31] M. Balog, M. Schieber, S. Patai, and M. Michman, "Thin Films of Metal oxides on Silicon by Chemical Vapor Deposition with Organometallic Compounds," Journal of Crystal Growth, vol. 17, p. 298, 1972.

[32] A.C. Greenwald, N.M. Kalkhoran, F. Namavar, A.E. Kaloyeros, and I. Stathakos, "Heteroepitaxial Si-ZrO_2-Si by MOCVD," Materials Research Society Symposium Proceedings, vol. 335, p. 123, 1993.

[33] K. Kukli, K. Forsgren, M. Ritala, M. Leskelä, J. Aarik, and A. Hårsta, "Dielectric Properties of Zirconium Oxide Grown by Atomic Layer Deposition from Iodide Precursor," Journal of the Electrochemical Society, vol. 148, p. F227, 2001.

[34] P.J. Martin, R.P. Netterfield, and W.G. Sainty, "Modification of the optical and structural properties of dielectric ZrO_2 films by ion-assisted deposition," Journal of Applied Physics, vol. 55, no. 1, p. 235, 1984.

[35] J. Robertson, E. Riassi, J.-P. Maria, and A.I. Kingon, "Band alignments of high-k dielectrics on Si and Pt," Materials Research Society Symposium Proceedings Series, vol. 592, 1999.

CHAPTER 2

ZrO_2 Process Optimization and Initial MOSCAP (Pt/ZrO_2) characterization

2.1 Motivation

The purpose of this chapter is to describe the preliminary work performed on ZrO_2 gate dielectrics. The results from this chapter will lay the groundwork for the experiments in chapters 3-5. Initially, experiments were performed to optimize the ZrO_2 deposition process in terms of both low EOT and low gate leakage current. These sputter-deposited ZrO_2 films were tested using techniques such as X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), atomic force microscopy (AFM), and X-ray diffraction (XRD) in order to answer questions about the ZrO_2 composition, interfacial layer composition, morphology, and surface roughness.

Platinum (Pt) gate electrodes were used to fabricate MOSCAPs in order to evaluate these ZrO_2 films. Pt was chosen as an evaluation gate electrode for several reasons. First, Pt has a high resistance to corrosion and is thermally stable [1]. Thus, Pt is not prone to reaction with oxygen to form platinum oxide or prone to reaction with the ZrO_2 gate dielectric. Secondly, Pt has a low resistivity and a high melting point (1172ºC) so it can withstand thermal processing [2]. Finally and practically, Pt was readily available, and the clean room had the facilities to deposit and pattern it.

However, it should be noted that Pt gate electrodes are not likely to be used in future MOS technology. First, Pt is a fairly expensive material. Secondly, although Pt is a fairly inert material, it can react with Si at relatively low temperatures (~450ºC) to form platinum silicide (PtSi) [2,3]. Consequently, with only a thin dielectric film separating the two, it is possible that the Pt gate electrode and silicon substrate could react to form PtSi after the high temperature processing necessary for self-aligned MOSFET fabrication. However, MOSCAP processing does not require high temperature annealing after Pt gate deposition, so the threat of PtSi formation can be avoided. Thus Pt was an acceptable candidate for an evaluation gate electrode material.

2.2 Process optimization

2.2.1 Pt/ZrO_2/Si MOSCAP process flow and measurement

Pt/ZrO_2/Si MOSCAPs were fabricated using the process flow in table 2.1.

1. Piranha clean
2. Field oxidation ~3500Å at 950ºC
3. Active area patterning (Buffered oxide etch): $5x10^{-5}$ cm^2
4. Piranha clean/HF dip/DI water rinse
5. Zr deposition ~20-40Å: DC magnetron sputtering
6. Post deposition anneal (PDA)
7. Pt deposition ~1500Å: DC magnetron sputtering
8. Pt electrode patterning (aqua regia)
9. Post-Pt anneal
10. Backside aluminum deposition

Table 2.1 Pt/ZrO_2/Si MOSCAP fabrication process

The starting materials were (100) p-type silicon wafers with a resistivity of ~5-25 Ω-cm. A 3500Å wet field oxidation was performed in conventional MRL furnaces at 950ºC. Wafers were then 1:1 contact patterned and etched using buffered oxide etch (BOE) to form the active areas of the capacitors ($5x10^{-5}$ cm^2). Immediately prior to Zr deposition, the active patterned wafers were piranha cleaned, dipped in HF solution (1:40, HF:H_2O), and rinsed in deionized (DI) water.

Both Zr and Pt were deposited using a Kurt J. Lesker sputtering machine with a base pressure $\leq 5.0x10^{-7}$ Torr. Around 20-40Å of Zr was deposited via DC magnetron sputtering of a four inch Zr (99.9%) target. The optimized ZrO_2 deposition conditions were a sputtering power of 200W, an argon (Ar) ambient at 30 mTorr, and temperature of ~25ºC. The deposition rate was approximately 120Å of ZrO_2 per minute. Section 2.2.3 will explain how these conditions were chosen.

Post deposition annealing (PDA) served to fully oxidize and densify the ZrO_2, and was performed in either a conventional furnace or a rapid thermal process (RTP) at temperatures ranging from 500-900ºC in nitrogen at atmospheric pressure. Some samples were also annealed after Pt deposition using similar conditions as the PDA. Pt was deposited using DC magnetron sputtering at 300ºC at an Ar pressure of 20 mTorr. Pt was wet-etched using aqua regia (H_2O:HCL:HNO_3, 5:7:1) at 80ºC. Aluminum was deposited on the wafer backside to improve the contact during measurements. ZrO_2 thickness was measured both before and after PDA using a single wavelength ellipsometer with the refractive index (n) fixed at 2.0 for thin films

(≤ 60Å). For thicker films, the ellipsometer iterated n to be ~ 1.9-2.0, which agreed with reported values [4,5].

MOSCAP capacitance-voltage (C-V) characteristics were measured using a HP 4194A Impedance/Gain-Phase Analyzer, and leakage current density-voltage (J-V) characteristics were measured using a HP 4156 Precision Semiconductor Parameter Analyzer. J-V measurements were performed by sweeping the MOSCAP gate voltage from 0V to -3V. Then, to prevent any stress-induced leakage effects, gate voltage was swept from 0V to +3V on a different device nearby. For J-V measurements, the optic lights were kept on to provide minority carriers. For all other measurements, the lights were turned off.

Capacitance equivalent thickness (CET) was calculated from the accumulation capacitance (C_A) of 1 MHz C-V curves using equation 2.1 where A is capacitor area ($5x10^{-5}$ cm^2); k is the dielectric constant of SiO_2 (3.9), and ε_o is the permittivity of free space (8.85 x 10^{-14} F/cm).

$$CET = (k\varepsilon_o A)/C_A \qquad (2.1)$$

The equivalent oxide thickness (EOT) was determined by deducting the quantum mechanical effect (~2Å) from the CET using the NCSU CVC program [6]; the term EOT will be used throughout this dissertation and implies the quantum mechanical deduction. As for material characterization techniques, XPS was used to analyze the ZrO_2 and interfacial layer (IL) film composition. TEM was used to investigate ZrO_2 and IL thickness, AFM for ZrO_2 surface roughness, and XRD for ZrO_2 crystallinity.

2.2.2 Oxidation of Zr [7]

One of the most interesting results was the oxidation of the Zr films during the post deposition anneal (PDA) in N_2 ambient. The oxidation could be attributed to two factors. The first factor was that oxygen adsorbs onto the Zr film from the air, and thus the top layers of Zr films could react with this oxygen to form ZrO_2 [8]. The second factor was the presence of residual oxygen in the RTP chamber or furnace during the PDA. Despite the fact that only N_2 was flowing during PDA, both the RTP and furnace were atmospheric pressure systems, so it was impossible to remove all traces of oxygen. The residual oxygen could easily diffuse through the ZrO_2 during the PDA to oxidize the remaining Zr, and finally the Si substrate as well [9].

X-ray photoelectron spectroscopy (XPS) data (figure 2.1) confirmed that thin Zr films (~20-40Å) could form ZrO_2 when exposed to air at room temperature. Figure 2.1 shows sputter-deposited Zr films of varying thickness that have been brought into atmosphere, but have not been annealed. As shown, all three films were at least partially oxidized because they all show distinct ZrO_2 chemical bonding energy peaks. Films with an original Zr thickness of 20Å show no signs of a Zr binding energy peak, indicating that they were fully oxidized upon exposure to air. However, thicker Zr films (~30-40Å) were only partially oxidized, and still show a small Zr peak. Thus, the PDA served to fully oxidize and densify the ZrO_2 film.

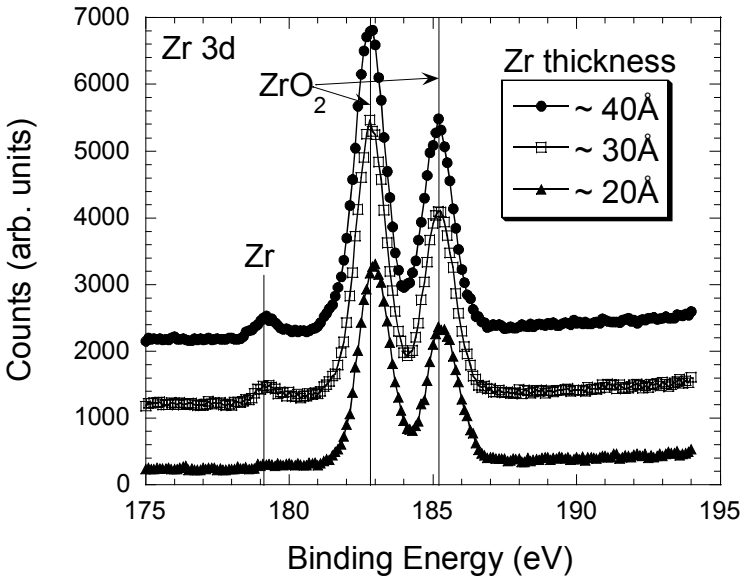

Figure 2.1 XPS data from three Zr films (~20-40Å) that have been oxidized by exposure to air at room temperature [7].

2.2.3 Zr deposition process optimization

The Zr deposition parameters were optimized in terms of temperature, ambient, target power, and deposition pressure in order to yield ZrO_2 films with low EOT and low leakage current. Deposition temperatures ranging from room temperature (~25ºC) to 500ºC were attempted, and it was discovered that the higher the deposition temperature, the higher the EOT. This behavior was attributed to out-gassing of oxygen from the chamber walls at higher temperatures resulting in interfacial layer growth and higher EOT. Figure 2.2 shows that the EOT of ZrO_2 films deposited at 25ºC have lower EOT (~2Å) than those deposited at 300ºC. Thus, room temperature was chosen as the optimal deposition temperature.

As for deposition ambient, Ar-only and Ar + O_2 were investigated. Although past experiments using reactively sputtered ZrO_2 (Ar + O_2 ambient) have yielded good electrical and material characteristics [10], samples sputtered in Ar-only have yielded similar characteristics. In addition, the Ar + O_2 process was less repeatable since the O_2 flow into the chamber was controlled manually in cycles [10]. During each cycle, when the O_2 mass flow controller was initially opened, the pressure increased ~20-40 mTorr before settling back down to its set point value. Also, studies have shown that Si with a thin layer of ZrO_2 on top is particularly vulnerable to plasma anodization, which causes rapid SiO_2 growth at the ZrO_2/Si interface [11], and thus increase in EOT. Consequently, an Ar-only ambient was chosen.

Sputtering target powers ranging from 100-300W were studied. Higher power (300W) resulted in increased sputter damage to the Si substrate, and thus increased leakage current. Low power (100W) had a lower deposition rate, and therefore films were less dense, and also had higher leakage current. Films sputtered at 200W had a high enough deposition rate to yield dense films, and low enough power to minimize sputter damage to the substrate.

Finally, deposition pressures (Ar-only) of 20-40 mTorr were investigated. High pressure (40 mTorr) resulted in lower deposition rates, and thus less dense film, and higher leakage as seen in figure 2.3. A deposition pressure of 30 mTorr yielded slightly lower leakage characteristics than 20 mTorr at PDA temperatures of 600-700ºC (figure 2.3). At 800ºC PDA, samples deposited at 20 mTorr had lower

leakage, but as seen in section 2.2.4, the optimal PDA temperature was ~600ºC. Consequently, 30 mTorr was chosen to be the optimal deposition pressure.

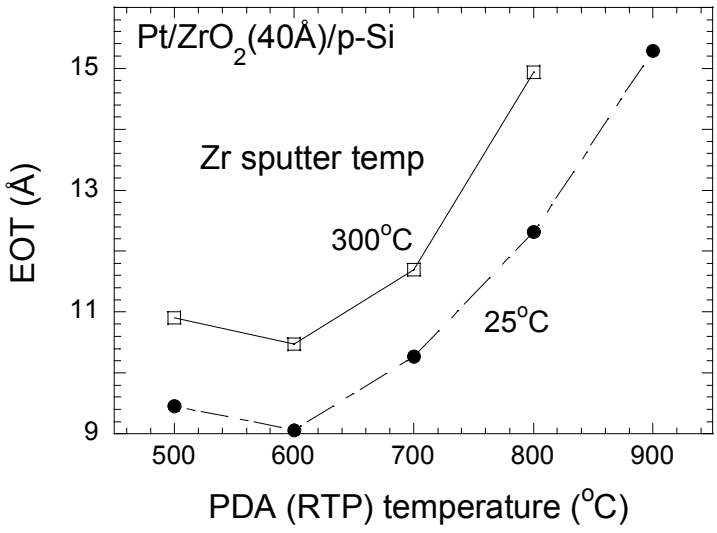

Figure 2.2 EOT versus PDA temperature for ZrO_2 sputtered at 25ºC and 300ºC.

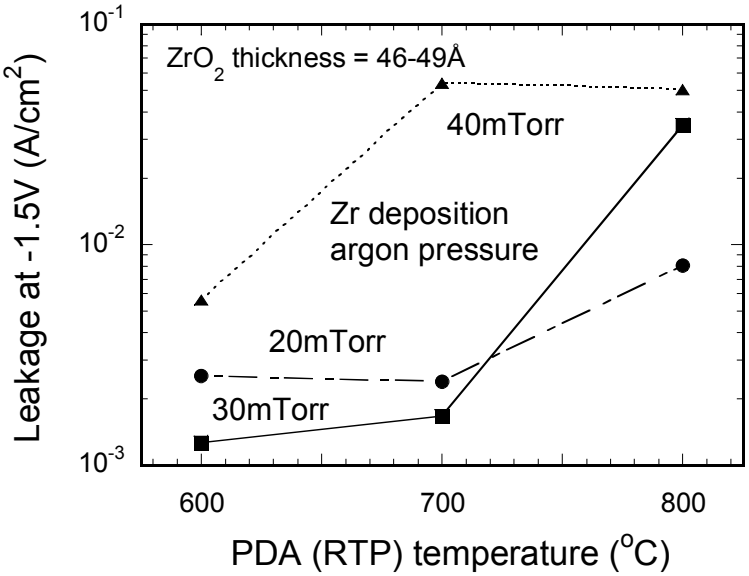

Figure 2.3 Leakage at V_g= -1.5 versus PDA temperature for Zr deposition pressure ranging from 20-40 mTorr.

2.2.4 PDA process optimization

As mentioned earlier, the post deposition anneal (PDA) occurred in either a rapid thermal process (RTP) or a conventional horizontal furnace at temperatures ranging from 500-800ºC in N_2 at atmospheric pressure. Because the furnace was a hot-walled process, the wafers were loaded into an ambient at temperatures ≥ 400ºC. When the wafers were loaded, air (i.e. moisture and O_2) could flow into the furnace, and as a result, the amount of residual oxygen in the furnace was fairly high compared to the RTP system. The RTP system was a cold-walled system, meaning that the wafers were loaded at room temperature, and that the chamber could be purged prior to annealing to remove residual O_2. Therefore, it was not surprising to find that the EOT of RTP annealed samples was lower than that of furnace annealed samples (figure 2.4). Because the RTP was a more controllable process in terms of minimizing residual O_2 and moisture, and thus minimizing EOT and yielding good ZrO_2 film quality, it was chosen as the optimal PDA process.

The next step was to optimize the RTP anneal itself. Figure 2.5 shows the basic steps in a RTP anneal: purge, pre-heat, temperature ramp-up, anneal, and cooling. The variables investigated to attain the optimal PDA conditions were purge time, anneal temperature, and anneal time. It was found that residual oxygen in the RTP chamber contributed to interfacial layer growth and thus increased EOT. As expected, longer N_2 purge (8-10 slm) times lowered the amount of residual O_2 and lowered EOT. As seen in figure 2.6, a 7-minute purge time was sufficient to minimize O_2 in the RTP chamber.

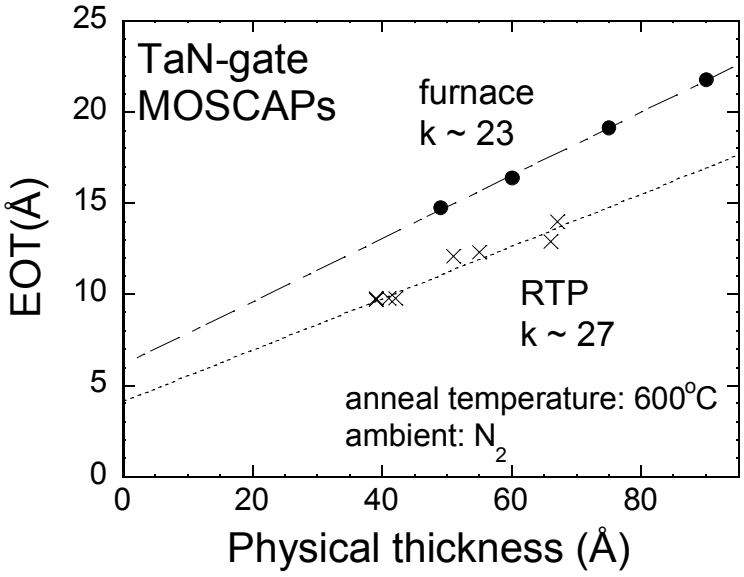

Figure 2.4 EOT versus ZrO_2 physical thickness for furnace and RTP annealed samples.

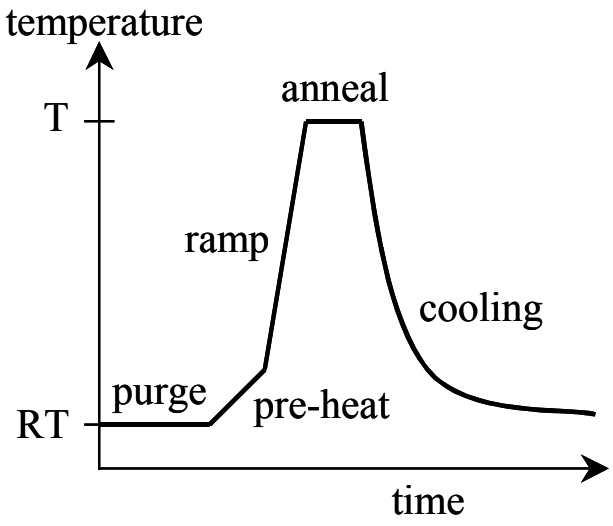

Figure 2.5 Cartoon depiction of a RTP anneal: temperature vs. time.

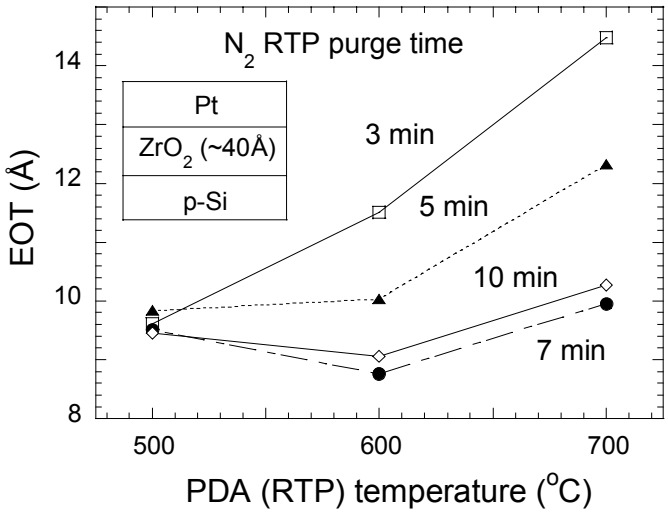

Figure 2.6 EOT versus PDA temperature shows 7-minute purge was sufficient to minimize EOT growth during annealing [7].

Although the residual O_2 was minimized with the 7-minute purge, it could not be removed completely from the RTP chamber. As a result, EOT values increased with increasing PDA annealing temperature (figure 2.7a) and annealing time (figure 2.7b).

In order to maintain both low EOT and low leakage current, PDA (RTP) conditions were set to a purge time of 7 minutes, anneal temperature of 500-600ºC, and anneal time of 10-30 seconds.

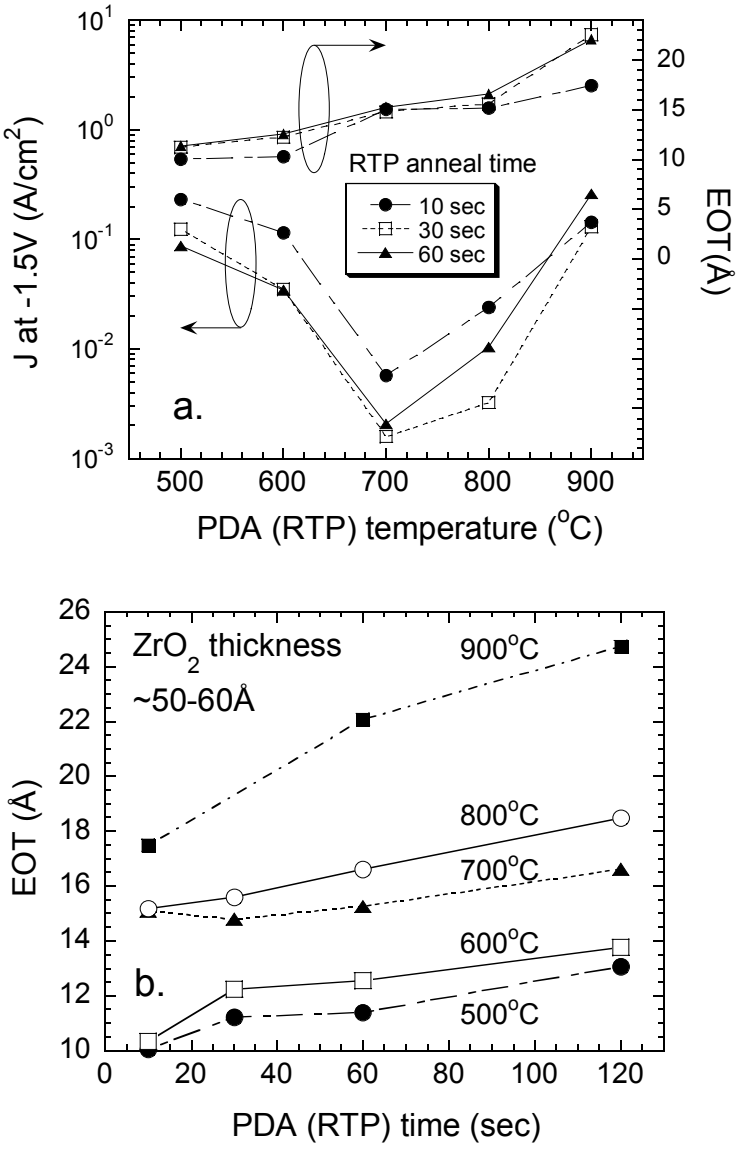

Figure 2.7 (a) Leakage current and EOT vs. PDA temperature shows increasing EOT with increasing temperature [7]. (b) EOT vs. PDA time shows increasing EOT with increasing time and temperature [7].

2.3 Basic ZrO_2 characteristics

2.3.1 Interfacial layer

Although ZrO_2 is thermally stable on Si [12], oxygen can still diffuse through the ZrO_2 to react with the Si to form an interfacial layer (IL). This diffusion can be enhanced by annealing at high temperatures for longer times (figure 2.7). Studies have shown that the growth of this IL can be prevented or controlled by performing the Zr deposition and annealing *in situ* in a vacuum system [13,14]. However, the existence of an IL can be advantageous if it has interface qualities similar to that of SiO_2 on Si. Thus, the IL was investigated in terms of thickness controllability, composition, and morphology.

As discussed in section 2.2.4, optimization of the PDA conditions minimized IL growth. From figure 2.4, the IL grown during RTP PDA had an EOT of ~4Å. One concern was that the wafer clean prior to Zr deposition – piranha, HF dip, DI water rinse – may contribute to the IL since the DI water may leave a monolayer or more of SiO_2 on the Si substrate. This concern was addressed with an experiment that compared a HF-last clean with a DI water-last clean. As shown in figure 2.8, there was no significant difference between the EOT or the leakage current (J) of the HF-last and the DI water-last process. Consequently, the DI water rinse-last clean was adopted since it made the wafers safer to handle than the HF-last clean.

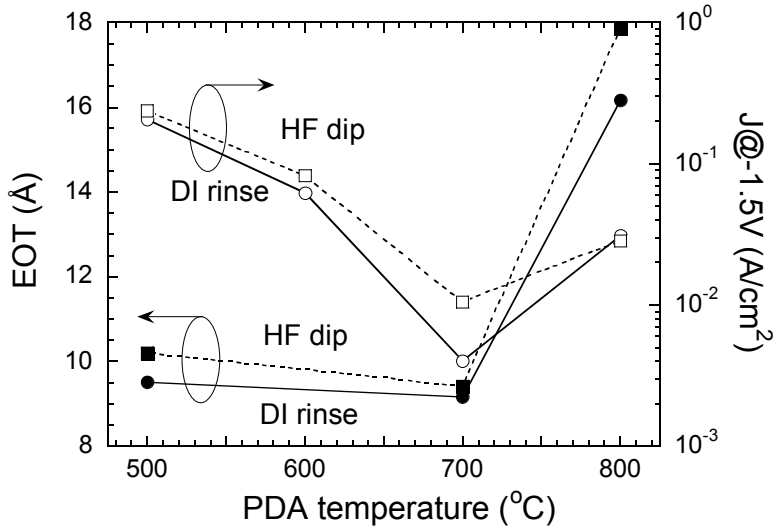

Figure 2.8 EOT and J versus PDA temperature are similar for two different cleans - HF-last and DI water-last.

By controlling the PDA conditions, the IL layer thickness could be controlled, but the IL composition was in question. From XPS data, it can be seen that the IL was not SiO_2, but a $Zr_xSi_yO_z$ or Zr-silicate layer (figure 2.9). As the PDA temperature increased, the composition shifted from a Zr-silicate towards a more stoichiometric SiO_2. TEM pictures confirmed that the IL was a Zr-silicate, and not SiO_2. The TEM in figure 2.10 was taken from a Pt/ZrO_2/p-Si MOSCAP with an EOT of 12.6Å. If a k of 20 is assumed for the ZrO_2 (33Å) layer, the EOT of the ZrO_2 layer is ~6.4Å. Then the k of the IL (11Å) is calculated to be ~7, which is higher than that of SiO_2 (3.9), indicating that the IL must be a Zr-silicate; additionally, the IL was amorphous (figure 2.10). These results have been confirmed in other ZrO_2 studies where the amorphous Zr-silicate IL had a reported k ranging from 5 to 11 [15,16,17].

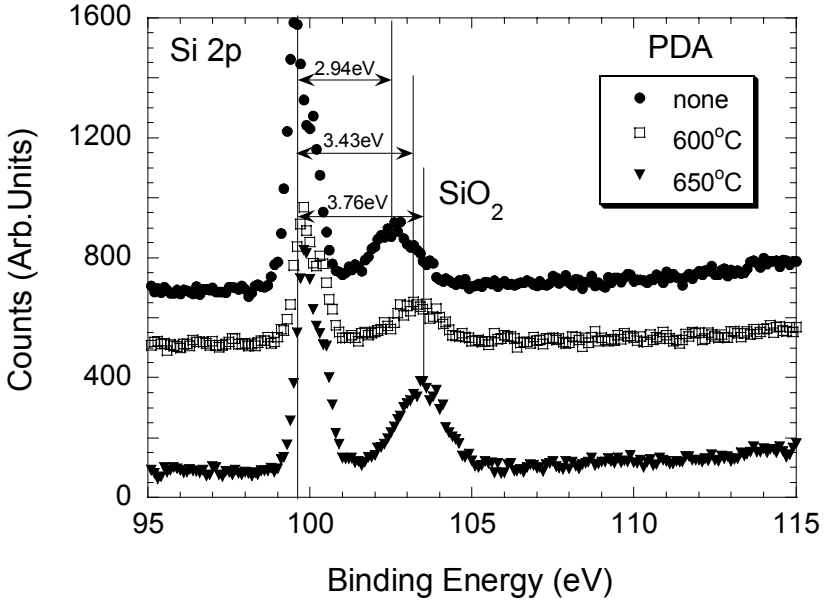

Figure 2.9 XPS spectra show that the IL was a Zr-silicate that converts to more stoichiometric SiO_2 after 650ºC PDA [10].

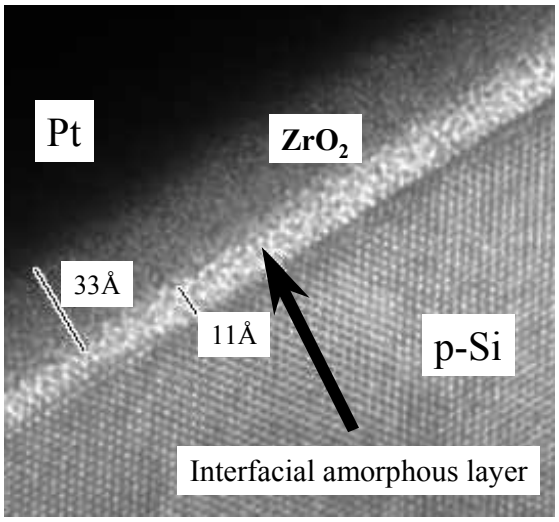

Figure 2.10 TEM of Pt/ZrO_2/Si MOSCAP with EOT of 12.6Å and an amorphous IL composed of Zr-silicate with a dielectric constant of 7.

2.3.2 ZrO_2 materials characteristics

To investigate materials characteristics such as composition, surface roughness, and crystallinity, the ZrO_2 films were subjected to XPS, TEM, AFM, and XRD. XPS data showed that the ZrO_2 films were stoichiometric with Zr:O having a 1:2 ratio. From the TEM in figure 2.10, the ZrO_2 showed smooth interfaces with both the IL/Si substrate and Pt. AFM analysis confirmed that a 50Å-thick ZrO_2 film after PDA was very smooth with a surface roughness value of ~1Å rms (figure 2.11). Other groups have reported similar results with AFM showing surface roughness values of 1-2Å rms [15,18].

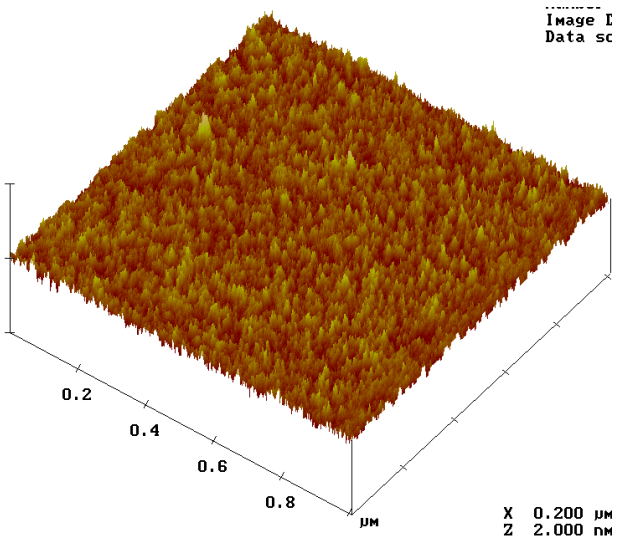

Figure 2.11 AFM picture of ZrO_2 (50Å) after 500ºC PDA shows surface roughness of 1Å (rms).

Film crystallization is a concern for high-k gate dielectrics due to possible issues with leakage current paths or impurity diffusion along grain boundaries. In

addition, non-uniform grain size and orientation of a polycrystalline dielectric may lead to inconsistent characteristics from device to device [19]. Glancing angle XRD analysis of ZrO_2 (100Å) showed signs of film crystallization after 400ºC annealing (figure 2.12). Unfortunately, this crystallization temperature was rather low, although it agreed with other published results [10,20]. However, despite the crystallization, ZrO_2 films yielded low leakage current and consistent electrical characteristics from device to device. ZrO_2 crystallization will be discussed further in section 5.3.2.

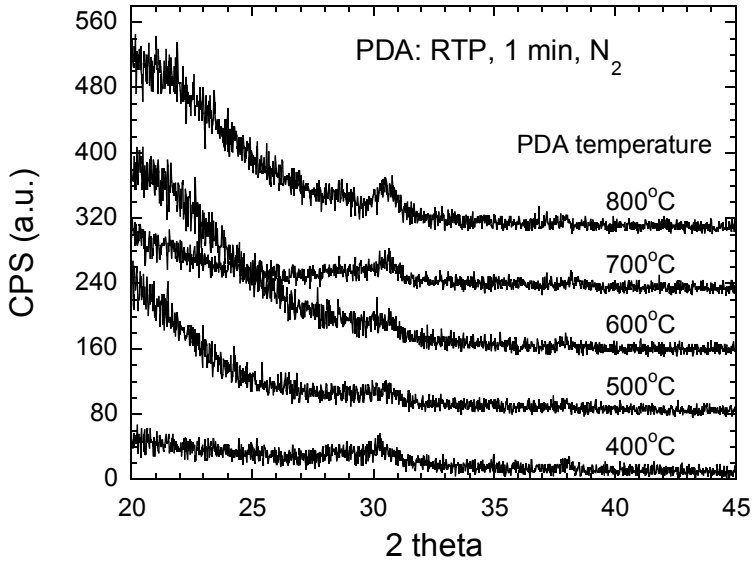

Figure 2.12 XRD analysis of ZrO_2 (100Å) films annealed up to 800ºC show crystallization after 400ºC annealing.

In conclusion, the ZrO_2 films demonstrated stoichiometry, smooth interfaces with the IL/Si and Pt, surface roughness of 1Å rms, and crystallization after 400ºC annealing.

2.3.3 Pt/ZrO_2 MOSCAP characteristics [7]

Overall, the Pr/ZrO_2/Si MOSCAPs produced extremely promising results. The MOSCAPs yielded well behaved C-V curve characteristics and demonstrated EOTs as low as 8.2Å (figure 2.13). Three C-V curves are featured in figure 2.13 to demonstrate the consistent characteristics across the sample. The 8.2Å EOT was calculated from the 1 MHz capacitance at -1.6V; this gate voltage was chosen because capacitance began to increase for voltages lower than -1.6V due to increasing leakage current. This sample had a relatively low leakage current of 2.7×10^{-1} A/cm^2 at a gate voltage of -1.5V and a ZrO_2 physical thickness of ~35Å. The leakage current characteristics were also well behaved as shown in the inset to figure 2.13.

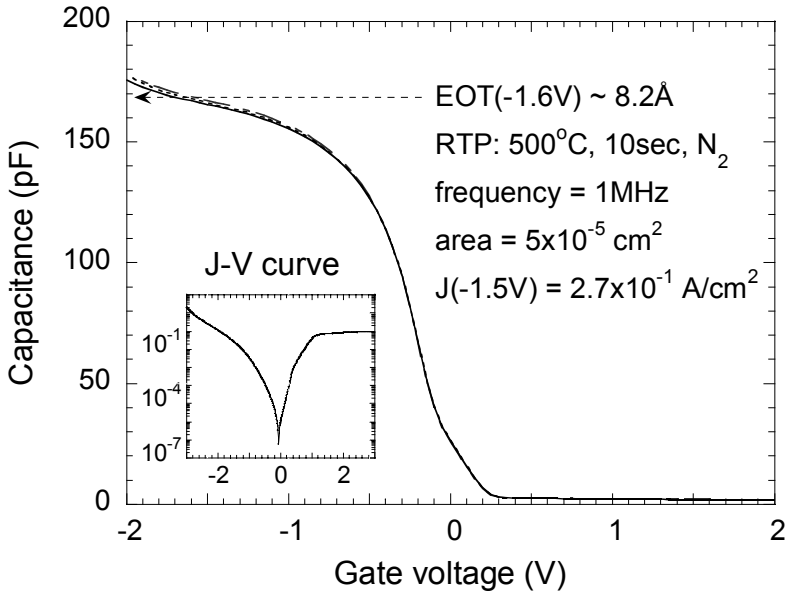

Figure 2.13 C-V curves of Pt/ZrO_2(35Å)/p-Si MOSCAP yielded low EOT (~8.2Å) and low leakage current (2.7×10^{-1} A/cm^2 at V_g= -1.5V) [7].

One concern regarding high-k dielectrics is C-V frequency dispersion, which was not a problem with ZrO_2. Figure 2.14 shows both the capacitance and EOT versus frequency of a Pt/ZrO_2(~48Å)/p-Si capacitor. The EOT only varied from 11.1-11.6Å, and the capacitance varied ~1.3% per decade in the frequency range of 2 kHz to 1 MHz (figure 2.14). The measurement voltage of -1V was chosen so that leakage current would not adversely affect the capacitance values. Leakage at -1V was on the order of $1.4x10^{-4}$ A/cm^2. Other studies have reported negligible ZrO_2 frequency dispersion < 2% per decade [21,10] for frequencies up to 46 GHz [22].

Another concern for high-k gate dielectrics is C-V hysteresis, which results in threshold voltage (V_t) instability. These ZrO_2 films typically exhibited a counterclockwise hysteresis loop as shown in the inset to figure 2.15. Hysteresis was measured from 1 MHz C-V curves by sweeping the gate voltage back and forth from -2V to +2V four times before measuring the change in flat band voltage. Typical hysteresis values were ~ 50-60mV for films with EOT < 11Å. Acceptable hysteresis values are considered to be ≤ 20mV. Hysteresis could be reduced to 20mV with high temperature PDA (800ºC), but at the cost of increased EOT as shown in figure 2.15. It was speculated that hysteresis might partially be due to damage caused by the Pt sputtering process. Post-Pt RTP annealing was performed at temperatures ranging from 500-800ºC in order to cure the sputtering damage. Indeed the post-Pt annealing did reduce hysteresis, but once again with the tradeoff of increased EOT values similar to the trend shown in figure 2.15. C-V hysteresis will be discussed in more detail in section 4.2.2.

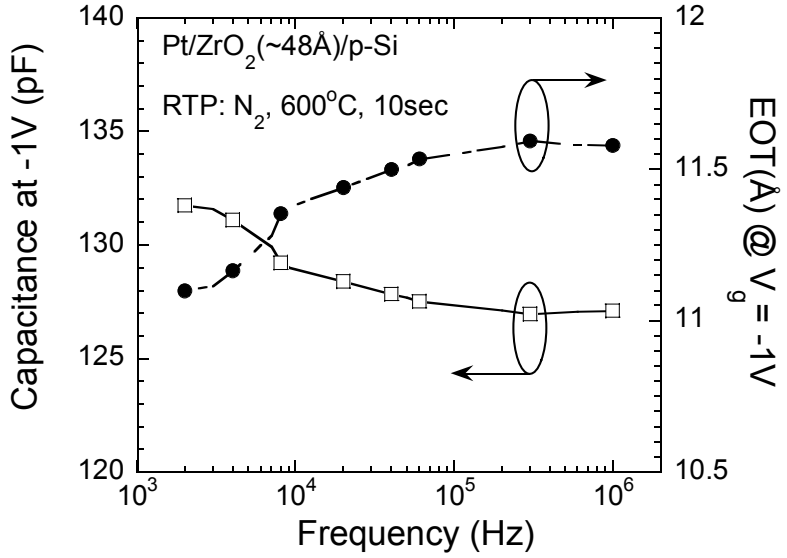

Figure 2.14 Capacitance and EOT at -1V versus C-V frequency of a Pt/ZrO_2(~48Å)/p-Si MOSCAP showed negligible frequency dispersion [7].

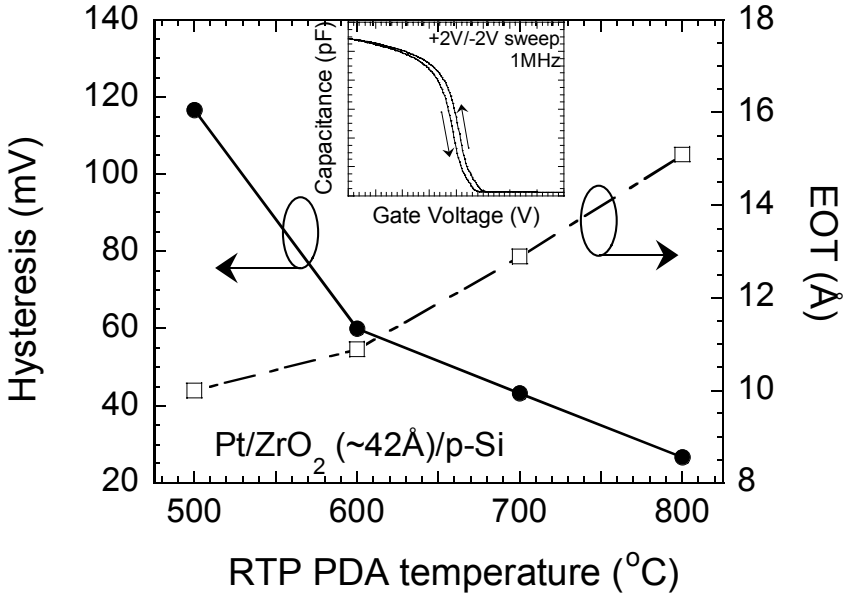

Figure 2.15 C-V Hysteresis decreased while EOT increased with increasing PDA temperature. Inset shows the typical counterclockwise behavior of the C-V hysteresis [7].

As mentioned earlier, leakage current for these RTP-oxidized ZrO_2 films was fairly low. Figure 2.16 shows the trend of leakage current values measured at -1.5V versus EOT of Pt/ZrO_2/p-Si capacitors. The gate voltage (V_g) value of -1.5V was chosen because it approximated a V_g of flat-band voltage minus 1V. Leakage varied for similar EOT values based on processing conditions. As expected, leakage current decreased with increasing PDA annealing temperature as a result of increased IL thickness.

Overall, the Pt/ZrO_2/Si MOSCAP characteristics were well behaved and demonstrated low EOT scalability (~8.2Å), negligible frequency dispersion, manageable hysteresis, and low leakage current.

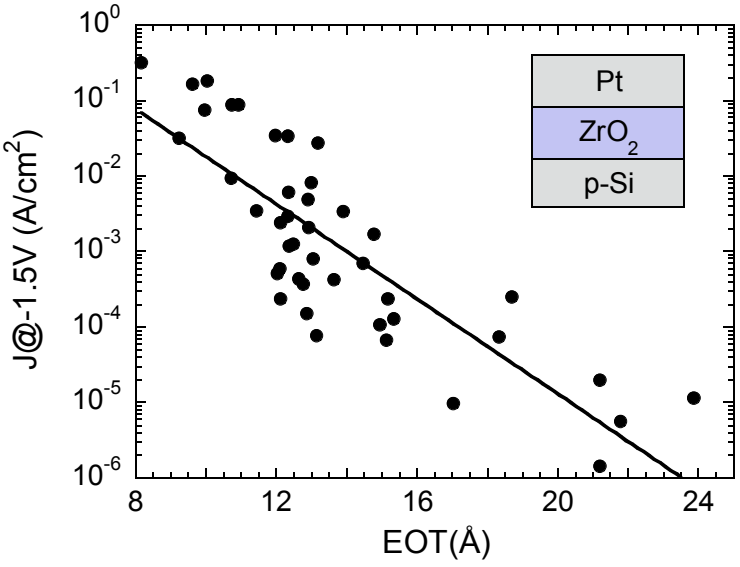

Figure 2.16 Leakage current vs. EOT of Pt/ZrO_2/p-Si MOSCAPs was low.

2.4 Summary

In summary, chapter 2 discussed the optimization of the ZrO_2 process as well as data yielded from the evaluation of Pt-gate MOSCAPs. The Pt/ZrO_2/Si MOSCAP fabrication process was described in detail as well as the material and electrical characterization techniques. It was found that a thin Zr layer could easily be converted to ZrO_2 by exposure to air, followed by further oxidation and densification in a post deposition anneal (PDA). Both the Zr and the PDA procedures were optimized in terms of both low EOT and low leakage current.

Although ZrO_2 was stable on Si, excess exposure to oxygen resulted in interfacial layer growth. This interfacial layer was composed of an amorphous Zr-silicate layer with a dielectric constant ~5-11, whose Zr concentration (and thus k) decreased with high temperature annealing. ZrO_2 exhibited good material properties such as smooth interfaces with both the Pt electrode and Si substrate; ZrO_2 surface roughness was ~1Å rms. XRD analysis revealed that ZrO_2 was already crystallized after 400ºC annealing, although device leakage was low and uniform from device to device.

As for MOSCAP characteristics, EOTs as low as 8.2Å were achieved with low leakage current. C-V characteristics such as dispersion and hysteresis were negligible with the proper process conditions. The leakage current versus EOT trend of ZrO_2 demonstrated encouraging low leakage current. Overall, the results were extremely promising, and ZrO_2 has proven itself a viable candidate for high-k gate

dielectric material. The following chapters will delve deeper into the device and materials characteristics of ZrO_2.

2.5 References

[1] J.H. Kim, S.I. Woo, B.Y. Nam, and W.J. Yoo, "Anisotropic Etching Characteristics of Platinum Electrode for Ferroelectric Capacitor," IEEE Transactions on Electron Devices, vol. 46, no. 5, p. 984, 1999.

[2] C.M. Soriano, "Platinum," IEEE Potentials, vol. 16, no. 5, p. 29, 1998.

[3] S.P. Murarka, "Rapid thermal processing for reproducible formation of the self-aligned silicides of cobalt and platinum," Proceedings of the IEEE/SEMI Advanced Semiconductor Manufacturing Conference, p. 211, 1992.

[4] M.A. Russak, C.V. Jahnes, and E.P. Katz, "Reactive magnetron sputtered zirconium oxide and zirconium silicon oxide," Journal of Vacuum Science & Technology A, vol. 7, no. 3, p. 1248, 1989.

[5] M.A. Cameron and S.M. George, "ZrO_2 film growth by chemical vapor deposition using zirconium tetra-*tert*-butoxide," Thin Solid Films, vol. 348, p. 90, 1999.

[6] J.R. Hauser and K. Ahmed, *Characterization and Metrology for ULSI Technology*, (AIP, New York, 1998), p. 235.

[7] R. Nieh, W.J. Qi, B.H. Lee, L. Kang, Y. Jeon, K. Onishi, S. Gopalan, C.S. Kang, E. Dharmarajan, R. Choi, and J.C. Lee, "Processing effects and electrical characterization of ZrO_2 formed by the RTP oxidation of Zr," Proceedings of the 5th International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues Session of the 197th Electrochemical Society Meeting, p. 214, 2000.

[8] E.E. Khawaja, F. Bouamrane, A.B. Hallak, M.A. Daous, and M.A. Salim, "Observation of oxygen enrichment in zirconium oxide films," Journal of Vacuum Science & Technology A, vol. 11, no. 3, p. 580, 1993.

[9] B.W. Busch, W.H. Schulte, E. Garfunkel, T. Gustafsson, W.-J. Qi, R. Nieh, and J.C. Lee, "Oxygen exchange and transport in thin zirconia films on Si(100)," Physical Review B, vol. 62, no. 20, p. R13290, 2000.

[10] W.J. Qi, "Study on High-k Dielectrics as Alternative Gate Insulators for 0.1μm and Beyond ULSI Applications," Ph.D. dissertation, The University of Texas at Austin, 2000.

[11] B. Pelloie, J. Perriere, J. Siejka, P. Debenest, A. Straboni, and B. Vuillermoz, "Investigation of ionic transport mechanisms during plasma anodization of Si and Si through ZrO_2," Journal of Applied Physics, vol. 63, no. 8, p. 2620, 1988.

[12] K.J. Hubbard and D.G Schlom, "Thermodynamic stability of binary oxides in contact with silicon," Journal of Materials Research, vol. 11, no. 11, p. 2757, 1996.

[13] J.-P. Maria, D. Wicaksana, A.I. Kingon, B. Busch, H. Schulte, E. Garfunkel, and T. Gustafsson, "High temperature stability in lanthanum and zirconia-based gate dielectrics," Journal of Applied Physics, vol. 90, no. 7, p. 3476, 2001.

[14] H. Watanabe, "Interface engineering of a $ZrO_2/SiO_2/Si$ layered structure by *in situ* reoxidation and its oxygen-pressure-dependent thermal stability," Applied Physics Letters, vol. 78, no. 24, p. 3803, 2001.

[15] J.P. Chang and Y.-S. Lin, "Dielectric properties and conduction mechanism of ultrathin zirconium oxide films," Applied Physics Letters, vol. 79, no. 22, p. 3666, 2001.

[16] B.-O. Cho, J. Wang, L. Sha, and J.P. Chang, "Tuning the electrical properties of zirconium oxide thin films," Applied Physics Letters, vol. 80, no. 6, p. 1052, 2002.

[17] T.P. Ma, "High-k Gate Dielectrics for Scaled CMOS Technology," Proceedings of the 6^{th} International Conference on Solid-State and Integrated Circuit Technology, p. 297, 2001.

[18] J.P. Chang, Y.-S. Lin, and K. Chu, "Rapid thermal chemical vapor deposition of zirconium oxide for metal-oxide-semiconductor field effect transistor application," Journal of Vacuum Science & Technology B, vol. 19, no. 5, p. 1782, 2001.

[19] G.D. Wilk, R.M. Wallace, and J.M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, vol. 89, no. 10, p. 5243, 2001.

[20] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo, and A. Nishiyama, "Thermally Stable Ultra-Thin Nitrogen Incorporated ZrO_2 Gate Dielectric Prepared by Low Temperature Oxidation of ZrN," International Electron Devices Meeting, IEDM Technical Digest, p. 459, 2001.

[21] S. Ramanathan, D.A. Muller, G.D. Wilk, C.M. Park, and P.C. McIntyre, "Effect of oxygen stoichiometry on the electrical properties of zirconia gate dielectrics," Applied Physics Letters, vol. 79, no. 20, p. 3311, 2001.

[22] D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, A. Murthy, B. Roberds, P. Stokley, and R. Chau, "High-Frequency response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 231, 2001.

CHAPTER 3

Polysilicon gate electrode on ZrO_2

3.1 Motivation

The purpose of this chapter is to present the experiments performed on ZrO_2 with polysilicon (poly) gate electrodes as well as to explain the results. As discussed in chapter 1, the poly depletion effect will eventually force the replacement of poly gate with dual metal gate electrodes. However, such a drastic change in the current MOS process will require much time and expense. In addition, due to the process complexity, industry will be hesitant to implement the change to metal gate during the same generation as the groundbreaking switch from SiO_2 to high-k gate dielectric. Consequently, industry would like to continue using poly electrodes for as many device generations as possible before switching to metal gates. Thus a high-k gate dielectric material that is compatible with poly gate is highly desirable.

Several high-k materials have demonstrated a compatibility with the poly gate process including Al_2O_3, Hf-silicate, and HfO_2 [1]. Al_2O_3 has been integrated into poly/Al_2O_3/poly devices for DRAM storage capacitor application yielding capacitance equivalent thickness (CET) as low as 28Å with good time-dependent dielectric breakdown (tddb) characteristics [2]. In addition, Al_2O_3 has been integrated into a conventional CMOS process to yield MOSFETs with EOT of 12Å and low leakage [3] as well as vertical replacement gate MOSFETs with EOT of 16Å [4]. The

main drawbacks to Al_2O_3 gate dielectric are its relatively low dielectric constant ~10-11 and the high levels of fixed charge in the film [3].

Hf-silicate and HfO_2 with poly gate electrodes have also demonstrated good device characteristics. Hf-silicate films have shown clear, smooth interfaces with poly gates and yielded well-behaved MOSFET characteristics with EOT of 14Å [5]. HfO_2 has also been integrated into conventional self-aligned poly gate MOSFETs and has exhibited low EOT (~10.4Å), low leakage current, negligible C-V hysteresis, and good MOSFET characteristics [6,7,8]. In addition, these poly/HfO_2 MOSFETs have shown excellent reliability such as negligible charge trapping and stress induced leakage current (SILC) [8], high 10-year lifetime operating voltages ~2.0-2.8V [9,10], and sufficient immunity to negative bias temperature instability (NBTI) [11].

With such encouraging results from Al_2O_3, Hf-silicate, and HfO_2 gate dielectrics, one might expect ZrO_2 to exhibit similar characteristics. After all, like Al_2O_3, Hf-silicate, and HfO_2, ZrO_2 is thermally stable on Si, and ZrO_2 shares many similar material properties with HfO_2. However, the results yielded from the following experiments led to the unfortunate conclusion that ZrO_2 was not compatible with the polysilicon gate process. This incompatibility will be described and the reasons behind it will be discussed fully.

3.2 Poly/ZrO_2 and Poly/ZrO_xN_y NMOSCAP characteristics

3.2.1 Poly/ZrO_2/Si MOSCAP process flow and measurement

Poly/ZrO_2/Si MOSCAPs were fabricated using the process flow in table 3.1 where steps labeled with a '*' were only performed in some of the process splits.

1. Piranha clean
2. Field oxidation ~3500Å at 950ºC
3. Active area patterning (Buffered oxide etch): $5x10^{-5}$ cm^2
4. Piranha clean/HF dip/DI water rinse
5. Zr deposition: DC magnetron sputtering in Ar
6. * ZrN deposition: DC magnetron sputtering in Ar + N_2
7. Post deposition anneal (PDA)
8. * Si deposition: PVD process
9. * Anneal of PVD Si layer in RTP/ HF dip
10. Poly deposition ~1500-2000Å: LPCVD silane process
11. Poly electrode patterning (wet etch)
12. Phosphorus implant: 30-50 keV, $5x10^{15}$ cm^2
13. Activation anneal: RTP, 850-950ºC, N_2, 30-60 seconds
14. Backside aluminum deposition
* step was not performed in every split

Table 3.1 Poly/ZrO_2/Si MOSCAP fabrication process

The first five process steps were identical to those described in section 2.2.1. The ZrN deposition took place immediately after the Zr deposition in the same Kurt J. Lesker sputtering system. ZrN sputtering conditions were a power of 200W, pressure of 30 mTorr, and ambient of Ar and N_2 at room temperature. Post deposition annealing (PDA) occurred in either a furnace or in a rapid thermal process (RTP) at atmospheric pressure and temperatures ranging from 500-800ºC in N_2 or O_2. On some wafers, a layer of sputtered Si (300-500Å) was deposited prior to poly

deposition. This Si was physical vapor deposited (PVD) in the Kurt J. Lesker machine at 100W, 20 mTorr of Ar, at 300-400ºC. This PVD Si layer was densified during a RTP anneal at 600ºC in N_2 for 1 minute. Immediately prior to low pressure chemical vapor deposition (LPCVD) of poly, the wafers were dipped in HF solution to remove any native oxide on the PVD Si layer.

Poly deposition (~2000Å) occurred in a conventional LPCVD process using silane (SiH_4) at temperatures of 550ºC, 580ºC, or 620ºC. Deposition at 550ºC and 580ºC actually yielded amorphous Si (α-Si), which was converted to poly during activation annealing. The poly or α-Si was patterned, wet etched, and then doped with a phosphorus implant at energies ranging from 30-50 keV and a dose of $5x10^{15}$ cm^{-2}. This implant was activated in a RTP anneal at temperatures ranging from 850-950ºC for 30-60 seconds in N_2. Finally, Al was deposited on the wafer backside. Once again, HP 4194 and HP 4156 were used to perform electrical measurements, C-V and J-V, respectively.

3.2.2 ZrO_2 incompatibility with the poly process

Many attempts were made to fabricate poly/ZrO_2 MOSCAPs using the process flow in table 3.1 (without the optional steps), and all yielded extremely leaky capacitors – indicative of an electrical short. Several other groups have reported similar results. Shappir *et al*. studied fairly thick ZrO_2 films ~400Å, and found that by lowering the poly deposition temperature from 620ºC to 550ºC, they could

produce reasonable C-V characteristics [12]. Thus, the poly deposition temperature was lowered to 550ºC in an attempt to prevent the shorting of the poly/ZrO_2 MOSCAPs. Although lowering the poly deposition temperature yielded some reasonable C-V and J-V characteristics, the EOTs were relatively high > 20Å, and J was relatively high ($J > 10^{-3}$ A/cm^2 at V_g= -1.5V).

Shappir *et al*. reported that after the poly deposition, the percentage of oxygen in ZrO_2 decreased from 60% to 40% while the Zr concentration increased from 30% to 40%, indicating that the ZrO_2 films were no longer stoichiometric and were Zr-rich [12]. Because these films became Zr-rich, they were prone to Zr-silicide formation, which explained the high leakage problem [13,14,15]. In addition, Lee *et al*. discovered via XPS analysis, that during poly deposition a SiO_2 layer forms, indicating a reaction between the ZrO_2 and SiH_4 [16]. The formation of a SiO_2 layer helped to explain the high EOT of the poly/ZrO_2 MOSCAPs. However, the cause of the oxygen reduction of the ZrO_2 films was not clear. One speculation was that during poly deposition, the hydrogen from the silane decomposition reacted with the oxygen in the ZrO_2 to form water vapor. Figure 3.1 shows a simplified depiction of how the ZrO_2 was reduced to a Zr-rich film during poly deposition, and how this film reacted with the deposited poly to form Zr-silicide during activation annealing. From Hobbs *et al*., it was reported that the Zr-silicide formation does not happen uniformly across the wafer, but in localized patches or nodes [13]. These areas of silicidation created high leakage paths, which resulted in the shorting of the MOSCAPs.

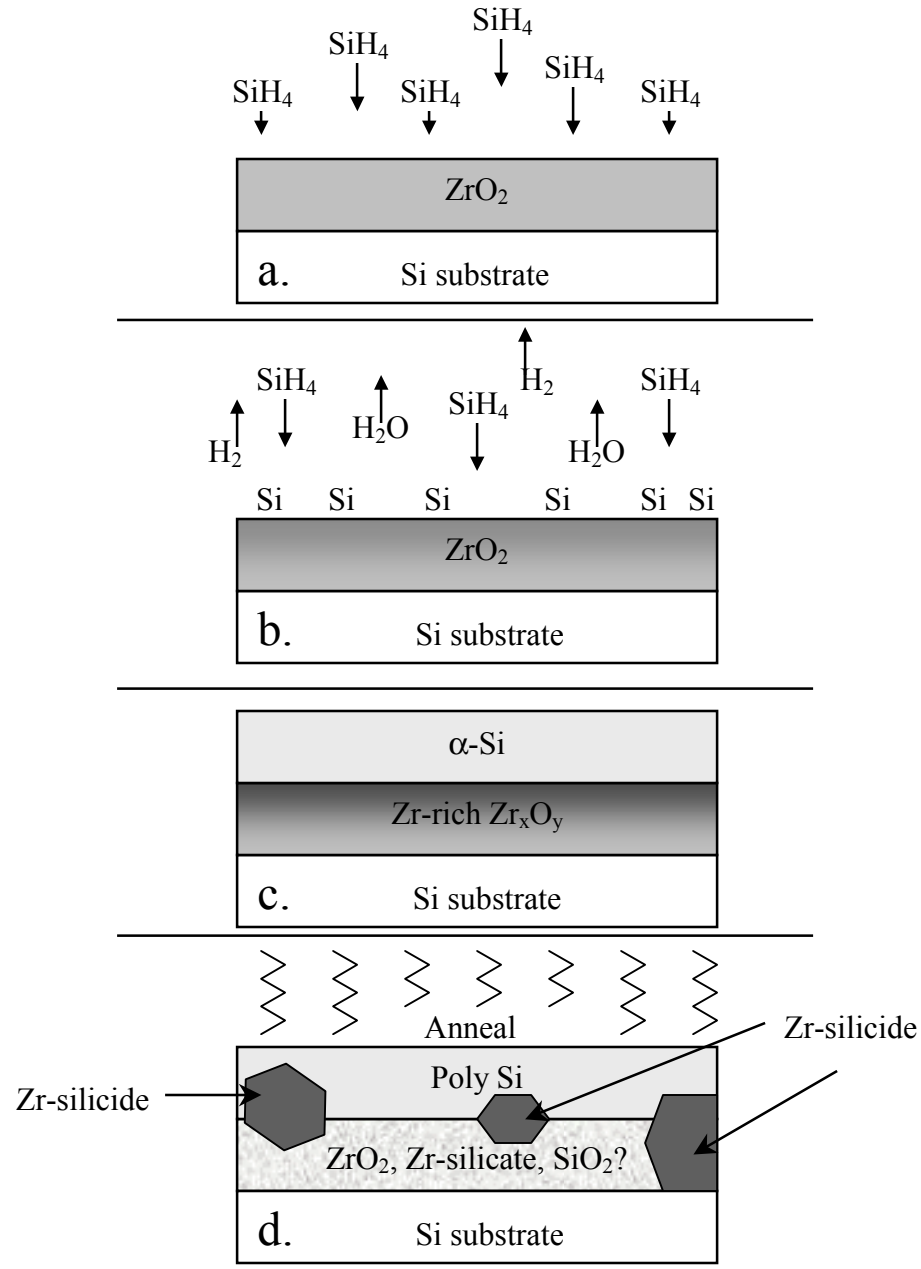

Figure 3.1 (a) At the start of the α-Si deposition process, silane arrives at the ZrO_2 surface. (b) As the α-Si deposition continues, SiH_4 decomposes to Si and H_2. The Si deposits on the ZrO_2 surface while some H_2 reacts with oxygen in the ZrO_2 to form H_2O. Both H_2 and H_2O leave the surface. (c) After α-Si deposition, a Zr-rich dielectric remains. (d) During activation annealing, the α-Si converts to poly and also reacts with the Zr-rich film to form patches of silicide [13]. The remaining dielectric may be a mixture of ZrO_2, Zr-silicate, and SiO_2.

3.2.3 Possible solutions to the incompatibility of ZrO_2 with poly

There were several attempts made to solve the incompatibility problem between ZrO_2 and the poly deposition process. As mentioned earlier, the poly deposition temperature was lowered to 550ºC. ZrO_2 film thickness was increased to ~50-70Å. In addition, the PDA process time was increased from a 10-30 second range to a 5-10 minute range in order to densify the ZrO_2 films so that they might be less prone to reaction and diffusion with H_2. The PDA process was also optimized in order to incorporate more oxygen into the ZrO_2 films by performing the PDA in the furnace, which has more residual oxygen than the RTP system. Also, some anneals were performed in an oxygen ambient. Lastly, the poly implant activation anneal temperature was kept below 950ºC − the higher the temperature, the higher the likelihood of silicidation. Although these solutions helped somewhat, the leakage current in the poly/ZrO_2 MOSCAPs was still too high considering the high EOTs (>20Å). However, the 550ºC α-Si deposition and the optimized PDA conditions were incorporated with the experiments described in this section and 3.2.3.

The next experiment was to try to create a barrier layer of sputter deposited or PVD Si on top of the ZrO_2, to protect it from reaction with the H_2. Approximately 300Å of Si was deposited and annealed for densification prior to LPCVD α-Si deposition. Although some C-Vs were yielded with EOTs ~ 19Å, the MOSCAPs were still leaky as seen in figure 3.2. As the activation temperature increased from 850ºC to 900ºC, the level of silicidation increased and thus leakage also increased

(figure 3.2b). Apparently, H_2 could still diffuse through the PVD Si to react with the ZrO_2 underneath.

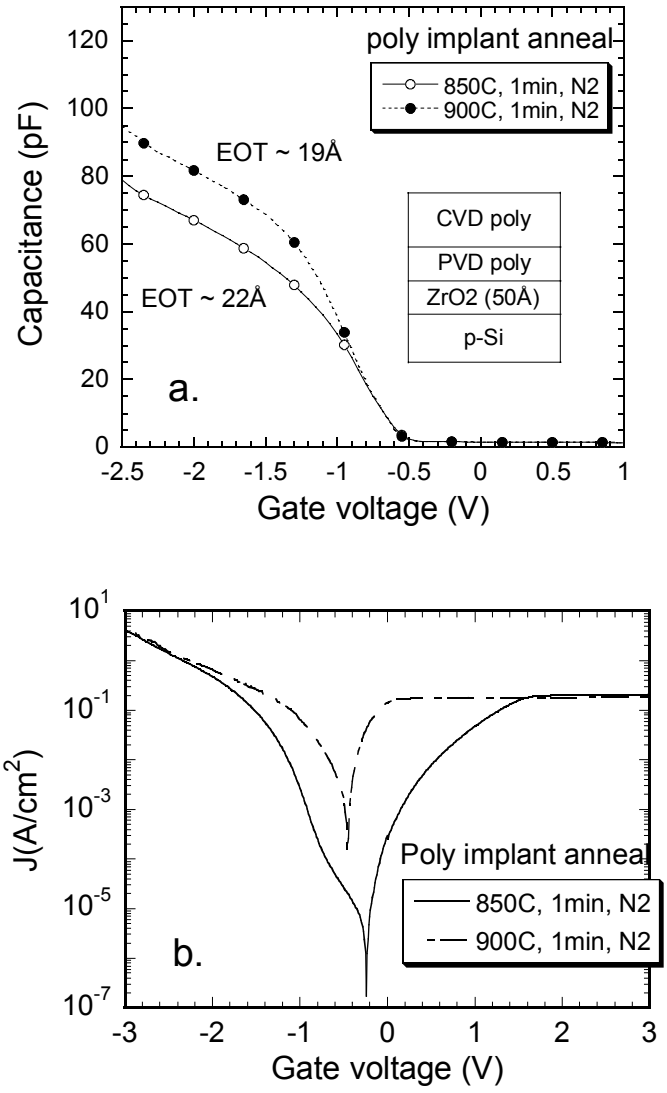

Figure 3.2 (a) C-Vs of a CVD poly/ PVD poly/ ZrO_2 MOSCAPs showed EOT as low as 19Å, but (b) leakage currents were high.

3.2.4 ZrO_xN_y with poly gate [17]

Finally, nitrogen was incorporated into the ZrO_2 film (ZrO_xN_y), in hopes that this would make it less prone to reaction and reduction. ZrO_xN_y films exhibited an improved thermal stability over ZrO_2 films due to decreased diffusion of oxygen through the dielectric during annealing and a more compositionally stable interfacial layer (see section 5.3). It was hoped that this improved immunity to oxygen diffusion might also improve the immunity to the diffusion of the H_2 that was reducing the ZrO_2 films during poly deposition. In addition, Koyama *et. al* reported well behaved C-V curves of poly/ZrO_xN_y with CET of 26.6Å and leakage comparable to gold/ZrO_xN_y MOSCAPs with the same ZrO_xN_y physical thickness of 30Å [18].

Initially, a thin layer (~10-20Å) of ZrO_xN_y was deposited on top of the ZrO_2 (~40-50Å) to form a barrier layer, but it was found that this was not effective enough. Consequently, the ZrO_2 was replaced completely by a ZrO_xN_y layer. Nitrogen was incorporated into the ZrO_2 film by sputtering ZrN in an Ar and N_2 ambient as described in section 3.2.1. The ZrN film was converted to ZrO_xN_y after PDA (see section 5.3.2). For comparison, MOSCAPs with tantalum nitride (TaN) gates were also fabricated using the same process flow except with TaN sputter deposition and RIE patterning (see section 4.2.1) instead of poly gates.

Figure 3.3 shows the C-V curves of a 50Å thick ZrO_xN_y film with TaN gate and poly gate. The TaN gate MOSCAP showed both a lower EOT of 13.6Å, and better C-V saturation characteristics than the poly gate capacitor, which had an EOT of 18.9Å. Thus, the ZrO_xN_y film was not immune to the oxygen reduction during

poly deposition. This fact was further supported by the leakage at V_g= -1.5V versus EOT characteristics shown in figure 3.4. Not only did poly/ZrO_xN_y have higher leakage at the same EOT as TaN/ZrO_xN_y MOSCAPs, but also even higher leakage than poly/SiO_2 MOSCAPs. Finally, high resolution TEM pictures showed evidence of silicide formation in poly/ZrO_xN_y MOSCAPs, whereas TaN/ZrO_xN_y devices showed smooth interfaces (figure 3.5). The poly/ZrO_xN_y MOSCAP shown in figure 3.5 had leakage too high to extrapolate an EOT value, whereas the TaN/ZrO_xN_y device had an EOT of 12.9Å.

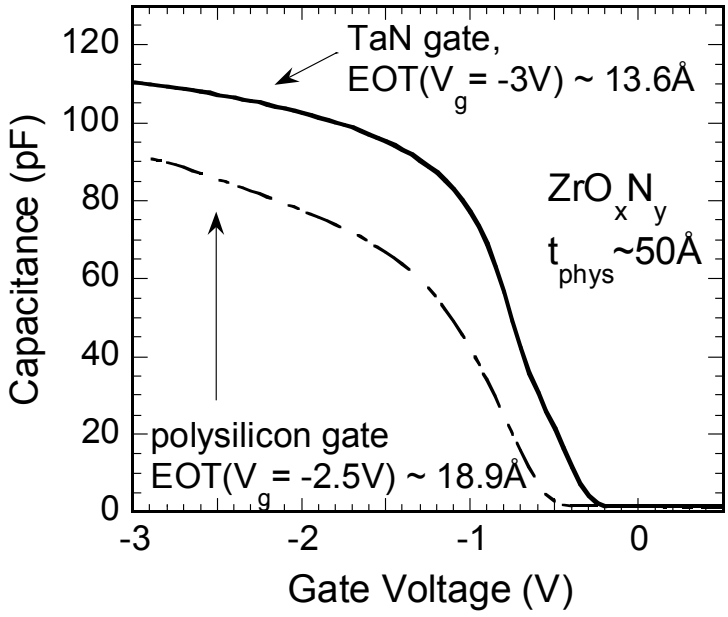

Figure 3.3 C-V curves of ZrO_xN_y (~50Å) with poly gate had higher EOT than TaN gate samples [17].

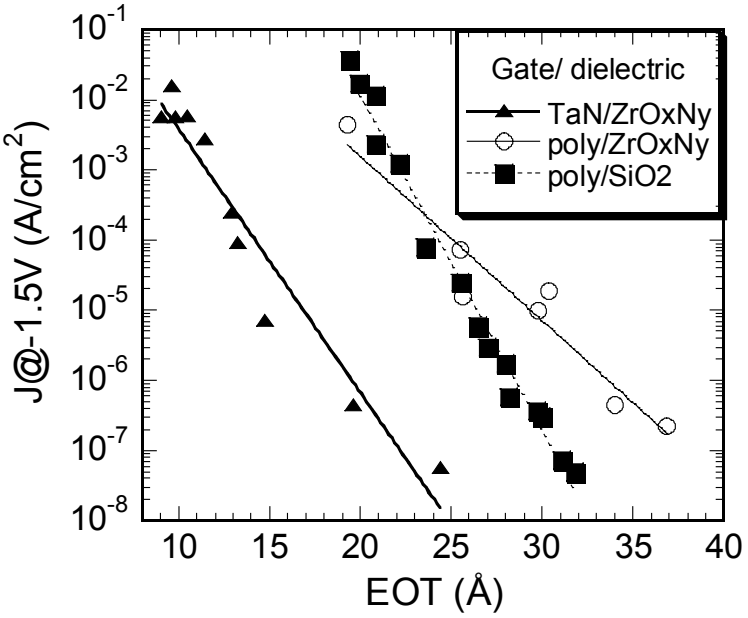

Figure 3.4 J at V_g= -1.5V versus EOT plot shows much lower leakage for TaN gate as compared to poly gate on ZrO_xN_y [17].

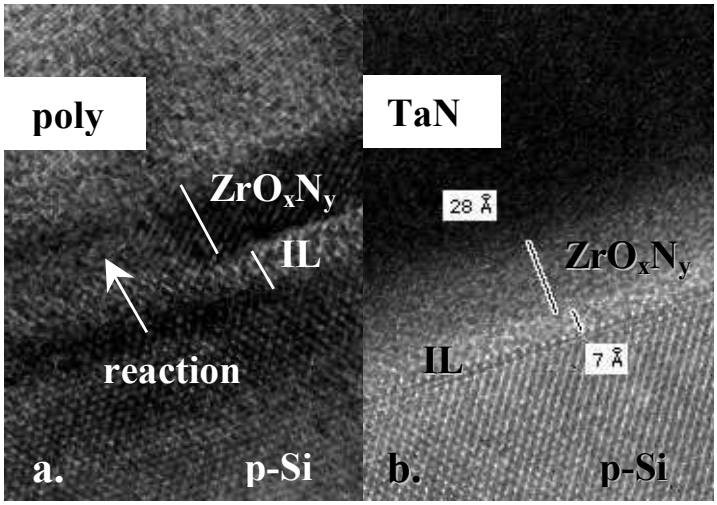

Figure 3.5 TEM pictures show (a) reaction between poly and ZrO_xN_y, and (b) a smooth interface between TaN and ZrO_xN_y [17].

The reasons why these results were different than those reported by Koyama *et. al* are not clear, however they did not report the physical thickness of their devices, or if the leakage characteristics presented were from the same MOSCAPs as the C-Vs presented [18]. Additionally, the level of nitrogen incorporation in their ZrO_xN_y was higher at 5% [18] as compared to 1.7% in the films presented here. This higher level of nitrogen may have been the key to a compatibility with ZrO_xN_y and poly gate. Nevertheless, their reported CETs were fairly thick at 26.6Å [18], while the EOTs achieved in this study were ~18.9Å, which is still too thick for high-k dielectric application.

3.3 Summary

Chapter 3 discussed the incompatibility of ZrO_2 and ZrO_xN_y with the polysilicon gate electrode process. It was speculated that during the LPCVD poly deposition process, H_2 from the silane decomposition stole oxygen from the ZrO_2 film, leaving a Zr-rich film. Poly was deposited on this Zr-rich film, and during high temperature implant activation annealing, the poly and Zr-rich film reacted to form patches of Zr-silicide. The Zr-silicide formation resulted in high leakage current and electrical shorting of the poly/ZrO_2 MOSCAPs.

Several possible solutions were evaluated in order to solve this incompatibility issue. Among them was optimization of the MOSCAP fabrication process including lowering the poly deposition temperature to 550ºC, depositing thicker ZrO_2 films,

increasing the PDA time, and performing the PDA in the furnace with N_2 or O_2 ambient. Additionally, depositing a PVD barrier layer of Si prior to LPCVD α-Si deposition, or a barrier layer of ZrO_xN_y after ZrO_2 deposition was attempted without success. Finally the ZrO_2 was replaced altogether with ZrO_xN_y. Although the poly/ZrO_xN_y MOSCAPs did yield lower EOTs (~18.9Å) than poly/ZrO_2 devices, they still had leakage current that was higher than that of poly/SiO_2 devices [17]. TEM pictures showed clear interaction of poly with the ZrO_xN_y films, whereas devices with TaN electrode had smooth interfaces [17].

While some groups have reported that ZrO_2 can be compatible with poly by using ZrO_xN_y [18] or by using submicron devices where silicidation nodule formation was less likely [13,14,19], no one has reported a consistent, repeatable process which yields EOT < 18Å and low leakage current as compared to poly/SiO_2 devices. Smaller EOTs have been demonstrated, but only with a titanium nitride (TiN) barrier layer between the poly and ZrO_2 [16,20,21], which adds process complexity and defeats the purpose of using poly gate. If the EOT cannot be scaled to at least < 15Å with low leakage, there is no point in trying to implement ZrO_2 with poly gate.

Consequently, when the poly/ZrO_2 MOSCAP process displayed such a narrow process window with high leakage current, it was clear that focus should be turned to implementing ZrO_2 with a more compatible, but also practical gate electrode – tantalum nitride (TaN).

3.4 References

[1] E.P. Gusev, D.A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P.C. Jamison, D.A. Neumayer, M. Copel, M.A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L-A. Ragnarsson, P. Ronsheim, K. Rim, R.J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin high-K gate stacks for advanced CMOS devices," International Electron Devices Meeting, IEDM Technical Digest, p. 451, 2001.

[2] Y.K. Kim, S.M. Lee, I.S. Park, C.S. Park, S.I. Lee, and M.Y. Lee, "Novel poly-Si/Al_2O_3/poly-Si Capacitor for High Density DRAMs," Technical Digest of Symposium on VLSI Technology, p. 52, 1998.

[3] D.A. Buchanan, E.P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M.A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R.J. Fleming, P.C. Jamison, J. Brown, and R. Arndt, "80 nm poly-silicon gated N-FETs with ultra-thin Al_2O_3 gate dielectric for ULSI application," International Electron Devices Meeting, IEDM Technical Digest, p. 223, 2000.

[4] J.M. Hergenrother, G.D. Wilk, T. Nigam, F.P. Klemens, D. Monroe, P.J. Silverman, T.W. Sorsch, B. Busch, M.L. Green, M.R. Baker, T. Boone, M.K. Bude, N.A. Ciampa, E.J. Ferry A.T. Fiory, S.J. Hillenius, D.C. Jacobson, R.W. Johnson, P. Kalavade, R.C. Keller, C.A. King, A. Kornblit, H.W. Krautter, J.T-C Lee, W.M. Mansfield, J.F. Miner, M.D. Morris, S.-H. Oh, J.M. Rosamilia, B.J. Sapjeta, K. Short, K. Steiner, D.A. Muller, P.M. Voyles, J.L. Grazul, E.J. Shero, M.E. Givens, C. Pomarede, M. Mazanec, and C. Werkhoven, "50 nm Vertical Replacement-Gate (VRG) nMOSFETs with ALD HfO_2 and Al_2O_3 Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 51, 2001.

[5] S. Gopalan, K. Onishi, R. Nieh, C.S. Kang, R. Choi, H.-J. Cho, S. Krishnan, and J.C. Lee, "Electrical and physical characteristics of ultrathin hafnium silicate films with polycrystalline silicon and TaN gates," Applied Physics Letters, vol. 80, no. 23, p. 4416, 2002.

[6] L. Kang, K. Onishi, Y. Jeon, B.H. Lee, C.S. Kang, W.-J. Qi, R. Nieh, S. Gopalan, R. Choi, and J.C. Lee, "MOSFET Devices with Polysilicon on Single-Layer HfO_2 High-K Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 35, 2000.

[7] S.J. Lee, H.F. Luan, C.H. Lee, T.S. Jeon, W.P. Bai, Y. Senzaki, D. Roberts, and D.L. Kwong, "Performance and reliability of ultra thin CVD HfO_2 gate dielectrics with dual poly-Si gate electrodes," Technical Digest of Symposium on VLSI Technology, p. 133, 2001.

[8] S.J. Lee, H.F. Luan, W.P. Bai, C.H. Lee, T.S. Jeon, Y. Senzaki, D. Roberts, and D.L. Kwong, "High quality ultra thin CVD HfO_2 gate stack with poly-Si gate electrode," International Electron Devices Meeting, IEDM Technical Digest, p. 31, 2000.

[9] S.J. Lee, C.H. Lee, C.H. Choi, and D.L. Kwong, "Time-dependent dielectric breakdown in poly-Si CVD HfO_2 gate stack," International Reliability Physics Symposium (IRPS) Proceedings, p. 409, 2002.

[10] Q. Lu, H. Takeuchi, R. Lin, T.-J. King, C. Hu, K. Onishi, R. Choi, C.S. Kang, and J.C. Lee, "Hot carrier reliability of n-MOSFET with ultra-thin HfO_2 gate dielectric and poly-Si gate," International Reliability Physics Symposium (IRPS) Proceedings, p. 429, 2002.

[11] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J.C. Lee, "Charging Effects on Reliability of HfO_2 Devices with Polysilicon Gate Electrode," International Reliability Physics Symposium (IRPS) Proceedings, p. 419, 2002.

[12] J. Shappir, A. Anis, and I. Pinsky, "Investigation of MOS Capacitors with Thin ZrO_2 Layers and Various Gate Materials for Advanced DRAM Applications," IEEE Transactions on Electron Devices, vol. ED-33, no. 4, p. 442, 1986.

[13] C. Hobbs, L. Dip, K. Reid, D. Gilmer, R. Hegde, T. Ma, B. Taylor, B. Cheng, S. Samavedam, H. Tseng, D. Weddington, F. Huang, D. Farber, M. Schippers, M. Rendon, L. Prabhu, R. Rai, S. Badchi, J. Conner, S. Backer, F. Dumbuya, J. Locke, D. Workman, and P. Tobin, "Sub-Quarter Micron Si-Gate CMOS with ZrO_2 gate dielectric," Proceedings of International Symposium on VLSI Technology, Systems, and Applications, p. 204, 2001.

[14] Y. Kim, G. Gebara, M. Freiler, J. Barnett, D. Riley, J. Chen, K. Torres, J. Lim, B. Foran, F. Shaapur, A. Agarwal, P. Lysaght, G.A. Brown, C. Young, S. Borthakur, H.-J. Li, B. Nguyen, P. Zeitzoff, G. Bersuker, D. Derro, R. Bergmann, R.W. Murto, A. Hou, H.R. Huff, E. Shero, C. Pomarede, M. Givens, M. Mazanec, and C. Werkhoven, "Conventional n-channel MOSFET devices using single layer HfO_2 and ZrO_2 as high-k gate dielectrics with polysilicon gate electrode," International Electron Devices Meeting, IEDM Technical Digest, p. 455, 2001.

[15] T. Ma, S.A. Campbell, R. Smith, N. Hoilien, B. He, W.L. Gladfelter, C. Hobbs, D. Buchanan, C. Taylor, M. Gribelyuk, M. Tiner, M. Coppel, and J.J. Lee, "Group IVB Metal Oxides High Permittivity Gate Insulators Deposited From Anhydrous Metal Nitrates," IEEE Transactions on Electron Devices, vol. 48, no. 10, p. 2348, 2001.

[16] C.H. Lee, H.F. Luan, W.P Bai, S.J. Lee, T.S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS Characteristics of Ultra Thin Rapid Thermal CVD ZrO_2 and Zr Silicate Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 27, 2000.

[17] R. Nieh, S. Krishnan, H.-J. Cho, C. S. Kang, S. Gopalan, K. Onishi, R. Choi, and J.C. Lee, "Comparison between ultra-thin ZrO_2 and ZrO_xN_y gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices," Technical Digest of Symposium on VLSI Technology, p. 186, 2002.

[18] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo, and A. Nishiyama, "Thermally Stable Ultra-Thin Nitrogen Incorporated ZrO_2 Gate Dielectric Prepared by Low Temperature Oxidation of ZrN," International Electron Devices Meeting, IEDM Technical Digest, p. 459, 2001.

[19] K.-Y. Lim, D.-G. Park, H.-J. Cho, J.-J. Kim, J.-M. Yang, I.-S. Choi, I.-S. Yeo, and J.W. Park, "Electrical characteristics and thermal stability of n^+ polycrystalline-Si/ZrO_2/SiO_2/Si metal-oxide-semiconductor capacitors," Journal of Applied Physics, vol. 91, no. 1, p. 414, 2002.

[20] C.H. Lee, Y.H. Kim, H.F. Luan, S.J. Lee, T.S. Jeon, W.P. Bai, and D.L. Kwong, "MOS Devices with High Quality Ultra Thin CVD ZrO_2 Gate Dielectrics and Self-Aligned TaN and TaN/Poly-Si Gate Electrodes," Technical Digest of Symposium on VLSI Technology, p. 137, 2001.

[21] D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, A. Murthy, B. Roberds, P. Stokley, and R. Chau, "High-Frequency response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 231, 2001.

CHAPTER 4

TaN/ZrO_2 MOSCAP and MOSFET characteristics

4.1 Motivation

This chapter will describe the experiments and results yielded from tantalum nitride (TaN)/ZrO_2 MOSCAP and MOSFET devices. In chapter 3, it was demonstrated that ZrO_2 was not compatible with the polysilicon process. However, as described in section 1.1, the poly depletion effect will force the replacement of poly gates with metal gate electrodes in the coming generations. Although ZrO_2 did not show good characteristics with poly gate, chapter 2 showed that both low EOT scalability and low leakage could be achieved with platinum (Pt) gates. Thus, ZrO_2 may also show good results with other more practical metal gate electrodes. The motivation behind using TaN electrode is that it is one of the more promising candidates for NMOS metal gate electrode. In this section, several metal gate electrode candidates will be presented, including TaN with high-k dielectrics.

There are several advantages and disadvantages to using metal gate over polysilicon gate electrode. Poly gate offers the flexibility of use as gate electrode for both NMOS and PMOS since it can be doped to yield the desired threshold voltage (V_t). In addition, poly gates can withstand high processing temperatures, and work well with the self-aligned MOSFET fabrication process. However, as described in chapter 1, poly gate electrodes will be replaced by metal gate electrodes due to the

increase in EOT (3-7Å) caused by the poly depletion effect [1]. Also, metal gates have the added benefit of lower sheet resistance and decreased boron penetration compared to poly gate. It is essential that these metal gate electrodes be compatible both with the high-k dielectrics as well as CMOS processing. It is possible that a replacement gate process will be used instead of a self-aligned MOSFET fabrication process. In a replacement gate process, the source/drain (S/D) implant and activation anneal are performed prior to gate dielectric and electrode deposition. Thus, the gate dielectric and electrode never face a high temperature (≥ 900ºC) step. However, the replacement gate method adds process complexity and difficulty in proper alignment of the gate to the S/D. Consequently, it is preferred that the metal gate electrodes are able to withstand high temperatures without any reaction with the high-k dielectric or degradation of the metal composition and resistivity.

There are two possible scenarios for the replacement of poly with metal or metal-like gate materials such as conducting metal oxides, metal nitrides, silicides, and metal alloys. The first is to use a metal with a Fermi level at the midgap of the Si substrate such that it can be used for both PMOS and NMOS. However, the V_t of a midgap metal will be ~0.5V, which will be too high for sub-0.13μm CMOS technology where the operating voltage will be ≤ 1.0V [2]. These high V_t values can be lowered by counterdoping the channel, but at the cost of degraded short channel effects [3]. Candidates for midgap metal electrode are titanium nitride (TiN) and tungsten (W). The second option is to replace poly with dual metal gate electrodes –

one metal for PMOS and another for NMOS. The NMOS and PMOS candidates are identified based on their work functions so that their Fermi levels line up accordingly with the conduction and valence bands of Si, respectively. Ideally, the desired work functions for PMOS and NMOS gate electrodes are ~5.17 eV and ~4.05 eV, respectively [4].

Candidates for PMOS metal or metal-like electrodes include Pt, gold (Au), ruthenium oxide (RuO_2), molybdenum (Mo), $Ti_{1-x}Al_xN_y$ (TiAlN), tungsten nitride (WN_x), and ruthenium-tantalum alloy (Ru_xTa_y). These candidates will be described briefly. Both Pt and Au are not likely to be used due to difficulty in etching, poor adhesion, film stress, and high cost [2,5]. RuO_2 has been used for DRAM storage capacitor electrode applications, and more recently as a possible PMOS metal electrode candidate. RuO_2 has demonstrated low resistivity (35-89 μm-cm), thermal stability up to 900°C, resistance to oxygen diffusion, and a compatibility with Zr-silicate and ZrO_2 gate dielectric [5,6]. The work function of RuO_2 was in the acceptable range of PMOS metal gate at 5.04 eV on SiO_2 and 5.10 eV on Zr-silicate and ZrO_2 [5,6]. One serious drawback to RuO_2 was that it formed a toxic and volatile species, RuO_4, if annealed above 900°C in a vacuum or in an ambient containing oxygen [6]. Mo is a candidate for not only PMOS gate electrode, but when implanted with nitrogen its work function can be modulated (~4.03 eV) to be a NMOS gate electrode as well [7]. In addition, Mo has shown compatibility with SiO_2, silicon nitride, Zr-silicate, and ZrO_2 gate dielectrics demonstrating a work function ranging

from 4.76-5.05 eV [7,8,9]. With the correct stoichiometry, TiAlN gates yielded a work function of 5.0-5.2 eV on SiO_2 [10]. In addition, TiAlN was compatible with ZrO_2 and HfO_2 gate dielectrics even after 950°C annealing [10]. Reactively sputtered WN_x electrodes on SiO_2 have been demonstrated and yielded a barrier height of 3.48 ± 0.20 eV [11,12]. However, WN_x films were only thermally stable up to 650ºC annealing [12], and thus could only be adopted in a replacement gate process. Ru-Ta alloys had the flexibility of application for both PMOS and NMOS gate electrode depending on the composition. Ru concentration ≥ 90% in the Ru-Ta alloy resulted in a PMOS work function ~5.2 eV, and Ta concentration ≥ 40% resulted in a NMOS work function ~4.2 eV [13]. On SiO_2, Ru-Ta alloys with Ta concentration ≤ 54% exhibited excellent thermal stability up to 1000ºC, but alloys with Ta concentration > 54% had problems with $TaSi_2$ formation or reaction with the SiO_2 to form Ta_2O_5 [13]. However, since Ta percentage of 40-54% yielded both NMOS work function and thermally stability, Ru-Ta alloys were promising candidates for both NMOS and PMOS gate electrode [13]. Of the PMOS metal gate candidates discussed here, RuO_2, Mo, TiAlN, and Ru-Ta alloys displayed the most promising characteristics, although further investigation of these materials' compatibility with high-k gate dielectrics is necessary.

Candidates for NMOS metal or metal-like electrodes include aluminum (Al), tantalum (Ta), $TaSi_xN_y$ (TaSiN), and TaN. Both Al and Ta have a similar problem in that they easily react to form oxide, Al_2O_3 and Ta_2O_5, respectively [2]. Thus, during

thermal processing both Al and Ta can react with the gate dielectric to form an additional high-k layer in the stack. Also, the formation of Al_2O_3 or Ta_2O_5 from an Al or Ta gate, respectively, leads to higher gate electrode resistivity, which is highly undesirable. TaSiN electrodes have been demonstrated using SiO_2 and HfO_2 gate dielectrics with a thermal stability up to 1000ºC and a work function in the range of 4.19-4.50 eV [10,14,15]. In addition, the TaSiN gate remained amorphous after MOSFET fabrication, minimizing the chance for grain boundary diffusion of dopants or oxygen [15].

Another promising NMOS gate electrode is TaN, which has been demonstrated successfully with SiO_2 [16] and Si_3N_4 [17] as well as various high-k gate dielectrics including Ta_2O_5 [18], HfO_2 [19,20], Hf-silicate [21], Zr-silicate [22], ZrO_2 [23,24], and ZrO_xN_y [24]. Stoichiometric (Ta:N, 1:1) TaN gate electrodes have demonstrated thermal stability and low sheet resistance (20-40 Ω/square) after 1000ºC annealing and a work function of ~4.15 eV [20,23]. Self-aligned TaN-gated MOSFETs using HfO_2 [19] and ZrO_xN_y [24] have demonstrated EOTs as low as 9.3Å and 10.3Å, respectively. Thus, with such encouraging results on TaN, attention was focused on integrating TaN gate electrode with the ZrO_2 gate dielectric described in chapter 2. Chapter 4 will describe the experiments and results yielded from these TaN/ZrO_2 MOSCAP and self-aligned MOSFET devices.

4.2 TaN/ZrO_2 MOSCAP characteristics

4.2.1 TaN/ZrO_2 MOSCAP/MOSFET process flow and measurement

TaN/ZrO_2 MOSCAP/MOSFETs were fabricated using the process flow in table 4.1 where steps labeled with a '*' were only performed in some of the process splits.

1. Piranha clean
2. Field oxidation ~3500Å at 950ºC
3. Active area patterning (Buffered oxide etch)
4. Piranha clean/HF dip/DI water rinse
5. Zr deposition: DC magnetron sputtering in Ar
6. Post deposition anneal (PDA): RTP, 600ºC, N_2, 10-30 seconds
7. TaN deposition ~2000Å: DC sputtering in Ar + N_2
8. TaN patterning (RIE in CF_4)
9. * Post-TaN anneal: RTP, N_2, 500-800°C
10. S/D implant: Phosphorus ($5x10^{15}cm^{-2}$, 50 keV)
11. LTO deposition
12. Contact patterning
13. S/D activation: RTP, 850-950ºC, 30-60 seconds, N_2
14. HF dip, Al deposition
15. Al contact patterning
16. Backside Al deposition
17. Forming gas anneal: 400ºC, 30 minutes
* step was not performed in every split

Table 4.1 $TaN/ZrO_2/Si$ MOSCAP/NMOSFET fabrication process

TaN-gated MOSCAPs with an active area of $5x10^{-5}$ cm^2 were fabricated using steps 1-9 and then step 16 of table 4.1. The first five steps in table 4.1 were identical to those described in section 2.2.1. The post deposition anneal (PDA) in step 6 was a

rapid thermal process (RTP) optimized to yield both low EOT and low leakage current as described in section 2.2.4.

TaN deposition occurred in a Kurt J. Lesker sputtering system with a base pressure $\leq 5.0 \times 10^{-7}$ Torr. TaN was reactively DC sputtered from a 4-inch Ta (99.95%) target in an Ar and N_2 (10 sccm) ambient at 10 mTorr at room temperature. The N_2 flow rate was optimized to yield stoichiometric TaN films as described by B.H. Lee [25]. Ta target power was 1100W, and the TaN sputter rate was ~450Å/min. After deposition, TaN sheet resistance was measured using a four-point probe and was typically in the range of 10-25 Ω/square. The TaN was patterned using 1:1 contact lithography on a Karl Suss aligner and then etched in a reactive ion etch (RIE). The RIE conditions were an ambient of CF_4 (60 sccm), pressure of 30 mTorr, a power of 200W, at room temperature; the etch rate was ~250Å/min. Some MOSCAPs underwent a post-TaN anneal (step 9) in an RTP from 500-800°C.

NMOSFET fabrication with gate width/length of 150μm/5μm continued with steps 10-17 in table 4.1. Wafers were implanted with phosphorus (5×10^{15} cm^{-2}, 50 keV) to form the source/drain (S/D). Next ~1200-1500Å of low temperature oxide (LTO) was deposited in a conventional low pressure chemical vapor deposition (LPCVD) process at 530°C. Contact holes were patterned using 1:1 contact printing on a Karl Suss aligner, and wet-etched using buffered oxide etch (BOE) at a rate ~1000Å/min. Because ZrO_2 was difficult to etch after high temperature annealing, S/D implant activation occurred after the contact etching to ensure that ZrO_2 was

removed from the contact areas. The S/D activation anneal was a RTP in N_2 at either 850-900ºC for 1 minute or 950ºC for 30 seconds. Prior to metallization, the wafers were dipped in hydrofluoric (HF) solution ($HF:H_2O$, 1:60) to remove any native SiO_2 from the contact areas. Aluminum (Al) was deposited in a Varian sputtering machine with a base pressure of $\leq 3.0x10^{-7}$ Torr at room temperature. The sputtering ambient was Ar at 3 mTorr. Al was patterned using 1:1 contact printing on a Karl Suss aligner, and wet-etched at 35ºC using commercial Al etchant at a rate of ~1000Å/min. Finally, Al was deposited on the wafer backside, and the MOSFETs were sintered in a Mini-brute furnace using forming gas at 400ºC for 30 minutes.

ZrO_2 film thickness was measured using a single wavelength ellipsometer as described in section 2.2.1. A HP 4194 was used to measure C-V and C-V hysteresis, where hysteresis was the change in V_{fb} after sweeping the gate voltage back and forth between +2/-2V four times. A HP 4156 was used to measure leakage (J-V) (as described in section 2.2.1), time zero breakdown (tzbd), drain current versus gate voltage (I_d-V_g), and drain current versus drain voltage (I_d-V_d) characteristics.

Mobility (μ_{eff}) was measured using the split C-V method [26] as shown in equation 4.1 where I_d represents drain current; L represents gate length; V_d represents drain voltage; W represents gate width, and Q_i represents inversion charge density.

$$\mu_{eff} = (I_d*L) / (V_d*W*Q_i) \qquad (4.1)$$

The I_d comes from the I_d-V_g characteristics measured at a V_d of 5mV. The W/L for these MOSFETs was 150µm/5µm. Q_i was measured by integrating the area under

inversion C-V curves. Inversion C-V curves were measured by connecting the gate to the high end of the C-V measurement and the S/D to the low end, and tying the substrate to 0V. The effective field (E_{eff}) was calculated using equation 4.2 where η is 0.5 for NMOS; Q_b is the body charge density; ε_{Si} is the dielectric constant of Si (11), and ε_o is the permittivity of free space (8.85×10^{-12} F/m) [26].

$$E_{eff} = (\eta * Q_i + Q_b) / (\varepsilon_{Si} * \varepsilon_o) \qquad (4.2)$$

Q_b was estimated using the substrate doping concentration which was ~3×10^{15} cm^{-3}. The universal electron mobility (μ_n) plot for SiO_2 was calculated using equation 4.3 [26].

$$\mu_n = 630 / [1 + (E_{eff}/0.75)^{1.67}] \qquad (4.3)$$

4.2.2 Evaluation of TaN/ZrO_2 MOSCAP electrical characteristics

Similar to the Pt-gated MOSCAPs presented in section 2.2.3, characteristics such as C-V, EOT scalability, frequency dispersion, leakage, and C-V hysteresis were evaluated. After post-Pt annealing, the Pt-gated MOSCAPs had the problem of Pt-silicide formation and thus shorting of the capacitors, and consequently, the results in chapter 2 did not include much post-Pt annealing. Since the TaN electrodes were thermally stable with the ZrO_2 stack, not only was post-TaN annealing possible, but self-aligned MOSFET fabrication as well. This section will focus on the MOSCAP results.

First, the results from MOSCAPs fabricated on both p-type and n-type Si substrates were evaluated to ensure comparable EOT. Both p-type and n-type Si wafers were of (100) orientation with a resistivity of ~ 5-25 Ω-cm. ZrO_2 films from 45-120Å thick were deposited and annealed (600ºC, RTP) using the same conditions for each substrate. The EOT versus physical thickness plot is shown in figure 4.1 and shows a similar trend for both n-type and p-type substrate. Unfortunately, the PDA process was not optimized for such thick ZrO_2 films, and in addition, the EOT from the thin films (45Å) was 2Å thicker than usual. As a consequence, the extrapolated k values for these films was only ~16, which is smaller than the more typical value ≥ 20 (see figure 2.4). Nevertheless, the main goal of this experiment was to demonstrate comparable characteristics on both n and p-type Si substrates, which was achieved.

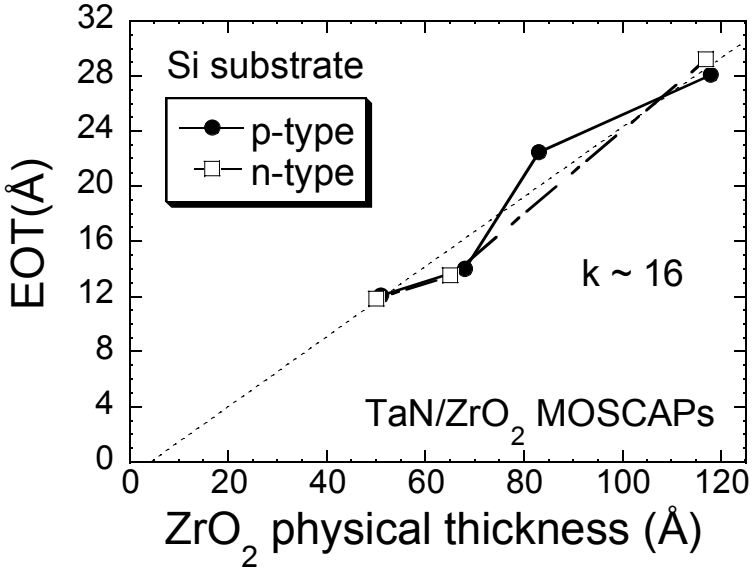

Figure 4.1 TaN/ZrO_2 shows comparable EOT characteristics on both n-type and p-type silicon substrates.

From this point forward, only NMOSCAPs were evaluated. Next, the frequency dispersion characteristics were investigated. Figure 4.2 shows the 100 kHz and 1 MHz C-V curves of a TaN/ZrO_2 (~42Å) MOSCAP, with an EOT of 9.8Å. The two curves show good agreement with the exception of the slight discrepancies near the base of the C-V curve and at gate voltage (V_g) ≤ -2V. However, these discrepancies were not due to frequency dispersion. The hump near the base of the C-V curve was due to slow interface states (D_{it}), and this hump became more pronounced at lower frequency. With proper post-TaN annealing, the D_{it} can be reduced, and this C-V hump becomes less pronounced. At V_g ≤ -2V, the leakage current was higher and thus caused the discrepancy between accumulation capacitances of 100 kHz and 1 MHz curves. Similar to these results, other studies have shown negligible frequency dispersion for ZrO_2, even up to 46 GHz [27].

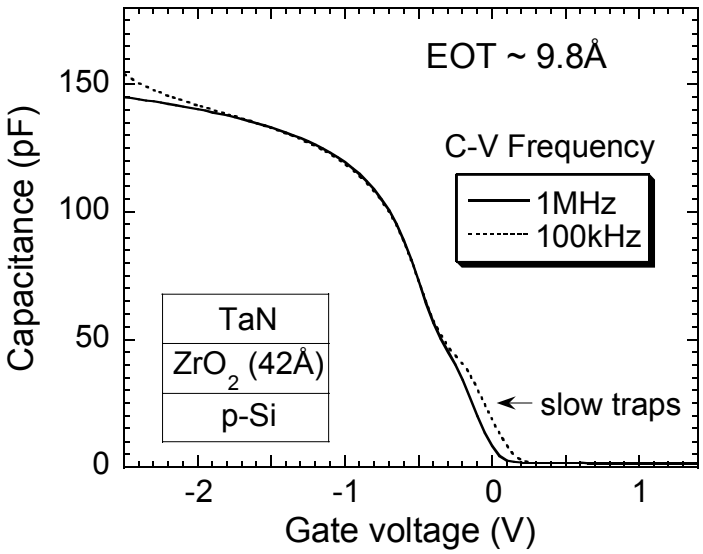

Figure 4.2 C-V curves at 1 MHz and 100 kHz for TaN/ZrO_2 MOSCAPs show good agreement.

The leakage characteristics for these TaN-gated ZrO_2 MOSCAPs were quite similar to that of the Pt-gated MOSCAPs presented in section 2.3.3. Once again, the lights were turned on during leakage measurements to provide minority carriers. Figure 4.3 shows the J-V characteristics for a MOSCAP with EOT of 9.8Å whose C-V characteristics are shown in figure 4.2. This J-V curve was quite typical of the TaN-gated devices with the exception of the breakdown around V_g = -2.7V. This breakdown voltage (V_{bd}) was smaller than the more typical value of -3.0V or higher, which will be seen later in section 4.3.1. The leakage for this MOSCAP was fairly low at $6.6x10^{-3}$ A/cm^2 at V_g = -1.5V. The leakage versus EOT trend for these TaN gated MOSCAPs can be seen later in figure 4.12 where leakage before and after MOSFET fabrication are compared.

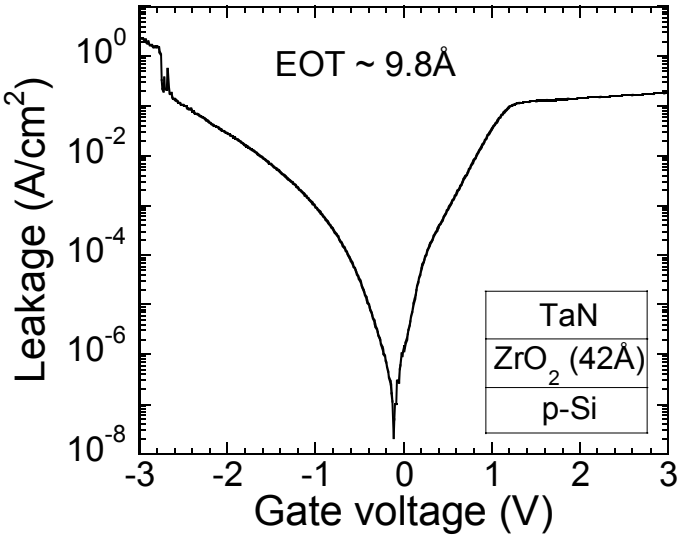

Figure 4.3 J-V curves show typical behavior of TaN-gated ZrO_2 MOSCAPs, with the exception of the low breakdown voltage.

Finally, MOSCAPs with post-TaN annealing were evaluated to determine its effects on C-V characteristics, EOT scalability, and hysteresis. It has been shown that damage caused by Pt sputtering resulted in increased D_{it} in ZrO_2 films [28]. Post-TaN annealing served an important role in reducing the TaN sputtering damage and D_{it}, thus improving the TaN/ZrO_2 interface quality. In addition, post-TaN annealing improved the ZrO_2 film characteristics in terms of reduced trapped charge (Q_{ot}) and reduced fixed charge (Q_f).

Figure 4.4 shows the C-V curves of a TaN/ZrO_2 (42Å) MOSCAP prior to post-TaN annealing, as well as after 700ºC, 800ºC, and 900ºC post-TaN annealing for 30 seconds. Not surprisingly, the capacitance decreased with increasing anneal temperature due to oxygen diffusion that caused interfacial layer (IL) growth. In addition, the higher temperature annealing caused the composition of the IL to shift from a Zr-silicate to a more stoichiometric SiO_2 (see section 2.3.1). The EOT increased from 9.7Å for no anneal to 13.4Å after 900ºC annealing. Also observed was a reduction in the hump near the base of the C-V with higher anneal temperature, indicating a reduction in D_{it}. Finally, there was a negative shift in flat band voltage (V_{fb}) with increasing anneal temperature. It has been reported that ZrO_2 films have negative Q_f, and that this Q_f can be reduced or compensated for during annealing [29]. Thus with higher temperature post-TaN annealing, the negatively charged Q_f was reduced/compensated resulting in a negative shift in V_{fb}. In summary, the post-TaN anneal was successful in decreasing both D_{it} and Q_f.

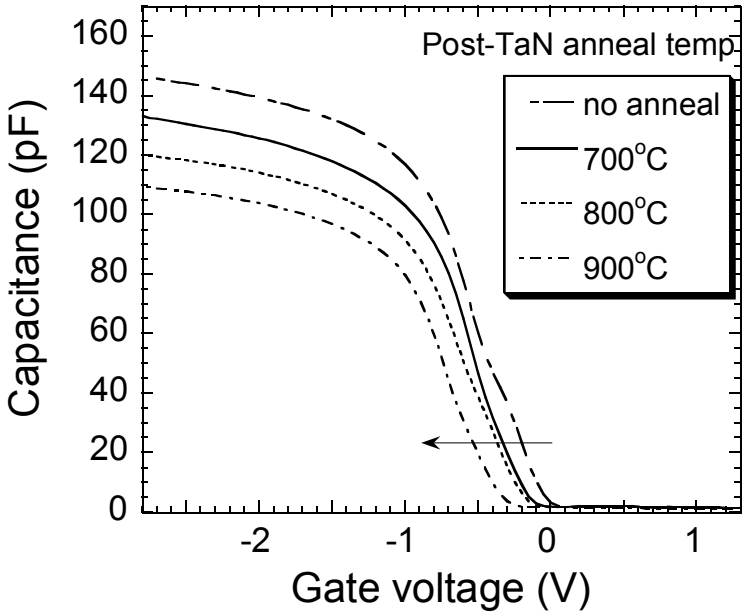

Figure 4.4 C-V after post-TaN annealing shows both reduced capacitance and reduced V_{fb} with increasing anneal temperature.

Next, the C-V hysteresis of these TaN/ZrO_2 MOSCAPs was studied. In gate dielectrics, such as SiO_2 [30], ZrO_2 [31,32,33], and HfO_2 [33], hysteresis is believed to be caused by trapped charge (Q_{ot}), particularly Q_{ot} near the dielectric/Si interface. In these experiments, ZrO_2 yielded a counterclockwise C-V hysteresis loop indicating positively charged Q_{ot} near the ZrO_2/Si interface [31,33].

Figure 4.5 shows both the EOT and hysteresis of the TaN/ZrO_2 (42Å) MOSCAPs after post-TaN annealing. As mentioned, the EOT increased from 9.7Å for samples with no anneal up to 13.4Å after 900ºC annealing due to IL growth and compositional changes. The hysteresis reduced from 113mV for samples with no annealing down to 20mV after 900ºC post-TaN annealing.

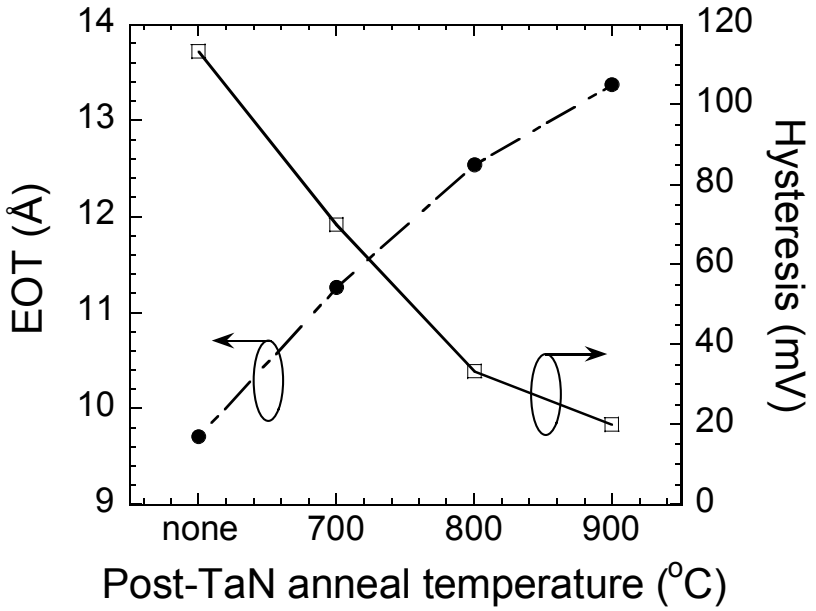

Figure 4.5 TaN/ZrO_2 EOT increases and C-V hysteresis decreases with increased post-TaN anneal temperature.

The reduction in hysteresis was attributed to the reduction of Q_{ot} after post-TaN annealing, and higher temperature annealing resulted in further reduction of Q_{ot}. In order to test the theory that positively charged Q_{ot} was causing the hysteresis, several different V_g sweeps were used for hysteresis measurements; typical hysteresis measurement V_g sweeps were +2V/-2V. 'Up' sweeps were from negative to positive V_g, and 'down' sweeps were from positive to negative V_g. Three different V_g were investigated: a 4V fixed range sweep (-3V/+1V to -1V/+3V), a sweep with the positive V_g fixed at 0V (-2.8V/0V to -1.5V/0V), and a sweep with the negative V_g fixed at -2V (-2V/+2V to -2V/0V). In figure 4.6, the hysteresis decreased from

167mV down to 25mV as the 4V fixed sweep range went from -3V/+1V to -1V/+3V, respectively; negative V_g served to recharge the positive or hole traps in the ZrO_2, whereas positive V_g served to detrap these holes [33]. Thus as the range approached a high negative voltage (-3V) most of the hole traps were filled, and caused the negative shift in V_{fb} (figure 4.6). In figure 4.7, the hysteresis decreased from 132mV down to 31mV as the sweep range went from -2.8V/0V down to -1.5V/0V, respectively. Once again, negative V_g affected the hysteresis more strongly than positive V_g, since negative V_g caused the filling of the hole traps and consequent negative V_{fb} shift. Finally, on figure 4.8, the hysteresis decreased slightly from 102mV down to 62mV as the sweep range went from -2V/+2V down to -2V/0V, respectively. Although higher positive V_g was effective at detrapping holes in the ZrO_2, and thus reducing hysteresis, it was the negative V_g that dominated the hysteresis. In figure 4.7, the reduction in hysteresis was 101mV just by changing the negative V_g from -2.8V to -1.5V, whereas in figure 4.8 the reduction in hysteresis was only 40mV by changing the positive V_g from +2V to 0V.

Figure 4.9 shows a cartoon depiction of what happened to the traps in the ZrO_2 near the ZrO_2/Si interface during negative and positive V_g bias. When negative V_g was applied, the traps were filled – with higher negative V_g resulting in more traps filled [33]. When positive V_g was applied, some of the traps were detrapped, and further detrapping occurred at higher positive V_g. Since the trapping of the holes dominated the hysteresis behavior, the negative V_g affected hysteresis more.

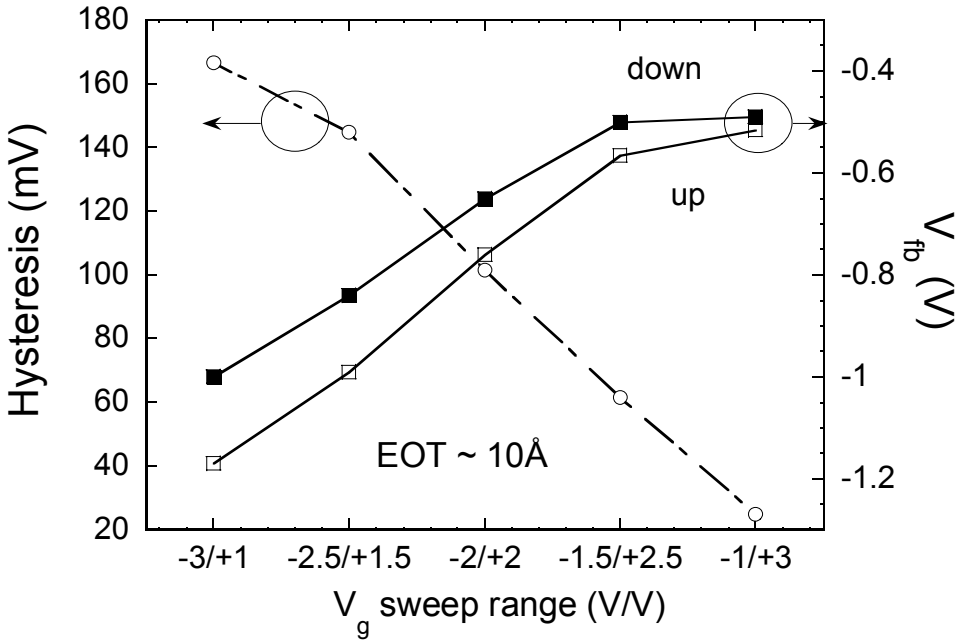

Figure 4.6 Hysteresis decreased as the V_g sweep range shifted positive from -3V/+1V to -1V/+3V.

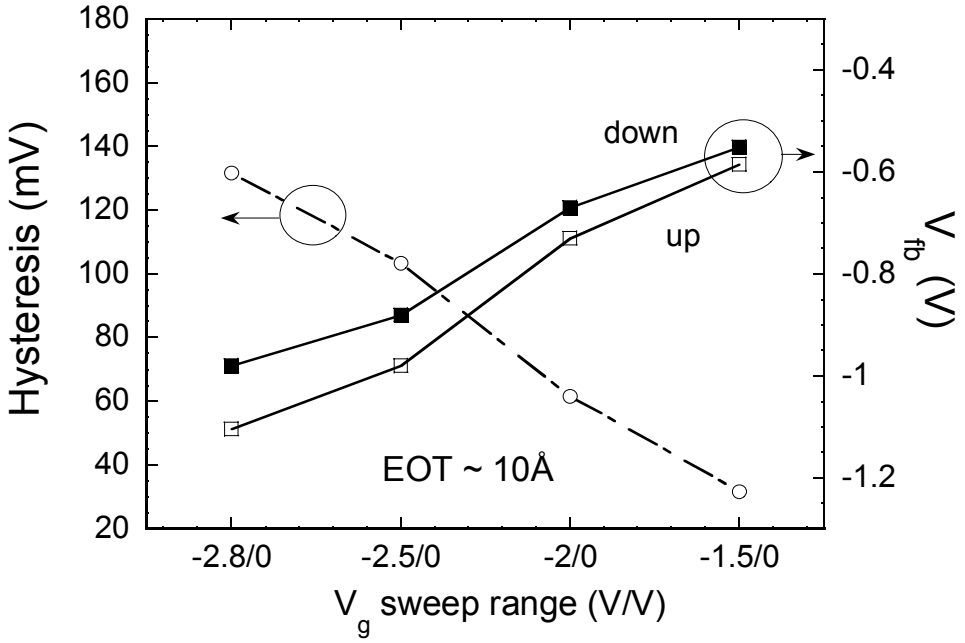

Figure 4.7 Hysteresis decreased as the V_g sweep range varied from -2.8V/0V to -1.5V/0V.

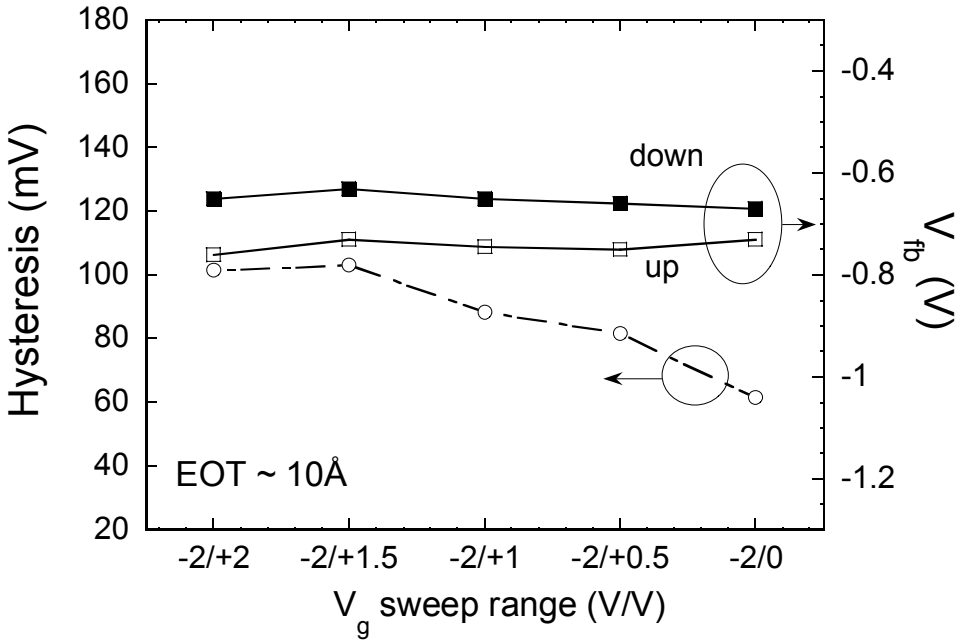

Figure 4.8 Hysteresis decreased slightly as the V_g sweep range varied from -2V/+2V to -2V/0V.

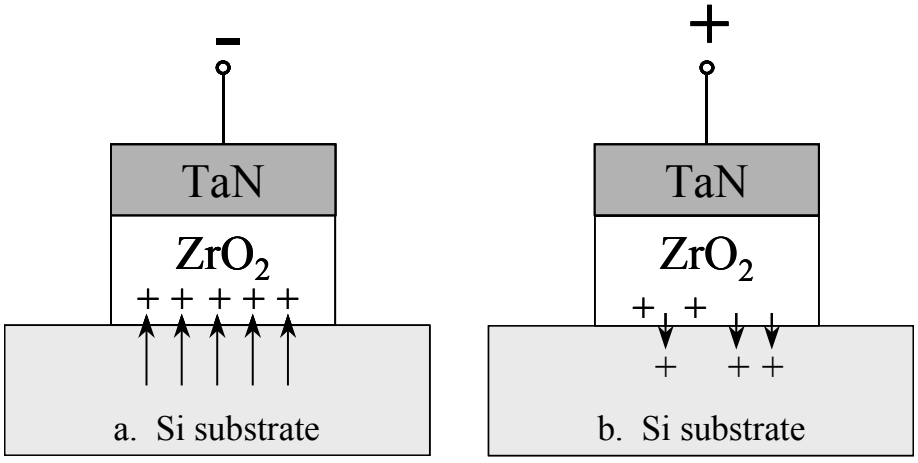

Figure 4.9 Cartoon of TaN/ZrO_2 MOSCAP. When (a) negative V_g is applied, holes are trapped in the ZrO_2 near the ZrO_2/Si interface. When (b) positive V_g is applied, some of these holes are detrapped.

An encouraging result from the experiments was that hysteresis was reduced drastically down to 10mV for TaN/ZrO_2 devices after MOSFET fabrication with a +2/-2V V_g sweep (figure 4.11). This reduction was explained by the reduction of Q_{ot} during the high temperature (≥ 900ºC) source/drain activation annealing. In addition, hysteresis decreased with decreasing V_g sweep, particularly the negative V_g limit. Consequently, by the time high-k dielectrics are adopted, hysteresis will be < 10mV since operating voltages will be closer to +1/-1V.

To summarize the results on TaN-gated ZrO_2 MOSCAPs, C-V, EOT scalability, frequency dispersion, leakage, and C-V hysteresis were evaluated. First, as expected, EOT was found to be similar for devices on both p and n-type Si substrate. MOSCAPs with EOT of 9.8Å demonstrated negligible frequency dispersion and low leakage. MOSCAPs with post-TaN annealing were evaluated and not surprisingly, EOT increased with increasing anneal temperature due to IL growth and compositional changes. However, Q_f, Q_{ot}, and D_{it} were reduced during post-TaN annealing, resulting in a negative V_{fb} shift, reduced hysteresis, and steeper C-V curves, respectively. C-V hysteresis was investigated in further detail, and it was discovered that positively charged Q_{ot} near the ZrO_2/Si interface was largely responsible for hysteresis. Negative V_g bias resulted in hole trapping, and positive V_g bias resulted in detrapping of some of these trapped holes. Ultimately, hysteresis can be reduced below 10mV after MOSFET processing using operating voltages ≤ 1V. Next, some TaN-gated ZrO_2 MOSFET characteristics will be presented.

4.3 TaN/ZrO_2 NMOSFET characteristics

Self-aligned TaN/ZrO_2 (42Å) NMOSFETs (W/L = 150μm/5μm) were fabricated using the process steps 1-8 and 10-17 in table 4.1 and characterized as described in section 4.2.1. Three different source/drain (S/D) RTP activation anneals were performed: 850ºC for 1 minute, 900ºC for 1 minute, and 950ºC for 30 seconds. In this section, C-V, hysteresis, leakage current, time-zero breakdown (tzbd), I_d-V_g, I_d-V_d, and electron mobility characteristics will be evaluated.

Figure 4.10 shows good agreement between the MOSCAP and MOSFET C-V curves annealed at 850ºC with an EOT of 11.3Å. Figure 4.11 summarizes the EOT and C-V hysteresis for the three S/D anneals as well as the MOSCAP before S/D annealing. As shown, the EOT increases slightly with increasing annealing temperature from 9.8Å for samples with no S/D anneal to 12.1Å for samples with 950ºC annealing. The C-V hysteresis after +2V/-2V sweep, reduced from 157mV for samples with no anneal down to 10mV after 950ºC annealing. As described in section 4.2.2, this reduction in hysteresis was due to reduction of trapped charge (Q_{ot}) in the ZrO_2 near the ZrO_2/Si interface. As for leakage, these TaN-gated samples yielded characteristics similar to the Pt-gated samples presented in section 2.3.3. Figure 4.12 shows leakage at V_g = -1.5 as a function of EOT both before and after MOSFET fabrication. After MOSFET fabrication, samples showed higher leakage – possibly due to increased ZrO_2 crystallization during S/D annealing. Overall, leakage characteristics were fairly low for the EOTs achieved.

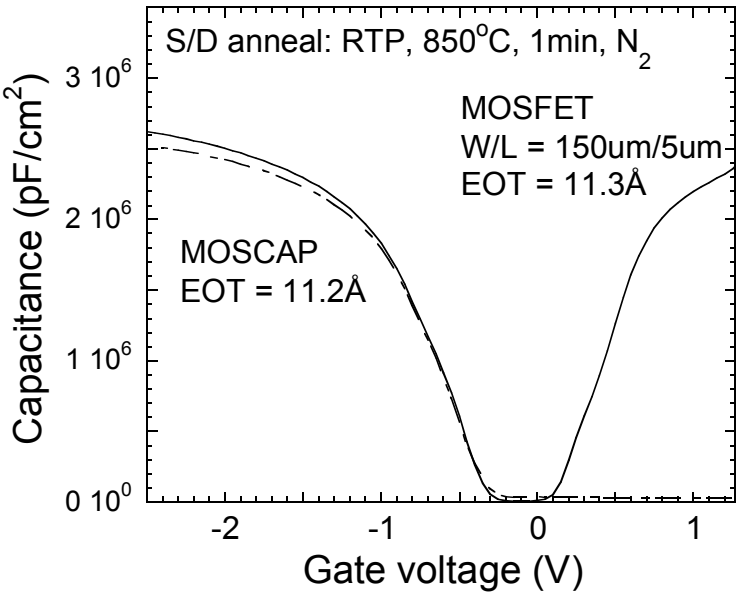

Figure 4.10 MOSCAP and MOSFET C-V curves show good agreement and an EOT ~11.3Å.

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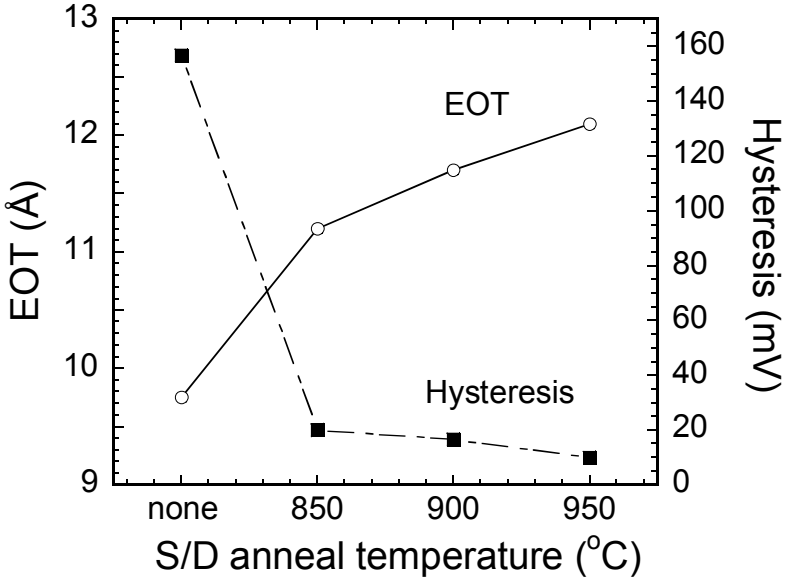

Figure 4.11 EOT increases and hysteresis decreases with increasing S/D annealing temperature.

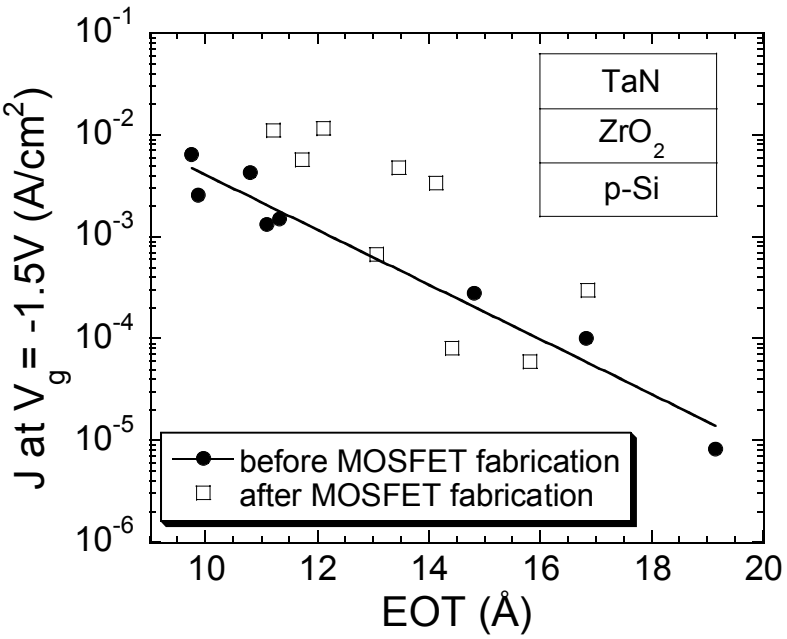

Figure 4.12 Leakage at V_g= -1.5V before MOSFET fabrication is lower than after MOSFET fabrication.

Ramped voltage tests were performed to analyze time-zero breakdown (tzbd) both before and after MOSFET fabrication. In figure 4.13, MOSCAPs yielded comparable effective breakdown field (E_{bd}), which is defined in equation 4.4 where V_{bd} is breakdown voltage, and V_{fb} is flat band voltage.

$$E_{bd} = |V_{bd}-V_{fb}|/EOT \qquad (4.4)$$

V_{fb} was subtracted from V_{bd} to compensate for differences in the V_{fb} before and after MOSFET fabrication.

Well behaved I_d-V_g characteristics for TaN/ZrO_2 NMOSFETs are shown in figure 4.14; this MOSFET had an EOT of 12.1Å after 950ºC S/D annealing. The subthreshold swing (S) of these MOSFETs was fairly high at around 90.3 mV/decade for the 950°C annealed sample up to 95.5 mV/decade for the 850°C sample.

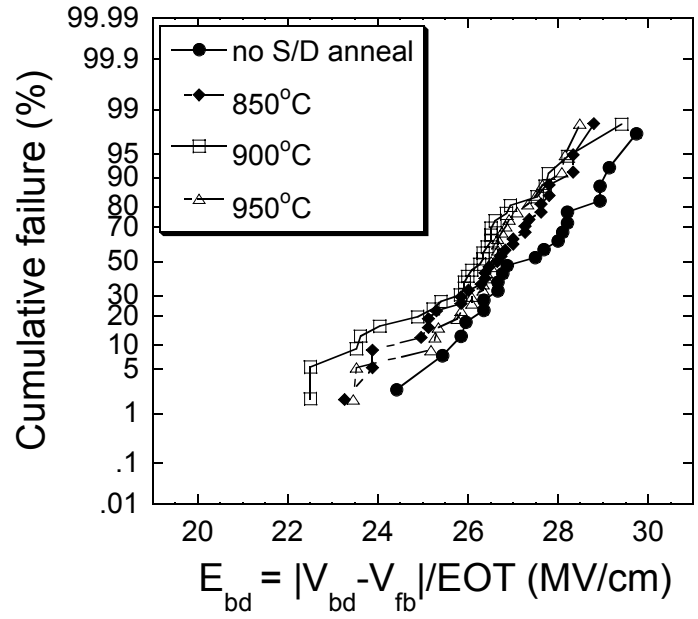

Figure 4.13 Tzbd characteristics for TaN/ZrO_2 MOSCAPs both before and after MOSFET fabrication are comparable.

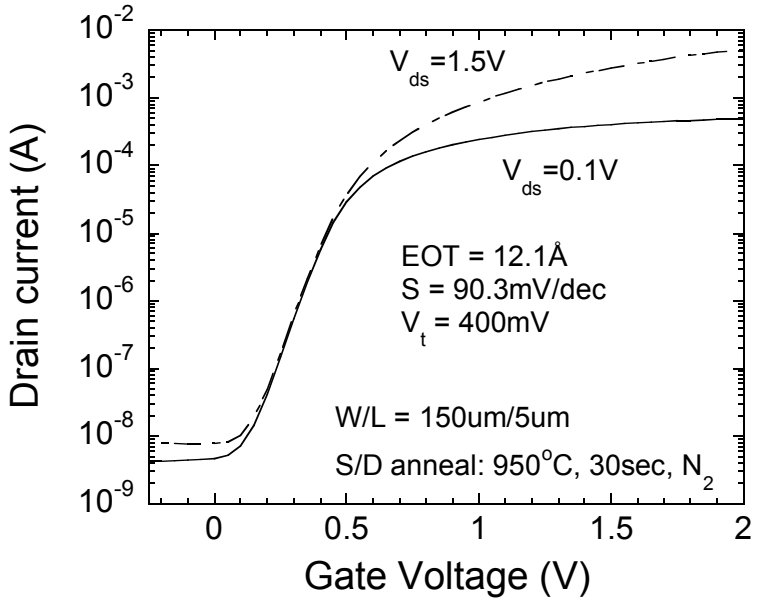

Figure 4.14 TaN/ZrO_2 I_d-V_g characteristics are fairly well behaved.

The S values presented here agree with other reported swing values for TaN/ZrO_2 NMOSFETs that range from 85-97 mV/decade [23,34]. With further process optimization such as the high temperature (500-600ºC) forming gas annealing described in section 5.4.2, these S values could be reduced. The threshold voltage (V_t) for these NMOSFETs ranged from 400-450mV depending on the S/D annealing conditions. Typical I_d-V_d characteristics for these TaN/ZrO_2 NMOSFETs are shown in figure 4.15 and compare well with other work [23,34]. The I_d-V_d curves were well behaved and demonstrated reasonable drive current with an EOT of 11.3Å after 850ºC S/D annealing.

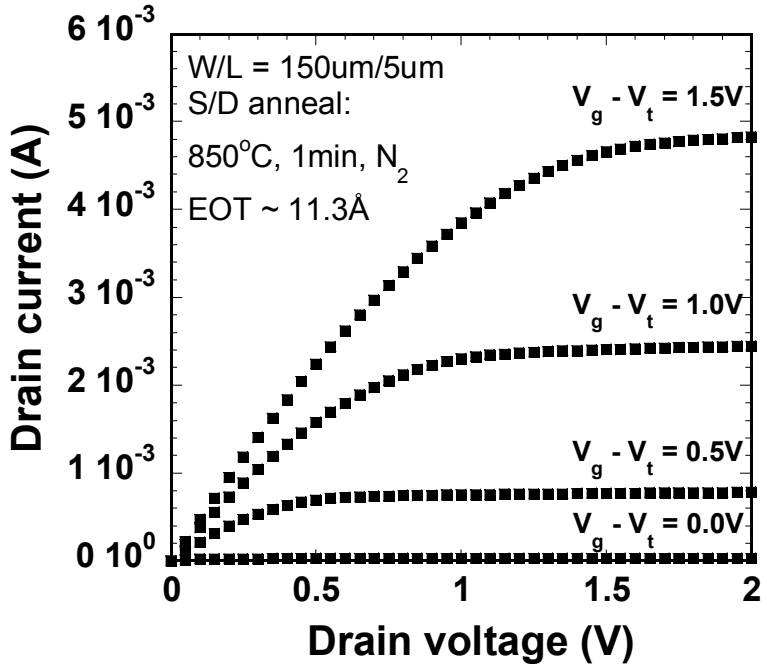

Figure 4.15 Output characteristics of TaN/ZrO_2 NMOSFETs are well behaved.

Finally, mobility was measured on these TaN/ZrO_2 NMOSFETs using the split C-V method described in section 4.2.1. As shown in figure 4.16, mobility was drastically degraded as compared to the universal curve for SiO_2 (equation 4.3). The main reason for this degradation was the degraded ZrO_2/Si interface quality as compared to that of SiO_2/Si. As will be seen in section 5.4.2, the mobility can be greatly enhanced via process optimization including a high temperature (500-600ºC) forming gas anneal.

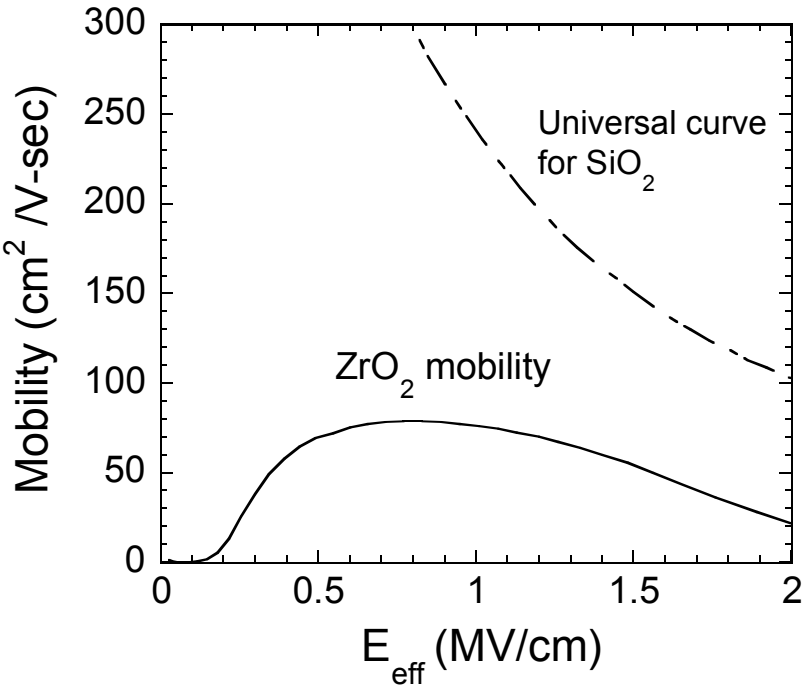

Figure 4.16 Mobility of TaN/ZrO_2 NMOSFETs was degraded compared to the universal curve for SiO_2.

Overall, the results on TaN/ZrO_2 NMOSFETs were fairly good, with EOTs down to 11.3Å and hysteresis down to 10mV after 950ºC S/D annealing. Leakage

versus EOT characteristics were slightly higher after MOSFET fabrication, although dielectric strength (tzbd) was not affected. I_d-V_g and I_d-V_d characteristics were well behaved and comparable with other published results on TaN/ZrO_2 NMOSFETs. Mobility characteristics were severely degraded compared to the universal curve, but could be improved with further process optimization (section 5.4.2).

4.4 Summary

Chapter 4 described the experiments performed and resulting electrical characteristics of TaN-gated ZrO_2 MOSCAPs and NMOSFETs. TaN gate is one of the more promising metal gate electrode materials for NMOS application in future MOS technology, due to its thermal stability and low resistivity. In addition, TaN has demonstrated compatibility and good device characteristics with several high-k candidates including ZrO_2 [23,24,34], HfO_2 [19,20], and their silicates [21,22].

Both MOSCAPs and self-aligned NMOSFETs (W/L = 150μm/5μm) using sputter-deposited TaN on ZrO_2 were fabricated and characterized. As expected, MOSCAPs on both p and n-type Si substrates yielded similar EOT at the same ZrO_2 physical thickness. EOTs of 9.8Å were achieved with negligible frequency dispersion and low leakage current.

Unlike Pt electrodes which tended to form Pt-silicide after annealing, these thermally stable TaN gates could be annealed, which was useful in reducing the sputter damage as well as reducing fixed charge (Q_f), oxide trapped charge (Q_{ot}), and

interface state density (D_{it}). After post-TaN annealing, EOT was increased, which was attributed to interfacial layer (IL) growth and IL compositional changes. However after post-TaN annealing, D_{it} was reduced, V_{fb} shifted in the negative direction due to a reduction in negatively charged Q_f, and C-V hysteresis was reduced. Reduction in hysteresis was caused by a reduction in positively charged Q_{ot} during annealing. It was discovered that hysteresis effects were dominated by the negative gate bias, which caused refilling of the hole traps in the ZrO_2 near the ZrO_2/Si interface. Positive gate voltage also affected hysteresis as it caused some detrapping of the holes.

Next self-aligned TaN/ZrO_2 NMOSFETs with W/L = 150μm/5μm and EOT in the range of 11.3-12.1Å were presented. MOSCAPs and MOSFETs showed good agreement with their C-V characteristics. After 950ºC source/drain annealing, hysteresis was reduced to 10mV at a +2/-2V sweep, and this would be reduced further at lower operating voltages. Leakage characteristics were low, although leakage increased slightly after MOSFET fabrication – possibly due to increased crystallization of the ZrO_2. Time-zero breakdown (tzbd) characteristics were fairly comparable before and after MOSFET fabrication. I_d-V_g characteristics were well behaved and yielded subthreshold swing of ~90 mV/decade and threshold voltage of ~400mV. I_d-V_d characteristics were also well behaved, although mobility was severely degraded as compared to the universal curve for SiO_2. The mobility degradation was attributed to the difference in interface quality between ZrO_2/Si and

SiO_2/Si. Without process adjustments, sputter-deposited ZrO_2 cannot match the excellent interface properties of thermally grown SiO_2. With process optimization, including a high temperature (500-600ºC) forming gas anneal, MOSFET characteristics such as mobility, drive current, and swing were improved as demonstrated in section 5.4.2.

Overall, the device characteristics of the TaN/ZrO_2 MOSCAPs and NMOSFETs presented were quite promising and agreed well with other published results [23,34]. Both TaN and ZrO_2 proved that they are compatible and viable candidates for future metal electrode and high-k gate dielectric, respectively. Of course, further investigation and process optimization of TaN and ZrO_2 are required before these materials can be adopted into MOS technology.

4.5 References

[1] C. Hu, "Gate oxide scaling limits and projection," International Electron Devices Meeting, IEDM Technical Digest, p. 319, 1996.

[2] G.D. Wilk, R.M. Wallace, and J.M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, vol. 89, no. 10, p. 5243, 2001.

[3] B. Cheng, M. Cao, R. Rao, A. Inani, P.V. Voorde, W.M. Greene, J.M.C. Stork, Z. Yu, P.M. Zeitzoff, and J.C.S. Woo, "The Impact of High-k Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFETs," IEEE Transactions on Electron Devices, vol. 46, no. 7, p. 1537, 1999.

[4] Y.-C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of High-k Gate Dielectric Materials on Metal and Silicon Gate Workfunctions," IEEE Electron Device Letters, vol. 23, no. 6, p. 342, 2002.

[5] H. Zhong, G. Heuss, and V. Misra, "Electrical Properties of RuO_2 Gate Electrodes for Dual Metal Gate Si-CMOS," IEEE Electron Device Letters, vol. 21, no. 12, p. 593, 2000.

[6] H. Zhong, G. Heuss, V. Misra, H. Luan, C.-H. Lee, and D.L. Kwong, "Characterization of RuO_2 electrodes on Zr silicate and ZrO_2 dielectrics," Applied Physics Letters, vol. 78, no. 8, p. 1134, 2001.

[7] Q. Lu, R. Lin, P. Ranade, T.-J. King, and C. Hu, "Metal Gate Work Function Adjustment for Future CMOS Technology," Technical Digest of Symposium on VLSI Technology, p. 45, 2001.

[8] J. Shappir, A. Anis, and I. Pinsky, "Investigation of MOS Capacitors with Thin ZrO_2 Layers and Various Gate Materials for Advanced DRAM Applications," IEEE Transactions on Electron Devices, vol. ED-33, no. 4, p. 442, 1986.

[9] Q. Lu, R. Lin, P. Ranade, Y.C. Yeo, X. Meng, H. Takeuchi, T.J. King, C. Hu, H. Luan, S. Lee, W. Bai, C.-H. Lee, D.L. Kwong, X. Guo, X. Wang, and T.P. Ma, "Molybdenum metal gate MOS technology for post-SiO_2 gate dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 641, 2000.

[10] D.-G. Park, T.-H. Cha, K.-Y. Lim, H.-J. Cho, T.-K. Kim, S.-A. Jang, Y.-S. Suh, V. Misra, I.-S. Yeo, J.-S. Roh, J. W. Park, and H.-K. Yoon, "Robust ternary

metal gate electrodes for dual gate CMOS devices," International Electron Devices Meeting, 2001. IEDM Technical Digest, p. 671, 2001.

[11] K. Nakajima, Y. Akasaka, M. Kaneko, M. Tamaoki, Y. Yamada, T. Shimizu, Y. Ozawa, and K. Suguro, "Work Function Controlled Metal Gate Electrode on Ultrathin Gate Insulators," Technical Digest of Symposium on VLSI Technology, p. 95, 1999.

[12] B. Claflin, M. Binger, and G. Lucovsky, "Interface studies of tungsten nitride and titanium nitride composite metal gate electrodes with thin dielectric layers," Journal of Vacuum Science & Technology A, vol. 16, no. 3, p. 1757, 1998.

[13] H. Zhong, S.-N. Hong, Y.-S. Suh, H. Lazar, G. Heuss, and V. Misra, "Properties of Ru-Ta Alloys as Gate Electrodes for NMOS and PMOS Silicon Devices," International Electron Devices Meeting, IEDM Technical Digest, p. 467, 2001.

[14] Y.-S. Suh, G. Heuss, H. Zhong, S.-N. Hong, and V. Misra, "Electrical Characteristics of $TaSi_xN_y$ Gate Electrodes for Dual Gate S-CMOS Devices," Technical Digest of Symposium on VLSI Technology, p. 47, 2001.

[15] S.B. Samavedam, H.H. Tseng, P.J. Tobin, J. Mogab, S. Dakshina-Murthy, L.B. La, J. Smith, J. Schaeffer, M. Zavala, R. Martin, B.-Y. Nguyen, L. Herbert, O. Adetutu, V. Dhandapani, T.-Y. Luo, R. Garcia, P. Abramowitz, M. Moosa, D.C. Gilmer, C. Hobbs, W.J. Taylor, J.M. Grant, R. Hedge, S. Bagchi, E. Lucowski, V. Arunachalam, and M. Azrak, "Metal Gate MOSFETs with HfO_2 Gate Dielectric," Technical Digest of Symposium on VLSI Technology, p. 24, 2002.

[16] Y.H. Kim, C.H. Lee, T.S. Jeon, W.P. Bai, C.H. Choi, S.J. Lee, L. Xinjian, R. Clarks, D. Roberts, and D.L. Kwong, "High Quality CVD TaN Gate Electrode for Sub-100nm MOS Devices," International Electron Devices Meeting, IEDM Technical Digest, p. 667, 2001.

[17] H. Shimada, I. Ohshima, S.-I. Nakao, M. Nakagawa, K. Kanemoto, M. Hirayama, S. Sugawa, and T. Ohmi, "Low Resistivity bcc-Ta/TaN_x Metal Gate MNSFETs Having Plane Gate Structure Featuring Fully Low-Temperature Processing below 450ºC," Technical Digest of Symposium on VLSI Technology, p. 67, 2001.

[18] Y. Nakamura, I. Asano, M. Hiratani, T. Saito, and H. Goto, "Oxidation-Resistant Amorphous TaN Barrier for MIM Ta_2O_5 Capacitors in Giga-Bit DRAMs," Technical Digest of Symposium on VLSI Technology, p. 39, 2001.

[19] R. Choi, C.S. Kang, B.H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J.C. Lee, "High-Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation," Technical Digest of Symposium on VLSI Technology, p. 15, 2001.

[20] B.H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W.-J. Qi, C.S. Kang, and J.C. Lee, "Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8-12Å)," International Electron Devices Meeting, IEDM Technical Digest, p. 39, 2000.

[21] S. Gopalan, K. Onishi, R. Nieh, C.S. Kang, R. Choi, H.-J. Cho, S. Krishnan, and J.C. Lee "Electrical and physical characteristics of ultrathin hafnium silicate films with polycrystalline silicon and TaN gates," Applied Physics Letters, vol. 80, no. 23, p. 4416, 2002.

[22] E. Dharmarajan, W.-J. Qi, R. Nieh, L. Kang, K. Onishi, and J.C. Lee, "Ultra-Thin Zirconium Silicate Films With Good Physical and Electrical Properties for Gate Dielectric Applications," Material Research Society (MRS) Symposium Proceedings, vol. 648, 2000.

[23] C.H. Lee, Y.H. Kim, H.F. Luan, S.J. Lee, T.S. Jeon, W.P. Bai, and D.L. Kwong, "MOS Devices with High Quality Ultra Thin CVD ZrO_2 Gate Dielectrics and Self-Aligned TaN and TaN/Poly-Si Gate Electrodes," Technical Digest of Symposium on VLSI Technology, p. 137, 2001.

[24] R. Nieh, S. Krishnan, H.-J. Cho, C.S. Kang, S. Gopalan, K. Onishi, R. Choi, and J.C. Lee, "Comparison between ultra-thin ZrO_2 and ZrO_xN_y gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices," Technical Digest of Symposium on VLSI Technology, p. 186, 2002.

[25] B.H. Lee, "Technology Development and Process Integration of Alternative Gate Dielectric Material; Hafnium Oxide," Ph.D. dissertation, The University of Texas at Austin, 2000.

[26] K. Chen, H.C. Waan, J. Dunster, P.K. Ko, C. Hu, and M. Yoshida, "MOSFET Carrier Mobility Model Based on Gate Oxide Thickness, Threshold and Gate Voltages," Solid-State Electronics, vol. 39, no. 10, p. 1515, 1996.

[27] D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, A. Murthy, B. Roberds, P. Stokley, and R. Chau, "High-Frequency response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 231, 2001.

[28] T. Ma, S.A. Campbell, R. Smith, N. Hoilien, B. He, W.L. Gladfelter, C. Hobbs, D. Buchanan, C. Taylor, M. Gribelyuk, M. Tiner, M. Coppel, and J.J. Lee, "Group IVB Metal Oxides High Permittivity Gate Insulators Deposited From Anhydrous Metal Nitrates," IEEE Transactions on Electron Devices, vol. 48, no. 10, p. 2348, 2001.

[29] M. Houssa, V.V. Afanas'ev, A. Stesmans, and M.M. Heyns, "Variation in the fixed charge density of SiO_x/ZrO_2 gate dielectric stacks during postdeposition oxidation," Applied Physics Letters, vol. 77, no. 12, p. 1885, 2000.

[30] D.M. Fleetwood, "Fast and Slow Border Traps in MOS Devices," IEEE Transactions on Nuclear Science, vol. 43, no. 2, p. 779, 1996.

[31] J.H. Han, R. Nieh, C.S. Kang, H.-J. Cho, K. Onishi, S. Gopalan, R. Choi, S. Krishnan, Y.H. Kim, A. Shahriar, and J.C. Lee, "Hysteresis Dependence on Interface Trapping Charge for $TaN/HfO_2/Si$ and $TaN/ZrO_2/Si$ Capacitors," submitted to Applied Physics Letters, 2002.

[32] S. Ramanathan, C.-M. Park, and P.C. McIntyre, "Electrical properties of thin film zirconia grown by ultraviolet ozone oxidation," Journal of Applied Physics, vol. 91, no. 7, p. 4521, 2002.

[33] K. Kukli, K. Forsgren, M. Ritala, M. Leskelä, J. Aarik, and A. Hårsta, "Dielectric Properties of Zirconium Oxide Grown by Atomic Layer Deposition from Iodide Precursor," Journal of the Electrochemical Society, vol. 148, no. 12, p. F227, 2001.

[34] W.-J. Qi, R. Nieh, B.H. Lee, K. Onishi, L. Kang, Y. Jeon, J.C. Lee, V. Kaushik, B.-Y. Nguyen, L. Prabhu, K. Eigenbeiser, and J. Finder, "Performance of MOSFETs with ultra thin ZrO_2 and Zr silicate gate dielectrics," Technical Digest of Symposium on VLSI Technology, p. 40, 2000.

CHAPTER 5

Nitrogen incorporation into the ZrO_2 gate stack

5.1 Motivation

The purpose of this chapter is to describe the experiments and explain the electrical, material, and reliability characteristics of nitrogen incorporation into the ZrO_2 gate dielectric. Nitrogen was introduced into the ZrO_2 gate stack by two different methods – ammonia (NH_3) annealing prior to ZrO_2 deposition and reactive sputtering of nitrogen-incorporated ZrO_2 or ZrO_xN_y in an Ar and N_2 ambient.

There are many motivations behind the incorporation of nitrogen into the dielectric stack. The incorporation of nitrogen into conventional SiO_2 dielectric or oxynitrides has been studied for years, and has already been adopted into the manufacturing process for flash memory and CMOS logic applications. Oxynitrides have demonstrated improved resistance to impurity/boron penetration, lower leakage current, lower stress induced leakage current (SILC), higher dielectric constant, improved hot-carrier reliability, higher resistance to radiation damage, and higher dielectric breakdown strength compared to conventional SiO_2 gate dielectric [1-4]. Oxynitrides also have some disadvantages such as increased fixed charge, interface states, and electron traps, and degraded mobility compared to SiO_2 [1].

Thus, it is hoped that the incorporation of nitrogen into the ZrO_2 gate stack may improve some of its characteristics. Possible improvements include:

- Improved thermal stability
- Prevent/reduce boron penetration
- Reduction of leakage current
- Improved reliability
- Higher crystallization temperature
- Compatibility with poly gate

Even though ZrO_2 is thermodynamically stable on Si, oxygen diffusion during thermal processing can result in interfacial layer growth and a consequent increase in EOT. Boron penetration into the ZrO_2 films may result in threshold voltage shift and reliability degradation. Like oxynitrides, nitrogen incorporation into ZrO_2 may help to reduce the leakage current and improve reliability characteristics. As shown in chapter 2, ZrO_2 films start to crystallize at fairly low temperatures (~400°C); nitrogen in the films may help to raise this temperature. Nitrogen in the ZrO_2 may also help to make the films less prone to the reduction of oxygen during the polysilicon deposition process, thus making ZrO_xN_y compatible with the poly gate electrode (section 3.2.3).

In summary, two methods of nitrogen incorporation – NH_3 surface nitridation and nitrogen incorporated ZrO_2 (ZrO_xN_y) - will be investigated to determine if there are any advantages to be gained. In addition, the possible disadvantages – increased fixed charge, interface states, and electron traps and degraded mobility – and their effect on device characteristics will be evaluated. In order to reduce the D_{it} and

improve mobility, a high temperature (500-600ºC) forming gas anneal was performed on ZrO_xN_y NMOSFETs and the results will also be presented.

5.2 NH_3 Si surface nitridation (SN)

Several studies have been performed on silicon surface nitridation (SN) using Hf-silicate and HfO_2 high-k gate dielectrics with promising results. Hf-silicate and HfO_2 on NH_3 nitrided substrates showed both reduced EOT and reduced leakage current as compared to samples without SN [5,6,7]. Also SIMS data and reduced flat band voltage shift indicated that HfO_2 with SN had reduced boron penetration during S/D activation as well [8]. HfO_2 samples with SN also showed improved hot carrier reliability compared to SiO_2 [9]. The main drawbacks to the SN process with Hf-silicate were higher C-V hysteresis, degraded swing, reduced transconductance, lower drive current, and lower mobility, which were most likely due to the increased fixed charge, interface states, and electron traps [5]. Similar advantages and disadvantages for ZrO_2 gate dielectrics with SN will be seen.

5.2.1 TaN/ZrO_2 NMOSCAP with SN process flow and measurement [10]

TaN/ZrO_2/Si NMOSCAPs with SN were fabricated using the process flow in table 5.1 where step 5 was not performed for the control samples – the samples without nitridation.

1. Piranha clean
2. Field oxidation ~3500Å at 950ºC
3. Active area patterning (Buffered oxide etch): $5x10^{-5}$ cm^2
4. Piranha clean/HF dip/DI water rinse
5. * Surface nitridation (SN): RTP, NH_3, 700°C, 10 seconds
6. Zr deposition: DC magnetron sputtering in Ar
7. Post deposition anneal (PDA): RTP, 500-800ºC, N_2
8. TaN deposition ~2000Å: DC sputtering in Ar + N_2
9. TaN patterning (RIE in CF_4)
10. * Post-TaN anneal: RTP, N_2, 500-800°C
11. Backside aluminum deposition

* step was not performed in every split

Table 5.1 TaN/ZrO_2 with SN NMOSCAP fabrication process

Post-TaN annealing was not performed for every sample. Steps 1-4 were the same as described in section 2.2.1. Samples with SN underwent a rapid thermal process (RTP) in NH_3 at 700ºC for 10 seconds prior to ZrO_2 deposition. These optimized nitridation conditions were chosen because they yielded both low EOT and leakage current as shown in figure 5.1. ZrO_2 (35-55Å) was deposited via DC sputtering and post deposition annealed as described in 2.2.1. TaN deposition and patterning and post-TaN RTP annealing were described in section 4.2.1.

Ellipsometry was used to measure the SN layer and ZrO_2 film thickness. Once again, a HP 4156 was used to measure leakage current and breakdown voltage, and a HP 4194 was used to measure C-V and C-V hysteresis. C-V hysteresis was measured after sweeping the gate voltage (V_g) back and forth from +2/-2V four times before measuring the change in flat band voltage (V_{fb}).

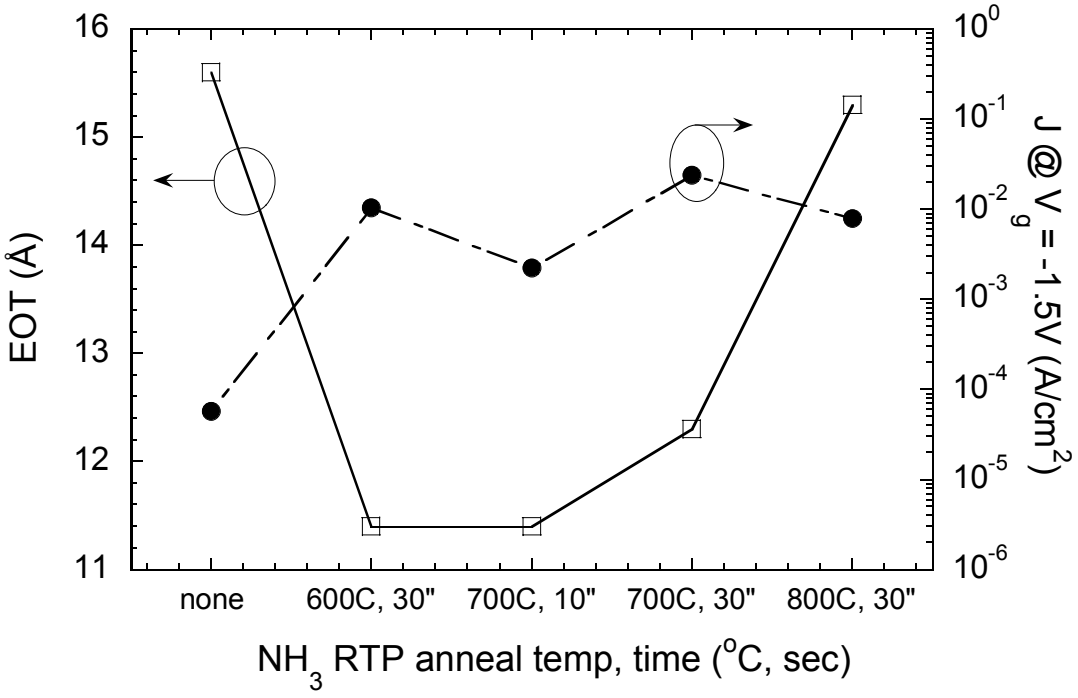

Figure 5.1 Optimization of SN process - NH_3 anneal temperature and time - to yield both low EOT and low leakage current.

5.2.2 Characterization of TaN/ZrO_2 NMOSCAPs with SN [10]

Figure 5.2 shows that the EOT values for SN samples were 2.6-4.3Å lower than non-nitrided samples with the same ZrO_2 physical thickness (~35Å) over all PDA temperatures. The difference in the EOT between the SN and non-nitrided samples increased slightly with temperature, indicating that the SN MOSCAPs had increased thermal stability over the non-nitrided MOSCAPs. As expected, the EOT increased with increasing PDA temperature due to interfacial layer (IL) growth and IL compositional changes. From figure 2.9, XPS analysis showed that the IL of non-nitrided ZrO_2 was a Zr-silicate whose Zr concentration and thus dielectric constant

decreased with increasing thermal budget. Thus the improved thermal stability of SN samples may be due to the combination of IL growth reduction and IL composition.

The thinnest EOTs achieved for ZrO_2 (~35Å) MOSCAPs were 8.7Å with SN and 11.3Å without SN; the 1 MHz C-V curves for these samples were well behaved (figure 5.3). The C-V for the SN sample was shifted negative relative to the non-nitrided sample, which was caused by the difference in fixed charge (Q_f) in the films. As discussed in section 4.2.2, ZrO_2 films have a negative Q_f; however, this negative Q_f can be compensated for by the positive Q_f that is common in samples with a heavy degree of nitridation [1]. Thus the SN samples have less Q_f than non-nitrided samples.

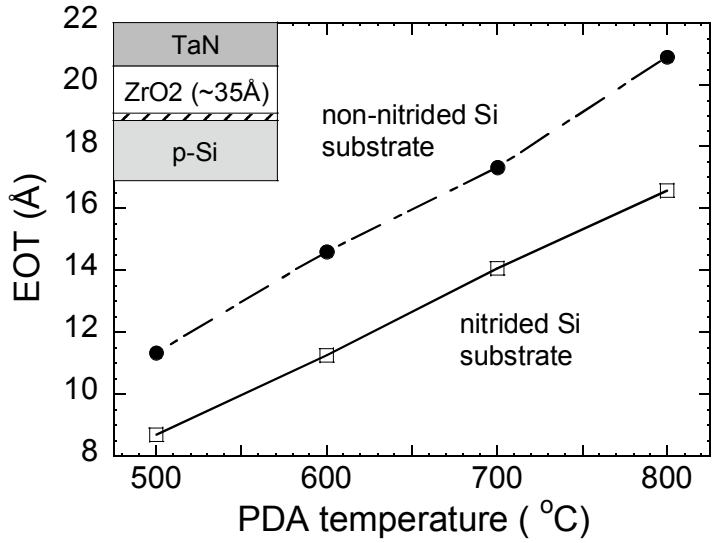

Figure 5.2 TaN/ZrO_2 MOSCAPs with SN have EOT 2.6-4.3Å lower than similar MOSCAPs without SN [10].

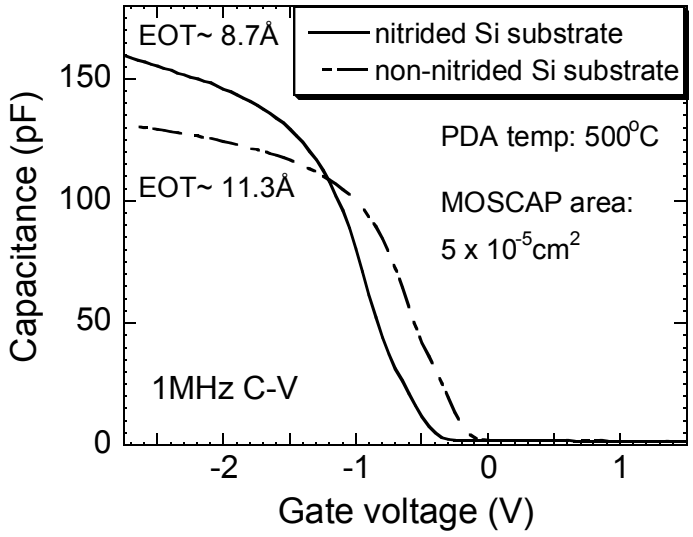

Figure 5.3 C-Vs of TaN/ZrO_2 MOSCAPs with SN show thinner EOT, and are shifted negative due to reduced positive Q_f [10].

Counterclockwise C-V hysteresis in these devices could be attributed to several factors including damage caused during the ZrO_2 and TaN deposition and trapped charges (Q_{ot}) [11] – all of which are reduced during annealing. Due to Q_{ot} near the ZrO_2/nitrided Si interface and Q_{ot} near the nitrided Si/Si substrate interface, the SN samples showed consistently higher hysteresis than non-nitrided samples (figure 5.4). Q_{ot} was higher for the SN samples due to the hydrogen-related traps, such as -H, -OH, and N-H bonds that result from the NH_3 decomposition during nitridation. Hysteresis did decrease with increasing PDA temperature (figure 5.4), and it should be noted that this hysteresis could be reduced further (< 50mV) with post-TaN annealing (not shown).

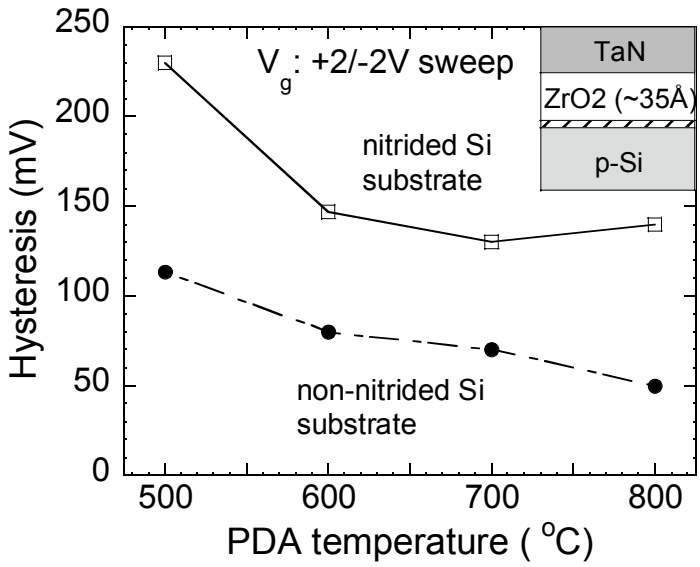

Figure 5.4 Hysteresis is higher for SN samples due to higher Q_{ot} than samples without SN [10].

High resolution TEM pictures of ~35Å thick ZrO_2 on non-nitrided (figure 5.5a) and nitrided (figure 5.5b) Si were compared. Both samples endured the same ZrO_2 deposition conditions and the same PDA conditions of 500ºC for 30 seconds in N_2. Both TEM pictures show an amorphous interfacial layer (IL), but the SN samples actually had a thicker IL than non-nitrided samples, even though the EOT for the SN sample (8.7Å) was lower than the non-nitrided sample (11.3Å). Consequently, it was concluded that the IL of the SN samples must have a higher dielectric constant than the non-nitrided IL. By estimating the dielectric constant of the ZrO_2 layer to be 20, the calculated values of the dielectric constant were 4.8 for the non-nitrided IL and 10.5 for the nitrided IL. Since these IL dielectric constant values were slightly higher

than those of SiO_2 (3.9) and nitride (7.5) [12], the composition of the non-nitrided IL was likely a Zr-silicate whereas the nitrided IL more resembled a Zr-doped silicon nitride layer.

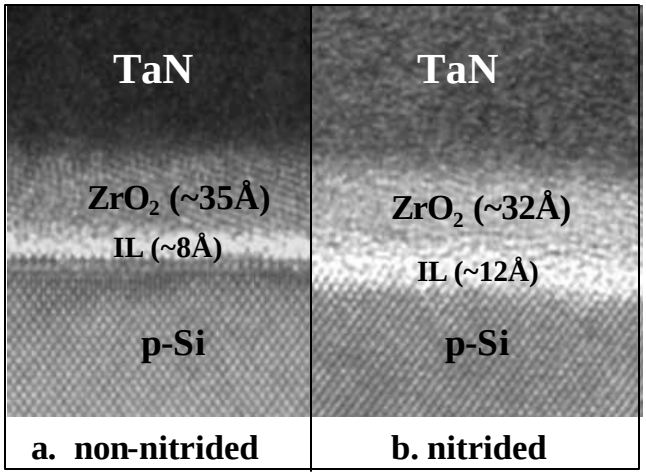

Figure 5.5 TEMs of TaN/ZrO_2 MOSCAPs (a) without SN and EOT ~11.3Å and (b) with SN and EOT ~8.7Å demonstrate that the SN IL has a higher k than the IL without SN [10].

Leakage current at a gate voltage of V_{fb}-1V versus EOT is shown in figure 5.6. With increasing annealing temperature, Q_f was reduced and thus V_{fb} increased; V_{fb} ranged from -0.65V to -0.75V for SN samples and -0.38V to -0.52V for non-nitrided samples annealed at 900ºC to 500ºC, respectively. Although the SN samples showed a thicker IL than the non-nitrided samples, they both showed similar leakage characteristics at the same EOT (figure 5.6). One possible explanation for this is difference in bandgap between the non-nitrided IL that more resembled SiO_2 (bandgap ~9.0eV) and the SN IL that resembled silicon nitride (~5.0eV) [12]. Consequently, the tradeoff between the thicker physical thickness and the lower

bandgap and barrier height of the nitrided IL resulted in comparable leakage current for the non-nitrided and nitrided samples. Nevertheless, the leakage currents were low for all the ZrO_2 samples; the SN sample with EOT of 8.7Å had leakage current ~$1.0x10^{-2}$ A/cm^2 at $V_g=V_{fb}$-1V.

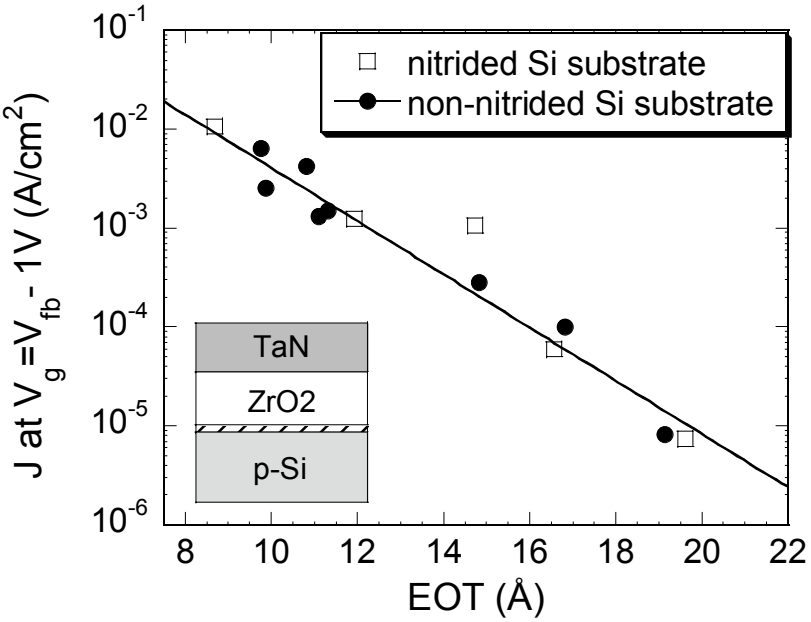

Figure 5.6 Leakage versus EOT characteristics for SN and non-nitrided samples show comparable leakage for the same EOT [10].

In summary, the effect of silicon surface nitridation (SN) on TaN/ZrO_2/p-Si NMOSCAP characteristics was investigated. It was discovered that SN samples exhibited lower EOT, comparable leakage current, but a thicker interfacial layer (IL) with a higher dielectric constant, and increased C-V hysteresis as compared to non-nitrided samples. Other studies have demonstrated similar results using ZrO_2 with a SN process with EOT ~8.9Å and low leakage [13], TEMs showing amorphous IL with k values higher than that of SiO_2 [14,15], and fairly high C-V hysteresis

~130mV [14]. Overall, the results were encouraging, and with further evaluation and optimization, surface nitridation may find an application to further scale the EOT of high-k dielectrics like ZrO_2. However, the high concentration of nitrogen and hydrogen-related traps from the SN process resulted in fairly high Q_{ot}, D_{it}, and C-V hysteresis. These problems may be avoided by using a method that incorporates less nitrogen at the ZrO_2/Si interface, and one that does not use NH_3. One method is the incorporation of nitrogen in the ZrO_2 via reactive sputtering or ZrO_xN_y.

5.3 Nitrogen-incorporated ZrO_2 or ZrO_xN_y

There have been various studies on nitrogen incorporation into the HfO_2 gate stack via reactive sputtering of HfN followed by annealing to convert the film to HfO_xN_y. These HfO_xN_y films have demonstrated improved thermal stability, lower leakage current, and higher crystallization temperature (~800º), compared to HfO_2 [16]. They also exhibited good transistor characteristics and EOT < 10Å [16]. Another study on HfO_xN_y focused on using a thin layer of HfO_xN_y on top of HfO_2 to avoid incorporating nitrogen at the HfO_2/Si interface. This top nitrided technique yielded excellent results with low EOT (<10Å), lower leakage current, lower C-V hysteresis, lower D_{it}, decreased boron penetration, higher breakdown voltage, smoother surface roughness, and improved thermal stability compared to HfO_2 control samples [17,18].

One study has presented ZrO_xN_y gate dielectrics using gold electrode MOSCAPs. The ZrO_xN_y yielded promising results with improved thermal stability and higher crystallization temperature [19]. However, the capacitance equivalent thickness (CET) was relatively high at 15Å, the gate electrode – gold – was not a potential metal gate candidate, and no MOSFET characteristics were reported. Consequently, ZrO_xN_y was investigated using a viable metal gate candidate – TaN – and compared to ZrO_2 in both MOSCAPs and MOSFETs, and materials characterization such as XPS, XRD, and TEM were performed.

5.3.1 TaN/ZrO_xN_y NMOSCAP/NMOSFET process flow and measurement

Both TaN gate NMOSCAPs and self-aligned NMOSFETs were fabricated as described in table 5.2 to compare the characteristics of ZrO_2 and ZrO_xN_y. TaN-gated MOSCAPs with an active area of $5x10^{-5}$ cm^2 were fabricated using steps 1-9 of table 5.2. NMOSFETs (W/L=150μm/5μm) did not undergo the post-TaN anneal (step 9) since they had a S/D activation anneal.

Both dielectrics were deposited in a Kurt J. Lesker sputtering system at room temperature, at a pressure of 30 mTorr, and gun power of 200W. The Zr film was sputtered in an Ar-only ambient whereas the zirconium nitride (ZrN) film was sputtered in an Ar and N_2 (5-20 sccm) ambient. The sputter rate of Zr (~1.9 Å/sec) was faster than that of the ZrN whose sputter rate decreased with increasing N_2 flow rate, and ranged from 0.33-0.41 Å/sec.

1. Piranha clean
2. Field oxidation ~3500Å at 950ºC
3. Active area patterning (Buffered oxide etch)
4. Piranha clean/HF dip/DI water rinse
5. Zr deposition: DC magnetron sputtering in Ar
   ZrN deposition: DC magnetron sputtering in Ar + N_2
6. Post deposition anneal (PDA): RTP, 600ºC, N_2, 10-30 seconds
7. TaN deposition ~2000Å: DC sputtering in Ar + N_2
8. TaN patterning (RIE in CF_4)
9. * Post-TaN anneal: RTP, N_2, 500-800°C
10. S/D implant: Phosphorus ($5x10^{15}$ cm^{-2}, 50 keV)
11. LTO deposition
12. Contact patterning
13. S/D activation: RTP, 900-950ºC, 30-60 seconds, N_2
14. ** High temperature forming gas anneal: 400-600ºC, 30 minutes
15. HF dip, Al deposition
16. Al contact patterning
17. Backside Al deposition
18. Forming gas anneal: 400ºC, 30 minutes

* step was only performed for MOSCAPs
** step was not performed for all MOSFETs

Table 5.2 TaN/ZrO_2 and TaN/ZrO_xN_y MOSCAP/MOSFET fabrication process [20]

Post deposition annealing (PDA) was optimized to produce both low leakage and low EOT. PDAs were performed in a rapid thermal process (RTP) at 600ºC in N_2 for 10-30 seconds. Ellipsometry (n=2.0) was used to measure film thickness both before and after PDA. TaN deposition and patterning via RIE were performed as described in section 4.2.1. Some MOSCAPs underwent post-TaN annealing in a RTP in N_2 at 500-800ºC. NMOSFET fabrication continued with steps 10-18, which were the same as described in section 4.2.1 with the exception of the high temperature forming gas anneal. Some MOSFETs were subjected to a high temperature forming

gas annealing (step 14) from 400-600ºC for 30 minutes; the results from these NMOSFETs will be described further in section 5.4.

ZrO_2 and ZrO_xN_y films were subjected to materials analysis such as angle resolved XPS, XRD, and TEM in order to answer questions about their chemical composition, crystallinity, interfacial layer (IL) thickness, and IL composition. As for electrical characterization, a HP 4156 was used to measure J-V, time zero breakdown (tzbd), time dependent dielectric breakdown (tddb), drain current vs. gate voltage (I_d-V_g), and drain current vs. drain voltage (I_d-V_d). A HP 4194 was used to measure MOSCAP and MOSFET C-V characteristics and C-V hysteresis as described in section 5.2.1. Mobility was measured using the split C-V method as described in section 4.2.1.

5.3.2 Comparison of ZrO_2 and ZrO_xN_y material characteristics

Angle resolved XPS was performed at 15º, 45º, and 75º on ~40Å thick ZrO_2 and ZrO_xN_y films both as deposited and after a PDA of 600ºC for 20 seconds in N_2. Analysis of the Zr 3d peak for the 'as deposited' films indicated that there was a Zr peak (~179.2 eV) for the ZrO_2 and a ZrN peak (~181.0 eV) for the ZrO_xN_y film (figure 5.7). After 600ºC PDA, the Zr was completely converted to ZrO_2 and the ZrN was completely converted to ZrO_xN_y (figure 5.7). In addition, after PDA, the ZrO_xN_y peaks were shifted towards a lower energy compared to the ZrO_2 peaks, indicating the presence of nitrogen in the ZrO_xN_y film.

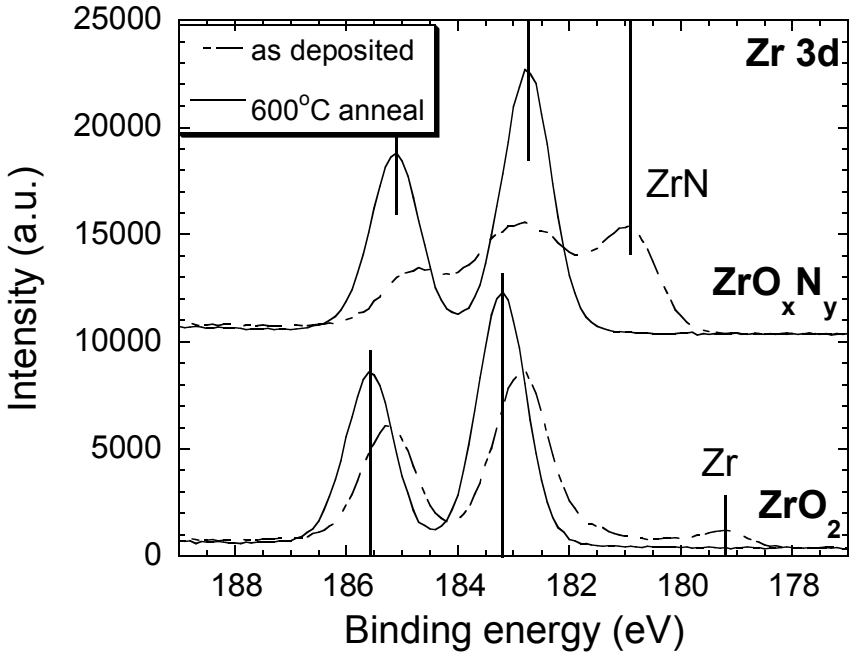

Figure 5.7 XPS data (75º) of Zr 3d peaks for ZrO_2 and ZrO_xN_y both before and after 600ºC PDA show that Zr and ZrN have been completely converted to ZrO_2 and ZrO_xN_y, respectively, after PDA.

As for the nitrogen in the films, figure 5.8 shows the N 1s peaks for both ZrO_2 and ZrO_xN_y, before and after 600ºC PDA at 75º. As expected, the ZrO_2 did not show any nitrogen peaks. Before PDA, the ZrO_xN_y exhibited a large ZrN binding peak (~396.1 eV) and a SiN binding peak (~397.6 eV). However, after PDA, only the SiN peak remained, indicating that most of the nitrogen was located in the IL layer between ZrO_xN_y and the Si substrate. Nitrogen pile-up near the ZrO_xN_y/Si interface was confirmed by angle resolved XPS (figure 5.9), which showed nitrogen concentration increasing with increasing XPS angle. SIMS and angle resolved XPS analysis of HfO_xN_y films yielded a similar increase in nitrogen concentration at the HfO_xN_y/Si interface [16].

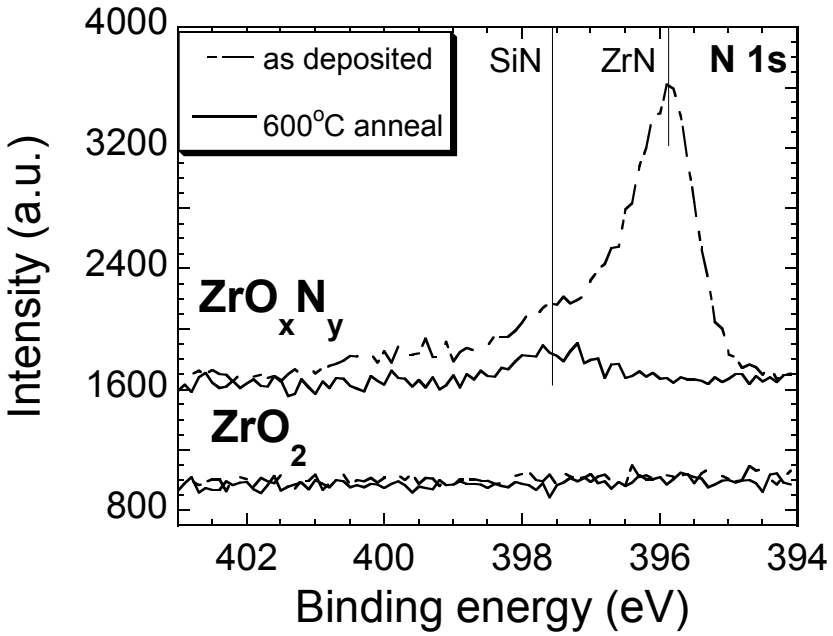

Figure 5.8 XPS data (75º) of N 1s peaks for ZrO_2 and ZrO_xN_y both before and after 600ºC PDA show ZrN and SiN peaks in ZrO_xN_y before PDA and only a SiN peak after PDA.

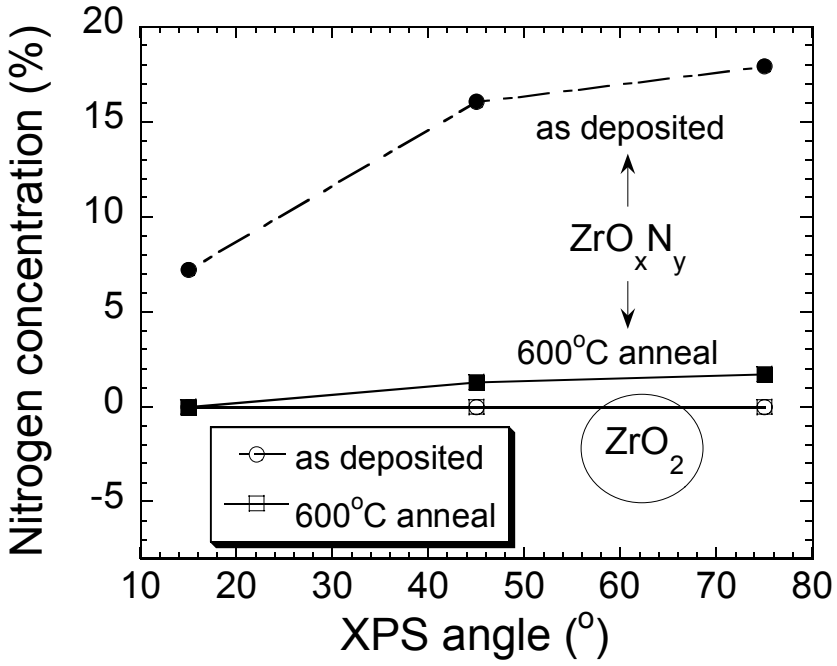

Figure 5.9 Nitrogen concentration in ZrO_xN_y increased with XPS angle, indicating a pile-up of nitrogen near the ZrO_xN_y/Si interface.

It was likely that the pile-up of nitrogen at the ZrO_xN_y/Si interface was facilitated by the stress/strain between the ZrO_xN_y and Si substrate. From figure 5.9, it is clear that the nitrogen concentration in the ZrO_xN_y decreased dramatically after PDA. Most of the nitrogen in the ZrN probably escaped in the form of N_2 gas during the PDA anneal during which the ZrN was fully converted to ZrO_xN_y. After PDA, the overall nitrogen concentration in the ZrO_xN_y was ~1.7% from the XPS data.

As discussed in section 2.3.2, high-k dielectric crystallinity is a concern due to possible problems with leakage paths and dopant/impurity diffusion along grain boundaries. Unfortunately, ZrO_2 crystallizes at a fairly low temperature ($\leq$ 400ºC) as shown in figure 2.12 and in the literature [19,21]. Some studies have attempted to raise the crystallization temperature of ZrO_2 and HfO_2 gate dielectrics by introducing Al into the high-k stack since Al_2O_3 has a crystallization temperature > 900ºC [22,23,24]. The addition of Al into ZrO_2 and HfO_2 has successfully raised the crystallization temperature up to 900ºC with higher Al% yielding higher crystallization temperature [24]. Unfortunately, high Al% also results in lower dielectric constant since the k for Al_2O_3 is only ~10. Additionally, Al_2O_3 has high fixed charge (Q_f), so $Hf_xAl_yO_z$ and $Zr_xAl_yO_z$ also have high Q_f. A better solution may be to incorporate nitrogen in the ZrO_2 (ZrO_xN_y) to increase the crystallinity temperature since it does not lower the k value. The introduction of nitrogen into HfO_2 films raised the crystallization temperature from ~600ºC to 800ºC [16].

Both 100Å thick ZrO_2 and ZrO_xN_y films were prepared for glancing angle X-ray diffraction (XRD) analysis. These films were first annealed in a furnace in N_2/O_2

at 400ºC for 3 minutes in order to fully oxidize the Zr and ZrN into ZrO_2 and ZrO_xN_y, respectively. Next, they were annealed in a RTP at temperatures ranging from 400-950ºC for 1 minute in N_2. As mentioned, the XRD spectra for the ZrO_2 were already shown in figure 2.12, and revealed that the ZrO_2 was crystallized after 400ºC RTP annealing. Figure 5.10 shows the XRD spectra for the ZrO_xN_y (100Å) annealed from 400-800ºC; these ZrO_xN_y films did not show signs of crystallization until ~600-700ºC. Thus, the addition of nitrogen (~1.7%) into ZrO_2 resulted in ~200-300ºC higher crystallization temperature. M. Koyama, *et al*. also showed that the crystallization temperature of ZrO_xN_y was ~700ºC, higher than that of ZrO_2 ~400ºC [19].

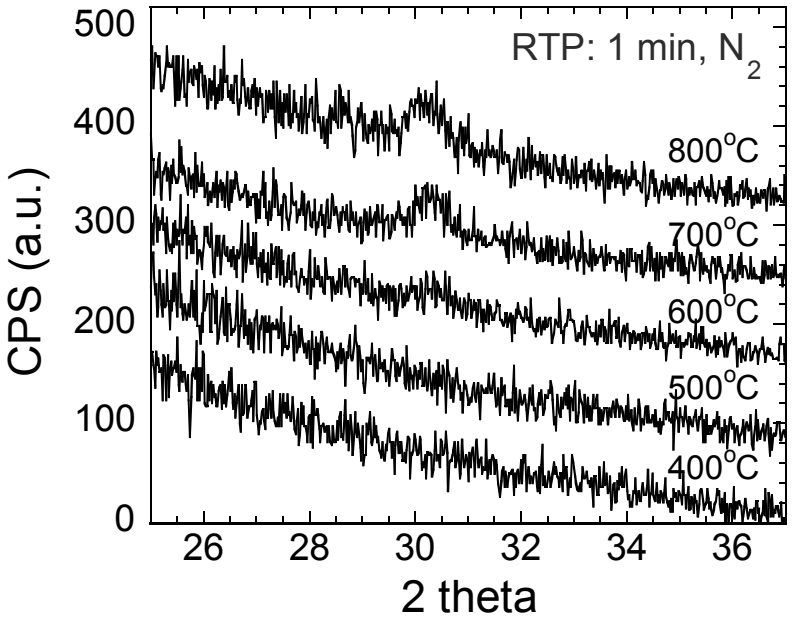

Figure 5.10 XRD analysis of ZrO_xN_y (100Å) films annealed up to 800ºC show signs of crystallization after ~600-700ºC annealing.

Admittedly, 600-700ºC is still a fairly low temperature range for the self-aligned CMOS process, but it may be adequate if the replacement gate process is adopted in the future. Additionally, nitrogen content higher than 1.7% in the ZrO_xN_y may increase the crystallization temperature higher than 700ºC.

Both angle resolved XPS and glancing angle XRD were used to analyze and compare ZrO_2 and ZrO_xN_y thin films. It was found that the PDA served to fully convert the Zr to ZrO_2 and ZrN to ZrO_xN_y. Similar to oxynitrides, the nitrogen in the ZrO_xN_y piled up near the ZrO_xN_y/Si interface, and the total nitrogen concentration in the film was ~1.7% after PDA. XRD showed that ZrO_xN_y films crystallize at a higher temperature (~600-700ºC) than ZrO_2, which crystallized at 400ºC as shown in section 2.3.2.

5.3.3 Comparison of ZrO_2 and ZrO_xN_y NMOSCAP characteristics [20]

As described in section 5.3.1, NMOSCAPs were fabricated and characterized in order to compare the EOT scalability, leakage current, thermal stability, C-V hysteresis, and dielectric strength of ZrO_2 and ZrO_xN_y. Prior to post-TaN annealing, both ZrO_2 and ZrO_xN_y demonstrated comparable scalability with EOTs as low as 9.5Å. Figure 5.11 shows the C-V characteristics of ZrO_2 and ZrO_xN_y MOSCAPs before post-TaN annealing with film thickness ~40Å and EOT of ~10Å; both films exhibited well behaved C-V characteristics. The ZrO_2 C-V was shifted positive relative to the ZrO_xN_y C-V, which was due to negative fixed charge (Q_f) in the ZrO_2. This negative Q_f was compensated for by the positive Q_f resulting from the nitrogen

in the ZrO_xN_y. Conventional oxynitrides also exhibit increased positive Q_f due to nitrogen pile-up at the oxynitride/Si interface [25]. Post-TaN annealing served to reduce Q_f and thus reduce the difference in flat band voltage between the ZrO_2 and ZrO_xN_y MOSCAPs.

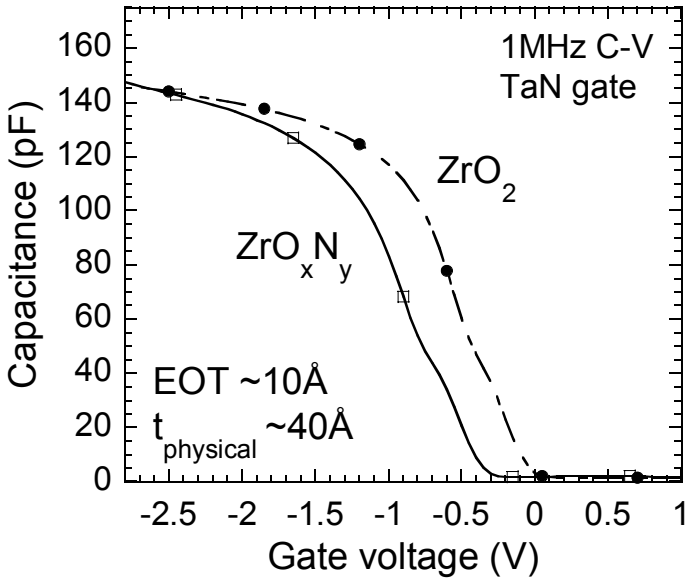

Figure 5.11 C-V curves of ZrO_2 and ZrO_xN_y are well behaved and show EOT ~10Å [20].

The leakage characteristics of the MOSCAPs with EOT ~10Å are shown in figure 5.12. The leakage of ZrO_xN_y was seemingly lower than ZrO_2, but when the difference in flat band voltage (V_{fb}) (seen in figure 5.11) was considered, the two leakages were quite similar. Both showed a leakage of $4x10^{-3}$ A/cm^2 at a gate voltage (V_g) of V_{fb} - 1V, which was quite low considering the low EOT of 10Å. V_{fb} was -0.25V for the ZrO_2 and -0.57V for the ZrO_xN_y. Overall, leakage at $V_g = V_{fb}$ - 1V for ZrO_xN_y and ZrO_2 was comparable for the same EOT values.

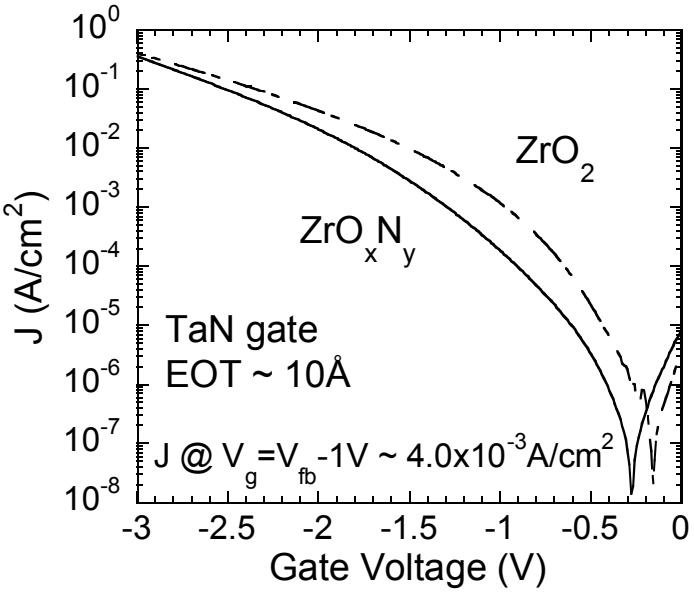

Figure 5.12 J-V curves of ZrO_2 and ZrO_xN_y MOSCAPs show comparable leakage [20].

The EOT scalability of ZrO_2 and ZrO_xN_y was quite comparable prior to post-TaN annealing, but the conventional self-aligned CMOS process requires a high temperature post-electrode anneal for S/D activation. Thus, it is crucial that these films retain their low EOT even after post-TaN annealing. Figure 5.13 shows the EOT of ZrO_2 and ZrO_xN_y for different post-TaN annealing temperatures (700-900ºC). Prior to post-TaN annealing, the EOT of both films was ~10Å, but after 900ºC for 30 seconds, the EOT of the ZrO_2 has increased by ~4Å, whereas the ZrO_xN_y EOT has only increased by ~1Å. Thus, the ZrO_xN_y demonstrated an improved thermal stability over the ZrO_2. This improved thermal stability could be attributed to two factors. The first factor was that the ZrO_xN_y was more resilient to oxygen diffusion during annealing than the ZrO_2. The second factor was that nitrogen-incorporated interfacial layer (IL) of the ZrO_xN_y was less prone to compositional changes during

annealing. In section 2.3.1, it was shown that the IL of ZrO_2 was a Zr-silicate whose Zr concentration decreased with increasing thermal budget. As the Zr concentration decreases, the k of the Zr-silicate also decreases and results in increased EOT. Consequently, if the IL of the ZrO_xN_y was more stable during annealing, the EOT would be more stable as well. M. Koyama, *et al*. reported that the EOT of ZrO_xN_y remained stable even after 1000ºC annealing [19], which bodes well for the integration of ZrO_xN_y into conventional CMOS processing.

As for ZrO_2 and ZrO_xN_y C-V hysteresis, hysteresis vs. post-TaN anneal temperature (700-900ºC) are plotted in figure 5.14. Not surprisingly, hysteresis decreased with increasing annealing temperature since annealing reduced the sputter damage and trapped charge (Q_{ot}) that heavily contribute to hysteresis. ZrO_xN_y demonstrated slightly higher hysteresis than ZrO_2, which was attributed to the increased Q_{ot} resulting from the nitrogen in the ZrO_xN_y. Further evidence of this can be seen in figure 5.15, which shows hysteresis as a function of nitrogen flow rate during Zr sputtering both before and after MOSFET fabrication. Higher nitrogen flow resulted in higher nitrogen concentration in the ZrO_xN_y, and indeed hysteresis increases with increasing flow rate (figure 5.15). However, it should be noted that the hysteresis was drastically reduced after MOSFET fabrication down to fairly low values of 10 mV for ZrO_2 and 30 mV for ZrO_xN_y (N_2 flow rate = 20 sccm). This reduction was primarily due to the high temperature S/D activation annealing (900-950ºC), which reduced Q_{ot}.

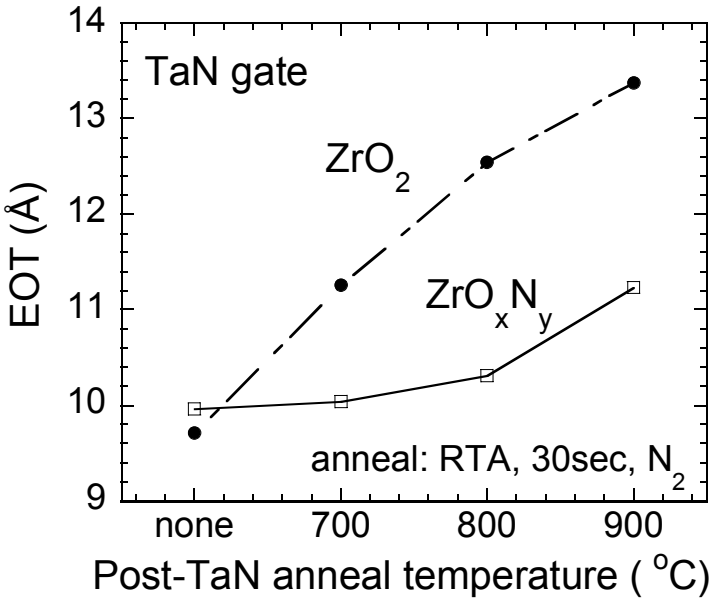

Figure 5.13 EOT vs. post-TaN anneal temperature shows improved thermal stability of ZrO_xN_y over ZrO_2 [20].

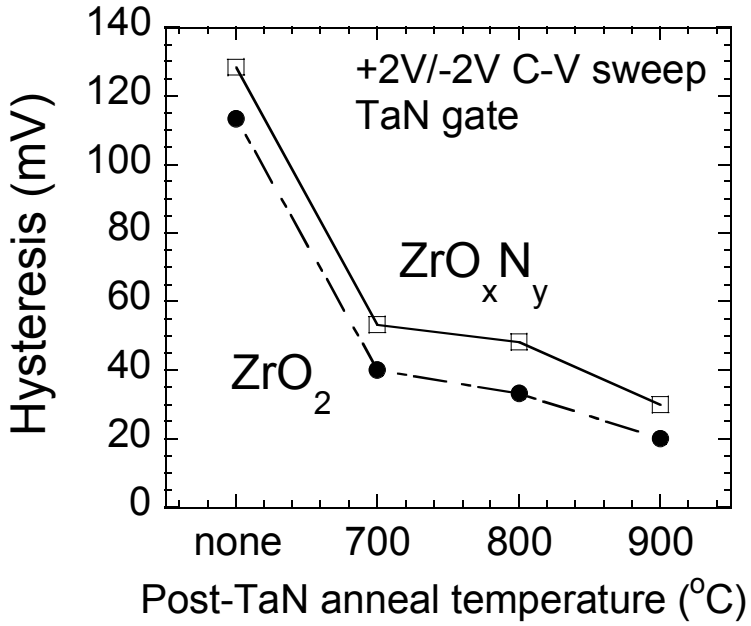

Figure 5.14 Hysteresis vs. post-TaN annealing temperature shows slightly higher hysteresis for ZrO_xN_y [20].

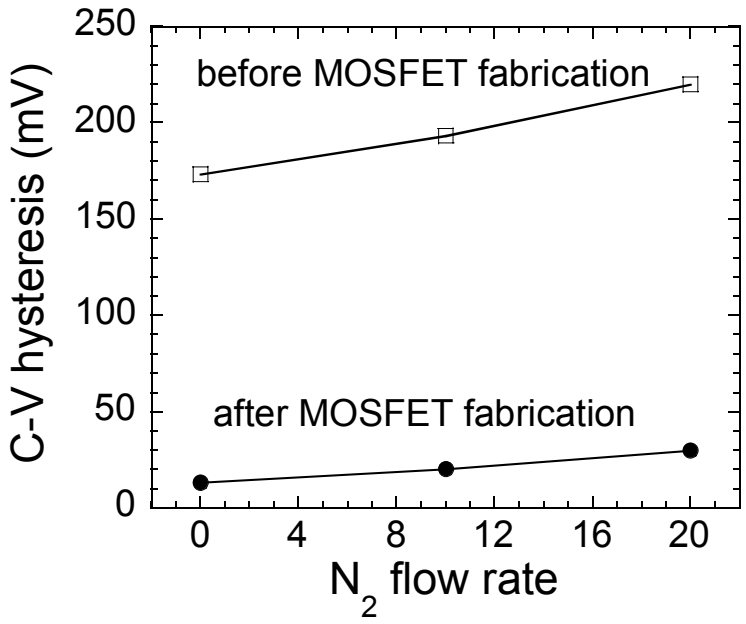

Figure 5.15 Hysteresis vs. N_2 flow rate during Zr sputtering shows increasing hysteresis with increasing nitrogen, and reduced hysteresis after MOSFET fabrication.

To summarize the results on TaN-gated ZrO_2 and ZrO_xN_y NMOSCAPs – these devices were analyzed to compare differences in EOT, leakage, thermal stability during annealing, and hysteresis. Prior to post-TaN annealing, both ZrO_2 and ZrO_xN_y exhibited low EOT (9.5Å) and comparable low leakage. After post-TaN annealing, it was discovered that ZrO_xN_y had improved thermal stability over ZrO_2 due to the nitrogen in the ZrO_xN_y interfacial layer (IL), which helped to prevent IL growth as well as prevent IL compositional changes. Nitrogen in the ZrO_xN_y also resulted in higher Q_{ot} that caused higher C-V hysteresis. In addition nitrogen in the ZrO_xN_y caused higher positive Q_f that actually compensated for the negative Q_f in ZrO_2. Q_f, Q_{ot}, and hysteresis were drastically reduced in both ZrO_2 and ZrO_xN_y after

MOSFET fabrication. These results were promising, and ZrO_xN_y warranted further study in MOSFET devices.

5.3.4 Comparison of ZrO_2 and ZrO_xN_y NMOSFET characteristics [20]

As described in section 5.3.1, long channel NMOSFETs (W/L = 150μ/5μm) were fabricated and characterized in order to compare the electrical characteristics of ZrO_2 and ZrO_xN_y. Figure 5.16 shows MOSFET C-V curves for ZrO_2 and ZrO_xN_y that showed good agreement between accumulation and inversion capacitance. Prior to MOSFET fabrication, these devices both had EOT of 9.5Å. However, after MOSFET fabrication, the EOT of the ZrO_2 increased to 13.8Å while the ZrO_xN_y EOT only increased to 10.3Å. Once again, the ZrO_xN_y demonstrated an improved thermal stability over ZrO_2.

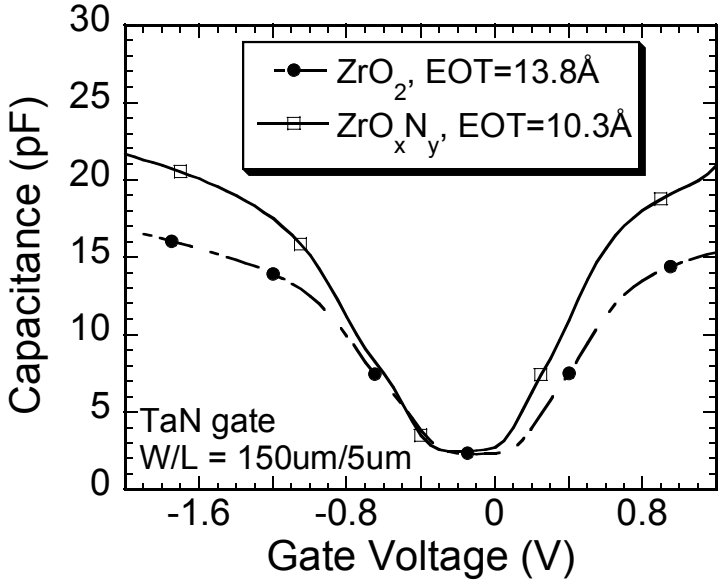

Figure 5.16 NMOSFET C-V curves for ZrO_2 and ZrO_xN_y are well behaved [20].

This thermal stability increased with increasing nitrogen in the ZrO_xN_y film as shown in figure 5.17 which shows the increase in EOT after MOSFET processing versus N_2 flow rate during Zr sputtering.

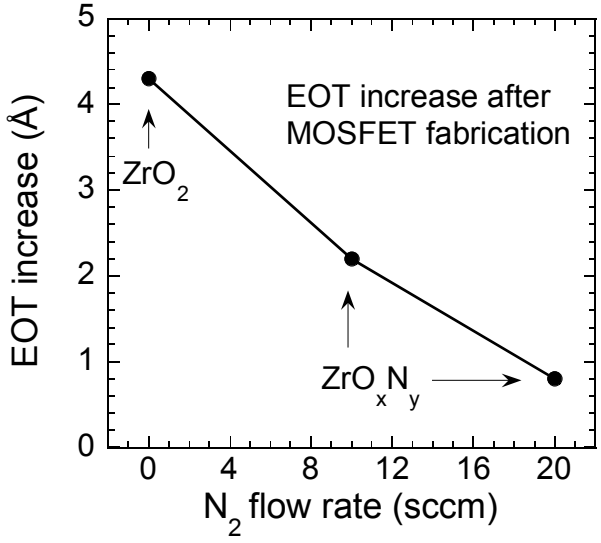

Figure 5.17 The increase in EOT decreases with increasing nitrogen flow rate during Zr sputtering. Prior to MOSFET fabrication, all these devices had EOT = 9.5Å.

To further investigate the thermal stability of these films, high resolution TEM pictures (figure 5.18) of ZrO_2 and ZrO_xN_y after MOSFET fabrication were analyzed. Once again, prior to MOSFET fabrication, these films both had EOT of 9.5Å, but after MOSFET fabrication, the ZrO_2 EOT increased to 13.8Å, and the ZrO_xN_y EOT increased to 10.3Å. From the TEMs, the ZrO_2 and ZrO_xN_y film thicknesses were about the same (~30Å), and the interfacial layer (IL) thicknesses were similar at ~9Å for the ZrO_2 and ~13Å for the ZrO_xN_y. However, since the EOTs of these two samples were so different, it was concluded that the dielectric constant of these two stacks must be different. From the MOSCAP data, it was concluded that the

dielectric constants of ZrO_2 and ZrO_xN_y were quite comparable ~20. Consequently, the k values of the ILs must be different. If one assumed a dielectric constant of 20 for the ZrO_2 and ZrO_xN_y films shown in figure 5.18, then the k of the ZrO_2 IL was ~4.4, and the k of the ZrO_xN_y IL was ~11.4. Thus the IL of ZrO_2 more closely resembled a Zr-silicate with a low Zr concentration, whereas the ZrO_xN_y IL more resembled a nitrogen-doped Zr-silicate with a higher Zr concentration. The difference in k values for the ILs supported the hypothesis that nitrogen in the IL helped to prevent compositional changes in the IL during annealing. The fact that the IL of ZrO_xN_y was actually thicker than the IL of ZrO_2 may be attributed to the migration of nitrogen to the ZrO_xN_y/Si interface during post deposition annealing.

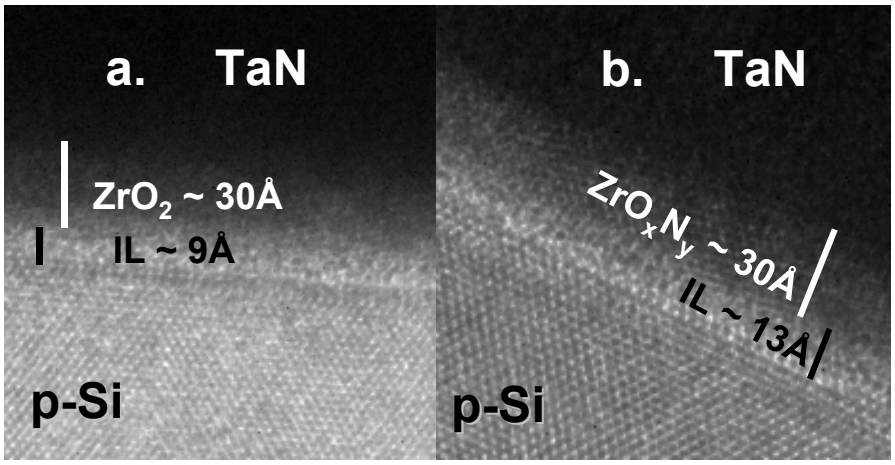

Figure 5.18 TEM pictures of TaN gated (a) ZrO_2 and (b) ZrO_xN_y after MOSFET fabrication. The EOT of the ZrO_2 sample was 13.8Å, and 10.3Å for the ZrO_xN_y sample.

As for other NMOSFET characteristics, figures 5.19 and 5.20 show the I_d-V_g and I_d-V_d curves, respectively, for these devices. Both I_d-V_g and I_d-V_d curves have been normalized to compensate for the difference in EOT between the ZrO_2 (13.8Å) and ZrO_xN_y (10.3Å). From figure 5.19, the ZrO_xN_y shows slightly higher saturation current (I_{dsat}), higher transconductance (G_m), and slightly lower subthreshold swing (S) than ZrO_2. Figure 5.20 also shows higher I_{dsat} for the ZrO_xN_y. These improved characteristics for ZrO_xN_y were unexpected since oxynitrides usually show comparable MOSFET characteristics to SiO_2 [1]. An explanation for these improvements is still under investigation.

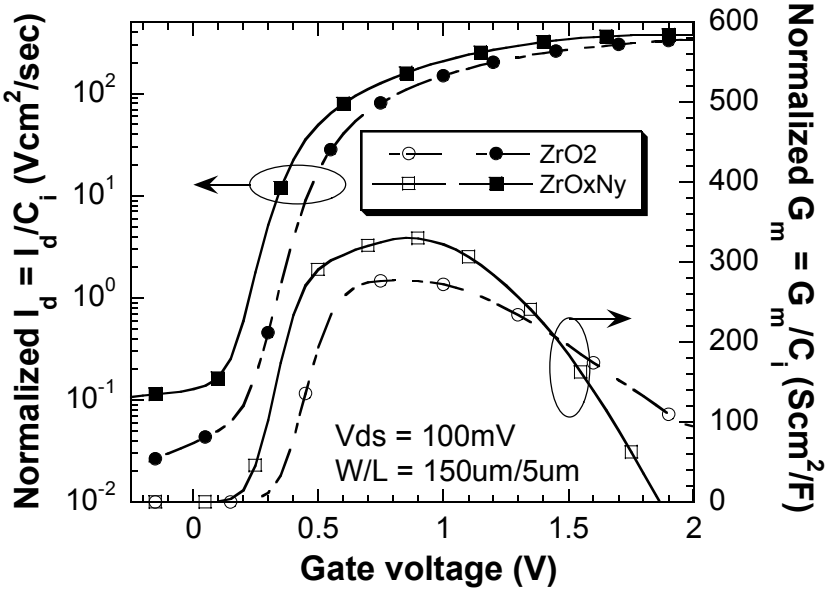

Figure 5.19 Normalized I_d and G_m versus V_g shows improved I_{dsat}, G_m, and S for ZrO_xN_y [20].

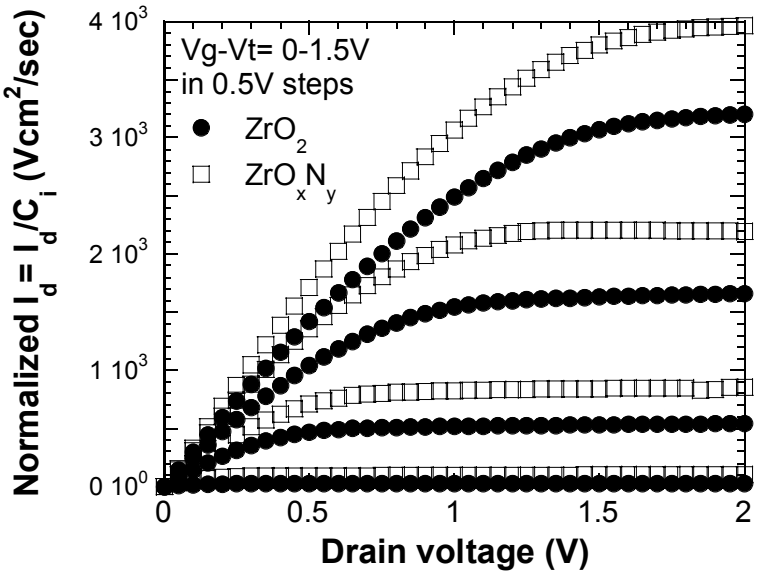

Figure 5.20 Normalized I_d versus V_d shows higher I_{dsat} for ZrO_xN_y [20].

The mobility characteristics for these MOSFETs were calculated using the split C-V method (as described in section 4.2.1) and are shown in figure 5.21. The peak mobility was quite comparable for the ZrO_2 and ZrO_xN_y, but the mobility at high field was higher for ZrO_2, most likely due to surface roughness caused by the nitrogen at the ZrO_xN_y/Si interface. Unfortunately, both ZrO_2 and ZrO_xN_y demonstrated a degraded mobility when compared to the universal curve for SiO_2. This degradation was attributed to the fact that the ZrO_2/Si and ZrO_xN_y/Si interfaces were of lower quality than the interface between Si and thermally grown SiO_2. The ZrO_2 and ZrO_xN_y have higher D_{it}, Q_{ot}, and Q_f than SiO_2 as well. Section 5.4 will further discuss mobility and process changes that led to improved mobility characteristics.

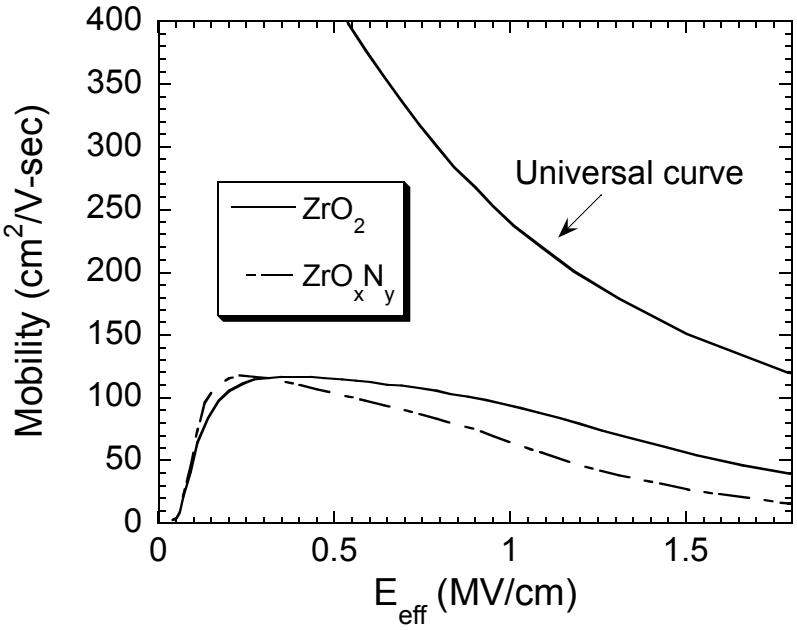

Figure 5.21 Mobility for ZrO_xN_y was lower at high field due to surface roughness caused by the nitrogen at the interface.

To summarize the results on TaN-gated ZrO_2 and ZrO_xN_y NMOSFETs, C-V, EOT scalability, TEM, I_d-V_g, I_d-V_d, and mobility were presented. MOSFET C-Vs were well behaved and showed good agreement between accumulation and inversion capacitance. Once again, ZrO_xN_y demonstrated improved thermal stability with an EOT of 10.3Å, compared to 13.8Å for ZrO_2 after MOSFET fabrication. The TEM revealed that the IL of ZrO_xN_y more resembled a nitrogen-doped Zr-silicate with a higher k than the IL of ZrO_2 that more resembled a lightly Zr-doped SiO_2. I_d-V_g and I_d-V_d revealed higher I_{dsat}, G_m, and lower S for ZrO_xN_y compared to ZrO_2. Finally, mobility was degraded for both ZrO_2 and ZrO_xN_y compared to the universal curve, and ZrO_xN_y demonstrated further degraded mobility at high field due to surface

roughness caused by the nitrogen at the ZrO_xN_y/Si interface. With fairly good MOSFET characteristics, attention was next turned to reliability characteristics.

5.3.5 Comparison of ZrO_2 and ZrO_xN_y reliability characteristics

Various reliability tests were used to evaluate the ZrO_2 and ZrO_xN_y films including ramped voltage tests, constant voltage stress to determine time dependent dielectric breakdown (tddb), and lifetime extrapolation. Ramped voltage tests were performed to test and compare the dielectric strength of the ZrO_2 and ZrO_xN_y. The time zero breakdown (tzbd) tests were performed on MOSCAPs with and without 800ºC post-TaN annealing (figure 5.22) and on MOSCAPs after MOSFET fabrication (figure 5.23). In all cases, the ZrO_xN_y had a higher effective breakdown field (E_{bd}) than ZrO_2 where:

$$E_{bd} = |V_{bd}-V_{fb}|/EOT \qquad (5.1)$$

V_{bd} represents the breakdown voltage, and flat band voltage (V_{fb}) was subtracted from it to compensate for the difference in V_{fb} between ZrO_2 and ZrO_xN_y. It is believed that the breakdown of the IL largely dominates the breakdown of the high-k dielectric stack. As discussed in section 5.3.4, the IL of the ZrO_xN_y more closely resembled a nitrogen-doped Zr-silicate, whereas the IL of the ZrO_2 more resembled a lightly Zr-doped SiO_2. Oxynitrides are known to have improved dielectric strength over SiO_2 [1], so the increased dielectric strength for ZrO_xN_y was likely a result of nitrogen in the IL.

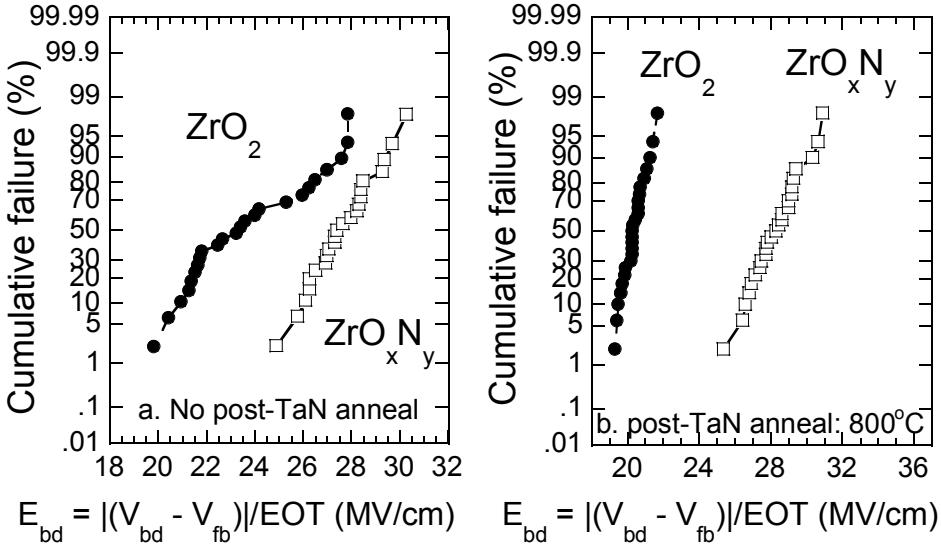

Figure 5.22 Tzbd of ZrO_2 and ZrO_xN_y both (a) before and (b) after post-TaN anneal at 800ºC shows higher breakdown field for ZrO_xN_y [20].

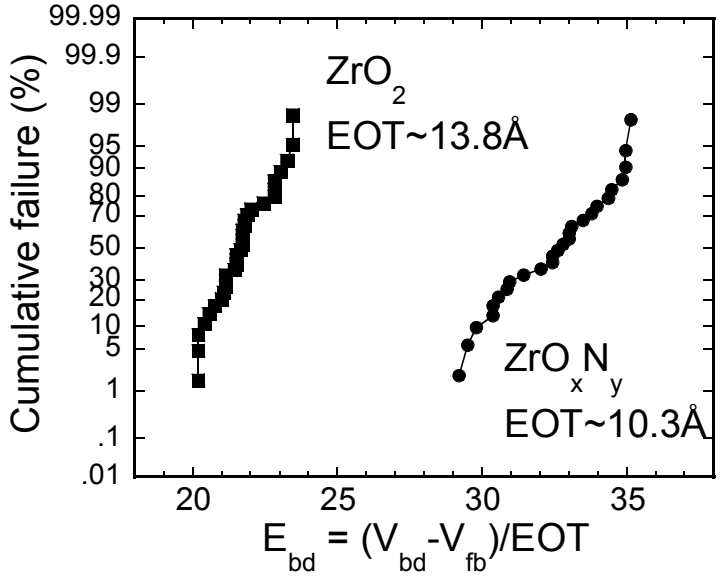

Figure 5.23 Tzbd of ZrO_2 and ZrO_xN_y after MOSFET fabrication shows higher breakdown field for ZrO_xN_y.

Next, some tddb tests were performed. After going through the MOSFET processing, MOSCAPs (area = $1.0x10^{-6}$ cm^2) were stressed at constant voltage until

either the device broke down or after 2000 seconds of stressing. MOSCAP J-V curves were measured before stressing to screen out any initial extrinsic defects. J was also monitored during stressing to ensure consistent behavior from device to device. Approximately 25 MOSCAPs were stressed at each voltage to yield the time-to-breakdown distributions for ZrO_2 and ZrO_xN_y shown in figure 5.24. The ZrO_2 had an EOT of 13.8Å and was stressed from -3.1V to -3.3V; the ZrO_xN_y had an EOT of 10.3Å and was stressed from -3.3V to -3.6V. The ZrO_xN_y exhibited a higher effective breakdown field (E_{eff}) than the ZrO_2, where E_{eff} was defined as:

$$E_{eff} = (V_{stress})/EOT \qquad (5.2)$$

V_{stress} was the stress voltage. From the 50% cumulative failure points in figure 5.24, a lifetime extrapolation was performed using the E-model and is shown in figure 5.25. The 10-year extrapolated operating voltage for ZrO_2 was -2.7V and compared well with values reported elsewhere [26]. For ZrO_xN_y the 10-year operating voltage was slightly lower at -2.4V. However, both of these values were encouraging since the operating voltage will be $\leq$ 1V by the time high-k dielectrics are adopted into manufacturing.

To summarize the reliability characteristics, ZrO_xN_y demonstrated a higher breakdown field than ZrO_2 in tzbd and tddb tests. However, ZrO_2 had a higher predicted 10-year lifetime operating voltage of -2.7V as compared to -2.4V for the ZrO_xN_y. Overall, the reliability characteristics were quite favorable.

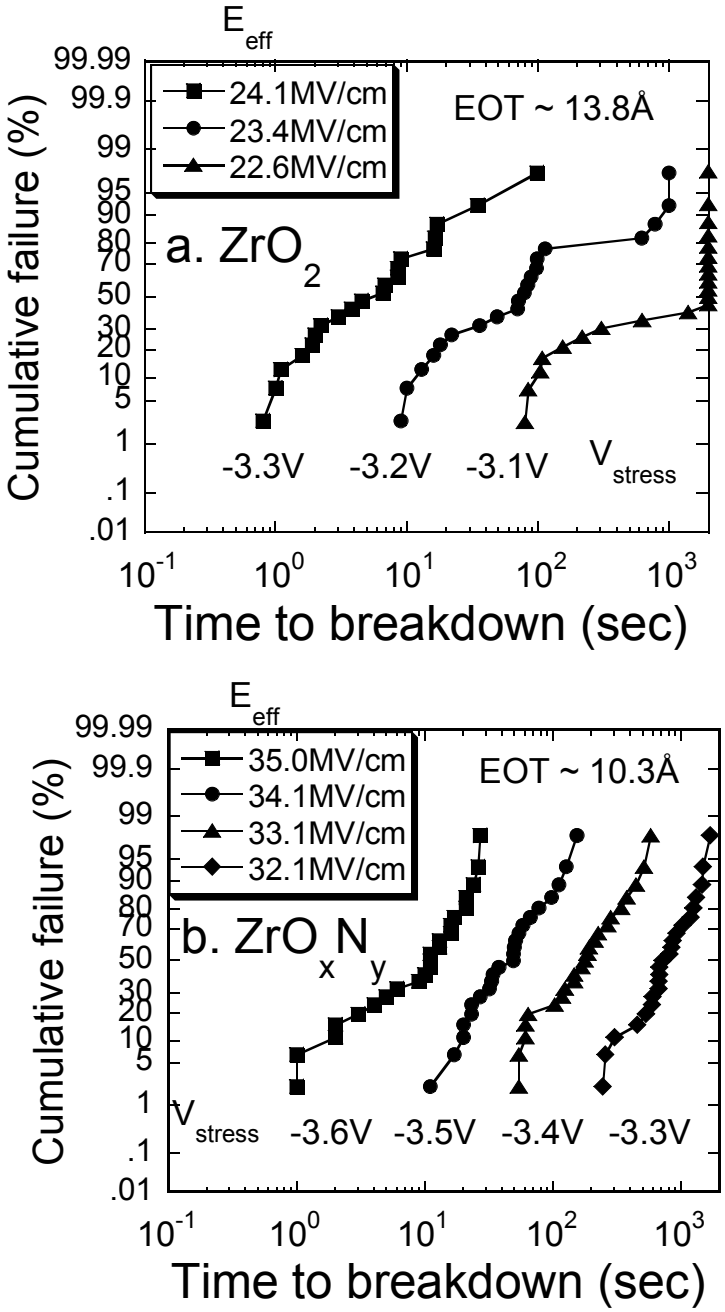

Figure 5.24 Cumulative failure distributions of tddb tests on (a) ZrO_2 and (b) ZrO_xN_y show higher effective breakdown field for ZrO_xN_y.

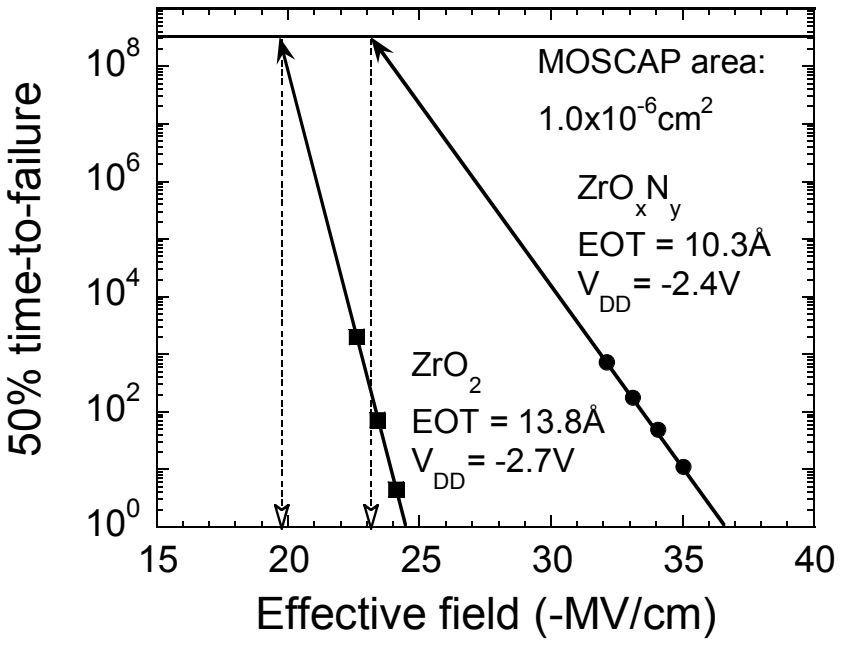

Figure 5.25 10-year lifetime extrapolated operating voltage for ZrO_2 was -2.7V and for ZrO_xN_y was -2.4V.

5.4 High temperature forming gas annealing of ZrO_xN_y NMOSFETs

One the greatest concerns regarding high-k dielectrics is the MOSFET channel mobility. Even if the EOT of these high-k dielectrics can be scaled below 10Å, these benefits are useless if the mobility is drastically degraded. As shown in sections 4.3 and 5.3.4, both ZrO_2 and ZrO_xN_y demonstrated severely degraded mobility compared to the universal curve for SiO_2. Other high-k materials such as HfO_2 [27,28,29] and Al_2O_3 [28] have also exhibited degraded mobility. A few reports have demonstrated relatively high mobility for high-k gate dielectrics [30,31], but these films had fairly thick EOT and probably a thick interfacial layer. Unless

high-k gate dielectrics can boast both low EOT (≤10Å) and a mobility ~80-90% of that of SiO_2, they are not likely to be adopted.

The main reason high-k dielectric mobility is so degraded compared to SiO_2 is the difference in interface quality. These deposited high-k dielectrics have a poorer quality interface with the Si substrate than thermally grown SiO_2. However, the interface quality can be improved by reducing the density of interface states (D_{it}). Onishi, *et al*. proposed a method to reduce D_{it} and thus improve mobility of HfO_2 gate dielectrics by high temperature (500-600ºC) forming gas (FG) annealing of MOSFETs prior to metallization [32]. This FG annealing was found to reduce D_{it} and increase mobility in both NMOSFET and PMOSFET poly-gated devices; peak mobility was increased ~50-85% as compared to samples without the FG treatment [32]. Mobility improvements were also seen for TaN-gated HfO_2 NMOSFETs with a ~75% increase in peak mobility and mobility comparable to the universal curve at high field [33]. These large improvements in mobility prompted the investigation of the effects of high temperature FG anneal on TaN-gated ZrO_xN_y NMOSFETs.

5.4.1 High temperature FG anneal process flow and device measurement

Self-aligned NMOSFETs were fabricated using TaN gate and ZrO_xN_y gate dielectrics as described in table 5.2 with the exception of step 9. Step 14 described the high temperature forming gas (FG) anneal which occurred prior to Al metallization, and was the final anneal step with the exception of the lower temperature sintering in FG at 400ºC (step 18). The high temperature FG (N_2:H_2,

95%:5%) annealing was performed in a conventional furnace at 400ºC, 500ºC, and 600ºC for 30 minutes with a FG flow rate of 10 slm.

After the MOSFET fabrication process, the C-V, J-V, hysteresis, and tzbd characteristics of MOSCAPs were measured as described in section 5.3.1. MOSFET characteristics such as I_d-V_g, transconductance (G_m), and mobility were also measured as outlined in section 5.3.1.

5.4.2 NMOSCAP/NMOSFET characteristics after high temperature FG anneal

Not only was the evaluation of the FG annealing effects on the mobility of interest, but the possible advantageous/disadvantageous effects on other characteristics as well. One concern was that the fairly long (30 minute) anneal would cause EOT increase due to interfacial layer (IL) growth. After MOSFET fabrication, these ZrO_xN_y (~42Å) devices demonstrated an EOT of 11.6Å. From figure 5.26, it can be seen that 500ºC and 600ºC FG annealing did not affect the EOT, and in fact, improved the C-V characteristics. The inset to figure 5.26 shows that the C-V slope was steeper with increasing FG anneal temperature, indicating a decreased D_{it} with increasing FG anneal temperature.

The leakage characteristics for these ZrO_xN_y (~42Å) MOSCAPs were also quite comparable and well behaved for no anneal, 500ºC, and 600ºC FG annealing (figure 5.27). The leakage for these devices was ~9.0×10^{-3} A/cm^2 at $V_g=V_{fb}$-1V, which was reasonable considering the EOT of 11.6Å.

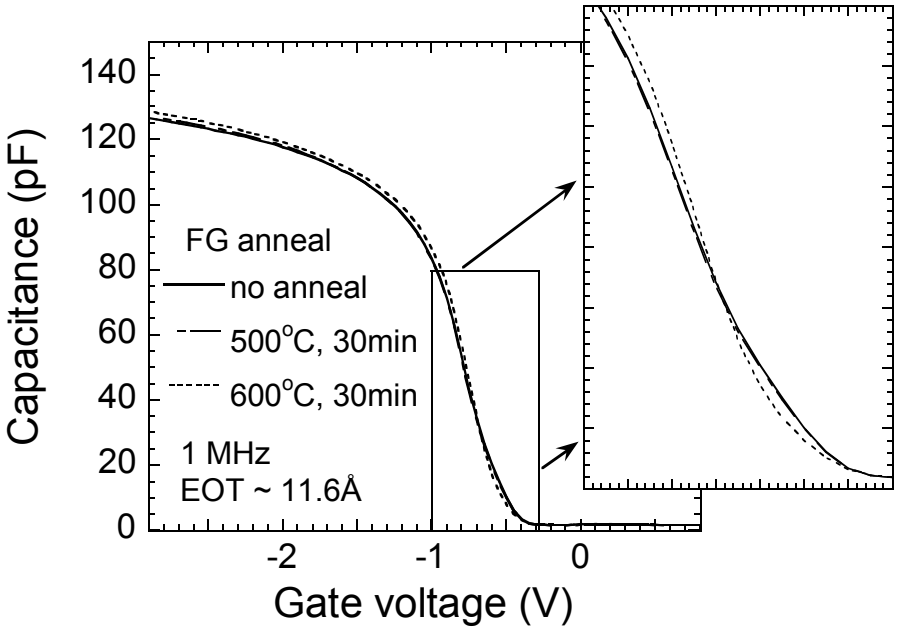

Figure 5.26 C-V curves show same EOT (11.6Å) for ZrO_xN_y with no anneal, 500ºC, and 600ºC FG annealing. Inset shows steeper C-V slope with increasing FG anneal temperature.

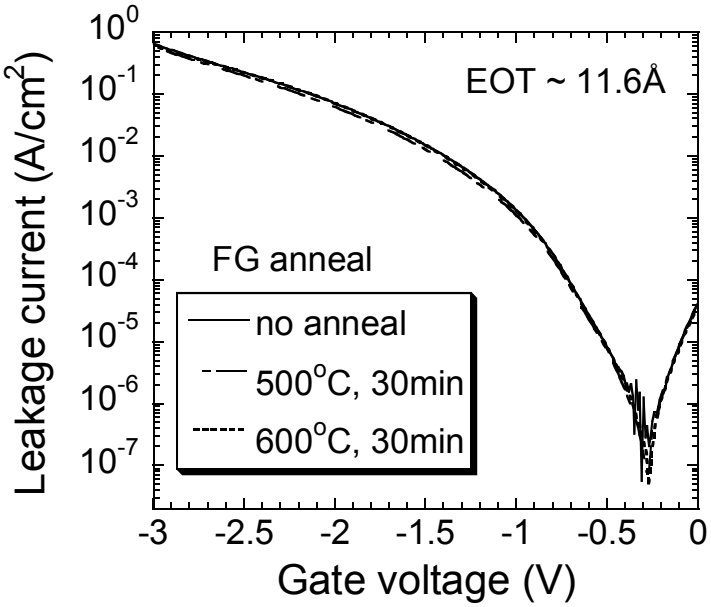

Figure 5.27 J-V curves show comparable leakage for ZrO_xN_y with no anneal, 500ºC, and 600ºC FG annealing.

One concern when using hydrogen (FG) annealing was the addition of hydrogen related traps in the dielectric. Additional trapped charge (Q_{ot}) in these ZrO_xN_y (~42Å) films would result in increased C-V hysteresis [11]. Thus hysteresis was evaluated for no anneal, 400ºC, 500ºC, and 600ºC samples. Figure 5.28 shows that the hysteresis values were actually quite comparable for all the samples at 22-29 mV, indicating that the FG anneal did not affect the hysteresis adversely.

Ramped voltage tests were performed in order to compare the tzbd characteristics of the samples (figure 5.29). Once again, the no anneal, 500ºC, and 600ºC FG annealed samples all showed comparable tzbd characteristics with fairly high effective breakdown field (E_{bd}) of 22-32 MV/cm as defined in equation 5.1.

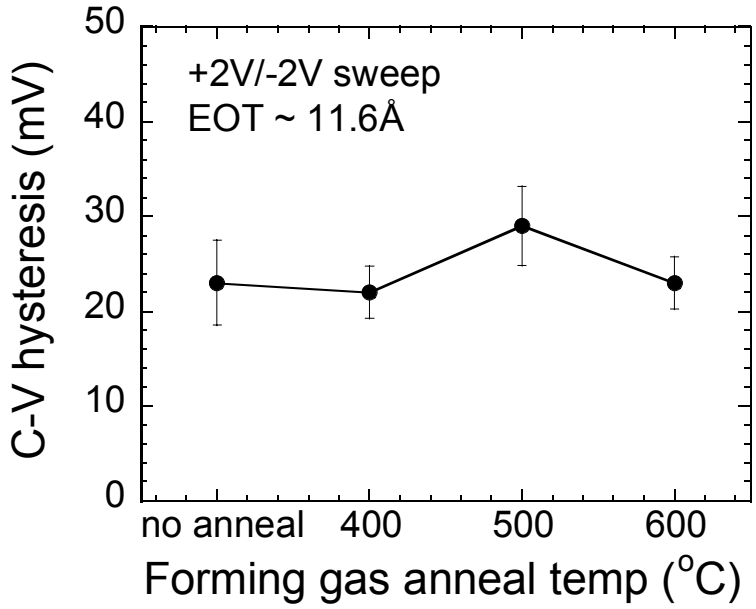

Figure 5.28 C-V hysteresis of ZrO_xN_y after no anneal, 500ºC, and 600ºC FG annealing was comparable.

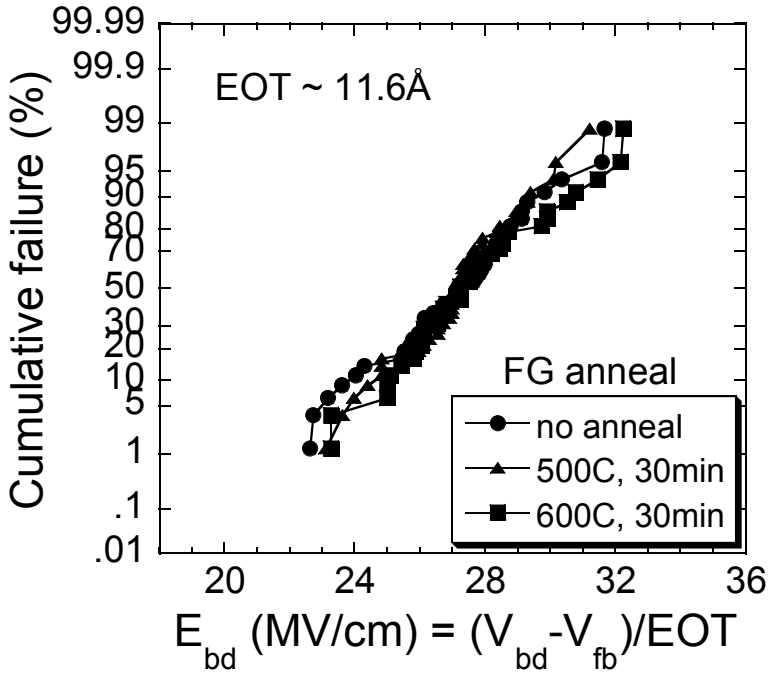

Figure 5.29 Tzbd characteristics of ZrO_xN_y after no anneal, 500ºC, and 600ºC FG annealing were similar.

Finally, NMOSFET characteristics were analyzed to determine the effects of the high temperature FG anneal. The I_d-V_g characteristics are shown in figure 5.30 and demonstrate several improvements of the FG treatment. First, the off-state leakage current was reduced with increased FG annealing temperature. Next, the subthreshold swing (S) was greatly reduced from 96 mV/decade with no FG anneal down to 69 mV/decade with 600ºC FG annealing. A subthreshold swing value of 60 mV/decade is the D_{it}-free ideal value, so the FG anneal has removed much of the D_{it} in these films. Figure 5.31 shows the transconductance (G_m) from these MOSFET devices, and once again improvements were observed for the FG annealed samples. Higher FG anneal temperature resulted in higher G_m.

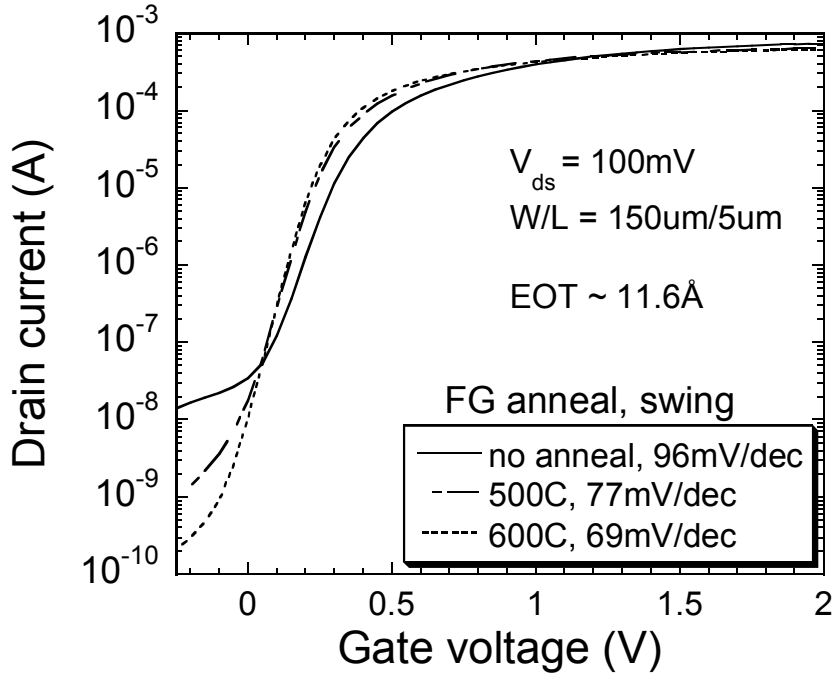

Figure 5.30 Higher temperature FG annealing helped to reduce off-state leakage current and to decrease subthreshold swing in TaN/ZrO_xN_y MOSFETs.

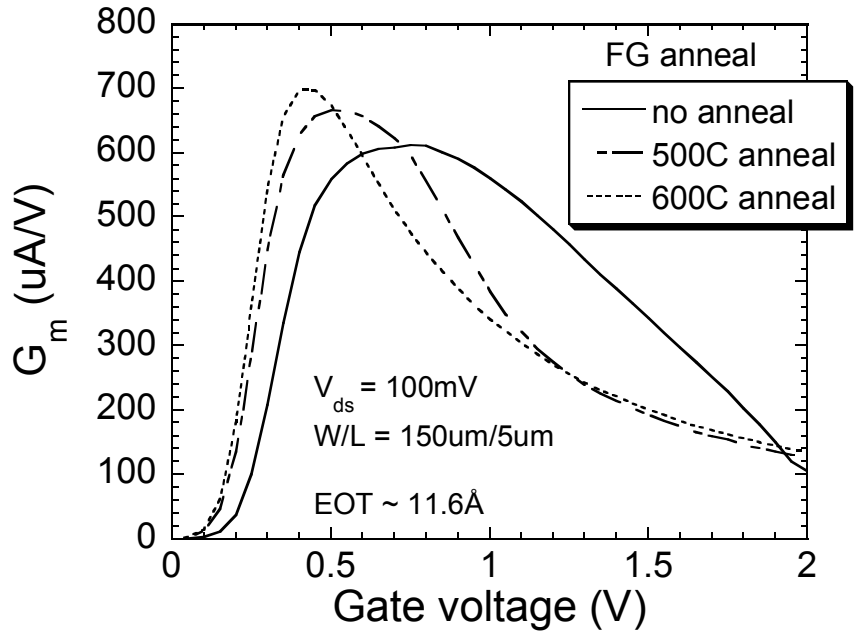

Figure 5.31 Higher temperature FG annealing helped to increase transconductance in TaN/ZrO_xN_y MOSFETs.

Using the split C-V method, the mobility characteristics were evaluated for these ZrO_xN_y (~42Å) films (figure 5.32). As expected from the I_d-V_g characteristics, the mobility was improved considerably with increasing FG annealing temperature. The peak mobility was only 97 cm^2/V-sec with no FG anneal and increased by almost 400% to 383 cm^2/V-sec after 600ºC FG annealing. The mobility at high field (E_{eff}) was also increased similarly for the 500ºC and 600ºC FG annealed samples. These increased mobility values were extremely promising, although they still fell short of the universal curve. With further optimization of the high temperature FG anneal process, ZrO_xN_y may achieve the industry goal of ~80-90% the mobility of SiO_2.

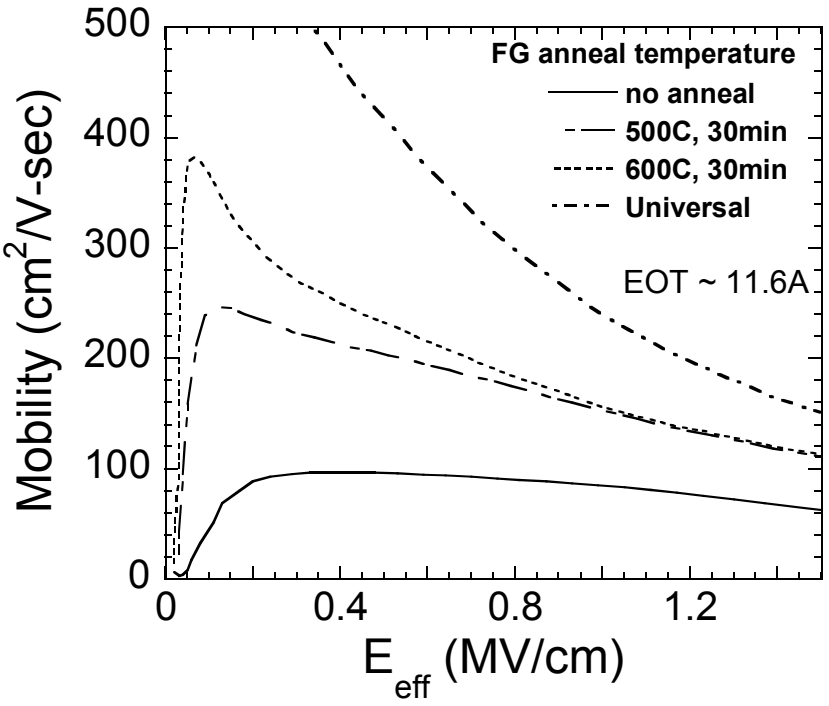

Figure 5.32 Mobility of ZrO_xN_y was appreciably enhanced after high temperature FG annealing.

5.5 Summary

Chapter 5 presented the electrical, material, and reliability characteristics of ZrO_2 with nitrogen incorporated into the dielectric stack. Two methods of nitrogen incorporation were discussed – NH_3 Si surface nitridation (SN) prior to ZrO_2 deposition and nitrogen-incorporated ZrO_2 (ZrO_xN_y) via reactive sputtering of Zr in Ar and N_2. The motivations behind nitrogen incorporation into the gate dielectric stack were possible improvements in thermal stability and thus EOT scalability, reduced leakage, improved reliability, prevention of boron penetration, and higher crystallization temperature.

For the SN evaluation, TaN-gated NMOSCAPs were fabricated and characterized. It was discovered that the SN samples had improved thermal stability (lower EOT) and comparable leakage with non-nitrided samples. In addition, the IL of SN samples was actually thicker than that of non-nitrided samples, but the SN IL had a higher dielectric constant than the non-nitrided IL. Thus the SN IL was a nitrogen-incorporated Zr-silicate with higher Zr concentration than that of the non-nitrided IL Zr-silicate. The main drawback to the SN process was increased trapped charge (Q_{ot}) that resulted in increased C-V hysteresis. These increased charges were a result of the hydrogen-related traps from the NH_3 decomposition as well as the nitrogen in the IL. With further process optimization, Q_{ot} could be reduced, and with the EOT scaling advantage and increased thermal stability, SN may find an application in the MOS process.

Next nitrogen-incorporated ZrO_2 or ZrO_xN_y was evaluated using both TaN gated NMOSCAPs and self-aligned NMOSFETs. Angle resolved XPS demonstrated that the ZrN was completely converted to ZrO_xN_y after post deposition annealing (PDA). XPS analysis also showed that there was ~1.7% nitrogen in the ZrO_xN_y after PDA and most of it was located near the ZrO_xN_y/Si interface. XRD revealed that the ZrO_xN_y films crystallized at a higher temperature (~600-700º) than ZrO_2 (~400ºC). Evaluation of MOSCAPs revealed that both ZrO_2 and ZrO_xN_y had comparable EOT scalability (<10Å) and leakage current prior to any post-TaN annealing. However, after post-TaN annealing, the ZrO_xN_y demonstrated an improved thermal stability over the ZrO_2. C-V hysteresis was slightly higher for ZrO_xN_y than ZrO_2 due to increased Q_{ot} caused by the nitrogen in the film. However, after MOSFET fabrication, the hysteresis was reduced to 10 mV for the ZrO_2 and 30 mV for the ZrO_xN_y. Finally, the positively charged Q_f caused by the nitrogen in the ZrO_xN_y compensated for the negatively charged Q_f in the ZrO_2.

ZrO_2 and ZrO_xN_y NMOSFETs demonstrated well-behaved characteristics. Although both films started with an EOT of 9.5Å prior to MOSFET fabrication, the improved thermal stability of the ZrO_xN_y resulted in lower EOT for the ZrO_xN_y of 10.3Å as compared to 13.8Å for the ZrO_2. TEM pictures revealed that the increased thermal stability of the ZrO_xN_y was due to two factors: reduced oxygen diffusion through the dielectric and resistance to compositional changes of the interfacial layer (IL) during annealing. Similar to the SN samples, the IL of the ZrO_xN_y was a nitrogen-incorporated Zr-silicate with higher Zr concentration and thus higher k than

that of the Zr-silicate IL of ZrO_2. I_d-V_g and I_d-V_d characteristics revealed that the ZrO_xN_y had higher I_{dsat}, higher transconductance, and lower swing than the ZrO_2. Peak mobility for the ZrO_2 and ZrO_xN_y MOSFETs was similar, although the ZrO_2 did yield a higher mobility at high field due to the surface roughness caused by nitrogen in the ZrO_xN_y. Reliability characterization revealed higher dielectric strength and breakdown field for the ZrO_xN_y than the ZrO_2. Extrapolated 10-year lifetime operating voltages from tddb tests were -2.7V for ZrO_2 and -2.4V for ZrO_xN_y.

Finally, improvements to HfO_2 MOSFET characteristics and mobility using high temperature (500-600ºC) forming gas (FG) annealing [32,33] prompted similar experiments using ZrO_xN_y. High temperature FG annealing prior to MOSFET metallization had no adverse effects on EOT, leakage, hysteresis, and breakdown field strength. However, FG annealed MOSFETs did have reduced D_{it}, which resulted in reduced swing (69 mV/decade), reduced off-state leakage current, higher transconductance, and higher mobility. These improved characteristics indicate that there is great promise for adoption of the high temperature FG anneal process with high-k gate dielectrics. Further optimization of the FG annealing process will likely lead to further improvements in mobility.

In conclusion, the two nitrogen incorporation techniques – SN and ZrO_xN_y – demonstrated many advantages over ZrO_2 including increased thermal stability, and thus EOT scalability. The disadvantages of the nitrogen incorporation techniques were the increased Q_{ot}, and D_{it}, although these may be controllable with process optimization. The high temperature FG annealing showed extremely good

characteristics including a reduction in D_{it}, which lead to increased mobility. Both the ZrO_2 nitrogen incorporation techniques and the high temperature FG annealing merit further study and optimization in order to apply them in MOS technology.

5.6 References

[1] T. Hori, *Gate Dielectrics and MOS ULSIs: Principles, Technologies, and Applications*, (Springer, Berlin, 1997).

[2] M. Fujiwara, M. Takayanagi, T. Shimizu, and Y. Toyoshima, "Extending Gate Dielectric Scaling Limit by NO Oxynitride: Design and Process Issues for Sub-100nm Technology," International Electron Devices Meeting, IEDM Technical Digest, p. 227, 2000.

[3] A. Chou, "Development of thin gate and tunnel dielectrics for MOS applications," Ph.D. dissertation, The University of Texas at Austin, 1997.

[4] A.G. Lucas, "The growth of oxynitrides and their use as gate dielectrics," Master's Thesis. The University of Texas at Austin, 1999.

[5] S. Gopalan, R. Choi, K. Onishi, R. Nieh, C.S. Kang, H.-J. Cho, S. Krishnan, and J.C. Lee, "Impact of NH_3 pre-treatment on the electrical and reliability characteristics of ultra thin hafnium silicate films prepared by re-oxidation method," Device Research Conference (DRC) proceedings, p. 195, 2002.

[6] R. Choi, C.S. Kang, B.H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J.C. Lee, "High-Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation," Technical Digest of Symposium on VLSI Technology, p. 15, 2001.

[7] P.D. Kirsch, C.S. Kang, J. Lozano, L.C. Lee, and J.G. Ekerdt, "Electrical and spectroscopic comparison of HfO_2/Si interfaces on nitrided and un-nitrided Si(100)," Journal of Applied Physics, vol. 91, no. 7, p. 4354, 2002.

[8] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C.S. Kang, B.H. Lee, R. Nieh, and J.C. Lee, "Dopant Penetration Effects on Polysilicon Gate HfO_2 MOSFETs," Technical Digest of Symposium on VLSI Technology, p. 131, June 2001.

[9] Q. Lu, H. Takeuchi, R. Lin, T.-J. King, C. Hu, K. Onishi, R. Choi, C.S. Kang, and J.C. Lee, "Hot Carrier Reliability of n-MOSFET with Ultra-thin HfO_2 Gate Dielectric and Poly-Si Gate," International Reliability Physics Symposium (IRPS) Proceedings, p. 429, 2002.

[10] R. Nieh, R. Choi, S. Gopalan, K. Onishi, C.S. Kang, H.-J. Cho, S. Krishnan, and J.C. Lee, "Evaluation of Silicon Surface Nitridation Effects on Ultra-thin ZrO_2 Gate Dielectrics," accepted to be published in Applied Physics Letters, 2002.

[11] D.M. Fleetwood, "Fast and Slow Border Traps in MOS Devices," IEEE Transactions on Nuclear Science, vol. 43, no. 2, p. 779, 1996.

[12] S.M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1982).

[13] C.H. Lee, H.F. Luan, W.P. Bai, S.J. Lee, T.S. Jeon, Y. Senzaki, D. Roberts, and D.L. Kwong, "MOS Characteristics of Ultra Thin Rapid Thermal CVD ZrO_2 and Zr Silicate Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 27, 2000.

[14] C.M. Perkins, B.B. Triplett, P.C. McIntyre, K.C. Saraswat, S. Haukka, and M. Tuominen, "Electrical and materials properties of ZrO_2 gate dielectrics grown by atomic layer chemical vapor deposition," Applied Physics Letters, vol. 78, no. 16, p. 2357, 2001.

[15] S. Ramanathan, G.D. Wilk, D.A. Muller, C.-M. Park, and P.C. McIntyre, "Growth and characterization of ultrathin zirconia dielectrics grown by ultraviolet ozone oxidation," Applied Physics Letters, vol. 79, no. 16, p. 2621, 2001.

[16] C.S. Kang, H.-J. Cho, K. Onishi, R. Choi, R. Nieh, S. Gopalan, S. Krishnan, and J.C. Lee, "Improved Thermal Stability and Device Performance of Ultra-thin (EOT less than 10Å) Gate Dielectric MOSFETs by using Hafnium Oxynitride (HfO_xN_y)," Technical Digest of Symposium on VLSI Technology, p. 146, 2002.

[17] H.-J. Cho, C.S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, S. Krishnan, and J.C. Lee, "Structural and Electrical Properties of HfO_2 with Top Nitrogen Incorporated Layer," IEEE Electron Device Letters, vol. 23, no. 5, p. 249, 2002.

[18] H.-J. Cho, C.S. Kang, K. Onishi, S. Gopalan, R. Nieh, E. Dharmarajan, and J.C. Lee, "Novel Nitrogen Profile Engineering for Improved TaN/HfO_2/Si MOSFET Performance," International Electron Devices Meeting, IEDM Technical Digest, p. 665, 2001.

[19] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo, and A. Nishiyama, "Thermally Stable Ultra-Thin Nitrogen Incorporated ZrO_2 Gate Dielectric Prepared by Low Temperature Oxidation of ZrN," International Electron Devices Meeting, IEDM Technical Digest, p. 459, 2001.

[20] R. Nieh, S. Krishnan, H.-J. Cho, C.S. Kang, S. Gopalan, K. Onishi, R. Choi, and J.C. Lee, "Comparison between ultra-thin ZrO_2 and ZrO_xN_y gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices," Technical Digest of Symposium on VLSI Technology, p. 186, 2002.

[21] W.J. Qi, "Study on High-k Dielectrics as Alternative Gate Insulators for 0.1μm and Beyond ULSI Applications," Ph.D. dissertation, The University of Texas at Austin, 2000.

[22] L. Manchanda, M.L. Green, R.B. van Dover, M.D. Morris, A. Kerber, Y. Hu, J.-P. Han, P.J. Silverman, T.W. Sorsch, G. Weber, V. Donnelly, K. Pelhos, F. Klemens, N.A. Ciampa, A. Kornblit, Y.O. Kim, J.E. Bower, D. Barr, E. Ferry, D. Jacobson, J. Eng, B. Busch, and H. Schulte, "Si-doped Aluminates for High Temperature Metal-Gate CMOS: Zr-Al-Si-O, A Novel Gate Dielectric for Low Power Applications," International Electron Devices Meeting, IEDM Technical Digest, p. 23, 2000.

[23] L. Manchanda, B. Busch, M.L. Green, M. Morris, R.B. van Dover, R. Kwo, and S. Aravamudhan, "High K Gate Dielectrics for the Silicon Industry," Extended Abstracts of International Workshop on Gate Insulator (IWGI), p. 56, 2001.

[24] W. Zhu, T.P. Ma, T. Tamagawa, Y. Di, J. Kim, R. Carruthers, M. Gibson, and T. Furukawa, "HfO_2 and HfAlO for CMOS: Thermal Stability and Current Transport," International Electron Devices Meeting, IEDM Technical Digest, p. 463, 2001.

[25] Y. Suizu, "Reexamination of the Role of Nitrogen in Oxynitrides – Fixed Charge Reduction in the p^+-Polysilicon Gate MOS," IEEE Transactions on Electron Devices, vol. 48, no. 12, p. 2777, 2001.

[26] W.-J. Qi, R. Nieh, B.H. Lee, L. Kang, Y. Jeon, K. Onishi, S. Gopalan, and J.C. Lee, "Temperature Effect on the Reliability of ZrO_2 Gate Dielectric Deposited Directly on Silicon," International Reliability Physics Symposium (IRPS) Proceedings, p. 72, 2000.

[27] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, E. Dharmarajan, and J.C. Lee, "Reliability Characteristics, including NBTI, of Polysilicon Gate MOSFETs," International Electron Devices Meeting, IEDM Technical Digest, p. 659, 2001.

[28] E.P. Gusev, D.A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P.C. Jamison, D.A. Neumayer, M. Copel, M.A. Gribelyuk,

H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L-A. Ragnarsson, P. Ronsheim, K. Rim, R.J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin high-K gate stacks for advanced CMOS devices," International Electron Devices Meeting, IEDM Technical Digest, p. 451, 2001.

[29] S.J. Lee, H.F. Luan, C.H. Lee, T.S. Jeon, W.P. Bai, Y. Senzaki, D. Roberts, and D.L. Kwong, "Performance and Reliability of Ultra Thin CVD HfO_2 Gate Dielectrics with Dual Poly-Si Gate Electrodes," Technical Digest of Symposium on VLSI Technology, p. 133, 2001.

[30] W.-J. Qi, R. Nieh, B.H. Lee, K. Onishi, L. Kang, Y. Jeon, J.C. Lee, V. Kaushik, B.-Y. Nguyen, L. Prabhu, K. Eigenbeiser, and J. Finder, "Performance of MOSFETs with ultra thin ZrO_2 and Zr silicate gate dielectrics," Technical Digest of Symposium on VLSI Technology, p. 40, 2000.

[31] A. Chin, C.C. Liao, C.H. Lu, W.J. Chen, and C. Tsai, "Device and Reliability of High-k Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}," Technical Digest of Symposium on VLSI Technology, p. 135, 1999.

[32] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J.C. Lee, "Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," Technical Digest of Symposium on VLSI Technology, p. 22, 2002.

[33] R. Choi, K. Onishi, C.S. Kang, R. Nieh, S. Gopalan, H.-J. Cho, S. Krishnan, and J.C. Lee, "High Quality MOSFETs Fabrication with HfO_2 Gate Dielectric and TaN Gate Electrode," Device Research Conference (DRC) proceedings, p. 193, 2002.

CHAPTER 6

Conclusion and future work

6.1 Summary and conclusion

MOS technology has steadily advanced in the past 30 years with transistor gate lengths shrinking exponentially each device generation (1.5-2 years). Each new device generation presents new challenges, and these have been overcome with the introduction of new materials, processes, and tools. The 90 nm node will face new problems such as SiO_2 scaling limits, the polysilicon depletion effect, and the quantum mechanical effect. With a SiO_2 dielectric only a few monolayers thick (~11-15Å), excessive gate leakage and reliability issues become huge concerns. In addition, the poly depletion effect and quantum mechanical effect will add a few angstroms of equivalent oxide thickness (EOT), making scaling even harder.

Oxynitrides or oxide/nitride stacks will serve as replacements for SiO_2 for a generation or two, but ultimately, high dielectric constant or high-k materials will have to be adopted as the gate dielectric material. One of the most promising among the high-k candidates is zirconium oxide (ZrO_2) due to its thermal stability on silicon, dielectric constant (~20), reasonable bandgap (~5.8 eV) and barrier height (1.4 eV for electrons and 3.3 eV for holes). In addition, ZrO_2 has demonstrated scalable EOT $\leq$ 10Å and low gate leakage current.

For this study, ZrO_2 was deposited via DC sputtering of Zr followed by a post deposition anneal (PDA) to fully oxidize and densify the ZrO_2. The deposition process – sputtering and PDA – was optimized to yield both low EOT and low leakage current. It was discovered that the despite the thermal stability of ZrO_2 on Si, an interfacial layer (IL) was formed during the fabrication process. This IL was composed of a Zr-silicate, whose Zr content decreased with increasing thermal budget. Despite the fact that ZrO_2 crystallized after 400ºC annealing, the ZrO_2 surface roughness was smooth (~1Å rms) after 600ºC PDA. Platinum (Pt) was used as an evaluation gate electrode, and low EOT (8.2Å), negligible frequency dispersion, manageable C-V hysteresis, and low leakage were achieved.

Because polysilicon gate electrodes are currently used in MOS technology, there is great interest in demonstrating a compatibility between poly gate and high-k dielectrics. Unfortunately, poly gate electrodes were investigated and found to be incompatible with ZrO_2. During poly deposition, the ZrO_2 films were reduced to form Zr-rich films; then, during poly implant activation annealing, patches of Zr-silicide were formed, which resulted in extremely high gate leakage – even higher than poly/SiO_2 at the same EOT. Several possible solutions were explored in order to combat the oxygen reduction of the ZrO_2 films. The solutions included changing the ZrO_2 PDA conditions, changing the poly deposition process conditions, lowering the poly implant activation anneal temperature, depositing a layer of sputtered Si prior to poly deposition, and replacing the ZrO_2 with ZrO_xN_y. Unfortunately, none of these solutions yielded low EOT (< 18Å) and all of them yielded high leakage. Thus, it

was concluded that ZrO_2 and ZrO_xN_y were not compatible with the poly process and that attention should be focused on metal gate electrode.

Although poly gates have been successfully used in current MOS technology, the poly depletion effect will eventually force the replacement of poly with dual metal gate electrodes. Due to its thermal stability and low resistivity, tantalum nitride (TaN) is one of the more promising candidates for NMOS metal gate electrode. In addition it has demonstrated compatibility with several high-k candidates including ZrO_2, HfO_2, and their silicates. TaN gate electrodes were deposited using reactive sputtering of Ta in an Ar and N_2 ambient, and patterned in a reactive ion etch (RIE) using CF_4. These TaN electrodes exhibited low sheet resistance (10-25 Ω/square) and thermal stability during MOSFET processing. Both MOSCAPs and NMOSFETs were fabricated using TaN gate and ZrO_2.

TaN-gated MOSCAPs demonstrated low EOT (9.8Å), negligible frequency dispersion, and low leakage current. Post-TaN annealing served to reduce negative fixed charge (Q_f), oxide trapped charge (Q_{ot}), and density of interface states (D_{it}), which led to a negative V_{fb} shift, lower C-V hysteresis, and steeper C-V curves, respectively. Hysteresis was caused by positive Q_{ot} near the ZrO_2/Si interface. Hysteresis was more affected by negative bias since traps were filled at negative bias, although there was some detrapping during positive bias. TaN-gated NMOSFETs (W/L = 150μm/5μm) also yielded good characteristics such as low EOT (11.3Å), low hysteresis (10mV), relatively low leakage current, high breakdown field, and well

behaved C-V, I_d-V_g, and I_d-V_d characteristics. Mobility was degraded compared to the universal curve for SiO_2, but could be improved along with subthreshold swing and drive current with high temperature (500-600ºC) forming gas annealing. Overall, TaN/ZrO_2 devices yielded good characteristics and merited further study.

Finally, nitrogen incorporation into the ZrO_2 stack was investigated using two methods – Si surface nitridation (SN) prior to ZrO_2 deposition and nitrogen-incorporated ZrO_2 (ZrO_xN_y). The motivation was that the nitrogen in the stack might help to improve thermal stability, prevent/reduce boron penetration, reduce leakage current, improve reliability, and increase the crystallization temperature.

Surface nitridation (SN) was introduced via rapid thermal annealing in ammonia (NH_3) prior to ZrO_2 deposition to form a thin silicon nitride layer. TaN/ZrO_2 MOSCAPs were fabricated with the SN technique and characterized. Samples with SN had lower EOT (8.7Å), higher C-V hysteresis, and similar leakage compared to samples without nitridation. Lower EOT was attributed to the interfacial layer (IL) of SN samples, which had a higher dielectric constant than the IL of non-nitrided samples. Thus, the IL of SN samples was less prone to further growth and compositional changes during annealing. The increased C-V hysteresis was due to the increased Q_{ot} cause by hydrogen-related traps from the decomposition of the NH_3. Overall, results from SN MOSCAPs were promising, but more work remains to done including analysis of MOSFET behavior.

ZrO_xN_y was deposited via reactive sputtering of ZrN in Ar and N_2 followed by post deposition annealing (PDA) to convert the films to ZrO_xN_y. It was discovered

that after PDA, there was ~1.7% nitrogen in the ZrO_xN_y and most of this was concentrated near the ZrO_xN_y/Si interface. Also, the ZrO_xN_y films yielded higher crystallization temperatures (~600-700ºC) than ZrO_2 (~400ºC). TaN-gated ZrO_2 and ZrO_xN_y NMOSCAPs were fabricated and characterized to compare the two dielectrics. Before post-TaN annealing, both ZrO_2 and ZrO_xN_y yielded similar EOT (10Å) and leakage current. After post-TaN annealing, the ZrO_xN_y demonstrated an improved thermal stability over ZrO_2. Hysteresis in the ZrO_xN_y (30mV) samples was slightly higher than the ZrO_2 (10mV), and increased with increasing nitrogen concentration.

Next, TaN-gated ZrO_2 and ZrO_xN_y NMOSFETs were fabricated and characterized. Prior to MOSFET fabrication, both dielectrics had an EOT of 9.5Å, but afterwards, the ZrO_xN_y had an EOT of 10.3Å and the ZrO_2 an EOT of 13.8Å – once again, the ZrO_xN_y demonstrated improved thermal stability over the ZrO_2. This thermal stability was attributed to a difference in IL composition and dielectric constant. For the ZrO_xN_y, the IL was composed of a nitrogen-doped Zr-silicate with a fairly high Zr concentration and k ~11.4. For the ZrO_2, the IL was composed of a Zr-silicate with a lower Zr concentration and lower k ~4.4. Thus, the nitrogen served not only to prevent further IL growth, but to prevent compositional changes to the IL during annealing. Reliability characterization such as time-zero breakdown (tzbd) and time dependent dielectric breakdown (tddb) were also investigated. ZrO_xN_y had higher effective breakdown field than ZrO_2 both before and after MOSFET

fabrication. As for tddb, ZrO_xN_y again showed higher breakdown field, but a lower 10-year lifetime operating voltage of -2.4V as compared to -2.7V for ZrO_2.

TaN-gated ZrO_2 and ZrO_xN_y NMOSFET C-V, I_d-V_g, and I_d-V_d characteristics were well behaved and revealed higher drive current, higher transconductance, and slightly lower swing for the ZrO_xN_y samples. Peak mobility for the ZrO_2 and ZrO_xN_y was comparable, but at high field the ZrO_xN_y mobility was degraded – likely due to surface roughness caused by nitrogen pile-up at the ZrO_xN_y/Si interface. Both ZrO_2 and ZrO_xN_y mobility were degraded compared to the universal curve for SiO_2.

In order to address the concern over mobility degradation, a high temperature (500-600ºC) forming gas (FG) anneal was introduced prior to the Al metallization step in TaN/ZrO_xN_y MOSFET fabrication. The high temperature FG anneal did not affect EOT (11.6Å), leakage, hysteresis, or tzbd. However, the high temperature FG anneal served to reduce D_{it} in the ZrO_xN_y and resulted in lower subthreshold swing (69 mV/decade), higher transconductance, lowered off-state leakage current, and most importantly, higher mobility. As these were just preliminary experiments, further optimization of the high temperature FG anneal and ZrO_xN_y process will likely lead to further improvements in mobility as well as other MOSFET characteristics.

In conclusion, ZrO_2 and ZrO_xN_y have demonstrated favorable electrical, material, and reliability characteristics and merit further study as potential high-k gate dielectric materials for future MOS technology.

6.2 Future work

Although both ZrO_2 and ZrO_xN_y have exhibited promising high-k gate dielectric characteristics, much work remains to be done before these materials can be adopted into MOS technology. The list below presents possible future work on ZrO_2 and ZrO_xN_y gate dielectrics.

- MOSFET reliability (e.g. negative/positive bias temperature instability)
- High temperature ($\geq$ 100ºC) measurement
- PMOS metal gate (e.g. RuO_2, Mo, Ru-Ta alloy) compatibility
- PMOS metal gate MOSCAP/MOSFET characterization
- Boron/impurity diffusion in ZrO_xN_y and SN samples
- Characterization of MOSFETs with SN
- Other forms of nitrogen incorporation into the ZrO_2 stack (e.g. NO or N_2O)
- Further optimization of high temperature FG anneal to improve mobility

Bibliography

[1] S. Borkar, "Obeying Moore's Law beyond 0.18 micron," Proceedings of the 13th Annual IEEE International ASIC/SOC Conference, p. 26, 2000.

[2] International Technology Roadmap for Semiconductors, 2001 edition. Semiconductor Industry Association, 2001.

[3] C.-H. Choi, P.R. Chidambaram, R. Khamankar, C.F. Machala, Z. Yu, and R.W. Dutton, "Gate Length Dependent Polysilicon Depletion Effects," IEEE Electron Device Letters, vol. 23, no. 4, p. 224, 2002.

[4] R. Rios, N.D. Arora, and C.-L. Huang, "An Analytic Polysilicon Depletion Effect Model for MOSFET's," IEEE Electron Device Letters, vol. 15, no. 4, p. 129, 1994.

[5] R. Rios, N.D. Arora, C.-L. Huang, N. Khalil, J. Faricelli, and L. Gruber, "A Physical Compact MOSFET Model, Including Quantum Mechanical Effects, for Statistical Circuit Design Applications," International Electron Devices Meeting, IEDM Technical Digest, p. 937, 1995.

[6] R. Rios and N.D. Arora, "Determination of Ultra-thin Gate Oxide Thicknesses for CMOS Structures using Quantum Effects," International Electron Devices Meeting, IEDM Technical Digest, p. 613, 1994.

[7] K. Yang, Y.C. King, and C. Hu, "Quantum Effect in Oxide Thickness Determination from Capacitance Measurement," Technical Digest of Symposium on VLSI Technology, p. 77, 1999.

[8] R.D. Shannon, "Dielectric polarizabilities of ions in oxides and fluorides," Journal of Applied Physics, vol. 73, no. 1, p. 348, 1993.

[9] G.D. Wilk, R.M. Wallace, and J.M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics," Journal of Applied Physics, vol. 15, no. 1, p. 484, 2000.

[10] S. Ezhilvalavan and T. Tseng, "Conduction mechanisms in amorphous and crystalline Ta_2O_5 thin films," Journal of Applied Physics, vol. 83, no. 9, p. 4797, 1998.

[11] J. Vuillod, "Preparation and characterization of plasma enhanced chemical vapor deposited silicon nitride and oxynitride films," Journal of Vacuum Science & Technology A, vol. 5, no. 4, p. 1675, 1987.

[12] J.A. Diniz, P.J. Tatsch, and M.A.A. Pudenzi, "Oxynitride films formed by low energy NO^+ implantation into silicon," Applied Physics Letters, vol. 69, no. 15, p. 2214, 1996.

[13] H. Hwang, W. Ting, D.-L. Kwong, and J.C. Lee, "Electrical and reliability characteristics of ultrathin oxynitride gate dielectric prepared by rapid thermal processing in N_2O," International Electron Devices Meeting, IEDM Technical Digest, p. 421, 1990.

[14] A. Ono, K. Fukasaku, T. Fukuda, N. Ilezawa, K. Imai, and T. Horiuchu, "A 70?m Gate Length CMOS technology with 1.0V Operation," Technical Digest of Symposium on VLSI Technology, p. 14, 2000.

[15] N. Fukushima, K. Abe, M. Izuha, T. Schimizu, and T. Kawakubo, "Epitaxial (Ba,Sr)TiO_3 Capacitors with Extremely High Dielectric Constant for DRAM Applications," International Electron Devices Meeting, IEDM Technical Digest, p. 257, 1997.

[16] R.B. Khamankar, M.A. Kressley, M.R. Visokay, T. Moise, G. Xing, S. Nemoto, Y. Okuno, S.J. Fang, A.M. Wilson, J.F. Gaynor, T.Q. Hurd, D.L. Crenshaw, S. Summerfelt, and L. Colombo, "A Novel BST Storage Capacitor Node Technology Using Platinum Electrodes for Gbit DRAMs," International Electron Devices Meeting, IEDM Technical Digest, p. 245, 1997.

[17] T. Chen, D. Hadad, V. Balu, B. Jiang, S. Kuah, P.C. McIntyre, S.R. Summerfelt, J.M. Anthony, and J.C. Lee, "Ir-Electroded BST Thin Film Capacitors for 1 Giga-bit DRAM Application," International Electron Devices Meeting, IEDM Technical Digest, p. 679, 1996.

[18] Y. Jeon, B.H. Lee, K. Zawadski, W. Qi, A. Lucas, R. Nieh, and J.C. Lee, "Effect of Barrier Layer on the Electrical and Reliability Characteristics of High-k Gate Dielectric films," International Electron Devices Meeting, IEDM Technical Digest, p. 797, 1998.

[19] R. Nieh, "High-k Gate Dielectrics for Future MOS Technology," Master's Thesis. The University of Texas at Austin, 1999.

[20] R. Nieh, W.J. Qi, Y. Jeon, B.H. Lee, A. Lucas, L. Kang, J.C. Lee, M. Gardner, and M. Gilmer, "Nitrogen (N_2) implantation to suppress growth of interfacial oxide in MOCVD BST and sputtered BST films," Materials Research Society Symposium Proceedings Series, vol. 567, p. 521, 1999.

[21] K.J. Hubbard and D.G Schlom, "Thermodynamic stability of binary oxides in contact with silicon," Journal of Materials Research, vol. 11, no. 11, p. 2757, 1996.

[22] B.H. Lee, "Technology Development and Process Integration of Alternative Gate Dielectric Material; Hafnium Oxide," Ph.D. dissertation, The University of Texas at Austin, 2000.

[23] L. Kang, "Study of HfO_2 as a Future Gate Dielectric and Implementation of Polysilicon Electrodes for HfO_2 films," Ph.D. dissertation, The University of Texas at Austin, 2000.

[24] M. Balog, M. Schieber, M. Michman, and S. Patai, "The chemical vapour deposition and characterization of ZrO_2 films from organometallic compounds," Thin Solid Films, vol. 47, p. 109, 1977.

[25] C.S. Hwang and H.J. Kim, "Deposition and characterization of ZrO_2 thin films on silicon substrate by MOCVD," Journal of Materials Research, vol. 8, no. 6, p. 1361, 1993.

[26] G.D. Wilk, R.M. Wallace, and J.M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, vol. 89, no. 10, p. 5243, 2001.

[27] J.S. Suehle, E.M. Vogel, M.D. Edelstein, C.A. Richter, N.V. Nguyen, I. Levin, D.L. Kaiser, H. Wu, and J.B. Bernstein, "Challenges of High-k Gate Dielectrics for Future MOS Devices," 6^{th} International Symposium on Plasma-Induced Damage, p. 90, 2001.

[28] M.A. Cameron and S.M. George, "ZrO_2 film growth by chemical vapor deposition using zirconium tetra-*tert*-butoxide," Thin Solid Films, vol. 348, p. 90, 1999.

[29] W.W. Davison and R.C. Buchanan, "ZrO_2 Thin Films for Packaging and Microelectronics Applications," Advances in Ceramics: Ceramic Substrates and Packages for Electronic Application, vol. 26, p. 513, 1989.

[30] M. Balog, M. Schieber, M. Michman, and S. Patai, "The Characteristics of Growth of Films of Zirconium and Hafnium Oxides (ZrO_2, HfO_2) by Thermal Decomposition of Zirconium and Hafnium ?-Diketonate Complexes in the Presence and Absence of Oxygen," Journal of the Electrochemical Society: Solid-state Science and Technology, vol. 126, no. 7, p. 1203, 1979.

[31] M. Balog, M. Schieber, S. Patai, and M. Michman, "Thin Films of Metal oxides on Silicon by Chemical Vapor Deposition with Organometallic Compounds," Journal of Crystal Growth, vol. 17, p. 298, 1972.

[32] A.C. Greenwald, N.M. Kalkhoran, F. Namavar, A.E. Kaloyeros, and I. Stathakos, "Heteroepitaxial Si-ZrO_2-Si by MOCVD," Materials Research Society Symposium Proceedings, vol. 335, p. 123, 1993.

[33] K. Kukli, K. Forsgren, M. Ritala, M. Leskelä, J. Aarik, and A. Hårsta, "Dielectric Properties of Zirconium Oxide Grown by Atomic Layer Deposition from Iodide Precursor," Journal of the Electrochemical Society, vol. 148, p. F227, 2001.

[34] P.J. Martin, R.P. Netterfield, and W.G. Sainty, "Modification of the optical and structural properties of dielectric ZrO_2 films by ion-assisted deposition," Journal of Applied Physics, vol. 55, no. 1, p. 235, 1984.

[35] J. Robertson, E. Riassi, J.-P. Maria, and A.I. Kingon, "Band alignments of high-k dielectrics on Si and Pt," Materials Research Society Symposium Proceedings Series, vol. 592, 1999.

[36] J.H. Kim, S.I. Woo, B.Y. Nam, and W.J. Yoo, "Anisotropic Etching Characteristics of Platinum Electrode for Ferroelectric Capacitor," IEEE Transactions on Electron Devices, vol. 46, no. 5, p. 984, 1999.

[37] C.M. Soriano, "Platinum," IEEE Potentials, vol. 16, no. 5, p. 29, 1998.

[38] S.P. Murarka, "Rapid thermal processing for reproducible formation of the self-aligned silicides of cobalt and platinum," Proceedings of the IEEE/SEMI Advanced Semiconductor Manufacturing Conference, p. 211, 1992.

[39] M.A. Russak, C.V. Jahnes, and E.P. Katz, "Reactive magnetron sputtered zirconium oxide and zirconium silicon oxide," Journal of Vacuum Science & Technology A, vol. 7, no. 3, p. 1248, 1989.

[40] J.R. Hauser and K. Ahmed, *Characterization and Metrology for ULSI Technology*, (AIP, New York, 1998), p. 235.

[41] R. Nieh, W.J. Qi, B.H. Lee, L. Kang, Y. Jeon, K. Onishi, S. Gopalan, C.S. Kang, E. Dharmarajan, R. Choi, and J.C. Lee, "Processing effects and electrical characterization of ZrO_2 formed by the RTP oxidation of Zr," Proceedings of the 5th International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues Session of the 197th Electrochemical Society Meeting, p. 214, 2000.

[42] E.E. Khawaja, F. Bouamrane, A.B. Hallak, M.A. Daous, and M.A. Salim, "Observation of oxygen enrichment in zirconium oxide films," Journal of Vacuum Science & Technology A, vol. 11, no. 3, p. 580, 1993.

[43] B.W. Busch, W.H. Schulte, E. Garfunkel, T. Gustafsson, W.-J. Qi, R. Nieh, and J.C. Lee, "Oxygen exchange and transport in thin zirconia films on Si(100)," Physical Review B, vol. 62, no. 20, p. R13290, 2000.

[44] W.J. Qi, "Study on High-k Dielectrics as Alternative Gate Insulators for 0.1?m and Beyond ULSI Applications," Ph.D. dissertation, The University of Texas at Austin, 2000.

[45] B. Pelloie, J. Perriere, J. Siejka, P. Debenest, A. Straboni, and B. Vuillermoz, "Investigation of ionic transport mechanisms during plasma anodization of Si and Si through ZrO_2," Journal of Applied Physics, vol. 63, no. 8, p. 2620, 1988.

[46] J.-P. Maria, D. Wicaksana, A.I. Kingon, B. Busch, H. Schulte, E. Garfunkel, and T. Gustafsson, "High temperature stability in lanthanum and zirconia-based gate dielectrics," Journal of Applied Physics, vol. 90, no. 7, p. 3476, 2001.

[47] H. Watanabe, "Interface engineering of a $ZrO_2/SiO_2/Si$ layered structure by *in situ* reoxidation and its oxygen-pressure-dependent thermal stability," Applied Physics Letters, vol. 78, no. 24, p. 3803, 2001.

[48] J.P. Chang and Y.-S. Lin, "Dielectric properties and conduction mechanism of ultrathin zirconium oxide films," Applied Physics Letters, vol. 79, no. 22, p. 3666, 2001.

[49] B.-O. Cho, J. Wang, L. Sha, and J.P. Chang, "Tuning the electrical properties of zirconium oxide thin films," Applied Physics Letters, vol. 80, no. 6, p. 1052, 2002.

[50] T.P. Ma, "High-k Gate Dielectrics for Scaled CMOS Technology," Proceedings of the 6th International Conference on Solid-State and Integrated Circuit Technology, p. 297, 2001.

[51] J.P. Chang, Y.-S. Lin, and K. Chu, "Rapid thermal chemical vapor deposition of zirconium oxide for metal-oxide-semiconductor field effect transistor application," Journal of Vacuum Science & Technology B, vol. 19, no. 5, p. 1782, 2001.

[52] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo, and A. Nishiyama, "Thermally Stable Ultra-Thin Nitrogen Incorporated ZrO_2 Gate Dielectric Prepared by Low Temperature Oxidation of ZrN," International Electron Devices Meeting, IEDM Technical Digest, p. 459, 2001.

[53] S. Ramanathan, D.A. Muller, G.D. Wilk, C.M. Park, and P.C. McIntyre, "Effect of oxygen stoichiometry on the electrical properties of zirconia gate dielectrics," Applied Physics Letters, vol. 79, no. 20, p. 3311, 2001.

[54] D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, A. Murthy, B. Roberds, P. Stokley, and R. Chau, "High-Frequency response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 231, 2001.

[55] E.P. Gusev, D.A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P.C. Jamison, D.A. Neumayer, M. Copel, M.A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L-A. Ragnarsson, P. Ronsheim, K. Rim, R.J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin high-K gate stacks for advanced CMOS devices," International Electron Devices Meeting, IEDM Technical Digest, p. 451, 2001.

[56] Y.K. Kim, S.M. Lee, I.S. Park, C.S. Park, S.I. Lee, and M.Y. Lee, "Novel poly-Si/Al_2O_3/poly-Si Capacitor for High Density DRAMs," Technical Digest of Symposium on VLSI Technology, p. 52, 1998.

[57] D.A. Buchanan, E.P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M.A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R.J. Fleming, P.C. Jamison, J.

Brown, and R. Arndt, "80 nm poly-silicon gated N-FETs with ultra-thin Al_2O_3 gate dielectric for ULSI application," International Electron Devices Meeting, IEDM Technical Digest, p. 223, 2000.

[58] J.M. Hergenrother, G.D. Wilk, T. Nigam, F.P. Klemens, D. Monroe, P.J. Silverman, T.W. Sorsch, B. Busch, M.L. Green, M.R. Baker, T. Boone, M.K. Bude, N.A. Ciampa, E.J. Ferry A.T. Fiory, S.J. Hillenius, D.C. Jacobson, R.W. Johnson, P. Kalavade, R.C. Keller, C.A. King, A. Kornblit, H.W. Krautter, J.T-C Lee, W.M. Mansfield, J.F. Miner, M.D. Morris, S.-H. Oh, J.M. Rosamilia, B.J. Sapjeta, K. Short, K. Steiner, D.A. Muller, P.M. Voyles, J.L. Grazul, E.J. Shero, M.E. Givens, C. Pomarede, M. Mazanec, and C. Werkhoven, "50 nm Vertical Replacement-Gate (VRG) nMOSFETs with ALD HfO_2 and Al_2O_3 Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 51, 2001.

[59] S. Gopalan, K. Onishi, R. Nieh, C.S. Kang, R. Choi, H.-J. Cho, S. Krishnan, and J.C. Lee, "Electrical and physical characteristics of ultrathin hafnium silicate films with polycrystalline silicon and TaN gates," Applied Physics Letters, vol. 80, no. 23, p. 4416, 2002.

[60] L. Kang, K. Onishi, Y. Jeon, B.H. Lee, C.S. Kang, W.-J. Qi, R. Nieh, S. Gopalan, R. Choi, and J.C. Lee, "MOSFET Devices with Polysilicon on Single-Layer HfO_2 High-K Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 35, 2000.

[61] S.J. Lee, H.F. Luan, C.H. Lee, T.S. Jeon, W.P. Bai, Y. Senzaki, D. Roberts, and D.L. Kwong, "Performance and reliability of ultra thin CVD HfO_2 gate dielectrics with dual poly-Si gate electrodes," Technical Digest of Symposium on VLSI Technology, p. 133, 2001.

[62] S.J. Lee, H.F. Luan, W.P. Bai, C.H. Lee, T.S. Jeon, Y. Senzaki, D. Roberts, and D.L. Kwong, "High quality ultra thin CVD HfO_2 gate stack with poly-Si gate electrode," International Electron Devices Meeting, IEDM Technical Digest, p. 31, 2000.

[63] S.J. Lee, C.H. Lee, C.H. Choi, and D.L. Kwong, "Time-dependent dielectric breakdown in poly-Si CVD HfO_2 gate stack," International Reliability Physics Symposium (IRPS) Proceedings, p. 409, 2002.

[64] Q. Lu, H. Takeuchi, R. Lin, T.-J. King, C. Hu, K. Onishi, R. Choi, C.S. Kang, and J.C. Lee, "Hot carrier reliability of n-MOSFET with ultra-thin HfO_2 gate dielectric and poly-Si gate," International Reliability Physics Symposium (IRPS) Proceedings, p. 429, 2002.

[65] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J.C. Lee, "Charging Effects on Reliability of HfO_2 Devices with Polysilicon Gate Electrode," International Reliability Physics Symposium (IRPS) Proceedings, p. 419, 2002.

[66] J. Shappir, A. Anis, and I. Pinsky, "Investigation of MOS Capacitors with Thin ZrO_2 Layers and Various Gate Materials for Advanced DRAM Applications," IEEE Transactions on Electron Devices, vol. ED-33, no. 4, p. 442, 1986.

[67] C. Hobbs, L. Dip, K. Reid, D. Gilmer, R. Hegde, T. Ma, B. Taylor, B. Cheng, S. Samavedam, H. Tseng, D. Weddington, F. Huang, D. Farber, M. Schippers, M. Rendon, L. Prabhu, R. Rai, S. Badchi, J. Conner, S. Backer, F. Dumbuya, J. Locke, D. Workman, and P. Tobin, "Sub-Quarter Micron Si-Gate CMOS with ZrO_2 gate dielectric," Proceedings of International Symposium on VLSI Technology, Systems, and Applications, p. 204, 2001.

[68] Y. Kim, G. Gebara, M. Freiler, J. Barnett, D. Riley, J. Chen, K. Torres, J. Lim, B. Foran, F. Shaapur, A. Agarwal, P. Lysaght, G.A. Brown, C. Young, S. Borthakur, H.-J. Li, B. Nguyen, P. Zeitzoff, G. Bersuker, D. Derro, R. Bergmann, R.W. Murto, A. Hou, H.R. Huff, E. Shero, C. Pomarede, M. Givens, M. Mazanec, and C. Werkhoven, "Conventional n-channel MOSFET devices using single layer HfO_2 and ZrO_2 as high-k gate dielectrics with polysilicon gate electrode," International Electron Devices Meeting, IEDM Technical Digest, p. 455, 2001.

[69] T. Ma, S.A. Campbell, R. Smith, N. Hoilien, B. He, W.L. Gladfelter, C. Hobbs, D. Buchanan, C. Taylor, M. Gribelyuk, M. Tiner, M. Coppel, and J.J. Lee, "Group IVB Metal Oxides High Permittivity Gate Insulators Deposited From Anhydrous Metal Nitrates," IEEE Transactions on Electron Devices, vol. 48, no. 10, p. 2348, 2001.

[70] C.H. Lee, H.F. Luan, W.P Bai, S.J. Lee, T.S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS Characteristics of Ultra Thin Rapid Thermal CVD ZrO_2 and Zr Silicate Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 27, 2000.

[71] R. Nieh, S. Krishnan, H.-J. Cho, C.S. Kang, S. Gopalan, K. Onishi, R. Choi, and J.C. Lee, "Comparison between ultra-thin ZrO_2 and ZrO_xN_y gate dielectrics in TaN or poly-gated NMOSCAP and NMOSFET devices," Technical Digest of Symposium on VLSI Technology, p. 186, 2002.

[72] K.-Y. Lim, D.-G. Park, H.-J. Cho, J.-J. Kim, J.-M. Yang, I.-S. Choi, I.-S. Yeo, and J.W. Park, "Electrical characteristics and thermal stability of n^+ polycrystalline-Si/ZrO_2/SiO_2/Si metal-oxide-semiconductor capacitors," Journal of Applied Physics, vol. 91, no. 1, p. 414, 2002.

[73] C.H. Lee, Y.H. Kim, H.F. Luan, S.J. Lee, T.S. Jeon, W.P. Bai, and D.L. Kwong, "MOS Devices with High Quality Ultra Thin CVD ZrO_2 Gate Dielectrics and Self-Aligned TaN and TaN/Poly-Si Gate Electrodes," Technical Digest of Symposium on VLSI Technology, p. 137, 2001.

[74] C. Hu, "Gate oxide scaling limits and projection," International Electron Devices Meeting, IEDM Technical Digest, p. 319, 1996.

[75] B. Cheng, M. Cao, R. Rao, A. Inani, P.V. Voorde, W.M. Greene, J.M.C. Stork, Z. Yu, P.M. Zeitzoff, and J.C.S. Woo, "The Impact of High-k Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFETs," IEEE Transactions on Electron Devices, vol. 46, no. 7, p. 1537, 1999.

[76] Y.-C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of High-k Gate Dielectric Materials on Metal and Silicon Gate Workfunctions," IEEE Electron Device Letters, vol. 23, no. 6, p. 342, 2002.

[77] H. Zhong, G. Heuss, and V. Misra, "Electrical Properties of RuO_2 Gate Electrodes for Dual Metal Gate Si-CMOS," IEEE Electron Device Letters, vol. 21, no. 12, p. 593, 2000.

[78] H. Zhong, G. Heuss, V. Misra, H. Luan, C.-H. Lee, and D.L. Kwong, "Characterization of RuO_2 electrodes on Zr silicate and ZrO_2 dielectrics," Applied Physics Letters, vol. 78, no. 8, p. 1134, 2001.

[79] Q. Lu, R. Lin, P. Ranade, T.-J. King, and C. Hu, "Metal Gate Work Function Adjustment for Future CMOS Technology," Technical Digest of Symposium on VLSI Technology, p. 45, 2001.

[80] Q. Lu, R. Lin, P. Ranade, Y.C. Yeo, X. Meng, H. Takeuchi, T.J. King, C. Hu, H. Luan, S. Lee, W. Bai, C.-H. Lee, D.L. Kwong, X. Guo, X. Wang, and T.P. Ma, "Molybdenum metal gate MOS technology for post-SiO_2 gate dielectrics," International Electron Devices Meeting, IEDM Technical Digest, p. 641, 2000.

[81] D.-G. Park, T.-H. Cha, K.-Y. Lim, H.-J. Cho, T.-K. Kim, S.-A. Jang, Y.-S. Suh, V. Misra, I.-S. Yeo, J.-S. Roh, J. W. Park, and H.-K. Yoon, "Robust

ternary metal gate electrodes for dual gate CMOS devices," International Electron Devices Meeting, 2001. IEDM Technical Digest, p. 671, 2001.

[82] K. Nakajima, Y. Akasaka, M. Kaneko, M. Tamaoki, Y. Yamada, T. Shimizu, Y. Ozawa, and K. Suguro, "Work Function Controlled Metal Gate Electrode on Ultrathin Gate Insulators," Technical Digest of Symposium on VLSI Technology, p. 95, 1999.

[83] B. Claflin, M. Binger, and G. Lucovsky, "Interface studies of tungsten nitride and titanium nitride composite metal gate electrodes with thin dielectric layers," Journal of Vacuum Science & Technology A, vol. 16, no. 3, p. 1757, 1998.

[84] H. Zhong, S.-N. Hong, Y.-S. Suh, H. Lazar, G. Heuss, and V. Misra, "Properties of Ru-Ta Alloys as Gate Electrodes for NMOS and PMOS Silicon Devices," International Electron Devices Meeting, IEDM Technical Digest, p. 467, 2001.

[85] Y.-S. Suh, G. Heuss, H. Zhong, S.-N. Hong, and V. Misra, "Electrical Characteristics of $TaSi_xN_y$ Gate Electrodes for Dual Gate S-CMOS Devices," Technical Digest of Symposium on VLSI Technology, p. 47, 2001.

[86] S.B. Samavedam, H.H. Tseng, P.J. Tobin, J. Mogab, S. Dakshina-Murthy, L.B. La, J. Smith, J. Schaeffer, M. Zavala, R. Martin, B.-Y. Nguyen, L. Herbert, O. Adetutu, V. Dhandapani, T.-Y. Luo, R. Garcia, P. Abramowitz, M. Moosa, D.C. Gilmer, C. Hobbs, W.J. Taylor, J.M. Grant, R. Hedge, S. Bagchi, E. Lucowski, V. Arunachalam, and M. Azrak, "Metal Gate MOSFETs with HfO_2 Gate Dielectric," Technical Digest of Symposium on VLSI Technology, p. 24, 2002.

[87] Y.H. Kim, C.H. Lee, T.S. Jeon, W.P. Bai, C.H. Choi, S.J. Lee, L. Xinjian, R. Clarks, D. Roberts, and D.L. Kwong, "High Quality CVD TaN Gate Electrode for Sub-100nm MOS Devices," International Electron Devices Meeting, IEDM Technical Digest, p. 667, 2001.

[88] H. Shimada, I. Ohshima, S.-I. Nakao, M. Nakagawa, K. Kanemoto, M. Hirayama, S. Sugawa, and T. Ohmi, "Low Resistivity bcc-Ta/TaN_x Metal Gate MNSFETs Having Plane Gate Structure Featuring Fully Low-Temperature Processing below 450ºC," Technical Digest of Symposium on VLSI Technology, p. 67, 2001.

[89] Y. Nakamura, I. Asano, M. Hiratani, T. Saito, and H. Goto, "Oxidation-Resistant Amorphous TaN Barrier for MIM Ta_2O_5 Capacitors in Giga-Bit DRAMs," Technical Digest of Symposium on VLSI Technology, p. 39, 2001.

[90] R. Choi, C. S. Kang, B.H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J.C. Lee, "High-Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation," Technical Digest of Symposium on VLSI Technology, p. 15, 2001.

[91] B.H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W.-J. Qi, C.S. Kang, and J.C. Lee, "Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8-12Å)," International Electron Devices Meeting, IEDM Technical Digest, p. 39, 2000.

[92] E. Dharmarajan, W.-J. Qi, R. Nieh, L. Kang, K. Onishi, and J.C. Lee, "Ultra-Thin Zirconium Silicate Films With Good Physical and Electrical Properties for Gate Dielectric Applications," Material Research Society (MRS) Symposium Proceedings, vol. 648, 2000.

[93] K. Chen, H.C. Waan, J. Dunster, P.K. Ko, C. Hu, and M. Yoshida, "MOSFET Carrier Mobility Model Based on Gate Oxide Thickness, Threshold and Gate Voltages," Solid-State Electronics, vol. 39, no. 10, p. 1515, 1996.

[94] M. Houssa, V.V. Afanas'ev, A. Stesmans, and M.M. Heyns, "Variation in the fixed charge density of SiO_x/ZrO_2 gate dielectric stacks during postdeposition oxidation," Applied Physics Letters, vol. 77, no. 12, p. 1885, 2000.

[95] D.M. Fleetwood, "Fast and Slow Border Traps in MOS Devices," IEEE Transactions on Nuclear Science, vol. 43, no. 2, p. 779, 1996.

[96] J.H. Han, R. Nieh, C.S. Kang, H.-J. Cho, K. Onishi, S. Gopalan, R. Choi, S. Krishnan, Y.H. Kim, A. Shahriar, and J.C. Lee, "Hysteresis Dependence on Interface Trapping Charge for $TaN/HfO_2/Si$ and $TaN/ZrO_2/Si$ Capacitors," submitted to Applied Physics Letters, 2002.

[97] S. Ramanathan, C.-M. Park, and P.C. McIntyre, "Electrical properties of thin film zirconia grown by ultraviolet ozone oxidation," Journal of Applied Physics, vol. 91, no. 7, p. 4521, 2002.

[98] W.-J. Qi, R. Nieh, B.H. Lee, K. Onishi, L. Kang, Y. Jeon, J.C. Lee, V. Kaushik, B.-Y. Nguyen, L. Prabhu, K. Eigenbeiser, and J. Finder, "Performance of MOSFETs with ultra thin ZrO_2 and Zr silicate gate

dielectrics," Technical Digest of Symposium on VLSI Technology, p. 40, 2000.

[99] T. Hori, *Gate Dielectrics and MOS ULSIs: Principles, Technologies, and Applications*, (Springer, Berlin, 1997).

[100] M. Fujiwara, M. Takayanagi, T. Shimizu, and Y. Toyoshima, "Extending Gate Dielectric Scaling Limit by NO Oxynitride: Design and Process Issues for Sub-100nm Technology," International Electron Devices Meeting, IEDM Technical Digest, p. 227, 2000.

[101] A. Chou, "Development of thin gate and tunnel dielectrics for MOS applications," Ph.D. dissertation, The University of Texas at Austin, 1997.

[102] A.G. Lucas, "The growth of oxynitrides and their use as gate dielectrics," Master's Thesis. The University of Texas at Austin, 1999.

[103] S. Gopalan, R. Choi, K. Onishi, R. Nieh, C.S. Kang, H.-J. Cho, S. Krishnan, and J.C. Lee, "Impact of NH_3 pre-treatment on the electrical and reliability characteristics of ultra thin hafnium silicate films prepared by re-oxidation method," Device Research Conference (DRC) proceedings, p. 195, 2002.

[104] P.D. Kirsch, C.S. Kang, J. Lozano, L.C. Lee, and J.G. Ekerdt, "Electrical and spectroscopic comparison of HfO_2/Si interfaces on nitrided and un-nitrided Si(100)," Journal of Applied Physics, vol. 91, no. 7, p. 4354, 2002.

[105] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C.S. Kang, B.H. Lee, R. Nieh, and J.C. Lee, "Dopant Penetration Effects on Polysilicon Gate HfO_2 MOSFETs," Technical Digest of Symposium on VLSI Technology, p. 131, June 2001.

[106] R. Nieh, R. Choi, S. Gopalan, K. Onishi, C.S. Kang, H.-J. Cho, S. Krishnan, and J.C. Lee, "Evaluation of Silicon Surface Nitridation Effects on Ultra-thin ZrO_2 Gate Dielectrics," accepted to be published in Applied Physics Letters, 2002.

[107] S.M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1982).

[108] C.M. Perkins, B.B. Triplett, P.C. McIntyre, K.C. Saraswat, S. Haukka, and M. Tuominen, "Electrical and materials properties of ZrO_2 gate dielectrics grown by atomic layer chemical vapor deposition," Applied Physics Letters, vol. 78, no. 16, p. 2357, 2001.

[109] S. Ramanathan, G.D. Wilk, D.A. Muller, C.-M. Park, and P.C. McIntyre, "Growth and characterization of ultrathin zirconia dielectrics grown by ultraviolet ozone oxidation," Applied Physics Letters, vol. 79, no. 16, p. 2621, 2001.

[110] C.S. Kang, H.-J. Cho, K. Onishi, R. Choi, R. Nieh, S. Gopalan, S. Krishnan, and J.C. Lee, "Improved Thermal Stability and Device Performance of Ultra-thin (EOT less than 10Å) Gate Dielectric MOSFETs by using Hafnium Oxynitride (HfO_xN_y)," Technical Digest of Symposium on VLSI Technology, p. 146, 2002.

[111] H.-J. Cho, C.S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, S. Krishnan, and J.C. Lee, "Structural and Electrical Properties of HfO_2 with Top Nitrogen Incorporated Layer," IEEE Electron Device Letters, vol. 23, no. 5, p. 249, 2002.

[112] H.-J. Cho, C.S. Kang, K. Onishi, S. Gopalan, R. Nieh, E. Dharmarajan, and J.C. Lee, "Novel Nitrogen Profile Engineering for Improved TaN/HfO_2/Si MOSFET Performance," International Electron Devices Meeting, IEDM Technical Digest, p. 665, 2001.

[113] L. Manchanda, M.L. Green, R.B. van Dover, M.D. Morris, A. Kerber, Y. Hu, J.-P. Han, P.J. Silverman, T.W. Sorsch, G. Weber, V. Donnelly, K. Pelhos, F. Klemens, N.A. Ciampa, A. Kornblit, Y.O. Kim, J.E. Bower, D. Barr, E. Ferry, D. Jacobson, J. Eng, B. Busch, and H. Schulte, "Si-doped Aluminates for High Temperature Metal-Gate CMOS: Zr-Al-Si-O, A Novel Gate Dielectric for Low Power Applications," International Electron Devices Meeting, IEDM Technical Digest, p. 23, 2000.

[114] L. Manchanda, B. Busch, M.L. Green, M. Morris, R.B. van Dover, R. Kwo, and S. Aravamudhan, "High K Gate Dielectrics for the Silicon Industry," Extended Abstracts of International Workshop on Gate Insulator (IWGI), p. 56, 2001.

[115] W. Zhu, T.P. Ma, T. Tamagawa, Y. Di, J. Kim, R. Carruthers, M. Gibson, and T. Furukawa, "HfO_2 and HfAlO for CMOS: Thermal Stability and Current Transport," International Electron Devices Meeting, IEDM Technical Digest, p. 463, 2001.

[116] Y. Suizu, "Reexamination of the Role of Nitrogen in Oxynitrides – Fixed Charge Reduction in the p^+-Polysilicon Gate MOS," IEEE Transactions on Electron Devices, vol. 48, no. 12, p. 2777, 2001.

[117] W.-J. Qi, R. Nieh, B.H. Lee, L. Kang, Y. Jeon, K. Onishi, S. Gopalan, and J.C. Lee, "Temperature Effect on the Reliability of ZrO_2 Gate Dielectric Deposited Directly on Silicon," International Reliability Physics Symposium (IRPS) Proceedings, p. 72, 2000.

[118] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, E. Dharmarajan, and J.C. Lee, "Reliability Characteristics, including NBTI, of Polysilicon Gate MOSFETs," International Electron Devices Meeting, IEDM Technical Digest, p. 659, 2001.

[119] A. Chin, C.C. Liao, C.H. Lu, W.J. Chen, and C. Tsai, "Device and Reliability of High-k Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}," Technical Digest of Symposium on VLSI Technology, p. 135, 1999.

[120] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J.C. Lee, "Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," Technical Digest of Symposium on VLSI Technology, p. 22, 2002.

[121] R. Choi, K. Onishi, C. S. Kang, R. Nieh, S. Gopalan, H.-J. Cho, S. Krishnan, and J.C. Lee, "High Quality MOSFETs Fabrication with HfO_2 Gate Dielectric and TaN Gate Electrode," Device Research Conference (DRC) proceedings, p. 193, 2002.

Vita

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1. Renee Nieh, Chang Seok Kang, Hag-Ju Cho, Katsunori Onishi, Rino Choi, Siddarth Krishnan, Jeong Han, Young Hee Kim, Akbar Shahriar, and Jack C. Lee, "Electrical Characterization and Material Evaluation of Nitrogen Incorporated ZrO_2 (ZrO_xN_y) Gate Dielectric in TaN-gated NMOSFETs with High Temperature Forming Gas Annealing," submitted to IEEE Transactions on Electron Devices.

2. Renee Nieh, Rino Choi, Sundar Gopalan, Katsunori Onishi, Chang Seok Kang, Hag-Ju Cho, Siddarth Krishnan, and Jack C. Lee, "Evaluation of Silicon Surface Nitridation Effects on Ultra-thin ZrO_2 Gate Dielectrics," accepted to be published in Applied Physics Letters, 2002.

3. Renee Nieh, Siddarth Krishnan, Hag-Ju Cho, Chang Seok Kang, Sundar Gopalan, Katsunori Onishi, Rino Choi, and Jack C. Lee, "Comparison between ultra-thin ZrO_2 and ZrO_xN_y gate dielectrics in TaN or poly-gated NMOSCAP

and NMOSFET devices," Technical Digest of Symposium on VLSI Technology, pp. 186-187, 2002.

4. Renee Nieh, Katsunori Onishi, Rino Choi, Hag-Ju Cho, Chang Seok Kang, Sundar Gopalan, Siddarth Krishnan, and Jack C. Lee, "Performance Effects of Two Nitrogen Incorporation Techniques on TaN/HfO_2 and poly/HfO_2 MOSCAP and MOSFET devices," International Workshop on Gate Insulators (IWGI), Extended Abstracts, pp. 70-74, 2001.

5. Renee Nieh, Jack C. Lee, Byoung Hun Lee, Laegu Kang, Wen-Jie Qi, Katsunori Onishi, Sundar Gopalan, Chang Seok Kang, and Rino Choi, "Future Gate Dielectrics Materials," Rapid Thermal and Other Short-Time Processing Technologies Session at the 199th Electrochemical Society (ECS) Meeting, Washington D.C., 2001.

6. Renee Nieh, Wen-Jie Qi, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, Katsunori Onishi, and Jack C. Lee, "Processing effects and electrical evaluation of ZrO_2 formed by RTP oxidation of Zr," Proceedings of the 5th International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues Session of the 197th Electrochemical Society Meeting, Toronto, pp. 214-221, 2000.

7. Renee Nieh, Wen-Jie Qi, Yongjoo Jeon, Byoung Hun Lee, Aaron Lucas, Laegu Kang, Jack C. Lee, Mark Gardner, and Mark Gilmer, "Nitrogen (N_2) implantation to suppress growth of interfacial oxide in MOCVD BST and sputtered BST films," Ultrathin SiO_2 and High-k Materials for ULSI Gate Dielectrics Symposium Proceedings Volume 567, Spring MRS Meeting, pp. 521-526, 1999.

8. Yang-Yu Fan, Renee E. Nieh, Jack C. Lee, Gerry Lucovsky, George A. Brown, L. Frank Register, and Sanjay K. Banerjee, "Voltage and Temperature Dependent Gate Capacitance and Current Model: Application to ZrO2 n-channel MOS Capacitor," Transactions on Electron Devices, accepted to be published, 2002.

9. Rino Choi, Katsunori Onishi, Chang Seok Kang, Sundar Gopalan, Renee Nieh, Young Hee Kim, Jeong H. Han, Siddarth Krishnan, Hag-Ju Cho, Akbar Shahriar, and Jack C. Lee, "Fabrication of High Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs Using Deuterium Anneal," International Electron Devices Meeting, IEDM Technical Digest, accepted to be published, 2002.

10. Young Hee Kim, Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Renee Nieh, Jeong H. Han, Siddarth Krishnan, and Jack C. Lee, "Hard and Soft-

Breakdown Characteristics of Ultra-Thin HfO_2 Under Dynamic and Constant Voltage Stress," International Electron Devices Meeting, IEDM Technical Digest, accepted to be published, 2002.

11. Chang Seok Kang, Hag-Ju Cho, Katsunori Onishi, Rino Choi, Young Hee Kim, Renee Nieh, Jeong Han, Siddarth Krishnan, and Jack C. Lee, "Nitrogen Concentration Effects and Performance Improvement of MOSFETs Using Thermally Stable HfO_xN_y Gate Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, accepted to be published, 2002.

12. Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Sundar Gopalan, Renee Nieh, Siddarth Krishnan, and Jack C. Lee, "Improvement of surface carrier mobility of HfO_2 MOSFET's by high-temperature forming gas annealing," submitted to IEEE Transactions on Electron Devices.

13. Jeong H. Han, Renee Nieh, Chang Seok Kang, Hag-Ju Cho, Katsunori Onishi, Sundar Gopalan, Rino Choi, Siddarth Krishnan, Young Hee Kim, Akbar Shahriar, and Jack C. Lee, "Hysteresis Dependence on Interface Trapping Charge for TaN/HfO_2/Si and TaN/ZrO_2/Si Capacitors," submitted to Applied Physics Letters, 2002.

14. Young Hee Kim, Katsunori Onishi, Chang Seok Kang, Hag-Ju Cho, Renee Nieh, Sundar Gopalan, Rino Choi, Jeong Han, Siddarth Krishnan, and Jack C. Lee, "Area Dependence of TDDB Characteristics for HfO_2 Gate Dielectrics and Its Implication," accepted to be published in Electron Device Letters, 2002.

15. Rino Choi, Katsunori Onishi, Chang Seok Kang, Renee Nieh, Sundar Gopalan, Hag-Ju Cho, Siddarth Krishnan, and Jack C. Lee, "High Quality MOSFETs Fabrication with HfO_2 Gate Dielectric and TaN Gate Electrode," Device Research Conference (DRC) proceedings, pp. 193-194, 2002.

16. Sundar Gopalan, Rino Choi, Katsunori Onishi, Renee Nieh, Chang Seok Kang, Hag-Ju Cho, Siddarth Krishnan, and Jack C. Lee, "Impact of NH_3 pre-treatment on the electrical and reliability characteristics of ultra thin hafnium silicate films prepared by re-oxidation method," Device Research Conference (DRC) proceedings, pp. 195-196, 2002.

17. Sundar Gopalan, Katsunori Onishi, Renee Nieh, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Siddarth Krishnan, and Jack C. Lee "Electrical and physical characteristics of ultrathin hafnium silicate films with polycrystalline silicon and TaN gates," Applied Physics Letters, vol. 80, no. 23, pp. 4416-4418, 2002.

18. Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Sundar Gopalan, Renee Nieh, Siddarth Krishnan, and Jack C. Lee, "Charging Effects on Reliability of HfO_2 Devices with Polysilicon Gate Electrode," International Reliability Physics Symposium (IRPS) Proceedings, pp. 419-420, 2002.

19. Hag-Ju Cho, Chang Seok Kang, Katsunori Onishi, Sundar Gopalan, Renee Nieh, Rino Choi, Siddarth Krishnan, and Jack C. Lee, "Structural and Electrical Properties of HfO_2 with Top Nitrogen Incorporated Layer," IEEE Electron Device Letters, vol. 23, no. 5, pp. 249-251, 2002.

20. Chang Seok Kang, Hag-Ju Cho, Katsunori Onishi, Rino Choi, Renee Nieh, Sundar Gopalan, Siddarth Krishnan, and Jack C. Lee, "Improved Thermal Stability and Device Performance of Ultra-thin (EOT less than 10Å) Gate Dielectric MOSFETs by using Hafnium Oxynitride (HfO_xN_y)," Technical Digest of Symposium on VLSI Technology, pp. 146-147, 2002.

21. Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Sundar Gopalan, Renee Nieh, Siddarth Krishnan, and Jack C. Lee, "Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," Technical Digest of Symposium on VLSI Technology, pp. 22-23, 2002.

22. Hag-Ju Cho, Chang Seok Kang, Katsunori Onishi, Sundar Gopalan, Renee Nieh, Easwar Dharmarajan, and Jack C. Lee, "Novel Nitrogen Profile Engineering for Improved TaN/HfO_2/Si MOSFET Performance," International Electron Devices Meeting, IEDM Technical Digest, pp. 665-668, 2001.

23. Katsunori Onishi, Chang Seok Kang, Rino Choi, Hag-Ju Cho, Sundar Gopalan, Renee Nieh, Easwar Dharmarajan, and Jack C. Lee, "Reliability Characteristics, including NBTI, of Polysilicon Gate MOSFETs," International Electron Devices Meeting, IEDM Technical Digest, pp. 659-662, 2001.

24. Sundar Gopalan, Easwar Dharmarajan, Katsunori Onishi, Renee Nieh, Chang Seok Kang, Rino Choi, Hag-Ju Cho, and Jack C. Lee, "Ultra-thin Hafnium Silicate films with TaN and Polysilicon gates for gate dielectric application," IEEE Semiconductor Interface Specialist Conference (SISC) Proceedings, 2001.

25. Katsunori Onishi, Laegu Kang, Rino Choi, Easwar Dharmarajan, Sundar Gopalan, Yongjoo Jeon, Chang Seok Kang, Byoung Hun Lee, Renee Nieh, and Jack C. Lee, "Dopant Penetration Effects on Polysilicon Gate HfO_2 MOSFETs," Technical Digest of Symposium on VLSI Technology, pp. 131-132, 2001.

26. Rino Choi, Chang Seok Kang, Byoung Hun Lee, Katsunori Onishi, Renee Nieh, Sundar Gopalan, Easwar Dharmarajan, and Jack C. Lee, "High-Quality Ultra-

thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation," Technical Digest of Symposium on VLSI Technology (Highlight Session), pp. 15-16, 2001.

27. Easwar Dharmarajan, Wen-Jie Qi, Renee Nieh, Laegu Kang, Katsunori Onishi, and Jack C. Lee, "Ultra-Thin Zirconium Silicate Films With Good Physical and Electrical Properties for Gate Dielectric Applications," Material Research Society (MRS) Symposium Proceedings, vol. 648, 2000.

28. Laegu Kang, Katsunori Onishi, Yongjoo Jeon, Byoung Hun Lee, Chang Seok Kang, Wen-Jie Qi, Renee Nieh, Sundar Gopalan, Rino Choi, and Jack C. Lee, "MOSFET Devices with Polysilicon on Single-Layer HfO_2 High-K Dielectrics," International Electron Devices Meeting, IEDM Technical Digest, pp. 35-38, 2000.

29. Laegu Kang, Byoung Hun Lee, Wen-Jie Qi, Yongjoo Jeon, Renee Nieh, Sundar Gopalan, Katsunori Onishi, and Jack C. Lee, "Electrical characteristics of highly reliable ultrathin hafnium oxide gate dielectric," IEEE Electron Device Letters, vol. 21, no. 4, pp. 181-183, 2000.

30. Laegu Kang, Yongjoo Jeon, Katsunori Onishi, Byoung Hun Lee, Wen-Jie Qi, Renee Nieh, Sundar Gopalan, and Jack C. Lee, "Single-layer thin HfO_2 gate dielectric with n+-polysilicon gate," Technical Digest of Symposium on VLSI Technology, pp. 44-45, 2000.

31. Byoung Hun Lee, Rino Choi, Laegu Kang, Sundar Gopalan, Renee Nieh, Katsunori Onishi, Yongjoo Jeon, Wen-Jie Qi, Chang Seok Kang, and Jack C. Lee, "Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8-12Å)," International Electron Devices Meeting, IEDM Technical Digest, pp. 39-42, 2000.

32. B.W. Busch, W.H. Schulte, E. Garfunkel, T. Gustafsson, W.-J. Qi, R. Nieh, and J.C. Lee, "Oxygen exchange and transport in thin zirconia films on Si(100)," Physical Review B, vol. 62, no. 20, p. R13290, 2000.

33. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, and Jack C. Lee, "Study on ZrO_2 Deposited Directly on Si as an Alternative Gate Dielectric Material," Proceedings of Materials Research Symposium, vol. 606, 2000.

34. Wen-Jie Qi, Keith Zawadzki, Renee Nieh, Yongjoo Jeon, Byoung Hun Lee, Aaron Lucas, Laegu Kang, and Jack C. Lee, "A study on Hysteresis Effect of

Barium Strontium Titanate Thin Films for Alternative Gate Dielectric Application," Proceedings of Materials Research Symposium, vol. 606, 2000.

35. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, Katsunori Onishi, Sundar Gopalan, and Jack C. Lee, "Temperature Effect on the Reliability of ZrO_2 Gate Dielectric Deposited Directly on Silicon," International Reliability Physics Symposium (IRPS) Proceedings, pp. 72-73, 2000.

36. Wen-Jie Qi, Byoung Hun Lee, Renee Nieh, Laegu Kang, Yongjoo Jeon, Katsunori Onishi, and Jack C. Lee, "High-k gate dielectrics," Proc. SPIE Vol. 3881, Microelectronic Device Technology III, pp. 24-32, 2000.

37. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Katsunori Onishi, Laegu Kang, Yongjoo Jeon, Jack C. Lee, Vidya Kaushik, Bich-Yen Nguyen, L. Prabhu, K. Eigenbeiser, and Jeff Finder, "Performance of MOSFETs with ultra thin ZrO_2 and Zr silicate gate dielectrics," Technical Digest of Symposium on VLSI Technology, pp. 40-41, 2000.

38. Wen-Jie Qi, Renee Nieh, Easwar Dharmarajan, Byoung Hun Lee, Yongjoo Jeon, Laegu Kang, Katsunori Onishi, and Jack C. Lee, "Ultrathin zirconium silicate film with good thermal stability for alternative gate dielectric applications," Applied Physics Letters, vol. 77, no. 11, pp. 1704-1706, 2000.

39. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, and Jack C. Lee, "Electrical and reliability characteristics of ZrO_2 deposited directly on Si for gate dielectric application," Applied Physics Letters, vol. 77, no. 20, pp. 3269-3271, 2000.

40. Byoung Hun Lee, Laegu Kang, Renee Nieh, Wen-Jie Qi, and Jack C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," Applied Physics Letters, vol. 76, pp. 1926-1928, 2000.

41. Byoung Hun Lee, Laegu Kang, Wen-Jie Qi, Renee Nieh, Yongjoo Jeon, Katsunori Onishi, and Jack C. Lee, "Ultra-thin Hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application," IEDM Technical Digest, pp.133-136, 1999.

42. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, and Jack C. Lee, "Study on ZrO_2 Deposited Directly on Si as an Alternative Gate Dielectric Material," Proceedings of Materials Research Symposium, Fall 1999.

43. Wen-Jie Qi, Renee Nieh, Byoung Hun Lee, Laegu Kang, Yongjoo Jeon, Katsunori Onishi, Tat Ngai, Sanjay Banerjee, and Jack C. Lee, "MOSCAP and MOSFET characteristics using ZrO_2 gate dielectric deposited directly on Si," International Electron Devices Meeting, IEDM Technical Digest, pp. 145-148, 1999.

44. Laegu Kang, Byoung Hun Lee, Wen-Jie Qi, Yongjoo Jeon, Renee Nieh, Sundar Gopalan, Katsunori Onishi, and Jack C. Lee, "Highly Reliable Thin Hafnium Oxide Gate Dielectric," Proceedings of Materials Research Symposium, Fall 1999.

45. Byoung Hun Lee, Yongjoo Jeon, Keith Zawadzki, Wen-Jie Qi, Renee Nieh, Aaron Lucas, and Jack C. Lee, "Leakage characteristics of TiO_2 films," Proceedings of American Vacuum Society Texas chapter Symposium, Austin, 1998.

46. Keith Zawadzki, Wen-Jie Qi, Yongjoo Jeon, Byoung Hun Lee, Aaron Lucas, Renee Nieh, and Jack C. Lee, "Sputtered BST Thin Films for Alternative High K Gate Dielectrics," Proceedings of American Vacuum Society Texas chapter Symposium, Austin, 1998.

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