The Dissertation Committee for Mohammad Mehedi Hasan certifies that this is the approved version of the following dissertation:

TECHNOLOGY COMPUTER AIDED DESIGN AND ANALYSIS OF NOVEL LOGIC AND MEMORY DEVICES

Committee:

_____
Leonard F. Register, Supervisor

_____
Sanjay K. Banerjee

_____
Seth Bank

_____
Allan H. MacDonald

_____
Mark W. McDermott

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by

Mohammad Mehedi Hasan, B.S.E.E.; M.S.E.

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To my family and my educators

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TECHNOLOGY COMPUTER AIDED DESIGN AND ANALYSIS OF NOVEL LOGIC AND MEMORY DEVICES

Mohammad Mehedi Hasan, Ph.D.

The University of Texas at Austin, 2012

Supervisor: Leonard F. Register

Novel logic and memory device concepts are proposed and analyzed. For the latter purpose the commercial technology computer aided design (TCAD) simulators Taurus and Sentaurus Device by Synopsys are used. These simulators allow ready definition of complex device geometries. Moreover, while not all device physics models are state-of-the-art, the wide variety of device physics considered is advantageous here when not all of the critical device physics is known a priori.

The initial device concept analyzed was a one transistor (1T), one capacitor (1C) – pseudo-static random access memory (SRAM). Simulations indicate that tri-gate pass-transistors will offer better gate control and reduced leakage, and tri-gate capacitors will offer increased capacitance, making the overall device performance comparable to SRAM.

The second device analyzed was a quantum dot non-volatile memory. In principle, such memories become more reliable for a given tunnel oxide thickness by localizing any leaks to individual dots. However, simulations illustrate limits on dot packing density to retain this advantage due to inter-dot tunneling.

The final device, proposed and extensively analyzed here, is a novel tunnel field-effect transistor (TFET), the "hetero-barrier TFET" (HetTFET). In complementary metal-oxide-semiconductor (CMOS) logic, while switching power decreases with voltages, standby power increases due to thermionic emission of charge carriers over the source-to-channel barrier in the constituent metal-oxide-semiconductor field-effect transistors (MOSFETs). As a result, CMOS voltage and, thus, power scaling is approaching an impasse. Because TFETs are not subject to thermionic emission, they are being considering as a replacement for MOSFETs. Various materials systems and device geometries have been considered. However, even in simulation, balancing switching and standby power at low voltages while still providing sufficient transconductance for rapid switching has not proven straightforward. HetTFETs are intended to achieve high on-to-off current ratios via a threshold defined by the onset of band overlap, and high ON-state transconductances via tunneling through thin barriers defined by crystal growth, rather than relying on gate-controlled barrier narrowing in whole or part for either purpose as with other designs. Simulations of n and p-

channel HetTFETs suggest the possibility of current CMOS-like performance at much lower voltages.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1. INTRODUCTION

1.1 Reaching Scaling Limits and Implications for Device Design

For many years, the way to improve device performance was to just make them smaller, with limitations imposed largely by fabrication technologies. Of course, some changes often altered their detailed physics, such as the advent of quasi-ballistic transport in short channel metal-oxide-semiconductor field-effect transistors (MOSFETs). However, in recent years, we have encountered limits associated with essential physics that have forced the basic device designs themselves to be reconsidered. Of particular relevance to my work, to improve gate control in MOSFETs and perhaps to save device areas, planar designs are being abandoned for multi-gate structures including FinFETs. In flash memory, unconventional floating gate structures are being considered to allow continued tunnel-oxide scaling. And indeed, the industry is looking toward replacing the MOSFETs with devices that employ entirely different switching mechanisms, including gated band-to-band tunneling in tunnel FETs (TFETs).

1.2 One Transistor (1T) One Capacitor (1C) pseudo-Static Random Access Memory (SRAM) with FinFET Pass-Transistor

FinFET technology has greatly improved conventional Silicon (Si) and Silicon-Germanium (Si_xGe_{1-x}) based MOSFET devices' performance. An added benefit of having dual or triple gates in this FinFET technology is that it drastically increases gate capacitance on the same chip surface area as that of a planar transistor. Narrow fins with gates wrapped around provide better gate control over the channel area, reducing leakage and increasing drive current for the same applied bias, by inducing volume inversion as opposed to surface inversion as in conventional MOSFETs. A FinFET pass-transistor as the read/write access transistor in a Dynamic Random Access Memory (DRAM)-type cell can help reduce the refresh rate of the memory, saving both active and leakage power. Such power savings, coupled with reduced refresh rate, can enable these DRAM-like structures to one day replace Static Random Access Memory (SRAM) in both performance-intensive (e.g. Central Processing Unit (CPU)) and power-aware (e.g. Memories and Graphics for mobile devices) designs. I have defined and simulated the characteristics of the FinFET pass-transistor of a 1T-1C pseudo-SRAM device in this work to qualify and quantify its potential benefits in memory design.

1.3 Quantum Dot Flash Memory

In flash memory, the use of thinner tunnel oxides allows lower voltage charging. However, it also makes such devices more prone to failure through localized leakage paths through the tunnel oxide, where a single leakage path could lead to discharge of the entire floating gate. Breaking the floating gate up into quantum dots could substantially alleviate this problem. However, this approach raises issues that I explore through simulation of maximum quantum dot packing densities to prevent inter-dot tunneling and associated maximum threshold voltage V_{Th} shifts.

1.4 Stepped Broken-Gap Hetero-barrier Field Effect Transistor (HetTFET)

Low power and high performance transistors are the fundamental building blocks of modern computing especially in the mobile area. In MOSFET (metal-oxide-semiconductor field-effect transistor) based CMOS (complementary MOS) logic, power savings have been achieved through both device size and supply voltage V_{DD} downscaling. Both approaches, however, are now approaching limits defined by essential physics rather than fabrication technology. Gate oxide thickness, real or effective, are now subject to quantum mechanical tunneling through the gate oxide for some time now, and source-to-drain tunneling through the channel barrier provides an ultimate limit for channel length, and channel capacitance scaling. Voltage scaling is quickly approaching an impasse with the

essential physics of OFF-state thermionic emission of charge carriers over the channel barrier in MOSFET-based CMOS logic. To continue improving computing at a lower power cost, considering that 7% of the power consumption in the United States is related to integrated circuits [1], it will be necessary to find a better transistor and perhaps even an associated new way computing. Here, I consider only the less drastic solution, a new transistor within a CMOS-like framework, and focus on the challenge of voltage scaling.

TFETs based on gated band-to-band tunneling are being widely considered for this purpose. TFETs are not nominally subject to thermionic emission, but they face their own challenges. Toward addressing these latter challenges, we have proposed a novel stepped-broken-gap variation on hetero-structure TFETs that we dubbed the "HetTFET" [28]. I explore the low-voltage device characteristics of n-channel and p-channel HetTFETs toward voltage scaling and performance retention. I consider both channel-normal tunneling and channel-parallel-tunneling within, specifically, single-gate and double gate geometries, respectively.

1.5 Use of Commercial Technology Computer Aided Design (TCAD) Software

For the purpose of simulating the novel memory and logic devices described above, the commercial technology computer aided design (TCAD) simulators Taurus and Sentaurus Device by Synopsys have been used [5][7]. These simulators allow ready definition of complex device geometries. Moreover, while not all device physics models are state-of-the-art, the wide variety of device physics considered is advantageous here when not all of the critical device physics is known a priori. The usage of these simulators and models available in them are further elaborated in a latter chapter.

1.6 Organization of the Dissertation

This dissertation is organized as following: In Chapter 2, I briefly describe industry-standard simulation tools chosen for this work, motivations behind choosing them, and relevant models available within these tools. In Chapter 3, I describe work on one transistor (1T), one capacitor (1C) pseudo-Static Random Access Memory (SRAM) devices. In Chapter 4, I describe work on quantum dot memory devices. In Chapter 5, I review and discuss in greater detail the need for reduced power consumption, the basic requirements for CMOS—or at least CMOS-like—circuits to minimized power consumption while still providing high performance, and detail voltage scaling limitation imposed by

thermionic emission over the MOSFET channel barrier top toward achieving these goals. I then describe the Zener tunneling concept [8] [9], based on which all band-to-band tunnel transistors are built, and I summarily review notable work that has already been done in the field of band-to-band tunnel transistors, to shed light on the benefits and drawbacks of band-to-band tunnel transistor designs that have been proposed so far. In this chapter, I also discuss some of my preliminary efforts as well to illustrate the challenges. In Chapter 6, I describe a novel III-V-semiconductor-based stepped broken-gap hetero-barrier TFET (HetTFET), describe its essential operating principles beyond simply tunneling, and discuss simulation results. In Chapter 7, I discuss preliminary simulation work toward a Junction-FET (JFET)-like variant of the HetTFET. In Chapter 8, I conclude with a brief summary of the work and propose future exploratory paths for HetTFETs and other similar devices.

CHAPTER 2. SIMULATION TOOLS FOR MODELING OF NOVEL MEMORY AND LOGIC DEVICES

2.1 Simulation Tools Chosen and Motivation

To simulate the 1T-1C pseudo-SRAM, the non-volatile quantum dot memory, and the homo and hetero-barrier TFETs, I have chosen Synopsys commercial Technology Computer Aided Design (TCAD) - Taurus [5], Datex [6] and Sentaurus [7] device design and modeling tools. These simulators allow ready definition of a wide variety of complex device materials and their properties. While not all device physics models are state-of-the-art, the wide variety of device physics considered is advantageous here when not all of the critical device physics relevant to these novel devices is known beforehand. The tools are also flexible enough to allow novel device geometries. Accordingly, these tools have been and are being widely used to simulate various semiconductor device, especially TFET designs [1][16][22][23][24][25][26][28][33][34][35].

2.2 Modeling for Homo and Hetero-barrier TFETs

For the simulations of the homo-barrier TFET devices described in chapter 5, the generally accepted Kane's band-to-band tunneling model has been used from Synopsys TCAD Taurus Device [5]. The equation is as follows:

$$G^{BB} = A.BTBT \frac{\xi^2}{\sqrt{E_g}} e^{-B.BTBT \frac{E_g^{\frac{3}{2}}}{\xi}}, \qquad (1)\ [5]$$

Here, G = conductance, and $A.BTBT$, $B.BTBT$ = fitting parameters, E_g = band gap of the semiconductor, and ξ = electric field.

Synopsys TCAD Taurus Device simulator used for simulations first performs a search along the direction opposite to the electric field to determine if there is an electric potential increase of at least E_g/q for the band-to-band tunneling to occur. Out of a few models, the model considered was the one where the tunneling electron generation rate is calculated non-locally; in this case, electrons are generated at the end of tunneling length [5].

For the Hetero-barrier TFET device, Synopsys TCAD Taurus Device 2-D [5] was again used, but only for device construction and mesh creation. Synopsys DATEX software [6] was then used to convert the constructed device and its mesh from .tdf format to .tdr format. Finally, Synopsys TCAD Sentaurus Device 2-D simulator [7] was used for full device simulation and characterization. Synopsys TCAD Sentaurus Device has a non-local barrier tunneling model that is

ideally suited for hetero-barrier tunnel device simulation. It computes the tunneling probability for an electron from the valence band to the conduction band using the modified-Wentzel-Kramer-Brillouin (WKB)-approximation considering the potential profile along the tunneling path [17][18]. Non-local tunneling model is self-consistently solved with Poisson and Continuity equations. The tunneling carrier generation rate is calculated with the following equation:

$$G(r) = gA\frac{T}{\kappa_B}F(r)P(r)\ln\frac{1+e^{\frac{E(r)-E_{s2}}{\kappa_B T}}}{1+e^{\frac{E(r)-E_{s1}}{\kappa_B T}}} \quad , \qquad (2)\ [7]$$

where, P(r) = Modified-WKB approximation for the tunneling probability, g = A_s/A with A_s = Richardson constant for carriers in semiconductor, A = Richardson constant for free electrons, F(r) = Electric field, E(r) = Carrier energy, E_{s2} = Carrier quasi-Fermi energy in semiconductor 2, E_{s1} = Carrier quasi-Fermi energy in semiconductor 1.

Sentaurus Device creates the tunneling path for simulation as shown in Figure 1 [7]. First an approximate tunneling path length is specified in the command file. The simulator then creates specific points for calculating the generation rate G(r). The actual tunneling depth is then determined through iterating simulations.

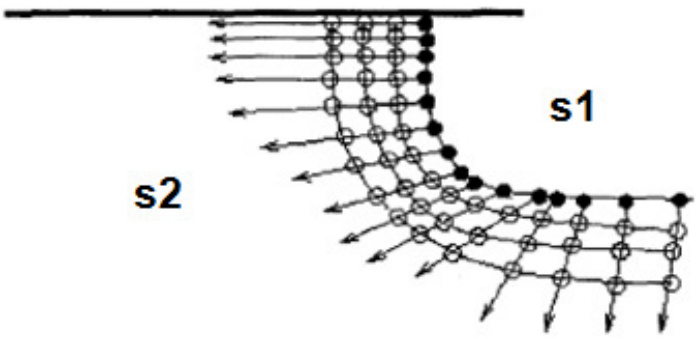


Figure 1. Non-local tunneling path calculation in Sentaurus Device [7]

CHAPTER 3. ONE TRANSISTOR (1T) ONE CAPACITOR (1C) PSEUDO-STATIC RANDOM ACCESS MEMORY (SRAM) DEVICE

3.1 Modeling Work on the FinFET Pass-Transistor of a 1T-1C pseudo-SRAM Device using TCAD Taurus Device

I have already briefly discussed the motivations behind simulating the characteristics of the FinFET pass-transistor of a 1T-1C pseudo-SRAM memory device in Chapter 1. To reiterate, though Dynamic Random Access Memories (DRAMs) offer greater packing density when compared to Static Random Access Memories (SRAMs), currently they are not used in performance-intensive or power-aware designs because of two weaknesses. In performance-intensive memory designs, "read" and "write" cycles are quite short. Reading a DRAM requires discharging the bit-line through the pass-transistor. Because a lot of DRAM cells are suspended from the bit-line, the bit-line capacitance is quite high. Discharging such high load capacitance in a short amount of time requires the pass-transistor size to be increased. Herein lays the trade-off problem of all DRAMs. If the pass-transistor size is increased, then the leakage through the pass-transistor increases, which can rapidly drain out the charges stored in the DRAM capacitor. If the pass-transistor size is decreased, then the bit-line load

capacitance discharge can take a lot more time when compared to actively-driven six-transistor (6T) SRAM cells. Thus, DRAMs are not currently used in performance-intensive applications, such as memories of Central Processing Units (CPU). Furthermore, DRAM "read" operations are destructive, meaning that a "write" has to be performed after every "read", which costs active power. In addition, due to leakage through the pass-transistor, a DRAM cell may have to be refreshed often, requiring even more active power. Thus despite requiring only one-third area of a SRAM bitcell due to having effectively a two-transistor construction as opposed to SRAM's six transistors, a DRAM cell is suitable neither for performance-intensive nor for power-aware operations. DRAMs are currently mostly used as extended system memories where their densities provide greater benefits.

However, if the leakage (thus refresh rate) and performance metrics of the DRAM cell can be improved to the extent that they are roughly comparable to those of SRAM cells, then such a DRAM cell can essentially be called pseudo-SRAM [36]. FinFETs, built on gate wrap-around technology, offer precisely these benefits. Hence I have defined and simulated the characteristics of the FinFET pass-transistor of a 1T-1C pseudo-SRAM device using TCAD Taurus Device [5]. Figure 2 is the picture of the FinFET pass-transistor. The height of the fin is 66 nm. The effective oxide thickness (EOT) is 1 nm, with the modeled

oxide being Hafnium-dioxide (HfO_2). Source and Drain doping is specified to be $10^{20}/cm^3$.

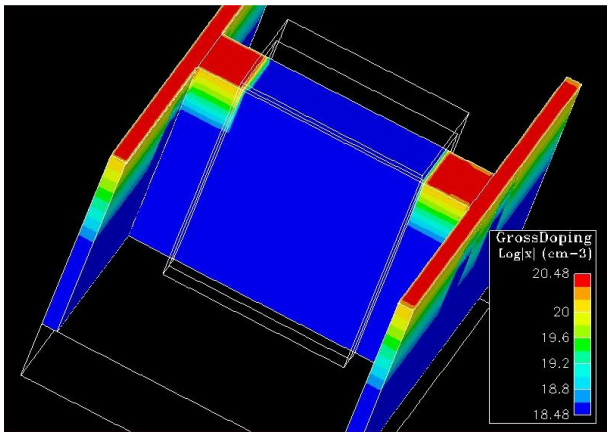


Figure 2. TCAD Taurus build of a FinFET pass-transistor

Figure 3 shows the gate leakage characteristics of the FinFET pass-transistor. Due to the usage of High-κ dielectrics, the gate leakage in this case is so small that it is negligible. The FinFET pass-transistor leakage would thus likely be dominated by subthreshold leakage, as shown in latter figures.

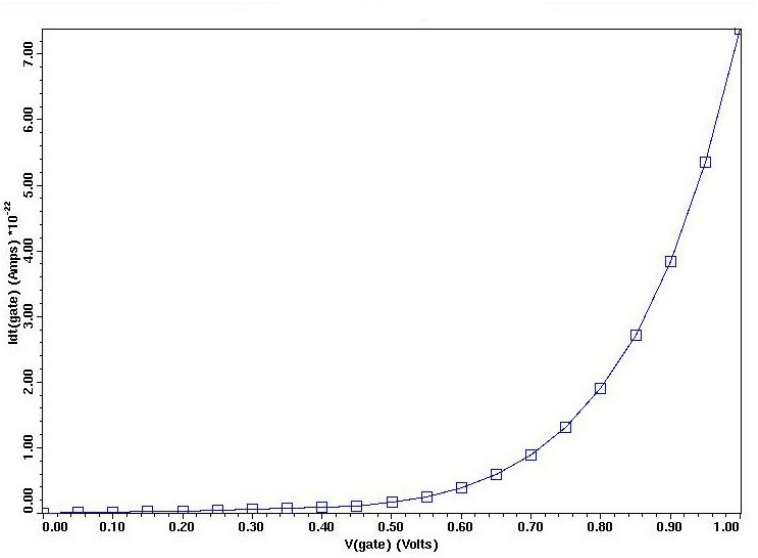


Figure 3. Taurus simulation of FinFET pass-transistor gate leakage

Figure 4 and Figure 5 show the FinFET pass-transistor's I_{DS} vs. V_{GS} characteristics at V_{DS} = 0.1 V and V_{DS} = 1.2 V. In both of these figures, subthreshold slope is approaching less than 100 mV/decade, which when compared to typical conventional planar MOSFET, and keeping in mind that the MOSFET technology is applicable to both planar MOSFETs and FinFETs, is limited fundamentally to 60 mV/decade subthreshold slope limit, is both a qualitative and quantitative improvement. ON-state drive current in the range of ~0.10 mA/μm is also comparable to mid-performance planar MOSFETs.

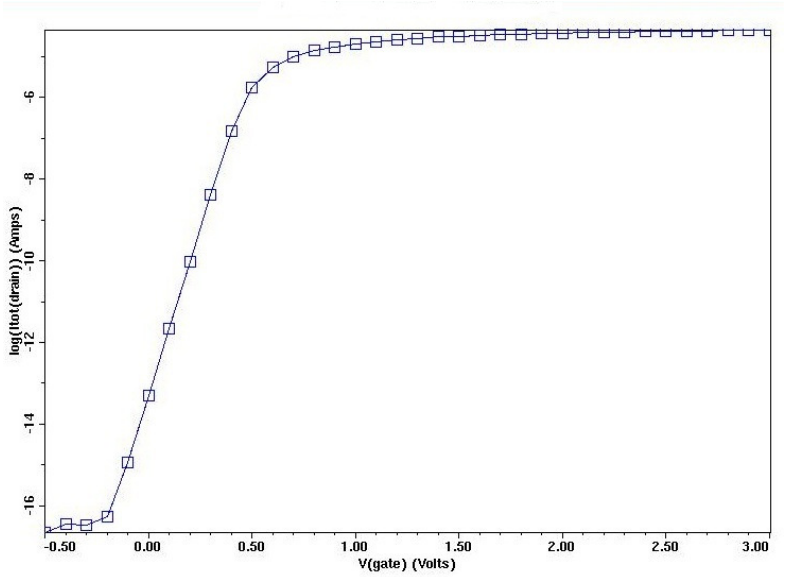


Figure 4. log(I_{DS})-V_{GS} of the FinFET pass-transistor at V_{DS} = 0.1 V

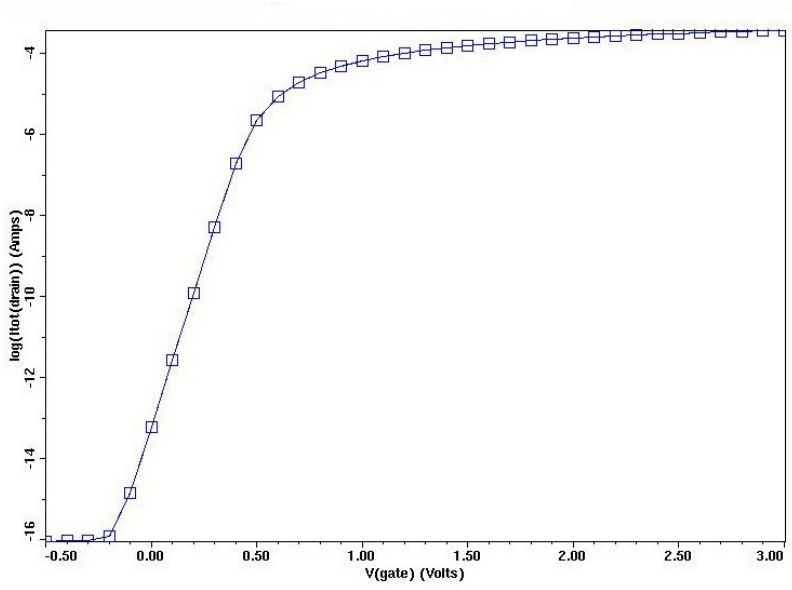


Figure 5. log(I_{DS})-V_{GS} of the FinFET pass-transistor at V_{DS} = 1.2 V

Finally Figure 6, Figure 7, Figure 8, and Figure 9 show the FinFET pass-transistor's I_{DS}-V_{DS} characteristics at V_{GS} = 0.3 V, 0.6 V, 0.9 V, and 1.2 V, all of which show characteristics similar to conventional planar MOSFETs.

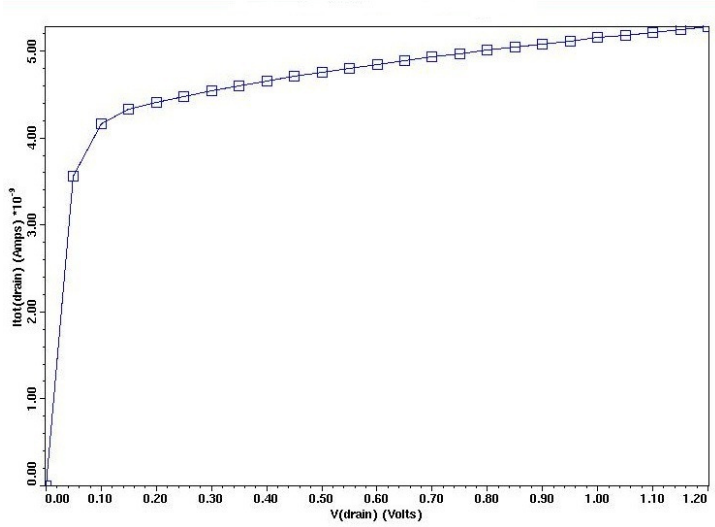


Figure 6. I_{DS}-V_{DS} simulation of the FinFET pass-transistor at V_{GS} = 0.3 V

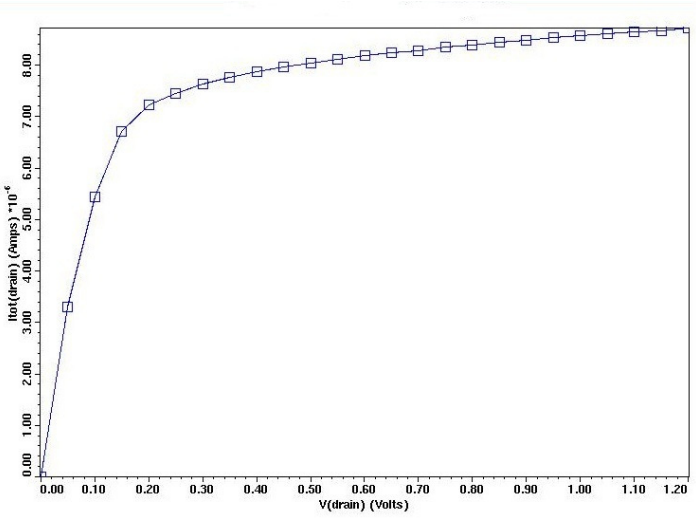


Figure 7. I_{DS}-V_{DS} simulation of the FinFET pass-transistor at V_{GS} = 0.6 V

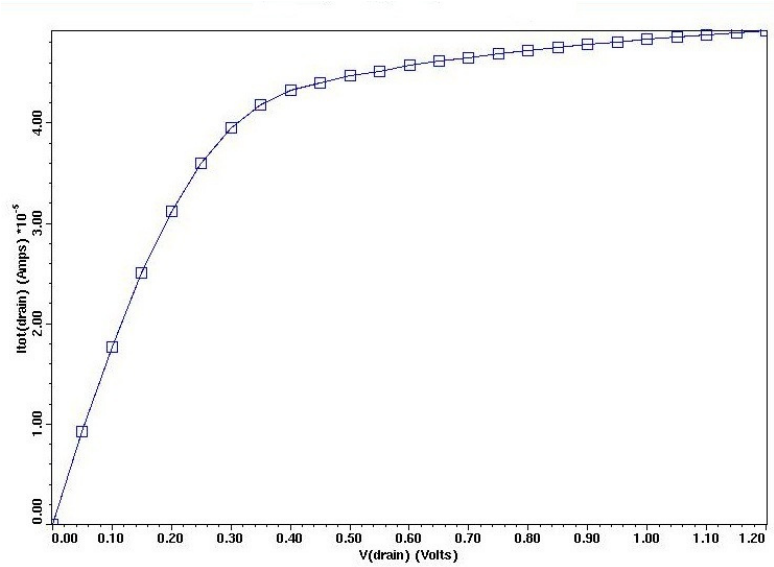


Figure 8. I_{DS}-V_{DS} simulation of the FinFET pass-transistor at V_{GS} = 0.9 V

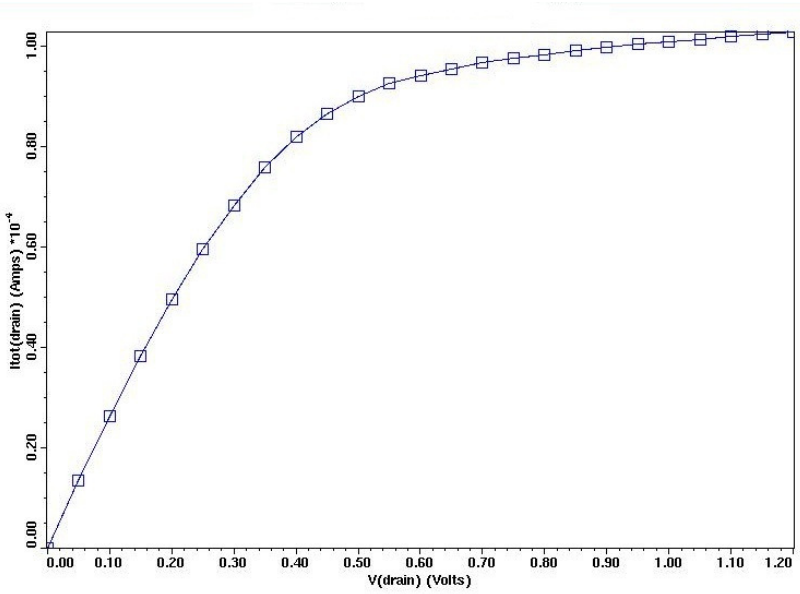


Figure 9. I_{DS}-V_{DS} simulation of the FinFET pass-transistor at V_{GS} = 1.2 V

To summarize, the various I_{DS}-V_{GS} and I_{DS}-V_{DS} simulations above show that using a FinFET pass-transistor in a 1T-1C pseudo-SRAM cell provides comparable drive current and transconductance, thus performance, to planar MOSFETs, while also providing reduced subthreshold leakage, and almost negligible gate leakage due to usage of high-κ gate dielectric. Though not simulated or shown here, device capacitance is much greater in a Fin-capacitor than a planar MOS-capacitor, for the same chip area. An 1T-1C DRAM-like memory cell, combining the FinFET pass-transistor and Fin-capacitor, can thus be a viable alternative to conventional six transistor (6T), actively-driven SRAM memory cell, providing at least close to three times better packing density [36].

CHAPTER 4. QUANTUM DOT NON-VOLATILE MEMORY DEVICE

4.1 Modeling Work on Quantum Dot Memory Device using TCAD Taurus Device

I have done exploratory simulation work on a quantum dot memory device structure using Synopsys TCAD Taurus Device to analyze the device's reliability [5]. Compared to conventional disc-based mechanical hard drive memories, non-volatile or flash memories offer no moving parts, and thus much greater reliability, especially in mobile applications. However non-volatile memories are in limited use due to restrictions on the number of times "write" operations can be performed to these cells. They also typically offer much lower storage volume compared to magnetic disc drives. Hence the current industry effort is focused on increasing the number of "write" cycles that can be performed on non-volatile memory cells as well as increasing storage volume in flash memory drives.

Increasing storage volume by packing more cells in a limited area offer several distinct advantages from a system level perspective. Firstly, it offers higher density, thereby lowering manufacturing cost. Secondly, more memory volume not only make non-volatile memory drives competitive with conventional hard drives in terms of capacity, it also provides improved reliability by making

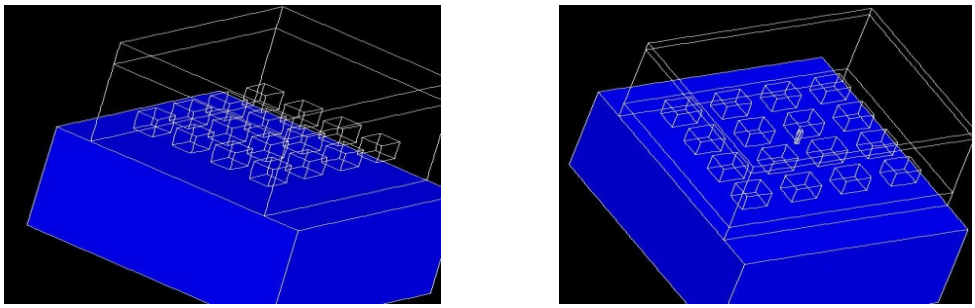
sure that "write" operations are performed over many distributed cells and that the same cell is not written to over and over again. The "write" operation restriction on non-volatile memory primarily comes from the application of high voltage during write cycles—which leads to tunnel oxide breakdown and trap-induced tunneling after repeated write operations, whereby cells simply leak out the charges stored in the floating gate. Apart from this problem, non-volatile memories offer much better performance due to their electrical operation rather than mechanical operation as in conventional disc drives.

Quantum-dot non-volatile memories address this reduced reliability problem due to tunnel oxide breakdown by using disconnected, physically separate dots as opposed to a continuous floating gate. This scheme has two-fold benefits. Firstly, the disconnected dots make sure that if there is a leakage path in the tunnel oxide, then it does not affect all dots at once as it does in a continuous floating gate. Secondly, by scaling the dot-to-dot oxide, the packing density can be increased, and by scaling the tunnel oxide, the "write" voltage can be reduced.

Thus, in this work, I address through simulation, the issues of inter-dot tunneling and tunneling between the channel and the dots through the tunnel oxide, which are the biggest concerns for quantum dot memories. The inter-dot tunneling mechanism can lower V_{Th} by leaking electrons from dot(s) to dot(s) that have higher tunneling probabilities to leak to the channel. This leakage can occur if the dot-to-dot distance is too small to prevent inter-dot tunneling, and if dot(s)

are leaking to the channel. Direct tunneling between the dots and the channel can also lower V_{Th} and is more likely if the tunnel oxide thickness is smaller than the inter-dot distance.

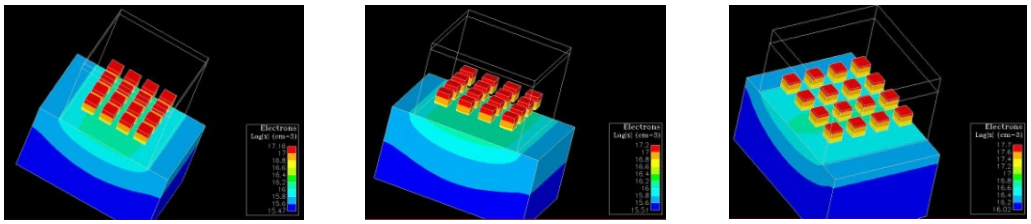
The Synopsys Taurus-simulated device in Figure 10 consisted of 16 Silicon dots. The control and tunnel oxide thicknesses were specified to be 13 nm and 4 nm, respectively, and chosen in consultation with ITRS guidelines [2]. The individual dot dimensions were 4 nm x 4 nm x 4 nm. The inter-dot distances were varied (2 nm, 3 nm, 4 nm) among different cases to study inter-dot tunneling. A "programming" simulation on the devices with different inter-dot distances but same control and tunnel oxide thicknesses was performed. In one case (Figure 10(a)), none of the dots was shorted to channel, emulating absence of leaky dots. In other case (Figure 10(b)), one of the dots was shorted to channel to emulate the behavior of the device in presence of a leaky dot.



(a) With no dot shorted to channel (b) With a dot shorted to channel

Figure 10. Quantum dot memory device with 4nm inter-dot distance

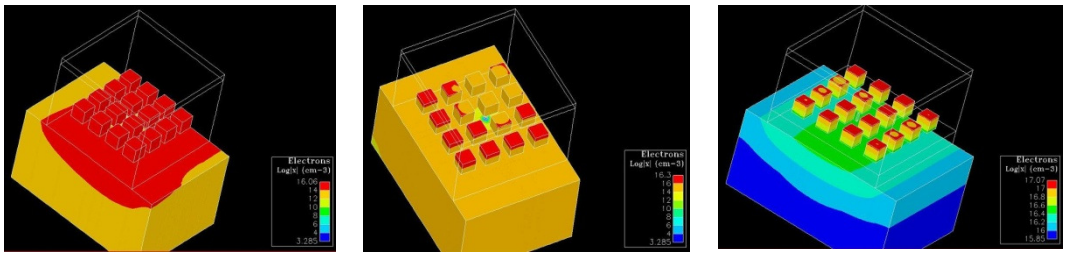
2 nm inter-dot distance 3 nm inter-dot distance 4 nm inter-dot distance



Max. e-conc. $10^{17.16}/cm^3$ Max. e-conc. $10^{17.2}/cm^3$ Max. e-conc. $10^{17.7}/cm^3$

Figure 11. "Programming" of memory device with no leaky dots and different inter-dot distances

2 nm sep. w/ 1 leaky dot | 3 nm sep. w/ 1 leaky dot | 4 nm sep. w/ 1 leaky dot



Max. e-conc. $10^{16.06}/cm^3$ | Max. e-conc. $10^{16.3}/cm^3$ | Max. e-conc. $10^{17.07}/cm^3$

Figure 12. "Programming" of memory device with 1 leaky dot and different inter-dot distances

As can be seen from the results in Figure 11 and Figure 12, the increased inter-dot distances result in higher electron-concentration in the dots despite, in the case of Figure 12, the device having one leaky dot with respect to the channel. This result clearly points to increased reliability of quantum dot memories where the memory cell is able to retain most of its charge despite having localized tunneling path(s) to the channel. It can be further noted from Figure 11 and Figure 12 that a leaky memory device has lower electron density than one without any leaky dot, even with large dot separation. It should also be noted that as the dot density is increased by reducing their inter-dot distances, the reduction in electron-concentration between a device with and without a leaky dot is more pronounced, pointing to the fact that increased dot-to-dot distance reduces inter-dot tunneling, enabling individual dots to retain more charge. These results point

to the trade-off between maximum charging, and, thus, maximum threshold shift, and device reliability over time.

CHAPTER 5. CMOS-LIKE CIRCUIT REQUIRMENTS, ZENER TUNNELING, AND PRIOR TUNNEL-FET WORK

5.1 Background

In this chapter, I describe the need for reduced power consumption, the device requirements of CMOS or CMOS-like circuits to reduced power consumption while still providing high performance, and detail voltage scaling limitations imposed by thermionic emission over the MOSFET channel barrier top toward achieving these goals. I also discuss the Zener tunneling concept [8][9], and I summarily review notable work that has already been done in the field of band-to-band tunnel transistors, to shed light on the benefits and drawbacks of band-to-band tunnel transistor designs that have been proposed so far.

5.2 CMOS-like Circuit Requirements and Limits for MOSFETs

As a framework for the device discussion, we begin with a brief review of the source of the voltage-scaling impasse and the circuit and—or vs.—device requirements for any MOSFET alternative.

To achieve high performance in CMOS—or CMOS-like—logic requires the ability to quickly charge the following transistor stages and interconnects, i.e.,

quickly charge the load capacitance C_L. With the voltage swing given by the power supply voltage V_{DD}, the switching time τ_s to charge or discharge C_L is roughly,

$$\tau_s \cong \frac{V_{DD}C_L}{I_{ON}} \cong \frac{V_{DD}C_L}{g_m(V_{DD} - V_{Th})}, \tag{3}$$

assuming drive current through an n-channel MOSFET for specificity, where C_L has been approximated as constant for simplicity for illustrative purposes. Here, $g_m = dI_{ON}/dV_G$ is the ON-state transconductance, V_{Th} is the threshold voltage for turning on the MOSFET, and I_{ON} is the MOSFET on-state source-to-drain current for the gate voltage V_G equal to V_{DD}. Therefore, fast switching requires a large g_m and an overdrive voltage $V_{DD} - V_{Th}$ that is at least comparable to V_{Th}. To be clear, however, fast switching alone does not intrinsically require a large I_{ON} or V_{DD}; to the extent V_{Th} can be reduced, so can I_{ON} and V_{DD} without sacrificing performance.

One limit on V_{Th} is the ability to control device-to-device variability. However, even absent that technological limitation, V_{Th} remains limited by intrinsic power P considerations. P, consisting of both stand-by (steady-state) power P_{SS} and switching (active) power P_A, must be controlled. The stand-by (steady-state) power is given by,

$$P_{SS} = I_{OFF}V_{DD}, \tag{4}$$

where I_{OFF} is the off-state leakage current through the gate. Within the approximations of Eq. (3), time-averaged switching power is given by roughly,

$$P_A = C_L V_{DD}^2 \alpha f_C = I_{ON} V_{DD} \alpha t_S f_C , \quad (5)$$

Here, α is the activity factor, the fraction of clock cycles during which the gate is actually switched. f_C is the clock frequency and, thus, and $t_S f_C$ is the fraction of the clock cycle required to change the gate output. Combining Eqs. (4) and (5) gives,

$$P = P_A \left[1 + \frac{P_{SS}}{P_A} \right] = P_A \left[1 + \frac{1}{\alpha t_S f_C \, (I_{ON}/I_{OFF})} \right] , \quad (6)$$

At one time P_{SS} was small compared to P_A. However, with reductions in V_{DD} and commensurate reductions in V_{Th} to maintain short switching times, P_{SS} increases rapidly, much faster than P_A decreases. As a result, an impasse for V_{DD} reduction is reached when P_{SS} and P_A become approximately equal, or from Eq. (6), when,

$$\frac{I_{ON}}{I_{OFF}} \approx \frac{1}{\alpha t_S f_C} \quad , \quad (7)$$

The factor $\alpha t_S f_C$ can be quite small as α can vary from unity for a clock to perhaps to ~0.01 depending on application, and $t_S f_C$ must allow for sequential switching of ten or more logic gates during a single clock cycle in CMOS. Therefore maintaining large I_{ON}/I_{OFF} current ratios is essential for CMOS-like logic.

For MOSFETs specifically, the change in I_{OFF} with V_{Th} is characterized by a subthreshold slope with a minimum theoretical value of,

$$S_{min} = \ln(10)\frac{k_B}{T} \cong \frac{60\,\text{mV}}{\text{decade}}\left(\frac{T}{300\,\text{K}}\right), \tag{8}$$

where k_B is Boltzmann's constant, T is temperature, and 300 K is roughly room temperature. At least consistent with the above discussion, "end-of-the-roadmap" estimates of MOSFET threshold voltages V_{Th} to maintain sufficient ON-state current I_{ON}/I_{OFF} ratios are 0.19V and 0.37V for low-operating-power and low-standby-power applications [2], respectively, or about 3 and 6 times the minimum room temperature value of S_{min}.

Combining the requirements for fast switching (Eq. (3)) with these latter values of V_{Th} to control power consumption, leads to end-of-the-roadmap values of V_{DD} of 0.5V and 0.7V [2], respectively for MOSFET-based CMOS logic. Even for high-performance applications requiring smaller ON/OFF ratios but also more speed, the limiting supply voltage appears to be 0.7V [2].

To summarize, $V_{DD} - V_{Th}$ values comparable to V_{Th} and substantial g_m for fast switching, and a large I_{ON}/I_{OFF} current ratios for minimizing power consumption, are intrinsic requirements for CMOS-like logic. However, end-of the roadmap limitations on minimum V_{Th} and, thus, minimum V_{DD} and I_{ON} are intrinsic only to the physical mechanism of subthreshold thermionic emission in MOSFETs, along with device-to-device variability considerations.

Finally, we must acknowledge that attempts to reduce V_{Th} must not substantially increase device size and associated load (gate and interconnect) capacitance C_L, which affects both performance (Eq. (3)) and active power (Eq. (5)).

5.3 Band-to-Band (Zener) Tunneling

Band-to-band tunneling or Zener tunneling is a well-known process. Heavily doped reverse biased p-n junctions show a drastic current increase under moderate reverse bias due to electrons tunneling from the valence band to conduction band under high electric fields [8] [9]. (Lower doped ones, show an increase at higher reverse bias due to the entirely different mechanism of impact ionization.) The basic process is shown in Figure 13 [10]. The p^+ side is heavily doped with p-type dopants such as boron, while the n^+ side is heavily doped with n-type dopants such as phosphorus. Application of a gate-bias can make the tunnel barrier in the middle thin enough to allow for electrons to migrate from the valence band on the left hand side to the conduction band on the right hand side.

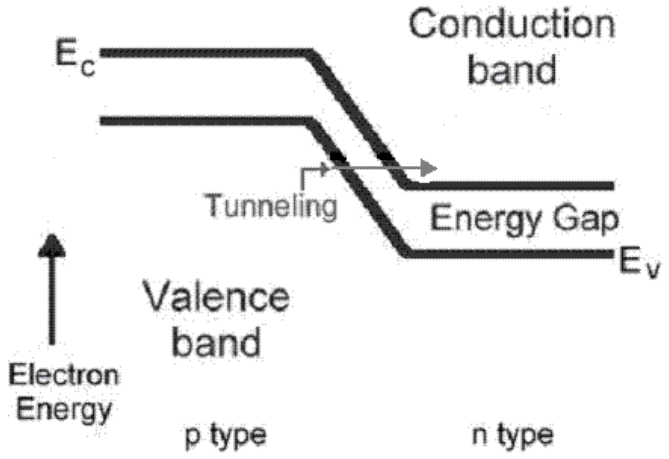


Figure 13. Zener tunneling process [10]

For tunneling associated with barrier thinning, the tunneling probability, $P_{\text{tunneling}}$, is frequently modeled by the following Eq. (9) [8].

$$P_{tunneling} = e^{-\left(\frac{4}{3}\right)\left(\sqrt{2m}\right)\frac{(2\pi)}{eFh}\left(E_g^{2/3}\right)} \quad (9)\ [8]$$

Here, m = electron mass, F = electric field, h = Planck's constant, and E_g = band-gap. As can be seen from this equation, a smaller band-gap semiconductor material, and a higher field, produced via high-doping for a given voltage bias, rapidly increases the tunneling probability of electrons.

However, of course, conduction band-to-valence band overlap remains a prerequisite. In the Esaki diode, as illustrated in Figure 14 [3], the Fermi level on the n^+ side is inside the conduction band while the Fermi level on the p^+ side is inside the valence band, and there is conduction band to valence band overlap under no bias. As the bias is increased to V_1, inter-band tunneling occurs and

current continues to increase. When the bias is V_2, the conduction band on the n^+ side is no longer aligned with the valence band on the p^+ side anymore. At this stage, the current decreases due to the lack of allowed states with corresponding energies that allow for tunneling. As the bias is further increased to V_3, current associated with the conventional mechanism of thermionic emission of charge carrier over the potential barrier in each band then dominates [3].

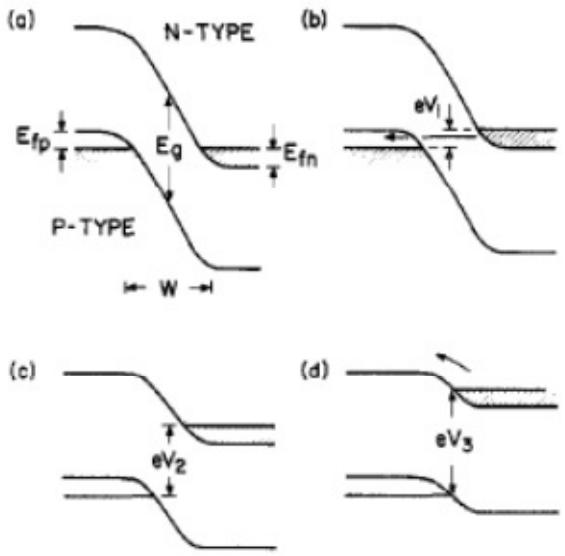


Figure 14. Tunnel diode band diagram at bias levels (V_1<V_2<V_3) [3]

In diodes, the band overlap and field is controlled self-consistently by the terminal currents. However, to the extent the barrier field and band overlap could be controlled by a gate bias, the field-induced variation of the tunneling current could be used for switching as well.

5.4 Prior Work on Tunnel-FETs

In the late 1980s, the possibility of a three-terminal MOS Zener tunneling device was first reported, as shown in Figure 15 [4][11]. The p^+ doping in the device is roughly $10^{19}/cm^3$, and the band-to-band tunneling occurs in this region. Electron-hole pairs are produced by the Zener breakdown of the p^+ Si-substrate, and electrons tunnel from the valence band to the conduction band. If the doping densities are lower, despite a larger band-bending, the depletion region becomes too wide for Zener tunneling to take place. If doping is beyond what is mentioned in [4], despite having a high surface electric field, most of the voltage drop occurs across the insulator, and band-bending becomes less than the band-gap, and as a result, no Zener tunneling occurs [4][11].

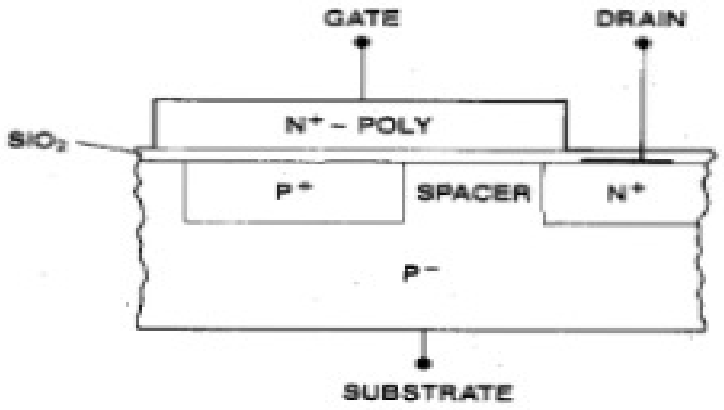


Figure 15. MOS tunneling device [4]

In 2004, band-to-band tunneling in Carbon nano-tube field effect transistors (CNFET) was reported in [12]. A Schottky barrier Carbon nano-tube

FET was used and it was observed that application of a bias voltage in the gate can cause electrons to tunnel between the conduction band and the valence band of the semiconducting carbon nano-tube. The combination of thin gate insulator with small diameter nano-tubes allow for both high tunneling current and an abrupt switching that is crucial in keeping the sub-threshold swing low [12]. The CNFET has a sub-threshold swing of 40 mV/decade at room temperature, at least at one point, showing that it's not limited by thermionic emission. However, average subthreshold swing over a subthreshold voltage range large enough to achieve the required ON/OFF current ratio and provide acceptable ON current above threshold was still not sufficient.

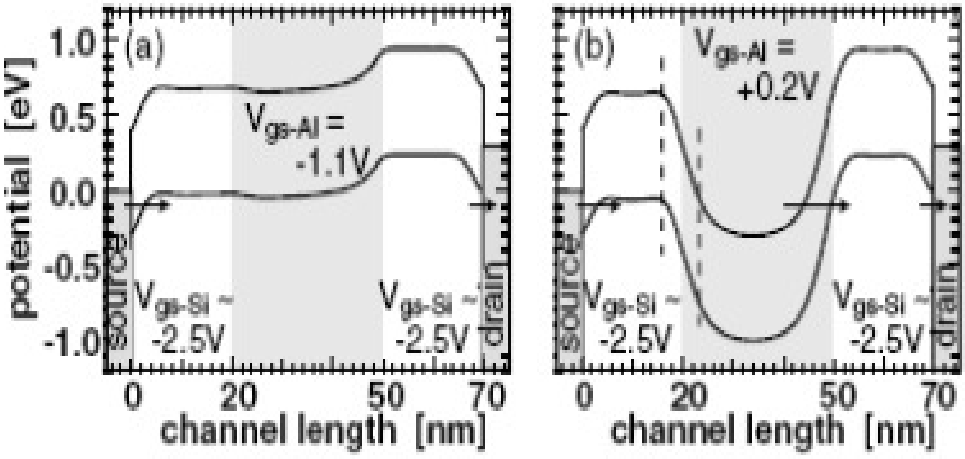


Figure 16. Band-to-band tunneling phenomenon in CNFET [12]

A variety of other materials and geometries have been considered over the years. "Green FET" (gFET) variations, based primarily on Silicon (Si) and Silicon-Germanium (SiGe) were introduced in 2008 [1][25][26]. Gate-parallel

[12][14][19][20][21][22][23][24] and gate-normal tunneling geometries [1][4][25][26][33] have been investigated. And devices employing staggered-gap (Type II) hetero-interfaces [22][25][26][34][35] and nominally broken-gap (Type III) hetero-interfaces within quantum wires [23][24][32] have been proposed, although with quantum confinement effects in the latter, they remained staggered-gap by design. However, while progress has been and is being made, obtaining large I_{ON}/I_{OFF} to balance switching and standby-power, sufficient g_m for rapid switching, and low V_{DD} for overall low power in a combination to widely challenge CMOS has not proven straightforward even in simulation. In particular, establishing a super-steep (sub-60 mV) subthreshold slope below some gate voltage and large transconductance above another is of limited value, at least as an end product, if the gap between these voltages is MOSFET-like or larger.

5.5 Preliminary Research Work on Homogenous TFET

Silicon (Si)-based TFETs are preferred because it would require minimal processing changes in fabrication of the devices, which would translate to large cost savings for mass-scale production. Also as a material, Si is cheaper than III-V semiconductors, e.g. Gallium Antimonide (GaSb), Indium Arsenide (InAs). Hence I started evaluating the homogenous surface-normal tunneling FET with Si as the primary substrate material. Si provides a mid-scale band-gap among

various semiconductor materials, ~1.12 eV and growing the dielectric material, SiO_2, has already been perfected over the years by the industry.

5.6 Si-based TFET with Surface-Normal direction Tunneling

The proposed Si-based TFET has a tunneling direction that is normal to the channel surface. In most of the proposed TFET structures published to date, the tunneling occurs in lateral direction with respect to the channel surface [14],[19],[20],[21],[22],[23],[24]. Tunneling normal to the transport direction creates a stronger tunneling current compared to similarly doped lateral TFETs due to the large surface area available for tunneling to occur directly beneath the gate [1],[4],[25],[26],[33],[34],[35]. As tunneling occurs over a large area, a significant number of electrons tunnel from the valence band of the p^+ region to the conduction band of the p^+ region, and then falls off toward the n^+ region as the conduction band level falls. The device structure is shown in Figure 17.

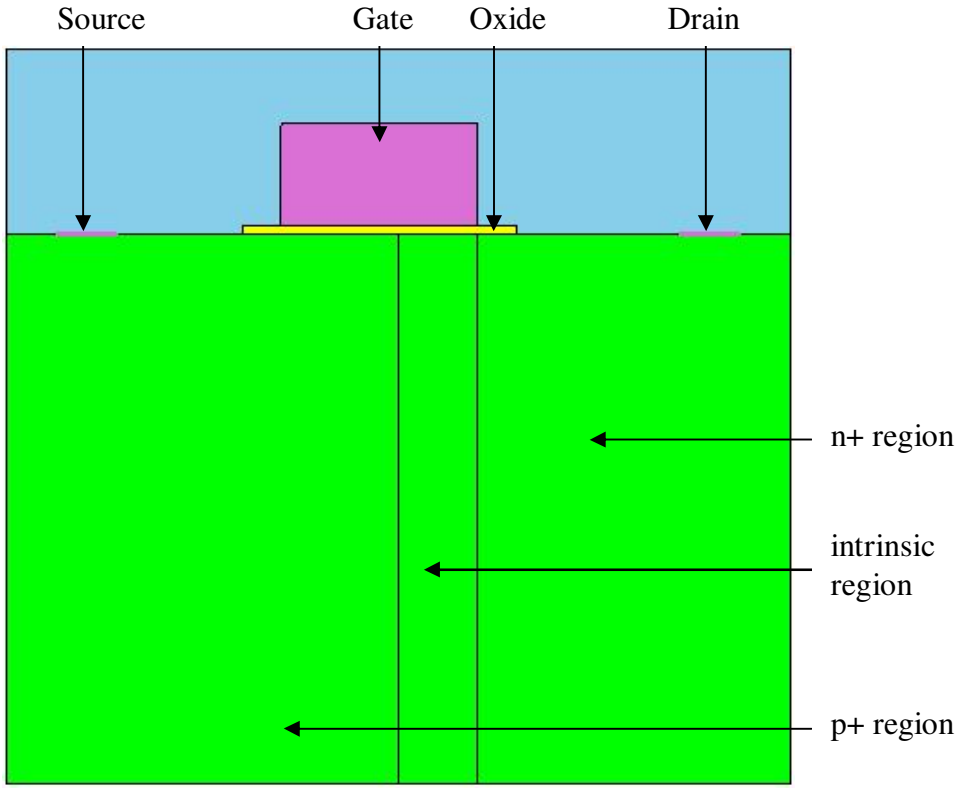


Figure 17. Si-TFET with surface-normal tunneling mechanism

5.7 TCAD Simulation of Si-TFET

In the first simulation, dubbed case-1, the n-type doping for the n^+ region is set to $2x10^{21}/cm^3$ and the p-type doping for the p^+ region is set to $10^{21}/cm^3$. The oxide thickness is 1 nm; widths of the p^+, intrinsic, and n^+ regions are 50 nm, 10 nm, and 40 nm respectively. The band diagram under no gate and drain biases is shown below in Figure 18.

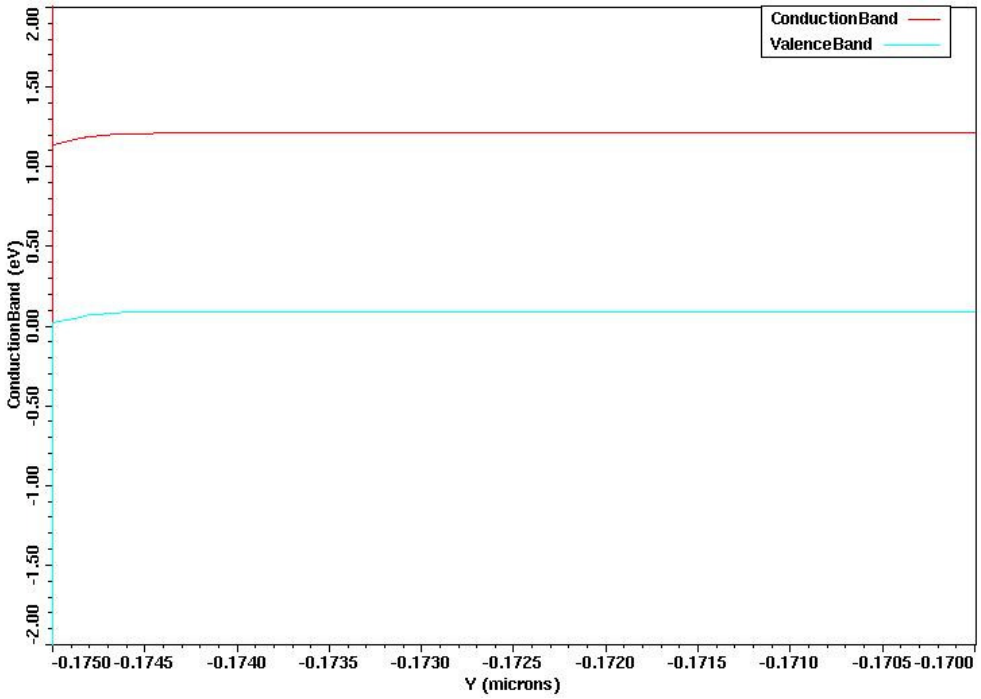


Figure 18. Band diagram of surface-normal tunneling Si-TFET under zero gate and drain bias for case-1

The gate-bias is then increased to 2 V in steps of 0.1 V, and the drain-bias is held constant at 100 mV. The band diagram at gate-bias of 2 V is shown in Figure 19. In this particular device, not enough band-bending has been achieved, leading to lower drive current.

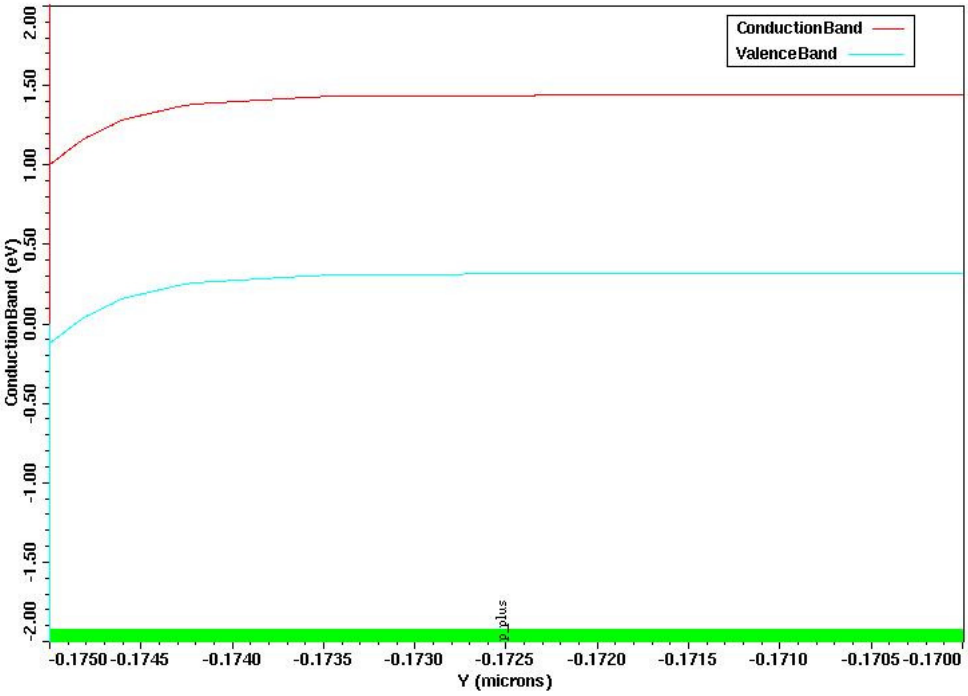


Figure 19. Band diagram of surface-normal TFET at V_G = 2V for case-1

The sub-threshold swing of this device was 706.925 mV/decade. The drain current at V_G=2 V was found to be ~3.84 μA/μm. The I_{DS}-V_G curve is shown in Figure 20.

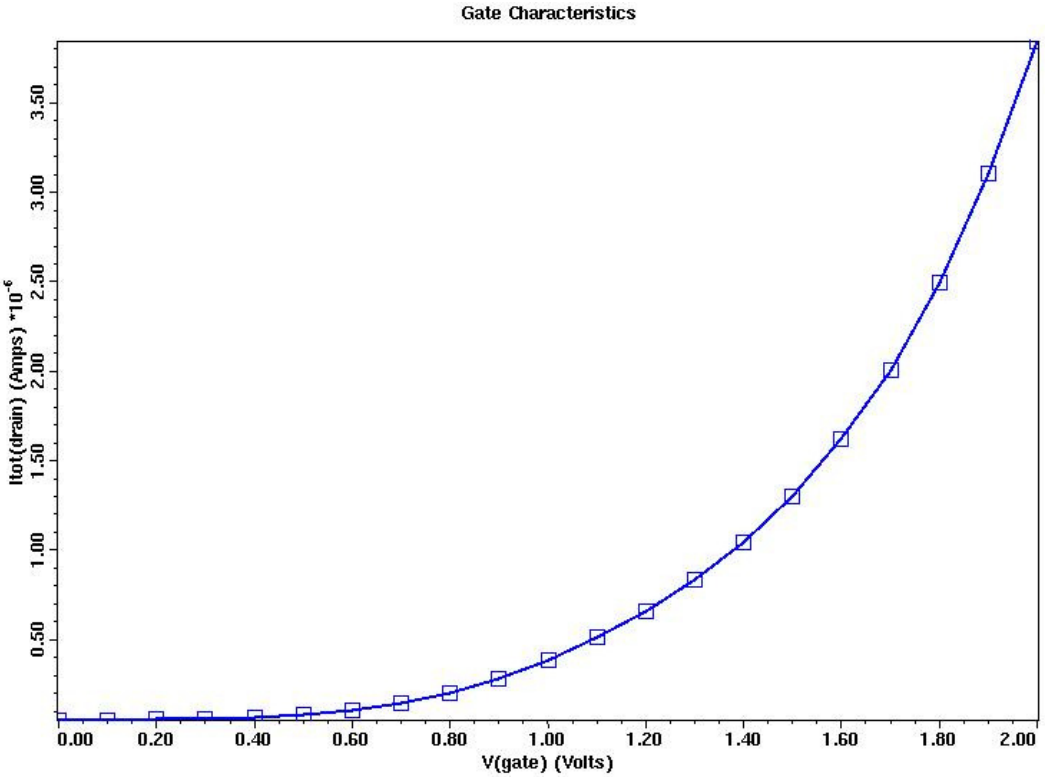


Figure 20. Drain current (I_{DS}) vs. Gate voltage (V_G) graph for case-1

The doping level in the next simulation, dubbed case-2, was reduced to $10^{20}/cm^3$ for p^+ region and $2x10^{20}/cm^3$ for n^+ region. Both the drain current and the sub-threshold swing improved significantly. The sub-threshold swing was found to be 110.392 mV/decade, while the drain current at V_{GS}=2 V was ~5.8 μA/μm. The band diagram at V_{GS}= 0 V, and V_{GS}=2 V with V_{DS}=0.1 V are shown in Figure 21 and Figure 22.

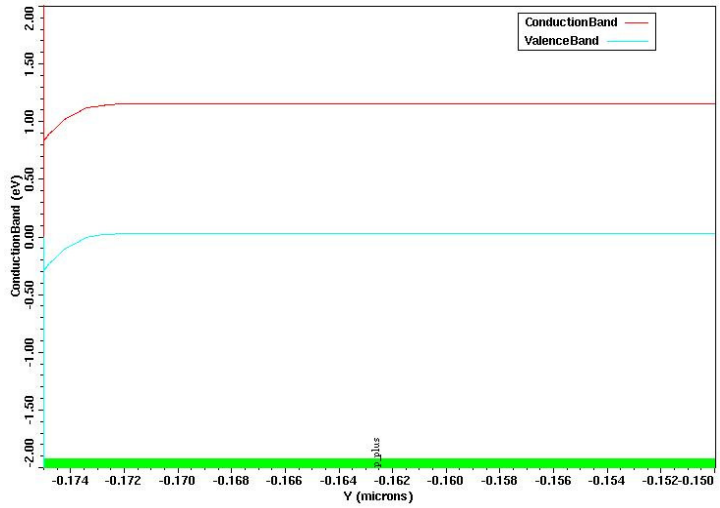


Figure 21. Band diagram without gate-bias for case-2

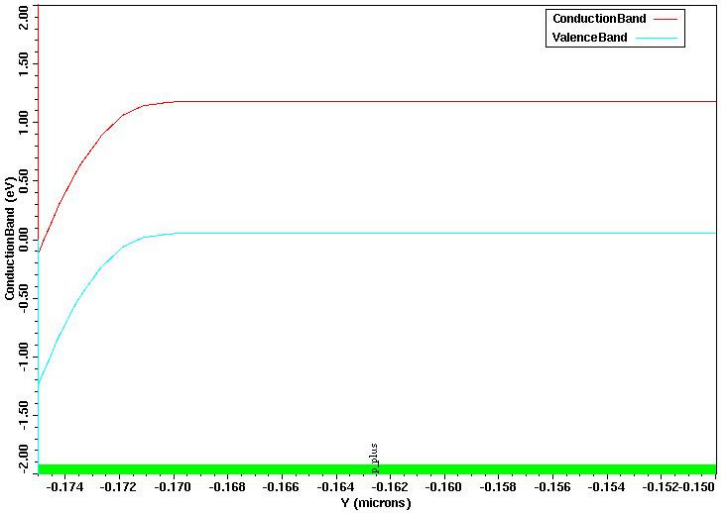


Figure 22. Band diagram with gate-bias for case-2

A comparison of these band diagrams to that in the previous case clearly shows the improvement in band-bending in this case, therefore better sub-

threshold swing, and drain current, resulting in better switching characteristics as compared to case-1. The I_{DS}-V_{GS} curve is shown in Figure 23.

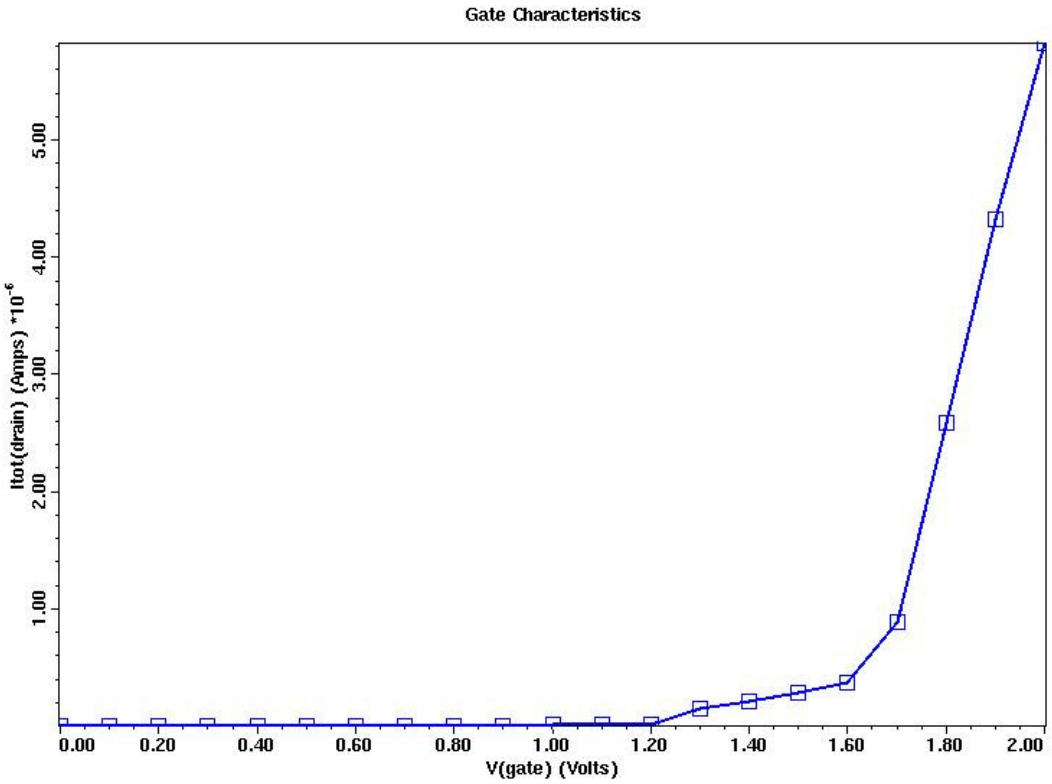


Figure 23. Drain current (I_{DS}) vs. gate voltage (V_{GS}) graph for case-2

These latter results indicated that further improvement in sub-threshold swing and drain current can perhaps be made by proper choice of doping. However, it seems unlikely that this process can lead to any acceptable device voltages or performance.

CHAPTER 6. RESEARCH WORK ON HETERO-BARRIER BAND-TO-BAND TUNNEL FIELD EFFECT TRANSISTORS (HETTFET)

6.1 III-V Semiconductor based Hetero-barrier TFET (HetTFET)

Since band-to-band tunneling depends mainly upon barrier width and band alignment, III-V semiconductor based hetero-structures are actually good candidates as process materials for TFETs [37]. Improved control over the barrier shape can be obtained by strategically placing the hetero-interfaces, and desired band alignment can be achieved by changing the mole fraction of these compound materials. III-V materials also generally offer higher mobility, which further improves conductivity. Either staggered-gap (type-II) or broken-gap (type-III) hetero-structures can, and as noted in the last chapter, have been considered previously, although the latter only with quantum confinement effects that make them effectively staggered-gap. In particular, here we consider for the purposes of simulation, a hetero-structure system composed of GaSb, $In_{0.20}Ga0._{80}As$ and $In_{0.85}Ga_{0.15}As$ system in which the alignment between the first and second, and between the second and third are staggered-gap, and the alignment between the first and third is marginally broken-gap.

6.2 Concept of the Proposed HetTFET

At the heart of the HetTFET design is a marginally broken-gap band alignment between source and channel materials, even after consideration of quantum confinement effects, but with a stepped (or graded) hetero-interface and associated thin tunnel barrier, as per the illustrations of Figure 24, Figure 25 and Figure 26, within the above-noted material system. HetTFETs are intended to achieve high ON/OFF current ratios via a threshold defined by the gate-controlled onset of conduction-to-valence band overlap, and high ON-state transconductances via tunneling through thin barriers defined by crystal growth, rather than relying on gate-controlled barrier narrowing in whole or part for either purpose as with other designs. I will elaborate on the consequences and design requirements as illustrative opportunities arise. The HetTFET concept was first disclosed in 2007 in [27], presented in [40][41][42], and the preliminary n-HetTFET results were published in 2011 [28].

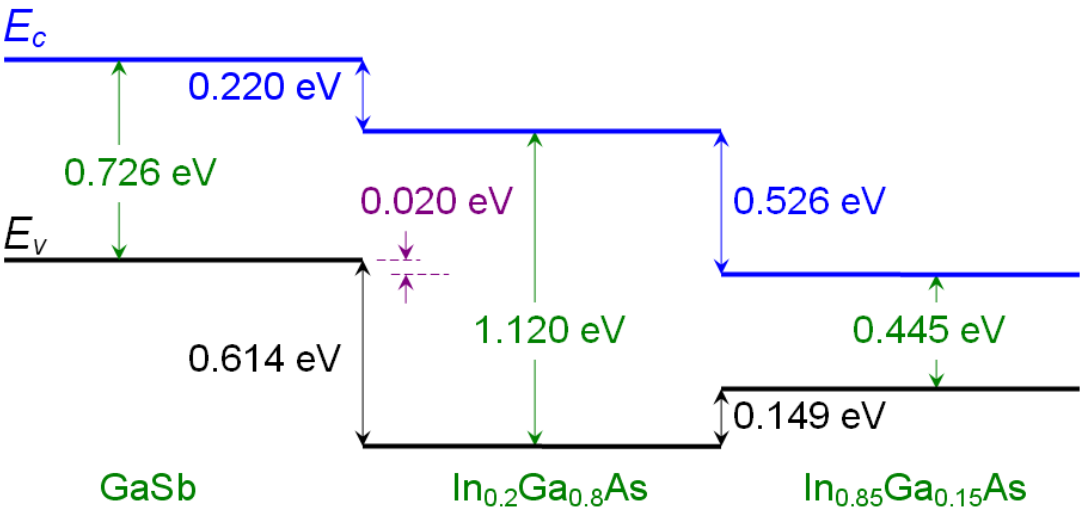


Figure 24. Flat-band stepped mildly type-III broken-gap band profile of Single-gate (SG) and Double-gate (DG) HetTFETs [28]

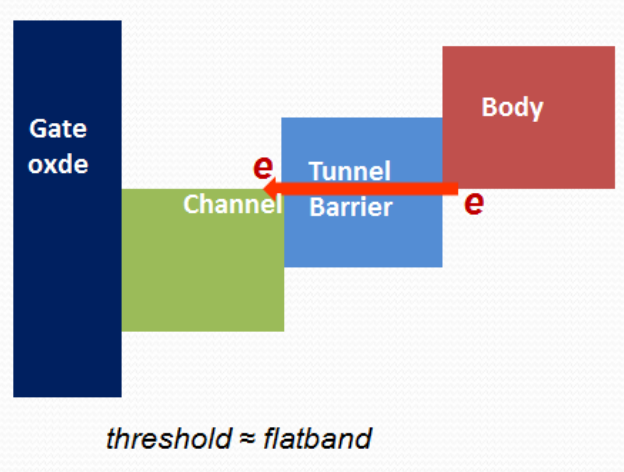


Figure 25. Hypothetical band alignment and tunneling path in a HetTFET

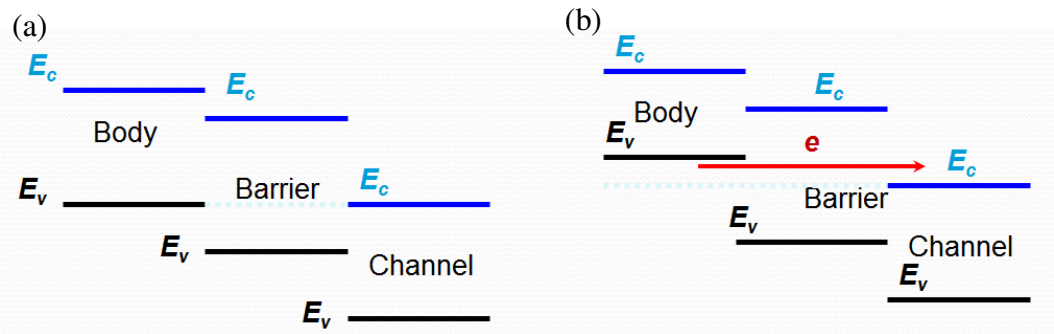


Figure 26. Hypothetical band alignment of a HetTFET (a) at threshold and (b) when fully on

6.3 Structure of the Proposed HetTFETs

In addition to n-channel and p-channel devices, both channel-normal and channel-parallel tunneling geometries are considered for each, as illustrated in Figure 27, Figure 28, Figure 29, and Figure 30 via the white arrows indicating the nominal direction of electron tunnel. For specificity in subsequent simulations, the channel-normal-tunneling devices have been depicted as single-gate (SG) devices, and the channel-parallel-tunneling devices, as vertical channel double-gate (DG) devices—in a vertical channel FinFET-like geometry. However, other geometries can be imagined within the confines of the overall concept. In terms of transport, channel-normal tunneling provides greater tunneling area, while cannel-parallel tunneling perhaps provides better gate control. The doping of the channel and substrate regions adjacent to the tunnel barrier must be adjusted to optimize gating and the tunneling process. Beyond that, the source and drain

regions immediately beneath the contacts should be optimized to serve as charge reservoirs.

Figure 27, Figure 28, Figure 29, and Figure 30 also show the dimensions and material composition of the simulated concept-representative single-gate and double-gate HetTFETs. The transistor has a channel length of 30 nm for the single-gate (SG) HetTFETs (Figure 27 and Figure 28) and 10 nm for the double-gate (DG) HetTFETs (Figure 29 and Figure 30).

For the SG-n-HetTFET in Figure 27, the layer closest to the gate is the channel layer and is made from $In_{0.85}Ga_{0.15}As$ (undoped). The 2 nm thick layer below the channel layer is the barrier layer, made from $In_{0.20}Ga_{0.80}As$ (undoped). The layer below and to the left of the barrier layer is the source and is made of GaSb, uniformly doped p^+ ($10^{18}/cm^3$). The layer to the right of the barrier layer is the drain and is made of $In_{0.85}Ga_{0.15}As$, uniformly doped n^+ ($10^{18}/cm^3$).

For the SG-p-HetTFET in Figure 28, the channel layer is made from GaSb, uniformly doped p^+ ($10^{18}/cm^3$). The barrier layer is made from $In_{0.20}Ga_{0.80}As$ (undoped) as was the case in SG-n-HetTFET. The layer below and to the left side of the barrier layer is the source and is made of $In_{0.85}Ga_{0.15}As$, uniformly doped n^+ ($10^{17}/cm^3$). The layer to the right side of the barrier layer is the drain and is made of GaSb, uniformly doped p^+ ($10^{18}/cm^3$).

For the DG-n-HetTFET in Figure 29, the layer above the channel layer is the drain and is made from $In_{0.85}Ga_{0.15}As$, uniformly doped n^+ ($10^{18}/cm^3$). The

channel layer itself is made from undoped $In_{0.85}Ga_{0.15}As$. The layer, immediately below the channel layer is the barrier layer and is made from $In_{0.20}Ga_{0.80}As$ (undoped). The layer below the barrier is the source, made from GaSb, and uniformly doped p^+ ($10^{18}/cm^3$).

In the case of the DG-p-HetTFET in Figure 30, the layer above the channel layer is the drain, and both channel and drain are made from GaSb, uniformly doped p^+ ($10^{18}/cm^3$). The barrier layer is made from $In_{0.20}Ga_{0.80}As$ (undoped). The layer below the barrier is the source - made from $In_{0.85}Ga_{0.15}As$, and uniformly doped n^+ ($10^{17}/cm^3$).

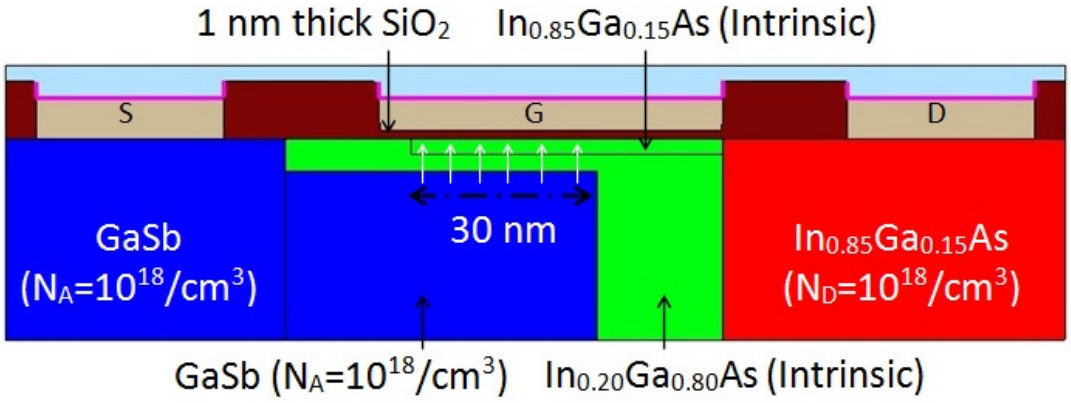


Figure 27. Single-gate (SG)-n-HetTFET

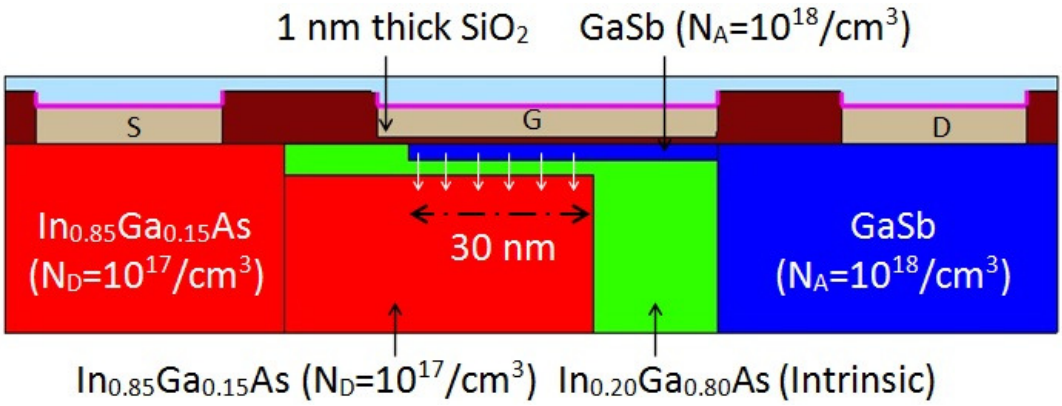


Figure 28. Single-gate (SG)-p-HetTFET

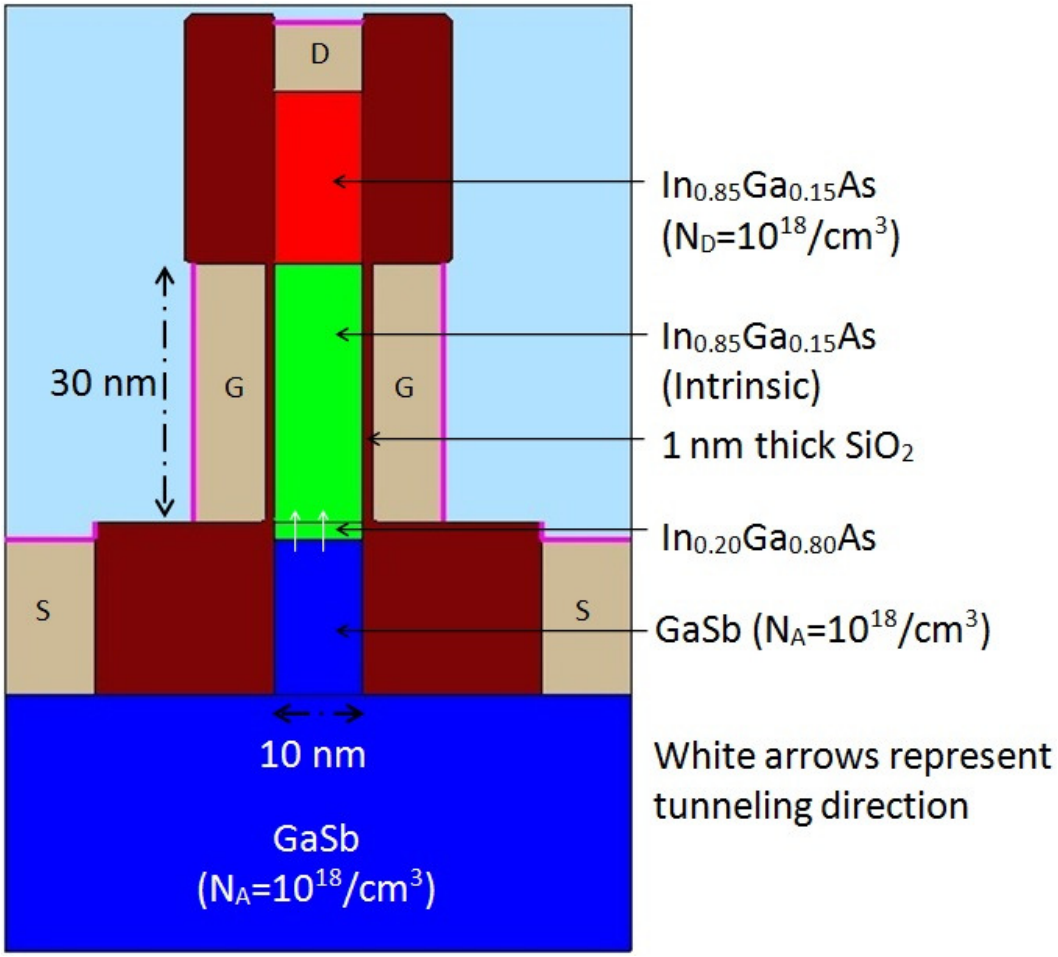


Figure 29. Double-gate (DG)-n-HetTFET

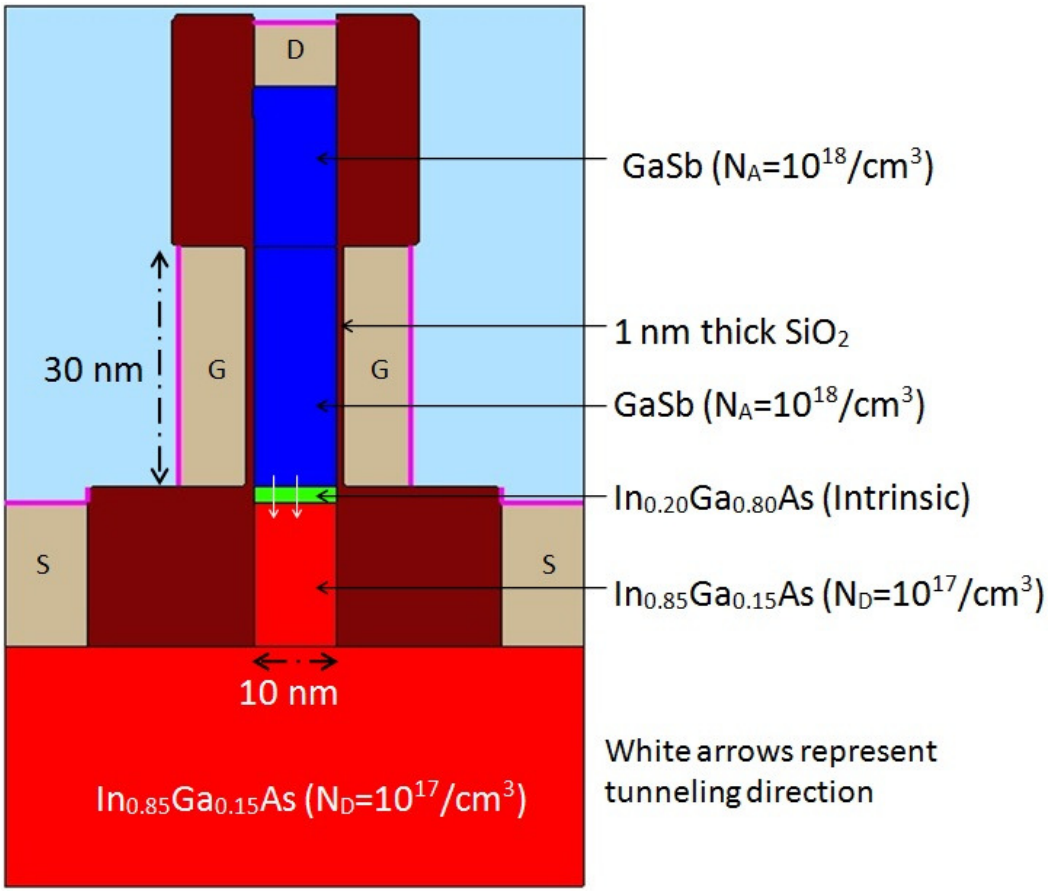


Figure 30. Double-gate (DG)-p-HetTFET

6.4 Device Definition

Many aspects of these devices were held constant as a control in these simulations. Our intent was not to fully optimize the device design, but rather to isolate and illustrate essential physics. We employed the GaSb-$In_{0.20}Ga_{0.80}As$-$In_{0.85}Ga_{0.15}As$ material system of Figure 24 for all HetTFETs simulated in this work; only material location and doping varied among the n-channel and p-

channel devices, and channel-normal and channel-parallel geometries. Quantum confinement effects were not considered, so that all devices also retained the same marginal broken-gap alignment of Figure 24. In reality, (sub) band-edge shifts associated with quantum confinement near threshold would have to be compensated for by increases in the band-offset across the broken-gap. The electron and hole effective masses, relative to free electron rest mass (m_0), were specified to be 0.041 and 0.4 for GaSb; 0.029 and 0.43 for $In_{0.85}Ga_{0.15}As$; and 0.055 and 0.49 for $In_{0.20}Ga_{0.80}As$; electron affinity and band-gap for GaSb layer were specified to be 4.06 eV and 0.726 eV respectively, all in consultation with [29]. Default values have been used for all other material parameters. The gate dielectrics of all devices were assumed to have a 1 nm effective oxide thickness, actually modeled as SiO_2 for specificity. In addition, for all simulations, the mesh near the tunnel barrier and/or in the channel region was specified to be 0.25 nm x 0.25 nm, and up to 4 nm x 4 nm outside these regions, as illustrated in Figure 31.

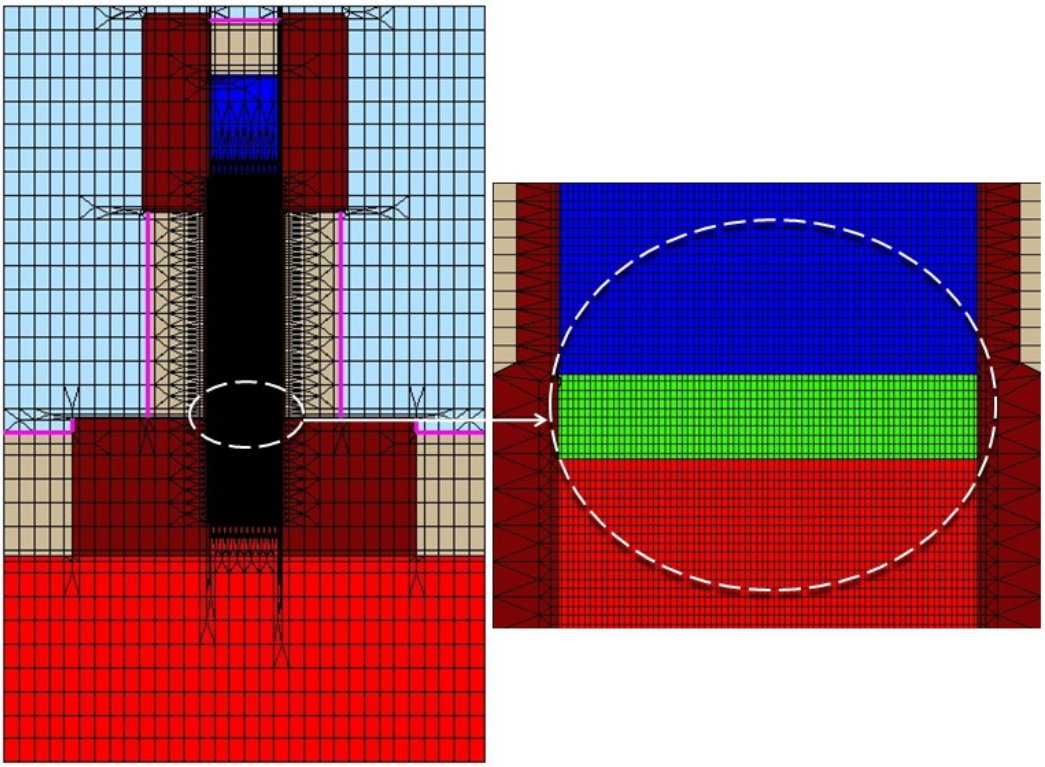


Figure 31. Simulation mesh for DG-p-HetTFET with 2 nm tunnel barrier, with 0.25 nm x 0.25 nm mesh for the channel, barrier, and nearby regions, and up to 4 nm x 4 nm mesh for regions further away

The quasi-2D simulated devices structures including critical device dimensions and ohmic source (S), drain (D) and gate (G) contacts are shown in Figure 27, Figure 28, Figure 29, and Figure 30. Also shown in these figures are the generally conservative employed donor and acceptor doping concentrations N_D and N_A in $In_{0.85}Ga_{0.15}As$ and GaSb, respectively. The $In_{0.20}Ga_{0.80}As$ tunnel barrier was taken as intrinsic in all cases.

We note that, as shown, the channel of the n-channel devices was left un-doped, while for the channel acceptor doping for the p-channel devices was set to $N_A = 10^{18}/cm^3$. The latter channel doping was used to increase the overall channel concentration and, thus, conductivity for the p-channel devices, given the limited hole mobility in GaSb of 1,000 $cm^2/V/s$. Note that there is no need to entirely deplete the channel region in the OFF-state as current is controlled by band alignment rather than just carrier concentration. In particular, even in parallel-tunneling thick-fin double gate or single gate geometries, this choice for N_A in combination with $N_D = 10^{17}/cm^3$ on the source side of the tunnel barrier would remain sufficient to prevent conduction to valence band overlap across the barrier away from the channel interface, so that only the near surface region could be switched ON. Because N_A remains small compared to the effective density of states, the gate would still effectively control the near-channel-surface charge layer. The exceptional electron mobility in the $In_{0.85}Ga_{0.15}As$ approaching 20,000 $cm^2/V/s$ eliminated the need for any channel doping in the n-channel devices.

Beyond what is explicitly indicated in Figure 27 and Figure 28, the tunnel barrier thickness in the horizontal direction in the normal-tunneling SG-HetTFETs is 20 nm in order to localize all tunneling to the intended vertical tunneling region (white arrows). The Vertical tunnel barrier thickness was varied between 1 and 3 nm for all devices. As with all device simulations in this work, the temperature T was taken to be 300 K.

The transistor nodes were contacted in accordance CMOS-inverter terminology. In a CMOS-inverter, the pMOS-source is connected to V_{DD}, pMOS and nMOS-drains are connected to the load, and nMOS-source is typically grounded.

6.5 Simulation Results

Figure 32, Figure 33, Figure 34, and Figure 35 provide illustrative examples of electron and hole 2D current density distributions, and tunneling-mediated electron and hole generation rate distributions for one particular ON-state biasing condition for the DG-n-HetTFET. Corresponding illustrations for DG-p-HetTFET are provided in Figure 36, Figure 37, Figure 38, and Figure 39. The non-local band-to-band tunneling through the tunnel barrier and the overall bi-polar nature of the current flow are evident. Also note that current flow and tunneling are fairly evenly distributed across the channel width, at least in this thin-fin DG structure, even without consideration of quantum effects; the device operates in a near-flat-band condition.

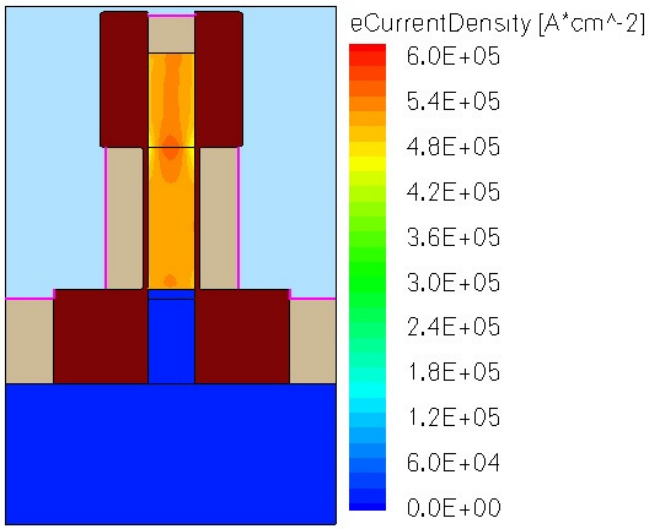


Figure 32. Electron (drift-diffusion) current in DG-n-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = 75 mV

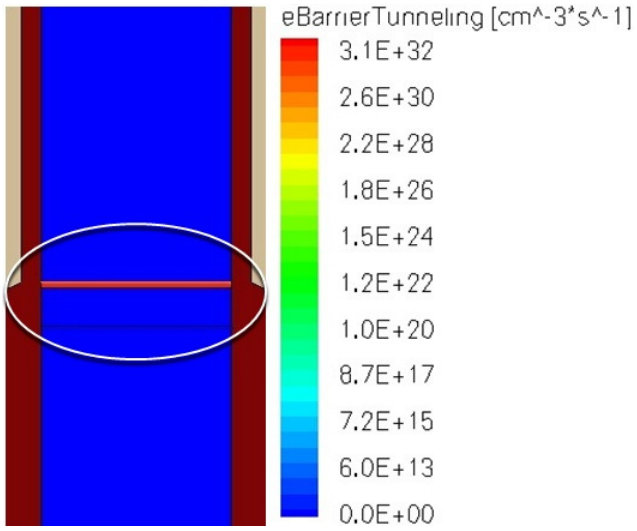


Figure 33. Electron tunneling-mediated generation rate in DG-n-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = 75 mV

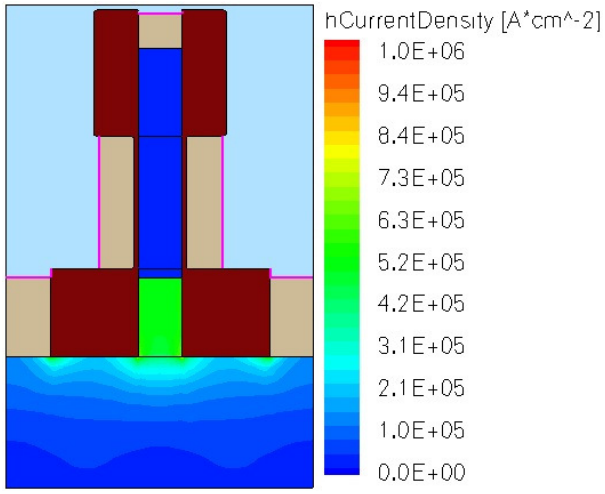


Figure 34. Hole current in DG-n-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = 75 mV

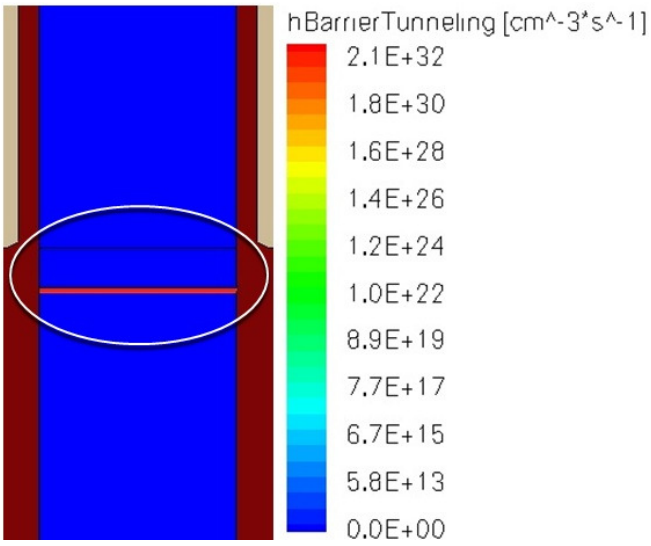


Figure 35. Hole tunneling-mediated generation rate in DG-n-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = 75 mV

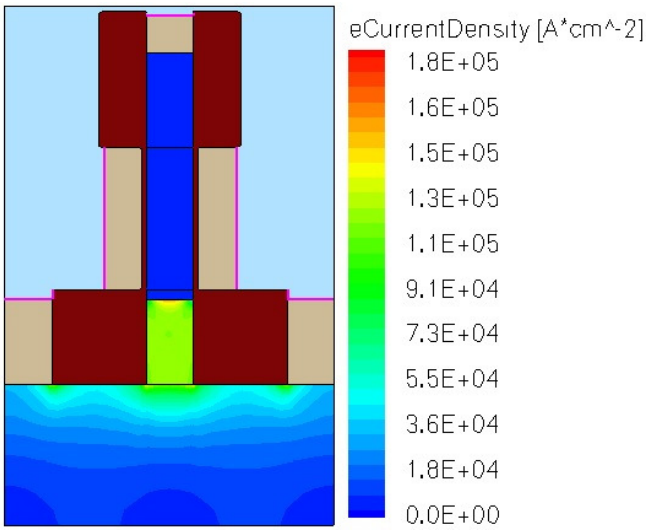


Figure 36. Electron (drift-diffusion) current in DG-p-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = -75 mV

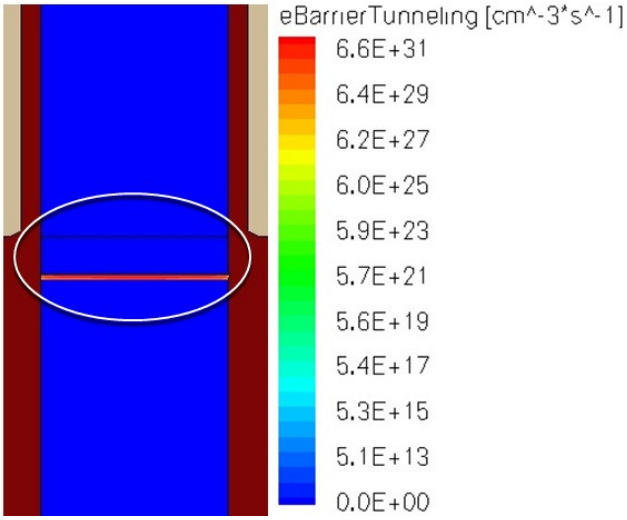


Figure 37. Electron tunneling-mediated generation rate in DG-p-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = -75 mV

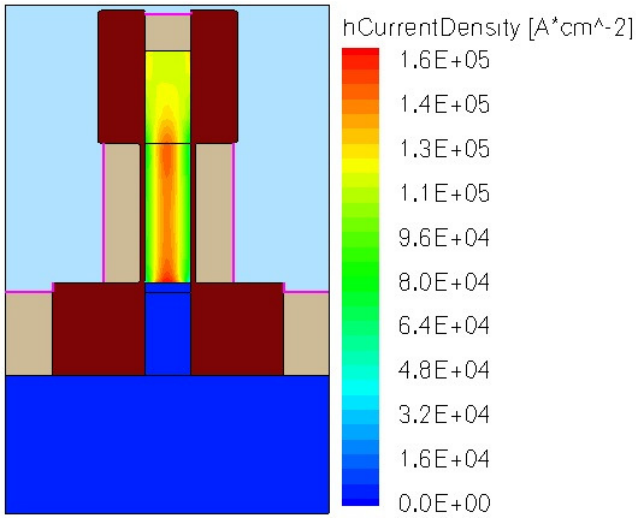


Figure 38. Hole current in DG-p-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = -75 mV

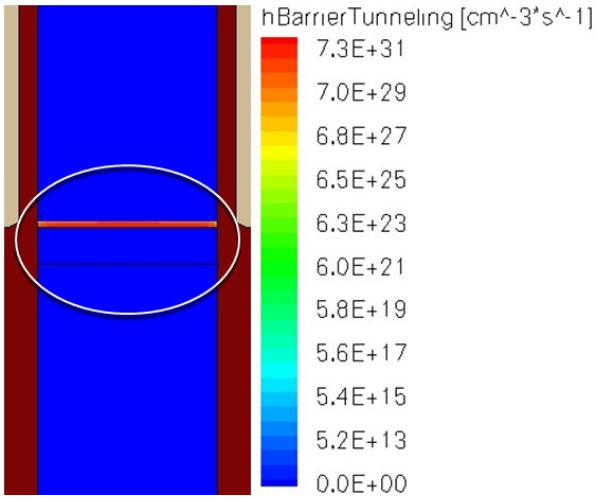


Figure 39. Hole tunneling-mediated generation rate in DG-p-HetTFET with a 2 nm tunnel barrier thickness and $V_D - V_S = V_G - V_{Th}$ = -75 mV

Figure 40, Figure 41, and Figure 42 show the band alignment along the channel surface near the tunnel barrier 25 mV below, at, and 75 mV above threshold in the same DG-n-HetTFET. Majority carrier Fermi levels E_F are shown which correspond to the source (right-hand-side) and drain (left-hand-side) contact voltages below and at threshold. Given the marginally broken-gap band alignment, the carrier concentrations to either side of the channel barrier are intrinsically slightly accumulated at threshold, at least relative to flat-band. Above threshold, ~10 mV of the total of 75 mV source-to-drain voltage is dropped to either side of the tunnel barrier, consistent with resistive losses in the source, channel and drain regions.

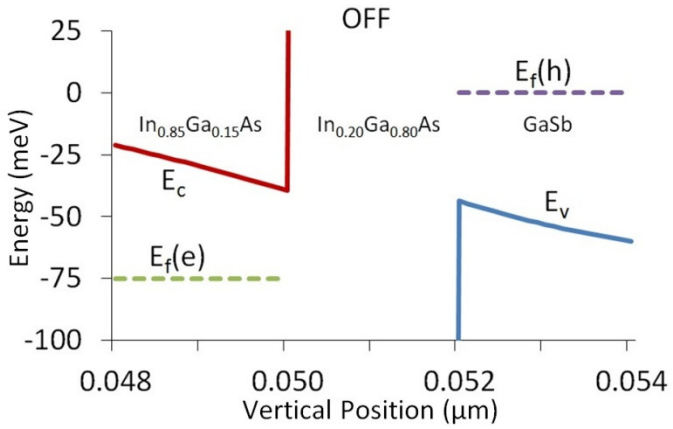


Figure 40. DG-n-HetTFET band alignment along the channel surface near the tunnel barrier with the gated-channel on the left and source on the right, below threshold (OFF, $V_G - V_{Th} = -25$ mV)

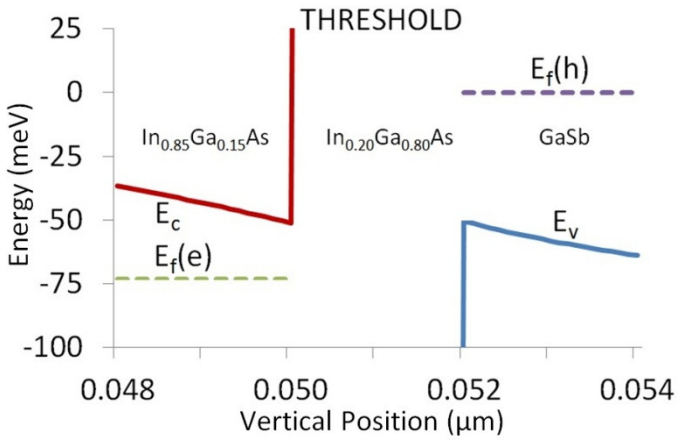


Figure 41. DG-n-HetTFET band alignment along the channel surface near the tunnel barrier with the gated-channel on the left and source on the right, at threshold

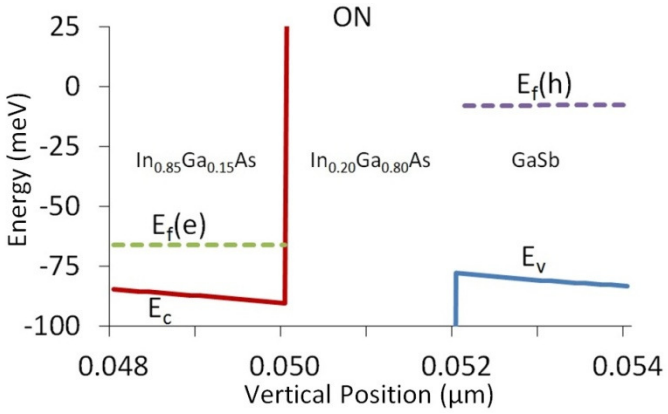


Figure 42. DG-n-HetTFET band alignment along the channel surface near the tunnel barrier with the gated-channel on the left and source on the right, above threshold (ON, $V_G - V_{Th}$ = 75 mV)

Note that channel becomes degenerate above threshold in this case, which may somewhat negatively impact the net tunneling current. The electron tunneling flux from source to channel (with electrical current in the opposite direction) varies linearly with the difference in the electron occupation probabilities from the source-side to channel-side of the barrier. Therefore, splitting the Fermi levels across the barrier equally about the band-overlap region would be optimal in terms of tunneling alone. Such splitting could be arranged by varying N_A on the source side near the barrier, which essentially sets the flat-band value of $E_F - E_v$ there. The voltage drop across the barrier then sets the value of $E_F - E_v$ on the channel side. However, such changes will also affect the resistive losses on either side of the barrier. In this work, the doping concentrations have not been fully optimized with respect to these considerations; they are merely reasonably acceptable.

Figure 43, Figure 44, and Figure 45 show the corresponding band alignment results for the DG-p-HetTFET. Note that above threshold, the resistive losses are larger, accounting for over half of the overall voltage drop between source and drain, with almost all of that voltage dropped within the lower conductivity p-type GaSb on the channel-side of the tunnel barrier.

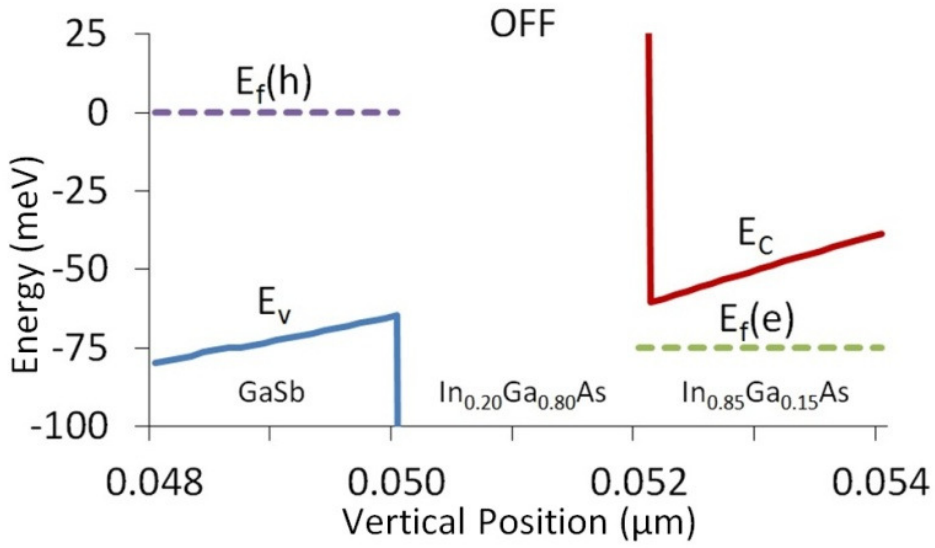


Figure 43. DG-p-HetTFET band alignment along the channel surface near the tunnel barrier with the gated-channel on the left and source on the right, below threshold (OFF, $V_G - V_{Th}$ = 25 mV)

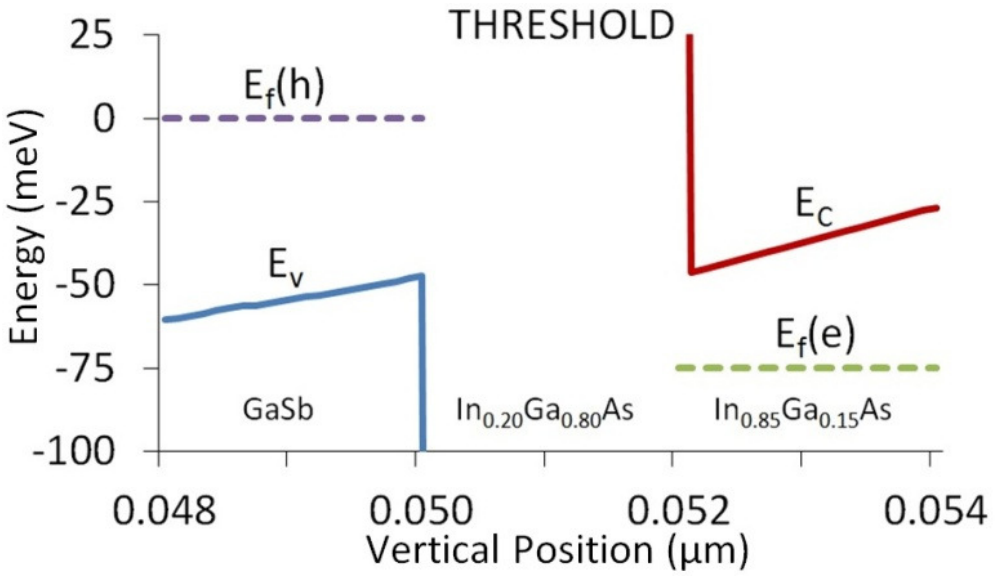


Figure 44. DG-p-HetTFET band alignment along the channel surface near the tunnel barrier with the gated-channel on the left and source on the right, at threshold

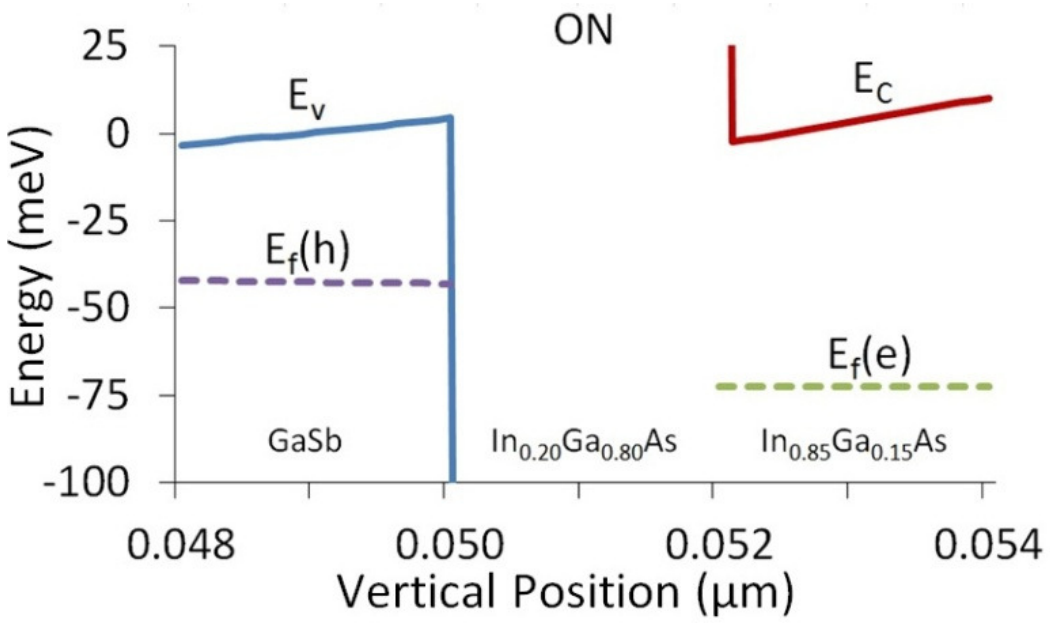


Figure 45. DG-p-HetTFET band alignment along the channel surface near the tunnel barrier with the gated-channel on the left and source on the right, above threshold (ON, $V_G - V_{Th} = -75$ mV)

For each device, many such simulations have been performed to obtain and understand their $|I_{DS}|$-V_G and I_{DS}-$|V_{DS}|$ characteristics. For initial $|I_{DS}|$-V_G simulations, the source V_S and drain V_D voltages for the n-channel and p-channel devices, were biased as if in the OFF-state or just switched to the ON-state within a CMOS-like inverter, although with a supply voltage V_{DD} of only 75 mV. For the n-channel devices, the source was grounded and V_D was set to V_{DD}; for the p-channel devices, V_S was set to V_{DD} and the drain was grounded. The gate voltages were then swept from 25 mV below threshold to 75 mV above threshold. Figure 46, Figure 47, Figure 48, and Figure 49 show the resulting I_{DS} vs. V_G graphs for

SG and DG-n-HetTFETs, and I_{SD} vs. V_G graphs for SG and DG-p-HetTFETs with 1, 2 and 3 nm barrier widths. Linear and logarithmic scales are provided in each case to exhibit above and below threshold behaviors, respectively.

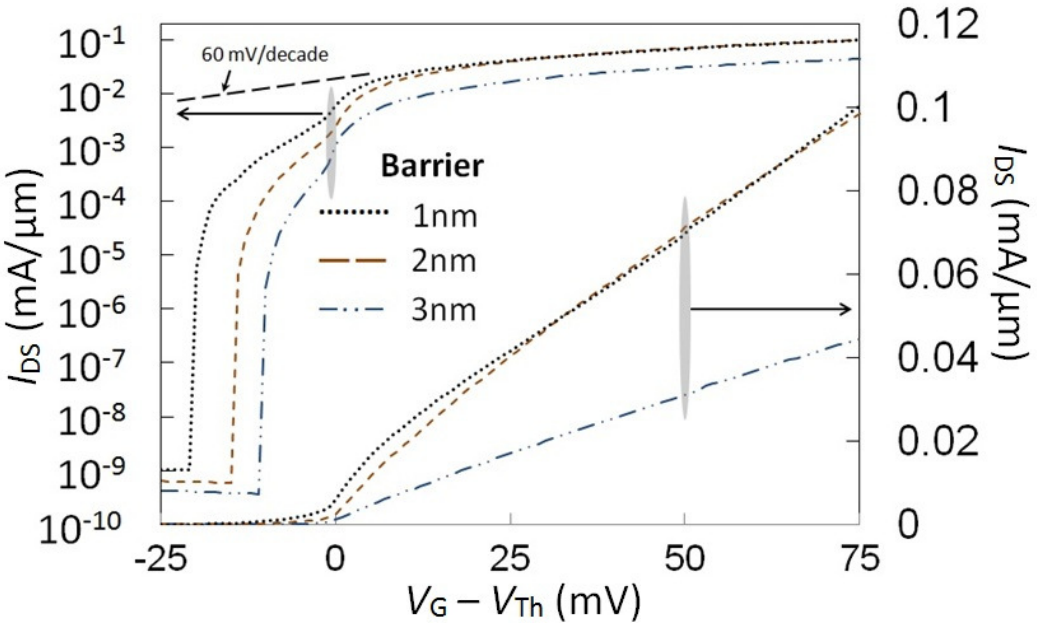


Figure 46. I_{DS}-V_G characteristics shown on both linear and logarithmic scales for simulated SG-n-HetTFET, with 1, 2, and 3 nm barrier widths

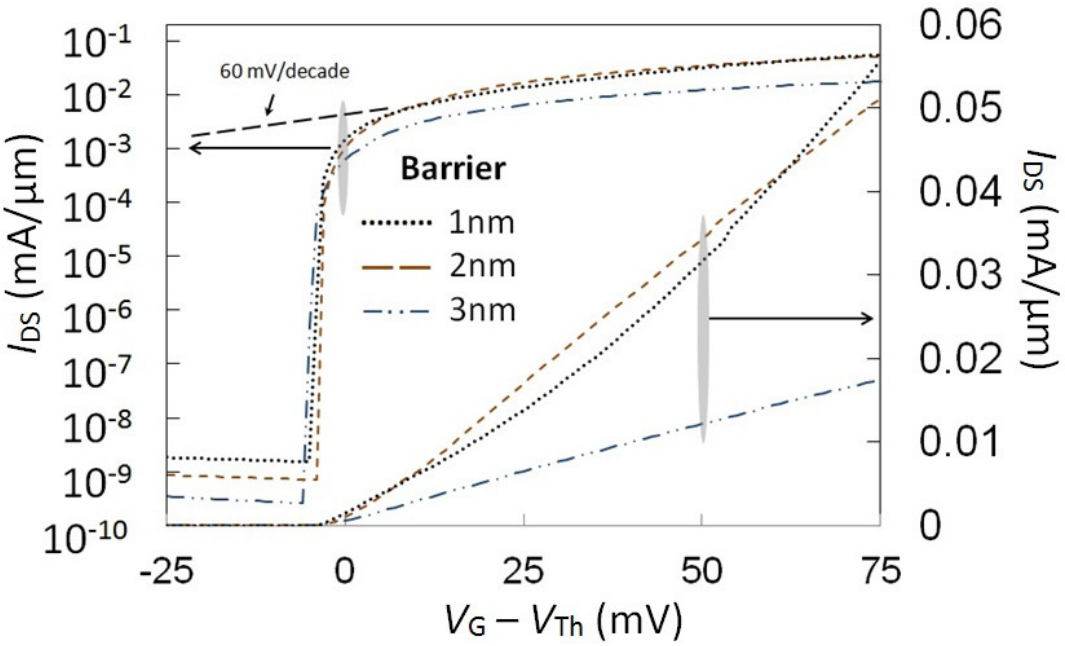


Figure 47. I_{DS}-V_G characteristics shown on both linear and logarithmic scales for simulated DG-n-HetTFET, with 1, 2, and 3 nm barrier widths

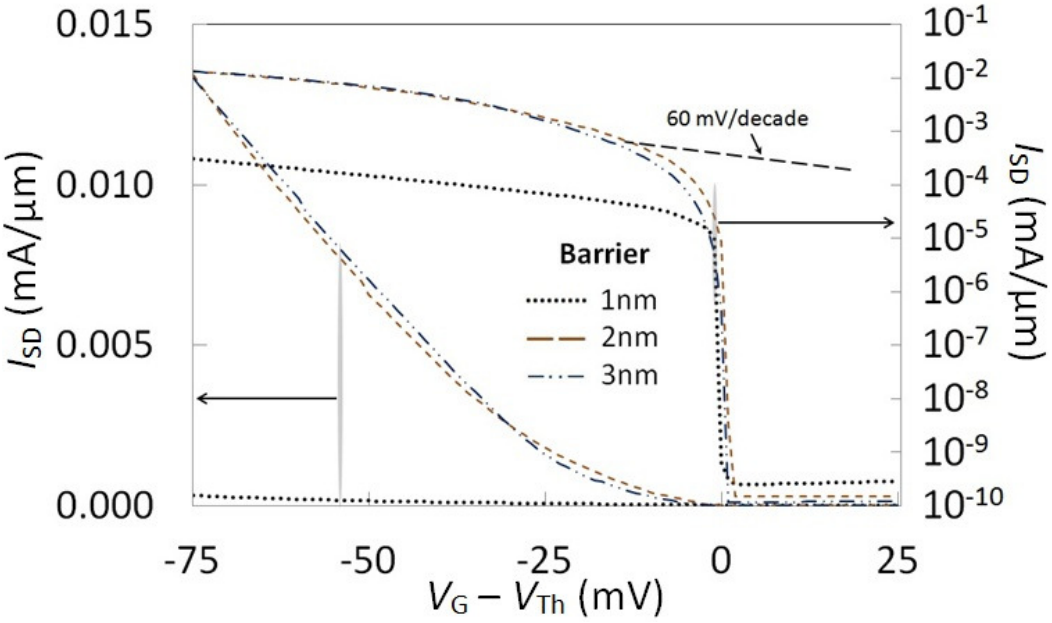


Figure 48. I_{SD}-V_G characteristics shown on both linear and logarithmic scales for simulated SG-p-HetTFET, with 1, 2, and 3 nm barrier widths

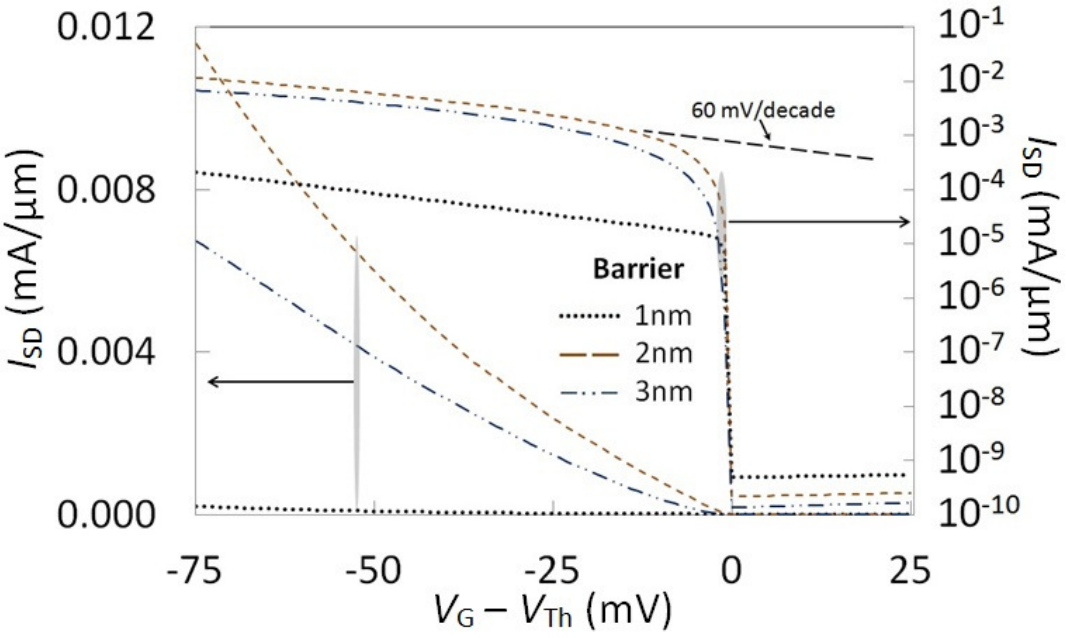


Figure 49. I_{SD}-V_G characteristics shown on both linear and logarithmic scales for simulated DG-p-HetTFET, with 1, 2, and 3 nm barrier widths

For all device prototypes, a ~2 nm or perhaps between 1 and 2 nm tunnel barrier thickness would prove roughly optimal. For reference, the tunneling would vanish for very thick barriers, while there would be no control over band overlap and the device would not turn off for a true broken-gap alignment (after quantum confinement) absent the barrier.

All devices show very abrupt switching in the critical subthreshold regime. The 60 mV/decade theoretical minimum subthreshold slope at the 300K simulation temperature is shown for reference in each case. In the worst case, the SG n-channel HetTFET device shows a two-tier switching characteristic due to achieving threshold at the source-end of the channel slightly before achieving it

elsewhere along the channel. Still, only ~15 mV in the 2 nm barrier device is required to achieve over a six order of magnitude change in the current until the Shockley-Reed-Hall thermal-generation current flow is reached. All other devices exhibit a similar change in current over perhaps under 5 mV. For these devices, based on the results alone, one could imagine operating, in particular, the DG devices at a few 10s of mV supply voltages V_{DD}. A more realistic way of describing this behavior is perhaps to say HetTFET subthreshold behavior would likely be entirely dependent on parasitic leakage paths—to be commented on in the next section.

In the ON-state for the 2 nm barrier devices, transconductances g_m for the SG-n-HetTFET, DG-n-HetTFET, SG-p-HetFET, and DG-p-HetTFET, were 1.2 mA/μm/V, 0.7 mA/μm/V, 0.27 mA/μm/V, and 0.17 mA/μm/V, respectively, at least approaching conventional short-channel MOSFET behavior qualitatively and quantitatively [30]. The n-channel devices exhibit higher conductance than p-channel devices as for MOSFETs, if perhaps a bit more so here than Si-based MOSFETs. A greater difference in electron and hole mobilities in these HetTFETS is a likely partial culprit for this. The SG devices exhibit larger g_m consistent with the larger tunneling areas. However, with scaling below the 30 nm channel lengths considered here, the tunneling area would scale with the gate length for the SG devices. For the DG devices, the gate length, if along with fin

thickness, could likely be reduced without adversely affecting g_m, and perhaps even improving it as for short-channel MOSFETs.

Finally, Figure 50 shows the I_{DS} vs. $|V_D - V_S|$ for a 75 mV gate overdrive voltage $|V_G - V_{Th}|$. As can be seen, saturation is more difficult to achieve at low voltages. For $|V_D - V_S|$ of only a few $k_B T$, back injection of charge carriers from the source would prevent saturation. The lack of saturation beyond that, however suggest perhaps some effect of the drain voltage on the channel tunneling barrier and/or channel potential profile, the TFET equivalent of drain-induced-barrier lowering. Of more concern than the lack of I_{DS} current saturation would be variation in the gate V_{Th} with $|V_D - V_S|$. However, as shown in Figure 51 and Figure 52 for the n-channel and p-channel DG HetFETs, respectively, the effect of $|V_D - V_S|$ on V_{Th} is limited.

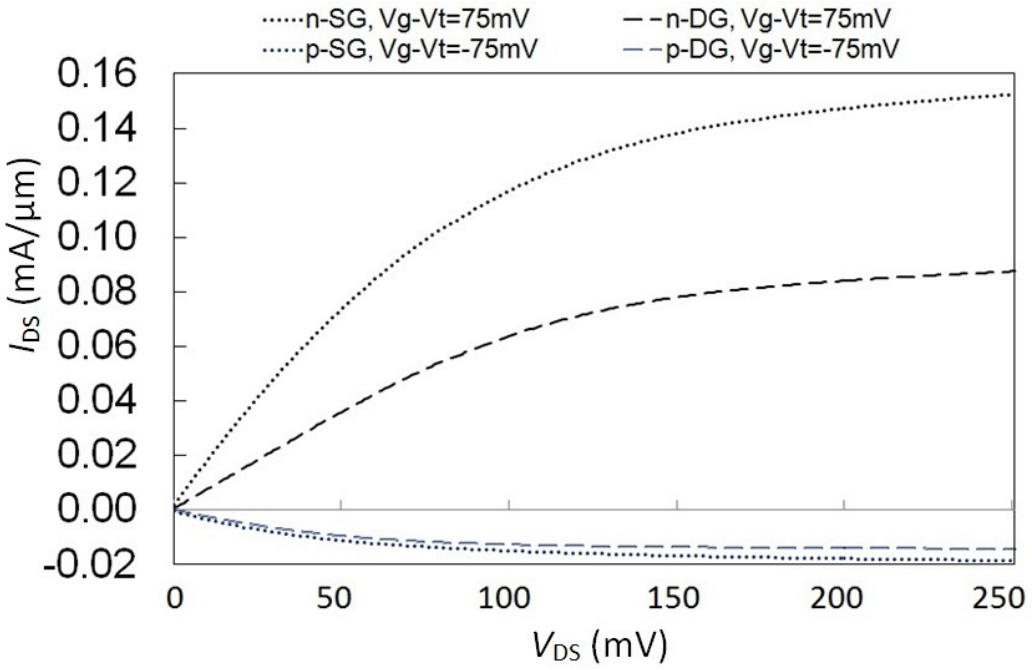


Figure 50. SG and DG n and p-HetTFET I_{DS}-$|V_{DS}|$ characteristics with $|V_G - V_{Th}|$ = 75 mV

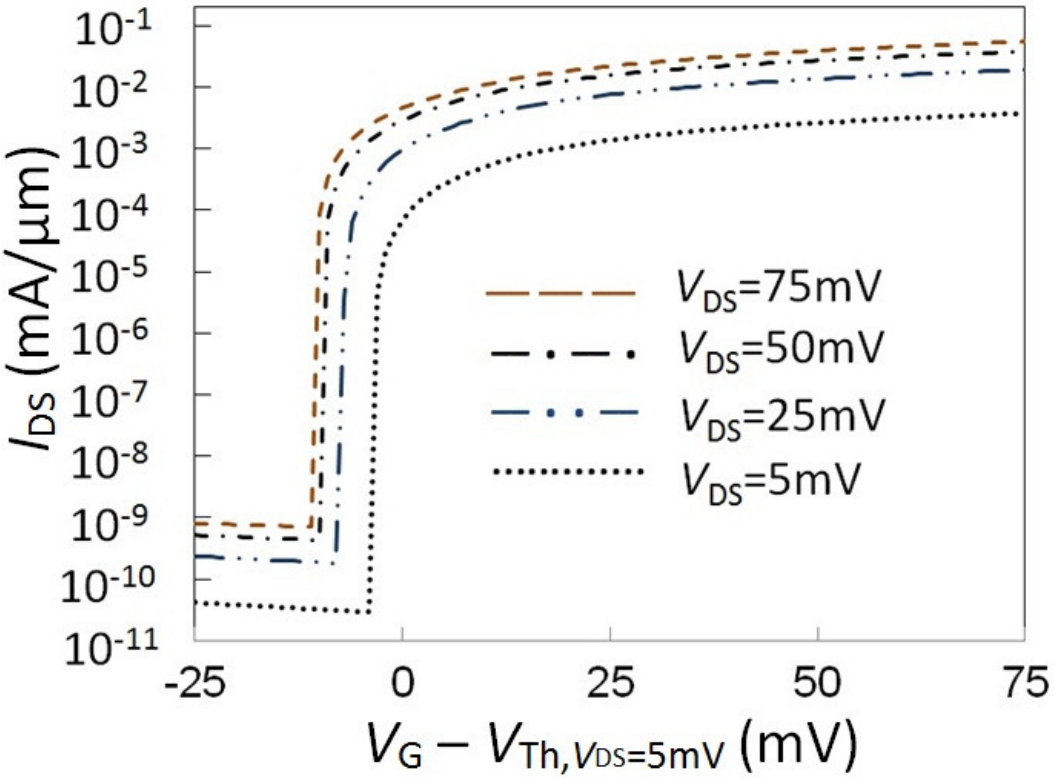


Figure 51. $|I_{DS}|$-V_G characteristics for $|V_{DS}|$ values of 5 mV, 25 mV, 50 mV, and 75 mV, for DG n-HetTFETs with common V_G reference, the V_{Th} for the $|V_{DS}|$ = 5 mV.

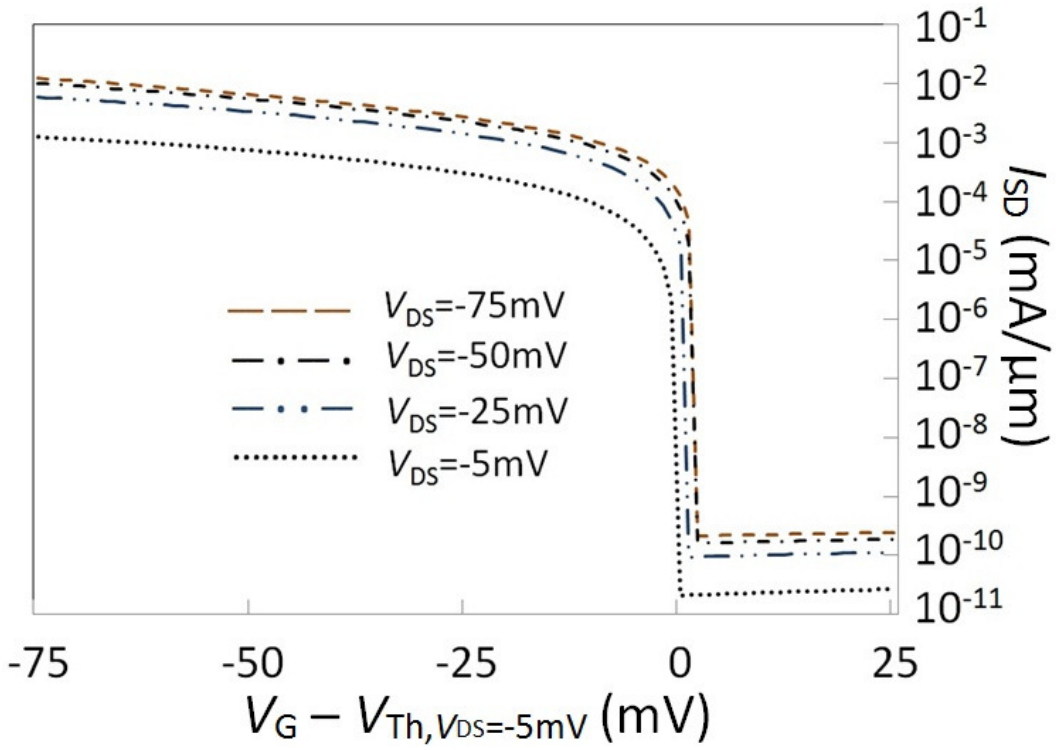


Figure 52. $|I_{DS}|$-V_G characteristics for $|V_{DS}|$ values of 5 mV, 25 mV, 50 mV, and 75 mV, for DG p-HetTFETs with common V_G reference, the V_{Th} for the $|V_{DS}|$ = 5 mV.

6.6 Regarding Parasitic Leakage Paths

We recognize that there are limitations to the modeling, particularly regarding the consideration of some parasitic leakage paths. For example, the simulations do not account for parasitic phonon-assisted and trap-assisted tunneling that could broaden the switching transition. However, the HetTFET has also been designed with these in mind. Inelastic tunneling would require phonon absorption rather than emission. Low-order phonon-assisted tunneling cannot

shorten the tunneling path as for other designs. Similarly, the stepped broken-gap band alignment provides a relatively large band offset at each hetero-interface to minimize local thermal generation along the interfaces—particularly important if there are interface band gap states—as compared to near-broken-gap single-hetero-interface TFET designs. Moreover, to the extent band tailing exists and/or tunneling to or from dopant states is possible, abrupt switching associated with the onset of band overlap will be broadened. The latter is good reason to minimize doping in the immediate vicinity of the tunnel barrier. However, the doping concentrations we used in simulation are already reasonably conservative. Lacking reliable simulations of (or, of course, experimental results for) these parasitic leakage mechanisms, their importance and, thus, that of these latter design advantages is admittedly unclear. Of course, our hope would be that these leakage mechanisms and, thus, these latter design advantages would be irrelevant.

CHAPTER 7. JUNCTION FET-TYPE HETTFET

7.1 Junction HetTFET

I have briefly considered the idea of Junction FET (JFET)-type HetTFET due to III-V semiconductor materials' susceptibility to interface states and associated leakage currents, as discussed in the preceding chapter (Chapter 6, Section 6). This can reduce subthreshold slope, enhance thermal generation and higher OFF-state current. In a JFET-type HetTFET device, the primary ON/OFF switching mechanism would be that of gate controlled band alignment, with perhaps the added incidental benefit of pinching of the depletion layer formed in the channel by application of gate bias. However, accurately controlling the depletion width to achieve steep subthreshold slope, high I_{ON}/I_{OFF} ratio, and meaningful drive current is a challenge by itself, and in the following work, I explore through simulation whether these goals are readily achievable in a JFET-type HetTFET geometry.

7.2 Junction HetTFET Simulation and Results

Several JFET-type HetTFET devices were considered. Figure 53 and Figure 54 show the first JFET-type DG-n-HetTFET. It has a widened 15 nm channel width compared to the HetTFET described in Chapter 6. The layer above the channel layer is the drain, and both channel and drain were made from

$In_{0.85}Ga_{0.15}As$, uniformly doped n^+ ($10^{19}/cm^3$). The layer, immediately below the channel layer is the barrier layer and is made from undoped $In_{0.20}Ga_{0.80}As$. The layer below the barrier is the source—made from GaSb, and uniformly doped p^+ ($10^{19}/cm^3$).

For simulation, we again employed Synopsys TCAD Taurus and Sentaurus Device simulators [5][7]. The device structure and mesh were first prepared using Taurus Device as was done in the case of HetTFETs in Chapter 6. The mesh in the channel and barrier region is 0.5 nm x 0.5 nm for all cases, and is 2 nm x 2 nm away from the channel and the barrier region. Synopsys Datex software was utilized to port the structure and the mesh to Sentaurus Device simulation environment [6]. The device simulation was then performed using Sentaurus Device simulator [7]. For simulation, Sentaurus non-local band-to-band tunneling model with Franz two-band model was utilized again, and the tunneling probability was calculated by modified-WKB approximation from [17][18]. The non-local band-to-band tunneling model was self-consistently solved with Poisson and Continuity equations. Transport away from the tunneling hetero-interfaces was calculated by Drift-Diffusion model as earlier. Local optical and Shockley-Read-Hall (SRH) inelastic thermal electron-hole generation and recombination were considered in the simulation. The electron and hole effective masses, relative to free electron rest mass (m_0), were again specified to be 0.041 and 0.4 for GaSb; 0.029 and 0.43 for $In_{0.85}Ga_{0.15}As$; and 0.055 and 0.49

for $In_{0.20}Ga_{0.80}As$; electron affinity and band-gap for GaSb layer were specified to be 4.06 eV and 0.726 eV respectively, all in consultation with [29]. The effective gate oxide thickness for the devices was 1 nm SiO_2. The source and drain contacts in all cases were designed to be ohmic contacts.

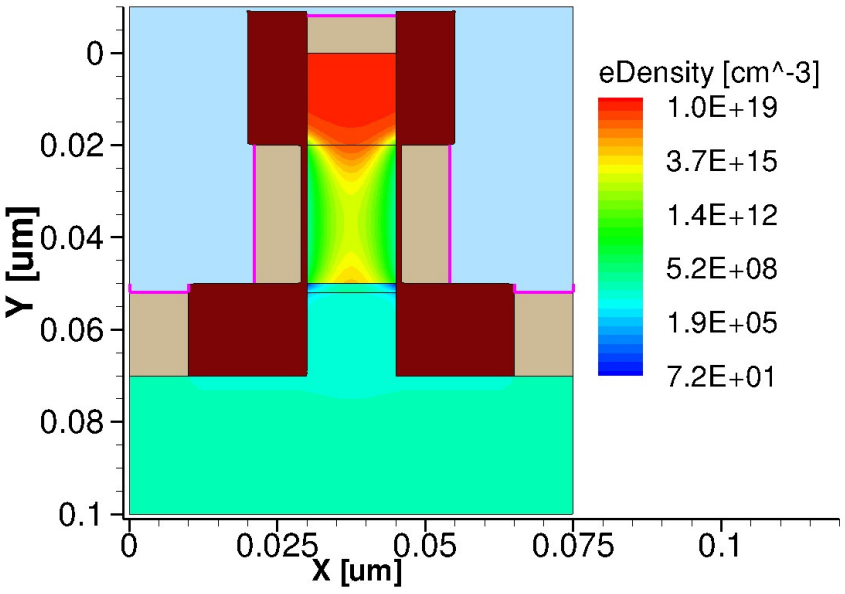


Figure 53. Electron density for JFET-type DG-n-HetTFET in OFF state at V_G = -0.75 V

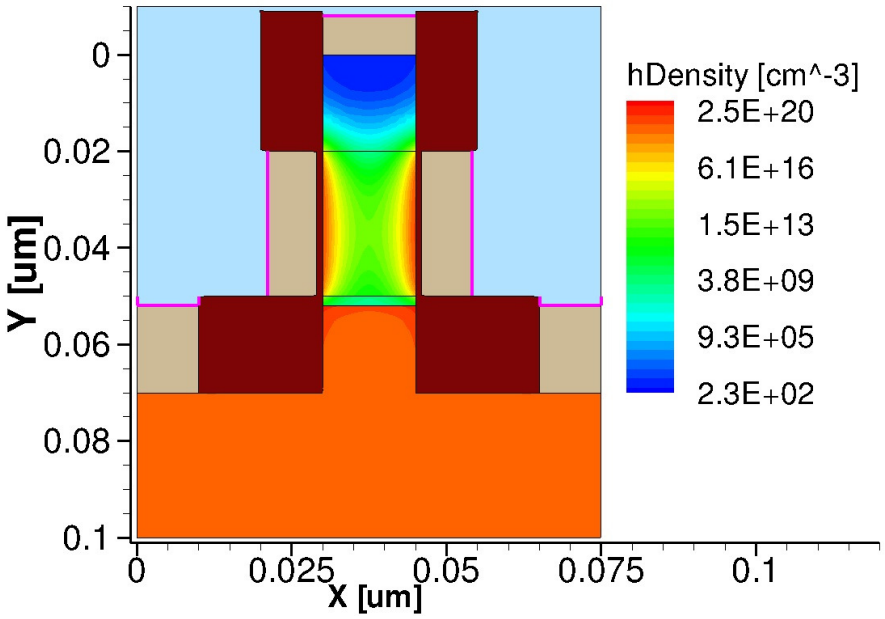


Figure 54. Hole density for JFET-type DG-n-HetTFET in OFF state at V_G = -0.75 V

Figure 53 and Figure 54 clearly show pinched-off and open gate channels in the junction-HetTFET. The electron densities peak right in the middle of the channel, and pinched from both sides, the device is in OFF state. Correspondingly, hole densities peak on both sides of the narrow opening of the channel. Figure 55 and Figure 56 show the linear and logarithmic I_{DS} vs. V_{GS} graphs for this first JFET-type DG-n-HetTFET device. Above threshold, a quite good transcoductance approaching 1 mA/μm/V is obtained. However, the subthreshold performance is clearly worse than the HetTFETs described in Chapter 6. (Note that the absolute gate voltages should be shifted by work-function engineering; as threshold is actually a bit of an ambiguous concept here, I did not reference the gate voltage to $V_{Th.}$) The critical problem is the misalignment in gate voltage by ~100 mV of the threshold as defined by band overlap across the tunnel barrier (Figure 56), and of channel pinch-off (Figure

55). This offset would effectively add ~100 mV to the required threshold voltage V_{Th}.

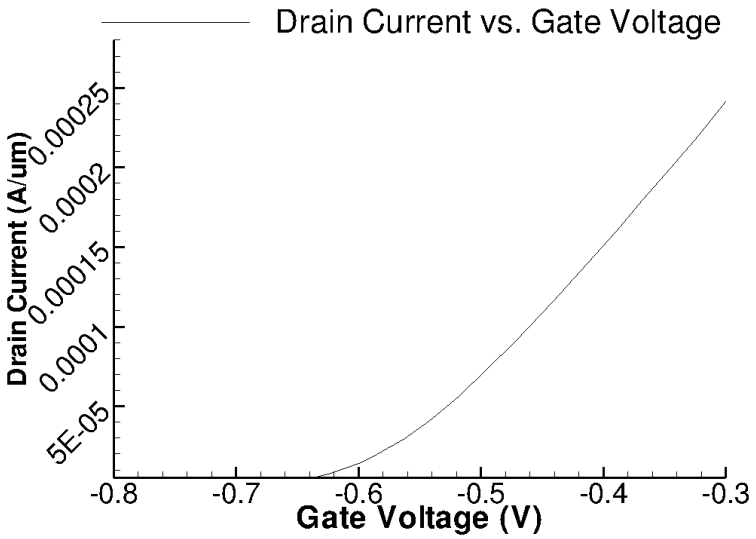


Figure 55. $I_{DS} - V_{GS}$ simulation for the device from Figure 53 and Figure 54

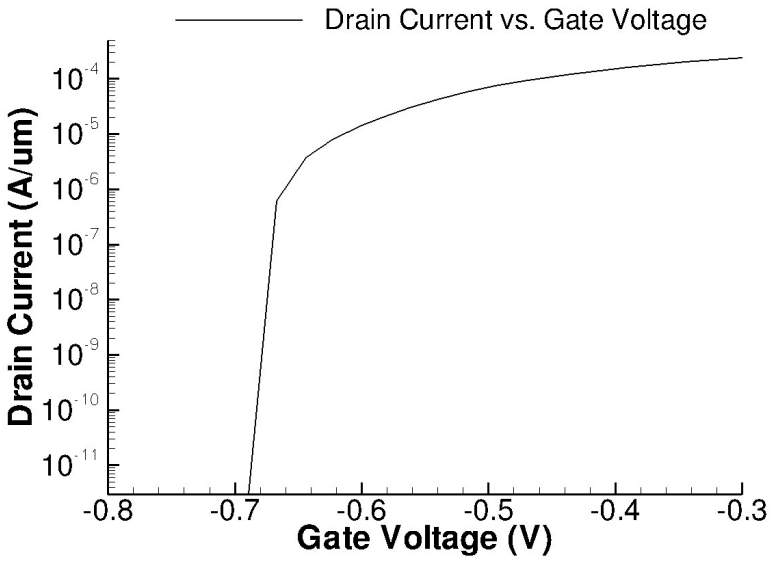


Figure 56. Log (I_{DS}) – V_{GS} simulation for the device from Figure 53 and Figure 54

Figure 57 and Figure 58 show the second JFET-type DG-n-HetTFET. It also has a widened 15 nm channel length, but only a 10 nm long gate. All other material parameters for this device are the same as the first device from Figure 53 and Figure 54. By limiting the gate length and forcing the pinch-off point in the channel closer to the tunnel barrier, we hoped to minimize the gate voltage difference between pinching off the channel and eliminating the band overlap across the tunnel barrier.

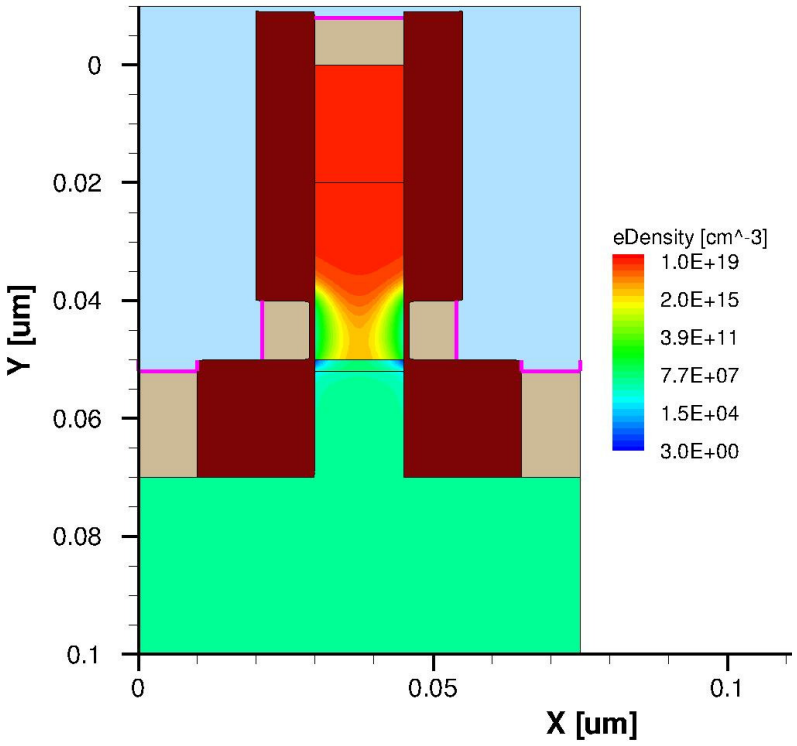


Figure 57. Electron density for JFET-type shortened-gate DG-n-HetTFET at V_G = -0.75 V

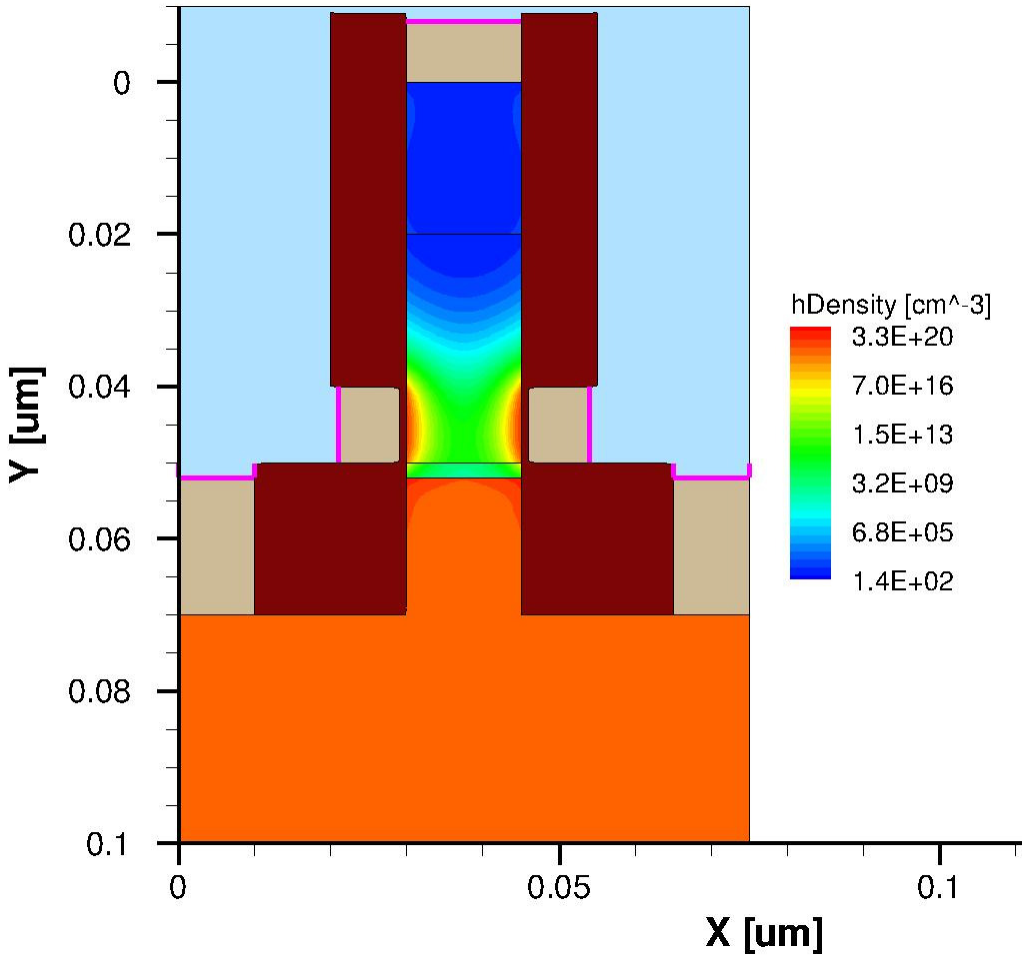


Figure 58. Hole density for JFET-type shortened-gate DG-n-HetTFET design at V_G = -0.75 V

Figure 59 and Figure 60 show the linear and logarithmic I_{DS} vs. V_{GS} graphs for this second JFET-type DG-n-HetTFET device. The subthreshold characteristic of this second device is only slightly, if at all, better than that of the first device, however, and the above threshold transconductance is somewhat worse.

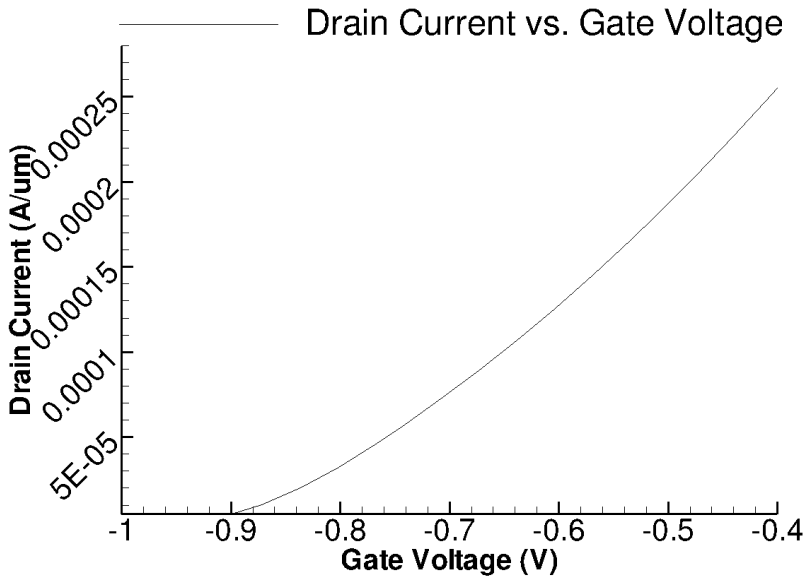


Figure 59. I_{DS} – V_{GS} simulation for the device from Figure 57 and Figure 58

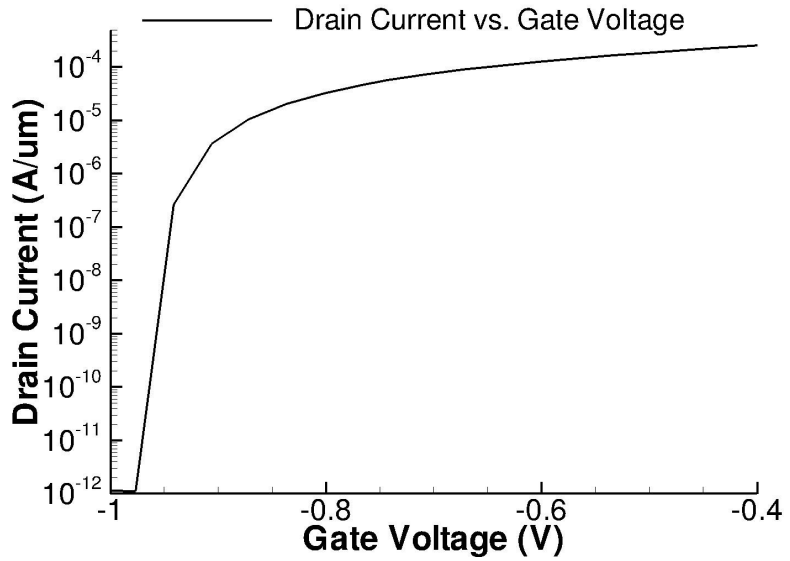


Figure 60. Log (I_{DS}) – V_{GS} simulation for the device from Figure 57 and Figure 58

Finally, Figure 61 and Figure 62 show the third JFET-type DG-n-HetTFET. It has a 10 nm channel length, and a 30 nm long gate, similar to the DG-n-HetTFET from Chapter 6. All other material parameters for this device are the same as the first device from Figure 53 and Figure 54, except that both n-type doping of drain and channel, and p-type doping of source have been doubled to $2x10^{19}/cm^3$.

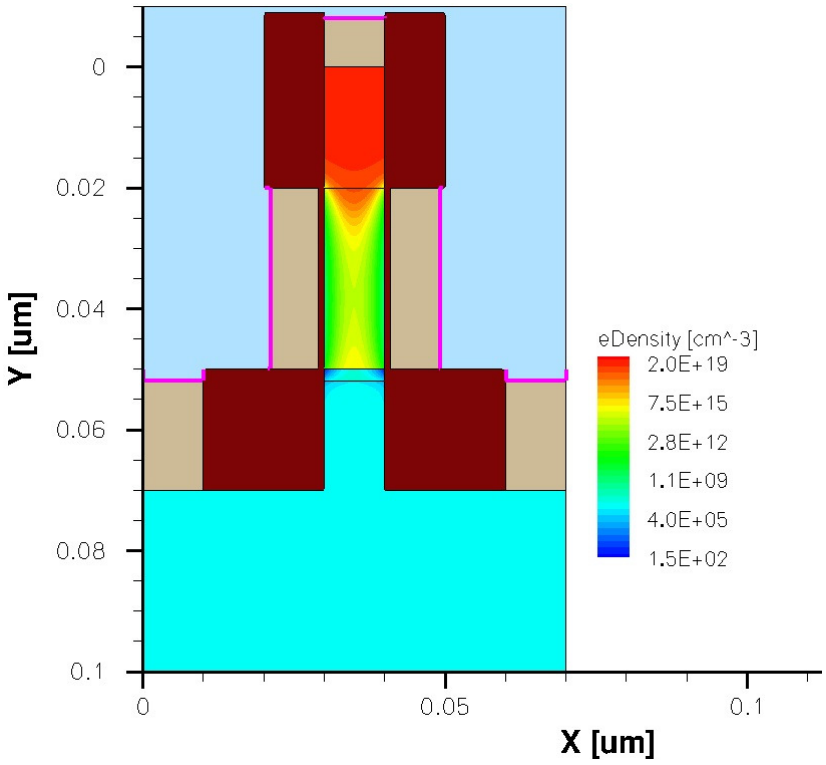


Figure 61. Electron density for 10 nm channel width JFET-type DG-n-HetTFET design at V_G = -0.75 V

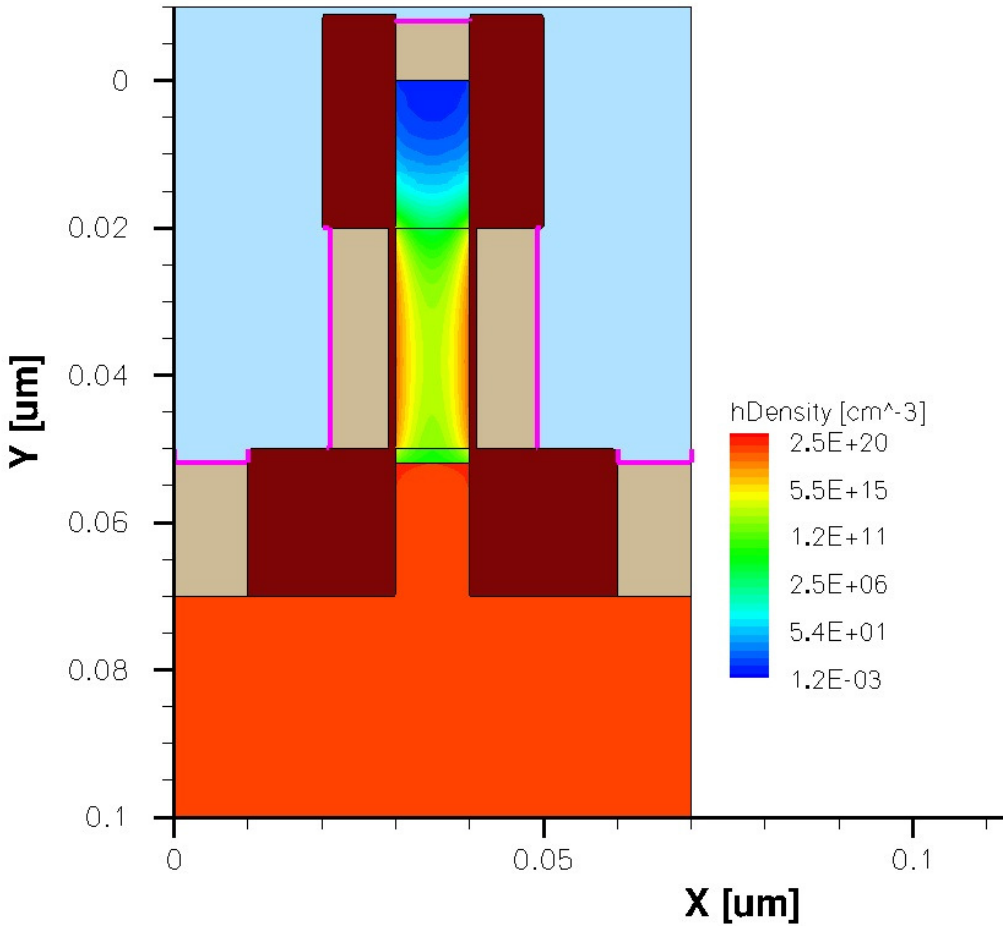


Figure 62. Hole density for 10 nm channel width JFET-type DG-n-HetTFET design at V_G = -0.75 V

Figure 63 and Figure 64 show the linear and logarithmic I_{DS} vs. V_{GS} graphs for this third JFET-type DG-n-HetTFET device. This device has the best subthreshold characteristics among the three devices discussed due to the more uniform potential distribution along the channel, with perhaps only a 50 mV lag between band-overlap and channel pinch-off, and with good above threshold behavior.

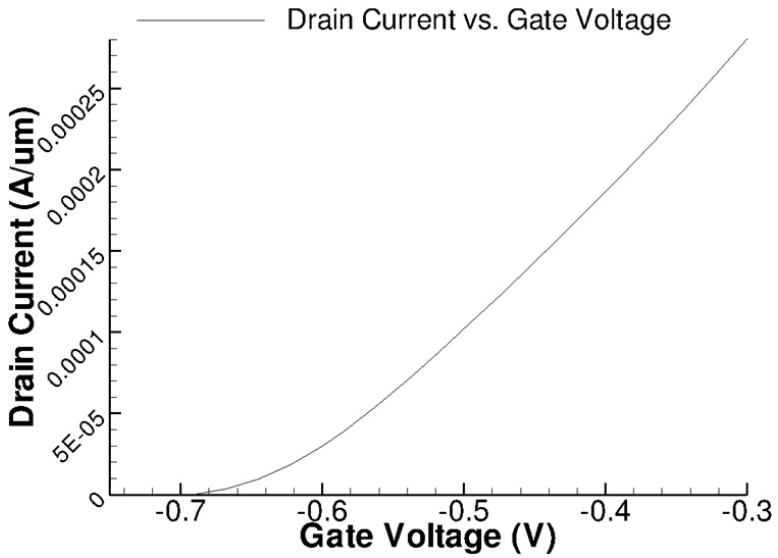


Figure 63. I_{DS} – V_{GS} simulation for the device from Figure 61 and Figure 62

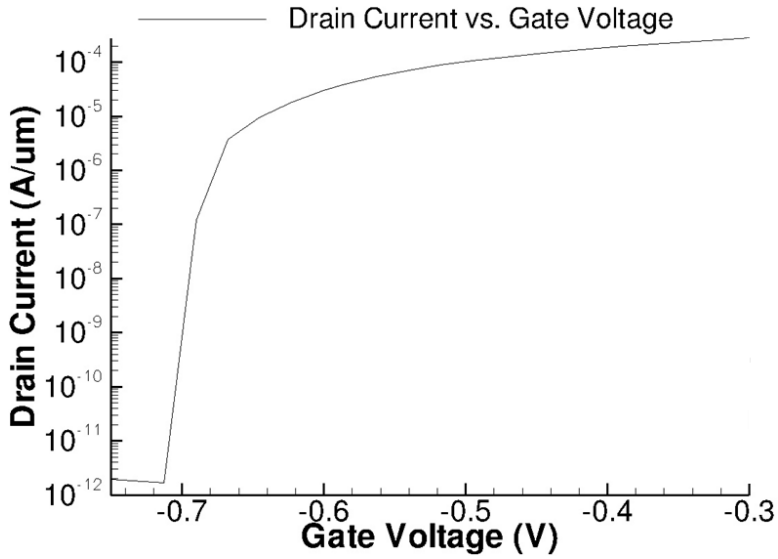


Figure 64. Log (I_{DS}) – V_{GS} simulation for the device from Figure 61 and Figure 62

7.3 Discussion

Overall, the results of this study on JFET-like versions of HetFET are mixed. As can be seen from the $I_{DS} - V_{GS}$ simulations of the three JFET-type DG-n-HetTFET designs, their simulated subthreshold performance is still quite good compared to conventional CMOS, with ~1 mA/μm/V transcondutances and a threshold voltage of only perhaps 50 mV to, allowing for some margin of error, 75 mV required for the latter device. However, as compared to the HetTFETs of Chapter 6, while their ON-state performance is on par, their subthreshold performance is significantly worse, again due to the gate voltage offset between band-overlap across the tunnel barrier and channel pinch-off. This approach could be susceptible to interface traps. However, the increased doping could produce more significant band tailing effects. In the end, based on simulation alone, the devices of Chapter 6 remain substantially superior. However, this approach, perhaps with further refinement, remains a plausible back-up design for HetTFETs.

CHAPTER 8. CONCLUSION

8.1 Summary

For 1T-1C pseudo-SRAM pass-transistor device, the results discussed in Chapter 3 are very promising. Further improvements can be made to the overall 1T-1C pseudo-SRAM design by using different Fin heights for the pass-transistor and for the storage capacitor. Perhaps even a DG-n-HetTFET-type pass-transistor that provides low leakage, rapid switching, and decent ON-current can be combined with the Fin-capacitor to get the perfect combination of low power, high performance, and large capacitance—all desirable characteristics of DRAM-like memory devices.

For the quantum dot memory device, further optimization is needed to balance the packing density needs against the drawbacks of inter-dot and dot-to-channel tunneling. Perhaps usage of high-κ dielectrics [38][39], as the gate and tunnel oxide, that permit greater physical separation among the dots and from the dots to the channel, yet offer smaller effective oxide thickness (EOT) will enable both increasing reliability and lowering the programming voltage.

For HetTFETs, very abrupt switching has been demonstrated with respect to V_g in simulation, which would allow for values of V_{Th} perhaps under 25 mV, that in turn could allow order of magnitude reductions in V_{DD} as compared to end-

of the roadmap CMOS and, thus, corresponding multi-order of magnitude reductions in power consumption which scales as V_{DD}^2. While the exhibited I_{ON} are small compared to those of CMOS, transconductances approaching CMOS-like values would still provide switching speeds approaching current CMOS-like values.

I recognize, however, that there are limitations to the modeling as well as technological challenges, e.g. the simulations do not account for parasitic phonon- or trap-assisted tunneling that could broaden the switching transition. Inelastic tunneling, however, would require phonon absorption rather than emission, and, low-order phonon-assisted tunneling cannot shorten the tunneling path as for other designs. Advances in III-V oxide technology would be required, perhaps leveraging on-going work on III-V MOSFETs to yet greater advantage. And design for manufacture is an already acknowledged need. But, by comparison, for MOSFETs, no technological advance can overcome the $\ln(10)k_BT/q$ subthreshold slope limit.

8.2 Future Work

The HetTFETs in this work represent a starting point to introduce the HetTFET concept for complementary logic, outline the basic operating principles, illustrate potential benefits through simulation, and motivate continued research. There are several avenues for refining this work. For experimental

implementation, it will be necessary to determine the precise alloy compositions of materials systems to achieve the marginal broken-gap alignments including the effects of quantum confinement, perhaps via density functional calculations. Other alloy material systems such as Cadmium-Mercury-Telluride ($Cd_xHg_{1-x}Te$) can be considered. Band tailing effects on the subthreshold behavior should be modeled, particularly as a function of barrier-adjacent doping concentrations. Atomistic tight binding or non-equilibrium density functional calculations of tunneling probability could be used to refine the desired barrier thicknesses. Spatially dependent doping concentrations could be optimized for overall performance improvements. Of course, simulation can only take one so far. Experiments work is the greatest future need.

APPENDIX

SAMPLE CODE FOR 2 NM BARRIER WIDTH DG n-HETTFET SIMULATION WITH SYNOPSYS TAURUS DEVICE 2-D AND SENTAURUS DEVICE 2-D SIMULATORS

```
# Device Structure Generation
# Enable device mode
Taurus {device}
# Define the device size, list the regions, and specify fixed mesh lines
DefineDevice (
        minX=0nm, maxX=70nm,
        minY=-10nm, maxY=100nm,
        Region (name=barrier1, material=InGaAs),
        Region (name=n_plus1, material=InGaAs),
        Region (name=n_plus2, material=InGaAs),
        Region (name=p_plus1, material=GaAsSb),
        Region (name=p_plus2, material=GaAsSb),
        Region (name=oxide1, material=Oxide),
        Region (name=oxide2, material=Oxide),
        Region (name=metal1, material=Metal),
        Region (name=metal2, material=Metal),
        Region (name=metal3, material=Metal),
        Region (name=metal4, material=Metal),
        Region (name=metal5, material=Metal)
)
DefineBoundary (
        region=p_plus2,
        Polygon2D (
                Point (x=0nm, y=70nm), Point (x=10nm, y=70nm),
                Point (x=30nm, y=70nm), Point (x=40nm, y=70nm),
                Point (x=60nm, y=70nm), Point (x=70nm, y=70nm),
                Point (x=70nm, y=100nm), Point (x=0nm, y=100nm)
        )
)
DefineBoundary (
        region=p_plus1,
        Polygon2D (
                Point (x=30nm, y=70nm), Point (x=30nm, y=52nm),
                Point (x=40nm, y=52nm), Point (x=40nm, y=70nm)
        )
```

```
)

DefineBoundary (
        region=barrier1,
        Polygon2D (
                Point (x=30nm, y=50nm), Point (x=40nm, y=50nm),
                Point (x=40nm, y=52nm), Point (x=30nm, y=52nm)
        )
)
DefineBoundary (
        region=n_plus1,
        Polygon2D (
                Point (x=30nm, y=20nm), Point (x=40nm, y=20nm),
                Point (x=40nm, y=50nm), Point (x=30nm, y=50nm)
        )
)
DefineBoundary (
        region=n_plus2,
        Polygon2D (
                Point (x=30nm, y=0nm), Point (x=40nm, y=0nm),
                Point (x=40nm, y=20nm), Point (x=30nm, y=20nm)
        )
)
# Define the oxide region
DefineBoundary (
        region=oxide1,
        Polygon2D (
                Point (x=10nm, y=50nm), Point (x=20nm, y=50nm),
                Point (x=21nm, y=50nm), Point (x=29nm, y=50nm),
                Point (x=29nm, y=20nm), Point (x=21nm, y=20nm),
                Point (x=20nm, y=20nm), Point (x=20nm, y=-9nm),
                Point (x=30nm, y=-9nm), Point (x=30nm, y=-8nm),
                Point (x=30nm, y=0nm), Point (x=30nm, y=20nm),
                Point (x=30nm, y=50nm), Point (x=30nm, y=52nm),
                Point (x=30nm, y=70nm), Point (x=10nm, y=70nm),
                Point (x=10nm, y=52nm)
        )
)
DefineBoundary (
        region=oxide2,
        Polygon2D (
```

```
                Point (x=40nm, y=70nm), Point (x=40nm, y=52nm),
                Point (x=40nm, y=50nm), Point (x=40nm, y=20nm),
                Point (x=40nm, y=0nm), Point (x=40nm, y=-8nm),
                Point (x=40nm, y=-9nm), Point (x=50nm, y=-9nm),
                Point (x=50nm, y=20nm), Point (x=49nm, y=20nm),
                Point (x=41nm, y=20nm), Point (x=41nm, y=50nm),
                Point (x=49nm, y=50nm), Point (x=50nm, y=50nm),
                Point (x=60nm, y=50nm), Point (x=60nm, y=52nm),
                Point (x=60nm, y=70nm)
        )
)
DefineBoundary (
        region=metal1,
        Polygon2D (
                Point (x=0nm, y=70nm), Point (x=0nm, y=52nm),
                Point (x=10nm, y=52nm), Point (x=10nm, y=70nm)
        )
)
DefineBoundary (
        region=metal2,
        Polygon2D (
                Point (x=60nm, y=70nm), Point (x=60nm, y=52nm),
                Point (x=70nm, y=52nm), Point (x=70nm, y=70nm)
        )
)
DefineBoundary (
        region=metal3,
        Polygon2D (
                Point (x=21nm, y=50nm), Point (x=21nm, y=20nm),
                Point (x=29nm, y=20nm), Point (x=29nm, y=50nm)
        )
)
DefineBoundary (
        region=metal4,
        Polygon2D (
                Point (x=41nm, y=50nm), Point (x=41nm, y=20nm),
                Point (x=49nm, y=20nm), Point (x=49nm, y=50nm)
        )
)
DefineBoundary (
        region=metal5,
```

```
        Polygon2D (
                Point (x=30nm, y=0nm), Point (x=30nm, y=-8nm),
                Point (x=40nm, y=-8nm), Point (x=40nm, y=0nm)
        )
)
DefineContact (name=drain, X (min=30nm, max=40nm), Y (min=-9nm, max=-
8nm))
DefineContact (name=source1, X (min=0nm, max=10nm), Y (min=50nm,
max=52nm))
DefineContact (name=source2, X (min=60nm, max=70nm), Y (min=50nm,
max=52nm))
DefineContact (name=gate1, X (min=20nm, max=21nm), Y (min=20nm,
max=50nm))
DefineContact (name=gate2, X (min=49nm, max=50nm), Y (min=20nm,
max=50nm))

Profile (name=Ntype, region=n_plus2, Uniform (value=1e18))
Profile (name=Ptype, region=p_plus1, Uniform (value=1e18))
Profile (name=Ptype, region=p_plus2, Uniform (value=1e18))

Profile (name=XMoleFraction, region=barrier1, Uniform(value=0.8))
Profile (name=XMoleFraction, region=n_plus1, Uniform(value=0.15))
Profile (name=XMoleFraction, region=n_plus2, Uniform(value=0.15))
#GaAsSb with 0% As
Profile (name=XMoleFraction, region=p_plus1, Uniform(value=0.0))
Profile (name=XMoleFraction, region=p_plus2, Uniform(value=0.0))
Regrid (gridProgram=pm, meshSpacingX = 4.0nm, meshSpacingY = 4.0nm)
Regrid (
        gridProgram=pm, meshSpacingX = 0.25nm, meshSpacingY = 0.25nm,
        minX=30nm, maxX=40nm, minY=15nm, maxY=65nm
)

Contact (name=gate1, workfunction=4.79606)
Contact (name=gate2, workfunction=4.79606)
Contact (name=drain, workfunction=4.79606)
Contact (name=source1, workfunction=4.79606)
Contact (name=source2, workfunction=4.79606)
Voltage( electrode=gate1, value=0.0 )
Voltage( electrode=gate2, value=0.0 )
Symbolic (carriers=0, newton, direct)
Numerics (iterations=200)
```

```
Solve {}

# Save structure
Save (meshfile=tunnelmos.tdf
Add (
        ConductionBand ValenceBand
        ElectronQuasiFermiEnergy HoleQuasiFermiEnergy
        )
)
```
 # End Device Structure Generation

 # Parameter File
```
Region = "p_plus1" {
Epsilon
{ *  Ratio of the permittivities of material and vacuum
  * epsilon() = epsilon
        epsilon= 15.7  # [1]
}
Epsilon_aniso
{ *  Ratio of the permittivities of material and vacuum
  * epsilon() = epsilon
        epsilon= 15.7  # [1]
}
Bandgap
{ * Eg = Eg0
# { * Eg = Eg0 + dEg0 + alpha Tpar^2 / (beta + Tpar) - alpha T^2 / (beta + T)
  * dEg0(<bgn_model_name>) is a band gap correction term.  It is used together
with
  * an appropriate BGN model, if this BGN model is chosen in Physics section
  * Parameter 'Tpar' specifies the value of lattice
  * temperature, at which parameters below are defined
  * Chi0 is electron affinity.
        Chi0    = 4.06  # [eV]
        Bgn2Chi         = 0.5    # [1]
        Eg0     = 0.726          # [eV]
        dEg0(Bennett)= 0.0000e+00  # [eV]
        dEg0(Slotboom)          = 0.0000e+00  # [eV]
        dEg0(OldSlotboom)   = 0.0000e+00  # [eV]
        dEg0(delAlamo)          = 0.0000e+00  # [eV]
        alpha   = 4.7300e-04   # [eV K^-1]
        beta    = 6.3600e+02  # [K]
```

```
        Tpar    = 300.0000e+00          # [K]
}
eDOSMass
{
  * For effective mass specificatition Formula1 (me approximation):
  * or Formula2 (Nc300) can be used :
        Formula         = 1     # [1]
  * Formula1:
  * me/m0 = 0.041
# me/m0 = [ (9 * mt)^2 *  ml ]^(1/3) + mm
  * mt = a[Eg(0)/Eg(T)]
  * Nc(T) = 2.1e17
#  * Nc(T) = 2(2pi*kB/h_Planck^2*me*T)^3/2 = 2.540e19
((me/m0)*(T/300))^3/2
        a       = 0.041                 # [1]
#       a       = 0.1905        # [1]
        ml      = 0.9163        # [1]
        mm      = 0.0000e+00  # [1]
}
hDOSMass
{
  * For effective mass specificatition Formula1 (mh approximation):
  * or Formula2 (Nv300) can be used :
        Formula         = 1     # [1]
  * Formula1:
  * mh =  m0*0.4
# mh =  m0*{[(a+bT+cT^2+dT^3+eT^4)/(1+fT+gT^2+hT^3+iT^4)]^(2/3) +
mm}
  * Nv(T) = 1.8e19
#  * Nv(T) = 2(2pi*kB/h_Planck^2*mh*T)^3/2 = 2.540e19
((mh/m0)*(T/300))^3/2
        a       = 0.443587      # [1]
        b       = 0.003609528           # [K^-1]
        c       = 0.0001173515          # [K^-2]
        d       = 1.263218e-06          # [K^-3]
        e       = 3.025581e-09          # [K^-4]
        f       = 0.004683382           # [K^-1]
        g       = 0.0002286895          # [K^-2]
        h       = 7.469271e-07          # [K^-3]
        i       = 1.727481e-09          # [K^-4]
        mm      = 0     # [1]
```

```
}
QuantumPotentialParameters
{ * gamma:  weighting factor for quantum potential
  * theta:  weight for quadratic term
  * xi:     weight for quasi Fermi potential
  * eta:    weight for electrostatic potential
  * nu :    weight for DOS mass change from stress
          gamma= 3.6 ,  5.6       # [1]
          theta    = 0.5 ,  0.5       # [1]
          xi       = 1 ,    1         # [1]
          eta      = 1 ,    1         # [1]
          nu       = 0.0000e+00 ,          0.0000e+00     # [1]
}
ConstantMobility:
{ * mu_const = mumax
# * mu_const = mumax (T/T0)^(-Exponent)
          mumax= 3.0e+03 ,      1.0e+03          # [cm^2/(Vs)]
          Exponent         = 2.5 ,  2.2       # [1]
          mutunnel         = 0.05 ,          0.05     # [cm^2/(Vs)]
}
ConstantMobility_aniso:
{ * mu_const = mumax
# * mu_const = mumax (T/T0)^(-Exponent)
          mumax= 3.0e+03 ,      1.0e+03          # [cm^2/(Vs)]
          Exponent         = 2.5 ,  2.2       # [1]
          mutunnel         = 0.05 ,          0.05     # [cm^2/(Vs)]
}
Scharfetter * relation and trap level for SRH recombination:
{ * tau = taumin + ( taumax - taumin ) / ( 1 + ( N/Nref )^gamma)
  * tau(T) = tau * ( (T/300)^Talpha )          (TempDep)
  * tau(T) = tau * exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)
          taumin = 0.0000e+00 ,          0.0000e+00     # [s]
          taumax= 1.0000e-05 , 3.0000e-06      # [s]
          Nref     = 1.0000e+16 ,          1.0000e+16     # [cm^(-3)]
          gamma= 1 ,     1         # [1]
          Talpha = -1.5000e+00 ,          -1.5000e+00    # [1]
          Tcoeff = 2.55 ,          2.55     # [1]
          Etrap   = 0.0000e+00  # [eV]
}
SurfaceRecombination * surface SRH recombination:
{ * s = S0 ( 1 + Sref ( N/Nref )^gamma ) recombination velocity
```

```
        S0      = 1.0000e+03 ,          1.0000e+03    # [cm/s]
        Sref    = 1.0000e-03  # [1]
        Nref    = 1.0000e+16  # [cm^(-3)]
        gamma= 1      # [1]
        Etrap   = 0.0000e+00  # [eV]
}
Auger * coefficients:
{ * R_Auger = ( C_n n + C_p p ) ( n p - ni_eff^2)
  * with C_n,p = (A + B (T/T0) + C (T/T0)^2) (1 + H exp(-{n,p}/N0))
        A       = 6.7000e-32 , 7.2000e-32     # [cm^6/s]
        B       = 2.4500e-31 , 4.5000e-33     # [cm^6/s]
        C       = -2.2000e-32 ,         2.6300e-32    # [cm^6/s]
        H       = 3.46667 ,     8.25688         # [1]
        N0      = 1.0000e+18 ,          1.0000e+18    # [cm^(-3)]
}
TrapAssistedAuger * lifetimes:
{ * 1/tau_TAA = c ( n + p )
        c       = 1.0000e-12 , 1.0000e-12     # [cm^3/s]
}
TrapAssistedTunneling
{ * See Sentaurus Device manual `Trap-Assisted Tunneling enhanced SRH'
        S       = 3.5   # [1]
        hbarOmega       = 0.068         # [eV]
        m_theta         = 0.258 ,       0.24    # [1]
        Z       = 0.0000e+00  # [1]
        MinField        = 0.0000e+00  # [V/cm]
        DenCorRef       = 1.0000e+03 ,          1.0000e+03    # [cm^-3]
}
HurkxTrapAssistedTunneling
{ * SRHlifetime = tau0/(1+Gt)
  * TrapXsection = Xsec0*(1+Gt)
  * Gt = pi^0.5*E*exp(E*E/3)*(2-erfc(0.5*(En/E-E))),      for E < En^0.5
  * Gt = (pi*E)^0.5*En^0.25*exp(-En+E*En^0.5+En^1.5/E/3)*
  *      erfc(E^0.5*En^0.25-En^0.75/E^0.5),              for E >= En^0.5
  * where
  *       E = F/Fref,
  *       F is the electric field,
  *       Fref = (8*mt*m0*(kB*T)^3)^0.5/q/h / ~4.3e5*mt^0.5*(T/300)^1.5 V/cm /,
  *       En is a function of trap level and carrier concentration (see manual),
  *            the trap level will be used from SRH or Trap specifications.
        mt      = 0.5 ,  0.5      # [1]
```

```
}
Band2BandTunneling
{ * See Sentaurus Device manual `Band-To-Band Tunneling'
        A         = 8.9770e+20  # [cm / (s V^2)]
        B         = 2.1466e+07  # [eV^(-3/2) V/cm]
        hbarOmega     = 0.0186          # [eV]
  * Traditional models for the following keywords in input file:
  * Band2Band(E1)  : A1*E*exp(-B1/E)
  * Band2Band(E1_5): A1_5*E^1.5*exp(-B1_5/E)
  * Band2Band(E2)  : A2*E^2*exp(-B2/E)
        A1        = 1.1000e+27  # [1/cm/sec/V]
        B1        = 2.1300e+07  # [V/cm]
        A1_5      = 1.9000e+24  # [1/cm/sec/V^1.5]
        B1_5      = 2.1900e+07  # [V/cm]
        A2        = 3.5000e+21  # [1/cm/sec/V^2]
        B2        = 2.2500e+07  # [V/cm]
  * Hurkx model for the following keywords in input file:
  * Band2Band(Hurkx)  : -Agen*D*(E/E0)^Pgen*exp(-Bgen*(Eg/Eg300)^1.5/E)
if D < 0
  *                -Arec*D*(E/E0)^Prec*exp(-Brec*(Eg/Eg300)^1.5/E) if D > 0
  *                D = (n*p-ni^2)/(n+ni)/(p+ni)*(1-|alpha|)+alpha, E0 = 1 V/cm
  *                So, if alpha = 0, it's original Hurkx model,
  *                    if alpha = -1, it's only generation,
  *                    if alpha = +1, it's only recombination.
        Agen      = 3.5000e+21  # [1/cm^3/sec]
        Bgen      = 2.2500e+07  # [V/cm]
        Pgen      = 2       # [1]
        Arec      = 3.5000e+21  # [1/cm^3/sec]
        Brec      = 2.2500e+07  # [V/cm]
        Prec      = 2       # [1]
        alpha     = 0.0000e+00  # [1]
  * nonlocal B2B models for the following keywords in command file:
  * Band2Band(Model=NonlocalPath1) : Nonlocal B2B tunneling with single
transition process   using the first tunneling path
  * Band2Band(Model=NonlocalPath2) : Nonlocal B2B tunneling with two
transition processes using the first and second tunneling paths
  * Band2Band(Model=NonlocalPath3) : Nonlocal B2B tunneling with three
transition processes using the all three tunneling paths
  * For the i-th nonlocal B2B process (i=1, 2, or 3):
  * Apathi : Prefactor Ad or Ap in the uniform field limit for the direct or indirect
tunneling
```

```
  * Bpathi : Exponent  Bd or Bp in the uniform field limit for the direct or indirect
tunneling
  * Dpathi : The conduction band offset D
  * Ppathi : The phonon energy P
  *         Note that the indirect tunneling process is assumed if P>0, and the direct
tunneling process is assumed if P=0
  * Rpathi : The ratio mv/mc. If Rpathi=0, it is automatically determined by
  *         mv/mc = (1 + 2*mr)/(1 - 2*mr)
  *         where mr=mc*mv/(mc+mv) is the reduced mass
  * In the uniform field limit, the generation rate can be expressed by
  * G = A * (F/F0)^2   * Exp(-B/F) for   direct tunneling
  *   = A * (F/F0)^2.5 * Exp(-B/F) for indirect tunneling
  * where
  * Ad = g * mr^0.5 * qF0^2 / (36 * pi * h_bar^2 *E_T^0.5)
  * Ap = g *(mc*mv)^1.5 * (1+2*N) * qF0^2.5 * Dop^2 / (2^7.75 * pi^2.5 *
h_bar^2.5 * mr^1.25 * E_T^1.75 * rho * P)
  * Bd = pi    * mr^0.5 * E_T^1.5 / (2 * h_bar * q)
  * Bp = 2^2.5 * mr^0.5 * E_T^1.5 / (3 * h_bar * q)
  * F0 = 1 V/cm, qF0 = 1 eV/cm, E_T = E_G + D
  * From the above expression, the microscopic parameters such as mr, mc, and
mv for the nonlocal B2B model are extracted internally
          Apath1= 4.0000e+14  # [1/cm^3/sec]
          Bpath1= 1.9000e+07  # [V/cm]
          Dpath1= 0.0000e+00  # [eV]
          Ppath1 = 0.037          # [eV]
          Rpath1= 0.0000e+00  # [1]
          Apath2= 0.0000e+00  # [1/cm^3/sec]
          Bpath2= 0.0000e+00  # [V/cm]
          Dpath2= 0.0000e+00  # [eV]
          Ppath2 = 0.0000e+00  # [eV]
          Rpath2= 0.0000e+00  # [1]
          Apath3= 0.0000e+00  # [1/cm^3/sec]
          Bpath3= 0.0000e+00  # [V/cm]
          Dpath3= 0.0000e+00  # [eV]
          Ppath3 = 0.0000e+00  # [eV]
          Rpath3= 0.0000e+00  # [1]
          MaxTunnelLength      = 1.0000e-05   # [cm]
  * min length to interfaces (for traditional & Hurkx models):
          dDist   = 5.0e-08        # [cm]
  * min potential difference on length dPot/E (for traditional & Hurkx models):
          dPot    = 0.0000e+00  # [V]
```

```
  * numeric smoothing
        MinField        = 0.0000e+00  # [V/cm]
        MinGradQF       = 0.0000e+00  # [eV/cm]
        DenCorRef       = 0.0000e+00 ,          0.0000e+00     # [cm^-3]
}
BarrierTunneling
{ * Non Local Barrier Tunneling
  * G(r) = g*A*T/kB*F(r)*Pt(r)*ln[(1+exp((E(r)-Es)/kB/T))/(1+exp((E(r)-
Em)/kB/T))]
  * where:
  *     Pt(r) is WKB approximation for the tunneling probability
  *     g = As/A, As is the Richardson constant for carriers in semiconductor
  *     A is the Richardson constant for free electrons
  *     F(r) is the electric field
  *     E(r) is carrier energy
  *     Es is carrier quasi fermi energy in semiconductor
  *     Em is carrier fermi energy in metal
  *     alpha is the prefactor for quantum potential correction
  *     eoffset and hoffset are lists of band offsets
        g         = 0.45767 ,     0.389   # [1]
        mt        = 0.041e+00 ,  0.4e+00          # [1]
        alpha     = 0.0000e+00 ,          0.0000e+00     # [1]
        eoffset = () # eV
        hoffset = () # eV
}
SchottkyResistance
{ * Schottky resistance parameters
  * Rsch = Rinf*(300/T)*exp(q*PhiB/E0)
  * where:
  *     PhiB is the Schottky potential barrier
  *     Rinf is the Schottky resistance for an infinite doping concentration
  *     E0 = E00*cosh(E00/kT), E00 = (qh/4pi)*(N/eps/mt)^0.5
  *     N is the doping concentration at the contact
  *     T is the device temperature (defined in Physics section)
  *     eps is the semiconductor permitivity
  *     mt is the tunneling mass
        Rinf      = 2.4000e-09 , 5.2000e-09      # [Ohm*cm^2]
        PhiB      = 0.6 ,  0.51     # [eV]
        mt        = 0.041 ,         0.4       # [1]
}
DirectTunnelling
```

```
{ * eps_ins:   insulator dielectricity,
  * E_F_M:     metal Fermi energy,
  * m_M:       metal effective mass,
  * m_ins:     insulator effective mass,
  * m_s:       semiconductor effective mass,
  * m_dos:     semiconductor DOS effective mass,
  * E_barrier: height of barrier between semiconductor and oxide,
  * E_i:       energy nodes for pseudo barrier,
  * See the manual for more details.
        eps_ins          = 2.13  # [1]
        E_F_M            = 11.7  # [eV]
        m_M   = 1        # [m0]
        m_ins  = 0.5 ,  0.77     # [m0]
        m_s     = 0.19 ,         0.16     # [m0]
        m_dos = 0.32 ,           0.0000e+00     # [m0]
        E_barrier        = 3.15 ,         4.73     # [eV]
        E0       = 0.0000e+00 ,          0.0000e+00     # [eV]
        E1       = 0.0000e+00 ,          0.0000e+00     # [eV]
        E2       = 0.0000e+00 ,          0.0000e+00     # [eV]
}
RadiativeRecombination * coefficients:
{ * R_Radiative = C * (T/Tpar)^alpha * (n p - ni_eff^2)
  * C
  * alpha
        C        = 0.0000e+00  # [cm^3/s]
        alpha    = 0.0000e+00  # []
}
BarrierLowering
{ * dB = a1 * ( (E/E0)^p1 - (Eeq/E0)^p1_eq ) +
  *      a2 * ( (E/E0)^p2 - (Eeq/E0)^p2_eq ),
  * where E is the electric field [V/cm],
  *       Eeq is the electric field at equilibrium (zero bias),
  *       E0 = 1 V/cm.
        a1       = 2.6000e-04   # [eV]
        p1       = 0.5    # [1]
        p1_eq  = 0.5    # [1]
        a2       = 0.0000e+00  # [eV]
        p2       = 1      # [1]
        p2_eq  = 1      # [1]
}
LatticeParameters
```

```
{ * Crystal system, elasticity, and deformation potential are defined.
  * X and Y vectors define the simulation coordinate system relative to the
  * crystal orientation system. Also there is an option to represent the crystal
  * system relative to the simulation one. In this case a keyword CrystalAxis
  * has to be in this section and X and Y vectors will represent [100] and [010]
  * axis of the crystal system in the simulation one.
  * Additional notes: 1 Pa = 10 dyn/cm^2; tensile stress/strain is positive.
  *
  * S[i][j] - elasticity modulus; i,j = 1,2,...6 and j>=i.
  * CrystalSystem is symmetry, used ONLY to define the elasticity matrics.
  *   Cubic (CrystalSystem=0): S[1][1],S[1][2],S[4][4]
  *   Hexagonal (CrystalSystem=1): S[1][1],S[1][2],S[1][3],S[3][3],S[4][4]
  * NC is a number of conduction band levels taken into account
  * NV is a number of valence band levels taken into account
  * DC2(l) defines deformation potentials for conduction subband = l
  * DV2(l) defines deformation potentials for valence subband = l
  * The subband energy shift due to strain (E) is equal to the following sum:
  * D2[1]*E11 + D2[2]*E22 + D2[3]*E33 +
  * D2[4]*(0.5*D2[5]^2*((E11-E22)^2+(E22-E33)^2+(E33-
E11)^2)+D2[6]^2*(E23^2+E13^2+E12^2))
  *
        X       = (1, 0.0000e+00, 0.0000e+00) #[1]
        Y       = (0.0000e+00, 1, 0.0000e+00) #[1]
        S[1][1]= 0.77  # [1e-12 cm^2/din]
        S[1][2]= -2.1000e-01 # [1e-12 cm^2/din]
        S[4][4]= 1.25  # [1e-12 cm^2/din]
        CrystalSystem = 0       # [1]
        NC      = 3     # [1]
        NV      = 2     # [1]
        DC2(1)          = 0.9, -8.6000e+00, -8.6000e+00, 0.0000e+00,
0.0000e+00, 0.0000e+00      #[eV]
        DC2(2)          = -8.6000e+00, 0.9, -8.6000e+00, 0.0000e+00,
0.0000e+00, 0.0000e+00      #[eV]
        DC2(3)          = -8.6000e+00, -8.6000e+00, 0.9, 0.0000e+00,
0.0000e+00, 0.0000e+00      #[eV]
        DV2(1)          = -2.1000e+00, -2.1000e+00, -2.1000e+00, -1.0000e+00,
0.5, 4  #[eV]
        DV2(2)          = -2.1000e+00, -2.1000e+00, -2.1000e+00, 1, 0.5, 4 #[eV]
  * Deformation potentials of k.p model for electron bands
        xis     = 7     # [eV]
        dbs     = 0.53  # [eV]
```

```
        xiu      = 9.16  # [eV]
        xid      = 0.77  # [eV]
  * Deformation potentials of k.p model for hole bands
        adp      = 2.1    # [eV]
        bdp      = -2.3300e+00# [eV]
        ddp      = -4.7500e+00# [eV]
        dso      = 0.044          # [eV]
  * Luttinger parameters and Sverdlov's k.p theory parameter
        gamma_1        = 4.27  # [1]
        gamma_2        = 0.315          # [1]
        gamma_3        = 1.4576         # [1]
        Mkp    = 1.2    # [1]
}
}
Region = "p_plus2" {
Epsilon
{ *  Ratio of the permittivities of material and vacuum
  * epsilon() = epsilon
        epsilon= 15.7  # [1]
}
Epsilon_aniso
{ *  Ratio of the permittivities of material and vacuum
  * epsilon() = epsilon
        epsilon= 15.7  # [1]
}
Bandgap
{ * Eg = Eg0
# { * Eg = Eg0 + dEg0 + alpha Tpar^2 / (beta + Tpar) - alpha T^2 / (beta + T)
  * dEg0(<bgn_model_name>) is a band gap correction term.  It is used together
with
  * an appropriate BGN model, if this BGN model is chosen in Physics section
  * Parameter 'Tpar' specifies the value of lattice
  * temperature, at which parameters below are defined
  * Chi0 is electron affinity.
        Chi0     = 4.06  # [eV]
        Bgn2Chi          = 0.5    # [1]
        Eg0      = 0.726          # [eV]
        dEg0(Bennett)= 0.0000e+00  # [eV]
        dEg0(Slotboom)         = 0.0000e+00  # [eV]
        dEg0(OldSlotboom)   = 0.0000e+00  # [eV]
        dEg0(delAlamo)         = 0.0000e+00  # [eV]
```

```
        alpha   = 4.7300e-04  # [eV K^-1]
        beta    = 6.3600e+02  # [K]
        Tpar    = 300.0000e+00        # [K]
}
eDOSMass
{
  * For effective mass specificatition Formula1 (me approximation):
  * or Formula2 (Nc300) can be used :
        Formula         = 1     # [1]
  * Formula1:
  * me/m0 = 0.041
# me/m0 = [ (9 * mt)^2 *  ml ]^(1/3) + mm
  * mt = a[Eg(0)/Eg(T)]
  * Nc(T) = 2.1e17
#  * Nc(T) = 2(2pi*kB/h_Planck^2*me*T)^3/2 = 2.540e19
((me/m0)*(T/300))^3/2
        a       = 0.041                 # [1]
#       a       = 0.1905        # [1]
        ml      = 0.9163        # [1]
        mm      = 0.0000e+00  # [1]
}
hDOSMass
{
  * For effective mass specificatition Formula1 (mh approximation):
  * or Formula2 (Nv300) can be used :
        Formula         = 1     # [1]
  * Formula1:
  * mh =  m0*0.4
# mh =  m0*{[(a+bT+cT^2+dT^3+eT^4)/(1+fT+gT^2+hT^3+iT^4)]^(2/3) +
mm}
  * Nv(T) = 1.8e19
#  * Nv(T) = 2(2pi*kB/h_Planck^2*mh*T)^3/2 = 2.540e19
((mh/m0)*(T/300))^3/2
        a       = 0.443587      # [1]
        b       = 0.003609528         # [K^-1]
        c       = 0.0001173515        # [K^-2]
        d       = 1.263218e-06        # [K^-3]
        e       = 3.025581e-09        # [K^-4]
        f       = 0.004683382         # [K^-1]
        g       = 0.0002286895        # [K^-2]
        h       = 7.469271e-07        # [K^-3]
```

```
        i       = 1.727481e-09          # [K^-4]
        mm      = 0     # [1]
}
QuantumPotentialParameters
{ * gamma:  weighting factor for quantum potential
  * theta:  weight for quadratic term
  * xi:     weight for quasi Fermi potential
  * eta:    weight for electrostatic potential
  * nu :    weight for DOS mass change from stress
        gamma= 3.6 ,  5.6       # [1]
        theta   = 0.5 ,  0.5    # [1]
        xi      = 1 ,    1      # [1]
        eta     = 1 ,    1      # [1]
        nu      = 0.0000e+00 ,          0.0000e+00    # [1]
}
ConstantMobility:
{ * mu_const = mumax
# * mu_const = mumax (T/T0)^(-Exponent)
        mumax= 3.0e+03 ,     1.0e+03          # [cm^2/(Vs)]
        Exponent        = 2.5 ,  2.2    # [1]
        mutunnel        = 0.05 ,         0.05    # [cm^2/(Vs)]
}
ConstantMobility_aniso:
{ * mu_const = mumax
# * mu_const = mumax (T/T0)^(-Exponent)
        mumax= 3.0e+03 ,     1.0e+03          # [cm^2/(Vs)]
        Exponent        = 2.5 ,  2.2    # [1]
        mutunnel        = 0.05 ,         0.05    # [cm^2/(Vs)]
}
Scharfetter * relation and trap level for SRH recombination:
{ * tau = taumin + ( taumax - taumin ) / ( 1 + ( N/Nref )^gamma)
  * tau(T) = tau * ( (T/300)^Talpha )         (TempDep)
  * tau(T) = tau * exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)
        taumin = 0.0000e+00 ,           0.0000e+00    # [s]
        taumax= 1.0000e-05 , 3.0000e-06     # [s]
        Nref    = 1.0000e+16 ,          1.0000e+16    # [cm^(-3)]
        gamma= 1 ,     1        # [1]
        Talpha = -1.5000e+00 ,          -1.5000e+00   # [1]
        Tcoeff = 2.55 ,         2.55    # [1]
        Etrap   = 0.0000e+00  # [eV]
}
```

```
SurfaceRecombination * surface SRH recombination:
{ * s = S0 ( 1 + Sref ( N/Nref )^gamma ) recombination velocity
        S0      = 1.0000e+03 ,          1.0000e+03    # [cm/s]
        Sref    = 1.0000e-03  # [1]
        Nref    = 1.0000e+16  # [cm^(-3)]
        gamma= 1      # [1]
        Etrap   = 0.0000e+00  # [eV]
}
Auger * coefficients:
{ * R_Auger = ( C_n n + C_p p ) ( n p - ni_eff^2)
  * with C_n,p = (A + B (T/T0) + C (T/T0)^2) (1 + H exp(-{n,p}/N0))
        A       = 6.7000e-32 , 7.2000e-32     # [cm^6/s]
        B       = 2.4500e-31 , 4.5000e-33     # [cm^6/s]
        C       = -2.2000e-32 ,         2.6300e-32    # [cm^6/s]
        H       = 3.46667 ,     8.25688         # [1]
        N0      = 1.0000e+18 ,          1.0000e+18    # [cm^(-3)]
}
TrapAssistedAuger * lifetimes:
{ * 1/tau_TAA = c ( n + p )
        c       = 1.0000e-12 , 1.0000e-12     # [cm^3/s]
}
TrapAssistedTunneling
{ * See Sentaurus Device manual `Trap-Assisted Tunneling enhanced SRH'
        S       = 3.5   # [1]
        hbarOmega       = 0.068         # [eV]
        m_theta         = 0.258 ,       0.24    # [1]
        Z       = 0.0000e+00  # [1]
        MinField        = 0.0000e+00  # [V/cm]
        DenCorRef       = 1.0000e+03 ,          1.0000e+03    # [cm^-3]
}
HurkxTrapAssistedTunneling
{ * SRHlifetime = tau0/(1+Gt)
  * TrapXsection = Xsec0*(1+Gt)
  * Gt = pi^0.5*E*exp(E*E/3)*(2-erfc(0.5*(En/E-E))),      for E < En^0.5
  * Gt = (pi*E)^0.5*En^0.25*exp(-En+E*En^0.5+En^1.5/E/3)*
  *      erfc(E^0.5*En^0.25-En^0.75/E^0.5),              for E >= En^0.5
  * where
  *       E = F/Fref,
  *       F is the electric field,
  *       Fref = (8*mt*m0*(kB*T)^3)^0.5/q/h / ~4.3e5*mt^0.5*(T/300)^1.5 V/cm /,
  *       En is a function of trap level and carrier concentration (see manual),
```

```
  *            the trap level will be used from SRH or Trap specifications.
        mt      = 0.5 ,  0.5      # [1]
}
Band2BandTunneling
{ * See Sentaurus Device manual `Band-To-Band Tunneling'
        A       = 8.9770e+20  # [cm / (s V^2)]
        B       = 2.1466e+07  # [eV^(-3/2) V/cm]
        hbarOmega     = 0.0186          # [eV]

  * Traditional models for the following keywords in input file:
  * Band2Band(E1)  : A1*E*exp(-B1/E)
  * Band2Band(E1_5): A1_5*E^1.5*exp(-B1_5/E)
  * Band2Band(E2)  : A2*E^2*exp(-B2/E)
        A1      = 1.1000e+27  # [1/cm/sec/V]
        B1      = 2.1300e+07  # [V/cm]
        A1_5    = 1.9000e+24  # [1/cm/sec/V^1.5]
        B1_5    = 2.1900e+07  # [V/cm]
        A2      = 3.5000e+21  # [1/cm/sec/V^2]
        B2      = 2.2500e+07  # [V/cm]

  * Hurkx model for the following keywords in input file:
  * Band2Band(Hurkx)  : -Agen*D*(E/E0)^Pgen*exp(-Bgen*(Eg/Eg300)^1.5/E)
if D < 0
  *                -Arec*D*(E/E0)^Prec*exp(-Brec*(Eg/Eg300)^1.5/E) if D > 0
  *                D = (n*p-ni^2)/(n+ni)/(p+ni)*(1-|alpha|)+alpha, E0 = 1 V/cm
  *                So, if alpha = 0, it's original Hurkx model,
  *                   if alpha = -1, it's only generation,
  *                   if alpha = +1, it's only recombination.
        Agen    = 3.5000e+21  # [1/cm^3/sec]
        Bgen    = 2.2500e+07  # [V/cm]
        Pgen    = 2       # [1]
        Arec    = 3.5000e+21  # [1/cm^3/sec]
        Brec    = 2.2500e+07  # [V/cm]
        Prec    = 2       # [1]
        alpha   = 0.0000e+00  # [1]
  * nonlocal B2B models for the following keywords in command file:
  * Band2Band(Model=NonlocalPath1) : Nonlocal B2B tunneling with single
transition process   using the first tunneling path
  * Band2Band(Model=NonlocalPath2) : Nonlocal B2B tunneling with two
transition processes using the first and second tunneling paths
```

```
  * Band2Band(Model=NonlocalPath3) : Nonlocal B2B tunneling with three
transition processes using the all three tunneling paths
  * For the i-th nonlocal B2B process (i=1, 2, or 3):
  * Apathi : Prefactor Ad or Ap in the uniform field limit for the direct or indirect
tunneling
  * Bpathi : Exponent  Bd or Bp in the uniform field limit for the direct or indirect
tunneling
  * Dpathi : The conduction band offset D
  * Ppathi : The phonon energy P
  *         Note that the indirect tunneling process is assumed if P>0, and the direct
tunneling process is assumed if P=0
  * Rpathi : The ratio mv/mc. If Rpathi=0, it is automatically determined by
  *         mv/mc = (1 + 2*mr)/(1 - 2*mr)
  *         where mr=mc*mv/(mc+mv) is the reduced mass
  * In the uniform field limit, the generation rate can be expressed by
  * G = A * (F/F0)^2   * Exp(-B/F) for   direct tunneling
  *   = A * (F/F0)^2.5 * Exp(-B/F) for indirect tunneling
  * where
  * Ad = g * mr^0.5 * qF0^2 / (36 * pi * h_bar^2 *E_T^0.5)
  * Ap = g *(mc*mv)^1.5 * (1+2*N) * qF0^2.5 * Dop^2 / (2^7.75 * pi^2.5 *
h_bar^2.5 * mr^1.25 * E_T^1.75 * rho * P)
  * Bd = pi    * mr^0.5 * E_T^1.5 / (2 * h_bar * q)
  * Bp = 2^2.5 * mr^0.5 * E_T^1.5 / (3 * h_bar * q)
  * F0 = 1 V/cm, qF0 = 1 eV/cm, E_T = E_G + D
  * From the above expression, the microscopic parameters such as mr, mc, and
mv for the nonlocal B2B model are extracted internally
        Apath1 = 4.0000e+14  # [1/cm^3/sec]
        Bpath1 = 1.9000e+07  # [V/cm]
        Dpath1 = 0.0000e+00  # [eV]
        Ppath1 = 0.037       # [eV]
        Rpath1 = 0.0000e+00  # [1]
        Apath2 = 0.0000e+00  # [1/cm^3/sec]
        Bpath2 = 0.0000e+00  # [V/cm]
        Dpath2 = 0.0000e+00  # [eV]
        Ppath2 = 0.0000e+00  # [eV]
        Rpath2 = 0.0000e+00  # [1]
        Apath3 = 0.0000e+00  # [1/cm^3/sec]
        Bpath3 = 0.0000e+00  # [V/cm]
        Dpath3 = 0.0000e+00  # [eV]
        Ppath3 = 0.0000e+00  # [eV]
        Rpath3 = 0.0000e+00  # [1]
```

```
        MaxTunnelLength      = 1.0000e-05   # [cm]
  * min length to interfaces (for traditional & Hurkx models):
        dDist   = 5.0e-08        # [cm]
  * min potential difference on length dPot/E (for traditional & Hurkx models):
        dPot    = 0.0000e+00  # [V]
  * numeric smoothing
        MinField        = 0.0000e+00  # [V/cm]
        MinGradQF    = 0.0000e+00  # [eV/cm]
        DenCorRef     = 0.0000e+00 ,          0.0000e+00     # [cm^-3]
}
BarrierTunneling
{ * Non Local Barrier Tunneling
  * G(r) = g*A*T/kB*F(r)*Pt(r)*ln[(1+exp((E(r)-Es)/kB/T))/(1+exp((E(r)-
Em)/kB/T))]
  * where:
  *     Pt(r) is WKB approximation for the tunneling probability
  *     g = As/A, As is the Richardson constant for carriers in semiconductor
  *     A is the Richardson constant for free electrons
  *     F(r) is the electric field
  *     E(r) is carrier energy
  *     Es is carrier quasi fermi energy in semiconductor
  *     Em is carrier fermi energy in metal
  *     alpha is the prefactor for quantum potential correction
  *     eoffset and hoffset are lists of band offsets
        g          = 0.45767 ,     0.389   # [1]
        mt         = 0.041e+00 , 0.4e+00          # [1]
        alpha    = 0.0000e+00 ,          0.0000e+00     # [1]
        eoffset = () # eV
        hoffset = () # eV
}
SchottkyResistance
{ * Schottky resistance parameters
  * Rsch = Rinf*(300/T)*exp(q*PhiB/E0)
  * where:
  *     PhiB is the Schottky potential barrier
  *     Rinf is the Schottky resistance for an infinite doping concentration
  *     E0 = E00*cosh(E00/kT), E00 = (qh/4pi)*(N/eps/mt)^0.5
  *     N is the doping concentration at the contact
  *     T is the device temperature (defined in Physics section)
  *     eps is the semiconductor permitivity
  *     mt is the tunneling mass
```

```
        Rinf    = 2.4000e-09 , 5.2000e-09     # [Ohm*cm^2]
        PhiB    = 0.6 ,  0.51    # [eV]
        mt      = 0.041 ,        0.4      # [1]
}
DirectTunnelling
{ * eps_ins:   insulator dielectricity,
  * E_F_M:     metal Fermi energy,
  * m_M:       metal effective mass,
  * m_ins:     insulator effective mass,
  * m_s:       semiconductor effective mass,
  * m_dos:     semiconductor DOS effective mass,
  * E_barrier: height of barrier between semiconductor and oxide,
  * E_i:       energy nodes for pseudo barrier,
  * See the manual for more details.
        eps_ins         = 2.13  # [1]
        E_F_M           = 11.7  # [eV]
        m_M     = 1     # [m0]
        m_ins   = 0.5 ,  0.77    # [m0]
        m_s     = 0.19 ,         0.16    # [m0]
        m_dos = 0.32 ,           0.0000e+00    # [m0]
        E_barrier       = 3.15 ,         4.73    # [eV]
        E0      = 0.0000e+00 ,           0.0000e+00    # [eV]
        E1      = 0.0000e+00 ,           0.0000e+00    # [eV]
        E2      = 0.0000e+00 ,           0.0000e+00    # [eV]
}
RadiativeRecombination * coefficients:
{ * R_Radiative = C * (T/Tpar)^alpha * (n p - ni_eff^2)
  * C
  * alpha
        C       = 0.0000e+00  # [cm^3/s]
        alpha   = 0.0000e+00  # []
}
BarrierLowering
{ * dB = a1 * ( (E/E0)^p1 - (Eeq/E0)^p1_eq ) +
  *      a2 * ( (E/E0)^p2 - (Eeq/E0)^p2_eq ),
  * where E is the electric field [V/cm],
  *       Eeq is the electric field at equilibrium (zero bias),
  *       E0 = 1 V/cm.
        a1      = 2.6000e-04   # [eV]
        p1      = 0.5    # [1]
        p1_eq   = 0.5    # [1]
```

```
        a2      = 0.0000e+00  # [eV]
        p2      = 1       # [1]
        p2_eq   = 1       # [1]
}
LatticeParameters
{ * Crystal system, elasticity, and deformation potential are defined.
  * X and Y vectors define the simulation coordinate system relative to the
  * crystal orientation system. Also there is an option to represent the crystal
  * system relative to the simulation one. In this case a keyword CrystalAxis
  * has to be in this section and X and Y vectors will represent [100] and [010]
  * axis of the crystal system in the simulation one.
  * Additional notes: 1 Pa = 10 dyn/cm^2; tensile stress/strain is positive.
  *
  * S[i][j] - elasticity modulus; i,j = 1,2,...6 and j>=i.
  * CrystalSystem is symmetry, used ONLY to define the elasticity matrics.
  *   Cubic (CrystalSystem=0): S[1][1],S[1][2],S[4][4]
  *   Hexagonal (CrystalSystem=1): S[1][1],S[1][2],S[1][3],S[3][3],S[4][4]
  * NC is a number of conduction band levels taken into account
  * NV is a number of valence band levels taken into account
  * DC2(l) defines deformation potentials for conduction subband = l
  * DV2(l) defines deformation potentials for valence subband = l
  * The subband energy shift due to strain (E) is equal to the following sum:
  * D2[1]*E11 + D2[2]*E22 + D2[3]*E33 +
  * D2[4]*(0.5*D2[5]^2*((E11-E22)^2+(E22-E33)^2+(E33-
E11)^2)+D2[6]^2*(E23^2+E13^2+E12^2))
  *
        X       = (1, 0.0000e+00, 0.0000e+00) #[1]
        Y       = (0.0000e+00, 1, 0.0000e+00) #[1]
        S[1][1] = 0.77  # [1e-12 cm^2/din]
        S[1][2] = -2.1000e-01 # [1e-12 cm^2/din]
        S[4][4] = 1.25  # [1e-12 cm^2/din]
        CrystalSystem = 0       # [1]
        NC      = 3       # [1]
        NV      = 2       # [1]
        DC2(1)          = 0.9, -8.6000e+00, -8.6000e+00, 0.0000e+00,
0.0000e+00, 0.0000e+00       #[eV]
        DC2(2)          = -8.6000e+00, 0.9, -8.6000e+00, 0.0000e+00,
0.0000e+00, 0.0000e+00       #[eV]
        DC2(3)          = -8.6000e+00, -8.6000e+00, 0.9, 0.0000e+00,
0.0000e+00, 0.0000e+00       #[eV]
```

```
        DV2(1)          = -2.1000e+00, -2.1000e+00, -2.1000e+00, -1.0000e+00,
0.5, 4  #[eV]
        DV2(2)          = -2.1000e+00, -2.1000e+00, -2.1000e+00, 1, 0.5, 4 #[eV]
 * Deformation potentials of k.p model for electron bands
        xis     = 7     # [eV]
        dbs     = 0.53  # [eV]
        xiu     = 9.16  # [eV]
        xid     = 0.77  # [eV]
 * Deformation potentials of k.p model for hole bands
        adp     = 2.1   # [eV]
        bdp     = -2.3300e+00# [eV]
        ddp     = -4.7500e+00# [eV]
        dso     = 0.044         # [eV]
 * Luttinger parameters and Sverdlov's k.p theory parameter
        gamma_1         = 4.27  # [1]
        gamma_2         = 0.315         # [1]
        gamma_3         = 1.4576        # [1]
        Mkp     = 1.2   # [1]
}
}
Region = "metal1" {
        Bandgap {
                WorkFunction = 4.79606
                Chi0 = 4.79606
        }
}
Region = "metal2" {
        Bandgap {
                WorkFunction = 4.79606
                Chi0 = 4.79606
        }
}
Region = "metal3" {
        Bandgap {
                WorkFunction = 4.79606
                Chi0 = 4.79606
        }
}
Region = "metal4" {
        Bandgap {
                WorkFunction = 4.79606
```

```
                Chi0 = 4.79606
        }
}
Region = "metal5" {
        Bandgap {
                WorkFunction = 4.79606
                Chi0 = 4.79606
        }
}
Region ="n_plus1" {
#Material = "InGaAs" {
        BarrierTunneling {
                mt = 0.0286175 , 0.425
                g = 0.03 , 0.4244
        }
}
Region ="n_plus2" {
        BarrierTunneling {
                mt = 0.0286175 , 0.425
                g = 0.03 , 0.4244
        }
}
Region ="barrier1" {
#Material = "InGaAs" {
        BarrierTunneling {
                mt = 0.05452 , 0.49
                g = 0.05825 , 0.4702
        }
}
Materials {
        GaAsSb {
                label = "GaAsSb"
                group = Semiconductor
                color = #ffb6c1
        }
}
# End Parameter File


# Simulation File
File {
```

```
        * input files:
        Grid     = "tunnelmos.tdr"
        Parameters = "input_gasb.par"
        * output files:
        Plot     = "vr_nfet_2nm_idvg.tdr"
        Current = "vr_nfet_2nm_idvg.plt"
        Output  = "vr_nfet_2nm_idvg.log"
        Bandstructure = "bandfile_vr_nfet_2nm_idvg"
}
Electrode {
        { Name="source1" Voltage=0.0 Barrier=0.0}
        { Name="source2" Voltage=0.0 Barrier=0.0}
        { Name="drain"  Voltage=0.075 Barrier=0.0}
        { Name="gate1"   Voltage=-0.04 Barrier=0.0}
        { Name="gate2"   Voltage=-0.04 Barrier=0.0}
}
Physics {
        Fermi
        EffectiveIntrinsicDensity(NoBandGapNarrowing)
}
Physics (MaterialInterface="InGaAs/InGaAs") {
        Thermionic
        Recombination(SRH eBarrierTunneling(Band2Band TwoBand))
        Recombination(SRH hBarrierTunneling(Band2Band TwoBand))
}
Physics (MaterialInterface="InGaAs/GaAsSb") {
        Thermionic
        Recombination(SRH hBarrierTunneling(Band2Band TwoBand))
        Recombination(SRH eBarrierTunneling(Band2Band TwoBand))
}
Physics (Region = "barrier1") {
        MoleFraction (xFraction=0.8, yFraction=0.2)
}
Physics (Region = "n_plus1") {
        MoleFraction (xFraction=0.15, yFraction=0.85)
}
Physics (Region = "n_plus2") {
        MoleFraction (xFraction=0.15, yFraction=0.85)
}
Plot {
        eDensity hDensity eCurrent hCurrent Band2Band ConductionCurrent
```

```
        ElectronAffinity NonLocal
        Current TotalRecombination eBand2BandGeneration
hBand2BandGeneration
        Potential SpaceCharge ElectricField
        eBarrierTunneling hBarrierTunneling
        eMobility hMobility eVelocity hVelocity
        Doping DonorConcentration AcceptorConcentration
        ConductionBandEnergy ValenceBandEnergy
}
Math(MaterialInterface="InGaAs/InGaAs") {
        Digits(NonLocal)=3
        EnergyResolution(NonLocal)=0.001
        Nonlocal(Length=4e-7)
}
Math(MaterialInterface="InGaAs/GaAsSb") {
        Digits(NonLocal)=3
        EnergyResolution(NonLocal)=0.001
        Nonlocal(Length=4e-7)
}
Math {
        CNormPrint
        NewtonPlot (Error)
        Extrapolate
        RelErrControl
}
Solve {
        Poisson
        Coupled { Poisson Electron Hole }
        Quasistationary ( MaxStep=0.008,
                PlotBandstructure {range=(0,1) intervals=3}
                Goal{ Name="gate1" Voltage=0.085 }
                Goal{ Name="gate2" Voltage=0.085 }
        )
                {
                        Coupled { Poisson Electron Hole } }
        }
```

 # End Simulation File

GLOSSARY

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TFET	Tunneling Field Effect Transistor
CNFET	Carbon Nano-tube Field Effect Transistor
HETTFET	Hetero-barrier Tunnel Field Effect Transistor
JFET	Junction Field Effect Transistor
SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory

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VITA

Mohammad Mehedi Hasan attended Mirzapur Cadet College, Tangail, Bangladesh for his secondary and higher secondary education. He was placed 11th on the Combined Merit List of Dhaka board in National Secondary School Certificate (S.S.C) examination, 1996, and was placed 6th on the Combined Merit List of Dhaka board in National Higher Secondary Certificate (H.S.C) examination, 1998. He completed his Bachelor's degree in Electrical Engineering (B.S.E.E) with Honors at the university in 2004 on Starr Foundation Scholarship, focusing on Circuit Design and Solid State Electronics. He then joined the Chemical Mechanical Polishing (CMP) division of Applied Materials where he worked on latest generation Reflexion, Reflexion LK, and ECMP tools. He was named a "Top Contributor" to the CMP Product Business Group efforts. He then joined the University of Texas at Austin once again as a graduate student in Electrical Engineering. There he earned his Master's degree in Electrical Engineering in 2007. He is currently employed at Intel Corporation as a Senior Design Engineer, working on latest generation mobile products.

Permanent Address: House no. 996, Monipur, Mirpur-2, Dhaka 1216,
Bangladesh

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