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A BIST Circuit for Random Jitter Measurement

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A BIST Circuit for Random Jitter Measurement

by

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Dedicated to Yu Jeong, Seong Hyuk, and our parents.
Jitter is a dominant factor contributing to a high bit error rate (BER) in high speed I/O circuitry, and it aggravates the quality of a clock signal from a phase-locked loop (PLL), subsequently impacting a given timing budget. The recent proliferation of systems-on-a-chip (SoCs) with help of technology scaling makes jitter measurement more challenging as the SoCs integrate more I/O circuitry and PLLs within a chip. Jitter has been, however, one of the most difficult parameters to measure accurately when validating the high speed serial I/O circuitry or PLLs, mostly due to its small value.

External instruments with full-fledged high precision measurement hardware, along with comprehensive analysis tools, have been used for jitter measurement, but increased test cost from long test time, signal integrity, and human intervention prevent this approach from being used for high volume manufacturing testing. Built-in self-test (BIST) solutions have recently become attractive to overcome these drawbacks, but complicated analog circuit designs that are sensitive to ever increasing process variations, and associated complex analysis methods impede their adoption in the SoCs.
This dissertation studies practical random jitter measurement methods that achieve measurement accuracy by exploiting a differential approach and make the proposed methods tester-friendly solutions for an automatic test equipment (ATE). We first propose a method of measuring the average value of the random jitter, rather than measuring the jitter at every clock cycle, that can be converted to the root-mean-square (RMS) value of the random jitter, which is the key indicator of the quantity of the random jitter. Then, we propose a simple but accurate delay measurement method which uses the proposed jitter measurement method for random jitter measurement when a reference signal, such as a golden PLL output in high speed I/O validation, is not available. The validity of the proposed random jitter measurement method is supported by measurement results from a test chip. The impact of substrate noise on the signal of interest is also shown with measurements using a test chip. To address the random jitter of a clock signal when the clock is operating in its functional mode, we demonstrate a novel method for random jitter measurement that explores the shmoo capability of a low-cost production tester without relying on any BIST circuitry.
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Chapter 1

Introduction

This chapter provides an overview of jitter and various approaches to jitter measurement. Advantages and disadvantages of the previous jitter measurement methods for built-in self-test (BIST) circuits and external equipment are also presented. These are two major approaches to jitter measurement.

1.1 Overview of Jitter

Jitter is defined as timing uncertainties of digital signals, including clock signals, at their intended ideal positions in time, and it can be interpreted as a phase noise in a frequency domain. Since there are many sources that introduce jitter to the digital signals, various jitter components are defined based on their sources, and aggregate jitter components are referred to as total jitter (TJ). Figure 1.1 shows the subcomponents of total jitter.

Total jitter is decomposed into deterministic jitter (DJ) and random jitter (RJ), and DJ is further divided into other jitter components such as periodic jitter (PJ) and data-dependent jitter (DDJ) [52]. Random jitter comes from device noise sources such as thermal noise and flicker noise. Power supply noise and substrate noise can also induce random jitter to the signal of
interest. Recent CMOS technologies favor a heavily-doped P+ substrate to reduce latch-up susceptibility. However, the low resistivity in the substrate creates undesired signal paths between devices that can corrupt sensitive signals by varying the $V_{th}$ of devices [59]. This $V_{th}$ modulation can result in timing uncertainties in the signal of interest. Because of its source, random jitter is unbounded, and it follows a Gaussian distribution that represents its probability density function (PDF). The standard deviation of the distribution is used to quantify the random jitter. Figure 1.2 shows an example of a histogram that reflects the PDF of random jitter measured from a clock signal with a sample size of 10K hits, and Figure 1.3 shows another histogram for the same random jitter, but with a sample size of 300K hits. In both cases, the standard deviation values are similar to each other, showing around 64\,\text{ps}, but their peak-to-peak jitter values are quite different: 419\,\text{ps} from 10K hits and 550\,\text{ps} from 300K hits.
The distribution of random jitter, \( RJ(x) \), can be defined as

\[
RJ(x) = \frac{1}{\sigma \sqrt{2\pi}} e^{\frac{-x^2}{2\sigma^2}}
\]  

(1.1)

when the standard deviation of random jitter is \( \sigma \). When multiple random jitter sources exist, since sources of random jitter are uncorrelated with each other, the resulting variance of the random jitter can be expressed as the sum of all individual variances as follows

\[
RJ_{Total} \approx \sqrt{RJ_{1RMS}^2 + RJ_{2RMS}^2 + \cdots + RJ_{N_{RMS}}^2}
\]

(1.2)

where \( RJ_{N_{RMS}} \) represents the root-mean-square (RMS) value of the \( N_{th} \) random jitter component.

Deterministic jitter is composed of several different components, unlike random jitter. Periodic jitter is a periodic variation of a signal edge position over time, and is also called sinusoidal jitter. Data-dependent jitter is correlated to the bit pattern transmitted on a communication link under test. It is usually caused by the low-pass filter characteristic of the cable used for transmitting the bit pattern, and becomes severe when a bit 0 is transmitted after a
long sequence of 1s or vice versa. The duty-cycle distortion (DCD) represents jitter where a signal has unequal pulse widths for high and low logic values, and it can be caused by a voltage offset between differential inputs or the difference between signal’s rising and falling times. The inter-symbol interference (ISI) is jitter that depends on the transmitted patterns, and is caused by bandwidth limitation, nonlinear phase response of the transmission media, and reflections [52]. This interference requires the use of a pre-emphasis or a de-emphasis circuit at a transmitter side and the use of an equalizer circuit at a receiver side. Encoding schemes such as 8b/10b also help in reducing this jitter component. Bounded uncorrelated jitter (BUJ) can come from electromagnetic interference, but it mainly comes from crosstalk [44].

All deterministic jitter components are bounded, and thus they can be quantified in their peak-to-peak values. Unlike random jitter, each deterministic jitter component can be correlated with each other depending on its source, and its peak-to-peak value does not increase with a larger sample size. The peak-to-peak value of deterministic jitter is at most the sum of individual peak-to-peak values of its components [2].

\[
DJ_{Total_{pp}} \leq DJ_{1_{pp}} + DJ_{2_{pp}} + \cdots + DJ_{N_{pp}} \tag{1.3}
\]

where \( DJ_{N_{pp}} \) represents the peak-to-peak value of the \( N_{th} \) deterministic jitter component.

Total jitter is the convolution of random jitter and deterministic jitter, or more exactly the convolution of the PDFs of those two jitter components [2],
as shown in (1.4).

\[ TJ(x) = R J_{Total}(x) \ast D J_{Total_{pp}}(x) \]  \hfill (1.4)

With the distribution of random jitter in (1.1), total jitter in (1.4) can be expressed as

\[ TJ(x) = \frac{1}{\sigma \sqrt{2\pi}} \int D J_{Total_{pp}}(x') \exp \left[ -\frac{(x - x')^2}{2\sigma^2} \right] dx' \]  \hfill (1.5)

where it is assumed that there is only one random jitter component. Among all aforementioned jitter components, this dissertation mainly focuses on the measurement of random jitter.

1.2 Effect of Jitter on System Behavior

Jitter is usually an undesired factor in the design of phase-locked loops (PLLs) or I/O circuitry except very rare cases such as the work published in [5, 6, 23], in which random jitter from the PLL output or in clock signals is actively used in generating true random numbers. In microprocessors or systems-on-a-chip (SoCs), clock signals are used for a timing or synchronizing purpose, but jitter in the PLL output clock undermines a given timing budget, along with clock skews. In critical paths, large random jitter manifests itself as a setup time violation.

The loop filter in the PLL can reduce jitter, or phase noise, in its reference clock due to its low pass transfer function, but the loop filter acts as a high pass filter to the voltage-controlled oscillator (VCO) noise of the
PLL. Figure 1.4 shows the phase noise in an oscillator [7, 43], where the main contributors to the phase noise are $1/f$ noise and thermal noise, and the phase noise is represented as a single-sideband noise spectral density. As shown in Figure 1.5, the PLL loop filter can filter a high frequency component of the input reference clock noise and a low frequency component of the VCO noise, but the loop filter passes a low frequency component of the input reference noise and a high frequency component of the VCO noise, resulting in the total
phase noise at the output of the PLL. It is difficult to correct this type of phase noise, or jitter, although the clock skews in a clock distribution tree can be minimized by adjusting variable delay lines if they are implemented to correct skews [24].

Jitter is also the major source of the bit error rate (BER) in I/O circuitry, and limits the maximum I/O operating speed in most serial high speed I/Os such as serializer-deserializer (SERDES), serial ATA (SATA), etc. To calculate the BER in I/O eye-margining test, the following equation is used to obtain total jitter [63].

\[ TJ \approx \alpha \cdot RJ_{rms} + DJ_{pp} \] (1.6)

where \( DJ_{pp} \) represents the peak-to-peak value of deterministic jitter after convolution in (1.4), and \( \alpha \) is determined by a complementary error function as shown in (1.7).

\[ BER = \frac{1}{2}erfc\left(\frac{\alpha}{\sqrt{2}}\right) \] (1.7)

For the BER of \( 10^{-12} \), which is commonly used for high speed I/O testing, \( \alpha \) becomes 14.069. When the \( RJ_{rms} \) value is too large to meet the given BER specification, the test can fail: eye is completely closed in the eye-margining test. However, jitter has been one of the most difficult parameters to measure accurately when validating high speed I/Os. Due to the small value of jitter, i.e., from several picoseconds to tens of picoseconds in high speed clock signals, measuring it has always been an issue for test engineers as well as circuit designers. Increasing requirements in the signal integrity of signal communi-
cations, BER of $10^{-15}$ for instance, require a very long test time to obtain statistically meaningful measurement results even in Gbps I/Os. High resolution is also essential in measuring jitter, often requiring picosecond resolution.

1.3 Prior Work Aimed at Jitter Measurement

Various research has addressed jitter measurement and testing, and two major approaches are a BIST-based approach and a method using external bench testers. The BIST-based approach came from time interval measurement techniques, which have a long history and wide applications including nuclear science [55]. The BIST-based approaches can be categorized, in general, into a time-to-digital conversion technique utilizing an analog-to-digital converter (ADC) to convert a measured voltage into digital values, time interval measurement techniques utilizing the Vernier principle for higher resolution, and counter-based time interval measurement techniques [22, 70], as follows.

- Under-sampling/beat-frequency method [19, 30, 64, 65]
- Vernier oscillator method [66, 71]
- Time-to-digital conversion using a charge-pump [31–33, 46]
- RMS measurement using a probability density function [9, 27, 29, 62]
- Time-to-digital conversion using an ADC [15, 16]
Although many of those methods originated from time interval measurement, they were modified to address the small amount of jitter to be measured. The majority of those methods capture and measure jitter at every clock cycle, and use them to do further analysis in order to obtain the RMS value of jitter or its peak-to-peak value.

When external instruments or equipment are used for jitter testing or jitter measurement, commonly used are a spectrum analyzer, a real-time or equivalent-time sampling oscilloscope, a time interval analyzer, a BER tester, or dedicated jitter testing equipment. Sophisticated jitter analysis software is often used in conjunction with them. For random jitter measurement, commercially available solutions include time interval measurement for high-speed I/O testing, the Tail-fitting algorithm [45], and frequency-domain analysis. Frequency-domain analysis utilizes the frequency spectrum of the signal of interest, and it is most useful in decomposing deterministic jitter components from total jitter. In this approach, the RMS value of random jitter can also be determined by integrating noise floor over the frequency range of interest, as shown in (1.8), after removing deterministic jitter components.

\[
RJ_{RMS} = \int_{f_L}^{f_H} S(f)df
\]

(1.8)

where \(S(f)\) represents the spectral density of random jitter. This method can provide good measurement resolution, but requires high bandwidth along with complex algorithm to remove deterministic jitter components, which are not suitable to the BIST-based approach.
1.3.1 BIST-based Approach

![BIST circuit](image)

Figure 1.6: A BIST circuit for jitter measurement using an under-sampling method [19, 30, 64, 65]

The under-sampling method, as shown in Figure 1.6, utilizes the same principle as the equivalent-time sampling oscilloscope in jitter measurement to enhance its measurement resolution up to 1 picosecond from one gate delay. To make this method work properly, a coherence sampling technique is used which requires the relationship of $F_D \neq NF_S$ [30]. The output of the measurement usually comes at the form of the cumulative distribution function (CDF), from which the corresponding PDF is extracted to estimate the RMS value of random jitter. This type of method requires a separate clean sampling clock ($F_S$) for accurate measurement since there is no way of compensating jitter in the sampling clock. This method also requires another step of analysis when there is deterministic jitter in the signal of interest.

The method shown in Figure 1.7 utilizes the PDF or the CDF constructed from the output of the BIST circuitry to estimate the RMS value of random jitter in the signal under test (SUT) since random jitter follows a Gaussian distribution. In estimating the amount of jitter, $-d$ in (1.9), an inverse CDF table is required to find the value of $-d$ from the $CDF_{Edge}$ [29]. This type of method does not require a separate reference signal, but usually
does not consider jitter at the other clock edge (the falling edge in S2) that is used as a reference, thus resulting in measurement errors.

$$p = \int_{-\infty}^{-d} PDF_{Edge}(t)dt = CDF_{Edge}(-d)$$  \hspace{1cm} (1.9)

The time-to-digital conversion method using a charge-pump is another approach for jitter measurement to enhance measurement resolution while not skipping many samples, unlike the under-sampling method. Figure 1.8 depicts one example of this method, where jitter at every \textit{Nth} clock cycle is measured using multiple flash-type analog-to-digital converters. Each of the \textit{Nth} clock edges is generated by a clock divider inside the \textit{Control Signal Generator} in Figure 1.8.

The jitter measurement method shown in Figure 1.9 combines the pre-
Figure 1.8: A BIST circuit for jitter measurement using a time-to-digital conversion method [46]

Previous two methods described in Figure 1.7 and Figure 1.8. To generate the delayed version (DCLK) of the reference clock (CLK) by the amount of the period of CLK, an adjustable delay line controlled by the Delay Controller is used. The jitter of interest manifests itself as a phase difference that subsequently controls the charge pump. The $V_{out}$ is measured with an off-chip probe to estimate the jitter value. The Phase Frequency Detector was later replaced with an XOR gate in [31].

Using the Vernier principle to enhance measurement resolution is one popular approach in the time-to-digital conversion area, and this method is also used in jitter measurement, as shown in Figure 1.10. To reduce silicon area consumed by the BIST circuitry, the Vernier delay line is often replaced with Vernier ring oscillators [13, 14, 66], where course measurement and fine measurement are combined to save testing time taken for measurement. To further improve measurement resolution, time amplifying circuitry can be used.
Figure 1.9: A jitter measurement method using a time-to-voltage conversion method [31–33, 72]

Figure 1.10: A BIST circuit for jitter measurement using the Vernier principle [35]

whose output is fed to the measurement circuit using the Vernier principle, as shown in Figure 1.11.

To generate a reference clock in the method shown in Figure 1.11, a self-referred clock generator is commonly used to generate the delayed version of the reference clock by an exact period, where a delay-locked loop (DLL) [17, 58] or inverters with capacitors in-between for fine tuning [13, 14] is a popular choice, but this method aims at jitter measurement for the clock of a fixed
Jitter amplification is also an active research area to enhance jitter measurement resolution. Most research related to jitter amplification uses analog circuits, such as an ADC [15] or an analog modulator [16], or exploits the behavior of metastability [14]. To address non-linearity in the amplification, those techniques require careful calibration steps. Recently, a jitter amplification method using only digital logic was proposed, in which switching from a fast signal path to a slow signal path occurs when triggered by a lagged signal due to jitter, thus leading to an increased buffer delay proportional to the amount of jitter in the reference signal [5, 6]. The jitter amplification gain in this method showed strong process and temperature dependencies since it operates in a very narrow linear region.

1.3.2 Challenges in Random Jitter Measurement

The approach using external bench testers has been widely used in jitter testing since it gives reliable and repeatable measurements without being
affected by environmental variation such as temperature. It also provides various analysis tools for post-processing. For random jitter measurement, the spectrum analyzer can measure jitter with sub-picosecond resolution by integrating noise floor in a frequency domain, as shown in (1.8), and by converting it into the RMS value of random jitter. As such, BIST circuits for random jitter measurement cannot completely replace the external instrument such as the spectrum analyzer in the foreseeable future when very accurate timing parameter measurement is required. With respect to measurement resolution in the BIST-based approach, 1ps resolution jitter measurement was proposed [34, 50], but the circuit is too large and complicated to use in common applications [50].

Although external bench testers offer the best measurement result in terms of accuracy and resolution, those benefits come at the cost of a long test time as well as human intervention, but cost-effective solutions and time-to-market are more preferred than ever with the current proliferation of SoCs. Moreover, another issue in using those external testers is degraded signal integrity caused by parasitic components in a probe or a package pin, or by the limited bandwidth of the package pin. For instance, jitter coming out of an output pin may not represent the actual jitter value seen by internal logic due to the limited bandwidth of the pin used for measurement. In other words, when the bandwidth, or the maximum attainable rising time, of the output pin is comparable to the rising time of the jittery signal inside a device under test (DUT), the measured jitter value using an oscilloscope will not be the same as the actual jitter value even if the oscilloscope is an ideal one [48]. Another
thing to consider here is the accessibility to the signal of interest. For example, when random jitter at the end-point of a clock distribution tree needs to be measured, the method using external bench instrument has no way to access that node for jitter measurement. Using high-bandwidth buffers and output pins degrade the signal of interest in any case.

When a jitter measurement solution is implemented inside an automatic test equipment (ATE), it can be effective since the solution can be used repeatedly for measurement or testing, and a valuable silicon area consumed by BIST circuitry can be used for other useful functional blocks. In addition, the ATE can provide repeatability that is crucial in high-volume manufacturing testing since it directly relates to deterministic testing results. However, the degraded signal integrity caused by parasitic components from a load board used with the ATE is still an issue. The overall timing accuracy (OTA) is another factor of the degraded signal integrity when the ATE is used. Budget ATEs show ±100ps for the edge placement accuracy (EPA), and even a state-of-the-art per-pin module for the ATE specifies ±30ps for the EPA [67].

On the other hand, the BIST-based approach can overcome aforementioned signal integrity issues by just placing dedicated test circuitry near the SUT, and then by just measuring it. Therefore, the signal degradation and accessibility issues are not applicable to the BIST-based approach for jitter measurement. The capability of self testing and parallel testing is another advantage of the BIST approach, and jitter testing or measurement for multiple PLLs or multiple high speed I/Os in a target SoC can benefit from this.
capability. As a result, BIST solutions are now becoming more attractive over the bench tester.

However, measurement reliability, measurement accuracy, and achievable resolution are still issues in the BIST-based approach, and they prohibit many proposed BIST solutions from being widely adopted in the industry. Process variations, which become more severe as technology advances to a smaller feature size, can degrade measurement accuracy as well as the measurement reliability, thus hampering a wide adoption of the BIST solutions. Recently, one BIST approach was demonstrated using a test chip for PLL production testing [40], but some of proposed BIST solutions target Go/No-Go testing [9, 28], rather than parametric testing.

Area overhead is another concern in the BIST-based approach. To achieve both a large measurement range and high resolution, the mixture of coarse measurement circuitry and fine measurement circuitry is commonly used [66], but increased area overhead is still inevitable in this type of circuitry. The fact that the increased silicon area for the BIST circuitry has a higher chance of being susceptible to manufacturing defects is another drawback of the BIST-based approach. If the BIST circuitry can greatly reduce post-silicon design validation time or high volume manufacturing test cost, however, the area used for the BIST circuitry can be justified.
1.4 Motivation

Many studies on BIST circuitry for jitter measurement aim at measuring jitter as accurately as possible every clock cycle, but these efforts can be too much of a burden to the BIST circuitry, and sometimes they are not necessary. For random jitter, which follows a Gaussian distribution, it is sufficient to measure, or to estimate, the correct value of its standard deviation since it quantifies random jitter. Therefore, directly measuring or estimating the RMS value of random jitter, rather than measuring the amount of jitter every clock cycle, will lead to a more practical solution, and this technique can be more easily implemented in BIST circuitry as a Design-for-Test (DFT) feature. Several jitter measurement techniques have been proposed that measure the RMS value of random jitter by using the under-sampling method or by constructing the PDF of random jitter. The measurement accuracy of these techniques depends on the number of bins as well as the sample size in the constructed histogram that is used for post-processing. For example, when the number of bins is fixed and not sufficient to accommodate all samples, the shape of the histogram does not represent the true distribution of random jitter, and measured jitter values are also affected. Thus, measuring the average value of random jitter and converting it into a corresponding RMS value can lead to more accurate measurement.

Most BIST solutions for jitter measurement only work for a dedicated frequency of input signal [13, 14, 27, 35, 64, 65, 72], while it is desirable to design a pragmatic BIST solution that is not confined to a single frequency of SUT. In
addition, when measuring a small quantity such as a timing uncertainty using analog circuitry, a differential approach can overcome the non-ideal behavior of analog circuitry better than complex circuit designs, which will be described in Chapter 2. Moreover, the differential approach can lead to better measurement accuracy.

As mentioned in the previous Section, neither the BIST-based approach nor the external instrument-based approach is a practical solution for high volume manufacturing jitter testing. The BIST circuitry for random jitter measurement does not need to be a self-complete solution by itself. In reality, most BIST-based jitter measurement solutions require an external tester or a device to read out measured results. Therefore, if an ATE that is commonly used for both design validation and high-volume manufacturing testing, can be used in conjunction with the BIST circuitry to generate required reliable signals and to perform calculations for post-processing, which are also common, the BIST circuitry for random jitter measurement can be simple without compromising its performance. In this way, the design for the BIST circuitry can be more easily ported from a product to another product and from a technology node to another technology node. The reduced area overhead for the BIST circuitry is another benefit of combining the BIST circuitry with the ATE, and thus the BIST circuitry can be less susceptible to manufacturing defects.
1.5 Organization of the Dissertation

In Chapter 2, we present a RMS estimation method for random jitter measurement using an AND operation and an OR operation, which can estimate random jitter over a wide clock frequency range. Since jitter in the clock is measured using a differential approach, the proposed method can measure a small random jitter value without relying on jitter amplification. Random jitter is first measured in its corresponding average voltage value, and the average value is then converted into an associated frequency value so that it can be easily measured without degrading its signal integrity. The frequency value can be also converted into digital values using a counter when needed. Using the relationship between the average jitter value and its probability density, the average jitter value is interpreted as a corresponding RMS value of the random jitter.

In Chapter 3, we describe the method of removing the requirement of a reference clock that was assumed to be available as an ideal jitter-free clean clock in Chapter 2. An adjustable delay line can be used to replace the reference clock by delaying the signal of interest, or a jittery clock, by the amount of the period of the jittery clock. The delayed amount, however, does not need to be an exact period of the clock since the resulting delay error can be compensated later as long as the delay can be measured accurately. For this, a delay measurement method using a shrinking clock signal with simple BIST circuitry is presented. The shrinking clock is generated by applying an AND operation to two clocks signals, which are provided by an external tester, whose
period difference is being utilized. Circuit-level simulation results support the validity of the proposed method on delay values ranging from 35\textit{ps} to 872\textit{ps} across process, temperature, and voltage variations. The measurement error for the delay line of 872\textit{ps} is less than 2\% even when timing uncertainties in the tester clock are considered.

In Chapter 4, we present the BIST circuit design of the proposed RMS estimation method in Chapter 2 in detail. Design considerations on a NAND gate and a NOR gate are the first topic in this chapter, followed by a way of using an inverter as a simple charge pump. Since the proposed method for jitter measurement exploits a differential approach, the inverter does not need to provide the same amount of charging and discharging currents, but its device ratio is used to set the proper operating point for a VCO. Then, the design of the VCO along with a voltage-to-current converter is described. The BIST circuit was validated using a 0.13\textit{\mu m} technology, and simulation results for various random jitter values over a wide range of an input clock frequency are demonstrated. For the fabrication of a test chip, the performance of the BIST circuit was validated again with a 0.18\textit{\mu m} technology.

In Chapter 5, we demonstrate measurement results from the test chip. The test chip comprises the random jitter measurement circuitry and a substrate noise injector. The test board design is first described, which includes jitter generation circuitry used for validating the test chip. Measurement results for various random jitter values are then presented, and error analysis on the measurement results when a periodic jitter component exists in the
injected jitter follows. The effect of substrate coupling noise on the signal of interest is also given with measurements using the substrate noise injector.

In Chapter 6, we present a novel method of indirectly measuring random jitter without the use of any dedicated jitter measurement circuitry. The method also considers the worst case random jitter that can be induced by power supply noise as well as substrate noise from digital logic blocks that use the clock of interest as a clock source. This method explores the shmoo capability of a low-cost production tester. For the validation of the proposed method, circuit-level simulation results are first shown, and measurement results from one of the latest SoC products using an ATE follow. The advantage and drawbacks of the proposed method along with possible future work for further improvement are also presented.
Chapter 2

The RMS Estimation Method using AND and OR Operations for Random Jitter Measurement

In this chapter, the RMS estimation method for random jitter measurement is presented, which uses an AND operation and an OR operation.

2.1 The Basic Idea

The jitter measurement method using the time-to-voltage conversion, as shown in Figure 1.9, was proven to measure periodic jitter with good linearity, but that method was not applicable to random jitter measurement because of finite conductance of charge pumps and capacitor leakage current [72]. The method also depends on accurate voltage measurement, which requires a careful signal routing effort for good signal quality, if the method is to be implemented as a BIST solution. Figure 2.1 depicts how the XOR operation on a jittery clock and a clean clock can extract the jitter components from the jittery clock. If a jittery clock is XORed with a clean, jitter-free, clock of the same period of $T$ as the jittery clock, the narrow output pulse widths represent the amount of jitter in the jittery clock. The timing differences re-
sulted from random jitter, or the narrow pulses as the output of the XOR, can be converted into a voltage, and can also be integrated into an average voltage ($V_{OUT}$) using a charge pump and a capacitor [33, 72]. When measuring periodic jitter, the converted voltage, $V_{OUT}$, shows a sinusoidal waveform whose frequency and amplitude represent the frequency of periodic jitter and the peak-to-peak value of period jitter, respectively [33, 72]. For random jitter, however, the $V_{OUT}$ will just fluctuate around its average value. Moreover, the frequency of the $V_{OUT}$ does not provide any meaningful information regarding random jitter.

If the narrow pulses in Figure 2.1 can be modulated into an average voltage that is proportional to the ratio of the average pulse width of the XOR output to the period $T$ of the clock, the average voltage can represent the average value of random jitter in the jittery clock, if not the RMS value of random jitter. The concept of this modulation is described in Figure 2.2. If the XOR gate can properly charge or discharge the capacitor connected to its output so that the voltage $V_{XOR}$ represents the ratio of the output pulse
width to the period, $T$, as shown in Figure 2.2, the $V_{XOR}$ will be given by

$$V_{XOR} = K_{MO}V_{dd} \frac{J_r + J_f}{T}$$  \hspace{1cm} (2.1)

where $K_{MO}$ is a modulation constant which will be explained later, $V_{dd}$ is the supplied voltage to the XOR gate, and $J_r$ and $J_f$ represent the jitter component at the rising edge and the jitter component at the falling edge, respectively. Note that there are two jitter components in one clock period in (2.1) although we are interested in only the jitter component at the rising edge. Assuming that both jitter components, $J_r$ and $J_f$, have the same value, the average jitter value can be obtained by

$$J_r \approx \frac{1}{2K_{MO}} \frac{V_{XOR}T}{V_{dd}}$$  \hspace{1cm} (2.2)
where the divisor 2 is used to remove the contribution from \( J_f \). In most cases, random jitter at the rising edge of the clock will have the same distribution as random jitter at the falling edge of the clock by its random nature, and thus the assumption that both \( J_r \) and \( J_f \) contribute to the voltage by the same amount can be justified.

However, considering the narrow pulse width from the XOR output as a result of the small timing difference, it is difficult to charge or to discharge the capacitor using the XOR output because charging and discharging processes in the CMOS circuit are strongly affected by the drive strength of current that sources charge to or sinks charge from the capacitor. In other words, the charging and discharging processes depend on a RC time constant if the behavior of the capacitor is symmetric for its charging and discharging. Here, the resistance corresponds to the \( R_{on} \) when either PMOS or NMOS is in its saturation region, and the capacitance is the sum of all capacitance at the capacitor node. When jitter to be measured has an extremely small value such as a couple of picoseconds, or tens of picoseconds, the XOR output may not even be able to make any transition due to the RC time constant. This can be resolved by implementing the XOR operation by utilizing the difference between an OR operation and an AND operation as shown in Figure 2.2 to subtract the result of an AND operation from that of an OR operation.

In Figure 2.2, the difference between the OR operation and the AND operation corresponds to the sum of \( J_r \) and \( J_f \), which is exactly the same output from the XOR operation. Consequently, the difference between \( V_{OR} \)
Figure 2.3: $V_C$ voltage dependency on current drive strength for the XOR gate from the OR operation and $V_{AND}$ from the AND operation will be the same as the $V_{XOR}$. This voltage difference will be used to measure the average value of, subsequently to estimate the RMS value of, random jitter since this voltage difference is modulated by the timing difference. Note that we always obtain a positive value, as a result, that varies around $1/2V_{dd}$ regardless of the order of the input sequence: both leading and lagging signals produce positive output voltages when the jittery clock signal is compared with the jitter-free reference clock. The (2.2) can be rewritten as follows.

$$J_r \approx \frac{1}{2K_{MO}} \frac{V_{OR} - V_{AND}}{V_{dd}} T$$

(2.3)

The beneficial effect of this property, using the difference of the OR operation and the AND operation to replace the XOR operation, arises from its differential nature. In Figure 2.3, when the output from the XOR gate drives a charge pump that charges a capacitor, the modulated $V_C$ voltage is
strongly dependent on the current drive strength of the charge pump since the change of voltage, $\Delta V$, is proportional to the driving current, $I$, in (2.4).

$$\Delta V = \frac{I}{C} \Delta T$$

(2.4)

where $C$ is the capacitance of the capacitor and $T$ is the time during which the charge pump charges the capacitor. Therefore, measurement results from the XOR gate are very susceptible to process variations. To make the driving current constant without being affected by process variations, a separate circuit for voltage bias generation, which usually uses the band-gap principle, is required. On the other hand, the proposed approach can maintain the same modulated $V_C$ voltage (the area of a parallelogram in Figure 2.4) regardless of the current drive strength since the $V_C$ voltage solely depends on the phase difference between two clock signals and the $V_{dd}$ as shown in Figure 2.4.

![Figure 2.4: $V_C$ voltage from the difference between the AND gate output and the OR gate output](image)

In addition, this differential approach is immune to the mismatch between the charging behavior and the discharging behavior of the capacitor,
thus making the divisor 2 in (2.3) more valid. The differential approach can also reduce measurement errors resulting from the capacitor leakage current and process variations such as the capacitance after fabrication. The circuit mismatch between the AND operation and the OR operation, however, can dominate the measurement error.

### 2.2 The Voltage-to-Frequency Conversion

![High-level schematic for the proposed random jitter estimation method](image)

Figure 2.5: A high-level schematic for the proposed random jitter estimation method

Figure 2.5 shows a high-level schematic for the proposed estimation method, where the $V_C$ voltage is converted into a frequency through a VCO.
A 2-input NOR gate and an inverter perform the OR operation, and a 2-input NAND gate and an inverter do the AND operation. By controlling the /OR signal, only one operation is enabled at a time since power is gated in the other operation. Although two inverters are tied together, there is no effect on the other operation but a small junction capacitance, which is much smaller than that of the capacitor connected to the inverter output, because their power is also gated by the /OR signal. Here, the inverter also plays a role of a simple charge pump since requirements on the current drive strength were much loosened as shown in Figure 2.4. More detailed explanations on the role of the inverters will be given later. Note that both PMOS and NMOS transistors are used for the power gating.

The capacitor voltage, $V_C$, varies with respect to the pulse width of the output from each operation. Unlike the XOR gate, where output will be zero when there is no jitter in the jittery clock, NOR and NAND gates will have output pulses with 50% duty cycle even if there is no jitter. This means that the $V_C$ will maintain its value around $V_{dd}/2$, and will fluctuate depending on how much the output pulse is modulated by random jitter.

For random jitter measurement, measuring jitter at every clock edge is not required unless deterministic jitter needs to be extracted. If random jitter is measured at every clock cycle, a histogram showing the distribution of random jitter from the measurements needs to be constructed to estimate the RMS value of random jitter, in most of cases with a separate analysis tool [13, 14, 35, 65].
In the proposed method, instead of measuring random jitter at every clock cycle, the average value of random jitter is measured by converting the modulated $V_C$ into a frequency value. In other words, the $V_C$ voltage, resulting from either AND or OR operation, is used to control the frequency of the VCO as shown in Figure 2.5 through a voltage-to-current converter.

![Transmit Response](image)

Figure 2.6: $V_{OR}$ and $V_{AND}$ voltages with and without random jitter

Figure 2.6 shows how $V_{OR}$ and $V_{AND}$ deviate in opposite directions by responding to random jitter in the jittery clock, when their nominal voltages are set to around 500mV for 50% duty cycle. Because the $V_C$ voltage varies at every clock edge due to random jitter, the VCO will also change its frequency according to the fluctuating $V_C$ voltage. The average voltage, however, will
be proportional to the RMS value of the random jitter, thus the average frequency of the VCO will be also proportional to that RMS value. Note that the proposed method estimates the RMS value of random jitter rather than measuring each jitter value at every clock edge, and only the mean value of the $V_C$ is required in estimating the value of random jitter. As a result, the inherent random jitter of the VCO will not affect the estimation result very much, and it can be also canceled out by the differential operation from the OR and AND operations.

The frequency of the VCO is a non-linear function of its control voltage due to the analog behavior of the VCO and the voltage-to-current converter, but the frequency can be approximated as a linear function of the control voltage near the operating region of the VCO, as shown in (2.5), which usually happens in modeling the behavior of a PLL.

$$f_{VCO}(V_C) = K_{VCO}V_C + C$$  \hspace{1cm} (2.5)

where $K_{VCO}$ is the gain of the VCO, and $C$ is a constant.

When $\overline{f_{VCO}(V_C)}$ represents the arithmetic mean frequency of the VCO at $V_C$, the average voltage of $V_C$, $V_{C_{AVG}}$, when there is random jitter will be given by

$$V_{C_{AVG}} = \overline{f_{VCO}^{-1}(V_{OR_{AVG}})} - \overline{f_{VCO}^{-1}(V_{AND_{AVG}})}$$  \hspace{1cm} (2.6)

The VCO frequency characteristics can deviate from its simulated value due to process variations after fabrication, so an effort for its characterization needs to be made to correctly estimate its control voltage by reading the
frequency. This characterization can be done by applying an external reference voltage to the VCO and by measuring its corresponding frequency. Since this open-loop test is one of the widely used features in the pose-silicon PLL characterization effort, it could be easily implemented. At least two different values for the external voltage reference are required to construct a linear relationship between the frequency of the VCO and the corresponding control voltage.

In the proposed method, although two separate measurements for the OR operation and the AND operation would involve increased test time in measuring jitter, and would require additional calculations for the jitter estimation, there are also a couple of benefits. First, the proposed method does not need a complicated design effort on the charge pumps for charging and discharging the capacitor, but just uses simple inverters for that purpose, instead. An additional advantage is that no biasing circuitry is required to drive the charge pump. More importantly, since the difference is used for the jitter estimation, the proposed method will be less susceptible to process variations. However, circuit mismatch between the NOR gate and the NAND gate could induce measurement errors, as previously mentioned, when jitter in the clock is so small that it is comparable to that mismatch.

2.3 Converting the Average Value into the RMS Value

It is evident that the average value is not always the same as the RMS value. For example, if the RMS value of random jitter is 10\(\text{ps}\) in the jittery
clock signal of 1GHz, this does not necessarily mean that its contribution to the voltage $V_C$ is also 1% of the $V_{dd}$, which will be true for random jitter with the average value of 10ps. This comes from higher probabilities for smaller jitter components than larger jitter components, and these probabilities follow a Gaussian distribution. Therefore, the average voltage should be related to the RMS value. In Figure 2.7, the solid line shows a Gaussian distribution with a normalized standard deviation (refer to left side y-axis), and the dotted line represents a jitter magnitude distribution having 10ps for its standard deviation (refer to right side y-axis). In this example, the probability that the magnitude of jitter is less than $\pm 10\text{ps}$ amounts to 68.26%.

![Figure 2.7: A Gaussian distribution with a jitter magnitude distribution](image)

If we regard the magnitude of random jitter as a random variable, $x$,
the mean value, or the expected value, of the $x$ can be given by

$$E\{x\} = \int_{-\infty}^{\infty} x f(x) dx$$  \hspace{1cm} (2.7)

Note that the magnitude of random jitter was used instead of the value of random jitter itself in (2.7) since otherwise the expected value becomes zero. The mean of this random variable can be solved using a Lebesgue integral [53]. When we divide the random jitter distribution into $\Delta x$ and by using that both the $f(x)$ and $x$ are even functions, the mean becomes

$$\int_{-\infty}^{\infty} x f(x) dx = 2 \int_{0}^{\infty} x f(x) dx \simeq 2 \sum_{0}^{\infty} x_k f(x_k) \Delta x$$  \hspace{1cm} (2.8)

Using $f(x_k)\Delta x \simeq P\{x_k < x < x_k + \Delta x\}$, the mean approaches

$$E\{x\} \simeq 2 \sum_{0}^{\infty} x_k P\{x_k < x < x_k + \Delta x\}$$  \hspace{1cm} (2.9)

For random jitter with its standard deviation of 10ps, if we use 1ps for $\Delta x$, the calculated mean value using (2.9) becomes 8.482ps, and this corresponds to the area under the solid line, ‘Probability × Jitter Magnitude’, in Figure 2.8.

The shape of the solid line in Figure 2.8 can be interpreted as follows. When jitter has a high probability of occurrence, the magnitude of jitter is small based on its Gaussian distribution so that its contribution to the average value is also small. On the other hand, when the magnitude of jitter is larger than $3\sigma$, the probability for jitter to occur is so small that its contribution to the average value is very small even if the magnitude of jitter is so large.
Figure 2.8 shows that the magnitude of jitter is maximized around the standard deviation of the jitter.

Although this calculation is based on $\pm 4\sigma$, since the probabilities for larger jitter components beyond this range are negligibly small, their contributions can be ignored. Therefore, without loss of generality, we use this result for all simulation runs and for all measurement results in converting the estimated average values of random jitter into the corresponding RMS values with which the RMS values of injected random jitter are to be compared. The constant for converting the average value to the RMS value, $K_{AVGtoRMS}$, is thus given by

$$K_{AVGtoRMS} = \frac{10\text{ps}}{8.482\text{ps}} \approx 1.1789$$

(2.10)
2.4 Summary

In this chapter, the basic idea of the jitter estimation method has been explained. The differential approach using the AND operation and the OR operation to replace, as well as to overcome the limitation of, the XOR operation has been proposed. This approach can capture smaller jitter components than the XOR method does, and can also contribute to reducing measurement errors. Since the outputs from the AND operation and the OR operation, unlike the output from the XOR operation, have a DC offset of 50% of \( V_{dd} \), the \( V_C \) voltage can be used to define the operating region of the VCO. Finally, the relationship between an average value and its corresponding RMS value of random jitter has been derived, which will be used for estimating the RMS value of random jitter in Chapter 4 and Chapter 5.
Chapter 3

Delay Measurement Method using a Shrinking Clock for Reference Clock Generation

This chapter describes the method for removing the requirement of the reference clock that was assumed to be available as an ideal, jitter-free, clean clock in the previous chapter. The basic idea of using an adjustable delay line to replace the reference clock is first presented, then followed by a delay measurement method using a shrinking clock signal with a simple BIST circuit along with clock signals provided by an external tester.

3.1 Basic Idea

In Chapter 2, a clean reference clock signal was assumed to be available to measure random jitter in a jittery clock signal, but the clean reference clock is not readily available. To address this issue, several BIST circuits aimed at jitter measurement used a delayed version of the clock of interest as the reference clock [13, 27, 35, 72]. The same method can be applied to the proposed jitter estimation method in Chapter 2 as shown in Figure 3.1. If the adjustable delay in Figure 3.1 can delay the clock by an exact one period of the clock, the BIST circuit measures jitter for both cycle A and cycle B.
Figure 3.1: Outputs from the AND and OR operations when the delayed version of the jittery clock replaced the reference clock

Unlike deterministic jitter components such as periodic jitter, random jitter does not have any correlation from a clock edge to another clock edge: their autocorrelation is zero. When $S(f)$ represents the power spectral density of a band-limited process as shown in (3.1),

$$S(f) = \begin{cases} \frac{1}{2}N_0 & |f| \leq B \\ 0 & \text{otherwise} \end{cases} \quad (3.1)$$

where $N_0$ is a constant for band-limited white noise and $B$ is the frequency band, the autocorrelation function $R(\tau)$ of the band-limited white noise process becomes $BN_0 sinc(2B\tau)$ [73]. Considering that the normalized sinc function can be used as a Dirac delta function, the $R(\tau)$ approaches $\frac{N_0}{2}\delta(\tau)$ as $B$ approaches $\infty$. As a result, random jitter values from successive clock edges
have zero correlation.

When the delayed jittery clock is used to sample the jittery clock in jitter measurement, if the RMS value of random jitter is $\sigma$, the measured jitter becomes $\sqrt{2}\sigma$, since jitter measured using a sampling method is the convolution of jitter distributions from those two clock signals [48]. In the proposed jitter measurement method, the pulse width from the AND operation becomes smaller due to the increased jitter by $\sqrt{2}$, and the pulse width from the OR operation becomes larger for the same reason. Thus, if we can delay the clock of interest for random jitter measurement by an exact amount of one period of that clock, we can measure random jitter in the jittery clock, which will be $\sqrt{2}$ times larger than the jitter of interest, without using the clean reference clock.

![Diagram of clock signals with AND and OR operations](image)

Figure 3.2: When the delayed clock edge is not accurately aligned with the clock edge

In reality, delaying the clock signal by the exact amount is not easily
attainable, and a fine tuning step is often required when the delaying circuitry was implemented [13]. When the delayed clock edge (A in Figure 3.2) is not aligned accurately with the clock edge (B in Figure 3.2) of the clock in the next cycle, the output pulse widths from the AND operation and the OR operation can have a shrunk or a stretched pulse even if there is no jitter in the clock. This can be overcome, however, if the amount of the adjustable delay can be accurately measured and can be used for the compensation of measured jitter values. In Figure 2.5, this shrunk or stretched pulse width can be regarded as a duty cycle modulation to the input of the inverters following the NOR and NAND gates, and it moves the $V_C$ voltage to a higher value (for the stretched pulse) or to a lower value (for the shrunk pulse).

In the following section, an accurate delay measurement method using a shrinking clock signal is presented, thus the jitter measurement method in Figure 2.5 can be applicable to random jitter measurement for a PLL output clock without relying on the clean reference clock.

### 3.2 A Delay Measurement Method Using a Shrinking Clock Signal

#### 3.2.1 The Proposed Delay Measurement Method

Time-to-digital converters (TDCs) have been widely adopted for measuring delay or time interval since they produce digitized values for the delay or the time interval of interest. The resolution of the TDCs can be improved by using a Vernier delay line or an interpolation method so that they can over-
come the minimum delay limitation set by a gate delay [3, 4, 36, 55]. TDCs based on pulse-shrinking delay elements using a current starved inverter or a skewed inverter were also proposed to overcome the limitation [11, 12, 20, 56]. In the pulse-shrinking delay cell, the rising time is set to take a longer time than the falling time in a way that the width of the pulse that propagates along the cascaded delay cells decreases by the amount of the time difference. The rising time can be increased by controlling the sink current of the first inverter in the delay cell, and a voltage bias is used to control the current. However, these delay cells are prone to process, voltage, and temperature (PVT) variations, and continuous calibration is essential to maintain their desired amount of pulse shrinking. For the calibration, an external bias voltage [57], an stable reference frequency [12], or a DLL that controls a bias voltage [37] is used so that the resolution in the delay cell is maintained during operation. The area consumed by the TDC is also of concern when the TDC is to be integrated to measure timing parameters.

In this section, a delay measurement method using a shrinking clock signal is presented. Instead of using the pulse-shrinking delay cells aforementioned, the shrinking clock is generated with a simple AND operation on two clock signals having slightly different frequencies. The clock signals are provided by external clock sources, and when the proposed delay measurement method is to be implemented as a BIST solution, an external tester can be used to generate such clock signals. Using an external tester as a clock source can facilitate the shrinking clock generation without the calibration process.
that uses external references while area overhead for the delay measurement circuit is greatly reduced compared to full-fledged BIST circuits shown in previous work [12, 56]. Since the proposed method only uses pure digital circuits, overall performance of the measurement is less affected by the PVT variations compared to the approach that uses analog delay cells. The linearity and achievable resolution of the measurement, however, are shifted toward the external clock source being used.

![A shrinking clock signal](image)

Figure 3.3: A clock with decreasing duty cycles by $d$ in each subsequent cycle

The proposed delay measurement method utilizes a clock with decreasing duty cycles, or a shrinking clock, along with an AND operation. As shown in Figure 3.3, the duty cycles of the shrinking clock decrease by the amount of $d$ for each subsequent cycle. Note that, unlike other pulse-shrink methods [12, 20, 56], the period of the shrinking clock is maintained. Figure 3.4(a) depicts a high-level configuration for the delay measurement. The shrinking clock is fed to both a delay line and one input of a NAND gate, and the delayed version of the clock is fed to the other input of the NAND gate. The output of the NAND gate is connected to an inverter to complete the AND operation.

The timing diagram in Figure 3.4(b) shows the basic idea of delay
Figure 3.4: The basic idea of measuring a delay using shrinking clock signals

measurement for the configuration shown in Figure 3.4(a). Suppose that the period of the shrinking clock is $T$, its initial duty cycle is 50%, and the delay from the delay line is $X$. The output pulse width of the AND operation will be $T/2 - X$ in the first cycle. The pulse width reduces to $T/2 - d - X$ in the next cycle due to the decreasing duty cycle by the amount of $d$, and the pulse width continues to shrink until the pulse disappears as the duty cycle keeps decreasing. This disappearance happens when two input signals to the NAND gate overlap in a marginal manner or do not overlap at all. The delay caused by the delay line is measured by counting the number of cycles until the output of the AND operation vanishes. When the counted number of cycles
is \( N \), the delay \( X \) is expressed by

\[
X = \frac{T}{2} - Nd + \epsilon
\]

(3.2)

where \( \epsilon \) represents a quantization error equal to or smaller than \( d \).

### 3.2.2 Generating the Shrinking Clock Signal

In generating the shrinking clock, another AND operation is used on the clock signals from the external clock source, and the ATE is considered for generating those clock signals throughout this section. Note that the ATE is not designed to generate the shrinking clock. Figure 3.5 describes how the shrinking clock signal is generated from two tester clock signals.

The tester provides two clock signals, Tester Clock 1 with the period of \( T_1 \) and Tester Clock 2 with the period of \( T_2 \), and \( T_1 \) is slightly larger

![Diagram of generating a shrinking clock](image)
than $T_2$. When $d_1$ represents the difference between duty cycles of the Tester Clock 1 and the Tester Clock 2 as follows,

$$d_1 = \frac{T_1}{2} - \frac{T_2}{2}, \quad (3.3)$$

the duty cycle, or the pulse width, of the output from the AND operation becomes $T_1/2 - d_1$ in the first cycle. In the next cycle, $d_2$ is given by

$$d_2 = (T_1 + \frac{T_1}{2}) - (T_2 + \frac{T_2}{2}) = (T_1 - T_2) + d_1 \quad (3.4)$$

and in the $n_{th}$ cycle, $d_n$ becomes

$$d_n = ((n - 1)T_1 + \frac{T_1}{2}) - ((n - 1)T_2 + \frac{T_2}{2}) = (n - 1)(T_1 - T_2) + d_1 \quad (3.5)$$

when $d_n$ is less than $T_2/2$. In this way, the shrinking clock whose duty cycle is decreased by the amount of $T_1 - T_2$ for each consecutive cycle can be generated.

Referring to (3.2), the measurement range of a delay is set by the initial duty cycle $T/2$ of the shrinking clock, and measurement resolution is determined by the shrinking amount $d$. In Figure 3.5, the initial duty cycle and the shrinking amount correspond to $T_1/2 - d_1$ and $T_1 - T_2$, respectively. Because these two variables can be easily controlled by the ATE, and are not fixed by the design of the measurement circuit itself, the measurement range and the resolution can also be easily adjusted even after fabrication, which provides great flexibility in measuring the delay of interest.

For example, when the delay to be measured in Figure 3.4(a) is very small, both $T_1/2 - d_1$ and $T_1 - T_2$ can be adjusted in a way that the delay can
be measured with finer resolution without causing the counter, which is used to count the number of cycles until the AND output vanishes, to overflow even if the bit-width of the counter is not very wide: in this case, both $T_1/2 - d_1$ and $T_1 - T_2$ are desired to be reduced in smaller values. On the other hand, when the delay to be measured is very large, both $T_1/2$ and $T_2/2$ can be increased to accommodate the large delay while keeping $T_1 - T_2$ small for fine measurement resolution.

### 3.2.3 Reducing Measurement Errors With a Differential Approach

![Figure 3.6: NAND gate output showing the transient effect of incomplete rail-to-rail swings](image)

Figure 3.6: NAND gate output showing the transient effect of incomplete rail-to-rail swings
When the pulse-shrinking method is used for delay measurement or for time interval measurement, a static measurement error, or an offset error, occurs in case the width of the pulse becomes too small [11]. This happens when two inputs to the AND operation barely overlap, and the output of the AND operation may not have rail-to-rail swings as a result. Figure 3.6 shows those transient effect at the output of a NAND gate from a circuit-level simulation run.

Those very narrow or incomplete pulses shown in Figure 3.6 have difficulties in driving the counter that counts the number of cycles before the pulse vanishes completely, and they contribute to the aforementioned measurement error. To cope with this offset error, instead of measuring the offset itself [11], a differential approach is used since errors arising from circuit mismatches can be also canceled. Figure 3.7 depicts an example configuration for the measurement of the delay difference between two delay lines, delay line 1 and delay line 2, and Figure 3.8 shows its corresponding timing diagram.

Figure 3.7: Configuration for a differential approach

In this example, the output of the AND operation with the delay line 1 lasts for 5 cycles, but it does for only 3 cycles with the delay line 2. By
Figure 3.8: Waveforms from the differential approach in measuring the delay difference of two delay lines

taking the difference of two measurements, the offset error in each measurement can be canceled, resulting in $2d$ as the delay difference of those two delay lines since the transient signals affect both measurements in a similar manner. Although two delay lines were used to describe the differential approach in the example, one of them can be replaced with a RC interconnect delay to measure the delay of the other delay line, which will be described in the circuit simulation section.
3.2.4 Circuit Implementation for the Delay Measurement

Each AND operation was implemented using a NAND gate and an inverter, and a 12-bit asynchronous counter was designed to count the number of cycles at the output of the AND operation. The asynchronous counter was chosen over a synchronous counter since it has less loading on its clock input. For the control of the counter, a simple logic circuit that generates a counter enable signal and a counter reset signal was also designed.

![Diagram of counter enable and reset signals](image)

**Figure 3.9**: Generating a counter enable signal and a counter reset signal ($T_1 > T_2$)

Figure 3.9 depicts the control logic to generate a **Counter Enable Signal**, a **/Counter Enable Signal** and a **Counter Reset Signal**. The logic for the **/Counter Enable Signal** was implemented using cascaded D-type flip-flops to address glitches resulting from random jitter in the tester.
clock signals. The faster clock signal, which corresponds to the **Tester Clock 2**, drives the D inputs of the flip-flops, and the slower clock, the **Tester Clock 1**, provides the clock inputs to the flip-flops. The Q output of the first flip-flop makes a transition to a logic high state when the slower clock starts lagging the faster one and the required setup time in the flip-flop is satisfied. The **Counter Enable Signal** is the delayed one of the first Q output, and is used to gate the counter input. This control logic was able to remove glitches successfully resulting from random jitter with a standard deviation of 15\(\text{ps}\) in **Tester Clock 1** and **Tester Clock 2**. For more severe jitter, a glitch killer circuit [56] can be used.

![Waveforms for control signals](image-url)

Figure 3.10: Waveforms for control signals
When the **Counter Enable Signal** transits to a logic low state, the delay measurement is completed, and the positive edge of **/Counter Enable Signal** can be used to latch the counter output to a register, whose value can be shifted out to read the measurement using a test access point (TAP) network if implemented. To make the proposed method work for consecutive measurements, the **Counter Reset Signal** is generated to reset the counter for the next measurement. Figure 3.10 shows the waveforms of the control signals along with their input signals. The **Counter Reset Signal** keeps resetting the counter, and it ceases when the **Counter Enable Signal** becomes active. Since the reset occurs a couple of cycles after the **Counter Enable Signal** is deactivated, there is enough time for the register to latch the counter output.

### 3.2.5 Consideration on Tester Accuracy

Although the shrinking clock in the proposed method will be much less sensitive to the PVT variations compared with delay cell-based shrinking pulses, the quality of the shrinking clock would suffer from jitter or skew in the tester clock signals. In other words, the uncertainties of the clock signals due to jitter or pin-to-pin skew directly affect the amount of shrinking. The OTA, which can be found in the specification for a tester, defines the overall accuracy of the tester considering both the driver side and the strobing side [1]. The EPA, the subset of the OTA, defines the accuracy of the driver side or the strobing side of the tester. Considering that the proposed method only utilizes tester output signals, whose quality is specified by the driver side EPA,
simulation demonstrating the validity of the proposed method focused on the effect of the EPA on the measurement accuracy.

3.2.6 Simulation Method and Results

3.2.6.1 Test Circuit Configuration

An example configuration for the proposed delay measurement is depicted in Figure 3.11, where two measurement paths, a *calibration path* and a *measurement path*, are shown. The Counter Enable Signal and Counter Reset Signal in Figure 3.11 are generated from the control logic in Figure 3.9. As previously mentioned, this differential approach can reduce the offset error as well as other possible measurement errors effectively. All simulation runs use this configuration.

In the calibration path, the shrinking clock signal goes through a pair of a dummy multiplexer and a dummy de-multiplexer, and arrives at the input of the AND operator. The other input of the AND operator is directly provided by the shrinking clock signal. The output of the AND operation, which is gated by the Counter Enable Signal, drives the counter, and the counter starts counting the number of cycles from the rising edge of Counter Enable Signal until the output from the AND operation disappears. The measurement from the calibration path functions as a reference for measurements that follow. Control signals for multiplexers and de-multiplexers, denoted by SEL1 through SEL3, are appropriately set to construct the calibration path, and those signals can be set by a TAP if used. Next, the measurement path is constructed by
appropriately setting the SEL1 through SEL3. In this path, the shrinking clock signal goes through the delay of interest. All other operations of the circuit are the same as those done for the calibration path. The contribution from multiplexers and de-multiplexer to the measured delay in this measurement path is canceled out by the differential measurement. The value of the delay to be measured is obtained by multiplying the measurement resolution, which is known a priori, by the cycle difference between two measurements.

For the delay line in Figure 3.11, two different types of delay mod-
els were used. The first type consists of inverter chains with various delay lengths: 35.07\(ps\), 67.70\(ps\), 100.15\(ps\), and 165.31\(ps\). The second type models a combinational delay path: one with a 14 logic-depth and the other with a 28 logic-depth. Their delay values correspond to 435.70\(ps\) and 872.40\(ps\), respectively.

3.2.6.2 Simulation Setup

The proposed method was validated with circuit-level simulation using Cadence Analog Design Environment (ADE), and all circuitry in the simulation used a 0.13\(\mu m\) technology. The simulation runs were divided into two different cases. The first case aimed at the validity of the differential approach, and clock signals from the ATE were assumed to be ideal and jitter-free. The second case validated the measurement accuracy when the EPA of the ATE was considered.

The period difference between two clock signals was set to from 2\(ps\) to 10\(ps\). For the second simulation case, the timing delay error coming from the pin-to-pin skew in the ATE was modeled as a signal delay between two input clock signals, and jittery clock signals were generated using Matlab and provided to the Cadence tools, which will be explained in the experiment result in detail. Since external clock signals drive the measurement circuit inside a chip, the parasitic components from the package and bond wires also need to be considered. For the parasitic components of the bond wire, 1.915\(nH\), 0.079\(m\Omega\), and 0.140\(pF\) were used for inductance, resistance, and capacitance,
respectively. The package resistance was set to 500\text{m}\Omega, and the capacitance of a bonding pad was set to 0.2\text{pF}.

### 3.2.6.3 Simulation Results with Ideal Clock Signals

Table 3.1: Simulation results with ideal clock signals

<table>
<thead>
<tr>
<th>Delay of interest [ps]</th>
<th>Measurements per resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2ps</td>
</tr>
<tr>
<td>35.07</td>
<td>32</td>
</tr>
<tr>
<td>67.70</td>
<td>66</td>
</tr>
<tr>
<td>100.15</td>
<td>98</td>
</tr>
<tr>
<td>165.31</td>
<td>164</td>
</tr>
<tr>
<td>435.70</td>
<td>436</td>
</tr>
<tr>
<td>872.40</td>
<td>874</td>
</tr>
</tbody>
</table>

Table 3.1 shows the simulation results of delay measurement for six delay values when the measurement resolution varies. In this simulation, no timing delay error nor jitter was considered since the purpose of the simulation was to validate the differential approach as well as the effect of quantization errors from the counter. In most cases, errors in \text{ps} were within corresponding measurement resolution, and percent errors for the same delay value tend to increase as the measurement resolution becomes coarse. The measurement error for the 35.07\text{ps} delay with 2\text{ps} resolution, which exceeds the measurement resolution by 1\text{ps}, was caused by the loading at the de-multiplexer that follows the delay line. The simulation results clearly show that measurement errors from the transient effect shown in Figure 3.6 can be minimized by the
differential approach.

3.2.6.4 Simulation Results Considering the EPA

To consider the EPA of the ATE, random jitter, an input timing delay error, and an input transition time variation need to be individually taken into account to model realistic clock signals from the ATE [1]. Their individual contributions to the EPA are, however, unknown outside the manufacturer of the ATE. Therefore, the input timing delay error and the input timing jitter were assumed to contribute to most of the EPA in modeling the tester clock signals, and their contributions were assumed to be similar to each other. The EPA was assumed to be around ±100\(\text{ps}\), which is a realistic value for most ATEs being widely used [18, 54]. For the input timing delay error, 40\(\text{ps}\), 55\(\text{ps}\), and 70\(\text{ps}\) were used. For the input timing jitter, only random jitter was considered [38], and 20\(ps_{RMS}\), 15\(ps_{RMS}\), and 10\(ps_{RMS}\) were used so that their 3\(\sigma\) values with corresponding input timing delay errors add up to 100\(\text{ps}\). For example, the EPA of 100\(\text{ps}\) can come from the 10\(ps_{RMS}\) random jitter and the 70\(\text{ps}\) input timing delay error as shown in (3.6).

\[
(10ps_{RMS} \times 3) + 70ps = 100ps
\]  

(3.6)

Note that the EPA of 100\(\text{ps}\) is a very pessimistic number when only a single tester is considered because the EPA value is used to guarantee the repeatability of testing results not only from multiple runs but also from tester-to-tester runs.
Table 3.2: Simulation results considering the EPA

<table>
<thead>
<tr>
<th>Delay of interest [ps]</th>
<th>Measurements per random jitter values</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10(ps_{RMS})</td>
</tr>
<tr>
<td>35.07</td>
<td>34</td>
</tr>
<tr>
<td>67.70</td>
<td>70</td>
</tr>
<tr>
<td>100.15</td>
<td>100</td>
</tr>
<tr>
<td>165.31</td>
<td>165</td>
</tr>
<tr>
<td>435.70</td>
<td>436</td>
</tr>
<tr>
<td>872.40</td>
<td>875</td>
</tr>
</tbody>
</table>

Table 3.2 shows the simulation results for the same six delay values while there are uncertainties in the tester clocks due to the EPA of the tester. The measurement resolution was set to 10ps, and an average value of ten measurements from different random jitter distributions was used for each result to improve measurement accuracy by minimizing quantization errors. As shown in Table 3.2, random jitter contributes to measurement errors more than the input timing delay when the amount of the EPA remains the same.

### 3.2.6.5 Simulation Results Considering PVT Variations

As previously mentioned, the shrinking amount of the shrinking clock is not affected by the PVT variations, unlike other pulse-shrink methods that use analog delay cells [12, 20, 56]. Figure 3.12 shows simulation results considering the EPA at different PVT corners, where the measurement accuracy is not affected by the PVT variations and measured delay values follow well the expected delay values. Note that the delay values to be measured were also
A new delay measurement method using a shrinking clock was proposed and validated using circuit-level simulation. Circuit-level simulation showed good linearity and measurement accuracy regardless of PVT variations when the EPA of the ATE amounts to 100 ps. The measurement accuracy and reso-
olution in the proposed method are closely related to the tester accuracy rather than the circuit design, and they can be improved when better per-pin modules are used in the ATE. The measurement range can be easily extended by using lower frequency clock signals. The dynamic range can be also increased, not by increasing the bit-width of the counter, but by increasing the duty cycle of the external clock signals. Using tester clock signals in generating the shrinking clock makes the delay measurement circuit simple and small. Another benefit of the proposed method is that it facilitates comparisons among the same delay of interest from different chips. This is due to the fact that signals provided by the ATE are used as references instead of delay elements included in the BIST circuitry.

The test time required for delay measurement depends on the periods of the clock signals as well as their period difference. When the periods of the clock signals are set to 5\(\text{ns}\) and 4.99\(\text{ns}\), the test time becomes

\[
\frac{5\text{ns}}{5\text{ns} - 4.99\text{ns}} \times 5\text{ns} \times 2 = 500\text{cycles} \times 5\text{ns} \times 2 = 5\mu\text{s} \tag{3.7}
\]

The multiplication factor of 2 comes from the differential measurement. When 10 measurements are required to reduce the effect of random jitter by averaging them, the total test time will be 50\(\mu\text{s}\), and overhead from calculations such as averaging and subtraction in tester software will add up to the total test time. Since the measurement for the calibration path is required only once, measurement on different delays in the same DUT will consume much less test time.
Chapter 4

Circuit Design for the RMS Estimation Method of Random Jitter

In this chapter, we present the BIST circuit design of the RMS estimation method presented in Chapter 2 in detail. Design considerations on a NAND gate and a NOR gate are the first topic, followed by a way of using an inverter as a simple charge pump. Then, the design of the VCO along with a voltage-to-current converter is described. The BIST circuit was validated using a 0.13\(\mu m\) technology, and simulation results for various random jitter values over a wide range of an input clock frequency are demonstrated. For the fabrication of a test chip, the performance of the BIST circuit was validated again with a 0.18\(\mu m\) technology.

4.1 Circuit Implementation and Design Considerations

4.1.1 Requirements for the AND Operation and the OR Operation

The proposed idea was first validated in behavioral-level simulation using Matlab. The NAND gate and the NOR gate used in the Matlab simulation have ideal behavior showing good linearity on their \(V_C\) output modulation when the RMS value of random jitter increases, but this is not what we can expect from real silicon, even from circuit-level simulation. In implementing
those gates with CMOS transistors, the following characteristics are desired for estimating random jitter accurately.

1. The rising and falling times of the gates are the same each other.

2. The NAND gate and the NOR gate have the same output pulse width when their input signals make transitions at the same time.

3. The duty cycle of each output amounts to 50% when its input signal has also 50% of duty cycle.

4. The output pulse widths from both gates change linearly when the timing difference of two input signals changes linearly.

5. The output pulse width does not depend on the order of input signals’ arriving time.

In reality, there is no known logic family or circuit which can fulfill all those requirements. A NAND gate and a NOR gate using pseudo-nMOS logic when their pull-down networks are modified to have symmetric behavior, for instance, can satisfy the second requirement: their output waveforms exactly match each other when their input signals make transitions at the same time. But they cannot satisfy the other requirements. So do a generic CMOS NAND gate and a generic NOR gate, and they cannot satisfy even the fifth requirement. Since the fifth requirement is essential for jitter measurement, the symmetric CMOS gates were chosen in implementing the NAND gate and
the NOR gate for the proposed method, and their W/L ratios as well as their current driving capability were adjusted to best meet all those requirements.

4.1.2 Symmetric NOR and NAND Gates

![Diagram of symmetric NOR gate](image)

(a) A common design for a symmetric NOR gate

![Simulation result for symmetric NOR gate](image)

(b) Simulation result for a symmetric NOR gate

Figure 4.1: A symmetric NOR2 gate and its output behavior

The clock edge in the jittery clock can lead or lag behind the edge of the clean clock due to its randomness. To be able to capture the amount of random jitter in both cases, the behavior of the NOR gate and the NAND gate should be consistent regardless of the order input clock signals arrive, or make transitions. The symmetrical NOR gate and the symmetrical NAND gate can address this issue better so that only the timing difference between two input signals, not the order of their arrivals, affects their output transitions.

Figure 4.1(a) depicts a common implementation of the symmetric NOR gate, and Figure 4.1(b) shows the simulation result for the symmetric NOR gate.
gate depicted in Figure 4.1(a), where the output of the symmetric NOR gate shows undesired behavior for jitter measurement at the falling edge. When two input signals, \( V_{in1} \) and \( V_{in2} \), make transitions from low to high simultaneously, both transistors in the pull-down network, \( M5 \) and \( M6 \), are turned on and sink current. On the other hand, when one input signal makes its transition first and the other follows it with a delay, either \( M5 \) or \( M6 \) is turned on first depending on which input arrives first, and the other is turned on sequentially. In Figure 4.1(b), when \( V_{in2} \) makes transition from low to high later than \( V_{in1} \) with a delay, the NOR2 output (dotted line) has a longer falling time than the other case without the delay (solid line). As a result, the behavior of the falling edge, or falling time, depends on the number of driving inputs at a time, whereas the rising time remains almost the same regardless of the number of driving inputs. The symmetric NAND gate also shows the similar behavior, but at its rising edge. Since the proposed method utilizes output pulse widths proportional to the amount of random jitter in the clock input, the pulse widths in these symmetric gates should only depend on the input timing difference, and should not be affected by the current driving strength.

To deal with this undesired behavior, those symmetric gates need to be modified so that the falling time and the rising time do not rely on their driving strength too much. One possible solution for this is to place an additional NMOS transistor below the NMOS network of the symmetric NOR gate as shown in Figure 4.2(a), and to place an additional PMOS transistor above the PMOS network in the symmetric NAND gate. These additional transistors can
Figure 4.2: A symmetric NOR2 gate with a current-limiting footer, and its output behavior

limit the maximum sink current in the NOR gate and the maximum source current in the NAND gate when their W/L ratios are set properly. Figure 4.2(b) shows the simulation result for the modified NOR gate shown in Figure 4.2(a), where the falling times in both cases (the solid line and the dotted line) are more similar to each other than the falling times in Figure 4.1(b).

Figure 4.3 shows the final designs for the NOR and NAND gates used in the proposed method. The added PMOS and NMOS transistors ($M_7$ and $M_8$) to pull-up networks and pull-down networks can control the maximum sink current for the NOR gate and the maximum source current for the NAND gate as previously mentioned. Note that those additional transistors can also function as power-gating transistors so that either the NAND gate or the NOR
gate can operate at a time.

(a) The modified symmetric NOR gate

(b) The modified symmetric NAND gate

Figure 4.3: The modified symmetric gates with both current-limiting header and footer

4.1.3 Using an Inverter as a Charge Pump

As previously mentioned, the inverter at each operation is used not only to invert the output from the NOR gate or the NAND gate to complete the OR operation or the AND operation, but is also used to function as a simple charge pump. The obvious advantage of using the inverter as a charge pump is no need for separate biasing circuitry, which involves the use of the bandgap reference voltage in most cases. Unlike the charge pump, the inverter does not source or sink current with the same amount, and this can result in
an asymmetric charging and discharging process: $I_P$ is not the same as $I_N$ in Figure 4.4. Considering that the proposed method uses the difference of average $V_C$ voltages from the AND operation and the OR operation, however, the sourcing current and the sinking current do not need to be matched, which was described in Figure 2.4.

![Figure 4.4: An inverter used to charge and discharge a capacitor](image)

Another point to consider here is that the voltage at the capacitor node, $V_C$, is affected by the channel-length modulation effect. The initial value of the $V_C$ will be around zero, and this favors $I_P$ over $I_N$. When the AND operation or the OR operation starts out, the $V_C$ value keeps increasing due to the difference between $I_P$ and $I_N$ until $\Delta V_C$ by the charging process becomes the same as $-\Delta V_C$ by the discharging process as expressed in (4.1) and described in Figure 4.5(a).
\[ V_C(t_n) = \frac{1}{C} \int_{t_{n-2}}^{t_n} (|I_P(t)| - |I_N(t)|)dt + V_C(t_{n-2}) \quad (4.1) \]

\[ = \frac{1}{C} \int_{t_{n-2}}^{t_{n-1}} K_p (V_{gs} - V_{thp})^2 (1 + \lambda_p (V_{dd} - V_C(t_{n-2}))) dt \quad (4.2) \]

\[ - \frac{1}{C} \int_{t_{n-1}}^{t_n} K_n (V_{gs} - V_{thren})^2 (1 + \lambda_n V_C(t_{n-1})) dt + V_C(t_{n-2}) \quad (4.3) \]

where \( K_p = 1/2 \mu_p C_{ox} W_p / L \), and \( K_n = 1/2 \mu_n C_{ox} W_n / L \), respectively.

(a) Initial charging and discharging processes where NMOS current (red solid line) is smaller than PMOS current (blue solid line) because of the initial value of \( V_C \) voltage

(b) The \( V_C \) voltage after it settled down

Figure 4.5: The behavior of the \( V_C \) voltage (a) in its initial state and (b) in its steady state

When the charging process and the discharging process reach their equilibrium states, the average \( V_C \) voltage also becomes consistent, or settles
down, as shown in Figure 4.5(b). In a very ideal case where the charging behavior and the discharging behavior of the capacitor are symmetric, this equilibrium state can be achieved when $I_P$ becomes the same as $I_N$ with an opposite sign. In reality, however, the final $V_C$ depends on charge transfer characteristics among the PMOS, the NMOS, and the capacitor. This means that the average $V_C$ voltage after it settled down depends on the ratio of sourcing current to sinking current in Figure 4.4 even if the charging behavior and the discharging behavior of the capacitor are symmetric.

![Inverter Output vs. Duty Cycle](image)

(a) Pre-layout simulation for a 400MHz input frequency (130nm)

(b) Pre-layout simulation for an 1GHz input frequency (180nm for fabrication)

Figure 4.6: The $V_C$ voltage across the entire duty cycle range of an inverter input with various P/N ratios

There are two contributing factors in the ratio of the $I_P$ and $I_N$ currents: one is the P/N ratio of the inverter and the other is the duty cycle of its input signal. Since the duty cycle, or the pulse width of the output from either the NAND gate or the NOR gate, is what the proposed method utilizes to
measure random jitter in the input clock, the P/N ratio of the inverter is the only quantity we can make use of. Figure 4.6 shows how the $V_C$ voltage (Y-Axis) changes across the duty cycles of an inverter input around 50% for various P/N ratios. Note that the slopes of the linear regions in Figure 4.6 are similar to each other, and they represent the modulation constant, $K_{MO}$, that was mentioned in (2.1) in Chapter 2. Interestingly, the slope does not depend on the size of the capacitor following the inverter nor the input frequency much as shown in Figure 4.7(a) and in Figure 4.7(b), respectively.

Since the slopes of the linear region in Figure 4.6 for different P/N ratios remain almost constant, the P/N ratio can be used to set the operating point of the VCO without affecting the modulation constant, $K_{MO}$, much. Figure 4.8
Figure 4.8: The behavior of $V_C$ voltages for AND and OR operations with and without random jitter. The rectangular in the left side was shown in Figure 4.5(a).

shows how $V_C$ voltages from the AND operation and the OR operation behave with and without random jitter in the jittery clock. The $V_C$ voltages from both operations settle down to around $500mV$ when there is no random jitter in the clock. On the other hand, the $V_C$ voltages deviate from their nominal values, but in opposite directions, when there is random jitter. The rectangular inside Figure 4.8 corresponds to the initial charging and discharging process shown in Figure 4.5(a).
Figure 4.9: The voltage-to-current converter and the voltage controlled oscillator

4.1.4 The Voltage Controlled Oscillator

Figure 4.9 depicts the diagram of the voltage-to-current converter and the VCO used in the implementation, and they convert the $V_C$ voltage at the capacitor node into a frequency value. The voltage-to-current converter design is based on a current mirror circuit, and it generates a $P_{control}$ signal and a $N_{control}$ signal from the $V_C$ voltage to control the amount of current in the current-starved inverter cells of the VCO. The VCO was implemented with a
5-stage single-ended ring oscillator, and a buffer was added to the last stage to minimize the effect on the oscillation behavior of the VCO from other circuits that use the VCO output clock. Due to the input gate capacitance of the buffer, however, the final stage of the oscillator sees larger capacitance than the other stages. To match the capacitance, four dummy buffers were added to the remaining nodes of the VCO. This helps in reducing intrinsic jitter caused by the VCO itself since the unbalanced capacitive burden causes deterministic jitter in the VCO output clock.

![VCO Frequency Characterization from Simulation](image)

Figure 4.10: VCO frequencies over $V_{\text{control}}$ across process corners (180nm)
The frequency of the VCO is determined by

\[ f_{VCO} = \frac{1}{2N(T_{d_{LH}} + T_{d_{HL}})} \]  

(4.4)

where \( N \) represents the number of stages, \( T_{d_{LH}} \) is a time delay for a low-to-high transition, and \( T_{d_{HL}} \) is a time delay for a high-to-low transition [59]. Since the \( P_{\text{control}} \) and the \( N_{\text{control}} \) limit the maximum current in the current-starved inverters, they control those time delays, and subsequently the frequency of the VCO. The frequency characteristic curves of the VCO over its control voltage are shown in Figure 4.10. The curve also consider the non-ideal, or non-linear, behavior of the voltage-to-current converter.

The VCO was designed to have an almost linear gain between 0.8\( V \) and 1.0\( V \) of the \( V_C \) voltage so that we can set the \( V_C \) voltage to 0.9\( V \) when there is no jitter in the jittery clock. The corresponding frequency ranges from 150MHz to 290MHz in a typical process corner. This operating point can be easily adjusted by actively utilizing the fact that changing the P/N ratio of the inverter moves the operating point, as previously mentioned.

### 4.2 Simulation Results for Random Jitter Measurement

#### 4.2.1 Simulation Environment and Estimation Methods

The proposed method was first validated with circuit-level simulation using a 0.13 \( \mu m \) technology to prove its measurement accuracy, and then it was validated using a 0.18 \( \mu m \) technology again before its fabrication. For simulation runs, Spectre Circuit Simulator was used for both cases. The jittery
clock signals were generated using Matlab with different clock frequencies with various RMS jitter values, ranging from 10\(\text{ps}\) to 150\(\text{ps}\) depending on the clock frequency. The generated jittery clock data were then provided to Spectre Circuit Simulator as input files so that they can be used for the simulation in the form of a \textit{pwlf} input source.

The average value of VCO output frequency for each simulation run was calculated from around 2,000 clock cycles, and a calculator tool in Analog Design Environment was used for the averaging. The \(V_c\) voltage was subsequently obtained from the calculated average frequency value using the VCO characterization curves. Although the fluctuating \(V_c\) voltage due to random jitter in the input jittery clock makes the VCO output clock jittery, the average frequency value can represent the average \(V_c\) voltage. Possible errors that can arise from this will be explained later.

For the characterization of the VCO, two \(V_c\) voltage values were chosen to construct a first-order linear equation that relates the VCO output frequency to its corresponding \(V_c\): 0.4\(V\) and 0.6\(V\) for simulation runs with the 0.13 \(\mu\text{m}\) technology, and 0.8\(V\) and 1.0\(V\) for simulation runs with the 0.18 \(\mu\text{m}\) technology. As shown in Figure 4.10, the frequency curves show large deviations from the typical process corner when there is a process variation. Therefore, the first-order linear equation, or the VCO gain, was derived for each process corner in the jitter estimation.

The modulation constant \(K_{MO}\) from the inverter output slope across inverter input duty cycles also needs to be derived and be applied to the jitter
calculation. For this, the slope of the inverter around the duty cycle of 50% was measured. As shown in Figure 4.6(a) and Figure 4.6(b), the slopes are different for different process nodes. As such, for the 0.13 $\mu$m technology, $K_{MO}$ resulted in 2.75, and for the 0.18 $\mu$m technology, $K_{MO}$ resulted in 3.75.

The $V_{CAVG}$ is the difference between $V_{ORAVG}$ and $V_{ANDAVG}$ as derived in (2.6), and $V_{ORAVG}$ and $V_{ANDAVG}$ represent the average $V_C$ voltage from the OR operation and the average $V_C$ voltage from the AND operation, respectively. When the $V_{CAVG}$ is obtained, the RMS value of random jitter in the jittery input clock, $RJ_{RMS}$, is estimated by

$$RJ_{RMS} = K_{AVGtoRMS} \frac{V_{ORAVG} - V_{ANDAVG}}{2K_{MO}V_{dd}} T = K_{AVGtoRMS} \frac{V_{CAVG}}{2K_{MO}V_{dd}} T\ (4.5)$$

where $T$ is again the mean period of the jittery input clock.

4.2.2 Jitter Estimation Results for a 0.13 $\mu$m Technology

4.2.2.1 Results for Different Input Clock Frequencies

Figure 4.11 shows jitter estimation results for three different input clock frequencies at a typical case (typical process corner, room temperature, and nominal Vdd). To compare the results from different clock frequencies, the RMS values in time have been converted into percentage values with respect to the corresponding clock period. For example, the 3% RMS jitter means 30$\text{ps}$ for a 1GHz input clock frequency, but it corresponds to 150$\text{ps}$ for a 200MHz input clock frequency. Peak-to-peak jitter values can be obtained by multiplying the RMS jitter value by six when $\pm 3\sigma$ is used.
Figure 4.11: Random jitter (RJ) estimations for different input frequencies

The simulation results show a good agreement between estimated RMS values and injected random jitter RMS values when the peak-to-peak jitter ranges from 3% to 18%, or the RMS value ranges from 0.5% to 3%, of the input clock period. Estimation error increases as the input clock frequency increases since the circuit mismatch between the NAND gate and the NOR gate became more evident at smaller clock periods. Large estimation error when the injected jitter is smaller than 1% in a RMS value is due to the non-ideality of circuits used to implement the AND and OR operations. As previously mentioned, the output pulse widths of the NOR gate and the NAND gate cannot follow their input changes in a linear manner especially when the timing difference between their input signals is very small. Due to the RC time
constant of a CMOS gate when it turns on, small arriving timing difference less than 10ps does not make any big difference compared with the case when two input signals arrive at the same time. This can be improved by using transistors with a smaller size, but they can suffer from a process variation more.

4.2.2.2 Results with Process Variation

Figure 4.12, Figure 4.13, and Figure 4.14 show the estimation results with a process variation for the input frequency of 200MHz, 400MHz, and 1GHz, respectively. In all cases, the injected random jitter values are in their RMS values, and the process variation covers a typical corner, a fast corner, and a slow corner. Temperature and power supply remain the same.

Figure 4.12: RMS value estimation results with a process variation when the input frequency is set to 200MHz

The slow process contributes more errors to the estimation results than
Figure 4.13: RMS value estimation results with a process variation when the input frequency is set to 400MHz

Figure 4.14: RMS value estimation results with a process variation when the input frequency is set to 1GHz
the fast process, and the error due to the slow process becomes large as the input frequency increases. Even with the process variation, the linearity of the estimated results is preserved well. Table 4.1 summarizes the jitter estimation results at different process corners when the input clock frequency is 200MHz. The maximum estimation error regardless of the process variation is 24% when the injected jitter ranges from 10\(\text{ps}\) to 180\(\text{ps}\), where the latter in peak-to-peak jitter amounts to 21.6% of the clock period.

Table 4.1: Estimation results for the input frequency of 200MHz at different process corners

<table>
<thead>
<tr>
<th>Injected RMS Jitter</th>
<th>Typical RMS</th>
<th>Error</th>
<th>Fast RMS</th>
<th>Error</th>
<th>Slow RMS</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0(\text{ps})</td>
<td>5.74</td>
<td>-</td>
<td>4.61</td>
<td>-</td>
<td>8.03</td>
<td>-</td>
</tr>
<tr>
<td>10(\text{ps})</td>
<td>9.34</td>
<td>7%</td>
<td>7.99</td>
<td>20%</td>
<td>12.26</td>
<td>23%</td>
</tr>
<tr>
<td>20(\text{ps})</td>
<td>16.69</td>
<td>17%</td>
<td>15.11</td>
<td>24%</td>
<td>20.58</td>
<td>3%</td>
</tr>
<tr>
<td>30(\text{ps})</td>
<td>26.41</td>
<td>12%</td>
<td>24.44</td>
<td>19%</td>
<td>31.48</td>
<td>5%</td>
</tr>
<tr>
<td>40(\text{ps})</td>
<td>37.30</td>
<td>7%</td>
<td>34.87</td>
<td>13%</td>
<td>43.73</td>
<td>9%</td>
</tr>
<tr>
<td>60(\text{ps})</td>
<td>57.41</td>
<td>4%</td>
<td>53.85</td>
<td>10%</td>
<td>66.73</td>
<td>11%</td>
</tr>
<tr>
<td>120(\text{ps})</td>
<td>117.39</td>
<td>2%</td>
<td>110.10</td>
<td>7%</td>
<td>135.00</td>
<td>13%</td>
</tr>
<tr>
<td>180(\text{ps})</td>
<td>169.68</td>
<td>6%</td>
<td>162.79</td>
<td>10%</td>
<td>193.33</td>
<td>8%</td>
</tr>
</tbody>
</table>

4.2.2.3 Discussion

In the proposed jitter estimation method, various factors can affect its estimation results. The linearity of the AND and OR operations, which is aforementioned, is the main contributor to the estimation error. Along with the RC time constant associated with turning on of CMOS gates, different
rising and falling times between the NAND gate and the NOR gate are also the source of the estimation error. When the circuit used for the jitter estimation cannot meet all requirements, it needs to be designed to show the best result for the amount of jitter values of interest, based on its characterization. For this design, the circuit utilizes its linear region when the injected jitter value is larger than 1% of the clock period in its RMS value. Two output pulse widths from the NAND gate and the NOR gate are not modulated linearly for the smaller timing difference, and this results in an error when there is no jitter in the input signal.

Figure 4.15: Random jitter estimation result when smaller transistors are used (input frequency of 400MHz with a process variation)

For better linearity with a reduced RC time constant, the size of tran-
sistors can be reduced, but this small size makes the design more vulnerable to the process variation. Figure 4.15 shows the estimation results for the input frequency of 400MHz when smaller transistors are used in designing inverters. The result shows a less estimation error at the typical corner when compared with Figure 4.13, but the error at the slow corner becomes worse.

![Diagram of Jitter estimation results for different capacitor sizes](image)

**Figure 4.16:** Jitter estimation results for the different size of the capacitor

Last, the inverter size is closely related to the size of capacitor. When a large capacitor is used, the size of the inverter used for charging or discharging the capacitor is not of a concern, as shown in Figure 4.7(a). When the size of the capacitor is small, however, the large inverter leads to large swings in the $V_C$ voltage, and this contributes to the error when the asymmetric charging and discharging behavior is considered. Thus, their sizes need to be adjusted.
to accommodate this. Figure 4.16 shows how the size of the capacitor affects the jitter estimation result.

4.2.3 Jitter Estimation Results for a 0.18 \( \mu m \) Technology

Figure 4.17: RJ estimation results for different process corners from post-layout simulation. Input clock frequency was set to 100MHz to compare with measurement results.

Figure 4.17 shows the random jitter estimation results for the 0.18 \( \mu m \) technology. Since the performance of the proposed method in estimating random jitter was validated using the 0.13 \( \mu m \) technology, simulation runs with this process technology were focused on the typical process corner although several data points from the slow corner and the fast corner are included to check deviations from the typical corner. In addition, more efforts were made...
for post-layout simulation since this simulation result is to be compared with measurement results after fabrication. All data points in Figure 4.17 are from post-layout simulation runs including $V_{dd}$ and GND pads.

Figure 4.18: Layout of the random jitter measurement circuitry (RJ BIST) including pads

Figure 4.18 shows the layout of the BIST circuitry for random jitter measurement. The area consumed by the AND-OR block and the VCO amounts to 2,820 $\mu m^2$, and the MIM (Metal-Insulator-Metal) capacitor block occupies 20,736 $\mu m^2$, in the 0.18 $\mu m$ CMOS technology. The MIM capacitor can be replaced by a capacitor with higher density since the accuracy of capacitance is not of concern in the circuit operation. Table 4.2 shows the area of each circuit block.
Table 4.2: Area of the BIST circuitry in a 0.18 µm CMOS technology

<table>
<thead>
<tr>
<th>Circuit Block</th>
<th>X-dim. [µm]</th>
<th>Y-dim. [µm]</th>
<th>Area [µm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND-OR</td>
<td>48</td>
<td>36</td>
<td>1728</td>
</tr>
<tr>
<td>VCO</td>
<td>42</td>
<td>26</td>
<td>1092</td>
</tr>
<tr>
<td>MIM Capacitors (14.4pF)</td>
<td>144</td>
<td>144</td>
<td>20736</td>
</tr>
<tr>
<td>Frequency Divider</td>
<td>82</td>
<td>10</td>
<td>820</td>
</tr>
</tbody>
</table>

4.3 Summary

In this chapter, the BIST circuit design for the RMS estimation method presented in Chapter 2 has been presented in detail. Design considerations on the symmetric NAND and NOR gates, the inverter that functions as a simple charge pump, and the VCO have been also discussed. The BIST circuit was validated using both the 0.13µm technology and the 0.18µm technology, and simulation results for various random jitter values over a wide range of the input clock frequency demonstrated the validity of the proposed method in estimating the RMS value of random jitter with good linearity. Process variation was considered in the simulation for both CMOS technologies, but temperature variations remained future work.
Chapter 5

Measurement Results for the RMS Estimation Method

This chapter presents the measurement results using a test chip fabricated for the RJ BIST circuitry described in Chapter 4. The effect of substrate noise on the signal of interest is also demonstrated with measurement results using a substrate noise injector fabricated along with the RJ BIST circuitry.

5.1 Measurement Setup

5.1.1 Test Chip and Test Board

For the validation of the RMS estimation method presented in Chapter 2, a test chip was fabricated using the 0.18\(\mu\)m CMOS technology. Figure 5.1 depicts the die photo of the test chip. The bottom part (labeled with RJ BIST) of the test chip contains circuit blocks for random jitter measurement: the circuit blocks named ‘AND-OR’, ‘VCO’, and ‘Capacitor’ are the major blocks for random jitter measurement as explained in Chapter 2 and Chapter 4. The ‘Frequency Divider’ block that comprises a counter and an output buffer is used to divide the VCO output frequency by 16 before the VCO output is delivered to an output pad: this avoids the bandwidth limitation of the output pad and its associated package pin in measuring the high frequency VCO output. The
'Counter for frequency-to-digital conversion' block is designed to convert the frequency of the VCO output into 16-bit digital values so that measurement results can be also available in a digital format.

The top part (labeled with Substrate Noise Injection Circuit) of the test chip was designed to serve two separate functions: substrate noise injection and VCO characterization. The output frequency of the VCO changes accordingly as its control voltage through an external pin varies. The design of this VCO is the same as the VCO used in random jitter measurement so that its VCO gain can be used for accurate jitter measurement, as explained in Chapter 2. The output of this VCO is also divided by 16 before it is brought to the outside of the test chip. The VCO also feeds a variable clock signal to a counter, whose outputs in turn drive the ‘noise injector’ shown in the middle of the die. The noise injector is composed of three large buffers, and these buffers drive capacitors connected to them to inject substrate noise to the jitter measurement circuitry. Depending on the purpose of this block, the counter can be either enabled or disabled.

For the measurement of the test chip, a 2-layer printed circuit board (PCB) was designed as shown in Figure 5.2. The test chip was packaged in a 68-pin Leaded Chip Carrier (LDCC), and was soldered to the test board for better signal integrity. The test board also includes clock sources for the test chip, an on-board power supply noise generator, and on-board DC power supplies. Figure 5.3 depicts the high-level block diagram of measurement setup configured to test the chip.
Figure 5.1: The die photo of the test chip. Upper part is for injecting substrate noise, and the lower part is for random jitter measurement.
Figure 5.2: The test board (the test chip sits in the upper right corner)

Figure 5.3: Measurement setup for the test chip
In the test board, a reference clock with a small amount of jitter and a jittery clock are fed to the $V_{in1}$ and $V_{in2}$ of the test chip, respectively, through clock buffers, and the amount of random jitter in the jittery clock is to be measured against the amount of random jitter in the reference clock. As a clock source, a SAW SMD-type crystal oscillator (XO) with the frequency output of 98.304MHz was used. The VCO output frequencies from both the AND operation and the OR operation carried out in the test chip are then measured to estimate the amount of jitter of interest. Although the frequency can be converted in a form of digital value and can be read through external pins, this method was not actively used in the jitter measurement since it requires an additional external pulse generator to control the counter window. The validity of this conversion was verified with circuit-level simulation, but only basic functionality was validated in the measurement.

The estimated RMS value of random jitter from the test chip was compared with $1\sigma$ value of injected random jitter to the input clock ($V_{in2}$) fed to the test chip using the histogram function in a digital oscilloscope, as shown in Figure 5.3 with dotted lines: more accurately, the additional amount of random jitter in the jittery clock was compared with the estimated RMS value from the test chip since the clean clock ($V_{in1}$) also contains a small amount of random jitter. To verify the accuracy of the jitter measurement using the aforementioned histogram function, the $1\sigma$ value from the histogram was compared to the $1\sigma$ value measured with another digital oscilloscope that measures the RMS value of random jitter by integrating the noise floor in a frequency
domain: both measurements showed similar results with around 10% to 30% errors for $10\text{ps}_{\text{RMS}}$ value, which is suspected from different probes used for measurement and different bandwidths of two oscilloscopes.

5.1.2 Design Considerations for Power Rail

Power supply noise is one of well-known sources for deterministic jitter. To avoid the power supply noise in the test board as much as possible and to provide a clean power source to both the test board and the test chip, lithium batteries were used for DC power sources to the test board. The 3.0V DC voltage from the battery was then regulated to 1.8V using a ultra low noise ($9\mu V_{\text{rms}}$ independent of $V_{\text{out}}$) CMOS low dropout (LDO) linear voltage regulator, and four of which were used in the test board as shown in Figure 5.3.

![Figure 5.4: Histogram for the crystal oscillator output](image)

Figure 5.4: Histogram for the crystal oscillator output
The crystal oscillator is powered by a dedicated voltage regulator (LDO1) along with a separate DC power source to isolate noise induced from other components on the test board. This helps in reducing jitter, especially deterministic jitter, in the reference clock. The random jitter measured using a histogram-based method at the rising edge of the output of the crystal oscillator amounted to \(10.45\text{ps}_{RMS}\), as shown in Figure 5.4. Considering the trigger jitter, \(8\text{ps}_{RMS}\), in the oscilloscope used in the measurement, as well as random jitter at the falling edge, the actual jitter becomes \(4.75\text{ps}_{RMS}\) as shown in (5.1).

\[
\sqrt{10.45^2\text{ps}_{RMS} - 8^2\text{ps}_{RMS}} \div \sqrt{2} = 4.75\text{ps}_{RMS}
\]

The RMS jitter value of the crystal oscillator from its specification is \(3\text{ps}\), and the peak-to-peak jitter value is \(25\text{ps}\). Therefore the excessive amount of jitter shown in the measurement is suspected to come from a little noisy ground plane of the test board. LDO3 in Figure 5.3 is dedicated to the RJ BIST circuitry in the test chip to minimize the effect of noise from other components on the test chip, and subsequently on measurement results.

5.1.3 Ground Plane Design

Early design decision was to isolate the ground plane for the clean clock from the ground plane for the jittery clock as much as possible so that noisy power supply for the jittery clock does not affect the clean clock signal. For a common signal ground, the isolated ground planes were then connected using narrow PCB strips. This decision, however, turned out to give an opposite
result because isolated ground planes could not provide proper return paths to the high speed signals such as the clock signal. As a result, even the crystal oscillator itself generated large ground noise amounting to 100mVpp, and this ground noise induced a large amount of jitter to the clean clock. After many trials and experiments, all ground planes were connected to each other with wide conductive strips, and more decoupling capacitors were added to the test board than the initial board design. The resulting ground noise went down to around 35mVpp, which showed an unnoticeable effect on the jitter in the clean clock.

5.1.4 Jitter Generation for the Jittery Clock

5.1.4.1 Background

In general, there are two methods in generating jitter to the signal of interest: using a phase delay modulation and using voltage noise. The method of using the delay modulation, previously, was limited to low frequency periodic jitter generation. Using the low-pass filtered output of a pseudo random binary sequence (PRBS), well-controlled amount of jitter can be generated by controlling a delay line digitally [48]. Basically this method is not different from the period modulation that is shown as the difference between two successive clock propagations through a delay line affected by slower power supply noise than signal propagation [69]. Recently, a phase delay modulation has been proven to be able to generate the controlled amount of random jitter in tester applications [47]. In that method, a pseudo random voltage se-
sequence is provided to a high-speed phase modulator to generate random jitter. When a sinusoidal voltage sequence is provided instead, periodic jitter can be generated.

On the other hand, since timing noise and voltage noise are not independent each other [44], voltage noise, or power supply noise, can also generate timing noise by converting it to timing noise, as described in (5.2) [48].

\[
\Delta T = T_r \times \frac{\Delta V}{V_{swing}}
\]

(5.2)

where \(T_r\) represents the rising time of the clock, \(\Delta V\) represents the amount of voltage noise, and \(V_{swing}\) represents the rail-to-rail swing voltage. In other words, the timing noise is proportional to both the rising time and the amount of voltage noise. This is one of active research area on the effect of power rail noise on data or clock signals [49]. This method can generate random jitter with better quality since it is not limited by the bandwidth of the random sequences, which will subsequently limit the bandwidth of the generated jitter. Also, this method can change both the rising edge and the falling edge of a clock signal independently, making the jitter more close to white noise [48].

5.1.4.2 Implementation on the Test Board

In order to inject jitter to the jittery clock signal in the test board, thus two methods can be considered: using the phase delay modulation and using power supply noise. Unlike the phase delay modulation method for injecting jitter to the clock, the method of using voltage noise can have a drawback:
injecting $V_{dd}$ noise, subsequently random jitter, with a well-controlled amount is difficult. For the random jitter generation to validate the test chip, however, injecting random jitter with the controlled amount is not of a primary concern unlike industrial jitter tolerance testing as long as the RMS value of the injected jitter amount is consistent and it can be measured using any external equipment to compare it with the measurement from the test chip.

Figure 5.5 shows how the Vdd noise generator in the test board was implemented. A crystal oscillator with the frequency output of 100MHz introduces $V_{dd}$ noise to the power rail from LDO4 to make it the noisy Vdd shown in Figure 5.3. The frequency of the noise is almost uncorrelated to the $V_{dd}$ noise in the jittery clock buffer in Figure 5.3, whose frequency is 98.304MHz. The crystal oscillator can be turned off by controlling Enable 1 signal when needed.

Figure 5.5: Generating the noisy Vdd using a crystal oscillator and clock buffers
On top of the $V_{dd}$ noise caused by the crystal oscillator, enabling clock buffers one at a time can add more $V_{dd}$ noise to the noisy power supply. When the first clock buffer is enabled, the $V_{dd}$ noise increases by the switching activity from the clock buffer. In addition, due to a slight phase delay from the clock source to the clock buffer, the $V_{dd}$ noise can be more distributed. If it is desired to further increase the amount of jitter in the jittery clock, load capacitors can be added to the outputs of each clock buffer to make the switching noise more worse. It needs to be mentioned that the generated $V_{dd}$ noise becomes weaker through the PCB trace impedance when it reached the target clock buffer: the amount of $V_{dd}$ noise that the clock buffer for the jittery clock sees depends on the PCB trace impedance between the noise source and its receiver.

For the load capacitors, the following combinations were used in the measurement: no capacitor, one 4$pF$ capacitor to each clock buffer, one 22$pF$ capacitor to each clock buffer, a 4$pF$ capacitor and a 22$pF$ capacitor to each clock buffer, and a 4$pF$ capacitor and a 22$pF$ capacitor to one clock buffer while another clock buffer has only a 4$pF$ capacitor. In the measurement, the third buffer controlled by Enable 4 was not used since it turned out to introduce an excessive amount of periodic jitter to the jittery clock.

Figure 5.6 shows the injected jitter values to the test chip. In ideal case, the RMS value of the jitter in the clean clock should remain the same even if the RMS value of the jitter in the jittery clock increases, but in reality, the RMS values in the clean clock were also affected especially when the RMS value in the jittery clock exceeds 40$ps$. To obtain the RMS value of the injected
jitter to the test chip, the root of the difference of squares of the RMS values, i.e., the RMS value of the jitter in the jittery clock and the RMS value of the jitter in the clean clock, was used. The result was then divided by $\sqrt{2}$ to obtain the jitter value only at the rising edge. The trigger jitter in the oscilloscope does not affect the calculation of the RMS value of the injected jitter since the trigger jitter occurs in both the clean clock and the jittery clock. Table 5.1 shows the configurations of the on-board $V_{dd}$ noise generator for all experiments shown in Figure 5.6.

The use of a voltage regulator with larger output noise of $250\mu V_{rms}$ was an another consideration for the jittery clock generation, but this did not help due to the larger $Vdd$ noise ($20mV_{pp}$) when all components in the test board
Table 5.1: Configurations of the on-board $V_{dd}$ noise generator

<table>
<thead>
<tr>
<th>Exp. No.</th>
<th>XO Stat.</th>
<th>Buffer 1</th>
<th>Buffer 2</th>
<th>RJ [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Stat.</td>
<td>Load1</td>
<td>Load2</td>
<td>Stat.</td>
</tr>
<tr>
<td>1</td>
<td>Off</td>
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<td>22pF</td>
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Note: All jitter values are in their RMS values. Experiments 1, 5, 20, and 21 have the same configurations as experiments 2, 6, 22, and 19, respectively, but the buffer 1 and the buffer 2 were disconnected.
5.1.4.3 Deterministic Jitter in the Jittery Clock

When jitter was generated using the $V_{dd}$ noise generation circuitry in the test board, it was not successful to generate a large amount, e.g. more than $10\text{ps}_{\text{RMS}}$, of random jitter without introducing deterministic jitter together. As a result, the jitter generation method added both random jitter and deterministic jitter to the jittery clock when large amounts of jitter were generated. Figure 5.7 shows a histogram resulted from the jitter generation method, where both a random jitter component and a deterministic jitter component exist together. The added deterministic jitter is suspected from the use of the low frequency crystal oscillator for the jitter generation. In our case, the deterministic jitter component can be mostly composed of periodic jitter since low frequency power supply noise is one of sources for periodic jitter.

When there is only a random jitter component in a clock signal, its probability density function follows a Gaussian distribution. In other words, when a histogram is constructed at the rising edge of the clock with enough samples, the probability of those samples within $\pm 1\sigma$ in the histogram should approach 0.6827, and the probability within $\pm 2\sigma$ should approach 0.9545. The $\pm 1\sigma$ value in Figure 5.7, however, shows 0.649 due to deterministic jitter, and this can contribute to measurement errors when the test chip is validated using the injected jitter with the deterministic jitter component. Therefore, among many cases of injected jitter, only the cases in which the periodic
Figure 5.7: Histogram showing both random jitter and periodic jitter. The hits in the histogram accumulated more than 20,000 hits.

jitter component does not dominate in the injected jitter were chosen in the validation of the test chip to minimize the measurement error, and separate error analyses were carried out that consider the deterministic jitter.

5.2 Measurement Results
5.2.1 VCO Characterization

Before actual jitter measurement, the VCO in the test chip was first characterized for the accuracy of measurement results. This characterization can also help in determining the process corner of the fabricated chips so that the process information can be used in a further error analysis if needed. Figure 5.8 shows the configuration in the test chip when the VCO is being character-
ized. The main part of the substrate noise injection circuitry is disabled by an external control switch (Enable) on the test board, and the VCO frequencies that are divided by 16 are measured while varying the control voltage to the VCO.

Figure 5.9 shows the VCO curves over its control voltage from three test chips. All three curves showed desired linear regions when the control voltage ranges from 0.8V to 1.0V. Figure 5.10 compares the VCO curves from test chips to VCO simulation results that are shown in dotted lines. Figure 5.10(b) focuses on the linear region of the VCO curves for a better comparison.
The curves from tests chips lie between the typical corner and the slow corner, but the actual process corner can be more close to the typical corner if we have to consider a small voltage drop from the external pin for the $V_{\text{Control}}$ to the circuitry in the die.

### 5.2.2 Random Jitter Measurement

For the random jitter estimation as described in Chapter 2, the frequency outputs from both the AND operation and the OR operation were measured for each jitter value. Figure 5.11 shows waveforms from the AND and OR operations, where the frequency of the OR operation (Figure 5.11(b)) is higher than that of the AND operation (Figure 5.11(a)) due to more jitter.
Figure 5.10: VCO curve measurements vs. post-layout simulation: the top dotted line for a FastFast corner, the middle dotted line for a Typical corner, and the bottom dotted line for a SlowSlow corner.
in the jittery clock than the clean clock. The measured frequency values are then used to convert into the amount of the random jitter in the clock signals using the VCO characterization results.

The random jitter values were then compared to the jitter values measured at the input clock signals to the test chip, where the latter is obtained from the $1\sigma$ value in the histogram using an external oscilloscope. The oscilloscope used for the measurement, Agilent Infiniium MSO 8104A, has a bandwidth of 1GHz, and its maximum sampling rate is 4Gsa/s. A passive probe was used for the measurement to avoid any additional random jitter from the probe itself, and the system rising time of the probe is less than 700ps. The rising time of the clock signal measured using the oscilloscope is an added RMS value of both the actual rising time of the signal and the rising times of the probe and oscilloscope [48], as shown in (5.3).

\[
T_{r,\text{measured}} \approx \sqrt{T_{r,\text{actual}}^2 + T_{r,\text{probe}}^2 + T_{r,\text{scope}}^2} \quad (5.3)
\]

Since the rising time of the clock signal measured is around 3ns, the rising time of the probe is less than 700ps, and the rising time of the oscilloscope is 350ps (the bandwidth of the oscilloscope is two times that of the probe), the actual rising time of the signal in the worst case would be as follows.

\[
T_{r,\text{actual}} \approx \sqrt{(3\text{ns})^2 - (0.7\text{ns})^2 - (0.35\text{ns})^2} = 2.896\text{ns} \quad (5.4)
\]

Thus, the bandwidth of the probe is not limiting the measurement much.

Figure 5.12 shows the RMS estimation results for random jitter using measurement results from test chip 2 with 22 different injected random jitter
Figure 5.11: Frequency outputs from the AND and OR operations. The OR operation always results in a higher frequency than the AND operation: 17.237MHz vs. 17.068MHz.

values. The blue circles represent the estimated RMS jitter values, and the blue solid line shows the trend of the estimation with a polynomial curve fitting. The red dotted line represents post-layout simulation results at a typical process corner. The RMS estimation results follow the simulation results, but with less measurement errors. Table 5.2 shows the injected RMS jitter values, the estimated RMS jitter values, and estimation errors.

5.2.3 Deterministic Jitter Compensation

When there is a periodic jitter component in total jitter, the probability distribution of the total jitter does not follow a Gaussian distribution since its resulting distribution comes from the convolution of a Gaussian distribution and the periodic jitter distribution. The dotted lines in Figure 5.13 show examples of the resulting probability distribution when both the periodic jitter
Table 5.2: Random jitter measurement results

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<td>36.39</td>
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component and the random jitter component exist. In this case, the standard deviation of the distribution increases due to the periodic jitter component, and the corresponding average jitter value (the area inside the solid blue line in Figure 5.13) also increases. This can be interpreted in the following way: compared to an ideal Gaussian distribution shown in Chapter 2, the probability of jitter with a large magnitude increases, and subsequently the average jitter value becomes bigger.

Although the constant used for converting the average jitter value to its RMS value, $K_{AVGtoRMS}$, changes accordingly with the periodic jitter, it is
Figure 5.13: Revised probability distributions and corresponding jitter magnitude distributions considering a periodic jitter component not changing too much since both the average value and the RMS value increase. For instance, if the peak-to-peak value of the periodic jitter amounts to 10ps, the $K_{AVGtoRMS}$ becomes 1.1858, and if the peak-to-peak value amounts to 24ps, the $K_{AVGtoRMS}$ becomes 1.2226. The blue dotted lines in Figure 5.14 show the compensated estimation results for two different periodic jitter amplitude values when the periodic jitter exists in the jittery clock. Although the compensated results in Figure 5.14 guides on the direction of the compensation for the periodic jitter, but they do not lead to an accurate compensation method since the amplitude of the periodic jitter is not constant across all measurement points.
Figure 5.14: Random jitter estimation results when the periodic jitter components in the jittery clock are compensated (blue dotted line above the trend of measured jitter)
5.3 The Effect of Substrate Noise on the Measurement

5.3.1 Substrate Noise Generation

Substrate noise induced from switching activities in digital logic is another source of random jitter in a clock signal. Some digital logic used in BIST circuitry for random jitter measurement, such as a counter, can inadvertently induce substrate noise to the SUT, and this can affect measurement accuracy depending on the implementation technique of the BIST circuitry.

This section demonstrates that substrate noise can add random jitter to the VCO output, using measurement results. Figure 5.15 shows the con-
configuration for the experiment. The *Substrate Noise Injector* in the test chip comprises a VCO, a 15-bit counter, three strong buffers, and capacitors attached to the buffers. The VCO provides a clock to the counter, and three counter outputs, $Q_1$, $Q_4$, and $Q_9$, drive the buffers, and in turn the capacitors. The similar approach was presented in [42], which showed how digital switching noise causes PLL jitter. Unlike the approach used in [42], where driving clocks for the noise generator are provided from outside the test chip, the internal VCO output drives the digital switching logic so that power supply noise, including ground noise, is not affecting the measurement result.

In the experiment, the external control voltage, as shown in Figure 5.15, was swept from 0V to $V_{dd}$ so that the VCO output frequency changes accordingly from a low frequency to a high frequency. The VCO output frequency can be measured using an external oscilloscope. The VCO also feeds a clock to the 15-bit counter, and the counter can be turned on or can be turned off by controlling an external switch on the test board. By doing this, the effect of substrate noise on the SUT, the VCO output from the RJ BIST, can be isolated from power supply noise. To compare the amounts of random jitter in the SUT with and without the induced substrate noise, the histogram function of the external oscilloscope was used to extract the RMS values of random jitter in the SUT.
Figure 5.16: RMS jitter values in the VCO (from RJ BIST) output clock when the VCO frequency of the Substrate Noise Injector changes

5.3.2 Measurement Results

Figure 5.16 shows how RMS jitter values increase due to the substrate noise as the VCO frequency is raised. The RMS jitter values at higher frequencies when the substrate noise injector is turned off also increased, and this can be attributed to the intervention to the measurement setup. For each VCO frequency measurement, the external control voltage had to be adjusted accordingly, and this involved a new probe connection to the clock output.

For a better controlled experiment, another measurement was performed without intervening the measurement setup except the change of the control voltage. The control voltage is adjusted by a variable resistor, or a
Figure 5.17: RMS jitter values in the VCO (from RJ BIST) output clock at the maximum and minimum frequencies of the VCO in the Substrate Noise Injector trimmer, on the test board. In this measurement, only the maximum frequency and the minimum frequency of the VCO were used since those two test conditions can be easily attained by turning the trimmer to its limit in either a clockwise direction or a counterclockwise direction. This experiment was repeated five times in an alternating matter: one measurement with the counter turned on, then another measurement with the counter turned off. Figure 5.17 shows the measurement results for this experiment, and Figure 5.18 shows the histograms for one of measurements in Figure 5.17(a).

5.4 Limitation of Measurement

Although the BIST circuit was designed to measure random jitter in a clock signal with a wide range of frequency up to 1GHz, its validation was
focused on the 100MHz clock, more accurately 98.304MHz, due to the following measurement issues: signal integrity in the test board, the availability of parts for the test board, and the jitter generation method on the test board. Designing a test board that can address signal integrity for clock signals with several hundred MHz is not simple because of ground noise in the test board. High $di/dt$ events from the clock buffers induce ground noise, which subsequently contributes to the jitter in the signal of interest. The 100MHz clock buffers introduced the ground noise of around $35mV_{pp}$ when they are operating even if near-end termination was properly done to all clock signal paths. This ground noise becomes worse when the clock frequency increases. In addition, the maximum frequency supported by a discrete clock buffer was 125MHz.

Another reason of choosing a low frequency clock is for jitter generation in the clock signal. As shown in (5.2), the timing jitter in the clock is proportional to the rising time of the clock signal as well as the voltage noise: the
higher clock frequency makes the jitter generation more difficult. In addition, the ringing in the power rail becomes severe when a higher clock frequency, or a faster rising time, is used, and this also results in undesired deterministic jitter [48]. Thus, the clock frequency in the measurement was limited to 100MHz for the practical reason.

There have been many research on jitter measurement using both external bench testers and BIST circuits, but not many of them provide random jitter measurement results with good linearity. For industries that perform jitter tolerance testing, they are focusing on the validation of jitter in SUT, not on the validation of BIST circuits for jitter measurement. In addition, generating a controlled amount of random jitter is still on-going research area [47]. On the other hand, many BIST circuits for random jitter measurement are proposed and designed in academia, but proper testing equipment for random jitter generation is usually not available, which is essential for validating the BIST circuits. As a result, the validation of measurement linearity in the BIST circuit for random jitter measurement barely happens. To overcome this limitation, many test points were used in validating the test chip (RJ BIST) with the on-board $V_{dd}$ noise generator, but those test points were limited to relatively low jitter values compared to circuit-level simulation runs.

5.5 Summary

In this chapter, the measurement results from the test chip have been presented to show the validity of the random jitter estimation method pro-
posed in Chapter 2. Although the clock frequency was limited to 98MHz, the linearity of the measurement was proven to be comparable to the simulation results. The effect of substrate noise on the SUT was also demonstrated with measurement results using the substrate noise injector in the test chip, and the results indicate that another type of jitter measurement method is required, which will be presented in the next chapter.
Chapter 6

Indirect Method for Random Jitter Measurement on SoCs using Critical Path Characterization

This chapter presents a novel method of measuring random jitter without using any dedicated jitter measurement circuit, which also considers the worst case random jitter that can come from power supply noise as well as substrate noise induced by switching activities from digital logic blocks that use the clock of interest as a clock source. For the validation of the method developed here, circuit-level simulation results are shown first, then measurement results using an external tester, ATE, on one of the latest SoC product follow. The advantage and drawbacks of the proposed idea along with possible future work for further improvement are also presented.

6.1 Indirect Measurement Method for Random Jitter Measurement

6.1.1 Motivation for the Indirect Method

In the previous chapter, it was shown that substrate noise can affect the SUT or jitter measurement accuracy by disturbing $V_{th}$ of CMOS transistors. When the substrate noise disturbs the clock signal, it manifests itself as
random jitter in the clock. As technology advances to reduce feature sizes, the density of transistors consequently increases, and the disturbance caused by the substrate noise can be more severe. For critical analog circuit blocks, e.g. a PLL, special care such as the use of guard rings can be given to them to minimize the effect of the substrate noise when a high-resistive substrate was used, but this is not a practical solution to the clock distribution network (CDN), which provides clock signals to the logic across the entire SoC for a timing or synchronization purpose. As such, a method for measuring the random jitter in the clock signal when the clock is in its functional state, not in a test mode, is required.

Jitter measurement on clock signals has been an active research area, and many designs and ideas have been proposed for BIST circuitry for jitter measurement, as described in Chapter 1. Although BIST approaches have the merit of accessing the target clock signal without much degradation of signal integrity compared to the approaches using external bench equipment or testers, they are not aiming at measuring jitter at the end of the CDN but at the output of the clock generating circuit such as the PLL. Therefore, even the BIST approach can fail in providing accurate timing information required for determining timing margins since the measured jitter at the clock generating circuit does not reflect the actual jitter the logic at the end of the CDN sees.

Many of BIST solutions also require another clock signal in a separate form to use it as a reference clock signal either for measurement or for calibrating the BIST circuits. In many cases, the reference clock signal is not
readily available, and the unknown magnitude of jitter in the reference can degrade the accuracy of the measurement even if it is available. However, compensation for the jitter in the reference signal is often neglected. Some of recent BIST circuits [13, 14] incorporate special circuitry to generate a delayed version of SUT by an exact amount of one period to overcome the needs for the reference clock signal, but the jitter in the SUT itself is often missed when the exact amount of delay is generated. Moreover, complicated circuit design, such as a measurement circuit using the vernier principle, requires careful calibration steps before actual measurements due to process variations which are increasing in deep sub-micron technology [35].

The method developed in this chapter measures the random jitter of the clock signal in the SoC using an ATE, or a low-cost production tester, without any use of BIST circuitry. This is attained by exploiting shmoo plot in the tester while leveraging tester period resolution in the shmoo plotting with a frequency multiplying PLL in the SoC. Critical paths and their associated functional test patterns identified during the characterization of the maximum operating frequency, or \( F_{max} \), of the microprocessor in the SoC are used for the shmoo plotting. If the period of the clock signal is swept with a very fine step size, e.g., 1ps, in the shmoo plotting around the \( F_{max} \), and scattered test pass/fail results from a sizable number of shmoo plots are overlapped, the resulting distribution of the test fail can represent the standard deviation of the random jitter in the clock signal, since the functional tests fail due to a timing uncertainty in the clock signal.
A similar type of inconsistent fail was also reported in the scan-based delay test, where tester timing uncertainties caused multiple scan flip-flops to fail to capture bits if marginal test clock periods were applied [54]. The authors also proposed to use an enough guard band in the test clock period to avoid test escapes, or suggested the use of an on-chip PLL to address both the test escape and yield loss. The proposed method in this chapter, however, makes proactive use of the test fails resulting from timing uncertainties rather than avoiding them, and measures the clock jitter seen by the critical path to achieve more accurate estimation of a timing budget in the design phase.

Although the proposed method measures the clock jitter indirectly without the use of any dedicated BIST circuit, the resulting measurement can be more accurate than other previous methods for the following reasons. First, there is no modification of the SUT in the proposed method. Second, there is no additional noise induced by the added measurement circuitry or reference clock signal through power supply, crosstalk, or substrate. Finally, the true clock jitter seen by the most critical paths can be measured.

6.1.2 Achieving Sub-picosecond Resolution for Jitter Measurement

Shmoo plotting can provide very condensed information in debugging a new microprocessor or SoC product [8], and $V_{dd}$ versus period shmoo plotting is widely used for validating performance of devices-under-test (DUTs), test contents stability, $V_{min}$, or $F_{max}$. Typically its pass/fail signature is difficult to apply in validating analog circuits or mixed-signals such as clock jitter.
However, if a fine period step size, such as a few picoseconds, is used in the typical $V_{dd}$ versus period shmoo plotting, the discrete pass/fail signature can expose the analog behavior of the clock signal, making it possible to use the shmoo plotting for clock jitter measurement or characterization.

Achieving picosecond resolution, or sub-picosecond resolution, in the tester clock period (or tester period) from production testers may not be a viable option for many low-cost testers although such a resolution is required for jitter measurement or characterization. However, a frequency multiplying PLL, which can be found in most microprocessors or SoC products, can serve as a period divider to overcome that limitation. In other words, the picosecond resolution can be attained by utilizing the relationship between the tester clock period and the output clock period of the PLL that uses the tester clock for its reference, thus making the low-cost testers suitable for clock jitter characterization.

### 6.1.3 Critical Paths Characterization

In validating the maximum operating frequency of a microprocessor, many potential critical paths are sensitized using a number of functional test patterns. Structural tests, which are less expensive for test writing, can also be used for delay testing, but they tend to undergo more power supply noise near clock edges due to simultaneous switching, leading to more pessimistic results [61]. To sensitize the critical paths, the $V_{dd}$ versus period shmoo plotting can be used to identify the most critical paths at the worst case temperature.
Figure 6.1: A typical shmoo plot (fictitious) from debugging critical paths within the design specification. Among information from the resulting shmoo plots are failing test patterns, failure signatures, and failing test vector addresses in the corresponding test patterns. Shmoo plots also reveal a pass/fail boundary since each test pattern is tested at increasingly higher, or decreasingly lower, clock frequency at each voltage. Figure 6.1 shows a typical $V_{dd}$ versus period shmoo plot from debugging critical paths, and Figure 6.2 depicts a high-level diagram for the critical path characterization in a SoC using a tester.

When the test fails not because of random defects but because of process-related speed variation, many parts share a small number of failure signatures [39], thus identifying the critical paths. The proposed method uses a functional test pattern that fails at the lowest clock frequency at a given $V_{dd}$
among a number of functional test patterns, which are written for the $F_{\text{max}}$ characterization. Note that the proposed method utilizes an already existing functional test, and does not require developing or writing a new functional test, which is usually expensive.

6.1.4 Constructing a CDF from Shmoo Plotting

Usually the shmoo study is done by sweeping the test period with a coarse step size. If we sweep the test period with a much finer step, e.g., 10ps, around the boundary of pass/fail condition, the boundary will include inconsistent pass or fail as shown in Figure 6.3(a), unlike the case that a coarse step was used. In this case, if we fix a Y-axis variable, i.e., $V_{dd}$, and obtain the same shmoo plot multiple times, we can see a higher chance of test fail at a
(a) One-dimensional shmoo with a fine step size (10 ps)

(b) One-dimensional shmoo plots with a fine step size from multiple attempts

Figure 6.3: Inconsistent test fails around the pass/fail boundary in a shmoo with a fine step size smaller period than at a larger period rather than a solid pass or fail. This can be interpreted as the probability of test fail at each period point (X-axis). For example, when 1D-shmoo plotting corresponding to the thick rectangular box in Figure 6.1 is performed five times with a fine step size of 10 ps, the resulting shmoo plots will show the inconsistent pass or fail at each period step as shown in Figure 6.3(b) between solid passing and failing regions. The probability of test fail will increase as the test period in the shmoo decreases as depicted in Figure 6.4, and the resulting distribution will construct a CDF whose standard deviation reflects the standard deviation of the random jitter from the clock signal seen by the critical path. If a significant amount of deterministic jitter
Figure 6.4: The probability of test fail across the test period from the multiple shmoo plots in Figure 6.3(b)

exists in the clock jitter, it will also appear in the distribution.

The measured jitter can represent the aggregated jitter seen by the critical path, rather than just the PLL output jitter. The power supply noise can contribute to the jitter through jitter amplification on the clock jitter originated from the PLL as well as dynamic skew variation in clock distribution trees [41, 60]. The aggregated timing uncertainty seen by the critical path is more important in most cases than the PLL output jitter itself when we consider what is contributing to the timing slack in the critical path delay. Static skew variation and static delay change in the delay of the critical path due to static IR drop [61] would not be seen in the probability distribution obtained from the shmoo plots since they would remain constant in the shmoo plotting when the test period varies with a very fine step. Note that the process variation and temperature are not of concern here since the shmoo plots come from a single DUT and temperature can be well controlled in the production tester except small temperature fluctuations induced by self-heating during
6.1.5 Shmoo Plotting with a Fine Step Size

The tester period resolution in low-cost testers can be too coarse as it is to characterize the aforementioned jitter, but this can be easily overcome by using a PLL inside a microprocessor or in a SoC and by understanding how the clock frequency that the critical paths see is related to the clock frequency of the tester clock. In modern microprocessors or SoCs, the use of frequency multiplying PLL(s) is essential to avoid signal integrity issues that can arise when a high frequency clock is directly driving the chips.

Assume that the tester provides the reference clock to the PLL, which is true in most of silicon validation using a tester, and that there is only one PLL between the reference clock and the target critical path as shown in Figure 6.2. If the PLL is supposed to multiply its reference clock by 10, i.e., the ratio of feedback path division to forward path division is configured to 10, when the tester provides a 100MHz reference clock (RefCLK), or 10\(\text{ns}\) in period, the period of the PLL output (CLK) becomes 1\(\text{ns}\). This relationship is illustrated in Figure 6.5(a). As a result, if the period of RefCLK increases by 10\(\text{ps}\), then the period of the CLK increases by 1\(\text{ps}\) as follows.

\[
\text{CLK}_{\text{Period}} = \frac{10.01\text{ns}}{10} = 1.001\text{ns}
\]  

Thus, if sweeping the period of CLK by \(\pm 100\text{ps}\) around the \(F_{\text{max}}\) with the step size of 1\(\text{ps}\) is desired for the jitter measurement, the tester just needs
Figure 6.5: The relationship between a tester clock period and a PLL clock period to sweep the period of the RefCLK by ±1ns with the step size of 10ps, not 1ps. Sub-picoseconds resolution can be achieved when the PLL feedback divider is configured to above 10 or the period step change in the tester is below 10ps, and both cases are not unusual nowadays. Figure 6.5(b) depicts this relationship, where the $dT_{REF}/2$ represents the amount of change in the RefCLK period and $dT_{PLL}/2$ represents the amount of change in the CLK period.

The EPA in tester clock signals usually exceeds tens of picoseconds, but the desired specification in this case is not the absolute accuracy but the
preciseness in increasing or decreasing the test rate, or the test rate resolution [21]. The test rate resolution is usually smaller than the EPA by more than an order of magnitude. Jitter in the tester clock signal can still affect the validity of the proposed idea, but high frequency components of the jitter outside the loop bandwidth of the PLL will mostly be filtered out.

Moreover, low frequency components of the jitter would not be a big problem since the timing uncertainty in the critical paths is affected by period jitter, not by the absolute jitter. Multiple PLLs are now common in the SoC implementation to provide various clock frequencies to the entire SoC, and some of those PLLs can be cascaded. The previously mentioned relationship between the periods of \texttt{RefCLK} and \texttt{CLK} still holds for this cascaded clocking architecture while the cascaded PLLs can filter out the jitter in the reference clock better.

### 6.2 Circuit Simulation

#### 6.2.1 Modeling and Simulation Setup

The proposed method was first validated with circuit-level simulations of an open source microprocessor, OR1200 [51], using Hspice. The circuit used in the simulation is composed of a power delivery network, a jittery clock source assumed to be a PLL output, a critical path, and clock buffers between the clock source and the critical path. To model the power delivery network, the distributed power delivery model in [25] was modified to a $3 \times 3$ on-chip grid model, as shown in Figure 6.6, with associated RLC parameters in Table
Figure 6.6: A $3 \times 3$ on-chip power grid which was instantiated for both a $V_{dd}$ grid and a $V_{ss}$ grid. In the on-die grid model, $C_{Bulk}$ represents the intrinsic parasitic capacitance of a functional block, and $C_{Space}$ represents the decoupling capacitance [25].

6.1. The $3 \times 3$ on-chip grid model was then instantiated for both a $V_{dd}$ power grid and a $V_{ss}$ power grid. A package model was not used since its response time is usually larger than the grid model by an order of magnitude, and most switching activity occurs in the early clock cycle [68]. For the $V_{dd}$ and $V_{ss}$ sources connected to the on-chip grid model, random Gaussian noise was modeled using Matlab and was added to the $V_{dd}$ and $V_{ss}$ sources instead of using ideal values.

For the critical path modeling, the critical path identified from the OR1200 by PrimeTime was used, but all fan-out paths were removed for simplicity of simulation and analysis. The critical path was placed at the center of the on-die grid model. The jittery clock signal was modeled to have a Gaus-
Table 6.1: RLC Parameters used in Figure 6.6 [25]

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Value</th>
<th>Inductance</th>
<th>Value</th>
<th>Capacitance</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{Bump}}$</td>
<td>40mΩ</td>
<td>$L_{\text{Bump}}$</td>
<td>72pH</td>
<td>$C_{\text{Bulk}}$</td>
<td>0.12nF</td>
</tr>
<tr>
<td>$R_{\text{Grid}}$</td>
<td>50mΩ</td>
<td>$L_{\text{Grid}}$</td>
<td>5.6fH</td>
<td>$C_{\text{Space}}$</td>
<td>1.5nF</td>
</tr>
</tbody>
</table>

Gaussian distribution, and Monte Carlo simulation was used in a way that each simulation run exhibits different amounts of period jitter with a predefined RMS value.

Since static clock skew from clock distribution trees does not contribute to the simulation result in the proposed idea, library clock buffers were used to model the effect of power supply noise on the buffer output. All jitter measurements were performed at the output of the clock buffers to see what the critical path undergoes. All circuits were modeled using a 0.18µm technology and its associated standard cell library.

To mimic one dimensional shmoo in the simulation, the period of the clock source was swept around the period where the critical path is marginally passing when there is no clock jitter. The step size of the sweeping was set to 4ps, and a total of 40 steps were used. The Monte Carlo simulation was performed 100 times at each period to obtain the distribution of test fail.

6.2.2 Simulation Result

Figure 6.7 depicts the simulation results that show the probability of test fail over the clock period for the different RMS values of the period jitter.
In the simulation the test is considered fail when the output of a capture flip flop in the critical path could not make an expected transition and made it at the next clock cycle. As shown in Figure 6.7, the probability of test fail gradually increases as the clock period decreases, thus resulting in the cumulative distribution of the test fail. The clock period was swept by 4\( \text{ps} \), and each distribution curve was constructed from 100 simulation runs at each clock period.

For the estimation of the RMS values that correspond to the 1\( \sigma \) values of the distributions, each cumulative distribution was first converted into a probability density function, then the 1\( \sigma \) value from each probability density
function was estimated using the maximum likelihood estimation (MLE) in Matlab. Figure 6.8 depicts the trend of the jitter estimation to the injected jitter values, where the estimated RMS values are closely following the injected jitter values, and Table 6.2 shows the estimated period jitter values compared to the injected period jitter values, both in the RMS values, showing up to 3% estimation error.

![Graph showing linear trend of estimated jitter values to injected jitter values](image)

Figure 6.8: Linear trend of estimated jitter values to injected jitter values

### 6.3 Measurement on a SoC using a Tester

To prove the proposed idea on silicon, measurements on one of the latest SoC products were carried out using the same approach as used in the simulation. For the shmoo plotting, a production tester was used, and for PLL
Table 6.2: Comparison of estimated jitter values to injected jitter values

<table>
<thead>
<tr>
<th>Injected Period</th>
<th>RMS Estimation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jitter in RMS [ps]</td>
<td>Estimated Value [ps]</td>
</tr>
<tr>
<td>5.6</td>
<td>5.7</td>
</tr>
<tr>
<td>6.9</td>
<td>7.1</td>
</tr>
<tr>
<td>8.3</td>
<td>8.4</td>
</tr>
<tr>
<td>9.7</td>
<td>9.9</td>
</tr>
<tr>
<td>11.1</td>
<td>11.2</td>
</tr>
<tr>
<td>12.5</td>
<td>12.6</td>
</tr>
<tr>
<td>13.9</td>
<td>14.0</td>
</tr>
<tr>
<td>15.2</td>
<td>15.4</td>
</tr>
<tr>
<td>16.6</td>
<td>16.8</td>
</tr>
<tr>
<td>18.0</td>
<td>18.1</td>
</tr>
<tr>
<td>19.4</td>
<td>19.5</td>
</tr>
<tr>
<td>20.7</td>
<td>20.7</td>
</tr>
<tr>
<td>22.1</td>
<td>22.4</td>
</tr>
</tbody>
</table>

jitter measurements, an oscilloscope was connected to a high bandwidth analog debug output, which can bring out the clock from the main clock grid, in the target SoC through the tester load board. Since the proposed idea utilizes the PLL that provides a high frequency clock to the target critical path, the PLL would filter out considerable amount of jitter in the tester clock.

The effectiveness of the filtering depends on the bandwidth of the PLL that acts as a low pass filter to the phase noise in its reference clock, which is the tester clock in this case. In general, depending on the design purpose of the PLL as well as the phase noise contribution from the reference clock and the VCO, the loop bandwidth of the PLL can be optimized. Normally half
of phase noise power is within the PLL loop bandwidth and the remaining is outside the bandwidth [7], where the latter is dominated by the VCO noise, not by the jitter in the reference clock. Since the SoC used in the measurement uses cascaded PLLs in the clock path from the tester clock to the target critical path, the contribution of the tester clock jitter to the jitter in the final clock signal is assumed to be negligible. Although the jitter in the tester clock was not measured based on the above assumption, it is known to have a Gaussian distribution, meaning that a random jitter component dominates in the tester clock jitter [18, 54], which spreads out over entire frequency range in the frequency domain.

6.3.1 Constructing a CDF from Shmoo Plots

For the critical path and a target functional test pattern selection, 2-dimensional $V_{dd}$ versus period shmoo plotting was carried out to identify one test pattern that gives speed-path type failure [39] from a suite of functional tests that are written to validate the maximum operating frequency of the microprocessor in the SoC. For the rest of all shmoo plotting and PLL jitter measurements, only the identified test pattern was used for consistency of the measurements.

For different amounts of period jitter, five pairs of $V_{dd}$ and clock frequency were randomly selected with more detailed 2-dimensional shmoo plotting because it is not so easy to control the amount of period jitter, which the critical path sees, as done in the simulation. The clock frequencies were cho-
sen in a way that the test starts to marginally fail at each $V_{dd}$ value. For each $V_{dd} - frequency$ pair, a $V_{dd}$ versus period shmoo plot with a very fine step size in period was obtained. Although 2-dimensional shmoo plotting was used to find the probability of test fail, the test program setting was modified so that the $V_{dd}$ remains constant when frequency is being swept. This is the same as testing the test pattern as many times as the number of the steps in the Y-axis (for the $V_{dd}$) at each period point. This made it possible to obtain hundreds of 1-dimensional shmoo plots easily, thus being able to construct the cumulative distribution of the test fail by just utilizing the shmoo capability incorporated in the tester environment without resorting to writing a new script for it.

After obtaining all shmoo plots, all the failing points were checked again to confirm that the failing signatures are the same before constructing the cumulative distributions of the test fail from the shmoo plots. The cumulative distributions of test fail constructed for the five different $V_{dd} - frequency$ pairs did not show very smooth shapes, which can result from the limited sample size. Figure 6.9 depicts the distributions aligned at the middle of probability of test fail after applying a moving average to smooth the distributions. The RMS value from each distribution was estimated with the same method as used in the simulation.

6.3.2 Measurement Results

To validate the estimated RMS values from shmoo plots, the period jitter in the clock from the clock grid was measured using the oscilloscope, and
Figure 6.9: Probability trends of test fail from tester shmoo plots across clock period (after applying a moving average to smooth the curves)

the measured RMS values were compared with the estimated RMS values. Due to the randomness of the jitter, the sample size needs to be determined first in measuring the jitter using the oscilloscope. Figure 6.10 shows the trends for both peak-to-peak values and corresponding RMS values of the period jitter. It can be seen that both trends become constant beyond 500K samples. Therefore, all measurements done with the oscilloscope used 500K as a sample size.

Figure 6.11 compares both estimated RMS values from shmoo plots with measured RMS values from the oscilloscope, where both estimated values and measured values are normalized to their average values, respectively. To
Figure 6.10: Dependency of the peak-to-peak value and the RMS value of the jitter on the size of sample when the jitter was measured using an oscilloscope.

confirm the repeatability of this experiment, both the shmoo plotting and the oscilloscope measurement were repeated three times for a $V_{dd} - frequency$ pair with a consistent result. The measured period jitter values from the oscilloscope are actually much larger than the estimated jitter values. This can be explained in the following way. Although the high bandwidth analog debug output was used to bring out the clock signal from the clock grid, the measured jitter would not represent the jitter that the speed path actually sees. This is because the signal path and output buffers between the clock source and the output pad amplify the jitter of interest with $V_{dd}$ noise and ground noise. Therefore, for better comparison, the use of a dedicated BIST circuit designed for jitter measurement is desirable so that the jitter amplification can
be avoided or minimized, which was not the part of this measurement.

![Figure 6.11: RMS values extracted from shmoo plots compared to oscilloscope measurements](image)

**6.3.3 The advantage and drawbacks of the proposed idea**

The advantage of the proposed method for random jitter measurement is to accurately estimate the jitter that the critical paths actually undergo without resorting to any special BIST circuitry or to external bench instruments. More importantly, the estimated jitter value from shmoo plots provides aggregated information rather than the PLL clock jitter since many possible noise sources such as crosstalk, dynamic skew variations, and power supply noise inside a SoC manifest themselves in the form of timing uncertainty. When there is a considerable amount of deterministic jitter in the timing un-

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certainty, a jitter decomposition technique such as the tail-fitting method [45] can be applied to the resulting probability distribution of test fail.

The contribution of dynamic power supply noise to the estimated RMS value is difficult to isolate, but it can be mitigated based on the fact that temporal power supply noise can increase or decrease the delay of the combinatorial logic [10, 26] and that the critical path is the longest delay path that is composed of the logic gates. Thus, an interesting experiment would be to apply the proposed method to several different logic paths to compare the estimated jitter, or to apply the proposed method to both functional tests and structural tests to see the effect of the power supply noise.

To address long testing time on account of the shmoo plotting, a regression technique needs to be developed in estimating the RMS value of jitter while minimizing the period points as well as the number of samples at each period point. Then, jitter analysis based on high-volume shmoo data from production testers would be possible without relying on BIST circuitry.

6.4 Summary

A new approach for validating random jitter in the SoC has been proposed, which exploits the shmoo plotting on production testers to estimate the RMS value of random jitter. The proposed approach was verified with circuit-level simulations, and was also validated using one of the latest SoC products. Although recent improvements on circuit techniques for PLL design have also led to reduced clock jitter, the current trends of low-power SoC products,
which require lower $V_{dd}$, denser integration, and deeper sub-micron technology below 45nm, can have an adverse effect on timing uncertainties. Thus, validating signal integrity in the SoC needs to include timing uncertainties.
Chapter 7

Conclusion

7.1 Conclusion

Many BIST techniques for measuring random jitter have been proposed, since the BIST-based approach has significant advantages over the approach using external bench testers. Self testing and parallel testing are becoming more crucial in the current trend of requirements for low-cost testing on the SoC products targeting a mobile market. As such, the BIST solution for random jitter measurement needs to be simple in its implementation while providing reliable measurement at the same time.

This dissertation aims at developing a solution for random jitter measurement that can be practically applicable to ever evolving and proliferating SoC products. To achieve this goal, we proposed a random jitter measurement technique that estimates the RMS value of random jitter by measuring its average quantity that represents the amount of random jitter, rather than measuring it at every clock cycle. This technique can also measure random jitter in the clock signal of a wide range of frequency, unlike other previous BIST-based methods. To avoid the requirement of a reference clock in the jitter measurement, an accurate delay measurement method using a shrink-
ing clock signal was also proposed, which exploits an ATE in generating the shrinking clock signal by just using two CMOS gates. Regarding measurement accuracy, a differential approach was used to accurately measure a small amount of random jitter as well as a small delay value. As a result, the BIST circuit design can be simple without compromising its measurement accuracy. Thus, the external tester and the BIST approach can be symbiotic.

The random jitter measurement method developed here was validated using a test chip, which was fabricated to support the proposed method, to prove the linearity of random jitter measurement that is comparable to simulation results. The effect of substrate coupling noise on the SUT was also demonstrated with measurement results, which becomes more significant along with power supply noise as more circuit blocks are integrated together in SoCs. To measure random jitter in clock signals when a SoC is in its functional mode, an indirect measurement technique for random jitter was proposed, which exploits the existing shmoo capability of the ATE, thus expanding the capability of the ATE from digital logic validation to analog parametric testing. As future work, the indirect random jitter measurement method needs to be used in conjunction with the BIST-based random jitter measurement method so that random jitter at the various places along a clock distribution network could be better understood inside the SoC, thus paving the way for the compensation of the random jitter.
Appendix
Appendix 1

Test Chip for Random Jitter Measurement

1.1 Bonding Diagram of the Test Chip

Figure 1.1: The bonding diagram of the Bevo3 test chip (package figure: the courtesy of Spectrum Semiconductor Materials Inc.)
### Table 1.1: Pin mapping in the bonding diagram

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Name of Pin</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td>VSS</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>OR ENABLE</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>VSS</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>VIN1</td>
<td>Reference clock</td>
</tr>
<tr>
<td>40</td>
<td>VIN2</td>
<td>Jittery clock</td>
</tr>
<tr>
<td>41</td>
<td>SEL</td>
<td>For digital output</td>
</tr>
<tr>
<td>42</td>
<td>ENABLE</td>
<td>For digital output</td>
</tr>
<tr>
<td>43</td>
<td>VDD</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>/CLEAR</td>
<td>For digital output</td>
</tr>
<tr>
<td>45</td>
<td>SEL1</td>
<td>For digital output</td>
</tr>
<tr>
<td>46</td>
<td>SEL2</td>
<td>For digital output</td>
</tr>
<tr>
<td>47</td>
<td>CLKDIV16 BUF</td>
<td>VCO output</td>
</tr>
<tr>
<td>48</td>
<td>VSS</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>CLKEXT</td>
<td>Disable VCO output</td>
</tr>
<tr>
<td>50</td>
<td>VSS</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>Q12to14</td>
<td>For digital output</td>
</tr>
<tr>
<td>52</td>
<td>Q08to11</td>
<td>For digital output</td>
</tr>
<tr>
<td>53</td>
<td>Q04to07</td>
<td>For digital output</td>
</tr>
<tr>
<td>54</td>
<td>Q00to03</td>
<td>For digital output</td>
</tr>
<tr>
<td>55</td>
<td>VDD</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>ENABLE2</td>
<td>For substrate noise injector</td>
</tr>
<tr>
<td>57</td>
<td>VSS</td>
<td>For substrate noise injector</td>
</tr>
<tr>
<td>58</td>
<td>VC IN</td>
<td>VCO control in substrate noise injector</td>
</tr>
<tr>
<td>59</td>
<td>VDD</td>
<td>For substrate noise injector</td>
</tr>
<tr>
<td>60</td>
<td>CLKDIV16 BUF2</td>
<td>VCO output in substrate noise injector</td>
</tr>
</tbody>
</table>
Bibliography


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Vita

Jae Wook Lee was born in Uiseong, South Korea on 10 January 1972, the son of Yoo Keun Lee and Bok Sook Kim. He received the Bachelor of Science degree and the Master of Science degree in Electrical Engineering both from Pohang Institute of Science and Technology (POSTECH) in 1995 and 1997, respectively. He joined Korea Electric Power Research Institute (KEPRI) in Taejeon, South Korea in 1997 and worked as a Member of Technical Staff until he applied to the University of Texas at Austin for enrollment in their engineering program. He joined the University of Texas at Austin in August, 2005, where he received the Master of Science degree in Electrical and Computer Engineering in 2009. During the program at the University of Texas at Austin to pursue his Ph.D. degree, he joined Intel in 2010. His research interests include jitter measurement, PLL design and testing, and low-power SoC validation.

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