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ANALYSIS AND CONTROL OF POWER CONVERTERS WITH INSTANTANEOUS CONSTANT-POWER LOADS

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ANALYSIS AND CONTROL OF POWER CONVERTERS WITH INSTANTANEOUS CONSTANT-POWER LOADS

by

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Dedication

To my parents:

Nwachukwu and Nnenna Onwuchekwa

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ANALYSIS AND CONTROL OF POWER CONVERTERS WITH INSTANTANEOUS CONSTANT-POWER LOADS

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Supervisor: Alexis Kwasinski

This dissertation examines the effects of instantaneous constant-power loads (CPLs) on power converters. These CPLs are prevalent in distributed power architectures and are also present in certain motor-drive applications. CPLs introduce a destabilizing nonlinear effect on power converters through an inverse voltage term that leads to significant oscillations in the main bus voltage or to its collapse.

Boundary control is studied in order to stabilize dc-dc converters with instantaneous CPLs. The three basic topologies are studied: buck, boost, and buck-boost. Converter dynamics are analyzed in both switching states and the various operating regions of switch interaction with a first-order switching surface are identified. The analysis reveals important characteristics of CPLs. For non-minimum phase converters, in order to avoid issues related with the fact that the closed-loop state-dependent switching function is undefined on the switching surface, reflective mode solutions to both converter systems are defined in the sense of Filippov. Sufficient conditions for large-signal stability of the closed loop converter operating points are established. It is shown that first-order switching surfaces with negative slopes achieve large-signal stability, while positive slopes lead to instability. In particular, for the boost converter it is illustrated via simulations and experiments that positive slopes may lead to another

closed-loop limit cycle. It is also shown that instability as well as system-stalling, which is termed the invariant-set problem, may still occur in reflective mode. However, a hysteresis band that contains the designed boundary may be used to prevent system-stalling, and also allow for a practical implementation of the controller by avoiding chattering. Regulation is also achieved.

The dynamic behavior of single-phase full-wave uncontrolled rectifiers with instantaneous CPLs is also explored. Stable operation is shown to be dependent on initial condition and circuit parameters, which must fall within reasonable ranges that validate a CPL model. A necessary condition for stable operation of the rectifier system is thus derived. Furthermore, input and output characteristics of the rectifier with a CPL are investigated, and comparisons are made with the resistive case. A more complete model for the rectifier system that incorporates line-voltage distortion is also utilized to study the rectifier system. Simulations and experimental results are included for verification.

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Chapter 1: Introduction

MOTIVATION

Multi-stage cascade distributed power architectures that include tightly regulated dc-dc converters are becoming prevalent today in many practical applications [1]-[3]. These tightly-regulated converters present an instantaneous constant-power (CP) characteristic at their input terminals; hence, they act as constant-power loads (CPLs) to other converters upstream in the power distribution system. The increased use of electronic loads and the expected expanded deployment of micro-grids make the study of CPLs not only important, but also practical. Nowadays, CPLs can be found in many applications with significant potential for micro-grid integration. One of such applications is in information and communications technology (ICT) facilities. These facilities—e.g., all few hundreds of thousands of telecom switches, wireless communications base stations, and data center servers—are CPLs and they account for 3% of US power consumption [4] and about 4.5% of the US yearly load increment. For this reason, CPLs are receiving more attention from the research community [5] – [9].

This interest on CPLs is also coupled with a number of initiatives and programs intended to develop a 380 Vdc-based power distribution architecture for ICT facilities, one of which is delineated in reference [10]. However, as smart grids are developed, potential grid-powered applications of distributed dc power architectures expand beyond the current ICT applications. Advanced smart grids intended for higher penetration of residential advanced lighting based on LEDs, renewable energy sources, such as photovoltaic systems, and energy storage are also driving development of residential dc distributed power architectures in which many of the loads—e.g. consumer electronics such as plasma TVs or computers, and electronic driven air conditioners or appliances—would behave as CPLs fed by a dc distributed power architecture [11]. These

technologies are motivating a search for a better understanding of the behavior of power converters with CPLs. Distributed power architectures are not limited to grid-powered applications. Distributed power architectures are also common in both grid connected and stand-alone micro and nano grids—particularly dc—because of their flexibility and compatibility with modular designs [12]. Additional advantages of dc micro-grids over ac distributed generation systems include potentially higher availability, efficiency, and power density. For this reason, micro-grids have attracted the attention for their use in ICT facilities [13] [14]. Other applications of micro-grid based distributed power architectures include proposed electric power architectures for a U.S. Navy full electric ship [15]. Fig. 1 shows two stages of a distributed power architecture, in which a line-regulating source-interface (LRSI) buck converter on the left feeds a CPL on the right.

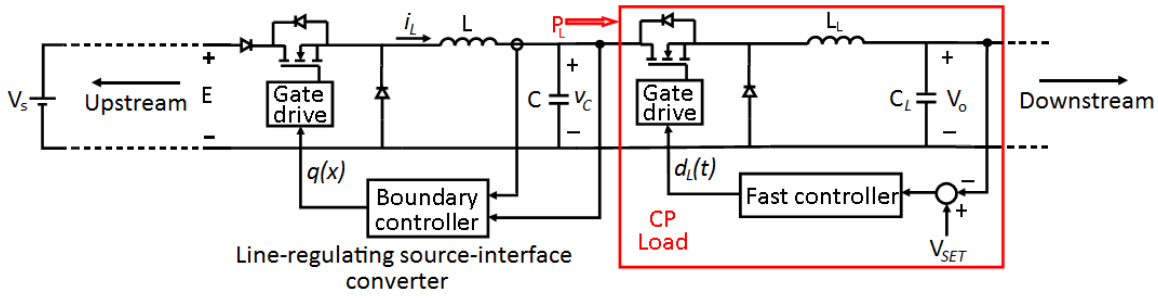


Figure 1: Circuit schematic showing a line-regulating source-interface converter on the left feeding a CPL on the right.

STABILIZING STRATEGY FOR DC-DC CONVERTERS

A geometric-based controller is presented for dc-dc converters that are subject to instantaneous constant-power loads (CPLs). Although dc-dc converter behavior is typically studied with resistive loads, many times loads do not have this resistive characteristic. These tightly-regulated converters present an instantaneous constant-power (CP) characteristic at their input terminals; therefore, they act as CPLs to other converters

upstream in the power distribution system, particularly to those interfacing the main system bus with the power sources or as the last stage in a more complex interface, such as a telecom rectifier.

The focus of this work is to study a boundary controller for a line-regulating source-interface converter, such as the one on the left in Fig. 1. In this figure, the tightly-regulated converter on the right could be either an intermediate bus-voltage regulating converter or a point-of-load (POL) converter [16] [17], whose output voltage is regulated to V_{SET} by a fast controller, so that the power at its output and input terminals stays practically constant regardless of its input voltage V_C. Hence, from a practical perspective many computers or modern consumer electronic devices are CPLs. Moreover, since most dc micro-grids, and information and communications technology (ICT) power plants have distributed power architectures, their loads are also CPLs [5]. Proposed dc power distribution systems for homes and office buildings also have cascade distributed architectures and hence, their loads could be CPLs. [6]. Another example of a CPL is a motor drive that maintains constant speed, with the motor having a one-to-one torque-speed characteristic [7]. Many previously published efforts in converter control subject to CPLs rely on restrictive linearization techniques [2] [3] [8], [9], [18]-[20]. The linearization step assumes small variations in a neighborhood of an equilibrium point (EP), so that the approximation is only valid if system behavior is being studied in close proximity to such EP. Away from the EP, linearization techniques become untrustworthy. Furthermore, it is difficult to determine the neighborhood around the equilibrium point where the linear approximation is valid. Sanders and Verghese [21] introduce a Lyapunov-based method that derives a control law for switched power converters. The method avoids the limitations of linearization and large-signal stability is guaranteed, but

it is assumed that the converter is open-loop stable. This is not the case with a dc-dc converter that is subject to a CPL.

Attempts have been made to tackle the CP control problem with the introduction of nonlinear methods. For instance, in [22], the control strategy employs hysteresis control in a current feed-forward loop to keep the current within specified limits, while a voltage feedback loop regulates the converter's output voltage using proportional-integral (PI) control. A major drawback of the scheme, however, is that the PI controller increases the dimension of the closed-loop system. In another effort, the sliding-mode control scheme used in [7] ensures stability under CP operation, but the output voltage varies within a specified range, yielding an unpractical output regulation characteristic. This prevents the technique from being used in applications where set-point voltage is desired; moreover, the hybrid CP/resistive load that is used in the analysis reduces the pure CPL destabilizing effect and may not be realistic in some applications, such as in ICT facilities [5]. Soto *et al.* [23] and Yousefzadeh *et al.* [24] also employ a combination of linear and nonlinear control. Using a non-linear passivity-based technique, Kwasinski and Krein [25] systematically derive a proportional-derivative (PD) controller. This is the same control law found empirically in [5] and [26]. The control law is relatively simple to implement and it achieves set-point regulation, but its main disadvantage is its sensitivity to noise, which is largely due to the derivative component of the controller. The same scheme is used in [27] to control boost and buck-boost converters under similar conditions; once again, the controllers contain differential components. Another drawback is that the CPL current and voltage experience overshoots during transients that may be undesirable in some applications.

Boundary control is another nonlinear approach. Krein [28] and Munzert and Krein [29] address general issues in boundary control, while Greuel *et al*. [30]

concentrates on design methods. First-order switching surfaces were used in these studies. Leung and Chung [31], [32], [35], Ordonez *et al*. [33], Chiu *et al.* [34], and Pitel and Krein [36] delve into the use of higher-order boundaries and Leung and Chung [31], [32] point out one important benefit—better transient performance—and associated design tradeoffs such as more complicated implementation. Analysis with second order surfaces can also be complex as is evident in [37], where a state-energy plane was necessary to derive a second order switching surface for the boost converter. Schlid *et al*. [38] derive a methodology for designing generalized boundary controllers for dc-dc converters. However, all past studies with this approach assume resistive loads, whereas the analysis presented here considers an instantaneous CPL—a type of load that is increasingly prevalent in today's power conversion environments. In addition to simple implementation, boundary control is also robust. This direct large-signal method has been proven to be able to achieve stable operation even for extreme disturbances and can directly guarantee important operating specifications, such as voltage and current ripple [28]. Conditions for large signal stability are also comparatively easy to evaluate with boundary control [29]. Furthermore, transient performance and ripple specification can be adjusted with relative ease, and in special applications current and voltage overshoots may be eliminated. In this dissertation, a geometric-based nonlinear method is employed to drive the two-state system of the buck converter feeding a CPL to a desired operating point (OP). The general structure of the system under analysis is shown in Fig. 1, where a line-regulating source-interface converter feeds a CPL.

This study also proceeds to investigate non-minimum phase (boost and buck-boost) converters with CPLs. Due to the non-minimal-phase nature of these other two basic second-order dc-dc converters, the conclusions reached for the buck converter cannot be *a priori* directly extended to these non-minimum phase topologies without

some necessary analysis. In addition to the non-minimal phase nature, it has been shown that hysteresis control for non-minimum phase converters with resistive loads is different from that of the buck, because the structure of the buck converter allows either voltage or current references to be used, but boost and buck-boost converters can only accept a current reference [28]. Thus, it is relevant to evaluate how boundary control can be implemented in non-minimum phase converters when they operate with instantaneous CPLs. This is another motivation for this work, i.e., to study the previously unaddressed practical problem of analyzing boundary controllers for non-minimum phase dc-dc converters with CPLs.

Control issues for non-minimum phase converters are known to be more challenging than those present in the buck converter. Even when non-minimum phase converters are subject to resistive loads, linear techniques yield right-half-plane zeros in the converter transfer functions, which tend to cause instability [39]. Eliminating this instability has been the subject of several studies [37], [39] – [45]. In particular, Song and Chung [37] control a boost converter that feeds a resistive load by forming a state-energy plane and then, uses boundary control to derive a second order switching surface. The method provides fast transient response, but requires sophisticated analog circuitry. Constant-power loads make the control problem for non-minimum phase converters even more challenging. So far, passivity-based control (PBC)—a nonlinear approach—has been used to control boost and buck-boost converters subject to CPLs [27]. However, controllers derived using PBC are subject to the same limitations that are encountered in the buck case. Experimental results verify both the analysis and the superiority of this controller with respect to previous approaches.

Boundary Control Overview

In order to provide some context to the next step of the analysis, it is essential to furnish an overview of the basic definitions on which this study is based. A more comprehensive description of boundary control, out of the scope of this dissertation, can be found in [29], and [30]. Boundary control refers to converter-system control with the use of switching surfaces [28]. This nonlinear technique makes use of the state variables of the converter system to select a boundary, where switching occurs. In an *n*–state system where all the states are utilized for feedback, the switching surface is of dimension n - 1. The switching surface is defined based on its interaction with the converter's trajectories. Switching occurs when the trajectories cross the boundary, so it is important to observe trajectory behavior around switching surfaces [28]. Fig. 2 shows the three possible behaviors and the points of transition between these possible behaviors. Let's define trajectories that approach a switching surface as *incident trajectories*, $\Phi_i(x)$ and trajectories that are directed away from a switching surface as *exiting trajectories* $\Phi_e(x)$. The time derivative of $\Phi_i(x)$ defines a "velocity" vector f_i (t) whereas the time derivative of Φ_e (x) defines a "velocity" vector f_e (t).

Refractive Behavior

On one side of the boundary the trajectories are incident, while on the other side of the boundary, the trajectories are exiting. At the switching surface, both the incident and exiting state-velocity vectors f_i and f_e, respectively, must have components in the direction of the defined normal to the switching surface, $\hat{n}$, at the point of incidence, or they both must have components in the direction opposing the defined normal, $\hat{n}$. This is represented graphically in Fig. 3. At the boundary, mathematically we have

$$\begin{cases} f_i \cdot \hat{n} > 0 \\ f_e \cdot \hat{n} > 0 \end{cases} \tag{1}$$

when both the incident and exiting trajectories have components in the direction of the defined normal, $\hat{n}$, and

$$\begin{cases} f_i \cdot \hat{n} < 0 \\ f_e \cdot \hat{n} < 0 \end{cases} \tag{2}$$

when both the incident and exiting trajectories have components in the direction opposing the defined normal, $\hat{n}$.

Reflective Behavior

Trajectories on both sides of the switching surface are incident. Hence, the mathematical description of this behavior is

$$f_i \cdot \hat{n} > 0 \tag{3}$$

when f_i (t) is directed towards the boundary and it also has a component in the direction of the defined normal, $\hat{n}$, at the point of incidence, and

$$f_i \cdot \hat{n} < 0 \tag{4}$$

when f_i (t) is still directed towards the boundary but it has a component in the direction opposing the defined normal, $\hat{n}$, at the point of incidence. Once Φ_i (x) intersects the boundary, the converter dynamics is then restricted to the boundary, thereby defining a sliding mode [46]-[48]. When reflective behavior occurs, the boundary determines system operation, so the dimension of the system can be reduced by one order. In this mode a hysteresis band may be necessary to prevent the switch from chattering [28]-[29] [49]. The hysteresis band creates, then, a hybrid system because switching is no longer dependent only on the trajectory crossing the hysteresis band's boundaries but it also depends on the system state prior to crossing the boundary [49]. For switched power converters, a notable distinction between state-dependent switching—which is employed here—and time-dependent switching is that with the former, the switching function in closed-loop operation is given by $q = q(x)$. Thus, with state-dependent switching, the

conventional concept of a duty ratio as the input signal of a PWM controller does not apply when controller action starts. As part of the analysis it is important to identify reflective behavior regions because a necessary but not sufficient condition in order to guarantee stability is that the boundary must be reflective in some region around the desired operating point [30].

Rejective Behavior

On either side, the trajectories are exiting. Hence, mathematically,

$$f_e \cdot \hat{n} < 0 \tag{5}$$

when $\Phi_e(x)$ is exiting the surface and has a component in the direction opposing the defined normal, $\hat{n}$, at the point where the trajectory leaves the boundary, and

$$f_e \cdot \hat{n} > 0 \tag{6}$$

when $\Phi_e(x)$ is exiting the surface and has a component in the same direction as the defined normal, $\hat{n}$, at the point where the trajectory leaves the boundary.

The behaviors of these trajectories at the boundary define the respective operating modes for the closed-loop-converter. For example, refractive behavior at the boundary implies a closed-loop converter system operates in refractive mode [29].

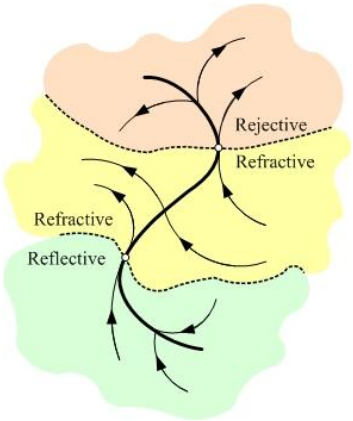


Figure 2: Possible trajectory behaviors at a switching surface.

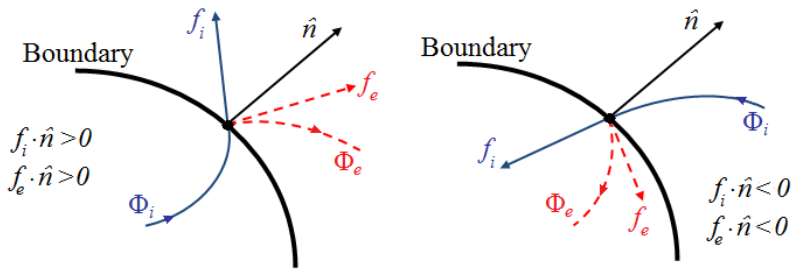


Figure 3: The two possible cases in the refractive mode.

DC MICRO-GRIDS WITH AC SOURCES

This dissertation also investigates the dynamic behavior if the system comprising a single-phase ac source, an uncontrolled full-wave rectifier stage, and a CPL. Downstream stages adding controls, such as dc-dc converters for output regulation are not commented on, because many of these conversion stages may be included in previous published works [5], [7] - [9], [25], [27], [50] – [54]. Various such efforts have examined CPL destabilizing effects in dc-cascade power architectures by assuming constant dc voltage sources, and thus, neglecting ac sources. However, ac sources such as micro and conventional turbines or traditional diesel generators may be deployed in dc micro-grids or in combination with dc sources in order to improve system availability by increasing power supply diversity (see Figure 4). Consequently, these ac sources have to be interfaced with the distributed power architecture through ac-dc converters (i.e., rectifiers). The micro-grid could also be based on an ac power distribution, but still include CPLs—e.g. a highly energy efficient building with computers and electronic driven air conditioners as its main loads— with rectifiers located at the first conversion stage of microturbines. Rectifiers can also often be situated at the first conversion stage in small wind turbines in order to condition the variable nature of wind generators output voltage. Although these generators will typically produce 3-phase power, three single-phase rectifiers could still be used as their interfaces in order to simplify their operation,

for example, in order to implement power factor correction techniques. Still, fewer studies mention the destabilizing effects that CPLs have on rectifier systems [55] – [59]. Liutanakun *et al.* [55], Harnefors and Pietl¨ainenardier [56], Moskull [57], Roux and Richardeau [58], and Wang *et al.* [59] all rightly observe that reducing dc link capacitance and/or increasing rectifier inductance may lead to instability. However, to simplify the analysis, these references ([55] – [59]) model an ac voltage source and rectifier as an equivalent dc source. Essentially, these efforts do not investigate effects of the CPL on the rectifier. Particularly, the assumption of a dc source prevents input and output characteristics of the rectifier from being explored.

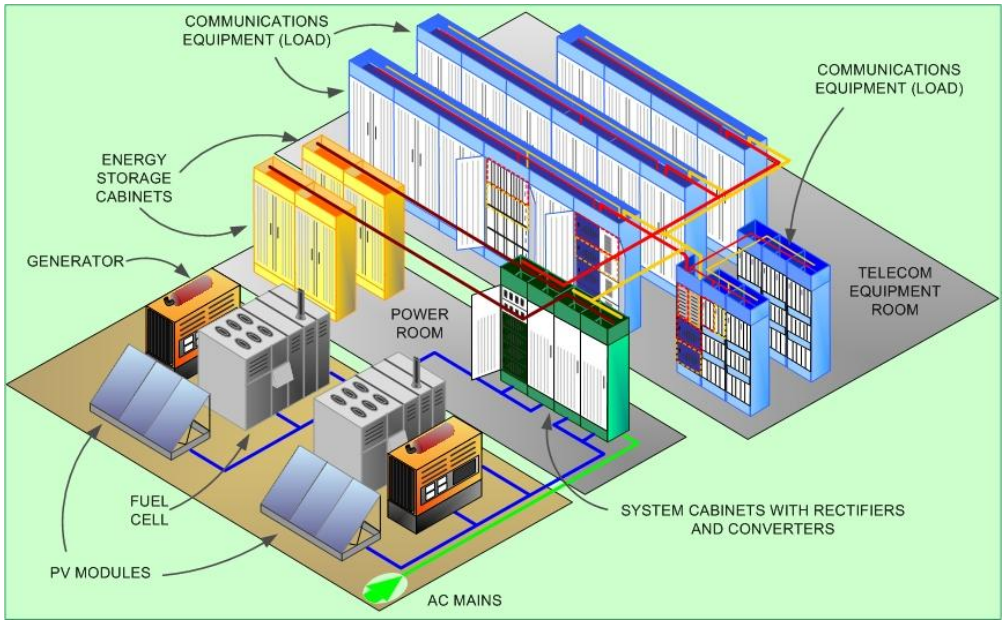


Figure 4: A practical microgrid architecture that includes ac power sources.

Chapter 2: Buck Converter with Constant-Power Loads

In practical CPLs, the instantaneous power is fixed only above a minimum voltage, V_{lim}. Below this voltage, a practical CPL shuts down operation in order to prevent damage due to an excessive current [16] [17]. Thus, the current through a general practical instantaneous CPL is given by

$$i(t) = \begin{cases} 0 & if \;\; v(t) < V_{\lim} \\ \dfrac{P_L}{v(t)} & if \;\; v(t) > V_{\lim} \end{cases}, \tag{7a}$$

where P_L is the power consumed by the CPL, and *i(t)* and *v(t)* are the CPL's instantaneous current and voltage, respectively. However, this representation lacks generality for the analysis because the choice for the value of V_{lim} may hide some important characteristics of the operation under a CPL. Thus, for the rest of this work, CPLs are represented as

$$i(t) = \frac{P_L}{v(t)} \;\; \forall \left\| v(t) \right\| > \varepsilon, \tag{7b}$$

where ε is some arbitrarily small positive value.

The dynamics of an ideal buck converter loaded with an ideal CPL and in continuous-conduction mode can be represented as

$$f(i_L, v_C) = \begin{bmatrix} \dfrac{di_L}{dt} \\ \dfrac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{L}\left(q(t)E - v_C\right) \\ \dfrac{1}{C}\left(i_L - \dfrac{P_L}{v_C}\right) \end{bmatrix} \tag{8}$$

$$i_L \geq 0, v_C > 0, \tag{9}$$

where *q(t)* is the (open-loop) switching function acting on the input switch in the line-regulating source-interface converter on the left in Fig. 1. For simplicity and in order to generalize the notation according to standard control system theory practices, in the following analysis the system state vector x has coordinates $x_1 = i_L$ and $x_2 = v_C$. If

$\Psi = R^2 - \{x_2 = 0\}$ and $\Omega = \Psi \cap \{x: x_1 \geq 0, x_2 > 0\}$ are defined, *f* is only *locally Lipschitz* on $\Psi - R^2$ i.e., it is not *globally Lipschitz*—hence the strict inequality on v_C in (9) [60]. In order to follow standard power electronics theory practices [1] [28], x_2 represents the horizontal state-space axis and x_1 is the vertical state-space axis.

Discussions henceforth take into account that in each switching state, (8) constitutes an autonomous nonlinear system. The analysis of a boundary controller considers each of the switch states as the basis for the analysis. The controller action follows a state-dependent switching strategy ($q = q(x)$) instead of a more conventional time-dependent switching method ($q = q(t)$). Hence, the study is inherently nonlinear as described next through each of the state dynamics for the line regulating source-interface buck converter.

ON-STATE DYNAMICS

When the switch is on, the dynamics of the line-regulating source-interface buck converter on the left in Fig. 1 is governed by

$$f_{ON}(x_1, x_2) = \begin{bmatrix} \frac{dx_1}{dt} \\ \frac{dx_2}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{L}(E - x_2) \\ \frac{1}{C}\left(x_1 - \frac{P_L}{x_2}\right) \end{bmatrix} \tag{10}$$

$$x_1 \geq 0, x_2 > 0 \tag{11}$$

As explained in [25] discontinuous conduction modeling requires including an additional term affecting x_1 dynamics with respect to the continuous conduction model. However, this additional term can be ignored in the analysis because the additional dynamics that it introduces are generally significantly less influencing than those owed to terms included in both the description of discontinuous and continuous mode operation.

For now, let's also neglect the effect that (6) has on the dynamics. Then $f_{ON}(x)$ yields one equilibrium point at

$$x_{EON} = \begin{bmatrix} \frac{P_L}{E} & E \end{bmatrix}^T \tag{12}$$

We can now investigate the stability properties of this EP with the help of Fig. 2 obtained by simulating a system such as the one in Fig. 1, with the line-regulating source-interface buck converter having the following parameters: E = 20 V, P_L = 100 W, L = 470 μH, C = 500 μF.

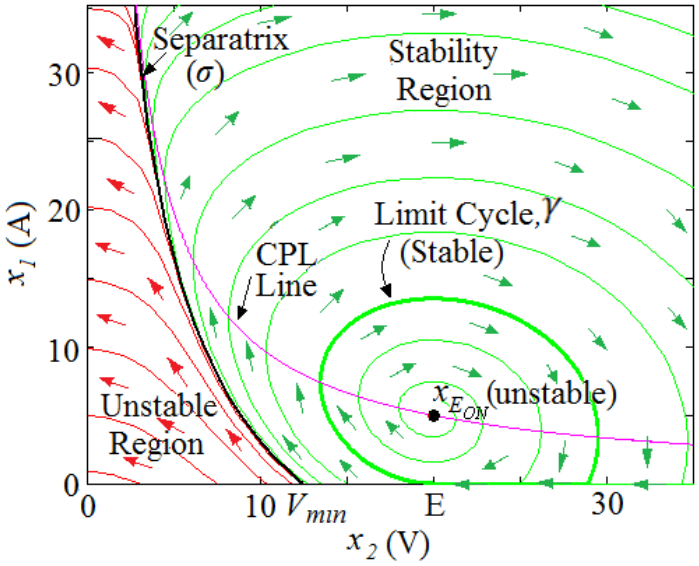


Figure 5: Phase portrait of converter dynamics with $q(t)$ = 1.

Consider the following *positive-definite* and *decrescent* energy-like function [61] as a candidate Lyapunov function

$$V(x) = \frac{1}{2}(x - x_{EON})^T Q(x - x_{EON}) > 0, \tag{13}$$

where $Q = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} > 0$. Differentiating $V(x)$ along the trajectories of (10) gives

$$\dot{V}(x) = \frac{P_L}{E x_2}(x_2 - E)^2 \geq 0. \tag{14}$$

LaSalle's invariance principle [62] was used in [63] to extend Chetaev's Instability Theorem [61], so that instability can be concluded even when $\dot{V}(x)$ is positive semi-definite. Instability can also be easily established by analyzing stability using LaSalle's principle in reverse time [64]. Consequently, x_{EON} is an unstable EP.

Once it has been determined that x_{EON} is not stable, it is possible to analyze the behavior of the line-regulating source-interface buck converter in the ON-state through its trajectories. If the constraint on x_1 is eliminated and x_1 is allowed to take negative values, all trajectories $\Phi_t(t) \in \Psi \cap \{x_2 > 0\}$ spiral out of x_{EON}. However, as Fig. 5 shows, when (10) is considered there are two regions characterized by different behaviors and separated by a separatrix, σ. To the right of the separatrix, the trajectories converge into a limit cycle around x_{EON}, whereas to the left of σ, the trajectories evolve into a point of a very high inductor current and a very low capacitor voltage. The separatrix is the trajectory that has the characteristic $lim_{t\to\infty} \Phi_t(t) = [\infty \quad 0]^T$ and that tends to be tangential to the CPL line at this singular point. An approximation of the separatrix is derived in [18]. With the restriction of equation (4) in place, the dynamics of the converter is confined to Ω, therefore trajectories that hit the $x_1 = 0$ line slide to the left until they reach the point $x_2 = E$. At this point they remain on one common trajectory: the limit cycle, γ. A more detailed description of the way the trajectories evolve and how they converge into a limit-cycle were presented in [25]. Essentially, the inequality $x_1 \geq 0$, induces a stable limit cycle, γ, in the dynamics. This limit cycle has a region of attraction, because only trajectories with initial conditions to the right of the separatrix are such that $lim_{t\to\infty} \Phi_t(t) = \gamma$.

OFF-STATE DYNAMICS

When the switch is off, the dynamics of the line-regulating source-interface buck converter on the left in Fig. 1 is governed by

$$f_{OFF}(x_1, x_2) = \begin{bmatrix} \frac{dx_1}{dt} \\ \frac{dx_2}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{L}(-x_2) \\ \frac{1}{C}\left(x_1 - \frac{P_L}{x_2}\right) \end{bmatrix} \tag{15}$$

$$x_1 \geq 0, x_2 > 0 \tag{16}$$

Equation (16) confines the dynamics of (15) to Ω. As shown in Fig. 3 and indicated in (15), when x_2 is almost zero, x_1 tends to be constant. Hence, trajectories approaching the $x_2 = 0$ line tend to end at a fixed coordinate on x_1. However, from (7) and (16), the behavior when x_2 equals zero is not determined because the line $x_2 = 0$ is out of the studied space. When the trajectories hit the $x_1 = 0$ line, they slide to the left, remaining on the line until x approaches the point $[0 \quad 0]^T$. The OFF-state trajectories evolve as depicted in Fig. 3.

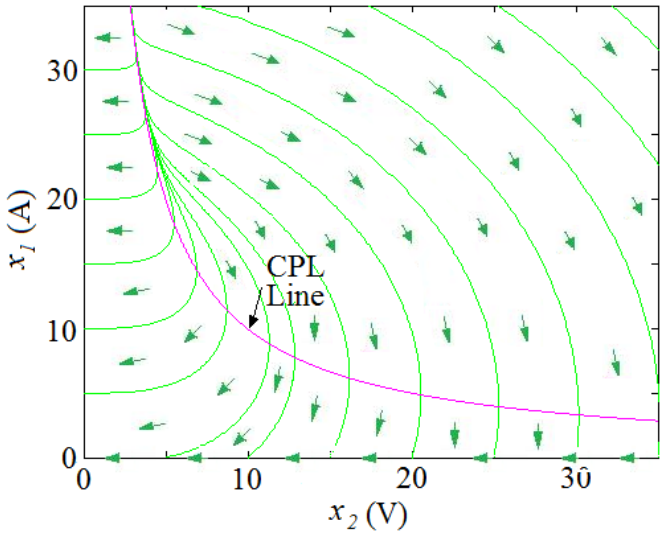


Figure 6: Phase portrait of converter dynamics with $q(t) = 0$.

CONTROLLER ANALYSIS

As mentioned earlier, references [31]-[37] study higher-order boundaries that may achieve faster transient responses, but they sacrifice implementation ease, which is a main advantage of boundary control. Thus, the controller design focuses on first-order (linear) boundaries. The method employed here to determine the various regions uses a pair of rays that originate at the desired OP, so that it is possible to track the direction of the trajectories in the entire planar state space with respect to the OP. In Fig. 7, the OP is the intended equilibrium point for the closed-loop system. The position of x_{EON}—the ON state equilibrium point defined in equation (12)—is consistent with buck-converter operation $v_C \leq E$. Figure 7 also illustrates the important conventions that are used in defining the various operating modes by depicting two ξ-rays originating at a particular OP. In particular, Fig. 7 indicates graphically the definition of the normal $\hat{n}$ of ξ, which implies that the half-lines are actually rays with the initial point coinciding with the OP. Let's now define a boundary λ as

$$\lambda : x_1 = k\left(x_2 - x_{2_{OP}}\right) + x_{1_{OP}}, \tag{17}$$

where $x_{OP} = [x_{1OP} \quad x_{2OP}]^T$ is the desired OP and k is the slope of the switching surface. In essence, the boundary λ defined in (17) is a special case of two ξ-rays as defined in Fig. 6, in which $\theta = 180^o$. Hence, for analysis purposes, on either side of the OP, the defined normal of λ is in opposing directions. Although part of the discussion considers k to be either positive or negative, due to large signal stability issues explained in part C of this section, the analysis will focus more on the cases with $k < 0$. Switching must be selected so that the trajectories on one side of the boundary are directed towards the other side of the boundary. For instance, an inspection of the trajectory directions in Figs. 5 and 6 indicates that in order to have the trajectories on one side of the boundary directed towards the other side, the converter should operate in the ON-state below the

switching surface and in the OFF-state above the surface. This condition is exemplified in Fig. 7 with an ON-state trajectory $\Phi_{ON}(x)$ incident to the left portion of ξ and an OFF-state trajectory $\Phi_{OFF}(x)$ exiting the switching surface at the same point. To the left of x_{EON}, this configuration directs the trajectories on one side of the boundary into the other side of the boundary. To the right of x_{EON}, however, both the ON and OFF trajectories have components in the direction of the positive normal as defined in Fig. 7.

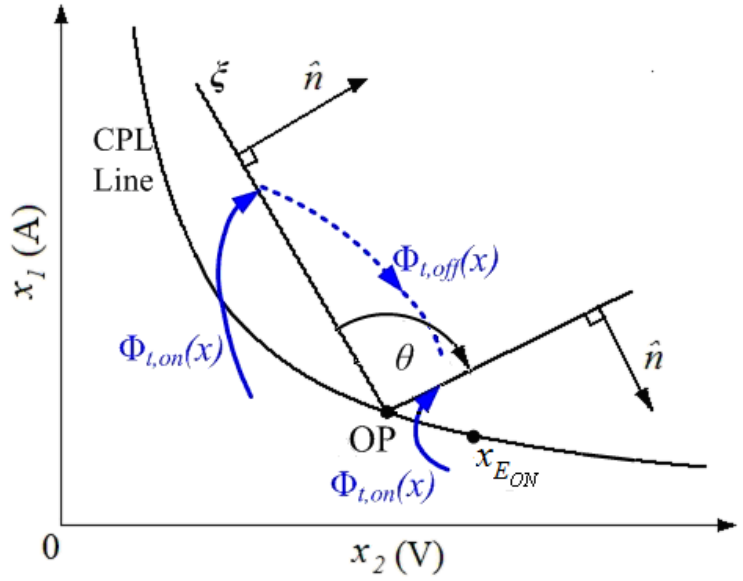


Figure 7: Sample boundary showing the defined normal unit vectors.

In order to explain in an analytical way the switching strategy mentioned in the previous paragraph, consider the definition of $\hat{n}$ as indicated in Fig. 7 into account. Then, boundary interaction with the trajectories defines the following operating modes at a first-order switching surface:

Refractive Mode

Naturally, refractive mode could occur in either direction on the boundary ξ. That is, before and after intersection with the switching surface, the incident and exiting

trajectories could both be in the direction of the normal or they could both oppose the direction of the normal. If ON-state trajectories define operation before boundary intersection—i.e., the ON-state is the incident-state—and OFF-state trajectories define operation after boundary intersection, then for refractive behavior at the switching surface, both the ON and OFF-state trajectories may have components in the direction of the defined normal

$$\begin{cases} f_{ON} \cdot \hat{n} > 0 \\ f_{OFF} \cdot \hat{n} > 0 \end{cases}, \tag{18}$$

or they may have components in the direction opposing the defined normal

$$\begin{cases} f_{ON} \cdot \hat{n} < 0 \\ f_{OFF} \cdot \hat{n} < 0 \end{cases}. \tag{19}$$

Reflective Mode

Due to the different unit-normal orientations on either side of x_{OP} indicated above, describing the reflective region becomes more subtle. Inspection of Figs. 5 and 6 in combination with Fig. 7, indicates that for the left half-line of ξ, if the converter operates in the ON-state below the switching surface, then f_{ON} may only be directed towards the boundary and have components in the same direction as the defined normal. Hence,

$$\begin{cases} f_{ON} \cdot \hat{n} > 0 \\ f_{OFF} \cdot \hat{n} < 0 \end{cases} \quad \text{if } x_2 < x_{2OP}. \tag{20}$$

Likewise, for the right half-line of ξ, if the ON-state still occurs below the switching surface, then f_{ON} may only be directed towards the boundary, but now has a component in the direction opposing the defined normal. This situation is exemplified in Fig. 7 with the ON-trajectory $\Phi_{ON}(x)$ incident to the right half-line of ξ. Thus,

$$\begin{cases} f_{ON} \cdot \hat{n} < 0 \\ f_{OFF} \cdot \hat{n} > 0 \end{cases} \quad \text{if } x_2 > x_{2OP}. \tag{21}$$

Rejective Mode

Rejective-mode operation is defined here by negating each of the components of the vectors in reflective mode.

$$\begin{cases} f_{ON} \cdot \hat{n} < 0 \\ f_{OFF} \cdot \hat{n} > 0 \end{cases} \text{ if } x_2 < x_{2OP} \tag{22}$$

$$\begin{cases} f_{ON} \cdot \hat{n} > 0 \\ f_{OFF} \cdot \hat{n} < 0 \end{cases} \text{ if } x_2 > x_{2OP}. \tag{23}$$

Based on the characteristics presented by the modes, it is possible to determine the various regions of phase space in which the defined modes can occur. Reference [29] indicates that transitions from refractive mode to reflective mode do not occur in a two-state system. This observation is true for converters loaded with resistive loads; however, for converters feeding CPLs, the behavior is more complex and transitions of this type do occur as will be demonstrated. As Fig. 4 indicates, at the boundaries between the operating modes, either the incident or exiting trajectories are tangential to the boundary. That is, at each point of transition between operation modes the velocity vector f_{ON} or f_{OFF} should be tangential to the switching surface and the following relationship holds:

$$\frac{f_{x_1}}{f_{x_2}} = \frac{dx_1}{dx_2} = k = \frac{x_1 - x_{1OP}}{x_2 - x_{2OP}}, \tag{24}$$

where f_{x_2} is the horizontal component (in x_2) of either f_{ON} or f_{OFF}, and f_{x_1} is the vertical component (in x_1) of either f_{ON} or f_{OFF}. Next, we substitute the right-hand-side expressions from (10) and (15) in (24). For the ON-state trajectories we have

$$\frac{C(E - x_2)}{L(x_1 - P_L / x_2)} = \frac{x_1 - x_{1OP}}{x_2 - x_{2OP}}. \tag{25}$$

This gives the locus of transition points for the ON-state trajectories as

$$\varphi_{ON}(x): L[x_1^2 x_2 - x_{1OP} x_1 x_2 - P_L x_1 + P_L x_{1OP}] + C[E x_{2OP} x_2 - (E + x_{2OP}) x_2^2 + x_2^3] = 0. \tag{26}$$

Similarly, for the OFF-state trajectories, we have

$$\frac{C(-x_2)}{L(x_1 - P_L / x_2)} = \frac{x_1 - x_{1OP}}{x_2 - x_{2OP}}, \tag{27}$$

and the locus of transition points for the OFF-state trajectories is given by

$$\varphi_{OFF}(x): L[x_1^2 x_2 - x_{1OP} x_1 x_2 - P_L x_1 + P_L x_{1OP}] - C[x_{2OP} x_2^2 - x_2^3] = 0. \quad (28)$$

Using (18) – (23), (26) and (28), we obtain a graphical representation of the transition-points loci and trajectory behaviors for linear boundaries passing through a desired OP. This is shown in Fig. 8. The switching strategy still considers that the ON-states occur below the switching surface while OFF states occur above. As observed earlier, to the right of x_E, the ON and OFF trajectories have components in the direction of the positive normal; hence it is not surprising that the only mode of operation in this region is refractive. As shown, rejective-mode operation does not occur with this configuration. The same parameters E = 20 V, P_L = 100 W, L = 470 μH, C = 500 μF are used in the illustrations given in Fig. 8 and Fig. 9. Here, the desired OP is x_{OP} = [6.67 15]^T. In order for the boundary to determine system behavior and to establish stability with relative ease it is usually desirable to have reflective-mode operation around the OP. Essentially, in reflective-mode the two-state system can be reduced to a one-dimensional system. Let's investigate the stability of the closed-loop system in reflective mode. For clarity, it is worth to mention that the various regions in the state space, such as those in Fig. 8, are the set of points of the state space where a trajectory of the system under study exhibits a same behavior when crossing a linear switching surface. For example, when a trajectory representing the dynamics of a buck converter with a CPL intersects any first-order switching surface at a point lying within the refractive behavior region, refractive behavior as indicated by equations (1) and (2) will be observed.

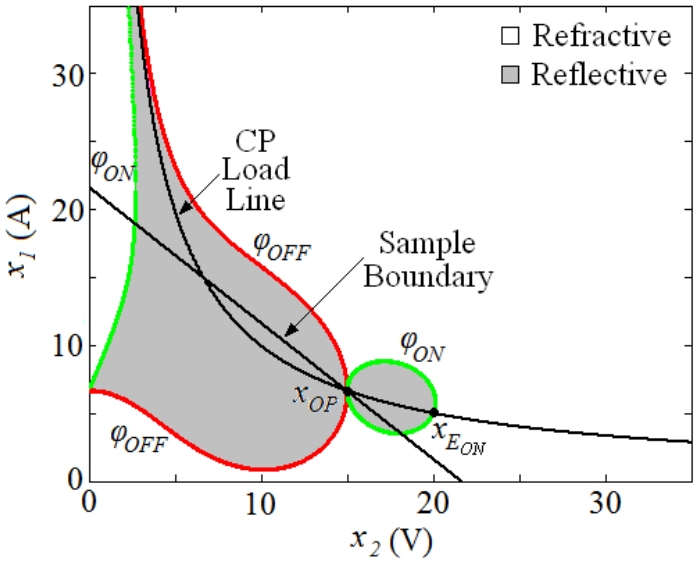


Figure 8: Locus of transition points for both states and operating regions of the closed-loop converter system.

Consider the following *positive-definite* and *decrescent* energy-like function [61] as a candidate Lyapunov function

$$V(x) = \frac{C}{2}\left\|x - x_{OP}\right\|^2 > 0. \tag{29}$$

Using (17) in (29) and taking the derivative of $V(x)$ along the trajectories of the converter system defined in (4) it yields

$$\dot{V}(x) = (1+k^2)\left(x_2 - x_{2_{OP}}\right)\left(x_1 - \frac{P_L}{x_2}\right). \tag{30}$$

$\dot{V}(x) < 0$ if $x_2 < x_{2OP}$ and $x_1 x_2 > P_L$, or if $x_2 > x_{2OP}$ and $x_1 x_2 < P_L$. These conditions guarantee asymptotic stability of the closed-loop system's OP. On the other hand, $\dot{V}(x) > 0$ if $x_2 < x_{2OP}$ and $x_1 x_2 < P_L$, or if $x_2 > x_{2OP}$ and $x_1 x_2 > P_L$; and the OP is unstable. Hence, the above analysis shows that instability may still occur in sliding mode. A powerful design tool is presented in Fig. 9 and it shows that the CPL line splits the reflective region into stable and unstable sections on either side of the line $x_2 = x_{2OP}$.

Define the sets $\Theta = \{x: x_1 x_2 = P_L\}$ and $\Delta = \{x : \dot{V}(x) = 0\}$. Examination of (30) reveals that in reflective mode $x_{OP} \in \Delta$ and $\Theta \subset \Delta$. Let's use the definition of an *invariant set* found in [61]. A set $\Gamma \subset \mathbb{R}^n$ is said to be invariant if whenever $x_0 \in \Gamma$, we have $\Phi_t(x) \in \Gamma \ \forall\, t \geq t_0$. This makes the set $\Delta = \{x : \dot{V}(x) = 0\}$ invariant. Thus, in reflective mode, in addition to the operating point, the CPL line is also an invariant set. This result may initially seem benign, but its consequences could be severe; since no switching action occurs at the boundary, if the closed-loop system has an initial condition at $x_0 = x_S$ or if trajectories pass through x_S after closed-loop operation has commenced, where x_S is the point where the boundary intersects the CPL line, then $\Phi_t(x) = x_S \ \forall\, t \geq t_0$. In other words, the converter stalls or remains at this point. In this study, this type of stalling is termed "*the invariant-set problem*."

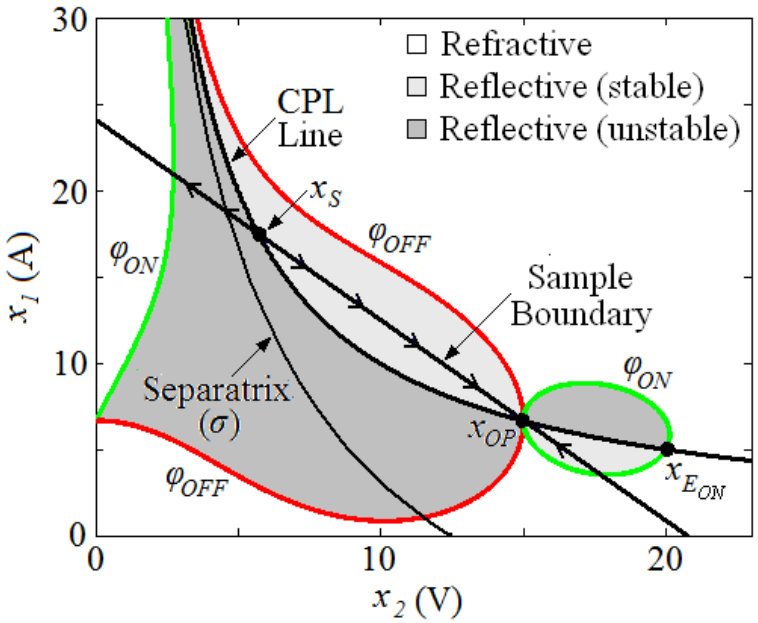


Figure 9: Interaction between sample boundary and operating regions of the closed-loop converter system.

LARGE-SIGNAL STABILITY

A converter is large-signal stable if there exists an arbitrarily small $\varepsilon \ni \lim_{t\to\infty} \|x - x_{OP}\| \le \varepsilon$ [30]. Operation in stable-reflective mode ensures this condition. As stated in the previous section, a necessary condition for stability is that the boundary must be reflective in some region around the OP. However, for the buck converter, switching surfaces with $k > 0$ do not furnish any stable reflective region around the OP [30]. Fig. 10 illustrates an example of converter operation using boundaries with positive slopes. System evolution starts at the initial point x_0. Initially, unstable-reflective mode is encountered when the trajectory hits the switching surface at x_a. Clearly, the boundary is in the unstable-reflective region at this point and sliding-mode operation moves the trajectory continuously away from the OP. At x_b, the trajectory enters the refracted mode so the trajectory moves away from the switching surface following a clockwise curve towards x_c. The boundary is hit next at x_c, which is still in the unstable-reflective region. Hence, once again, the trajectory is driven away on the switching surface until it crosses into the refractive mode region. When this situation happens, the trajectory moves towards the left and the system never recovers. This observation is in accordance with the aforementioned requirement that is stated in [29]. It suffices to say that in this application, boundaries with $k > 0$ are undesirable and it is assumed henceforth that they are not employed. Similar to the result stated in [25], another necessary condition for large-signal stability for the boundary-controlled buck converter feeding a CPL is that the initial condition of the closed-loop converter system should be inside the stability region of γ (to the right of the separatrix, σ). It is also assumed that this necessary condition is satisfied. However, these stipulations do not guarantee stability of the closed-loop converter system. For instance, if a switching surface that passes through the unstable-reflective region is used, the closed-loop system exhibits unstable-reflective behavior in

$\{x: x_2 < x_{2OP}\}$, sliding-mode operation occurs, but the trajectory is driven away from the operating point. Eventually, system operation transitions into the refractive mode. This transition takes places inside the unstable region of γ and the system never recovers. In this application, if the initial condition of the closed-loop converter system is in the stability region of γ and part of the switching surface passes through the stable-reflective region, refractive-mode operation may guarantee stability.

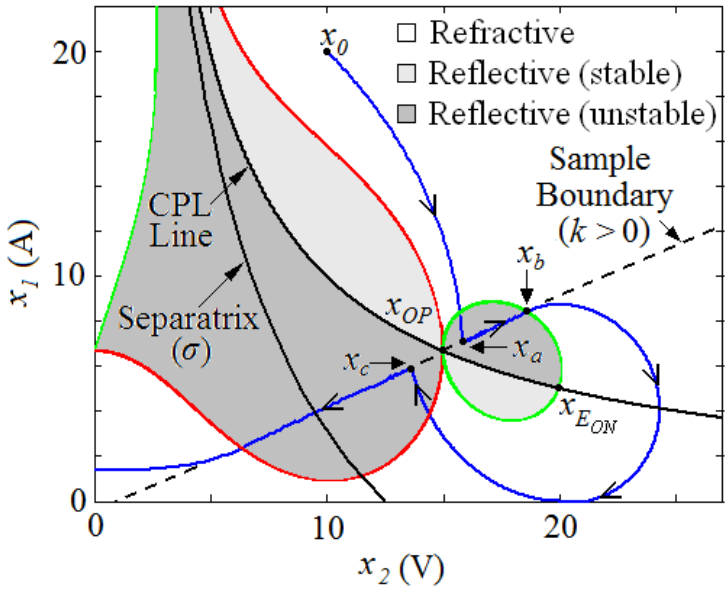


Figure 10: Simulation showing attempted recovery of the closed-loop converter system from instability.

In refractive-mode, the trajectories may be deflected to a point on the boundary that lies in the refractive or reflective regions, or to the $x_1 = 0$ line. Let's consider the case where the trajectory is deflected to another point on the switching surface that is still in the refractive region. Fig. 11 depicts this behavior. Clearly, x_a is in the refractive region, and upon intersecting the switching surface at x_a the trajectory is deflected towards x_b. Since x_b is still inside the refractive region, the trajectory is further deflected to x_c which

now lies in the stable-reflective region and the trajectory is driven successfully to the desired OP. When a trajectory is deflected directly to the $x_1 = 0$ line, however, the behavior is more intricate. If a switching surface crosses the $x_1 = 0$ line at a point $x_2 = -\alpha/k \geq E$, where α is the x_1–intercept of the boundary, a transition to the ON dynamics occurs when the boundary is crossed, but the natural evolution of the converter's dynamics restrict the trajectory to the $x_1 = 0$ line until $x_2 = E$, where the trajectory leaves the $x_1 = 0$ line. On the other hand, if a switching surface crosses the $x_1 = 0$ line at a point $x_2 < E$, the OFF-converter dynamics restricts the trajectory to the $x_1 = 0$ line until the point $x_2 = -\alpha/k$. This is illustrated in Fig. 12. Both trajectories *1* and *2* eventually pass through the stable-reflective region; hence, it is desirable that the switching surface lies sufficiently within this region.

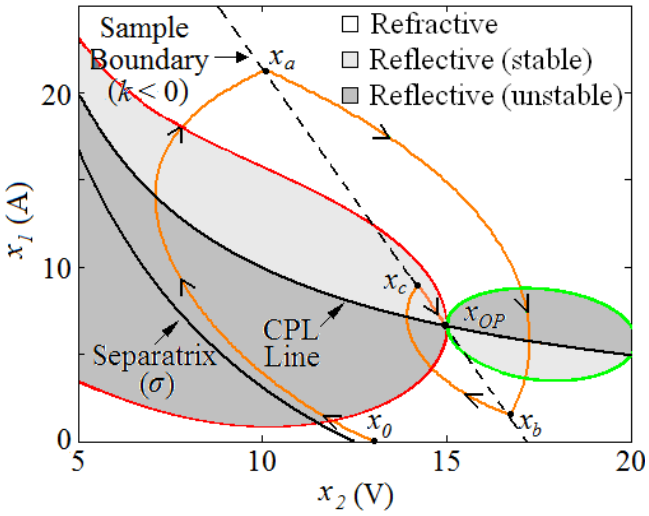


Figure 11: Transition of closed-loop converter from refractive to stable-reflective-mode operation.

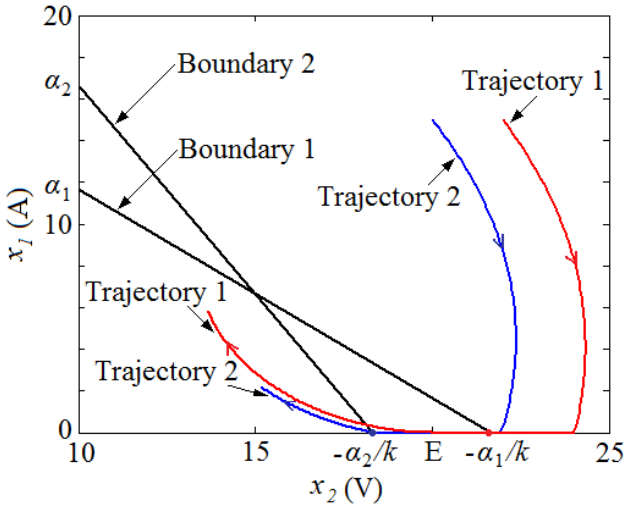


Figure 12: Trajectory behavior on the $x_2 = 0$ line for two different boundaries.

It has been previously determined that in the ON-state, all trajectories that have initial conditions to the right of V_{min} remain inside Ω. In addition, if a boundary that has a negative slope is used and refractive-mode operation occurs inside Ω, the off-state trajectories can only be driven towards the boundary or towards the $x_1 = 0$ line. Then, the two possible trajectory behaviors are depicted in Fig. 12—the trajectories end up passing through the stable-reflective region. As verified by the analysis, stable-reflective mode leads to direct asymptotic stability of the converter. For clarity, we restate here that the prescribed switch selection ($q(x) = 1$ below the boundary and $q(x) = 0$ above the boundary) and switching surfaces of the form $x_1 = x_{1OP} - k(x_2 - x_{2OP}) = 0$, $k < 0$ are employed. Hence, if the initial condition of the closed-loop converter system is inside the stability region of γ, then in this application the boundary controller ensures large-signal stability of the closed-loop system if the first interaction of the system's trajectory with the boundary results in stable-reflective-mode or refractive-mode operation.

DESIGN CONSIDERATIONS

Some design choices have been mentioned during the theoretical analysis. As stated earlier, a linear boundary, as opposed to quadratic or higher-order ones, was used for simplicity. In addition, a switch selection was prescribed so that the switch is ON below the boundary and it is OFF above the boundary. This switching strategy was chosen by inspecting Figs. 5 and 6 with the goal of ensuring that the various trajectories on one side of the boundary are directed into the other side. Subsequently, the use of boundaries with positive slopes was eliminated from the analysis, because such boundaries do not provide any stable-reflective region around the OP. The regions were determined via a method that uses rays that originate at the OP to track the directions of the various trajectories in the entire plane. The linear boundary finally chosen can be viewed as a special case of two of these rays.

With this control, reflective behavior is necessary around the OP in order to ensure stability, because in this behavior the trajectory stays as desired on the boundary. Hence, in reflective behavior and with a suitable controller design, the trajectory will converge into the desired operating point while evolving on the boundary. Around the OP, both rejective and refractive behaviors are undesirable. Thus, the design challenge is to select switching surfaces that, despite the presence of rejective and/or refractive behaviors, makes the trajectory to cross the switching boundary at a region where there is a stable reflective behavior so the trajectory converges to the desired closed-loop equilibrium point while staying on the boundary. The conditions that ensure large-signal stability provide some degree of freedom with regards selection of initial conditions when the controller starts to operate. Ultimately, design preferences determine this selection.

The proposed analysis approach allows identifying all possible system behaviors when trajectories in the state space intersect a boundary, and, thus, it provides a more

flexible design than other well known strategies, such as identifying the region of attraction of a sliding-mode controller through a candidate Lyapunov function proportional to the square of the switching surface [60]. The advantages of this approach in term of design flexibility gains can be used to understand transient behavior into closed-loop operation and to achieve adequate load coordination when dealing with real CPLs. For faster transients, it may be desirable to have mostly refractive operation initially, and then reflective operation close to the OP. However, if overshoot is a major concern, it may be desirable to have only reflective-mode operation, even though the result may be a longer transient. These behaviors are depicted in Fig. 12 where trajectory *B* is refracted from x_{B1} to x_{B2} and trajectory *A* first hits the switching surface in the stable-reflective region. Clearly, $\|x_{B2} - x_{OP}\| < \|x_{A1} - x_{OP}\|$ and trajectory *A* may result in faster transients. Another design parameter is the slope of the boundary, *k*. Inspection of Fig. 8 reveals that boundaries with slopes that are more negative may give a smaller reflective region around the boundary. However, they may be preferable if fast transients are desirable. Hence, if overshoots are a concern, a "*k*" that keeps most of the boundary inside the reflective region is desirable. As mentioned through (1) real CPLs exhibit such a behavior above an input voltage threshold V_{lim}. Hence, overshoot characteristics can be specified with the need for coordination between the length of the trajectory excursions and the expected V_{lim} encountered in real CPLs. For example, in Fig. 13 designs that allow lower output voltages such as those observed with *Trajectory B* can be used when CPLs are expected to have lower V_{lim}. However, if the allowable input voltage range is lower, evolutions such as that indicated by *Trajectory A* needs to be used.

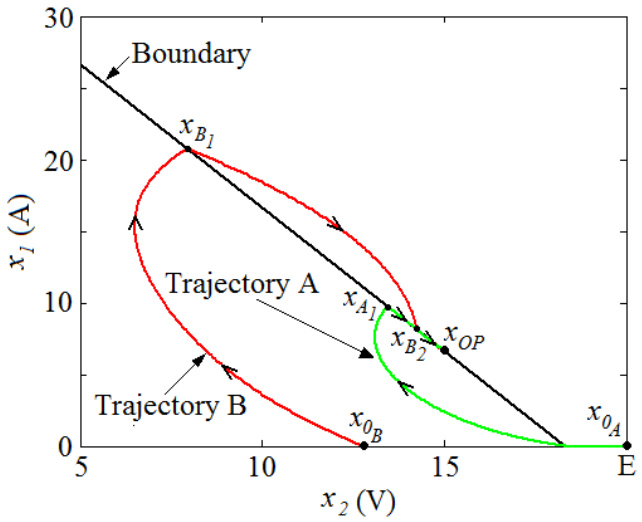


Figure 13: Selection of different initial conditions for transient optimization.

In open-loop, the capacitor, C charges up relatively quickly to E; thus, a separate start-up circuitry may not be necessary, because the loop can be closed as soon as the converter exhibits limit-cycle behavior. The initial condition of the closed-loop system is then $x_0 = \gamma$, which ensures that the necessary condition that x_0 should be in the stability region of γ for large-signal stability. Care should also be taken when selecting the value of k to ensure that the converter does not operate in unstable-reflective mode. To reduce the risk of this occurrence, the switching surface should be selected such that the point of intersection of the switching surface and the CPL, x_S (see Fig. 9), is as close as possible to the separatrix, σ. There are three alternative values for which the switching surface is tangential to φ_{OFF}: zero, infinity or some negative value. To ensure that the risk of unstable-reflective behavior is eliminated, for any given set of parameters, k can be selected slightly lower than the negative value of k that makes the switching boundary tangential to the upper φ_{OFF} curve. Another useful design tactic when possible would be to select equal numerical values for the inductance, L and capacitance, C, thereby

simplifying the computations of (18)-(28) that are used to obtain the design tool depicted in Fig.8.

There is a notable practical problem found in boundary control. Since crossing the switching surface commands the switch to turn on or off, once the trajectory intersects the boundary within a reflective region, it will evolve staying on the switching surface and leading to a very rapidly succession of alternate turn-on and turn-off commands. This behavior is termed chattering. In order to prevent chattering from occurring, the switching surface is replaced by two similar and parallel boundaries that form a hysteresis band. Switching decisions at the limits of the hysteresis bands depend not only on having the trajectory hitting one of the band's boundaries, but it also depends on the system state prior to crossing the boundary.

In reflective mode, the hysteresis band utilized has a direct effect on the amount of ripple present in both the inductor current and capacitor voltage ripples. That is, a wider hysteresis band corresponds to larger ripple content, while a narrower hysteresis band implies a relatively smaller ripple. However, if the hysteresis band gets too narrow, the converter may be forced to switch at a frequency higher than its maximum switching frequency, which may be destructive. Such situations should be avoided. It is noteworthy to mention that in addition to its role in preventing chattering, the use of a hysteresis band also guarantees that the invariant-set problem is averted, because the switching surface does not exactly pass through x_S.

We note here that the prior analysis is based on the implicit assumption that E and P_L take values within acceptable ranges—that is, E should not be excessively low and P_L should not be excessively high—that prevent very high-current conditions characteristic of the region to the left of the separatrix. A mathematical discussion of this range has

already been presented in the literature in [25] and for this reason is not further discussed in here.

Control Algorithm

The control algorithm presented here is based on the design process that yields a line with a negative slope that passes through the stable-reflective region, which is determined by equations (18) – (23), (26) and (28). A hysteresis band is added to avoid chattering. This hysteresis band contains the desired switching surface.

1. For simplicity, the buck converter could be started with $q(t) = 1$ prior to controller action, limit-cycle operation at the highest possible voltage serves as the closed-loop system's initial condition. This initial condition ensures that operation remains to the right of the separatrix and that practical loads are not self-disconnected due to very low input voltages.
2. After a short transient, the controller is started. When the controller action starts, if x is below the (lower) boundary, $q(x) = 1$ and the corresponding ON-state trajectory proceeds upwards until it hits the (upper) boundary where the switch function changes to $q(x) = 0$. Note that switching does not occur inside the hysteresis band.
3. If instead, when the controller action starts, x is above the (upper) boundary, the switch function becomes $q(x) = 0$ and the corresponding OFF-state trajectory proceeds to hit the (lower) boundary from above where the switch function changes to $q(x) = 1$.
4. Once switching occurs at the lower boundary, the trajectory evolve under $q(x) = 1$ until it hits the upper boundary, at which point $q(x)$ changes to zero and the cycle repeats again.

5. Switch action at the boundary also depends on the direction from which the trajectory is approaching the boundary. For instance, consider an ON-state trajectory approaching the switching surface from below. Switching does not happen when it hits the lower boundary. The trajectory passes through the hysteresis band until it hits the upper boundary, where switching occurs from $q(x) = 1$ to $q(x) = 0$. Similarly, an OFF-trajectory that approaches the boundary from above remains unchanged when it hits the upper boundary. It proceeds through the hysteresis band until it hits the lower boundary, where switching occurs into an ON trajectory. So, the switch function changes from $q = 0$ to $q = 1$ at the lower boundary only when the trajectory approaches the boundary from above. Conversely, switching occurs at the upper boundary only when a trajectory approaches the boundary from below and with $q = 1$. That is, thanks to a hysteretic action that is later implemented with an SR flip-flop. Switch action not only depends on the position, but also the direction that the trajectory approaches the boundary from. In addition, no switching occurs inside the hysteresis band.

SIMULATED AND EXPERIMENTAL VERIFICATION

The previous theoretical analysis was verified with simulations and an experimental setup in which a boundary controller is applied to a line-regulating source-interface buck converter feeding a buck converter with a tightly regulated output, as represented in Fig. 1. As shown in Fig. 14, the boundary controller is realized with a simple circuit that comprises operational amplifiers, an SR-flip flop—that provides the hysteretic behavior—and a gate drive chip. The buck converter with a tightly regulated output on the right in Fig. 1 has the following parameters: $R_L = 0.8\ \Omega$, $L_L = 100\ \mu H$, $C_L = 1.5\ mF$, V_L is regulated to about 7 V with a PI controller. Since the behavior of the CPL

converter is not the focus of this study these parameters were chosen in order to represent some average conditions found in [16] [17] and to show clearly the behavior of the line-regulating source-interface converter. The line-regulating source-interface converter comprises component values $L = 480\ \mu H$ and $C = 480\ \mu F$. The input voltage is $E =$ 17.5V. These parameters were also chosen to clearly demonstrate system behavior. The POL converter presents a CPL of approximately 68 W to the line-regulating source-interface and the system is driven to the OP, $x_{OP} = [5.5 \quad 12.4]^T$ by a switching surface with slope $k = -2.2$. A narrow hysteresis band with a vertical separation of 0.03 A is included to prevent the system from chattering. A measured open-loop ($q(t) = 1$) efficiency close to 99% indicates that the circuit's internal losses are well below the level for which they could affect the evaluation by damping the oscillatory behavior that are introduced by the CPL. That is, parasitics and capacitor leakage resistance are small enough to ensure CPL behavior. Sufficient conditions for the existence of CPL behavior in the presence of circuit parasitics and capacitor leakage resistance are easily derived by the approach used in [65], which along with the good match obtained between theory, simulations, and experiments, demonstrate that the assumptions made in the analysis are valid. The simulation results using *MATLAB/Simulink* and shown in Fig. 15 are in agreement with theoretical analysis. Initially and as recommended, the converter is operated in open loop with a duty cycle of 1. The closed loop has initial condition $x_0 = \gamma$ and when the switch is closed, the trajectory intersects the $x_1 = 0$ line. Then similar to *Trajectory 2* in Fig. 12, it slides to the left of the $x_1 = 0$ line until $x_2 = -\alpha/k$. At this point, the converter evolves according to the ON-state dynamics until stable-reflective mode is encountered; the trajectory is successfully driven to its OP. Figure 16 exemplifies the usefulness of introducing an hysteresis band by showing a magnified plot of the simulated system with a such a band with a vertical separation of 1 A, so that the

trajectory in closed-loop can be clearly seen within the hysteresis band. As shown, the switch commands do not occur at the boundary but are delayed until the trajectories hit either side of the hysteresis band. Hence, the switching frequency is limited and chattering may be prevented. Figure 16 also depicts how the hysteresis band directly affects the ripple present in the inductor current and capacitor voltage. The inductor current and capacitor voltage ripple are limited by the vertical separation and the horizontal separation of the hysteresis band respectively.

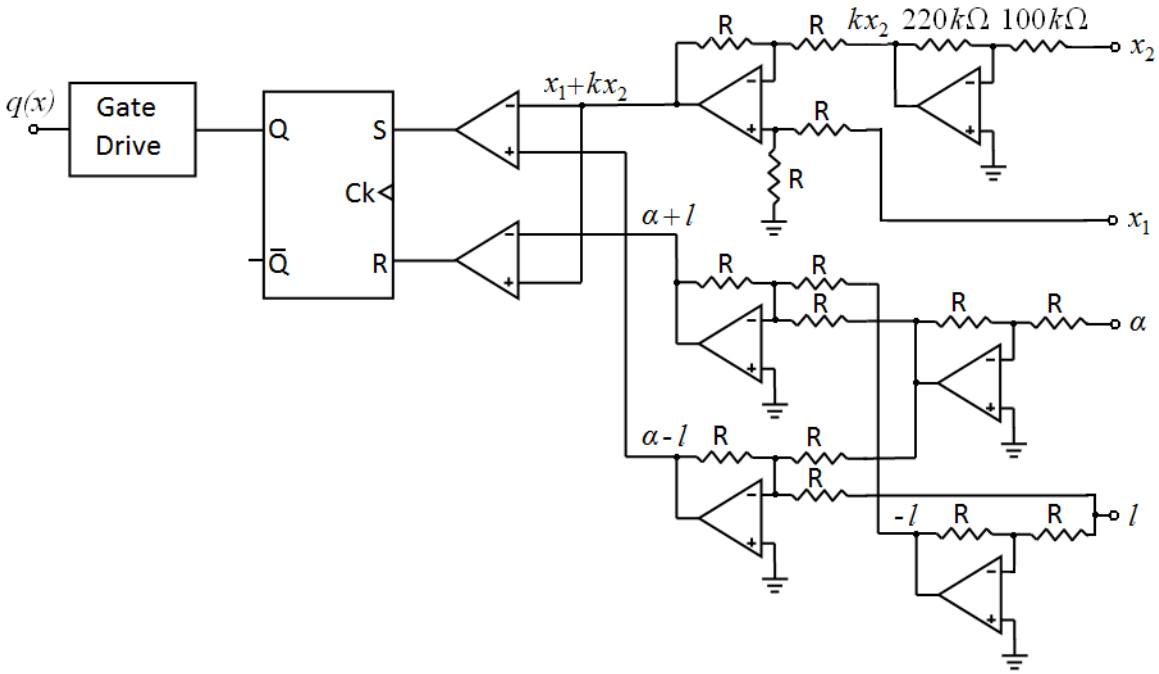


Figure 14: Schematic showing experimental implementation of the boundary controller. x_1, x_2, α and l are voltage signals; α is the x_1-intercept of the switching surface and $2l$ is the vertical separation of the hysteresis band. All resistances R = 100 $k\Omega$.

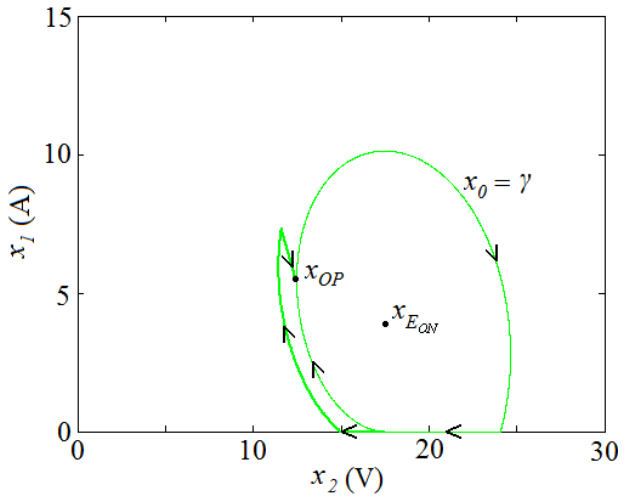


Figure 15: Simulated phase portrait showing controller action.

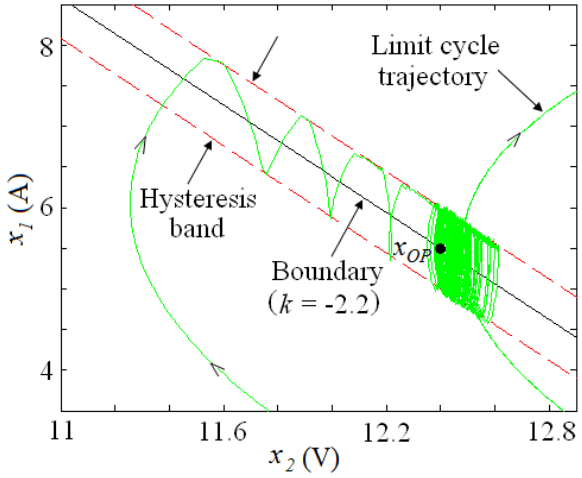


Figure 16: Magnified view of simulated verification showing hysteresis band ($\Delta x_1 \approx$ 1A).

This simulation and the previous theoretical analysis were both further verified with the experimental results presented in Figs. 17 to 21. Figure 17 shows the current and voltage waveforms for the line-regulating source-interface converter in the open loop. The CPL destabilizing effect is affirmed by the oscillatory waveforms. Figure 18 depicts the controller action. It is also illustrated in this figure that steady state operation at x_{OP} = [5.5 12.4]^T is obtained 1.4 ms after the boundary controller is turned on. This transient

is shorter than what is obtainable with other methods used to control CPLs, particularly linear PID or PD controllers such as those discussed in [5] and [25]-[27]. Also, as opposed to [22], with the boundary control method the order of the system is at worst the same. At best, and as mentioned earlier, the system's order is reduced by one when reflective mode is observed. Another advantage of this controller over those used in [25] [27], which is verified by experimental results, is that possible presence of noise does not affect the stabilization goal, whereas the differential term in [25] and [27] and in other works using linear controllers, such as [5] and [26], tend to introduce high noise sensitivity. In its practical implementation linear controllers such as those in [25] and [27] require adding filters in order to limit the noise amplification created by the differential term. In addition to complicating the controller design, these filters limit the controller bandwidth and slow-down its dynamic response. None of these limitations affect the proposed boundary controller, leading to still a very simple implementation and to a much faster convergence from the limit cycle into the operating point as it is evident by comparing Fig. 18 with Fig. 8 in [25]. Although circuit parameters are not equal, both experiments were conducted with parameters similar enough to allow valid comparisons between Fig. 18 here and Fig. 8 in [27]. Comparison of these two experimental figures also indicates a significant and undesirable current overshoot in the linear controller when the controller is commanded into closed-loop operation. This overshoot is not observed in the proposed boundary controller. Other advantages of the proposed strategy can be found over other past control methods. When compared to the controller in [7] the linear boundary proposed here can reach a user-set output operating voltage whereas the controller in [7] may not necessary achieve such a goal. Furthermore for the boundary controller no resistive load needs to be added to ensure stability; as it was necessary in [7].

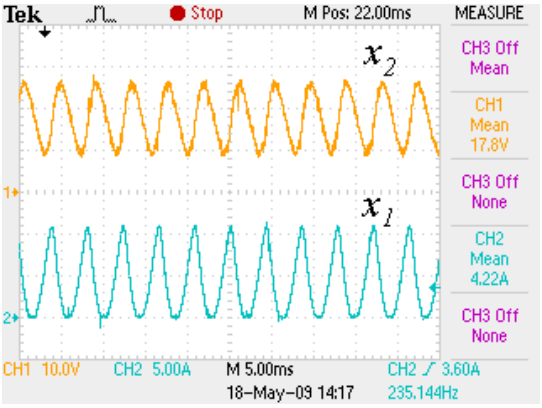


Figure 17: Experimental waveforms showing depicting CP-load behavior in open-loop.

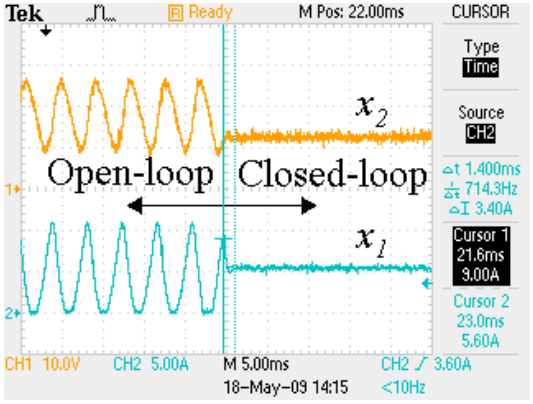


Figure 18: Experimental waveforms showing controller action from open to closed-loop operation and transient duration.

Figures 19 and 20 utilize experimentally generated phase portraits to further support the conclusions of the analysis showing an oscillatory (limit cycle) behavior when the converter operates in open loop. Figure 19 experimentally demonstrates the open-loop converter's limit-cycle behavior, while Fig. 20 portrays controller action by showing the state space trajectory from the limit cycle to the operating point within. Careful examination of Fig. 19 reveals that the experimentally generated phase portrait matches the simulation result presented in Fig. 15. Figure 21 shows steady state operation in time domain and demonstrates that the converter output achieves the desired operating

points without oscillations. Finally, Fig. 22 and Fig. 23 further support the simulations presented in Fig. 9 and Fig. 10 respectively. In both figures, the experimentally generated phase portraits are superimposed on the analytically determined regions. In Fig. 23, the POL converter presents a CPL of approximately 60 W to the line-regulating source-interface converter and the desired OP is x_{OP} = [4.8 12.5] ^{T}. However, a boundary with a positive slope of k = 1 is used and when the loop is closed, the switching surface is encountered in the unstable-reflective region. As predicted, the system closed-loop system does not recover from instability. In Fig. 22, the system trajectory is successfully stabilized to the desired OP of x_{OP} = [6.2 10] ^{T} by a first order boundary with k = –2.2. This time the line-regulating source-interface converter is subject to a CPL of approximately 62 W. Furthermore, with an average input current of 3.77 A, the closed-loop efficiency of the line-regulating source-interface converter was measured to be about 94%. This result shows that the losses and parasitics are small even with closed-loop operation. A comparison of the closed-loop efficiency with an open-loop efficiency of 99% stated earlier, reveals that most of the losses are from switching. As such, the parasitics did not affect the dynamics in both open and closed-loop operation. As with any state-dependent switching scheme, one minor drawback is that switching frequency varies with converter conditions. This issue can be resolved by applying a clocked pulse at the SR-flip flop's Ck-input in order to provide a fixed frequency, but it may result in increased ripple in the inductor current and capacitor voltage.

In order to evaluate the performance of the controller under real operating conditions, stable behavior with load and input voltage changes, and with and without load and line regulation were investigated. The parameters used in the simulations are the same used before with L = 480 μH, C = 480 μF, E = 17.5 V, P_L = 68.2 W, and x_{OP} = [5.5 12.4]^{T}. Figure 25 shows how the locus of ON and OFF transition points

change and reveals that in this application a linear boundary controller can be immune to variations in the input voltage E. Essentially, with variations in E, the OP remains at the same position; only x_E and φ_{ON} change. Figure 26 illustrates experimentally, that variations in E do not affect the control objective and system behavior. However, a change in load level, P_L, changes the load line and moves the OP from x_{OP} to x_{OPA} as shown in Figure 27. These predictions are confirmed when the system is simulated using a first order boundary controller with k = -2.2. In order to keep the output voltage of the line-regulating source-interface converter, x_{2OP}, constant, x_{1OP} is varied with corresponding variations in P_L. The OP becomes $x_{OP} = [P_L/x_{2OP} \quad x_{2OP}]^T$. That is, x_{2OP} is fixed and $x_{1OP} = P_L/x_{2OP}$ is fed back to the boundary controller. This translates to a vertical motion of the switching surface, so that the controller now regulates x_{OP} to x_{OPB}. In other words, the controller changes only the x_{1OP} component of x_{OP}. As Fig. 27 shows, the boundary for the new operating point still passes through reflective stable regions corresponding to the new load conditions. Hence, the trajectories for the new load condition will still intersect the boundary at a reflective stable region, which implies that the stability behavior for the new load will still conserve the same characteristics observed for the original load. That is, stability is preserved. Figure 28 shows a phase portrait of the regulation with an increase and a decrease in P_L. Variations in E are also introduced, but as expected, they cause no problems. Figure 29, shows the evolution of the state variables with load variation in both cases. Figures 30 and 31 are experimental results obtained when P_L is increased from about 60 W to about 105 W. Without regulation, (Fig. 30), the OP is shifted from $x_{OP} = [4.0 \quad 15.0]^T$ to $x_{OP} = [9.0 \quad 11.7]^T$, while with regulation (Fig. 31), the OP is moved to $x_{OP} = [7.0 \quad 15.0]^T$, maintaining the output voltage at 15 V. A change in operating point is observed in both cases;

however, in Fig. 31, the output voltage is successfully regulated. As expected, stable steady operation is maintained.

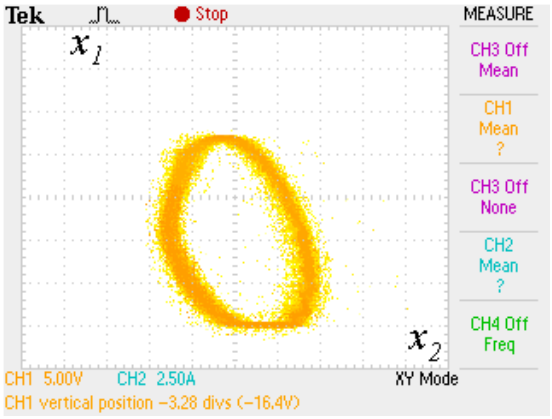


Figure 19: Experimentally generated phase portrait showing CP-load behavior in open-loop.

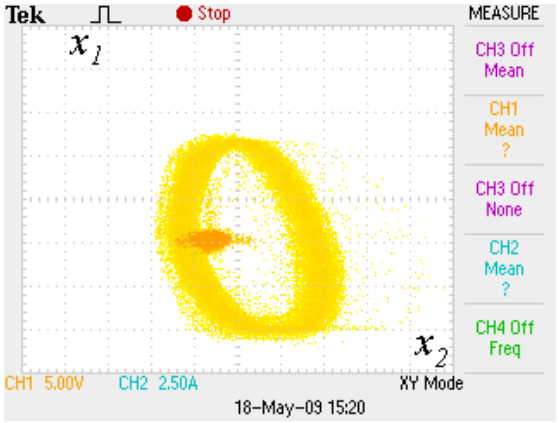


Figure 20: Experimental generated phase portrait showing controller action.

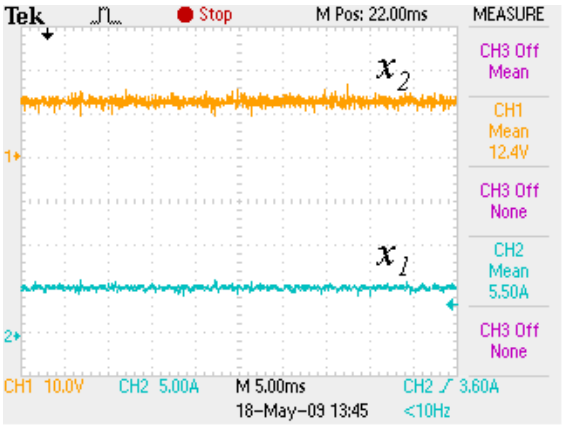


Figure 21: Experimental waveforms showing closed-loop converter behavior.

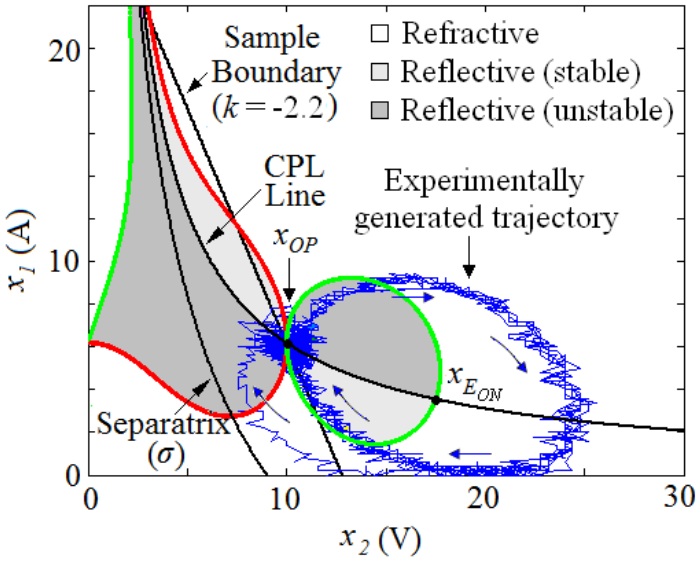


Figure 22: Experimentally generated phase portrait showing stable behavior with a boundary with negative slope.

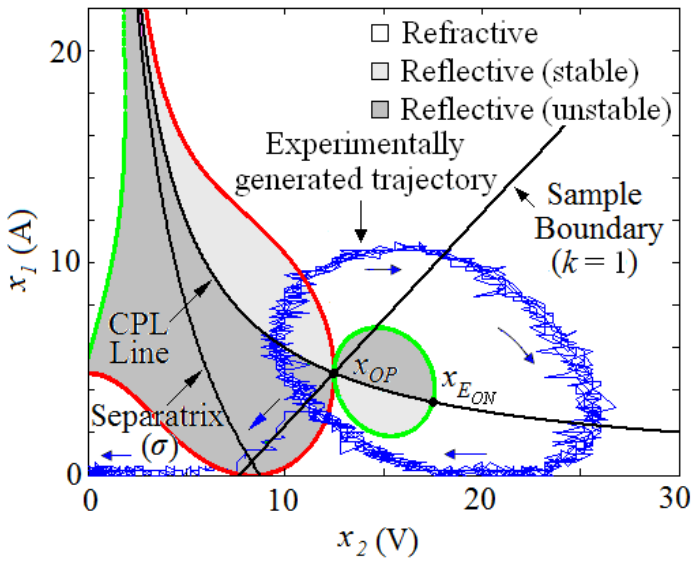


Figure 23: Experimentally generated phase portrait showing instability with a boundary with positive slope.

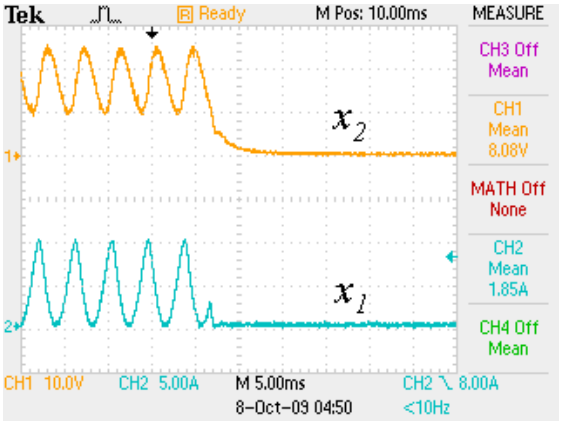


Figure 24: Experimental waveforms showing instability with a boundary with positive slope.

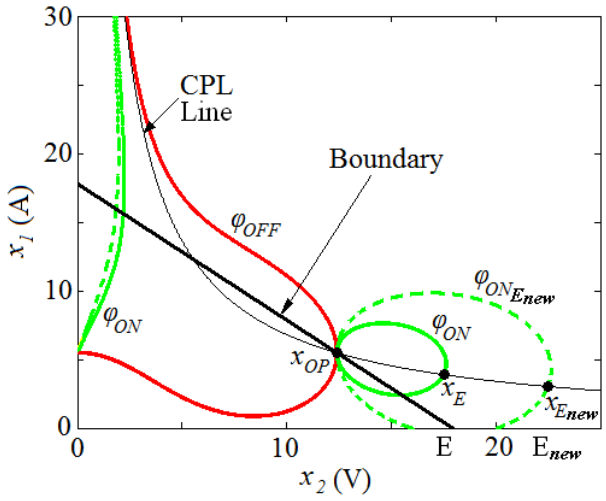


Figure 25: Loci of transition points with an increase in E from 17.5 V (solid) to 22.5 V (dashed).

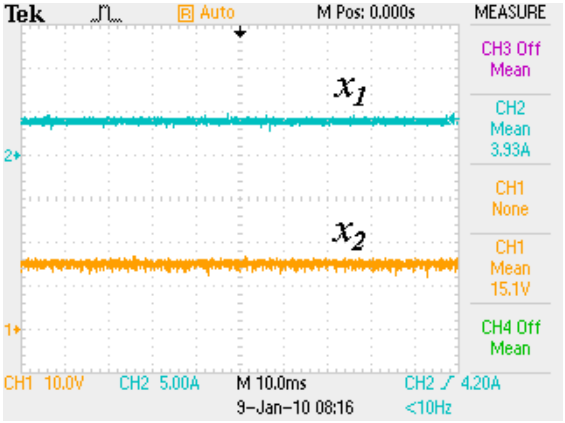


Figure 26: Experimental waveforms showing immunity of the controller to variations in E when it increases from 17.5 to 27.5 V.

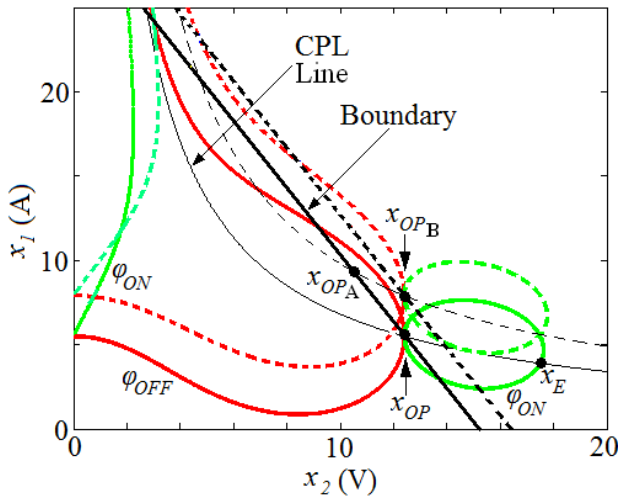


Figure 27: Load line and loci of transition points with an increase in P_L from 68.2 W (solid) to 88.2 W (dashed).

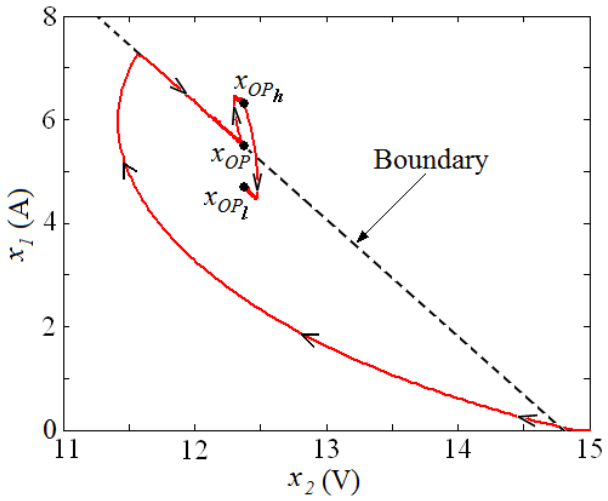


Figure 28: Phase portrait showing regulation with a 10 W increase and a subsequent 20 W decrease in P_L.

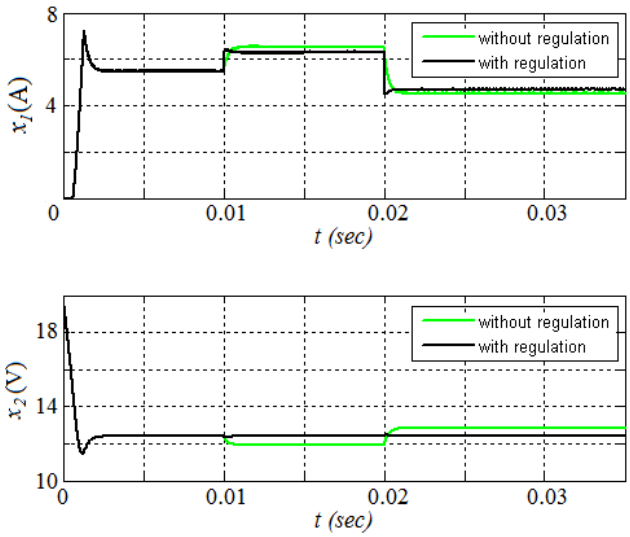


Figure 29: Simulation showing operation under load change with and without regulation. P_L increases by 10 W at 0.01 s and decreases by 20 W at 0.02 s. E increases by 10 V at 0.015 s and decreases by 10 V at 0.025 s.

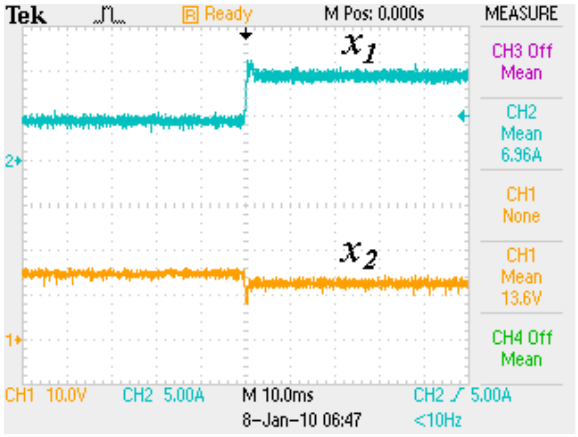


Figure 30: Experimental waveforms showing a change in the OP when P_L increases from approximately 60 W to 105 W.

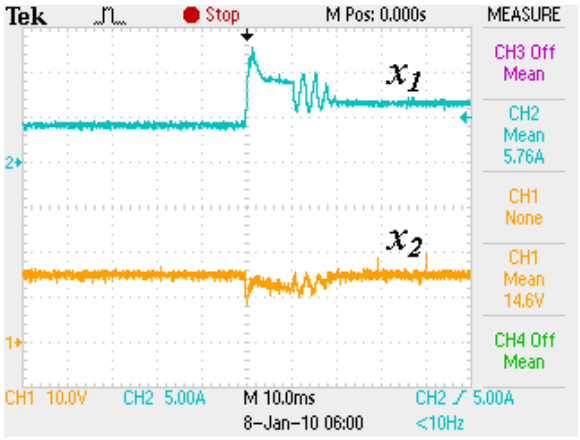


Figure 31: Experimental waveforms showing successful regulation of the output voltage of the line-regulating source-interface buck converter when the CPL suddenly increases from approximately 60 W to 105 W.

Chapter 3: Non-Minimum Phase Converters with Constant-Power Loads

In this section, the other two basic converter topologies are studied: boost and buck-boost. Figures 32 and 33 each show two stages of distributed power architectures, in which boost and buck-boost LRSI converters are subject to CPLs. Firstly, the dynamics of both converters is described. Next boundary control is analyzed for these two converters. The study shows that analysis of boundary control for non-minimum phase converters is more challenging than the buck case; however, similar results are achieved.

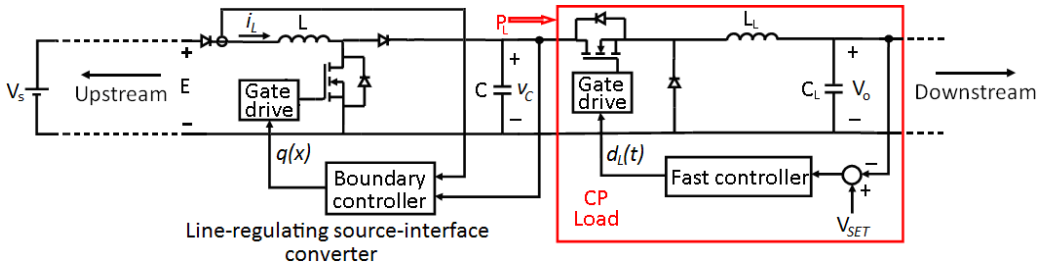


Figure 32: Circuit schematic showing a line-regulating source-interface (boost) converter on the left feeding a CPL on the right.

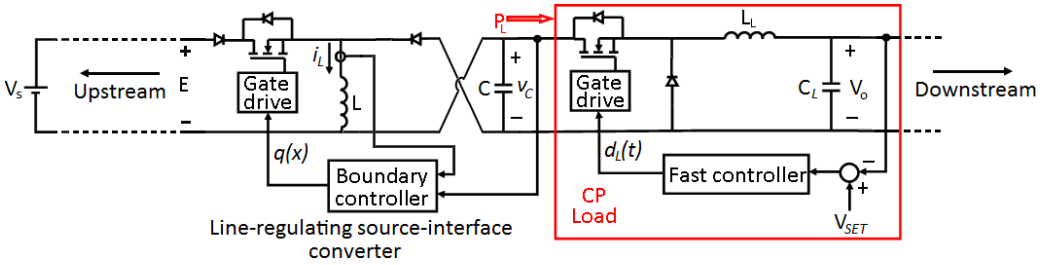


Figure 33: Circuit schematic showing a line-regulating source-interface (buck-boost) converter on the left feeding a CPL on the right.

BOOST CONVERTER WITH INSTANTANEOUS CONSTANT-POWER LOADS

Ideal boost converter dynamics with an ideal CPL and in continuous conduction mode can be represented as

$$f\left(i_L, v_C\right) = \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{L}\left(E - \left(1 - q(t)\right)v_C\right) \\ \frac{1}{C}\left(\left(1 - q(t)\right)i_L - \frac{P_L}{v_C}\right) \end{bmatrix} \tag{31}$$

$$i_L \geq 0, v_C > 0, \tag{32}$$

where *q(t)* is the (open-loop) switching function acting on the input switch in the line-regulating source-interface converter on the left in Fig. 32. From conventional power electronics nomenclature $x = [x_1 \quad x_2]^T = [i_L \quad v_C]^T$ [28]. With this model, the load line is a constant-current line given by

$$x_1 = \frac{P_L}{E}. \tag{33}$$

It can be observed that existence and uniqueness of solution is guaranteed only on $\Psi = R^2 - \{x_2 = 0\}$ [27]. As in the buck case, in this section, our analysis is performed on $\Omega = \Psi \cap \{x: x_1 \geq 0, x_2 > 0\}$. Discontinuous conduction mode is neglected, because in most practical applications its effect on the converter dynamics with CPLs is not significant [27]. When the switch is off, $f(i_L, v_C)$ is termed $f_{OFF}(x)$; when the switch is on, $f(i_L, v_C)$ is termed $f_{ON}(x)$. The OFF-state dynamics for the boost converter with CPLs is the same as that of the ON-state dynamics for the buck converter [50]. It is observed that in this state the equilibrium point x_{EOFF}, which is located at $[P_L/E \quad E]^T$, is unstable, and within reasonable ranges of E and P_L, characteristic CPL oscillations occur [27]. Similar to the buck converter ON-state, the constraints given by (32) induce limit cycle behavior in the boost converter OFF-state dynamics. As a result, depending on the initial conditions, boost converters with CPLs may exhibit either a limit cycle behavior or may tend to a high-current, low-voltage condition [27].

Controller Analysis and Large-Signal Stability

In this section, the loci of transition points and the various regions of operation of the boost converters with CPLs are obtained based on the procedure outlined in [50] for the buck converter. The controller action follows a state-dependent switching strategy ($q = q(x)$) [49] [50]. The analysis is still based on a first order switching surface of the form

$$\lambda : x_1 = k(x_2 - x_{2OP}) + x_{1OP}, \tag{34}$$

which determines switching operation and where x_{OP} is the desired closed-loop operating point (OP). Inspection of phase portraits of the boost converter in each switching state helps us to prescribe our switch selection as: $q(x) = 1$ (ON trajectories) below, and $q(x) = 0$ (OFF trajectories) above the boundary, for both boost and buck-boost converters [50] [29] [30].

The locus of ON and OFF transition points for the boost converter is given by

$$\varphi_{ON}(x) = LP_L(x_1 - x_{1OP}) + CEx_2(x_2 - x_{2OP}) = 0 \tag{35}$$

$$\varphi_{OFF}(x) = L(x_1 - x_{1OP})(x_1x_2 - P_L) - Cx_2(E - x_2)(x_2 - x_{2OP}) = 0, \tag{36}$$

and the various regions of operation are depicted in Fig. 3. Parameters used in the simulation are: $E = 10$ V, $P_L = 61.25$ W, $L = 470\ \mu H$, $C = 500\ \mu F$, $x_{OP} = [6.13 \quad 30]^T$. In order to investigate the stability properties of the OP in reflective mode, consider the following *positive-definite* and *decrescent* energy-like function [60] as a candidate Lyapunov function

$$V(x) = \frac{1}{2}\|x - x_{OP}\|^2 > 0. \tag{37}$$

Unlike the buck converter, the discontinuous function $q(x)$, appears in the expression for $\dot{V}(x)$ when $V(x)$ is differentiated along the trajectories of the boost converter given by (31). To avoid dealing with $q(x)$, which is undefined on the switching surface, we use Filippov's method [66] [67] to define a solution in reflective-mode operation, which is the mode of interest here. Our switched system is represented by

$$\dot{x} \in f(x) = \begin{cases} f_{ON}(x) & ,\lambda < 0 \\ f_{OFF}(x) & ,\lambda > 0 \end{cases}. \tag{38}$$

In reflective mode ($\lambda = 0$), we define an extension of $f(x)$ as

$$F(x) = \overline{co}\{f_{ON}(x), f_{OFF}(x)\} := \{\alpha f_{ON}(x) + (1-\alpha) f_{OFF}(x) : \alpha \in [0,1]\}. \tag{39}$$

The set-valued function $F(x)$ is compact and convex by definition. In addition, $f_{ON}(x), f_{OFF}(x) \in F(x)$ implies that $F(x)$ is upper semicontinuous. An absolutely continuous function *x* is a solution of our switched system in the sense of Filippov, if it satisfies the differential inclusion

$$\dot{x} \in F(x). \tag{40}$$

Existence of a Filippov solution is guaranteed by virtue of $F(x)$ being bounded, closed, convex and upper semicontinuous [66]. Furthermore, the transversality condition is satisfied, because with reflective mode operation there is always a cross intersection of the orbit with the switching surface. Hence, *x* is unique for all initial conditions, $x_O \in \{x : \lambda = 0\}$ in reflective mode operation [67] [68]. Notice, however, that the intersection of f_{ON} and f_{OFF} with the switching surface at transition points, φ_{ON} and φ_{OFF}, respectively, are not transversal. Thus, these transition points φ_{ON} and φ_{OFF} are not included as part of any region. For instance, in Figure 34, φ_{ON} and φ_{OFF} do not belong to reflective, refractive or rejective regions. They are simply boundaries of the various regions in the plane. Furthermore, transition points should generally be avoided to prevent system stalling [50]. If the derivative of λ is taken, we have $\dot{x}_1 = k\dot{x}_2$. Then, *V(x)* is differentiated along the trajectories of $F(x)$ and α can be eliminated, to yield

$$\dot{V}(x) = \frac{1+k^2}{kLx_1 + Cx_2}(x_2 - x_{2_{OP}})(Ex_1 - P_L). \tag{41}$$

where $(1+k^2)/(kLx_1 + Cx_2) > 0$ simply corresponds to reflective-mode operation. Hence, $\dot{V}(x) < 0$ if $x_2 < x_{2OP}$ and $Ex_1 > P_L$, or if $x_2 > x_{2OP}$ and $Ex_1 < P_L$. These conditions guarantee stable reflective-mode operation. On the other hand, $\dot{V}(x) > 0$ if $x_2 < x_{2OP}$ and

$Ex_1 < P_L$, or if $x_2 > x_{2OP}$ and $Ex_1 > P_L$; and the OP is unstable in reflective mode. Hence, instability may still occur in reflective mode. In particular, first order boundaries with $k > 0$ create an unstable reflective region around the OP. Hence, first-order (linear) boundaries with $k > 0$ must not be used. Equation (41) also reveals that in reflective mode, the load line is invariant and the converter may stall—the "invariant-set" problem also present in the buck converter [50]. The rejective region (see figures 34 and 35) must be avoided, because in this region trajectories are directed away from switching surfaces [28] [49]. In the case of the boost converter, when controller action begins, the use of switching surfaces with $k > 0$ may yield another (stable) limit cycle that is manifested as undesirable large oscillations in both state variables (see Figure 37).. This limit cycle occurs because the trajectory slides on the boundary away from the OP as soon as it hits the switching surface at "c." The trajectory then leaves the switching surface when it crosses φ_{OFF} and enters the refractive region at "d". Figures 36 and 37 simulate the behaviour of the converter with a switching surface that has a negative and a positive slope respectively. Simulation parameters are: $E = 10$ V, $P_L = 25$ W, $L = 470\ \mu H$, $C = 500\ \mu F$. As shown, a boundary with $k < 0$ yields stable-reflective operation, while a boundary with $k > 0$ gives unstable-reflective operation.

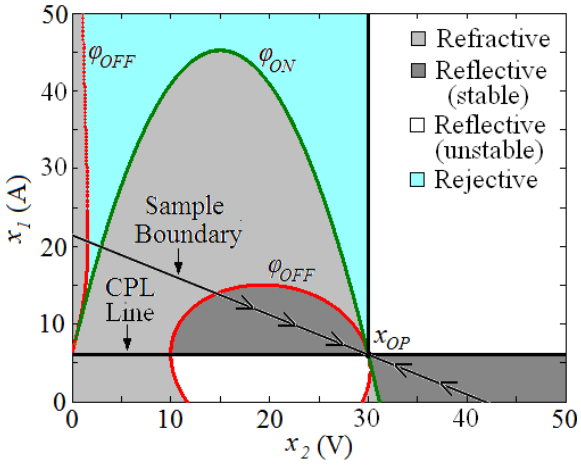


Figure 34: Simulations showing regions of operation for a boost converter with a CPL.

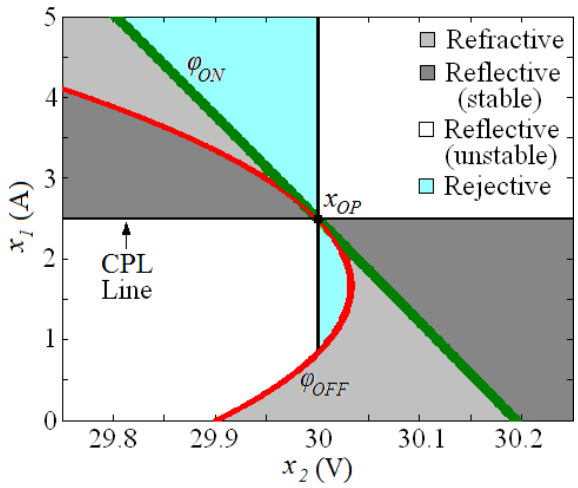


Figure 35: Magnified plot showing rejective region around the desired OP for a boost converter.

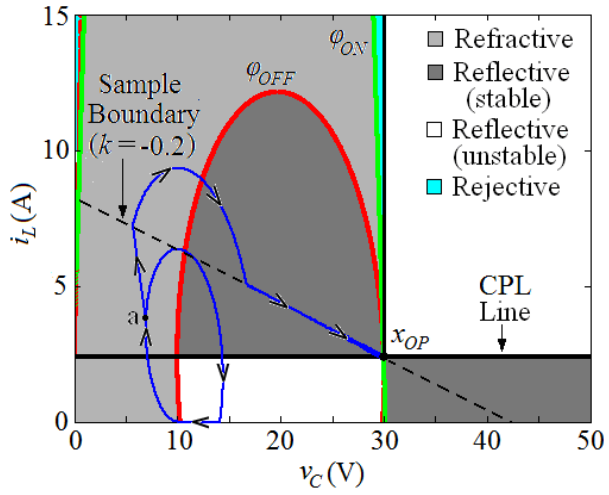


Figure 36: Simulation results for a boost converter showing stable reflective operation, $k < 0$; controller action starts at point "a."

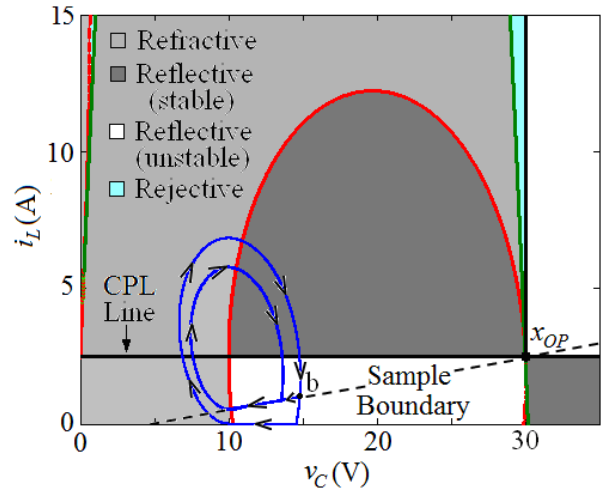


Figure 37: Simulation results for a boost converter showing unstable operation, $k > 0$; controller action starts at "c."

BUCK-BOOST CONVERTER WITH INSTANTANEOUS CONSTANT-POWER LOADS

Ideal buck-boost converter dynamics with an ideal CPL and in continuous conduction mode can be represented as

$$f(i_L, v_C) = \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{L}(q(t)E - (1-q(t))v_C) \\ \frac{1}{C}\left((1-q(t))i_L - \frac{P_L}{v_C}\right) \end{bmatrix} \tag{42}$$

$$i_L \geq 0, v_C > 0 \tag{43}$$

The load line of the buck-boost converter with a CPL is given by

$$x_1 = \frac{P_L}{Ex_2}(E + x_2) \tag{44}$$

Buck-boost converter ON-state dynamics is the same as that of the boost converter, and the OFF-state dynamics is the same as that of the buck converter with a CPL [50]. In both ON and OFF states, the ideal buck-boost converter has no equilibrium points within the finite state space. However, thanks to the nonlinear nature of the system, and equation (43), limit cycles can be observed for duty cycles between 0 and 1 [27], particularly for modest to large duty cycles that make the limit cycle to be further away from the separatrix that separates the trajectories that converge to the limit cycle from those that tend to a point of very low capacitor voltage and very large inductor current [27]. This is a very interesting display of nonlinear phenomena in switched system dynamics, in which even though in both duty cycle extremes there is no steady state, for certain intermediate duty cycle ranges, limit cycle behavior still occurs.

Controller Analysis and Large-Signal Stability

Again, inspection of phase portraits of both converters in each switching state helps us to prescribe our switch selection as: $q(x) = 1$ (ON trajectories) below, and $q(x) = 0$ (OFF trajectories) above the boundary, for both boost and buck-boost converters [50] [29] [30]. The locus of ON and OFF transition points for the buck-boost converter is given by

$$\varphi_{ON}(x) = LP_L(x_1 - x_{1OP}) + CEx_2(x_2 - x_{2OP}) = 0, \tag{45}$$

$$\varphi_{OFF}(x) = L(x_1 - x_{1OP})(x_1 x_2 - P_L) + C{x_2}^2(x_2 - x_{2OP}) = 0, \tag{46}$$

and the various regions of operation are depicted in Fig. 38. Figure 39 shows a detailed view of Fig. 38 around the OP clearly. Simulation parameters are: E = 10 V, P_L = 25 W, L = 470 μH, C = 500 μF, x_{OP} = [4.06 16] ^{T}. Using the same candidate Lyapunov function defined in (10) to investigate the stability of the OP in reflective mode. Just as was done for the boost converter case, for the buck-boost converter we differentiate λ, and $V(x)$ along $F(x)$ and eliminate α to obtain

$$\dot{V}(x) = \frac{1+k^2}{x_2\left(kLx_1 + C\left(x_2 + E\right)\right)}\left(x_2 - x_{2_{OP}}\right)\left(Ex_1x_2 - P_L\left(x_2 + E\right)\right), \tag{47}$$

where $(1+k^2)/(kLx_1 + C(x_2 + E)) > 0$ corresponds to operation in reflective-mode. Equation (47) reveals that for the buck-boost converter, the reflective region also comprises stable and unstable sections on either side of the load line as shown in Figure 38. Converter stalling may also occur with the buck-boost converter [50]. Similar to the buck [50] and boost converters, a linear switching surface with $k < 0$ ensures that reflective-mode operation directs the trajectory to the OP, while boundaries with $k > 0$ cause sliding away from the OP. Figures 40 and 41 illustrate these behaviors with simulations. In Fig. 40, k = –0.65 gives stable-reflective operation, while in Fig. 41, k = 0.5 yields unstable-reflective operation.

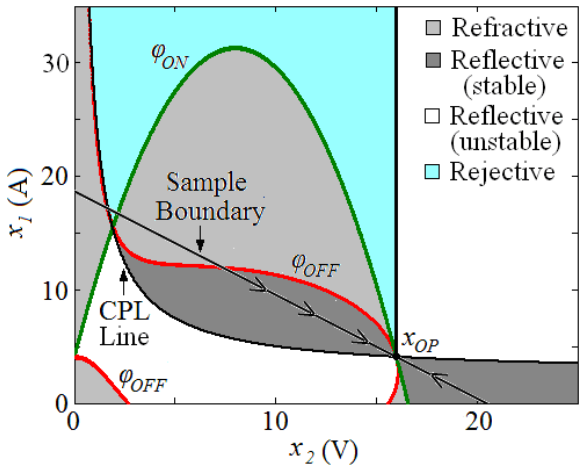


Figure 38: Simulation of buck-boost converter with CPL showing the regions of operation.

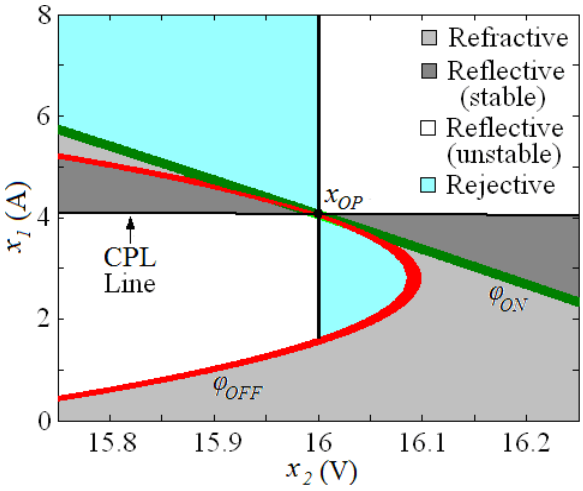


Figure 39: Simulation of buck-boost converter with CPL showing detail of Fig. 4 (a) around the desired OP.

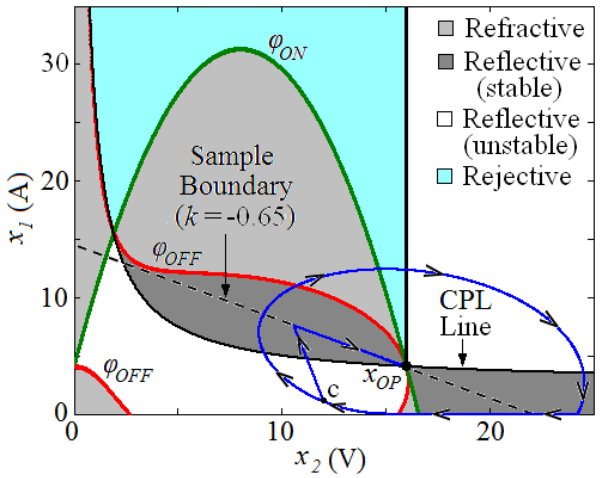


Figure 40: Simulation results showing stable reflective operation for a buck-boost converter, $k < 0$; controller action starts at point "c."

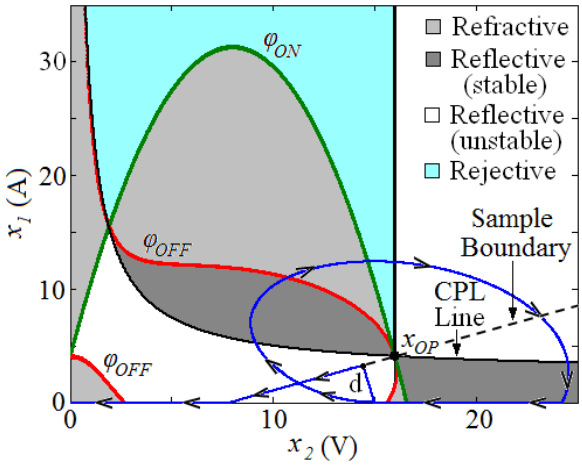


Figure 41: Simulation results showing stable reflective operation for a buck-boost converter, $k > 0$; controller action starts at point "d."

DESIGN REMARKS

For the boost converter, limit cycle operation with $q(t) = 0$ can successfully initiate closed loop operation, but in the case of the buck-boost converter, a start up circuitry is necessary, because none of the two switching states yields an equilibrium state [27]. It is noteworthy to mention that in both converters, refractive behavior may still lead to stability if subsequent trajectory interaction with the switching surface occurs

in the stable-reflective region. In the case of the boost converter, if interaction with the switching surface in refractive mode occurs in the unstable region of the limit cycle ($q(t) = 0$), then a high-current, low-voltage condition—voltage collapse—may occur. Contrary to the results obtained with the buck converter [50], rejective-mode operation can occur with the boost and buck-boost converters. Switching surfaces that pass through rejective regions must be avoided because trajectories on either side of boundaries in this region are directed away from the switching surface. In both simulation and experiment, the boundary's slope, k, was chosen such that to the right of the separatrix, the switching surface did not pass through the rejective region. As with the buck converter [50], the design trade-off between fast transients and overshoot is also present here. In addition, switching surfaces with lower (more negative) slopes tend to yield higher overshoots for both converters. Current overshoot is more unpredictable with the boost converter when trajectory interaction with the switching surface occurs outside the stable-reflective region as shown in Fig. 36. Then, the natural evolution of the OFF-state trajectory determines the current overshoot value. However, in the case of the buck-boost converter, phase portraits can easily reveal that the OFF trajectories are always directed downwards (towards the $x_1 = 0$ line), so the trajectories are better behaved in that regard. Finally, it is desired that the first closed-loop trajectory interaction with the switching surface takes place in the stable-reflective region because this guarantees large-signal stability of boost and buck-boost closed-loop converter system [50]. For the buck-boost converter, the limit cycle passes through the stable-reflective region on both sides of the OP, so if the boundary is situated sufficiently inside this region, large-signal stability of the OP follows. In the case of the boost converter we take advantage of the nature of the OFF-state trajectories, which are still directed towards the $x_1 = 0$ line (as in Fig. 36), so that subsequent interaction with the boundary occurs in the stable-reflective region.

EXPERIMENTAL VERIFICATION

Experimental verification of the analysis is presented in this section. The boundary controller circuit is realized with operational amplifiers, an SR-flip flop that provides hysteretic behavior, a gate drive chip and analog multipliers for regulation. A hysteresis band with a vertical separation of 0.04 A was implemented to prevent chattering [28].

Figure 42 and 43 show successful stabilization of a boost converter with an instantaneous CPL using a boundary with a negative slope ($k = -0.2$). As recommended, the closed-loop system's initial condition was the OFF-state stable limit cycle. The intended OP is $x_{OP} = [2.4 \quad 30]^T$, and parameters used in the experimental setup are $E =$ 10 V, $P_L \approx$ 24 W, $L = 470\ \mu H$, $C = 500\ \mu F$. Instability caused by a wrong choice for the boundary is demonstrated in Fig. 44 using a switching surface that has a positive slope ($k = 0.2$). The intended OP is $x_{OP} = [2.8 \quad 20]^T$, but instead, another limit cycle is obtained in closed loop operation. Figures 43 and 44 show that experimental waveforms match the expected simulated behaviors presented in Figs. 36 and 37. Load and line regulation were also implemented by varying x_{1OP}, thus restricting the OP to movements in the x_1 direction [50]. Here, x_{1OP} was replaced by P_L/E in the controller. Figures 45 and 46 indicate successful load and line regulation. In the former figure, P_L is increased from approximately 16.2 W to 39.2 W, whereas in the latter E is increased from 10 V to 15 V. The output voltage stays steady at 30 V in both cases. A measured efficiency of about 95% reveals that losses were low and the effects of parasitics were minimal. Hence, the analysis based on an ideal converter is valid as the effects of parasitics, such as those that could have attenuated the limit cycle oscillations, are not significant.

For the buck-boost converter, a start-up circuitry was necessary to ensure that limit-cycle behavior was obtained prior to controller action. Thus, a duty ratio of 0.6 was

used to ensure that a limit cycle was obtained in open-loop operation and this limit cycle also served as an initial condition for closed-loop operation. The same values for *E, L* and *C* that were selected for the boost converter were used for the buck-boost. Figure 47 shows successful stabilization using a boundary with a negative slope ($k = -0.6$); $P_L \approx$ 27.6 W, $x_{OP} = [4.8 \quad 13.5]^T$. An average input current of 2.94 A implies a relatively high efficiency of about 94% at closed loop, which validates having neglected parasitics during the analysis. Figure 48 illustrates instability using a boundary with $k = 0.4$. Load regulation is shown in Fig. 49, where the output voltage stays steady at 20 V when P_L is increased from approximately 18.7 W to 37.3 W. The relatively large overshoots present stem from interaction of the almost opposing ON and OFF trajectories of the buck-boost converter with the moving boundary during regulation. Figure 50 shows line regulation when E is increased from 10 V to 15 V; $P_L \approx$ 38 W. In all cases the proposed boundary controller achieved its intended objectives.

Figures 42 and 47 show that stabilization for the boost and buck-boost converters occurs in about 15ms and 12.5ms respectively, as compared to about 300ms and 50ms with the linear controller in [20] respectively—faster transient performance. Figures 46 and 50 show that line regulation for the boost and buck-boost converters is achieved in about 5ms (with a 50% variation in input voltage), as comparable to about 200ms and 400ms (with only a 25% variation in input voltage) that is attained with the linear controller in [27]. That is, faster line regulation is obtained with boundary control even with larger input-voltage variation. Figures 45 and 49 reveal that, for load regulation, it takes about 12.5ms and 75ms to reach the new steady state for the boost and buck-boost converters respectively—with over 200% variation in load. Comparison with [27] is not possible in this case because in [27] only a 15% variation in the load was considered.

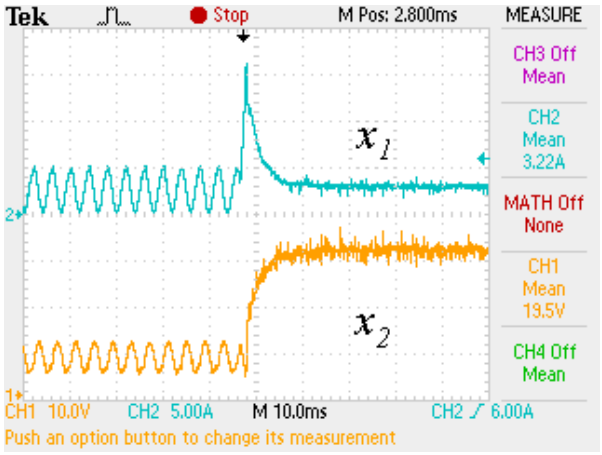


Figure 42: Boost converter experimental waveform showing stabilization using a boundary with a negative slope

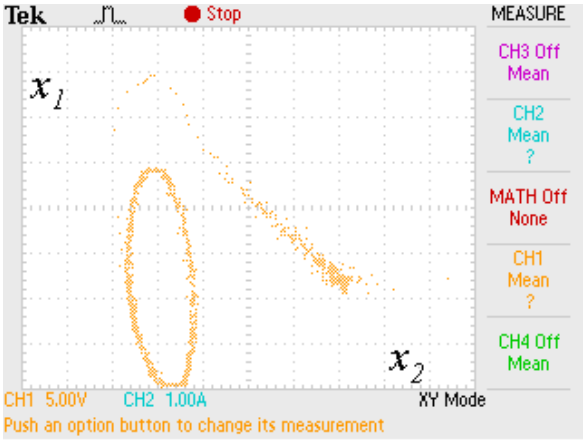


Figure 43: Boost converter experimental phase-portrait showing stabilization using a boundary with a negative slope.

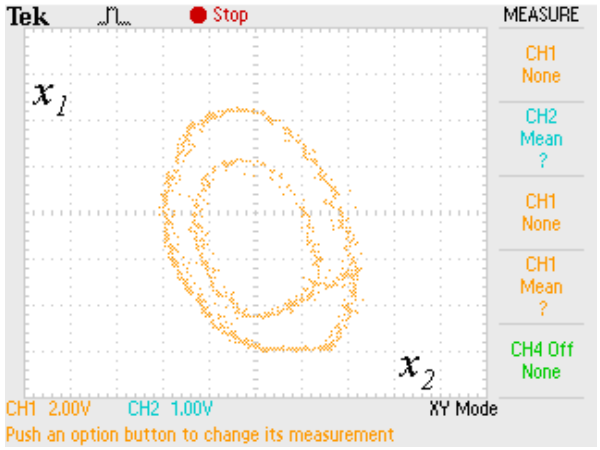


Figure 44: Boost converter experimental phase-portrait showing instability (closed-loop limit cycle operation) when a boundary with a positive slope is used.

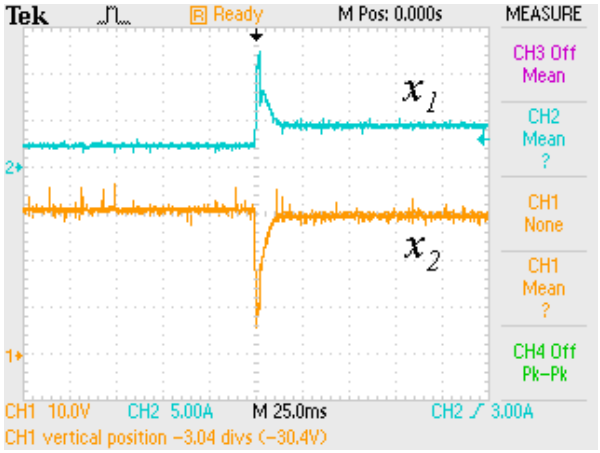


Figure 45: Boost converter experimental waveforms showing load regulation.

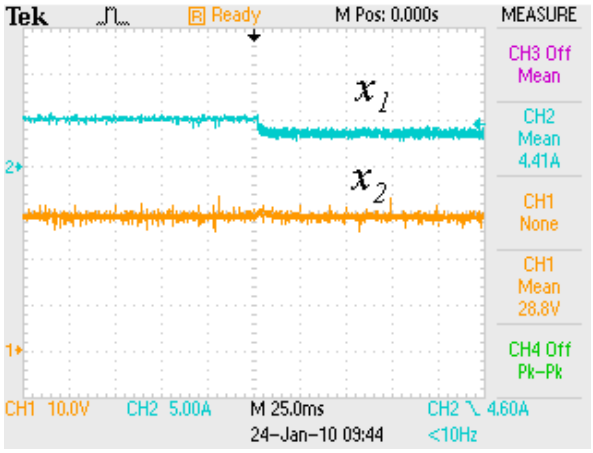


Figure 46: Boost converter experimental waveforms showing line regulation.

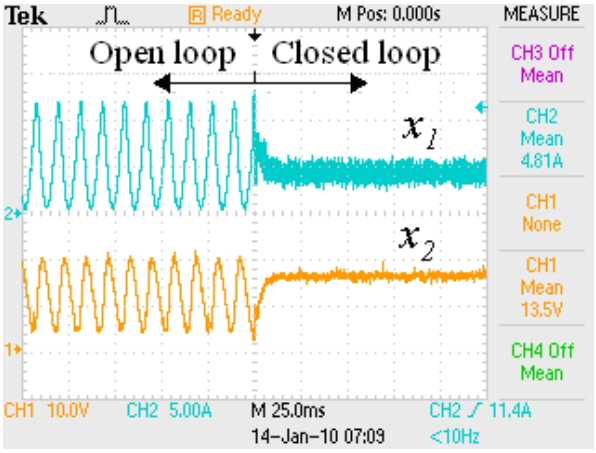


Figure 47: Buck-boost converter experimental waveforms showing stabilization using a boundary with a negative slope.

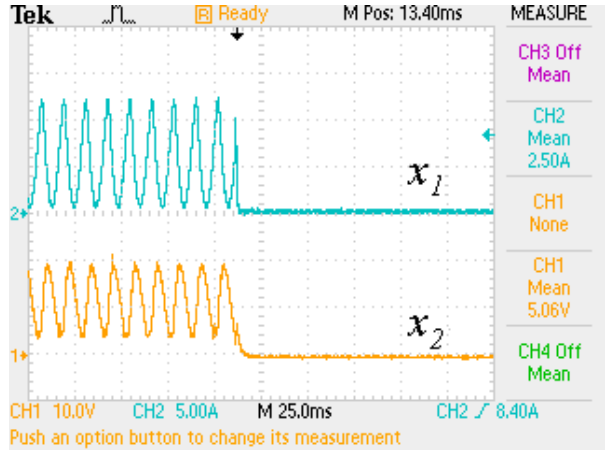


Figure 48: Buck-boost converter experimental phase-portrait showing instability when a boundary with a positive slope is used.

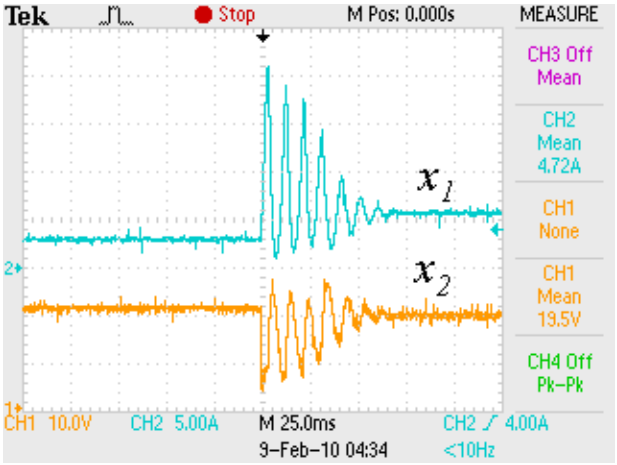


Figure 49: Buck-boost converter experimental waveforms showing load regulation.

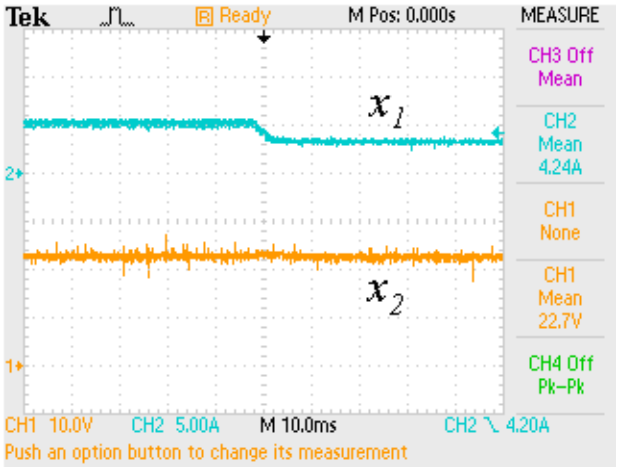


Figure 50: Buck-boost converter experimental waveforms showing line regulation.

Chapter 4: Single-Phase Full-Wave Uncontrolled Rectifiers with Instantaneous Constant-Power Loads

Here, stability properties of the system are studied and described in detail. In addition, a necessary condition for stable rectifier operation that depends on circuit parameters is derived. The study also investigates input and output characteristics of the rectifier with a CPL. In particular, the input power factor and the total harmonic distortion (THD) in the output voltage are compared with the resistive-load case. Furthermore, unlike the resistive case, the dynamical system of the rectifier with a CPL displays certain nonlinear phenomena that act as useful practical indicators of instability onset—period-doubling behavior is seen to occur before instability. Figure 51 shows a schematic of an ac source feeding a CPL through a single-phase full-wave rectifier.

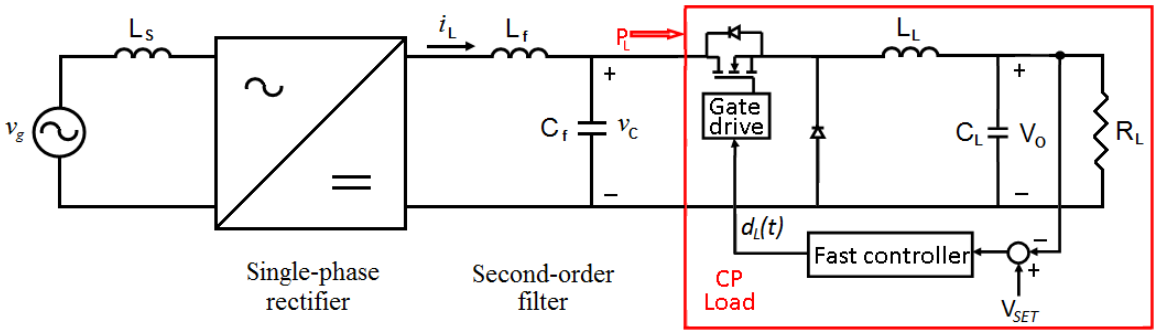


Figure 51: Schematic of a single-phase rectifier subject to a constant-power load.

RECTIFIER SYSTEM DYNAMICS WITH CONSTANT-POWER LOADS

In general, the concept of distributed generation implies that generation is usually in close proximity to its loads, this discussed case may correspond to a dc micro-grid with ideal ac sources and with a distributed power architecture such as the one discussed in Section I. Thus, for initial analysis purposes, an ac-source voltage, v_S, is feeding a rectifier as shown in Fig. 52, so any line inductance, L_S, is eliminated by now from

analysis. Ideal components are also assumed. Thus, based on Fig. 53 the dynamics of such ideal single-phase uncontrolled full-wave rectifier with an ideal CPL can be represented by the non-autonomous nonlinear system

$$f(i_L, v_C) = \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_f}\left(|v_S| - v_C\right) \\ \frac{1}{C_f}\left(i_L - \frac{P_L}{v_C}\right) \end{bmatrix} \tag{48}$$

$$i_L \geq 0, v_C > 0, \tag{49}$$

where $v_S = V_{in}\sin\omega t$, V_{in} is the peak supplied ac voltage, $\omega\,(=2\pi f)$ is the angular frequency of the ac supply voltage, P_L represents the magnitude of the constant power load, and C_f and L_f are the filter capacitance and inductance respectively, as shown in Figs. 51 and 53.

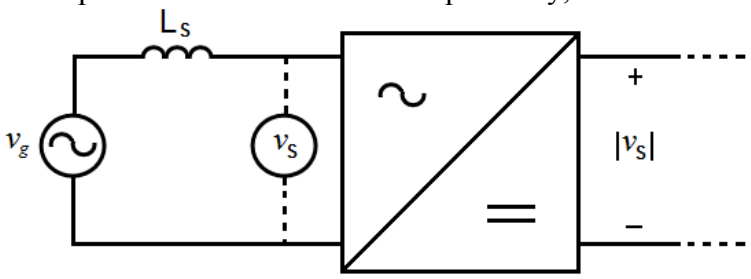


Figure 52: Schematic illustrating the approximation $L_S \approx 0$ used in first portion of the analysis.

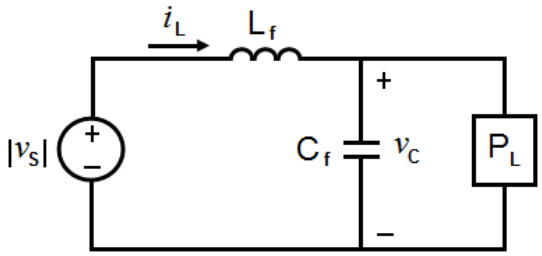


Figure 53: Simplified model of the rectifier system with a CPL.

Depending on the filter capacitor voltage, v_C, and the source voltage, v_S, a rectifier circuit switches between a first-order and a second-order system. That is, when v_C is greater than

v_S, no current flows through the inductor; then, the system effectively comprises only one state variable— the capacitor voltage [69]. On the contrary, when v_C is less than v_S, the inductor current flows, and the system must now be represented by two state-variables— the capacitor voltage and inductor current. However, unlike resistive loads, with CPLs rectifier instability may occur. This instability is due to the inverse term on v_C in (48). The second-order rectifier system shown in Fig. 53 may exhibit stable or unstable behaviors. Unstable behavior will be demonstrated by considering an equivalent constant input voltage $V_{S,o}$ equal to the magnitude of $|v_S|$ when $|v_S| = v_C$. Before this time, the filter capacitor merely discharges through the CPL. However, at the point when $|v_S| = v_C$— defined as the time $t = t_{S,o}$, the rectifier system becomes a second-order system until $t = t_1$, as shown in Fig. 54, so the singularity at $v_C = 0$ may be avoided. According to classic rectifier operation, after $t = t_1$ the system reverts back to a first-order system (the capacitor and the CPL as shown in Fig. 55) for the remainder of the period. At $t = t_{S,o}$ the initial inductor current is zero, and the initial capacitor voltage determines whether the system will operate in the stable or unstable region [50]. Here, the filter capacitor voltage at $t = t_{S,o}$ (and zero filter inductor current) is going to be considered the initial condition for the study. Once $V_{S,o}$ is used in (48) instead of $|v_S|$, the system described by (48) becomes an autonomous nonlinear system with dynamics represented by

$$f(i_L, v_C) = \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_f}(V_{S,o} - v_C) \\ \frac{1}{C_f}\left(i_L - \frac{P_L}{v_C}\right) \end{bmatrix}, \tag{50}$$

$$i_L \geq 0, v_C > 0\,. \tag{51}$$

This system has the same dynamic behavior as a buck converter in the ON-state. However, a subtle difference in the case of the rectifier is that unlike the buck converter that has a fixed input voltage with varying initial conditions, here the initial capacitor

voltage (and initial condition) is always $V_{S,o}$ [50]. As shown in Fig. 56, for high enough values of $V_{S,o}$ the system exhibits stable limit-cycle behavior. Yet, for voltages to the left of the separatrix, the trajectories tend to a low-voltage and high current condition, which is an undesirable outcome. From Fig. 56, we also deduce that higher values of $V_{S,o}$ yield smaller oscillations that are generally desirable with rectifier operation. Henceforth, we use the term "analogous-buck-converter operation" to describe the system described by equations (50) and (51)—the onset of the rectifier operating as a second-order system. Evidently, the similitude of (50) with a buck converter when the main switch is conducting is not arbitrary as the output interface of the rectifier is the same as that found in a buck converter. Hence, the equilibrium point (EP) of the system represented by (50) is $\begin{bmatrix} i_L & v_C \end{bmatrix}^T = \begin{bmatrix} P_L/V_{S,o} & V_{S,o} \end{bmatrix}^T$ [12] – [13]. A linearization about this EP shows that it is an unstable EP. Parameter changes can alter the properties of this unstable EP such that for certain ranges of circuit parameters, the EP is either an unstable node or an unstable focus. For certain parameter ranges, when the EP is an unstable focus, the restrictions put in place by (51) induce a stable limit cycle in the dynamics [50]. The analysis below illustrates these possible behaviors for the EP. The eigenvalues at the unstable equilibrium point are obtained by linearizing (50), and are given by

$$\lambda_1, \lambda_2 = \frac{P_L}{2C_f V_{S,o}^2} \pm \sqrt{\left(\frac{P_L}{2C_f V_{S,o}^2}\right)^2 - \frac{1}{L_f C_f}} \tag{52}$$

Locally, the EP is an unstable focus if

$$\frac{P_L}{V_{S,o}^2} < 2\sqrt{\frac{C_f}{L_f}}, \tag{53}$$

which is a necessary condition for the characteristic CPL (limit-cycle) oscillations that are shown in the stable region in Fig. 56 to occur. Figure 56 indicates that lower values of $V_{S,o}$ yield larger limit cycles and eventually drive the autonomous system represented by

(50) closer to instability. Two of the limit-cycles that represent stable operation are explicitly indicated in Fig. 56 ($V_{S,o}$ = 17.5V, and $V_{S,o}$ = 25 V). Since the condition in (53) is valid locally because it is derived from a linear analysis, the results are necessary but not sufficient. If the inequality given in (53) is not satisfied, then the EP becomes an unstable node and the rectifier output voltage essentially collapses. Thus, the EP's behavior changes with system parameters [50].

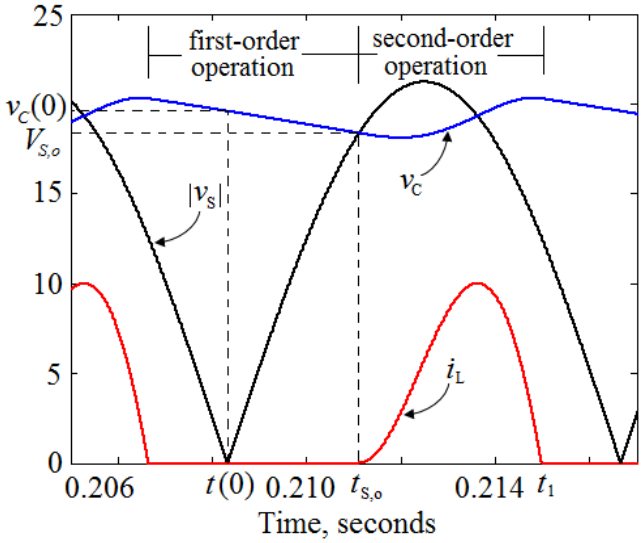


Figure 54: Simulation showing rectifier behavior (stable operation). Parameters: $v_C(0)$ = 15V, V_{in} = 15V, P_L = 50W, C = 6 mF, L = 500 μH.

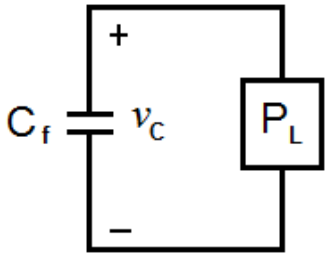


Figure 55: Circuit schematic during one-state operation.

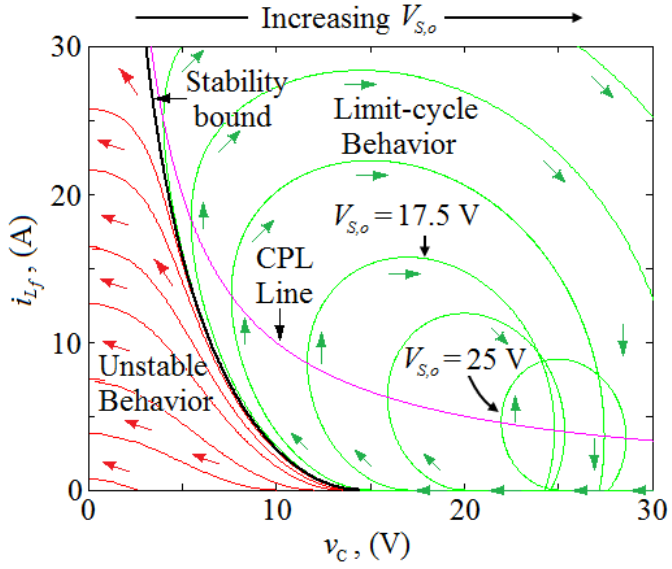


Figure 56: Phase portrait showing characteristic CPL oscillations in a rectifier with different values of $v_S = V_{S,o}$. Simulation parameters: P_L = 100W, C = 1000μF, L = 470 μH.

Necessary Condition for Stable Rectifier Operation

The operation of the system depicted in Fig. 54 assumes stable operation. This section provides an approximation for the minimum capacitor voltage that keeps the rectifier with a CPL in stable operation during analogous-buck-converter operation, as shown in Fig. 56. To avoid the singularity that occurs when the capacitor is discharged in the rectifier model given by (50), it is assumed that the initial condition of the system during analogous-buck-converter operation is $\begin{bmatrix} i_L & v_C \end{bmatrix}^T = \begin{bmatrix} 0 & V_{S,o} \end{bmatrix}^T$, where $V_{S,o} > 0$. Note that $V_{S,o}$ is determined by $v_C(0)$—the capacitor voltage at time $t(0)$ (see Figure 54)—and circuit parameters—including the magnitude of the CPL—that yields the capacitor's rate of discharge. From (53), we deduce that if the inequality is not satisfied for some $V_{S,o} < V_{in}$ (V_{in} is the highest possible value that $V_{S,o}$ can possibly attain), stable rectifier operation may not be achieved with that particular $V_{S,o}$. However, even if the inequality (53) is satisfied for some $V_{S,o} < V_{in}$, instability may still occur. In other words,

(53) presents only a necessary condition. Consider a rectifier system with a CPL operating from start-up with initial condition, $v_C(0)$. The rectifier system is initially a first-order system (see Fig. 55) and the dynamics of the capacitor voltage is described by

$$C_f \frac{dv_C}{dt} + \frac{P_L}{v_C} = 0. \tag{54}$$

If we solve for v_C, we obtain

$$v_C = \sqrt{v_C^2(0) - 2\frac{P_L}{C_f}t}, \quad v_C > 0, \tag{55}$$

which shows that v_C discharges during first-order operation. Equation (55) governs the trajectory of v_C until $t = t_{S,o}$ when $v_C = V_{S,o}$. At $t = t_{S,o}$, v_S and v_C are equal, so

$$V_{S,o} = V_{in}\left|\sin \omega t_{S,o}\right| = \sqrt{v_C^2(0) - 2\frac{P_L}{C_f}t_{S,o}}\,, \tag{56}$$

and $t_{S,o}$ satisfies the equation

$$\cos 2\omega t_{S,o} - \frac{4P_L}{C_f V_{in}^2}t_{S,o} + 2\left(\frac{v_C(0)}{V_{in}}\right)^2 - 1 = 0. \tag{57}$$

Obtaining a closed-form expression for $v_C(0)$ from equation (57) is difficult, due to the nonlinear (sinusoidal) term. Consequently, we choose to approximate the sine wave by a triangle so that $V_{S,o} \approx V_{S,o}^*$. This approximation is illustrated in Figure 57. We can deduce from equation (55) that a larger filter capacitance and a lower CPL will decrease the discharge rate, which in turn will provide a better approximation for $V_{S,o}$.

$$V_{S,o} \approx V_{S,o}^* = 4fV_{in}t_{S,o}, \qquad 0 \le t_{S,o} \le \frac{1}{4f}. \tag{58}$$

We then equate $V_{S,o}^*$ from equation (58), to $V_{S,o}$ and obtain

$$\left(4fV_{in}\right)^2 t_{S,o}^2 + \frac{2P_L}{C_f}t_{S,o} - v_C^2(0) = 0. \tag{59}$$

$t_{S,o}$ is then eliminated between equations (58) and (59).

$$V_{S,o}^{*} = \frac{1}{4fV_{in}}\left[-\frac{P_L}{C_f} \pm \sqrt{\left(\frac{P_L}{C_f}\right)^2 + \left(4fV_{in}v_C(0)\right)^2}\right]. \tag{60}$$

Hence, from inequality (53) CPL in order to observe sustained CPL oscillations,

$$\frac{1}{4fV_{in}}\left[-\frac{P_L}{C_f} \pm \sqrt{\left(\frac{P_L}{C_f}\right)^2 + \left(4fV_{in}v_C(0)\right)^2}\right] > \left(\frac{L_f P_L^2}{4C}\right)^{\frac{1}{4}}. \tag{61}$$

Note that since $V_{S,o} > V_{S,o}^{*}$, $V_{S,o}$ automatically satisfies inequality (53) whenever $V_{S,o}^{*}$ does. Ultimately, we arrive at

$$v_C(0) > \sqrt{\frac{1}{2fV_{in}}\left(\frac{L_f P_L^2}{4C_f}\right)^{\frac{1}{4}}\left[2fV_{in}\left(\frac{L_f P_L^2}{4C_f}\right)^{\frac{1}{4}} + \frac{P_L}{C_f}\right]}. \tag{62}$$

Equation (62) provides an approximation for the minimum initial filter capacitor voltage that must be exceeded in order to sustain CPL oscillations. Below this voltage, the rectifier EP may exhibit an unstable behavior. Figure 58 depicts stable rectifier operation with circuit parameters that satisfy (6). Figures 59 and 60 illustrate unstable rectifier operation. Note that the parameters used in simulating Fig. 59 satisfy (62), while in Fig. 60, P_L is increased so that the parameters used do not satisfy (62). The resulting instability in both cases serves to further illustrate that the condition stipulated by (62) is necessary, but not sufficient.

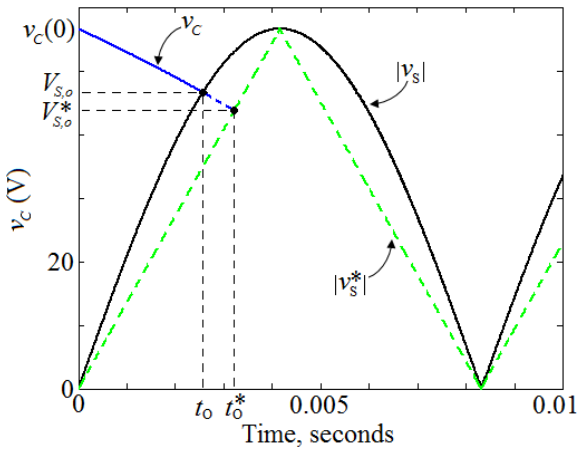


Figure 57: Simulation showing approximation used to determine the minimum initial filter capacitor voltage.

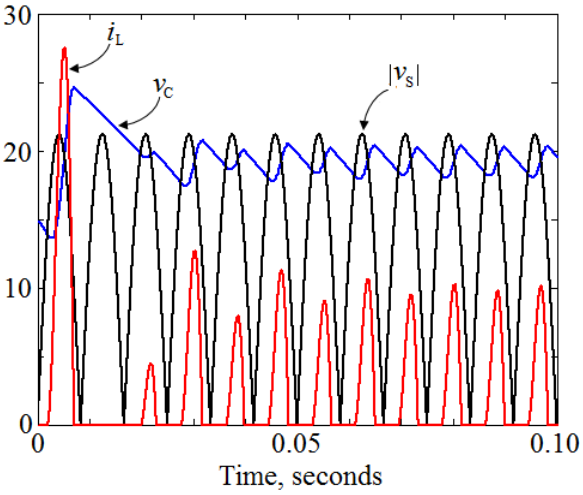


Figure 58: Simulation showing stable behavior with circuit parameters that satisfy inequality (6). Simulation parameters: $v_C(0)$ = 15V, V_{in} = 15V, P_L = 50W, C = 6 mF, L = 500 μH.

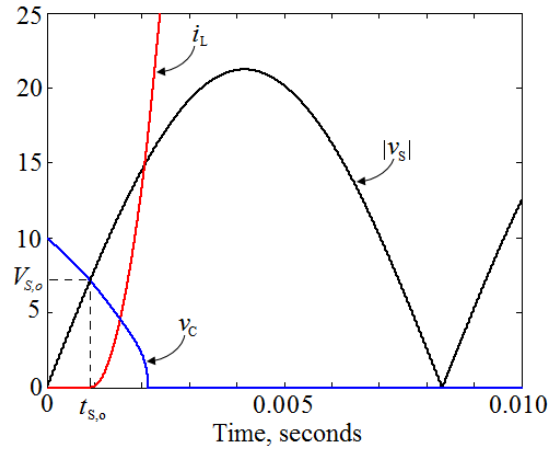


Figure 59: Simulation showing instability with parameters that satisfy inequality (53): $v_C(0) = 10\text{V}$, $V_S = 15\text{V}_{\text{rms}}$, $L = 500\ \mu\text{H}$, $C = 6$ mF, $P_L = 80\text{W}$.

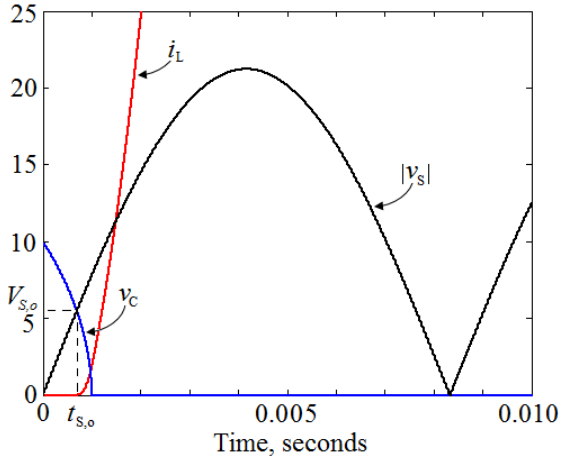


Figure 60: Simulation showing instability with parameters that do not satisfy inequality (53): $v_C(0) = 10\text{V}$, $V_S = 15\text{V}_{\text{rms}}$, $L = 500\ \mu\text{H}$: $C = 6$ mF, $P_L = 80\text{W}$: $C = 3$ mF, $P_L = 150\text{W}$.

Practical Considerations

In practical rectifier circuits, under no-load operation, the filter capacitor, C_f, is being charged by v_S. Hence, $0 \le v_C(0) \le V_{in}$. That is, without the CPL, the capacitor is charged almost instantaneously to V_{in}; when the CPL can then be connected to the rectifier and v_C discharges according to (55). If the circuit parameters are chosen correctly

to ensure stable (limit-cycle) operation according to (62), then the following inequality is derived by replacing $v_C(0)$ with V_{in} in (62).

$$\left(\frac{L_f P_L^2}{4C_f}\right)^{\frac{1}{4}} V_{in} + \frac{P_L}{2fC_f} < \left(\frac{4C_f}{L_f P_L^2}\right)^{\frac{1}{4}} V_{in}^3 . \tag{63}$$

For a given filter inductance, L_f, and a filter capacitance, C_f, (63) is satisfied for lower values of P_L. As P_L is increased the equilibrium point of the system tends to be unstable. This is seen clearly if we assume L_f and C_f are of the same order of magnitude. For example, if $L_f = C_f$, we have

$$\frac{P_L}{2} V_{in} + \frac{1}{fC_f}\left(\frac{P_L}{2}\right)^{\frac{3}{2}} < V_{in}^3 . \tag{64}$$

Close examination of (64) reveals that stable operation is facilitated by lower values of CPL, a higher rectifier (ac) input voltage, higher supply frequency and larger filter capacitances, which is in agreement with (53). Examination of (63) also indicates that lower values of L_f facilitate stable rectifier operation. The supply frequency and input voltage are usually fixed, so for a given CPL, only proper filter capacitance design choices can be used to ensure stable rectifier operation. In addition, larger filter capacitances yield, like in the resistive case, lower output voltages ripple.

INPUT AND OUTPUT CHARACTERISTICS

Some initial insights have been obtained from the system in Fig. 3. The next step addressed in this section is to derive a more complete mathematical model of the rectifier system with a CPL. This expanded model mirrors the setup used in the experimental verification and considers a non-zero input inductance L_S. Thanks to this addition, it accounts for line-voltage distortion and, as such, is a more practical model. The dynamical equations of the more complete model are simulated using MATLAB/Simulink. The rectifier system is also shown to undergo a period-doubling

bifurcation when it approaches its stability limit. Furthermore, the input and output characteristics of the rectifier with a CPL are experimentally compared with the resistive case.

Derivation of Model

A more practical setup of the rectifier with a CPL is depicted in Fig. 61.a. The model now includes an input inductance L_S, i.e.,

$$v_S = nv_g - L_S \frac{di_S}{dt}. \tag{65}$$

Since the instantaneous input power for the rectifier is constant, the system shown in Fig. 61.a has the following property: $v_g i_S \geq 0$ and constant. As illustrated in Fig. 61.b, during both half cycles, the same voltage v_S appears across the load. That is, both half cycles have the same effect on the circuit's operation. Hence, for analysis purposes, we can define an equivalent circuit that generates $|v_S|$ after the rectifier stage. The result is an equivalent circuit shown on the right of Fig. 61.b. Mathematically,

$$|v_S| \doteq n|v_g| - L_S \frac{d|i_S|}{dt} = n|v_g| - L_S \frac{di_L}{dt}, \tag{66}$$

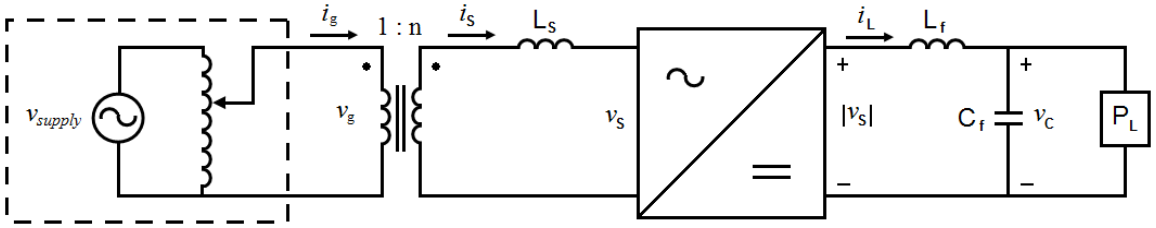
This equation allows us to further simplify the circuit shown in Fig. 61.b to that depicted in Fig. 61.c, so that L_S also "sees" current i_L and the circuit is fed by $n|v_g|$. Substituting (66) in (48) the dynamical equations of the complete model shown in Fig. 12c can then be written as

$$f(i_L, v_C) = \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_S + L_f}\left(n|v_g| - v_C\right) \\ \frac{1}{C_f}\left(i_L - \frac{P_L}{v_C}\right) \end{bmatrix}, \tag{67}$$

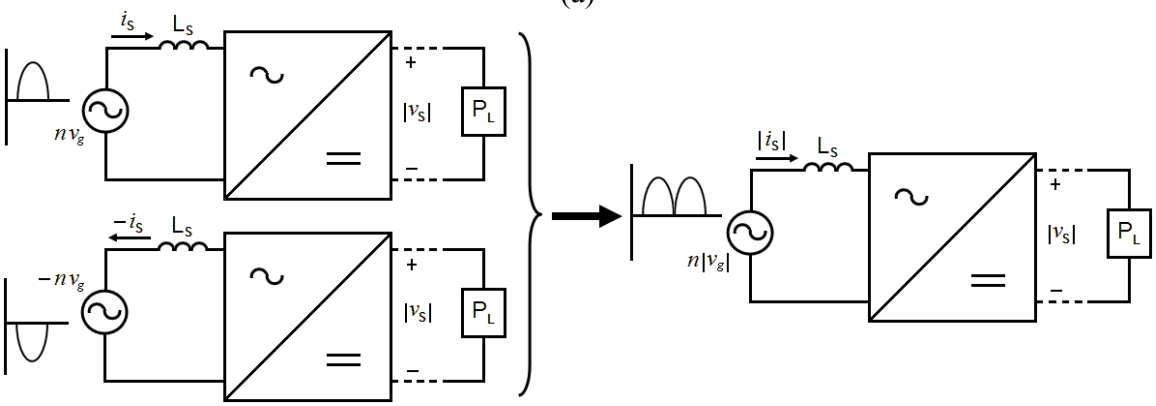
$$i_L \geq 0, v_C > 0, \tag{68}$$

where L_S represents the lumped transformer series inductance of the isolation transformer referred to the low-voltage side as shown in Fig. 61.a; L_S may also include the winding

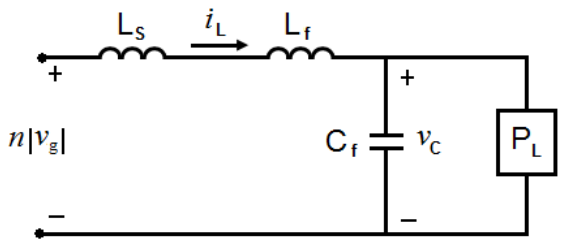
inductance of a generator, and the line. In the model from Fig. 61.a, v_g is the voltage at the secondary terminal of the variac. A low distortion variac—POWERSTAT L2M116C—was used in the experiments. Hence, we assume that v_g is our ideal ac source voltage. In the event that an ac generator such as a microturbine is deployed, its equivalent single-phase series impedance can be referred accordingly and lumped together with the reactance due to L_S. The model described by (67) and (68) was also simulated in MATLAB/Simulink. The same parameters were used in both simulations and experiments. It is noteworthy to mention that L_S can be obtained by performing a simple short circuit test on the isolation transformer shown in Fig. 61.a, and noting that the reactance, $2\pi f L_S$, accounts for most of the series impedance.



(a)



(b)



(c)

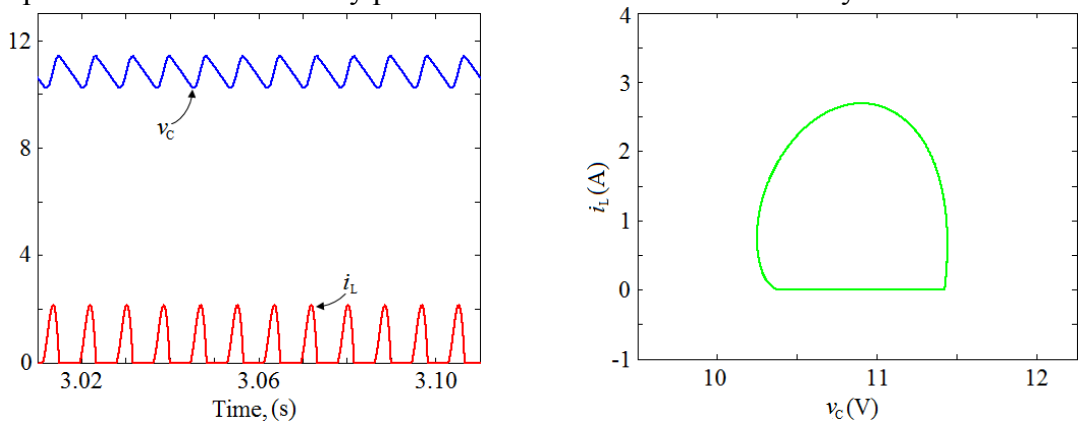
Figure 61: (a) Schematic of more complete model and experimental setup. (b) Justification of equivalent model. (c) Equivalent model for analysis.

Nonlinear Phenomena

Steady-state operation is usually characterized by stable-limit-cycle operation, but it is observed that when parameter values are changed to drive the system closer to instability—according to (53) — the system exhibits a bifurcation phenomena, and the period of the limit cycle may double. This behavior exhibited by the rectifier with a CPL is called, in a general case, period-doubling bifurcation [61] [70]. It is observed that this period-doubling occurs closer to the stability limits defined by (53). Here, periodic oscillations that characterize conventional rectifier steady-state limit-cycle operation is termed "period-1 behavior." "Period-2 behavior" refers to period-doubling of the limit cycle which is observed—due to the nonlinearity present—when the parameters of the rectifier system with a CPL are changed. In section II, an estimate of the stability limit was derived by considering an equivalent constant input voltage at the onset of second-order operation, and subsequently applying small signal techniques. Hence, instability may still occur if inequality (53) is satisfied—as mentioned in section II, inequality (53) presents only a necessary condition. An example of such instability was depicted in Fig. 59, in which circuit parameters satisfy (53). For practical purposes, the bifurcation parameter could be the CPL, P_L, so that, period-doubling oscillations can also serve as an indicator that the system may be approaching instability as load levels are increased.

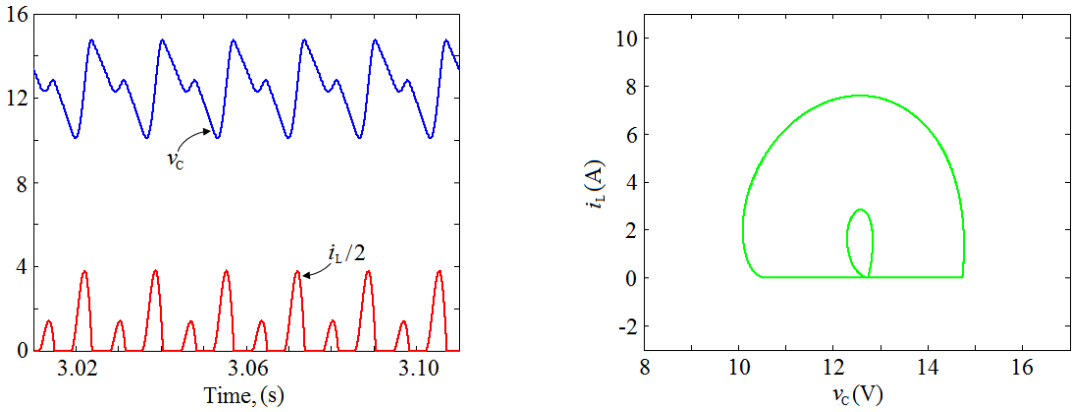
Alternatively, the existence of this bifurcation may be used for parameter selection to ensure limit-cycle operation, which provides a condition more suitable to be controlled than the alternative behavior of voltage collapse.

Simulations and experiments provide the necessary verification. The more complete model of Fig. 61.a was also simulated using the equivalent analytical model shown in Fig. 61.c. Figure 62 shows period-1 behavior when P_L is 7.6W. However, when P_L is increased to 20W, the system bifurcates and the period of oscillation doubles, as depicted in Fig. 63. The same parameters used in simulating the model (Fig. 61.c) were used in an experimental setup. The results from experiment closely match, and thus, verify the behavior observed by simulation Figs. 64 and 65 show waveforms obtained experimentally. Figure 64 shows period-1 behavior ($P_L \approx$ 7.6W). When the system is pushed closer to its stability limit by increasing P_L to about 20W (see (6)), period-2 behavior is observed. This is shown in Fig. 65. These results also show that the more complete model can accurately predict the behavior of the rectifier system with a CPL.



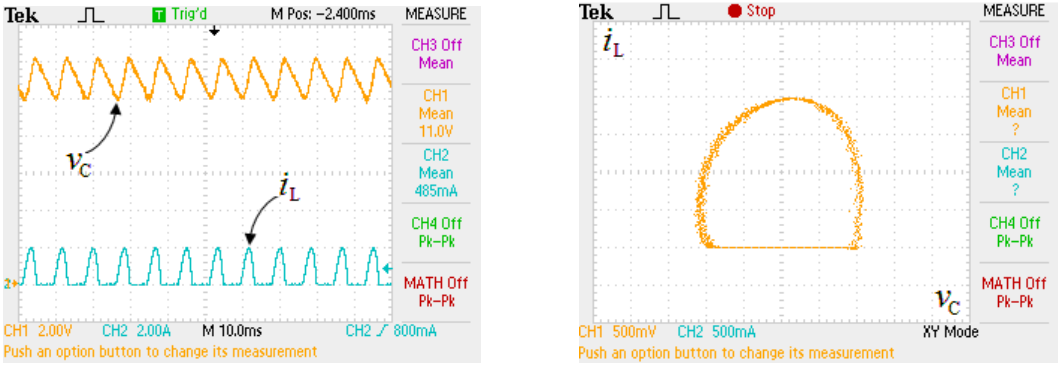
(a) (b)

Figure 62: Simulated plots (more complete model) showing period-1 behavior. Parameters: V_G = 46V_{rms}, n = 25/115, C_f = 3 mF, L_S = 574 μH, L_f = 480 μH, P_L = 7.6W. (a) time plot, (b) phase-portrait.



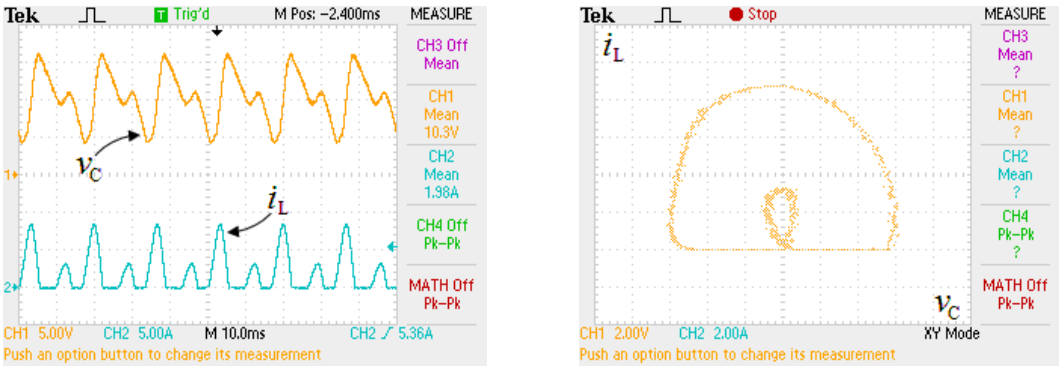
(a) (b)

Figure 63: Simulated plots (more complete model) showing period-2 behavior. Parameters: $V_G = 46V_{rms}$, n = 25/115, $C_f = 3$ mF, $L_S = 574$ μH, $L_f = 480$ μH, $P_L = 20$W. (a) time plot, (b) phase-portrait.



(a) (b)

Figure 64: Experimental waveforms showing period-1 limit-cycle behavior. Parameters: $V_G = 46V_{rms,}$, $v_C(0) = V_{Speak}$, $P_L \approx 7.6$W, $C_f = 3$ mF, $L_f = 480$ μH. (a) time plot, (b) experimentally-generated phase-portrait.



(a) (b)

Figure 65: Experimental plots showing period-2 limit cycle behavior. Parameters: V_G = 46V_{rms}, $v_C(0) = V_{Speak}$, $P_L \approx 20$W, $C_f = 3$ mF, $L_f = 470$ μH. (a) time plot, (b) experimentally-generated phase-portrait.

Output Voltage Ripple, Input Power Factor, and Output Voltage THD

We estimate the output voltage ripple by considering the discharge interval of a fully charged capacitor. It is assumed that the capacitor is discharged from V_{in} over one period of $|v_g|$ that lasts $1/2f$ [28]. This last approximation typically yields an over estimate because the capacitor does not discharge over a full half-period of the supply frequency. In addition, the approximation considers that the capacitor discharges from V_{in}. Depending on whether the actual peak capacitor voltage is greater (or less) than V_{in}, the ripple estimate may underestimate (or overestimate) the actual ripple content of the output voltage. According to (48) and (67), with lower values of C_f, v_C evolves faster; hence, peak capacitor voltages may tend be higher than V_{in}. This behavior is also observed with resistive loads [69]. Hence, the assumption that considers the peak capacitor voltage to be V_{in} is analogous to traditional assumptions used to estimate an approximate output voltage ripple in rectifiers with resistive loads [28]. Figure 66 depicts simulation results that illustrate period-1 and period-2 operation of the rectifier circuit in steady state, and shows that the ripple during period-2 behavior cannot be estimated over

a single discharge interval (1/2*f*). For this reason, we limit the validity of the ripple approximation derived here to period-1 operation. Using (55) to obtain the expression for v_C at $t = 1/2f$, we derive the approximate output ripple voltage as

$$\Delta v_C \approx V_{in} - \sqrt{V_{in}^2 - \frac{P_L}{C_f f}}. \tag{69}$$

Note that equation (69) is valid whether or not L_S is considered, because the derivation is done assuming first-order operation (see Figure 54 and Figure 55)

We now propose that the ripple content in the output voltage of a single-phase uncontrolled rectifier is greater when the circuit is loaded with a CPL than when it has a resistive load of an equivalent power level. This statement can be proved with the following reasoning: for estimating ripple consider that that in both resistive and CPL cases, the capacitor voltage discharges from some peak capacitor voltage, $V_{C,peak}$, over half a period, 1/2*f*, of the supply frequency, *f*. Now, from [38] the approximation for output voltage ripple for resistive loads is

$$\Delta v_{C,R} \approx \frac{V_{C,peak}}{2R_L C_f f}, \tag{70}$$

where $\Delta v_{C,R}$ is the output voltage ripple for the resistive case, and R_L is the resistive load. The output voltage ripple for the CPL case will be represented by $\Delta v_{C,CPL}$. It is assumed that the parameter ranges considered do not yield large ripples in the output voltage, so that the mean output voltage, $V_{Cmean} \approx V_{C,peak}$. Next, assume the contrary to the aforementioned statement. That is, $\Delta v_{C,CPL} < \Delta v_{C,R}$. Using equations (69) and (70), we have

$$V_{C,peak}^2 - \frac{P_L}{C_f f} > V_{C,peak}^2 \left(1 - \frac{1}{2R_L C_f f}\right)^2. \tag{71}$$

From the statement of the proposition,

$$P_L = \frac{V_{mean}^2}{R_L} \approx \frac{V_{C,peak}^2}{R_L}. \tag{72}$$

Using equation (71) in equation (72) yields.

$$\frac{1}{\left(2R_L C_f f\right)^2} < 0, \tag{73}$$

which is a contradiction, and proves that $\Delta v_{C,CPL} > \Delta v_{C,R}$.

As previously mentioned, depending on circuit parameters, period-2 behavior may occur. In general, the results obtained in this sub-section are valid for parameters that yield period-1 behavior. As noted in the preceding subsection, period-2 behavior renders the ripple-approximation given by (69) invalid, because the underlying assumptions considered to derive (69) do not apply. Figures 67.a and 67.b show experimental plots that verify (69). Theoretical approximation using the same aforementioned circuit parameters yields an output voltage ripple, Δv_C = 2.49V; while the experimental ripple, Δv_C = 2.00V ($P_L \approx$ 28.8W). Figure 67.b shows waveforms for an increased power level. Our approximation predicts an output voltage ripple, Δv_C = 10.24V; while the experimental ripple, Δv_C = 6.80V ($P_L \approx$ 96.8W). As expected, experiment shows that (22) is an overestimate and ripple increases as the power level increases. Figures 68.a and 68.b are simulated waveforms that show a close match with the experimental plots in Fig. 67. In particular, the ripple estimates from the model are Δv_C = 1.80 ($P_L \approx$ 28.8W), and Δv_C = 5.11 ($P_L \approx$ 96.8W), which are closer to the experimental values than the theoretical estimate. Note that there is some discrepancy between the ripple content in the output voltage obtained from simulation and the actual (experimental) ripple content, because the model assumes ideal components—parasitics are omitted from the mathematical model.

As expected, in both simulation and experiment (see Figs. 67, 68, and 69) v_g is undistorted, while v_S contains some distortion. In addition, both in simulation and experiment, v_S appears more distorted at increased power levels. Next, experiments are used to compare the input and output characteristics of a rectifier system with a CPL and a resistive load, at the same power levels. The results are displayed in Table I and illustrated graphically in Fig. 70. Figure 70 reveals that the input power factor and average output voltage for CPLs and resistive loads have similar values at the same power level. However, the rectifier output voltage THD_{dc}—as defined in (27) based on modifying the conventional definition of THD in order to make it suitable for evaluating harmonic content in a rectifier output—in the CPL case is higher than the THD_{dc} in the resistive case. The proposition made above shows that this observation may be expected; essentially, the higher output voltage ripple content with a CPL (as opposed to a resistive load at an equivalent power level) translates into higher output voltage THD_{dc}. The effect of this increased THD_{dc} may be more stringent line regulation requirements for the POL converter in Fig. 1. In both cases, however, the mean output voltage has similar values. In addition, the mean output voltage decreases as the load power is increased. Essentially, under stable operation, CPLs have similar effects on the input characteristics than resistive loads, but output distortion may vary. As mentioned, distortion is measured here based on a factor called THD_{dc} defined as follows:

$$THD_{dc} \doteq \sqrt{\frac{v_{rms}^2 - v_{dc}^2}{v_{dc}^2}} \tag{74}$$

Equation (74) defines the square of the total harmonic distortion in the output voltage, $(THD_{dc})^2$, as the fraction of unwanted harmonics present in the dc output voltage.

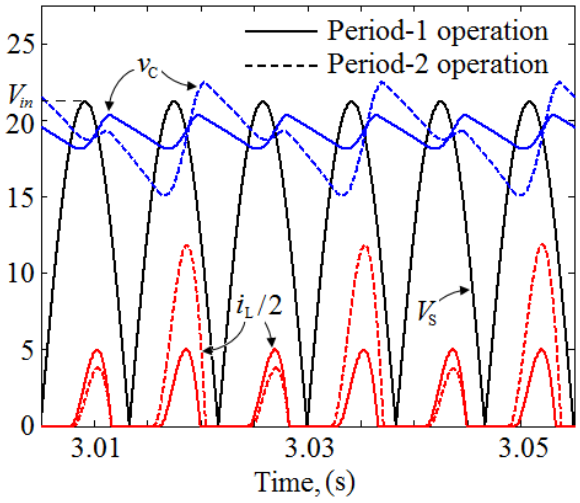
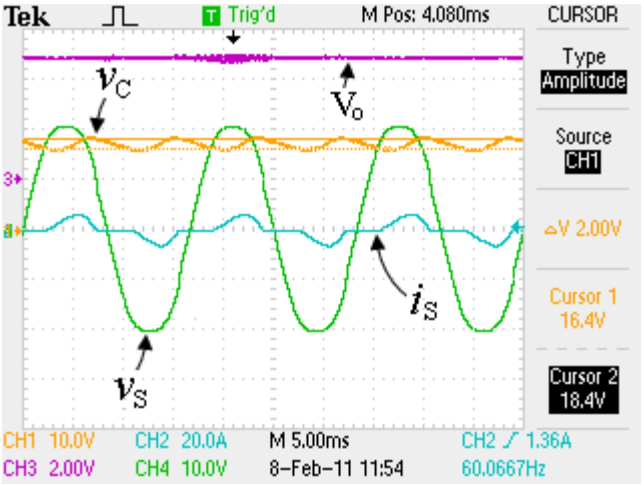


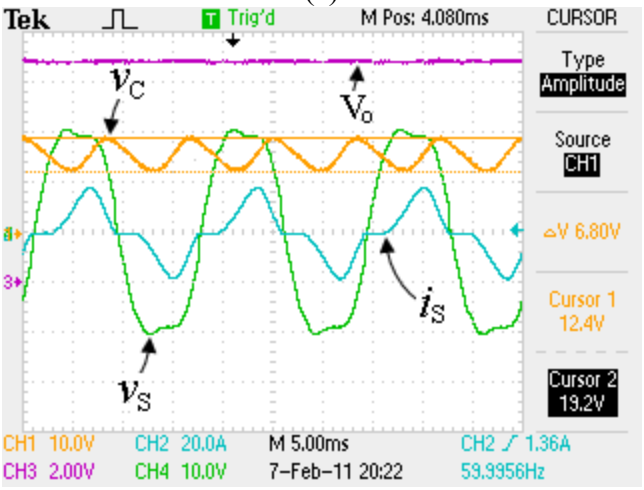
Figure 66: Simulated waveforms showing period-1 operation and period-2 (period doubling) operation. Parameters: $V_S = 15V_{rms}$, $C_f = 6$ mF, $L_f = 480$ μH. $P_L = 50$W (Period-1), $P_L = 90$W (period-2).

Output Power (W)	Input p.f.		Output voltage THD (%)		Mean output voltage (V)	
	CPL	Resistive load	CPL	Resistive load	CPL	Resistive load
27.25	0.8080	0.8011	7.71	2.65	19.45	19.68
40.93	0.8250	0.8237	9.89	4.16	18.43	18.61
50.53	0.8317	0.8320	11.15	5.32	17.79	17.95
63.20	0.8335	0.8406	13.41	7.01	16.94	17.10
66.22	0.8382	0.8419	14.84	7.41	16.46	16.91
76.06	0.8388	0.8465	15.70	8.90	16.10	16.28
84.02	0.8385	0.8504	17.11	10.22	15.72	15.78
91.97	0.8391	0.8539	19.00	11.57	15.27	15.31
101.28	0.8476	0.8583	20.65	13.31	14.96	14.77
111.76	0.8521	0.8641	22.99	15.39	14.01	14.18
118.43	0.8667	0.8672	23.86	16.77	13.04	13.81

Table 1: Input and output characteristics: comparison between resistive and CPLs.

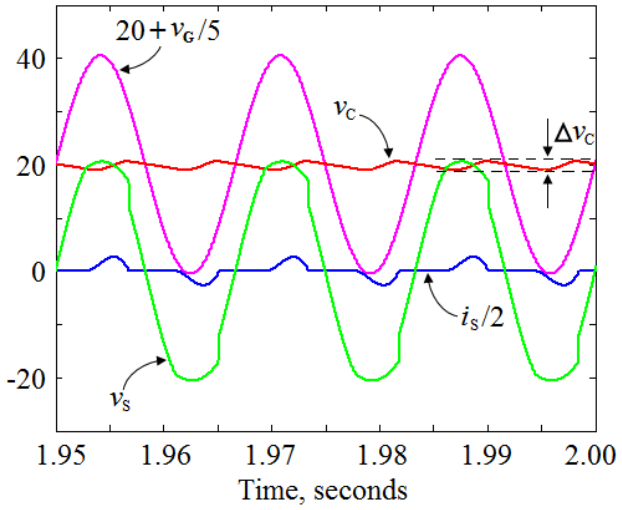


(a)

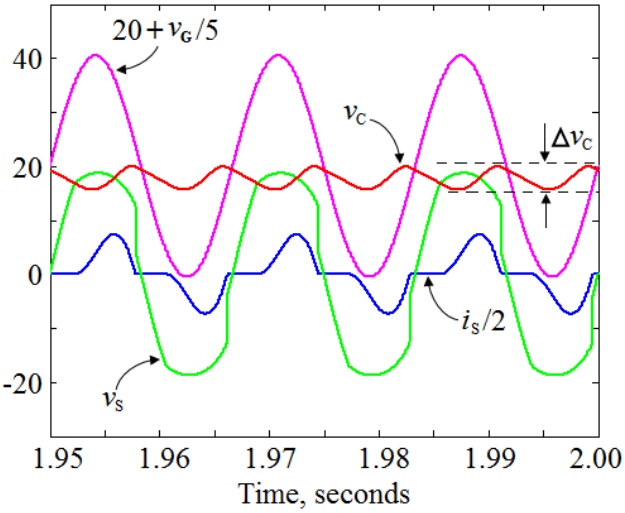


(b)

Figure 67: Experimental waveforms verifying ripple approximation. Parameters: V_G = 70V_{rms}, n = 25/115, C_f = 4.5 mF, L_S = 574 μH, L_f = 480 μH. (a) $P_L \approx$ 28.8W. (b) Increased output voltage ripple for a higher CPL, $P_L \approx$ 96.8W.



(a)



(b)

Figure 68: Simulated waveforms showing accurate ripple estimation. Parameters: V_G = 70V_{rms}, n = 25/115, C_f = 4.5 mF, L_f = 480 μH. (a) $P_L \approx$ 28.8W. (b) $P_L \approx$ 96.8W.

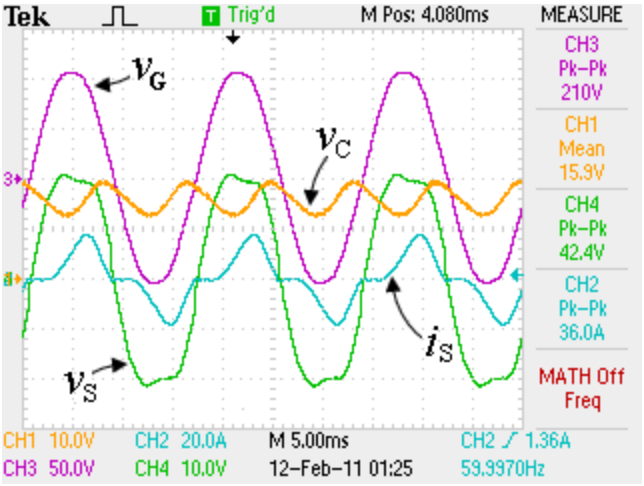


Figure 69: Experimental waveforms showing distortion. Parameters: V_G = 70V$_{rms}$, n = 25/115, $P_L \approx$ 96.8W, C_f = 4.5 mF, L_f = 480 μH.

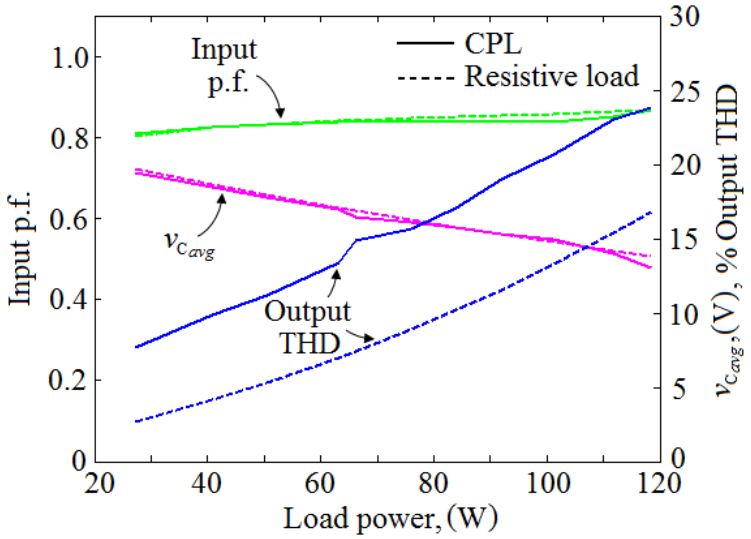


Figure 70: Plots from experiments comparing input power factor, *p.f.*, mean output voltage, v_{Cavg}, and output voltage THD, between resistive and CPLs. Parameters: V_{supply} = 120V$_{rms}$, n = 25/115, C_f = 4.5 mF, L_f = 480 μH.

Chapter 5: Conclusion

This dissertation has discussed operation of power electronic interfaces in dc systems under instantaneous constant-power loads, with focus on boundary control of dc-dc converters. Boundary control is used to overcome the destabilizing effects introduced by constant-power loads and to drive two-state dc-dc converter systems to desired operating point. The dynamics of the nonlinear system in open-loop is characterized by either an oscillatory limit cycle or an equilibrium state in which the output voltage is almost zero.

The study starts with analyzing buck converters with instantaneous CPLs, and subsequently extends the analysis of boundary control of dc-dc converters with CPL from the buck case [50] into the more challenging non-minimum phase converters. Operation modes related with switching surfaces in the proposed system are described and the region that guarantees asymptotic stability of the closed-loop system is derived. Furthermore, sufficient conditions for large-signal stability are established. For the non-minimum-phase (boost and buck-boost) converters, Filippov's method is employed in order to define solutions on the switching surface in reflective-mode operation. The analysis then uses Lyapunov's direct method to identify stable and unstable reflective regions. Despite the significant differences in dynamic behaviour between buck converters and both boost and buck-boost topologies, it is shown that the same boundary controller that achieves stable operation in buck converters—i.e., a linear boundary with a negative slope—can also successfully eliminate large oscillations caused by the non-linear nature of CPLs for boost and buck-boost circuits. Boundary control also has added advantages when compared with other stabilising controls, in particular PID controllers [25] [27]. These advantages include a more robust operation, avoidance of noise

susceptibility due to differential controllers, and faster performance. Simulated and experimental results validate the analysis. These results also include verification of load and line regulation.

Thanks to the inherently robust nature of boundary controllers, the control objective is achieved in theory and practice despite the presence of unknown and stray parameters that are omitted in the model. Design considerations infer that depending on the application, a separate start-up circuit may not be necessary for buck and boost converters, and that the loop can be closed once limit-cycle behavior is encountered. Furthermore, starting the closed-loop system at $x_0 = \gamma$ ensures that the initial condition is inside the stability region of γ. In this application, a hysteresis band serves two functions: one is to prevent chattering and the other is to prevent the closed-loop system from stalling. The experimental results show a very good match between the theoretical analysis and the empirical verification. They also show that operating the closed-loop system with $x_0 = \gamma$ yields practically no overshoot in the buck-converter case, and in general, negative slopes should be chosen for the first-order boundary. In addition, shorter transients are obtained by this technique. Line and load regulation has also been achieved.

Diversity of supply may lead to inclusion of ac sources in dc microgrids. Hence, a single-phase uncontrolled rectifier that is subject to instantaneous constant-power loads has also been investigated. This study pointed out important effects that CPLs have on the rectifier system. In particular, unlike the resistive case, instability, which depends on circuit parameters, may occur. A necessary condition for stable rectifier operation with a CPL has been derived. A more complete mathematical model was introduced. The model accounts for the distortion observed in the ac voltage just before the rectifier. Furthermore, comparisons were made between input and output characteristics for CPLs

and resistive loads; respective similarities and differences were pointed out. Particularly, it was seen that input power factor and output voltage distortion were similar for both the CPL and resistive load cases. However, the distortion present in the output voltage was seen to be greater for the CPL case than for the resistive load case. This disparity is expected, because when compared to a resistive load at an equivalent power level, the output voltage of a rectifier with a CPL has greater ripple content. Important nonlinear behavior was also observed. As the CPL is increased, a period-doubling bifurcation is seen to occur. The limit-cycle with a doubled period, or "period-2 behavior", occurs before instability and as such, can serve as a practical indicator that the system is approaching its stability limit.

Throughout this dissertation, simulations and experiments have been provided to elucidate the concepts presented, and to verify predictions from analysis.

FUTURE WORK

State-dependent switching has been applied to stabilize the basic dc-dc converter topologies. The future of power conversion will see more complex topologies being deployed in distributed power architectures. In particular, multiple-input-converter (MIC) topologies are already receiving a lot of attention from the research community [12] – [13], [71] – [83]. Many of these MIC topologies comprise more than two storage elements; hence, classic tools such as the phase plane that is used for boundary control cannot be used. Other state-dependent switching techniques for MICs may have to be developed. A more general characterization of dc-dc converter topologies with CPLs, perhaps as a class of nonlinear systems, may be another area for research; this characterization may lead to the development of equally robust controllers for CPLs. Finally, the more common case of three-phase rectifiers feeding CPLs should be studied.

Appendix

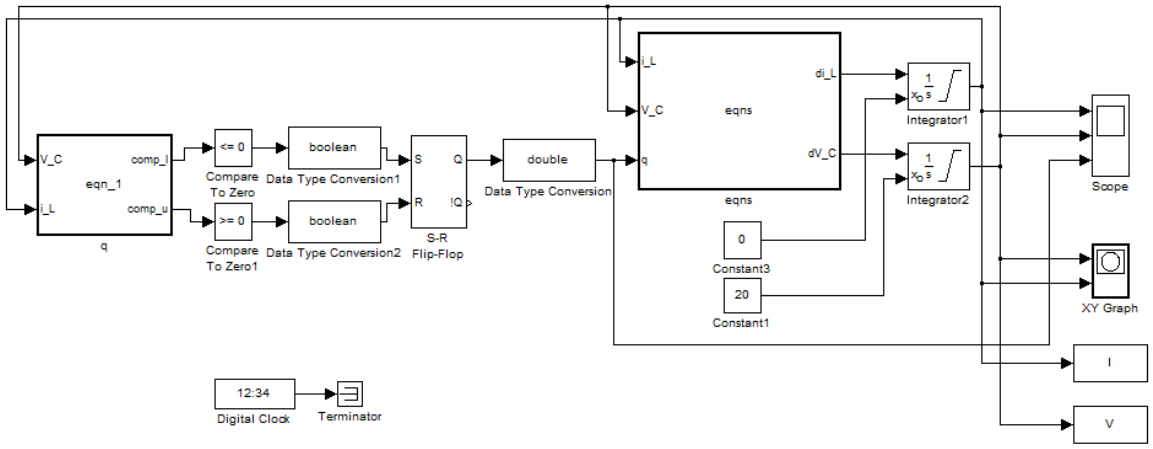


Figure 71: Boundary control implementation for buck, boost and buck-boost converters in MATLAB/Simulink.

eqns

%Insert parameters: L = 480e-6; C = 480e-6; P = 68.2; E = 17.5;

%buck converter equations
di_L = 1/L*(q*E – V_C);
dV_C = 1/C*(i_L – P/V_C);

%boost converter equations
di_L = 1/L*(E – (1-q)*V_C);
dV_C = 1/C*((1-q)*i_L – P/V_C);

%buck-boost converter equations
di_L = 1/L*(q*E – (1-q)*V_C);
dV_C = 1/C*((1-q)*i_L – P/V_C);

eqn_1

y = i_L; x = V_C; y_op = 5.5; x_op = 12.4;
m = 2.2; *%boundary slope = –m; selected accordingly*
comp_u = y – y_op + m*(x – x_op) + 0.025;
comp_l = y – y_op + m*(x – x_op) – 0.025;

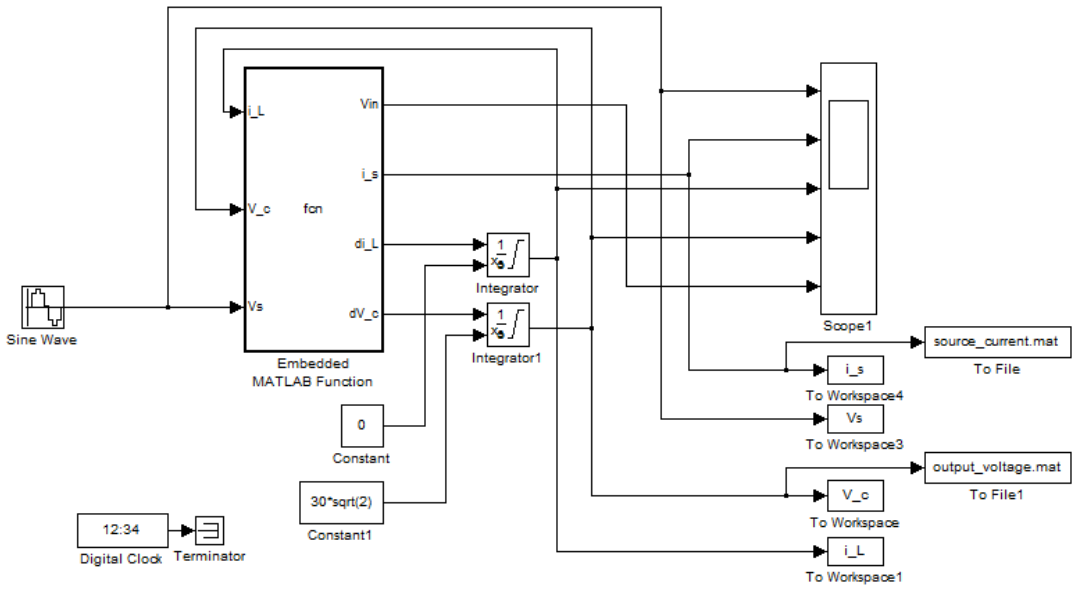


Figure 72: Boundary control implementation for single-phase full-wave uncontrolled rectifier in MATLAB/Simulink.

fcn

% Insert parameters: L = .5e-3; C = 2.5e-3; P = 100; R = 100;

```
Vin = 0;
if Vs < 0
      Vin = -Vs;
else
      Vin = Vs;
end

% dynamics
di_L = 1/L*(Vin - V_c);
dV_c = 1/C*(i_L - P/V_c);

i_s = i_L;
if Vs < 0
      i_s = -i_L;
elseif Vs >= 0
      i_s = i_L;
else
end
```

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