Copyright

by

Tanvi Dhananjay Joshi

2011

The Thesis Committee for Tanvi Dhananjay Joshi
Certifies that this is the approved version of the following thesis:

Device Modeling and Circuit Design for ZTO based Amorphous Metal Oxide TFTs

APPROVED BY
SUPERVISING COMMITTEE:

Supervisor:

Ananth Dodabalapur, Supervisor

T R Viswanathan, Co-Supervisor

Device Modeling and Circuit Design for ZTO based Amorphous Metal Oxide TFTs

by

Tanvi Dhananjay Joshi, BE

Thesis

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

The University of Texas at Austin

May 2011

Dedication

To my family and friends

Acknowledgements

I wish to thank my advisor Dr. Ananth Dodabalapur for his support and guidance throughout the course of this work. His vision enabled this project and his encouragement helped in keeping up the pace of this research work. I would also like to thank my co-advisor Dr. T R Viswanathan for his constant support and advice both within and outside the scope of this thesis project. His invaluable inputs elevated the level of research involved in this thesis.

I would also like to thank my research group members and fellow students Dr. Brian Cobb, Chen Guan Lee and Kiran Divakar for their support and advice throughout this work. This thesis is a result of close co-operation and dynamic exchange of ideas within this research group. I convey my sincere regards to Dr. T L Viswanathan for her guidance on circuit simulations. My specials thanks to Christopher Lombardo and Davianne Duarte for helping me get used to the new work environment and supporting me otherwise.

Lastly I would like to thank my parents and my friends for being there for me when I most needed them and for their motivation, which has got me this far.

Abstract

Device Modeling and Circuit Design for ZTO based Amorphous Metal Oxide TFTs

Tanvi Dhananjay Joshi, M.S.E.

The University of Texas at Austin, 2011

Supervisor: Ananth Dodabalapur
Co-Supervisor: T R Viswanathan

Amorphous Oxide semiconductors have gained large interest in the display industry owing to their high carrier mobilities and low fabrication costs. In this thesis, n-channel solution based zinc-tin oxide (ZTO) thin-film transistors (TFTs) are studied from a circuit design perspective. The study includes an iterative process of circuit design, layout and test procedure of the fabricated devices in the lab. The device models used in circuit simulations are refined following the data fed back from each of these iterations which has enabled more accurate design of complex circuits using ZTO devices. The requirement and development of a physical compact model for performing accurate and predictive circuit simulations has been presented. The use of ZTO devices in low cost, transparent and flexible electronic applications has been investigated through the study of basic circuit blocks such as amplifiers, ring oscillators, inverters and a four stage Operational Amplifier.

Table of Contents

List of Tables

List of Figures

CHAPTER 1
Introduction

The LCD screens using amorphous Silicon (a-Si) Thin Film Transistor (TFT) were introduced in mid 1990's. With commercial success of these display arrays, study and development of various materials useful as semiconductor in TFTs has caught a lot of attention in recent times. Currently the most useful application areas for these devices are large display arrays, sensor arrays, RFID tags and other disposable electronics.

This thesis discusses the device modeling of Zinc Tin Oxide (ZTO) based TFTs and explores its use in circuit design. As a part of this study, a total of four masks containing circuits built using ZTO devices and various test structures were laid-out. Fabrication of circuits using these masks was done at the Micro-Electronics Research (MER) facility in The University of Texas at Austin. Starting with the Level 1 SPICE approximation of the device model, the need to devise a new physical compact model for the ZTO TFTs was closely investigated through several revisions. The sufficiently accurate fit obtained by modifying an available a-Si model was used for circuit simulations and its validity was verified through lab tests. Also, ZTO based TFTs were explored to understand their performance in circuit applications such as ring oscillators, logic gates and high-gain amplifiers.

1.1 INTERESTS BEYOND SILICON

The use of electronics has now touched upon every aspect of life. With rapid advancements in multidisciplinary fields like bioelectronics, chemotronics and electromechanics, there is a pressing need for investigation of materials which can produce low-cost, bio-compatible, flexible and more environment friendly electronics. The semiconductor industry is currently dominated by silicon, which is very costly in terms of manufacturing, physically brittle and much less bio-compatible as compared to materials such as organic polymers and metal oxides such as zinc oxide. Research on

exotic semiconductor materials such as organic semiconductors, amorphous oxides, carbon nano-tubes has thus attracted much attention in the past two decades.

There are limitations to these alternative materials with respect to tradeoffs between process costs, device performance, and reliability. But significant progress has been made in this area to make such technologies rival the cost effectiveness of silicon in large-area and low-cost applications like display arrays, sensors, LEDs, RFID and photovoltaic cells [1-2]. Successful demonstrations of circuits with complementary devices (p-type and n-type i.e. CMOS technology) made of organic semiconductors, imply the scope of low-power, high noise-immunity, fast circuit designs in this area [3].

Figure 1.1 below illustrates the different semiconductors used in TFTs and applications based on their field-effect mobilities.

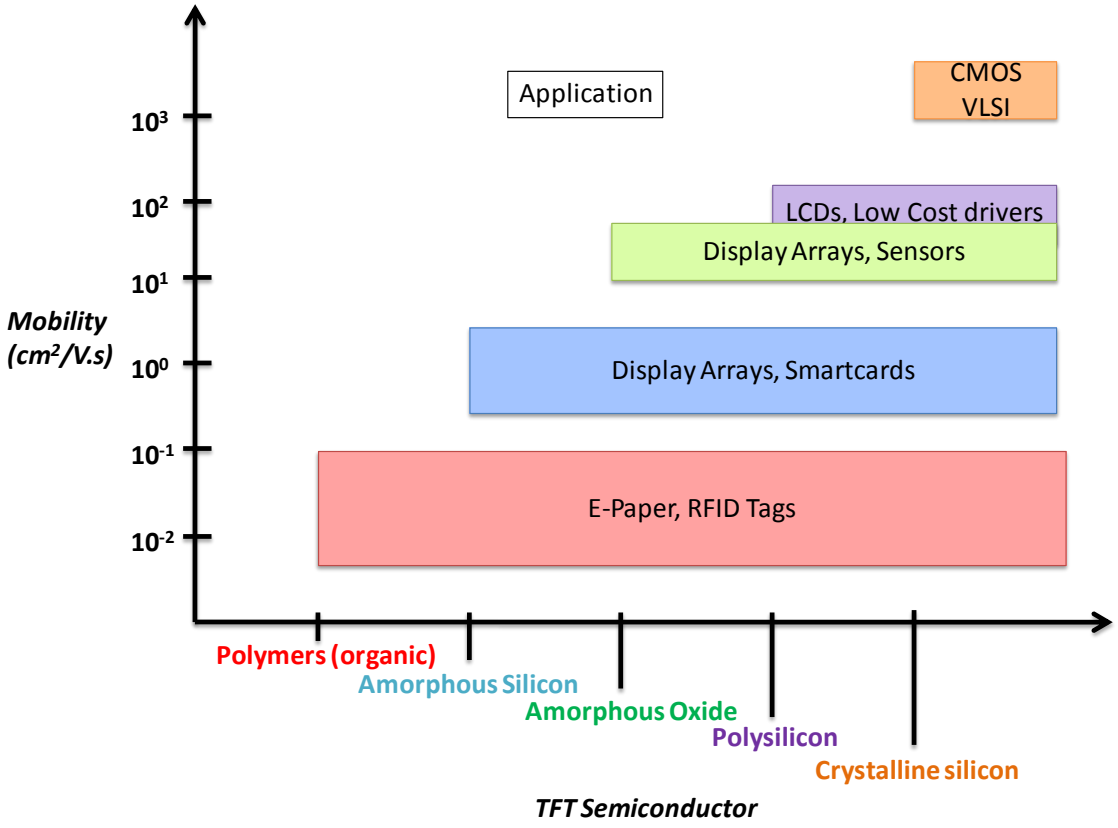


Figure 1.1 Applications of TFTs

The focus of our research has been the study and use of amorphous oxide semiconductor: Zinc Tin Oxide (ZTO) TFTs for circuit applications. Commercially viable display applications using amorphous-oxide TFTs have been demonstrated in [4] and [5]. Demonstrations of basic circuit blocks including inverters, ring oscillators and amplifiers are reported in [6-9].

Other potential contenders for applications contemplated for ZTO include: Hydrogenated Amorphous Silicon (a-Si:H) and organic/polymeric semiconductor materials such as Pentacene. ZTO being an amorphous inorganic semiconductor, possesses higher mobilities, better stability and transparency, compared to organic semiconductors. Since the stability of device characteristics and a high current drive are some of the key requirements of analog circuit applications, ZTO devices enable the design of complex and high performance circuits using these devices.

In this thesis we present the design of a high-gain, multistage Operational-Amplifier (OPAMP) based on ZTO devices. Motivation behind this design is the future integration of such OPAMPs on flexible substrates in organic sensor networks or large area sensor applications. This will probably help to reduce the dependence of sensors on high-performance silicon peripherals, required for processing their low amplitude output signals. On a larger scale, this would help to make the system more compatible with extreme physical, chemical and biological environments such as outer space or in vivo environments.

1.2 INTERESTS BEYOND SILICON

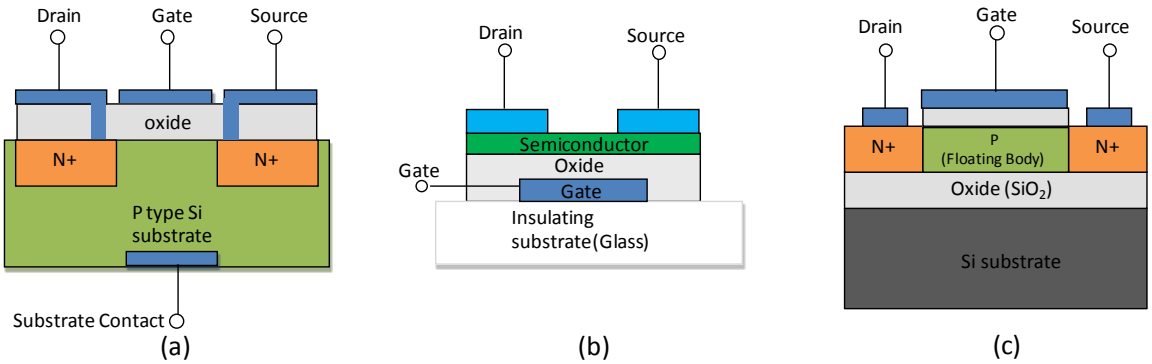


Figure 1.2 Device Structure (a) Conventional Bulk Substrate NMOS, (b) Bottom Gate - Top Contact TFT, (c) Partially Depleted NMOS SOI Device

The first TFT was developed at RCA Laboratories (Princeton) in 1962 using cadmium sulphide as the semiconductor. This was immediately after the introduction of Silicon FET (in 1960) at Bell Labs. But commercially successful TFTs did not arrive until 1980's, which used Hydrogenated Amorphous Silicon (a-Si:H) as the active layer.

TFT is essentially a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). The main distinction is the semiconductor deposited as a thin film layer on an insulating substrate in TFT, as opposed to the bulk substrate/body in conventional MOSFET. TFTs also typically operate in the accumulation mode and not the inversion mode. To get a comparative view, the film thickness of semiconductor layer in TFT is typically in the range of 30 – 100 nm and for bulk single-crystal silicon device, substrate depth is equal to the wafer thickness, which is 100 μm – 1 mm.

For better understanding, a comparison with Silicon-On-Insulator (SOI) technology is illustrated in Figure 1.2. Similar to the SOI devices (more like partially-depleted SOI, where the channel does not extend through the whole depth of the semiconductor), TFTs also operate with a floating body. This makes TFTs advantageous in terms of low leakage with good device isolation, better latch-up immunity, protection against radiation (reduces soft errors) , low parasitic capacitances (junction) and reduced substrate-noise [10-11].

Practically any material can be used as a substrate in TFTs. Widely used insulating substrate are glass and various plastics. However, these substrates cannot withstand temperatures higher than 180°C (e.g. PEN plastic) / 600°C (e.g. borosilicate glass). The deposition process used for the semiconductor layer, the annealing process and oxidation can demand high temperatures, as in the case with single crystal silicon and polysilicon. Thus, the use of low-temperature processes such as Chemical Vapor Deposition (CVD), physical vapor deposition (PVD or sputtering) is favorable for TFT fabrication [12]. Deposition processes that employ even lower temperatures will be even more advantageous.

Unlike bulk MOSFETs which typically operate in the inversion mode, most TFT devices conduct in accumulation mode. Operation of ZTO TFT at different vertical electric fields is discussed later in Chapter 2. The simplicity of the TFT device architecture means that doped source and drain regions are usually not employed. As can be seen from Figure 1.2 (b), the source and drain are formed wherever the metal contact overlaps with the Gate-Oxide-Semiconductor MOS structure.

One major disadvantage of TFTs is the low mobility of charge carriers. In amorphous semiconductors, the low mobility is a result of the charge transport being dominated by thermally-activated transport of localized charge carriers. Mobility of carriers determines the maximum current handling capacity and switching speed of the device. But for applications such as display arrays and sensors, current in a few microamperes and frequencies in a few megahertz can be sufficient. E.g. in display arrays, driving current which can charge all the pixels in a row while the row is being addressed, is sufficient.

Table 1.1 Comparison of semiconductor materials used in TFTs

	ProcessingTemperatures (Celcius)	Typical Field Effect Mobility ($cm^2/V.s$)	Key features
Single Crystal Silicon (BULK)	1000	1500	Highly ordered High processing costs
Single Crystal Silicon On Insulator (SOI) [13]	800 – 1100	400 (100nm buried oxide)	High speed Low power
Polysilicon [14]	150 – 300	> 100	Not transparent Unstable due to grain boundaries
Amorphous-silicon [14]	350	~ 1	Transparent Low reliability Low leakage
Amorphous Metal-oxide	~100	50 – 100	High mobility Good reliability Transparent Low processing costs

1.3 ZINC TIN OXIDE TFTS

Zinc Tin Oxide (ZTO) is an N-type amorphous oxide semiconductor obtained by combining zinc oxide and tin oxide, both of which are transparent materials. The first high performance transparent TFT using ZTO was reported in 2005 [15].

ZTO is an optically transparent semiconductor with a wide band gap of 3.35eV. It is chemically stable, with respect to oxidation and etching, robust in terms of being scratch-free and produces very smooth thin films. ZTO deposited from solution has exhibited electron mobilities as high as 30 $cm^2/V.s$ [15].

What makes this material interesting is that it can be deposited using a solution based process. Previously investigated deposition methods for amorphous oxide include

atomic–layer deposition (ALD), plasma-enhanced atomic-layer deposition pulse laser deposition and RF magnetron sputtering. However the high-vacuum equipment required for these methods makes manufacturing very costly. Thus, low-temperature, low-cost processing of ZTO makes it an ideal candidate for large-area and low-cost applications as well as a very 'green' process with conservation of resources and energy [14].

1.4 ZINC TIN OXIDE TFTS

Compared to the traditional vacuum-based or vapor-deposition processes, solution based processes are simpler and can be performed at much lower temperatures (even at ambient) and lower costs. The need of photolithography for patterning the semiconductor is eliminated as devices can be printed using the solution.

The steps carried out for thin-film deposition of ZTO for devices studied in this thesis are discussed briefly. First, a stable precursor solution of the target film is prepared. The solution is then spin-coated on the substrate. (Alternatives to spin-coating are inkjet printing and dip-coating.) The unwanted solution is then evaporated by heating the substrate in a nitrogen box. Annealing at 500°C is performed to convert the precursor film into oxide form [16].

1.5 ZINC TIN OXIDE TFTS

The bottom gate, top contact structure (Figure 1.3) is chosen for these devices. The semiconductor layer is very sensitive to high temperatures and physical stress caused by deposition and patterning procedures. Thus, it should be the last layer to be deposited. This way, bottom gate structure avoids degradation of the characteristics of the semiconductor layer due to the deposition of oxide and gate layers on top of it [16] and is widely adopted for TFTs. However, for the ZTO TFTs, another important consideration is the fact that, the Aluminum layer (source/drain electrodes) cannot withstand high annealing temperatures (~500°C). With the choice of bottom-gate, top-contact structure, Al layer becomes the last layer to be deposited and thus, is protected.

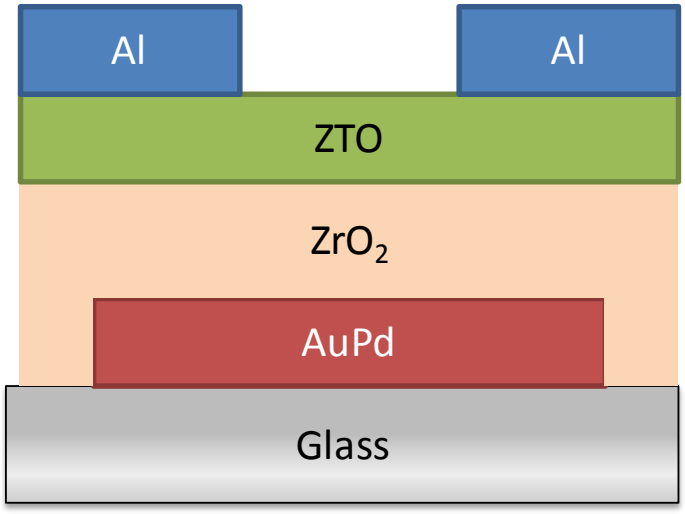


Figure 1.3 Device Structure of ZTO TFT

The gate electrode material is a gold-palladium alloy (AuPd), and is deposited using an e-beam evaporator, thickness of the gate being 40nm. Photolithography is used for patterning the gate. Different types of patterning schemes employed for the gate layer are discussed in Chapter 3. Zirconium Oxide (ZrO_2) (a high-k dielectric) is deposited over the top of the gate using solution based processing similar to that of ZTO. In the third step, ZTO film is spin-coated as described in the previous section. Finally, 100nm thick drain and source electrodes in Aluminium (Al) are deposited in a thermal evaporator and patterned using photolithography. The Al layer forms the top metal contacts. Silver (Ag) is used to plug the vias that connect gate and top metal layer and ensure electrical connectivity between the two metal levels. Contacts for the gate layer are brought to the top level through vias and silver plugs.

A field effect mobility (> 20 $cm^2/V \cdot s$), drain current on/off ratio (> 10^7) and sub-threshold slope (~110 mV/decade) have been observed and reported for the optimally fabricated ZTO devices described above [16].

1.6 ORGANIZATION OF THESIS

This thesis is divided into 6 chapters. Chapter 2 elucidates the importance of a predictive simulation device model for the ZTO TFTs and also the development process that led to a fairly accurate fit for ZTO TFTs obtained from the available a-Si. In Chapter 3, the CAD tool-setup used for the circuit-design and its layout process is discussed. In Chapter 4, the design and fabrication process of various basic circuit blocks are discussed in detail. Chapter 5 is dedicated to the design of a high-gain OPAMP built using ZTO TFTs. Finally, chapter 6 contains the conclusions drawn from this study and the scope for future work in this area.

CHAPTER 2

Compact Device Model for ZTO TFT

The need to depend on CAD tools for the design and for predicting the performance of circuit behavior grows multifold with the increasing complexity of integrated circuits. The requirement of an accurate model that describes and predicts the behavior of the device under different circuit configurations and environmental conditions is very crucial in this process. Along with accuracy, convergence of solution is an important metric for simulation model.

This chapter starts with the background of the physics behind the operation of ZTO TFTs. A review of available models that describe TFT devices is presented. The need to develop a charge based physical compact model for the ZTO TFT devices is demonstrated. The choice of VerilogA open-source platform for implementing this model is proposed. Finally an expression is derived for the gate voltage and temperature dependent carrier mobility observed in ZTO devices.

2.1 WHAT IS A PHYSICAL COMPACT MODEL?

A physical compact model is the representation of device physics in the form of equations. Appropriate assumptions and simplifications are made in the derivation of these equations to make the model computationally efficient. The technology computer-aided design (TCAD) model, used in the design and evaluation of devices, is computationally expensive and thus is not suitable for circuit simulations. Empirical models, which are built by fitting the experimental data, have too many empirical coefficients that do not have any significant physical meaning. An empirical model is thus, not a good choice for analog circuit designs, where fair amount of accurate prediction of the device behavior is desirable. Table-based (lookup) models probably produce the fastest simulation results, however these models depend on the extrapolation techniques for accuracy. This makes them unfit for scalability and statistical variations in

the process. However in the case of a physical compact model, it is possible to account for statistical variations within limits. Also, such a model can be conveniently upgraded to accommodate changes in the process technology by changing parameters, as these parameters have physical significance involved [17].

In circuit simulation, a model that strikes a good balance between accuracy and computational speed is ideal.

2.1.1 Choice of VerilogA

VerilogA is the analog subset of Verilog-AMS, a hardware description language with a subset that defines analog/mixed-signal behavioral modeling. The behavior of analog/ mixed-signal modules is described using mathematical equations and external parameters (e.g. voltage) applied to the module's terminals. The compact modeling extension (Verilog-AMS LRM ver. 2.2) was added to VerilogA in order to have a standard modeling interface between different SPICE-like compact models and analog simulators. Currently, most of the compact models that are released are developed in C language, which has fast and direct access to the simulator. However, these models have simulator specific implementation and development of these models requires extensive knowledge of the simulator. Also, modification of most of these models is a time consuming and complicated process [18]. VerilogA implementation of compact models, on the other hand, is (i) simulator independent, (ii) can be directly used with most commercial circuit simulators (Spectre, HSPICE, ADS, Eldo), (iii) provides features like direct use of symbolic partial derivative and integration for defining currents and voltages and (iv) allows easy upgrades to the model. The Compact Model Council has encouraged the release of VerilogA source code for next generation of MOSFET models [19].

In view of the advantages of this language, VerilogA is proposed as the platform for implementation of the compact model of ZTO TFT devices. The process technology of ZTO devices might still need to go through some modifications, in order to achieve better uniformity and higher carrier mobilities. Hence, the model would have to be upgraded (e.g. in terms of process specific constants) as the process matures. Future

integration of ZTO in CMOS technology is also a consideration behind the choice of VerilogA based simulation model.

In the next section, the background of ZTO device operation and the charge transport mechanism in these devices is elaborated.

2.2 OPERATION OF ZTO DEVICES

The operation of a ZTO device, which is an n – ch accumulation-mode TFT (i.e the semiconductor layer forms an electron accumulation layer upon appropriate bias and is n-type), is explained with the help of energy band diagrams in Figure 2.1. These energy bands are represented with gate of the device as the reference. These band diagrams are applicable to ideal n-type accumulation mode TFTs [20].

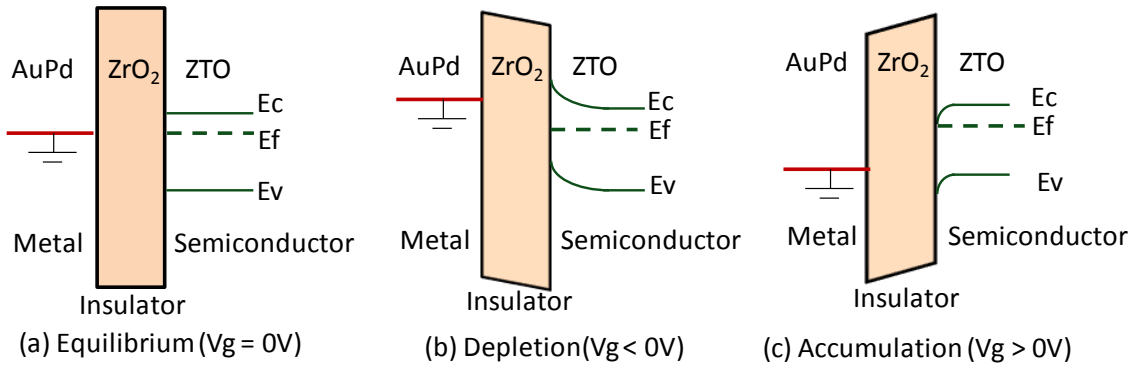


Figure 2.1 Energy Band Diagram of n–ch Accumulation Mode TFT

Figure 2.1 illustrates the effect of vertical field of the gate voltage (V_g) on the charge carriers present at the boundary of the semiconductor and oxide layers.

Equilibrium Mode: In equilibrium, (Figure 2.1(a)), the gate is held at zero volts and there is negligible negative charge accumulation near the surface (assuming flat-band voltage to be zero). The Fermi level of the semiconductor is thus aligned with that of the metal layer and there is no flow of charges. (semiconductor being n-type, the E_f level is closer to E_c). This can be considered as the off-state of the device.

Depletion Mode: When a negative voltage is applied to the gate (Figure 2.1 (b)), mobile electrons are repelled from the semiconductor surface. This creates a depletion region near the insulator/semiconductor interface and the device is said to be in the depletion mode. Away from the surface boundary in bulk, the carrier concentration remains the same as the intrinsic concentration, indicated by the flattening of the energy bands. Band bending of E_c away from the Fermi level E_f, indicates depletion of electrons near the interface. The ZTO film does not allow transport of holes through it and any holes induced by the negative V_g are trapped in its localized states. Thus, the leakage current due to minority carriers i.e. holes in the off and depletion mode of operation is negligible.

Accumulation Mode: When a positive voltage is applied at the gate, mobile electrons are attracted towards the insulator/semiconductor interface. The conduction band bends closer to the Fermi level, indicating increase in the concentration of electrons near the interface. This results in higher conductance of the film or channel formation near the interface. This is the accumulation mode of the device.

The accumulation mode of a TFT is the normal operational mode and is thus equivalent to the inversion mode of a bulk Si MOSFET. ZTO devices are never operated in the inversion mode.

The threshold voltage (V_{th}) is defined as the minimum gate voltage required for the formation of a conducting channel. Another parameter commonly associated with the operation of TFTs is $V_{ON,}$ the onset voltage of drain current. For bulk MOSFETs, the threshold voltage V_{th} is extracted by linear extrapolation of I_D - V_{gs} transfer curve. But in case of amorphous semiconductor TFTs, V_{th} cannot be defined precisely due to the shape of the I_D - V_{gs} transfer curve. However, the onset voltage where drain current rises considerably over the gate leakage and noise floor of the device can be clearly defined from the *log*(I_d) - V_{gs} curve (Figure 2.2).

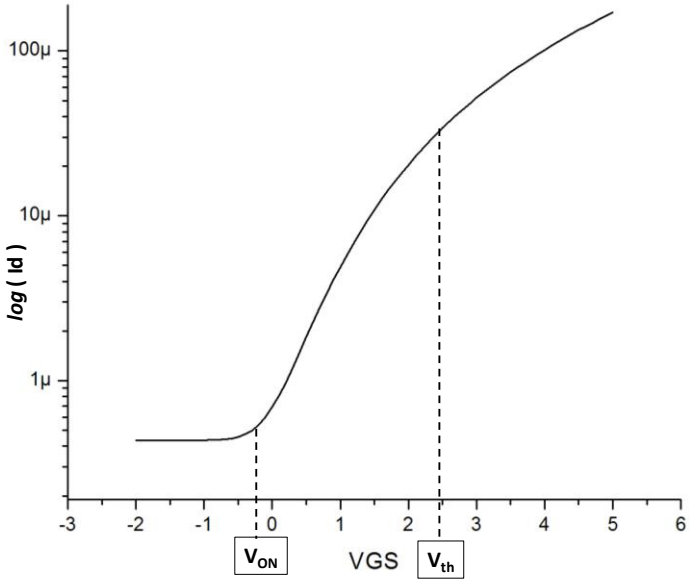


Figure 2.2 V_{ON} and V_{th} from *log*(I_d) –V_{gs} curve

For a ZTO device already biased in the accumulation mode, the effect of lateral field caused by the voltage between drain and source terminals is discussed next.

When the device is in the accumulation mode, a channel is already formed near the semiconductor/oxide interface, below the gate terminal. Now, if a positive voltage is applied between the drain and source terminals, charges drift under this lateral electric field, i.e., current conduction takes place through this channel from drain to source (drain being the terminal held at higher potential). As the drain voltage (with respect to source voltage, i.e., V_{ds}) becomes more positive, the accumulation charges near the drain terminal are repelled and the region begins to deplete. Initially as V_{ds} increases, current increases linearly with it. After a certain V_{ds} termed as V_{dsat}, the carriers near the drain terminal are completely depleted i.e. the channel is pinched-off near the drain. As V_{ds} increases further, the pinch-off point moves away from the drain terminal towards the source. In this case, when $V_{gs} > V_{th}$ and $V_{ds} >= V_{dsat}$, the device is said to be in the saturation regime. These electrons drift through the depletion region between the pinch-off point and the drain.

From the discussion above, it can be said that the operation of a TFT is sufficiently similar to that of a bulk MOSFET. Hence, the gradual channel approximation model can be applied to arrive at the drain current expression i.e.

in linear regime : $I_d = \left(\frac{W}{L}\right) . C_{ox} . \mu . [\left(V_{gs} - V_{th}\right) * V_{ds} - \frac{V_{ds}^2}{2}]$ (2. 1)

in saturation regime: $I_d = \left(\frac{W}{2L}\right) . C_{ox} . \mu . [(Vgs - Vth) * \left(V_{gs} - {V_{th}}^2\right)]$ (2.2)

In the above equations, C_{ox} is the capacitance of the gate insulator per unit area, μ is the mobility of the electrons in the channel.

The gradual channel approximation however assumes the mobility (μ) to be independent of gate voltage and contact resistances to be negligible. SPICE level 1 model for MOSFET uses the gradual channel approximation to derive the drain current expression. This model was modified (APPENDIX B: SPICE Level 1 MOSFET model) to accommodate the mobility value and gate-insulator capacitance value obtained from the experimental data. Simulation results obtained using the modified SPICE level 1 model were compared with the experimental data (Figure 2.3, Figure 2.4) [20].

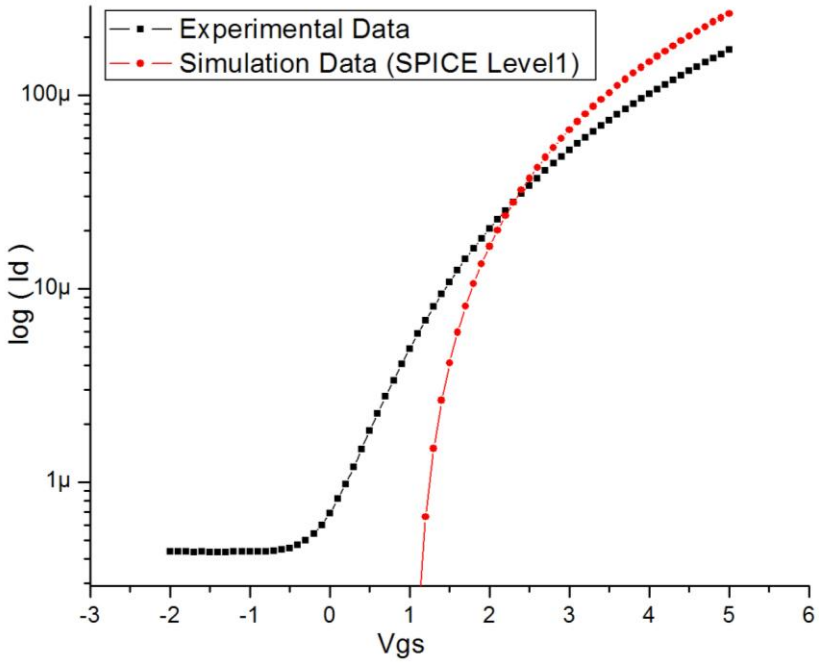


Figure 2.3 Comparison of Experimental Data and SPICE Level 1 model simulations for Transfer Characteristic Curve ($I_d - V_{gs}$) of W=80um, L=4um ZTO Device

It is observed that the behavior of ZTO cannot be described accurately with the level 1 model. The reason behind this difference is the fact that, the mechanics of charge transport that governs the current conduction in the thin film of amorphous semiconductor is quite different from that in the case of crystalline silicon.

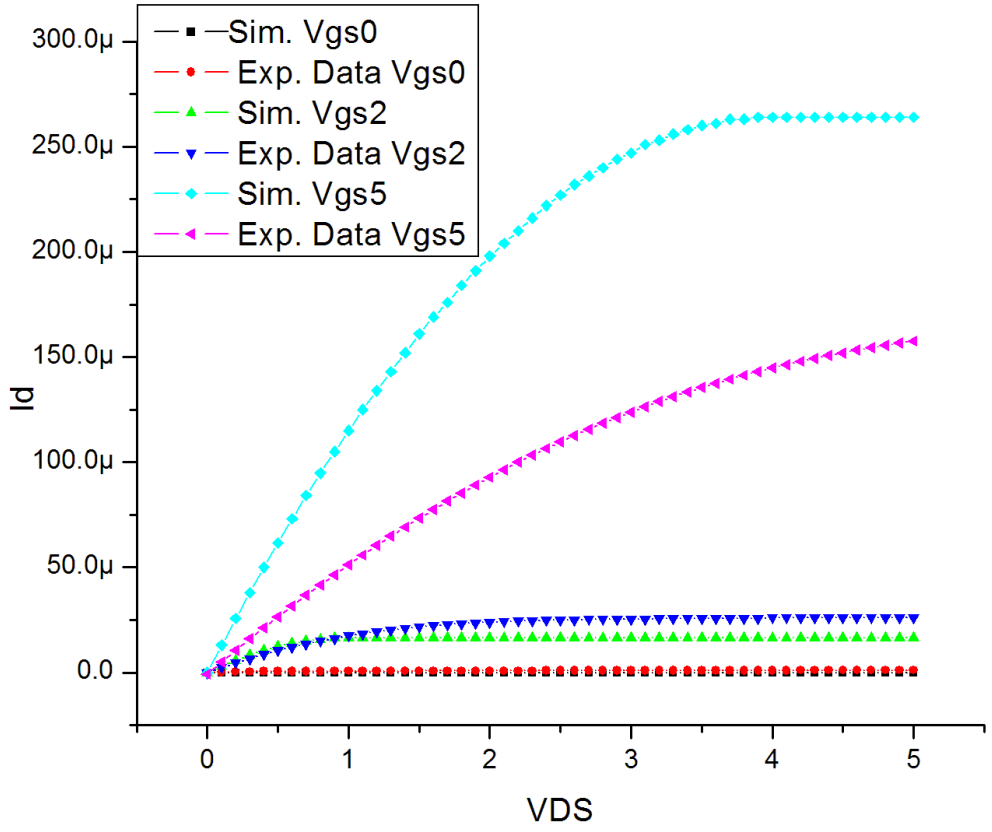


Figure 2.4 Comparison of Experimental Data and SPICE Level 1 Model Simulations for Output I-V (I_d – V_{ds}) Curves of W=80um, L= 4um ZTO Device

2.3 CHARGE TRANSPORT

2.3.1 Charge Transport in crystalline semiconductors

The mechanism of charge transport in highly ordered crystalline inorganic semiconductors (e.g. single crystalline silicon, polysilicon) is called as band transport. Due to the ordered nature of the lattice in crystalline semiconductor, atoms interact closely with each other in such a way that carriers (electrons or holes) move easily between atoms in the crystal. Analogous to the valence orbital of an atom, valence energy band has the lowermost energy level and is mostly occupied by electrons in a lightly doped semiconductor which can be considered as an insulator at room temperature. The conduction band, on the other hand, consists of mostly unoccupied states. The Fermi

level is a statistical energy level that lies between the conduction and valence bands (in non-degenerately doped semiconductors) and has 50% probability of occupancy. The energy gap between the conduction and valence bands is called as bandgap. The difference in the bandgaps of metals, semiconductors and insulators is illustrated in Figure 2.5. The bandgap is also called as the forbidden gap as energy levels of states should never fall in this region. The probability of occupancy of these available states by charge carriers is determined by the Fermi-Dirac distribution.

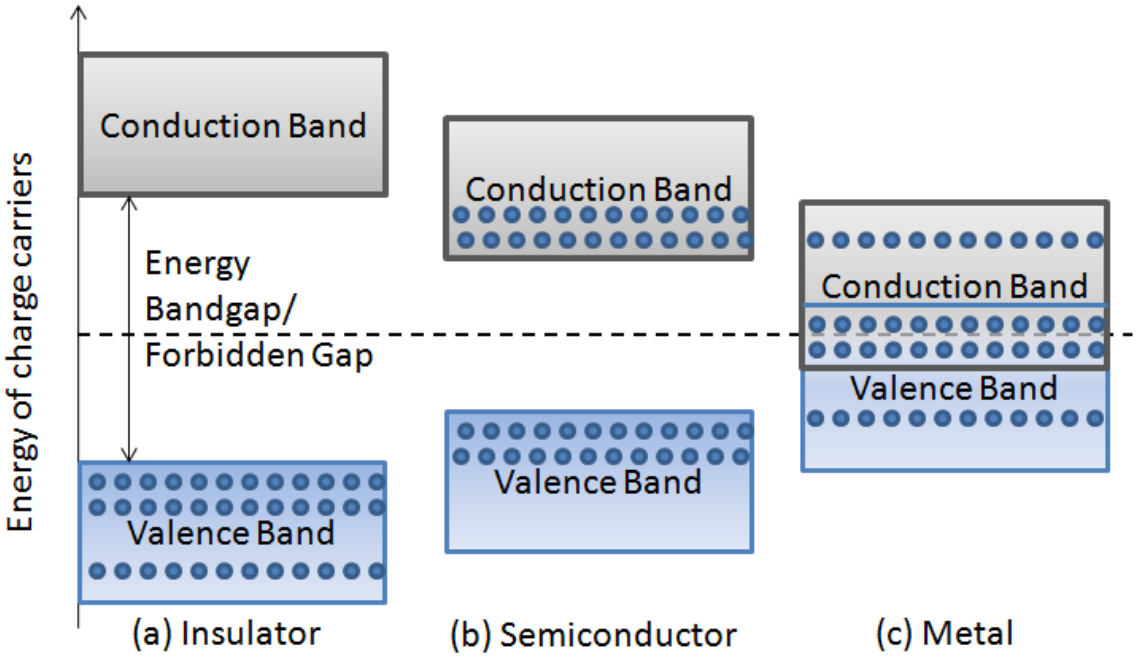


Figure 2.5 Energy Bands of (a) Insulator , (b) Semiconductor, (c) Metal

The transport of electrons in a crystalline semiconductor with band transport can be described by the Drude model [21]. In this model the electrons are assumed to move freely under the effect of electric field, with the only impedance being caused by the collision with the lattice. Thus the mobility (μ) of electrons can be expressed as

$$\mu = \nu / E \qquad (2.3)$$

where ν is the velocity of electrons and E is the lateral electric field in the channel. The mobility is given by $\mu = q\tau/m^*$, where τ is the scattering time and m^* is the effective mass.

This mobility has a power law relation with temperature, where the mobility increases with decrease in temperature and decreases at higher temperatures due to phonon scattering (caused by vibration of the lattice).

2.3.2 Charge transport in amorphous semiconductors

The charge transport in an amorphous semiconductor is essentially different from that in a crystalline semiconductor due to the dominating effect of trap states in the forbidden gap. Many localized trap-states are formed in the semiconductor film due to structural defects /disordered atoms and unwanted impurities. These trap states can be imagined to be closely placed energy levels in the bandgap, often forming a continuous distribution. Once a charge carrier is able to attain the energy level of a particular trap-state, it is captured in that state and is released only after a specific retention period or in other words, a charge carrier gets trapped at this. The release of a carrier from the trap state is often governed by thermal energy. The released carrier gets thermally excited to the band where it moved before being re-trapped. Such a transport mechanism is called multiple trap and release and is observed in amorphous semiconductors such as amorphous Si and zinc tin oxide. The trap-and-release mechanism limits charge-transport in the amorphous semiconductor film, as a trapped carrier cannot move in till it gets released [22]. The electronic density of states (DOS), describes the energetic distribution of such localized states. In non-crystalline semiconductors, the highest energy at which states are still localized is called as the mobility edge (E_C).

Multiple theories have been proposed to explain this trap limited transport, with Multiple Trap and Release (MTR) and Variable Range Hopping (VRH) being the two most widely used models.

The MTR model assumes that the localized states lie near the transport band edge. The transport band edge is a statistical energy level, above which the charge transport is

band like transport (delocalized bands) and states below this edge are all trap states. In the MTR model, as charge carriers transit in the trasport band, they get trapped and released (thermal release) multiple number of times from the localised trap states in the vicinity of the band edge. Figure 2.6 illustrates this mechnism.

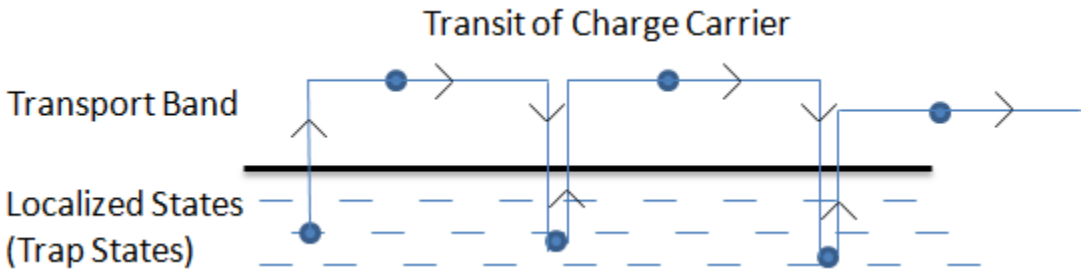


Figure 2.6 Charge Transport in MTR model

The effective mobility of charge carriers is thus given by:

$$\mu_{eff} = \mu_o \,.\, \alpha \,.\, e^{-(Ec-Et)/kT} \cong \frac{N_t}{N_c} \,.\, e^{-(Ec-Et)/kT} \qquad (2.4)$$

where, μ_o is the mobility in the transport band, α is a constant depending on the ratio of carriers in the band to the total charge carriers, ($E_c - E_t$) is the difference in energy levels of the transport band and the trap state level. An approximate expression in terms of N_c (effective DOS near the band edge) and N_t (DOS of the trap state) is obtained by assuming single trap state of energy level E_t (Eq. (2.4)). It can be observed from this equation that the band mobility gets scaled depending on the ratio of carriers promoted to the transport band to the total number of carriers. Thus, the effective charge mobility observed is usually much smaller than the band mobility.

The Monroe model is an extension to the MTR model [23]. This model is better applicable to charge transport at low temperatures. In the MTR model, the DOS is like a tail to the delocalised transport band and the mobility edge (E_c) is defined as the highest energy level of a localised (trap) state. However in the Monroe model, the transport states are also considered to be in the band tail. Monroe model assumes exponential distribution of trap / localised states in the band tail, expressed as:

$$g(E) = \left(\frac{N_L}{kTo}\right).\, e^{(E\,/\,k.To)} \qquad (2.5)$$

where, E is the energy of a the trap state with respect to the mobility edge and it is more negative for deeper states (away from the edge towards the valence band), N_L is the total number of trap states in the band tail, T_o is the characteristic temperature obtained from the width of the exponential. As can be observed from illustration in Figure 2.7, deeper states have lower density as compared to the densely populated shallow states. Thus, it is easier to find a neighbouring state of around the same energy level when a carrier is in shallow states. This way, carriers can hop to the neighbouring states even at low temperatures. However, when in deep states, it is easier for the carrier to jump to a shallower state with higher energy level due to thermal excitation. Eventually the carriers are trapped in a deep state, as being at a lower energy level is favourable state.

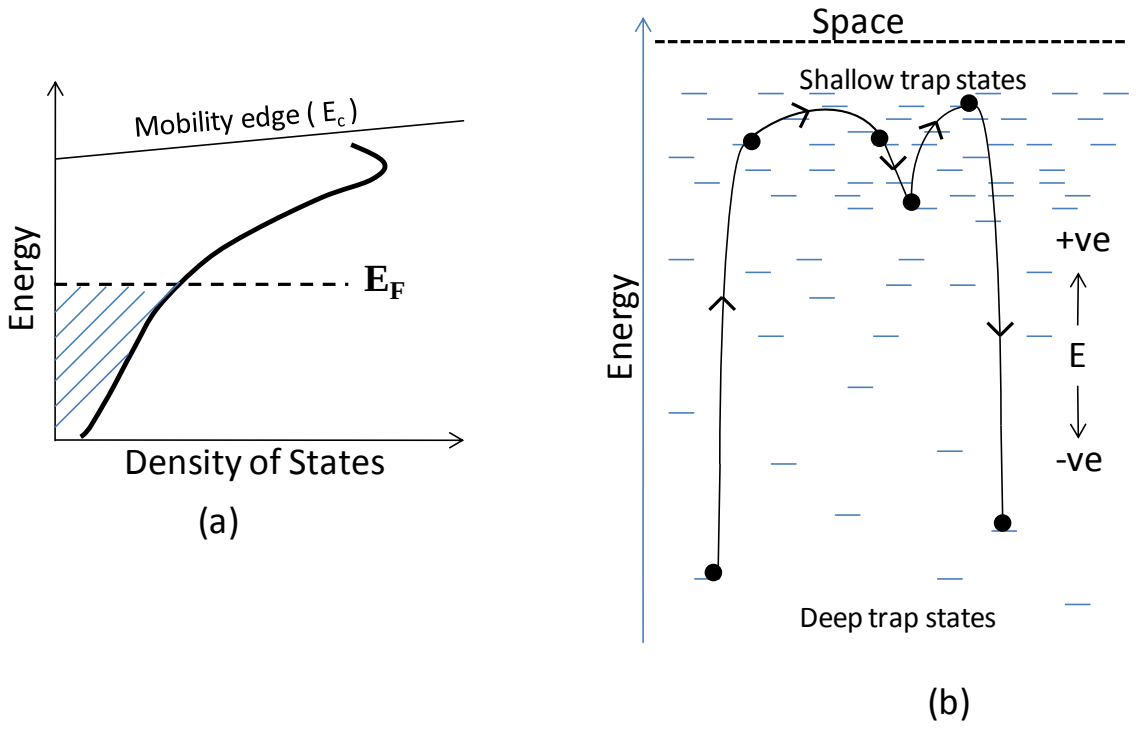


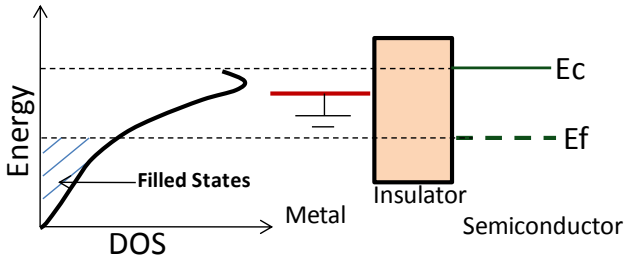
Figure 2.7 (a) Mobility edge and Band tail DOS in MTR model, (b) Charge transport in Monroe model

The Variable Range Hopping (VRH) model on the other hand, assumes Gaussian distribution of the localised (trap) states. It is widely accepted as the charge transport mechanism for disordered semiconductors (especially organic semiconductors). According to this model, carriers can hop over a long horizontal distance (to a neighbouring state with similar energy level) with a low activation energy or hop over a small vertical distance (to a state with higher energy level) with a higher activation energy. The charge transport in this model is thus, based on the thermal hopping of carriers between localised states.

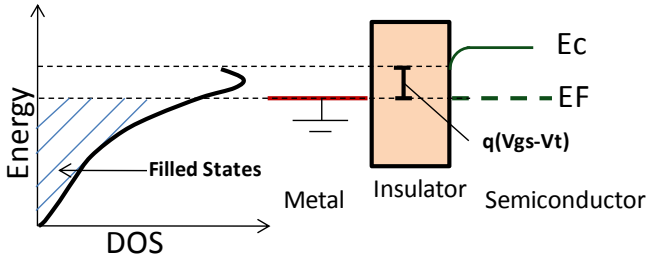
2.3.2.1 Gate bias dependence of mobility

An important outcome of the MTR and Monroe models is that the mobility of charge carriers can no longer be considered to be voltage independent. The shift in energy band diagrams with the externally applied electric field or gate bias has been discussed at the beginning of section 2.2. This relative shift of energy levels can be associated with the DOS and total number of filled states, as illustrated in

Figure **2.8**. In the accumulation regime ($V_{gs} - V_t > 0$), the difference between filled trap states ($E_f \cong E_t$) and the edge of the transport band (E_c) reduces. Thus, release of trapped carriers to the transport band becomes easier, increasing the effective mobility of charge carriers. This can be analytically explained using Eq. (3.4). As the difference ($E_c - E_t$) reduces, the value of the effective mobility increases.



(a) Equilibrium (Vgs - Vt = 0V)



(b) Accumulation (Vgs - Vt> 0V)

Figure 2.8 Shift in the level of filled states makes mobility gate-bias dependent

2.3.3 Charge transport in ZTO

Temperature-dependent measurements of the solution-processed ZTO devices under study have shown that, the charge transport in these devices is a combination of MTR and band transport [24]. At low values of (V_g - V_{ON}), the effective mobility is observed to increase with increasing temperatures. This is an indication of the multiple trap and thermally activated release of charge carriers between the localized states and the transport band. However, at higher values of (Vg - V_{ON}), the effective mobility of carriers decreases with increasing temperature. This effect can be attributed to the phonon scattering or lattice vibrations that limit the mobility of carriers at high temperatures in band transport. As illustrated in Figure 2.9 (b), as the gate voltage becomes highly positive, most localized states get filled up with induced carriers. Thus, the Fermi level (E_f) starts approaching the mobility edge and at a sufficiently high (V_g - V_{ON}), E_f crosses the edge. In this scenario carriers move freely in the delocalized states and thus, band

transport dominates. The cross-over from thermally activated to band transport accounts for the high mobility values (μ (300K) > 20 cm^2/V.s) observed in ZTO.

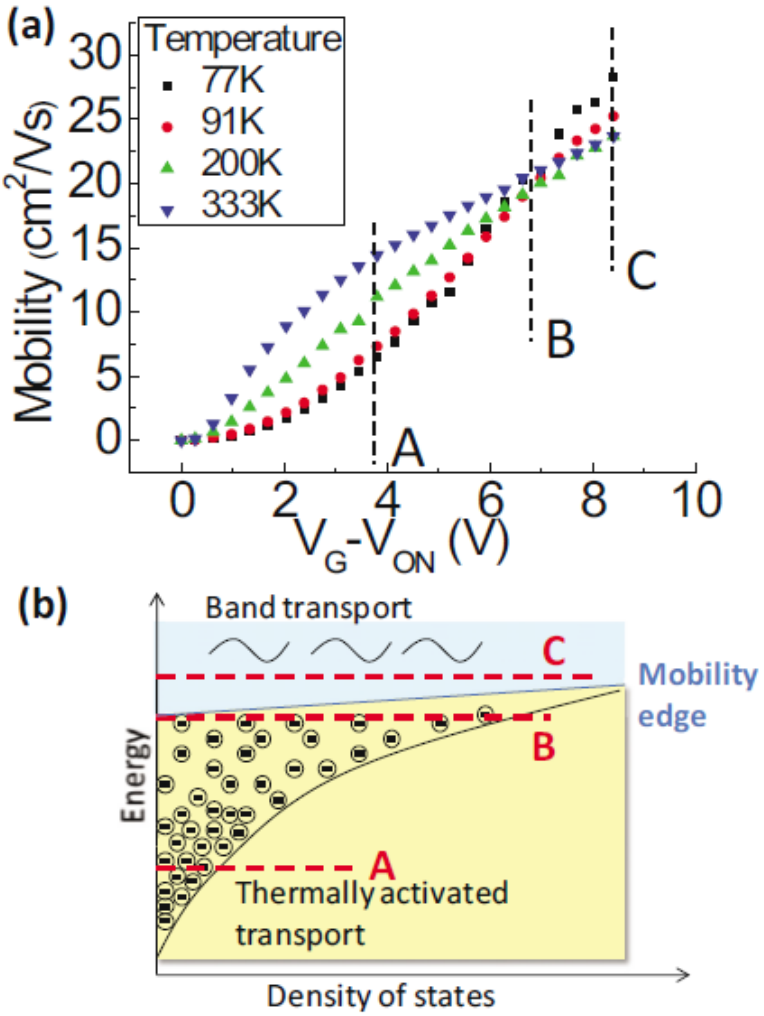


Figure 2.9 (a) Temperature and V_G Dependent Effective Mobility, (b) Charge Transport in Different Regimes.[25]

It has been shown in [24] that there is a fairly accurate fit between the MTR model (Eq. 2.4) and the experimental data obtained at different temperatures(Figure 2.9 (a)), provided (V_g - V_{ON}) is below the crossover point to band transport. Thus, the effective mobility (μ_{eff}) has the following relation with the band mobility (μ_0):

$$\mu_{eff} = \mu_0 \cdot e^{\left(\frac{-E_a}{kT}\right)} \quad (2.6)$$

where, E_a is the activation energy or $(E_c - E_t)$, k is the Boltzman's constant and T is the temperature.

2.4 COMPACT MODELING OF AMORPHOUS OXIDE SEMICONDUCTOR TFTS

Although there have been significant improvements in the performance of TFTs, accurate simulations of their electrical characteristics are still rendered difficult by the parasitics and unusual characteristics observed in these devices. These effects could be arising from the process, could be intrinsic to the electronic properties of the material or material combination or the device design. Often, the basic expressions developed for drain current in bulk MOSFETs, are used to extract quantities like mobility, threshold voltage, contact resistance, leakage currents, subthreshold slope of the TFT devices. Owing to the fundamental difference in the charge transport mechanism in these materials as discussed in section 2.3, such extracted parameters poorly describe the characteristics of interest. Moreover, TFTs have a floating body structure which cannot be compared with the bulk MOSFET models available in SPICE.

2.4.1 Review of available models

Several research groups have been working on the development of accurate compact models of TFTs, which can be useful for circuit simulations. There have been many attempts to describe the physical characteristics of different TFTs using analytical models [26-30]. A closed form DC analytical solution verified against the measured data of zinc oxide and ZTO TFTs has been derived in [31]. This model is based on an nth order polynomial fit for deriving the effective mobility and requires an order of 6 to get accurate results, which seems impractical to be implemented in circuit simulators. Considering the importance of a suitable model for circuit simulations, many analytical models have been proposed in recent years which include suitable extensions for TCAD / Compact models [32]. One such generic compact model suitable for circuit simulations of OTFTs, has been proposed in [33], that eliminates the empirical parameters (which

make DC modeling, process specific) from current and voltage expressions. Some of these models were eventually adopted for converting into SPICE-like compact models which could describe the non-linearities such as, gate voltage dependent mobility and non-ohmic contact resistances in terms of circuit components. Such models were then implemented for circuit simulations. One widely recognized model in this case was the analytical model proposed by Shur M [34]. This model was initially proposed to describe the behavior of aSi and polysilicon TFTs and later on got extended to other TFTs as well. The Estrada M et.al. group then developed the unified model and parameter extraction method (UMEM) to fit this model to a wide range of TFTs: aSi-H [35], polysilicon [36], nanocrystalline silicon [37] and OTFTs [38]. The original model proposed in 1997 by Shur M was improved over the years and came to be commonly known as the RPI (Rensselaer Polytechnic Institute) model. Often such models end up being dominated by multiple fitting parameters, which are oblivious to the device physics. The extraction procedures required to obtain these fitting parameters for a particular process is quite complicated. In view of this, a universal compact model using only 8 parameters was proposed in [39]. This model is basically an extension of the RPI model that accounts for short-channel effects and non-linear contact resistances. The authors propose that this model should be used as the first iteration in the development of a new device/ technology.

An accurate DC model is sufficient to describe the current and voltage characteristics of a device. But to be useful in circuit simulations, the DC model has to be accompanied by the dynamic and/or small signal model as well. The dynamic model is used to observe the large signal transient behavior of the device. The small signal model assumes the DC operating point of the circuit to be stable and performs frequency response analysis or AC analysis at that particular bias/DC-OP point. Very few compact models of TFTs have been reported, that include both DC and dynamic/ AC solutions. A DC/AC unified model based on Variable Range Hopping (VRH) mechanism has been developed in [40], which targets the use of OTFTs in circuit design for RFID applications. This model contains a total of 19 parameters and it has already been used

for designing some RFID circuits. In [41], a mathematical model has been proposed for DC/ dynamic operation of TFT. Due to the charge – based approach adopted in this model, a very clean solution is available to arrive at the dynamic model. The simple mathematical expressions derived, make it suitable for circuit simulator implementations. This model is also based on the VRH mechanism.

Development of a physical compact model can be identified as the niche in the area of study and application of amorphous oxide TFTs in circuit design. The model is expected to have minimal dependence on empirical parameters and strong correspondence with the device physics. It should consist of simple mathematical expressions which would result in fast convergence of the circuit simulations.

2.4.2 Simulations with RPI model

The sophisticated compact models developed by the RPI group for aSi:H and polysilicon TFTs, have been integrated successfully in the commercial circuit simulators like Spectre, AIM-SPICE, T-SPICE. This model has 6 geometrical and technology related parameters (CGDO, CGSO, TOX, EPS, EPSI, IOL), 3 trap distribution and intrinsic layer quality related parameters (DEF0, GMIN, V0) and 18 other fitting parameters [42]. Other than the exceptions of a few open–source VerilogA implementations of TFTs (unpublished), this is the only commercially available TFT model which has been implemented for circuit simulators.

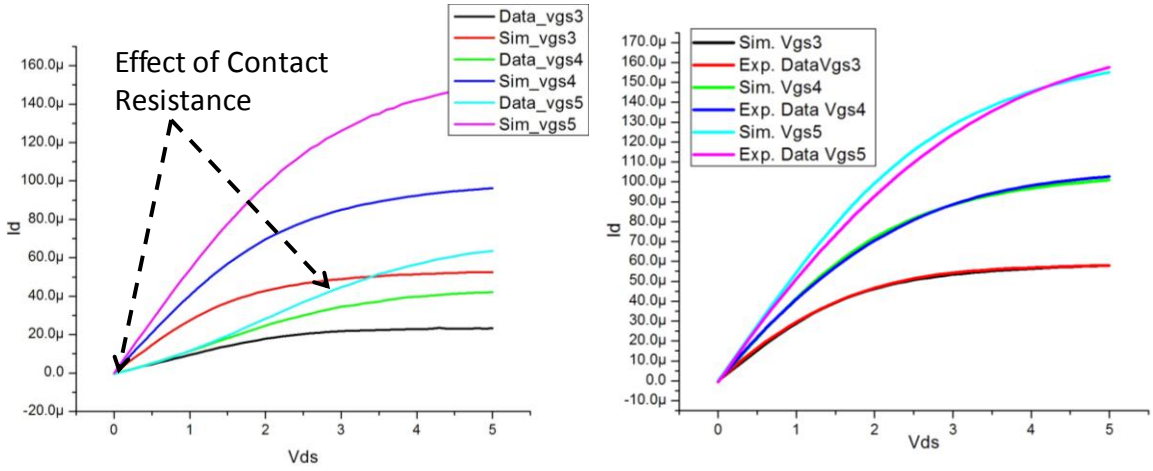
In this study, the RPI aSi model available in Spectre simulator [42] was used to fit I- V curves of the experimental data of ZTO devices. A close fit was obtained by varying the fitting parameters available in the model [APPENDIX B: aSi_model]. However, following shortcomings were observed in this fit:

(i) The contact resistance values fit for I-V data of one device did not apply to data of other devices. (Figure 2.10)

(ii) The simulations for $I_d - V_{ds}$ curves deviated from the experimental data at low values of V_{gs}. (Figure 2.11)

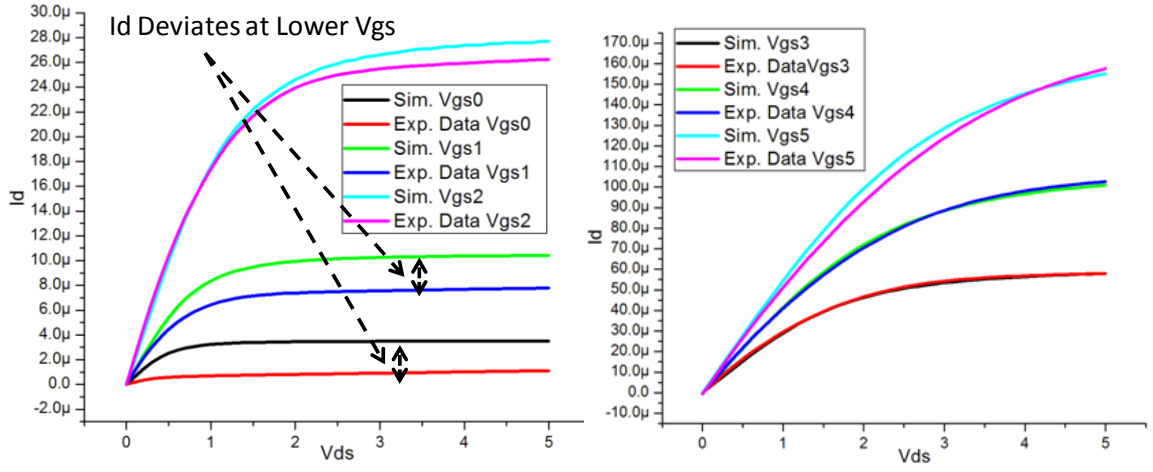
(iii) The effect of dominating gate leakage observed in small ZTO devices at low V_{ds} values, was not accounted for by the fit. (Figure 2.12)

(iv) The exponential dependence between effective mobility and activation energy could not be observed clearly from the simulations.



(a) W = 81u L= 4u (b) W = 80u L= 4u

Figure 2.10 Fitting of contact resistance for Device1 [W/L = 80u/4u] does not fit Device2 [W/L = 81u/4u]



(a) W = 80u L= 4u : Vgs (0, 1, 2 V) (b) W = 80u L= 4u : Vgs (3, 4, 5 V)

Figure 2.11 I_d – V_{ds} data fits better at higher V_{gs} (3, 4, 5V) than lower V_{gs} (0, 1, 2 V) values

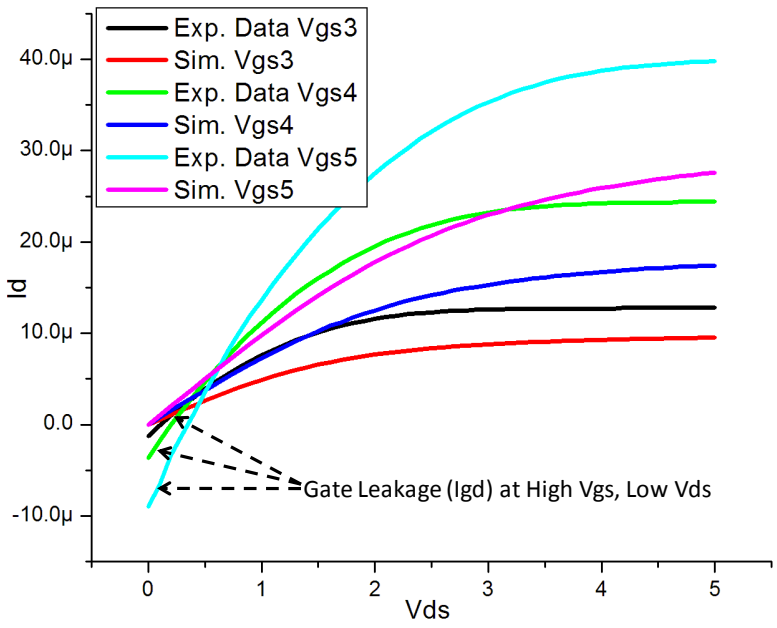


Figure 2.12 Gate leakage (I_{gd}) observed in small device [W/L = 14u/4u] at high V_{gs} and low Vds, cannot be seen in simulations

The deviation of simulation data from the experimental data could be accounted for, by the fact that the RPI model does not attend closely to the charge transport mechanism of the device. In this model, a power law expression with fitting parameters is used to describe the gate bias dependent effective mobility:

$$\mu_{eff} = \mu_0 . \left(\frac{V_{gs}-V_{th}}{Vaa}\right)^{\gamma} \qquad (2.7)$$

where μ_0 is mobility of the conduction band, while Vaa and γ are fitting parameters.

It can be observed from Eq. (2.7) that, the strong interaction between the effective mobility and charge transport mechanism is missing in the derivation.

The next section describes the derivation of the expression for effective mobility, based on the physical phenomena behind the operation of the ZTO devices.

2.4.3 Expression for Effective Mobility in ZTO Devices

From the discussion in section 2.3.3, charge transport mechanism of ZTO devices can be modeled as a multiple trap and thermal release phenomenon. Thus, Eq. (2.4) is used as a starting point to derive the effective mobility:

$\mu_{eff} = \mu_o \,.\, \alpha \,.\, e^{-(Ec-Et)/kT}$ (from Eq.(2.4))

In this model, band mobility scaled by the ratio of free carrier density (volume) to the total carrier density (volume) is termed as the effective mobility.

$$\mu_{eff} = \mu_o \,.\, \left(\frac{n_c}{n_t+n_c}\right) \qquad (2.8)$$

where, the free carrier (carriers in the transport band) density n_c ,based on Boltzman's approximation is:

$$n_c = N_c \,.\, e^{-(Ec-Ef)/kT} \qquad (2.9)$$

and the density of trapped carriers in single trap energy level (E_t) with DOS of N_t is:

$$n_t = N_t \,.\, e^{-(Et-Ef)/kT} \qquad (2.10)$$

From Eq. (3.8 , 3.9 and 3.10),

$$\mu_{eff} = \mu_o \,.\left(\frac{1}{1+\frac{N_t}{N_c}e^{(Ec-\ Et)}}\right) \cong \frac{N_c}{N_t} e^{-\,(\,Ec-Et\,)/kT} \qquad (2.11)$$

From the study of charge transport in ZTO devices , the trap distribution below the band edge is given by an exponential band tail [16]. The expression derived in Eq. (2.11) assumes the distribution to be a constant value i.e. a single (dominating) trap level. As ZTO devices exhibit a continuous range of trap states, the above expression cannot be directly applied to describe the effective mobility of these devices.

The exponential band tail trap distribution is given as:

$$N_t\,(E) = \frac{N_{to}}{kTo} \,.\, e^{-\,(\,Ec-E)/kTo} \qquad (2.12)$$

where, N_t is expressed as an exponential function of the energy level E, N_{t0} is the total density (per unit area) of the trap states and T_0 is the characteristic width of the density distribution.

The density of trapped charges can be given as (assuming that a large number of carriers are trapped i.e. $n \approx n_t$) :

$$n = \int_{-\infty}^{Ec} N_t\,(E).\,f(E)\,dE \qquad (2.13)$$

where, f (E) is the Fermi Dirac distribution that decides the probability of charge carriers at an energy level E.

The expression for Fermi Dirac distribution is,

$$f\,(E) = \frac{1}{1+ e^{(E-Ef)/kT}} \qquad (2.14)$$

For simplification, the Fermi Dirac distribution can be neglected by assuming absolute zero operation. With this condition substituted in Eq.(2.14), for energy level (E) above E_f, the value of distribution equals zero while, for E below E_f, it equals to 1. Thus, in absolute zero operation, carriers fill up the states only till the Fermi level (E_f), and all charge is trapped.

With the above assumption, bounds of the integral in Eq. (2.13) can be taken as $-\infty$ till E_f. Also, the value of Fermi Dirac distribution f (E) can be substituted as 1.

Thus, Eq. (2.13) becomes,

$$n = \int_{-\infty}^{Ef} \frac{N_{to}}{kTo}.\,e^{-\,(Ec-E)/kTo}.1\,dE$$

$$n = N_{t0}\,.\,e^{-\,(Ec-Ef)/kTo} \qquad (2.15)$$

From Eq. (2.15),

$$(E_c - E_f) = kT_0\,.\ln\left(\frac{n}{N_{to}}\right) \qquad (2.16)$$

From Eq. (2.9) and (2.17),

$$n_c = N_c\,.\;e^{-\left(\frac{To}{T}\right)\ln\left(\frac{n}{N_{to}}\right)} \qquad (2.17)$$

Now, Eq. (2.8) can be expressed as,

$$\mu_{eff} = \mu_o\,.\left(\frac{n_c}{n}\right) \qquad (2.18)$$

where, n is the density of total induced carriers.

Thus, using Eq. (2.15, 2.17 and 2.18),

$$\mu_{eff} = \mu_o\,.\left(\frac{N_c}{N_{to}}\right).\left(\frac{n}{N_{to}}\right)^{\left(\frac{To}{T}-1\right)} \qquad (2.19)$$

The total induced carrier (voulme) density can be expressed as,

$$n = \frac{C_g\,(V_{gs} - V_{ON})}{q.t} \qquad (2.20)$$

where, Cg is the gate capacitance, q is the charge of an electron and t is the estimate of thickness of the channel formed (depth of channel penetration into the semiconductor film)

Thus, the expression for effective mobility of ZTO device is obtained as (From Eq. (2.19 and 2.20)):

$$\mu_{eff} = \mu_o \cdot \left(\frac{N_c}{N_{to}}\right) \cdot \left(\frac{C_g.(V_{gs}-V_{ON})}{q.N_{to}.t}\right)^{\left(\frac{To}{T}-1\right)} \qquad (2.21)$$

2.4.4 Curve fitting of effective mobility

The various parameters in the expression of effective mobility derived in the above section are:

μ_o : Mobility of carriers in the transport band

N_c : Total density of states (per volume) in the extended states/ near the transport band edge

N_{t0} : Total density of states (per volume) in the band tail i.e. total DOS of trap states

Cg : Gate capacitance (Cox) per unit area

V_{gs}: Externally applied gate voltage w.r.t. source

V_{on} : Onset voltage

q : Unit charge

t : Depth of penetration of channel into the semiconductor film (Estimated as 150 nm)

T_0 : Characteristic temperature that decides the width of the distribution of trap states (Kelvin)

T : Operating temperature in Kelvin

Out of these parameters, estimate values were avaliable for N_{t0} and T_0 from the experiments performed previously [16] .Through these experiments a plot of the density

of states (DOS) (states/ meV. cm^3) as a function of the activation energy (E_a) (meV) was available. As illustrated in Figure 2.13, a linear fit was obtained for the DOS to evaluate its intercept with the y-axis ($E_a = 0$). Using the relation, ($E_a = E_c - E_t$) and Eq. (2.12), the intercept is evaluated as (N_{t0}/ kT_0) (states/ meV. cm^3). The linear fit was then integrated over the available range of E_a to obtain the total number of density of states: N_{t0} (states / cm^3).

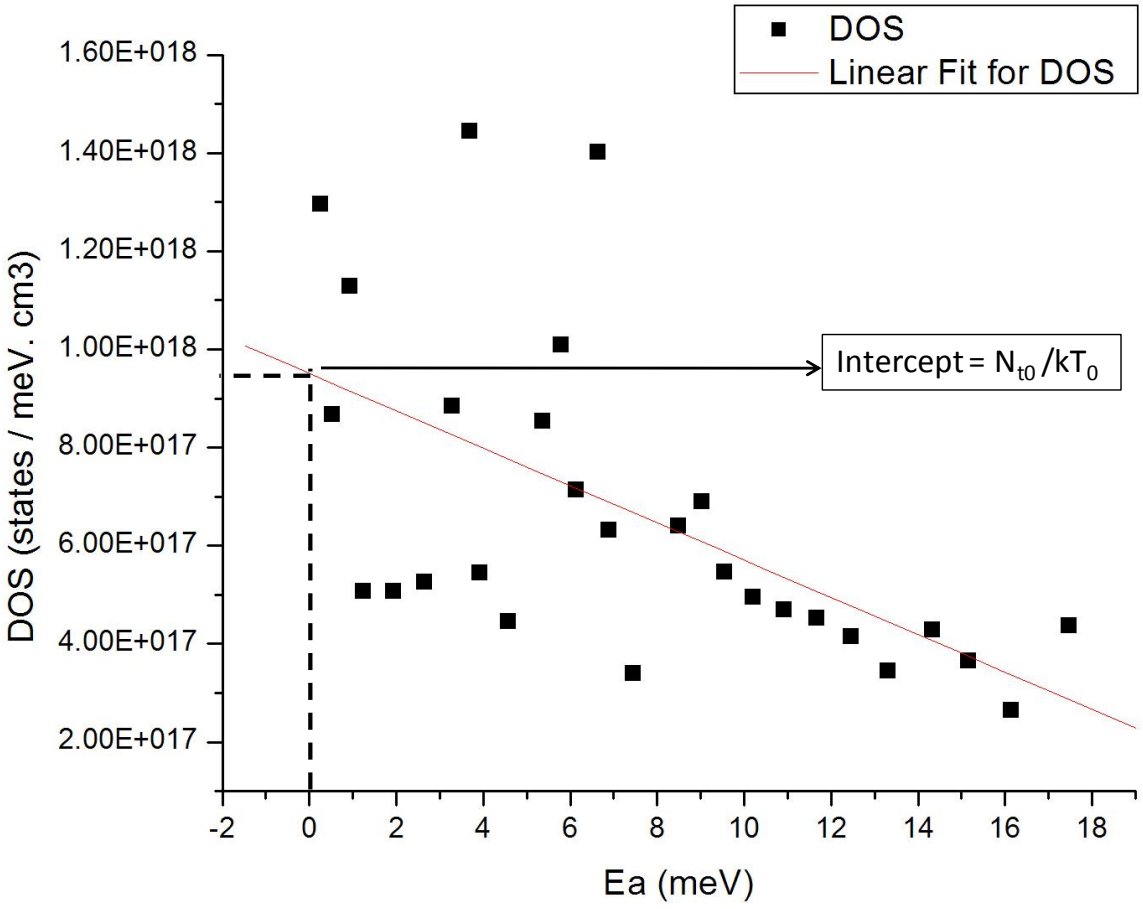


Figure 2.13 Linear fit for DOS as a function of Ea

Thus, the values obtained for N_{t0} and T_0 were:

N_{t0} = 1.26855e19 states /cm^3

T_0 = 159.36 K

These values were used as initial estimates to fit the expression in Eq. (2.21) to the temperature dependent experimental data for effective mobility. Fairly accurate fits were obtained over the temperature range of 77K – 333K (Figure 2.14 ,Figure 2.15, Figure 2.16).

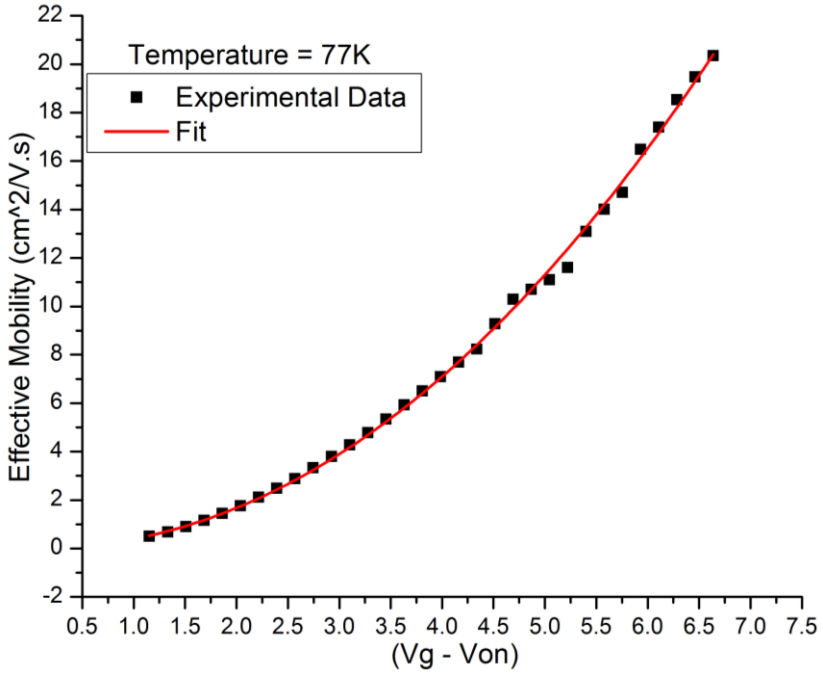


Figure 2.14 Effective mobility fit for data measured at temperature 77K

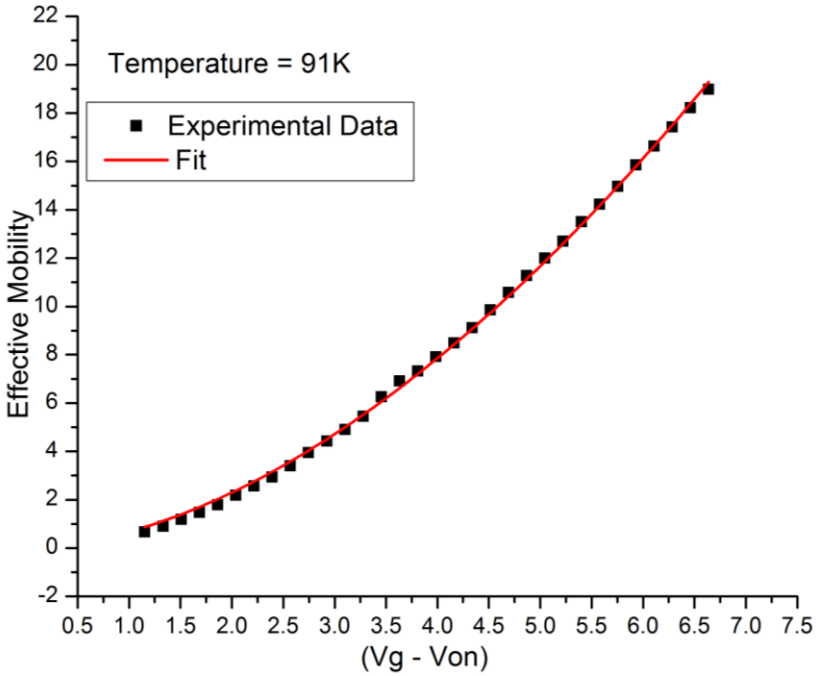


Figure 2.15 Effective mobility fit for data measured at temperature 91K

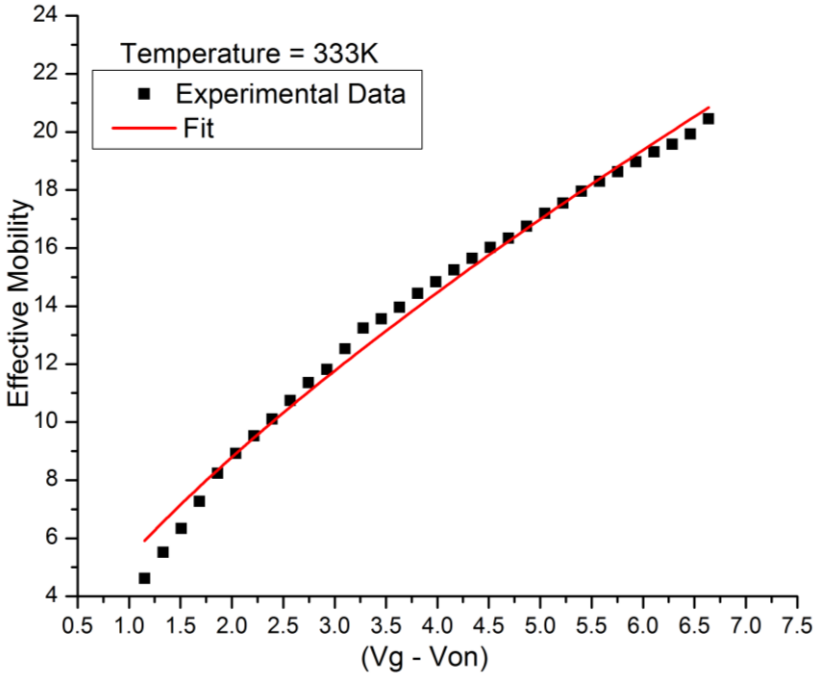


Figure 2.16 Effective mobility fit for data measured at temperature 333K

The fitting parameters obtained for the above plots are:

Table 2.2: Curve fitting parameters for effective mobility

T	N_{t0} (states/eV.cm^3)	T_0 (K)	$\mu_o.N_c$ (states/cm.V.s.eV)
77K	1.26855e19	237.51	2.634e22
91K	1.26855e19	252.377	1.2487e22
333K	1.26855e19	572.54	1.30285e21

Thus, it can be observed that the expression for effective mobility (Eq. (2.21)) gives fair fits for the temperature dependent experimental data. The fitting parameter values obtained from the above exercise are in resonable range of agreement with the initial estimates available for N_{t0} and T_0 (from the activation energy experiments).

The similarity in the form of the expression for effective mobility derived in section 2.4.3 to that of the emperical constants based expression used in RPI model (Eq. (2.7)) is evident. Similar expression obtained by Horowitz *et al.* [43] for OTFTs considering MTR mechanism, validates the approach used in this derivation. To devise a complete DC model and finally arrive at the small signal and dynamic model for ZTO TFTs, charge based approach adopted in [41] needs to be followed. However, VRH charge transport mechanism is assumed in [41]. This mechanism does not apply to ZTO TFT devices. Thus, the expression for conductivity needs to be revisited using the MTR model of charge transport (applicable at higher temperatures). However, that would be out of the scope of this thesis.

The simplifying assumptions made for arriving at the effective mobility of ZTO TFTs would be a source of inaccuracy in circuit simulations based on this model. Nevertheless, the resemblance of the effective mobility expression used by the RPI models to that obtained for the ZTO TFTs is significant for the purpose of this study. The RPI a-Si model [APPENDIX B: aSi_model], is thus chosen as a compact model for circuit simulations for ZTO TFTs.

Next chapter describes the EDA tool setup used for circuit design and laying out of these circuits using ZTO TFT devices. Circuits fabricated using these devices are discussed in the subsequent chapters.

CHAPTER 3

EDA Setup and Layout Details

There are multiple stages involved in the design flow that starts with circuit design and ends with the layout being sent out for fabrication. Different types of Electronic Design Automation (EDA) or Computer Aided Design (CAD) tools are required for each of these stages. Advanced CAD suits having integrated environment for all such stages, are available to designers these days.

For this study, two such suits were utilized: Cadence Design Environment and Tanner EDA. A combination of these tools was used to accomplish the design flow for ZTO devices/circuits.

3.1 EDA SETUP FOR ZTO DESIGN FLOW

Cadence Design Environment is widely used in industry and is well established for silicon design. The '*techlib'* is an extensive database format specific to Cadence that defines all aspects of technology required to setup the tool flow in EDA. Developing such database for a non – silicon and a relatively new technology process, which is still in developmental stage, is a cumbersome task. It requires in-depth knowledge of the Cadence EDA platform. Tanner EDA on the other hand offers comparatively easy and flexible interfaces to setup the flow for a new technology. Thus, a hybrid approach has been devised that combines the best features of both environments.

Cadence EDA's Spectre simulator provides sophisticated circuit simulation features, and is hence used for schematic level circuit design. The option of development of a compact model in VerilogA and direct integration of this model for circuit simulations is also a big advantage of using Cadence EDA [44]. Making layouts and performing extraction on these layouts for verification is quite convenient in Tanner EDA. Simple user interfaces are available in L-Edit – the layout tool of Tanner EDA, to define the new layers of the technology and also to set the DRC and extraction rules [45].

The complete design flow using the hybrid approach of Cadence and Tanner EDA is explained in the next section using inverter design as an example.

3.2 DESIGN FLOW FOR INVERTER USING ZTO DEVICES

3.2.1 Schematic design in Cadence

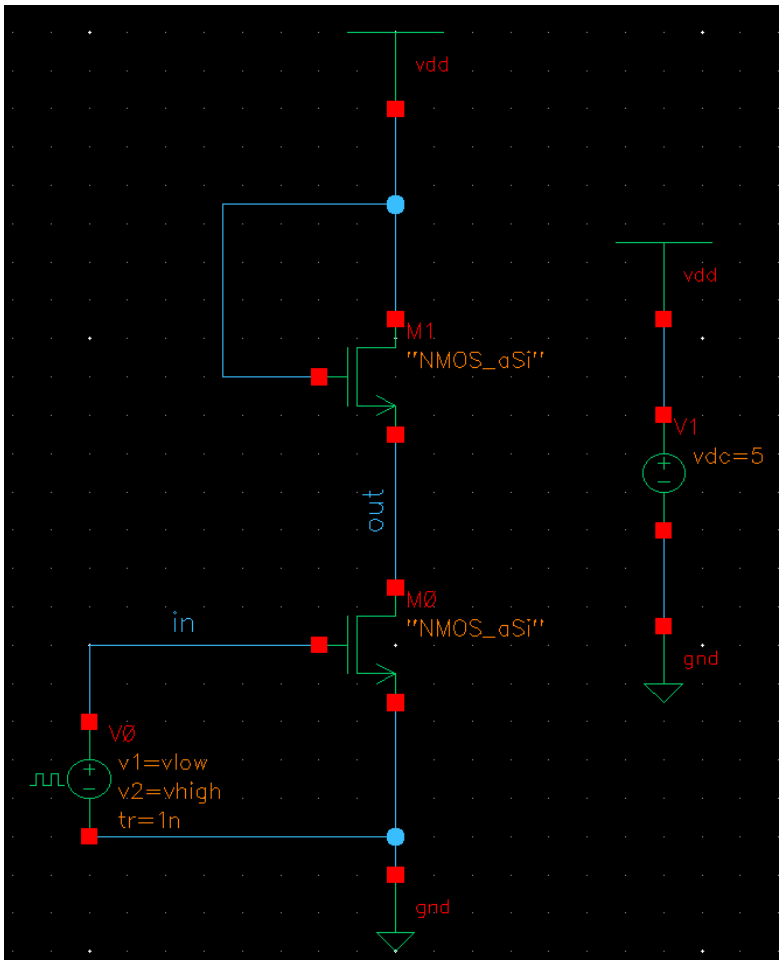


Figure 3.1 Schematic of an inverter in Cadence Schematic Editor

Firstly, a three terminal FET symbol is created in the Cadence Symbol Editor. The SPICE model file created for ZTO devices (APPENDIX B) is then associated with these devices. These FETs are further used to realize the inverter circuit in the Schematic Editor (Figure 3.1). Using Spectre simulator in Analog Design Environment (ADE), the

dimensions of the inverter are optimized to achieve the required I-V and transient characteristics. Once the design is fixed, the SPICE simulator is run in ADE to obtain SPICE netlist of this circuit.

3.2.2 Layout in Tanner EDA – Ledit

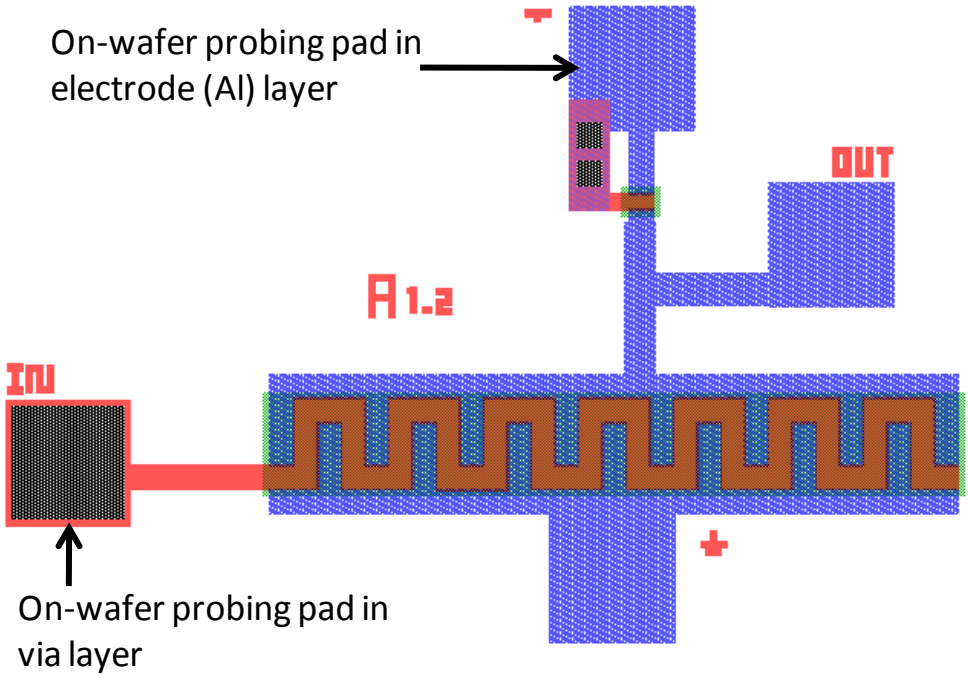


Figure 3.2 Layout of inverter in Ledit

Once the device sizes are finalized in the circuit design step, Tanner EDA Ledit (Layout Editor) tool is used for the layout. The different layers involved in layout and their required orientation for ZTO devices is explained in APPENDIX C. To conserve area, devices with bigger widths are preferably laid out using multiple fingers for the source and drain electrodes (Figure 3.3). Thick metal lines (25 μm – 100 μm) are used for interconnect routing. For on chip probing, (100 μm x 100 μm) pads are provided in via ('IN' pad in Figure 3.2) or electrode ('OUT', vdd and gnd pads in Figure 3.2) layers.

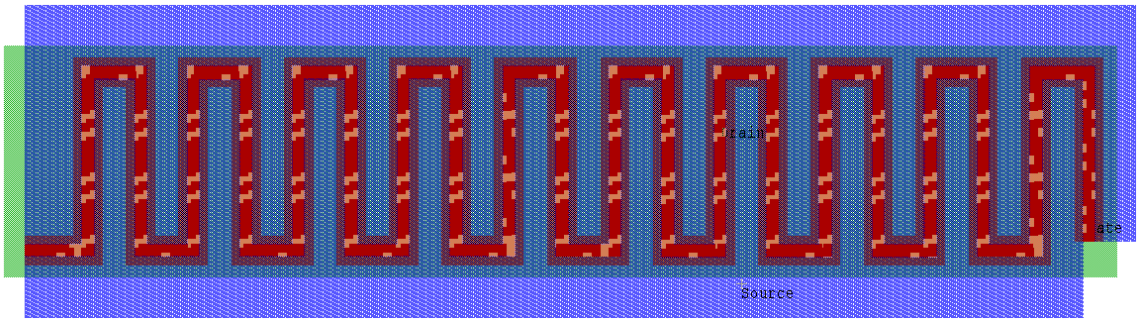


Figure 3.3 Layout of a multiple-fingers device with W=1000 μm and L = 3μm

Some circuit configurations require provisions to connect external components. Bigger pads (2 mm x 2 mm), in the electrode or via layer, are provided on the boundary of the wafer and connection to these pads is routed using thick (~ 100 μm) metal lines from the node of interest in the circuit. These boundary pads are separated by a minimum distance of 1 mm. This allows bonding of the surface-mounted components with silver epoxy between these pads.

Design Rule Check (DRC) feature is used to check for violation parameters like limits on spacing between layers, thickness of layers in the layout and enclosure of one layer by another. These limits are set by the fabrication process. Ledit provides a simple user interface to set these rules for DRC. Details of DRC command file used for ZTO layouts are included in APPENDIX D.

After all the DRC checks are cleared, extraction process is performed in Ledit. The extraction process converts the physical layout back into the circuit level netlist. Usually, circuit extraction involves a first level that extracts only the devices and their connectivity in the form of a netlist, while the second level extracts devices along with the parasitics that get added to the circuit due to physical characteristics such as interconnect resistances and capacitances. The netlist extracted in the first level, can be used to perform Layout Vs Schematic (LVS) verification. The LVS step verifies that all the intended devices have been physically realized in the layout and they are connected in the same configuration as in the schematic. The second level extraction is useful in post-layout processing like static timing analysis, signal integrity and power analysis.

Considering the unknowns involved in the developing process technology of ZTO devices, the extraction step has been restricted to the first level in this study. Details of the extraction definition file are included in APPENDIX D.

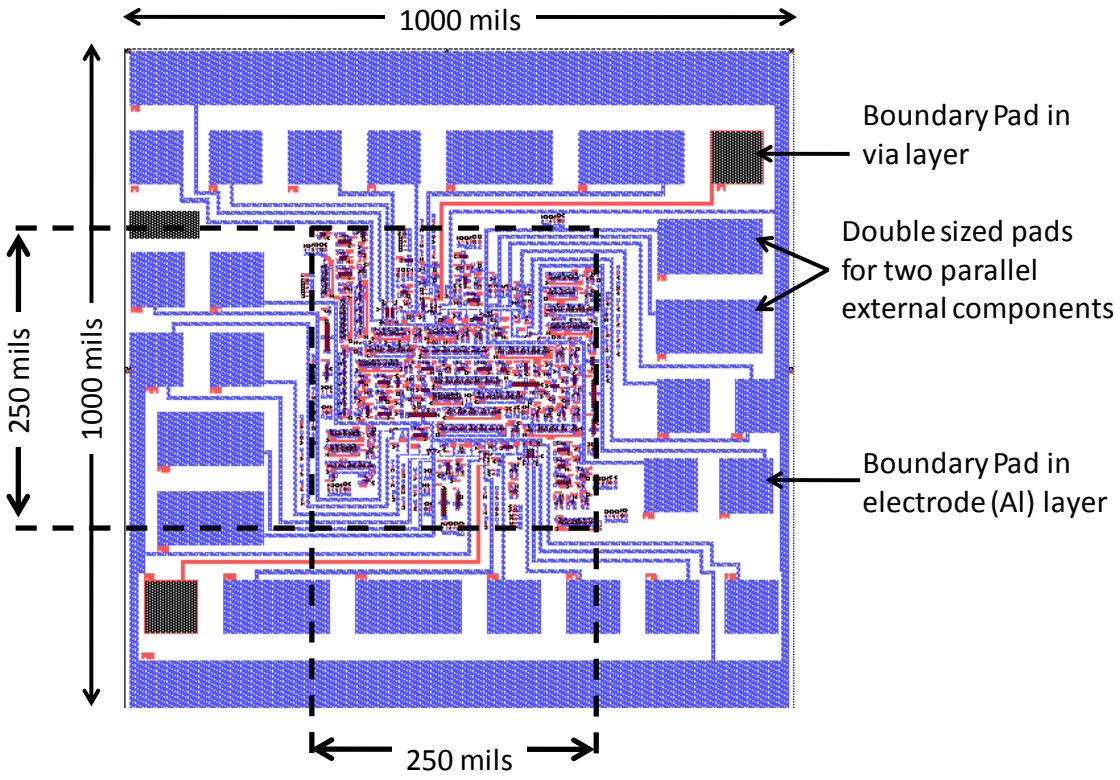


Figure 3.4 Layout of the entire wafer (Mask 3: gate electrode, source/drain electrodes, semiconductor and via layers combined) with boundary pads

3.2.3 Layout Vs Schematic (LVS) verification in Tanner EDA

The Layout Vs Schematic (LVS) verification is the last step of the design flow. The LVS tool of Tanner EDA is used to verify the netlist extracted from the layout in Ledit against the SPICE netlist obtained from Cadence Spectre. This step ensures one-to-one correspondence of devices and their connectivity, in the schematic netlist and the netlist extracted from layout.

After LVS, the four layers (gate electrode, SOURCE/DRAIN electrodes, via and active) are separated to form a (2000 mils x 2000 mils) or (2″ x 2″) layout (Figure 3.5). This layout is sent out to in DXF format for photolithography. The photomask obtained has features as chromium on glass substrate. The photomask is used to define desired features and align the layers during fabrication. Alignment marks are added in each layer (APPENDIX C) to assist the alignment process with an alignment tolerance of one micron.

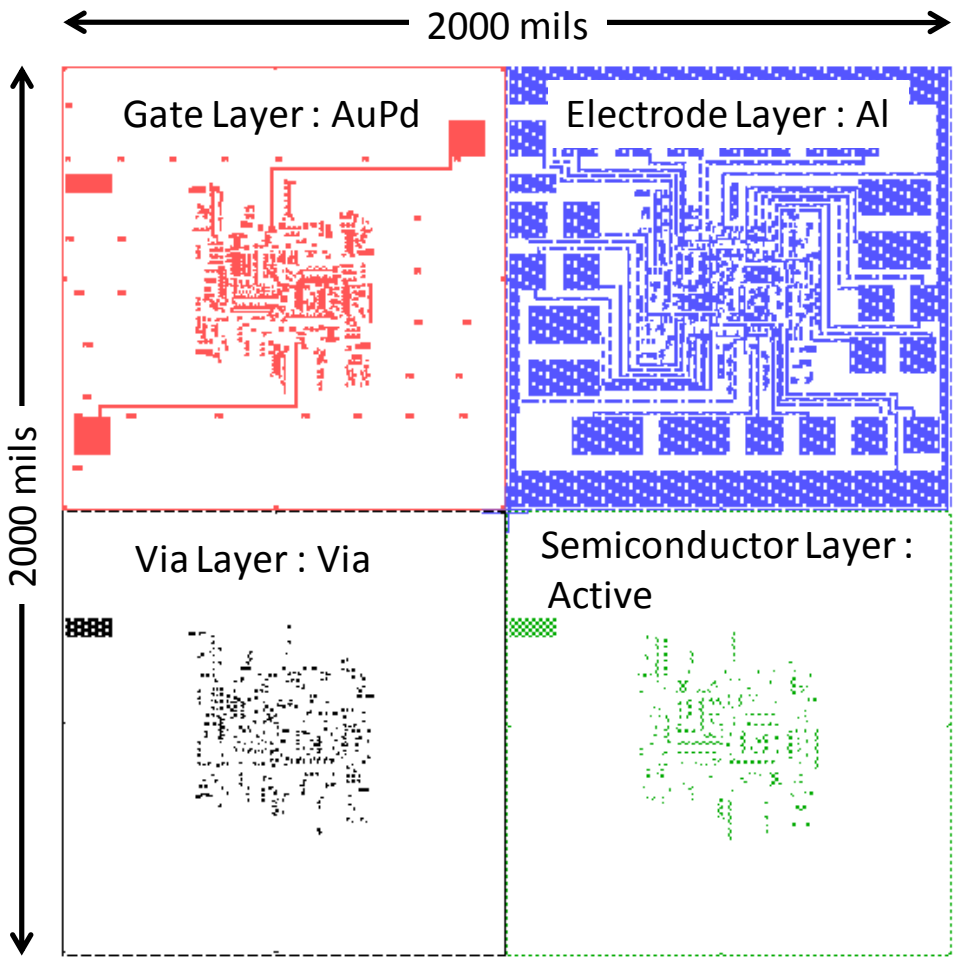


Figure 3.5 Layout of wafer (mask 3: gate electrode, source/drain electrodes, semiconductor and via) with 4 layers separated

A total of 4 masks were designed in the course of this study. The next section discusses the details of each of these masks.

3.3 MASKS DESIGNED FOR ZTO-BASED CIRCUITS

This section discusses the circuits included, main features and modifications, and the results obtained from each of the mask runs. Multiple copies of every circuit and device were placed at different areas in the mask, in order to achieve high probability of functional components in presence of process variations. This also assisted in studying the effects of non-uniform performance of the solution-processed ZTO film, especially towards the edges of the sample. All the devices and circuits included were numbered and labeled using the gate (AuPd) layer.

3.3.1 Mask1: Oscillators and Amplifiers

- Multiple copies of the following circuits were included in mask 1 layout
  - 13 different ring oscillators (one 3-stage, ten 5-stage and two 7-stage oscillators)
  - 13 inverters corresponding to single stages in the above oscillators
  - 4 different common source amplifiers (two with external load resistors and the other two with NMOS enhancement loads)
  - 1 cascode amplifier
  - Buffers as standalone and as part of oscillators
  - Single devices used for all the above circuits
  - Test structures to measure the capacitance values at different parts of the mask
  - Alignment marks to help with mask alignment issues during fabrication (APPENDIX C)
- Minimum channel length used was 3 μm.

- (2 mm x 2 mm) boundary pads were used in order to allow wire bonding of external resistors. All internal pads used for on-chip probing were 100 μm x100 μm (as illustrated Figure 3.2 and Figure 3.4).
- Gate overlap with source/drain was 1 μm. Semiconductor extended at least 5 μm beyond the channel boundaries (Figure 3.6)

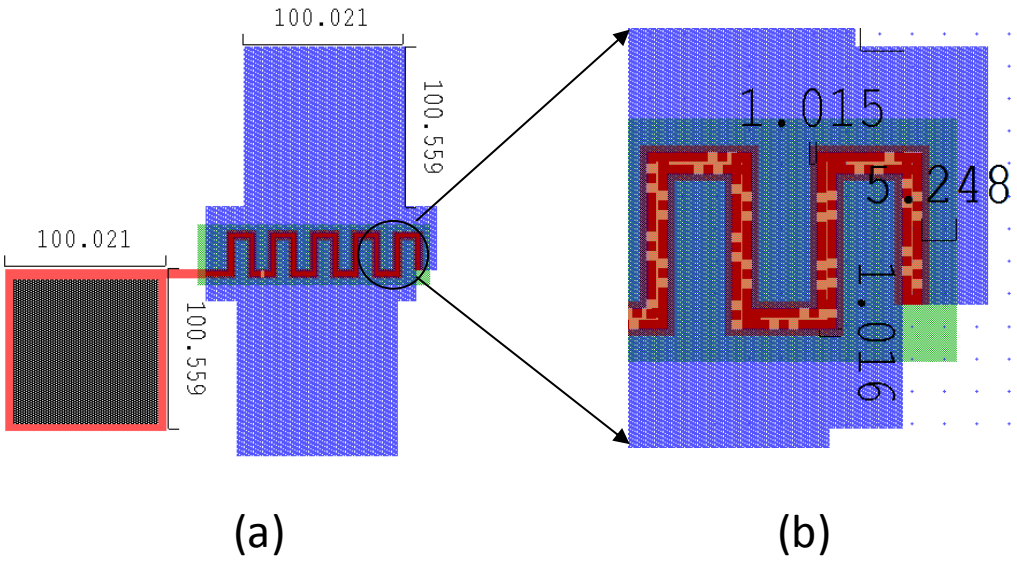


Figure 3.6 (a) An multiple fingers device with 100 μm X 100 μm internal pads, (b) Enlarged version of the device showing gate overlap of (1 μm) and semiconductor overlap of (5 μm)

This mask revealed a lot of uniformity issues in the lab tests. A lot of the components turned out to be ill-fabricated, due to broken or defective layers. The process was tuned to improve on these shortcomings.

In mask 1, a few inverters with reasonable output characteristics yet low bandwidth were successfully tested in the lab. A few enhancement load amplifiers exhibited a low-frequency gain of around 8-9 with a unity-gain bandwidth of around 5 kHz. These results are discussed in detail in Chapter 4.

3.3.2 Mask 2: OPAMP

The new addition in this mask was a multistage op-amp (discussed in Chapter 5) along with the basic circuit blocks built in the previous mask. To study the cause of the non-uniformity observed in mask 1, different layout configurations for devices were tried out in this mask. Sharp spikes were observed in the gate electrode near the edges of source/drain overlap in some of the devices fabricated in mask 1. This was thought to be an effect caused by the photolithography and lift-off steps performed on the gate layer. Devices with wider gate to source/drain overlaps were laid out to counter this effect. Devices with patterned semiconductor layer were also included in the mask to check for spreading current effects. The features of this mask were:

- 2 copies of a 3 stage modified Gray OPAMP (is the S-M OPAMP discussed in Chapter 5). Layout of the OPAMP was designed such that each of the 3 stages could be isolated and tested separately by scratching thin metal lines provided as part of the connection between stages.
- Minimum channel length was kept at 3 μm
- All single devices, common source amplifiers and oscillators were laid out in three different configurations (Figure *3.7*) – gate to source/drain overlap of 1 μm, gate to source/drain overlap of 2 μm, and gate to source/drain overlap of 2 μm along with patterned semiconductor – to identify the optimum configuration.

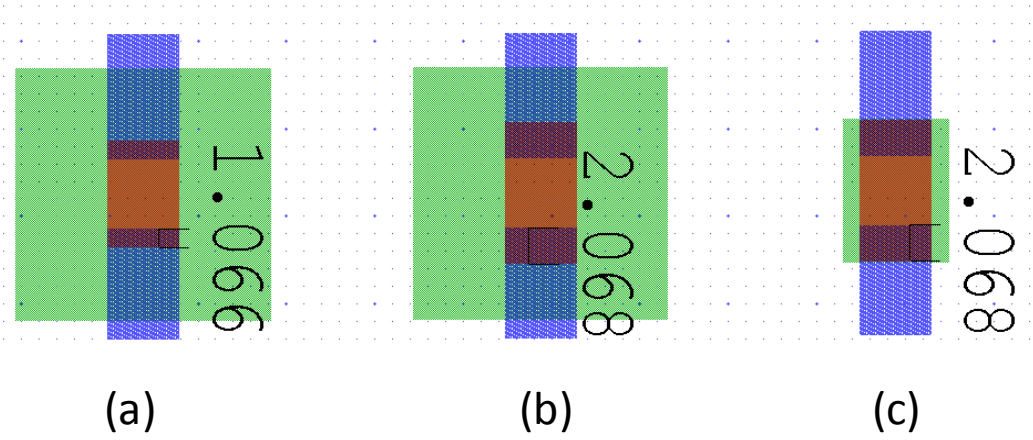


Figure 3.7 Layouts from mask 2 showing the device (W = 4 µm, L = 4 µm) laid out in three configurations: (a) overlap of 1 µm, (b) overlap of 2 µm, and (c) overlap of 2 µm with patterned semiconductor

The experimental data from mask 2 showed that having higher overlaps helped to improve the overall uniformity, even though the performance remained very similar (average mobility values of around 2 $cm^2/V.s$ were observed). The mask had more functional inverters and amplifiers due to the better uniformity in layout. DC-gains of around 8 were consistently observed for the NMOS enhancement load CS amplifiers. But the deposition of ZTO film was not uniform enough for the OPAMPs and oscillators to work.

Patterned semiconductor devices exhibited much lower tunneling gate currents (I_{gs}) compared to their unpatterned counterparts. This reinforced the assumption that patterning of semiconductor layer reduces the spreading currents. Larger the semiconductor film area, more is the spreading of accumulation charges in the film. This increases the probability of tunneling of these carriers to the gate through defects in the film. This phenomenon is known as spreading currents.

3.3.3 Mask 3: OPAMP with Extended Gate Configuration I

To counter the uniformity issues from mask 2, all devices in mask 3 were designed with an extended gate configuration. The gate was extended by a minimum of

2 μm beyond the source and drain on all sides, thus increasing the overlap between gate and source/drain electrodes (Figure 3.8). This provided a more uniform surface for the deposition of the ZTO film. The minimum channel lengths for all devices were also increased to 4 μm to enable easier fabrication.

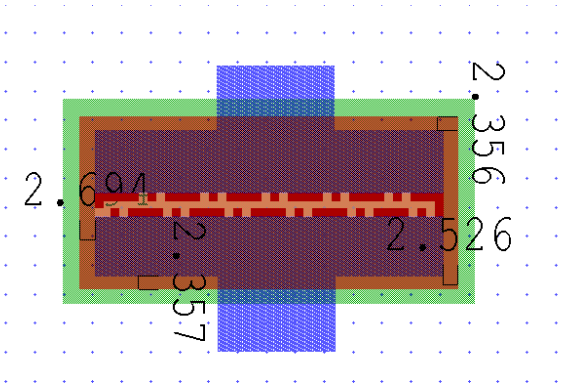


Figure 3.8 Snapshot of a device in mask 3 laid out with an extended gate

- The opamp, oscillators, amplifiers and inverters from mask 3 were laid out with extended gate configuration and multiple copies were included.
- Inverters with channel lengths 12 μm, 15 μm, and 20 μm, with aspect ratio (W/L > 10) were added to observe the variations in device performance with respect to channel lengths.
- Devices with 4-point probe configuration having channel lengths of 100 μm and 50 μm were added to gauge the contact resistance experienced by ZTO devices (Figure 3.9). A known voltage was applied on the source and drain electrodes of this device. The resultant current and the effective voltage drop across the channel were measured using the voltage probe pads. The contact resistance value was then calculated as the difference between the overall resistance (voltage between source and drain over the drain current) and the channel resistance (voltage between the probes divided by the drain current).

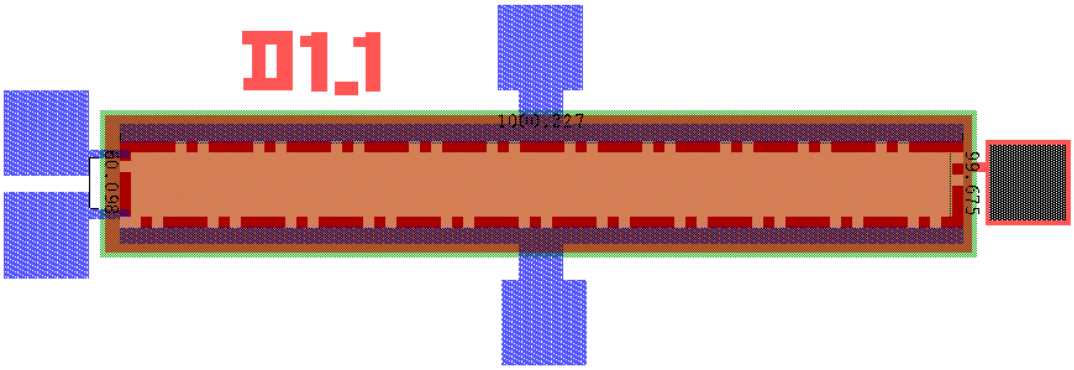


Figure 3.9 Device with 4-point probe configuration from mask 3 (L = 100 μm, W = 1000 μm, probe thickness = 10 μm, probe distance from channel edge = 10 μm, distance between probes = 60 μm)

The extended-gate configuration helped to tackle the uniformity issues observed in the earlier masks and improved the overall device performance (average mobility of around 5 $cm^2/V.s$). Most of the single stage amplifiers and inverters had a dc-gain close to 10. The improved uniformity was demonstrated best by the functioning of several ring oscillators, out of which best performance was shown by a 7 stage ring oscillator which operated at a frequency of 106 kHz and an output swing close to 3V with a 14V supply voltage. The op-amp was tested in individual stages and the output stage (common source + buffer stage) was verified to provide a gain of around 3. However, the first and second stages of the OPAMP could not be tested as the thin aluminum connections (5 μm in width) at metal crossings got burnt out on passage of current. This was attributed to the thin deposition (~ 50 nm compared to the usual of ~100 nm) of the Al layer during this fabrication cycle.

3.3.4 Mask 4: OPAMP with Extended Gate configuration II

Since the extended gate configuration improved the device performance in mask 3, the gate was extended even further out for the devices designed in mask 4 (Figure 3.10). The gates were extended 50 μm beyond the source/drain boundary, while the width of the fingers was reduced to 5 μm. This was done to reduce the total overlap between the

gate and source/drain electrode electrodes that corresponds to the overlap capacitance. The functional 7-stage ring oscillator from mask 3 was laid out, along with its 50 μm extended and 100 μm extended gate versions to study the relative improvement in performance with respect to the increased gate area. All the circuits, including the OPAMP, oscillators and inverters were redesigned for optimum performance based on the modified a-Si model (discussed in Chapter 4 and 5). Buffers were designed for all the oscillators to prevent against output loading that affects the output swing. Specific devices were also designed and laid out for measuring contact resistance.

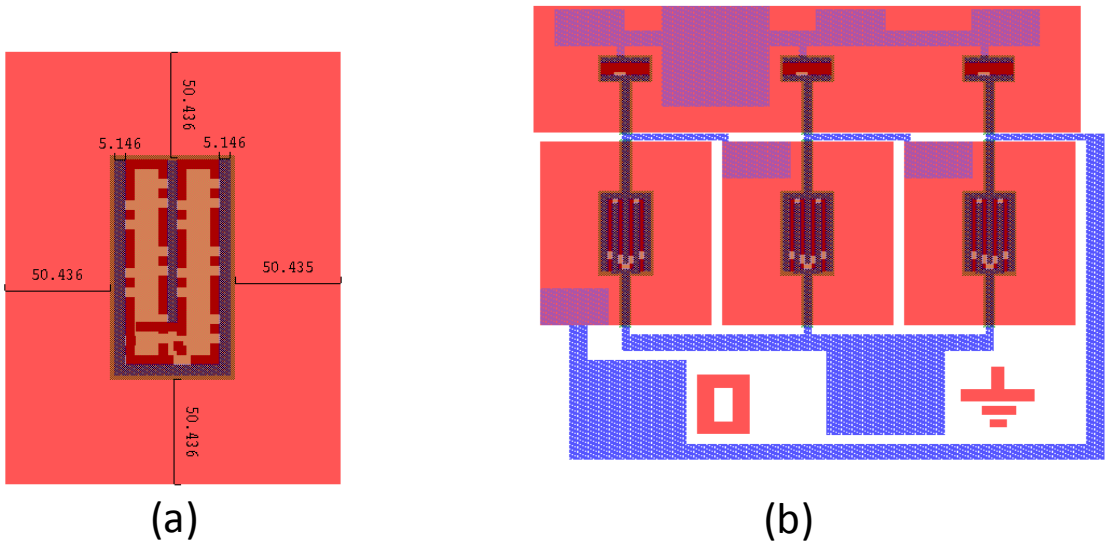


Figure 3.10 (a) A device from mask 4 with 5 μm source/drain widths and 50 μm extended gate, (b) 3-stage ring oscillator

- Multiple copies of the following devices were included in mask 4
  - Two copies of a modified a-Si model based 3 stage OPAMP with an output buffer stage
  - 8 different ring oscillators with provision to disconnect the buffer stages (one 3-stage, three 5-stage, two 7-stage, one 100 μm extended gate 7-stage and one 7-stage from mask 3)

- 3 enhancement load amplifiers
- Devices of varying channel lengths with a constant aspect ratio of 10 to estimate contact resistance (devices with L = 4 μm, 8 μm, 12 μm, 20 μm, 30 μm, 60 μm and 80 μm). The overall resistance would be measured for each device. The y-intercept of the plot of resistance versus length (resistance for channel length = 0) would give an estimate of the contact resistance value for ZTO devices.
- Devices with 4-point probes having a channel length of 100 μm were also included as an alternative method to measure contact resistance (probe thickness = 5 μm, distance of probe from channel edge = 5 μm, effective distance between probes = 80 μm).

This mask is currently under fabrication and would be tested in lab soon.

Design of basic circuit blocks for ZTO devices is discussed in the next chapter.

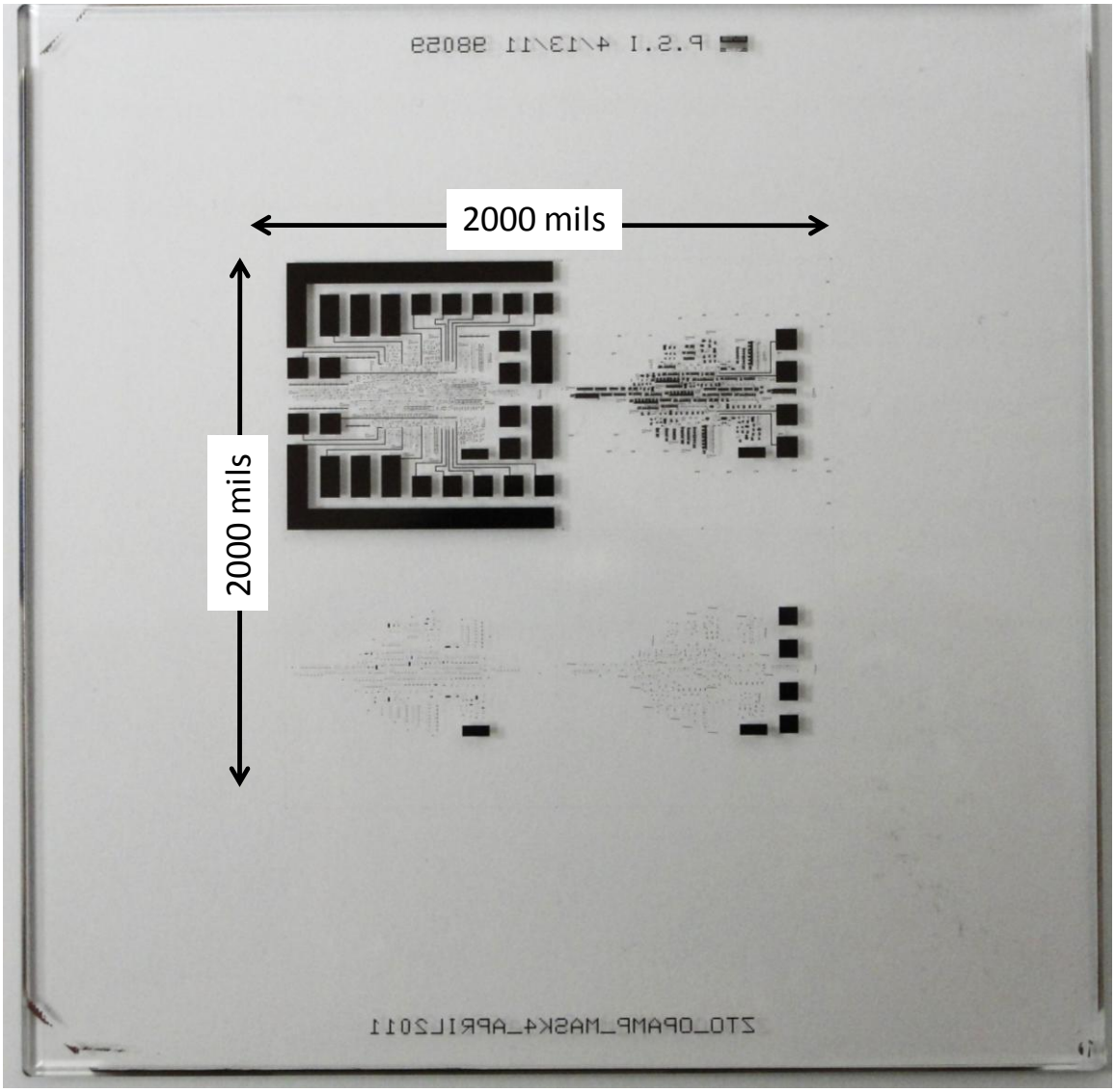


Figure 3.11Photomask of mask 4

CHAPTER 4

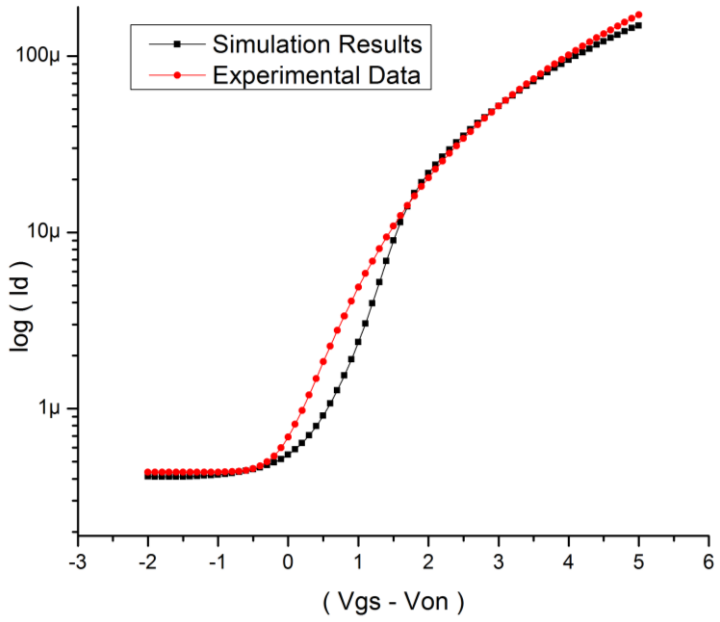
ZTO TFT Based Circuits

Exploring the possible circuit applications of a new technology is an essential step towards evaluation and validation of the proposed process.

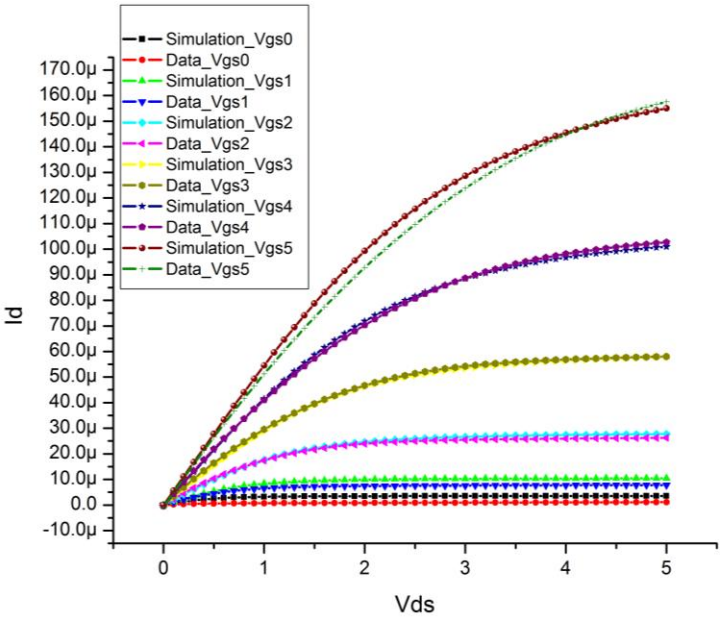
In this study, basic building blocks of circuit design, namely: inverters, ring oscillators and amplifiers were designed using enhancement mode n-channel ZTO TFTs. This chapter elaborates the design process of these circuits and compares the simulation results against the experimental results obtained from the lab tests. This comparison helps in understanding the accuracy of the device model used for simulations during circuit design. The improved performance of circuit blocks over revisions of the design flow enhances the possible application of the solution based ZTO TFT devices in wide range of electronics.

4.1 CIRCUIT SIMULATIONS

The SPICE Level 1 MOSFET model [APPENDIX B: SPICE Level 1 MOSFET model] was used for circuit simulations during first two design cycles. In chapter 2, it was illustrated with the help of experimental data that these models had low level of accuracy when applied to ZTO TFTs. Thus, the modified RPI a-Si model [APPENDIX B: Amorphous – Si TFT model], fit to the I-V curves of ZTO TFT devices was used for simulations in the subsequent design cycles. Figure 4.1 (a) and (b) illustrate these fairly accurate fits obtained for I_d-V_{ds} and I_d-V_{gs} curves of a ZTO device.



(a)



(b)

Figure 4.1 Comparison of simulation results using modified RPI a-Si model and experimental data obtained for the device (W/L = 80 µm/4 µm): (a) I_d-V_{gs} curve, (b) I_d - V_{ds} curve

The next section presents circuit designs using ZTO TFTs and discussion of results obtained for inverters, ring oscillators and amplifiers.

4.2 CIRCUIT DESIGN AND VERIFICATION OF SIMULATION RESULTS

4.2.1 Inverters

Inverters are the basic building blocks in digital and analog circuit design. Inverters fabricated using high vacuum deposition of ZTO have been reported previously [6-7] . A solution processed ZTO devices with issues like low static gain and non-uniform performance have been reported in [46].

Several inverters with diode connected enhancement loads were designed and fabricated using the solution based ZTO TFT devices. The voltage transfer characteristics curves obtained for these inverters were used as a metric to gauge the uniformity of this process. Inverters with different aspect ratios (W_{driver} / W_{load}) were designed to study the effect of scaling on their DC characteristics.

Figure 4.2 is an instance of an inverter fabricated in mask 3. The voltage transfer characteristics and dc gain plots obtained for this inverter are presented in Figure 4.3.

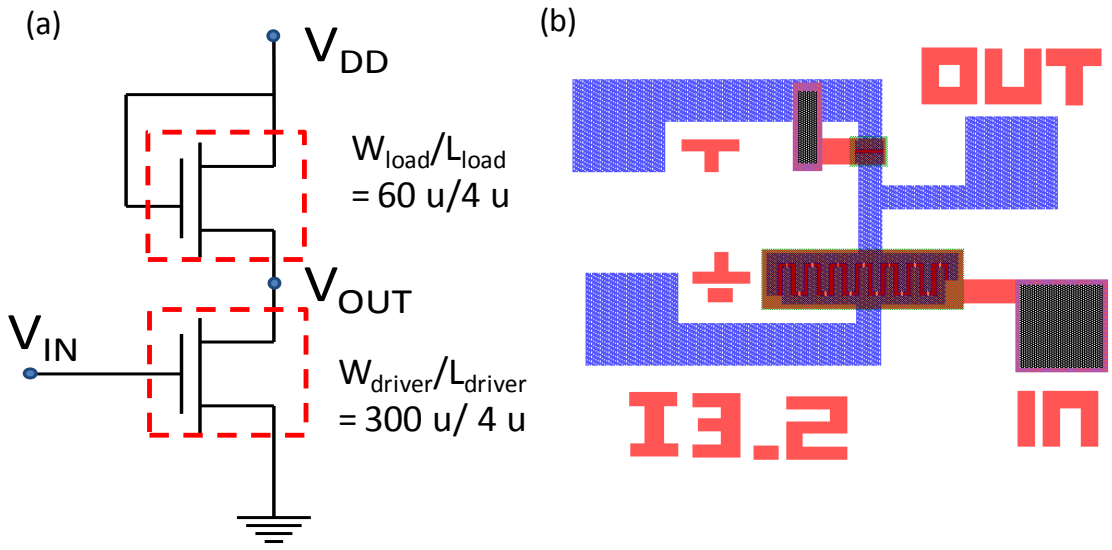


Figure 4.2 Inverter (I_3) from mask 3: (a) Schematic, (b) Layout

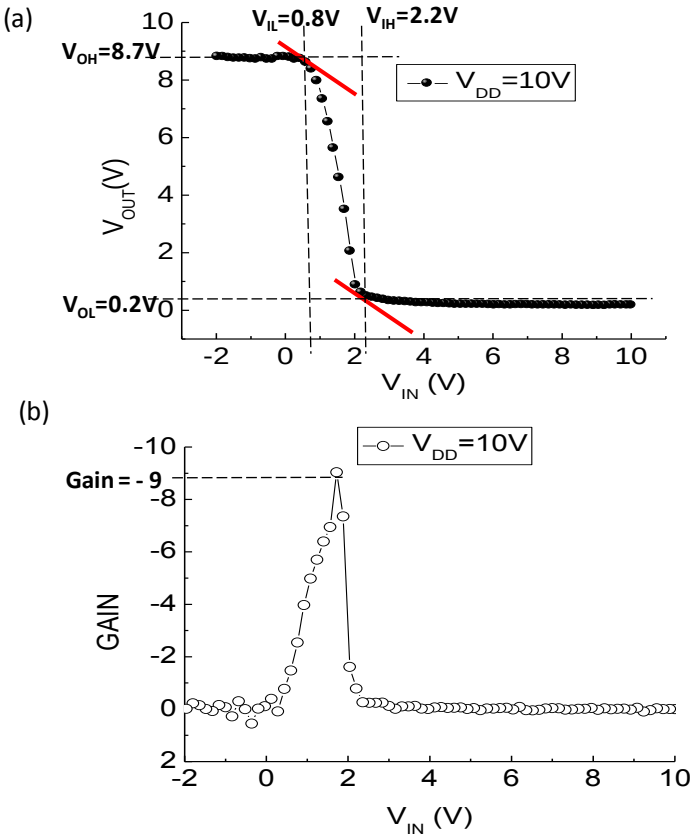


Figure 4.3 Results obtained for inverter I_3: (a) Voltage transfer characteristics, (b) DC gain

The measurement results obtained for inverter I_3 operated at a supply voltage of 10 V show a DC or static gain of around -9 (180^o phase inversion) (19 dB) and an output swing of 8.5 V. The static noise margins obtained can be observed in Figure 4.3 (a). The noise margin for low input is,

$$NM_L = V_{IL} - V_{OL} = 0.6 \text{ V}$$

and noise margin for high input is,

$$NM_H = V_{OH} - V_{IH} = 6.5 \text{ V}$$

Thus, reasonable static gain and noise margins can be obtained from n-channel enhancement load inverters designed using ZTO devices.

4.2.2 Amplifiers

Voltage amplification is probably the most common and yet one of the most important operations in analog circuits. The basic building block of voltage amplifiers is a common source (CS) amplifier. A TFT, like a MOSFET, would convert the variation in its gate-source voltage into small variations in the drain current. This property called as 'transconductance' and denoted as 'g_m' is the essence of a CS amplifier.

Quite a few CS amplifiers were designed during each design cycle, including passive load (external resistance) and active load (diode connected n-channel enhancement mode ZTO TFT) configurations. The passive load configuration was used to provide more control over the DC operating of the amplifier in presence of variations in parameters like charge mobility (more elaboration of this point in Chapter 5). Some cascode amplifiers were also designed and tested using ZTO TFT devices.

A CS amplifier is essentially an inverter designed to have a sharp transition region in the voltage transfer characteristics and is operated at an input DC voltage lying approximately midway in the transition band of this characteristics. This choice of DC voltage keeps the driver device in saturation hence, providing maximum g_m and output resistance r_o which results in maximum voltage gain. The expression for voltage gain obtained for a CS amplifier is shown in Figure 4.4. The design process of CS amplifiers involves, optimizing the dimensions of the driver and load devices in order to get high g_{m1} (larger width) and at the same time maintain the bandwidth of operation (limited by larger parasitic capacitances of larger widths) without affecting the stability of the system (phase). In case of ZTO TFTs, the value of g_m is inherently low, which is attributed to the low carrier mobilities observed in these devices. Thus, it is relatively difficult to obtain a high voltage gain from ZTO TFT based amplifiers as compared to bulk MOSFETs.

Figure *4.5* (a) shows the optical image of the amplifier fabricated in mask 2. The transient voltage response (Figure *4.5* (b)) is obtained by applying a small ac signal of amplitude 350 mV (peak-to-peak), frequency 1 kHz and of DC offset of 1.8 V. The voltage gain (low frequency) observed from this response is around 7 (~16 dB). The

frequency response obtained for this amplifier is shown in Figure *4.5* (c). The unity gain bandwidth is measured to be ~10 kHz.

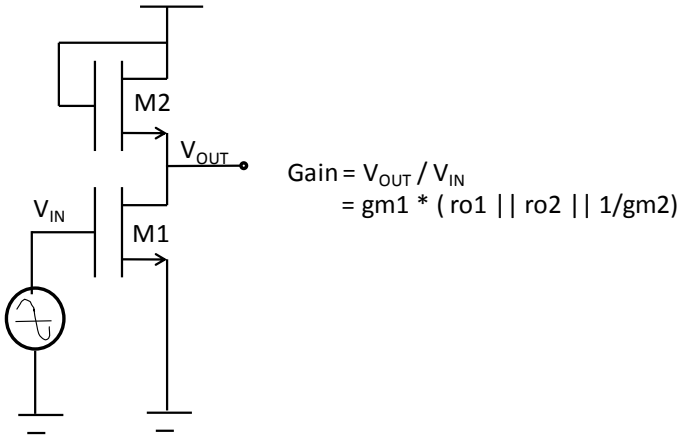


Figure 4.4 Schematic of a CS amplifier with its gain expression

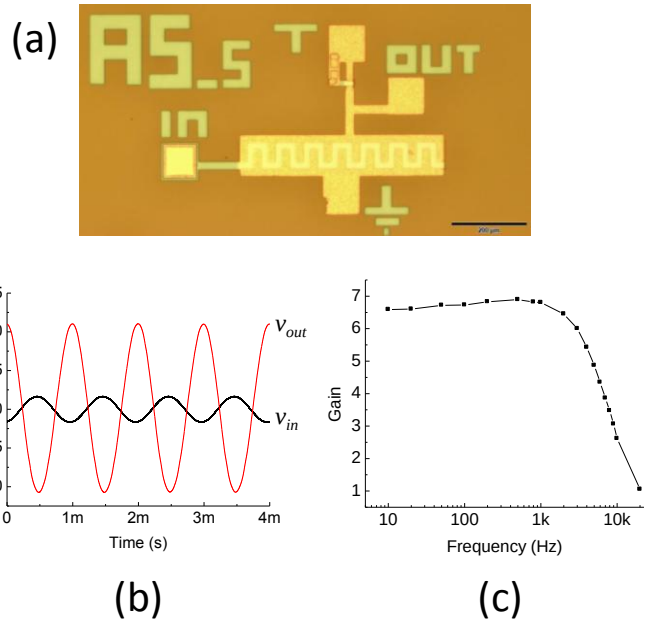


Figure 4.5 CS amplifier (Driver: W/L = 1000u/18u, Load: W/L = 20u/12u): (a) Optical image from mask 2, (b) Output and input transient Voltages , (c) Frequency response

4.2.3 Ring Oscillators

A ring oscillator is a cascade of odd number of inverters with the output of last stage fed back to input of the first stage. Each inverter stage provides a gain (> 1) that amplifies the noise in the circuit until sustained oscillations are obtained at each node. Thus on application of a supply voltage, a ring oscillator would generate fixed frequency oscillations at its output node (after steady state is reached). The frequency of oscillation is a function of the number of inverter stages and the individual delay of each stage. The two conditions required for sustained oscillations are (i) closed loop gain of 1 and (ii) phase shift of 180^o around the loop. The expression of minimum gain of each inverter stage for sustained oscillations is given as:

$$A_o = \sqrt{1 + \tan(\frac{180}{N})^2} \qquad (4.1)$$

In this study, numerous 3, 5 and 7 stage ring oscillators were designed and fabricated. All the inverter stages were identical and the gain of each inverter was designed according to the Eq. (4.1). Figure 4.6 shows the schematic of a 7 stage ring oscillator. The lab measurements for the best performing 7 stage oscillator are presented as an illustration (Figure 4.8).

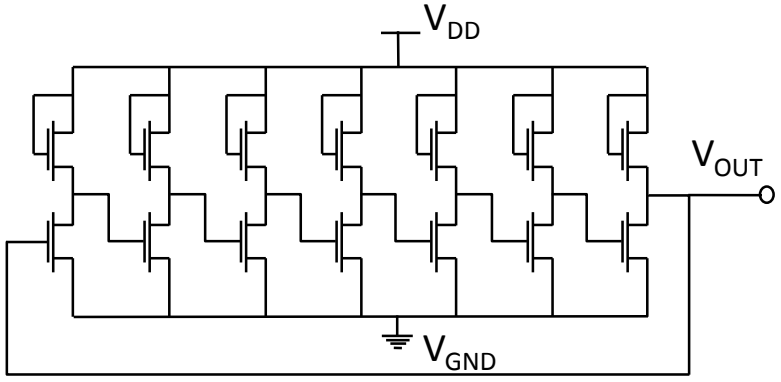


Figure 4.6 Schematic of 7 stage ring oscillator

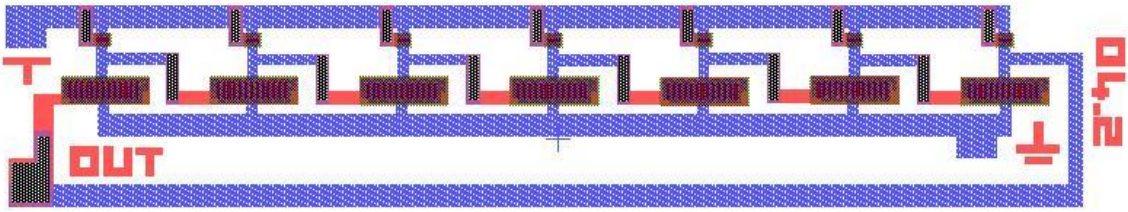


Figure 4.7 Layout of 7 stage oscillator (O_4) from mask 3 (Inverter stage: Driver W/L = 600u/4u, Load W/L = 30u/4u)

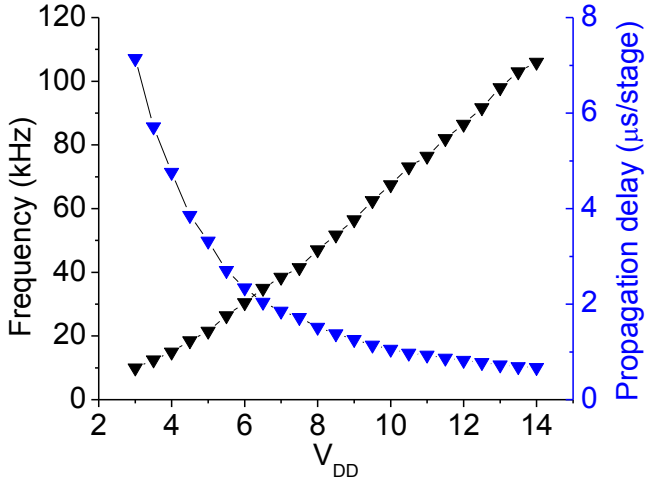
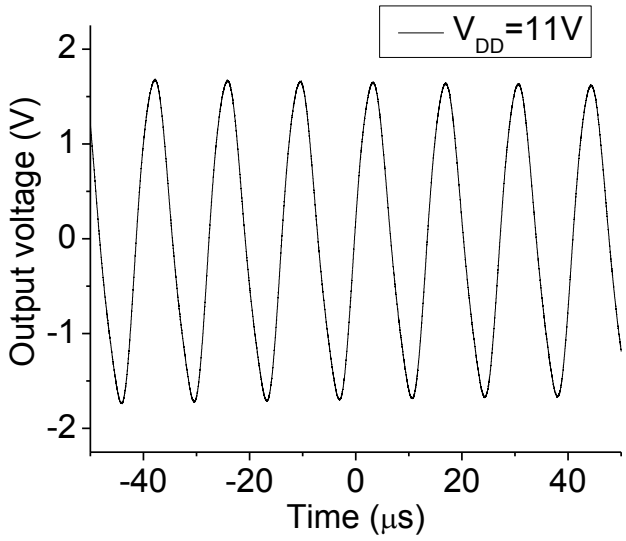


Figure 4.8 Oscillation frequency and stage delay as a function of supply voltage measured for the 7 stage oscillator O_4 from mask 3

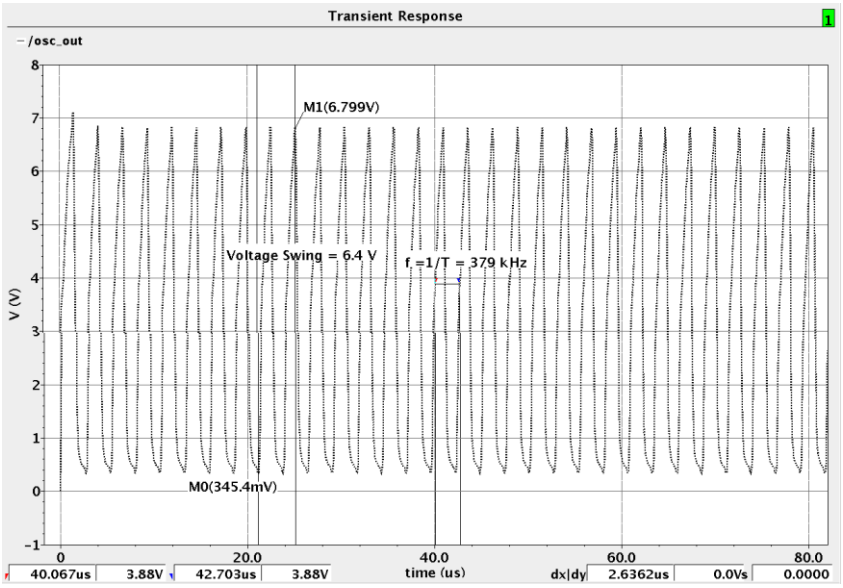
To get a comparative picture, the plot of experimental data and the simulation results obtained using SPICE Level 1 model and those obtained using the RPI a-Si model have been illustrated in Figure 4.9. It is evident from this comparison that the modified RPI a-Si model is a fairly accurate predictive model for the circuit design using ZTO TFT devices.

To avoid loading of the output node of the ring oscillator by the measurement setup, a picoprobe is use to measure the response of the ring oscillators. The picoprobe has a very small input capacitance (0.1 pF) and reasonable input resistance (1 MΩ).

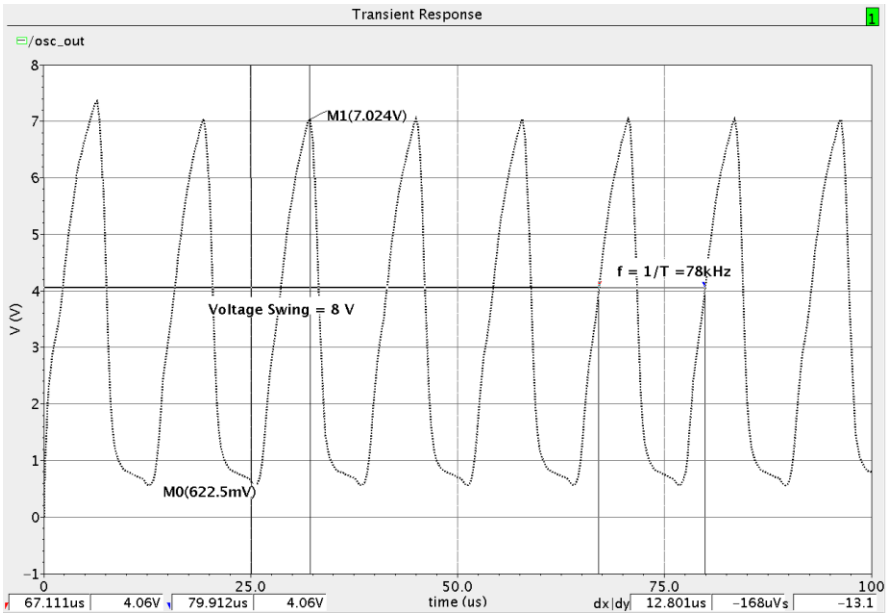
The difference in simulated and measured voltage swing of the oscillator from Figure 4.9 could either indicate process variations or loading the output node of the oscillator by some unknown source in the measurement setup. To eliminate the possibility of loading of the oscillator, buffer stages (two inverters) were designed for all the oscillators in mask 4.



(a) Measured Frequency= 76.5 kHz



(b) SPICE Level 1 simulated Frequency= 379 kHz



(c) RPI a-Si simulated Frequency= 78 kHz

Figure 4.9 Comparison of results obtained for 7 stage ring oscillator O_3 from mask 3 operated at VDD = 11 V: (a) Measured data (Freq. = 76.5 kHz, Volt. Swing = 3.9 V), (b) SPICE Level 1 simulation (Freq. = 379 kHz, Volt. Swing = 6.4 V), (c) RPI a-Si simulation (Freq. = 78 kHz, Volt. Swing = 8 V)

4.3 CIRCUITS UNDER TEST

Following is a listing of the active load amplifiers and ring oscillators designed for mask 4. The sizing and other dc operating point parameters have been listed to illustrate the effect of each of these on the specifications achieved in simulations. The effect of variations in mobility values and external control achieved by varying the supply voltage is also presented through these tabulations. Currently this mask is under fabrication and would be tested soon.

Table 4.1: Design parameters, external parameters and specifications met in simulations for Active Load Amplifiers in mask 4

Amplifier Dimensions (μm)	*gm_1*	*ro_1*	*$1/gm_2$*	*ro_2*	*Mobility (cm^2/V.s), Vdd (V) , I_d (uA)*	*3dB Frequency*	*G ain (V/V)*
Driver: 500/4 Load: 100/20	84u	1.5M	0.09M	0.6M	Mob = 4, Vdd =7, I_d = 16	125kHz	6.33
	112u	5M	0.08M	0.57M	Mob = 4, Vdd =10, I_d = 39	163kHz	7.43
Driver: 500/4 Load: 40/4	147u	0.32M	0.042M	0.32M	Mob = 4, Vdd =7, I_d = 63u	292kHz	4.96
	137u	5M	0.05M	0.36M	Mob = 4, Vdd =10, I_d= 51.5u	286kHz	5.72
Driver: 1000/20 Load: 80/12	37u	1.37M	0.23M	1.6M	Mob = 4, Vdd =7, I_d= 12u	33kHz	6.64
	63u	2.41M	0.17M	1.25M	Mob = 4, Vdd =10, I_d = 23u	44kHz	8.79
Driver: 200/4 Load: 20/12	34u	2M	0.24M	1.7M	Mob = 4, Vdd =7, I_d = 11u	144kHz	6.64
	57u	3.4M	0.17M	1.3M	Mob = 4, Vdd =10, I_d = 21u	185kHz	8.53

Table 4.2: Design parameters, external parameters and specifications met in simulations for Ring Oscillators in mask 4

Ring Oscillator	*Single stage gain*	*Mobility (cm^2/V.s), Vdd (V) , I_d (uA)*	*Frequency*	*Voltage Swing*
Dr: 300/4 **Ld: 40/12** **Stages: 3** **Required gain: 2**	3.15	Mob = 4, Vdd =5, I_d = 35	200kHz	0.7V
	3.41	Mob = 4, Vdd =10, I_d= 65	250kHz	1.4V
	2.98	Mob = 10, Vdd=10, I_d= 157	500kHz	1.29V
Dr: 180/4 **Ld: 60/8** **Stages: 5** **Required gain: 1.23**	1.67	Mob = 4, Vdd =5, I_d = 127	337kHz	3V
	1.47	Mob = 10, Vdd =10, I_d = 252	500kHz	2.52V
	1.44	Mob = 10, Vdd =15, I_d = 544	581kHz	3.22V
	1.28	Mob = 20, Vdd =15, I_d = 958	900kHz	1.27V
Dr: 600/4 **Ld: 60/12** **Stages: 5** **Required gain: 1.23**	4.12	Mob = 4, Vdd =10, I_d= 100	100kHz	4.4V
	2.38	Mob = 10, Vdd =10, I_d = 439	270kHz	3.65V
	1.67	Mob = 10, Vdd =15, I_d = 917	312kHz	3.36V
Dr: 400/4 **Ld: 80/20** **Stages: 5** **Required gain: 1.23**	3.67	Mob = 4, Vdd =10, I_d= 79	90kHz	3.67V
	3.12	Mob = 10, Vdd =10, I_d = 189	200kHz	3.78V
	2.12	Mob = 10, Vdd =15, I_d = 417	251kHz	5.64V
	1.78	Mob = 20, Vdd =15, I_d = 753	400kHz	4V
Dr: 600/4 **Ld: 30/4** **Stages: 7** **Required gain: 1.11**	2.15	Mob = 10, Vdd =15, I_d = 271	91kHz	8.3V

CHAPTER 5

OPAMP Design Using ZTO Devices

The Operational Amplifier or OPAMP is a basic building block of analog circuit design. Currently the most important application areas for amorphous and organic semiconductor materials are large area displays and sensors. These rely on high-performance CMOS technology for the analog interface. A high gain amplifier is an essential block of this interface for performing operations such as signal processing in sensor applications and driver circuitry for display arrays. A point worth noting here is that these are mostly low frequency applications. If these peripheral components are implemented using organic / amorphous semiconductors, the manufacturing costs would reduce considerably. The characteristics that limit the use of amorphous and organic semiconductors in building such analog blocks are: low mobility, device-to-device variations, lack of complementary devices and limited corner frequency (f_T).

A technique to boost the load impedance of an a-Si NTFT using positive feedback, has been proposed in [47]. High voltage gain is achieved by using this high impedance element as load in an amplifier. A two stage OPAMP implementation using this gain boosting technique in a-Si technology and use of this OPAMP to build a 4bit DAC has been reported in [48]. A three stage OPAMP using pentacene-based dual-gate OTFTs has been used in [49], as a building block for a first order implementation of ΔΣ ADC. This high-gain amplifier is a cascade of three differential stages, each of which uses four techniques: bootstrapped gain-enhancement, CMFB, cascoding and backgate steering.

As a part of this thesis, possibility of OPAMP design using ZTO NTFTs has been investigated. This chapter deals with the design exploration, implementation details and performance optimization based on the feedback obtained from lab tests of ZTO based OPAMP.

5.1 DESIGN EXPLORATION

One of the important constraints on the choice of topology for the OPAMP design using ZTO devices was the availability of only n-channel devices. An NMOS only topology proposed by Y. Tsividis and P. Gray [50] for LSI technology in 1976 provided a good starting point. An adaptation of the Tsividis - Gray topology for the ZTO devices has been reported by R. Sarpeshkar and A. Moini, in their unpublished work [51]. The Sarpeshkar-Moini OPAMP (S-M OPAMP) was designed using a modified Level 1 SPICE MOSFET model and was reported to meet the specifications of a 741 BJT based OPAMP through SPICE simulations. As a first step towards design exploration, the S-M OPAMP was laid out (mask 2) and tested in the lab. In the next subsection, the topology of the original Tsividis - Gray OPAMP and its adaptation in the S-M OPAMP is discussed.

5.1.1 Adaptation of the Internally Compensated Differential Amplifier Topology

The Tsividis - Gray OPAMP consists of three main stages : (i) Input gain stage (ii) cascode gain stage, (iii) buffer and output driver stage (Figure 5.1). It incorporates a differential-input, single-ended output topology. Being a multi-stage design, Miller compensation or frequency compensation is achieved through the feedback applied using a source follower stage acting as a buffer and a capacitor from the output of the cascode stage to its input. The buffer prevents the feedfoward path otherwise presented by the capacitor to high frequency signals. The cascode stage provides single ended gain as well as avoids loading of the first stage by high Miller capacitance otherwise presented at the input of the second stage. The third stage consists of a buffer and an output driver circuit. The buffer serves as a level shifter and also avoids loading of the first two stages by the output driver block. The output driver stage consists of a common source (CS) amplifier that provides high current to support large capacitive loads.

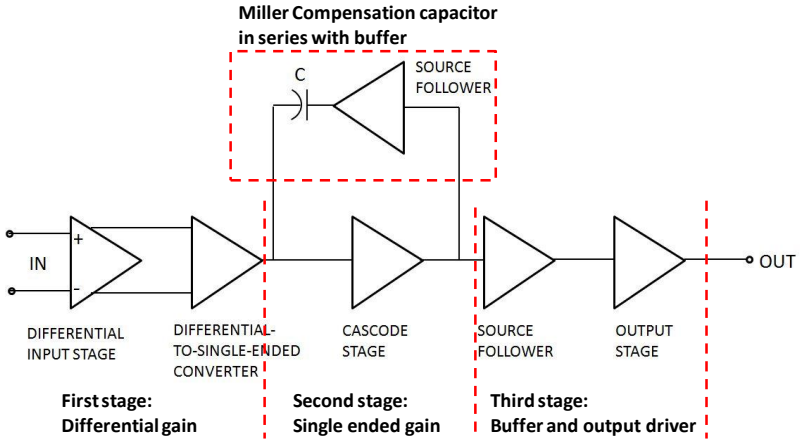


Figure 5.1 Block diagram of Tsividis - Gray OPAMP

The S-M OPAMP also has three stages similar to the Tsividis - Gray OPAMP. An important difference being the use of a resistors instead of the diode connected loads (not acting as current mirrors). With this modification, the parasitic capacitance seen at many nodes due to wide devices was eliminated, which effectively increased the unity gain bandwidth as well as allowed higher gain at stages where the gain was limited by the low load resistance ($1/g_m$). The feedback path from the output of the second stage to its input was achieved using a series RC combination. The left-half plane zero provided by R was used in achieving better frequency response. Carefully chosen values for the parallel RC combination added in the third stage, can provide a low impedance path to the signal and block the dc offset (high-pass operation).

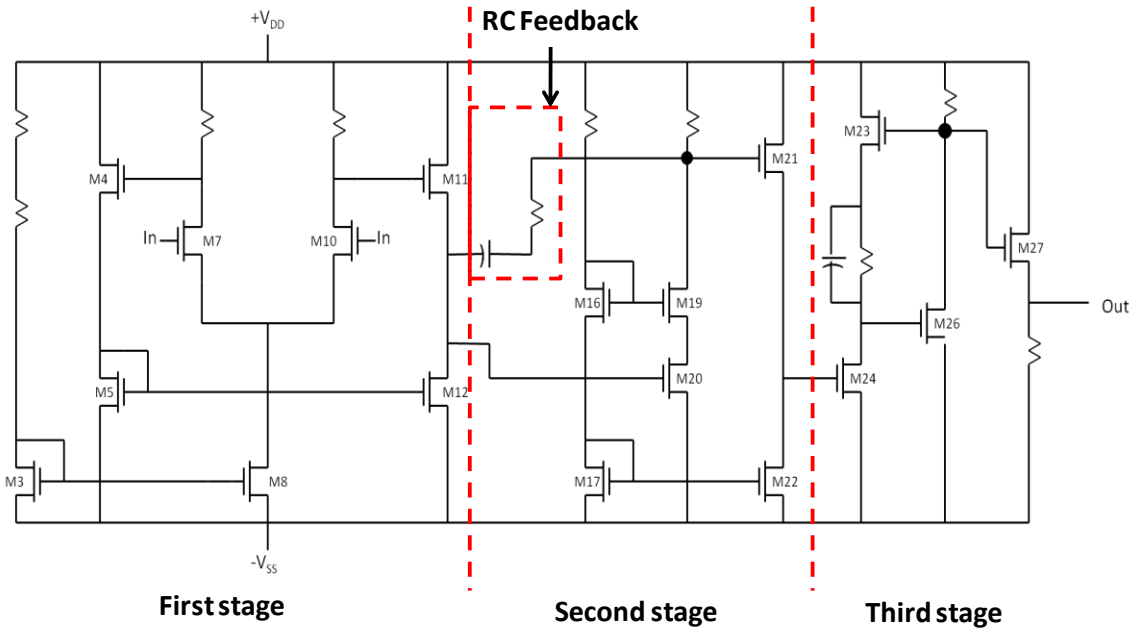


Figure 5.2 Schematic of S-M OPAMP

However the results obtained in [51] by using the modified Level 1 SPICE MOSFET model could not be matched using the fit of RPI a-Si simulation model introduced in Chapter 2. Thus, it was necessary to explore a new topology which could counter the limitations of the ZTO technology and achieve optimized performance.

5.1.2 Process dependent design considerations

As discussed in Chapter 3, the layout configurations were revised after every iteration of the design cycle, in order to improve the uniformity of the fabrication process. During circuit design, the sizing of the devices had to be done using the estimated value for mobility in the improvised process. In case of variations in the mobility value, it was very difficult to maintain all the devices at the desired operating point. Thus, provision was made to connect external resistances and capacitances in as many branches as possible. This provided external control over the currents in each branch and thus desired operating point could be achieved in spite of process variations.

In bulk silicon technology, often a small aspect ratio (W/L < 1) is chosen for the diode connected NMOS device used as a load. This results in high load resistance

(comparable to that of a complementary PMOS), which is desirable for achieving high gain. However in the case of ZTO technology, fringing currents start to dominate the drain current in devices with small aspect ratios. This limitation makes use of external resistances favorable.

With the high overlap capacitance (250 nF/cm^2) observed in ZTO devices, it was hard to achieve a high unity-gain bandwidth and phase margin specifications. To tackle this issue, harsh scaling was done to reduce the parasitic capacitances of devices. The scaling lowered the transconductance (g_m) of the devices, resulting in lowering of the overall gain. Thus, there was a tradeoff between achieving reasonable gain and bandwidth. To achieve reasonable phase margin, the pole-splitting technique using series RC combination was applied at multiple nodes.

The biasing of devices had to be handled differently to account for the gate voltage dependence of carrier mobility in ZTO devices. High g_m for the devices in the gain providing stages required high gate voltages, which meant that higher headroom was required to maintain the devices in saturation regime. However, headroom was controlled by the external resistances in most of the branches. Hence, sizing of the device and choice of resistance values required careful investigation.

It was observed that the cascode configuration did not provide any considerable advantage in terms of gain over a common-source (CS) amplifier in designs using ZTO devices. This was again attributed to the inclusion of external resistance in this branch, as it dominated the effective output resistance of the cascode stage. Hence, high gain implied inclusion of high external resistances, which resulted in headroom issues as described above. Thus, the cascode stage was replaced by a CS amplifier.

The implementation details of the OPAMP based on these process specific requirements are discussed next.

5.2 ZTO BASED OPAMP

5.2.1 Topology

A high gain OPAMP was built using three stages and an output buffer/driver stage as shown in the block diagram. Frequency and phase response was achieved using pole-zero Miller compensation technique across two stages.

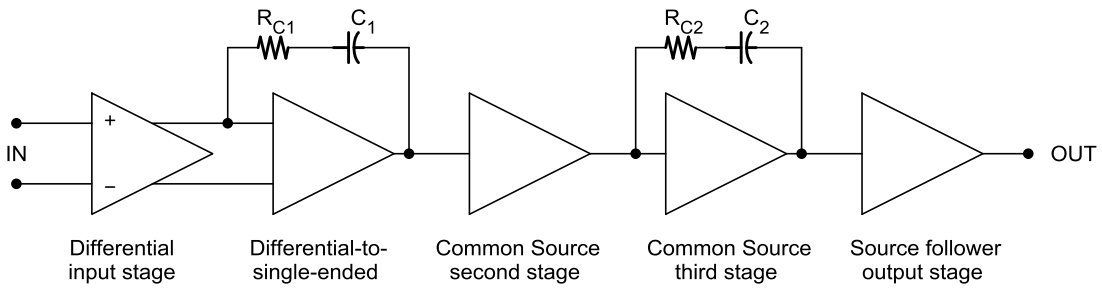


Figure 5.3 Block diagram of the ZTO based OPAMP

5.2.2 Circuit Analysis

The differential input stage (Figure 5.4 (a)) consists of a differential pair with resistive loads and a tail current source. Current mirroring is used to bias the tail current source. Moderate dimensions are used for the differential pair, as these devices affect the frequency response severely. All the devices except for the current source have minimum channel lengths (4 μm). Higher channel length (20 μm) of the tail device, helps in improving the common mode rejection ratio (CMRR) of the amplifier. A differential gain of 2.5 (8 dB) is achieved in this stage and is given as:

$$A_{d1} = g_{m1}(r_{o1} \parallel R1) \qquad (5.1)$$

where, $g_{m1} = g_{m2}$ and $r_{o1} = r_{o2}$

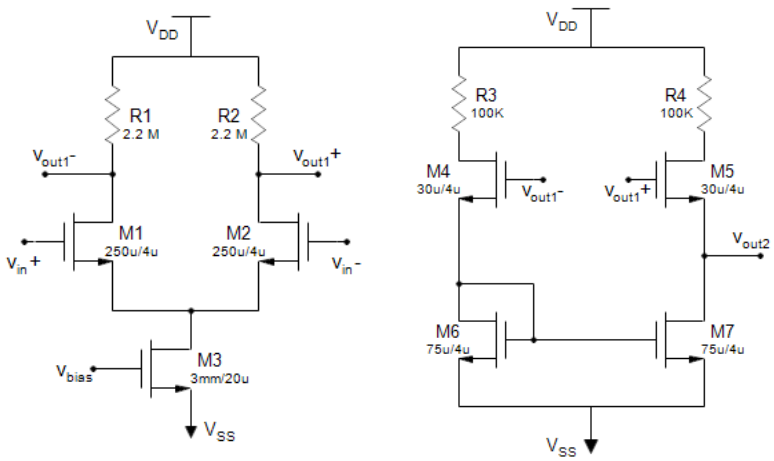


Figure 5.4 Schematic: (a) Differential input stage, (b) Differential-to-single ended converter stage

In the differential-to-single ended converter stage (Figure 5.4 (b)), the phase of the signal applied at V_{out1}- gets inverted at the output of the CS stage formed by M7 and M5. The differential signals thus get added at the node V_{out2}. A nominal gain of 1.2 (1.6 dB) was observed in this stage.

The second and third stages are implemented as common source (CS) amplifiers with external load resistances (Figure 5.5). The gain expressions of these stages are:

$$A_{v2} = g_{m9}(r_{o9} \parallel R6) \qquad (5.2)$$

$$A_{v3} = g_{m10}(r_{o10} \parallel R7) \qquad (5.3)$$

A gain of 7 (17 dB) and 6 (15.6 dB) is obtained from the second and third stages respectively.

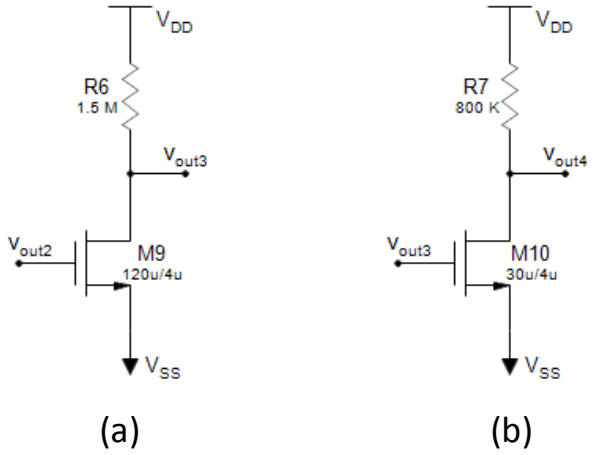


Figure 5.5 Schematic: (a) Second CS stage, (b) Third CS stage

The output buffer stage implemented as a source follower helps drive capacitive loads up to 15pF without affecting the stability of the amplifier. The gain of this stage is given as:

$$A_{v4} = \frac{gm11R8}{1+gm11R8} \qquad (5.4)$$

As seen from the Eq. (5.4), gain of the buffer stage is less than unity (0.79) and thus it reduces the overall gain of the OPAMP stages from 120 (41.6 dB) to an output gain of 100 (40 dB).

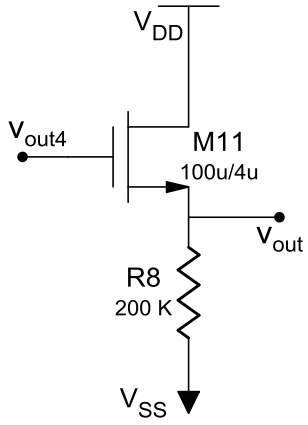


Figure 5.6 Schematic: Source follower output stage

Figure 5.7 shows the complete schematic of all the four stages along with Miller compensation connections and current mirror branches.

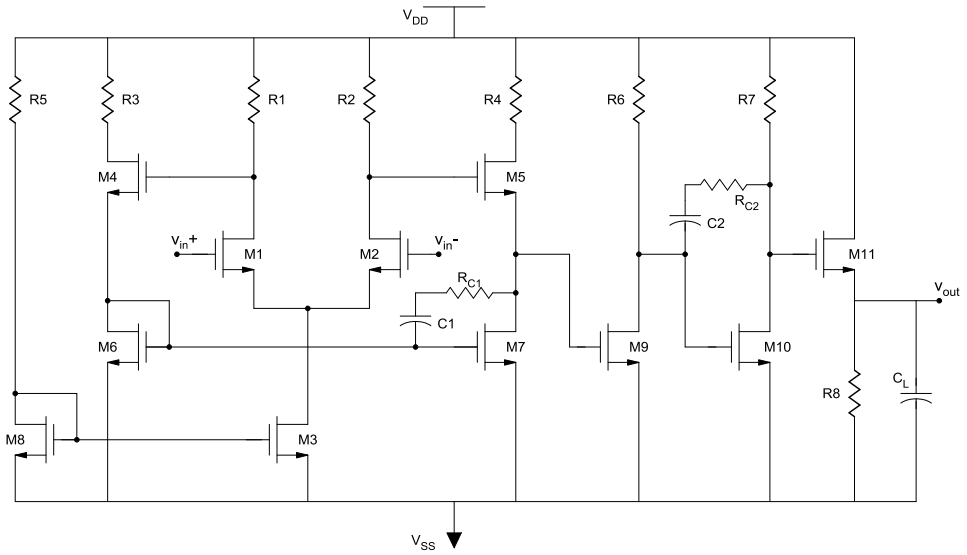


Figure 5.7 Schematic of the ZTO based OPAMP

Table 5.1 Values of pole-zero Miller Compensation components in ZTO based OPAMP

Component	Value
R_{C1}	1MΩ
C_1	300pF
R_{C2}	550kΩ
C_2	500pF

The layout of this circuit (from mask 4) is shown in Figure 5.8. The connections for external resistance and capacitances are provided on boundary pads. This OPAMP has been implemented with the extended gate configuration II discussed in Chapter 3.

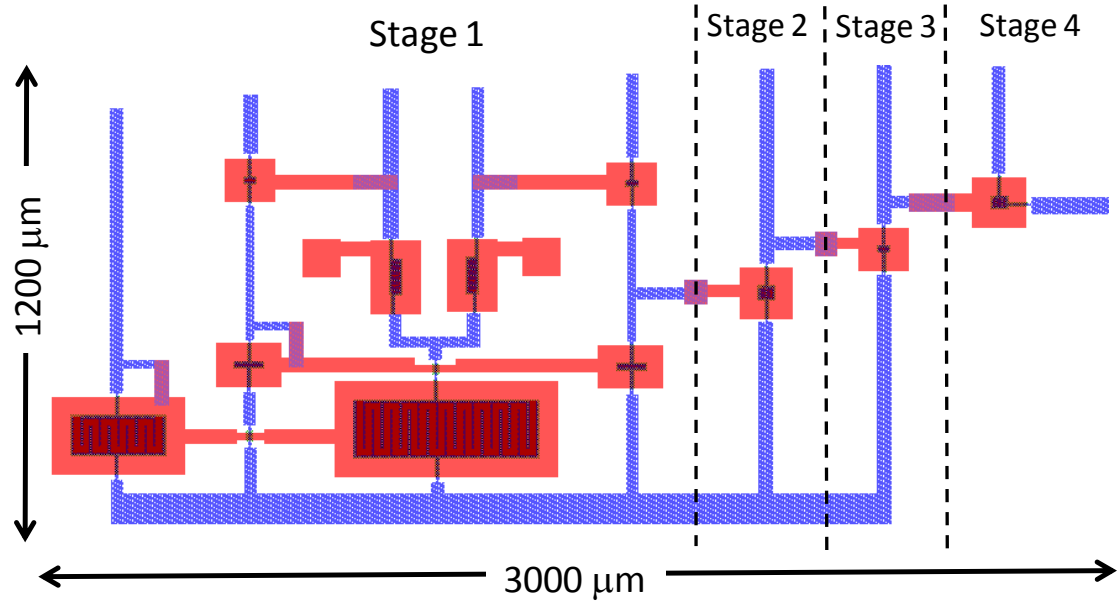


Figure 5.8 Layout of ZTO based OPAMP (mask 4)

5.2.3 Simulation Results

The modified RPI a-Si model has been used in the design process of this OPAMP. Following is tabulation of the simulation results obtained assuming a 5 pF load capacitance and supply voltage of 5V. The OPAMP can sustain a maximum capacitive load of 15pF with a phase margin of 45^{o}.

Table 5.2 Simulation results of ZTO based OPAMP

Specification	Simulation Results
Supply Voltage	5 V
Low frequency gain	98.9 = 39.9 dB
Unity gain frequency	27.7 kHz
Phase Margin	45.1^{0}
Gain Margin	3.888dB
CMRR	10.73 dB

PSRR	21.4 dB
Output voltage swing (30dB gain)	0.4 – 2.5V

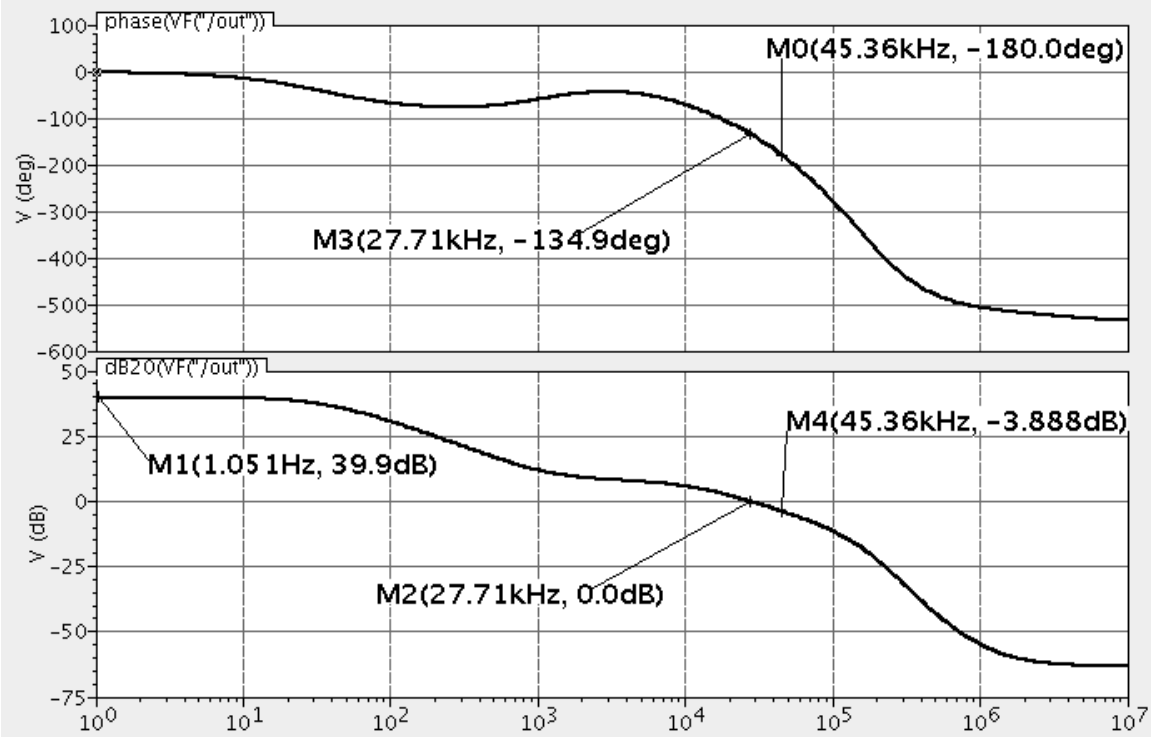


Figure 5.9 Magnitude and Phase response of ZTO based OPAMP with low frequency gain of 39.9 dB, unity gain frequency of 27.7 kHz, phase margin of 45.1^{o} and gain margin of 3.888dB

The results of ZTO based OPAMP compare favorably with the a-Si based high gain amplifiers reported in [48-49] operating at supply voltages of ±15V.

Currently this design is under fabrication and would be tested soon.

CHAPTER 6
Conclusion and Future Work

6.1 CONCLUSION

In this thesis, an in depth investigation of various aspects of device modeling of solution based zinc-tin oxide (ZTO) TFT devices was presented and the validity of the proposed models was established through circuit results. The design flow for introducing a device model, circuit simulations and layout, and extraction and verification of layouts was set up for a new process. The accuracy of the device model used for ZTO TFTs and circuit performance was improved during each iteration of the design flow. The process uniformity of solution based ZTO devices was refined through four mask designs. The orientation of device layout and other fabrication related specifications was revised in each of these masks, to resolve the uniformity and performance issues encountered. The implementation of high gain OPAMP using the ZTO devices has established the scope of building complex circuits using this process. This study has thus built a strong base for future research in the area of low-cost, flexible and transparent electronics using solution based ZTO TFT devices.

The areas of research identified as important steps in order to further the development of this technology, are discussed in the next section.

6.2 FUTURE WORK

6.2.1 Device modeling

The requirement of a new physical compact model for ZTO devices and for amorphous oxide TFT devices as a whole has been discussed in Chapter 2. The simplifying assumptions made for deriving the expression for the effective mobility in ZTO TFTs (Eq. (2.21)) would result in inaccurate predictions of the circuit behavior. Following are the main assumptions which need to be handled carefully in future:

(i) The step function behavior assumed for the Fermi–Dirac distribution function could be a good approximation for low quality ZTO films where the localized band-tail is deep and Fermi level is away from the band-edge. However, as the semiconductor film becomes more ordered with refinement of the deposition process, the band-tail would shrink. In this case the assumption would become less valid. Thus, an accurate expression to calculate the density of trapped charges needs to be derived.

(ii) The total induced charge density approximated as the total trapped charge density becomes invalid in higher quality ZTO films and also at higher temperatures. In both these cases, the density of carriers promoted to the transport band (n_c) is considerable and hence,

$$n = n_c + n_t \approx n_t$$

would no longer hold.

(iii) For ZTO TFTs, the charge transport is dominated by the Multiple Trap and Release (MTR) mechanism at higher temperatures [24]. At lower temperatures, different charge mechanism transports need to be examined.

(iv) The ZTO devices are assumed to be always operated in the lower gate voltage range ($V_G - V_{ON} < 7$ V), hence the crossover of charge transport mechanism from MTR to band transport has not been accounted for. Also as the quality of ZTO improves, more carriers can crossover to transport band even at lower voltages. These effects should be accommodated in the new model.

(v) The band mobility (μ_0) is assumed to be constant in the current derivation. However the temperature and DOS (applicable to the transport band) dependence should be incorporated in the band mobility expression.

The new DC model obtained by covering for all the shortcomings listed above would thus be a very close representation of the physical phenomena governing the operation of ZTO devices. A charge based approach similar to that adopted in [41] for deriving the physical compact model would be ideal. It is quite convenient to arrive at the

equations to describe the dynamic behavior of the device from the charge based DC model. The node currents would have to be expressed in the form:

$I_i = I_{dc(i)} + \frac{dQi}{dt}$ where, i ∈{gate, source, drain}

The small signal model assumed in [41] can be applied to the ZTO devices. With the option of direct use of symbolic partial derivative and integration for defining currents and voltages available in VerilogA, it would be an apt choice for an implementation platform for the AC/DC model of ZTO TFTs.

6.2.2 Circuit design

As discussed in Chapter 5, the performance of ZTO TFT based circuits is constrained by the limitations of the solution processed ZTO technology. These limitations being: high parasitic capacitance, lack of complementary (p-channel) devices and uniformity issues.

A work around for the unavailability of the complementary device is fabrication of a hybrid organic-inorganic complementary circuit configuration. Using the organic p-channel devices higher gains can be achieved from currently limited circuit configurations like the cascode. The leakage current would also be lower in these hybrid circuits.

As the process matures, active loads (n-channel enhancement) can be incorporated in the circuits which would help resolve the issues currently faced due to the use of external resistances as loads.

With a more stable technology it would be possible to make use of the positive feedback and other gain boosting techniques implemented for a-Si technology [48-49] to achieve higher gain in the OPAMP.

The use of ZTO devices in making digital logic gates still needs to be explored. Successful implementation of inverters has already been demonstrated in this thesis. Design and characterization of other logic gates like OR, NAND, NOR, EX-OR needs to

be done. These gates then can be used as basic building blocks for designing complex digital circuits and also mixed signal applications like ADC/ DAC.

APPENDIX A

Following is the graphical representation of the steps involved in fabrication of solution based ZTO devices.

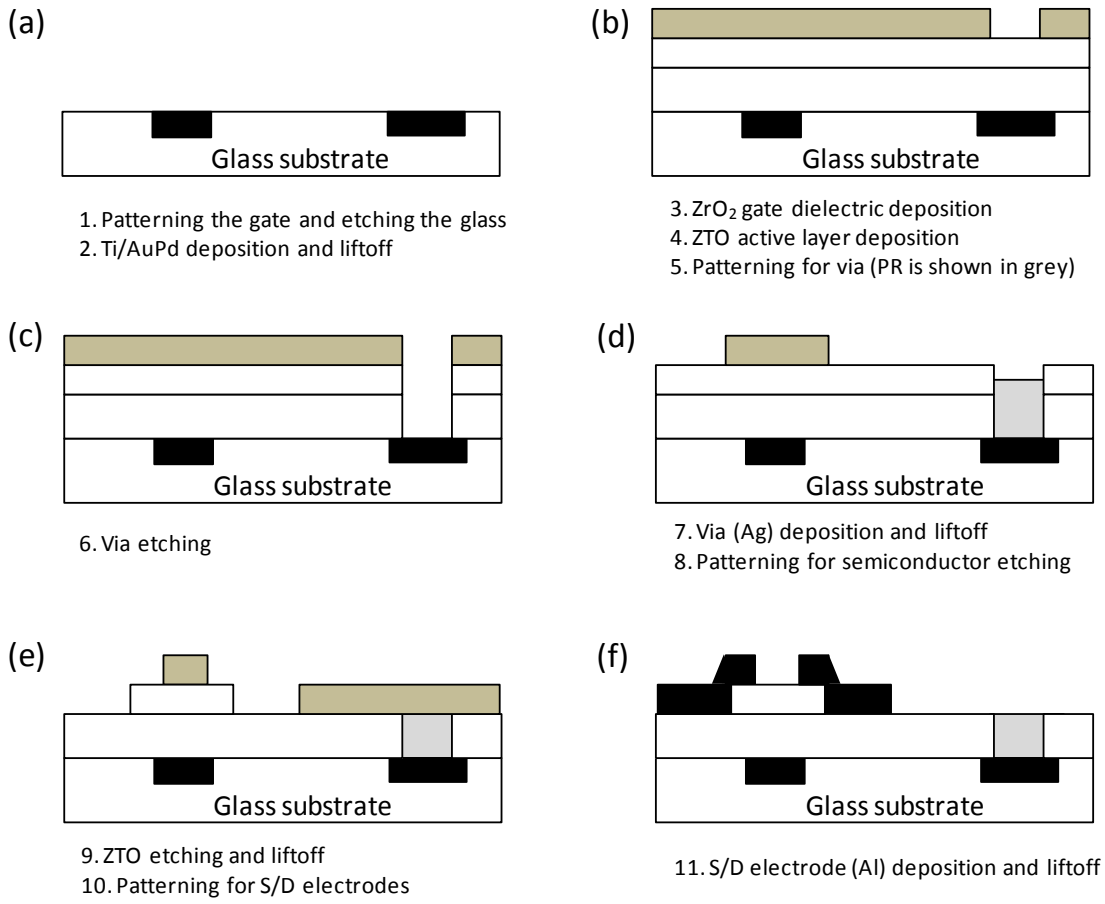


Figure A1 Fabrication steps of ZTO TFTs

APPENDIX B

Following is the list of different model files used during circuit simulations.

I. Modified SPICE Level 1 MOSFET model

(i) Simulator : Spectre

```
simulator lang = spice
.MODEL NMOS_VTL nmos LEVEL=1
+ TOX=42E-9 TPG=1 VTO=1 UO=5 GAMMA=0 LAMBDA=1E-3
+ NSUB=1e11
+cgso = 2.5e-9    cgdo = 2.5e-9
```

(ii) Simulator: SPICE [Exclude the "simulator lang" directive from the Spectre model]

```
.MODEL NMOS_VTL nmos LEVEL=1
+ TOX=42E-9 TPG=1 VTO=1 UO=5 GAMMA=0 LAMBDA=1E-3
+ NSUB=1e11
+cgso = 2.5e-9    cgdo = 2.5e-9
```

(i) RPI amorphous silicon TFT model fit to experimental data of ZTO devices

(i) Simulator : Spectre

```
simulator lang = spice
.MODEL NMOS_aSi atft type=n
**GEOMETRIC AND TECHNOLOGY PARAMETERS**
+TOX=100e-9
```

+cgso = 2.5e-8 cgdo = 2.5e-8

+EPS=1.5

+EPSI=18

+IOL=20e-9

TRAP DISTRIBUTION RELATED PARAMETERS

default values

+DEF0 = 0.6

+GMIN = 1.0e23

+V0 = 0.12

OTHER PARAMETERS

*onset voltage *

+VTO= 0

series contact resistance

+rd=500 rs= 500

saturation knee parameters - default values

+ALPHASAT = 0.6

+m = 2.5

--removing temperature dependence--

+tnom=27

+kvt = 0

+kasat = 0

--physics--

gate dependence of mobility

+GAMMA= 0.29

activation energy

+EMU= 0.05

flat band voltage

```
+VFB= 1.4
**---leakage---****
+sigma0= 50e-9
+delta= 2
+VGSL= 2

**--Band Mobility--**
+MUBAND= 0.003
```

(ii) Simulator : Spectre

This model is a modification of the RPI aSi model listed above (II. (i)). In model II.(i), the activation energy given by Eq. (2.16) is not observed to affect the effective mobility exponentially at all temperatures as seen in (Eq. 2.21).

$\mu_{eff} \cong \mu_o . \frac{Nc}{Nt} e^{-(Ec-Et)/kT}$ (From Eq. (2.21))

where (E_c - E_t = E_a) is the activation energy in eV.

Temperature dependence was eliminated by setting *tnom* parameter to ambient temperature and *kvsat, kvt* to zero. Then the MUBAND parameter was directly set to the value of effective mobility value extracted from experimental data. This model showed fits as close to the experimental values as model II.(i). Through this modification, flexibility to set the effective mobility observed in experimental data directly in simulation models was added to the model.

```
simulator lang = spice
.MODEL NMOS_aSi atft type=n

+GAMMA=0.026
```

```
+VTO=0
+TOX=100e-9
+cgso = 2.5e-8    cgdo = 2.5e-8
+rd=500 rs=500
** Removing Temperature Depenedence**
+tnom=27
+kvt = 0
+kasat = 0
**********************************
+VFB=1.4
+EPS=1.5
+EPSI=18
+sigma0=50e-9
+delta=3
+IOL=20e-9
+VGSL=2
** Effectove Mobility **
+MUBAND=4e-4
**********************************
```

APPENDIX C

The layout tool provided by Tanner EDA- Ledit is used for layouts of the ZTO TFT based circuits. The different drawn layers used for the layout in Ledit are listed below:

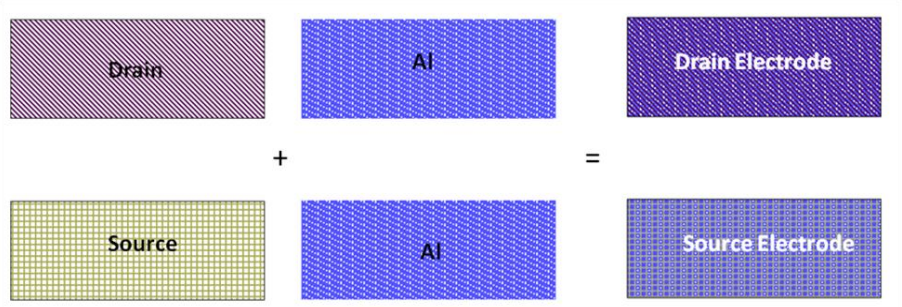
Table C3: Layers used in the layout of ZTO based circuits

Layer	**Function**	**Type**
AuPd	Gate	Fabrication
Al	Source/ Drain	Fabrication
Active	ZTO (Semiconductor)	Fabrication
Via	Via and Silver plug	Fabrication
NMOS	Define device	Verification
Source	Define Al layer as source	Verification
Drain	Define Al layer as drain	Verification
ntran	Define conductive channel	Verification

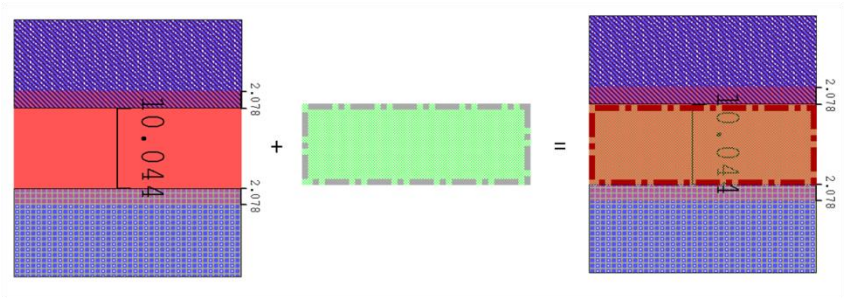
The layers classified as ‘Fabrication’ are actually deposited during the fabrication of ZTO devices. While the layers classified as ‘Verification’ are defined only for the purpose of extraction and verification of the layout.

I. Steps for laying out a ZTO TFT device and its interconnects:

(i) Define the Source and Drain electrodes of the device

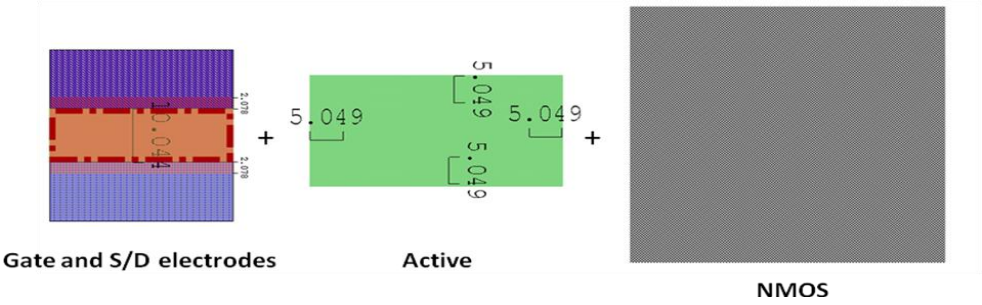


(ii) Define gate and channel (for extraction) of the device



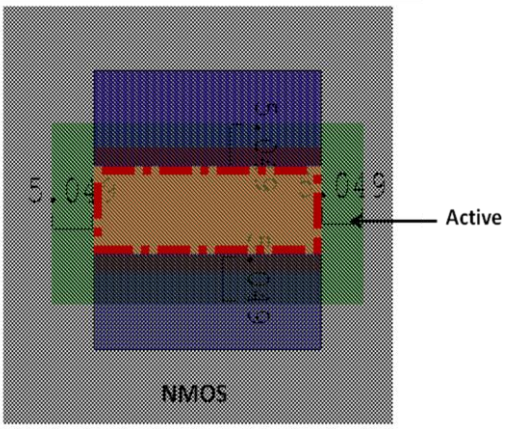
Al and AuPd ntran Gate, Source , Drain defined

(iii) Adding semiconductor layer (Active) and the identifying layer (NMOS - for extraction of the device)

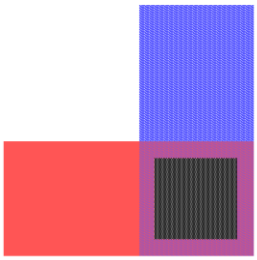


Gate and S/D electrodes Active NMOS

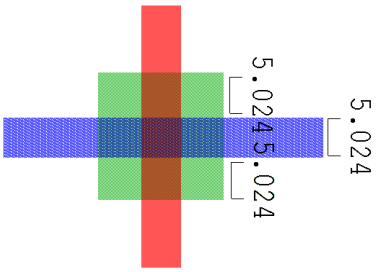
(iv) ZTO TFT layout



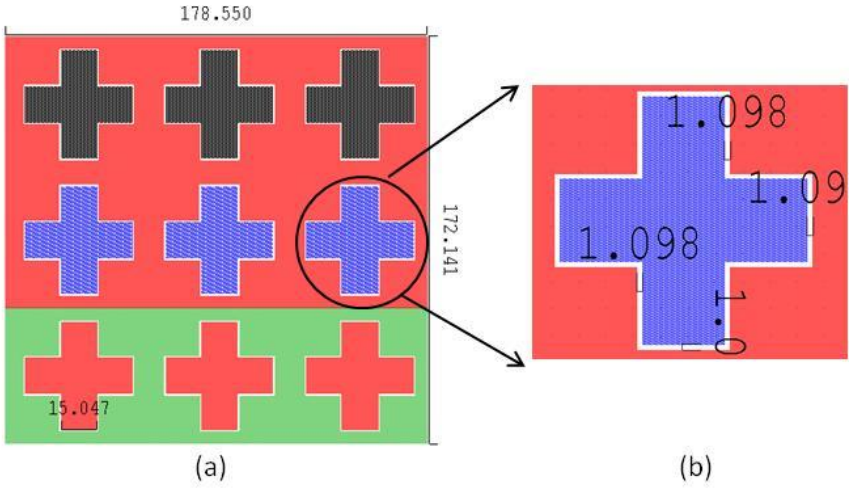
(v) Connecting Al and AuPd layers by Via



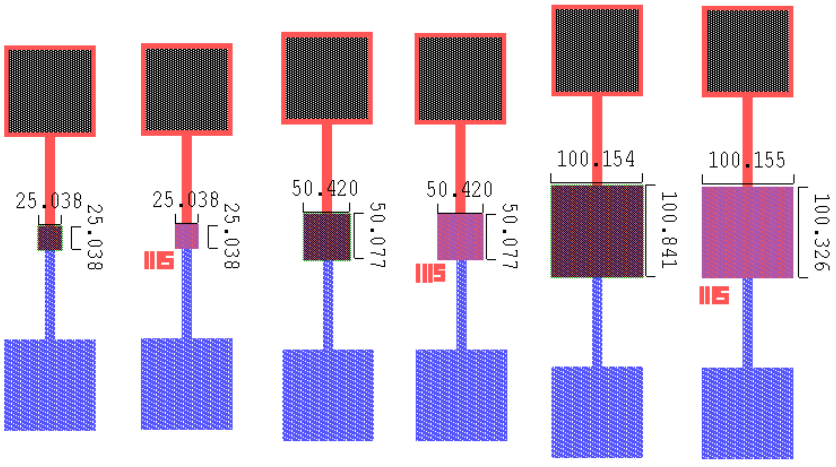
(vi) Crossing of Al and AuPd layers surrounded by Active (to avoid short between these layers due to extra etching of the oxide during patterning of the Al layer)



II. Alignment marks added in the layout for aligning different layers during fabrication



III. Test structures used for capacitance measurements



APPENDIX D

Following are the command files defined for the Design Rule Check (DRC) and layout extraction in Tanner EDA:

(i) DRC commend file

```
TITLE "Organic_ZTO"
//      Setup Info
PRECISION   1000
RESOLUTION      5
UNIT LENGTH     u
FLAG ACUTE YES
FLAG NONSIMPLE YES
FLAG SKEW YES
FLAG ZEROWIDTHWIRES YES
FLAG POLYGONVERTEXLIMIT 199
FLAG WIREVERTEXLIMIT 200
VIRTUAL CONNECT COLON NO
VIRTUAL CONNECT SEMICOLON AS COLON NO
VIRTUAL CONNECT DEPTH PRIMARY
DRC TOLERANCE FACTOR 0.005

LAYOUT PRIMARY "OPAMP_Mask4_final"


//      Input Layers
LAYER       Active 4
LAYER       Al     2
LAYER       drain  1009
LAYER       n_mos  5
LAYER       ntran  1011
LAYER       Pd_Au  1
LAYER       source 1010
LAYER       Via1   13


//      Rules
PdAu_Min_Width { @ < 4.9 Microns
        INTERNAL  Pd_Au < 4.9 ABUT >= 0 < 90 SINGULAR
```

```
        }
        al_without_via =  NOT INTERACT Al Via1
        gold_al_overlap =  AND al_without_via Pd_Au
        Gold_Al_Active_surround { @ < 2 Microns
                ENCLOSURE   gold_al_overlap   Active  <  2  ABUT  >=  0  <  90
INSIDE ALSO OUTSIDE ALSO SINGULAR REGION REVERSAL
        }
        PdAu_Al_Overlap { @ < 1 Microns
                INTERNAL  Pd_Au  Al > 0 < 1 ABUT >= 0 < 90 SINGULAR
        }
        Intermediate_0001 =  AND drain n_mos
        ndiff_d =  AND Intermediate_0001 Al
        Intermediate_0002 =  AND source Al
        ndiff_s =  AND Intermediate_0002 n_mos
        Min_Channel_Length { @ < 3 Microns
                EXTERNAL   ndiff_d   ndiff_s  <  3  ABUT  ==  0  INSIDE  ALSO
SINGULAR REGION REVERSAL
        }
        PdAu_PdAu_Spacing { @ < 9.9 Microns
                EXTERNAL  Pd_Au < 9.9 SINGULAR
        }
        PdAu_Al_Spacing { @ < 2.45 Microns
                EXTERNAL  Pd_Au  Al < 2.45 ABUT >= 0 < 90 SINGULAR
        }
        Al_Min_Width { @ < 4.9 Microns
                INTERNAL  Al < 4.9 SINGULAR
        }
        Al_Al_Spacing { @ < 3.9 Microns
                EXTERNAL  Al < 3.9 SINGULAR
        }
        Via_Al_Surround { @ < 3 Microns
                ENCLOSURE  Via1  Al < 3 ABUT == 0 SINGULAR
               Result1 =  CUT Via1 Al
        }
        Via_PdAu_Surround { @ < 3 Microns
                ENCLOSURE  Via1  Pd_Au < 3 ABUT == 0 SINGULAR
               Result1 =  CUT Via1 Pd_Au
        }
        Via_Via_Spacing { @ < 10 Microns
                EXTERNAL  Via1 < 10 SINGULAR
        }
        Active_ntran_Surround { @ < 2 Microns
                ENCLOSURE  ntran  Active < 2 ABUT == 0 SINGULAR
```

```
        }
        Via_Min_Width { @ < 20 Microns
                INTERNAL  Via1 < 20 ABUT >= 0 < 90 SINGULAR
}
```

(ii) Layout extraction command file

```
        # File: Organic_ZTO.ext
        # For: Extract definition file
        # Technology: Solution based ZTO Process
        # Technology Setup File and Test/Demo Suite:
Organic_ZTO_TechSetup.tdb
        # Copyright © 2002-2003 Tanner EDA
        # All Rights Reserved
        #
        # This file will work only with L-EDIT Version 7 and greater.
        #
**********************************************************************
**********
        connect(Pd_Au,Al, Via1)

        #Commands to recognize ports

        attach(Al,ndiff_s)
        connect(Al,ndiff_s,ndiff_s)
        attach(Al,ndiff_d)
        connect(Al,ndiff_d,ndiff_d)
        attach(Al,Via1)
        attach(Al,Pd_Au)
```

```
attach(Label,Al)
attach(Label,Active)
attach(Label,Pd_Au)

connect(gate_org,Pd_Au,Pd_Au)



# NMOS transistor with pDAU gate
device = SUBCKT(
        RLAYER=ntran, LW, WIDTH;
        Dr=ndiff_d, AREA, PERIMETER;
        Ga=gate_org, LW, WIDTH;
        So=ndiff_s, AREA, PERIMETER;
        MODEL=NMOS_VTL;
        )
```

References

[1] G. Patton and Ieee, *Semiconductor Technology - Trends, Challenges and Opportunities*, 2009.

[2] A. Dodabalapur, "Organic and polymer transistors for electronics," *Materials Today*, vol. 9, pp. 24-30, Apr 2006.

[3] J. D. Choe, *et al.*, "A 22-nm damascene-gate MOSFET fabrication with 0.9-nm EOT and local channel implantation," *Ieee Electron Device Letters*, vol. 24, pp. 195-197, Mar 2003.

[4] M. Ito, *et al.*, "Application of amorphous oxide TFT to electrophoretic display," *Journal of Non-Crystalline Solids*, vol. 354, pp. 2777-2782, May 2008.

[5] J. K. Jeong, *et al.*, "12.1-in. WXGA AMOLED display driven by InGaZnO thin-film transistors," *Journal of the Society for Information Display*, vol. 17, pp. 95-100, Feb 2009.

[6] D. P. Heineck, *et al.*, "Zinc Tin Oxide Thin-Film-Transistor Enhancement/Depletion Inverter," *Ieee Electron Device Letters*, vol. 30, pp. 514-516, May 2009.

[7] H. Frenzel, *et al.*, "High-gain integrated inverters based on ZnO metal-semiconductor field-effect transistor technology," *Applied Physics Letters*, vol. 96, Mar 2010.

[8] D. L. Zhao, *et al.*, "Fast Flexible Plastic Substrate ZnO Circuits," *Ieee Electron Device Letters*, vol. 31, pp. 323-325, Apr 2010.

[9] D. A. Mourey, *et al.*, "Self-Aligned-Gate ZnO TFT Circuits," *Ieee Electron Device Letters*, vol. 31, pp. 326-328, Apr 2010.

[10] N. M. Kodeti, "White Paper On Silicon On Insulator (SOI) Implementation," Infotech Enterprises Ltd.2009.

[11] T. Sakurai, *et al.*, *Fully-depleted SOI CMOS circuits and technology for ultra-low power applications*: Birkhäuser, 2006.

[12] S. M. Han, *et al.*, "Poly-Si TFT fabricated at 150 degrees C using ICP-CVD and excimer laser annealing," *Proceedings of the Ieee*, vol. 93, pp. 1297-1305, Jul 2005.

[13] C. M. Tan, *et al.*, "Temperature and stress distribution in the SOI structure during fabrication," *Ieee Transactions on Semiconductor Manufacturing*, vol. 16, pp. 314-318, May 2003.

[14] D. A. Good, "Novel Processes for Poly-Si Thin-Film Transistors on Plastic Substrates," Electrical Engineering and Computer Sciences, UNIVERSITY OF CALIFORNIA, BERKELEY, 2007.

[15] H. Q. Chiang, *et al.*, "High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer," *Applied Physics Letters*, vol. 86, Jan 2005.

[16] C.-G. Lee, "Solution-Processed Zinc-Tin Oxide Thin-Film Transistors and Circuit Applications," Ph.D. Dissertation, Electrical and Computer Engineering, The University of Texas at Austin, Austin, 2011.
[17] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, 2010.
[18] G. Depeyrot, *et al.* (2011, Guidelines for Verilog-A Compact Model Coding. *Design & Reuse Industry Articles*.
[19] G. J. Coram and Ieee, *How to (and how not to) write a compact model in Verilog-A*, 2004.
[20] D. Hong, *et al.*, "Electrical modeling of thin-film transistors," *Critical Reviews in Solid State and Materials Sciences*, vol. 33, pp. 101-132, Apr-Jun 2008.
[21] Z. Bao and J. J. Locklin, *Organic field-effect transistors*: CRC Press, 2007.
[22] W. Brutting, "Physics of organic semiconductors," ed, 2005.
[23] D. Monroe, "HOPPING IN EXPONENTIAL BAND TAILS," *Physical Review Letters*, vol. 54, pp. 146-149, 1985.
[24] C. G. Lee, *et al.*, "Band transport and mobility edge in amorphous solution-processed zinc tin oxide thin-film transistors," *Applied Physics Letters*, vol. 97, Nov 2010.
[25] e. a. Reprinted with permission from [C. G. Lee, "Band transport and mobility edge in amorphous solution-processed zinc tin oxide thin-film transistors," Applied Physics Letters, vol. 97, Nov 2010]. Copyright [2010], American Institute of Physics., ed.
[26] M. Shur and M. Hack, "PHYSICS OF AMORPHOUS-SILICON BASED ALLOY FIELD-EFFECT TRANSISTORS," *Journal of Applied Physics*, vol. 55, pp. 3831-3842, 1984.
[27] E. Calvetti, *et al.*, "Analytical model for organic thin-film transistors operating in the subthreshold region," *Applied Physics Letters*, vol. 87, Nov 2005.
[28] L. Torsi, *et al.*, "AN ANALYTICAL MODEL FOR SHORT-CHANNEL ORGANIC THIN-FILM TRANSISTORS," *Journal of Applied Physics*, vol. 78, pp. 1088-1093, Jul 1995.
[29] P. V. Necliudov, *et al.*, "Modeling of organic thin film transistors of different designs," *Journal of Applied Physics*, vol. 88, pp. 6594-6597, Dec 2000.
[30] F. Torricelli, *et al.*, "A charge control analytical model for organic thin film transistors," *Applied Physics Letters*, vol. 92, Mar 2008.
[31] R. L. Hoffman, "A closed-form DC model for long-channel thin-film transistors with gate voltage-dependent mobility characteristics," *Solid-State Electronics*, vol. 49, pp. 648-653, Apr 2005.
[32] S. Mijalkovic, *et al.*, *Modelling of organic field-effect transistors for technology and circuit design*, 2008.
[33] O. Marinov, *et al.*, "Organic Thin-Film Transistors: Part I-Compact DC Modeling," *Ieee Transactions on Electron Devices*, vol. 56, pp. 2952-2961, Dec 2009.

[34] M. S. Shur, *et al.*, "SPICE models for amorphous silicon and polysilicon thin film transistors," *Journal of the Electrochemical Society,* vol. 144, pp. 2833-2839, Aug 1997.
[35] A. Cerdeira, *et al.*, "New procedure for the extraction of basic a-Si : H TFT model parameters in the linear and saturation regions," *Solid-State Electronics,* vol. 45, pp. 1077-1080, Jul 2001.
[36] M. Estrada, *et al.*, "Extraction method for polycrystalline TFT above and below threshold model parameters," *Solid-State Electronics,* vol. 46, pp. 2295-2300, Dec 2002.
[37] A. Cerdeira, *et al.*, "Modeling and parameter extraction procedure for nanocrystalline TFTs," *Solid-State Electronics,* vol. 48, pp. 103-109, Jan 2004.
[38] A. Estrada, *et al.*, "Accurate modeling and parameter extraction method for organic TFTs," *Solid-State Electronics,* vol. 49, pp. 1009-1016, Jun 2005.
[39] B. Iniguez, *et al.*, "Universal compact model for long- and short-channel Thin-Film Transistors," *Solid-State Electronics,* vol. 52, pp. 400-405, Mar 2008.
[40] M. Fadlallah, *et al.*, "DC/AC unified OTFT compact modeling and circuit design for RFID applications," *Solid-State Electronics,* vol. 51, pp. 1047-1051, Jul 2007.
[41] F. Torricelli, *et al.*, "A Charge-Based OTFT Model for Circuit Simulation," *Ieee Transactions on Electron Devices,* vol. 56, pp. 20-30, Jan 2009.
[42] *Virtuoso® Simulator Circuit Components and Device Models Manual*: Cadence Design Systems, 2007.
[43] G. Horowitz, *et al.*, "Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors," *Journal of Applied Physics,* vol. 87, pp. 4456-4463, May 2000.
[44] "Virtuoso® Spectre® Circuit Simulator Reference," ed: Cadence Design Systems, Inc, 2004.
[45] "L-Edit 15 User Guide," ed: Tanner EDA Documentation.
[46] Y. H. Kim, *et al.*, "Ink-Jet-Printed Zinc-Tin-Oxide Thin-Film Transistors and Circuits With Rapid Thermal Annealing Process," *Ieee Electron Device Letters,* vol. 31, pp. 836-838, Aug 2010.
[47] S. Sambandan, "High-gain amplifiers with amorphous-silicon thin-film transistors," *Ieee Electron Device Letters,* vol. 29, pp. 882-884, Aug 2008.
[48] Y. C. Tarn, *et al.*, "An Amorphous-Silicon Operational Amplifier and Its Application to a 4-Bit Digital-to-Analog Converter," *Ieee Journal of Solid-State Circuits,* vol. 45, pp. 1028-1035, May 2010.
[49] H. Marien, *et al.*, "A Fully Integrated Delta Sigma ADC in Organic Thin-Film Transistor Technology on Flexible Plastic Foil," *Ieee Journal of Solid-State Circuits,* vol. 46, pp. 276-284, Jan 2011.
[50] Y. P. Tsividis and P. R. Gray, "INTEGRATED NMOS OPERATIONAL-AMPLIFIER WITH INTERNAL COMPENSATION," *Ieee Journal of Solid-State Circuits,* vol. 11, pp. 748-753, 1976.
[51] A. Moini, "Op-amps on flexible substrates with printable materials," 2009.