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A novel 10-bit hybrid ADC using Flash and Delay Line Architectures

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A novel 10-bit hybrid ADC using Flash and Delay Line Architectures

by

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THESIS

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

THE UNIVERSITY OF TEXAS AT AUSTIN

May 2011

Dedicated to my parents, and my lovely sister, who have always supported me in all my endeavours.

Acknowledgments

This thesis is an important milestone in my life. It represents the fulfillment of my childhood dream of completing a graduate degree in engineering. There have been several individuals who in one way or another, contributed and extended their valuable assistance in the preparation and completion of this study.

First and foremost, I would like to express my utmost gratitude to my thesis advisor, Prof. Jacob A. Abraham for allowing me to be a part of his research team. Ever since I met him, he has been my role model in paving the way for my research. He gave me a deep insight into the topics like data convertors and came up with the thesis topic. It was only his constant patience and steadfast encouragement, both academically and emotionally, that I could finish this challenging pursuit. He also gave me the opportunity to intern at two companies only to enhance my knowledge. I hereby extend many a thanks for his relentless support and guidance in all forms. I would also like to express my gratitude to Prof. Mark McDermott for providing me with vital inputs during the course of my research work, which were very helpful in compiling my work and writing the thesis.

I am also indebted to all the students in the Computer Engineering Research Center (CERC) and especially Chaoming Zhang, Prof. Abraham's

PhD student, for always being there to clear my doubts related to the topic. I would also like to thank my colleagues, Rituraj Singh and Ameya Chaudhary, for all the imperative discussions and interactions during the long hours in the lab. I thank Andrew Kieschnick for providing such wonderful computing resources. Also, I really appreciate the kind help from Debi Prather and Melissa Campos in all the administrative procedures related to the university.

Lastly and most importantly I would like to thank my lovely family back in India. Words don't do justice to what I feel, but it is totally their unconditional love and support that kept me going in these years away from home. I dedicate my thesis to my mom, dad, younger sister and grand parents.

Thank you dear Lord for answering my prayers and giving me the strength to complete this challenge.

Statement of Originality and Academic Integrity

I certify that I have completed the online ethics training modules[1], particularly the Academic Integrity Module[2], of the University of Texas at Austin - Graduate School. I fully understand, and I am familiar with the University policies and regulations relating to Academic Integrity, and the Academic Policies and Procedures.[3]

I also attest that this thesis is the result of my own original work and efforts. Any ideas of other authors, whether or not they have been published or otherwise disclosed, are fully acknowledged and properly referenced.

I also acknowledge the thoughts, direction, and supervision of my research advisor, Prof. Jacob A. Abraham.

[1]The University of Texas at Austin - Graduate School's online ethics training modules, http://www.utexas.edu/ogs/student_services/ethics/

[2]The University of Texas at Austin - Graduate School's online ethics training on academic integrity, http://www.utexas.edu/ogs/student_services/ethics/academic.html

[3]The University of Texas at Austin, General Information, 2006-2007, Chapter 11, Sec. 11 - 101, http://www.utexas.edu/student/registrar/catalogs/gi06-07/app/appc11.html

A novel 10-bit hybrid ADC using Flash and Delay Line Architectures

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This thesis describes the architecture and implementation of a novel 10-bit hybrid Analog to Digital Converter using Flash and Delay Line concepts. Flash ADCs employ power hungry comparators which increase the overall power consumption of a high resolution ADC. High resolution flash also requires precision analog circuit design. Delay line ADCs are based on digital circuits and operate at low power. Both Flash based ADCs and delay line based ADCs can be used to get a fast analog to digital conversion, but with limited resolution. These two approaches are combined to achieve a 10-bit resolution (4 bits using Flash and 6 bits using delay line) without compromising on speed and maintaining low power operation. Low resolution of Flash also helps in reducing the analog circuit design complexity of the voltage comparators. The ADC was capable of running at 100M samples/s, with an ENOB of 8.82 bits, consuming 8.59mW at 1.8V.

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Chapter 1

Introduction

Analog to Digital (ADC) and Digital to Analog (DAC) converters are the link between the analog world of sensors and transducers and the world of Digital Signal Processing (DSP) and data handling. With the advancement in the IC fabrication technologies and massive scaling of devices, it is now possible to carry out very advanced data processing at a low cost. But the real world is analog and almost all of the real signals are continuous time and continuous amplitude signals. DSP on the other hand, can only work on discrete time and discrete amplitude signals. There is, thus a need for conversion of signals between the analog and digital domains.

Data converters is an area that has been widely researched on for many years and a large number of ADC and DAC architectures have been invented. Depending on the final application, these data converters differ in resolution, speed and power consumption.

A look at the design of Analog to Digital Converters reveals the fact that most of the ADCs have been implemented as analog circuits. Traditional ADCs like Flash [1], Successive Approximation [1], Integrating type [1] and Sigma Delta [1] have been implemented as hard-core analog systems, where

conversion is done by direct comparison of the analog voltage with a reference voltage level.

A Flash ADC is extremely fast and simple as compared to many other types of ADCs. It requires a huge number of comparators in comparison to other ADCs, especially as the precision increases. A Flash converter requires 2^n - 1 comparators for an n-bit conversion. The size and cost of all those comparators limits the resolution of Flash converters to 4 to 6 bits. 8-bit flash ADCs have also been built, but they require very fine comparator designs to overcome the issues of offset, and even then, they suffer from non-linearity, and high power consumption. In place of these comparators, most other ADCs substitute more complex logic, which can be scaled more easily for increased precision. Recently, offset calibration has been introduced in flash ADC designs. Instead of properly designing the analog circuit (which actually means increasing the component sizes to suppress variation) the offset is removed during use. Due to the heavy calibration effort, the design have been limited to 4-bits.

Even though data converters has been an active area of research for a very long time, most ADCs implemented to date have been analog systems. In an analog system, bandwidth is limited by device and element performance and by the parasitics introduced. Thermal noise generated in active and passive components limits the dynamic range of an analog signal. A digital circuit approach over traditional analog ADC architectures is particularly important in deep sub-micron integrated circuit processes. These processes are optimized

for digital signals, where delay and timing are the focus rather than voltage levels. Accordingly, the systems developed using such technologies can process, compare and analyze time much more robustly than voltage levels. In addition, certain digital circuit families consume extremely small static power as compared to the power-hungry voltage amplifiers used in voltage comparison architectures. The other advantage of such ADCs will be their scalability. It is a well known fact that the performance of voltage comparison circuitry in integrated circuits is affected adversely by fabrication process scaling; however, timing comparison is not affected and moreover becomes even more power efficient as technology scales.

Given the limitations described above, a new architecture of analog to digital converters, namely, delay line based ADC [2],[3],[4] has been developed. It is a purely digital circuit which first converts the input voltage to a delay, and then uses a delay line to convert the delay into a digital word. Since it uses digital gates, it is inherently fast, scalable and requires low power and very small silicon area. The ADCs developed so far using this technique have been limited to a low resolution of 6 bits. To add an additional bit of resolution, the number of delay elements need to be doubled. This reduces the linearity of the ADC as the resolution is increased. New ways of increasing the resolution are thus required.

To overcome the problem of low resolution, flash and delay line based techniques are combined in this thesis to achieve a 10 bit resolution. The upper 4 bits are taken from a 4 bit Flash ADC while the lower 6 bits come from the

delay line ADC. This requires just 15 comparators in the design as opposed to 1023 required for a 10-bit Flash ADC. The area and power consumption of this ADC is therefore very small. Since both the architectures are fast, the overall speed of the ADC is also quite good.

The thesis is organized as follows. Chapter 2 describes the fundamentals of analog to digital conversion using flash and delay line architectures, and compares them for their speed, resolution, power and other metrics. Implementations of these architectures as well as any hybrid structures are also discussed. Chapter 3 outlines the architecture and implementation of the proposed hybrid Analog to Digital converter using Flash and Delay Line concepts. Chapter 4 looks at the static and dynamic characteristics of the hybrid ADC. Chapter 5 concludes with some pointers for future research in this area.

Chapter 2

Flash and Vernier Delay Line ADCs

This chapter discusses the architecture, implementation, applications and benefits of the two Analog to Digital conversion topologies, namely Flash and Vernier Delay Line ADCs, which are used to make this hybrid ADC. Previous work done in Flash and delay line ADC areas, along with any Hybrid ADCs developed using these concepts are also discussed.

In most analog-to-digital converters, the input analog voltage is converted into a digital code by an explicit voltage comparison [5], which is the basis for Flash ADCs . However, when integrated circuit fabrication technologies reach the deep-submicrometer regime, circuits that process analog voltage signals encounter scaling impediments [6], [7]. In particular, due to supply voltage reduction, the voltage domain is becoming noisier. In addition, although the new submicron processes have natural low V_t and negative V_t devices, the available voltage headroom is still very small, because of the relatively high threshold voltages, which makes the design of sophisticated analog architectures very challenging. On the positive side of scaling, with rise and fall times in the order of 10 ps, the switching characteristics of MOS transistors offer excellent timing accuracy at high frequencies. A new design

paradigm with deep-submicrometer CMOS technologies is possible, in which the time-domain resolution of a digital signal edge transition is superior to the voltage resolution of an analog signal [4]. This, along with considerations of chip area and power dissipation, gives rise to an upcoming trend to digitize part of or even the whole mixed-signal blocks [7]. These encourage us to study ADC structures based on digital blocks and compatible with scaling. Functionally, ADCs are quite similar to time-to-digital converters (TDCs) [8], which are used to quantize time intervals in applications such as phase-locked loops [4]. A digital delay-line-based TDC approach has recently become attractive, particularly for deep-submicrometer technologies [7].

The basic outline of the implementation of these two approaches for analog to digital conversion, and also a comparison among them for speed, resolution, die area and power requirements is discussed below.

2.1 Flash ADCs

Flash ADCs (also known as a parallel or Direct conversion ADCs) are the fastest type of analog-to-digital converters. Flash ADCs use a linear voltage ladder with a comparator at each step of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are made using resistors; however modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital encoder, which converts the inputs into a binary value.

2.1.1 Architecture and Implementation

Flash ADCs are made by cascading high-speed comparators. Figure 2.1 shows a typical Flash ADC block diagram. For an N-bit converter, the circuit employs $2^N - 1$ comparators. A resistive-divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a '1' when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is '0'. If the analog input is between V_{X4} and V_{X5}, comparators X_1 through X_4 produce '1's and the remaining comparators produce '0's. The point where the code changes from ones to zeros is the point at which the input signal becomes smaller than the respective comparator reference-voltage levels. This architecture is known as thermometer code encoding. This name is used because the design is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code.

The comparators are typically a cascade of wideband low-gain stages. They are low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. The comparators are designed for low-voltage offset, so that the input offset of each comparator is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code that is not representative of a thermometer

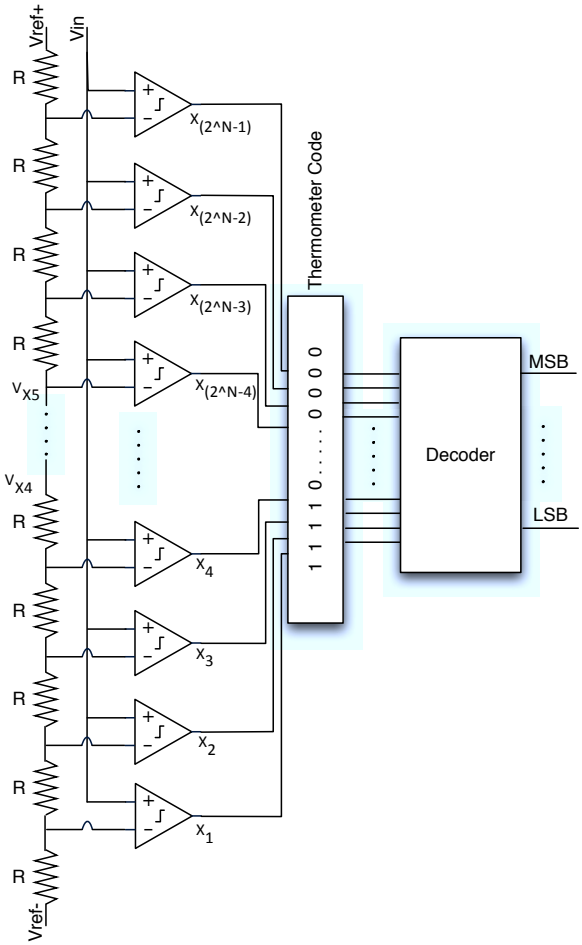

Figure 2.1: Flash ADC Architecture

code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a 1 or a 0.

The comparators are possibly preceded by an amplification stage. The reason to add an amplifier is twofold: it amplifies the voltage difference and therefore suppresses the comparator offset, and the kick-back noise of the

comparator towards the reference ladder is also strongly suppressed. Typically, designs from 4-bit up to 6-bit, and sometimes 7-bit are produced.

Recently, offset calibration [9] has been introduced in the flash ADC designs. Instead of properly designing the analog circuit (which actually means increasing the components sizes to suppress variation) the offset is removed during use. A test signal is applied and the offset of each comparator is calibrated to below the LSB size of the ADC. Due to the heavy calibration effort the designs are mostly limited to 4-bits.

A recent improvement in the design of flash ADCs is the integration of error correction algorithms [10] to address random errors in the digital output. When the ADC is used in harsh environments or constructed in very advanced submicron integrated circuit processes, there is a heightened risk of a comparator randomly outputting a wrong code. Bubble error correction is a digital correction mechanism that will prevent a comparator, that has tripped high, from outputting a high code if it is surrounded by comparators that have not tripped high.

2.1.2 Benefits and Drawbacks

Flash converters are extremely fast compared to many other types of ADCs like Pipelined, Successive Approximation, Sigma Delta ADCs [1], which usually narrow in on the correct answer over a series of stages. Compared to these, a Flash converter is also quite simple and, apart from the analog comparators, only requires logic for the final conversion to binary.

A Flash converter requires a huge number of comparators compared to other ADCs, especially as the precision increases. A Flash converter requires $2^n - 1$ comparators for an n-bit conversion. The size and cost of all those comparators makes Flash converters generally impractical for precisions much greater than 8 bits (255 comparators). Although 9 and 10 bit Flash ADCs which consume a lot of power have been implemented, most other ADCs substitute more complex logic in place of these comparators, which can be scaled more easily for increased precision.

2.1.3 Applications

Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters consume considerable power, have relatively low resolution, and can be quite expensive. This limits them to high-frequency applications that typically cannot be addressed any other way. Typical applications include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives [1]. More often the flash ADC is embedded in a large IC containing many digital decoding functions. Also a small flash ADC circuit may be present inside a Delta-sigma modulation loop [1].

2.2 Vernier Delay Line based ADCs

In contrast to the traditional ADCs where voltage levels are compared, delay line based ADCs compare the time difference between different travelling

waves. This underlying concept makes the ADC much more power efficient. The advantages of these time domain Analog to Digital converters over traditional converters are particularly important in deep submicron Integrated Circuit processes. These processes are optimized for digital signals, where delay and timing are the main focus, rather than voltage levels. Thus, systems built using such processes can process, compare and analyze timing much more robustly than voltage levels [2]. In addition to being robust, these digital processes consume very small static power as compared to the power hungry voltage comparators in the traditional architectures. Another advantage of a digital circuit is scalability. It is a well known fact that the performance of voltage comparison circuitry is perversely affected by fabrication process scaling. Scaling lowers the available voltage swings in analog circuits, fundamentally limiting the achievable SNR. The intrinsic voltage gain of devices also decreases with scaling. However, timing comparison is not affected by process scaling, and moreover it becomes even more power efficient.

2.2.1 Architecture and Implementation

Functionally ADCs are similar to time-to-digital converters (TDC) [4], which are used to quantize time intervals in applications such as phase-locked loops. A digital delay line based TDC approach has recently become attractive, particularly for deep submicron technologies. The basic structure consists of buffers and flip-flops, as shown in Figure 2.2. Initially, all the buffers are reset to "0". Then a rising edge is fed into 'Start' and propagates along the delay

line. After a while, 'Stop' goes high and triggers the flip-flops to sample the delay line, which produces a thermometer code. The number of 1s in the codeword provides a measure of the delay between 'Start' and 'Stop', with a resolution of D, which is the delay per buffer. The vernier structure in Figure 2.3 is often used to achieve a higher resolution. Each stage reduces the delay between 'Start' and 'Stop' rising edges by δ, i.e., the difference between the two delay cells, which leads to a time resolution of δ. Other advanced structures include the pulse-shrinking delay line and the local time interpolation technique.

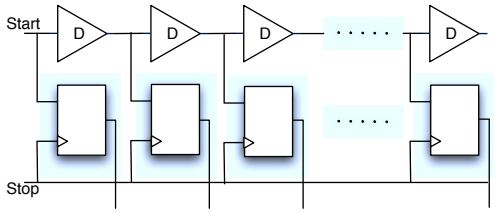

Figure 2.2: Delay Line based TDC Architecture

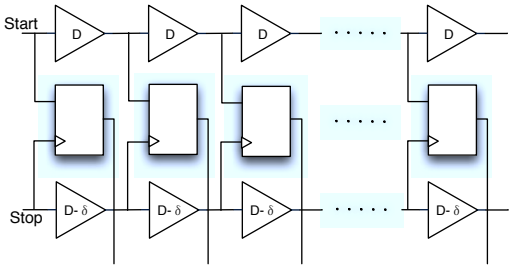

Figure 2.3: Vernier Delay Line based TDC Architecture

In light of the similarity between ADCs and TDCs, a straightforward

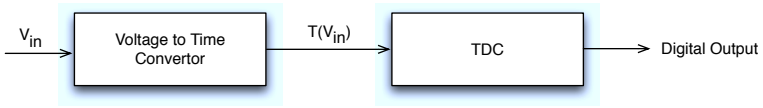

Figure 2.4: Voltage-to-time-to-digital Converter

ADC design is voltage-to-time-digital approach, as shown in Figure 2.4. The sampled input voltage Vin is first converted into a time window T(Vin), which is then quantized by a TDC. [4]

Another way of using delay lines is the voltage-to-delay-to-digital scheme [4]. The input signal modulates the delay per buffer instead of the time-window (Figure 2.5), and thus, the number of delay cells the signal passes through in a constant time window is proportional to the input voltage. This idea has been implemented in [11], where a 14-bit 10-KS/s ADC was developed.

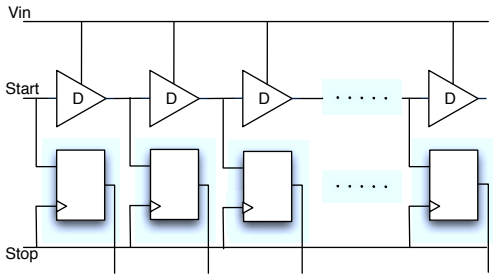

Figure 2.5: Voltage-to-delay-to-digital Converter

2.2.2 Benefits and Drawbacks

A major advantage of the delay-lined based structure lies in its all-digital implementation, which makes it compatible with technology scaling.

In addition, the delay-line structure introduces time-domain amplification into the design and potentially leads to better solutions. In particular, signal can be 'amplified' in the time domain by simply extending the time window, in contrast to voltage amplification involving complicated analog amplifiers. This is particularly attractive to weak-signal acquisition. Another advantage of its all-digital nature is its low power requirement.

Although a delay line based ADC offers a good technique of analog to digital conversion, its speed is dependent on its resolution. An increase in 1 bit of resolution thus doubles the time required for conversion. High resolution low speed delay line A/D converters can also be built, but with an increase in the length of the delay line, the process and temperature variations effect the linearity of the conversion. This limits the delay line converters to 4 to 6 bits of resolution.

2.2.3 Applications

Delay Line based ADCs are relatively new in the field of data converters and have been used in the area of weak signal acquisition, such as integrated sensors. Advanced systems (automobiles, medical and other electronic devices) have come to use multiple sensors in recent years, and the number is expected to increase even more in the future. Since the signal level is generally very low, these weak signals must be amplified several hundred times by an analog circuit. On the other hand, user requirements for sensors have become more and more demanding, including the need for high performance and lower cost.

Delay line based ADCs address the problems of scaling, self-correction and reliability of these sensors based on their digital nature. [11]

2.3 Architectural Comparison

The principal trade-offs among these two ADC alternatives are described below.

2.3.1 The time it takes to complete a conversion (conversion time)

For flash converters, the conversion time does not change materially with increased resolution. The conversion time for vernier delay line based ADCs, however, doubles with every bit increase in resolution.

2.3.2 Component matching requirements in the circuit

Flash ADC component matching typically limits resolution to around 8 bits. Calibration and trimming are sometimes used to improve the matching available on chip. Component matching requirements in Flash ADC double with every bit increase in resolution. In a delay line based ADC, since majority of the circuit is based on digital gates, the dependence of resolution on component matching is not a major issue.

2.3.3 Die size, cost, and power

For flash converters, every bit increase in resolution almost doubles the size of the ADC core circuitry. The DC power also doubles. This is

mainly because of the power hungry comparators used in Flash. In contrast, in a digital delay line ADC, although the length of the delay line doubles with each bit increase in resolution, and the dynamic power consumption of the circuit may also increase, but the DC power does not increase as much, because majority of the circuit is digital in nature. An increase in resolution thus increases the cost of a Flash based ADC more as compared to a delay line based ADC.

2.4 Hybrid ADCs

A new type of ADC architecture, called the Folding ADC [12] was invented, to reduce the number of comparators by adding a folding circuit in front. Instead of using the comparators in a Flash ADC only once, during a ramp input signal, the folding ADC re-uses the comparators multiple times. If a m-times folding circuit is used in an n-bit ADC, the actual number of comparator can be reduced from $2^n - 1$ to 2^{n-m} (there is always one needed to detect the range crossover).

A vernier delay line based hybrid ADC has been implemented in [3]. In this 9-bit ADC, a delay line based ADC is used to get 8 bits of resolution. Voltage comparators are used to get the MSB of the digital output word. If the input voltage signal is greater than $V_{fs}/2$, the MSB is 1 otherwise the MSB is 0. Voltage to time conversion is done using a ramp-down generator. A two level vernier delay line is used to get the 8-bit resolution. The ADC was capable of running at a speed of 5Msps, with a DNL of 0.5 LSB and INL

within -0.22 and 0.56 LSB and consumed 15mW of power.

2.5 Conclusion

For applications requiring modest resolutions, typically up to 8-bits, at sampling frequencies in the high hundreds of MHz, the flash architecture used to be the only viable alternative. But with time domain processing, delay line ADCs is a promising technique, especially for low power operation.

Chapter 3

Proposed ADC Architecture and its Implementation

A hybrid 10-bit ADC, designed to run at 100 Msps, is implemented in 180nm technology node, using Flash and Vernier delay line architectures. In this architecture, as shown in the block diagram (Figure 3.1), the most significant 4 bits of the ADC are realized using a 4-bit flash ADC, and the lower 6 bits of resolution are achieved using a 6-bit vernier delay line based ADC. A sample and hold (S/H) circuit samples the input voltage and holds it during the conversion time of the ADC. The input voltage for the 6-bit ADC block is generated by the subtraction of the analog output voltage of the DAC from the sampled input voltage. 4-bit and 6-bit Wallace tree encoders are used to generate the 10-bit digital output of the hybrid ADC from the thermometer codes given by the 4-bit Flash and 6-bit delay line ADC respectively. Since the Flash ADC is used to get 4 bits of resolution, the number of comparators required is just 15 (2^4 - 1), and since the delay line based ADC is mostly digital in nature, the static power consumption of this 10-bit ADC is kept to a minimum. The architecture and circuit topologies used in the proposed ADC are discussed below.

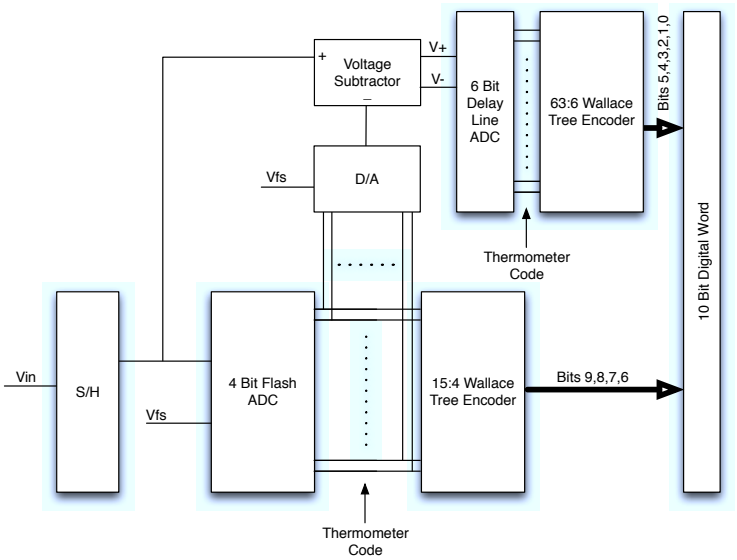

Figure 3.1: Block Diagram of Proposed ADC

3.1 Sample and Hold

Sample-and-hold (S/H) is an important analog building block which is used to sample the analog input signal and hold the sampled value over the entire conversion time for subsequent processing. To limit the errors due to charge injection and clock feedthrough, a single-ended bottom plate switched capacitor sample and hold circuit [13] was used in this ADC.

3.2 Flash ADC

This 10-bit hybrid ADC can be visualized as a folding type ADC with the 4-bit Flash acting as the coarse analog to digital converter. A Flash ADC, as described in Section 2.1.1, uses explicit voltage comparison for analog to

digital conversion. For a 4-bit Flash, 15 comparators are required. The Flash block has to distinguish only 16 levels in the entire full scale range (FSR) of 1.8V. As can be seen in Table 3.1, which lists the transition points of the Flash ADC, the LSB_{4-bit} required from the Flash ADC is 112.5mV, which is quite high. This reduces the design constraints on the Flash ADC to some extent, and a very precise analog design is not required for the comparators. But for an overall 10-bit resolution over the 1.8V FSR, the LSB_{10-bit} is 1.75mV, so for a good linear performance of the ADC, the offset errors of Flash are kept under $LSB_{10-bit}/4$, i.e., under 0.43mV.

Table 3.1: 4-bit Flash transition points

Transition Point	Thermometer Code
0.1125V	000000000000001
0.225V	000000000000011
0.3375V	000000000000111
0.45V	000000000001111
0.5625V	000000000011111
0.675V	000000000111111
0.7875V	000000001111111
0.9V	000000011111111
1.0125V	000000111111111
1.125V	000001111111111
1.2375	000011111111111
1.35V	000111111111111
1.4625V	001111111111111
1.575V	011111111111111
1.6875V	111111111111111

The sampled signal coming from the sample and hold block is fed into the 4 bit Flash as well as the delay line block (Figure 3.1). The four bit flash consisting of 15 comparators, produces a 15 bit thermometer code. The thermometer code is fed into a 15:4 Wallace Tree Encoder to produce the most significant 4 bits of the ADC. The thermometer code is also used to select a subtraction voltage for the voltage subtractor using a Digital to Analog converter (DAC). The comparator used in the Flash ADC is described in the following paragraphs.

3.2.1 Flash Comparator Design

A comparator is a circuit which makes the decision whether the input voltage is greater than the reference voltage and gives a 1/0 output accordingly. Since offset errors of the comparators in the 4-bit Flash need to be kept low, a good comparator design is required. The topology shown in Figure 3.2 is used to design the comparator for this ADC. A regenerative sense-amplifier latch is used as the comparator. To suppress the errors introduced due to offset and kick-back noise of the latch, a pre-amplifier is used. The pre-amplifier and sense amplifier latch designs are described below.

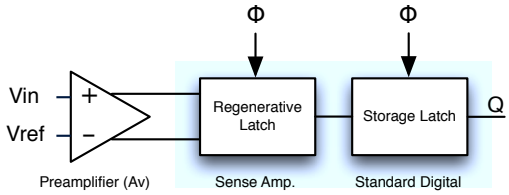

Figure 3.2: Block Diagram of Comparator used in Flash ADC

3.2.1.1 Pre-Amplifier

A simple single stage differential amplifier, as shown in Figure 3.3 is used as the pre-amplifier for the comparator. The transistors in the differential amplifier are sized up to reduce the offset of the amplifier itself. Transistors M1 and M2 form the differential pair, with M3 and M4 acting as the diode connected active load. The drawn length of these transistors is made long to achieve a high output resistance for an increased gain. Transistors M5 and M6 act as diode clamps for improved overdrive recovery [14].

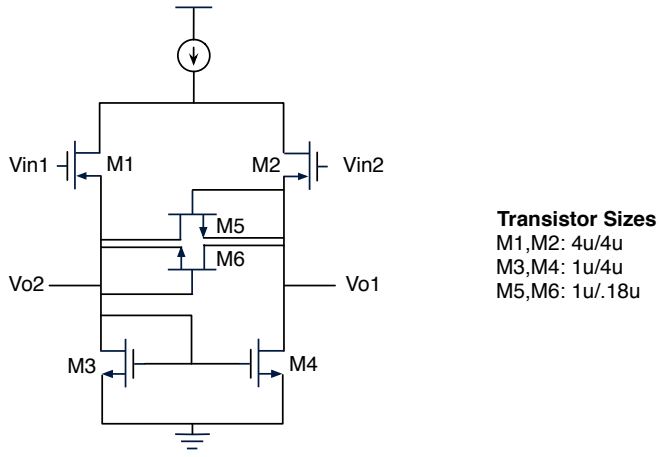

Figure 3.3: Pre-amplifier for the comparator

3.2.1.2 Sense Amplifier based Latch

The sense amplifier based latch used for making the comparison between the input signal and the reference voltage is shown in Figure 3.4. The differential inputs V_{o1} and V_{o2} of the latch come from the pre-amp. When the clk input is low, the transistors M7 and M8 are ON and they pre-charge the

outputs of the cross-coupled inverters to VDD. Transistor M9 is OFF at this time, so the circuit is cutoff from ground.

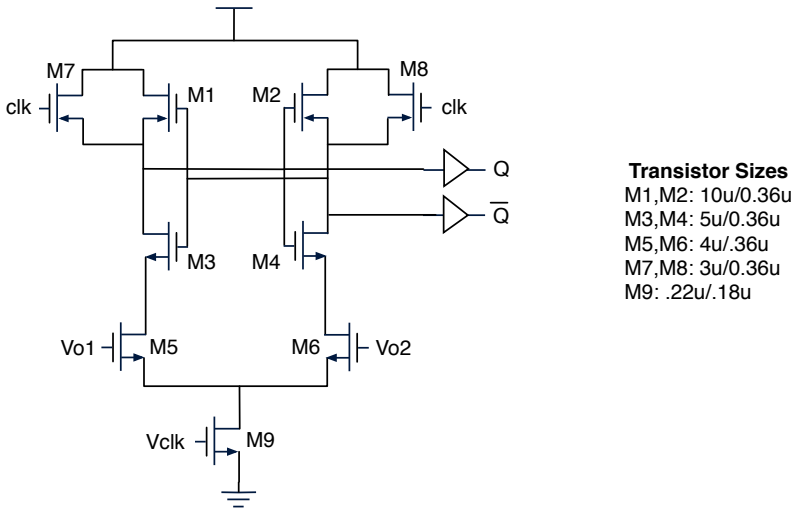

Figure 3.4: Sense Amplifier based Latch for the comparator

When Vclk goes high, transistor M9 turns ON, thereby connecting the sources of M3 and M4 to ground. Also, M7 and M8 turn OFF, thus the outputs of the cross-coupled inverters are no longer connected to VDD. Since both the cross-coupled inverters have a high output, this circuit is in a very unstable equilibrium, and the output of one of these two inverters will try to go low. This happens due to the difference in the levels of V_{o1} and V_{o2}. If V_{o1} is slightly greater than V_{o2}, more current will flow in the left inverter, and therefore, its output node will transition to ground faster than the right inverter. Due to the cross-coupling, a slight change in equilibrium will quickly make the output of left inverter transition to ground. The higher the difference

between the inputs, the faster the outputs will be resolved. The preamplifier, by amplifying the difference between Vin and Vref, helps to resolve the outputs quickly.

3.3 Digital to Analog Converter (DAC)

The 4-bit Flash ADC converts the input voltage into a 15-bit thermometer code. If the FSR is 1.8V, the 4-bit Flash can distinguish between 15 levels which are separated by 112.5mV. The 6-bit Vernier Delay Line ADC now needs to resolve in between these 15 levels, thus, the FSR for the delay line ADC is 112.5mV. To get the input voltage for the Vernier Delay Line ADC, the analog voltage corresponding to the digital output of the 4-bit Flash is subtracted from the input voltage. The subtracted voltage then lies in the range of 0 - 112.5mV, and is used by the fine vernier delay line ADC to get the lower 6 bits. A Digital to Analog Converter is needed to convert the digital output of Flash into an analog voltage for subtraction. Since the LSB for the DAC is 112.5mV, which is quite high, a simple resistor ladder based DAC gives a good linearity and a precise design is not required.

Figure 3.5 shows the architecture of the digital to analog conversion circuit. The thermometer code generated by the Flash ADC is used by the DAC as its input. Each of the 15 bits of the thermometer code is XOR-ed with its immediate neighbouring bits. Bit $T<1>$ is XOR-ed with VDD and bit $T<15>$ is XOR-ed with ground. The XOR gate with the opposite inputs will give a high output. A thermometer code consists of a series of '1's followed

by a series of '0's. The XOR gate where the series of '1's end and the series of '0's begin will therefore give a high output. All the other XORs will give a low output.

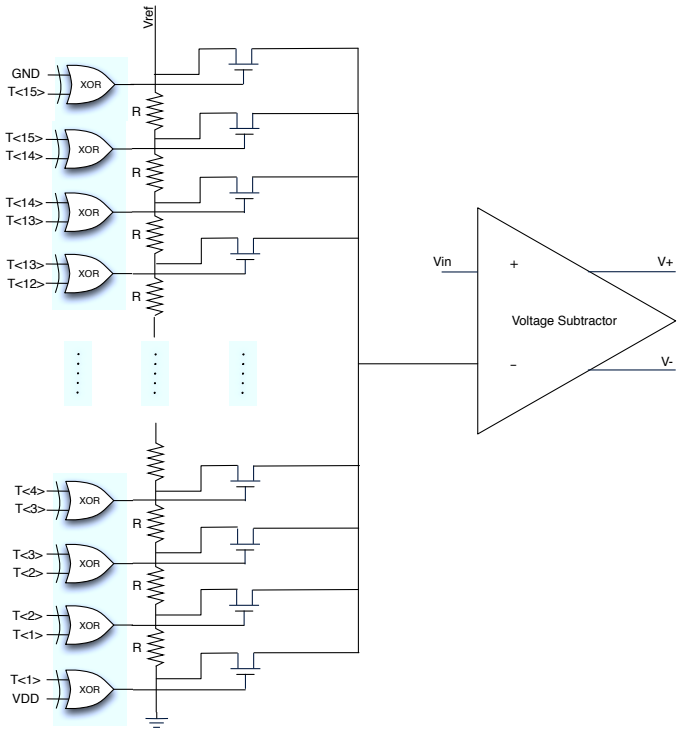

Figure 3.5: Digital to Analog Converter

The XOR gate which gives a high output will turn one of the CMOS switches (shown as an nMOS) connected to the reference ladder ON, and provide a reference voltage to appear on the negative terminal of the voltage subtractor. As an example, lets say the input voltage is 1.6V. In the 4 bit Flash, the voltage of 1.6V will give an output of '011111111111111' (Table 3.1), which when applied to the DAC, causes the XOR connected to $T<14>$ and $T<15>$,

giving a high output. A voltage equal to 1.575V will appear at the negative terminal of the voltage subtractor which results in a voltage equal to 1.6V - 1.575V = 25mV at the output of the voltage subtractor. The differential output voltage of the subtractor is applied to the vernier delay line ADC, which produces the lower 6 bits of the output.

3.4 Voltage Subtractor

The voltage subtractor is used to subtract the voltage generated by the Digital to Analog converter from the input voltage signal. The voltage subtractor consists of a differential amplifier with negative feedback. The closed loop gain of the differential amplifier is set to 4. A differential output with a common mode of 0.9V is created by the voltage subtractor. The maximum difference of the inputs of the voltage subtractor can be 112.5mV and since the gain of the subtractor is 4, the output of the subtractor can go from 0 to 450mV.

3.5 6-bit Vernier Delay Line ADC

A vernier delay line based Analog to Digital converter is used to get the low 6-bits of resolution of the hybrid 10-bit ADC. Figure 3.6 gives the block diagram of the vernier delay line ADC. The differential input voltage coming from the subtractor is given to a voltage controlled variable delay block, which converts the input voltage into a delay between the two pulses. Two opposite pulses (one rising and one falling) are fed into two variable delay transmission

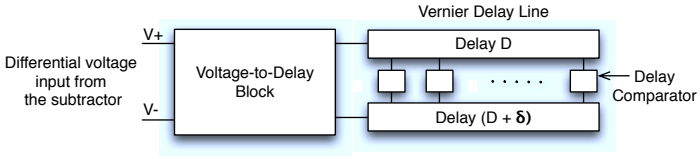

Figure 3.6: Block Diagram of the Vernier Delay Line ADC

lines. These two pulses are delayed with respect to each other based on the input voltage, and come out as delayed pulses. The delayed pulses are then fed into the vernier delay line with a constant delay. Delay comparators compare the delay between these two pulses at equal distances along the delay line. As long as the delay between these two pulses is greater than a fixed threshold, the output of the delay comparators is '1'. The two delayed pulses travel through the vernier delay line, and the delay between them keeps decreasing. At one point in the vernier delay line, the difference in the delays becomes less than the threshold, and the subsequent comparators give a '0' output. A thermometer code similar to that generated by the Flash ADC is generated, which is then converted into a 6-bit binary output using a 63:6 Wallace Tree encoder. All these blocks are discussed in detail below.

3.5.1 Voltage to Delay Block

After the sample and hold circuitry, the linearity of the voltage to delay block determines the linearity of the Vernier delay line ADC [2]. All previous delay line based ADC designs change the delay by varying the power supply of the inverters in the delay line [15]. A PMOS and NMOS current starved

interleaved method [2] is used for voltage to delay conversion, which produces enough linearity for the 6-bit ADC. The schematics are shown in Figure 3.7.

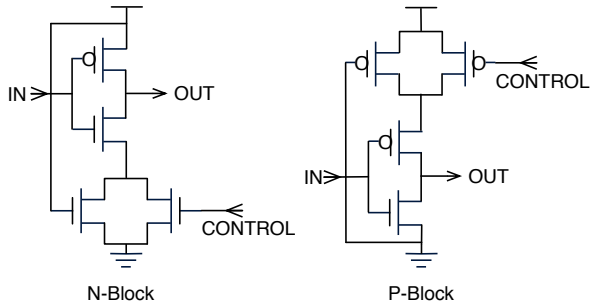

Figure 3.7: Schematics of N-block and P-block of voltage to delay block

The N block accelerates the pulse propagation under a high control voltage, while the P block does the opposite. The sampled signal is applied to the CONTROL pin. A pulse passes through the blocks, and the delay time is determined by the sampled signal levels.

The overall voltage to delay block is shown in Figure 3.8. The differential voltage output of the voltage subtractor is applied to the P and N blocks. The signal V+ can lie anywhere between 900mV and 1125mV and the signal V- can lie between 675mV and 900mV. In both these ranges, the nMOS and pMOS are ensured to be out of sub-threshold region. For a high voltage level, the N block will be a faster path and the P block will be a slower path. The N block in the upper transmission line is connected to V+ and the P block is connected to V-. Both P and N blocks in the upper transmission line speed up the pulse, whereas both P and N blocks slow down the pulse travelling in

the lower transmission line. This is because the N block is connected to V- and the P block is connected to V+ in the lower transmission line.

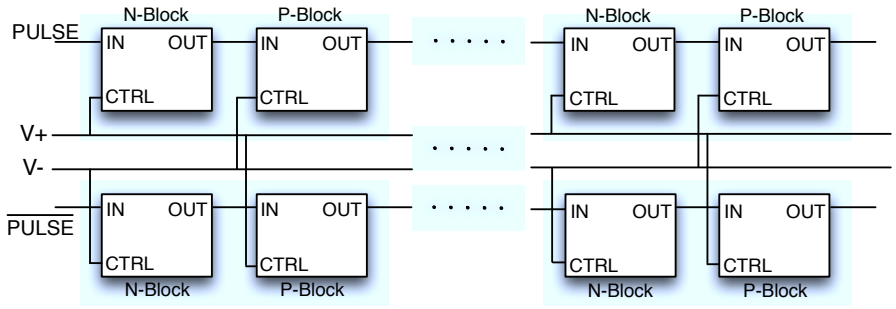

Figure 3.8: Interleaved N-block and P-block forming the Voltage to Delay Block

As the pulses travel further in these variable delay lines, the delay between them keeps on increasing. The time difference between these two paths varies linearly with the input voltage level. In this way, in a wide input voltage range, a linear relationship is formed between the analog voltage and the pulse delay difference. The linearity of this voltage to delay block is enough to achieve a 6-bit resolution.

3.5.2 Vernier Delay Line based delay to digital block

The two pulse signals coming from the Voltage to Delay block are applied to a vernier delay line Figure 3.6 after the conversion of the input voltage to a delay. The Vernier Delay Line consists of two transmission line made of constant delay buffers. The delay of a buffer in one transmission line is D, and in the other transmission line, it is D + δ. After each delay stage in the

vernier delay line, the delay between the two pulses reduces by δ. For this ADC, δ is designed to be 8ps. At each buffer stage in the vernier delay line, a delay comparator is used to compare the two pulses. If the delay between them is larger than a preset threshold, the output of the comparator is '1'. As the pulses pass through the delay line, the delay between them keeps on decreasing. At one point, their delay goes below the threshold delay, and the output of the delay comparator goes to '0'. A thermometer code is created at the output of the Vernier Delay Line block, which is stored in standard D type flip flop registers, for use by a Wallace Tree for digital encoding. The design of the delay comparator used in the Vernier Delay Line is discussed below.

3.5.2.1 Delay Comparator

The delay comparator is the most important block in the vernier delay line based ADC. It is used to compare the delays between two signals, and give a 'high' output if the delay between them is more than a threshold value.

Figure 3.9 shows the circuit diagram of the Delay Comparator [2] used in the vernier delay line ADC. In phase I, the CLK input is low, so the capacitor C on node A is precharged to VDD, causing the output of the delay comparator to be '0'. In phase II, the CLK signal goes low. Now the cross-coupled latch circuit is free to move in any direction. The delayed signals from the Voltage to Delay Block are applied to inputs In1 and In2. Both In1 and In2 are 'high' at this time. First the signal In1 goes low, thereby causing the PMOS M6 to turn ON. Since the NMOS M7 is already ON, current flows through M6 and

M7, and tries to discharge the node A. After some time δ, the signal In2 also goes low, thereby switching the NMOS M7 OFF, and thus opening the path of A to ground. If the delay δ between the falling edges of In1 and In2 is greater than the threshold delay (designed to be 500ps in this case), the voltage at node A goes to ground and the output of the cross-coupled inverter flips to '1'. If the delay δ is smaller than 500ps, node A will not discharge completely, and thus the output of the comparator stays at '0'.

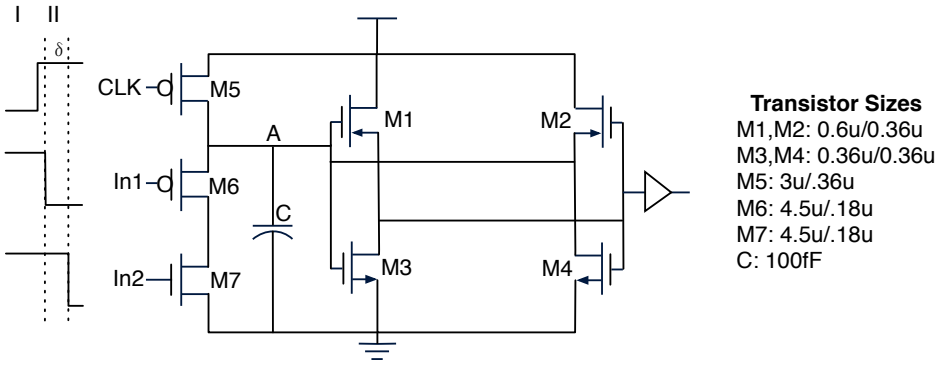

Figure 3.9: Delay Comparator for Voltage to Delay Block

3.6 Wallace Tree Encoders

There are 15 comparators in the Flash ADC and 63 comparators in the 6 bit Vernier Delay line ADC. The direct output of both these ADCs is a 15-bit and a 63-bit thermometer code, which needs to be converted to a 4-bit and a 6-bit binary code respectively. The encoder scheme is chosen as a Wallace tree structure, which is fast, and can efficiently solve the bubble error in the thermometer code [16]. The thermometer code consists of a string of

zeros followed by a string of ones (or vice-versa). A bubble error is a situation where a '1' may be found among the '0's, or vice versa, in the thermometer code. This usually results from the timing difference between clock and signal lines and from comparator offsets. A 15:4 Wallace Tree structure gives the high 4-bits of the 10-bit hybrid ADC, and a 63:6 Wallace Tree structure gives the low 6-bits of the ADC.

Chapter 4

Simulation Results

The 10-bit hybrid ADC was implemented in CMOS 180nm technology node using Cadence tools. The circuits were simulated using Spectre. The present chapter describes an account of the methodology used for simulation and the results achieved, in terms of differential and integral non-linearities (DNL and INL respectively), and the dynamic performance.

4.1 Simulation Methodology

The 10-bit ADC was simulated as a combination of two ADCs, i.e., the 4-bit Flash and the 6-bit Delay Line ADC, and the results were combined using MATLAB. To find the transfer function of these two ADCs, parametric sweeps were carried out in Analog Design Environment (ADE), in which the input analog voltage of these two ADCs was varied from 0 to V_{fs}. The V_{fs} for the Flash ADC is 1.8V, while that for the 6-bit Vernier Delay Line ADC is 112.5mV. OCEAN scripts (scripting language for Cadence) were written to run parametric sweeps in the background on multiple machines to decrease the turnaround time of the simulations. The OCEAN scripts dumped out the results as comma separated value (.csv) files, which were parsed in MATLAB

for post processing.

4.2 Simulation Results for the 4-bit Flash ADC

The Flash ADC was simulated in Cadence Analog Design Environment, with a sampling frequency of 100M samples/s. A very slow rail-to-rail (0V - 1.8V) ramp signal was used as the input to the Flash to get the transfer function. The transfer function of the 4-bit Flash ADC is highly linear as shown in Figure 4.1. The transition points of the 4-bit Flash ADC (Table 4.1), differ from the ideal transition points by atmost a few microvolts. The use of the high gain pre-amp highly reduced the non-linear effects by suppressing the offset of the latch, as well as the kickback noise.

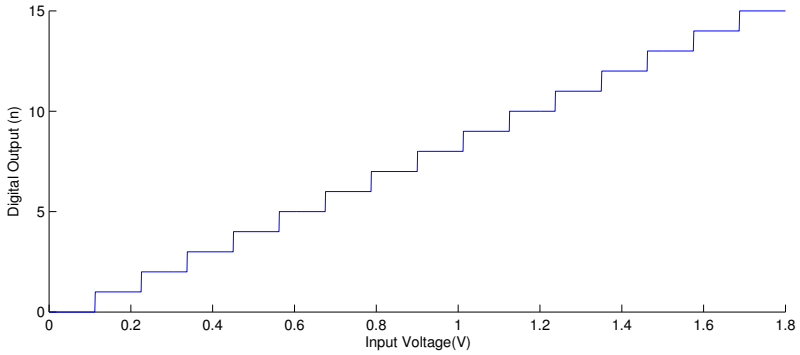

Figure 4.1: Transfer Function of 4-bit Flash ADC

Table 4.1: Transition Points of the 4-bit Flash ADC

Transition Point	Thermometer Code
0.113V	000000000000001
0.2255V	000000000000011
0.3377V	000000000000111
0.4502V	000000000001111
0.5627V	000000000011111
0.67525V	000000000111111
0.78757V	000000001111111
0.9002V	000000011111111
1.0127V	000000111111111
1.1252V	000001111111111
1.2377	000011111111111
1.3502V	000111111111111
1.4627V	001111111111111
1.5752V	011111111111111
1.6877V	111111111111111

The linearity of the Flash ADC can be gauged from its differential and integral non-linearities as shown in Figure 4.2. The performance of the 4-bit Flash ADC is highly linear, with the maximum and minimum DNL of 1.5 x 10^{-3} LSB and -2.5 x 10^{-3} LSB respectively and maximum and minimum INL of 1.9 x 10^{-4} LSB and -2.7 x 10^{-3} LSB respectively. The linearity of the Flash ADC is quite high owing to the low offset of the comparators and the high LSB of the Flash ADC.

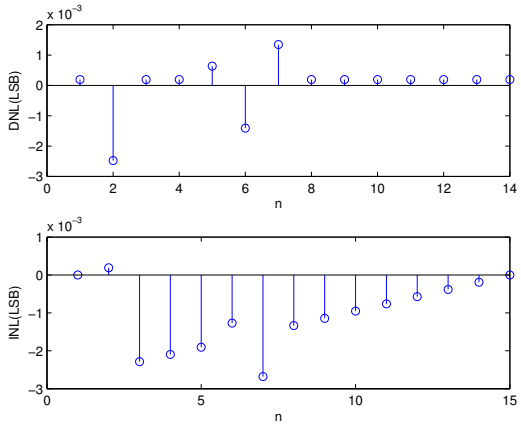

Figure 4.2: DNL and INL of 4-bit Flash ADC

The dynamic performance of the 4-bit Flash ADC is shown in Figure 4.3. It is possible to run this Flash ADC up to a speed of 500M Samples/s. It demonstrates an SNR of 26.78dB, an SNDR of 25.59dB and the effective number of bits (ENOB) equal to 3.94, for a 1MHz input signal. The overall power consumption of the 4-bit Flash ADC is 6.1mW with a 1.8V power supply.

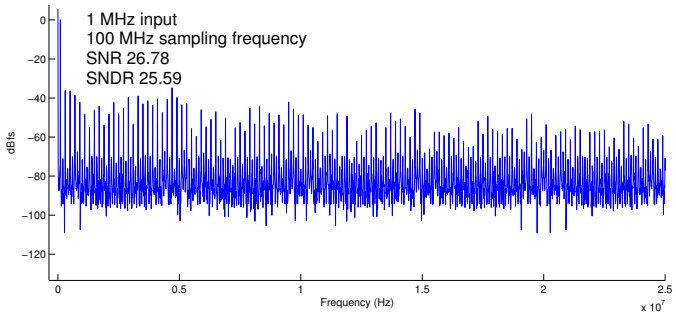

Figure 4.3: Frequency Response of 4-bit Flash ADC

4.3 Simulation Results for Voltage Subtractor

The 4-bit Digital to Analog converter converts the digital thermometer code from the 4-bit Flash ADC into an analog voltage. The level of the output voltage of the DAC is a multiple of 112.5mV. The LSB of the DAC (112.5mV) is quite large, so it is possible to get a very linear DAC, with very small offset. The output voltage of the DAC is to be subtracted from the sampled input voltage using a voltage subtractor. An opamp based voltage subtractor was implemented. The output of the voltage subtractor is bound between 0 and 450mV, as shown in Figure 4.4. The output of the voltage subtractor is very linear through the entire range (0-1.8V) of the input signal. A look at the transfer function of the voltage subtractor reveals the similarity of this hybrid ADC to the Folding type ADCs, where the same transfer function repeats periodically with the LSB of the course ADC (Flash in this case).

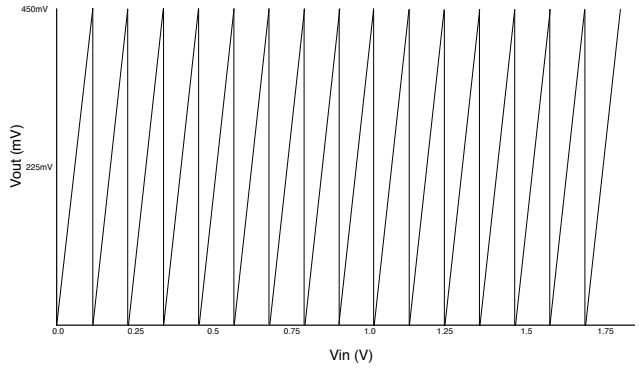

Figure 4.4: Transfer Function of Voltage Subtractor

4.4 Simulation Results for the 6-bit Vernier Delay Line ADC

The most important block in the vernier delay line ADC is the voltage to delay block. The linearity of this block determines the overall linearity of the ADC. A parametric sweep of delay vs input voltage was plotted, and was found to be linear over a wide range of voltages. The plot of delay vs input voltage for the voltage to delay block is shown in Figure 4.5. The linearity achieved is good enough for a 6-bit ADC.

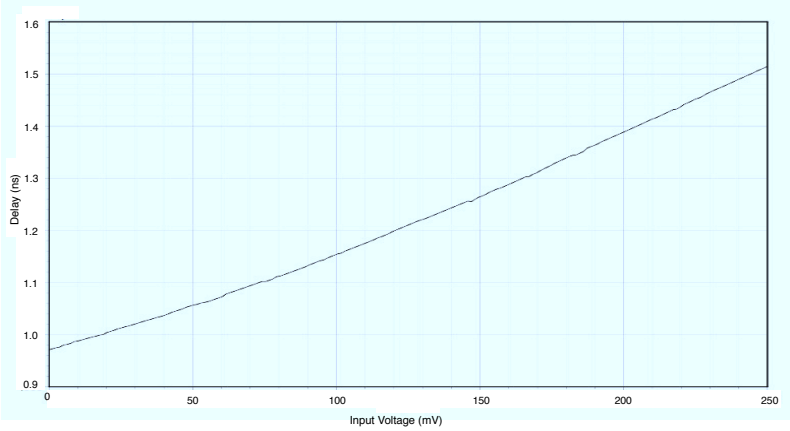

Figure 4.5: Transfer Function of Voltage to Delay Block

The transfer function of the 6-bit delay line ADC is shown in Figure 4.6. The slight non-linearity in the ADC comes from the non-linearity present in the voltage to delay transfer function. The transfer function of the subtractor and that of the delay line ADC therefore look similar. The non-linearity in

the ADC results in a maximum and minimum DNL of 0.22 LSB and -0.17 LSB respectively, and maximum and minimum INL of 2.13 LSB and -0.1 LSB respectively, as shown in Figure 4.7. The INL of the ADC is quite high, which tends to give rise to some harmonics in the frequency response of the ADC. This reduces the ENOB of the ADC.

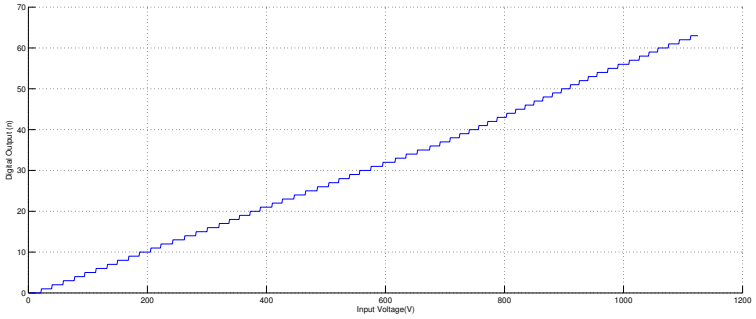

Figure 4.6: Transfer Function of 6-bit Vernier Delay Line ADC

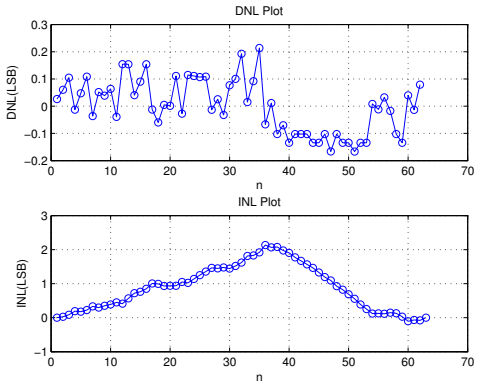

Figure 4.7: DNL and INL of 6-bit Vernier Delay Line ADC

The dynamic performance of the 6-bit Vernier Delay Line ADC is shown

in Figure 4.8. It is possible to run the vernier delay line ADC up to a speed of 150M Samples/s. The vernier delay line ADC showed an SNR of 37.818dB, SNDR of 29.9507 dB and effective number of bits (ENOB) equal to 4.7, for a 1MHz input. The overall power consumption of the 6-bit Vernier Delay Line ADC was found to be 2.1mW, with a 1.8V power supply voltage. This power is one-third the power consumed by the 4-bit Flash ADC. This is mainly because most of the Vernier Delay Line ADC is made up of digital gates and latches, which consume dynamic power and hardly any static power is consumed.

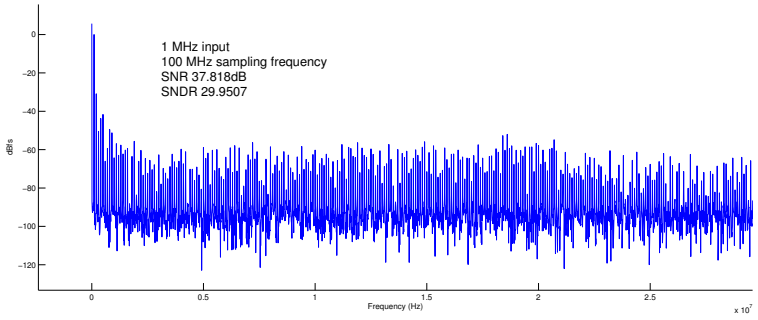

Figure 4.8: Frequency Response of 6-bit Vernier Delay Line ADC

4.5 Simulation Results for hybrid 10-bit ADC

The overall 10-bit ADC gives a good performance and is capable of running at 100M samples/s. The non-linearity of the Delay Line block is the only factor which affects the linearity of the hybrid ADC. Figure 4.9 gives the transfer function of the 10-bit ADC. The transfer function is mostly linear.

The maximum and minimum DNL for the 10-bit ADC is 0.2189 LSB and -0.4329 LSB respectively, and maximum and minimum INL is 2.429 LSB and -0.2524 LSB respectively, as shown in Figure 4.10. The two dips in the DNL plot are due to the slightly high DNL in the 4-bit Flash ADC, for bit 2 and bit 6 4.2.

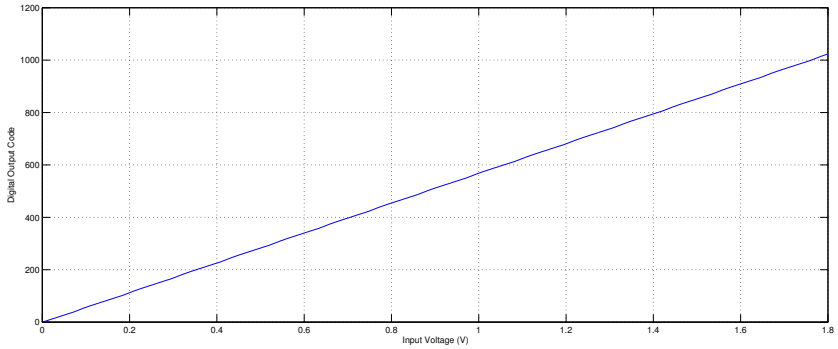

Figure 4.9: Transfer Function of 10-bit hybrid ADC

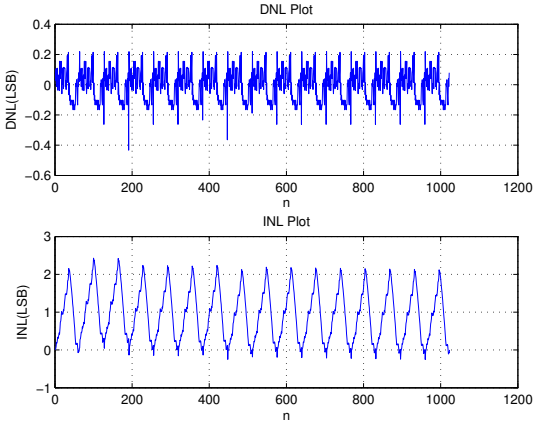

Figure 4.10: DNL and INL of 10-bit hybrid ADC

Figure 4.11 shows the dynamic performance of the 10-bit hybrid ADC. The hybrid ADC showed an SNR of 56.47dB, SNDR of 54.69 dB and effective number of bits (ENOB) equal to 8.82, for a 1MHz input. Due to the high linearity of the Flash block, the overall linearity of the hybrid ADC is better than that of the vernier delay line ADC. The overall power consumption of the 10-bit hybrid ADC was found to be 8.59mW, with a 1.8V power supply voltage. The 6-bit Vernier Delay Line ADC consumes one-third of the power consumed by the 4-bit Flash ADC. Increasing a single bit of resolution in the Flash ADC, increases its power by a factor of two. The 10-bit hybrid ADC thus consumes even lesser power than a 5-bit Flash ADC.

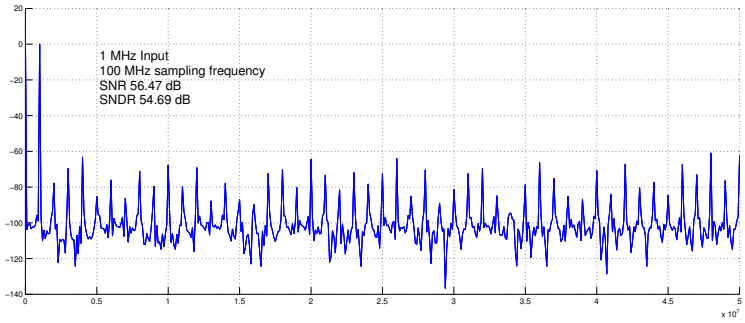

Figure 4.11: Frequency Response of 10-bit hybrid ADC

Chapter 5

Conclusion

Flash ADCs have been used for data conversion for a very long time. Vernier Delay Line ADCs were implemented recently and are based on the concept of TDCs. A novel architecture for analog to digital conversion was implemented in this thesis as a 10-bit hybrid ADC using Flash and Vernier delay line architectures. The hybrid architecture achieves high resolution while maintaing a high sampling speed.

5.1 Rationale

The analog nature of the physical world and the trend towards working in the digital domain keeps us interested in the field of Analog to Digital converters. The increasing number of applications requiring digital processing are pushing the research in data converters. Even though various data converter architectures have been invented, technology scaling is posing serious questions for those architectures. It is becoming tougher and tougher to design good quality analog circuits in the digital design centric sub-micron technologies. There is thus a need to develop new digital circuit techniques for conversion from analog to digital. The vernier delay line based ADC, which

uses digital gates and latches, is first of its kind. A new architecture was needed to improve the low resolution of the vernier delay line ADC. Increasing the resolution by one bit reduces the speed of delay line ADC by 50%. There was a need to develop some kind of a hybrid structure, which improves upon the resolution of the vernier delay line ADC, without compromising much on the speed. The present architecture addresses the problem of low resolution by adding a Flash design in front of the vernier delay line structure.

5.2 Methodology

A structure similar to folding analog to digital converters was implemented in the design of the 10-bit hybrid ADC. A 4-bit Flash ADC was used to get the high 4-bits of resolution. The low 6-bits were taken from a 6-bit Vernier Delay Line ADC. A folding structure consisting of a DAC and a voltage subtractor was used to compute the input voltage for the Vernier Delay line ADC.

5.3 Results

A 10-bit hybrid ADC, capable of running at 100M samples/s was implemented. It was characterized by very low differential non-linearity (-0.4329 to 0.2189 LSB) and a moderate integral non-linearity (-0.25 to 2.4 LSB). An SNR of 56.47dB and an SNDR of 54.59dB was realized from the hybrid ADC. The effective number of bits achieved from the design is 8.82. Owing to a very small analog ciruitry, the power consumption of the ADC was very small

(8.59mW at 1.8V).

5.4 Scope for Future Work

The major non-linearity in the present design stems from the voltage to delay block. Better designs can be implemented, which transform voltage to time in a highly linear fashion. In addition, developing temperature and voltage dependent delay blocks would be an interesting area of research. In order to ensure a linear performance in the manufactured product, some kind of digitally assisted calibration algorithms could also be incorporated in the design.

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