THE DISSERTATION COMMITTEE FOR SEUNG HOON CHOUNG CERTIFIES THAT THIS IS THE APPROVED VERSION OF THE FOLLOWING DISSERTATION:

A TOPOLOGY DEVELOPMENT AND ANALYSIS FOR MULTIPLE INPUT DC/DC CONVERTER

Committee:

Alexis Kwasinski, Supervisor

W. Mack Grady

Aristotle Arapostathis

Mircea D. Driga

You Seok Son

A TOPOLOGY DEVELOPMENT AND ANALYSIS FOR MULTIPLE INPUT DC/DC CONVERTER

by

SEUNG HOON CHOUNG, B.E. M.S.

DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT AUSTIN

MAY 2011

Dedication

Dedicated to my wife Jungeun Kim; parents, Young Choung and Youngsook Sagong.

Acknowledgements

First and foremost, I would like to thank Professor. Alexis Kwasinski, my advisor for his assistance and guidance. It was very honorable for me that I could be his first doctoral student. My doctoral studies would not have been possible without his kind support and encouragement. I will remember his wholeheartedness and would like to express my gratitude once again.

I wish to thank the members of my committee; Dr. W. M. Grady, Dr. M. D. Driga, Dr. A. Arapostathis in the Department of Electrical of Computer Engineering and Dr. Y S. Son at E.ON for serving as my committee. Their encouragement and suggestions have help me immensely in the completion of this dissertation.

During my time at UT as a doctoral student, I have been very fortunate to have the opportunity to work with people from the UT Power Electronics Research Group with whom I shared an office space. They are have great individuals both personally and academically. I would like to thank them for their help during my time here at UT. I must extend special thanks to Sungwoo Bae, Jooyoung Jung, Seynghyun Chun, and Junsuk Song who are always supportive of my research in my personal life. Without their help, I could not have completed my dissertation successfully.

I would like to express to my deepest thanks to my friends and colleagues in Austin. I especially thank Byungchul Jang, Jin Hur and Wonjin Cho, who always gave me thoughtful advice and were always willing to help me and my family.

I would also like to express my appreciation for Professor Sungsoo Hong at Kookmin University, Seoul, Korea. From him, I could learn not only what engineering is but also how to become an engineer.

I also say thank you to my uncle, Professor Seokjin Sagong, who first led me to the electrical engineering field. His brilliant foresight and mentorship has always helped me in technical and spiritual.

I would like to thank my parents, Young Choung and Youngsook Sagong, for their continued and enthusiastic support of my education, as well as my parents-in-law, Soochun Kim and Jongin Park for their great support. I would like to express my deepest love to my precious daughter and son, Jayla and Minchan. Being their father is the greatest pride of my life. Last but not least, I would like to thank my wife, Jungeun Kim. Her support and sacrifice has always been invaluable to me.

TOPOLOGY DEVELOPMENT AND ANALYSIS FOR MULTIPLE INPUT DC/DC CONVERTER

Publication No._____

Seung Hoon Choung, Ph.D.

The University of Texas at Austin, 2011

Supervisor: Alexis Kwasinski

Nowadays, the number of applications which need more than one power source is increasing. Distributed generating systems or micro-grid systems normally use more than one power source or more than one kind of energy source. Also, to increase the utilization of renewable energy sources, diversified energy source combination is recommended. For example, a wind-photovoltaic generating system, a combination of a wind generator and photovoltaic array, can give a greater degree of freedom when choosing the install location. The combination of more power sources and diversified power sources makes it possible to obtain higher availability in a power system. A parallel connection of converters has been used to integrate more than one energy source in a power system. However, a multiple-input converter (MIC) can generally have the following advantages compare to a combination of several individual converters; (1) cost reduction, (2) compactness, (3) more expandability and (4) greater manageability.

First, this research suggests MIC topology comparison criteria that can be used as a decision guide for choosing a MIC topology depending on the application. Even though there are some MIC topology classification methods such as by the kind of combining methods, the classification methods are not enough to choose one particular topology. The comparison criteria presented in this dissertation are practical enough to decide which topology is suitable and should be chosen.

Second, a new MI modified inverse Watkins-Johnson converter (MIMIWJC) without a coupled inductor is proposed. The circuit configuration of this converter and its operation principles are described, including the open-loop and closed-loop circuit. For control purposes, a small signal model of the proposed converter is developed using Middlebrook's extra element theorem. In addition, two possible control methods are introduced in this dissertation.

Finally, the theoretical analysis of the proposed converter is verified with simulations and experiments.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 Dissertation Organization

Recently, many power systems use parallel connections to achieve specific requirements such as low output current ripple, fast transient response or high availability. From a control and efficiency points of view interleaved converters which are a parallel connection of power stages in switching converters can have several advantages over single power stage converters [1-2]. For example, a voltage regulator module (VRM), which is one of the interleaved converters for microprocessors, can manage very high current slew rate (1A/μs) during transients and has high efficiencies [3].

Similarly, to obtain high availability, paralleling the whole system, including the power sources, as in Fig. 1.1 (a), can be the best solution even though its cost could be high. If costs and availability are being considered at the same time, then a MIC with modular parts can be selected, like the one shown in Fig. 1.1 (b). Lately, because of their high availability and low cost, MIC converters are being used and studied in aerospace, electric and hybrid vehicles, sustainable energy sources, and microgrid applications [4],[5].

The definition of a MIC is a converter which can combine different energy sources with a single conversion stage. Fig. 1.1 (b) shows a simple conceptual diagram of a power system configuration using a MIC. In Fig. 1.1, Source 1 to Source N-1 can be

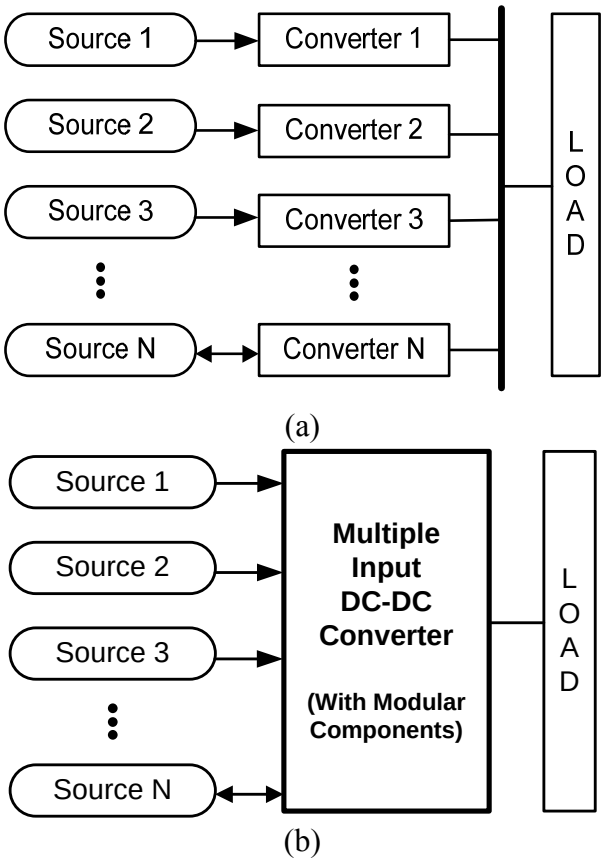


Figure 1.1: Multiple DC power sources connection structure (a) Fully distributed system using bus converters (b) MIC system configuration

composed of any kind of energy source combinations, such as wind generators, photovoltaic modules, fuel cells, micro turbines and/or electric grid, and Source N could be a storage unit, such as a battery, ultra-capacitor, flywheel or superconducting magnetic energy storage system (SMES).

High availability in a power system with MICs can be achieved by diversifying or mutiplying power sources and utilzing modular designed MICs. This configuration has

some advantages compare to fully distributed power systems. A structure that use a MIC can have fewer conversion steps and requires fewer components than a fully distributed system. These advantages can make the system not only economically but also thermally efficient [5]. The disadvantage of the MIC configuration is that the output stage of a MIC can act as a single point of failure. However, a modular designed MIC can compensate for this weakness by reducing the mean down time (MDT) of the system.

1.2 SCOPE OF THIS RESEARCH

It is obvious that a MIC has some advantages as a power electronic interface. Although many MIC topologies are introduced and studied in literature, most of them have been developed and described only in consideration of very limited applications, such as electric vehicles [6],[7] or fuel-cell and battery combinations [8],[9]. Some of them have been proposed with little description of the advantages and disadvantages [10]. Thus, it is necessary to study how a MIC can affect a given power plant. In this research, the desirable topological properties of a MIC are studied, and a clear criterion based on a MIC comparison framework is found.

From the comparison work, one new MIC, a multiple input modified inverse Watkins-Johnson converter, is proposed. A topological and analytical description of the proposed converter is shown in this dissertation. A MIC operational technique is introduced, different from that in a single input dc-dc converter. The proposed converter and its operation techniques are verified through simulation and experiments.

1.3 DISSERTATION ORGANIZATION

Chapter 2 describes the classification method of MICs and proposes the four MIC's comparison categories. Then ten MIC topologies are evaluated and compared in the proposed categories. Comparison results are discussed.

In Chapter 3, a multiple input modified inverse Wakins-Johnson converter (MIMIWJC) is proposed. The fundamental steady-state operation principles of the proposed converter are described, and its critical waveforms and equations are found.

In Chapter 4, a dynamic modeling and control method for the MIMIWJC are discussed. A small signal model is built using an averaged switch circuit model of the converter. Since the proposed converter consists of four reactive components, the converter transfer functions are found using the extra element theorem.

Chapter 5, the analyzed results and proposed control methods are verified with simulation and experimental results.

Finally, Chapter 6 summarizes and concludes this dissertation. Future research opportunities are discussed based on the current research objectives and outcomes. It is followed by the list of references.

Chapter 2: Multiple Input DC-DC Converter Topology Comparison

2.1 INTRODUCTION

To date, various MIC topologies have been developed and studied in the literature [5-23]. However, since each of the topologies that have been proposed in the literature have their own advantages and disadvantages, it is difficult to choose a suitable MIC topology for a specified application. Although it is impossible to say one particular topology is the best for all applications, it is still meaningful to provide a selection guide considering the MIC's characteristics. Central to this section is to provide analytical and useful criteria for selecting an appropriate MIC topology. So far, the MICs are classified and reviewed based on which circuit point is connected to make a MIC [10, 17]. The three possible interfacing methods can be classified as follows: sharing only the output filter capacitor, method I [6], connecting through a magnetic core, method II [8] [9], and sharing some switches and energy transfer inductors and capacitors, method III [11-13, 23]. These three combining methods for MICs are described in Fig. 2.1. It is true that this classification by combining strategy can represent one of the most important characteristics of MIC topologies, but the classification alone, is not enough to allow a definitive topology selection. Besides, it is possible to have different characteristics even when the strategy to couple input sources is the same. Thus, it is necessary to find definitive selection criteria in order to realize a reasonable MIC comparison framework.

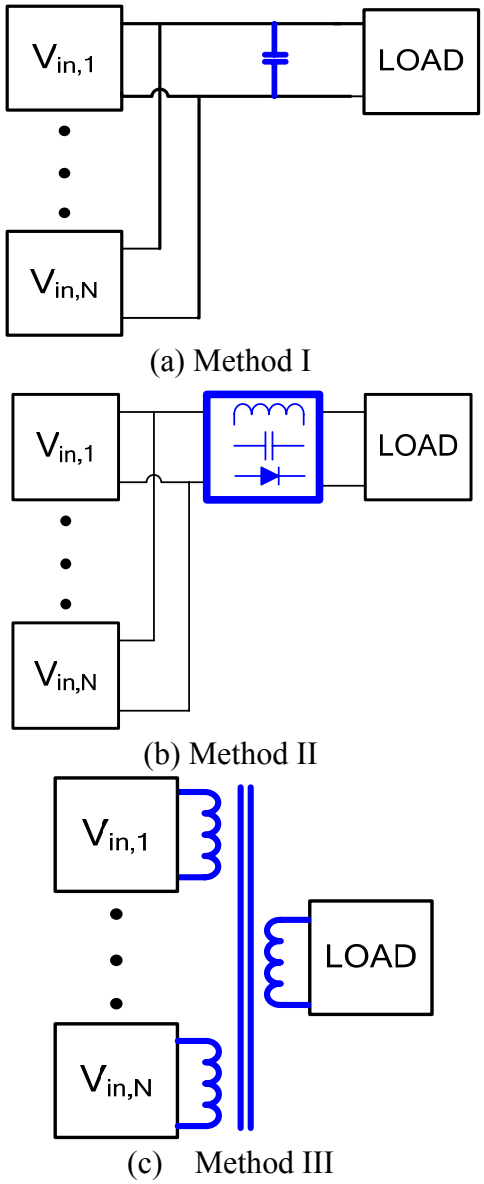


Figure 2.1: The three MIC combining strategies: (a) sharing only the output capacitor (b) sharing the switching device and other energy storage components (c) interfacing through the magnetic core

This chapter is organized as follows. First, a few MIC topologies used as benchmarking configurations are introduced. Then, the comparison criteria and results are explained. Finally, a conclusion and summary of the topics included in this chapter are presented.

2.2 MULTIPLE INPUT CONVERTER TOPOLOGIES

Table 2.1 shows the list of the surveyed and proposed MIC topologies to be compared in this chapter. The listed MIC topologies are selected because they all present relatively significant differences both in topologies and operation. Although there are some more topologies besides those listed in Table 2.1, most of the other topologies are modified versions of these basic MIC topologies. For this reason, the converters in Table 2.1 are treated as their simplest forms in this chapter. The objective of this chapter is to provide a simple but reasonable guide to help choosing the most suitable topology in a given application. For comparison purposes, the topologies' configurations are taken as the combination of power stages and output filters only. That is to say, control parts, additional stages to provide a special functionality, such as zero voltage switching (ZVS), zero current switching (ZCS), snubbers to suppress voltage and/or current spikes or filters to provide a modified input or output interface are not considered. The reason is that such an inclusion would affect the basis for a reasonable comparison among topologies. In Table 2.1, the lower case "b" of MIb stands for buck converter, and the upper case "B" of MIB stands for boost converter.

Abbreviation	Description
MIb [22]	multiple input buck
MIB [6]	multiple input boost
MIbB [20]	multiple input buck-boost
MIĆUK [12]	multiple input ĆUK
MISEPIC [13]	multiple input SEPIC
MIMIWJC [11]	multiple input modified inverse Watkins-Johnson
MIBbB [5]	multiple input boost/buck-boost
MIF [20]	multiple input flyback
MIHB [9]	multiple input half-bridge
MIFB [8]	multiple input full-bridge

Table 2.1: The abbreviated identification of MIC topologies

2.2 Comparison Criteria and Evaluation for Multiple Input Converters

The applications of MICs may be different from single input converters. Thus, different aspects need to be considered for MIC comparison. The authors of [10] and [17] reviewed some of the MIC topologies. However, the authors in [10] only focused on describing each MIC's characteristics, and the authors in [17] focused on introducing the three combining strategies. Although the classification method can help to understand the characteristics of MICs, to choose one particular topology, a comparison is necessary.

Four criteria are selected for the MIC topology comparison. The most prominent advantages of using MIC over single input dc-dc counterparts are to provide a cost-effective solution and an improved system availability through the implementation of modular components. Hence, cost, modularity, reliability and flexibility are the chosen categories for this MIC topology comparison. A more detailed explanation about the four comparison criteria is presented later in this section.

2.2.1 Expected Cost

Lower cost is one of the most important reasons to use a MIC system instead of using a parallel bus converter system. Since the total number of necessary components of MICs can be lower than that of parallel converters, it is possible that the MIC can be built with at a lower cost. Hence, the reduced cost effect can be maximized by increasing the number of components in MICs common stage. In that respect, one can expect that the more shared components in a topology, the cheaper the circuit is. In the same manner, MIC topologies that need fewer components in their input modules can be cheaper. Consequently, a topology consisting of input legs connection at the output filter capacitor, as shown in Fig. 2.1 (a), tends to provide few cost savings because the only common component is the common output filter capacitor. In addition, since the production cost of magnetic components is relatively high in a dc-dc converter, MIC topologies that use an input legs connection at a common magnetic core, as shown in Fig. 2.1 (c) can be more expensive than MIC topologies whose common modules consist of the switch and passive components in Fig. 2.1 (c). Moreover, if the input module is

composed of a small number of components, it can be favorable when a large number of input sources is combined.

The cost evaluation is divided into two parts: one is input module price comparison, and the other one is output common module price comparison. The input module price comparison is summarized in Table 2.2. The input module Group I is the input module whose component is only a switch, the input modules in Group II are composed of one switch, one inductor and one capacitor, and the input modules in Group III are composed of more than one switch and/or one inductor. Thus, in terms of price, Group I is the cost effective, Group III is the most expensive, and Group II is in between. The output module price comparison results are shown in Table 2.3. In Table. 2.3, Group I topologies' output modules are composed of only passive devices, Group II's output modules are composed of one passive switch and other passive components, inductors and capacitors, and Group III's output modules have the transformer, inductors, capacitors, and/or active switches. Within one group, it is possible to add more detail to the comparison, such as in Group III, where the MIHB can be cheaper than the MIFB because it has fewer switches. However, since the transformer is usually the most expensive component in a dc-dc converter, both the MIHB and the MIFB can be in the same group.

Group I	Group II	Group III
MIb	**MIBbB**	**MIB**
MIbB	**MIĆUK**	**MIHB**
MIMIWJC	**MISEPIC**	**MIFB**
MIF		

Table 2.2: Input module price comparison: Group I is the most cost effective, Group II is second and Group III is the most expensive.

Group I	Group II	Group III
MIB	**MIb**	**MIF**
MIBbB	**MIbB** **MIĆUK**	**MIHB** **MIFB**
	MISEPIC **MIMIWJC**	

Table 2.3: Output module price comparison: Group I is the cheapest, Group II is second and Group III is the most expensive.

2.2.2 Modularity Potential

As it is indicated in Eq. (2.1), a shorter down time can result in the following availability [24].

$$Availability = \frac{Mean\ Uptime}{Mean\ Uptime + Mean\ Downtime} \tag{2.1}$$

Since a modular converter can reduce the down time of a power system, in the interest of availability, it is worthwhile to compare with which MIC topology is easier to make a modular converter. Modularity potential can be defined as how easy it is to develop each of the converters in a modular way. In order to compare the modularity potential, input combining methods and the types of devices for each input module can be considered. Also, since it is beneficial that input and output modules have a simple structure, simplicity of the configurations is considered. Among the three combining methods, Method I is considered to be the simplest way to make a module because not only can each input module be made using the same configuration, but also the output module just consists of an output capacitor. On the contrary, interconnection through a magnetic core is considered to be the most complex method. Configurations in which the common stage includes at least one switch (e.g. a diode) tend to be slightly more difficult to modularize than configurations in which only the output capacitor is shared, because mechanical and thermal requirements are added, such as the need to mount the diode and the main switch on different heat sinks.

Group I	Group II	Group III	Group IV	Group V
MIB	**MIb**	**MIbB**	**MIHB**	**MIF**
	MIMIWJC	**MIBbB**	**MIFB**	
		MIĆUK		
		MISEPIC		

Table 2.4: Modularity potential comparison: Group I has the highest, Group II has the second, Group III has the third, Group IV has the fourth, and Group V has the lowest modularity potential

Based on the above factors, the modularity potential comparison results are summarized in Table 2.4. The MIB toplogy can be evaluated as having the highest modularity potential since it shares only the output capacitor.

2.2.3 Reliability

First, it is true a MICs' reliability can be lower than that of a parallel connection of equivalent single-input dc-dc converter configurations. The reason is that a MIC shares some components, which may act as a single point of failures. In other words, reliability decreases as the number of common components increases. Thus, the number of common components in a MIC topology is considered for the reliability evaluation. Another consideration factor when evaluating reliability of MIC is the reliability of a each part that is placed in a common module. For example, the reliability of sharing electrolytic capacitors is lower than that of sharing inductors because generally an inductor has a

	Switching Device	Magnetic Device	Capacitor
Relative failure rate	**0.2**	**0.01**	**1**

Table 2.5: Relative failure rate of devices for the MIC topology

higher reliability than a capacitor [25]. Hence, there are two aspects when comparing reliability of MIC topologies: the number of common components and the types of common components. Since every component is considered to be ideal, stress from current and voltage spikes are ignored during the reliability evaluation. Furthermore because reliability may change dependably operation conditions, it is very difficult and even impossible to get an accurate reliability result. Thus, reliability is simply based on a relative failure rate, as shown in Table 2.5 [26]. The relative failure rate can only be used for comparison purposes, not for the reliability calculation of each converter.

Based on the above reliability consideration factors and Table 2.5, the input module reliability comparison result is shown in Table 2.6. As expected, input modules that have a capacitor are evaluated as relatively less reliable. On the other hand, the input modules which consist of only one switching device are ranked in the highest reliability group since these are comprised of the least number of components. Table 2.7 displays the output module reliability comparison results. The output modules that have two or more capacitors are judged as relatively less reliable. In particular, since the MIHB's output module has four capacitors, the output module is listed in the least reliable group.

Group I	Group II	Group III	Group IV
MIb	**MIHB**	**MIFB**	**MIĆUK**
MIbB			**MISEPIC**
MIBbB			
MIMIWJC			
MIF			

Table 2.6: Input module reliability comparison: Group I is the most reliable, Group II is the second, and Group III is the least reliable

Group I	Group II	Group III
MIb	**MIFB**	**MIHB**
MIB	**MIMIWJC**	
MIBbB		
MIĆUK		
MISEPIC		
MIF		

Table 2.7: Output module reliability comparison: Group I is the most reliable, Group II is the second, and Group III is the least reliable

2.2.4 Flexibility

Different source combination in MICs can increase the availability of the power system. Flexibility means that a MIC topology is compatible with various kinds of input sources. To evaluate flexibility, it is necessary to examine which topology can meet the various source requirements. The types of input source interfaces and voltage conversion ratios are considered for flexibility comparison. First, regarding the input source interface, there are two types of converters: one is a current interfacing converter (CIC), and the other one is a voltage interfacing converter (VIC). The difference between a CIC and a VIC is whether the input voltage source is directly connected through an inductor or not. If the input source is connected through an inductor, the converter is called a CIC, and if the input source is not connected to the inductor, that converter is called a VIC, as shown in Fig. 2.2. The MIC topologies which are CICs can have higher flexibility. The reason is that, some input sources, such as fuel-cells, require low input current ripple. Also, other input sources, such as photovoltaic modules, may also require a CIC to implement maximum power tracking controls [27]. Second, the conversion ratio of a MIC topology is evaluated. In MICs, it is desirable that a given topology can provide wide input and output voltage ranges. That is, a converter that can do a step-up or step-down conversion is less flexible than a converter that can do both step-up and step-down functions. In this sense, the existence of a transformer can be beneficial because it may provide a large input-to-output voltage ratio by adjusting the transformer turns ratio. Also, step-up converters can be evaluated as more flexible converters than step-down

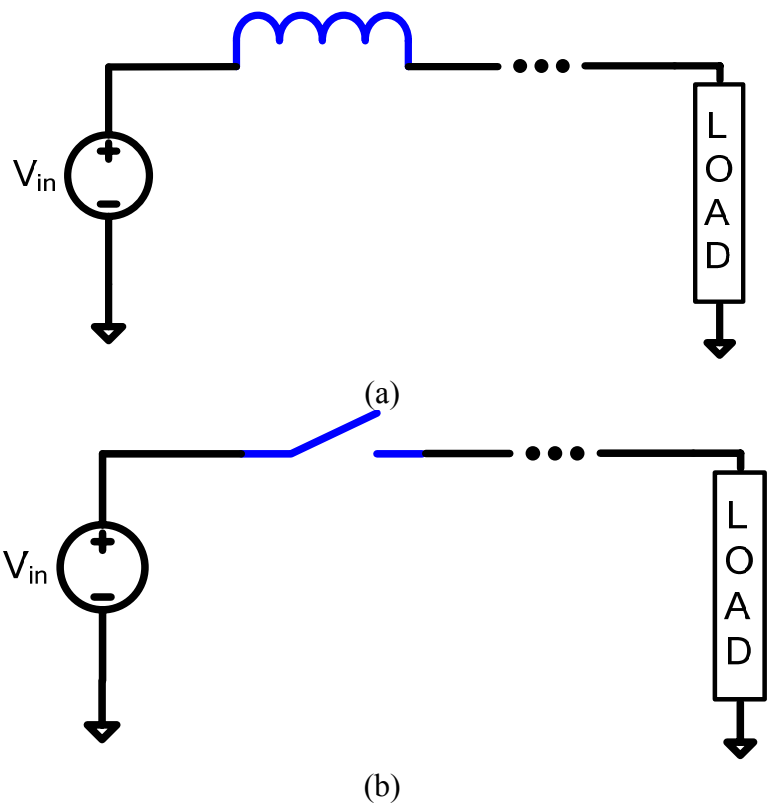


Figure 2.2: Two interfacing methods of dc-dc converter: (a) Current interfacing converter (CIC) (b) Voltage interfacing converter (VIC)

only converters. That is, because some sources, such as photovoltaic and energy storage units, have relatively low voltage magnitudes, so the step-up conversion is needed.

First, relating to the input module flexibility evaluation, source interfacing methods are considered and Table 2.8 shows the results. The CSI topologies are shown in Group I while VSI converters are shown in Group II, in Table 2.8. The output module flexibility comparison results can be grouped according to the voltage conversion ratios of the selected topologies, as shown in Table 2.9. The step-up step-down converters are

Group I	Group II
MIB	**MIb**
MIĆUK	**MIbB**
MISEPIC	**MIMIWJC**
MIBbB	**MIF**
MIHB	**MIHB**

Table 2.8: Input module flexibility comparison: Group I has higher flexibility than Group II

Group I	Group II	Group III
MibB	**MIB**	**MIb**
MIĆUK		
MISEPIC		
MIMIWJC		
MIBbB		
MIF		
MIHB		
MIFB		

Table 2.9: Output module flexibility comparison: Group I is the most Group II is the second Group III is the least flexible

ranked the highest flexible group while the step down only converter ranked as the least flexible output module.

2.3 DISCUSSION

In Section 2.2, the four comparison criteria, expected cost, modularity potential, reliability and flexibility, and their evaluations are described. However, the evaluations have been done without considering the number of input sources. Since the number of input legs can affect the comparison results, the number of input sources should be determined before the comparison. Thus, in this section, the comparisons and discussions are carried on assuming four input legs for each MIC topology.

The comparison results for each criterion are summarized in Table 2.10 based on the evaluation of the MIC topologies under consideration. Once again, it should be mentioned that the comparison result can only be interpreted in a relative way. The reason why the positive and negative signs and zeroes are used is to avoid the misunderstandings that can arise from using numbers. That is, the results can be interpreted in the following way: '+' in a given converter indicates that it has better attributes than '0' or '-' in other converters in the same category. Similarly, a '0' represents better attributes than '-'. Hence, '++' should not be interpreted as two times better than a '+' but should be interpreted as merely better than a '+'.

	Expected Cost	Modularity Potential	Reliability	Flexibility
MIb	++	+	++	--
MIB	-	++	+	0
MIbB	+	0	+	0
MIĆUK	-	0	-	+
MISEPIC	-	0	-	+
MIMIWJC	+	+	+	0
MIBbB	0	0	++	+
MIF	++	--	++	+
MIHB	--	-	-	++
MIFB	---	-	0	+

Table 2.10: Comparison table for four input MIC topologies. This table can be interpreted in a relative comparison only.

This table can be used for choosing the appropriate MIC topology in a given application. For example, if various different types of sources should be combined, or if an unknown source is going to be added in the future, then the MIHB converter can be a good choice even though the other factors, such as cost saving effects, are not as good as the other MIC topologies'. When low cost is the driving design goal, then either one the MIb, MIbB, MIMIWJC, or MIF can be a good candidate. As shown in Table 2.10, there are three topologies that do not have negative evaluations: the MIbB, MIMIWJC, and MIBbB. Among them, the MIMIWJC is the only one that has three positive evaluations in the four categories with one '0' evaluation. Hence, the MIMIWJC seems to provide a good trade-off option for many applications. The MIMIWJC analysis will be discussed in the following chapters of this dissertation. Since the MIBbB is the only topology which allows integrating two different kinds of single input converters, boost and buckboost converters, it could obtain a relatively good evaluation in all four comparison criterion categories. Hence, the MIBbB could also be a good general purpose topology.

2.4 SUMMARY AND CONCLUSION

A MIC topology classification method based on input source combining strategies was introduced. In this chapter, considering the MIC's characteristics, four comparison criteria were introduced: expected cost, modularity potential, reliability and flexibility. Also, the meanings of each category were described. In section 2.2, the evaluation methods were explained. Except for the modularity potential category, the other three criteria are compared separately as input and output module so that one can expand the

comparison by changing the number of input sources of the converter. Table 2.10 showed the comparison results for MIC topologies comprised of four input legs. This table can be used to choose a certain MIC topology in a given application.

Chapter 3: Fundamental Analysis of a Multiple Input Modified Inversed Watkins-Johnson DC-DC Converter

3.1 INTRODUCTION

The main objective of this chapter is to analyze the fundamental MIMIWJC circuit operation and to find related equations. There are two topologies whose evaluation does not have any negative in chapter 2 the multiple input boost buck-boost (MIBbB) [5] and the multiple input modified inverse Watkins-Johnson converter (MIMIWJC) [11].

In this chapter, the principle analysis of a proposed MIMIWJC is described. The single-input type modified inverse Watkins-Johnson converter (IWJC) was first introduced by Tymerski and Vorperian in Table II cell G1 (1) [28]. The input to output voltage conversion ratio of the IWJC shows a desirable characteristic for a MIC application because the output voltage can be either higher or lower than the input voltage, like a buck-boost converter case. Besides, it is notable that the IWJC's conversion ratio can be higher than the buck-boost's for the same duty ratio [29], as shown in Fig 3.1. Figure 3.1 shows the normalized voltage conversion ratios of the boost, buck-boost, and IWJC. The boost, buck-boost and IWJC converter's input-to-output voltage conversion ratios which are used for Fig. 3.1 are shown in Eq. (3.1), (3.2), and (3.3), respectively.

$$V_{OUT} = \frac{1}{1-D} V_{IN} \tag{3.1}$$

$$V_{OUT} = \frac{D}{1-D} V_{IN} \tag{3.2}$$

$$V_{OUT} = -\frac{D}{1-2D} V_{IN} \qquad \text{where, } D<0.5 \tag{3.3}$$

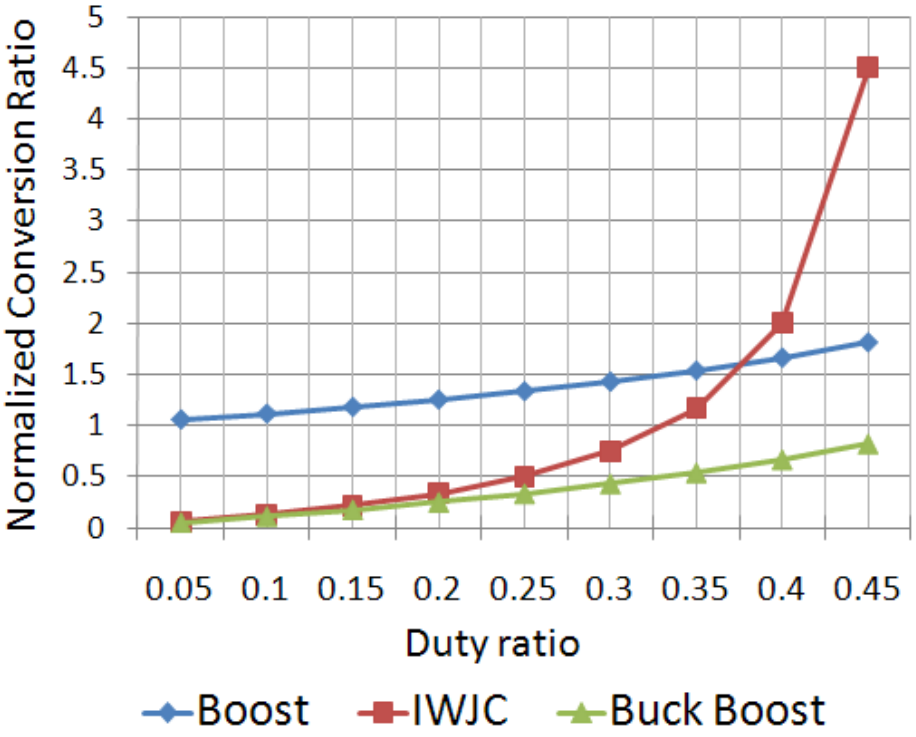
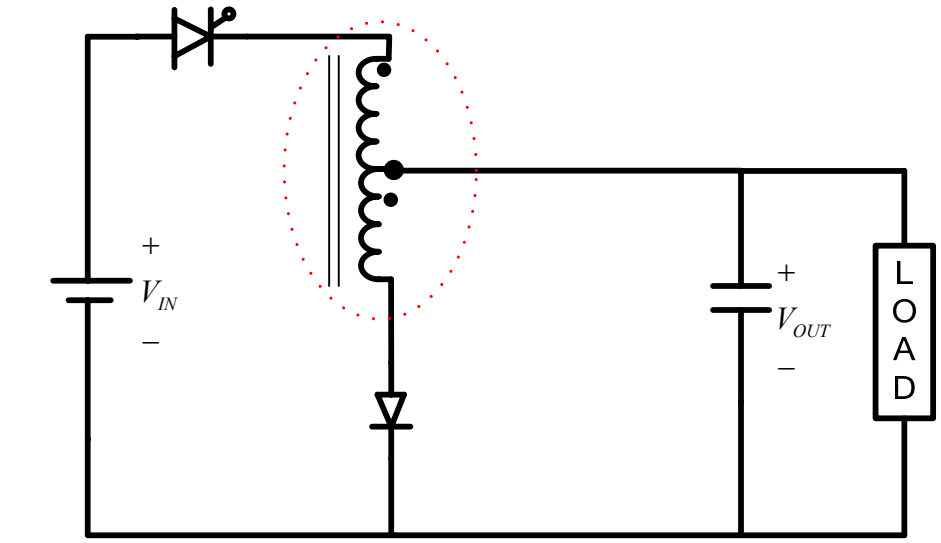


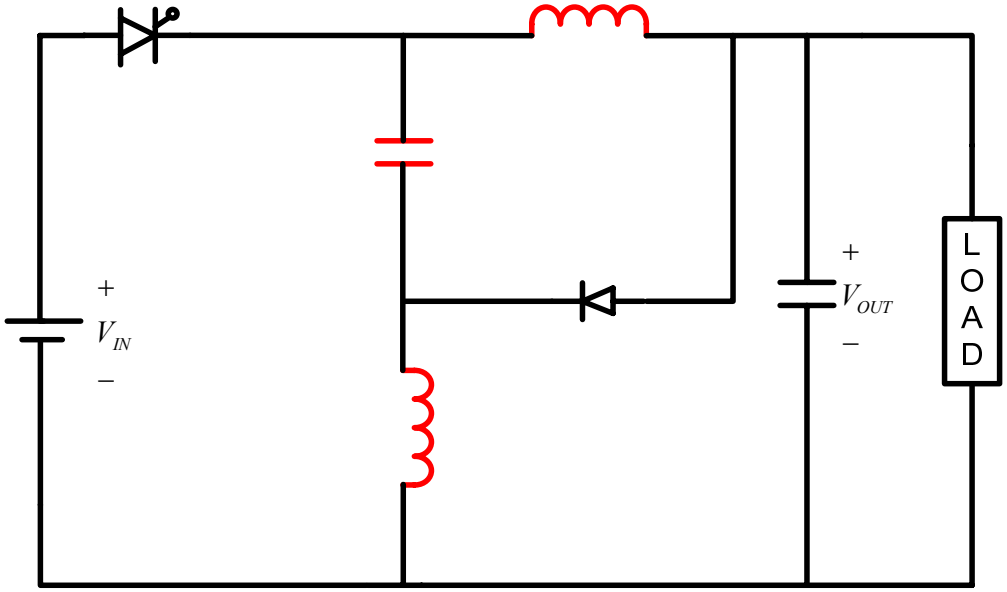
Figure. 3.1: Conversion ratio comparison in IWJC, Buck-boost and boost converter

As it is explained in Chapter 2, the unmodified IWJC shown in Fig. 3.2 (a) might have drawbacks in modularity potential and price since a transformer exists in its topology. Thus, if it is possible to keep the same voltage conversion ratio without magnetic coupling, it can be more desirable to develop as a MIC topology. Figure 3.2 (b) shows the modified IWJC converter which is a more favorable converter type than an unmodified IWJC to connect more than one input source. The differences between the modified IWJC and the original IWJC are that one capacitor is added, and the magnetic coupling between two inductors is disconnected, which is marked with red in Fig. 3.2 (b).

The schematic of a multiple input version of the modified IWJC (MIMIWJC) is shown in Fig. 3.3. The input modules can be composed of only one single switch and an input source combination. This is the simplest form of the input module, and its use in a MIC maximizes the modularity of the MIC. In addition, regarding expected cost, this kind of structure can have some advantages since the circuit does not include a transformer, and the price of each input module can be relatively low. Although the modified IWJC has one more capacitor in it than the unmodified IWJC, its cost cannot increase much because a capacitor is not only a relatively inexpensive component in such a dc-dc converter circuit but also because it is placed in the common module side.



(a)



(b)

Figure 3.2: Circuit diagram for IWJC: (a) Original inverse Watkins-Johnson converter (b) Modified inverse Watkins-Johnson converter

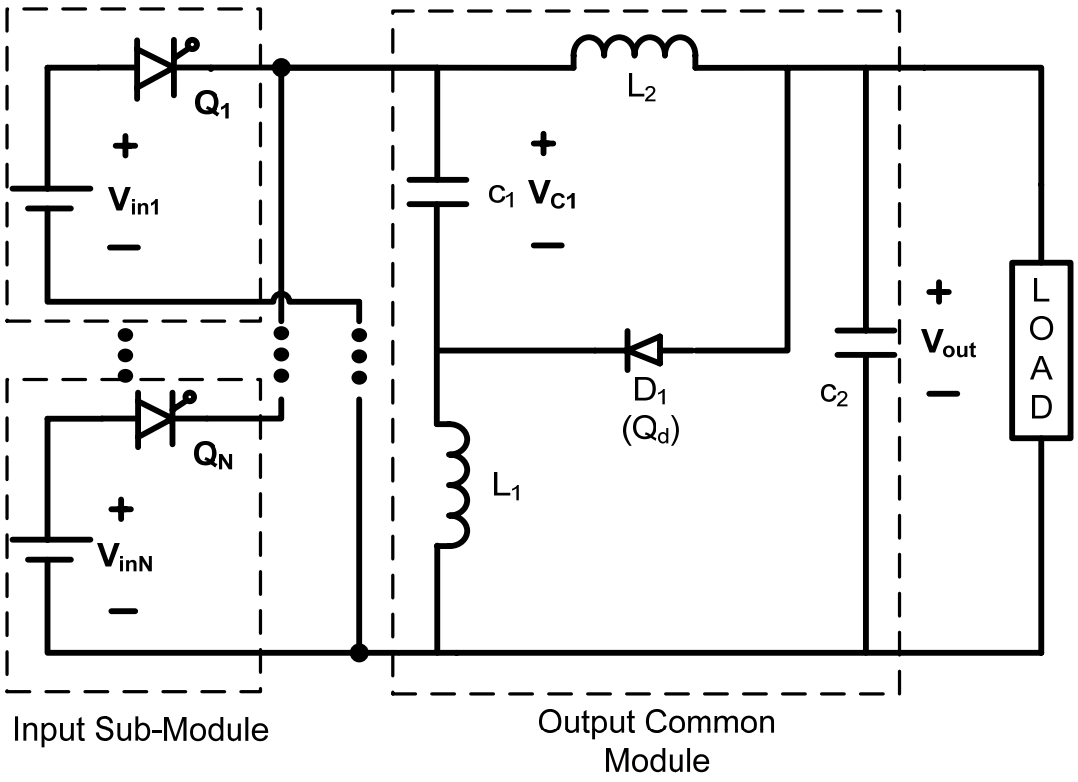


Figure 3.3: Multiple input modified inverse Watkins-Johnson Converter (MIMIWJC) circuit diagram

3.2 SWITCHING STRATEGY OF MICS

Since most MIC topologies do not allow power flow from two or more input sources at the same time, a proper switching scheme is needed. A time sharing switching concept can be a good choice as a MIC's switching scheme [20]. To realize the time sharing switching scheme, a FCBB switch can be used. In this section, a brief introduction of FCBB switches and time sharing switching are described.

3.2.1 FCBB SWITCHES

Electrical switches can be classified by the arrangement of their electrical contacts or current flow direction capability [30]. First, a switch can be classified by the number of pole points and throwing points, such as single-pole single-throw (SPST), single-pole double-throw (SPDT) and double-pole double-throw (DPDT), etc. Secondly, a switch can be sorted according to the conducting direction and blocking characteristics. The classification by switching action is shown in Table 3.1. Usually, single input dc-dc

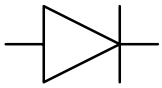
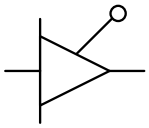
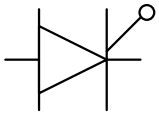
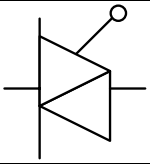
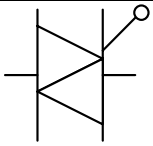
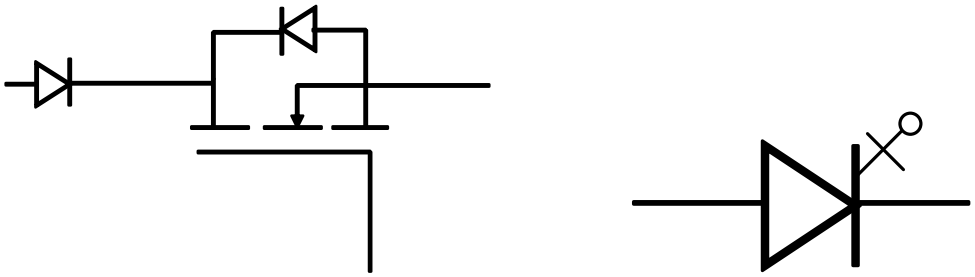
Abbreviation of Switch Type	Description	Symbol	Device
FCRB	Forward-conducting reverse-blocking		Diode
FCFB	Forward-conducting forward-blocking		BJT
FCBB	Forward-conducting bidirectional-blocking		GTO
BCFB	Bidirectional -carrying forward-blocking		MOSFET
BCBB	Bidirectional -carrying bidirectional-blocking		Ideal Switch

Table 3.1: Switch classification by switching function [30]



(a) (b)

Figure 3.4: FCBB switch realization (a) a pair of diode and MOSFET series connection (b) GTO

converters use a bidirectional-conducting bidirectional-blocking (BCFB) switches, or forward-conducting forward-blocking (FCFB) switches are used as a main switch to control the power flow from input sources. That is, the bidirectional-blocking ability of a main switch is not required for a single input dc-dc converter. However, in the case of a MIC, the reverse current should be blocked to avoid current flow between input sources. Hence, a FCBB switch is needed for a MIC's main switch. A FCBB switch can be realized with a GTO or a series connection of a diode and MOSFET, as shown in Fig. 3.4.

3.2.2 TIME SHARING SWITCHING

Fixed switching frequency is the most widely used switching technique because electromagnetic interface (EMI) and electromagnetic compatibility (EMC) problems can be solved easily [31]. A time sharing switching concept can be used for a MIC converter that uses a fixed switching frequency operation. For time sharing switching, all duty

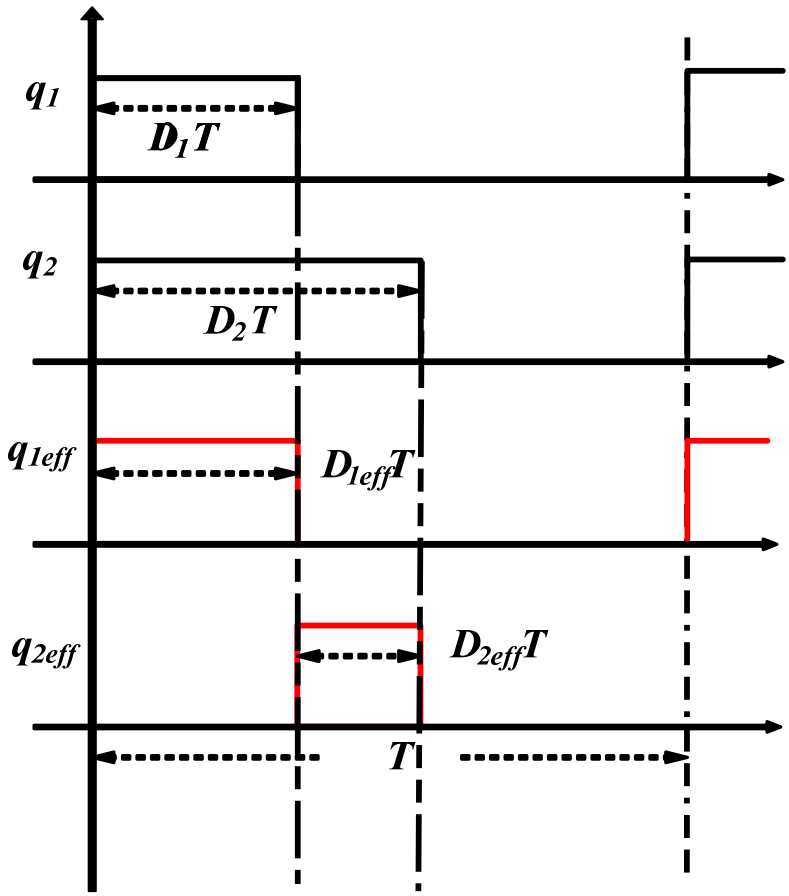


Figure 3.5: Multiple input modified inverse Watkins-Johnson Converter (MIMIWJC) circuit diagram

cycles are realized with the same carrier signal so that the leading edges of all switching signals occur simultaneously. However, the falling edges of each switching signal are different, as shown in Fig. 3.5. During this time when both switching commands are on, the FCBB switches can block the current flow between two input sources. Therefore, it is not possible that two or more input sources deliver power simultaneously with this time sharing switching concept. That is, the FCBB switches yield effective duty cycles which are different from the commanded switching signal. The effective duty cycle D_{eff} is

defined by the portion of the switching period when the switch conducts current. The i^{th} effective operation, D_{ieff}, can be expressed as

$$D_{ieff} = D_i - D_{i-1} \qquad \text{where } D_i > D_{i-1} \text{ and } D_0 \equiv 0 \tag{3.4}$$

For example, in the case of a two input converter: $D_{1eff}=D_1$ and $D_{2eff}=D_2-D_1$.

3.3 STEADY-STATE CIRCUIT ANALYSIS

In this section, the main operation principles of principles of steady-state MIMIWJC are described. For analytical simplicity, first, two-input MIMIWJC analyses are described, and then generalized equations for *N*-input MIMIWJC are found. The circuit diagram for a two input IWJC is shown in Fig. 3.6. In addition, some more

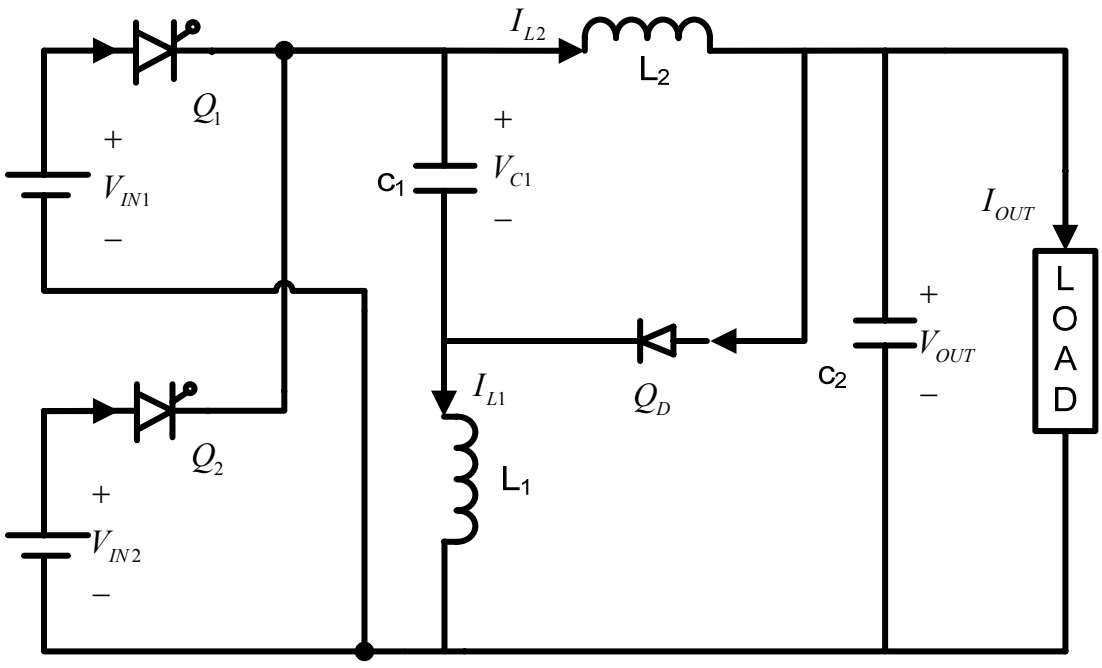


Figure 3.6: Two input modified inverse Watkins-Johnson converter circuit diagram

assumptions are made throughout this section. First, all the components are treated as ideal and a continuous conduction mode (CCM) operation is assumed. The load is considered as a purely resistive load, and a small ripple approximation is assumed throughout this section. First, all the components are treated as ideal, and a continuous conduction mode (CCM) operation is assumed.. This section can be divided in two parts: (1) averaged voltages and currents analysis and (2) ripple components analysis for each switching period. Averaged voltage and current analysis can help to understand the fundamental behavior of the converter, such as the input to output voltage relationship. Ripple component analysis can be useful to observe how the circuit works for each switching action. Appropriate equivalent circuits are provided for both analyses.

3.3.1 AVERAGED EQUIVALENT CIRCUIT ANALYSIS

Averaged relationships can explain some meaningful information of the converter. For example, the most important equation to describe the dc-dc converter topology is the input to output voltage conversion equation. To find an input to output voltage relationship, the two most widely used techniques are the inductor volt-second balance and the capacitor charge balance. By directly applying the volt-second balance to the inductor or the charge balance to a capacitor, the input to output dc relationship can be found. However, it is difficult to gain a physical understanding of the circuit behavior because these methods use equations instead of equivalent circuits. On the other hand, the averaged equivalent circuit analysis that is introduced in this section can provide a greater physical insight. The averaged equivalent circuit analysis is possible, since *Kirchhoff*'s

voltage law (KVL) and *Kirchhoff*'s current law can be applied in the averaged sense, too [32]. Thus, the averaged voltage relationships can be found by applying KVL to the averaged voltage mode equivalent circuit and the averaged current relationships can be found by applying KCL to the averaged current mode equivalent circuit.

3.3.1.1 AVERAGED CIRCUIT ANALYSIS IN VOLTAGE MODE

A voltage mode averaged circuit can provide an understanding of the voltage relationships between input voltage, output voltage and voltages across capacitors, C_1 and C_2 (Fig 3.6). In order to make the voltage mode averaged equivalent circuit, the voltages across the components in Fig.3.6 should be expressed in their averaged forms. First, in steady-state, the averaged inductor voltages should be zero so that the inductor can be expressed as a short circuit, i.e., a wire, in the averaged voltage mode equivalent circuit. The capacitors in the voltage mode averaged circuit can be represented as independent voltage sources, and the switching components, whether they are active or passive type switches can be expressed as dependant voltage sources. Figure 3.7 shows the component substitution process to make the averaged voltage mode equivalent circuit. The components are represented in terms of circuit symbols. The key point of this analysis is to represent the dependant voltage sources relationships in terms of the other known parameters, such as V_{IN}, V_{OUT}, duty ratios, and etc. The averaged voltage mode IWJC circuit diagram for the two input converter is shown in Fig. 3.8.

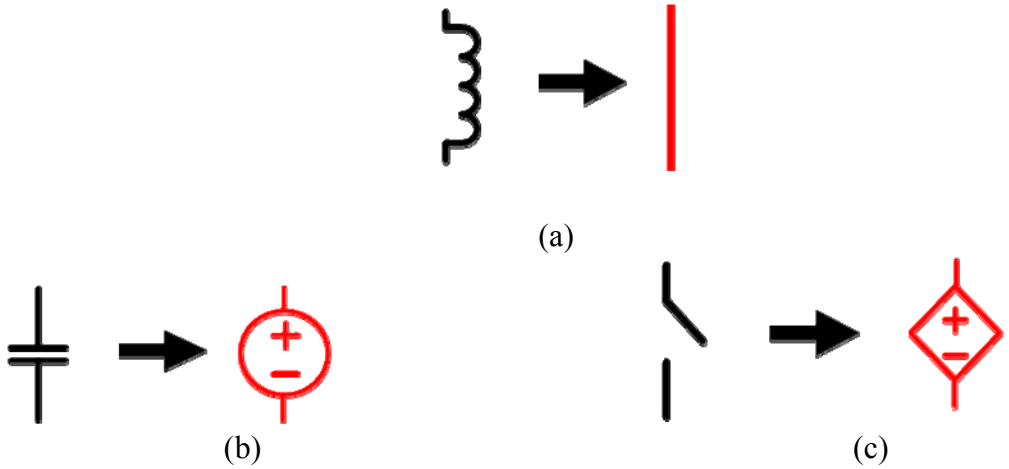


Figure 3.7: Components representation for averaged voltage analysis; (a) a inductor is replaced with a ideal wire (b) a capacitor is replaced with a independent voltage source (c) a switch is replaced with a dependant voltage source

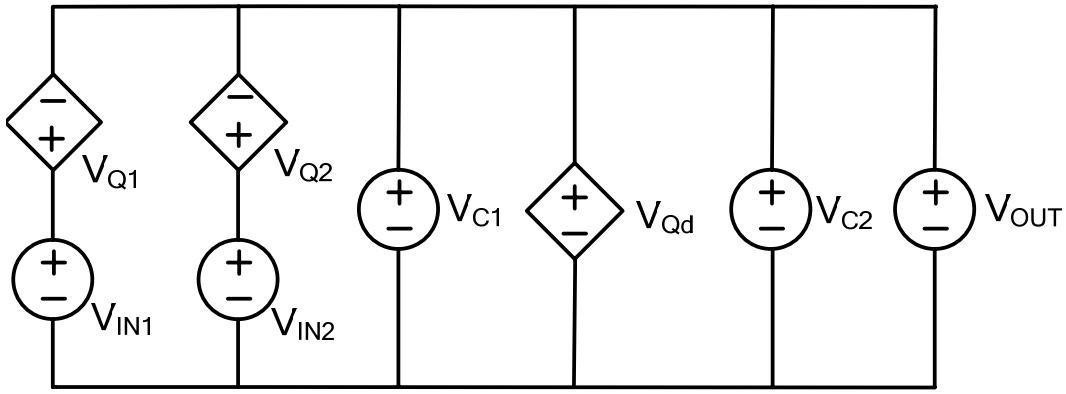


Figure 3.8: Averaged voltage mode equivalent circuit of two input modified inverse Watkins-Johnson Converter (MIMIWJC)

As can be seen in Fig.3.8, the equivalent circuit can be made easily just by replacing the original components with the averaged voltage mode components that are shown in Fig. 3.7. From Fig. 3.8, the two capacitors' average voltages, VC1, and VC2, are the same as the output voltage, hence,

$$V_{C1} = V_{C1} = V_{OUT} \tag{3.5}$$

Now, the dependent voltage sources can be expressed considering the switching status as shown in Fig. 3.5. First, the voltage across the main switch, V_{Q1}, only appears when the switch Q_1 is off. In other words, the voltage can be observed when the switch Q_2 and the diode Q_d are conducting, i.e., $D_{2eff}\ T_s$ and $(1\text{-}D_2)T_s$. The dependent voltage source, V_{Q1}, can be represented by

$$V_{Q1} = D_{1eff} \cdot 0 + D_{2eff}\left(V_{IN1} - V_{IN2}\right) + \left(1 - D_2\right)\left(V_{IN1} - 2V_{OUT}\right) \tag{3.6}$$

In a similar manner, the other two independent voltage source equations can be expressed by Eq. (3.7) and (3.8), respectively.

$$V_{Q2} = D_{1eff} \cdot \left(V_{IN2} - V_{IN1}\right) + D_{2eff} \cdot 0 + \left(1 - D_2\right)\left(V_{IN2} - 2V_{OUT}\right) \tag{3.7}$$

$$V_{Qd} = D_{1eff} \cdot (2V_{OUT} - V_{IN1}) \ + \ D_{2eff} \cdot (2V_{OUT} - V_{IN2}) \ + \ (1 - D_2) \cdot 0 \tag{3.8}$$

The above three equations, Eq. (3.6), (3.7) and (3.8), can be simplified by using the duty ratio relationship which is expressed in Eq. (3.9) and some simple algebraic manipulation.

$$D_{2eff} = D_2 - D_{1eff} \tag{3.9}$$

Equations (3.12), (3.13) and (3.14) are simplified forms of Eq.(3.8), (3.9) and (3.10), respectively.

$$V_{Q1} = V_{IN1} D_{1eff} + V_{IN2} D_{2eff} - 2V_{OUT}\left(1 - D_2\right) \tag{3.12}$$

$$V_{Q2} = V_{IN1} D_{1eff} + V_{IN2} D_{2eff} - 2V_{OUT}\left(1 - D_2\right) \tag{3.13}$$

$$V_{Qd} = -V_{IN1} D_{1ef\,f} - V_{IN2} D_{2eff} \; + \; 2V_{OUT} D_2 \tag{3.14}$$

Now, since all of the component values in Fig. 3.8 have been found, the averaged voltage relationships can be obtained by simply applying KVL in Fig. 3.8. The input to output relationship equation can be found by applying KVL to the loop that contains any dependent voltage source. The KVL equation for the outside loop that includes V_{IN1}, V_{Q1}, and V_{OUT} is

$$V_{IN1} - V_{Q1} = V_{OUT} \tag{3.16}$$

By plugging in Eq. (3.12) to Eq. (3.16) and doing some simple algebraic manipulations, the output voltage can be expressed in terms of input source voltages and duty ratios, as shown in Eq. (3.16).

$$V_{OUT} = -\frac{D_{1eff} V_{IN1} + D_{2eff} V_{IN2}}{1 - 2D_2} \qquad \text{where, } D < 0.5 \tag{3.16}$$

The other loops that contain the dependant voltage sources can be used to find the voltage relationships, too. For an *N*-input MIMIWJC, the averaged voltage mode circuit can be easily realized from Fig. 3.8. The *N*-inputs MIMIWJC averaged voltage mode circuit is shown in Fig. 3.9 by just adding a parallel branch for each input source and switch series combination. After obtaining the circuit diagram for the *N*-input case, the analysis is

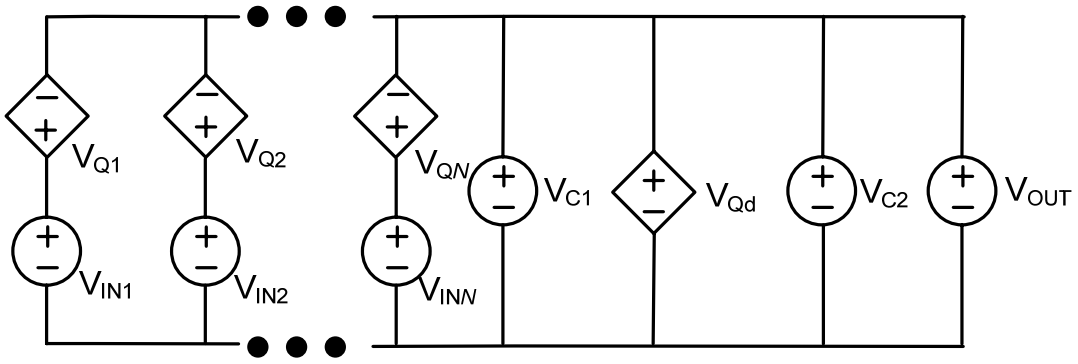


Figure 3.9: Averaged voltage mode equivalent circuit of N-inputs modified inverse Watkins-Johnson Converter (MIMIWJC)

analogous to the two-input case. The dependent voltage sources, V_{Qi} and V_{Qd}, can be expressed by Eq. (3.17) and (3.18), respectively.

$$V_{Qi} = \sum_{j=1}^{N} D_{jeff}(V_{INi} - V_{INj}) + (1 - D_N)(V_{INi} - 2V_{OUT}) \tag{3.17}$$

where, $j=i+1$.

$$V_d = \sum_{i=1}^{N} D_{i\_eff}(2V_{OUT} - V_{INi}) \tag{3.18}$$

By applying KVL to the Fig. 3.9, the *N*-input MIMIWJC converter's input to output voltage relation can be found by

$$V_{OUT} = -\sum_{i=1}^{N} \frac{D_{i\_eff}}{1 - 2D_N} V_{INi} \tag{3.19}$$

3.3.1.2 AVERAGED CIRCUIT ANALYSIS IN CURRENT MODE

Similarly to the averaged voltage mode analysis, the averaged current mode analysis can explain dc current relationships between input sources, output load currents

and currents in inductors. The analysis technique is also similar to the averaged voltage mode analysis. The averaged current mode equivalent circuit should be made first. To make the equivalent circuit, the averaged currents in each component in Fig. 3.6 have to be found. The equivalent circuit building process is a similar concept as that of the averaged voltage mode equivalent circuit. That is, the averaged current in the capacitor in steady-state can be represented as an open circuit by Eq. (3.6) in the averaged current mode circuit. The inductors can be represented as independent current sources in the averaged current mode circuit as the capacitors are replaced by voltages sources in the averaged voltage mode circuit. The switching components can be represented as dependent current sources as these are expressed as dependent voltage sources in the averaged voltage mode circuit. Figure 3.10 shows the component substitution process to make the averaged current mode circuit, where the components representations are shown in terms of circuit symbols. Figure 3.11 shows the equivalent current mode averaged circuit of the two-input MIMIWJC based on the rules in Fig. 3.10. The averaged currents of switches can be found by observing the current waveforms during each switching action. The currents of the FCBB switches only exist while the switches are in the on-state. Thus, the averaged Q_1 and Q_2 switch current can be expressed by

$$I_{Q1} = D_{1eff} \cdot I_{in1} \tag{3.20}$$

$$I_{Q2} = D_{2eff} \cdot I_{in2} \tag{3.21}$$

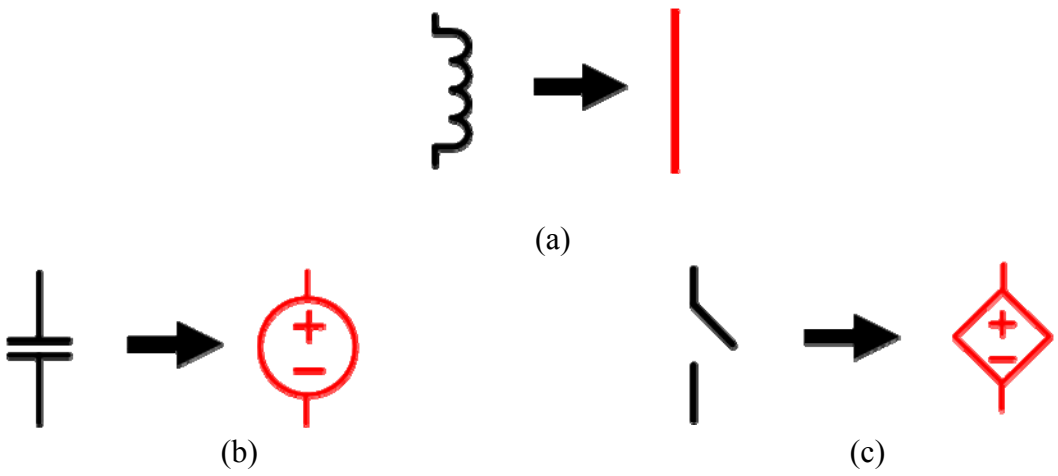


Figure 3.10: Components representation for the averaged current analysis; (a) an inductor is replaced with an ideal wire (b) a capacitor is replaced with an independent voltage source (c) a switch is replaced with a dependent voltage source

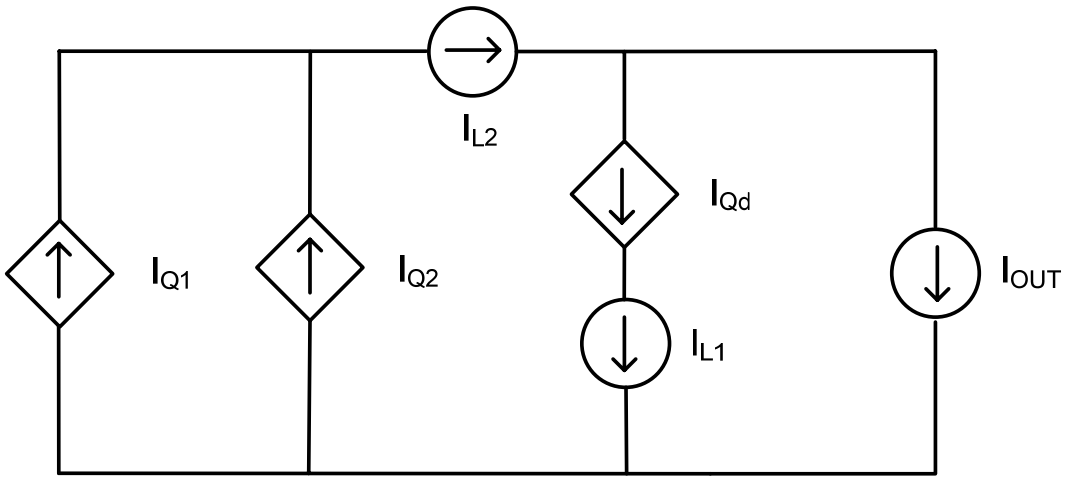


Figure 3.11: Averaged current mode equivalent circuit for a 2-inputs modified inverse Watkins-Johnson Converter (MIMIWJC)

Note that in here, although I_{in1} and I_{in2} are dc values, these are not the averaged currents of the input sources but flat topped values of each input source current. To aid understanding the input currents definition, the average power of each source and output are expressed in (3.22) and (3.23).

$$P_{IN1} = V_{IN1} \cdot D_{1eff} I_{in1} \tag{3.22}$$

$$P_{IN2} = V_{IN2} \cdot D_{2eff} I_{in2} \tag{3.23}$$

To find the diode average current, the current waveform of the diode can be considered. The capacitor current in many converters, such as the output filter capacitor of buck, boost, and buck-boost converters, is zero if the averaging interval is set to either on-time or off-time of the main switch. However, the averaged capacitor currents in the MIMIWJC are zero only when the average interval is set to whole switching period, T_S. Considering capacitor current characteristics, the averaged diode current, I_{Qd}, can be found by

$$I_{Qd} = (1 - D_2)(I_{L1} + I_{L2}) = I_{L1} \tag{3.24}$$

Although tt is true that the averaged diode current is equal to the inductor current I_{L1} as can be seen in Fig. 3.11, the diode current is not always the same as the inductor current. That is, the averaged diode current is the same as the inductor current I_{L1} only in the average sense. From Eq. (3.24), it is interesting that the two inductor current relationships can be expressed by the function of the maximum duty ratio, D_2 as shown in Eq. (3.25).

$$\frac{I_{L1}}{I_{L2}} = \frac{1 - D_2}{D_2} \tag{3.25}$$

In equation (3.25), it is interesting that the ratio of the two inductor currents is constant if the maximum duty ratio D_2 is fixed, even though the two inductors are not magnetically coupled. Since all the dependent current sources are expressed in terms of the other circuit parameters, the averaged current relationships can be found by applying KCL to the Fig. 3.11 just as KVL was applied in Fig. 3.8. The inductor L_2 average current is the sum of the two FCBB switches current, as shown in Eq. (3.26)

$$I_{L2} = D_{1eff} I_{in1} + D_{2eff} I_{in2} \tag{3.26}$$

The average output current can be determined by the difference between the two inductor average currents as shown by

$$I_{OUT} = I_{L2} - I_{L1} \tag{3.27}$$

Finally, the average input to output current relationship can be found by using KCL and some algebraic manipulation, resulting in

$$I_{OUT} = -\frac{(1-2D_2)}{D_2}\left(D_{1eff} I_1 + D_{2eff} I_2\right) \tag{3.28}$$

For an *N*-input MIMWJC, the average current mode equivalent circuit can be easily realized by adding parallel current sources which is shown in Fig. 3.12. Hence, Eq. (3.26) and (3.28) can be extended to Eq. (3.29) and (3.30), respectively.

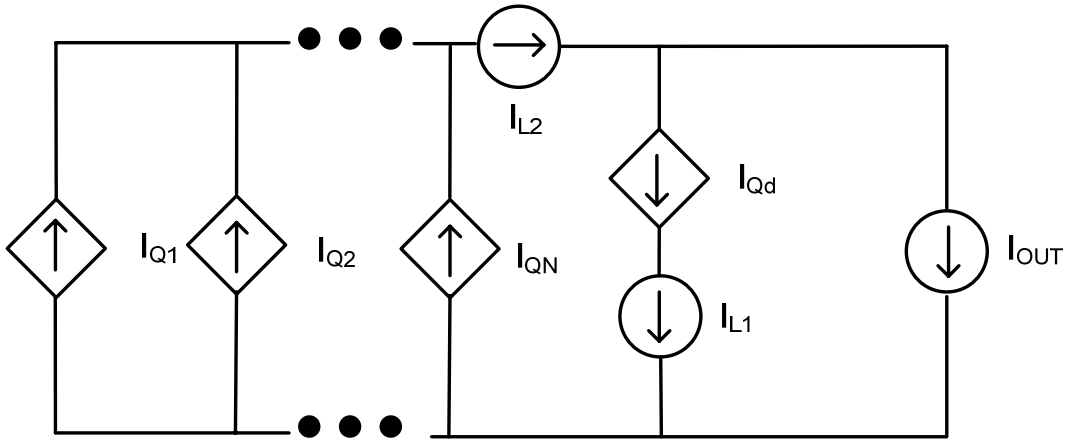


Figure 3.12: Averaged current mode equivalent circuit of N-inputs modified inverse Watkins-Johnson Converter (MIMIWJC)

$$I_{L2} = \sum_{i=1}^{N} D_{i\_eff} I_i \tag{3.29}$$

$$I_{OUT} = -\frac{(1-2D_N)}{D_N} \sum_{i=1}^{N} D_{i\_eff} I_i \tag{3.30}$$

3.3.2 RIPPLE COMPONENT ANALYSIS BY SWITCHING ACTION

In this section, current and voltage waveforms are analyzed based on switching commands and circuit states. The waveform shapes can be used for calculating rms or peak current and voltage values of components along with the averaged information from the previous section. For the two input MIMIWJC case, the switching status can be divided into three modes, as shown in Fig. 3.13 according to the switching commands. Mode I and Mode II are charging periods, and Mode III is a discharging period of the circuit. That is, in the CCM operation, the number of MIMIWJC converter's charging periods is the same as the number of input sources, and the discharging period happens

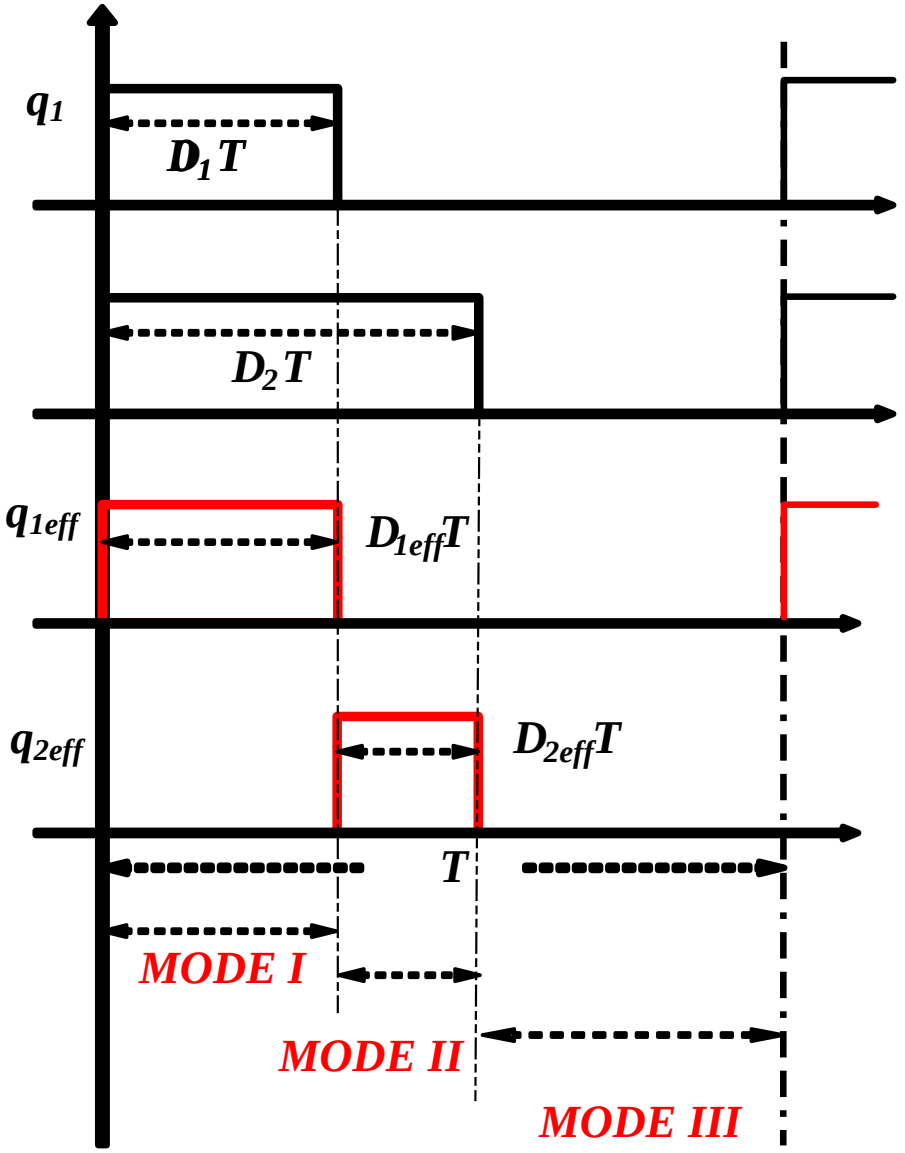


Figure 3.13: Switching status diagram based on switching commands, q_1 and q_2.

once in one switching period, T_s. A reduced equivalent circuit according to each switching status can be made. Most of the assumptions which are made in Section 3.3.1 are also valid throughout this section. A small ripple approximation is applied, and the loading effects or other non-linear effects are ignored in this section.

3.3.2.1 MODE I

The Mode 1 period is defined as follows: both switching commands are on and the diode is reverse biased. The switching state and time period can be expressed as

$$q_1=1 \;\&\; q_2=1 \;\&\; q_d=0 \qquad\qquad (0 < t \le D_{1eff}T_s)$$

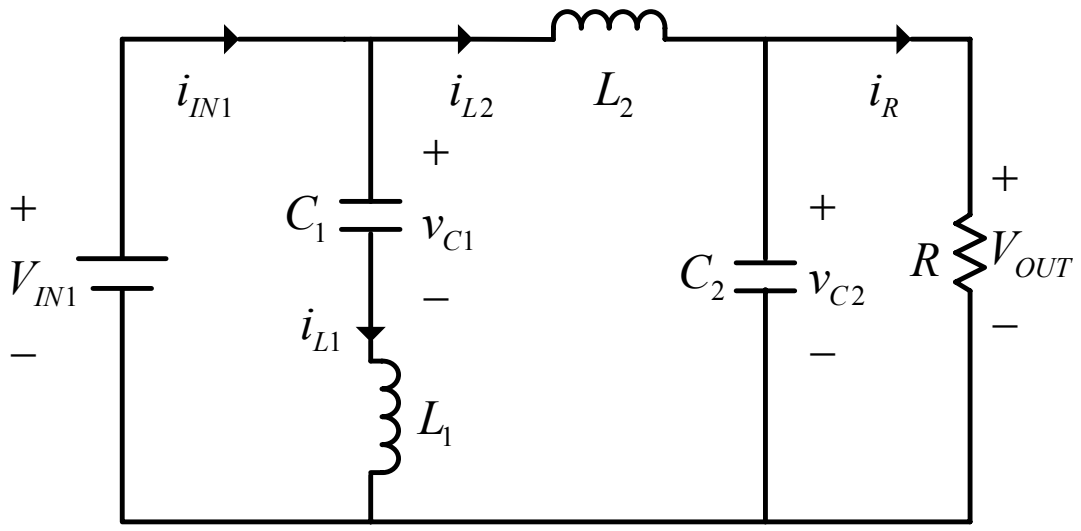


Figure 3.14: Equivalent circuit for mode I. ($0 < t \le D_{1\text{eff}}T_s$)

At this mode, even though the q_2 switching command is on i.e., 1, the current, I_{in1}, can only flow from V_{in1} since the V_{in1} is assumed to have a higher voltage than $V_{in2.}$ The equivalent circuit for this period is shown in Fig. 3.14. At Mode I, all the passive reactive components, L_1, L_2, C_1, and C_2 are charging from V_{in1}, so the currents in the inductors, i_{L1} and i_{L2} are ramping up, and the voltages across the capacitors, v_{C1} and v_{C2} are also ramping up. From the equivalent circuit, Fig. 3.14, with the small ripple approximation, the charging equation for inductors and capacitors can be found. During this interval, the two inductor currents, i_{L1} and i_{L2} are given by

$$\begin{aligned} i_{L1} &= \frac{(V_{in1} - V_{C1})}{L_1} t \\ i_{L2} &= \frac{(V_{in1} - V_{C2})}{L_2} t \end{aligned} \tag{3.31}$$

During this mode, the two capacitor voltages, v_{C1} and v_{C2}, can be found by observing the capacitor currents of C_1 and C_2.

$$\begin{aligned} v_{C1} &= \frac{I_{L1}}{C_1} t \\ v_{C2} &= \frac{I_{L2} - I_R}{C_2} t = \frac{I_{L1}}{C_2} t \end{aligned} \tag{3.32}$$

In Eq. (3.32), it is interesting that the charging currents for the two capacitors are the same as I_{L1}.

3.3.2.2 MODE II

$$q_1=0 \;\&\; q_2=1 \qquad (D_{1\text{eff}}T_s < t \le D_2T_s)$$

During this period, the input energy source is changed from V_{IN1} to $V_{IN2,}$ and it is still in charging mode. The equivalent circuit for this period is shown in Fig. 3.15, which is the same as Fig. 3.14 except for the input source. Most waveforms are similar to the wave forms of Mode I, except for changing the input power source. Since it is still operated in charging mode, the I_{L1}, I_{L2}, V_{C1} and V_{C2}, are also ramping up. However, the inductor currents ramping up slopes are mitigated because V_{in2} is assumed to be less than V_{in1} while the capacitor voltages keep the same ramping up slope since the charging current is the same under the small ripple approximation. Thus, the capacitor charging equations is not expressed in this section because that is the same as Eq. (3.32). The inductor currents charging equation during this interval can be obtained by

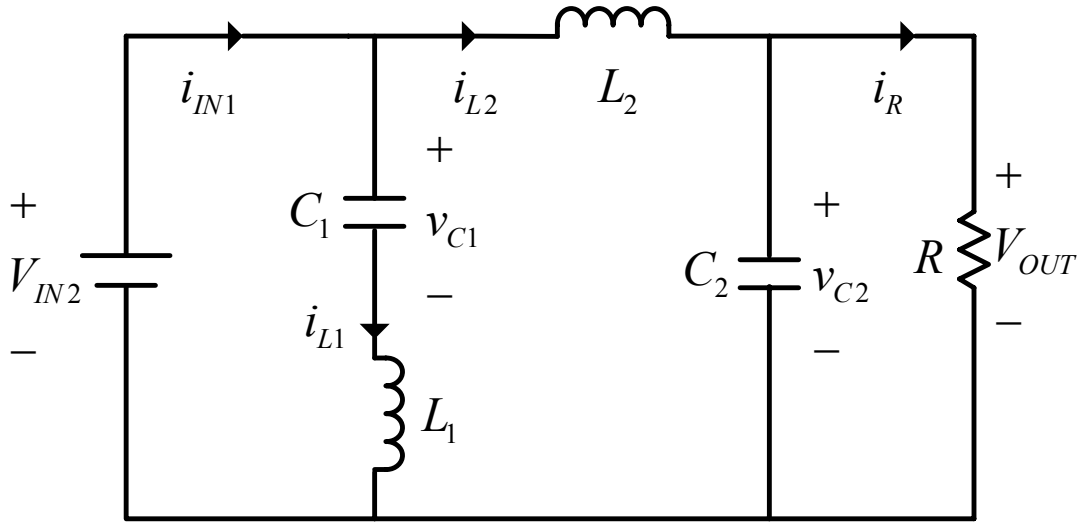


Figure 3.15: Equivalent circuit for Mode II. ($D_{1\text{eff}}T_s < t \leq D_2T_s$)

$$i_{L1} = \frac{(V_{in2} - V_{C1})}{L_1} t$$
$$i_{L2} = \frac{(V_{in2} - V_{C2})}{L_2} t \tag{3.33}$$

3.3.2.2 MODE III

Mode III appears when Q_1 and Q_2 are off and, hence, the diode is forward biased. The switching state and time interval can be expressed as

$$q1=0 \;\&\; q2=0 \qquad (D_2T < t \leq T)$$

The equivalent circuit for Mode III is shown in Fig. 3.16. During this period, all the passive storage elements are discharging since there is no connection between passive elements and any of the input power sources. Thus, all the voltages and currents have a negative slope in this period. For the mode I and II, the C_1 and L_1 are connected in a series, and C_2 and L_2 are connected in a series, and each of these branches are

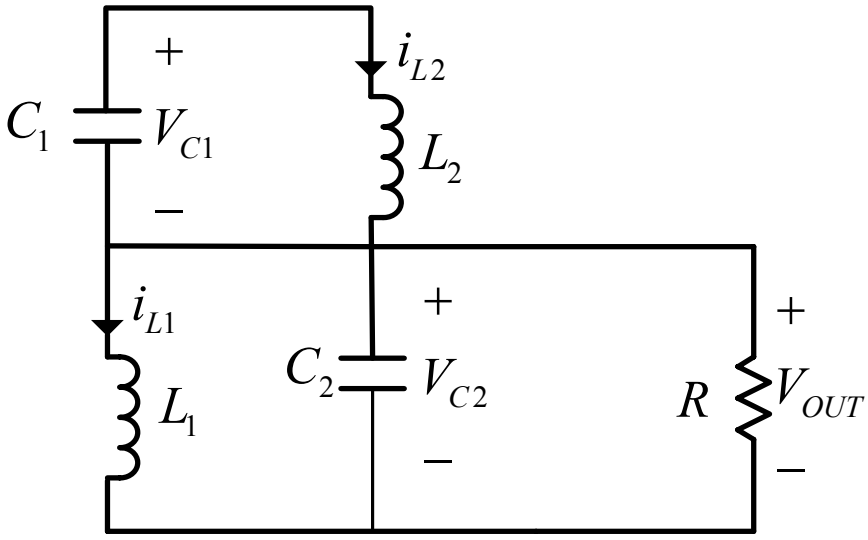


Figure 3.16: Equivalent circuit for Mode III. ($D_2T_s < t \leq T_s$)

connected in parallel with the input voltage source. However, at this period, Mode III, C_1 and L_2 are in parallel and L_1 and C_2 are in parallel, as shown in Fig 3.17. During this period, the voltage across the L_1 inductor is the same as V_{C2} and the voltage across L_2 is equal to V_{C1}. On the other hand, the current in the C_1 becomes the I_{L1}, and the current in the C_2 becomes the I_{L2} even though the current direction is reversed. Equation (3.34) and (3.35) shows the inductor currents and capacitor volages during this mode.

$$\begin{aligned} i_{L1} &= \frac{V_{C2}}{L_1} t \\ i_{L2} &= \frac{V_{C1}}{L_2} t \end{aligned} \tag{3.34}$$

$$\begin{aligned} V_{C1} &= -\frac{I_{L2}}{C_1} t \\ V_{C2} &= -\frac{I_{L1} + I_R}{C_2} t = -\frac{I_{L2}}{C_2} t \end{aligned} \tag{3.35}$$

3.4 BOUNDARY CONDITION BETWEEN CCM AND DCM

So far, the CCM operation has always been assumed in this chapter. Then, it is worthwhile to find the circuit parameters of the MIMIWJC in order to maintain the CCM operation. In many dc-dc converters, continuous conduction mode (CCM) can be defined by whether the inductor current goes to zero or not. Thus, in many cases, CCM stands for continuous current mode of the filter inductor, too. However, if there are two inductors in a converter, such as Ćuk and SEPIC, the zero currents in the inductors cannot tell the discontinuous conduction mode (DCM). Figure 3.17 (a) and (b) shows the inductor current waveforms in DCM for a single inductor topology and a two inductor topology.

As can be seen in Fig. 3.17 (b), the inductor current never goes to zero even in the DCM operation in the two inductor dc-dc converter. In the case of a dc-dc converter topology which has two inductors in it, the existence of a zero voltage across the inductor can be used to distinguish the CCM and DCM. In other words, if a zero voltage across the inductor appears, the converter is operated in DCM. However, the diode current goes to zero while the main switch is off whether a converter has a single inductor topology or two inductors. The diode current, i_{Qd}(t), in DCM is shown in Fig. 3.18. Since the MIMIWJC has two inductors, the diode current waveform can be use to find a boundary condition between CCM and DCM.. If the diode current is zero at the end of its conduction time, i.e., just before the FCBB switches begin to conduct, then the converter is operated in boundary condition. From Fig. 3.16, the diode current at the discharging period is

$$i_D = i_{L1} + i_{L2} \tag{3.36}$$

By definition of the boundary condition, the Eq. (3.36) is zero at the end of the discharging time. Then, the Eq. (3.36) can be

$$\begin{aligned} i_d &= i_{L1} + i_{L2} \\ &= I_{L1} + I_{L2} + \frac{1}{2}\left(\frac{V_{OUT}}{L_1}\right)\Delta t + \frac{1}{2}\left(\frac{V_{OUT}}{L_2}\right)\Delta t \\ &= 0 \end{aligned} \tag{3.37}$$

where, $\Delta t = (1\text{-}D_2)T_s$, discharging time.

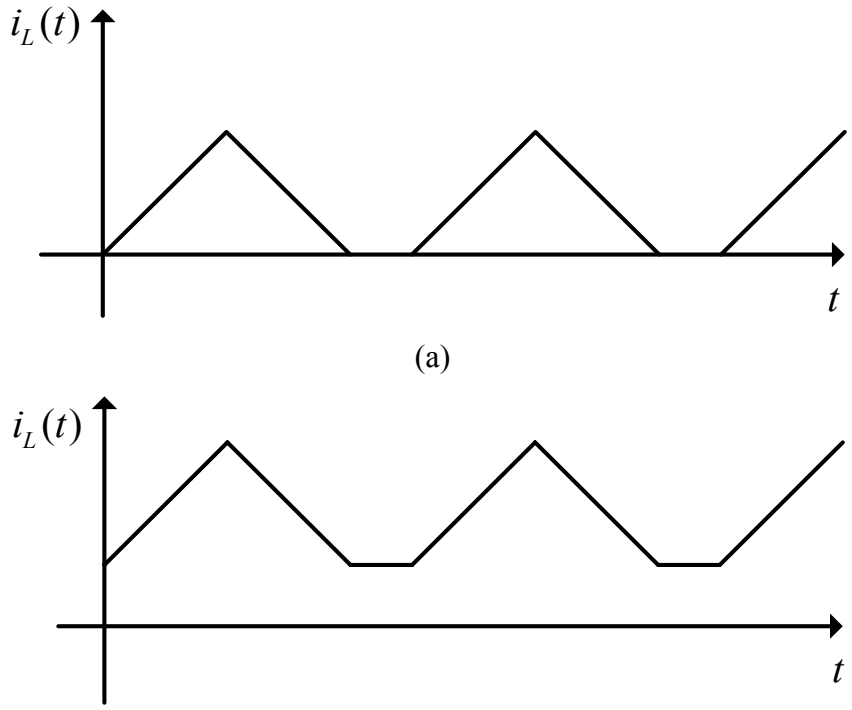


Figure 3.17: Inductor current waveforms in discontinuous conduction mode: $i_L(t)$ in single inductor topology, (b) $i_L(t)$ in two inductor topology

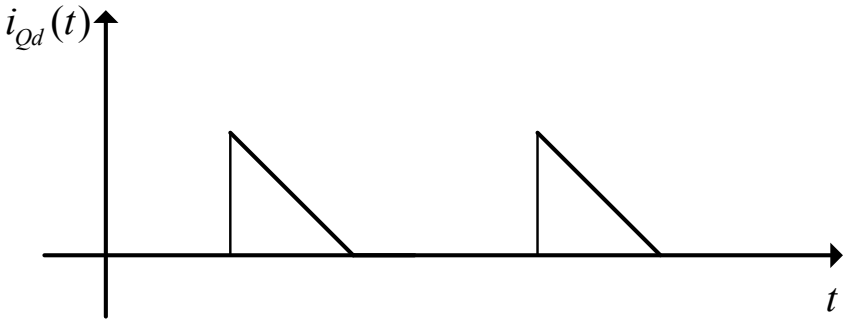


Figure 3.18: Diode current waveform in discontinuous conduction mode

The critical inductance, L_{crit}, necessary to maintain CCM operation, can be obtained by plugging in Eq. (3.25) and doing some algebraic manipulation, as shown in Eq. (3.38).

$$L_{crit} = \frac{R(1-2D_2)(1-2D_2)}{2} T_s \tag{3.38}$$

where, $L_{crit} = L_1 \| L_2$.

The critical inductance can be used to determine the inductor values of the MIMWJC to operate in CCM. In other words, if the parallel impedance of the two inductors is greater than or equal to L_{crit} then the MIMIWJC can be guaranteed to operate in CCM.

3.5 DISCUSSION

This section provides an analysis of the results of the MIMIWJC which have been discussed in Sections 3.2 and 3.3, and some important waveforms are shown, based on the analysis of Section 3.2 and 3.3. The inductor current and capacitor voltage wave forms can be obtained by summing the averaged and ripple components which are analyzed Sections 3.2 and 3.3 respectively. To simplify the analysis and help to understand the circuit behavior characteristics easily, the same inductance for L_1 and L_2 and the same capacitance for C_1 and C_2 are used in this section.

Since both capacitor charging currents are the same as I_{L1}, and the discharging currents of each capacitor are the same as I_{L2}, the voltage wave forms of the two capacitors should always be the same, which is expressed in Eq. (3.32) and (3.35).

It is interesting that the two inductor average current relationships are deteremined by the higest duty ratio D_2 as expressed in Eq. (3.25) and the difference between two inductor currents, (i_{L2} - i_{L1}), becomes the output current I_{out}. Since the maximum duty ratio cannot exceed 0.5, the magnitude of I_{L1} is always greater than that of I_{L2} by Eq. (3.25). As a result of that, the output current, I_{OUT} in Fig. 3.6, is always smaller than zero. The curreent shapes in both inductors can be the same if the two inductor values are the same. It is also interesting that if either FCBB switch Q_1 or Q_2 is on, the currents in each capacitor are same as I_{L1}, whereas when the all the switches are off, the currents in the capacitors become -I_{L2}. Inductor current and capacitor voltage waveforms are shown in Fig.3.19. For FCBB swith, the switch voltages and diode current waveforms are displayed in Fig. 3.20.

Assuming a perfect lossless conversion process, the input-to-output power balance serves to obtain the power at each input leg, which is given by

$$P_{IN,k} = -\frac{V_{OUT}}{R}\frac{D_{eff,k}}{1-2D_N}V_{IN,k} \qquad k = 1,2,3.....N \tag{3.39}$$

From Eq. (3.39), if the output voltage is fixed, then the power drained from each source is not fully independent of the other. For the two input source case, the power relationship between P_1 and P_2 is expressed by

$$P_2 = \frac{D_{2e}(1-D_1)}{D_1(1-D_{2e})}P_1 \tag{3.40}$$

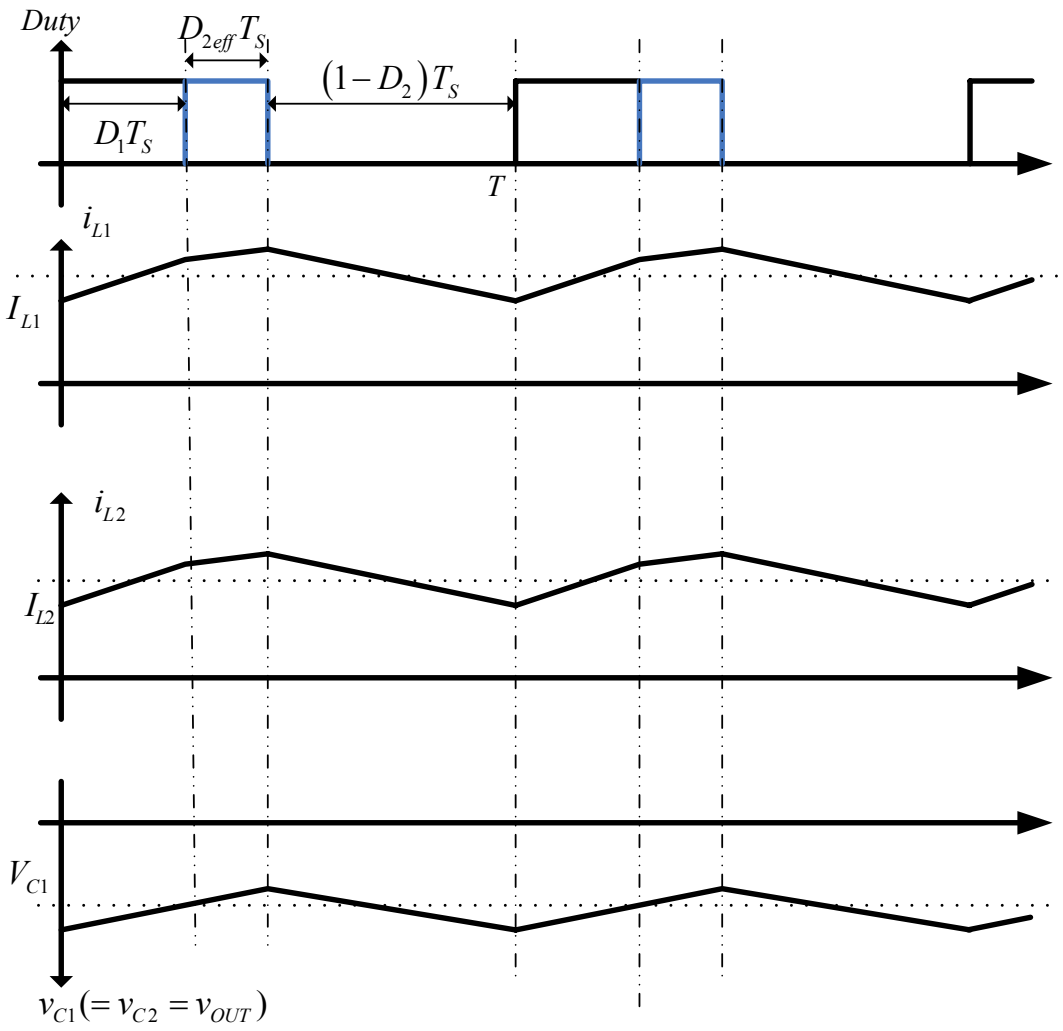


Figure 3.19: Inductor currents and capacitor voltage waveforms according to switching action

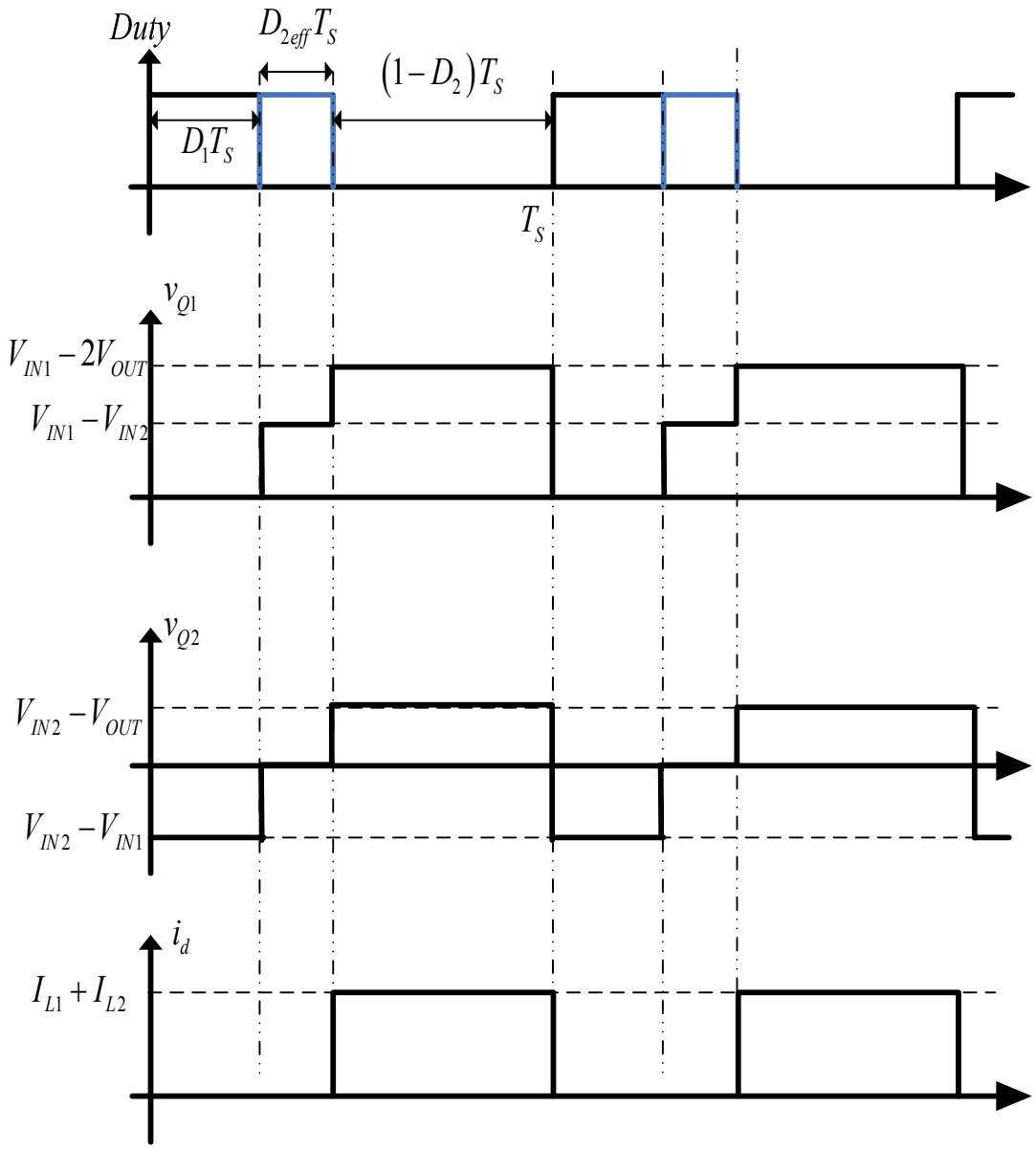


Figure 3.20: Two main switch voltages and the diode current waveforms.

3.6 CONCLUSION

A new MIMIWJC is proposed, and having made reasonable assumptions, an analysis is done through the averaged circuit model and ripple component analysis. As shown in Fig. 3.1, since the MIMIWJC can have a higher conversion ratio than that of boost or buck-boost converter for the same given duty ratio, it can provide more operational flexibility. Besides, since the input module can consist of one FCBB switch, the proposed topology can be favorable in terms of expected cost. In addition, because the proposed topology has been modified not to have a transformer in its configuration, modularity potential can be increased. The averaged voltage and current equivalent circuit analyses shown in Section 3.2 can give meaningful information for understanding the dc behavior of the proposed converter and they can be extended easily for an N-input MIWJC analysis by just adding input source branches to the equivalent circuit. The ripple components analysis results can be used for understanding how each component behaves during each switching state. The critical waveforms that are shown in Fig. 3.19 and 3.20 could serve as a foundation for hardware design and power budgeting for a MIMIWJC. Some of these equations and waveforms are verified with simulation and hardware experiments in Chapter 5 of this dissertation.

Chapter 4: Proposed Converter Dynamics and Control

4.1 INTRODUCTION

This chapter is devoted to describing modeling and operation techniques for the proposed converter. To operate the dc-dc converter or any power system, a dynamic system analysis is one of the key parts. Typically, to make the feedback system stable, the understanding of system behavior is desired through a well developed model. Since the linear analysis technique is not only familiar but also very well developed in the literature, it is beneficial to use the linearized models [1, 33]. However, the dc-dc converter is not a linear circuit since it has switching components in it. Thus, to apply a linear control theory, the linearization process of the switching converter should precede the dynamic analysis. In this chapter, two linearization techniques are introduced for analyzing the switching of power supplies. First, the state space averaging [34] is presented, and second, the circuit averaging method [35-37] is described. To make the analysis simpler, the following two assumptions are made throughout this chapter. First, all the components are ideal. Secondly, the switching frequency is high enough to ignore switching ripples on the passive components. That is, the system's natural frequency is much lower than the switching frequency so that the small ripple approximation can be applied. The averaging and linearizing methods are based on one single input MIWJC with the equivalent source concept of MIC. The two possible operation methods for MIC are also introduced and described in this chapter.

4.2 AC MODELING METHODS AND APPROACH

Power converter circuits are nonlinear system s since they include nonlinear devices, i.e., switching devices. To apply a linear control theory, a linearized converter circuit model is needed. The averaging method not only yields meaningful information but also helps to make the linearized switching power converters simple to analyze [38]. The two most frequently used ac modeling methods for dc-dc converters are state-space averaging and circuit-averaging methods, which are both based on averaging and linearization. The state-space averaging method is more convenient for numerical computer simulation, and it can be standardized for all dc-dc converters since the state-space is a canonical form of the differential equation [39]. However, the state-space averaging method needs matrix algebra, and the amount of calculations could be large. The circuit-averaging can give more intuitive physical insight because it is based on circuit analyses instead of matrix equations. The ac modeling method described in this section can be used for any MICs based on the equivalent source concept shown in Section 4.3.

4.2.1 STATE-SPACE AVERAGING METHOD

A linear differential equation can be represented based on the matrix form of the state equation as shown in Eq. (4.1).

$$\begin{aligned} \mathbf{K}\dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{E}\mathbf{u}(t) \end{aligned} \tag{4.1}$$

Here, the vector, $\mathbf{x}(t)$ is the state vector and its components are state variables which are mostly composed of inductor currents and capacitor voltages. The vector, $\mathbf{u}(t)$ is the input or control vector, such as the input voltage, and $\mathbf{y}(t)$ is the output vector, usually the output voltage can be chosen for the output vector. Here, $\mathbf{K}$ is a matrix which contains system parameters, such as the values of capacitance and inductance, etc. The matrices A, B, C, E contain constants to describe the linear relationships of the Eq. (4.1).

In continuous conduction mode, PWM converters can have two switching states and therefore the two different equivalent circuits can be made by the switching status [34]. When main switch is on, the converter can be seen as a linear circuit, and the state equation can be represented by

$$\begin{aligned} \mathbf{K}\dot{\mathbf{x}}(t) &= \mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_1\mathbf{x}(t) + \mathbf{E}_1\mathbf{u}(t) \end{aligned} \tag{4.2}$$

When the main switch in off, the converter can be seen as another linear circuit and its state equation is

$$\begin{aligned} \mathbf{K}\dot{\mathbf{x}}(t) &= \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_2\mathbf{x}(t) + \mathbf{E}_2\mathbf{u}(t) \end{aligned} \tag{4.3}$$

When the PWM converter's natural frequency is much lower than the switching frequency, the steady-state dc state-space averaged model equation is

$$\begin{aligned} \mathbf{X} &= -\mathbf{A}^{-1}\mathbf{B}\mathbf{U} \\ \mathbf{Y} &= \left(-\mathbf{C}\mathbf{A}^{-1}\mathbf{B} + \mathbf{E}\right)\mathbf{U} \end{aligned} \tag{4.4}$$

The **X**, **U,** and **Y** represent the dc state vectors and the averaged matrices, **A, B, C, E** can be found by

$$\begin{aligned}\mathbf{A} &= D\mathbf{A}_1 + D'\mathbf{A}_2 \\ \mathbf{B} &= D\mathbf{B}_1 + D'\mathbf{B}_2 \\ \mathbf{C} &= D\mathbf{C}_1 + D'\mathbf{C}_2 \\ \mathbf{E} &= D\mathbf{E}_1 + D'\mathbf{E}_2\end{aligned} \tag{4.5}$$

where, D is the dc component of the duty cycle and D'=1-D.

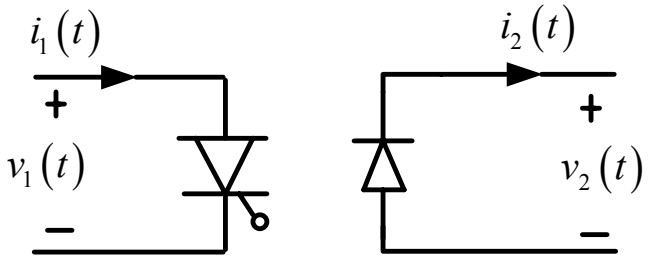
The state-space equation for the linearized small-signal ac model can be represented by

$$\begin{aligned}\mathbf{K}\dot{\hat{\mathbf{x}}}(t) &= \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \left\{(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}\right\}\hat{d}(t) \\ \hat{\mathbf{y}}(t) &= \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \left\{(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{E}_1 - \mathbf{E}_2)\mathbf{U}\right\}\hat{d}(t)\end{aligned} \tag{4.6}$$

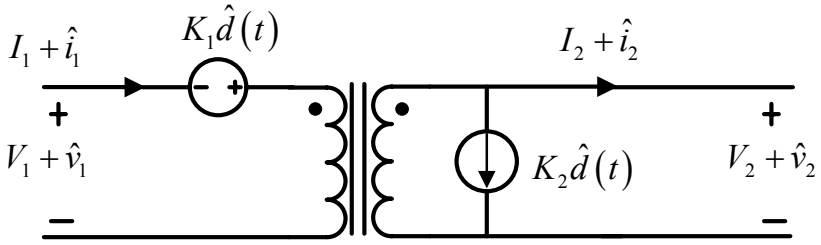
where, $\hat{\mathbf{x}}(t), \hat{\mathbf{u}}(t), \hat{\mathbf{y}}(t)$ and $\hat{d}(t)$ are small ac variations or perturbed quantities. Equations. (4.4) and (4.6) can be used for any CCM operating dc-dc converter to obtain the steady-state averaged model of the converter.

4.2.2 CIRCUIT AVERAGING METHOD

The nonlinear components in a switch mode power supply include the switching devices, such as MOSFET, IGBT, diode, and others. Thus, if the switching components can be represented as continuous circuit components by using averaged current and voltage relationship, a switching converter can be viewed as a continuous circuit. There are some modeling techniques for representing a switching network, but in this section the simplest method is applied. Although the Vorperian's PWM switch model [37] is one of the most frequently used models, it is not easy to be directly applied to a switch



(a)

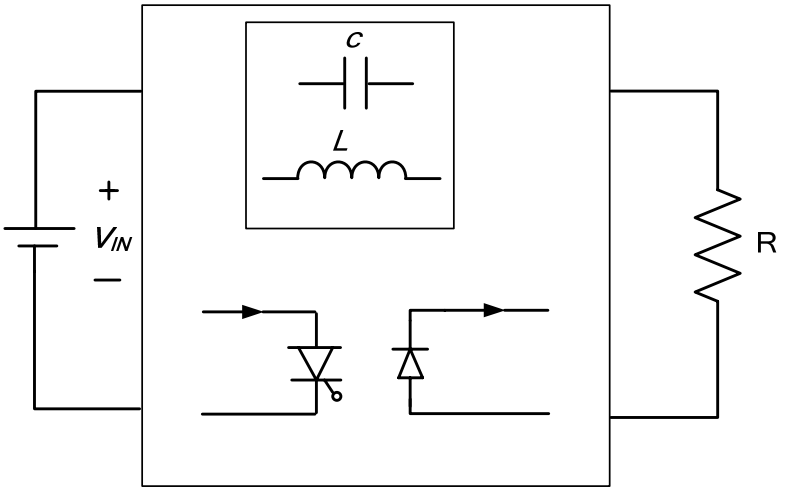


(b)

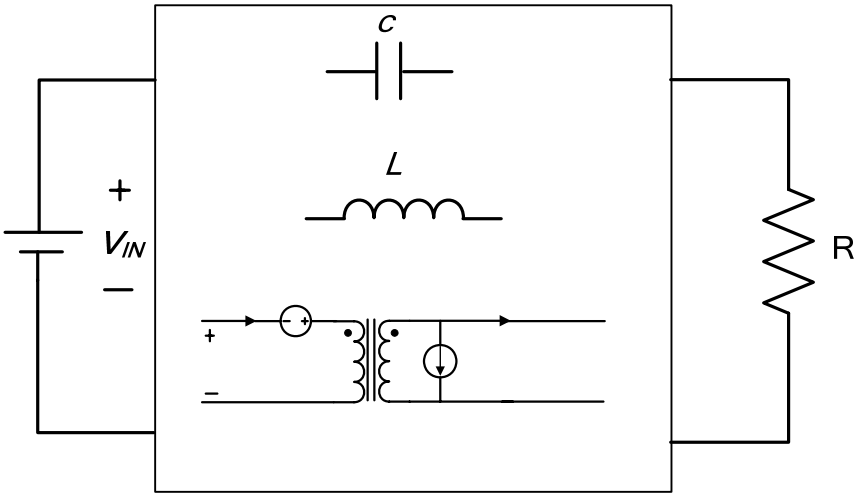
Figure 4.1: Switch modeling. (a) Switch network of a dc-dc converter. (b) Averaged switch network of a dc-dc converter

network that does not have a common connecting point. The inverse Watkins-Johnson converter's switching network does not have a common point, so the averaged switch model is more proper than Vorperian's model.

Figure 4.1 (b) shows the averaged switch network representation of the switching network. Here, K_1 and K_2 are constants which are composed of the averaged voltages and currents of the switching network, V_1, V_2, I_1, I_2, and the normalized duty ratio, D. The detailed method of how to find the K_1 and K_2 will be explained later in this chapter with an example of the real converter, an inverse Watkins-Johnson convert case. The large signal averaged circuit model can be obtained by simply replacing the switch network



(a)



(b)

Figure 4.2: Conceptual diagram of an averaged circuit model: (a) Switched circuit a dc-dc converter. (b) Averaged circuit model

with the averaged switch model as shown in Fig. 4.2. The detailed method of how to make a complete averaged circuit model for dc and small signal analyses will also be explained with an example of an inverse Watkins-Johnson converter.

4.3 EQUIVALENT SOURCE REPRESENTATION

Since a multiple input converter is a multiple input single output (MISO) system, the analysis should be different with single input converter case. However, in the case of the combination of the main FCBB switches and the time sharing concept with a single PWM carrier signal, it is possible that multiple sources can be represented as a single averaged equivalent source. That is, a MIC can be represented and analyzed in the same way as a single input dc-dc converter. In the case of the two input MIC, the Eq. (4.7) can be used for the averaged source value, and for the ***N*** input case, Eq. (4.8) can be used for the value of the equivalent source. This equivalent source can be applied to both state-space averaging and circuit averaging methods of a MIC.

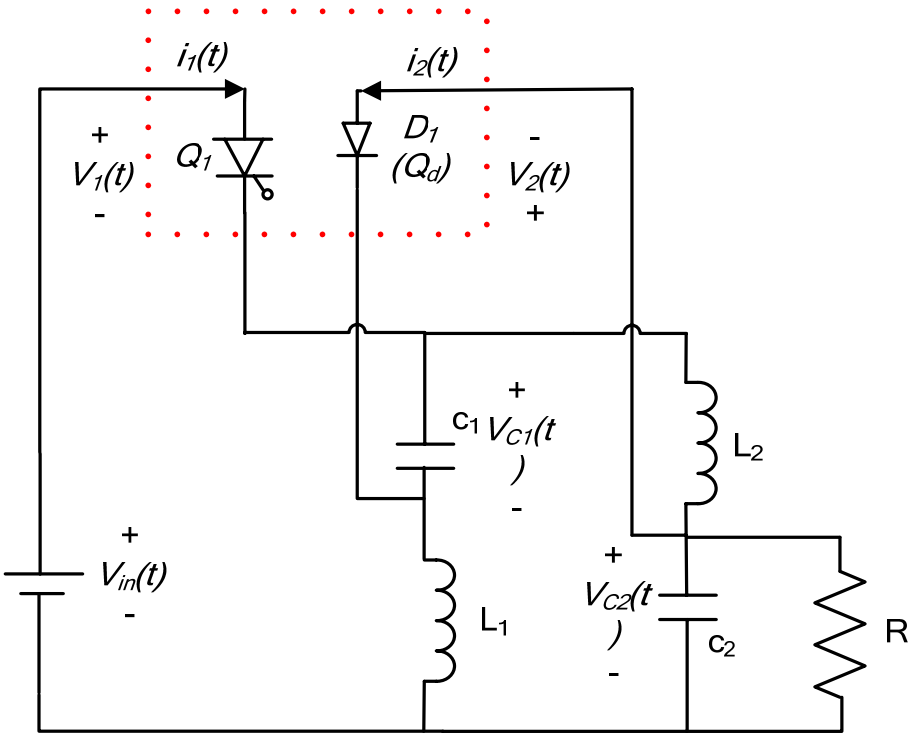
$$V_{eq} = \frac{D_{1e}V_{in1} + D_{2e}V_{in2}}{D_2} \tag{4.7}$$

$$V_{eq} = \frac{\sum_{i=1}^{N} D_{ieff}V_{in\_i}}{D_N} \tag{4.8}$$

4.4 AVERAGED CIRCUIT MODEL OF THE PROPOSED MIMIWJC

In this section the small signal model of the proposed MIMIWJC is derived. As mentioned in Section 4.2, the model can be derived by using either a state-space or an

averaged circuit model. However, since an averaged circuit model can give more intuitive knowledge of the circuit, in this section the small signal model is derived using the averaged switch network. To develop a linearized circuit model, a switching network should be modeled linearly since the only nonlinear devices in a dc-dc converter are its switching components. Figure 4.3 shows a modified inverse Watkins-Johnson converter topology with an emphasis on the switching network. Based on two-port network theory, one can choose one terminal voltage and current as independent inputs. For convenience, $i_1(t)$, and $v_2(t)$ in Fig. 4.4 are chosen for the independent inputs of the switch network.



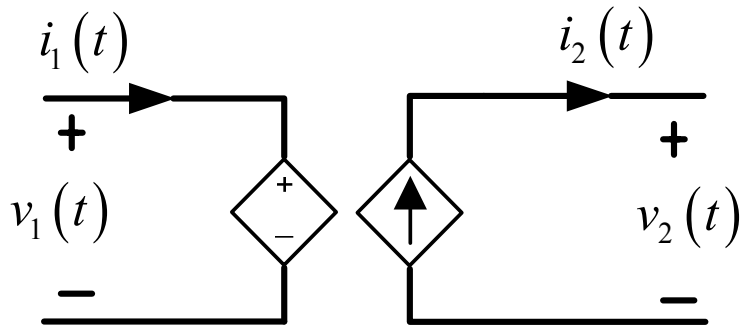


Figure 4.4: Two port network model of switch network

Then the other voltage and current can be expressed as dependent outputs, as shown in Fig. 4.4

The observed voltages and current waveforms at each port of the MIWJC's switching network are expressed in Fig. 4.5. The averaged waveforms over one period at each switch terminal can be expressed as follows:

$$\left\langle v_1(t)\right\rangle_{T_s} = d'(t)\left(V_{in} - \left\langle v_{C1}(t)\right\rangle_{T_s} - \left\langle v_{C2}(t)\right\rangle_{Ts}\right) \tag{4.9}$$

$$\left\langle i_1(t)\right\rangle_{T_s} = d(t)\left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{Ts}\right) \tag{4.10}$$

$$\left\langle v_2(t)\right\rangle_{T_s} = d(t)\left(V_{in} - \left\langle v_{C1}(t)\right\rangle_{T_s} - \left\langle v_{C2}(t)\right\rangle_{Ts}\right) \tag{4.11}$$

$$\left\langle i_2(t)\right\rangle_{T_s} = d'(t)\left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{Ts}\right) \tag{4.12}$$

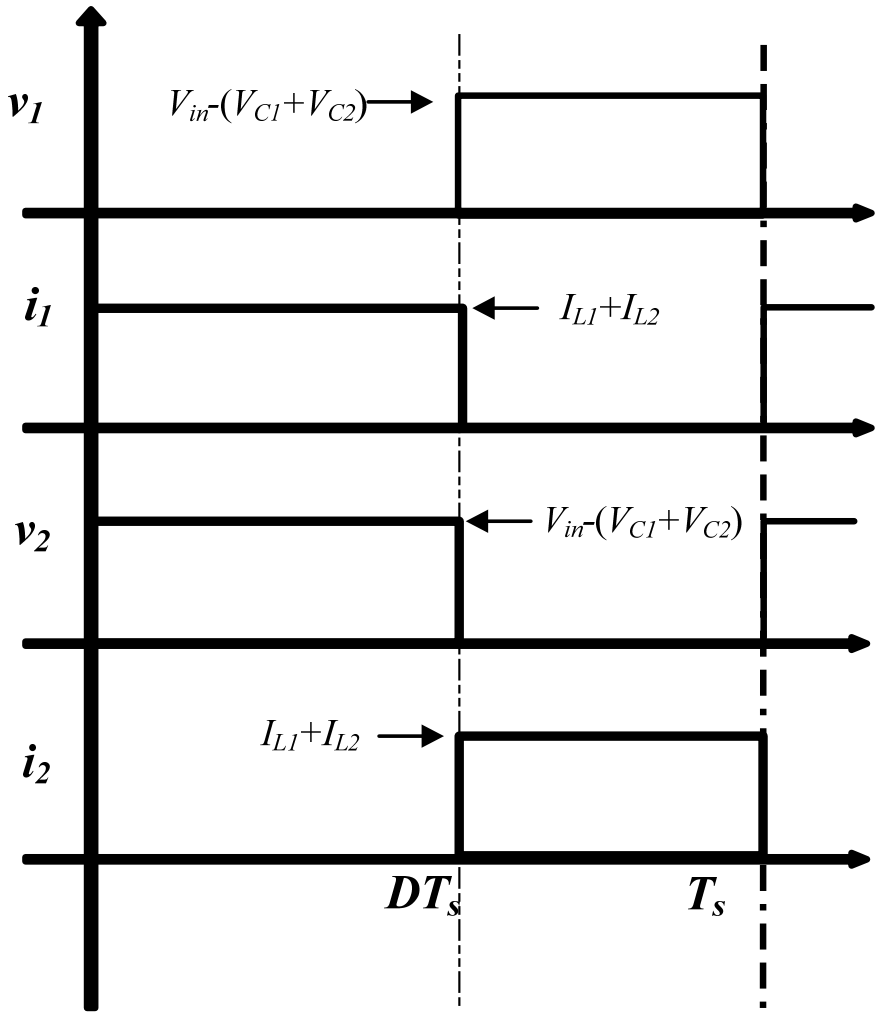


Figure 4.5: Voltage and current waveform at each switching port

Since $i_1(t)$ and $v_2(t)$ are chosen as independent inputs, the other parameters, $v_1(t)$ and $i_2(t)$, should be expressed as dependent sources. By some simple algebra steps, the relationship can be found to be

$$\langle v_1(t)\rangle_{T_s} = \frac{d'(t)}{d(t)}\langle v_2(t)\rangle_{T_s} \tag{4.13}$$

$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{d'(t)}{d(t)}\left\langle i_1(t)\right\rangle_{T_s} \tag{4.14}$$

The averaged switch network circuit diagram is shown in Fig. 4.6, which is based on Eq. (4.13) and (4.14). However, even though this circuit only includes the averaged components, that is, this model excludes the switching frequency harmonics, the circuit still has nonlinear components since there are products of time varying components: $d(t)\cdot v_2(t)$ and $d(t)\cdot i_1(t)$.

The averaged switch model can be linearized by perturbing and neglecting the products of perturbations. To linearize, assume that:

$$\|V_1\| \gg \|\hat{v}_1\| \tag{4.15}$$

$$\|I_1\| \gg \|\hat{i}_1\| \tag{4.16}$$

$$\|V_2\| \gg \|\hat{v}_2\| \tag{4.17}$$

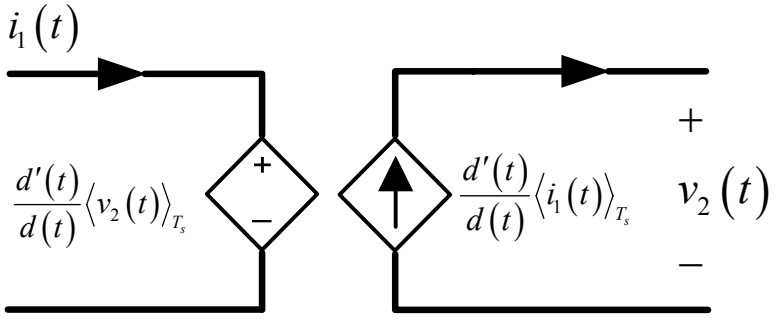


Figure 4.6: Averaged switch network model of a MIMIWJC with dependent sources

$$\|I_2\| \gg \|\hat{i}_2\| \tag{4.18}$$

$$\|D\| \gg \|\hat{d}\| \tag{4.19}$$

First, perturb all the signals about the nominal operating points. The perturbed signals are

$$\langle v_1(t)\rangle_{T_s} = V_1 + \hat{v}_1(t) \tag{4.20}$$

$$\langle i_1(t)\rangle_{T_s} = I_1 + \hat{i}_1(t) \tag{4.21}$$

$$\langle v_2(t)\rangle_{T_s} = V_2 + \hat{v}_2(t) \tag{4.22}$$

$$\langle i_2(t)\rangle_{T_s} = I_2 + \hat{i}_2(t) \tag{4.23}$$

$$d(t) = D + \hat{d}(t) \tag{4.24}$$

By substituting from Eq.(4.20) and (4.24) into Eq. (4.13) and (4.14), Eqs. (4.25) and (4.26) are

$$V_1 + \hat{v}_1(t) = \frac{D' - \hat{d}(t)}{D + \hat{d}(t)}\left(V_2 + \hat{v}_2(t)\right) \tag{4.25}$$

$$I_2 + \hat{i}_2(t) = \frac{D' - \hat{d}(t)}{D + \hat{d}(t)}\left(I_1 + \hat{i}_1(t)\right) \tag{4.26}$$

These two equations can be divided in two parts; one is a dc term and the other part is an ac term. Since both the left hand side and right hand side of the dc quantities should be the same, one can extract the dc term equation, and these dc equations are

$$V_1 = \frac{D'}{D} V_2 \tag{4.27}$$

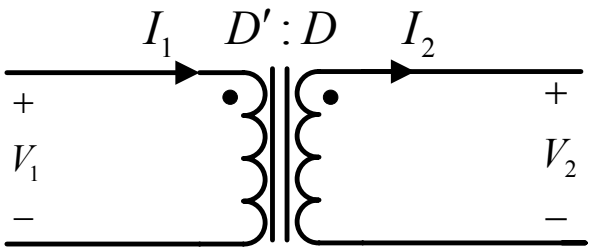


Figure 4.7: Averaged dc switch network model of a MIMIWJC

$$I_2 = \frac{D'}{D} I_1 \tag{4.28}$$

The dc model of the switch is represented in Fig. 4.7. Also, the ac terms can be divided into two parts; one is first order ac terms and the others are second order terms. However, the second order terms, i.e., the product of perturbed variations, can be neglected by the assumptions which are shown in Equations (4.15) to (4.19). Thus, the linearized switch network equations are

$$V_1 + \hat{v}_1(t) = \frac{D'}{D}\left(V_2 + \hat{v}_2(t)\right) - \frac{V_1}{DD'} \tag{4.29}$$

$$I_2 + \hat{i}_2(t) = \frac{D'}{D}\left(I_1 + \hat{i}_1(t)\right) - \hat{d}(t)\frac{I_2}{DD'} \tag{4.30}$$

Equations (4.29) and (4.30) can be expressed as the combination of dependent voltage and current source with the connection of an ideal transformer. Figure 4.8 shows the linearized averaged switch network model of the modified inverse Watkins-Johnson converter. The linearized and averaged circuit model can be found by simply plugging in

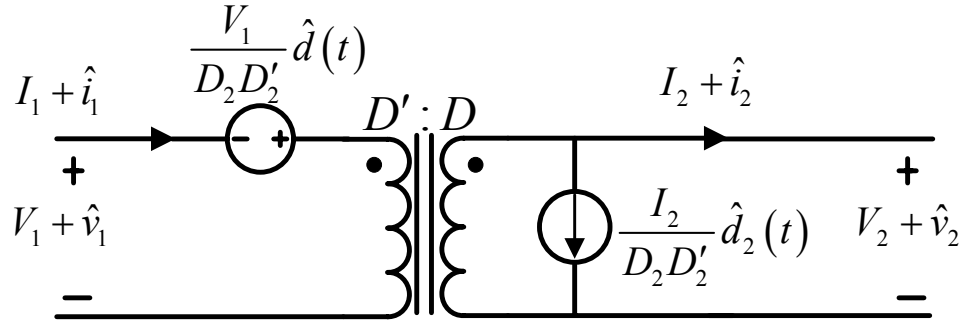
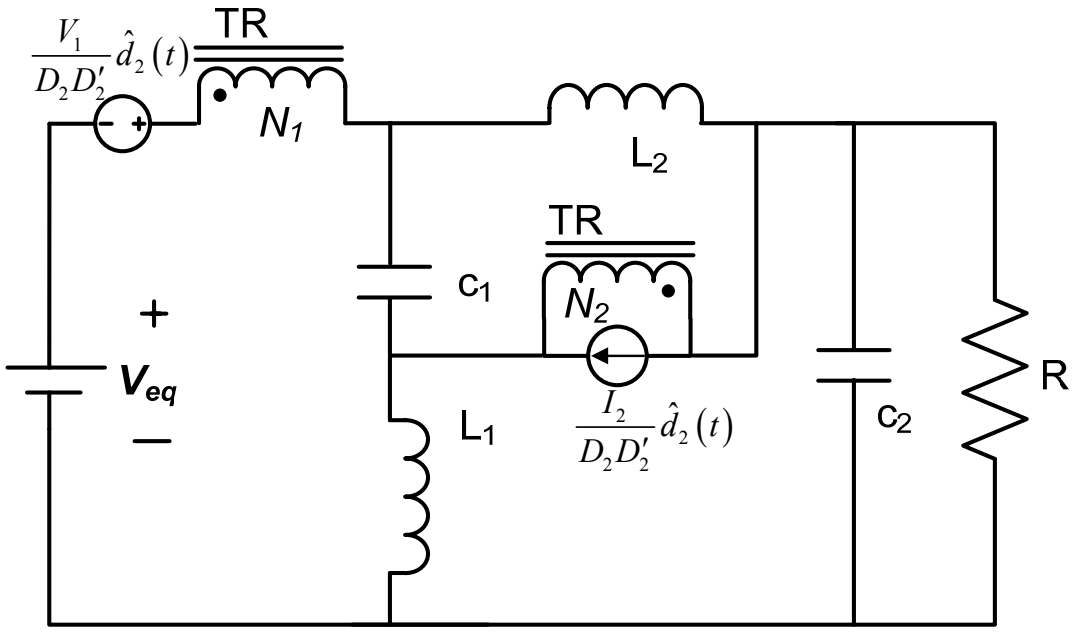


Figure 4.8: Averaged and linearized switch network model of a MIWJC



$N_1:N_2 = D':D$

Figure 4.9: Averaged and linearized circuit model of a MIWJC

the averaged and linearized switch network to the original circuit. The completed linearized switching model of a IWJC is shown in Fig. 4.9

4.5 TRANSFER FUNCTION USING MIDDLEBROOK'S EXTRA ELEMENT THEOREM

In this section, converter transfer functions are presented using Middlebrook's Extra Element Theorem (EET) [33, 40-42]. The circuit analysis by EET enables one to use fewer algebra steps. In this section, a brief description of the EET is introduced, and more detailed explanation is presented in Appendix A.

First, since a multiple input converter has more than one FCBB switch, it is necessary to define the variations of duty ratios. In this section, we will observe how the output voltage is varied by the sum of each duty ratio. For the two input converter, $\hat{d}_2$(t) is the variation parameter to observe the output voltage variation. The duty ratio can be expressed by

$$d_1(t) = D_1 + \hat{d}_1 \tag{4.31}$$

$$d_{2e}(t) = D_{2e} + \hat{d}_{2e} \tag{4.32}$$

$$\begin{aligned} d_2(t) &= D_1 + D_{2e} + \hat{d}_1 + \hat{d}_{2e} = D_2 + \hat{d}_2 \\ d_2' &= 1 - d_2(t) \end{aligned} \tag{4.33}$$

The basic idea of the EET is to find how the extra element can affect the original circuit's transfer functions. There are two typical forms of EET expressions, as shown in Eq. (4.34) and (4.35).

$$G_{new} = \left(G_{old}\big|_{Z\to\infty} \right) \left(\frac{1+\frac{Z_N}{Z}}{1+\frac{Z_D}{Z}} \right) \tag{4.34}$$

$$G_{new} = \left(G_{old}\big|_{Z\to 0} \right) \left(\frac{1+\frac{Z}{Z_N}}{1+\frac{Z}{Z_D}} \right) \tag{4.35}$$

where Z is the extra element impedance. The parameters in Eq. (4.34) and (4.35) are explained in this section with an example based on the MIMIWJC. Equation (4.34) can be used when the additional element, Z, is added where the original port is open circuited, and Eq. (4.35) can be useful when the extra element is inserted where the original port is shorted.

To find the control to output transfer function, G_{vd}, using EET, one should choose the extra element in the circuit. In Fig. 4.10, C_1 is chosen as an extra element theorem because the existence of C_1 is the most significant difference between a modified IWJC and a conventional unmodified IWJC. The control to the output transfer function can be found by setting the input voltage variation to zero as shown in Eq. (4.36).

$$G_{vd}(s) = \left. \frac{\hat{v}_{out}(s)}{\hat{d}_2(s)} \right|_{\hat{v}_{in}=0} \tag{4.36}$$

The small signal equivalent circuit for finding $G_{vd}(\underline{s})$ is shown in Fig. 4.10. The final EET form of the open loop control-to-output transfer function of the MIMIWJC in the *s*-domain is

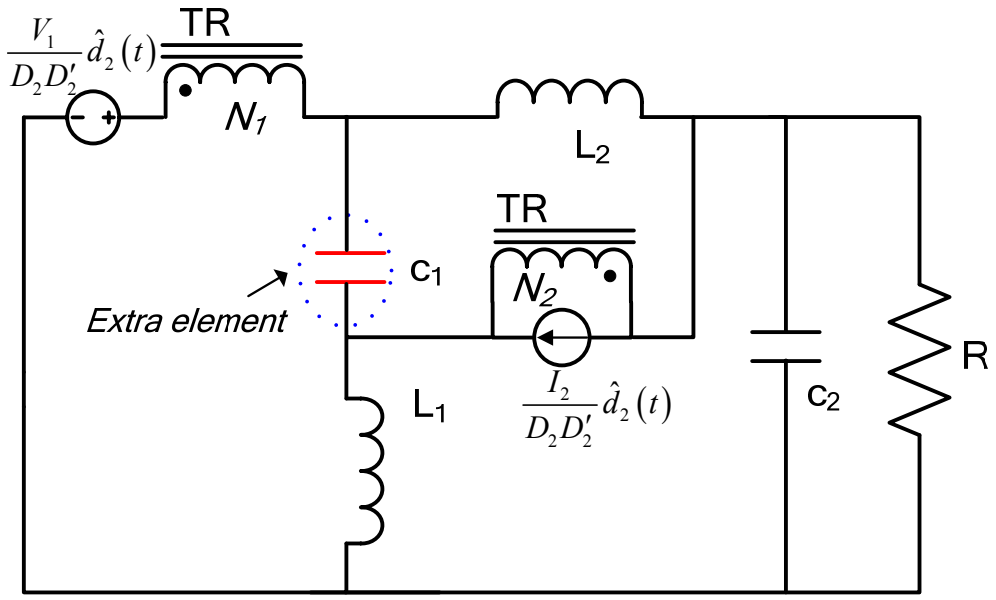


Figure 4.10: Averaged small signal model of MIMIWJC with $\hat{v}_{in} = 0$.

$$G_{vd}(s) = G_{vd\,old}\frac{1+\frac{Z_N(s)}{Z(s)}}{1+\frac{Z_D(s)}{Z(s)}} \tag{4.37}$$

The transfer function, G_{vd_old}, can be derived by eliminating C_1, i.e., the open-circuit, as shown in Fig. 4.11. By using some simple circuit analysis techniques, such as Kirchoff's laws, and algebraic operations, G_{vd_old} is derived as

$$G_{vd\,old}(s) = M\frac{1-\frac{s}{\omega_{Z1}}}{1+\frac{s}{Q_1\omega_1}+\left(\frac{s}{\omega_1}\right)^2} \tag{4.38}$$

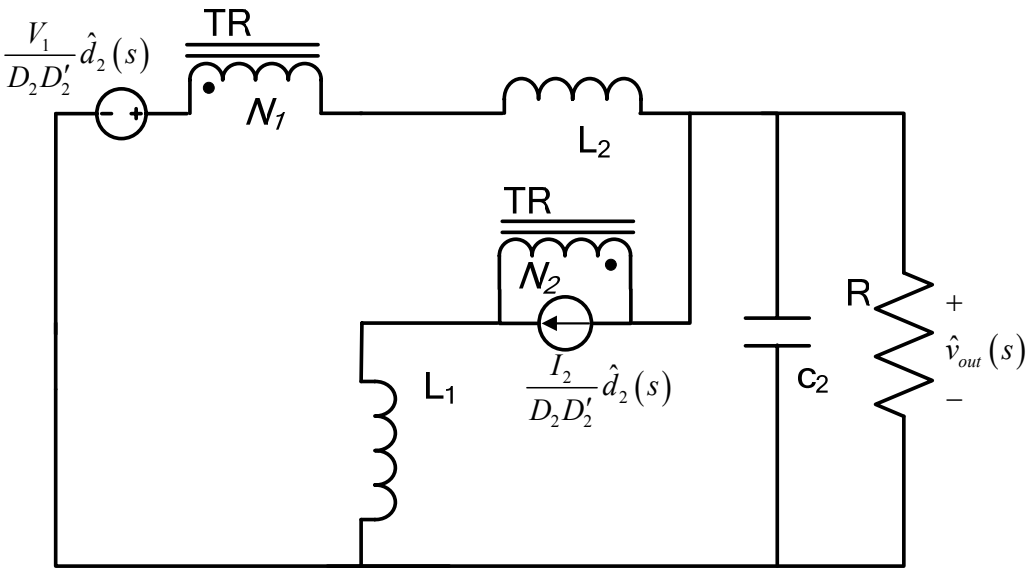


Figure 4.11: Equivalent circuit to find G_{vd_old} .

Equation(4.38) is expressed as a normalized rational pole zero form. The parameters are composed of dc gain, M, quality factor, Q_1, and angular frequencies, ω_{z1} and ω_1 which are shown as follows.

$$M = -\frac{D_2}{1-2D_2} \tag{4.39}$$

$$Q_1 = (1-2D_2)R\sqrt{\frac{C_2}{L_{eq1}}} \tag{4.40}$$

$$\omega_{Z1} = -\frac{1-2D_2}{M}\frac{R}{L_{eq1}} \tag{4.41}$$

$$\omega_1 = (1-2D_2)\frac{1}{\sqrt{L_{eq1}C_2}} \tag{4.42}$$

where, $L_{eq1} = D_2'L_1 + D_2L_2$

The impedance $Z_D(s)$ in the denominator part of Eq. (4.37) can be defined as a driving point impedance where C_1 is originally located. To find the driving point impedance, $Z_D(s)$, the independent current source can be used as a test signal, as shown in Fig. 4.12. The normalized rational form of $Z_D(s)$ is

$$Z_D(s) = \frac{v(s)}{i(s)} = \frac{D_2^2 L_1 + D_2'^2 L}{1-2D_2} s \frac{1 + \frac{s}{Q_2 \omega_{Z2}} + \left(\frac{s}{\omega_{z2}}\right)^2}{1 + \frac{s}{Q_3 \omega_2} + \left(\frac{s}{\omega_2}\right)^2} \tag{4.43}$$

The related parameters of Eq. (4.43) are as follows:

$$\omega_{Z2} = \frac{D_2 D_2'}{\sqrt{L_{eq2} C_2}} \tag{4.44}$$

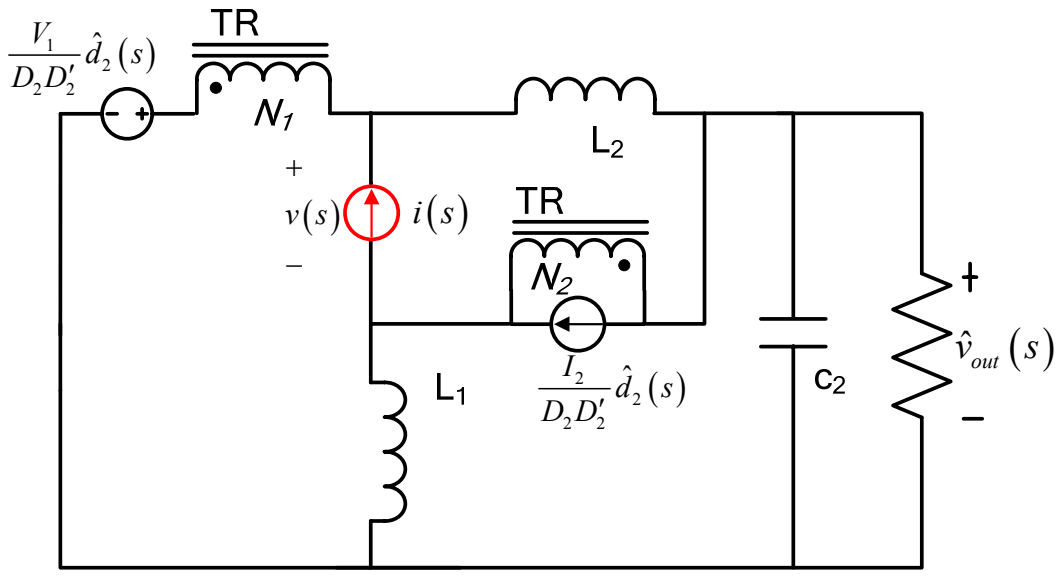


Figure 4.12: Measurement of the driving point impedance, Z_D.

$$\omega_2 = \frac{1-2D_2}{\sqrt{L_{eq3}C_2}} \tag{4.45}$$

$$Q_2 = D_2 D_2' \sqrt{\frac{C_2}{L_{eq2}}} \tag{4.46}$$

$$Q_3 = (1-2D_2) R \sqrt{\frac{C_2}{L_{eq3}}} \tag{4.47}$$

where, $L_{eq2} = D_2^2 L_1 \| D_2' L_2$ and $L_{eq3} = D_2 D' L_1 + D_2^2 L_2$ The impedance, $Z_N(S)$, can be defined by the driving point impedance where C_1 is located under the output voltage is in null condition. The null condition does not mean just a short circuit but a special condition that can make the output voltage go to zero under the special condition of $i(s)$. Figure (4.13) shows the circuit that can be used to measure the impedance, $Z_N(s)$.

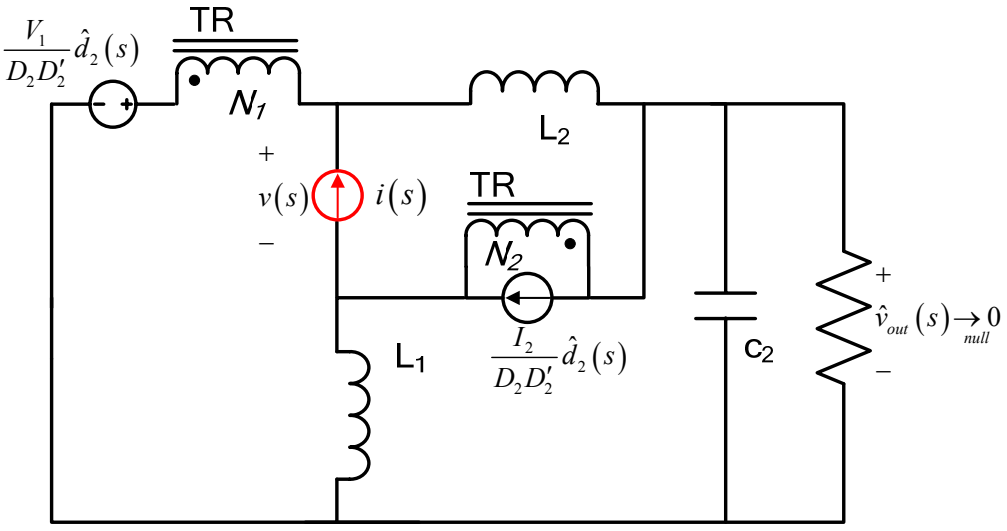


Figure 4.13: Measurement of the driving point impedance, Z_N. Note that the output voltage is nullified.

The normalized pole zero form of the impedance, $Z_N(s)$ is

$$Z_N(s) = \left.\frac{v(s)}{i(s)}\right|_{\substack{v_{out} \to 0 \\ null}} = \frac{L_{eq4}}{1-2D_2} s \frac{1-\frac{s}{\omega_{z3}}}{1-\frac{s}{\omega_3}} \tag{4.48}$$

The angular frequencies of $Z_N(s)$, which are expressed in terms of circuit parameters is

$$\omega_{z3} = -\frac{1}{M}\frac{L_{eq4}R}{L_1 L_2} \tag{4.49}$$

$$\omega_3 = \frac{1-2D_2}{M}\frac{R}{L_{eq1}} \tag{4.50}$$

where, $L_{eq4} = D_2 L_1 + D_2' L_2$

Now we have obtained all the components of Eq. (4.37) except the extra element impedance, Z(s). The extra element impedance, Z_{C1}, is

$$Z(s) = \frac{1}{sC_1} \tag{4.51}$$

Thus, the finalized form of the open loop control to output transfer function of the MIMIWJC, $G_{vd}(s)$, is

$$G_{vd}(s) = M \frac{1-\frac{s}{\omega_{Z1}}}{1+\frac{s}{Q_1\omega_1}+\left(\frac{s}{\omega_1}\right)^2} \frac{\frac{L_{eq4}}{1-2D_2} s \frac{1-\frac{s}{\omega_{z3}}}{1-\frac{s}{\omega_3}}}{1+\frac{1}{sC_1}} \Bigg/ \frac{\frac{D_2^2 L_1 + D_2'^2 L}{1-2D_2} s \frac{1+\frac{s}{Q_2\omega_{Z2}}+\left(\frac{s}{\omega_{z2}}\right)^2}{1+\frac{s}{Q_3\omega_2}+\left(\frac{s}{\omega_2}\right)^2}}{1+\frac{1}{sC_1}} \tag{4.52}$$

By plugging in the numerical values of Table 4.1 into Eq. (4.52), the Bode plot can be made as shown in Fig. 4.14.

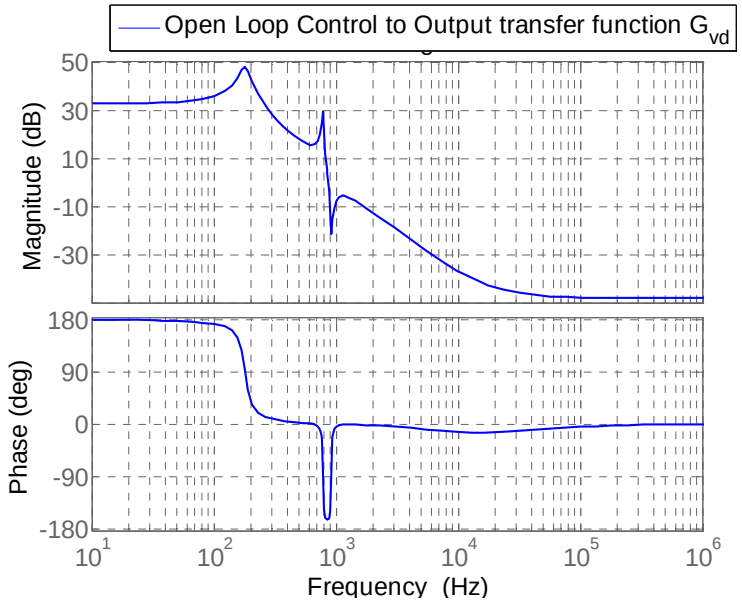


Figure 4.14: Control to output voltage transfer function, G_{vd}, bode diagram

System Parameters	Value	Unit
L_1	300	μH
L_2	300	μH
C_1	100	μF
C_2	1500	μF
R	20	Ω
V_{IN1}	15	V
V_{IN2}	8	V
D_1	0.1	None
D_2	0.35	None

Table 4.1: System parameters and components values for Fig. 4.13

4.6 OPERATION STRATEGIES OF THE MIMIWJC

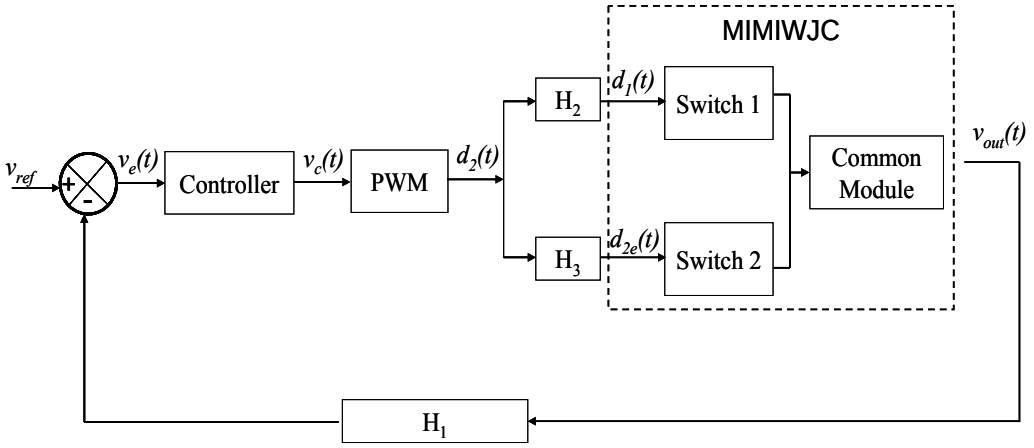
There could be several strategies for operating MICs for their own application purposes. In this section, two possible operation methods are introduced. Both of the two methods can maintain a constant output voltage, and they use only one compensator. The first method is using both duty ratios, $d_1(t)$ and $d_2(t)$ to regulate the output voltage, as shown in Fig. 4.15 (a). Power demand for each input power source is divided by certain constant ratios through the H_2 and H_3 block in Fig. 4.15 (a). Since the flat topped value of each input current can be assumed to have the same value as the sum of the two inductor currents that are shown in Eq. (4.53), the ratio for the drained power from each source can be determined by the ratio of the constant gains, H_2 and H_3.

$$I_{in1} = I_{in2} = I_{L1} + I_{L2} \tag{4.53}$$

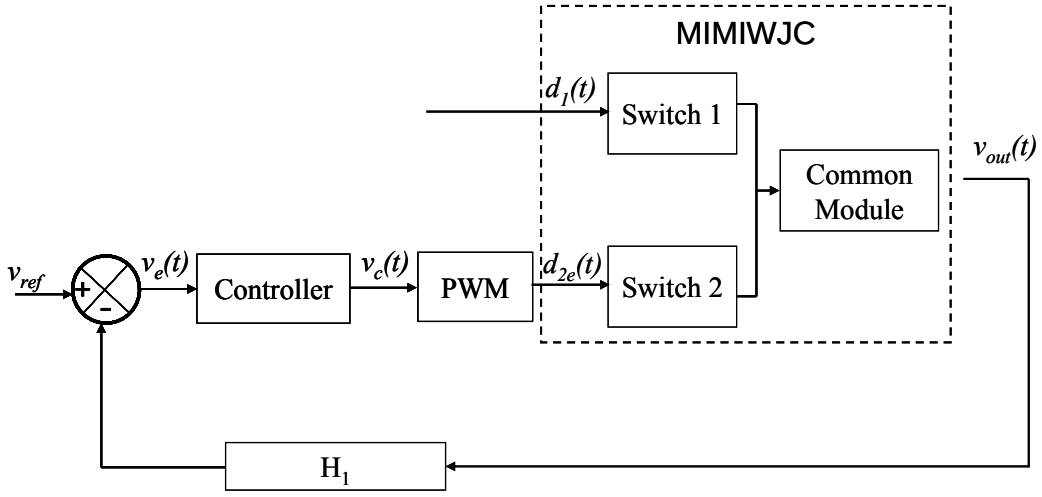
As a demonstrative strategy, if two input sources need to draw power equally, then H_2 and H_3 should be

$$\frac{H_2}{H_3} = \frac{V_2}{V_1} \tag{4.54}$$

The block diagram of second proposed operation method is described in Fig 4.14 (b). In this operation mode, one duty ratio is decided by the power regulation and the other duty ratio contributes to the output voltage regulation. In a situation where power is drained from both sources, the second source deals which abrupt load changes.



(a)



(b)

Figure 4.15: Suggested operation strategies: (a) both duty ratios contribute to regulate the output voltage (b) one duty ratio is decided by the power and the other duty ratio is decided by output voltage regulation.

4.7 CONCLUSIONS

The two small signal modeling techniques for a dc-dc converter, state-space averaging modeling and averaged circuit modeling, have been introduced. The ac dynamic modeling methods for the proposed converter are explained. The equivalent source concept of MICs can make the analysis as simple as a single input dc-dc converter. The proposed equivalent source representation can be applied to all MICs so that the converter circuit analysis can be the same as a single input dc-dc converter. By using Middlebrook's EET, the proposed converter transfer function is derived in terms of circuit parameters, and its Bode plot is shown. To regulate the output voltage of a MIC, two possible operational strategies are proposed in this chapter; the first method is that both duty ratios can contribute to the output voltage regulation, and the other method is that one duty ratio is determined by the power regulation, and the other duty ratio is determined by the output voltage regulation. These proposed control methods are proven by simulation and experiments in Chapter 5.

Chapter 5: Simulations and Experimental Results

In this chapter, the proposed converter analysis and suggested control methods which have been done in the previous chapters are verified with simulations using MATLAB/Simulink and PSIM and experimental works with a prototype hardware. The simulated and experimental works have been done with both open-loop and closed-loop analyses of the proposed MIMIWJC. To simplify the prototype, a two input MIMIWJC is used for this chapter, and the circuit schematic is shown in Fig. 5.1.

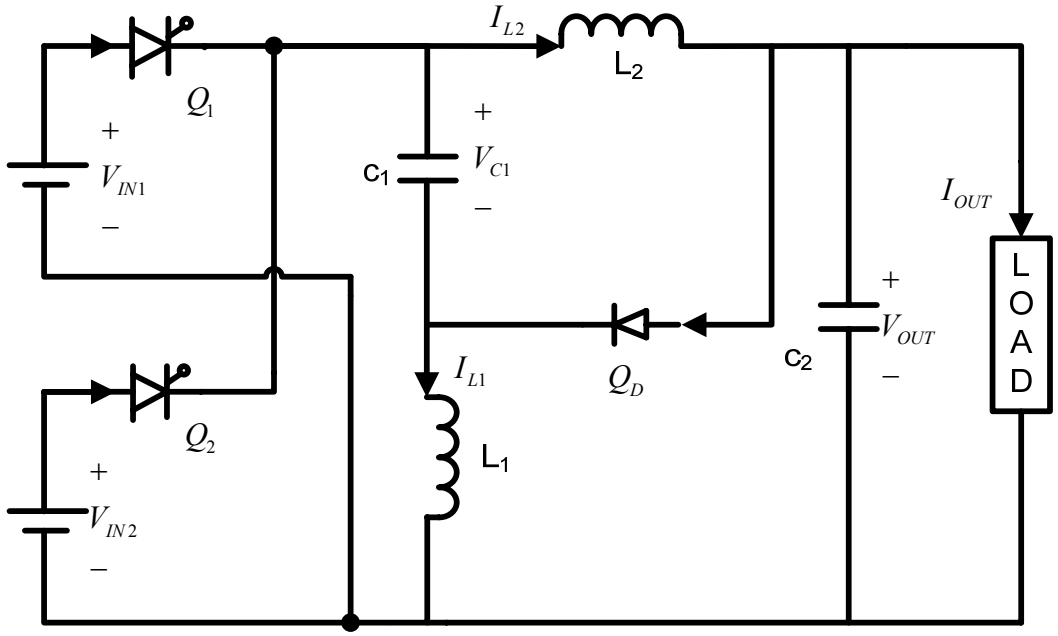


Figure 5.1: Proposed two input modified inverse Watkins-Johnson converter circuit diagram

5.1 OPEN-LOOP SIMULATION

In this section, the open-loop two-input MIMIWJC simulation results are shown to verify the analysis and aid understanding of the fundamental circuit behavior characteristics in CCM. These simulation results can prove the analysis results shown Chapter 3 in this dissertation. Table 5.1 indicates the parameters used for the open-loop

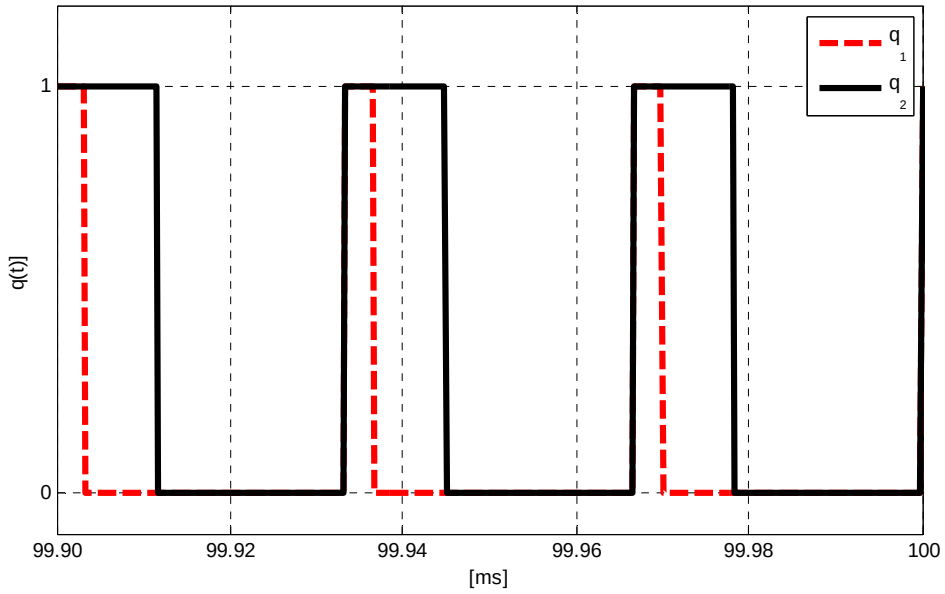
System Parameters	Value	Unit
L_1	300	μH
L_2	300	μH
C_1	600	μF
C_2	600	μF
R	10	Ω
V_{IN1}	15	V
V_{IN2}	8	V
D_1	0.1	None
D_2	0.35	None
fs	20	kHz

Table 5.1: System parameters and components values for the open-loop simulation

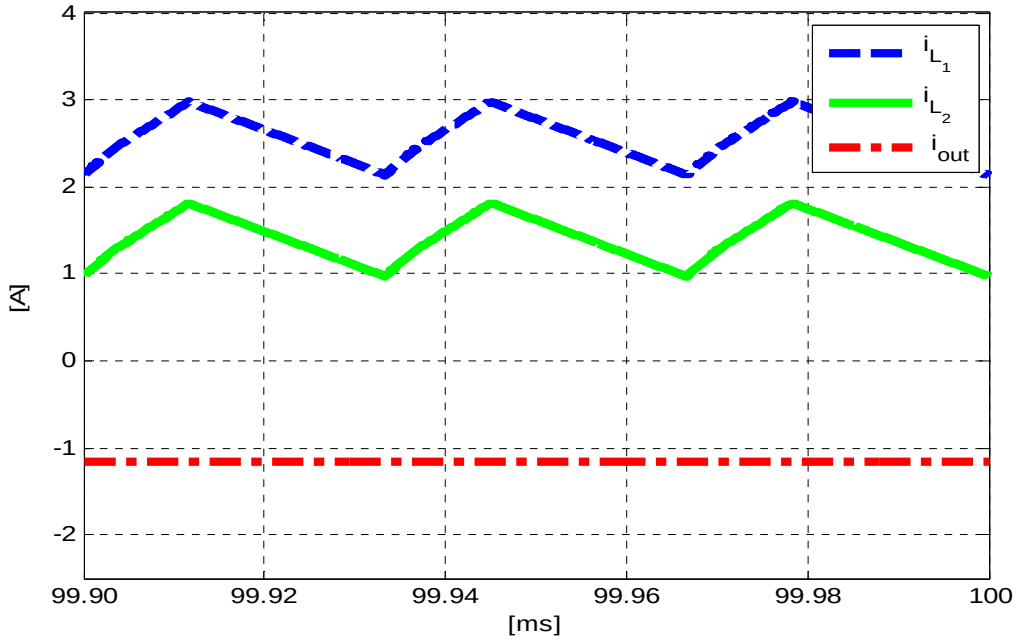
simulation. The same inductances and capacitances are used for this simulation as were assumed in Section 3.4.

First, the switching commands and inductor current and output load current waveforms are shown in Fig. 5.2. The two inductor current relationships as indicated in (3.28), can be verified because the all the current values are well matched with the analyzed results in Chapter 3. Since the two inductor values are the same, the current shapes are exactly the same, except for their average values. The average inductor current magnitudes are determined by Eq. (3.25) and the simulation results can show the relationship which is shown in Fig. 5.2 (b).

The two capacitor voltages are shown in Fig. 5.3. As it is indicated in Table 5.1, the same capacitances are used for open-loop simulation in this section. As discussed in Chapter 3, (3.32) and (3.35), the two capacitor voltages, v_{c1} and $v_{c2,}$ should always be the same, and Figures 5.3 (a) and (b) show the same waveforms as expected. The input to output relationship that is shown in Eq. (3.28) can also be verified with Fig.5.3. Although the input voltage sources are changed from V_{IN1} to V_{IN2}, during the charging periods Mode I and Mode II, the capacitor voltage waveform slopes are not changed since the charging current is the same as I_{L1}.

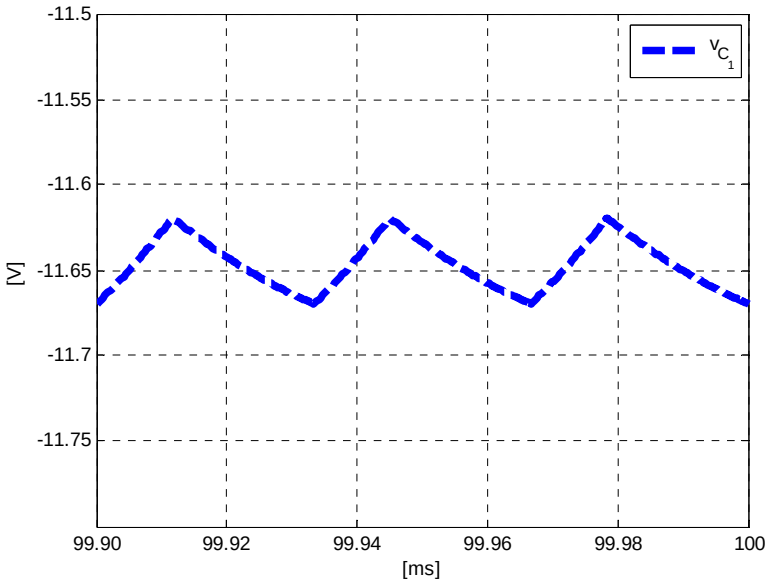


(a)

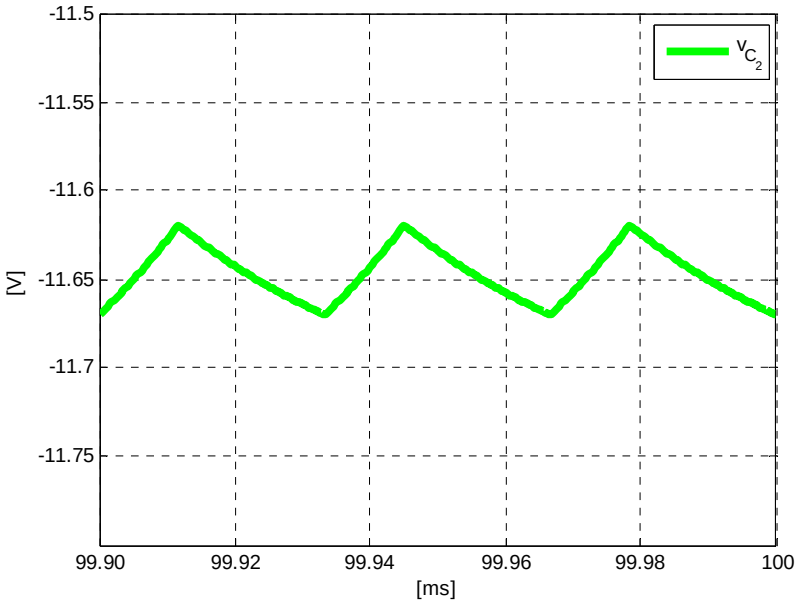


(b)

Figure 5.2: The inductor currents and output current waveforms by switching commands: (a) switching function q_1 and q_2 (b) inductor currents i_{L1} and i_{L2} and output current i_{out}.



(a)



(b)

Figure 5.3:The capacitor voltage waveforms: (a) voltage across the C_1,$v_{c1,}$ (b) voltage across the C_2,v_{c2}

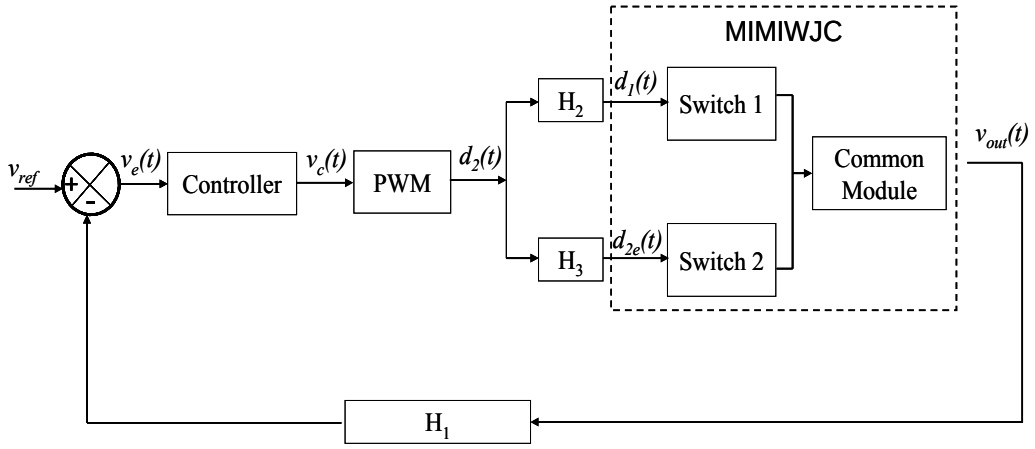
5.2 CLOSED-LOOP SIMULATION

The two-input MIMWJC closed-loop behavior characteristics are simulated using PSIM. For the closed-loop simulation, the circuit parameters and component values are indicated in Table 5.2. As shown in Fig. 5.4, both control methods are verified through simulation. The proportional and integral (PI) controller is used as a controller in Fig. 5.4.

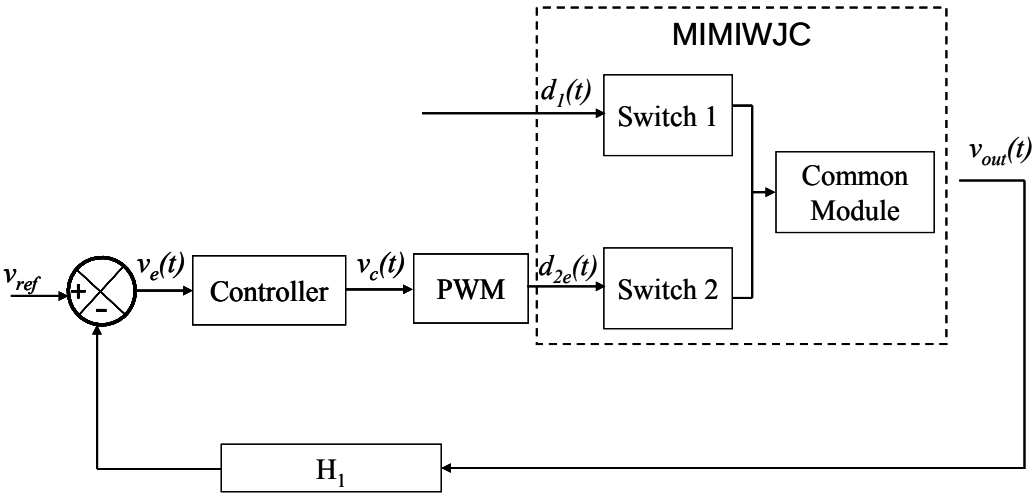
The first control method which is indicated in Fig. 5.4 (a) is simulated with the parameters H_1=-1, H_2=0.4,and H_3=0, and the PI controller has k_p= 0.05 and k_i= 0.83. Figure 5.5 shows the simulation results when the load is changed from 10 Ω to 5 Ω at 0.7 seconds. The simulation confirms that the output voltage is regulated to the desired goal.

System Parameters	Value	Unit
L_1	300	μH
L_2	300	μH
C_1	100	μF
C_2	1500	μF
R	10	Ω
V_{IN1}	15	V
V_{IN2}	8	V
V_{ref}	-5	V
f_s	25	kHz

Table 5.2: System parameters and components values for the close-loop simulation



(a)



(b)

Figure 5.4: Proposed MIC operation strategies: (a) both duty ratio contribute to regulate the output voltage (b) one duty ratio is decided by the power and the other duty ratio is decided by output voltage regulation.

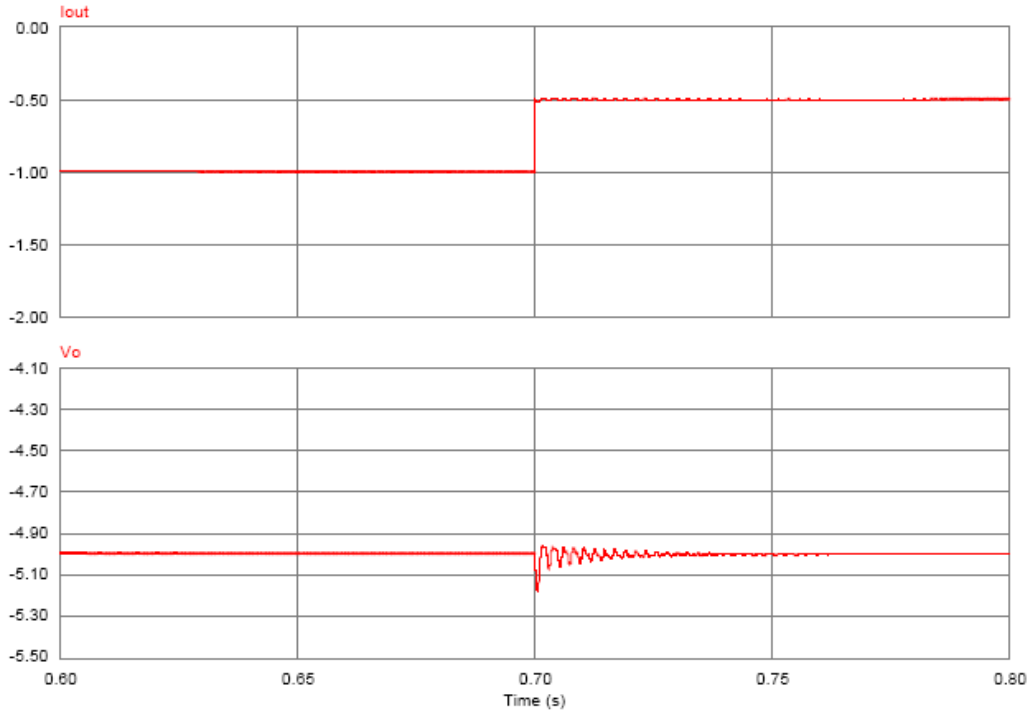


Figure 5.5: Simulation results showing the transient when the load is changed from 1A to 0.5A at t=0.7 sec.

The second proposed control method that is shown in Fig. 5.4 (b) is also verified with a simulation. For this simulation, a PI controller with gains k_p=0.08 and k_i=0.008 is used to regulate the output voltage and H_1 is set to -1. Since only one switch signal, q_2, is connected with the feedback loop, the other duty ratio should be fixed to the constant, and 0.1 is used for D_1 for this simulation. Figure 5.5 shows the simulation results when the load is changed from 2 A to 4 A at 1.2 sec. The simulation confirms that the output voltage is regulated to the desired goal.

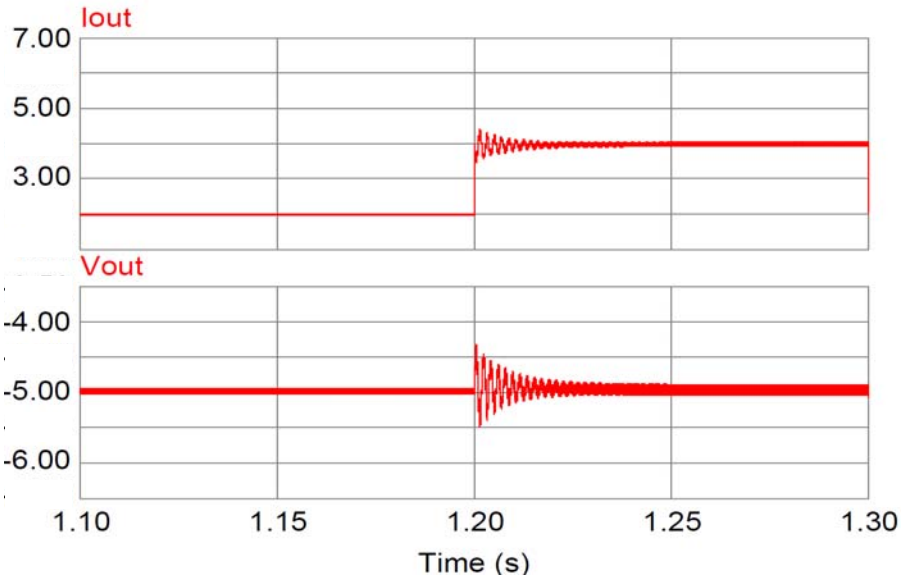


Figure 5.6: Simulation results showing the transient when the load is changed from 2A to 4A.

5.3 EXPERIMENTAL RESULTS

A hardware prototype was built to verify the operational analysis and control methods. The same system parameters are used as in Table 5.2. The FCBB switches used in the experiments are realized by the series combination of IRFP140A MOSFET and S60SC6M diode. The same S60SC6M is used for the diode Q_D in Fig. 5.1. Figure 5.7 shows the calculated and measured open-loop output voltage with a fixed duty ratio D_2 at 0.35 and varying D_1. Differences between the calculated value and the measured value were most likely caused by semiconductor switch losses, which were used to calculate the theoretical trace of V_{OUT} in Fig. 5.6.

Figure 5.8 shows the experimentally obtained inductor and output current waveforms. Since L_1 and L_2 are the same and the output capacitor is large enough to

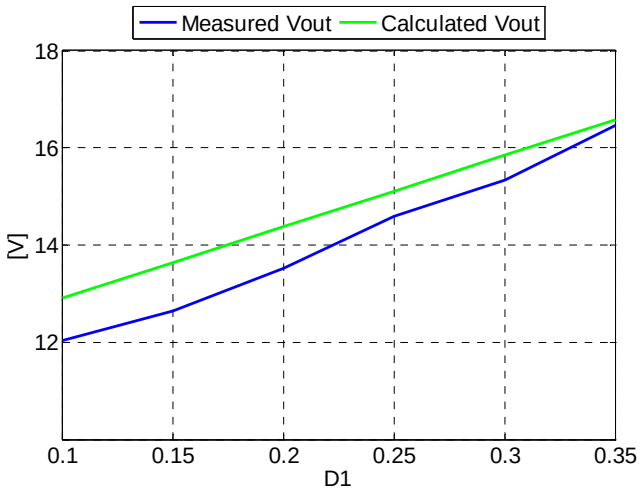


Figure 5.7: Output voltage, V_{out}, with D_1 varies at $D_2 = 0.35$

ignore the output current ripple, the instantaneous output current i_{out} equals the difference between the two inductor currents i_{L2} and i_{L1}. As expected, the waveforms are similar to those observed in Fig. 5.2.

The first control operation strategy, Control Method 1, which is shown in Fig. 5.4 (a), is verified with the experimental works and the oscilloscope traces are shown in Fig. 5.9-5.11. Figures 5.9 and 5.10 show the output voltage regulation for the input voltage changes. Figure 5.9 shows the output voltage regulation case when the input voltage V_{IN1} is changed from 18 V to 12 V while the V_{IN2} remains at 12V. Figure 5.10 shows the output voltage traces when V_{IN2} is changed from 15 V to 10 V while the V_{IN1} remains at 18V. For the load change case, Fig. 5.11 can verify the regulated output voltage when load current is changed 500 mA to 1A.

The first control operation strategy, Control Method 1, which is shown in Fig. 5.4 (a), is verified with the experimental works and the oscilloscope traces are shown in Fig.

5.9-5.11. Figures 5.9 and 5.10 show the output voltage regulation for the input voltage changes. Figure 5.9 shows the output voltage regulation case when the input voltage V_{IN1} is changed from 18 V to 12 V while the V_{IN2} remains at 12V. Figure 5.10 shows the output voltage traces when V_{IN2} is changed from 15 V to 10 V while the V_{IN1} remains at 18V. For the load change case, Fig. 5.11 can verify the regulated output voltage when load current is changed 500 mA to 1A.

The second operation strategy, Control Method 2, which is shown in Fig. 5.4 (b), is verified through experiments with input voltage changes and output load changes, and the captured oscilloscope figures are shown in Figures 5.12-5.14. Figures 5.12 and 5.13 show the oscilloscope traces which display the output voltage regulation. Figure 5.12 shows the results when the V_{IN1} is changed from 18 V to 12 V, and Fig. 5.13 shows the results when V_{IN2} is changed from 15 to 10V, respectively. Figure 5.14 shows the voltage regulation when the load current varies from 2 A to 4 A.

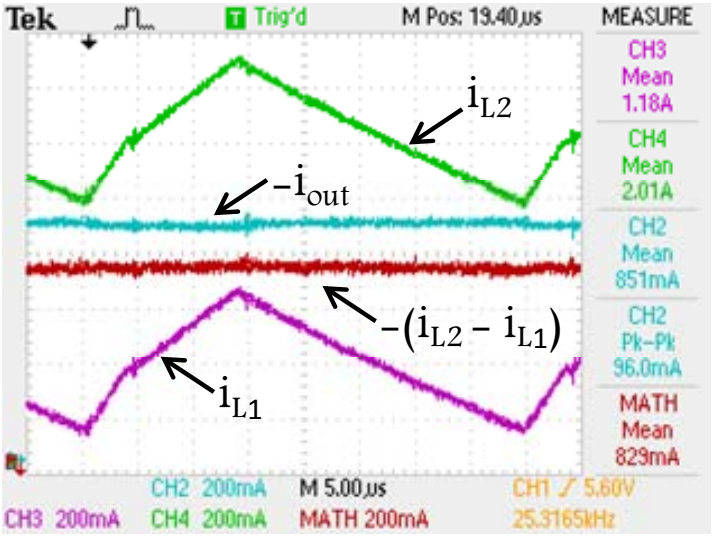


Figure 5.8: Experimentally obtained inductor and load current.

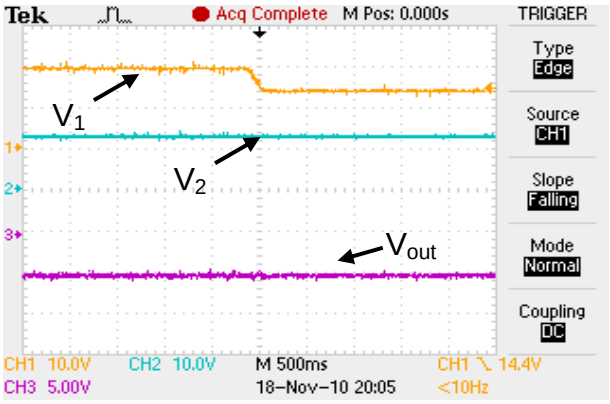


Figure 5.9: Voltage Regulation Method I when input source voltage V_1 changed from 18V to 12V while V_2 stays at 12V.

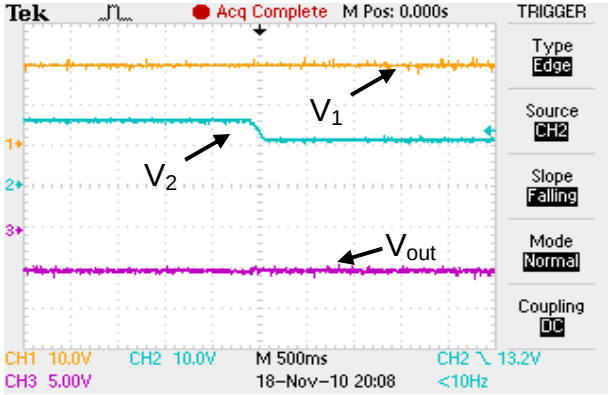


Figure 5.10: Voltage Regulation Method I when input source voltage V_2 changed from 15V to 10V while V_1 stays at 18V.

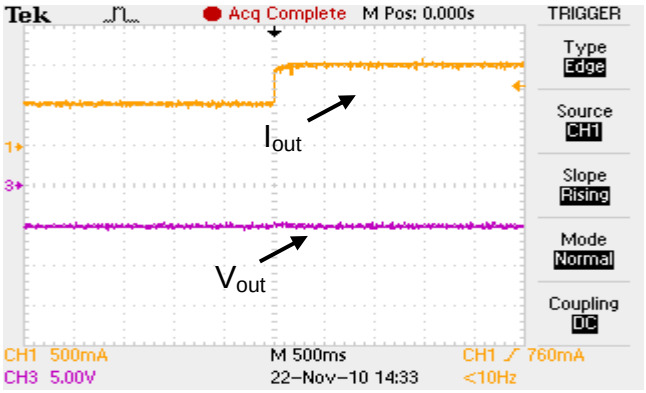


Figure 5.11: Voltage Regulation Method I when load current varies 500mA to 1A.

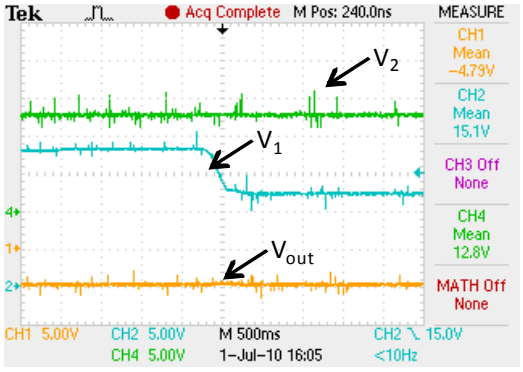


Figure 5.12: Voltage Regulation Method II when input source voltage V_1 changed from 18V to 12V while V_2 stays at 12V.

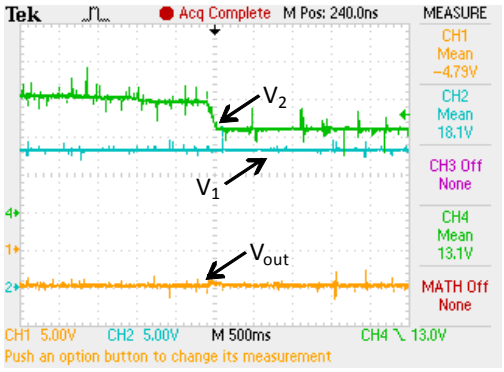


Figure 5.13: Voltage Regulation Method II when input source voltage V_2 changed from 15V to 10V while V_1 stays at 18V.

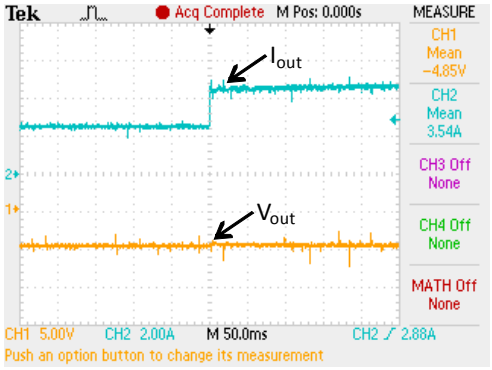


Figure 5.14: Voltage Regulation Method II when load current varies 2A to 4A.

5.4 CONCLUSION

This chapter showed simulation and experimental results to verify the analytical results which were shown in Chapters 3 and 4. The fundamental operational principles of the two input MIMIWJC are verified with the open-loop simulation with MATLAB/Simulink and PSIM and experimental results with prototype hardware. The error between the experiments and theoretical values mostly come from the non-ideal components. The two proposed control methods that were shown in Chapter 4 are verified with the PSIM simulation and experimental works with PI controllers. Both control methods can regulate the output voltage, but when both duty ratios contribute to regulate the output voltage, the voltage can be more tightly regulated. The maximum efficiency is 76% and the minimum is 55%. .Even though the efficiency of the proposed converter is not the main issue of this research, its efficiency could be increased in the future. To increase the efficiency, other switching schemes might be used for the MIC, such as the phase shift switching strategy. Since the FCBB switches are not ideal, there are some overlap periods while one switch is turning-off and the other switch is turning on. If the phase switching command is used then the switching transient loss which caused from the overlap switching commands can be reduced. Moreover, efficiency can be improved by reducing voltage overshoots and losses and/or employing efficiency oriented design using snubbers and selecting low loss components.

Chapter 6: Conclusion

These works have presented the multiple input dc-dc converter (MIC) topology evaluation and development. The MIC converter evaluation criteria and results are shown, and a new topology, a multiple input modified inverse Watkins-Johnson converter is proposed. The fundamental analysis and operational strategies are explained.

The four MIC topology comparison criteria, --expected cost, modularity potential, reliability and flexibility-- are described, which can be used to choose one particular MIC topology based on a given situation or application. Ten MIC topologies, including a proposed MIMIWJC are evaluated according to these four criteria. The comparison results are shown in a table form. Also, the use of the comparison table has been explained in Chapter 2. The comparison criteria also can be used when developing a new MIC topology.

The possible merits of the proposed multiple input modified inversed Watkins-Johnson converter (MIMIWJC) is described, in Chapter 3. The single input Watkins-Johnson converter is properly modified to be a more favorable circuit as a MIC, which is explained in Chapters 2 and 3. For a MIC switching scheme, FCBB switch and time sharing switching concepts are explained. To understand the fundamental circuit operation, the voltage and current mode averaged equivalent circuits are built, and these circuit models can be easily extended when more input sources are added to a MIC. By using the equivalent circuit analysis, the critical waveforms can be obtained, which can serve as a foundation for hardware design and power budgeting for a MIMIWJC.

The small signal model of the MIMIWJC is obtained using the extra element theorem (EET). The proposed equivalent source concept makes it possible to analyze the MIC in the same manner as a single input converter. By using the one source representation and the EET, the proposed converter transfer function is derived in terms of circuit parameters, and its Bode plot is drawn. Two operational strategies are proposed for the MIC; the first method is that both switching signals are generated by the output voltage feedback loop, and the other method is that one duty ratio is determined by the source power or input current regulation, and the other duty ratio is determined to make the designated output voltage.

In Chapter 5, the analytical results are verified with simulation and experimental work. The fundamental operational principles are verified with the open-loop simulation with MATLAB/Simulink and PSIM and experimental results with prototype hardware. From the simulation and experimental results, the fundamental circuit analysis which has been done in Chapter 3 and the output voltage regulation methods in Chapter 4 are confirmed. Although errors exist between the theoretical values and the experimental values, the errors come from the non-ideal switch and other components and switching transient characteristics.

6. 1 FUTURE WORK

Since this research is mostly intended to propose a new topology, a MIMIWJC, the optimization processes are not sufficient. For the power stage of this converter, the efficiency should be considered in design stage. That is, an efficiency oriented design

guide can be made in the future. Also, other switching strategies can be adopted for this converter, such as phase shift switching. From a control point of view, more analysis on proposed control methods such as stability margin and speed can be done. In addition, a protection algorithm can be provided for unexpected load and source conditions. Since the proposed MIMIWJC is not a current source interface converter, such an interface design could be developed, such as for a fuel cell interface filter design.

Appendix A: Middlebrook's Extra Element Theorem

Middlebrook's extra element theorem (EET) is a quite useful and powerful circuit analysis method [33, 40-42]. To date, nodal and loop analysis are the two most commonly used methods among engineers. Although, these methods work well with numerical values, it is hard to obtain analytical solution forms except in very simple circuits. The EET can provide analytical solutions with fewer algebraic computations in a complex circuit. In this section, the EET is derived.

A.1 THE EET DERIVATION

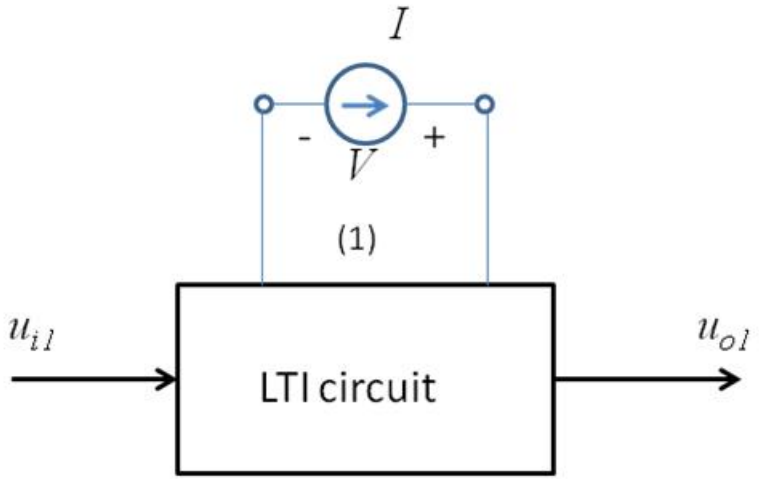
Let us consider a linear time invariant with two excitation sources so that the linear superposition can be used as shown in Fig. A.1. As it is indicated in Fig. A.1, the u_{i1} and I are two excitation sources and $u_{o1}$and V are the output response. Then, by the superposition theorem each output can be represented by

$$u_{o1} = a_{11}u_{i1} + a_{12}I \tag{A.1}$$

$$V = a_{21}u_{i1} + a_{22}I \tag{A.2}$$

where,

$$a_{11} = \left.\frac{u_{o1}}{u_{i1}}\right|_{I=0} \tag{A.3}$$



Le

Figure A.1: Linear time invariant circuit with two independent excitation sources, u_{i1} and I.

$$a_{12} = \left.\frac{u_{o1}}{I}\right|_{u_{i1}=0} \tag{A.4}$$

$$a_{21} = \left.\frac{V}{u_{i1}}\right|_{I=0} \tag{A.5}$$

$$a_{22} = \left.\frac{V}{I}\right|_{u_{i1}=0} \tag{A.6}$$

The transfer function, a_{11}, can be found when the port (1) in Fig. A.1 is open. The tranfer function a_{22} is just the same as the definition of the driving point impedance at (1) since $u_{i1} = 0$. Let us call this driving point impedance is Z_D. That is,

$$Z_D = \left.\frac{V}{I}\right|_{u_{i1}=0} \tag{A.7}$$

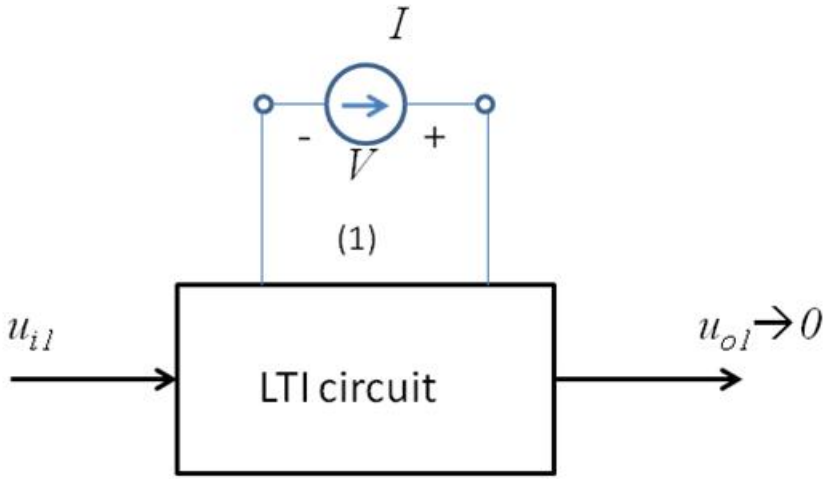


Figure A.2: The special condition to find null driving point impedance Z_N

Now let us consider the special case when the u_{o1} is nulled as shown in Fig. A.2. Then the Eq. (A.1) and (A.2) can be expressed as

$$0 = a_{11}u_{i1} + a_{12}I \tag{A8}$$

$$V = a_{21}u_{i1} + a_{22}I \tag{A.9}$$

Now let us define another impedance, $Z_{N,}$ when the u_{o1} is nulled. By Eq. (A.8) and (A.9), the Z_N can be defined by

$$Z_N = \left.\frac{V}{I}\right|_{u_{o1} \underset{null}{\to} 0} = \frac{a_{11}a_{22} - a_{12}a_{21}}{a_{11}} \tag{A.10}$$

The Z_N is[24] called the null driving point impedance.

The extra element impedance, i.e, the impedance of the exitation source I can be easily found by

$$Z = \frac{V}{I} \tag{A.11}$$

Equations (A.1) and (A.2) can be solved by eliminating I and V to draw the transfer function, *G*.

$$G = \frac{u_{o1}}{u_{i1}} = a_{11} \frac{1 + \frac{a_{11}a_{22} - a_{12}a_{21}}{a_{11}} \frac{1}{Z}}{1 + \frac{a_{22}}{Z}} \tag{A.11}$$

If the transfer function a_{11}, which is defined in Eq. (A.3), is renamed G_{old} and using Eqs. (A.7) (A.10) replacing the $\frac{a_{11}a_{22} - a_{12}a_{21}}{a_{11}}$ term as Z_{N} as shown in Eq. (A.10), then the transfer function *G* can be expressed as

$$G = G_{old} \frac{1 + \frac{Z_N}{Z}}{1 + \frac{Z_D}{Z}} \tag{A.12}$$

This is the equation form of the typical EET. This equation shows how the original transfer function G_{old} can be changed when adding the extra element, Z, to the circuit.

References

[1] S. S. Ang and A. Olivia, *Power-Switching converters*. Orlando: CRC Press, 2005.

[2] R. Miftakhutdinov, "Optimal design of interleaved synchronous buck converter at high slew-rate load current transients," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, pp. 1714-1718 vol. 3.

[3] F. C. Lee and Z. Xunwei, "Power management issues for future generation microprocessors," in *Power Semiconductor Devices and ICs, 1999. ISPSD '99. Proceedings., The 11th International Symposium on*, 1999, pp. 27-33.

[4] H. Keiichi*, et al.*, "Study on Field Demonstration of Multiple Power Quality Levels System in Sendai," in *Telecommunications Energy Conference, 2006. INTELEC '06. 28th Annual International*, 2006, pp. 1-6.

[5] A. Kwasinski and P. T. Krein, "Multiple-input dc-dc converters to enhance local availability in grids using distributed generation resources," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 1657-1663.

[6] A. Di Napoli*, et al.*, "Multiple-input DC-DC power converter for power-flow management in hybrid vehicles," in *Industry Applications*

Conference, 2002. 37th IAS Annual Meeting. Conference Record of the, 2002, pp. 1578-1585 vol.3.

[7] G. J. Su and F. Z. Peng, "A low cost, triple-voltage bus DC-DC converter for automotive applications," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, 2005, pp. 1015-1021 Vol. 2.

[8] J. L. Duarte*, et al.*, "Three-Port Bidirectional Converter for Hybrid Fuel Cell Systems," *IEEE Transactions on Power Electronics,* vol. 22, pp. 480-487, 2007.

[9] H. Tao*, et al.*, "Multi-input bidirectional DC-DC converter combining DC-link and magnetic-coupling for fuel cell systems," in *Industry Applications Conference, 2005. Fortieth IAS Annual Meeting. Conference Record of the 2005*, 2005, pp. 2021-2028 Vol. 3.

[10] N. D. Benavides and P. L. Chapman, "Power budgeting of a multiple-input buck-boost converter," *IEEE Transactions on Power Electronics,* vol. 20, pp. 1303-1309, 2005.

[11] S. H. Choung and A. Kwasinski, "Multiple-input modified inverse Watkins-Johnson converter without coupled inductors," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 3253-3260.

[12] B. Sungwoo and A. Kwasinski, "Maximum power point tracker for a multiple-input Cuk dc-dc converter," in *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International*, 2009, pp. 1-5.

[13] Z. Ruichen and A. Kwasinski, "Multiple-input single ended primary inductor converter (SEPIC) converter for distributed generation

applications," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 1847-1854.

[14] A. Kwasinski, "Identification of Feasible Topologies for Multiple-Input DC–DC Converters," *IEEE Transactions on Power Electronics,* vol. 24, pp. 856-861, 2009.

[15] S. H. Choung and A. Kwasinski, "Multiple-input DC-DC converter topologies comparison," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008, pp. 2359-2364.

[16] L. Yuan-Chuan and C. Yaow-Ming, "A Systematic Approach to Synthesizing Multi-Input DC/DC Converters," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 2626-2632.

[17] H. Tao*, et al.*, "Family of multiport bidirectional DC-DC converters," *IEE Proceedings -Electric Power Applications,* vol. 153, pp. 451-458, 2006.

[18] K. Kobayashi*, et al.*, "Novel Solar-Cell Power Supply System Using a Multiple-Input DC/DC Converter," *IEEE Transactions on Industrial Electronics,* vol. 53, pp. 281-286, 2005.

[19] H. Matsuo*, et al.*, "Characteristics of the multiple-input DC-DC converter," *IEEE Transactions on Industrial Electronics,* vol. 51, pp. 625-631, 2004.

[20] B. G. Dobbs and P. L. Chapman, "A multiple-input DC-DC converter topology," *IEEE Power Electronics Letters,* vol. 1, pp. 6-9, 2003.

[21] C. Yaow-Ming, *et al.*, "Multi-input DC/DC converter based on the multiwinding transformer for renewable energy applications," *IEEE Transactions on Industry Applications,* vol. 38, pp. 1096-1104, 2002.

[22] F. D. Rodriguez and W. G. Imes, "Analysis and modeling of a two-input DC/DC converter with two controlled variables and four switched networks," in *Energy Conversion Engineering Conference, 1996. IECEC 96. Proceedings of the 31st Intersociety*, 1996, pp. 322-327 vol.1.

[23] F. Caricchi, *et al.*, "Testing of a new DC/DC converter topology for integrated wind-photovoltaic generating systems," in *Power Electronics and Applications, 1993., Fifth European Conference on*, 1993, pp. 83-88 vol.8.

[24] E. Vargas, "High Availability Fundamentals," *Sun BluePrints™,* Nov. 2000.

[25] G. Chen, *et al.*, "Reliability-oriented design considerations for high-power converter modules," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 419-425 Vol.1.

[26] W. K. Denson, "Reliability Assessment of Critical Electronic Components," Rome Laboratory Air Force Systems CommandJUL 1992.

[27] T. Esram, *et al.*, "Dynamic Maximum Power Point Tracking of Photovoltaic Arrays Using Ripple Correlation Control," *IEEE Transactions on Power Electronics,* vol. 21, pp. 1282-1291, 2006.

[28] R. Tymerski and V. Vorperian, "Generation and classification of PWM DC-to-DC converters," *IEEE Transactions on Aerospace and Electronic Systems,* vol. 24, pp. 743-754, 1988.

[29] D. A. Grant and Y. Darroman, "Inverse Watkins-Johnson converter - analysis reveals its merits," *Electronics Letters,* vol. 39, pp. 1342-1343, 2003.

[30] P. T. Krein, *Elements of Power Electronics*. New York: Oxford University Press, Inc., 1998.

[31] D. M. Mitchell, *DC-DC switching regulator analysis*. New York: McGraw-Hill, 1988.

[32] W. M. Grady. (2008, *Materials for EE362L and EE394, Power Electronics, Fall 08*. Available: http://users.ece.utexas.edu/~grady

[33] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York: Springer, 2001.

[34] R. D. Middlebrook and S. Cuk, "A general Unified Approach to Modeling Switching-Converter Power Stages," *International Journal of Electronics,* vol. 42, pp. 521-550, June 1977.

[35] G. W. Wester and R. D. Middlebrook, "Low-Frequency Characterization of Switched dc-dc Converters," *IEEE Transactions on Aerospace and Electronic Systems,* vol. AES-9, pp. 376-385, 1973.

[36] R. Tymerski and V. Vorperian, "Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells," in *Telecommunications Energy Conference, 1986. INTELEC '86. International*, 1986, pp. 181-195.

[37] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode," *IEEE Transactions on Aerospace and Electronic Systems,* vol. 26, pp. 490-496, 1990.

[38] P. T. Krein*, et al.*, "On the use of averaging for the analysis of power electronic systems," *IEEE Transactions on Power Electronics,* vol. 5, pp. 182-190, 1990.

[39] N. S. Nise, *Control Systems Engineering*, Third ed. New York: John Wiley & Sons, INC, 2000.

[40] R. D. Middlebrook*, et al.*, "The N Extra Element Theorem," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 45, pp. 919-935, 1998.

[41] R. D. Middlebrook, "The two extra element theorem," in *Frontiers in Education Conference, 1991. Twenty-First Annual Conference. 'Engineering Education in a New World Order.' Proceedings.*, 1991, pp. 702-708.

[42] R. D. Middlebrook, "Null double injection and the extra element theorem," *IEEE Transactions on Education,* vol. 32, pp. 167-180, 1989.