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A Low-cost and Novel Method for Fabricating Bifacial Solar Cells

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A Low-cost and Novel Method for Fabricating Bifacial Solar Cells

by

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Thesis

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

The University of Texas at Austin

December 2010

Abstract

A Low-cost and Novel Method for Fabricating Bifacial Solar Cells

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The University of Texas at Austin, 2010

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In this work we proposed and demonstrated a novel and very cost effective method to fabricate bifacial solar cells with conventional structure. Bifacial cells collect sunlight from both faces, and hence have an obvious advantage over monofacial cells by occupying the same physical area and converting solar energy to electricity more efficiently. Despite this fact, bifacial cells are not that popular simply because of the costs associated with them. These costs are related to both manufacturing of the actual cells and integration of modules/solar panels. The cost of manufacturing is higher than regular commodity cells because the number of processing steps for fabrication is higher than their monofacial counterparts. The main reasons for that is a necessity of some kind of lithography step and/or alignment to make the grid pattern on both sides separately. Also metallization has to be done on both sides separately, one at a time. The method proposed

in this work gets rid of both of those limitations by use of a lithography/alignment-less method for patterning contact holes, and a low temperature metallization scheme used for both the front and rear surfaces to grow metal simultaneously. This technique is simple and cost effective enough to be potentially incorporated in a batch process in industry, thereby reducing the cost of manufacturing. In this thesis we have presented preliminary results from the cells (bifacial and monofacial) fabricated using the above technique with proposals for further improvements. The measurement data underscores the clear advantage in using bifacial cells over monofacial cells fabricated using this method, in terms of efficiency. This also demonstrates that this proposed method is a viable way to manufacture bifacial cells with lower cost and relative ease. We also fabricated and measured monofacial solar cells in order to study the beneficial effects of including buried contacts as a possible part of device structure. The study shows significant improvement in efficiency due to incorporation of deep trenches for metal contacts in device design.

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Chapter 1: Introduction

1.1 SOLAR ENERGY AND SOLAR CELLS

In recent times we have witnessed Gulf of Mexico oil spill tragedy and its vast impact on environment and ecosystem; combined with that the potential shortage of supply to the demand of oil, coal, and natural gas, and climate change awareness at its peak, people have become more acutely aware of need for safer and greener alternative to fossil fuels. There is no single silver bullet as a solution to this problem. People are looking into all sorts renewable resources which are environment friendly like solar energy, wind energy, geo–thermal energy, bio-mass, and hydro energies. Among these photovoltaics or solar energy perhaps has the most potential to meet the substantial fraction of world's energy needs. It is perhaps the most elegant and direct way of generating renewable electricity. In this technology solar energy is used to convert solar radiation directly in to electricity. Devices that convert solar radiation in to electricity are called photovoltaic devices, or solar cells. Sun's radiation incident every year on earth is approximately equivalent to 120,000TW of power when measured, 0.02% of that solar power is enough to meet the energy need of the whole world [1]. It has been estimated that even with as low 10% efficiency solar cells covering 0.3% of the land area in the southwestern desert region of United States can theoretically meet the electricity need of the entire country [2].

The rapid progress in solar power technology in past two decades has been making it a proven alternative to conventional energy systems. In fact solar power is becoming one of the key players in the market of renewable energy. Between years 2000

and 2009, the global photovoltaic demand grew at an impressive average of 51% per annum. The annual capacity installed has risen from 170MW in 2000 to 7.118GW in 2009 (Fig. 1.1) [3].

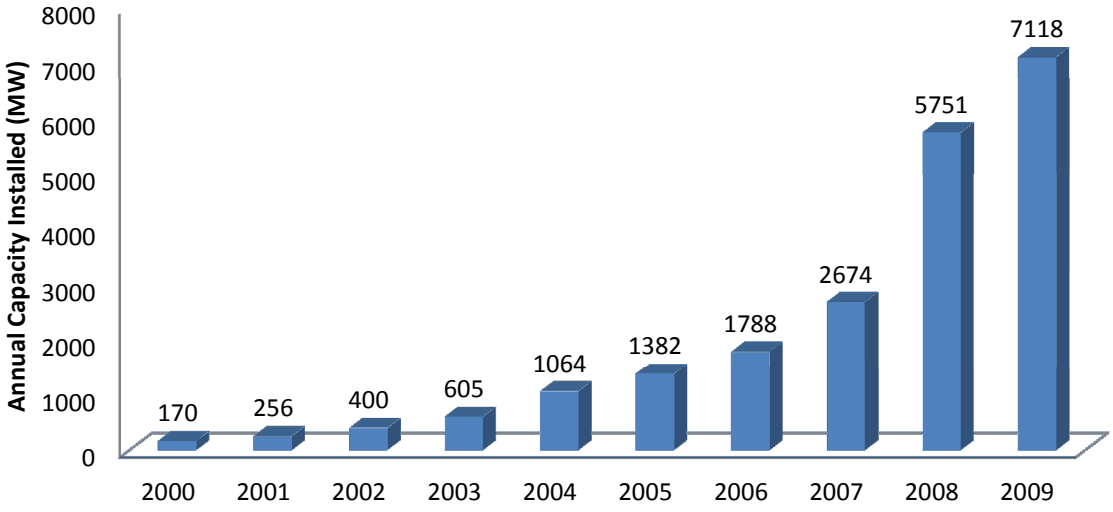

Figure 1.1 Annual global photovoltaic modules demand from 2000 to 2009 [3]

1.2 SOLAR CELL MATERIALS:

There are several materials & technology that are currently in use for making solar cells in the industry, like crystalline silicon, amorphous silicon, CdTe, CIGS (Copper Indium Gallium di-Selenide). Among these crystalline silicon dominates the market share. Fig. 1.2 shows the market share for different materials for solar cells in the year 2009.

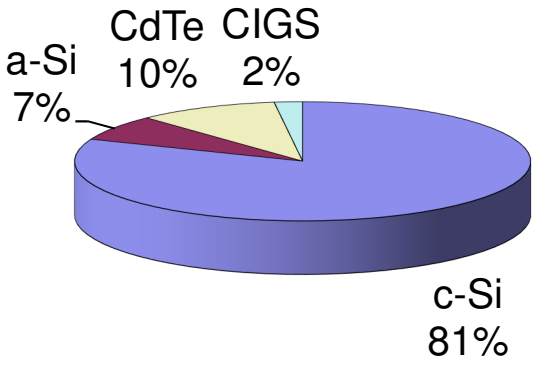

Figure 1.2 Market share for different types of solar cells in the year 2009 [4]

There are a lot of compelling reasons for crystalline silicon to have the most demand in solar cell business. Silicon has good semiconductor properties e.g., band gap etc. which enables solar cells made out of mono or multi-crystalline silicon have much higher conversion efficiencies compared to amorphous silicon, CdTe, or CIGS. It also has excellent performance stability with very little degradation over time, as opposed to thin film (amorphous silicon) solar cells. Crystalline silicon is also non-toxic, whereas CdTe is a known carcinogen [5]. And finally silicon is the 2nd most abundant element on earth crust. The most efficient single junction photovoltaic cells in current technology available are based on p-n junctions in bulk crystalline silicon.

Two types of crystalline silicon based on the size of a single grain are used in bulk crystalline silicon solar industry. “Monocrystalline” silicon, where just a single grain (>10cm) characterizes the whole material. “Multicrystalline” silicon, where there are different sizes of grains is present but sizes vary from 1mm to 10cm. The cost of single crystal is greater than multicrystalline silicon, because starting material to obtain single

crystal material has to be of very pure quality. But single crystal bulk silicon solar cells do give us better performance when used in fabricating photovoltaic devices. The energy conversion efficiency i.e. the ratio of electrical power output to solar power input in a given area of a device, bulk single crystal tend to outperform bulk multicrystalline solar cells. The theoretical limit for single crystal silicon solar cells under the AM 1.5 spectrum is well over 30%, whereas the solar cells made out of multicrystalline silicon has an upper limit in efficiency of approximately 19% [6].

1.3 CHALLENGES IN SOLAR INDUSTRY

Despite all of these advantages and the prices of both types of crystalline silicon coming down drastically in recent years [7], manufacturing cost for crystalline silicon solar modules are still more expensive than solar cell module made of other materials. That is why manufacturing cost containment is one of the key focuses in solar industry. The most important and standardized number for cost effectiveness that is used in photovoltaic industry on which prices, sales number, and growth are based is cost per watt or cost per generated power. The two main strategies of bringing down the cost per watt are –

1) increasing the energy conversion efficiencies of the solar cells, and
2) decreasing the cost per unit area.

1.3.1. Increasing solar cell efficiency

Increasing the solar cell efficiency would be one way to counter the challenges. But there are fundamental limits to efficiency which prevents increasing it indefinitely. In this section we talk about three different kinds of solar cell architectures which produce

the highest levels of energy conversion, and the difficulties that are faced in fabricating them. And then we briefly discuss about the limiting factors in efficiency.

1.3.1.1 *High Efficiency Solar Cells*

There are several high efficiency single crystal large area silicon cells structures out there either available commercially or developed in laboratory which have conversion efficiencies over 20%. Some of the most important ones among them are discussed below.

1) Back contact solar cells: Interdigited Back Contact (IBC) cell and the Emitter Wrap Through (EWT) cell are two different types of back contact cells. IBC includes all of those cell designs which rely upon carrier collection at a rear junction alone. The EWT class of cells can accomplish carrier collection at both sides and relies upon current conduction from the front to the back through some sort of perforation in the cell. These cells must be fabricated on material with a long minority carrier diffusion length. The distance from any point in the cell to the junction must be much less than the diffusion length. This imposes a restriction on gridline geometry for metal contacts requiring fine lines and tight tolerances. As material quality decreases, the restrictions on grid geometry become more severe. Another requirement is excellent front silicon surface passivation, since the junction is on the back and most photogeneration occurs at the front. This surface passivation must remain stable as well [8].

2) Laser grooved buried contact: In this approach grooves are formed using laser at the top surface of a cell, through a previously lightly diffused layer and dielectric coating. The grooves expose bare silicon which can be heavily doped using a second diffusion confined by the dielectric to the grooved region. Then electroless metal plating

is done on these heavily doped regions. The shallow doping in most of the places allows these types of cells to respond to blue light. Low shadowing effect from the contacts due to grooves and narrower finger size increase the performance more. But in this process laser has to be used to create cross-hatch texturing in the front surface in addition to create macro grooves for contacts. This increases the surface area, and consequently causes more recombination there, resulting in increase in dark saturation current. To counter this problem the top surface needs to be very well passivated [9].

3) Heterojunction with Intrinsic Thin layer (HIT): This types of cells combine both crystalline and amorphous silicon materials. The cell structure utilizes hydrogenated amorphous intrinsic silicon deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) sandwiched between p+/n+ amorphous silicon at the front and back surface. These intrinsic amorphous layers provide a hetero interface high band gap with bulk crystalline silicon. A transparent conducting oxide layer is added on top of heavily doped p+/n+ layers, to good lateral carrier transport to screen printed metal contacts on both surfaces. Since the rear side is patterned the cell can respond to light entering from both sides. But besides having fairly complex structure one of the main drawbacks in this cell architecture is the transparent conducting oxide which is neither fully transparent nor perfectly conducting and hence causes 10%-15% current loss due poorer light absorption [10].

All the large area terrestrial cells efficiencies for AM 1.5 spectrum are given in Table 1.1.

Cell Type	Efficiency (%)	Developed By
Back contact	21.4±0.6	SunPower
Laser grooved buried contact	21.7±0.7	University of New South Wales, Australia
HIT	23.0±0.6	Sanyo

Table 1.1 Efficiencies of different large area terrestrial single crystal solar cells under AM 1.5 spectrum and cell temperature of 25ºC [11].

All of these cells described above fall in to high efficiency bulk silicon solar cells that are currently available in the market with the exception of Laser grooved buried contact solar cells. None of the above falls in to the category of simple vertically structured p-n junction solar cells, which are known as the conventional solar cells. Thereby manufacturing cost for them are still higher than where they need to be.

1.3.1.2. *Fundamental Limits to Efficiency*

The fundamental limit to the efficiency of a conventional p-n junction silicon solar cell, under the global AM1.5 spectrum, which is the present standard for cell testing, is 30.1% [12]. This efficiency is calculated assuming a sunlight that is isotropic.

There are numerous issues that are limiting performance of a silicon solar cell. They are discussed below.

1) **Photon generated current limits:** Absorbed photons in a solar cell are the reason for energy conversion. Each photon above a certain threshold energy is absorbed generates an electron hole pair (sometimes it can generate more than

one pair). So just by calculating the threshold energy above which maximum numbers of photons are collected should give us the maximum limit to the photon generated current. But that is not the case. This is because there is no single minimum threshold energy for light absorption in silicon. Experimental data shows [13] that rather than there being a single minimal threshold energy for effective light absorption in silicon, there are a series of thresholds of decreasing energies which correspond to progressively weaker absorption processes. These weak sub bandgap absorption processes will face increasing competition from other intrinsic absorption processes (free carrier absorption and lattice absorption) as the photon energy decreases. Hence effective electron-hole pair generated would be a fraction of what it could be due to all the absorption processes.

2) **Open circuit voltage limits:** In order to draw power from a solar cell there has to be a finite voltage drop across it. Theory and experimental data suggest that as this voltage increases the electron hole product and recombination rate throughout the cell increase. The maximum open circuit voltage is obtained when the recombination process throughout the cell is kept at a minimum. It is possible to eliminate recombination via bulk defects by having defect free substrates of silicon. Therefore the intrinsic recombination processes i.e. band-to-band radiative (recombination by giving up energy and relaxing back to original band energy level) and Auger recombination (recombination by energy transfer to a second carrier which happens in heavy doping condition) will determine the open circuit voltage limit. Previous work [14] shows for a

wide base cell (which is in most of the cases) where the base length (which is effectively the thickness of the silicon substrate) is greater than the minority carrier diffusion length (distance a minority carrier travels before it recombines), open circuit voltage is limited by the values which is less than 715mV.

3) **Fill factor limits:** Fill factor is a measure of maximum power output that can be obtained from a solar cell. It is a very important parameter for a cell. Fill factor is heavily dependent on the open circuit voltage of the cell [15]. This dependency is somewhat monotonic. Therefore this particular parameter is limited by the limitation of open circuit voltage as discussed in the previous point.

4) **Energy conversion efficiency limits:** For solar cells which are not multi-junction the maximum current which can be generated for a given thickness of the substrate depends on the angular distribution of sunlight across the sky. Most current will be generated when the cell is with a 90º acceptance and an isotropic response. These kinds of restrictions give us theoretical limit for maximum short circuit current density and open circuit voltage. For an optimum thickness of 100um substrate the cell short circuit current density is 42.2mA/cm^2, and open circuit voltage is 772mV [12]. That limits the fill factor to 89.5% and efficiency to 30.1%. Bottom line is that the cell performance is limited by the directionality of the sunlight used for the maximum performance.

5) **Material requirement:** In order to approach the limiting performance efficiency, the quality of the silicon material, surface passivation, and rear surface reflectivity need to meet certain minimal requirements. Starting silicon material for solar cells should be defect free; otherwise it will cause a lot of recombination in the bulk. Similarly the surface of the cell should be well passivated (i.e. defect free), so that the carriers generated due to light excitation does not get recombined at the surface. The light with longer wavelengths that are absorbed in the substrate should be retained by reflection from the rear surface by having oxide layer at the rear side as the reflector.

1.3.2 Decreasing cost

Increasing the efficiency of a solar cell without decreasing the cost per generated power is not economical since sunlight is free. Thus the "efficiency" matters only when the "cost" is defined as the cost per unit solar irradiation on cell, per unit area of the cell, per unit weight of the cell, or unit power generated. Therefore the challenge in increasing the "efficiency" is great point of interest both in industry and in academia.

A lot of efforts are being put in to making high efficiency and low cost photovoltaic energy conversion. Despite the rapid growth in the manufacturing volume, together with significant drop in module selling price, the high costs associated with solar power generation are one of the main obstacles to widespread global use of solar electricity. Up to a certain level, the key to the solution this problem is higher production volume. However, apart from using thinner and thinner silicon wafers to get the material cost down in conjunction with more improved and higher efficiency generating solar cell

processing methods, the manufacturing cost reduction in the long run would be the main key for solar industry to replace conventional energy industry and become niche to mainstream.

Most commercially available low-cost bulk crystalline silicon solar cells have the efficiencies in 10%-15% range. Those at the high ends of this range are based on single crystal silicon, and those in the middle range are made of multi-crystalline silicon. The lower end of the range tends to be occupied by silicon ribbon or sheet type or more inferior type multi-crystalline silicon solar cells.

1.4 MOTIVATION FOR BIFACIAL CELL

Commonly available bulk silicon commodity solar cells with simple p-n homojunction mentioned in the previous section with medium and high end of the range in efficiency are screen-printed front side contact on plasma-enhanced chemical vapor deposition (PECVD) Si_3N_4 and aluminum (Al) back surface field (BSF) on the rear side. But these receive sunlight only from one side.

To get the maximum efficiency out of these conventional solar cells they should always face the sun directly. But due to change in sun's position in the sky over the course of a day, any flat plate collector in a fixed position will face the sun directly a part of the time. Tracking system can be used for the solar panel to follow the sun, but it only increases the cost. There's another problem due to scattering of sunlight in the atmosphere. That means that a significant fraction (~15%) of light is diffuse, i.e., incident from different angles rather than directly from the sun. Since the light rays in diffuse sunlight are not parallel, they cannot be refracted or concentrated very efficiently [16].

The bifacial solar cells unlike regular monofacial solar cells can collect sunlight from both sides and convert them into electrical power. The sunlight incident on the front side and the reflected sunlight from ground (diffuse sunlight) or intentionally designed glass panels collected at the rear side are the sources of photo generated currents in bifacial solar cells. The reflected sunlight in this case has a specific term named *albedo*. Bifacial cells therefore effectively can have similar structures to conventional solar cells, with some minor modifications at the rear side of the cell, and still can produce 25% to 80% additional power output [17]. Bifacial cells utilize silicon material more effectively in generating power thereby reducing the material cost, and bifacial solar panels occupy less area to generate the same amount of power that their monofacial counterparts. Besides these advantages, bifacial cells made on thin substrates operate at reduced temperature compared to the conventional monofacial ones, because of the lower infrared absorption on the open-grid rear metallization, [18]. And since they generate more power, they have a higher power to material weight ratio than other commercial cells making them more cost effective. Besides using bifacial cells instead of monofacial ones for conventional uses, a broad spectrum of applications is possible; applications in places such as for shop windows, private homes, offices and industrial buildings [19].

There have been many efforts in the past to develop and find applications for these devices in space and terrestrial systems. Numerous studies have been done on bifacial solar cells with regular p-n homojunctions on different grades of silicon substrates. The highest efficiency among bifacial cells using multicrystalline silicon that has been reported is 15.4% on the front side and 10.2% on the rear side under illumination [20]. In the monocrystalline area, work has been done on both CZ and FZ

type wafers. The highest efficiencies on two sides of a bifacial cell on CZ silicon substrate reported [21] are 17.7% and 15.2% respectively. The record for having the highest efficiencies belongs to bifacial cells made on FZ wafers. Those efficiencies are 21.3% on the front and 19.8% on the rear surface [22].

All these efficiency numbers are impressive, but there are many processing complexities exist to make those solar cells. That makes it harder to have low cost manufacturing method to make bifacial cells. The multicrystalline cells described in [20] does not employ optical lithography which is economic, but it employs screen-printing technique for metal contacts, which requires a certain level of alignment, a two-step process for metallization, and high temperature co-firing. The bifacial cells reported in [21] uses optical lithography, and evaporated metal stack of Ti-Pd-Ag for the front and Al-Ti-Pd-Ag for the back contact, followed by silver electroplating. The highest efficiency cells reported in [22] used thirteen photo masking steps and vacuum evaporation for metallization, rendering the whole process too expensive for commercial manufacturing purposes.

The take home message from the studies above is that one of the main challenges for bifacial cells is having a low cost fabrication method. Hubner et. al. [18] presented a cost effective method where cells were made without optical lithography by using shadow mask to evaporate metal Ti-Pd-Ag metal stack, and then depositing Silicon Nitride on both sides using remote-plasma chemical vapor deposition (RPCVD) to get very good surface passivation. However, the fact that the fabrication technique described here still uses evaporation process for metal deposition in two separate steps on both

sides, and RPCVD which is incompatible with industry standards, make it commercially unviable process.

In this work we propose a very low cost, method for making a conventional bifacial solar cell. The number of steps employed is significantly lower as we do not use optical lithography for patterning surfaces to have metal contact openings. Instead a shadow mask is used for Silicon Nitride deposition that passivates the surface at the same time it acts as an Anti-Reflective Coating (ARC). In addition to that we have employed a technique where the contact metal is deposited on both surfaces at the same time, rather than one surface at a time, and instead of evaporating the metal or screen printing, we have a cheaper way to deposit the metal. This method does not require any kind of alignments, and could potentially be used as a batch process compatible to industry.

The proposed technique of fabrication can potentially boost the efficiency by 50% or more from the typical efficiencies that we get from commodity solar cells that are available in the market, while keeping the cost of manufacturing same or even possibly less. The boost in efficiency simply comes from having the rear surface collect sunlight too, and converting it to electricity. Therefore converting from monofacial to bifacial architecture and keeping the cost same or less as that of manufacturing of conventional monofacial cells is the novelty of this work.

1.5 OUTLINE OF THE THESIS

In the next chapter of this thesis, basic principles and workings of a solar cell are introduced. In Chapter 2 we talk about intensity and spectrum of solar radiation. Then we talk about basic theory of p-n junction, which is the main part of a solar cell. After that

we take a look at operations of a solar cell and relevant definitions of different parameters followed by a discussion on structure of a solar cell with design considerations taken into account.

In third chapter we discuss a 2-D/3-D numerical simulation software Sentaurus Device, and simulation study of bifacial silicon solar cell on single crystal silicon substrate is discussed. Then we describe our bifacial cell design and the novel fabrication method that we proposed. Both monofacial and bifacial cells are fabricated using identical method. Measurement done on both cells clearly shows bifacial having an edge over monofacial cells. This is only preliminary data with scope of lot of optimization to be done to improve on the efficiency significantly.

Suggestions for future work are presented at the 4^{th} and concluding chapter of this thesis. In this chapter we discuss various ways to improve on our methods to get to the optimum performance level, followed by the conclusion drawn from our experimental work.

Chapter 2: Theory of Solar Cells

2.1 SOLAR IRRADIANCE

In order to discuss solar cell, it is necessary to define magnitude and spectral content of the solar energy incident on earth surface. At the sun's surface the irradiative power density is 62 MWm^{-2}. This is reduced to 1353 Wm^{-2} above the earth's atmosphere and is greatest in the visible wavelength range, peaking at blue to green. This solar spectrum is roughly similar to the spectrum of a black body at 5760 K, reduced by the factor 4.6×10^{4}. The comparison between the solar and black body spectra is shown in Fig. 2.1. When the sun is directly overhead, nearly 70% of solar radiation incident to Earth's atmosphere reaches the surface undisturbed. Another 7% reaches the ground scattering from the atmosphere at every angle. The rest is absorbed or scattered back into space.

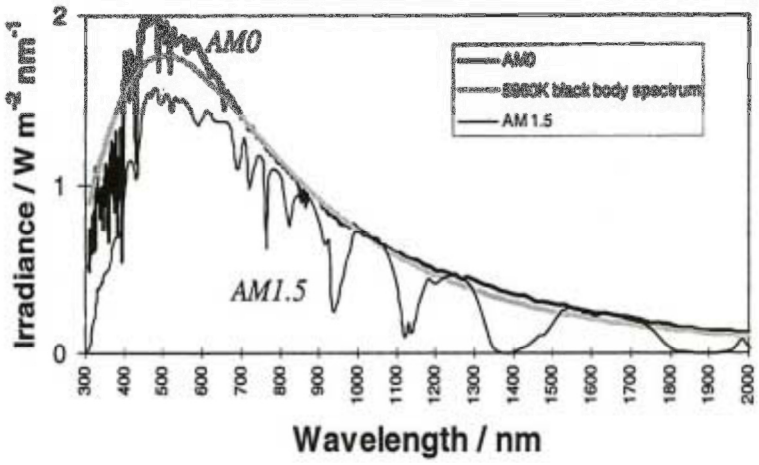

Figure 2.1: A comparison solar spectrum in Earth's atmosphere with black body spectrum at 5760K reduced by the factor 4.6×10^{4} and with standard terrestrial (AM 1.5) spectrum [16]

Such loss of solar radiation caused by atmosphere is quantified by 'Air Mass' factor, η_{AirMass}, defined by

$$\eta_{AirMass} = \frac{\text{optical path length to sun}}{\text{optical path length if sun is directly overhead}}$$

The Air Mass n_{AirMass} spectrum is an extraterrestrial solar spectrum attenuated by n_{AirMass} thicknesses of an Earth atmosphere of standard thickness and composition. The standard solar spectrum is defined as AM 1.5 spectrum normalized, so that the integrated irradiance is 1000Wm^{-2}. But the actual irradiance varies with changes in seasons and sun's orientation in different parts of the world on different times on a single day [16].

2.2 BASICS OF A SOLAR CELL

Solar cells convert suns electromagnetic radiation in to electrochemical potential energy by absorbing a photon which causes electron to jump to a higher excited state. This gained potential energy can be extracted by separating the excited state from the ground state by having an energy gap greater than thermal kinetic energy *kT*, where *k* is Boltzmann's constant (8.62eVK^{-1}), and *T* is the temperature in Kelvin, and the photovoltaic material having two or more energy levels separated by more than *kT*. This separation allows excited electrons to stay at higher state for longer time compared to thermal relaxation time, so that it could be collected [Nelson J, "*The Physics of Solar Cells"*, 1st edition, London: Imperial College Press, 2003].

2.2.1 P-N Junction

One of the vital parts of a solar cell consists of two different layers of silicon that have with small quantities of impurity atoms (e.g., phosphorus, arsenic or boron) deliberately introduced (doping) to it. This is done to form what is called a p-n (positive carrier or hole rich-negative carrier or electron rich) junction. The addition of such dopants is crucial to the cells operation and provides the mechanism which forces electron hole pairs generated by light to do useful work in an external circuit.

Optical or thermal excitation can cause alteration of silicon's electrical properties. Another way to alter that is to add small amounts of impurity atoms or dopants. For example if arsenic is added to molten silicon and then the solidified crystal would contain some arsenic atoms in the crystal in place of silicon atoms. Arsenic has 5 valence electrons instead of silicon's 4 valence electrons. Therefore there would be an extra electron for every phosphorus atom (Fig. 2.2). That is why these impurity atoms are called a "donor". These free electrons are known as majority carriers. Generally there are also few holes present due to thermal electron hole pair generation as in intrinsic silicon. These holes are called minority carriers. The silicon in this state would be called an n-type material and would have some current conducting capability.

On the other hand if silicon is doped with boron, which has only 3 valence electrons, each boron atoms can only form full bonds with 3 of the silicon electrons while leaving the 4th bond broken or incomplete thereby creating a hole as a free carrier. That is why these impurity atoms are called an "acceptor". In this case holes would be considered as the majority carriers, and the electrons as minority carriers. In this case the silicon would be known as p-type material.

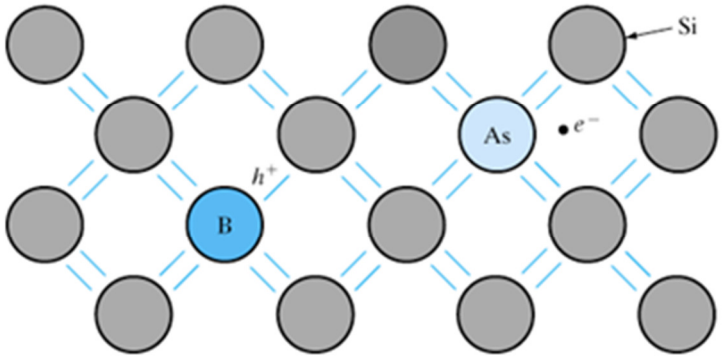

Figure 2.2: Donor atom (As) and acceptor atom (B) in the covalent bonding model of Silicon crystal generating electron and hole respectively [23]

The p-n junction is created when a p-type and n-type regions are adjacent to each other in the same silicon body. Near the interface, free electrons in the n-type material start diffusing into the p-side, leaving behind a layer that is positively charged due to the presence of fixed donor atoms. Holes in the p-type material diffuse into the n-type, leaving behind a layer that is negatively charged by the fixed acceptor atoms. This diffusion of the two types of majority carriers, in opposite directions across the interface, has the extremely important effect of setting up a strong electric field, creating a potential barrier to further flow of carriers. Equilibrium is established when the tendency of electrons and holes to continue diffusing down their respective concentration gradients is offset by their difficulty in surmounting the potential barrier. In this condition there are hardly any mobile charge carriers left close to the junction and a so called *depletion region* is formed. The depletion region makes the p– n junction into a diode, a device that conducts current easily in one direction only. Fig 2.3 shows an external voltage *V* applied

to the diode, making the *p* – type material positive with respect to the *n* – type, referred to as *forward bias.* In effect the external voltage counteracts the "built–in" potential barrier, reducing its height and enabling large numbers of majority carriers to cross the junction – electrons from the n–side and holes from the p–side. This results in substantial forward current flow. Conversely, if the external voltage is inverted to produce a *reverse bias,* the potential barrier increases and the only current flow is a very small *dark saturation current* (I_0). This is because a bias that increases the potential barrier for majority carriers decreases it for minority carriers – and at normal temperatures there are some of these present on both sides of the junction due to thermal generation of electron–hole pairs.

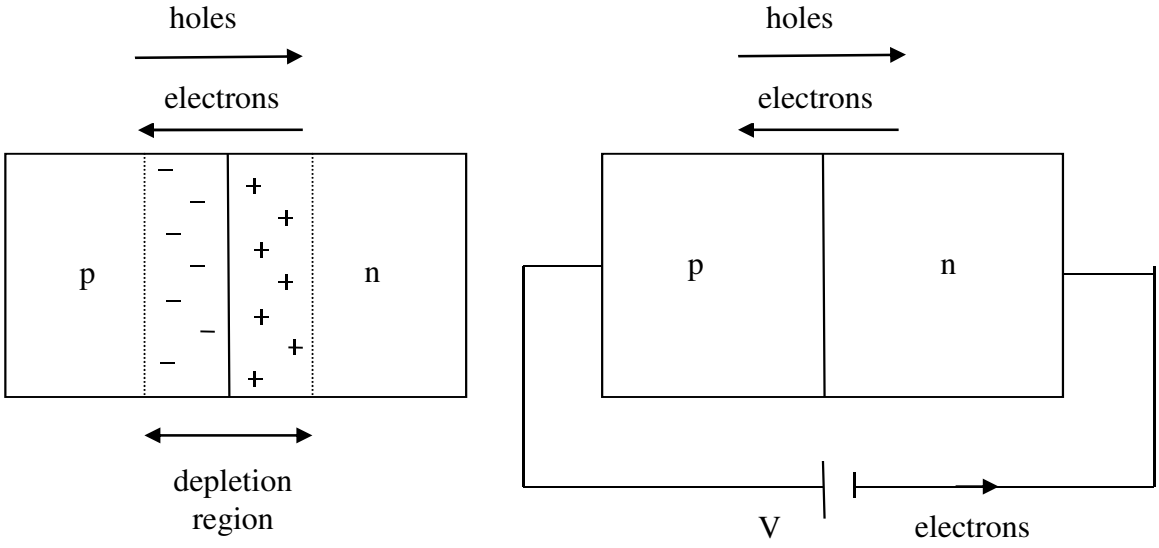

Fig. 2.3 (a) A p-n junction, (b) p-n junction under forward bias

The practical result of these movements of electrons and holes is summarized by the diode characteristic in Figure 2.3. Diode current *I* increases with positive bias, growing rapidly above about 0.6 V; but with negative bias the reverse current ' saturates ' at a value I_0 called *dark saturation current*. Mathematically the curve is expressed as:

$$I = I_o(e^{qV/kT} - 1) \qquad (2.1)$$

This is known as the *Ideal Diode Equation*.

2.2.2. Operation of a Solar Cell

The fundamentals of solar cells can be explained further with the simplest example, the design of which is described next. In practice most photovoltaic energy conversion is based p-n junction made in semiconducting materials rather than Schottky barrier, because it has more reliability and higher open circuit voltage. A typical p-n junction based solar cell is shown in Fig. 2.4. It has six main components emitter, base, front side passivation layer, antireflection layer, front side metal grids, and back side metal contact. Normally the emitter and base are made out of two different (p-type or n-type) types of doped regions to form a p-n junction.

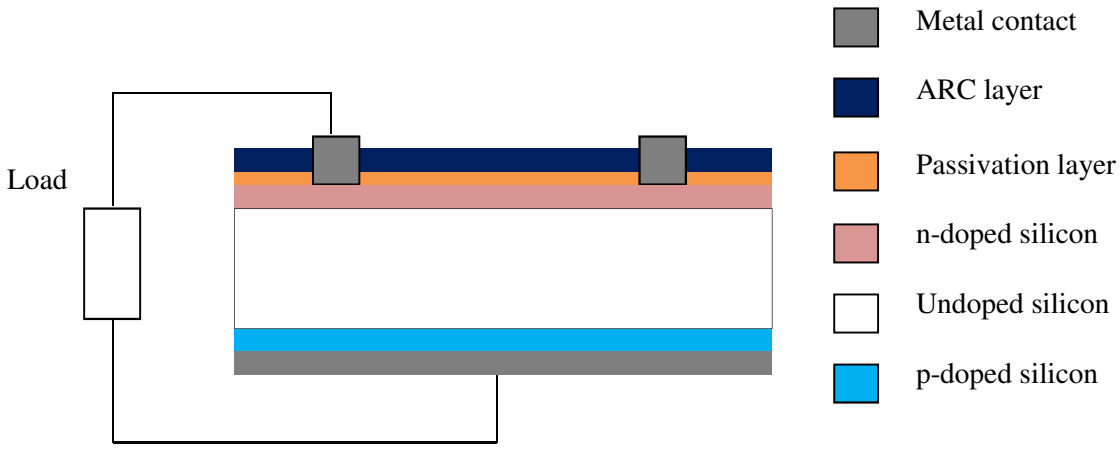

Figure 2.4: Structure of a conventional monofacial homojunction solar cell

The basic operation of solar cell is as follows. Photons in sunlight, incident on the light facing side of the cell get absorbed in the base region. The absorption excites electrons to higher energy level, creating electron-hole pairs or carriers. Carriers are generated only when incident photons have equal or greater energies than the band gap of the semiconductor. However, minority carriers, such as electrons in p-type material, hole in p-type material exists only for a certain amount of time before recombination. This time is known as minority carrier lifetime. Therefore those carriers must be collected before they recombine, and this collection is done at the p-n junction. If the light generated carriers reach p-n junction, they will be swept across the junction by the electric field and become majority carriers.

If the metal contacts of emitter and base are connected together through an external circuit, the carriers flow through the load, dissipates energy, and return to the solar cell, thereby completing the circuit and generating current. This photocurrent closely follows the ideal diode equation (Eq. 2.1) in terms of its dependence on voltage

Dark saturation current as mentioned before is a relatively small amount of current that flows through photosensitive diode even when there are no photons entering the device. It happens due to random generation of electrons and holes in the depletion region of the device while swept by high electric field.

Since solar cell operates under light, the *I-V* curve of solar cells is superposition of the same for a normal p-n junction diode under no illumination and the photo-generated current. Effectively the light shifts the p-n junction dark curve down to the fourth quadrant where power is generated from the diode. Thus the ideal diode law becomes

$$I = I_o(e^{qV/kT} - 1) - I_L \qquad (2.2)$$

Where I_L = the photo-generated component of the current.

The dark and light *I-V* characteristics of a p-n junction solar cell are shown in Figure 2.5. For convenience's sake the current axis is inverted sometimes as shown in this figure.

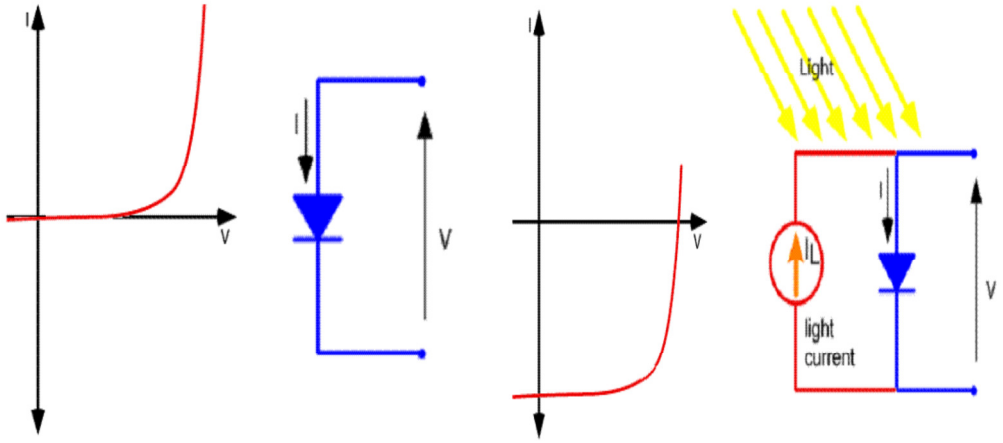

Figure 2.5: Dark (left) and light (right) I-V characteristics of a simple p-n junction solar cell [24]

2.2.3 Performance Parameters of a Solar Cell

The *I-V* curve of a solar cell gives us information about several important parameters relevant to the characteristics and performance of a solar cell. These parameters are –

1) **Short circuit current (I_{SC})**: It is the current flowing through the solar cell when voltage across the cell is zero. This current is due to the generation and collection of photo-generated carriers. So this is essentially the photo-

generated current, and is the largest current that can be drawn from a solar cell for power generation purpose.

2) **Open circuit voltage (V_{OC}):** This is the maximum voltage that is available when there is no current flowing through the solar cell. By setting the current value equal to zero on the left hand side of the ideal diode equation in the the modified ideal diode equation, we get

$$V_{OC} = \frac{kT}{q}\ln(\frac{I_L}{I_0} + 1) \qquad (2.3),$$

which shows V_{OC} is dependent on both dark saturation current I_0 and the photo-generated current I_L. Since I_L typically has very small variation, the dark saturation current I_0 has major effect in varying the value of V_{OC} from solar cell to solar cell.

3) **Fill factor (*FF*):** The power output of a cell for any operating point can be represented by the rectangle shown in Figure 2.4. The operating point (I_{mp}, V_{mp}) in the figure denotes the point where the power output is maximized.

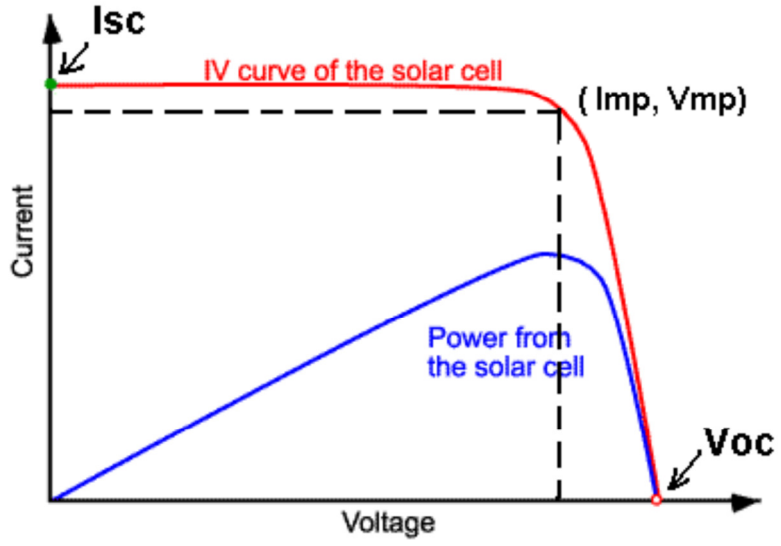

Figure 2.6: I-V curve, Power curve, and some essential parameters [24]

Fill factor (*FF*), is a parameter related to the maximum power from a solar cell. It is a measure of the *squareness* of the *I-V* curve, and is defined as the ratio of the maximum power from the solar cell to the product of *Voc* and *Isc* as following equation:

$$FF = \frac{V_{mp} \times I_{mp}}{V_{OC} \times I_{SC}} \qquad (2.4)$$

The theoretical maximum value of *FF* can be found by taking the derivative of power with respect to the voltage and equaling to zero, i.e.

$$\frac{d(I \times V)}{dV} = 0 \qquad (2.5)$$

But the solution to above equation doesn't give a closed form for *FF*. That is why there's an empirical formula which is used for finding the theoretical maximum for *FF*, which is given by

$$FF = \frac{\frac{q}{kT}V_{OC} - \ln(\frac{q}{kT}V_{OC} + 0.72)}{\frac{q}{kT}V_{OC} + 1} \qquad (2.6)$$

4) Efficiency (η) – it can be defined as the ratio of output energy from solar cell to the input energy from incident sunlight:

$$\eta = \frac{P_{max}}{P_{in}} = \frac{V_{OC} I_{SC} FF}{P_{in}} \qquad (2.7)$$

This is the most important and widely used parameter to evaluate the performance of a solar cell.

Besides the parameters that are discussed above there are some other very useful components of a solar cell that we need to understand its electronic behavior. That is why

a solar cell has electrical equivalent based on discrete electrical elements, whose behaviors are well known. An ideal solar cell may be modeled by a current source in parallel with a diode, shown in Fig. 2.7.

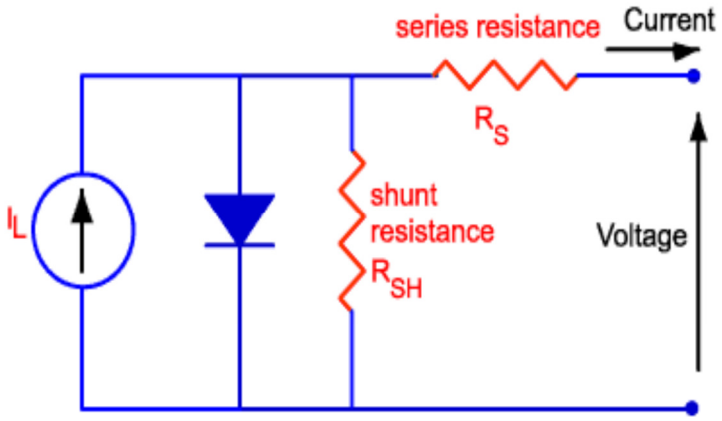

Figure 2.7: Circuit representation of a solar cell [24]

The figure above shows a parasitic series (R_S) and shunt resistance (R_{SH}) associated with solar cell. The contributing factors to series resistance are the bulk resistance of silicon, resistance in the metallic contacts and interconnects, and the contact resistance between the metallic contacts and the semiconductor. The shunt resistance, R_{SH}, is caused by leakage across the p-n junction and in surface regions in the presence of crystal defects and precipitates of foreign impurities. Both types of parasitic resistances act to reduce the fill factor.

Another important parameter is the ideality factor n, which is a measure of how closely the diode follows the ideal diode equation. The simple diode equation is considered ideal because of certain assumptions about the cell. In practice, there are 2nd order effects present in a real world solar cell so that the diode does not follow the simple

diode equation, and the ideality factor provides a way of describing this. Thus for actual diodes, the Eq. (2.2) becomes:

$$I = I_o(e^{qV/nkT} - 1) - I_L \qquad (2.8)$$

Correspondingly, the term kT in equations (2.3)-(2.7) would all be replaced with nkT when the non-ideality is included.

2.3 DESIGN OF A MONOFACIAL SOLAR CELL

While designing solar cells we have to consider design architecture that would maximize light absorption, charge separation and charge transport, and to maximize photo-voltage.

Among these design considerations, light absorption requires -

1) high optical depth
2) minimized shading
3) minimized reflection
4) light trapping structure (texturing)

Charge separation requires –

1) good quality junction
2) high built-in bias in the junction

Efficient charge transport requires –

1) good quality crystal
2) low bulk and surface recombination
3) good majority carrier conductivity

Maximizing photovoltage requires –

1) different layer's thicknesses
2) doping levels of the layers
3) surface treatment
4) optimum surface pattern

We will now take a look at the most conventional example for a solar cell, and see how above mentioned objectives for achieving a good solar cell design is done. The solar cell structure discussed below is the architecture that very closely resembles most commonly available cells in the market with screen-printed front side contact on PECVD Si3N4, and aluminum (Al) back side field (BSF) on the rear side.

A typical design for solar cell has already been shown in Fig. 2.4. We start with a lightly doped p-type or n-type (p-type wafer is most commonly used). Then a heavily doped n-type (n+) or p-type (p+) region known as emitter created at the front. This could be achieved using several different methods. Some of the most commonly used methods are solid source doping (using ceramic wafers made of compound of dopant atoms), gas flow in high temperature furnace (POCl3, BBr3, etc.), and laser assisted doping. Then passivation layer (SiO_2, a-Si) are grown thermally, or using PECVD or ALD systems. An ARC is deposited using either a furnace or PECVD system. After that we both pattern the cells (using optical lithography) and etch to open up the front contact holes, or use screen printing technique to make the front and back contacts.

However, while making the solar cells, we need to take care of several design aspects in order to get improved performance from a solar cell. Those important aspects are going to be discussed now.

Back Surface Reflectors (BSR): The performance of silicon solar cell is limited by much optical reflection of incident light on the cell thereby reducing optical absorption. Absorption of photons from incident sunlight depends on the absorption coefficient, which is high for short wavelengths and low for longer wavelengths. Therefore red and infrared light penetrate deeper into the silicon material and a big portion is scattered or absorbed at the rear side contact. Polishing and coating the rear side with aluminum (Al) metal or some other metal as reflector helps most of those longer wavelength lights which are not absorbed the first time to be reflected back in the material and absorbed on a second chance. These kinds of back surface reflectors (BSR) improve performance of thin cells.

Anti-Reflective Coating (ARC): The silicon surface reflects 35-50% of light incident on it [25] depending on wavelength. One of the technological measures that can be used to reduce those optical losses is to use an "antireflective" thin coating on the surface that is facing sun. This thin coating is usually silicon nitride (Si_3N_4), which is an optically denser material. Optimal thickness of Si_3N_4 enables lights of certain wavelength incident vertically on it to be extinguished completely via destructive interference causing minimal reflection.

Texturing: Aside from antireflective coating thickness optimization, another way to reduce reflection losses is to use textured surfaces. Surface texturing is achieved by creating topology of small densely packed tetrahedral grooves, V-grooves or random

pyramids [26] that acts as light traps on the solar cell's surface. When light gets incident on the surface, the reflection occurs in such an angle that it is deflected into a new point on the surface. Multiple interactions like this occur at the surface causing reduction in amount of light normally lost through reflection.

Combination of antireflection coating and texture can keep the reflection of the sunlight from the surface down to 3%, making the cell appear black ("black cell"). The textured surface also provides reduction in path length to the junction. This is beneficial for longer wavelength of light as it increases the longer wavelength collection efficiency. For thinner cells it is an important factor. It also increases radiation tolerance. As the bulk region diffusion length is reduced by the effects of radiation, the reduced effective path length enables a contoured surface device to maintain more of the lower wavelength response than a comparable smooth cell.

Minimization of shading from metal grid: Front side of a solar cell (emitter) created by diffusion process consists of three regions –

1) A shallow region created by extremely high dopant concentration above solid solubility limit which is called "dead region". This region has extremely short minority carrier lifetime.
2) A high field region maintained by the impurity profile.
3) A space charge region, which is the transition region between the emitter and the substrate. It has some uncompensated donor and acceptor (defects) sites.

The defect density decreases sharply going from the dead region to space charge region. Hence reduction of emitter thickness to reduce the dead region is desirable. But that would cause increase in lateral resistance, which could be compensated by increasing the

number of metal grid lines with finer features to draw more current. This would avoid any shading losses by keeping the active area of a solar cell (area that absorbs light) constant.

Charge Separation: Charge separation is caused by a driving force of charges which must be built into the device. There are many ways to provide a charge separation mechanism by variation in the electronic materials. The most basic principle for a conventional cell with an n-type emitter at the front and a p-type BSF at the back is to have top metal contact grid to provide low resistance for the electrons to flow, but block holes, and a bottom metal contact to provide easy path for holes and a barrier to electrons.

Reduction of Bulk Recombination: Minority carrier generated at the surface due to light action travels through the bulk of the substrate to be collected at the BSF region thereby generating current. In order for the minority carrier to travel through the substrate and not get recombined, the bulk material has to be as defect free as possible. It has been observed that the source for the defects in the bulk is a group of intrinsic thermal point defects (self-interstitial vacancies) which are present in silicon at increasing concentrations as temperature increases [27]. During the growth of high quality dislocation free silicon from the melt in Czochralsky (CZ) method, these thermal point defects supersaturate the silicon as it cools and then condenses to form micro-defects. The source of these defects is predominantly carbon coming from heating element, susceptor, and silicon feedstock. The other source of defects to some extent is oxygen originating from quartz crucible. That is why silicon obtained from Float Zone (FZ) process is preferable to boost device performance, as the defect levels as two orders of magnitude lower [28].

Surface passivation: In order to get high-efficiency solar cells reduction of carrier recombination is highly important. Exposed surfaces between metal gridlines at the top of the cell or the interface between the ohmic metal contacts and doped semiconductor have rather severe defects in a crystalline structure and are the sites of many allowed states within the forbidden energy gap in the silicon. Excellent surface passivation is achieved through the growth of good quality dielectric (e.g. SiO_2, Si_3N_4, Al_2O_3, etc.) or amorphous silicon (a-Si) which helps the cells to get to higher efficiency. Furthermore due to use of thinner and thinner silicon substrates in the present industry passivation of front and/or rear surface has become more necessary as it provides increased internal optical reflection, resulting in better light trapping.

Optimum doping: The doped regions need to have enough number of impurities to have good contact with low series resistance with the metal, so that fill factor improves. But having heavy doping might have detrimental effects on carrier mobility. This happens due to increased scattering of carriers which in result in hindrance in charge transport. Doped region using diffusion causes recombination which increases with increase in dopant density. Experimental data shows that for heavy diffusions most recombination occurs at the heavily diffused regions [29]. Typical metallurgical junctions are usually 0.25μm or less deep. But they can't be two shallow as it will increase the sheet resistance of the top layer and increase the dark current. On the other hand deeper junction is not efficient in collecting carriers excited near the surface, especially light from the shorter wavelength, which has higher absorption coefficient.

2.4 DESIGN OF A BIFACIAL SOLAR CELL

The structure of a conventional homojunction bifacial cell wouldn't be much different from conventional monofacial structure, excepting the rear surface would have metal grid pattern instead of covered wholly by metal. This is to facilitate light collection from rear side. The structure is shown in Fig. 2.8.

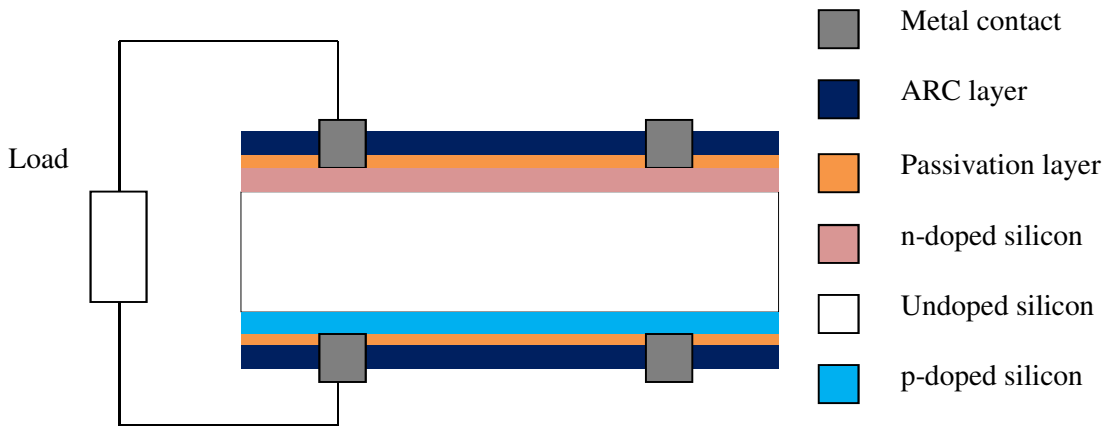

Figure 2.8: Structure of a conventional bifacial homojunction solar cell

The bifacial cell that we fabricated in this work does away with SiO_2 as passivation layer. Instead we use PECVD deposited Si_3N_4 to passivate the surface . This nitride layer acts as an ARC at the same time. It also helps in barrier to help selective growth of metal contact in our process.

Chapter 3: Simulation and Fabrication of a Bifacial Cell

In this chapter we present 2-D simulation of a bifacial solar cell with an n+pp+ structure with metal contacts on both sides. The simulation is carried out with the aid of simulator Sentaurus Device in the commercial semiconductor software package TCAD from Synopsys. In the simulation light collection is done from both sides independently. After that we describe our process for fabricating bifacial cells followed by some data we gathered from the devices we made in both CZ and FZ wafers. The data proves our technique is viable but all the processes used are still sub-optimal. There is a lot of room for improvement to increase the efficiencies on both sides of the cell.

3.1 SIMULATION OF A BIFACIAL CELL:

Sentaurus Device is a numerical semiconductor device simulator that is capable of simulating the electrical, thermal, and optical characteristics of various devices in 1-D, 2-D, and 3-D domain. In this thesis we use Sentaurus Device to simulate a silicon-based simple bifacial structure to have a better understanding of the practical behavior of devices and find out what are the optimum values of the device parameters that one needs to get in order to fabricate high efficiency cells.

The general process flow for simulating a device in Sentaurus Device is given below.

1) **Build the device structure:** This could be done by using directly drawing the device structure on Sentaurus Structure Editor Tool, or one can write down the structure using “scheme” command language and make files with extensions “_dvs.cmd” and “_fps.tdr”.

2) **Build the meshes:** This is established in the files with extension "_msh.tdr". These files contain information regarding device geometry, including the region and material specifications, contact and mesh definitions, including the location of all the discrete mesh points, also called nodes or vertices They also contain field values in the device, for example, the doping-profile distributions inside a device on a given Mesh. The mesh file can be generated automatically while running Sentaurus structure.
3) **Simulate the device:** This is done with some input files containing the information discussed in previous two points, fed to Sentaurus Device Tool. This tool is a standalone simulation program that behaves as a number crunching program.
4) **Output the results:** The simulated device performance results could be seen using Tecplot. This is a program which used for 2-D simulation.

The process flow diagram is shown in Fig 3.1.

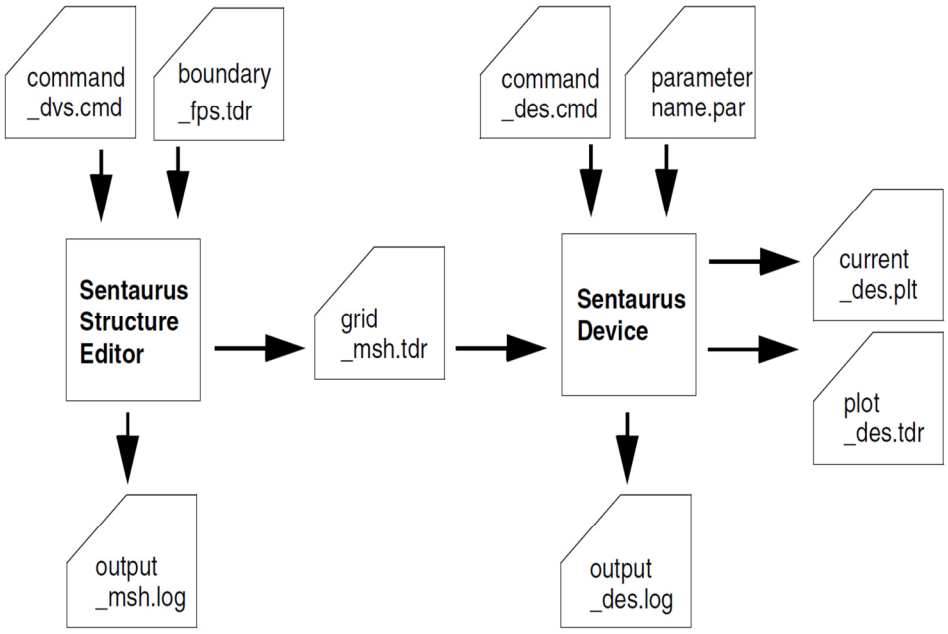

Figure 3.1: Typical tool flow for simulation using Sentaurus Device [30**]**

We start out by writing the command file (.cmd) to and run it using structure editor to generate the grid structure and mesh refinements.

The specifics about the device structure, doping (e.g substrate thickness, substrate width, junction depths, substrate doping concentration, etc.) are given in Table 3.1.

Information related device structure and doping	Values
Substrate thickness	200µm
Substrate width	1000µm
Substrate length	1µm (default value)
Si_3N_4 thickness	80 nm
Top/Bottom contact width	200µm
Pitch (distance between two metal contacts)	400µm
Top/Bottom junction depth	Varied from 1µm to 0.25µm
Substrate doping concentration	1e16 atoms/cm^3
N-type emitter doping concentration	Varied from 1e20 to 1e19 atoms/cm^3
P-type BSF/emitter doping concentration	Varied from 1e20 to 1e19 atoms/cm^3

Table 3.1: Structure parameter values used in the simulation

We checked the device geometry, doping profiles, and mesh refinements for any kind of errors in design using Tecplot. A screenshot of the designed device on Tecplot [31] window is shown in Fig. 3.2.

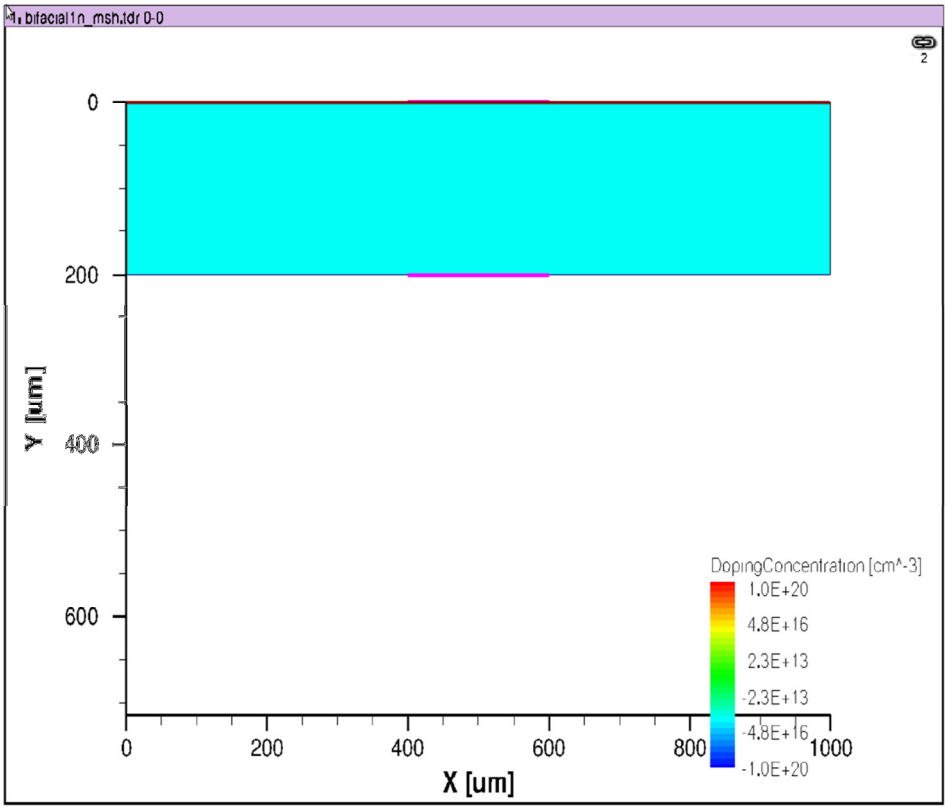

Figure 3.2: Screenshot of the 2-D structure of the bifacial cell on Tecplot window

After the structure editor creates the grid file with extension "_msh.tdr, it is used as the essential input file for Sentaurus Device to perform the simulation. There is another optional parameter file (.par) for input, which specifies user defined model parameters to override the built-in defaults, but we have used default model parameter values for our materials, and hence didn't use the parameter file.

A Sentaurus Device simulation produces several output files:

1) **current file (_des.plt):** contains the electrical output data such as currents, voltages, and charges at each of the contacts.
2) **plot file (_des.tdr):** contains the final spatial solution for all variables of the structure, such as the electron distribution at specific bias point.

3) **log file (_des.log):** contains all the informative texts that it has downloaded during a run, such as physical model activated and parameter values used, and error messages.

The input and output file names are defined in the command file (_des.cmd). This command file [30] typically consists of several sections: File, Electrode, Physics, Math, Solve and Plot, with each section executing a relatively independent function.

1) **File section:** It defines all input and output files of the simulation.
2) **Electrode section:** It defines the electrical contacts of the device, together with their initial bias conditions and special boundary condition (if any).
3) **Physics section:** All the physical models to be used in the simulation are declared here. They can be defined globally or material wise. In our case, we defined them globally. We used carrier mobility model, carrier optical generation model, carrier recombination model (SRH and Auger), carrier excitation model, etc. We have used the parameters for the models with their default values.
4) **Math section:** It is used to control the numeric solvers in the simulation.
5) **Solve section:** The Solve section consists of a series of simulation commands to be performed that are activated sequentially. The specified command sequence instructs the simulator as to which task must be solved and how. The Solve section is the only section in which the order of commands and their hierarchy are important.
6) **Plot section:** It is used to specify the solution variables that are to be saved in the Plot file (named in the File section).

One more important thing we considered is the optical generation. An AM1.5G solar spectrum is used in all simulations of the current density-voltage (J-V) curve under standard one-sun illumination conditions at intensity of 100 mW/cm^2. Each surface was independently illuminated in the simulation.

We could see the simulated illumination J-V curve using Inspect [32]. Screenshot for one such curve is shown in fig 3.3.

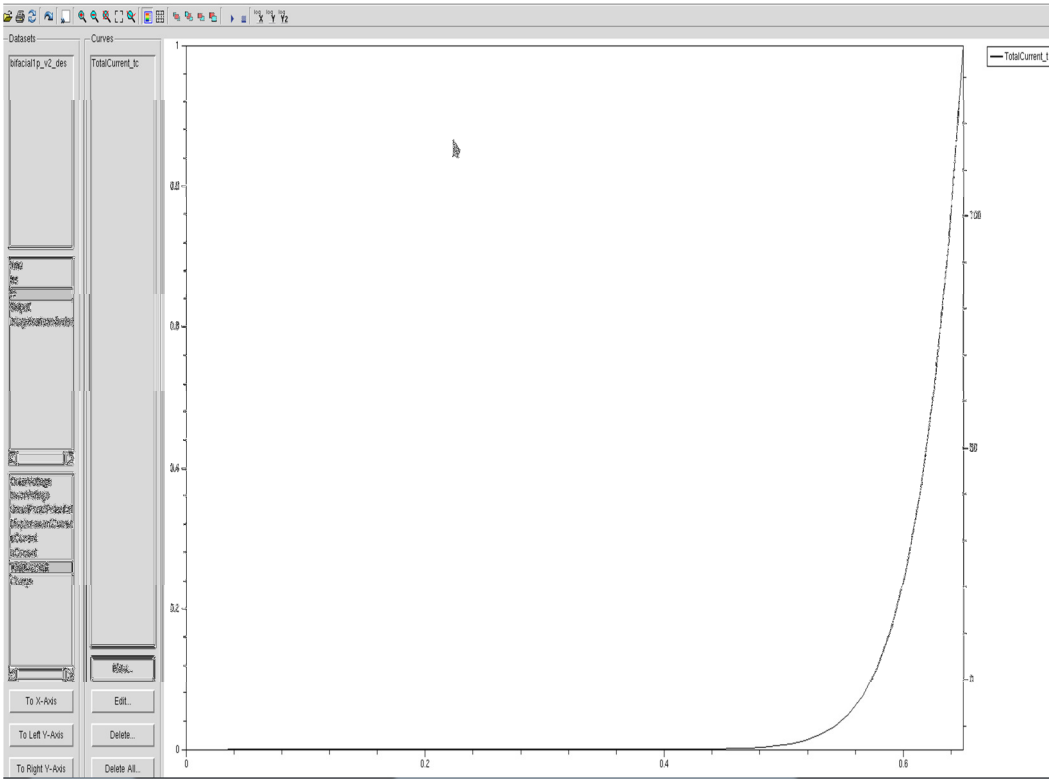

Figure 3.3: Screenshot of simulated J-V curve for the p-type side on Inspect window

1st Pass Simulation: In our first pass of simulation we have used default parameter values for all the models of physics we invoked in our simulation. Those

parameters are far from the ideal, and hence simulated performance after running the code was sub-optimal. However, since our processes in the experimental section themselves are far from optimized, we wanted see with right kind of metallization, but with sub-par quality material (low minority carrier lifetime), and un-optimized passivation (high surface recombination velocity), what the device efficiency would be like. For example, electron and hole lifetimes are in few microseconds range, whereas they should be 100s of microseconds or even a millisecond range for a solar grade material which we haven't used in our first simulation. Again, for Shockley-Read-Hall (SRH) recombination model we have used the default values of 10^3 cm/s for the surface recombination velocity, whereas for a well passivated surface it should be 10cm/s or even less than that. Since our passivated layer is un-optimized, for now we wanted to see the simulation data with such high values. The junction depth used is 1μm and the doping density at both the surfaces is 1e20 atoms/cm^3.

After exporting the data from curves we observed from Inspect, the performance parameter values are given in Table 3.2.

Sun facing side	V_{OC} (V)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
n-type	0.585	23.169	82.358	11.163
p-type	0.572	15.127	82.439	7.133

Table 3.2: 1st pass simulation results

2nd Pass Simulation: These numbers could be further improved by reducing the junction depth to decrease recombination on both surfaces. The doping density is also reduced for the same reason. The new values for junction depth and doping densities are 0.25µm and 1e19 atoms/cm^3 respectively. The performance parameter values are given in Table 3.3.

Sun facing side	V_{OC} (V)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
n-type	0.586	25.006	81.318	11.916
p-type	0.574	15.059	81.495	7.044

Table 3.3: 2nd pass simulation results

The simulation clearly shows some incremental improvement in V_{OC}, J_{SC}, and Efficiency on the n-side. The Fill Factor actually went down for both the surfaces, probably due to added series resistance due to shallower junctions with lower doping density. On the p-type side current decreased, and so did the Efficiency. Overall the shallower junction and lower doping density showed minor improvement because we are still severely limited in our performance by lack of proper passivation.

3rd Pass Simulation: We reduced the minority carrier surface recombination velocity S_{front} (cm/s) at the nitride/silicon interface on both surfaces to simulate a better passivated surface to reduce SRH recombination. The performance parameter values are given in Table 3.4.

Sun facing side	V_{OC} (V)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
n-type	0.651	26.318	83.519	14.309
p-type	0.665	25.368	83.824	14.141

Table 3.4: 3rd pass simulation results

The results show significant change in performance. V_{OC} number shot up for both surfaces, although V_{OC} for the n-type side was lower than the p-type side. This could be attributed to lower absorption capability of n-type emitter in lower wavelength (blue light) region of the solar spectrum. Further improvement could be made in the simulated performance with more optimization.

3.2 FABRICATION AND MEASUREMENT OF BIFACIAL CELL

Both monofacial and bifacial cells are processed first on 500µm thick CZ wafer pieces with 1-10 Ω-cm resistivity. Then to see the effect of using thinner wafer and switching material with better minority carrier lifetime we processed our cells on 200µm thick float zone wafer pieces with very high resistivity (3k-5k Ω-cm). Minority carrier spec is not provided for either type of wafers by the vendor. Metal grid used on both surfaces of the surfaces is the same. Monofacial cell does not have grid pattern at the back side instead it is wholly covered by metal.

1. We start with a bare silicon wafer piece, and subject it to standard wet clean like piranha (1 part hydrogen peroxide and 2 parts sulfuric acid) followed by a dip in 1% hydrofluoric acid (HF) solution to dewet the silicon surfaces.
2. Then we deposit silicon dioxide (SiO_2) using PECVD method as a diffusion barrier on one side.
3. We introduce this piece of wafer in a high temperature furnace where Boron Nitride wafers are used as p-type planar source for silicon diffusion to dope the bare silicon side of the wafers. This is done at 1000°C for 30 min, typically in a nitrogen ambience.
4. During the boron deposition cycle a thin, metallic compound forms under the deposited glassy film. This layer is boron silicide and is beneficial for silicon processing because it produces uniform sheet resistivity in the doped silicon slices, and it can be used as a limited source of boron in certain drive cycles. However, this compound is removed so that it does not become a problem later. That is why the piece after doping process is cleaned again using standard wet processes and introduced to another high temperature furnace to put it through 850°C for 25 minutes in steam ambient to oxidize a thin layer of this boron silicide phase. The new oxide layer is then masked with photoresist and the PECVD oxide from the other side is etched off using buffered oxide etch (BOE). Now, the steam oxide grown, will act as a diffusion barrier for our next dopant diffusion process.
5. After wet cleaning the piece again, it is introduced in $POCl_3$ diffusion furnace at 840°C for 40 minutes. This would grow a doped oxide layer on the exposed

silicon surface. Now we etch off the oxide from both sides of the wafers using BOE.

6. Now we have a silicon substrate that has n-type doping with sheet resistance of 38 Ω/□ on one side and p-type doping with sheet resistance of 33 Ω/□ on the other side. We use shadow mask to deposit silicon nitride by PECVD method to have metal contact openings with a grid structure with a central bus bar. This is done on each surface one at a time for bifacial cell. During deposition no alignment is needed for the patterns on either surface. After the deposition is completed we anneal the sample in a furnace in N_2 ambience at 600C to make the nitride denser in quality.
7. The sample is deglazed using BOE. The samples are then immediately put into a mixture of $PdCl_2$ and BOE. $PdCl_2$ comes from a solution called SOLUTION B from Transene Company, Inc [33]. This is described as a sensitizer and conditioner used in room temperature metallization scheme. In this process, palladium displaces a single atomic layer of silicon with a single atomic layer of palladium, forming an ideal nucleation layer for the subsequent nickel plating. This step is necessary to grow a seed layer for the nickel electroplating that is required to form metal contacts. Nickel can be directly electroplated on highly doped silicon surface. However, some researchers have reported the formation of a thin silicon dioxide film growth between the Si and nickel layer during plating and thought to be formed due to chemical attack in the bath [34]. Such a SiO_2 film, separating the metal from the silicon, would introduce abnormally high contact resistance in the finished solar cell. The incorporation of an immersion

palladium plating prior to plating nickel has proved to be beneficial to facilitate nucleation during the nickel plating process and thereby improve coverage and adherence to the silicon [35]

8. In the final step the sample was subjected to plating of nickel on both sides simultaneously to form metal contacts for the cell.

The process for fabrication of the cell is shown in Fig. 3.4(a)-(i).

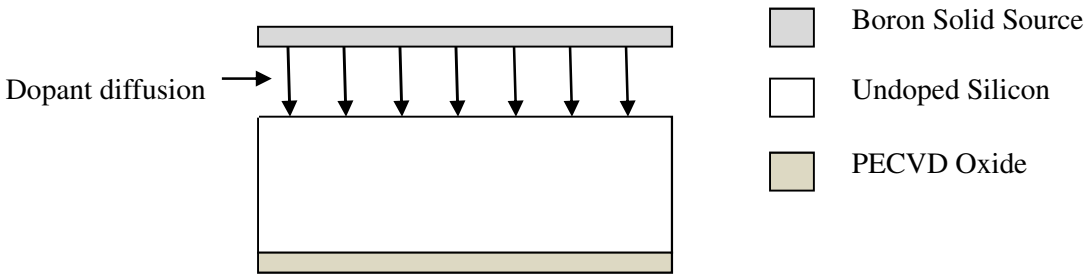

Figure 3.4(a): Dopant diffusion for global BSF/backside emitter using boron solid source.

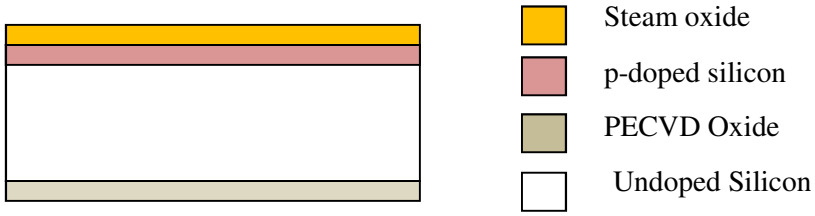

Figure 3.4(b): Steam oxide growth to remove defective boron silicide.

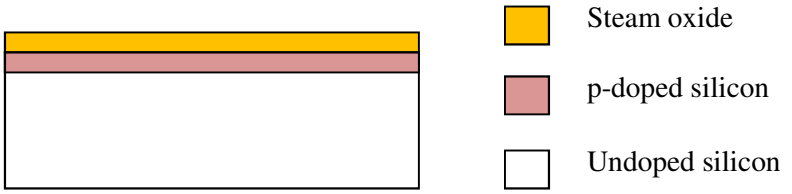

Figure 3.4(c): Stripping the PECVD oxide to prepare it for n-type doping process.

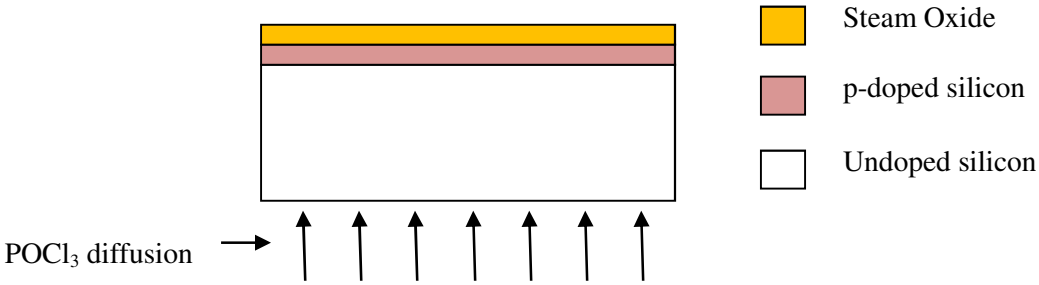

Figure 3.4(d): $POCl_3$ diffusion for global n-type emitter.

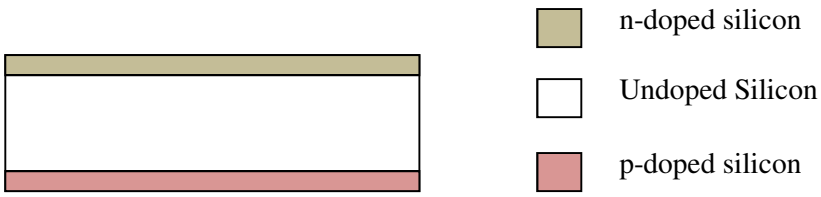

Figure 3.4(e): Deglazing of the sample using BOE.

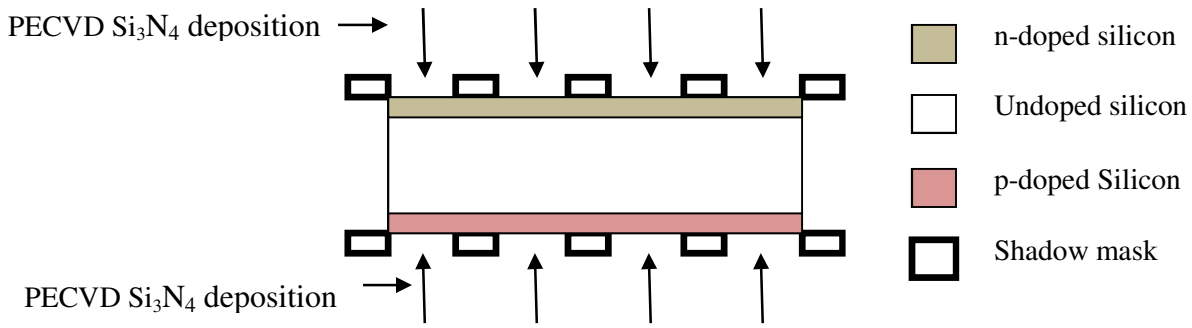

Figure 3.4(f): Deposition of Si_3N_4 using PECVD through a shadow mask.

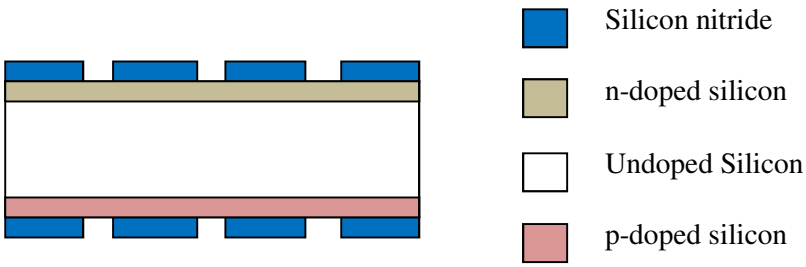

Figure 3.4(g): Si_3N_4 patterning is done for metal contact openings at the same time as deposition rendering optical lithography or any alignments unnecessary.

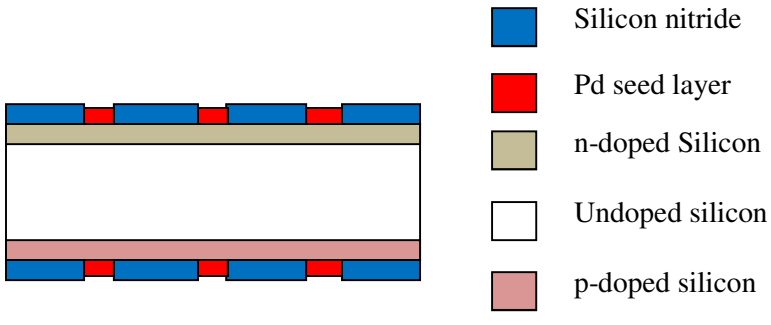

Figure 3.4(h): Pd seed layer is grown on both sides simultaneously.

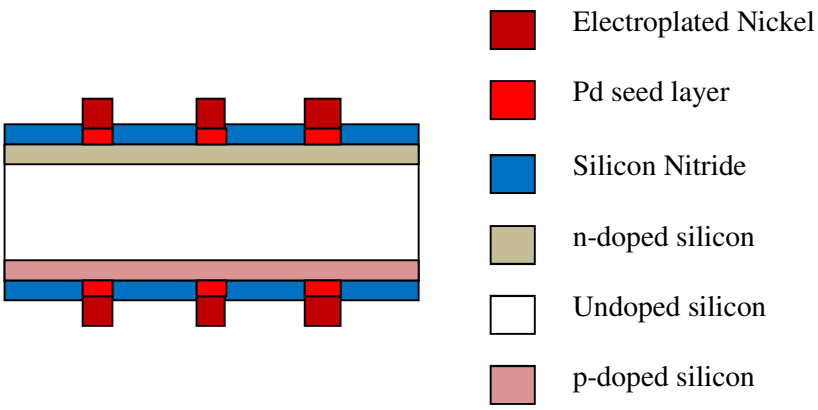

Figure 3.4(i): Nickel is electroplated on both sides simultaneously.

After finishing the processing to complete the cell measurements are taken for CZ wafers on both the n-type side and p-type side facing the sun simulator independently. Measurements are taken under AM1.5 spectra. The current versus voltage (I-V) curve is shown in fig. The V_{OC}, J_{SC}, Fill Factor (FF), and Efficiency (η) numbers are given in table 3.5.

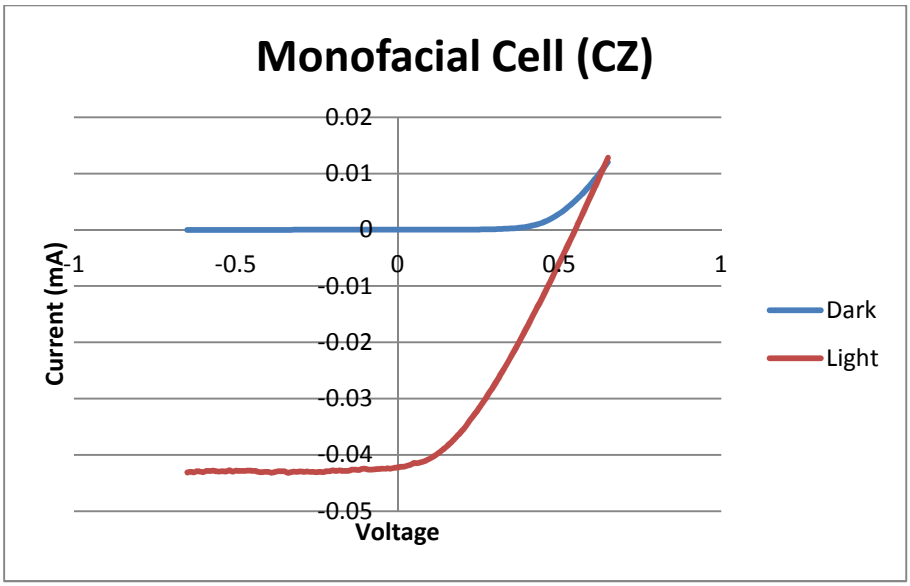

Figure 3.5: I-V curve for fabricated monofacial cell (CZ) under AM1.5G spectra

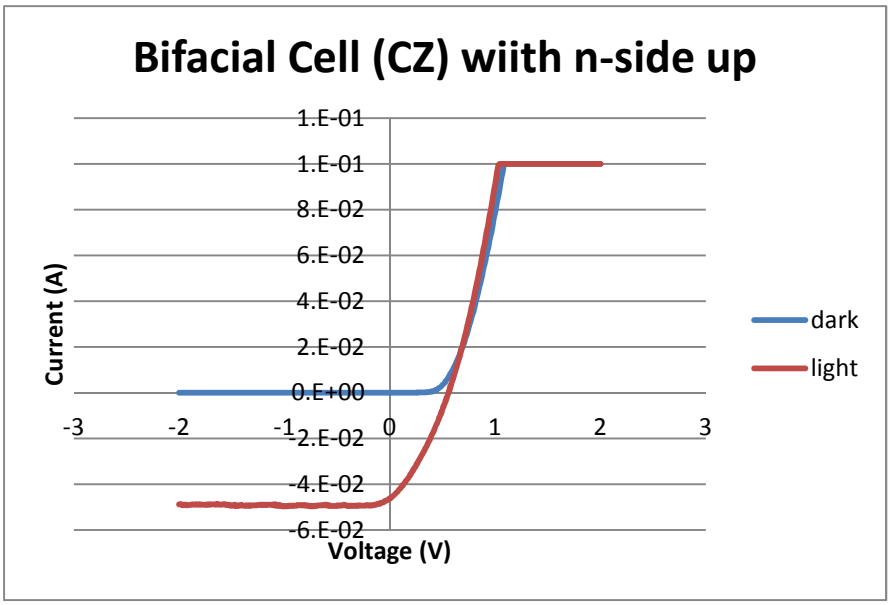

Figure 3.6: I-V curve for n-type side of fabricated bifacial cell (CZ) under AM1.5G spectra

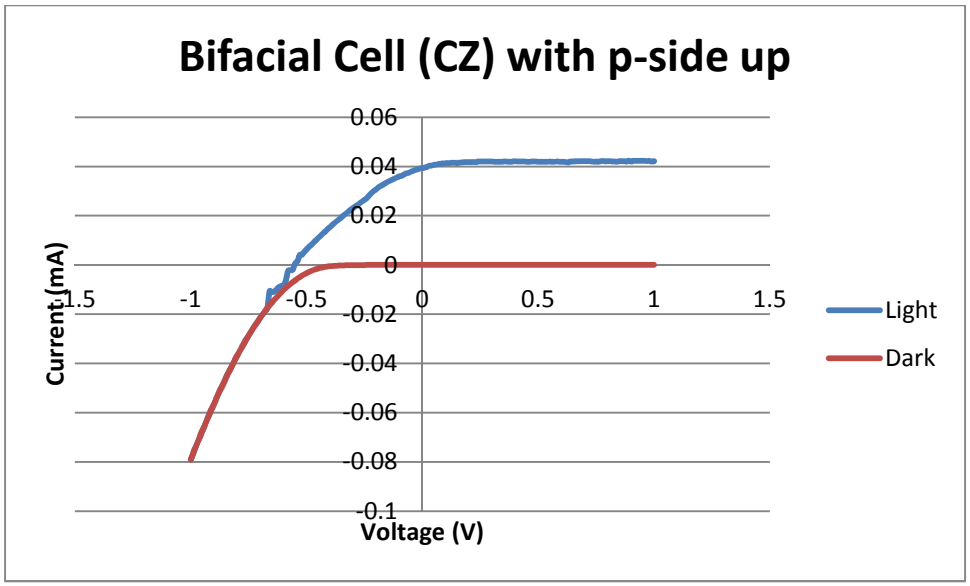

Figure 3.7: I-V curve for p-type side of fabricated bifacial cell (CZ) under AM1.5G spectra

Sun facing side	V_{OC} (V)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
n-type emitter side of monofacial cell (3.6cm^2 area)	0.548	11.711	35.577	2.286
n-type side of bifacial cell (3.6cm^2 area)	0.556	12.817	32.257	2.301
p-type side of bifacial cell (3.6cm^2 area)	0.564	10.928	31.273	1.930

Table 3.5: Experimental results from CZ wafers

The results clearly show an issue with metallization scheme. The metal coverage is not uniform enough to draw current from everywhere efficiently. That is why Fill Factor numbers are so low. The reason for such non-uniformity can be attributed to electroplating a large area of metal grid. The cathode contact to the grid gets metal plated at the very beginning, and from there on due to lateral plating the metal coverage expands. Therefor larger the area, less electroplated metal will be at places far away from the cathode contact. It seems, one obvious way to solve this problem would be to plate for a longer time. However, longer plating time does pose a problem. It will create different plated metal thickness in different areas. The vicinity of cathode contact to metal grid region would plate so much that it would exceed beyond tolerance limit for aspect ratio for metal plating, thereby causing peeling off of the metal. Therefore one quick fix to this problem is to try to electroplate on smaller areas. This ploy is adopted in case of the cells made on FZ wafer pieces. However, for large area cells we need to have a different plating scheme. One way to improve electroplating for large area samples would be to use multiple cathode contact points.

We completed making both monofacial and bifacial solar cells on FZ wafer pieces. Cell measurements are taken for CZ wafers on both the n-type side and p-type side facing the sun simulator independently. Measurements are taken under AM1.5 spectra. The current versus voltage (I-V) curve is shown in fig. The V_{OC}, J_{SC}, Fill Factor (FF), and Efficiency (η) numbers are given in table 3.6.

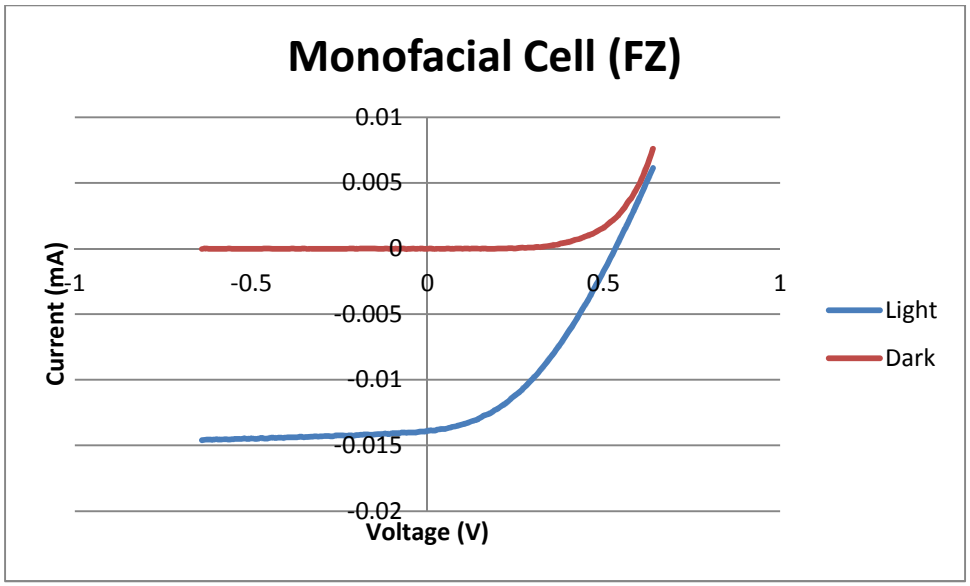

Figure 3.8: I-V curve for fabricated monofacial cell (FZ) under AM1.5G spectra

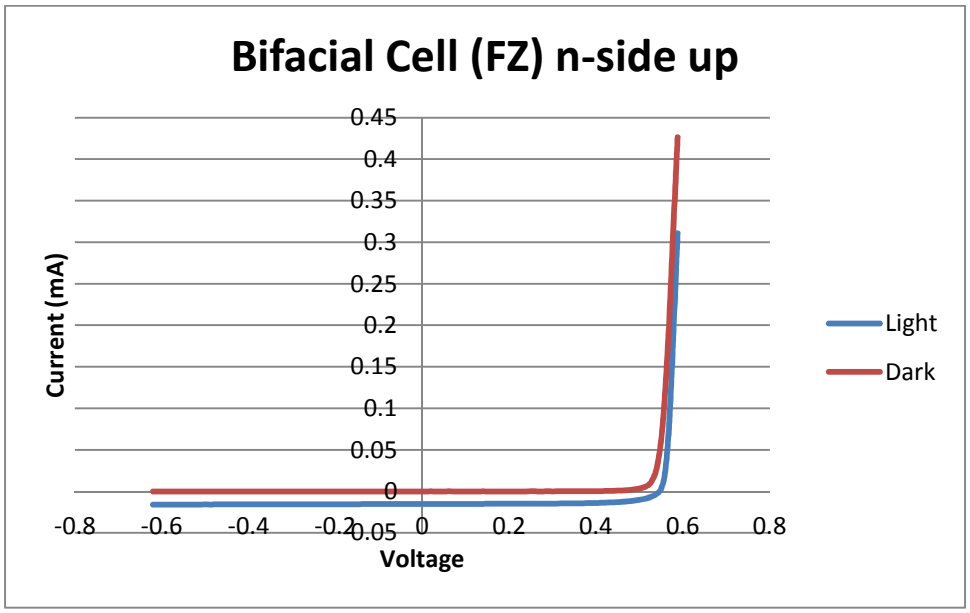

Figure 3.9: I-V curve for n-type side of fabricated bifacial cell (FZ) under AM1.5G spectra

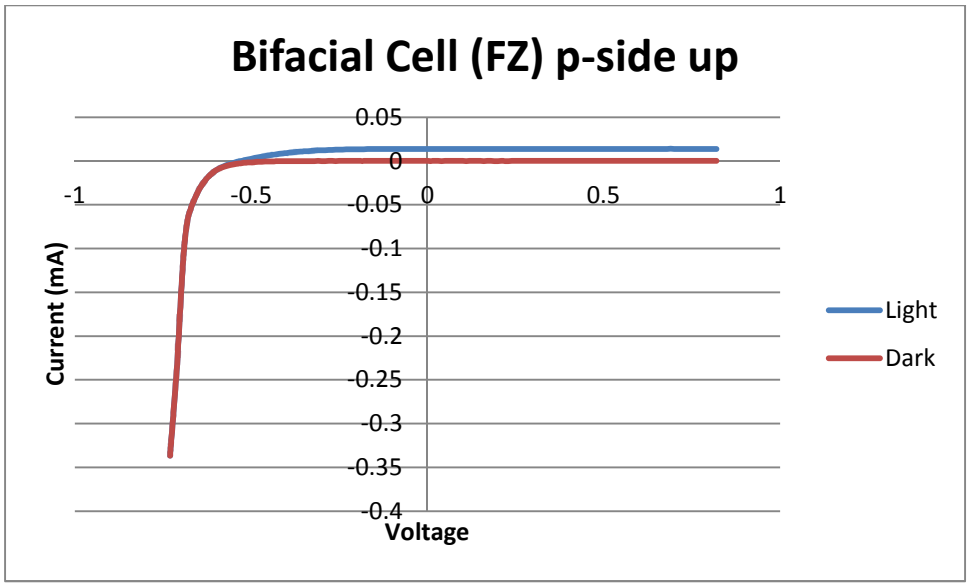

Figure 3.10: I-V curve for p-type side of fabricated bifacial cell (FZ) under AM1.5G spectra

Sun facing side	V_{OC} (V)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
n-type emitter side of monofacial cell (0.8cm^2 area)	0.533	17.375	40.142	3.715
n-type side of bifacial cell (0.7cm^2 area)	0.544	21.778	69.808	8.273
p-type side of bifacial cell (0.7cm^2 area)	0.530	19.525	53.311	5.516

Table 3.6: Experimental results from FZ wafers

Monofacial cell measured has lower efficiency compared to either of the sides of the bifacial counterpart. This is because the nucleation layer at the p-type side is not very uniform due to greater coverage required in the entire rear surface, thereby having poor quality nickel plating for the BSF contact.

The performance indicating numbers are far below their potential limits. V_{OC} numbers are low, predictably because the passivation provided by the PECVD S_3N_4 is not optimum quality. Current density is low probably because of we haven't used the right metal grid pattern resulting in shading related current loss, and the metallization itself wasn't very uniform everywhere, thereby not being able to draw current to its fullest capacity. Shading and non-uniform metallization related loss, combined with the fact that we have high resistivity (3k-5k Ω-cm) base region contributing in high series resistance, are bringing down the fill factor. During measurement due to the probe bar casting shadow on the cell we lost some current there. And all of these effects aggregated is causing lower efficiency numbers.

The measurement data shown here is for cells facing directly at sun simulator, whereas in real world the cells/panels have to be placed at an angle facing the sun. Due to that angular placement the efficiency numbers on either side might go down, but the combined efficiency for bifacial cells would still be greater than monofacial cells by an significant amount.

Chapter 4: Study on Effects of Buried Contact in Device Design

In this chapter, we studied the effect of incorporating buried contact in the device design. We have fabricated monofacial cells with help of conventional optical lithography, and studied effects of having different groove depths on V_{OC}, I_{SC}, fill factor, and efficiency numbers. The micro-trenches for buried metal contacts are achieved by doing chemical etching using potassium hydroxide (KOH).

Normally, in a solar cell without grooves, one of the key deterrents to efficiency result from the low height to width metal contact ratios and the relatively high reflective losses due to surface metallization. However, the buried solar cell contact design fixes many of these problems significantly. With the buried contact design, a much larger front side metallization can be done with minimal front side reflective losses. By burying the front side metal deep into the silicon substrate, one can achieve a significantly higher height-width metal aspect ratio. This in turn allows much shorter diffusion lengths in order for the charge carriers to be collected. Therefore one can expect a much higher short circuit current than one could achieve without grooves. The metallization may realistically only be limited by the width of the groove itself. Another added benefit comes from the reduced reflective losses. In cells without grooves, the exposure of the front side to sunlight must inherently be offset by the front side metal contact. This in turn causes large reflective losses because of the reflective properties of the metal. However, in the grooved design, because the same amount of metal can be deposited with significantly less used front side area, the wafer is capable of absorbing much more light and therefore producing more current.

4.1 FABRICATION OF BURIED CONTACT SOLAR CELLS

The final device structure diagram (with grooves) is given in Fig. 4.1. Scanning Electron Microscope (SEM) images of the buried contacts are given in Fig. 4.2(a)-(b). The process flow is presented in Table 4.1.

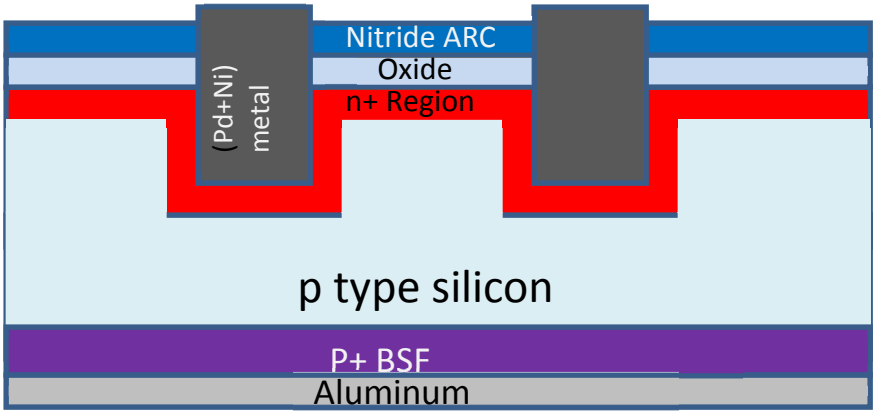

Figure 4.1 Cross-sectional diagram of our buried contact monofacial solar cell

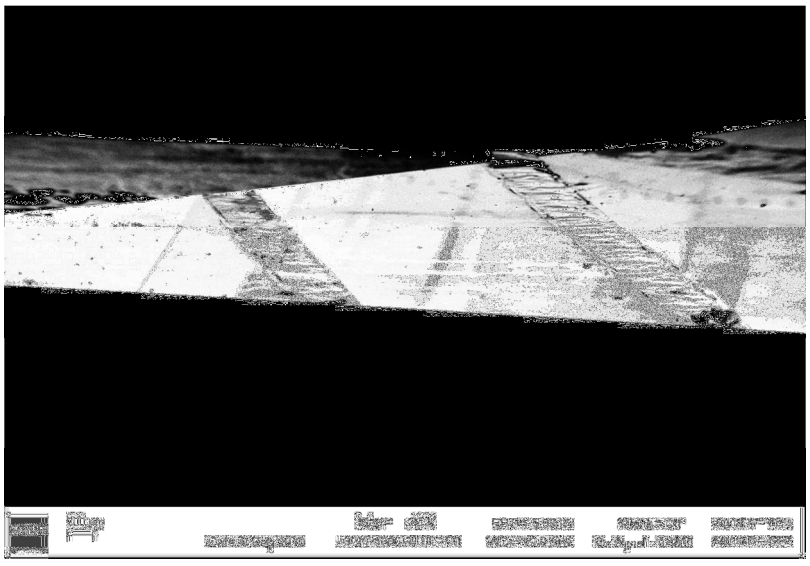

Figure 4.3(a) SEM image of surface of cell showing metal fingers

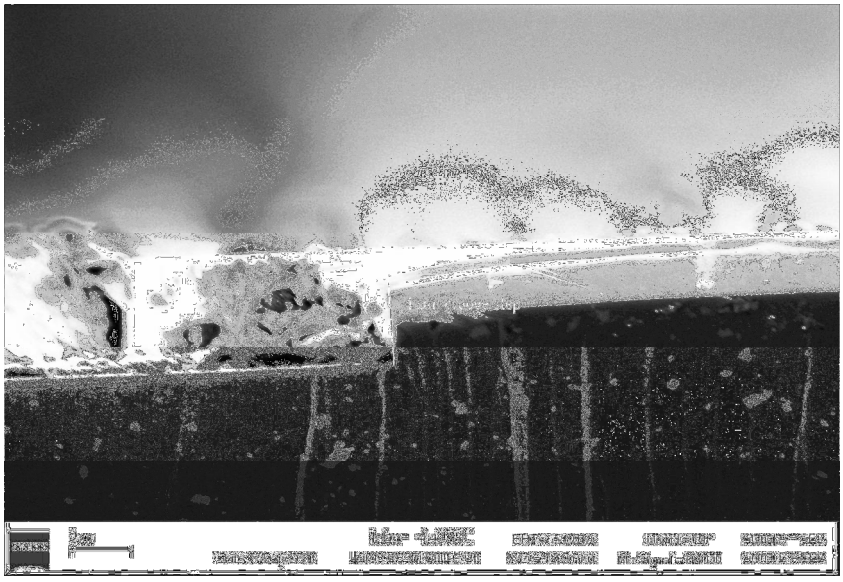

Figure 4.3(b) SEM image showing cross-sectional view of metal filled trenches

1. Grow steam oxide (~385nm) growth on cleaned wafers
2. Patterning using optical lithography, followed by wet etching using BOE
3. KOH etch to create the grooves selectively using steam oxide as hard mask
4. Etch off all of steam oxide using BOE (Our control sample didn't go through steps 1-4)
5. $POCl_3$ furnace and drive in to do a global doping
6. Grow dry thermal oxide for passivation
7. Grow LPCVD nitride with ~80nm thickness for ARC
8. Re-align to the trench pattern, followed by etch through nitride and oxide
9. e-Beam evaporation of Aluminum on the back side and firing for BSF and back contact
10. Front side metallization using palladium activation and electroplating

Table 4.1 Complete process flow for fabrication of our monofacial cells

4.2 RESULTS:

The cells are tested under solar simulator to study the effects on key cell parameters: V_{OC}, I_{SC}, fill factor and efficiency. We fabricated cells with grooves of 1, 2, 4, and 35 µm depths, and a control sample without any grooves.

The I-V curves for all of the devices are shown in Figs. 4.4-8. A summary of all the performance parameters are shown in Table 4.2.

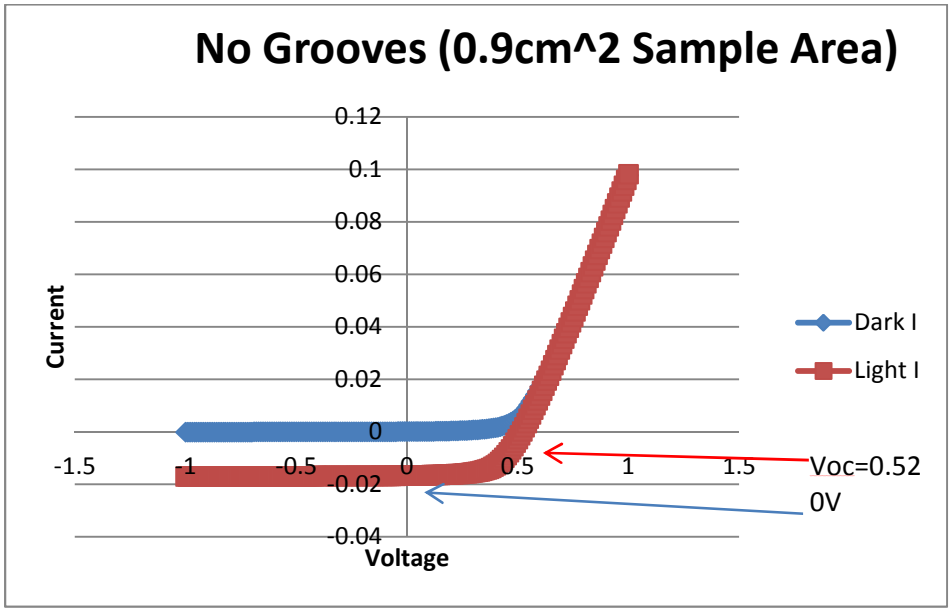

Figure 4.4 I-V curve for monofacial cell with no grooves

This is the "control" sample with no grooves, corresponding to a conventional solar cell. The metal fingers on the surface cause a certain level of "shadowing". Also, the photon absorption and carrier collection are both in the vertical direction. In the grooved contacts shown next, the photon absorption is vertical, but the carrier collection is partly "lateral" by the deep contacts, thus improving carrier collection efficiency.

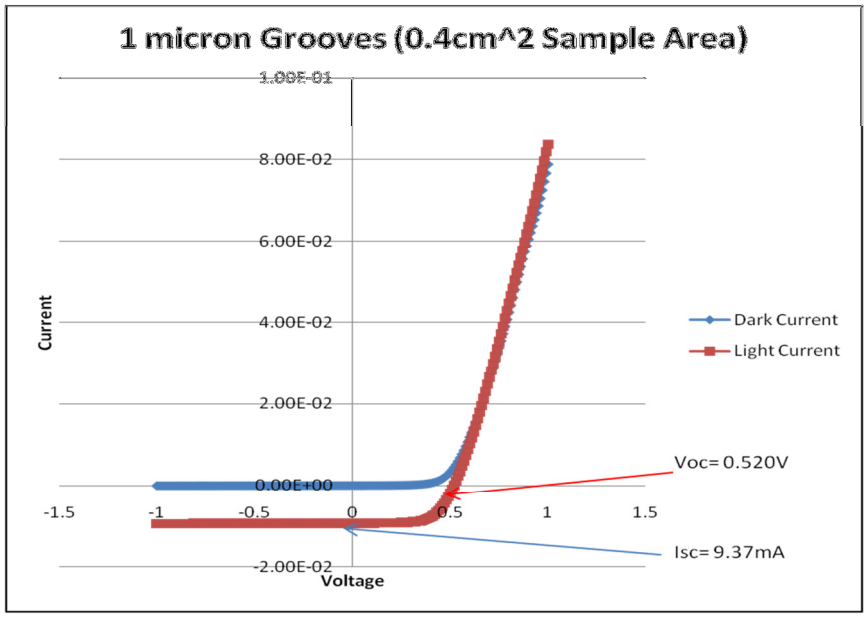

Figure 4.5 I-V curve for monofacial cell with 1µm groove

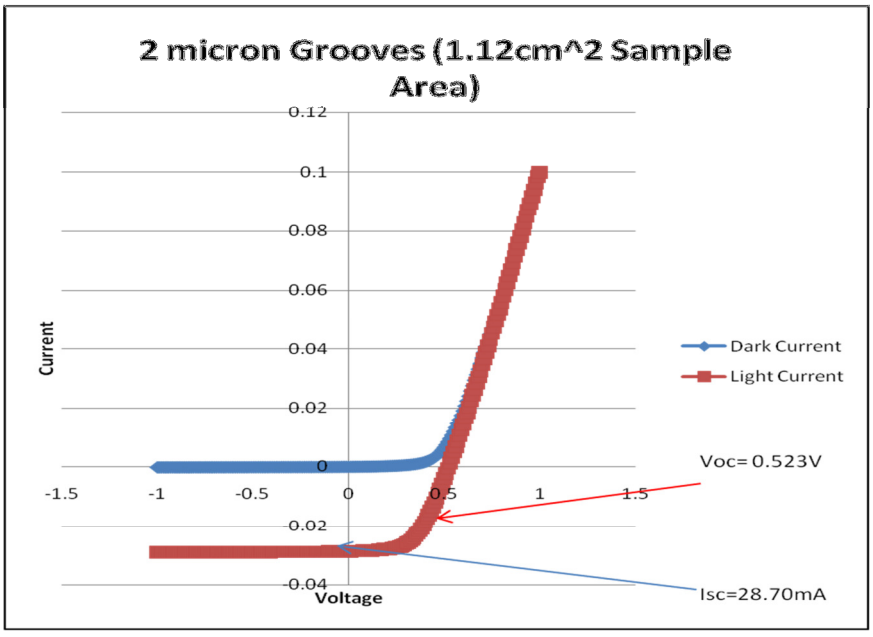

Figure 4.6 I-V curve for monofacial cell with 2µm groove

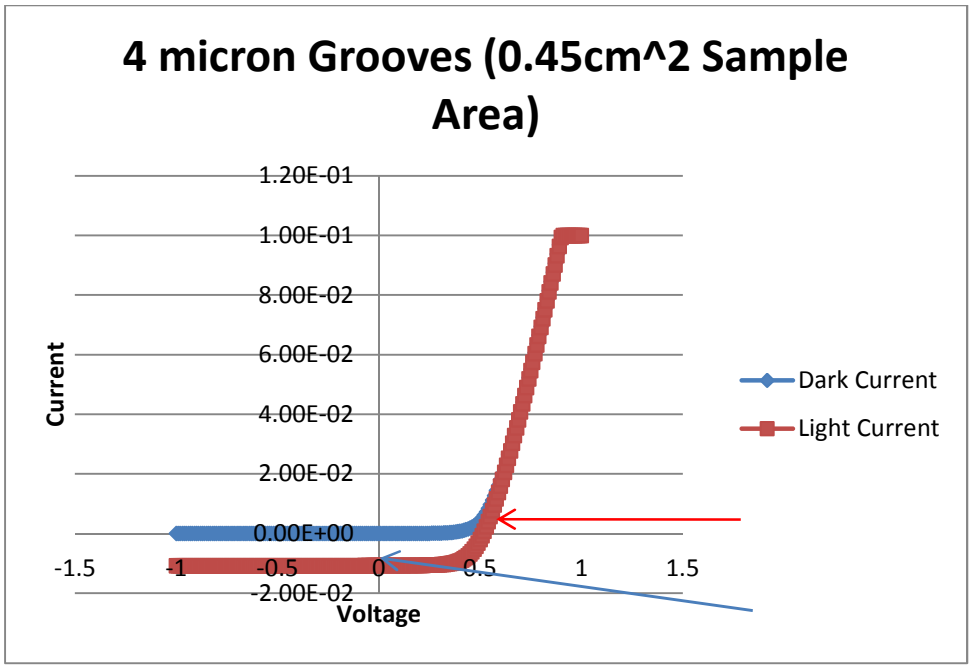

Figure 4.7 I-V curve for monofacial cell with 4μm groove

The 4 micron groove cell has the highest values of FF and efficiency. This cell has the optimal groove depth in terms of fill factor and efficiency. It can capture more photons than the planar or shallower groove cells, presumably because the "average" photon absorption depths are approximately 4 microns.

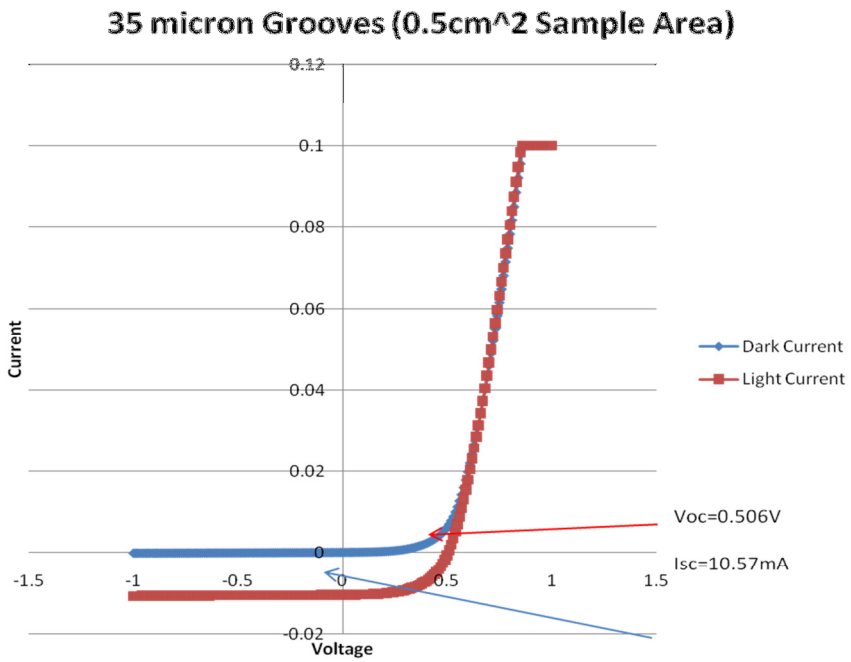

Figure 4.8 I-V curve for monofacial cell with 35µm groove

The cell with 35µm groove depth shows that making very deep grooves is counter-productive. Beyond a certain depth, there are very few photons to be collected, and the J_{SC} tends to level off. In fact, it actually drops slightly presumably because for these very deep grooves, the sidewalls got roughened, and the quality of metallization degraded. It also probably causes excessive shadowing of the photons by the metal groove contacts.

Wafer Number	Groove Depth	Efficiency	Fill Factor
1	0 micron	5.83 %	60.18%
2	1 micron	7.93%	65.16%
3	2 micron	7.32%	54.67%
4	4 micron	8.18%	66.36%
5	35 micron	5.97%	55.83%

Table 4.2: Summary of results from different cells

4.3 DISCUSSION

In this section we discuss the effects of different groove depths on different performance parameters.

Open Circuit Voltage:

The values of the open circuit voltage show an increasing trend from the 0 micron groove to the 2 micron grooved sample with a maximum of 0.523V. However, the values begin to decrease in all further samples ultimately deteriorating to 0.506V.

Ultimately, V_{OC} is affected by carrier recombination. And so, when looking at the I-V curve, despite the series resistance of the cell, the curve can still pass through the same V_{OC} point. Also, when further looking at the cell, the parasitic resistance voltage becomes a value of zero because V = IR, and in V_{OC}, I equals zero.

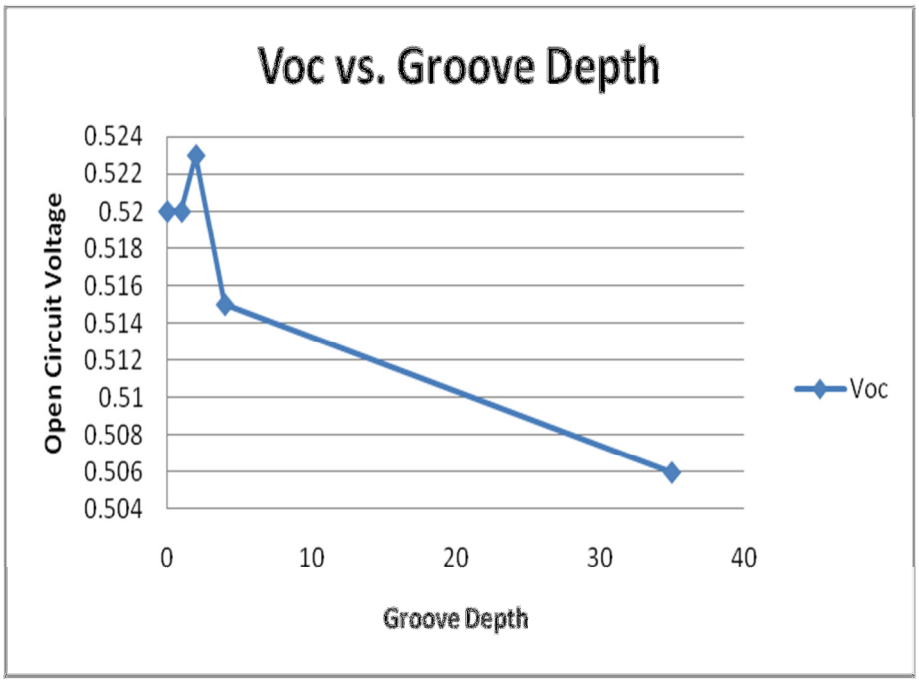

Figure 4.9 Open circuit voltage (V_{OC}) vs. groove depth in microns

The V_{OC} number shows a slight downward trend excepting 2um grooved sample as the groove depth increases. This is probably because for deeper trenches, there is more metal in contact with n+ emitter and acting as potential recombination sites. The anomaly in 2µm grooved sample might be just noise in measurement. Highest V_{OC} = 0.523V is found for 2µm.

Short Circuit Current:

I_{SC} is affected by carrier recombination also. Therefore when looking at the IV curve, the series resistance has minimal effects on the Short Circuit Current. In terms of the graph, one sees a vertical shift of the I_{SC} point as a function of the magnitude of series resistance. However, because the bulk of the series resistance comes from bad metal

contacts, the effects are second order mainly because recombination remains relatively constant.

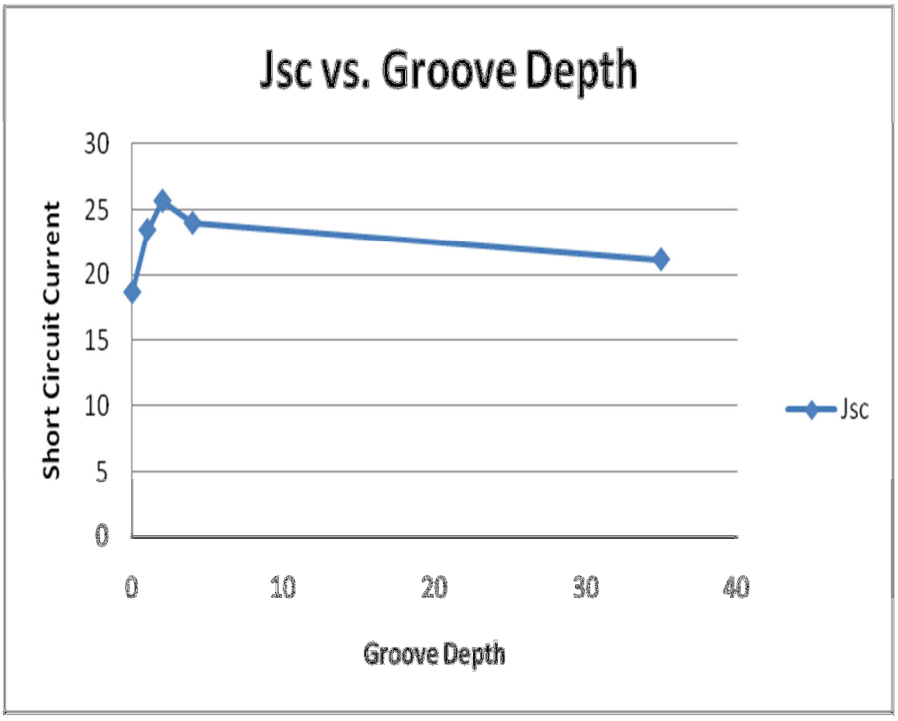

Figure 4.10 Short circuit current density (J_{SC}) vs. groove depth in microns

The J_{SC} numbers should show an increasing trend as the trenches become deeper, as the photo carriers generated closer to the sidewalls of the trenches have to travel less distance to the junction and should be easily collected. For groove depths beyond the "average" photon absorption depth, we expect the J_{SC} to level off because we do not have additional photo-generated carriers to be collected. But we didn't see a consistent trend beyond 2um grooved sample in our results. That might be because the metal may not

have grown everywhere in the trenches for deeper grooved samples. Highest J_{SC} = 25.63mA/cm^2 is found for a groove depth of 2 micron.

Fill Factor:

Fill factors generally showed an increasing trend from 0 to 4 microns. Afterwards, the 35 micron sample showed serious deterioration because of the roughness of the grooves. The fill factor magnitude can most directly be seen as a function of series resistance within the circuit diagram, and so, as series resistance goes up (bad metallization/bad contact between the silicon metal interfaces) fill factor goes down. One can see the effect of this directly on the I-V curve as the illuminated curve distance becomes smaller in the 4th quadrant. This is to say that the enclosed area becomes more triangular while the maximum power point remains relatively constant.

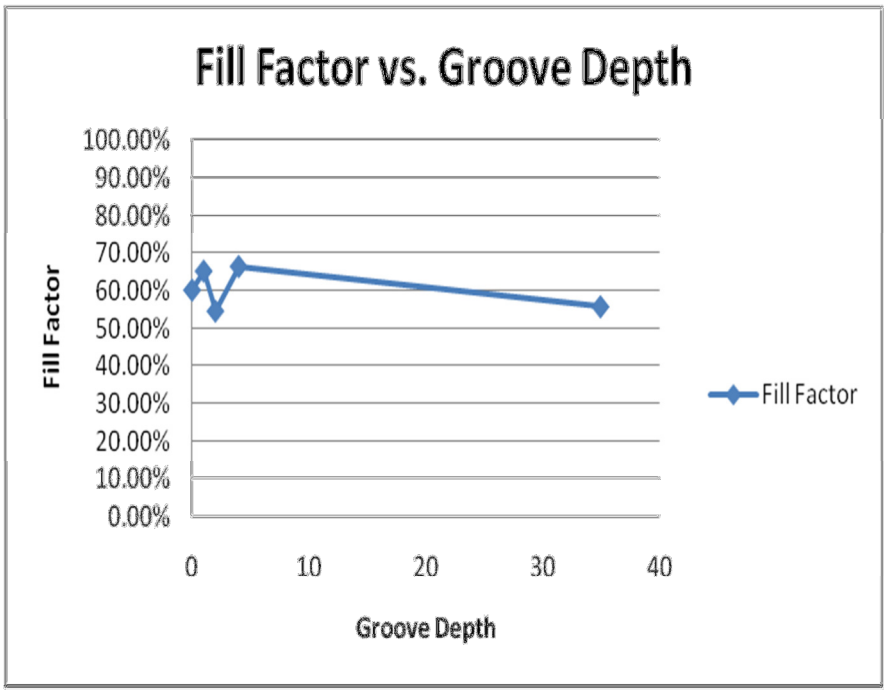

Figure 4.11 Fill factor (FF) vs. groove depth in microns

The metallization wasn't of the same quality for every groove depth. In general, deeper grooves are not electroplated as well as shallower ones. The range of fill factor is between 55% to 66%. A more optimum metallization process should be developed in future. Highest Fill Factor is 66.36% for 4μm grooves which appears to be the optimal groove depth.

Efficiency:

Based on the raw efficiency data, one can see a generally increasing trend from 0 to 4 micron grooves, while a noticeable decrease in efficiency in the 35 micron groove depth. It is clear that across all samples, implementing grooves resulted in increased efficiencies. The efficiency, as taken from the solar simulator can be most directly be affected by the fill factor, and so, the lower values are therefore merely a result of high series resistances. One can see a clear anomaly in the 2 micron grooved sample, this is because of very high series resistance and consequently because of non-uniform metallization of the grooves.

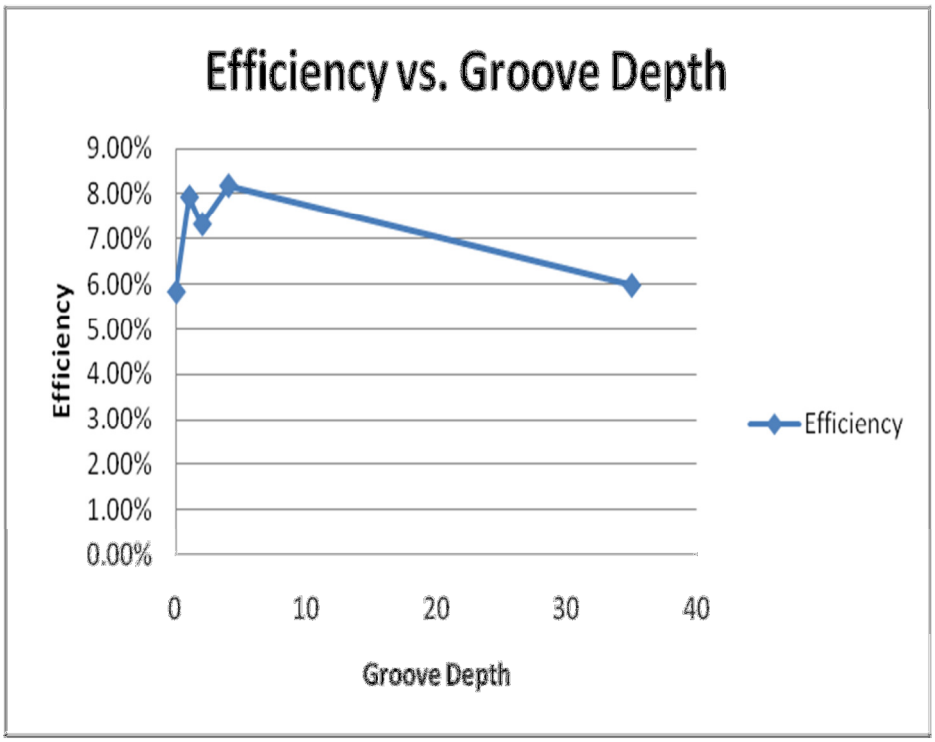

Fig. 4.12 Efficiency vs. groove depth in microns.

Trends generally show an increase in efficiency up to 4 microns. The extreme case in 35µm grooved sample (showing lower efficiency than the other grooved samples) proves that we cannot go on indefinitely increasing the groove depth**.** Highest Efficiency is 8.18% for 4 micron deep grooves, which appears to be the optimal depth.

It is clear that the buried contact solar cell design is beneficial towards improving solar cell efficiencies. We determined that there is an optimal groove depth, beyond which cell performance suffers due to poor metallization in these very deep grooves which leads to increased series resistance and degraded fill factors. We can use this optimal groove depth to include in our bifacial cell design for performance improvement.

Chapter 5: Future Work and Conclusion

5.1 FUTURE WORK

The results presented here are only preliminary results, to find a proof of concept. The devices made in this report are far from optimal. There could be several improvements that could be made to improve efficiency numbers.

1) **Texturing:** The samples fabricated here did not go through texturing process at any stage. If we introduce texturing via potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH), that might improve the light trapping in the cell. More light trapping should lead to more current generation. However, there is a downfall to have texture on the surface. Textured surface has effectively more area, hence would require better passivation scheme.
2) **Optimum doping:** Most industrial silicon solar cells are fabricated with a phosphorus-doped n+-emitter layer having a sheet resistance of 40-50 Ω/sq. The relatively low sheet resistance in conventional cells is chosen to promote a low-resistance ohmic contact between the contact metal and the emitter layer. However the heavy doping increases carrier recombination in the emitter layer [36] and increases the emitter surface recombination velocity [37]. An improvement to solar cell efficiency can be achieved if the emitter doping can be reduced to minimize recombination, without degrading the fill factor.

3) **Better quality of PECVD nitride:** The PECVD Si_3N_4 deposited in this process flow is not optimized to give best possible surface passivation. Optimized Si_3N_4 deposition should cause much less recombination at the surface and hence yield higher V_{OC} value. The nitride also changes color during the 1st step of metallization process due to the etching it goes through in presence of HF in the $PdCl_2$ solution. Even though extra thick nitride is deposited to offset that, and the sample has been annealed post deposition to make the nitride quality denser, the process still needs improvement so that we end up with a uniform, deep blue colored ARC. One way to overcome this challenge would be to use a better setup or a better recipe to deposit denser Si_3N_4, so that nitride becomes more dense and resistant towards HF etching. We used a more silicon rich recipe, i.e. higher silane (SiH_4) : ammonia (NH_3) ratio, and that deposited a nitride which was more resistant towards HF etching than silicon deficient nitrides.

4) **Selective Emitter:** Ideally, a lower junction depth for the emitter better would lead to better performance of a solar cell. But that would mean poor ohmic contact between metal and silicon causing high series resistance. That is why it is desirable to have very low doping on most of the surface with the exception of silicon underneath the metal contacts where the doping is heavier [38] [39]. The doping process could be done after the grid pattern is formed by depositing PECVD Si_3N_4, so that dopants could be locally diffused underneath the front contact or back contact or both, thereby forming a so-called *selective emitter*.

5) **Buried Contact:** We can make a selective chemical etching along the top and bottom surface of the substrate after Si_3N_4 deposition to remove silicon in order to create deep trenches. The metal grown on the surfaces of these grooves will maximize photo-carrier collection by reducing shading loss caused by tall metal grid on light collecting surface. If the concept of selective emitter is incorporated on it by doping the sidewalls of the trenches, we can achieve better photo-generated carrier collection efficiencies. These buried contact structure in these grooves will also reduce internal series resistance.

6) **Optimization of metallization method:** In the work presented by Guo et al. [40], metallization scheme similar to this work has been implemented on a double sided buried contact. In that report they have tried to sinter the Pd and Ni after they are deposited, with success in increasing the efficiency. We could try similar method to raise the efficiency numbers in our devices.

7) **Lower cell thickness and low resistivity of base:** Using thinner cells and increasing the base doping density will improve the base conductivity. Reduced resistivity through doping of the base will be helpful for improving series resistance; however, such material will have reduced lifetime and could be more susceptible to further reduction in lifetime if impurities are introduced during the cell process. Similarly, reduction in cell thickness will increase the collection of minority carriers photo-generated at the cell front and decrease series resistance. Both of these measures should increase fill factor in turn.

8) **Better measurement setup:** Finally the cell measurement has to be done in a simulated environment closer to real world situation where both monofacial cell and bifacial cell has to be mounted in an angle facing the sun. Then the performance measured simultaneously from both sides of a bifacial cell would represent the true effective efficiency. That effective efficiency has the potential to be greater than the monofacial cell efficiency by 25% to 80%.

5.2 CONCLUSION:

In this work we proposed a novel and very cost-effective method to fabricate bifacial solar cells. Bifacial cells collect sunlight from both faces, and hence have an obvious advantage over monofacial cells by occupying the same physical area and converting solar energy more efficiently. Despite this fact bifacial cells are not that popular simply because of the costs associated with them. These costs are related to both manufacturing of the actual cells and integration of modules/solar panels. The cost of manufacturing is higher than regular commodity cells due to the number of processing steps for fabrication being higher than their monofacial counterparts. The main reasons for that are:

1) Necessity of some kind of lithography step and or alignment to make the grid pattern on both sides separately, and
2) Metallization has to be done on both sides separately, one at a time.

The method proposed in this work gets rid of both of those necessities, because we use:

1) A shadow mask to deposit our passivation layer/ARC on both sides using PECVD, and

2) Simultaneously grow contact metal selectively on both surfaces.

This technique is simple and cost-effective enough to be potentially incorporated in a batch process in industry, thereby reducing the cost of manufacturing. In this thesis we have presented preliminary results from the cells fabricated using this technique with room for additional improvements. This demonstrates that this proposed method is viable to manufacture bifacial cells with reduced cost and relative ease.

We also studied effects of having buried contact by fabricating and measuring monofacial cells with different groove depths, and found an optimal depth value to get us maximum benefit of incorporating trenches in our design. We can use this optimum depth value in our device design for bifacial cells for future improvements.

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