The Dissertation Committee for Tackhwi Lee
certifies that this is the approved version of the following dissertation:

Device characterization and reliability of Dysprosium (Dy) incorporated HfO_2 CMOS devices and its application to high-k NAND flash memory

Committee:

Sanjay K. Banerjee, Supervisor

Leonard F. Register

Jack C. Lee

Ray Chen

John Ekerdt

Device characterization and reliability of Dysprosium (Dy) incorporated HfO_2 CMOS devices and its application to high-k NAND flash memory

by

Tackhwi Lee, B.S.; M.S.Phy.

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

December 2010

Dedication

To my loving wife, Jee, my family and GOD who loves me.

Acknowledgements

I would like to thank my advisor, Dr. Sanjay K. Banerjee, for his patience, persistent support and valuable advice. The experience and achievements that I obtained from his supervision during the completion of my doctoral studies enabled me to have confidence on a successful career in the semiconductor industry. I respect his character and mentorship greatly. Special thanks go to Dr. Jack C. Lee, Dr. L. Frank Register, Dr. Ray Chen, and Dr. John Ekerdt for serving on my dissertation committee. Dr. Jack C. Lee, in particular, has been kind enough in giving me the opportunity and the motivation to do research on the high-k dielectrics project.

I would like to thank the administrative and technical staff at the Microelectronics Research Center for their support: Jeannie Toll, Joyce Kokes, Bill Ostler, Jesse James, William Fordyce, James Hitzfelder, Steve Moore, Cheryl Ragland, Gerlinde Sehne, Marylene Palard. Without their help, I could not have finished my work at MER.

I would also like to thank my colleagues and fellow graduate students for their fellowship and collaborations. In addition to their friendship, I would like to thank them for their key contributions in my work. I would also like to thank the following current or former graduate students that have supported me with friendship, counsel, assistance, and resources: Shan Tang, Sachin Joshi, Yueran Liu, Se Hoon Lee, Feng Zhu, Manhong Zhang, Sergei. Koveshnikov, Se Jong Rhee, Hyoung-sub Kim, Injo Ok, Changhwan Choi, Chang Yong Kang, Seyoung Kim, Joenghyo Nah. During my internship at IBM T. J. Watson Research Center, I earned many precious experiences from Zhibin Ren, Issac Lauer, Jin Cai, Dechao Guo, Unoh Kwon, Masaharu Kobayashi, Takashi Ando and Kisik Choi. Their mentorship and deep discussions on the research problem made me step up to the next level. Especially, my manager, Dae-Gyu Park gave me great mentorship by

counseling and guiding me in the maze of industry research problems. Special thanks go to Tak H. Ning, IBM fellow at IBM T. J. Watson research center, for his valuable discussions and recommendations to my research. It was a great help for publishing my paper and gave me confidence in my problem-solving ability. I would also like to express my dearest appreciation for all the family at New Covenant Church. Their unstoppable prayer and fellowship were a great source of encouragement.

Finally, I wish to thank my family for their love and encouragement over the years. Particular thanks go to Jee Paik, my wife, who loved me and supported me through this whole process. Thank you for helping me improve my English. I cherish our times together.

This is for you, Lord. I will always remember the unfailing grace and unconditional love You have provided me throughout my life.

Device characterization and reliability of Dysprosium (Dy) incorporated HfO_2 CMOS devices and its application to high-k NAND flash memory

Publication No._____

Tackhwi Lee, Ph.D.

The University of Texas at Austin, 2010

Supervisor: Sanjay K. Banerjee

Dy-incorporated HfO_2 gate oxide with TaN gate electrode nMOS device has been developed for high performance CMOS applications in 22nm node technology. DyO /HfO bi-layer structure shows thin EOT with reduced leakage current and less charge trapping compared to HfO_2. Excellent electrical performance of the DyO-capped HfO_2 oxide n-MOSFET such as lower V_{TH}, higher drive current, and improved channel electron mobility are reported. DyO/HfO samples also show better immunity for V_{TH} instability and less severe charge trapping characteristics. Its charge trapping characteristics, conduction mechanisms and dielectric reliability have been investigated in this work. As an application to memory device, HfON charge trapping layered NAND flash memory is developed and characterized.

First, temperature-dependent Dy diffusion and the diffusion-driven Dy dipole formation process are discussed to clarify the origin of V_{TH} shift, and eventually modulate the effective work function in Dy-Hf-O/SiO_2 system. The Dy-induced dipoles are closely related to the Dy-silicate formation at the high-k/SiO_2 interfaces since the V_{FB} shift in Dy_2O_3 is caused by the dipole and coincides with the Dy-silicate formation. Dipole formation is a thermally activated process, and more dipoles are formed at a higher temperature with a given Dy content. The Dy-silicate related bonding structure at the interface is associated with the strength of the Dy dipole moment, and becomes dominant in controlling the V_{FB}/V_{TH} shift during high temperature annealing in the Dy-Hf-O/SiO_2 gate oxide system. Dy-induced dipole reduces the degradation of the electron mobility.

Second, to understand the reduced leakage current of the DyO/HfO sample, the effective barrier height of Dy_2O_3 was calculated from FN tunneling models, and the band diagram was estimated. The higher effective barrier height of Dy_2O_3, which is around 2.32 eV calculated from the F-N plot, accounts for the reduced leakage current in Dy incorporated HfO_2 nMOS devices. The lower barrier height of HfO_2 result in increased electron tunneling currents enhanced by the buildup of hole charges trapped in the oxide, which causes a severe increase of stress-induced leakage current (SILC), leading to oxide breakdown. However, the increased barrier height in Dy incorporated HfO_2 inhibits a further increase of the electron tunneling from the TaN gate, and trapped holes lessen the hole tunneling currents, resulting in a negligible SILC. The lower trap generation rate by the reduced hole trap density and the reduced hole tunneling of the Dy-doped HfO_2

dielectric demonstrates the high dielectric breakdown strength by weakening the charge trapping and defect generation during the stress. Based on these fundamental studies of the dielectric breakdown, modeling of time-dependent dielectric breakdown (TDDB) was done. The intrinsic TDDB of the Dy-doped HfO_2 gate oxide having 1 nm EOT is characterized by the progressive breakdown (PBD) model. At high temperature, the PBD becomes severe, since thermal energy causes carrier hopping between the localized weak spots. The voltage acceleration factor derived from the power law shows a realistic prediction in comparison with those from the 1/E model. The increase of the voltage acceleration factor at lower stress voltage is due to the lower trap generation rate in Dy-incorporated HfO_2. This voltage acceleration factor can be easily extended to include temperature dependency, and the effective activation energy derived from the power law is voltage dependent.

Lastly, I studied the device characteristics of thin HfON charge-trap layer nonvolatile memory in a $TaN/Al_2O_3/HfON/SiO_2/p\text{-}Si$ (TANOS) structure. A large memory window and fast erase speed, as well as good retention time, were achieved by using the NH_3 nitridation technique to incorporate nitrogen into the thin HfO_2 layer, which causes a high electron-trap density in the HfON layer. The higher dielectric constant of the HfON charge-trap layer induces a higher electric field in the tunneling oxide at the same voltage compared to non-nitrided films and, thus, creates a high Fowler-Nordheim (FN) tunneling current to increase the erase and programming speed. The trap-level energy in the HfON layer was calculated by using an amphoteric model.

Table of Contents

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW OF HIGH-K METAL GATE STACK CMOS TECHNOLOGY

Since the advent of CMOS devices over 40 years ago, SiO_2 has been used successfully as the transistor gate insulator. Equivalent oxide thickness (EOT) was scaled down at the rate of ~0.7x per generation up to around the 130nm node, but EOT scaling slowed down at the 90nm and 65nm nodes as the SiO_2 gat dielectric layer ran out of atoms and gate leakage power limited further scaling, as illustrated in Figure 1.1 [1].

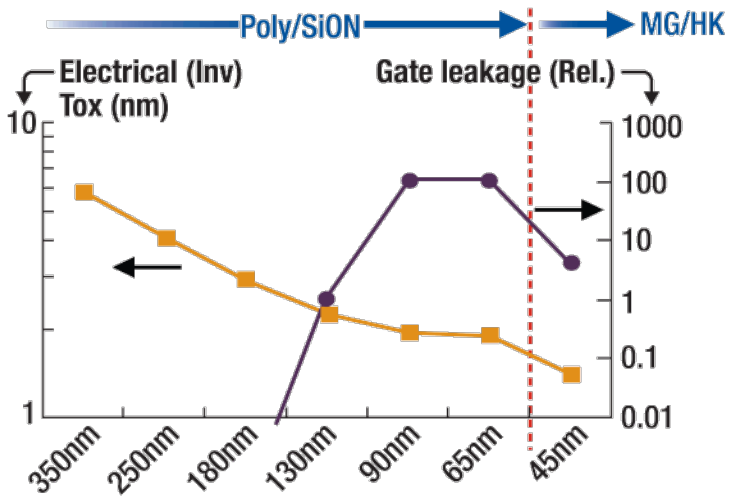


Figure 1.1. Intel's technology roadmap illustrating how migrating from Poly/SiON to metal gate/high-k (MG/HK) enabled the resumption of electrical T_{ox} scaling, while containing gate leakage [1].

Metal gate/high-k stack (HK/MG) technology promises to enable conventional scaling of the transistor as well as reduced stand-by power due to a reduction in gate leakage. For example, Intel's HK/MG at the 45nm node demonstrated EOT scaling further, while reducing the gate leakage by more than 10x (Figure 1.1). The improved device performance can be achieved by introducing HK/MG due to the higher permittivity ε_0 of the high-k dielectric over SiO_2 and the suppression of poly depletion. However, performance at high operating clock frequency can be bothered by increased gate capacitance. To minimize the shortcoming of using HK/MG, it is mandatory to concurrently scale down the gate length of the transistor. As shown in Figure 1.2 [2], this can be readily achieved thanks to the intrinsically superior electrostatic control of HK/MG over Poly/SiON.

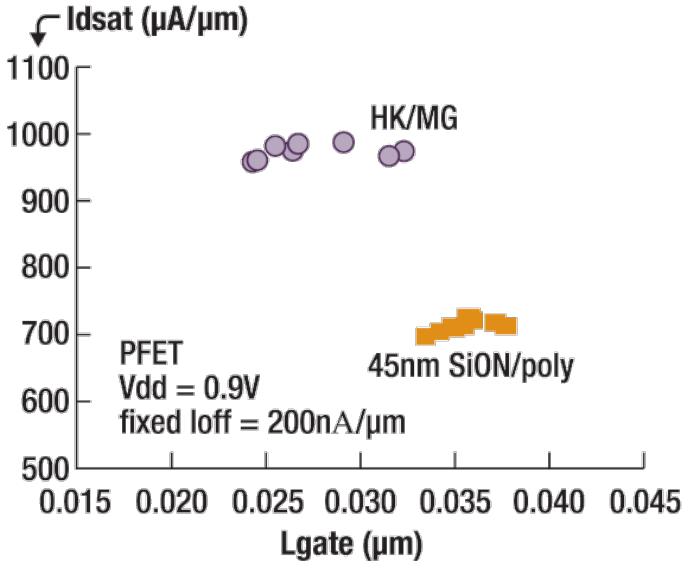


Figure 1.2. EOT(T_{ox}) scaling of HK/MG over Poly/SiON enables higher drive current as well as L_{gate} scaling, thanks to improved electrostatic control [2].

Concerning material options for high-k, extensive research has been done for more than 10 years. Taking into account the many requirements for a gate dielectric (e.g., barrier height, permittivity, thermal stability, interface quality, gate electrode compatibility), an Hf-based high-k films has the first priority. However, it is still unclear what the choice of the metal electrode should be due to the large impact of various processing parameters on the final effective work function of the gate stack. Among many candidates, near-midgap nitrided metals like TiN or TaN are considered as the most promising materials.

Two different integration schemes have been developed to achieve a high performance: gate-first (often referred to as metal inserted poly-silicon or MIPS) and gate-last (also called replacement metal gate, RMG). Even though the terminology 'first' and ‘last’ simply refers to whether the metal electrode is deposited before or after the high temperature anneal(s) to activate S/D, each process flows is totally different. The gate-first approach in a fully-depleted CMOS process integration scheme for extremely thin silicon-on-insulator (ETSOI) devices, aimed at the 22 nm node and beyond, was initially developed by IBM. It relies on very thin capping layers — Al_2O_3 for the PMOS and LaO_x for the NMOS transistors — to create dipoles that modulate the threshold voltage of the device. However, thermal instabilities in HK/MG devices can lead to threshold voltage shifts and re-growth in the gate stack. This issue is particularly acute for pMOS at scaled EOT, as illustrated in Figure 1.3 [4]. In the extremely thin EOT region, it is clear that replacement metal gate (RMG) can deliver significantly higher

effective work function (EWF) (meaning lower pMOS V_{TH}) than MIPS. Note that this specific issue impedes essentially the use of gate-first process for high performance applications. For low standby power (LSTP) or DRAM applications, where V_{TH} and EOT requirements are typically more relaxed, gate-first remains a very viable and promising option for integrating a cost effective HK/MG CMOS solution [5,6].

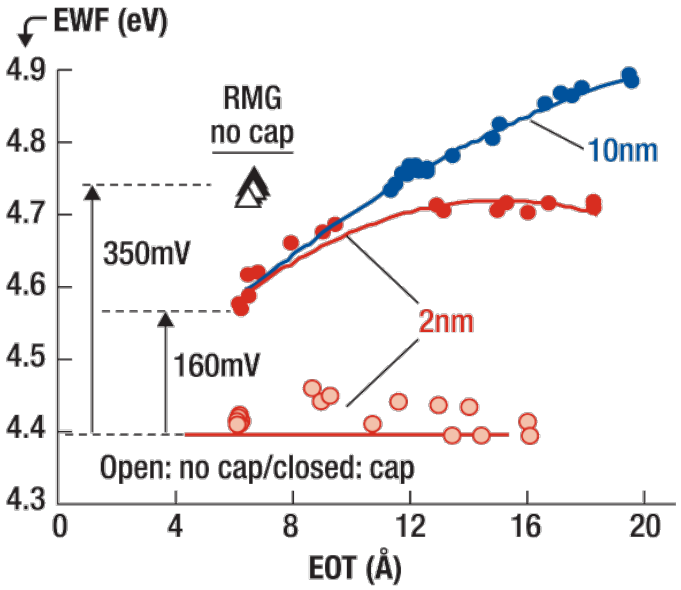


Figure 1.3. Effective workfunction (EWF) roll-off towards mid-gap at thin EOT for MIPS, irrespective of the metal gate thickness (2nm or 10nm).

Nevertheless, significant efforts to enable gate-first for high-performance applications are still under way. One promising work-around to the high V_{TH} issue proposed consists in forming by epitaxy a SiGe channel for pMOS devices [7]. This approach intrinsically lowers V_{TH} (through valence band off-set) and presents the additional benefit of higher

hole mobility than in Si. However, the extra cost associated with this epitaxy tends to offset the process complexity advantage of gate-first over gate-last.

The second way of integrating HK/MG, with a so-called gate-last process, was initially developed by Intel, implementing it in its 45nm technology [1]. In the process flow as shown in Figure 1.4, the hafnium dielectric was deposited before a sacrificial polysilicon gate was created. After the high-temperature S/D and silicide annealing cycles, the dummy gate was removed and metal gate electrodes were deposited later. More recently, Intel introduced second generation RMG in their 32nm technology, which is a slightly different scheme where the high-k is deposited last, right before the metal gate electrodes, and after the complete removal of the dummy gates.

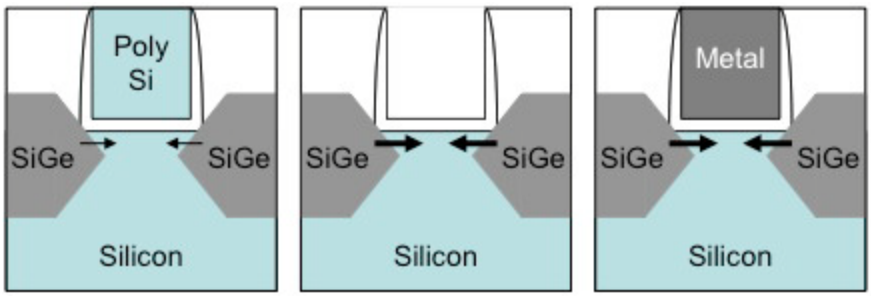


Figure 1. 4. Increased channel strain due to RMG process flow.

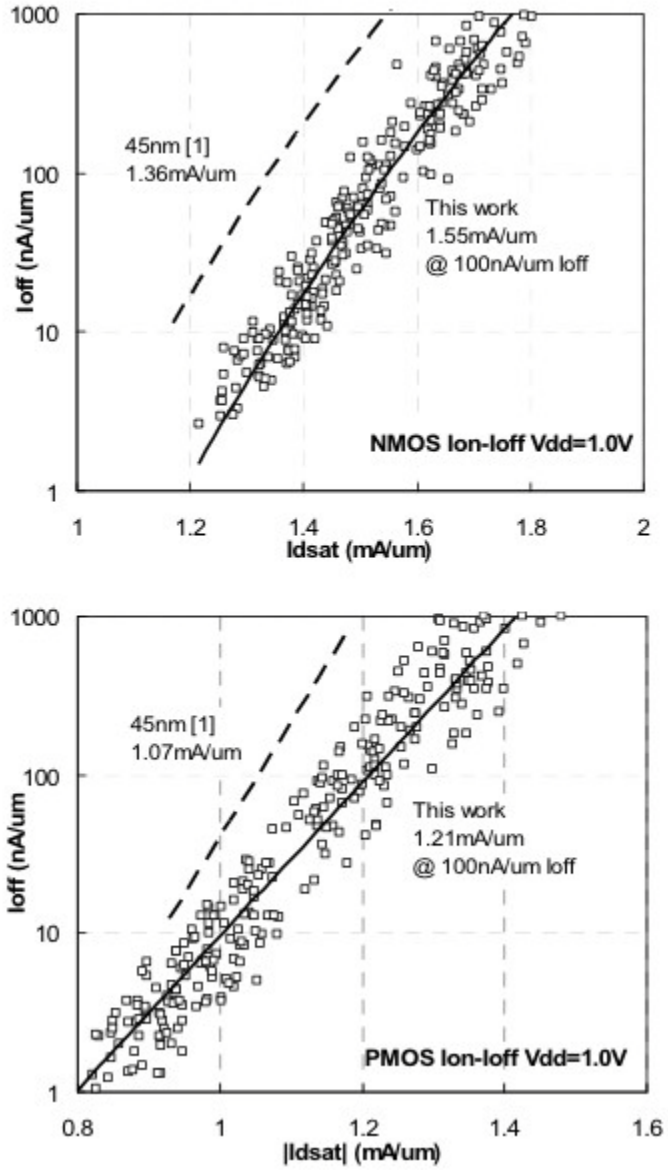


Figure 1. 5. nMOS (top) and pMOS (bottom) I_{dsat} vs. I_{off} at 1.0V.

Drive currents were the best reported yet for 32nm with 112.5nm contacted gate pitch. There was an average 40% improvement over the previous 45nm devices (Figure 1.5.).

The techniques were used for the largest SRAM with more than 1.9B transistors. One possible advantage with this new approach is to improve the device reliability and mobility at scaled EOT, which can be significantly degraded when the high-k dielectric has gone through the high thermal steps of the flow, just like in the gate-first approach [8]. One of the concerns often brought up concerning gate-last is its process complexity. As described by Intel [10], the dual metal gate formation involves some critical CMP steps. To maintain sufficient process window, such approach requires more restricted design rules (RDRs), like the 1-D design approach (where gates are all aligned in a given direction). However, at the 28nm node and more so at the 22nm node, this layout restriction is becoming mainstream anyway due to lithography constraints. Therefore, the higher design flexibility of gate-first might fade away for the future nodes, as more and more RDRs will need to be implemented.

Looking beyond the 22nm node, the device architecture itself might change from conventional planar to multi-gate (like FinFET or Trigate), in order to improve further the electrostatic control of the device. Those 3D devices might have a significant impact on the integration strategy of HK/MG. Most certainly a CMP-based approach (as in today's RMG flow) would become extremely complex, if not impossible, making the gate-first scheme the only solution (Figure 1.6).

	MIPS (Metal Inserted Poly-Si)	FUSI (FUlly SIlicided gate)	RMG (Replacement Metal-Gate)
			
Dielectric	First	First	First or last
Electrode	First	Last	Last
Pros	• Conventional process flow	• Low complexity • Thermal budget	• Thermal budget • Higher strain from embedded SiGe S/D
Cons	• Thermal budget • Complex V_T tuning • Mobility, reliability at thin EOT	• Silicide phase process window • Low V_T difficult	• Complexity, cost • More restricted DRs

Figure 1.6. Pros and cons of different HK/MG integration options. FUSI being abandoned, only gate-first (also commonly called MIPS) or gate-last (or RMG) are actively developed today.

1.2 MODULATION OF V_{TH} SHIFT IN DY-INCORPORATED HfO_2

1.2.1 Motivation

The V_{TH} modulation of high-k metal gate (HK-MG) stack has been one of the critical issues for CMOS applications. Even though it is still challenging to control the V_{TH} by the work function modulation of metal for the gate-first process, the EWF can be modulated to obtain the target V_{TH} by introducing dipoles or charges in the gate oxide [3.1]. La or Al doped oxides are well known to change the V_{TH} by the La or Al-induced dipole [3.2-3.4]. Dysprosium (Dy) incorporation, which is one of the possible candidates in CMOS application, also shows the V_{TH} shift and promising transistor characteristics [3.5-3.7]. Even though Dy incorporated Hf-based high-k and SiON gate dielectrics have shown the larger V_{TH} shift as well as improved mobility and reliability [3.6-3.7], the

mechanism of V_{TH} shift by Dysprosium (Dy) incorporation has not been reported yet. The mechanism of negative V_{TH} shift by lanthanide oxides are often explained by dipole formation [3.2-3.4, 3.8]. One explanation for the origin of intrinsic dipole formation is positively charged mobile oxygen vacancies which are responsible for the negative shift in V_{FB} and V_{TH} due to the aliovalent substitution of two La^{3+} cations for two Hf^{4+} cations forming one positively charged oxygen vacancy (V_O) in LaO/HfO system [3.3]. The electronegativity and ionic radii of dopant rare earth in (La, Sc, Sc+Er, Er, Sr)/HfO_2 oxide stack has been proposed as a possible origin of the dipole formation at the high-k/SiO_2 interface [3.9]. Another suggestion is that the areal density differences of oxygen atoms at the high-k/SiO_2 interface play a crucial role in the intrinsic dipole formation in that the oxygen movement from the higher density to the lower side determines the direction of the interface dipole. The driving force of the oxygen movement can be explained by the bonding energy relaxation at the interface [3.10]. Although the high-k/SiO_2 interface is known to be a determining factor in controlling the threshold voltage, experiment data should be analyzed in the context of comparing the V_{TH} shifts of different high-k materials with respect to the structural effects and the diffusion of dopant material corresponding to the different annealing temperatures. The V_{TH} shift mechanism of Dy incorporated HfO_2 will be investigated in relation to the Dy-induced dipoles formation in this report.

In our approach, we made nMOS capacitors and transistors to investigate the mechanism of V_{FB}/V_{TH} shift of co-sputtered DyHfO and bi-layered DyO/HfO oxides which were annealed at 500 °C post-dielectric deposition anneal (PDA) condition after

Dy and Hf thin films were deposited on the p-type Si wafers. We compared the V_{FB} of the MOSCAPs annealed at 500 °C with the V_{FB} of the same samples after 900 °C post metallization annealing (PMA) while considering the relationship between EOT and V_{FB}/V_{TH}. To clarify whether the mechanism is related to Dy-induced charges or dipole formation in the Dy-Hf-O/SiO_2 system, we characterized the electrical data, checked the Dy diffusion with respect to a different annealing temperature and oxide stack (i.e. co-sputtered DyHfO/Si p-sub and bi-layered DyO/HfO/Si p-sub and HfO/DyO/Si p-sub), performed X-ray Photoelectron Spectroscopy (XPS) analysis, supported by Scanning Transmission Electron Microscopy (STEM) Energy Dispersive X-Ray Spectrometry (EDXS) with the DyO/HfO/Si p-sub samples annealed at 500 °C PDA and after 900 °C PMA, respectively.

1.2.2 Background of Workfunction Modulation in Metal Gate High-k Gate Stack

Poly-silicon gates on HfO_2 and Al_2O_3 have been shown to suffer from Fermi-level pinning, which lead to undesirable threshold voltage values [3.17]. This caused the tremendous interest in understanding the mechanism of V_{TH} shift in metal high-k stack. However, to understand whether issues such as metal induced gap states [3.18] and the presence of dipoles may impact the work function, one must measure the work function accurately in the presence of charges. Since most metal high-k gate stacks result in a bi-layer structure consisting of a SiO -rich interface region and a bulk high- region, charges can be located at: a) bulk high-k layer, b) interface of high-k and SiO rich interface layer, c) bulk of the interfacial layer, d) Si-SiO rich interface and e) high-k- metal gate electrode

interface. In order to extract an accurate work function, the charges at these locations must be either accounted for or measured in such a manner that they do not impact the work function extraction. A systematic methodology to extract the accurate work function of metal gates on high- dielectrics in the presence of charges was developed [3.8]. This methodology consists of dependently varying the interfacial layer (with constant high-k thickness) and independently varying the high-k layer (with constant interface layer) to decouple the impact of charges from the work function.

The primary equation that relates the flatband voltage, $V_{FB,}$ to the gate dielectric charge distribution per unit volume $\rho(x)$, and EOT is [3.19]

$$V_{FB} = \Phi_{ms} - \frac{1}{\varepsilon_{OX}}\left[\int_0^{EOT} x\,\rho(x)\,dx\right] \quad (1)$$

where ε_{OX} is the permittivity of SiO_2 and Φ_{ms} is the work function difference between gate and substrate. The top high-k dielectric EOT is defined as EOT_1 and bottom SiO_2 dielectric EOT is defined as EOT_2. Now, Eq. 1 can be rewritten as

$$V_{FB} = \Phi_{ms} - Q_f\frac{EOT}{\varepsilon_{OX}} - \frac{1}{\varepsilon_{OX}}\left[\int_0^{EOT_1} x\,\rho(x)\,dx + \int_{EOT_1}^{EOT} x\,\rho(x)\,dx\right] \quad (2)$$

where $EOT = EOT_1 + EOT_2$. Eq. 2 is a fundamental equation, which can be extended to multiple dielectric stacks with various charge distributions. For the system being considered, a bi-layer stack is a reasonable assumption based on the extensive materials characterization of this gate stack [3.20]. The charges at the SiO_2/Si interface are defined as Q_f (per unit area) and SiO_2 bulk charges are defined as ρ_{bulk} (per unit volume). Hence, Eq. 2 can be written as

$$V_{FB} = \Phi_{ms} - \frac{1}{\varepsilon_{OX}}\left[\int_0^{EOT_1} x\,\rho(x)\,dx\right] - Q_f\frac{EOT}{\varepsilon_{OX}} - \rho_{bulk}\frac{EOT^2}{2\times\varepsilon_{OX}} + \rho_{bulk}\frac{EOT_1^2}{2\times\varepsilon_{OX}} \quad (3)$$

Now, if EOT_1 is kept constant and the total is changed only by varying EOT_2 (the SiO_2 layer), then from Eq. 3 V_{FB} dependence on EOT will be a polynomial of order two. If ρ_{bulk} is negligible compared to Q_f , Eq. 3 can be approximated to a polynomial of order one. This is a reasonable assumption as will be shown later. The intercept C is given by

$$C = \Phi_{ms} - \frac{1}{\varepsilon_{OX}}\left[\int_0^{EOT_1} x\,\rho(x)\,dx\right] \quad (4)$$

where the latter integral represents the dipole contribution, which is the product of the centroid of charge distribution and the total charge per unit area in the high- layer. Therefore, the intercept of the above equation is now a value of the Φ_{ms} and the charge in the high-k. The coefficients of the first order and the second order terms in the above polynomial, measure the charges in SiO_2–Si interface and in the bulk SiO_2 respectively.

1.2.3 Origin of V_{TH} Shift in High-K/Metal Gate

The EOT-V_{FB} relationship is usually used to clarify the dipole formation or the interface charges. From reference [3.8], the equation of V_{FB} and EOT can be written for accurate calculation.

$$V_{FB} = \phi_{ms} + \Delta D - Q_f\frac{EOT}{\varepsilon_{OX}} - \rho_b\frac{EOT^2 - EOT_h^2}{2*\varepsilon_{OX}} \quad (5)$$

where φ_{ms}, ΔD, Q_f, ρ_b, EOT and EOT_h are the work function difference between the metal gate and the Fermi energy of the Si substrate, dipole term, interface fixed charges, bulk charge density in the high-k layer, EOT of the total gate stack, and EOT of the high-k layer, respectively. According to Eq. 5, the dipole is independent of EOT, so that the

V_{FB} will remain unchanged with respect to the EOT increase. Meanwhile, the V_{FB} will be linearly dependent on the EOT change if the fixed charges are formed at the bottom SiO_2/Si interface. If the contribution of bulk charges is significant, then a quadratic dependence of V_{FB} on EOT is expected to be observed. The V_{FB} change by dipole is expressed by

$$\Delta V_{FB} = \frac{Q \times d_{dipole} \times N_{dipole}}{\varepsilon_{dipole}} \quad (6)$$

where Q is the charge amount at both ends of the unit dipole ($+Q$ and $-Q$), d is the distance between the charges, N_{dipole} is the areal density of the unit dipole, and ε_{dipole} is the permittivity of the dipole layer. It has been reported that La in SiO_2 forms a silicate layer with a saturation compound of $La_2Si_2O_7$ [3.10]. Upon the La-silicate-forming reaction, it is expected that the areal density of La atoms at the SiO_2 interface becomes smaller than that for the original La_2O_3/SiO_2 interface. In addition, La-induced dipole effect on the band bending is nearly constant in the temperature range between 500 and 800 °C. This indicates the formation of the long range (increase in d_{dipole}) dipole spanning the La-silicate layer, which compensates the reduction in N_{dipole} and keeps the strength of the dipole moment constant. As a result, charges within the La-O-Si network are cancelled out and long-range and low-density net dipole moment may be formed [3.11-3.12]. Since the strength of the dipole moment is proportional to $N_{dipole} \times d_{dipole}$, a sufficient V_{TH} shift can be maintained by compensating the reduction of N_{dipole} by the increase of d_{dipole}. Dy dipole formation mechanism will be discussed in associated with the formation of Dy-silicate in the interface. The temperature-dependent Dy-silicate

formation in the interface will be proven with the material analysis data such as XPS and STEM EDX, and the mechanism of V_{FB}/V_{TH} shift of Dy-Hf-O/SiO_2 stack will be discussed in later sections. The similar results of the Al- and La-induced dipole was reported to control the flatband voltage of Al_2O_3 film and La_2O_3 film [3.11]. Their minimum activation temperature to form the dipole is 300 °C. When La and Al atoms coexist on a SiO_2 surface, the La-induced dipole becomes dominant after a silicate-forming reaction at temperatures above 600 °C due to the different nature of the La- and Al-induced dipoles. As the La-silicate layer forms in the interface during the high temperature annealing, the Al-induced dipole is released due to the disappearance from the original Al_2O_3/SiO_2 interface. So in our DyO/HfO/SiO_2 system, the fact that Dy-induced dipole became dominant in controlling the V_{FB}/V_{TH} shift indicates the different nature of the Dy- and Hf-induced dipoles. While Dy-induced dipoles increase during high temperature annealing, Hf-induced dipoles are released. Thus, the areal density of net Dy-induced dipole at the interface accounts for the V_{FB}/V_{TH} shift in Dy-Hf-O/SiO_2 system.

1.3 Device Characterization and Oxide Reliability in Dy-incorporated HfO_2

1.3.1 Characterization of Charge Trapping in Dy-incorporated HfO_2

Lanthanide materials including Lanthanum (La) have been implemented for improving HfO_2-based gate dielectric and one of the most possible alternative gate oxides in currently developing CMOS technology [4.1-4.3]. Dysprosium (Dy) is one of the lanthanide rare earth materials and its electrical properties are reasonable for CMOS application [4.4]. The advantage of Dy-doped HfO_2 oxide MOSFETs in terms of the electron mobility, drive current and gate leakage current has been discussed [4.5]. DyO-capped HfSiON and SiON with Ni-FUSI CMOS lowered V_{TH} by 300mV/500mV and improved the gate leakage, mobility and reliability [4.6]. Charge trapping characteristics such as positive bias temperature instability (PBTI) also improved during constant voltage stress at room and high temperature. However, the mechanism responsible for the reduced leakage current and charge trapping characteristics of Dy-incorporated HfO_2 gate dielectric device has not been reported yet. Most HfO_2-based dielectrics suffer from charge trapping/detrapping during stress and it is reported to be strongly polarity-dependent due to the inherent asymmetry of the bi-modal stack [4.7-4.8]. Even though there is controversy about the polarity issue, the reliability of the high-k dielectrics is believed to be dominated by the breakdown of the interfacial layer rather than the high-k itself. Intrinsic effects, rather than the extrinsic, also dominate time-dependent dielectric breakdown (TDDB) [4.9-4.10].

1.3.2 Oxide Reliability in High Temperature

In the second part, we compare the characteristics of Dy-incorporated HfO_2 (DyO/HfO) and HfO_2 gated n-MOSCAP by measuring the gate leakage currents and capacitances with various voltage stresses and by performing the time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) with a various constant voltage stress. To clarify the reason for the reduced leakage current and charge trapping characteristics of the Dy-doped HfO_2, the effective barrier heights of Dy_2O_3 and DyO/HfO oxide were extracted from the Fowler Nordheim (FN) tunneling current. Stress-induced leakage current (SILC) and stress-induced flatband shift was analyzed for the charge trapping characteristics and interpreted with a proposed band diagram [4.11-4.12]. TZDB and TDDB were performed with small area capacitors to ensure intrinsic breakdown, and the Weibull slope was obtained [4.11, 4.13]. Among all of the reliability issues associated with high-k dielectrics, Time Dependent Dielectric Breakdown (TDDB) has been most intensively studied. The reliability of high-k gate dielectrics is dominated by the breakdown of the interfacial layer rather than the high-k layer itself. The fact that the interfacial layer plays a strong role in the failure process is reported in studies of lifetime extraction [5.1]. The Weibull failure time dispersion β dependence on the overall dielectric thickness is much less pronounced in high-k stacks compared to SiO_2. The measured β values do correlate well with the interfacial thickness [5.1]. To understand the mechanism of the intrinsic dielectric breakdown, we measured the TDDB by varying the stress voltage and temperature, and analyzed data by using two models, the thermochemical breakdown model (E model) and the hole-induced breakdown model

(1/E model) [5.2]. However, these models that were developed for SiO_2 cannot be directly applied to the thin EOT high-k dielectrics because the charge trapping phenomena and its conduction mechanisms are behaving differently. For example, the higher trap generation rate in bias-temperature instability (BTI), stress-induced leakage current (SILC), and higher leakage current before breakdown in these high-k dielectrics complicates the study of time dependent dielectric breakdown (TDDB) [5.3-5.5]. Furthermore, the charge trapping/detrapping in high-k dielectrics is related to the wear-out of oxide in bulk as well as at the interface, and its conduction mechanism often follows the Poole-Frenkel emission. In fact, the higher leakage current in the thinner HfO_2 gate dielectric device and the irregular distribution of the soft breakdown and hard breakdown modes are the reasons for the poor Weibull slope [5.6].

1.4 DEVICE CHARACTERISTICS OF HFON CHARGE-TRAP LAYER NAND FLASH MEMORY

1.4.1 Overview of NAND Flash Memory and Cell Operation

Flash memory or a flash RAM is a type of nonvolatile semiconductor memory device where stored data exists even when the power is off. It is an improved version of the electrically erasable programmable read-only memory (EEPROM). The difference between Flash Memory and EEPROM is that the EEPROM erases and rewrites its content one byte at a time, or in other words, at byte level, whereas Flash Memory erases

or writes its data in entire blocks, which makes it a very fast memory compared to the EEPROM. Flash memory cannot replace DRAM and SRAM because the speed at which the DRAM/SRAM can access data and also their ability to address at byte level cannot be matched by Flash. The flash memory is also termed Solid-state Storage Device (SSD) due to the absence of moving parts in comparison to traditional computer hard disk drive. The two main types of flash memory are the NOR Flash and NAND Flash. Intel was the first company to introduce commercial (NOR type) flash chip in 1988 and Toshiba released the world's first NAND-flash in 1989. NOR-flash is slower in erase-operation and write-operation compared to NAND-flash. That means the NAND-flash has faster erase and write times. Moreover, since NAND cells are erased by block units, small numbers of erase operations are needed. NOR-flash can read data slightly faster than NAND. NOR offers complete address and data buses to randomly access any of its memory location (addressable to every byte). This makes it a suitable replacement for older ROM BIOS/firmware chips, which rarely needs to be updated. Its endurance is from 10,000 to 1,000,000 erase cycles. NOR is highly suitable for storing code in embedded systems. Most of today's microcontrollers come with built-in flash memory. NAND-flash occupies a smaller chip area per cell. This makes NAND available in greater storage densities and at lower cost per bit than NOR-flash. It also has up to ten times the endurance of NOR-flash. NAND is more fit as storage media for large files including video and audio. The USB thumb drives, SD cards and MMC cards are of NAND type. NAND-flash does not provide a random-access external address bus, so the data must be read on a block-wise basis (also known as page access), where each block

holds hundreds to thousands of bits, resembling a kind of sequential data access. This is one of the main reasons why the NAND-flash is unsuitable to replace the ROM, because most of the microprocessors and microcontrollers require byte-level random access.

A write operation in any type of flash device can only be performed on an empty or erased unit. So, in most cases write operation must be preceded by an erase operation. The erase operation is fairly straightforward in the case of NAND-flash devices. But for a NOR-flash, it is mandatory that all bytes in the target block should be written with zeros before they can be erased. The size of an erase-block in NOR-flash ranges from 64 to 128 Kbytes. Here, a write/erase operation can take up to 5 s. But the NAND-flash erase blocks are 8 to 32 Kbytes in size. So it is obvious that the NAND performs the identical operation in a lesser time duration. INOR-flash interface resembles closely a SRAM memory interface, which has enough address pins to map its entire media, allowing for easy access to every byte contained in it, whereas the NAND-flash go for serially accessed complicated I/O mapped interface. Here, the same pins are used for control, address and data. In traditional single-level cell flash devices, each cell stores only one bit of information. Later, many developers have developed a new form of flash memory known as multi-level cell flash that can store/hold more than one bit rather than a single bit in each memory cell, thus doubling the capacity of memory.

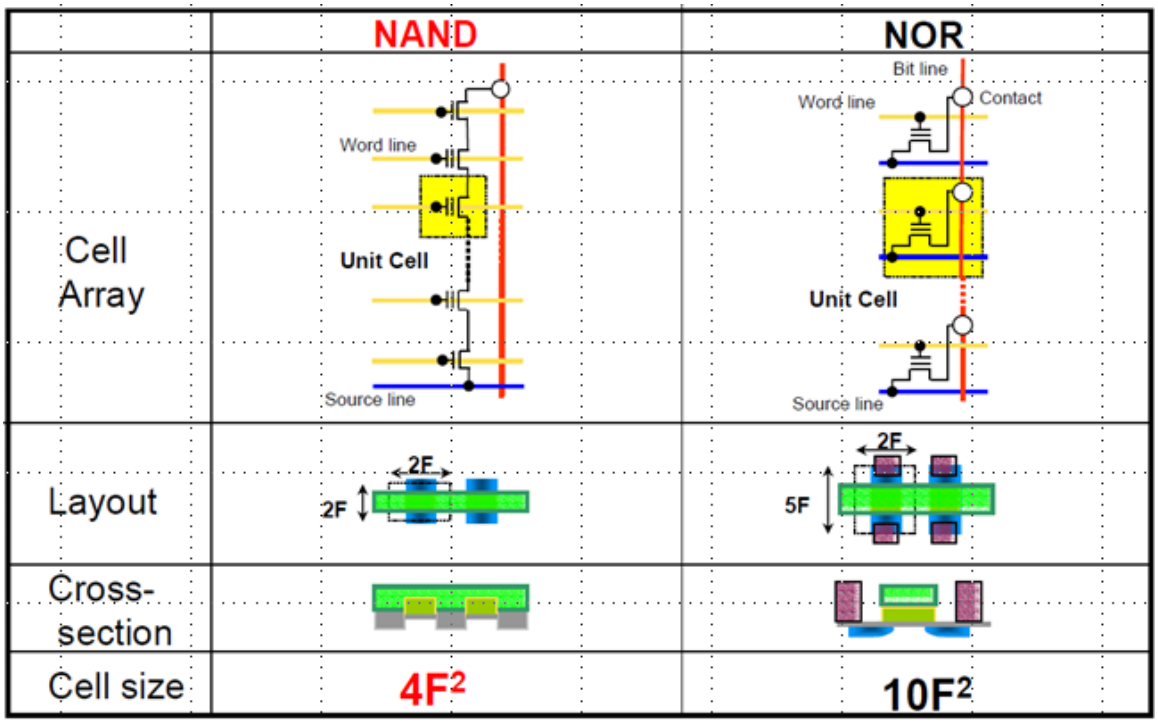


Figure 1.7. Comparison of NAND and NOR flash memory.

Flash memory cell structure:

Flash memory stores data in an array of memory cells. The memory cells are made from floating-gate MOSFETs (known as Floating-Gate Flash memory). This FG Flash memory has the ability to store electrical charge for extended periods of time (2 to 10 years) even without connecting to a power supply. The FG Flash memory is actually fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to this gate (floating-gate) (see Figure 1.7). A secondary gate (more than one in the case of multiple gate transistor) known as control gate is then

deposited above this floating gate and is electrically isolated from it using an insulator like SiO_2. There will be only capacitive connection between the new inputs (control gates) and the floating gate, because the floating gate is completely surrounded by highly resistive material (SiO_2). So, in terms of its DC operating point, the FG is a floating node. Each cell (FGMOS) of a NOR-flash memory resembles a standard MOSFET, except for the FGMOS that has two gates instead of one. On top is the control gate, as in ordinary MOS transistors. Below this control gate, is the new gate called floating gate, which is insulated all around by the oxide layer (SiO_2). The floating gate is interposed between the control gate and the MOSFET channel. Because the floating gate is electrically isolated by the oxide layer, any electrons placed on it are trapped there and, under normal conditions, will not discharge for many years.

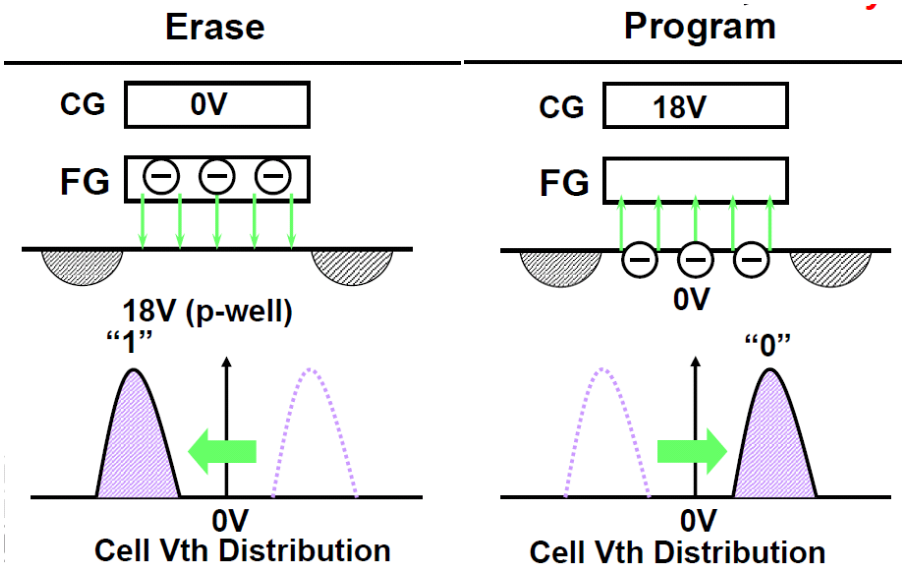


Figure 1.8. Cell structure of Flash memory and the electron trapping by FN tunneling

The names, NOR-flash and NAND-flash came from the structure used for the interconnections between memory cells. Cells in NOR-flash are connected in parallel to the bit lines so that each cell can be read/written/erased individually. This parallel connection of cells closely resembles the parallel connection of transistors in a CMOS NOR gate, thus the name NOR flash. In NAND-flash, cells are connected in series resembling a NAND gate, and thus the name. The series connection prevents the cells from being programmed individually. These cells must be read in series.

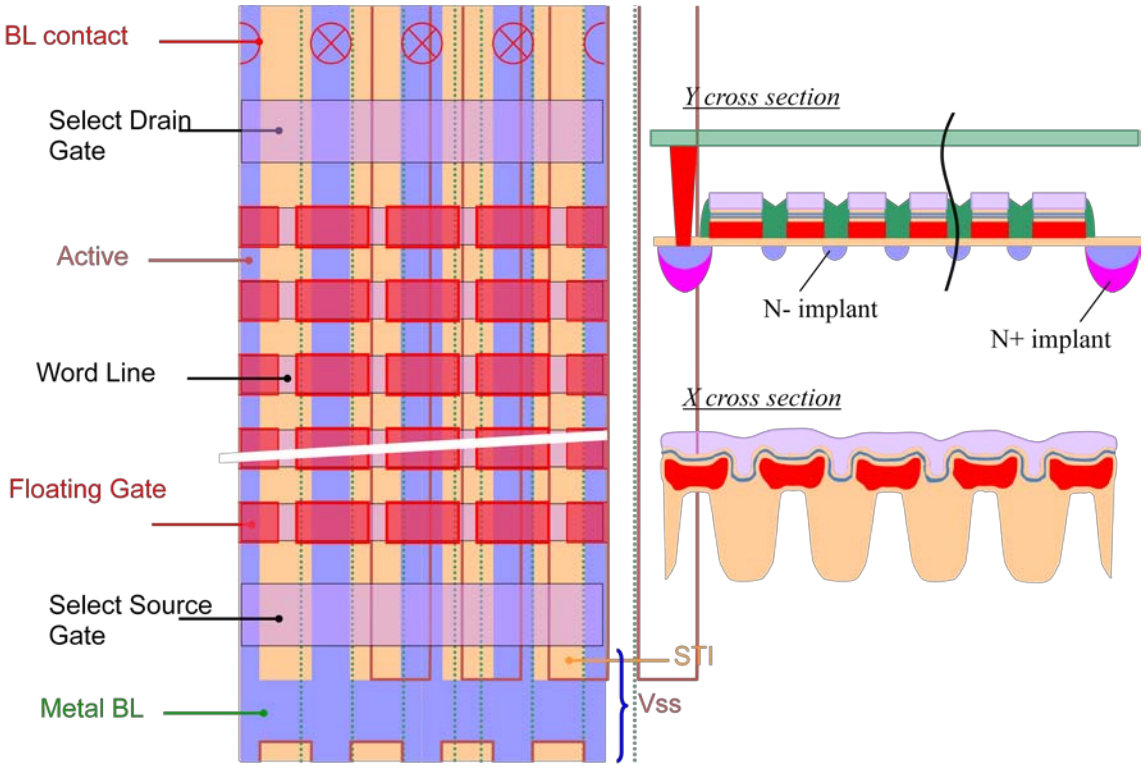


Figure 1.9. Cell structure of NAND flash memory

A typical flash-array has a grid of columns and rows of FGMOS-transistor cells as shown in Figure 1. 9. The word line WL is the horizontal line and bit line BL is the vertical line (shown in Figure 1.9). The Control gates of the FGMOS cells are connected to the word-line WL. The decoded address is actually applied to this word-line. The bit line BL connects drains of the FGMOS cells together and represent data bus. The Source-line SL

connects sources of the FGMOS to a common ground. The voltage combinations applied to WL and BL define an operation, whether it is read, erase or program.

Operating scheme:

Flash memory stores the data by removing or putting electrons on its floating gate (see Figure 1. 8). Charge on floating gate affects the threshold of the memory element. When electrons are present on the floating gate, no current flows through the transistor, indicating a logic-0. When electrons are removed from the floating gate, the transistor starts conducting, indicating a logic-1. This is achieved by applying voltages between the control gate and source or drain. Fowler-Nordheim (F-N) tunneling and hot-electron injection are some of the processes by which these operations are carried out in the flash cell.

Tunneling is a process where electrons are transported through a barrier. Here, the barrier is considered as the thickness of the SiO_2 insulator layer surrounding the floating gate. Let us now see how a NAND-flash cell operates. In NAND-flash, the program operation (or the memory write) is carried out via "F-N tunneling" and the erase operation via hot-hole injection.

1. Write (program) operation:

A NAND flash cell can be programmed, or set to a binary "0" value, by the following procedure. While writing, a high voltage of around 18V is applied to the selected word line (WL) for the F-N tunneling, but only 10V is applied to the unselected WLs for inhibiting the electron tunneling by reducing the potential between the gate electrode and the channel. 10V is sometimes called V_{pass} voltage since it makes the currents flow from drain to source. The V_{pass} voltage can be further optimized for solving the disturbance problem on the inhibit cells. 0V is applied on the drain/source and SSG, but 3.4V is applied on the SDG to turn on the channel as shown in Figure 1. 10. Since the channel potential became 0V by flowing the currents, the potential difference between the selected WL and the channel is 18V, which is sufficiently high to cause some electrons to tunnel through the insulating layer into the floating gate, via a process called F-N tunneling. On the other hand, for the unselected WLs, the same voltage as that of SDG is applied on the drain gate to turn off the channel. Hence, there is no current flowing in the channel of SDG, but the channel potential under the unselected WLs is floated. According to Ref. 11, the voltage in the channel, V_{ch}, can be estimated as follows

$$V_{ch} = \frac{C_{ins}}{C_{ins} + C_{channel}} V_{CC} \quad (7)$$

where C_{ins} is the total capacitance between control gate and channel (C_{ono} in series with C_{tunnel})

$$C_{ins} = \frac{C_{ono}\ C_{tunnel}}{C_{ono} + C_{tunnel}}.$$

In program inhibited strings, as the coupled channel voltage rises to $V_{CC} - V_{th}$ (of the SDG), the SDG transistor shuts off (Figure 1.10) and the channel becomes a floating node.

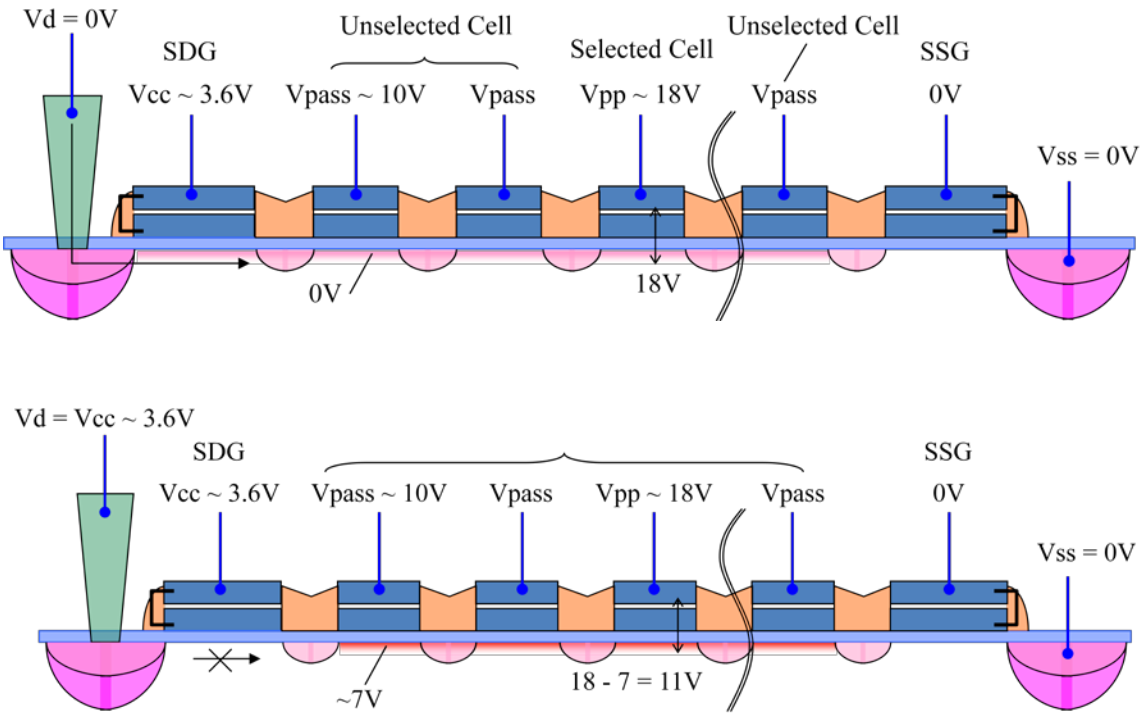


Figure 1.10. Cell program or write operation schematic

By calculating Eq. 7, the floating channel voltage rises to approximately 80% of the gate voltage, Thus, channel voltage of program inhibited cells are boosted to around 7 V when program (18 V) and V_{pass} (10 V) are applied to the control gate. This high channel voltage

prevents F-N tunneling occurring in the program inhibited cells. This is called self-boosting scheme. Since floating gate is insulated by oxide, the charge accumulated on the floating gate will not leak out, even if the power is turned off. A device called cell sensor watches the level of the charge passing through the floating gate. If the flow through the gate crosses the 50 percent threshold, it has a value of 1.

2. Erase operation:

The raw state of flash memory cells (a single-level NAND flash cell) will be bit 1's, (at default state) because floating gates carry no negative charges. Erasing a flash-memory cell (resetting to a logical 1) is achieved by applying 0V across WLs and -18V to the body in the sector and by floating the drain/source, SDG and SSG, so every cell in that sector will be erased (Figure 1. 11). This is the reason why the erasing speed of NAND flash in block unit is faster than the NOR. The -18V difference in each cell by the floating scheme enables the electrons in the floating gate to pull off by injecting the hot-holes.

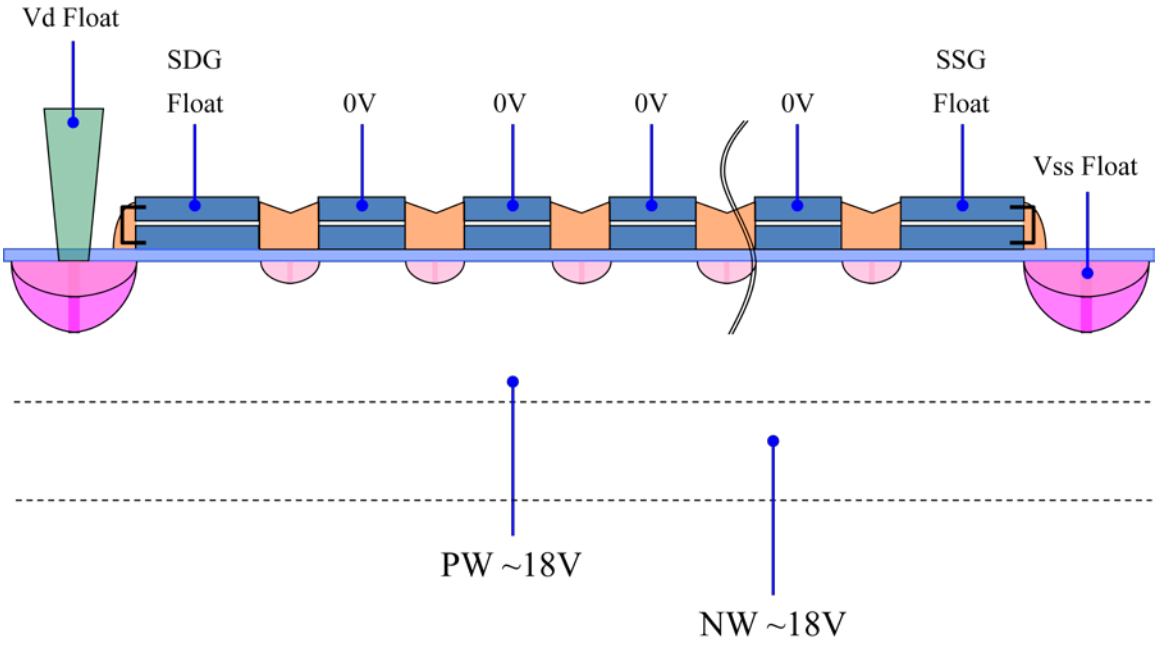


Figure 1.11. Cell erase operation schematic

3. Read operation:

Apply a voltage around 4V to the unselected WL, 0V to the selected WL and around 1V to the drain and 0V to the source at the selected block (or BL), respectively. For the unselected block, 0V is applied on all gates. 4V on the SDG, SSG and unselected WLs enables the channel to flow the currents along the BL between the drain and the source (Figure 1. 12). To read the data, 0V is applied to the selected WL, and the MOSFET channel will be either conducting or remain insulating, based on the threshold voltage of the cell, which is, in turn, controlled by charge on the floating gate. The current flow

through the MOSFET channel is usually small, so it needs to be amplified by the sense amplifier and forms a binary code, reproducing the stored data.

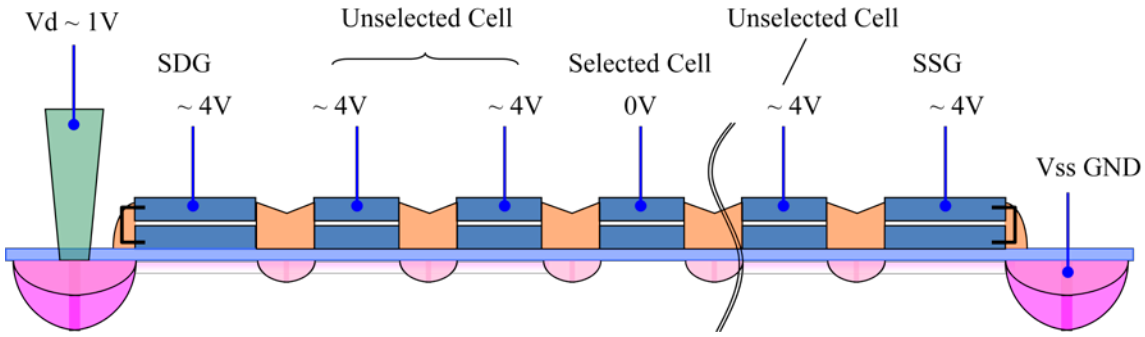


Figure 1.12. Cell read operation schematic

1.4.2 HfON Charge-trap layer NAND Flash Memory

We demonstrate the material and electrical characteristics of the TaN/ Al_2O_3/HfON/ SiO_2/Si-sub (TANOS) cell flash memory by using a thin HfON as a charge-trapping layer. The thin HfON layer is simply processed by NH_3 nitridation of the thin HfO_2 layer during rapid thermal annealing (RTA). NH_3 nitridation induces a large electron-trap density in the HfON layer. For this reason, NO gas is commonly used, instead of NH_3 in manufacturing to grow the ONO layer when low trap densities are desired [6.7, 6.8]. In flash-memory process, NO gas annealing is sometimes used to passivate the shallow traps in nitride by oxidation. Moreover, the high-dielectric constant of the HfON charge-trap layer enhances the electric field in the tunneling oxide, leading

to faster erasing and programming speeds due to the higher FN tunneling current. The HfON film has a high intrinsic trap density due to the non-stoichiometry. According to the phase diagram of the Hf-O-N system, we can easily modulate the bandgap and dielectric constant by changing the concentration of nitrogen [6.9]. We performed material analysis such as spectroscopic ellipsometry, to find out the optical bandgap of HfON thin film, and high-resolution transmission electron microscopy (HRTEM), electron energy loss spectroscopy (EELS), and energy-dispersive x-ray spectrometry (EDXS) for the composition and layer thicknesses of the TANOS cell. A wide memory window, fast erasing/programming characteristics, and good retention time were achieved. Endurance characteristics were measured by performing stress-induced leakage currents (SILC) analysis. Finally, retention characteristics were measured at different temperatures and the activation energy of the HfON trap layer was extracted from Arrhenius plots. The distribution of the trap energy levels is calculated by using an "amphoteric" model, which is used to explain the charge-loss mechanism [6.10].

1.5 CHAPTER ORGANIZATION

This chapter has presented an overview of issues in the process integration toward the 22nm or beyond technology related to high-k metal gate stack with eSiGe to enhance the device performance. Since this dissertation focuses on demonstrating and characterizing of Dy incorporated HfO_2, the next chapter will be devoted to providing a detailed process flow and improved device performance such as a lower V_{TH}, higher over-drive current and enhanced mobility. Chapter 3 and chapter 4 will investigate the

mechanism of V_{TH} shift and the charge trapping characteristics, respectively. In chapter 5, oxide breakdown at the higher temperatures will be discussed. Chapter 6 is allocated to describe the fabrication, device performance, and characterization of trap level energy of the thin HfON charge-trap layer nonvolatile memory in a $TaN/Al_2O_3/HfON/SiO_2/p\text{-}Si$ (TANOS). Chapter 7 will summarize the findings of this research and provide some concluding remarks.

CHAPTER 2

DEVICE PERFORMANCE OF DY INCORPORATED HfO_2 GATE N-MOSFET

2.1 BACKGROUND OF DY-INCORPORATION INTO HFO2

Hafnium oxides seem to be one of the most promising candidates for the aggressive scaling of CMOS devices. HfO_2, however, is vulnerable to the diffusion of oxygen that causes formation of a low-k interfacial layer at the Si interface. In addition, it crystallize at relatively low temperature (< 600 °C). Nitrogen incorporation into high-k dielectrics has been used to reduce EOT and improve its thermal stability [1-3]. Although nitrogen incorporation reduces interfacial reaction to obtain the lower EOT, it also degrades Si interface quality, resulting in large hysteresis, increased charge trapping and lower channel mobility due to trap charges caused by nitrogen itself [4-5]. Recently, Gd_2O_3 incorporated HfO_2 bi-layer n-MOSFETs to overcome the demerits of nitrogen incorporation, demonstrated a promising EOT scaling below 1nm regime [6]. Lanthanide oxides have been known to provide various advantages such as good thermal stability, moderately high dielectric constant, and high conduction offset to Si. However, their hygroscopic nature that leads to the retention of moisture and subsequent reaction with water imposes some challenge in integration issues. Dy_2O_3 has been reported as the least reactive with water, and thermodynamically stable with Si [7]. It was reported that lanthanide-doped HfO_2 exhibits a significant reduction in leakage current at the same

EOT [8]. Especially, Dy-doped HfO_2 gate dielectric is a promising candidate for applications. However, their approach was limited by doping Dy effectively into the HfO_2 [9].

In this study, structural approaches by incorporating dysprosium on the HfO_2 are systematically investigated and significantly improved device characteristics are demonstrated.

2.2 DEVICE FABRICATION AND ELECTRICAL MEASUREMENT

Active patterned p-type Si substrates having a 3×10^{15} cm^{-3} doping concentration were used for preparing samples after diluted-HF cleaning. Three different structures (top DyO with bottom HfO, top HfO with bottom DyO, and co-sputtered DyHfO mixture) were chosen for optimization of electrical characteristics. A thin Hf pre-deposition followed by Dy deposition were formed with DC sputtering (30 mTorr, Ar ambient, room temperature), and oxidized with the residual O_2 in the furnace during annealing for 5 min at 500 °C in N_2 at atmospheric pressure for DyO/HfO_2 structure. For HfO/DyO structure, the deposition sequence was reversed. The DyHfO structure was deposited by co-sputtering of Hf and Dy targets and annealed for oxidation with the same PDA condition. For comparison, the bi-layer structures all have the same total physical thickness while the co-sputtered DyHfO were fabricated with varying ratio of Dy and Hf. The physical thickness of oxide layers were measured by using a single-wavelength (632.8 nm) ellipsometer. TaN was deposited by using reactive sputtering (Ar + N_2, 10

mTorr, room temperature, ~ 2000 Å) for the gate electrode and then patterned by reactive ion etching (RIE) with CF_4. After implanted with a phosphorous at 50 keV with a 5×10^{15} cm^{-2} dose, Source/Drain regions were activated with a rapid thermal process (900 °C, 1 min, N_2). Al was used for both contact pad and back-side metal contact. Finally, forming gas annealing at 400 °C for 30 min was performed to make sure lower contact resistance. For the XPS, STEM EELS and EDX analysis, co-sputtered DyHfO film and bi-layered DyO/HfO film were deposited on the bare Si substrate and then were annealed with the same PDA (500 °C, 5min) and PMA (900 °C, 1 min, N_2) condition, respectively.

2.3 DEVICE PERFORMANCE AND ANALYSIS OF IMPROVED ELECTRON MOBILITY

In Figure 2.1, DyHfO mixture structures show trend that capacitance and flatband are related to the Dy concentration. As Dy ratio increased, EOT increased and flatband shifted in a negative direction. It is reasonable that when two different materials with the different dielectric constant intermixed, the total effective dielectric constant value should be in between of each value. The effective dielectric constant of DyO and HfO is 14 and 19, respectively. Negatively shifted V_{FB} of Dy incorporated sample means that Dy induced positive charge or dipoles in DyHfO mixture dielectric MOSCAPs. Even though leakage current was reduced in comparison to HfO_2 control, DyHfO mixture structures still have no advantage to the EOT scaling in CMOS technology (see Figure 2.2). Lower

EOT with reduced leakage current was obtained by using the top DyO and bottom HfO stack.

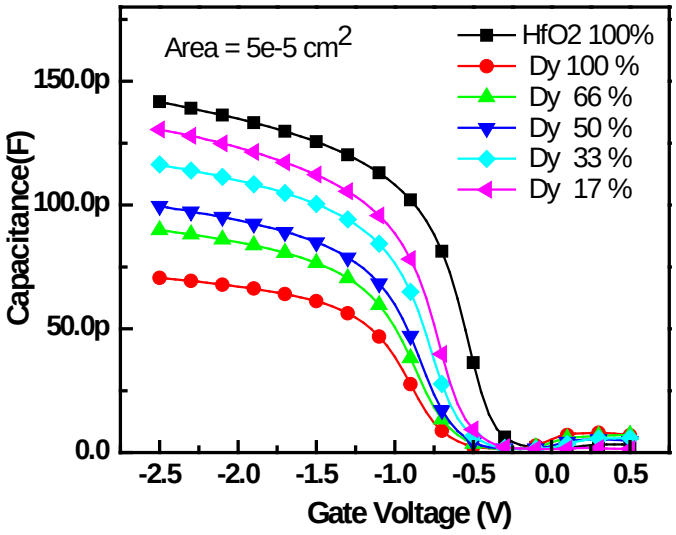


Figure 2. 1. Capacitance was decreased and flatband was shifted in a negative way as Dy ratio increased in co-sputtered DyHfO samples.

Figure 2.2 compares various dielectric structures in terms of leakage current density at $V_g = V_{FB} – 1V$ with a given EOT. The thickness dependency of HfO and DyO is quite important in this stack structure. Our other experiments for the different thickness show that the leakage current of the DyO/HfO nMOSCAP with a below 22Å physical thickness of HfO_2 was getting worse and the device with the higher thickness of DyO than the HfO resulted in a higher EOT. Therefore, the top DyO and bottom HfO (> 22 Å) structured devices with a 1:1 ratio are an definite strategy for the EOT scaling in CMOS technology.

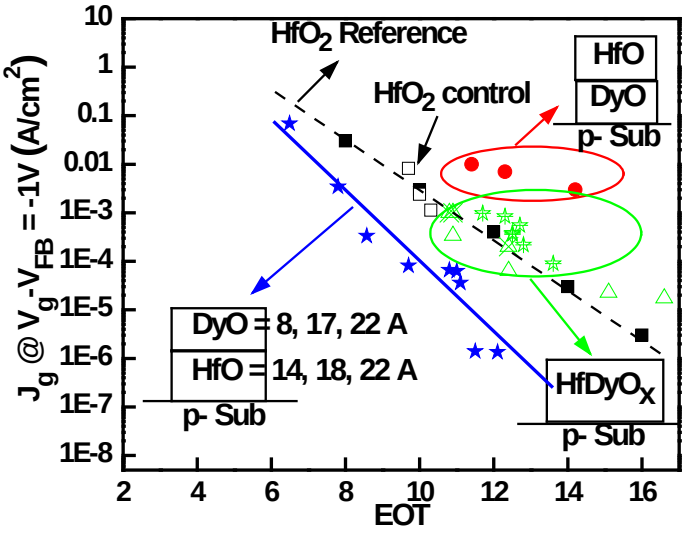
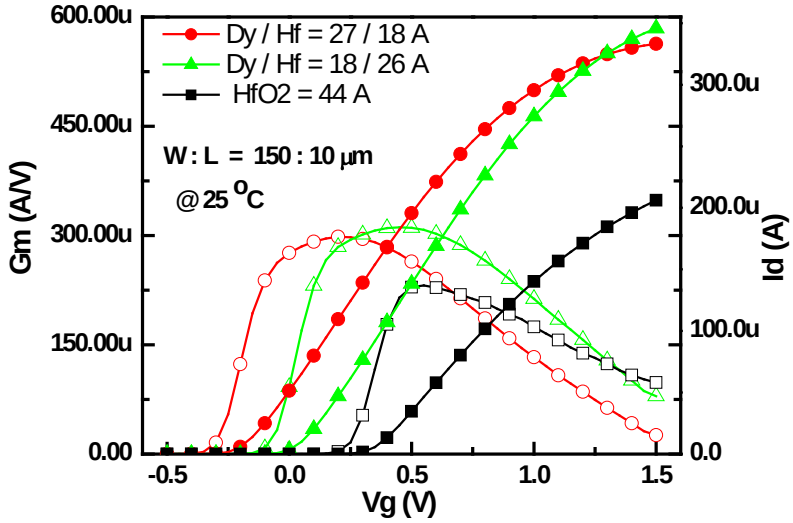


Figure 2. 2. Leakage currents were compared for different dielectric structures by differently incorporating Dy into HfO_2. Top DyO with bottom HfO structure shows significantly reduced leakage current for the same EOT.

In Figure 2.3 (a), DyO/HfO multi-metal stack oxide n-MOSFET shows excellent electrical properties such as $V_T \sim 0.031$ V, S ~ 66 mV/decade, Id ~ 9.9 mA, and $\mu_n \sim 320 cm^2/V\text{-sec}$. To investigate the charge trapping characteristic of these samples, bias-temperature instabilities (BTI) was performed. The results show that the DyO/HfO sample was observed to have better immunity for the charge trapping than the HfO_2 control sample (Figure 2.3 (b)). At even high temperature, HfO_2 sample has gone through

the “turn around” effect. This reduced charge trapping can be explained to a higher mobility.

(a)



(b)

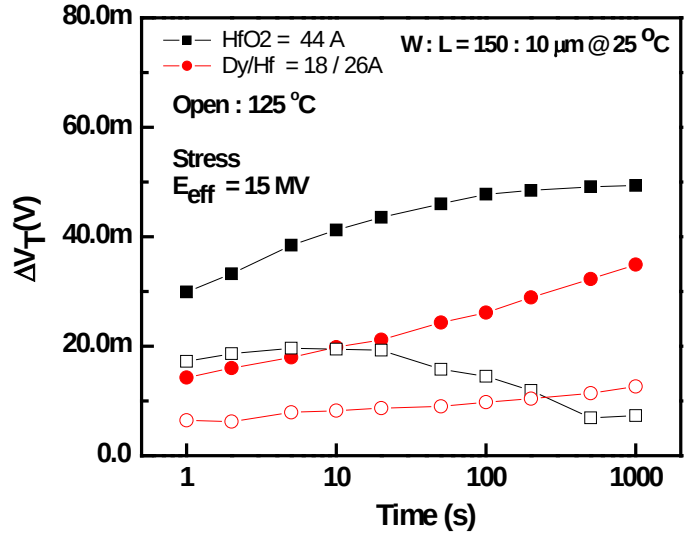
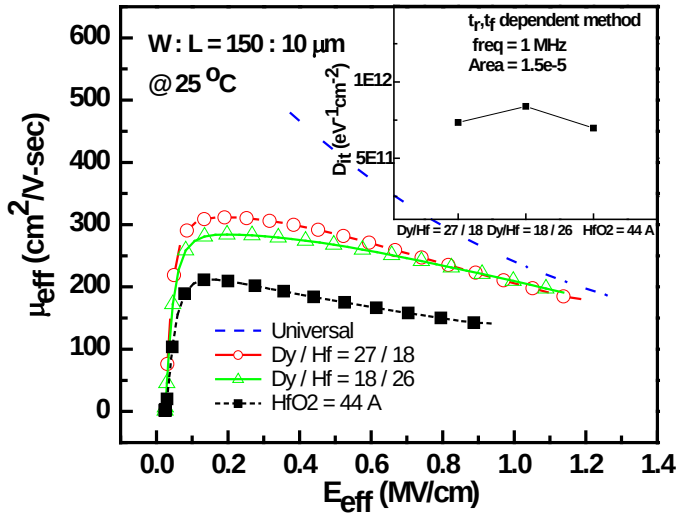


Figure 2. 3. (a) Id-Vg characteristics for several ratios of DyO/HfO bi-metal dielectric n-MOSFETs are shown. Reduced threshold voltage and higher output current are observed. (b) Time-dependent V_{TH} instability of the DyO/HfO sample shows less charge trapping than the HfO_2 control sample.

The DyO/HfO stacked transistors with the same total physical thickness as HfO_2 used to compare the channel mobility (Figure 2.4 (a)). However, the leakage current of the device for the DyO/HfO = 27/18 Å was worse than the HfO_2 one so that we will focus on the device for the DyO/HfO = 18/26 Å. Improved channel mobility in DyO/HfO structure means that some of the factors that degraded the channel mobility of HfO_2 were reduced by laminating DyO onto the HfO_2. In order to investigate the role of DyO layer for reduced channel mobility in stacked DyO/HfO n-MOSFET, interface quality was investigated first. Interface state density (D_{it}) was measured by charge pumping technique, in which the rise and fall time of the pulse signal was varied with a fixed frequency (1 MHz) in order to exclude the bulk traps. Inset in Figure 2.4 (a) indicates a reasonable and similar interface quality (~$10^{11}eV^{-1}cm^{-2}$). It is to be expected that the interfacial quality should be similar for both DyO/HfO bi-layer structure and HfO_2 since Hf was directly deposited on Si. Therefore, degradation in mobility due to interface traps should be similar for both cases. To analyze the mobility degradation for the phonon scattering, the effective mobility data was decomposed into three regime; coulomb, phonon and surface scattering [10]. According to the Matthiessens rule, the equation can be modified as follows; $\frac{1}{\mu_{phonon}} = \frac{1}{\mu_{eff}} - \frac{1}{\mu_{coulomb}} - \frac{1}{\mu_{surface}}$, where μ_{eff} is the total effective mobility, $\mu_{coulomb}$ is the mobility dominated by Coulomb scattering, $\mu_{surface}$ is the mobility dominated by surface scattering and μ_{phonon} is the mobility dominated by phonon scattering. $\mu_{coulomb}$ can be extracted from the effective mobility at low field

region by linear fitting and then extrapolated to high fields, and $\mu_{surface}$ can be calculated from the equation $\mu_{surface} = B \times E_{eff}^{-2.6}$, where B is 4.5×10^{19} [11], the unit for E_{eff} is V/m and the unit for $\mu_{surface}$ is m^2/V-sec. Figure 2.4 (b) shows the extracted mobility limited by phonon scattering is a dominant factor for mobility degradation. The HfO_2 gated MOSFET has been known to have additional source related to a soft optical phonon scattering [12]. The mobility degraded by the phonon scattering in DyO/HfO n-MOSFET was significantly reduced compare to the HfO_2 counterpart.

(a)



(b)

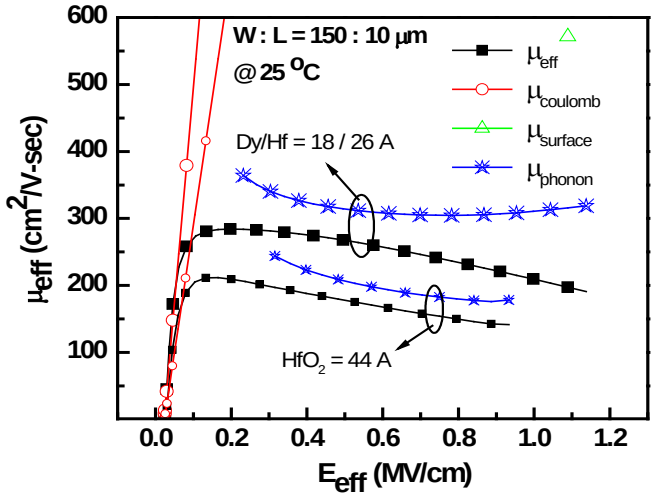


Figure 2. 4. (a) Electron channel mobility was increased for DyO/HfO structure n-MOSFET devices. Inset shows that interface quality is quite similar to each other. (b) Phonon scattering seems to be a dominant factor to determine the improved channel mobility.

2.4 SUMMARY

DyO-incorporated HfO_2 n-MOSFETs were fabricated and their electrical characterization was done. Optimized DyO/HfO bi-layer gate dielectric shows better scaling and improved MOSFET characteristics. This suggests that DyO/HfO gate stacks are promising for CMOS technology. Improved channel electron mobility can be explained by reduced charge trapping and phonon scattering.

CHAPTER 3

MECHANISM OF V_{FB}/V_{TH} SHIFT IN DYSPROSIUM (DY) INCORPORATED HFO_2 GATE DIELECTRIC NMOS DEVICES

3.1 THE DY-INDUCED DIPOLE IN DY_2O_3/SiO_2 GATE OXIDE

To identify the origin of the V_{FB} shift involving Dy, three different thicknesses of the Dy_2O_3 gate oxide layers were deposited on the p-type Si substrate and annealed at 500 °C PDA. The EOT-V_{FB} relationship is usually used to clarify the dipole formation or the interface charges. From reference [8], the equation of V_{FB} and EOT can be written for accurate calculation.

$$V_{FB} = \phi_{ms} + \Delta D - Q_f \frac{EOT}{\varepsilon_{OX}} - \rho_b \frac{EOT^2 - EOT_h^2}{2*\varepsilon_{OX}} \quad (1)$$

where φ_{ms}, ΔD, Q_f, ρ_b, EOT and EOT_h are the work function difference between the metal gate and the Fermi energy of the Si substrate, dipole term, interface fixed charges, bulk charge density in the high-k layer, EOT of the total gate stack, and EOT of the high-k layer, respectively. According to Eq. 1, the dipole is independent of EOT, so that the V_{FB} will remain unchanged with respect to the EOT increase. Meanwhile, the V_{FB} will be linearly dependent on the EOT change if the fixed charges are formed at the bottom SiO_2/Si interface. If the contribution of bulk charges is significant, then a quadratic dependence of V_{FB} on EOT is expected to be observed. In Figure 1, the dependency of the V_{FB} changes is plotted against EOT. It is clear that the slope of the V_{FB} change is very small, and the fixed charge extracted from the regression is 8.7×10^{10} q/cm^2, which is

negligibly small. Also a quadratic EOT dependence cannot be observed, indicating that the contribution of bulk charge density is also ineligible. The V_{FB}-axis interceptions of the linear regression lines in EOT vs. V_{FB} plot is now defined by the sum of dipole and $\varphi_{ms,}$ and the value of -0.998 V is obtained from Figure 3.1 Since the work function (φ_m) of TaN is 4.2 eV [11, 12] and the φ_s of the Si substrate used in this experiment with a $3x10^{15}$ cm^{-3} doping is 4.9 eV, the work function difference ($\varphi_{ms} = \varphi_m - \varphi_s$) is only -0.7 eV. Therefore, the rest of the V_{FB} shift can be attributed to a constant term of 0.3 eV from these set of samples.

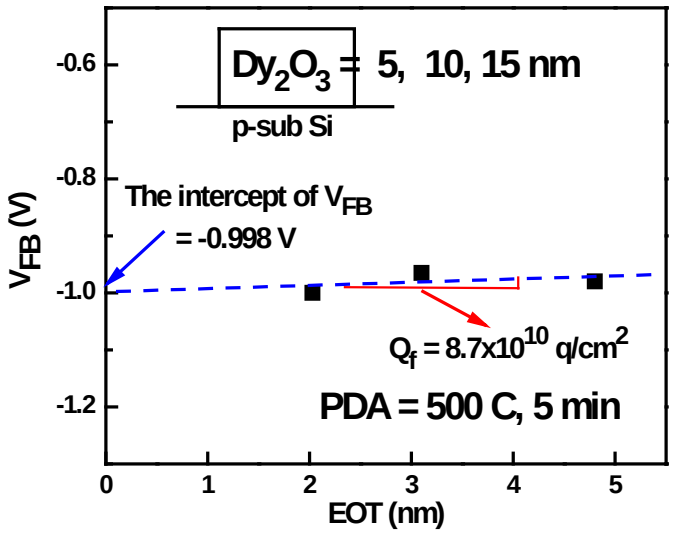


Figure 3.1. V_{FB} is independent of EOT for the Dy_2O_3 oxide MOSCAPs having different physical thicknesses. This is evidence of Dy-induced dipole formations rather than interface fixed charges controlling the V_{FB} shift of Dy_2O_3 oxide samples.

The V_{FB} and EOT relationship indicates that the main mechanism of V_{FB} shift is the formation of Dy dipoles at the DyO_x/SiO_2 interface is rather than fixed charges in the SiO_2/Si interface or bulk charges in the Dy_2O_3 film. According to the proposed model for the physical origin of the dipole formed at the high-k/SiO_2 interface [10], the difference in an areal density of oxygen atoms at high-k/SiO_2 interface causes the oxygen movement, and decides the direction and strength of the interface dipole. The number of oxygen atoms per unit area (σ) is approximately $V_u^{-2/3}$, where V_u is defined by the volume of unit structure containing a single oxygen atom, and can be calculated from the formula weight and the density of oxide. The extracted V_u of Dy_2O_3 is 28.7 since the molecular weight and the density of Dy_2O_3 is 373.99 (g/mol) and 7.81 (g/cm^3), respectively. Then, the extracted areal density difference (σ/σ_{SiO2}) of Dy_2O_3 is 0.85, where V_u of SiO_2 is 22.7 and the value of σ_{SiO2} is 1, which is summarized in Table 3.1

Oxide	Dy_2O_3	La_2O_3	HfO_2
EN (Pauling)	1.22	1.1	1.3
EN (Sanderson)	2.27	2.18	2.49
Density (g/cm^3)	7.81	6.51	9.6
Molecular Weight (g/mol)	373.99	325.82	210.49
V_u (Å^3)	28.7	27.7	22.7
σ/σ_{SiO2}	0.85	0.88	1.20

Table 3.1. ENs and normalized areal oxygen density (σ/σ_{SiO2}) is summarized in accordance to the structural parameters of Dy_2O_3. Data of La_2O_3 and HfO_2 is from reference [10] to be compared with Dy_2O_3.

This predicts that the direction of the dipole moment is from the high-k layer to the interfacial SiO_2 layer (i.e. negative V_{FB} shift), which agrees with the result. Dysprosium is one of the lanthanide materials and the atomic behavior seems to be very similar to La. Electronegativity (EN) and normalized areal oxygen density of Dy_2O_3 shown in Table 3.1 is also similar to La_2O_3, suggesting that Dy would show similar tendency as La in terms of V_{FB} shift [3, 10]. La in SiO_2 was reported to form a silicate layer resulting in the compound $La_2Si_2O_7$ [13]. In addition, the La-induced dipole has been explained by the La-silicate formation at the interface [3-4]. We will investigate the bond structure of Dy-O and Si-O in the interface with the XPS analysis to correlate with the silicate formation. The mechanism of V_{FB}/V_{TH} shift of the Dy-Hf-O/SiO_2 network will be discussed in conjunction with the temperature-dependent Dy-silicate formation at the interface with the material analysis data such as XPS and STEM EDX in the following sections.

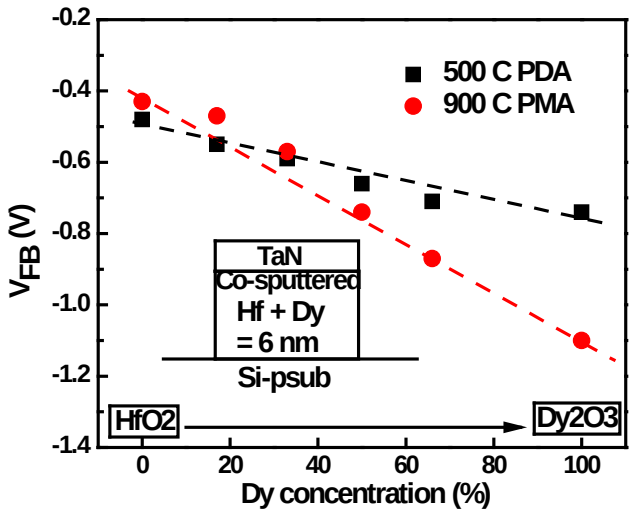


Figure 3.2. V_{FB} shift of the co-sputtered DyHfO gate oxide n-MOSCAPs are proportional to the percentage of the Dy atom and their values are between the V_{FB} of Dy_2O_3 and HfO_2. After 900 °C PMA, the flatbands were shifted more.

3.2 THE V_{FB}/V_{TH} SHIFT OF DY-DOPED HfO_2 MOS DEVICE

From Figure 3.2, the V_{FB} of co-sputtered DyHfO nMOS capacitors that were annealed at 500 °C PDA and after 900 °C PMA show a trend with respect to the Dy concentration. V_{FB} shift are proportional to the percentage of the Dy atom and their values are varying between that of Dy_2O_3 and that of HfO_2. In other words, V_{FB} of DyHfO can be controlled by the amount of Dy concentration at 500 °C PDA, and even larger amount of V_{FB} shift can be obtained by 900 °C PMA at the corresponding Dy concentration. This implies that the areal density of the net Dy-induced dipole at the interface can be modulated by both Dy concentration and annealing temperature. Dipole formation is known to be a thermally activated process [3], and more dipoles are formed at a higher temperature with a given Dy content. It is observed that the EOT increases with Dy concentration in DyHfO and anneal temperature. The increases in EOT of the DyHfO samples can be attributed to the lower dielectric constant of Dy_2O_3 oxide and Dy-silicate as shown in [6]. It is likely that interface layer growth is more responsible for the higher EOT in case of 900 °C PMA.

To understand the mechanism of V_{FB}/V_{TH} modulation with respect to Dy diffusion in DyO capped HfO_2 samples corresponding the annealing temperature, V_{FB} of DyO/HfO (=22Å/22Å), HfO/DyO (=17Å/26Å), and HfO_2 (=44 Å), are compared after 500 °C PDA and 900 °C PMA, respectively, as shown in Figure 3.3. After 500 °C PDA, the V_{FB} shift of DyO/HfO is the same as V_{FB} of HfO_2, and the V_{FB} shift of HfO/DyO corresponds to the V_{FB} of the single Dy_2O_3 oxide, which indicates that the bottom high-k layer deposited on Si substrate directly control the V_{FB} shift. In other words, the interface

that determines the V_{FB} shift is not the metal/high-k interface but the high-k/SiO_2 interface [2]. However, after 900 °C PMA, a larger V_{FB} shift was observed in the DyO/HfO, which corresponds to V_{TH} of each sample obtained after 900 °C PMA. This implies that the DyO layer and HfO layer in the DyO/HfO and HfO/DyO bi-layered oxides were fully intermixed and Dy atoms diffused down to the SiO_2/Si interface and formed Dy-induced dipoles after 900 °C PMA. In this regard, 500 °C annealing does not seem to provide enough thermal energy for full intermixing of the DyO layer and HfO layer in DyO/HfO nor the formation of Dy dipole at the high-k/SiO_2 interface as it results in negligible V_{FB} shift from that of HfO_2. In order to investigate the evidence of the chemical reaction that is associated with the dipole formation, we performed material analysis.

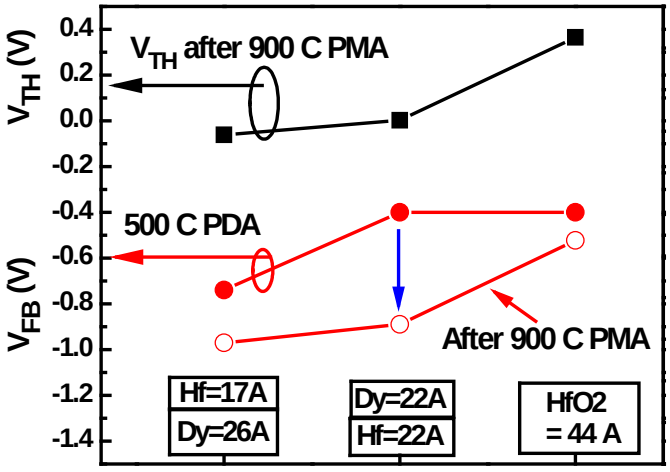
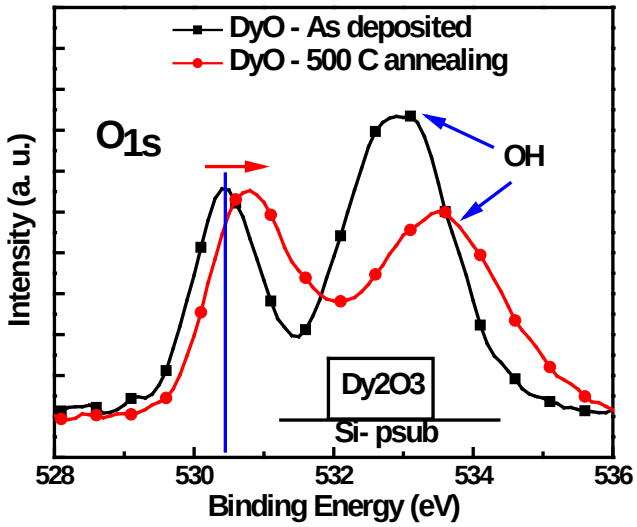


Figure 3.3. V_{FB} and V_{TH} of the bi-layered DyO/HfO=22Å/22Å and HfO/DyO=17Å/26Å samples are compared. After 500 °C PDA, V_{FB} of the bi-layered DyO/HfO=22Å/22Å is the same as HfO_2 =44 Å, but the larger flatband was shifted negatively after 900 °C PMA. V_{TH} of each sample was obtained from the bi-layer HfO/DyO, DyO/HfO and HfO_2 n-MOSFET after 900 °C PMA. V_{TH} of each sample follows the trend of V_{FB} shift extracted from n-MOSCAPs after 900 °C PMA.

3.3 MATERIAL CHARACTERIZATION WITH XPS AND STEM EDX DATA

To clarify the Dy diffusion into the high-k/SiO_2 interface, we analyze the binding energy shift of O1s core-level XPS data of each sample with a different annealing temperature. Figure 3.4(a) and 4(b) show the binding energy shift of O1s core-level XPS data of Dy_2O_3 and co-sputtered DyHfO samples annealed at 500 °C PDA. The main peak position of Dy_2O_3 and co-sputtered DyHfO samples increase to the higher binding energy after 500 °C temperature annealing. The binding energy shift toward a higher energy indicates Dy-silicate formation at the Dy_2O_3/SiO_2 interfaces when DyO films are deposited on the Si directly and annealed at 500 °C [14-15]. However, in the bi-layered DyO/HfO case shown in Figure 3.5, the peak binding energy was lowered after 500 °C annealing from the peak position of as-deposited state, but it was shifted to a higher binding energy after 900 °C annealing, meaning that Dy silicate was not formed at the HfO_2/SiO_2 interfaces after 500 °C annealing, but formed after 900 °C PMA. This result suggests that the thermal energy given by 500 °C process is not sufficient for Dy diffusion and subsequent silicate formation. We believe that this Dy-O-Si bonding is closely associated with the dipole formation since the V_{FB} shift in Dy_2O_3/SiO_2 is caused by the dipole and coincides with the Dy-silicate formation. Therefore, the magnitude of the Dy-induced dipole depends on the amount of the diffused Dy into the high-k/SiO_2 interface. Devices with DyO-capped HfSiON and SiON showed different V_{TH} shifts of 300mV and 500mV, respectively [7], which indicating that different amounts of Dy are diffused into the SiO_2/Si interface in HfSiON and SiON.

(a)



(b)

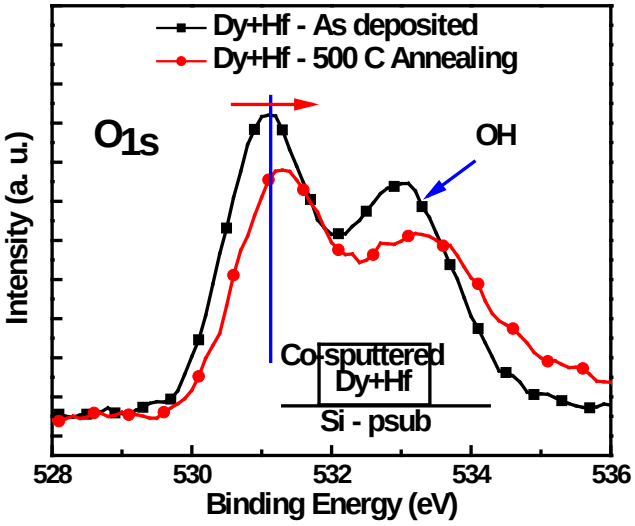


Figure 3.4. The binding energy (BE) shift of O1s core-level XPS data of (a) Dy_2O_3 and (b) co-sputtered DyHfO sample were compared before and after 500 °C PDA. The BE shift to a higher energy indicates the formation of Dy silicate at the high-k/SiO_2 interfaces.

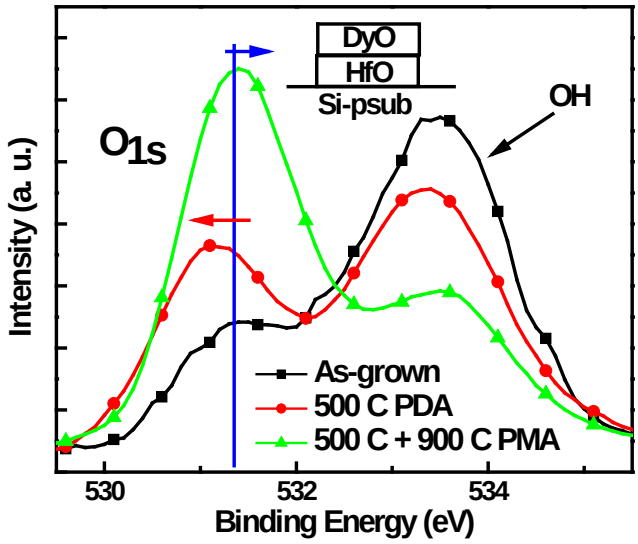


Figure 3.5. The binding energy shift of O1s core-level XPS data of DyO/HfO bi-layered sample was analyzed. Peak binding energy was lowered after 500 °C temperature annealing from the peak position of as-deposited state, but it was shifted to the even higher binding energy than the original peak of un-annealed sample after 900 °C temperature annealing. It suggests that Dy-silicate was formed after 900 °C PMA, but Dy-silicate was not formed at the high-k/SiO_2 interfaces after 500 °C annealing.

The direction of the dipole induced in the DyO/HfO/SiO_2 system can be estimated with the difference in the Sanderson's electronegativity (EN) of the capping material and the bottom reference layer [16]. If the value in Sanderson's EN of the capping layer is smaller than the one of the bottom reference material, the threshold voltage will be shifted in a negative direction. On the other hand, when the capping layer's EN is larger than the bottom one, a positive shift of V_{TH} is predicted. The calculated electronegativity of the Dy_2O_3 by Sanderson criterion is 2.27, whereas the Pauling's electronegativity of

Dy_2O_3 is 1.22, as summarized in Table 3.1. Therefore, the EN of Dy_2O_3 (2.27) is smaller than the one of HfO_2 (2.49). This means that the threshold voltage shift will be lowered from the reference V_{TH} of bottom layer, which is consistent with our data. In addition, the strength of the dipole is related to the amount of Dy dipoles created by Dy-silicate at the interface corresponding to the annealing temperature.

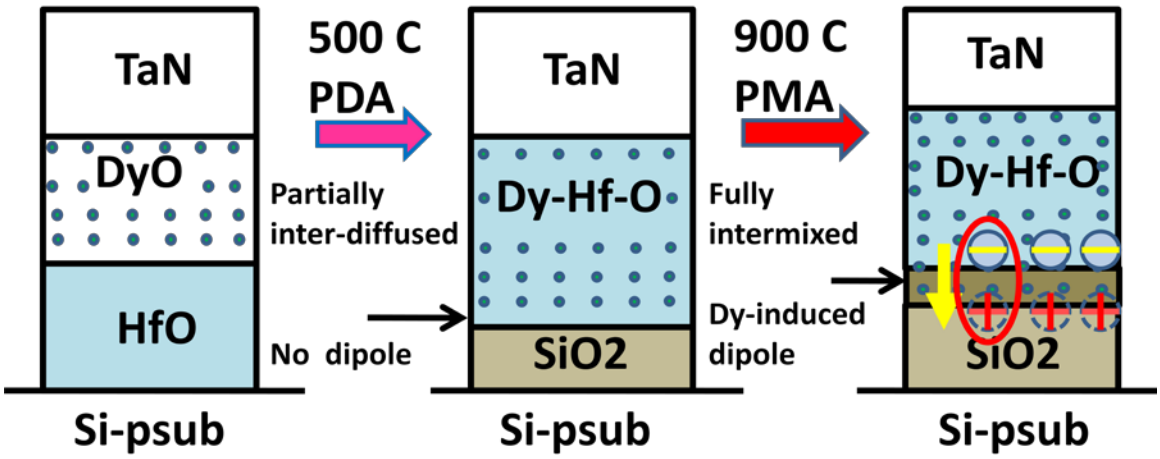
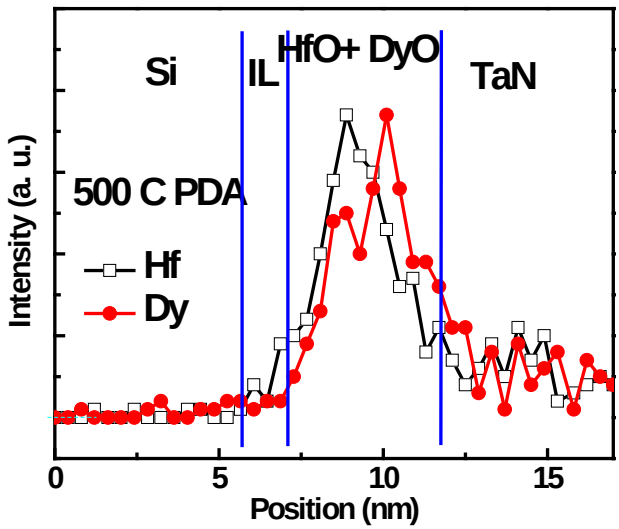


Figure 3.6. The temperature-dependent Dy diffusion and diffusion-driven Dy-induced dipoles formation process of the DyO/HfO bi-layer sample is illustrated in this schematic. DyO layer and HfO layer was partially intermixed, but did not form Dy-silicate at the high-k/SiO_2 interfaces for 500 °C annealing. After 900 °C PMA, DyO layer and HfO layer was fully intermixed and Dy-silicate were formed at the high-k/SiO_2 interfaces. This implies that Dy-silicate related bonding is associated with the dipole formation, which modulate the V_{FB}/V_{TH} shift of Dy-Hf-O/SiO_2 system.

As HfO_2 is known to possess the dipole moment [9], the net dipole moments induced by ionic Hf-related bonding and by Dy-silicate related bonding would determine the flatband and threshold voltage shift in Dy-Hf-O/SiO_2 system [17-18]. However, the Dy-induced dipole becomes dominant during high temperature annealing due to the different nature of the Dy- and Hf-induced dipoles. While more Dy atoms diffuse into the interface and formed Dy-silicate, Hf atoms are believed to be released from the original HfO_2/SiO_2 interface [3]. Consequently, the areal density of the Dy-silicate accounts for the net amount of Dy-induced dipole, resulting in the V_{FB}/V_{TH} shift. The schematic depicted in Figure 3.6 illustrate the temperature-dependent Dy diffusion and diffusion-driven Dy-silicate formation process. To support the diffusion of Dy, we measured the STEM EELS and STEM EDX of DyO/HfO/Si p-sub samples annealed at 500 °C PDA and 900 °C PMA, respectively. We compared the Dy and Hf profile in STEM EDX data for each temperature (Figure 3.7). According to STEM EDX data, Dy atoms and Hf atoms are only partially intermixed at the 500 °C PDA, but Dy intermixing with SiO_2 is not noticeable in the interfacial layer. However, a gradual Dy depth profile is clearly extending into the interfacial layer after 900 °C PMA. This agrees with the formation of Dy-silicate at the interfacial layer by XPS.

(a)



(b)

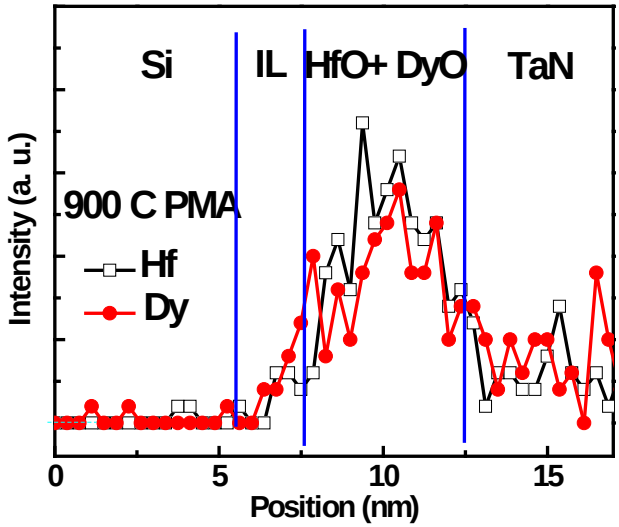


Figure 3.7. STEM EDX analysis of DyO/HfO/p-Si sample annealed at 500 °C and 900 °C. Dy atoms and Hf atoms are partially intermixed after 500 °C PDA, but Dy intermixing with SiO_2 is not noticeable in the interfacial layer (a). However, a gradual Dy depth profile clearly extending into the interfacial layer after 900 °C PMA can be seen (b). This indicates the formation of Dy-silicate at the interface, which is contributing to the Dy-induced dipole, resulting in the V_{TH}/V_{FB} shift.

3.4 ELECTRICAL CHARACTERISTICS OF DYO/HFO MOS DEVICES

Figure 3.8 compares the Ig-Vg characteristics of DyO/HfO and HfO_2 only sample. We obtained comparable over-drive current, subthreshold swing (~70 mV/dec) and lower V_{TH} (~1 mV) with DyO/HfO stack. EOT of this sample is around 1.38nm and the equivalent gate oxide thickness (Tox_gl) is around 1.72nm. The over-drive current, normalized by width and measured at 1V over-drive voltage, is improved. The electron mobility with respect to EOT was plotted to check the mobility degradation in terms of the Dy-induced dipole, where the electron mobility was chosen at 1 MV/cm effective field (Figure 3.9). The effective electron mobility is enhanced by Dy incorporation. According to the reference of [18], the mobility degradation at low fields comes from the dipole layer formed at the HfO_2/SiO_2 interface rather than from remote phonon scattering. This dipole layer is also known to be responsible for the anomalous V_{FB} and V_{TH} shift in HfO_2 MOSFETs. However, based on the result, Dy-induced dipole does not seem to degrade the electron mobility similarly to the La-induced dipole case where mobility degradation was interpreted by the thinning of the interfacial layer (IL) rather than the La dipole [4]. This means that the Dy-induced dipole helps reduce the degradation of the effective electron mobility in HfO_2. Data suggests that we may keep scaling down the EOT without degrading mobility, while maintaining the lower leakage current and oxide wear-out by Dy incorporation. Further research is being conducted to check the mobility degradation in terms of the interfacial layer (IL) scaling down (or EOT scaling down).

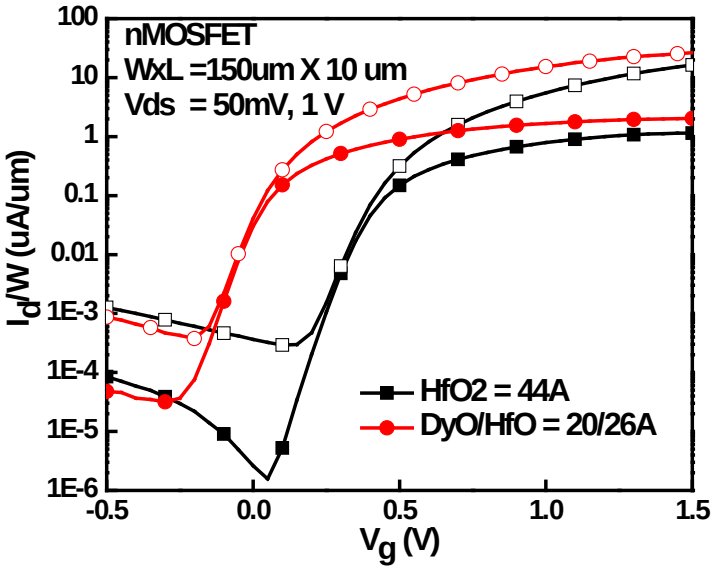


Figure 3.8. The comparable over-drive currents, subthreshold swing (~70 mV/dec) and lower V_{TH} (~1 mV) were obtained from the DyO/HfO=20Å/26Å sample. EOT of this sample is around 1.38nm and the equivalent gate oxide thickness is around 1.72nm. The over-drive current, normalized by width and measured at 1V over-drive voltage, is improved.

.

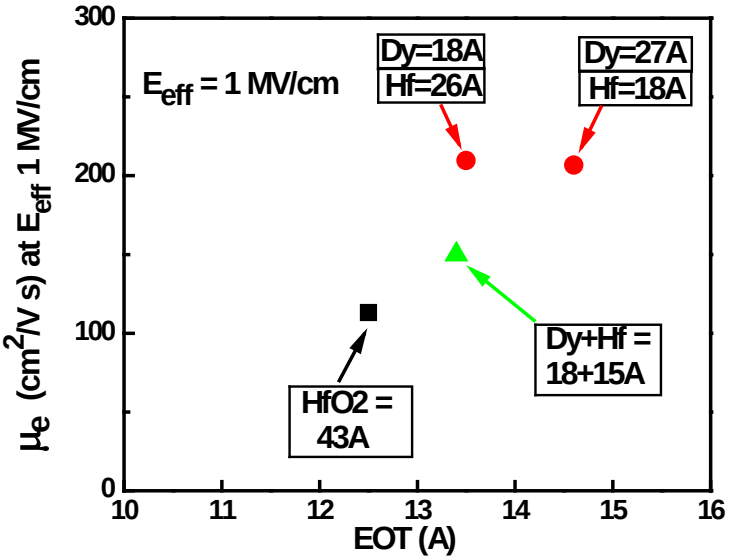


Figure 3.9. The Dy-induced dipoles have an effect on reducing the effective electron mobility degradation. The Dy-induced dipole does not seem to degrade the electron mobility similarly to the La case.

3.5 SUMMARY

Dy-incorporated HfO_2 gate oxide nMOS devices were fabricated for CMOS applications and investigated for the mechanism of V_{FB}/V_{TH} shift in a systematic approach. We observed that the Dy atoms formed Dy-silicate at the high-k/SiO_2 interfaces, resulting in the Dy-induced dipole formation. Dy-induced dipoles at the high-k/SiO_2 interfaces caused the negative flatband shift of co-sputtered DyHfO. In the DyO/HfO/p-Si bi-layered sample, the diffusion of Dy into the interfacial layer was

determined by the annealing temperature. After 900 °C PMA, DyO and HfO were fully intermixed and form the Dy-silicate, which contributes to the Dy-induced dipole. Meanwhile, since the driving force of Dy diffusion is insufficient to form the Dy-silicate at the high-k/SiO_2 interfaces after 500 °C annealing, the flatband voltages of DyO/HfO/Si p-sub MOS capacitor annealed at 500 °C were the same as the flatband voltage of HfO_2. This implies that the Dy-induced dipoles by the Dy-silicate related bonding at the high-k/SiO_2 interfaces play a crucial role in controlling the V_{FB} shift in DyO/HfO MOS device. We support this Dy-silicate at the interface with XPS data and STEM EDX data. Dy-induced dipole doesn't seem to degrade the electron mobility.

CHAPTER 4

REDUCED GATE LEAKAGE CURRENT AND CHARGE TRAPPING CHARACTERISTICS OF DYSPROSIUM (DY) INCORPORATED HFO_2 DEVICES

4.1 INTRODUCTION

Charge trapping characteristics such as positive bias temperature instability (PBTI) also improved during constant voltage stress at room and high temperature. However, the mechanism responsible for the reduced leakage current and charge trapping characteristics of Dy incorporated HfO_2 gate dielectric device was not reported yet. Most HfO_2-based dielectrics suffer from charge trapping/detrapping during stress and it is reported to be strongly polarity-dependent due to the inherent asymmetry of the bi-modal stack [7-8]. Even though there is controversy about the polarity issue, the reliability of the high-k dielectrics is believed to be dominated by the breakdown of the interfacial layer rather than the high-k itself. Intrinsic effects, rather than the extrinsic, also dominate time-dependent dielectric breakdown (TDDB) [9-10].

In this study, we compared the characteristics of Dy incorporated HfO_2 (DyO/HfO) and HfO_2 gated n-MOSCAP by measuring the gate leakage currents and capacitances with various voltage stresses and by performing the time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) with a various constant voltage stress. To clarify the reason for the reduced leakage current and charge trapping characteristics of the Dy-doped HfO_2, the effective barrier heights of Dy_2O_3 and

DyO/HfO oxide were extracted from the Fowler Nordheim (FN) tunneling current. Stress-induced leakage current (SILC) and stress-induced flatband shift was analyzed for the charge trapping characteristics and interpreted with a proposed band diagram [11-12]. TZDB and TDDB were performed with small area capacitors to ensure intrinsic breakdown, and the Weibull slope was obtained [11, 13].

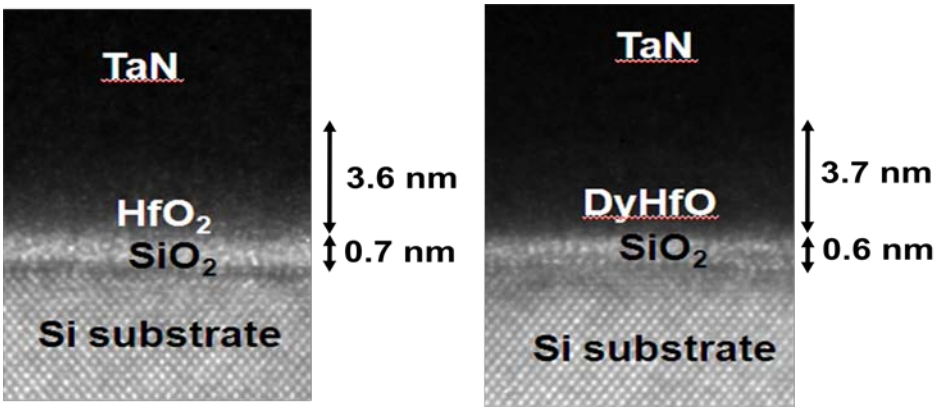


Figure 4. 1. Cross sectional view of HRTEM for the HfO_2 and DyO/ HfO sample, and the interfacial layer is 0.7 nm and 0.6 nm, respectively.

4.2 GATE LEAKAGE CURRENT

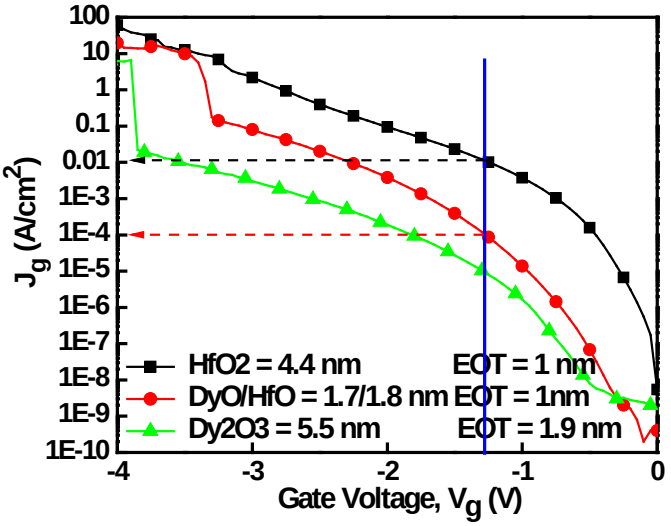
The gate leakage currents for DyO/HfO and HfO_2 sample having a 1nm EOT are compared. As shown in Figure 4.2(a), the leakage current is reduced in Dy incorporated HfO_2 compared to HfO_2. To understand the reduction of leakage current, we draw the F-N plot to extract the effective barrier height of Dy_2O_3. Fowler Nordheim (FN)

tunneling current is the flow of electrons through the triangular potential barrier deformed by the external high field. FN currents are given by

$$J_{FN} = A E_{OX}^2 \exp\left(\frac{-B}{E_{OX}}\right) \quad (1)$$

where A = $\frac{q^3(m/m_{OX})}{8\pi h \Phi_B}$ and B = $\frac{8\pi\sqrt{2m_{OX}\Phi_B^3}}{3qh}$. Φ_B is an effective barrier height that considers barrier height lowering and quantization of electrons at the semiconductor surface. m_{OX} is the effective mass in oxide [15]. We used the E_{ox} = $(Vg-V_{fb}-\varphi_s)/EOT$ to calculate the electric field, where φ_s is the surface potential and consists of the gate and substrate surface potential. This surface potential is negligible since it is operating in an accumulation mode. The effective mass of electrons in HfO_2 is reported as 0.2 [16]. Even though the effective mass of electrons for Dy_2O_3 is unknown, 0.2 is enough to estimate the effective barrier height of the Dy_2O_3 roughly. By the fact that the effective mass in oxide is dependent on the bandgap of the oxide, the effective mass of Dy_2O_3 is lower than 0.2 since the bandgap of Dy_2O_3 is 4.8eV and that of HfO_2 is 6 eV. This means that the effective barrier height of Dy_2O_3 should be even higher than the one calculated with 0.2 effective mass in oxide. The effective potential barrier height ($\sqrt{\Phi_B^3}$) is directly related to the slope (B) extrapolated from the F-N plot shown in Figure 4.2(b). So the steeper the extrapolated slope in the F-N plot, the higher the effective barrier height. The estimated effective barrier height for Dy_2O_3 and HfO_2 is 2.32 eV and 1.43 eV, respectively.

(a)



(b)

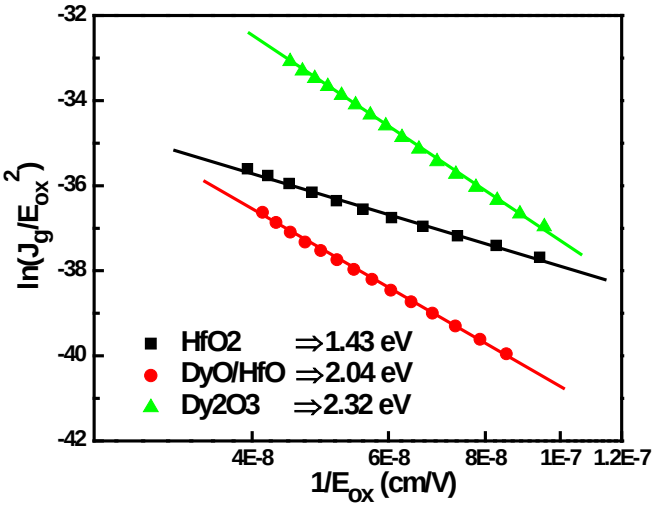


Figure 4. 2. The leakage current density of the HfO_2 and Dy incorporated HfO_2 sample having 1nm EOT are compared (a). The effective potential barrier height is calculated for Dy_2O_3 and HfO_2 samples from the F-N plot to understand the reduction of the leakage current (b). The estimated effective barrier height for Dy_2O_3 and HfO_2 is 2.4 eV and 1.5 eV, respectively.

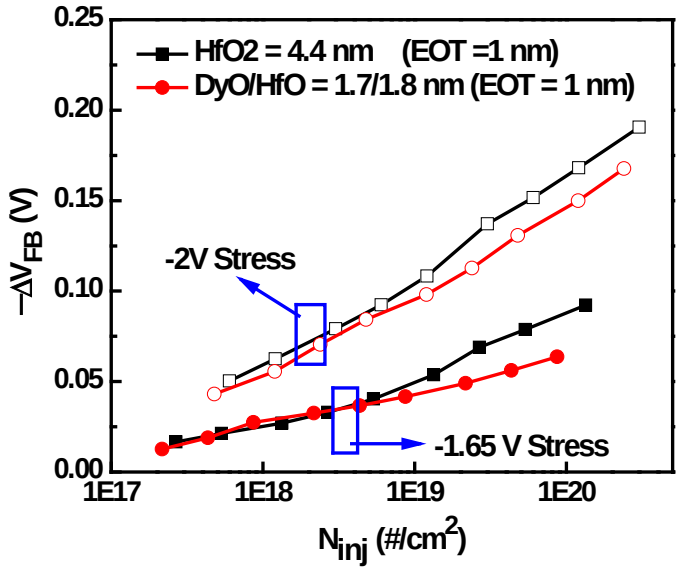
Around 0.9 eV difference in the barrier height characterizes the reduction of the electron tunneling currents and the charge injection since the direct tunneling currents is reciprocally proportional to the barrier height. Thus, the extracted effective barrier height of the DyO/HfO=1.7/1.8 nm sample is 2.04 eV. The 0.6 eV difference in the effective barrier height of the DyO/HfO=1.7/1.8 nm sample compared to HfO_2 accounts for the lower electron tunneling current, resulting in the reduced gate leakage currents.

The EOT and V_{FB} of the Dy-Hf-O system are dependent on the Dy concentration. For example, the EOT of the co-sputtered DyHfO samples described in Ref. 5 increased according to the Dy concentration because of the lower dielectric constant of the Dy_2O_3 and the Dy-silicate at the interface. This Dy-silicate formed at the interface also shifted the flatband of the co-sputtered samples. However, the EOT increase in the DyO/HfO bi-layered oxide can be minimized by delaying the Dy-silicate formation which has a lower dielectric-constant and can be controlled by the annealing temperature. As a result, the EOT of the DyO/HfO sample annealed at 500 °C PDA is comparable to the HfO_2 sample. The V_{FB} shift is also similar to the HfO_2 since Dy diffusion is insufficient to form Dy-silicate at the interface at this annealing temperature. This increased barrier height of Dy-doped HfO_2 also explains the improved charge trapping characteristics, such as stress-induced flatband shift and SILC.

4.3 STRESS-INDUCED CHARGE TRAPPING CHARACTERISTICS

To examine the charge trapping characteristics, various stresses are applied to the HfO_2 and DyO/HfO sample having 1nm EOT. Stress-induced flatband voltage and stress-induced leakage current (SILC) are measured with the same electric field to do a fair comparison. According to the stress-induced flatband voltage data shown in Figure 4.3(a), hole trapping in oxide are observed for both HfO_2 and DyO/HfO sample, since all C-V curves are shifted in a negative way when the negative voltage stresses applied on the gate. When the hole currents are tunneling through the oxide from the accumulated hole in the Si-substrate, some amounts of holes are trapped in oxide from the hole tunneling currents during the stress. To compare the charge trapping, we plot the shifted V_{FB} verse the injected charge density, N_{inj}. Initially, at lower level charge injection, the charge trapping is not severe for both samples, but trap generation rate increases differently at the high level injection. HfO_2 sample shows a higher trap generation rate than DyO/HfO. This decreased hole trapping can be explained by the reduced hole tunneling current and reduced hole trap density. The hole capture cross-section is also believed to be reduced by Dy incorporation, resulting in lower trap generation. And this trap generation rate is dependent on the stress voltage, and is related to the oxide wear-out. The trapped holes in the oxide could enhance the electron tunneling current from the TaN electrode, or reduce the hole tunneling current. The effective field enhanced by the trapped holes in oxides can modify the energy band, which induces the increase of the electron tunneling through hopping when the effective barrier height of the oxide is low. This, in turn, results in a gradual increase of the leakage current due to SILC.

(a)



(b)

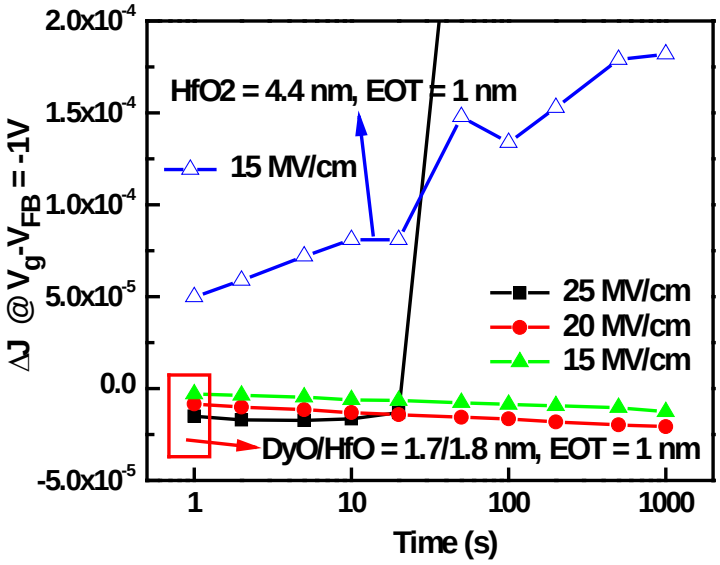


Figure 4. 3. (a) Stress-induced flatband shift shows a hole trapping in oxide and (b) stress-induced leakage current (SILC) characteristics in HfO_2 and DyO/HfO show a different mode for the oxides wear-out and breakdown. SILC in HfO_2 sample is dominated by the increase of the electron tunneling currents, leading to wear out the oxide gradually into a soft breakdown mode. However, The hole tunneling currents lessened by hole trapping account for the decrease of SILC of Dy incorporated HfO_2 until it went to a hard breakdown.

If the effective barrier height of the oxide is high enough to block a further increase of the electron tunneling from the TaN gate, the trapped holes in the oxide can reduce the hole tunneling currents. This flatband shift by the hole trapping in the oxide is related to the SILC characteristics and will be illustrated with the band diagram.

SILC characteristics in HfO_2 and DyO/HfO show different behaviors from the perspective of oxide wear-out and breakdown. SILC in HfO_2 keeps increasing severely, eventually leading to an oxide breakdown, but does not show an abrupt increase of current such as a hard breakdown mode. On the contrary, gate leakage in the DyO/HfO sample decreases until hard breakdown occurs. The mechanism of charge trapping for both samples can be explained with the band diagram in Figure 4.4 in relation to the electron tunneling current and hole trapping by the hole tunneling. For the HfO_2 case, trapped holes enhance the electron tunneling from the TaN gate through the thinned triangular barrier because of the lower barrier height. Hence, SILC in HfO_2 sample, dominated by the increase of the electron tunneling currents, kept increasing up to an oxide breakdown, distinct from a hard breakdown. On the other hand, the increased barrier height in Dy-doped HfO_2 inhibits a further increase of the electron tunneling from the TaN gate, and trapped holes reduce the hole tunneling currents, resulting in a negligible SILC. Therefore, the reduced hole tunneling currents and the reduced hole trap density determine the SILC characteristics of Dy-doped HfO_2, and the percolation path caused by the high voltage stress and high level charge injection breakdown the dielectric eventually**.** The lower trap generation rate and reduced leakage current of the Dy-doped

HfO_2 dielectric are responsible for the improved charge trapping characteristic and reliability such as TZDB and TDDB.

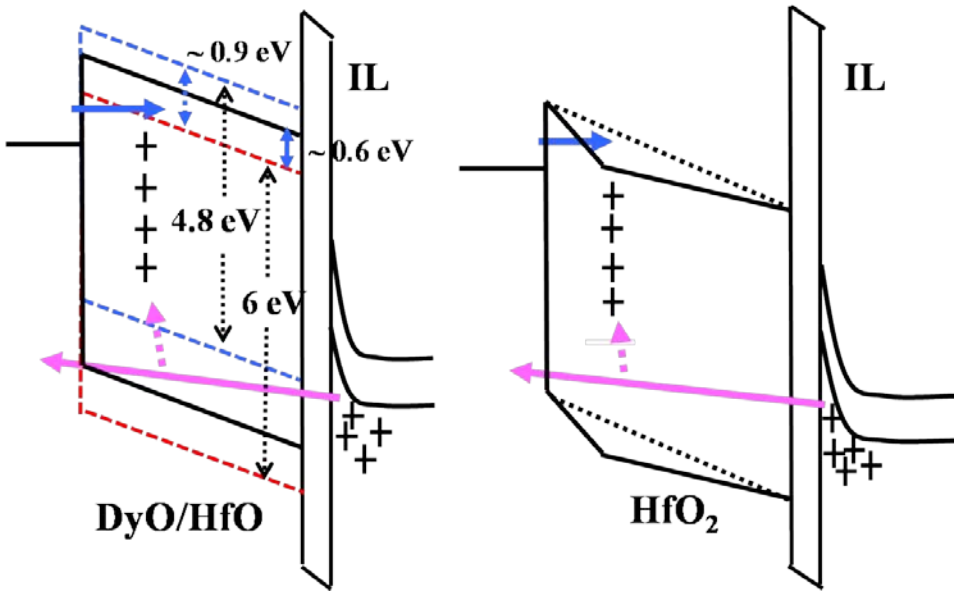


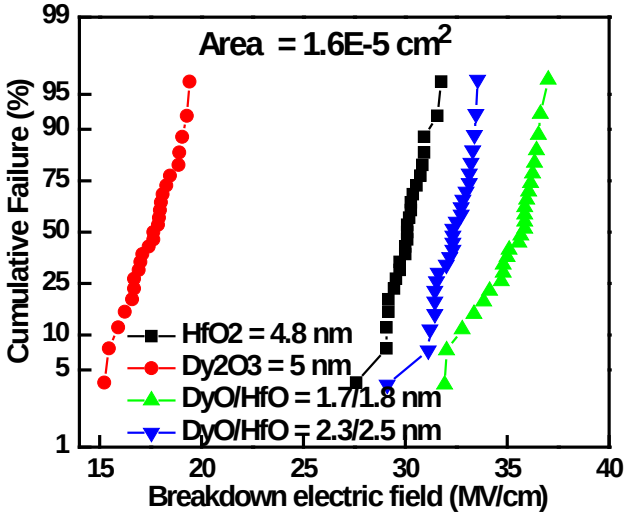
Figure 4. 4. The lower barrier height of HfO_2 accounts for the electron tunneling currents enhanced by the buildup of hole charges trapped in oxide, which contribute to the increase of SILC, leading to a soft breakdown. However, the increased barrier height in Dy-doped HfO_2 inhibit the electron tunneling from the TaN gate, and trapped holes lessen the hole tunneling currents, resulting in the decrease of the gate leakage until it went to a hard breakdown during the stress.

4.4 DIELECTRIC BREAKDOWN

To characterize the defect-related (or extrinsic and B-mode) and intrinsic (C-mode) breakdown field, TZDB is usually measured by the ramp-voltage breakdown test.

The defect-related breakdown field increases with the decrease of oxide thickness, but the separation of intrinsic mode and defect-related mode is difficult in the case of thin oxide. In Figure 4.5 (a), we compare the breakdown field of the HfO_2, Dy_2O_3 and Dy incorporated HfO_2 samples. Even though HfO_2 and Dy_2O_3 samples have the lower breakdown field, the increased breakdown field is attained for DyO/HfO = 1.7/1.8 nm and DyO/HfO = 2.3/2.5 nm samples. Defects created during the fabrication processes might be one of the reasons for the lower breakdown field of Dy_2O_3 and HfO_2 samples. The thinner DyO/HfO sample has a highest breakdown field, which implies that defects can be controlled by the oxide physical thicknesses. The lessened trap generation rate and charge trapping are responsible for reduced leakage current in Dy-doped HfO_2 dielectric, and result in the high dielectric breakdown strength. The lower barrier height of HfO_2 characterizes the electron tunneling currents enhanced by the buildup of hole charges trapped in oxide, which contribute to the increase of SILC, leading to a severe increase of leakage current up to an oxide breakdown, distinct from a hard breakdown mode. Breakdown voltage for DyO/HfO=1.7/1.8 nm having 1nm EOT is 4.1 V, the Weibull slope is 2 and -2.1 V operating voltage is achievable for a 10-year lifetime (Figure 4.5). Considering the fact that the interfacial layer limits the dielectric reliability and results in low Weibull slopes for the gate injection case [9, 14], the interfacial layer created by incorporation of Dy into the HfO_2 might determine the Weibull slope. Therefore, the improved charge trapping and SILC characteristics by the increased effective barrier height of DyO/HfO sample enable the longer lifetime of the dielectric at the same operating vdtage.

(a)



(b)

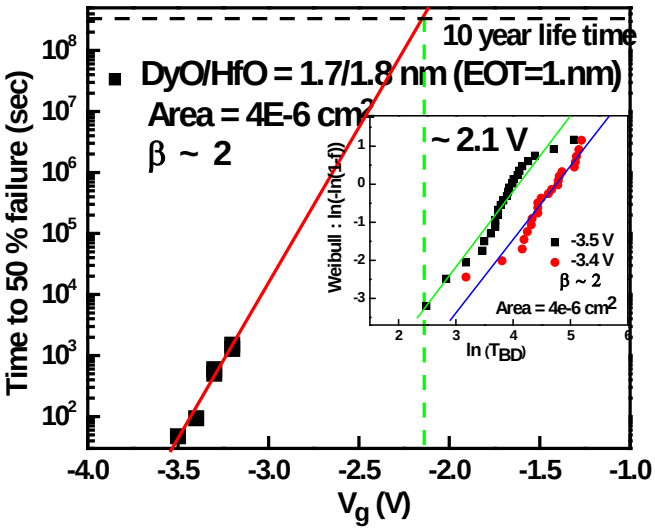


Figure 4.5. The time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) with a various constant voltage stress were performed. Breakdown field distribution for Dy_2O_3, HfO_2 and Dy incorporated HfO_2 sample are compared (a). Breakdown voltage for DyO/HfO=1.7/1.8 nm having 1nm EOT is 4.1 V, the Weibull slope is 2 (inset in Figure 5 (b)) and -2.1 V operating voltage is achievable for 10 year lifetime (b).

4.5 SUMMARY

Dy-incorporated HfO_2 gate dielectric with TaN gate nMOS devices were developed for high performance CMOS applications. The effective barrier height of Dy_2O_3 is extracted from the F-N plot to understand the reduction of leakage current of the DyO/HfO sample. We investigated the mechanism of the charge trapping characteristics with a band diagram, and discussed the reliability of dielectric breakdown. The increased effective barrier height of DyO/HfO sample compared to HfO_2 accounts for the lower gate leakage and the less charge trapping, such as stress-induced flatband shift and SILC. The negative flatband shifts by the gate voltage stresses show hole trapping in oxide for both HfO_2 control and Dy-incorporated HfO_2 nMOSCAP. The reduced hole tunneling currents and hole trap density account for the decrease of SILC of Dy-incorporated HfO_2 and a higher oxide breakdown field. However, in the case of HfO_2, the increased electron tunneling currents induced by hole trapping and the lower barrier height contribute to the severe increase of SILC, leading to an oxide breakdown, distinct from a hard breakdown mode. Breakdown voltage and Weibull slope were estimated for the DyO/HfO sample having 1nm EOT and a relatively low 10-year operating voltage of -2.1 V was demonstrated.

CHAPTER 5

TEMPERATURE DEPENDENT TIME DEPENDENT DIELECTRIC BREAKDOWN FOR THIN EOT DYSPROSIUM (DY) DOPED HFO_2 DIELECTRIC DEVICE

5.1 INTRODUCTION

Among all of the reliability issues associated with high-k dielectrics, Time Dependent Dielectric Breakdown (TDDB) has been most intensively studied. The reliability of high-k gate dielectrics is dominated by the breakdown of the interfacial layer rather than the high-k layer itself. The fact that the interfacial layer plays a strong role in the failure process is reported in studies of lifetime extraction [1]. The Weibull failure time dispersion β dependence on the overall dielectric thickness is much less pronounced in high-k stacks compared to SiO_2. The measured β values do correlate well with the interfacial thickness [1]. To understand the mechanism of the intrinsic dielectric breakdown, we measured the TDDB by varying the stress voltage and temperature, and analyzed data by using two models, the thermochemical breakdown model (E model) and the hole-induced breakdown model (1/E model) [2]. However, these models that were developed for SiO_2 cannot be directly applied to the thin EOT high-k dielectrics because the charge trapping phenomena and its conduction mechanisms are behaving differently. For example, the higher trap generation rate in bias-temperature instability (BTI), stress-induced leakage current (SILC), and higher leakage current before breakdown in these high-k dielectrics complicates the study on the time dependent dielectric breakdown

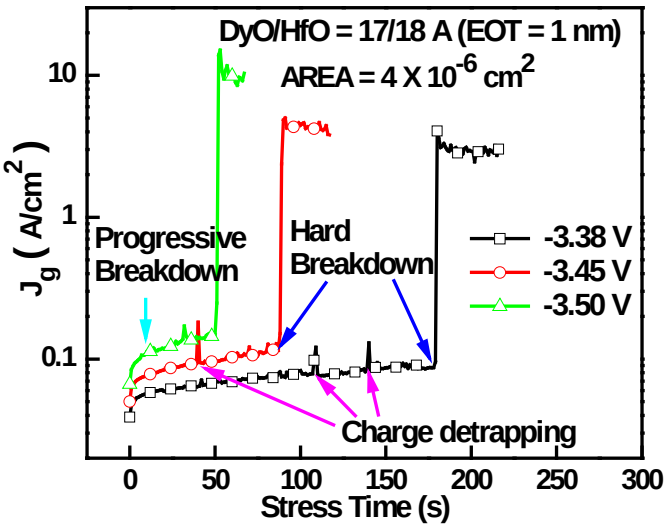
(TDDB) [3-5]. Furthermore, the charge trapping/detrapping in high-k dielectrics is related to the wear-out of oxide in bulk as well as at the interface, and its conduction mechanism often follows the Poole-Frenkel emission. In fact, the higher leakage current in the thinner HfO_2 gate dielectric device and the irregular distribution of the soft breakdown and hard breakdown modes are the reasons for the poor Weibull slope [6].

We investigate the gate leakage current of thin EOT Dy incorporated HfO_2 gate oxide and HfO_2. The lower barrier height of HfO_2 (~1.5 eV) characterizes the electron tunneling currents enhanced by the buildup of hole charges in oxide and the increase of stress-induced leakage current (SILC), leading to a soft breakdown. However, Dy incorporation into HfO_2 increased the effective barrier height in DyO/HfO/Si p-sub sample since the effective barrier height of Dy_2O_3 is high (~ 2.32 eV), which enable to block the electron tunneling from the TaN gate, and trapped holes reduce the hole tunneling currents, resulting in the decrease of the gate leakage during the stress. This reduction of gate currents accounts for the wear-out, breakdown mechanism and Weibull slope at high temperature. Furthermore, the lower leakage current and less charge trapping in Dy-doped HfO_2 sample enable the study of the intrinsic time dependent dielectric breakdown (TDDB) [3]. In this report, we describe the breakdown mechanism of thin DyO/HfO sample based on the power law ($V^{-n(T)}$). We discuss the voltage acceleration factor extracted from the power law, and expand this model to include the temperature dependency to obtain the voltage dependent activation energy.

5.2 PHYSICAL MODEL OF THE THIN EOT DYO/HFO DEVICE FOR TDDB

When high voltage is applied to the gate, electrons tunnel through the oxide. In the gate, these energetic electrons cause impact ionization to produce holes, resulting in hole trapping inside the oxide and creating defects by inelastic heat [3, 12]. This mechanism is similar to the Anode Hole Injection model except for the fact that the excited element is not the electron-hole pair but the interfacial Si-H bond [13]. For the HfO_2 case, the probability of electron tunneling is higher than for the DyO/HfO bi-layered sample because of the lower barrier height, and will be increasing by the hole trapping. Trapped holes in oxides enhance the effective field, which modifies the energy band and causes electron tunneling through hopping. This, in turn, results in a gradual increase of leakage current due to SILC and band diagram describing these phenomena is presented in Figure 4.4 [2, 12]. The SILC current in HfO_2 is too high to do TDDB measurement. On the contrary, the reduced leakage current by the increased barrier height and reduced hole trapping by the lower trap generation rate of DyO/HfO sample enable to do the oxide breakdown. According to the percolation theory, more traps are created in the oxide with continuous stress and eventually these traps are connected like a chain between the cathode and anode, sometimes called percolation path, leading to high leakage current, which results in oxide breakdown [2].

(a)



(b)

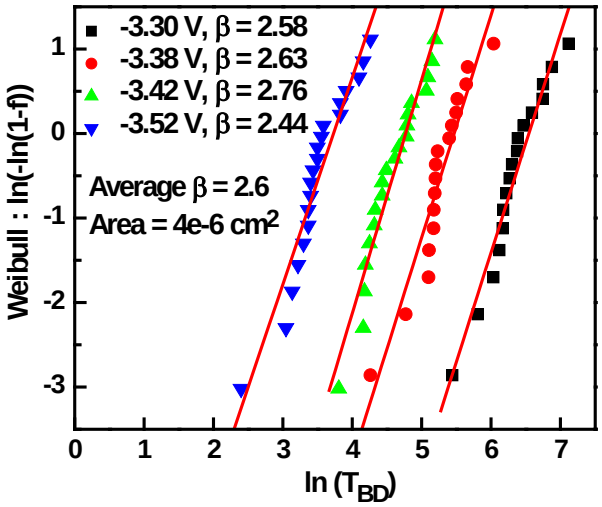


Figure 5. 1. The noise in currents occur right after the stress and the peaks in currents is called a progressive breakdown (PBD) and prevails for oxide thinner than 20 Å. After this failure occurrence, leakage level increase continuously until the hard breakdown (HBD) and is dependent on the applied voltage (a). The Weibull slope β of hard breakdown is obtained for different voltages and their average value (β=2.6) is quite comparable to the same physical thickness of SiO_2 (b).

As shown in Figure 5.1(a), the leakage current was monitored with various constant voltage stresses. The noise in the currents occurring right after the stress and the peaks in the currents happening during the measurement are due to the charge trapping/detrapping in SILC. These increasing noise currents constitute a new kind of failure phenomenon, called progressive breakdown (PBD), and are dominant for oxides thinner than 20 Å [13]. The noise occurrence is randomly distributed all over the device area affecting the area scaling and the Weibull statistics. After the occurrence of failure, the leakage level increases continuously until hard breakdown (HBD) and is dependent on the applied voltage [13]. We observed that PBD and the leakage current level right before the hard breakdown increased as the stress voltage increased. In fact, the PBD was reported to be the initiator of the hard or soft breakdown [14].

Oxide breakdown (BD) is marked by a discontinuity in current or voltage as a result of stress. This onset of gate conduction is usually believed to cause the failure of the circuit employing the broken FET. The occurrence of oxide BD has a random nature and requires a statistical description. Moreover, since it has a “weakest-link” character, the usual choice for the statistical description of the experimental data is the Weibull distribution model, given by

$$F(T_{BD}) = 1 - \exp\left[-\left(\frac{T_{BD}}{\alpha}\right)^{\beta}\right] \quad (1)$$

where F is the cumulative failure probability and TBD is the time-to-breakdown. The characteristic time, α, is the time-to-breakdown at approximately the 63 or 50%, β is the Weibull shape factor, often called Weibull slope. In the Weibull model, a graphical

representation of the data in a ln(-ln(1-F)) versus ln(T_{BD}) yields a straight line [23]. The Weibull slope β of hard breakdown is obtained for different voltages and their average value (β=2.6) is quite comparable to the same physical thickness of SiO_2 in Figure 5.2(b). Since the Weibull slope β is determined by the relative thickness of the oxide and the trap diameter, the thicker oxide has a higher value [2].

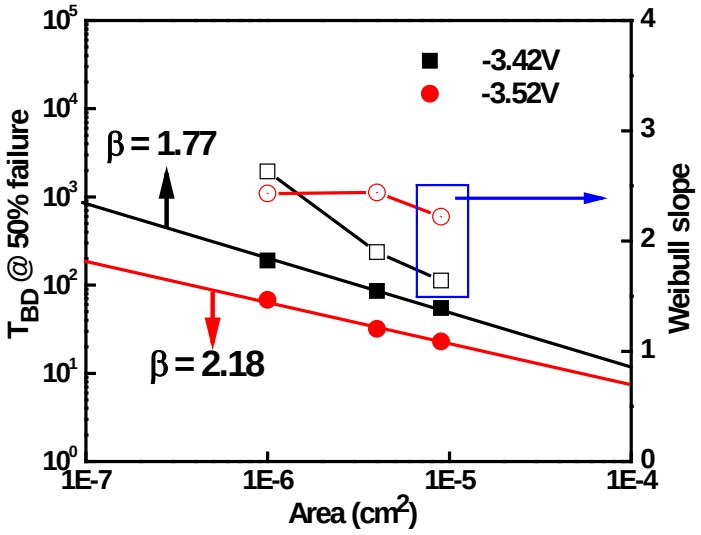


Figure 5. 2. Area dependency of dielectric breakdown time and Weibull slope. High field stress makes the breakdown intrinsic. The area scaling factor (1/β) depends on the electric field. The lower the voltage stresses the higher the scaling factor.

According to the reports in [13], for the thick high-k stack, the Weibull slope of the time-to-breakdown exhibits a good correlation with the SiO_2 interfacial layer thickness. But charge-to-breakdown in the thin high-k stack is higher than the corresponding SiO_2 interfacial layer thickness (10 Å), which probably suggests that the high-k layer plays a

main role in the defect generation probability or in the critical defect density. The reduced defect generation rate and decreased thickness of the trap-rich HfO_2 in the thin EOT DyO/HfO bi-layered stack having the interfacial layer (0.7 nm) can account for the higher value of the Weibull slope. For the same physical thickness, high-k dielectrics have a higher effective electric field at the same voltage than SiO_2, which indicates that high voltage stress makes the dielectric breakdown intrinsic.

The real operating voltage is far lower than the voltage applied for TDDB, so we should consider the high field effect in modeling. Figure 5.2 plots the time-to-breakdown (50%) versus capacitor sizes as a function of different stress voltages. To obtain β, we use the following equation

$$\frac{T_{lifetime}}{T_{test}} = \left(\frac{A_{test}}{A}\right)^{1/\beta} \quad (2)$$

where A_{test} is the area of the test structure and A is the area of real devices [2, 6]. As one can see in Figure 5.2, the area scaling factor (1/β) depends on the electric field. The lower the voltage stresses, the higher the scaling factor. It is also interesting to notice that the Weibull slope is not much different at high voltage. The dielectric breakdown is not intrinsic for larger area capacitors, but it is intrinsic for smaller area capacitors at high voltage stress. This fact is quite important in modeling intrinsic TDDB because when we do accelerated tests to extrapolate the lifetime for a real operating condition, different degradation mechanisms providing different voltage dependence of oxide breakdown can be active at different voltages. In other words, the breakdown mechanism at higher voltage might still be applicable for lower voltages. Therefore, we

should take consideration this fact in building a TDDB model for thin EOT DyO/HfO bi-layered dielectric.

5.3 TDDB MODELS FOR THE HIGH-K DIELECTRICS

The breakdown mechanism of the thin high-k oxide is needed to project the lifetime of oxides under low operating voltages, and to guarantee that products will function well for 10 years within the customer's specific requirements. To begin with, the field dependence of the failure lifetime should be clarified. The E model is called the thermochemical model and attributes the generation of the oxide trap to the interaction of the electric field with weak bonds. The oxygen vacancy is believed to be the cause of polarized Si-Si bonds. Even though the E model has a linear relationship to the electric field, it has less physical basis in relation to the conduction mechanism and a linear field acceleration factor is still questionable [2, 16]. Recently, the power law model has become popular because of the characteristics of the voltage acceleration factor. Since the breakdown of ultra thin oxides is voltage-driven, a few models relating directly to the applied voltage to T_{BD} have been presented [17].

$$T_{BD} = \tau_0 \, V^{-n(T))} \tag{3}$$

The voltage acceleration factor of this model is proportional to n/V, which increases as the voltage decreases [17]. The value of n extracted from our data is 44.54 shown in inset of Figure 5.3, and this value will be used in voltage acceleration factor and the effective activation energy. 1/E model is based on FN tunneling and anode hole injection [15]. It is

well established that one can extract the defect density by using the effective oxide thinning concept. This model can be easily expended to include the temperature dependency. The voltage acceleration factor extracted from 1/E model will be compared with the one from the power law.

5.4 VOLTAGE ACCELERATION FACTOR

As we mentioned before, time-to-breakdown has a strong dependence on the applied bias and it is entirely due to the voltage dependence of the trap generation rate. The physically-based model can provide the expression of trap generation rate from a specific physical phenomenon. Then, the phenomenological models adopt an empirical relation between T_{BD} and stress conditions suggested by the experimental data, without a well-defined mechanism responsible for that relation. It must be pointed out that a comprehensive model is not available. This is because oxide breakdown is a very complex phenomenon, not well understood yet in its microscopic aspects. A sound model for the trap creation process at the microscopic level is needed [2].

One of the key elements that a trap generation rate model has to provide is the voltage acceleration factor γ as defined below [16]

$$\gamma\,(V_G) = -\frac{d\left(\log\left(T_{BD}\right)\right)}{dV_G} = \frac{n}{V_G}\left[\frac{\text{decade}}{V}\right] \qquad \text{for the power law} \qquad (4)$$

It indicates how fast the T_{BD} changes with the applied bias. Thus, it is of fundamental importance for the reliability projection for real operating conditions. We plotted the voltage acceleration factor versus the gate voltage for each model based on our measured

data. According to the E model, the voltage acceleration factor is always constant for all the gate voltage, which indicates the underestimation of the field effect. By comparing the 1/E model, power law as shown in Figure 5.3, it is quite different in the lower voltage region.

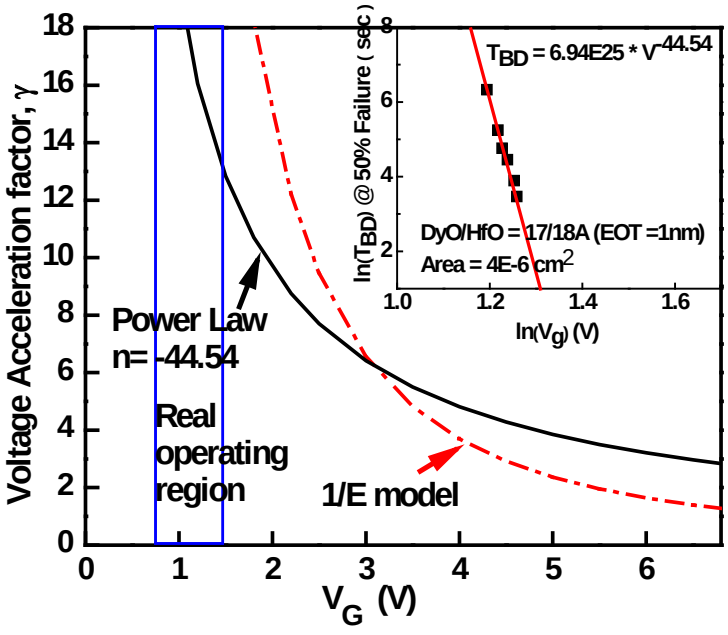


Figure 5. 3. Inset shows the linear relationship in time-to-breakdown and the applied voltage. The voltage acceleration factor is constant for the gate voltage in the E model, which indicates the underestimation of the field effect. The prediction from the 1/E model overestimates for the lower voltage region. The power law predicts a realistic trend in the real operating voltage regime.

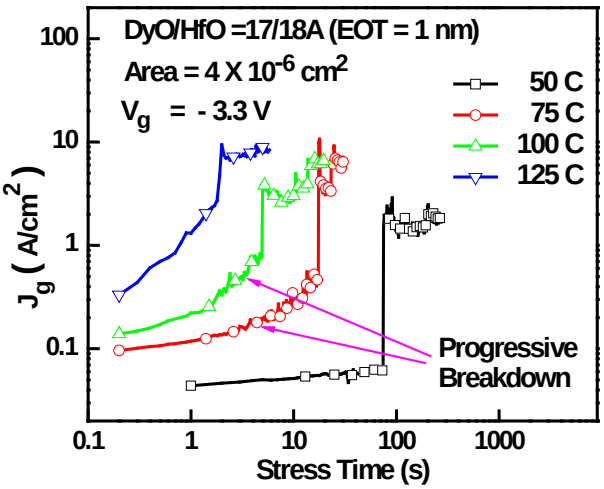
The prediction from the 1/E model is overestimated for the lower voltage region. Meanwhile, the power law shows a reasonable value in the real operating voltage regime. For the reliability projection, the voltage dependence of the failure time is critical. A rapidly increasing lifetime for the high-k metal gate (HK+MG) stacks is the prediction derived by the charge injection models such as hydrogen release (HR), multi-vibrational hydrogen release (MVHR) and anode hole injection (AHI) as the stress voltage is lowered [13]. Recent measurements of the voltage acceleration with decreasing gate voltage are consistent with a charge injection model [18]. The thermo-chemical model applied to explain the high-k dielectric breakdown phenomena predicts a more conservative and pessimistic reliability projection [19]. The increase of the voltage acceleration factor at lower stress voltage is due to the lower trap generation rate. Under the low voltage operation, the electrons often do not have sufficient energy to impact ionize as easily. Most of the holes may be too cold to tunnel back through the oxide, and therefore the number of holes injected back decays exponentially, resulting in a reduced trap generation rate [16]. The reduced trap generation rate in the DyO/HfO bi-layer structure obtained by the measurement of the stress-induced flatband voltage is possibly the main reason for the rapid increase of the voltage acceleration factor [3].

5.4 TEMPERATURE ACCELERATION

The temperature behavior of the breakdown can help determine which layer is first broken down in the high-k stack. According to the report [13], the authors present

results on HfO_2 with metal gate and HfSiO with polysilicon gate. The times-to-breakdown display similar activation energy for both stacks.

(a)



(b)

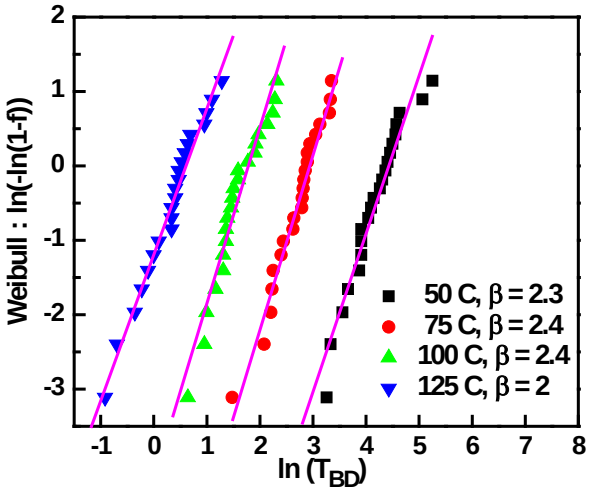


Figure 5. 4. The leakage current (a) and Weibull distribution (b) of the TDDB data at the higher temperature. Temperature has an effect on the progressive breakdown. This means that the higher temperature provided energy for carrier hopping between the localized weak spots.

Furthermore, the activation energies are in agreement with those measured for SiO_2. The similarity of the temperature behavior between these completely different stacks indicates an interfacial layer breakdown. They also conclude that the Q_{bd} shift between both stacks seems to originate rather from a high-k thickness dependence of the defect generation probability that is dependent on gate current density. As shown in Figure 4, we performed the TDDB test at high temperature. The gate current increased during the stress before the hard breakdown at higher temperature. Moreover, temperature has an effect on the progressive breakdown [20]. This means that the higher temperature provides energy for carrier hopping between the localized weak spots. This behavior is consistent with the data reported by Intel Co. on 45 nm Metal gate and high-k transistor stack [21]. The Weibull distribution is still valid at high temperature since the gate leakage currents are reduced in thin EOT DyO/HfO bi-layer structure as we investigated for the thermionic emission study [3]. It has been found that the effective activation energy for the dielectric breakdown is dependent on the electric field and the acceleration factor depends on temperature [15, 22]. The statistical model can be extended to account for the temperature dependence of n and τ_0. The general expression is

$$n(T) = n\left(1 + \frac{\delta}{k}\left[\frac{1}{T} - \frac{1}{300}\right]\right) \quad (5)$$

$$\tau_0(T) = \tau_0 \exp\left(\frac{-E_b}{k}\left[\frac{1}{T} - \frac{1}{300}\right]\right) \quad (6)$$

The power law is easily expanded to include temperature dependency by putting (5) and (6) into (3),

$$T_{BD} = \tau_0 \exp\left(\frac{-E_b}{k}\left[\frac{1}{T} - \frac{1}{300}\right]\right) \times V^{-n\left(1+\frac{\delta}{k}\left[\frac{1}{T} - \frac{1}{300}\right]\right)} \quad (7)$$

where E_b and δ characterize the temperature dependent $\tau_0(T)$ and acceleration factor $\kappa(T)$. The temperature-dependent voltage acceleration factor defined by (4) can also be obtained

$$\gamma\,(V_G, T) = -\frac{d\left(\log\left(T_{BD}\right)\right)}{dV_G} = \frac{n}{V_G}\left[1 + \frac{\delta}{k}\left\{\frac{1}{T} - \frac{1}{300}\right\}\right] \tag{8}$$

This equation indicates that temperature dependent γ is inversely proportional to gate voltage and temperature. Then, if the temperature goes up over room temperature, the voltage acceleration factor decreases. The effective activation energy for the dielectric breakdown is determined from the Arrhenius plot and is defined by

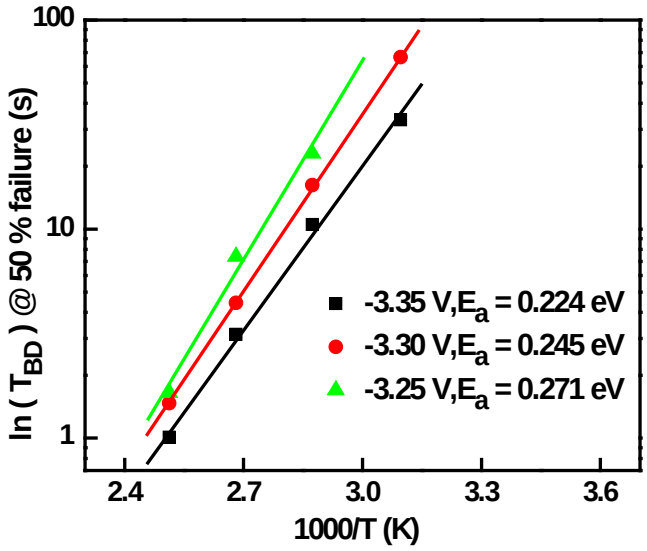
$$E_a \overset{\text{def}}{=} k\frac{d\ln\left(T_{BD}\right)}{d(1/T)} = -E_b - n_0\delta \ln V_G \ \ (\text{eV}) \tag{9}$$

This equation shows that activation energy decreases as the applied field increases. This explains the strong dependency of the gate voltage on the time-to-breakdown. With TDDB data at different temperatures, the activation energy can be extracted from the slope of the Arrhenius plot in Figure 5.5(a). The effective activation energy has the field dependency and can be obtained directly from the linear line in Figure 5.5(b).

$$E_a = 1.644 - 1.175\ \ln V_G \ \ (\text{eV}) \tag{10}$$

By extrapolating the data in Figure 5(b) and using the equation (9), we can determine the temperature characterization parameter E_b and δ is 1.644 and 0.026, respectively. Equation (10) also shows the relationship to the high field effect.

(a)



(b)

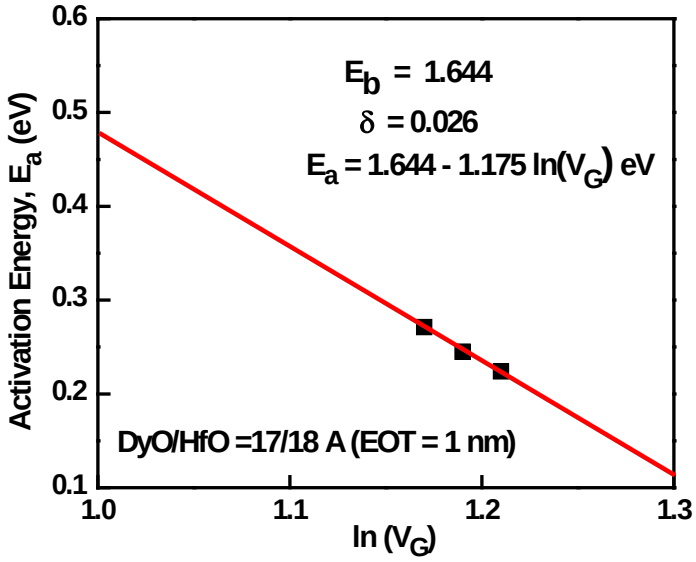


Figure 5. 5. With TDDB data at different temperatures, the activation energy can be extracted from the slope of the Arrhenius plot (a). The effective activation energy has the field dependency and can be obtained directly from the linear slope plotted in (b). The effective activation energy depends on the applied voltage.

5.4 SUMMARY

We discussed TDDB of thin EOT Dy incorporated HfO_2 gate oxide devices. The reduced gate currents account for the improved wear-out, the breakdown mechanism and the Weibull slope at high temperature. According to the MVHR model, the charge-to-breakdown depends on the gate current, which indicates the breakdown of the high-k layer. In gate injection, the gate current increases until hard breakdown after the interfacial layer is worn out first. The intrinsic TDDB of the thin EOT DyO/HfO gate oxide is characterized by the PBD model. At high temperature, PBD becomes worse, which means that the higher temperature causes carriers to hop more easily between the localized weak spots. Based on the power law, we extrapolate the lifetime of the thin DyO/HfO gate oxide having 1nm EOT. The voltage acceleration factor extracted from this model estimating the high field effect predicts the lifetime of the oxide reasonably. Finally, this model is easily expanded to include the temperature dependency. The effective activation energy derived from this model is dependent on the applied gate voltage.

CHAPTER 6

DEVICE CHARACTERISTICS OF HFON CHARGE-TRAP LAYER NONVOLATILE MEMORY

6.1 INTRODUCTION

Floating gate cells suffers from severe interference, known as disturbance, between adjacent cells in sub-43 nm NAND flash memory devices [1]. A conventional SONOS core cell based on Fowler-Nordheim (FN) tunneling cannot be used in high-density NAND flash memory due to poor data-retention characteristics. Nitride-based charge-trapping flash-memory devices have received considerable attention lately because of the fast programming speed, low-power operation voltage, high-density integration, and good reliability characteristics [2]. It was reported that relatively thin tunnel oxides (~ 30 Å) are usable as long as high-k blocking oxide having a high barrier height (Al_2O_3) and TaN gate having high work function are adopted [3-5, 14, 15]. To further improve the vertical scaling and charge-retention characteristics of nonvolatile memory devices, a high-k-based oxide layer is necessary for the charge-trapping layer. The thermal stability and trapping characteristics of HfON in comparison to a HfO_2 trap layer have been reported [6]. However, the physical thickness of the HfON layer needs to be reduced for further scaling and lower programming voltage in sub-43 nm NAND flash-memory devices [7]. To reduce the nitride-trap layer, a thicker top layer is indispensable, not only to inhibit gate injection, but also to block the charges injected by FN tunneling from the silicon, resulting in a higher trapping efficiency and reduced programming voltage.

We demonstrate the material and electrical characteristics of the TaN/ Al_2O_3/HfON/ SiO_2/Si-sub (TANOS) cell flash memory by using a thin HfON as a charge-trapping layer. The thin HfON layer is simply processed by NH_3 nitridation of the thin HfO_2 layer during rapid thermal annealing (RTA). NH_3 nitridation induces a large electron-trap density in the HfON layer. For this reason, NO gas is commonly used, instead of NH_3 in manufacturing to grow the ONO layer when low trap densities are desired [7, 8]. In flash-memory process, NO gas annealing is sometimes used to passivate the shallow traps in nitride by oxidation. Moreover, the high-dielectric constant of the HfON charge-trap layer enhances the electric field in the tunneling oxide, leading to faster erasing and programming speeds due to the higher FN tunneling current. The HfON film has a high intrinsic trap density due to the non-stoichiometry. According to the phase diagram of the Hf-O-N system, we can easily modulate the bandgap and dielectric constant by changing the concentration of nitrogen [9]. We performed material analysis such as spectroscopic ellipsometry, to find out the optical bandgap of HfON thin film, and high-resolution transmission electron microscopy (HRTEM), electron energy loss spectroscopy (EELS), and energy-dispersive x-Ray spectrometry (EDXS) for the composition and layer thicknesses of the TANOS cell. A wide memory window, fast erasing/programming characteristics, and good retention time were achieved. Endurance characteristics were measured by performing stress-induced leakage currents (SILC) analysis. Finally, retention characteristics were measured at different temperatures and the activation energy of the HfON trap layer was extracted from Arrhenius plots. The

distribution of the trap energy levels calculated by using an “amphoteric” model is discussed to explain the charge-loss mechanism [10].

6.2 DEVICE FABRICATION AND ELECTRICAL MEASUREMENT

Thin thermal SiO_2 oxide was grown by dry oxidation at 850° C as a tunnel-oxide layer. Hafnium thin films were deposited by DC sputtering (30 mTorr, Ar ambient, room temperature), followed by rapid thermal annealing for 30 sec at 700° C with NH_3 gas at atmospheric pressure to incorporate nitrogen in HfO_2. Atomic-layer deposition (ALD) of Al_2O_3 with different physical thickness was deposited on the thin HfON layer to be optimized as a blocking oxide. TaN and Al metal were patterned after deposition as a gate electrode and the backside contact, respectively.

Spectroscopic ellipsometry (SE) was used to find the optical bandgap and dielectric constant of the HfON thin film. HRTEM, EELS, and EDXS measurement were done on cross-sectioned samples to determine the composition of each layer. Electrical characterization was performed using, a HP4194A impedance/gain-phase analyzer and HP4156A semiconductor-parameter analyzer. Equivalent-oxide thickness (EOT) and flatband voltage were extracted from measured C-V curves using the NCSU CVC program.

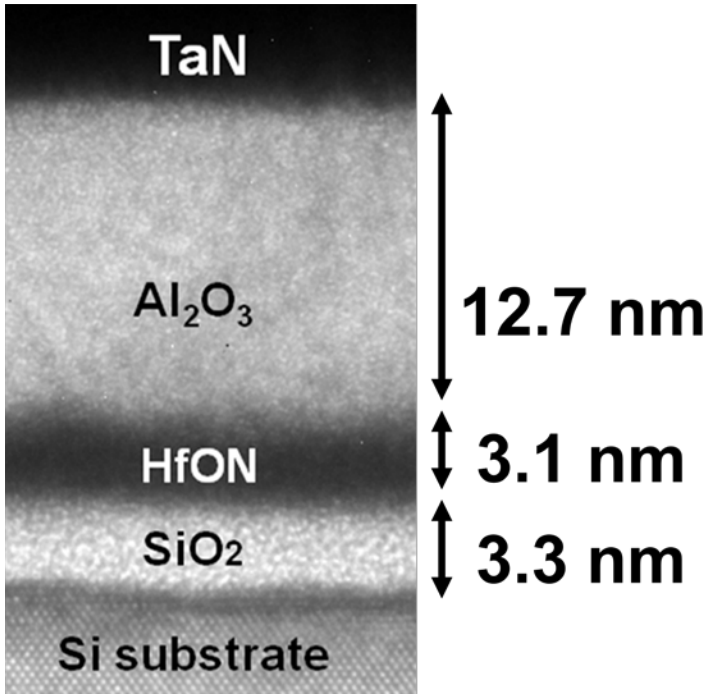


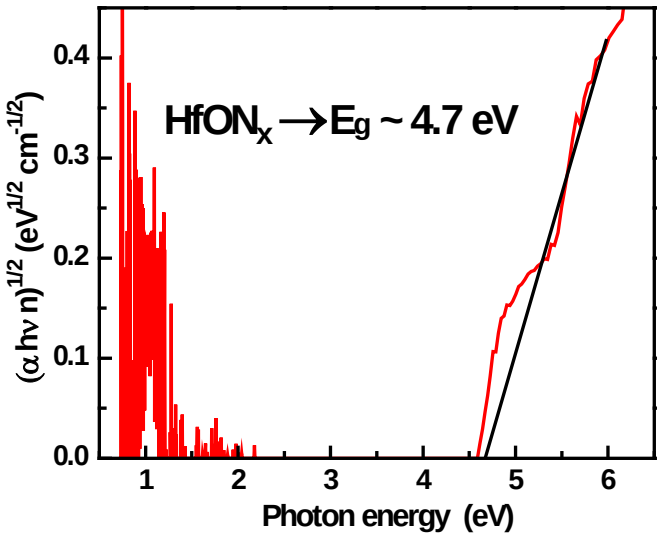
Figure 6. 1. Cross section of TaN/Al_2O_3/HfON/SiO_2/p-Si (TANOS) cell was obtained with high-resolution TEM to determine the thickness of each layer.

6.3 MATERIAL AND ELECTRICAL CHARACTERISTICS

6.3.1 Material Characterization of HfON

Cross-section of the device structure obtained by HRTEM is shown in Figure 1. The approximate thicknesses of the Al_2O_3 layer, HfON layer and the SiO_2 layer are 12.7 nm, 3.1 nm, and 3.3 nm, respectively. The ALD Al_2O_3 layer was observed to be polycrystalline, while the HfON and the SiO_2 layers are amorphous. Nitrogen concentration is obtained indirectly from the optical bandgap by using spectroscopic ellipsometry, as shown in Figure 6.2.

(a)



(b)

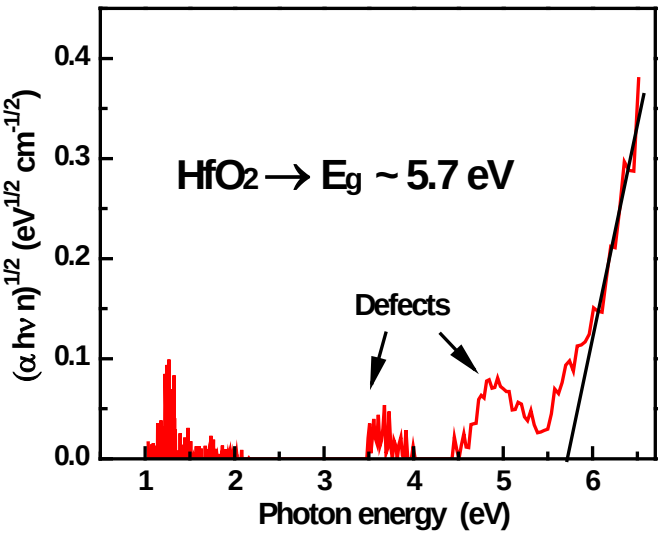


Figure 6. 2. Spectroscopic ellipsometry was used for measuring the optical bandgaps of HfON and HfO_2 thin films. The optical bandgaps of HfON and HfO_2 thin layers are estimated to be around 4.7 eV and 5.7 eV, respectively.

HfO_2 films were sputtered on the Si substrate directly and subjected to 500° C post-deposition anneal (PDA) condition, and HfON films were formed by 700° C anneal of the same HfO_2 in a NH_3 ambient for 30s. The optical bandgaps were measured by Spectroscopic Ellipsometry (SE) using a J. A. Woollam ellipsometer over a 0.75-8.55 eV spectroscopic range in 0.05 eV increments. Since parameterized optical models such as the Tau-Lorentz model or the Cauchy model cannot account for the localized absorption sites below the bandgap, the point-by-point extraction method available in the J. A. Woollam software was used. This method is analogous to the data inversion method described in Ref. 11. The optical bandgap is defined by the point where the extrapolated line crosses the x-axis. The estimated bandgaps are 4.7 eV and 5.7 eV for the HfON and HfO_2 layers, respectively. The extracted optical band gap of 5.7 eV for the HfO_2 thin layer matches well with the published data [11]. According to Ref. 9, we can easily extract the percentage of nitrogen from graphs describing the relationship between the nitrogen ratio and bandgap, so the nitrogen ratio of this HfON sample is 17%. The corresponding value of the conduction-band offset is 2.5 eV and the dielectric constant is 23, which is higher than the dielectric constant of 20 for HfO_2. This NH_3 nitridation technique allows us to optimize the bandgap of the Hf-O-N system by adjusting the annealing temperature and time. The signal from the band edge in HfON and the extra absorption peak in HfO_2 come from the defects in the thin oxide layer. These defects are believed to be due to the oxygen deficiency within the HfO_2 thin film and depend on the annealing condition [11]. Another explanation for the sub-band-gap absorption features at the HfO_2/Si interface by SE was reported in Ref. 12. From that

reference, oxygen deficient defects are not intrinsic to HfO_2, but reside primarily at the HfO_2/Si interface rather than in the bulk of the dielectric. So the defects in the HfON/SiO_2 interface might be reduced due to the interfacial-layer growth after 700° C RTA.

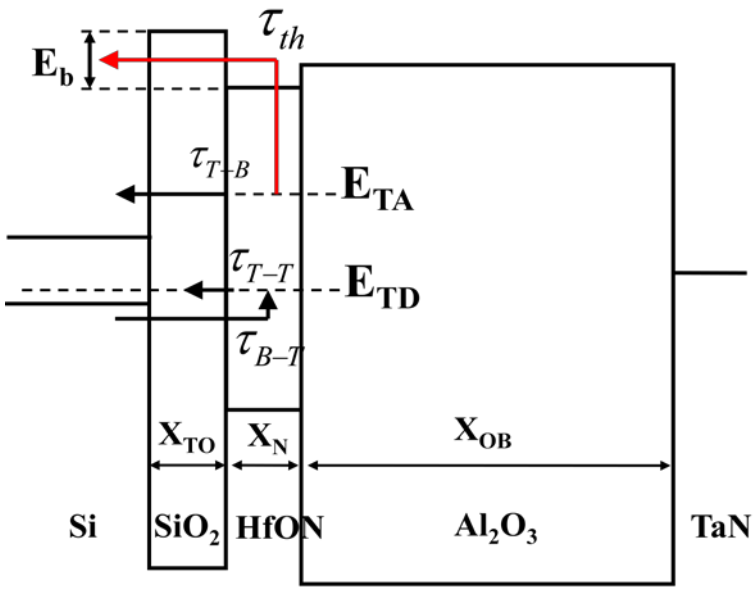


Figure 6. 3. Band alignment is presented for the TaN/Al_2O_3/HfON/SiO_2/p-Si (TANOS) cell and the charge decay model is illustrated to extract the trap level energy.

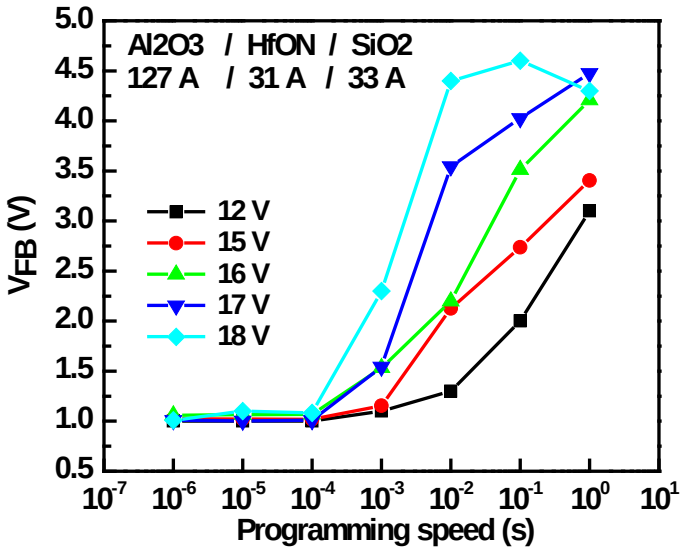
By using the bandgap of HfON, we can draw the band diagram as illustrated in Figure 6.3. The charge-decay characteristics of SONOS non-volatile memory was explained by an “amphoteric” trap model and thermal emission of trapped charges, which includes the effect of bottom oxide thickness to extract the trap density distribution in energy levels of the nitride layer [10]. E_{TA} and E_{TD} are the transitional energy levels associated with the

doubly and singly occupied electron states, respectively. τ_{T-B} is the time constant associated with trap-to-band tunneling of an electron, τ_{T-T} with trap-to-trap tunneling, τ_{B-T} with the band-to-trap tunneling of a hole, and τ_{th} with thermal emission of an electron, followed by tunneling through the bottom oxide. Among the four charge loss mechanisms, thermal emission is the dominant charge decay mechanism when the baking-temperature is above 150° C. The extraction of the trap density and trap level energy of the HfON trap layer will be discussed in Section 6.4.

6.3.2 Erasing and Programming Characteristics

The ALD Al_2O_3 oxide layer is usually used as a blocking barrier of the electrons from the gate electrode due to its larger band offset in the TANOS cell [1-3]. The thinner control oxide should result in a higher charge-trapping efficiency because it has a larger coupling ratio. However, a very thin control-oxide layer may not be enough to block the charges injected from the gate electrode and even from the silicon substrate. By the relation $\Delta V_{FB} = -\Delta Q_t * d/\varepsilon_{CO}$, where d and ε_{CO} are the physical thickness and permittivity of the control oxide, the thicker Al_2O_3 layer can produce a wider flatband shift with even a small amount of trapped charges [7]. To achieve the higher speed erase/program, we utilize the trap density and the high dielectric constant of the HfON trap layer, which induces a high electric field and high FN tunneling through the tunnel oxide.

(a)



(b)

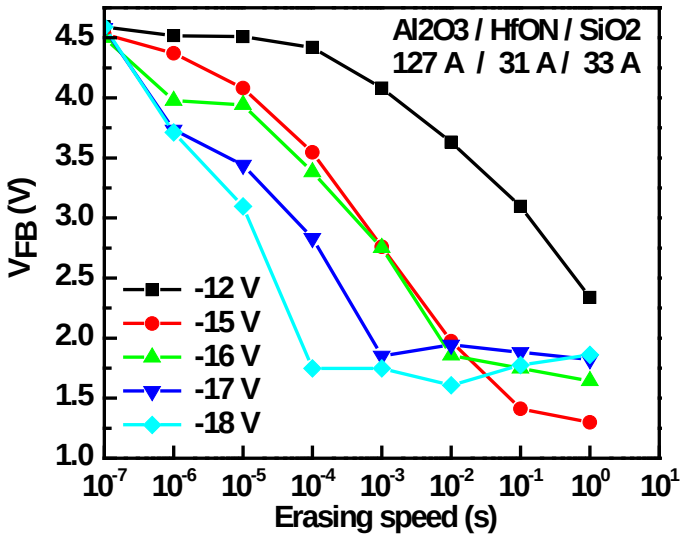


Figure 6. 4. (a) Programming speed and (b) erasing speed with varying gate voltage. This shows that the Al_2O_3 layer does not block the injected charges coming from the gate electrode at the higher voltage. The erasing speed is faster than the programming speed.

According to Figure 6.4(a), the programming speed is dependent on the programming voltage and is faster at 18 V (4.5 V at 10 ms), but the control oxide cannot block the electrons injected from the gate electrode at higher voltage for longer times. This leakage through the control oxide is related to the quality of the control ALD Al_2O_3 oxide layer. The erase speed was improved noticeably and most trapped electrons were erased by -18V, 100 μs pulse, but the flatband shift was not reduced further at longer stress (Figure 6.4(b)). Since electron injection is faster than the hole injection, the program speed is supposed to be higher than the erase speed due to the difference of tunneling masses of electrons and holes. However, the erase speed is faster than the program speed according to the data shown in Figures 6.4(a), and 6.4(b). This implies that the trapped electrons are detrapped directly from the HfON trap layer, and hole injection is negligible in our system. We believe that this is attributed to the thin tunnel oxide thickness and a lower hole trap density in HfON charge-trap layer. Thus, the flatband is saturated, rather than going down further during the erase operation as shown in Figure 6.5(a).

We acknowledge that there is room for optimizing the HfON thickness to obtain a wider memory window by increasing the number of traps and for implementing n+ source/drain pocket to improve the programming speed by supplying sufficient electrons for tunneling. The charge loss to the control gate at high voltage stress and the speed of the charge trapping of HfON layer can be improved further by increasing the thickness of both the HfON and ALD Al_2O_3 oxide layers.

6.3.3 Endurance Characteristics

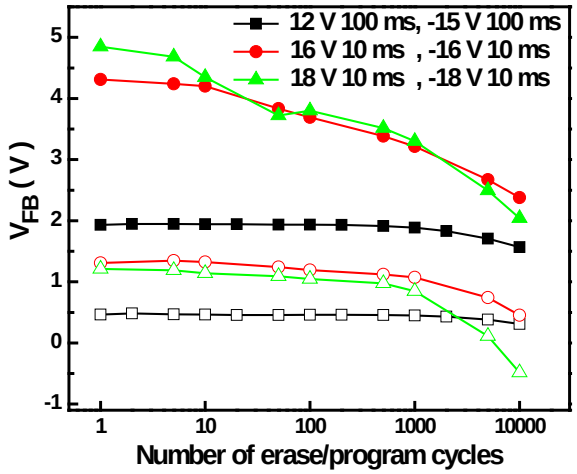
To check the endurance characteristics, several program voltages (12, 16, 18 V) and erase voltages (-15, -16, -18 V) were applied to the device and the flatband voltages were monitored. As shown in Figure 6.5(a), the flatband voltages were reduced, but the memory window narrowing, which is a common feature in floating-gate and SONOS cell flash memory devices, was not severe in our case. The tunnel oxide started to be degraded after 1 K erase/program cycles because the high dielectric constant of the HfON layer induced a high electric field in the tunnel oxide, resulting in a significantly increased level of operating stress. We can determine the effective field in each layer from the dependence on thickness and dielectric constant of each layer [13].

$$E = \frac{V_G}{d_2 \frac{\varepsilon}{\varepsilon_2} + d_1 \frac{\varepsilon}{\varepsilon_1} + d}, \quad E_1 = \frac{\varepsilon}{\varepsilon_1} E, \quad E_2 = \frac{\varepsilon}{\varepsilon_2} E \tag{1}$$

where E is the electric field on SiO_2 layer, E_1 is the electric field on the HfON layer, and E_2 is the electric field in Al_2O_3. One can easily see that the field in the SiO_2 would increase (Eq. (1)), where d_1 and ε_1 refer to the HfON trap layer. So if one chooses a high-k oxide having a higher ε_1 value, then the electric field in the SiO_2 increases. This increased electric field will cause higher FN tunneling currents, and result in the faster erase/program speed. According to the above equations, the electric field in SiO_2 layer is 5.9 times higher than the electric field in the HfON layer and 2.3 times higher than in the Al_2O_3 layer. This means that small increases of the applied voltage for the erasing and

programming operation increase the electric field in the SiO_2 tunneling oxide significantly.

(a)



(b)

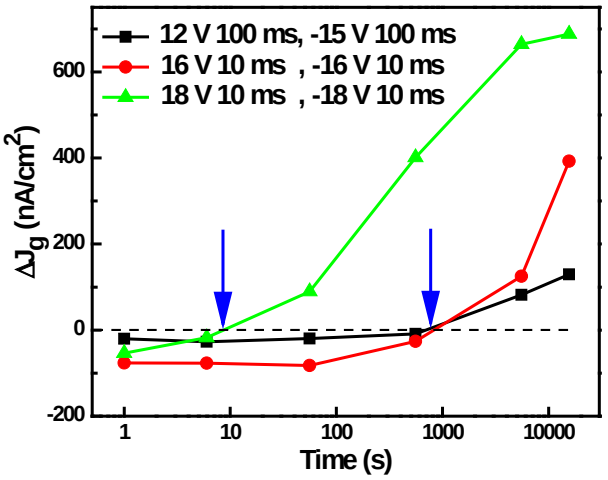


Figure 6. 5. Endurance test (a) and SILC current monitoring (b) were done simultaneously at several accelerated stress voltages to investigate the degradation mechanism. The memory window narrowing is not severe, but the flatband voltages shifted downward due to hole trapping in the HfON layer during the erase/program cycles.

During the erase/programming cycling, charges can also become trapped in the oxide, and then these trapped charges inhibit further charge injection in the trapping layer and cause the memory cell to require a higher program voltage [7, 14].

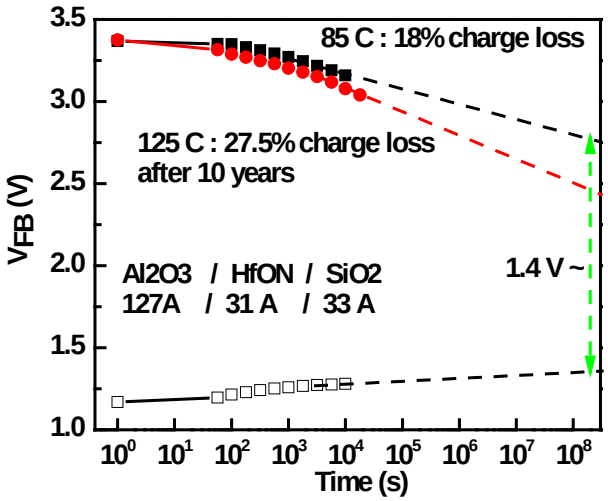
To investigate the oxide degradation, stress-induced gate-leakage current (SILC) measurements were performed. SILC was monitored at different cycles of the erase/program stress. The gate currents were measured before the stress and after one cycle of the erase/program operation and then measured after 10 cycles of the erase/program stress. As shown in Figure 6.5(b), the SILC is closely related to the stress voltage. The voltage stress degrades the oxide layers, resulting in the increase of the gate-leakage currents. The larger the voltage stress, the higher the gate-leakage currents. These increases in SILC imply the increase of the hole tunneling currents from the substrate created during the erase stress. Since initial trapped-hole charges from the hole tunneling currents reduce the hole tunneling currents and the Al_2O_3 blocking oxide inhibits the electron tunneling currents from the TaN gate, gate leakage currents decrease after a small initial number of erase/program cycles. However, the hole tunneling currents increase rapidly as the oxide wears out eventually due to the high field stress. As we mentioned before, a small change in stress voltage increases the electric field in the SiO_2 tunneling oxide layer significantly, accelerating the oxide degradation. At the 18 V stress, oxide degradation was worse and the memory window shifted in a negative direction. This indicates that some fraction of holes are trapped from the hole tunneling currents created by the higher and longer erase stress in the HfON layer. If there are hole traps in the SiO_2, then the memory window should be narrowed as usually observed in a

conventional floating gate flash memory [7]. In our experiments, the amount of the electrons trapped from the FN tunneling currents is unchanged because the memory window narrowing is not severe. Instead, the negative shift of the memory window characterizes the hole trapping in the HfON charge-trap layer.

6.3.4 Retention Characteristics

The main concern about small cell size flash memory is its charge retention characteristic, which has to meet the 10 year retention condition. To understand the mechanism of charge loss, we measured the flatband shift as a function of time for various bakeout temperatures (85 ~ 225° C) to examine the retention characteristics. At 85° C bake retention test shown in Figure 6.6(a), the charge loss is around 18% and can retain a memory window of over 1.4 V after 10 years [4, 5, 15]. The activation energy of the thin HfON charge trap layer extracted from the Arrhenius plot is 0.87 eV (Figure 6.6(b)).

(a)



(b)

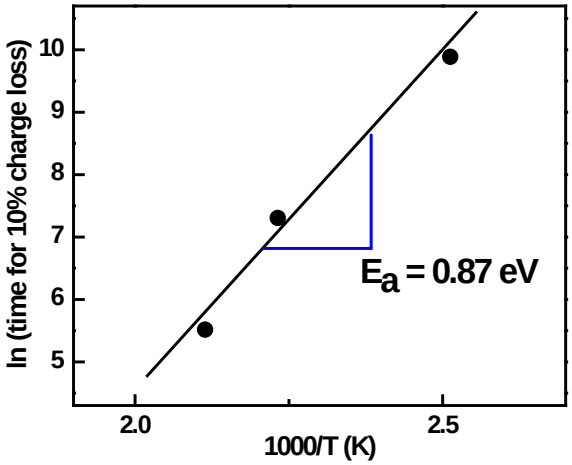


Figure 6. 6. Bake retention tests were performed from 85° C to 125 ° C. Data retention characteristics (a) and Arrhenius plot for the activation energy (b).

To examine the retention characteristics, it is necessary to investigate the trap-density energy distribution in HfON. The trap-levels can be calculated by using the

charge decay model illustrated in Figure 3. Kim [10] suggested an amphoteric trap model based on the thermal emission of the trapped charges. The decay rate of the trapped charge and the decay rate equation is

$$1/\tau_{th} = e_{ox}\, e_{th} = \alpha\, \beta T^2 \exp(-E_A / kT) \quad \beta = \exp\left(-2X_{OT}\sqrt{2qm^*_{OX}E_b}/\hbar\right) \tag{2}$$

$$\frac{dQ(E_{TA},t)}{dt} = -e_{ox}\, e_{th}\, Q(E_{TA},t) \tag{3}$$

$$E^*_{TA1} = (kT_1/q)\ln(\alpha\, \beta T_1^{\,2}\, t_1) \quad = \quad E^*_{TA2} = (kT_2/q)\ln(\alpha\, \beta T_2^{\,2}\, t_2) \tag{4}$$

Eq. 4 expresses the trap level (E_{TA}^*) and can be simply calculated after obtaining α. By equating two different trap level energies calculated with data measured at two different temperatures and times for the same charge loss, the α value can be obtained as follows,

$$\alpha = (T_2^2\, \beta\, t_2)^{(T_2/T_1 - T_2)} / (T_1^2\, \beta\, t_1)^{(T_1/T_1 - T_2)} \tag{5}$$

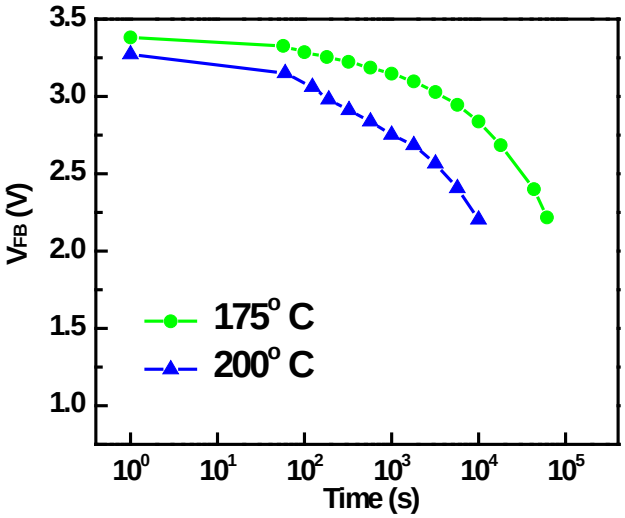
Thermal emission of the trapped electrons from the trap sites to the nitride conduction band is the dominant charge-loss mechanism. The final equation derived for trap density is

$$\frac{\partial \Delta V_{FB}}{\partial \log(t)} \approx -2.3qkT\, X_N \left(\frac{X_N}{2\,\varepsilon_N} + \frac{X_{OB}}{\varepsilon_{OX}}\right) g\left(E^*_{TA}\right) \tag{6}$$

With the above equations, $g(E^*_{TA})$, the trap density of HfON can be calculated with data measured at 175° C and 200° C shown in Figure 6.7(a). In Figure 6.7(b), trap densities are distributed from 0.73 to 1.1eV and the peak trap level is located at 1 eV with

1.3 * 10^{20} cm^{-3} eV^{-1} trap density, which is comparable to the trap-level energy of 1.1 eV for the Si_3N_4 trap layer [10].

(a)



(b)

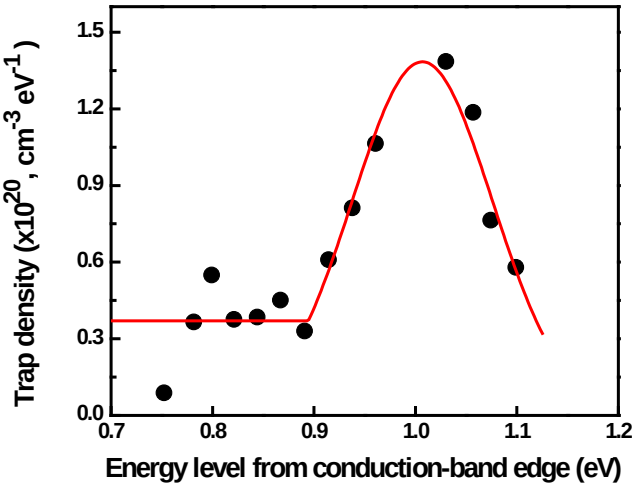


Figure 6. 7. Retention tests were done at 175° C and 200° C to extract the trap-level energy of the HfON trap layer (a). Trap density is located at 1 eV, which is comparable to the trap level energy of 1.1 eV for the Si_3N_4 trap layer.

The mechanism of the charge loss during the retention test is related to the thickness of the tunnel oxide and the barrier height, as well as the trap level of the HfON layer. The difference of the barrier height between the SiO_2 layer and the HfON charge-trap layer is 1 eV, which accounts for the good retention characteristics (Figure 6.8). The trapped charges might be thermally diffused out through the tunnel oxide and the barrier height of the control oxide. However, the deep trap energy level of the HfON layer is able to retain the charges for a longer time.

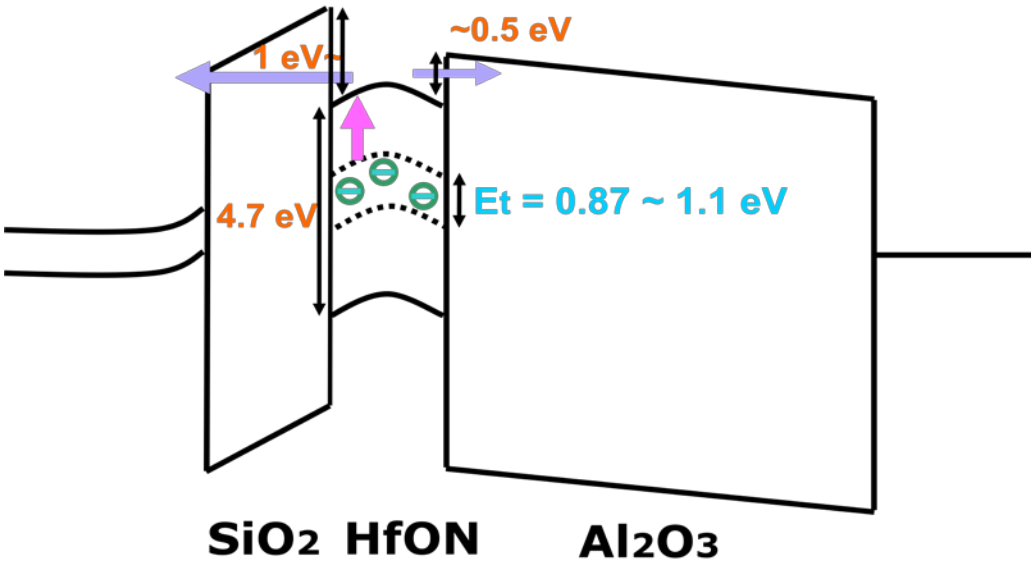


Figure 6. 8. Band diagram illustrates the charge-loss mechanism and the position of the trap-level energy. The mechanism of the charge loss in retention is related to the thickness of the tunnel oxide and the barrier height, as well as the trap level in the HfON layer.

6.4 SUMMARY

We developed thin HfON as the charge-trap layer in TANOS nonvolatile memories. A larger memory window and faster erasing speed, as well as good retention time, were achieved by using the NH_3 nitridation technique to incorporate nitrogen into the HfO_2 layer, because ammonia nitridation causes a large amount of electron-trap sites in the HfON layer. The bandgap of HfON can be further adjusted to optimize the charge-trap density and the retention characteristics by simply changing the nitrogen ratio in HfON. In addition, a higher electric field in the tunneling oxide induced by the high dielectric constant of HfON results in high-speed erasing and programming. The high dielectric constant of the HfON trap layer induces 6 times higher electric field in the SiO_2 tunnel layer compared to HfON. The memory window narrowing during the endurance test is not severe, but is shifted downward further due to hole trapping in the HfON layer during the erase/program cycles. Endurance analyses show a degradation of the tunnel oxide because the high dielectric constant of the HfON layer causes the tunnel oxide to be subjected to a significantly increased level of operating stress.

SILC accounts for the possible degradation mechanism during the endurance test. SILC is closely related to the stress voltage. So, a small increase in stress voltage increases the electric field to a much higher level in the SiO_2 tunneling-oxide layer, accelerating the oxide degradation. We suggest implementing a source/drain pocket to attain a faster programming speed and increasing the thickness of all three layers to reduce this high field effect since the decreased operating voltage will reduce the oxide degradation during the program/erase cycles. Finally, the trap density distribution versus

trap energy level of the HfON trap layer was estimated to explain qualitatively the charge-loss mechanism with the band diagram.

CHAPTER 7

CONCLUSION

7.1 SUMMARY AND FUTURE WORK

Despite the severe challenges of CMOS logic devices from 45nm technology node to 32nm node generation, device scaling has been achieved via high-k/metal gate (HK/MG) technology with relevant performance enhencement. Control of HK/MG gate stack with good device stability was realized by providing appropriate device structures such as gate-first HK/MG and gate-last HK/MG integration schemes. For the next generation CMOS logic devices toward 22nm node and beyond, it is imperative to keep scaling down the design rule of contact-to-gate pitch and equivalent oxide thickness (EOT), while maintaining decent channel mobility and device variability control. It should be noted that device pitch scaling has historically experienced performance loss, which in turn compels an introduction of novel technology elements to restore the performance shortfall. All of these requirements will require new integration schemes with the best known technology components into products, which may include the scaling of gate stack, channel mobility enhancement, parasitic resistance and capacitance reduction. Scaling of gate stack may involve the reduction of EOT or inversion thickness (Tinv), gate length, and gate height reduction. Channel mobility gain can be attained through the implementation of enhanced embedded source/drain (S/D) stressors such as embedded SiGe on p+ S/D, embedded Si:C on n+ S/D area, deposited stressor layers, and the use of high channel mobility substrate. Future work may deal with issues related to SRAM yield in the context of 32nm SOI technology using the high-k dielectrics

discussed in this thesis, and research challenges and future directions of HK/MG gate stack on different Si substrates in terms of device scalability and channel mobility enhancement. The focus of future work can be on the development of performance boosters such as HK/MG, embedded SiGe, channel SiGe, halo implant for controlling short channel effects and replacement gate in 22nm SOI technology. One can also further study V_{TH} variability of nano-scale devices due to random telegraph noise.

References

Chapter 1

[1] K. Mistry et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," *IEDM Tech. Dig.*, pp. 247-250, 2007.

[2] K. Henson et al., "Gate Length Scaling and High Drive Currents Enabled for High Performance SOI Technology using High-k/Metal Gate," *IEDM Tech. Dig.*, pp. 645-648, 2008.

[3] P. Ranade et al., "High Performance 35nm LGATE CMOS Transistors Featuring NiSi Metal Gate (FUSI), Uniaxial Strained Silicon Channels and 1.2nm Gate Oxide," *IEDM Tech. Dig.*, p. 217, 2005.

[4] L. Ragnarsson et al., "Ultralow-EOT (5 Å) Gate-First and Gate-Last High Performance CMOS Achieved by Gate-Electrode Optimization," *IEDM Tech. Dig.*, pp. 663-666, 2009.

[5] F. Arnaud et al., "32nm General Purpose Bulk CMOS Technology for High Performance Applications at Low Voltage," IEDM Tech. Dig., pp. 633-636, 2008.

[6] T. Tomimatsu et al., "Cost-effective 28nm LSTP CMOS Using Gate-First Metal Gate/High-k Technology," *VLSI Tech. Dig.*, pp. 36-37, 2009.

[7] H. R. Harris et al., "Band-engineered Low PMOS VT with High-k/Metal Gates Featured in a Dual Channel CMOS Integration Scheme," *VLSI Tech. Dig.*, pp. 154-155, 2007.

[8] K. Choi et al., "Extremely Scaled Gate-First High-k/Metal Gate Stack with EOT of 0.55nm Using Novel Interfacial Layer Scavenging Techniques for 22nm Technology Node and Beyond," *VLSI Tech. Dig.*, pp. 138-139, 2009.

[9] C. Lai et al., "A Novel Hybrid High-k/Metal Gate Process for 28nm High Performance CMOSFETs," *IEDM Tech. Dig.*, pp. 655-658, 2009.

[10] C. Auth et al., "45nm High-k + Metal Gate Strain-enhanced Transistors," *VLSI Tech. Dig.*, pp. 128-129, 2008.

[11] K.-D. Suh et al., "A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme", *Journal of Solid-State Circuits*, vol. 30, pp. 1149-1156, 1995.

Chapter 2

[1] C. S. Kang, H. –J. Cho, K. Onishi, R. Choi, R. Nieh, S. Krishnan, and J. C. Lee, "Improved Thermal Stability and Device performance of Ultra-thin (EOT<10Å) Gate Dielectric MOSFETs by using Hafnium Oxynitride (HfO_xN_y)" in *VLSI Symp. Tech. Dig.*, 2002, pp. 146-147.

[2] M. R. Visckay, J. J. Chambers, A.L. P. Rotondaro, A. Shanware, and L. Colombo, "Application of HfSiON as a gate dielectric material," *Appl. Phys. Lett.*, vol. 80, pp. 3185-3185, 2002.

[3] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi, and A. Nishiyama, "Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics," in *IDEM Tech. Dig.*, 2002, pp. 849-852.

[4] Changhwan Choi, C. Y. Kang, S. J. Rhee, M. S. Akbar, S. A. Krishnan, M. Zhang, H. S. Kim, T. Lee, F. Zhu, and Jack C. Lee, "Aggressively scaled ultra thin undoped HfO_2 gate dielectric (EOT < 0.7 nm) with TaN gate Electrode using engineered interface layer" *IEEE Eletron Device Lett.*, vol. 26, NO. 7, pp. 454-457, July 2005.

[5] Mohammad Shariar Akbar, S. Gopalan, H. J. Cho, K. Onishi, R. Choi, R. Neih, C. S. Kang, Y. H. Kim, J. Han S. Krishnan and Jack C. Lee, " High-performance TaN/HfSiON/Si metal-oxide-semiconductor structures prepared by NH_3 post-deposition anneal," *Appl. Phys. Lett.*, vol. 82, pp. 1757-1759, March 2003.

[6] S. J. Rhee; H. –S. Kim; C. Y. Kang; C. H. Choi; Akbar, M.S.; M. Zhang; T. Lee; I. Ok; F. Zhu; Krishnan, S.A. and J. C. Lee; "Structural optimization and electrical characteristics of ultra-thin gadolinium (Gd_2O_3) incorporated HfO_2 n-MOSFETs" *Device Research Conference Digest*, 2005. DRC '05, 2005 pp. 219 – 220.

[7] S. Jeon and H. Hwang, "Effects of hygroscopic nature on the electrical characteristics of lanthanide oxides (Pr_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3)," *J. Appl. Phys.*, vol 93, no. 10, pp. 6393-6395, May. 2003.

[8] S. Jeon, K. Im, H. Yang, H. Lee, H. Sim, S. Choi, T. Jang, and H. Hwang, "Excellent Electrical Characteristics of Lanthanide (Pr, Nd, Sm, Gd and Dy) Oxide and Lanthanide-doped Oxide for MOS Gate Dielectric Applications," *IEDM Tech. Dig.*, 2001, pp. 471-474.

[9] H. Lee, S. Jeon and Hwang, "Electrical characteristics of a Dy-doped HfO_2 gate dielectric" *Appl. Phys. Lett.*, vol. 79, no. 16, pp. 2757-2776, Oct. 2001.

[10] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility Measurement and Degradation Mechanisms of MOSFETs Made With Ultrathin High-k Dielectrics," *IEEE Trans. Electron Device*, vol. 51, no. 1, pp. 98-105, Jan. 2004.

[11] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universal mobility of inversion layer mobility in SI MOSFETs: Part II—Effect of surface orientation," *IEEE Trans. Electron Devices*, vol. 41, pp. 2363–2368, Dec. 1994.

[12] M. Fischetti, D. Neumayer, and E. Carttier, "Effective electron mobility in Si inversion layers in MOS systems with a high-k insulator: The role of remote phonon scattering," *J. Appl. Phys.*, vol. 90, pp. 4587–4608, 2001.

Chapter 3

[1] K. Choi, H-C Wen, G. Bersuker, R. Harris and B. Lee, "Mechanism of flatband voltage roll-off studied with Al_2O_3 film deposited on terraced oxide," *Applied Physics Letters*, 93, 133506, 2008.

[2] Y. Yamamoto, K. Kita, K. Kyuno, and A. Toriumi, "Study of La-Induced Flat Band Voltage Shift in Metal/$HfLaO_x$/SiO_2/Si Capacitors," *Jpn. J. Appl.Phys.* 46, pp. 7251-7255, 2007.

[3] H. Arimura, R. Haight, S. L. Brown, A. Kellock, A. Callegari, M. Copel, H. Wantanabe, V. Narayanan and T. Ando, "Temperature-dependent La- and Al-induced dipole behavior monitored by femtosecond pump/probe photoelectron spectroscopy," *Applied Physics Letters*, 96, 132902, 2010.

[4] T. Ando, M. Copel, J. Bruley, M. M. Frank, H. Wantanabe and. V. Narayanan, "Physical origins of mobility degradation in extremely scaled SiO_2/HfO_2 gate stacks with La and Al induced dipoles," *Applied Physics Letters*, 96, 132904, 2010.

[5] H. Iwai, S. Ohmi, S. Akama, C. Ohshima, A. Kikuchi, I. Kashiwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama, Y. Yoshihara, "Advanced gate dielectric materials for sub-100 nm CMOS," *IEDM Tech. Dig.*, pp. 625–628 2002.

[6] T. Lee, S. Rhee, C. Y. Kang, F. Zhu, C. Choi, I. Ok, M. Zhang, S. Krishnan, G. Thareja, J. C. Lee, "Strutural advantage for the EOT scaling and improved electron channel mobility by incorporating dysprosium oxide (Dy_2O_3) into HfO_2 n- MOSFETs, " *IEEE Electron Device Letter*, vol. 27, pp. 640-643, 2006.

[7] H.Y. Yu, Chang, S.Z. A. Veloso, A. Lauwers, C. Adelmann, B. Onsia, S. Van Elshocht, R. Singanamalla, M. Demand, R. Vos, T. Kauerauf, S. Brus, X. Shi, S. Kubicek, C. Vrancken, R. Mitsuhashi, P. Lehnen, J. Kittl, M. Niwa, K. M. Yin, T Hoffmann, S. Degendt, M. Jurczak, P. Absil, S. Biesemans, **"**Low Vt Ni-FUSI CMOS Technology using a DyO cap layer with either single or dual Ni-phases,**"** *Tech. Dig. VLSI Symp.*, pp 18-19, 2007.

[8] R. Jha, J. Gurganos, Y. H. Kim, R. Choi, J. Lee and V. Misra, "A capacitance-based methodology for the work function extraction of metals on high-k, " *IEEE Electron Device Letter*, vol. 25, pp. 420-423, 2004.

[9] P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, M. A. Quevedo-Lopez, H. C. Wen, H. Alshareef, K. Choi, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker H. R. Harris, P. Majhi, R. Choi, P. Lysaght, B. H. Lee, H.-H. Tseng, R. Jammy, T. S Böscke, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, "Dipole model explaining high-*k*/metal gate field effect transistor threshold voltage tuning," *Applied Physics Letters*, 92, 092901, 2008.

[10] K. Kita and A. Toriumi, "Origin of electric dipoles formed at the high-k/SiO_2 interface," *Applied Physics Letters*, 94, 132902, 2009.

[11] M. Copel, E. Cartier, and F. M. Ross, "Formation of a stratified lanthanum silicate dielectric by reaction with Si (001)" *Applied Physics Letters*, 78, number 11, 2001.

[12] G. He, M. Liu, L.Q. Zhu, M. Chang, Q. Fang and L.D. Zhang, "Effect of post-deposition annealing on the thermal stability and structural characteristics of sputtered HfO_2 films on Si (1 0 0)," *Surface Science*, vol. 576, pp. 67-75, 2005.

[13] S. Q. Wang and J. W. Mayer, "Reactions of Zr thin films with SiO_2 substrates," *J. Appl. Phys.* vol. 64, pp 4711, 1988.

[14] H. Jagannathan, V. Narayanan and S. Brown, "Engineering High Dielectric Constant Materials for Band-Edge CMOS," *ECS Trans.*, pp 16, 2008.

[15] P. Sivasubramani, T. S. Boscke, J. Huang, C. D. Young, P. D. Kirsch, S. A. Krishnan, M. A. Quevedo-Lopez, S. Govindarajan, B. S. Ju, H. R. Harris, D. J. Lichtenwalner, S. J. Jur, A. I. Kingon, J. Kim, B. E. Gnade, R. M. Wallace, G. Bersuker, B. H. Lee, R. Jammy, "Dipole Moment Model Explaining nFET Vt Tuning Utilizing La, Sc, Er, and Sr Doped HfSiON Dielectrics," *Tech. Dig. VLSI Symp.*, pp 68-69, 2007.

[16] H. Ota, A. Hirano, Y. Watanabe, N. Yasuda, K. Iwamoto, K. Akiyama, K. Okada, S. Migita, T. Nabatame and A. Toriumi, "Intrinsic Origin of Electron Mobility Reduction in High-k MOSFETs - From Remote Phonon to Bottom Interface Dipole Scattering," *IEDM tech. Dig.*, pp. 65-68,2007.

[17] C. Hobbs *et al.*, "Fermi-level pinning at the polySi/metal oxide interface", in *VLSI Symp. Tech. Dig.*, pp. 9–10, 2003.

[18] Y.-C. Yo, P. Ranade, Q. Lu, R. Lin, T.-J. King, and C. Hu, "Effects of high-_ dielectrics on the workfunction. of metal and silicon gates," in*VLSI Symp. Tech. Dig.*, pp. 49–50, 2001.

[19] *Device Electronics for Integrated Circuits,* R. S.Muller and T. I. Kamins, Eds.

[20] C. Hobbs *et al.*, "80-nm poly-Si gate CMOS with HfO gate dielectric" in *IEDM Tech. Dig.*, pp. 30.1.1–30.1.4, 2001.

Chapter 4

[1] V. Narayanan, V.K. Paruchuri, N.A. Bojarczuk, B.P. Linder, B. Doris, Y.H. Kim, S. Zafar, J. Stathis, S. Brown, J. Arnold, M. Copel, M. Steen, E. Cartier, A. Callegari, P. Jamison, J.-P. Locquet, D.L. Lacey, Y. Wang, P.E. Batson, P. Ronsheim, R. Jammy, M.P. Chudzik, M. Ieong, S. Guha, G. Shahidi, T.C. Chen, "Band-Edge High-Performance High-k/Metal Gate n-MOSFETs Using Cap Layers Containing Group IIA and IIIB Elements with Gate-First Processing for 45 nm and Beyond," *Tech. Dig. VLSI Symp.*, pp 178-179, 2006.

[2] P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, M. A. Quevedo-Lopez, H. C. Wen, H. Alshareef, K. Choi, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker H. R. Harris, P. Majhi, R. Choi, P. Lysaght, B. H. Lee, H.-H. Tseng, R. Jammy, T. S Böscke, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, "Dipole model explaining high-*k*/metal gate field effect transistor threshold voltage tuning," *Applied Physics Letters*, 92, 092901, 2008.

[3] T. Ando, M. M. Frank, K. Choi, C. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber, A. Callegari, D. Lacey, S. Brown, Q. Yang and V. Narayanan, "Understaning Mobility Mechenisms in Extremely scaled HfO_2 (EOT 0.42 nm) using remote interfacial layer scavenging technique and Vt-tuning dipoles with gate-first process," *IEDM tech. Dig.*, 17-1-1, 2009.

[4] H. Iwai, S. Ohmi, S. Akama, C. Ohshima, A. Kikuchi, I. Kashiwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama, Y. Yoshihara, "Advanced gate dielectric materials for sub-100 nm CMOS," *IEDM Tech. Dig.*, pp. 625–628 2002.

[5] T. Lee, S. Rhee, C. Y. Kang, F. Zhu, C. Choi, I. Ok, M. Zhang, S. Krishnan, G. Thareja, J. C. Lee, "Strutural advantage for the EOT scaling and improved electron channel mobility by incorporating dysprosium oxide (Dy_2O_3) into HfO_2 n- MOSFETs, " *IEEE Electron Device Letter*, vol. 27, pp. 640-643, 2006.

[6] H.Y. Yu, Chang, S.Z. A. Veloso, A. Lauwers, C. Adelmann, B. Onsia, S. Van Elshocht, R. Singanamalla, M. Demand, R. Vos, T. Kauerauf, S. Brus, X. Shi, S. Kubicek, C. Vrancken, R. Mitsuhashi, P. Lehnen, J. Kittl, M. Niwa, K. M. Yin, T. Hoffmann, S. Degendt, M. Jurczak, P. Absil, S. Biesemans, "Low Vt Ni-FUSI CMOS Technology using a DyO cap layer with either single or dual Ni-phases," *Tech. Dig. VLSI Symp.*, pp 18-19, 2007

[7] A. Kerber, E. Cartier, R. Degraeve, L. Pantisano, P. Roussel, G. Groeseneken, "Strong correlation between dielectric reliability and charge trapping in SiO_2/Al_2O_3 gate stacks with TiN electrodes", *VLSI Tech.*, 2002.

[8] S. Zafar, A. Callegari, E. Gusev, M. V. Fischetti, "Charge Trapping in High K Dielectric Stacks", *IEDM Tech. Dig.*, 2002, pp. 517-520.

[9] A. S. Oates, "Reliability Issues for High-K Dielectrics," *IEDM Tech. Dig.*, pp. 923-926, 2003.

[10] S. Lombardo, "Intrinsic dielectric breakdown of ultra-thin gate oxides," *Microelectronic Engineering*, 59, pp. 33-42, 2001.

[11] A. Kerber, E. Cartier, R. Degraeve, P. J. Roussel, L. Pantisano, T. Kauerauf, G. Groeseneken, H. E. Maes, U. Schwalke, "Charge Trapping and Dielectric Reliability of SiO_2-Al_2O_3 Gate Stacks with TiN electrodes " *IEEE Trans. Eletron Devices*, vol. 50, NO. 5, pp. 1261-1269, May 2003.

[12] Z.Xu, M. Houssa, R. Carter, M. Naili, S. D. Gendt and M. Heyns, "Constant voltage stress induced degeneration in HfO_2/SiO_2 dielectric stacks ," *J. Appl. Phys.*, vol 91, no. 12, pp. 10127-10129, June 2002.

[13] S.-C. Chang, S.-Y. Deng and J. Y.-Min Lee, "Electrical characteristics and reliability properties of metal-oxide-semiconductor field-effect transistors with Dy_2O_3 gate dielectric," *Appl. Phys. Lett.*, vol. 89, 053504, August. 2006.

[14] T. Kauerauf, R. Degraeve, E. Cartier, C. Soens, G. Groeseneken, "Low Weibull Slope of Breakdown Distributions in High-k Layers," *IEEE Electron Device Letters*, vol. 23, no. 4, pp. 215-217, April 2002.

[15] D. K. Schroder, "Semiconductor Material and Device Characterization", Second Edition, Addison-Wesley, 1998.

[16] C.L. Hinkle, C. Fulton, R.J. Nemanich, G. Lucovsky, "A novel approach for determining the effective tunneling mass of electrons in HfO_2 and other high-k alternative gate dielectrics for advanced CMOS devices", *Microelectronic Engineering* 72, pp.257–262, 2004.

Chapter 5

[1] A. S. Oates, "Reliability Issues for High-K Dielectrics," *IEDM Tech. Dig.*, pp. 923-926, 2003.

[2] A. Ghetti, "Gate Oxide Reliability: Physics and Computational Models," Springer Series in Materials Science, 2004.

[3] T. Lee, J. C. Lee and S. K. Banerjee, "Characterization of Dysprosium oxide (Dy_2O_3) incorporated HfO_2 gate oxide devices," *IEEE SISC* 2007.

[4] S. Rhee and Jack C. Lee, "Threshold voltage instability characteristics of HfO_2 dielectrics n-MOSFETs," *Microelectronics Reliability*, vol. 45, pp.1051-1060, 2005.

[5] K. Onishi, C. S. Kang, R. Choi, S. Gopalan and J. C. Lee, "Reliability characteristics, Including NBTI, of Polysilicon Gate HfO_2 MOSFETs," *IEDM Tech. Dig.*, 2001.

[6] Y. Kim and J. C. Lee, "Reliability characteristics of High-K dielectrics," *Microelectronics Reliability*, vol. 44, 2004.

[7] T. Lee, S. Rhee, C. Y. Kang, F. Zhu, C. Choi, I. Ok, M. Zhang, S. Krishnan, G. Thareja, J. C. Lee, "Strutural advantage for the EOT scaling and improved electron channel mobility by incorporating dysprosium oxide (Dy_2O_3) into HfO_2 n- MOSFETs, " *IEEE Electron Device Letter*, vol. 27, pp. 640-643, 2006.

[8] S.M. Sze, "Physics of Semiconductor Devices,"2nd edition, 1981.

[9] A. Yassine and R. Hijab, "Temperature Dependence of Gate Current in Ultra Thin SiO_2 in Direct-Tunneling Regime," *IEEE IRW Final Report*, pp. 56-61, 1997.

[10] C. K. Maiti, G. K. Dalapati, S. Chatterjee, S. K. Samanta, S. Varma, S. Patil, "Electrical properties of high permittivity ZrO_2 gate dielectrics on strained-Si," *Solid-State Electronics*, vol. 48, pp. 2235-2241, 2004.

[11] J. Kolodzey, E. A. Chowdhury, T. N. Adam, G. Qui, I. Rau, J. O. Olowolafe, S. Suehle and Y. Chen, "Electrical Conduction and Dielectric Breakdown in Aluminum Oxide Insulator on Silicon," *IEEE Trans. Elec. Dev.*, vol. 7, no. 1, 2000.

[12] M. Alam, "SILC as a Measure of Trap Generation and Predictor of *TBD* in Ultrathin Oxides," *IEEE Trans. Elec. Dev.*, vol.49, no.2, pp. 226–231, 2002.

[13] G. Ribes, J. Mitard, M. Denais, S. Btuyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on High-k Dielectrics Reliability Issues," *IEEE Transactions on Device and Materials Reliability*, vol. 5, March 2005.

[14] F. Monsieur, E. Vincent, G. Ribes, V. Huard, S. Bruyere, G. Pananakakis, and G. Ghibaudo, "Evidence for defect-generation-driven wear-out of breakdown conduction path in ultra thin oxides," in *Proc. IRPS*, 2003, pp. 424-431.

[15] J. C. Lee, I. Chen and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," *IEEE Trans. Electron Dev.*, pp. 2268-2278, 1989.

[16] M. Alam, B. Weir and P. Silverman, "A Future of Function or Failure?" *IEEE Circuits & Magazine*, March 2002, pp. 42-48.

[17] E. Wu, J. Aitken, E. Novak, A. Vayshenker, P. Varekamp, G. Hueckel, and J. McKenna, "Voltage-Dependent Voltage-Acceleration of Oxide Breakdown for Ultra-Thin Oxides," *IEDM Tech. Dig.*, pp. 541-544 2000.

[18] Y. Harada, M. Niwa, S. Lee and D. L. Kwong, "Specific structural factors influencing on reliability of CVD-HfO_2," *Symp. VLSI Technology Dig. Tech. Papers*, 2002, pp. 26-27.

[19] J. W. McPherson, J. Kim, A. Shanware, H. Mogul and J. Rodrigues, "Trends in the ultimate breakdown strength of high dielectric-constant materials," *IEEE Trans. Electron Devices*, vol. 50, no. 8, pp. 1771-1778, Aug. 2003.

[20] F. Monsieur, E. Vincent, G. Pananakakis, and G. Ghibaudo, "Wear-out, breakdown occurrence and failure detection in 18–25 Å ultrathin oxides," *Microelectronics Reliability.*, vol. 41, pp. 1035-1039, 2001.

[21] J. Hicks, D. Bergstrom, J. Jopling, J. Maiz, S. Pae, C. Prasad and J. Wiedemur, "45 nm Transistor Reliability" *Intel Technology Journal*, vol. 12, issue 2, 2008.

[22] R. Moazzami, J. C. Lee and C. Hu, "Temperature Acceleration of Time-Dependent Dielectric Breakdown," *IEEE Trans. on Electron Dev.*, vol. 36, no. 11, 1989.

[23] E. Y. Wu and Jordi Sune, "Power-law voltage acceleration: A key element for ultra-thin gate oxide reliability," *Microelectronics Reliability.*, vol. 45, pp. 1809-1834, 2005.

Chapter 6

[1] C.-H. Lee, J. Choi, C. Kang, Y. Shin, J.-S. Lee, J. Sel, J. Sim, S. Jeon, B.-I. Choe, D. Bae, K. Park, and K. Kim, ""Multi-Level NAND Flash Memory with 63nm-node TANOS (Si-Oxide-SiN-Al2O3-TaN) Cell Structure", *Symp . on VLSI Tech.*, 2006.

[2] Y. Shin, J. Choi, C. Kang, C.-H. Lee, J.-S. Lee, J. Sel, V. Kim, B. Choi, J. Sim, D. Kim, H.-J. Cho, and K. Kim, "A Novel NAND-type MONOS Memory using 63nm Process Technology for Multi-Gigabit Flash EEPROMs", *Int. Elec. Dev. Meeting*, 2007.

[3] C.-H. Lee, K. I. Choi, M. Cho, Y. H. Song, K. C. Park, and K. Kim, "A novel SONOS structure of SiO2/SiN/Al2O3 with TaN metal gate for multi-giga bit flash memories", *Int. Elec. Dev. Meeting*, 2007.

[4] M. She, H. Takeuchi, and T.-J. King, "Silicon-Nitride as a Tunnel Dielectric for Improved SONOS-Type Flash Memory", *IEEE Electron Device Letters,* vol. 24, no. 5, 2003

[5] S Maikap, H Y Lee, T-Y Wang, P-J Tzeng, C C Wang, L S Lee, K C Liu, J-R Yang and M-J Tsai, "Charge trapping characteristics of atomic-layer-deposited HfO_2 films with Al_2O_3 as a blocking oxide for high-density non-volatile memory device applications", *Semicond. Sci. Technol.* 22, 884, 2007.

[6] S. Jeon, "Thermal Stability and Memory characteristics of HfON trapping layer for Flash Memory Applications ", *ElectroChem. Solid-State. Lett.,* 12, H412, 2009.

[7] W. D. Brown and J. E. Brewer, *Nonvolatile Semiconductor Memory Technology* (IEEE Press Series, Piscataway, 1998.

[8] V. J. Kapoor and S. B. Bibyk, edited by G. Lucovsky, S. Pantelides, and G. Galeener, "*Energy distribution of electron trapping defects in thick-oxide MNOS structures,*" in *Physics of MOS Insulators* (NCSU, Raleigh, 1980).

[9] T. Ino, Y. Kamimuta, M. Suzuki, M. Koyama, and A. Nishiyama, "Dielectric Constant Behavior of Hf–O–N System", *Jpn. J. Appl. Phys.* 2908, 2006.

[10] T. H. Kim, J. S. Sim, J. D. Lee, H. C. Shin, B.-G. Park, "Charge decay characteristics of silicon-oxide-nitride-oxide-silicon structure at elevated temperatures and extraction of the nitride trap density distribution", *Appl. Phys. Lett.*, 85, 4 (2004).

[11] H. Takeuchi, D. Ha, and T.-J. King, "Observation of bulk HfO2 defects by spectroscopic ellipsometry", *J. Vac. Sci. Technol. A,* 22, 4, 2004.

[12] J. Price, P. S. Lysaght, S. C. Song, H. J. Li, and A. C. Diebold, "Identification of Sub-Bandgap Absorption Features at the High-κ / Silicon interface and Their Relation to Charge Trapping States ", *Appl. Phys. Lett.,* 91, 061925, 2007.

[13] T. Lee, J. C. Lee, and S. K. Banerjee, "Characterization of Dysprosium oxide (Dy_2O_3) incorporated HfO_2 gate oxide devices", *IEEE SISC* 2007.

[14] Y. N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, B. J. Cho, "High-k HfAlO charge trapping layer in SONOS-type nonvolatile memory device for high speed operation", *Int. Elec. Dev. Meeting*, 2004.

[15] X. Wang and D.-L. Kwong, "A novel high-κ SONOS memory using $TaN/Al_2O_3/Ta_2O_5/HfO_2/Si$ structure for fast speed and long retention operation", *IEEE Trans. Electron Device*, 53, 1, 2006.

Vita

Tackhwi LEE received the B. S. and M. S. degrees in Physics from Yonsei University, Seoul, Korea, in 1996 and 1998, respectively. He obtained the Ph. D degree in Electrical and Computer Engineering at the University of Texas, Austin, in 2010.

He participated in the development of the 15nm CMOS device at the T. J. Watson Research Center, where he designed and characterized the Ebeam-patterned devices before he joined the characterization group of 32nm SOI technology at IBM, Fishkill. He also worked on developing the 43 nm SONOS NAND flash memory working 4Gbit at Spansion Inc. from 2008 to 2009.

His research area is the development of the process integration and electrical characterization of metal gate high-k stack and its reliability, including the charge trapping characteristics and dielectric breakdown mechanism of the thin high-dielectric MOS device. He also explored GaAs MOSFET, charge trap layer Flash memory and Graphene nano-device intensively during his graduate study.

E-mail address: tack0@mail.utexas.edu

This dissertation was typed by Tackhwi Lee