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A Study of Electrical and Material Characteristics of III-V MOSFETs and TFETs with High-κ Gate Dielectrics

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A Study of Electrical and Material Characteristics of III-V MOSFETs and TFETs with High-κ Gate Dielectrics

by

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Dedication

My husband for his love and suppor

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A study of electrical and material characteristics of III-V MOSFETs and TFETs with High-κ Gate Dielectrics

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The performance and power scaling of metal-oxide-semiconductor field-effect-transistors (MOSFETs) has been historically achieved through shrinking the gate length of transistors for over three decades. As Si complementary metal-oxide-semiconductor (CMOS) scaling is approaching the physical and optical limits, the emerging technology involves new materials for the gate dielectrics and the channels as well as innovative structures. III-V materials have much higher electron mobility compared to Si, which can potentially provide better device performance. Hence, there have been tremendous research activities to explore the prospects of III-V materials for CMOS applications. Nevertheless, the key challenges for III-V MOSFETs with high-κ oxides such as the lack of high quality, thermodynamically stable insulators that passivate the gate oxide/III-V interface still hinder the development of III-V MOS devices.

The main focus of this dissertation is to develop the proper processes and structures for III-V MOS devices that result in good interface quality and high device performance. Firstly, fabrication processes and device structures of surface channel

MOSFETs were investigated. The interface quality of $In_{0.53}Ga_{0.47}As$ MOS devices was improved by developing the gate-last process with more than five times lower interface trap density (D_{it}) compared to the ones with the gate-first process. Furthermore, the optimum substrate structure was identified for inversion-type $In_{0.53}Ga_{0.47}As$ MOSFETs by investigating the effects of channel doping concentration and thickness on device performance. With the proper process and channel structures, the first inversion-type enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs with equivalent oxide thickness (EOT) of ~10 Å using atomic layer deposited (ALD) HfO_2 gate dielectric were demonstrated.

The second part of the study focuses on buried channel InGaAs MOSFETs. Buried channel InGaAs MOSFETs were fabricated to improve the channel mobility using various barriers schemes such as single InP barrier with different thicknesses and InP/InAlAs double-barrier. The impacts of different high-κ dielectrics were also evaluated. It has been found that the key factors enabling mobility improvement at both peak and high-field mobility in $In_{0.7}Ga_{0.3}As$ quantum-well MOSFETs with InP/InAlAs barrier-layers are 1) the epitaxial InP/InAlAs double-barrier confining carriers in the quantum-well channel and 2) good $InP/Al_2O_3/HfO_2$ interface with small EOT. Record high channel mobility was achieved and subthreshold swing (SS) was greatly improved.

Finally, InGaAs tunneling field-effect-transistors (TFETs), which are considered as the next-generation green transistors with ultra-low power consumption, were demonstrated with more than two times higher on-current while maintaining much smaller SS compared to the reported results. The improvements are believed to be due to using the $In_{0.7}Ga_{0.3}As$ tunneling junction with a smaller bandgap and ALD HfO_2 gate dielectric with a smaller EOT.

Table of Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 Motivation for high mobility channels with high-κ oxide

To achieve higher density and performance and lower power consumption, silicon (Si) complementary metal-oxide-semiconductor (CMOS) devices have been scaled for more than 30 years. Transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years [1]. The key enabler for the exponential growth of the transistor density on a chip is the scaling of the metal-oxide-semiconductor field-effect-transistors (MOSFETs) gate length by a factor of 0.7 per technology node (Figure 1.1). In addition, other transistor dimensions have been scaled according to Dennard's scaling theory [2]. However, from the 90 nm node onward, the conventional scaling trend of bulk Si CMOS has appeared to have been stymied due to several physical limitations and technological challenges.

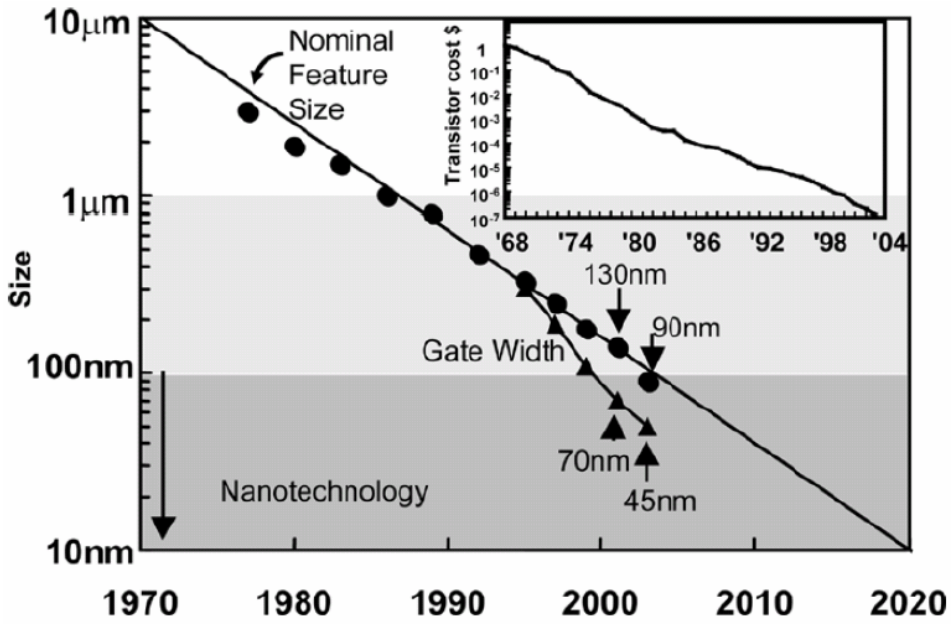

Figure 1.1 Historical trend of CMOS scaling.

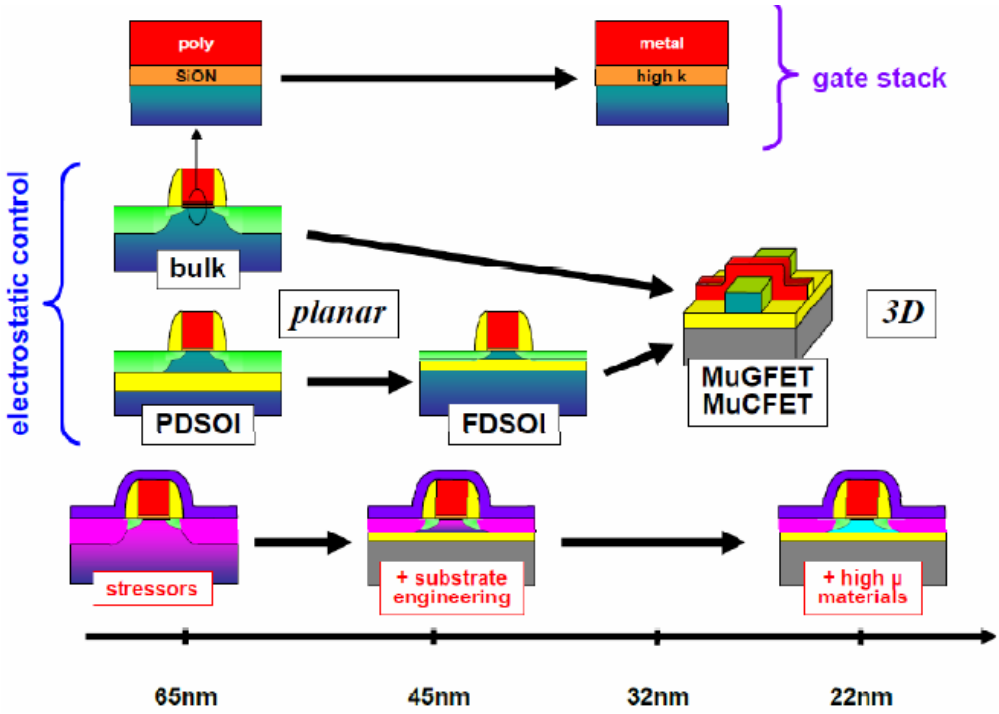

Figure 1.2 The structures and technology innovation for 65 nm node onward from 2007 edition of International Technology Roadmap for Semiconductors.

The half pitch of the 1st metal and physical gate length of the transistors for high performance logic circuits are going to be 29 nm and 16 nm in 2014 according to 2008 IRTS [3]. This is approaching the optical limit of the photo lithography. Due to the physical limit (~ 14 Å thickness [4], [5]) and high gate leakage of SiO_2 gate oxide, Intel Inc. has used high-κ oxide in their 45 nm node products [6]. All these constraints and limits are calling a new material and/or a new device structure to continue semiconductor products improvements. The 2007 edition of International Technology Roadmap for Semiconductors (ITRS) [7] states the structures and technology innovation from 65 nm node onward (figure 1.2). Employing a group of technology boosters, such as stained Si [8]-[9], high-κ/ metal gate [4], [10]-[12] and high-mobility channels [13]-[15] can mitigate the problems and provide performance benefit. The following parts of this

section will focus on one of the potential solutions: high mobility channels with high-κ gate oxide.

Stating from device characteristics, a high on-current (I_{on}) for MOSFETs can provide smaller transistor switching time thus improved transistor performance. The saturation current of MOSFETs is shown in equation (1.1):

$$I_{dsat} = \mu \frac{A\xi_0\xi_r}{T_{ox,inv}} \frac{W}{2L}(V_g - V_t)^2 \tag{1.1}$$

The gate length L and oxide thickness (T_{ox}) are the dominant scaling and performance enablers. V_g (or supply voltage V_{dd}) is also continuous decreasing to reduce the power consumption.

Power consumption for a CMOS circuit is constituted by active power (P_{active}) and standby power ($P_{standby}$). Their relationship with transistor characteristics is shown in equation (1.2) and (1.3), in which "a" is the active ratio, "f" is the frequency, and C_{load} is the load capacitance.

$$P_{active} = a \bullet f \bullet C_{load} \bullet V_{DD}^2 \tag{1.2}$$

$$P_{s\tan dby} = I_{off} \bullet V_{DD} \tag{1.3}$$

The I_{off} is consisted of subthreshold leakage, gate induced drain leakage (GIDL) and gate leakage [16]-[17]. To reduce the power consumption, both I_{off} and V_{dd} have to be reduced.

In summary, to obtain a semiconductor device with low power consumption and high performance, a high I_{on}, a low I_{off} and a small V_{dd} are required.

To illustrate this point more clearly, figure 1.3 shows the power constrained CMOS scaling trend for performance. In figure 1.3(a), when traditional MOSFETs are scaling down, as SiO_2 thickness keeps decreasing, the gate leakage current I_g becomes the dominant factor for high I_{off}. With high-κ oxide/ metal gate gate stacks replacing

SiO_2/poly silicon gate stacks [4], [10]-[12], the I_g can be reduced, then the junction leakage I_j (by increased GIDL [16] due to increasing junction/substrate doping and equivalent oxide thickness (EOT) scaling required by Dennard's rule [2]) limits the I_{off} (figure 1.3(b)). To reduce I_j, fully depleted Si can be used (figure 1.3(c)). From figure 1.3(a) to 1.3(c), all work are done to reduce I_{off} thus power consumption. To improve device performance, a higher mobility channel can be used, which can provide higher I_{on} at the same V_{dd} or the same I_{on} at lower V_{dd} (figure 1.4(d)). Strained Si technology is widely accepted to increase mobility (μ) thus current [8]-[9], but we are going to need even higher mobility channels (Germanium (Ge), III-V based) to provide both high performance (high I_{on}) and low power (V_{dd} scaling).

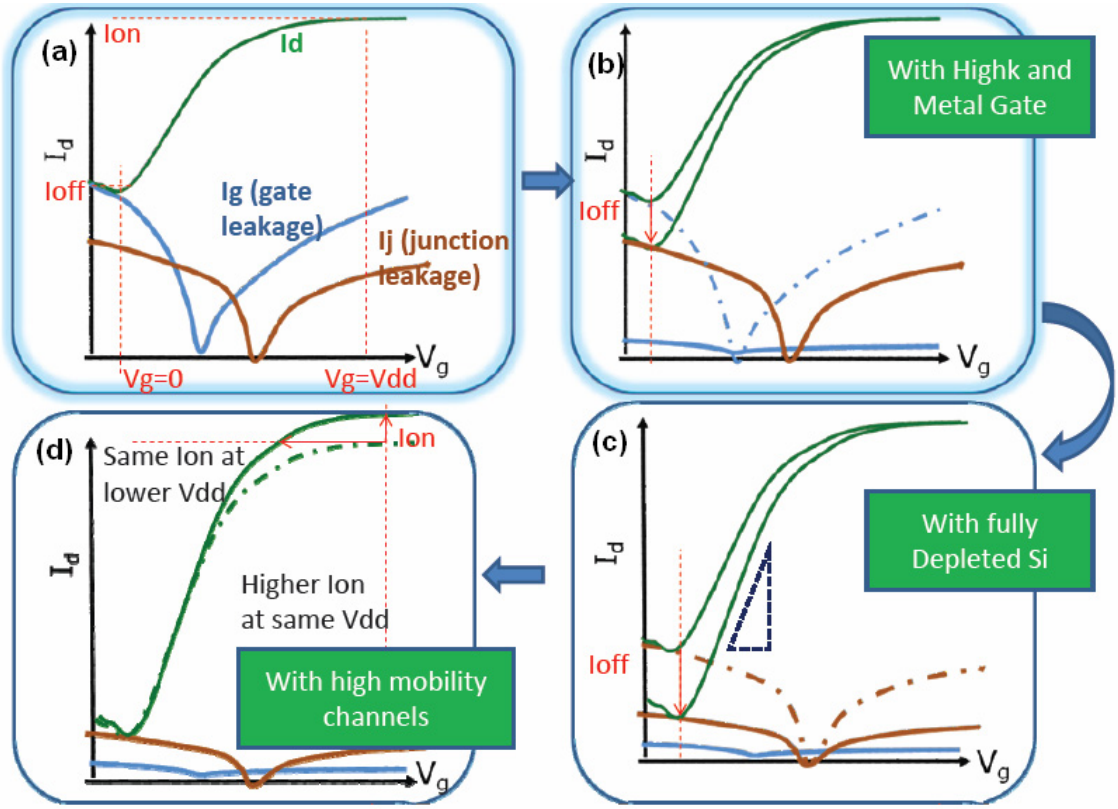

Figure 1.3 The power constrained CMOS scaling trend for performance.

1.2 III-V MOSFETs with high-κ oxides

Table 1.1 shows the material properties of various semiconductors. III-V materials have much higher electron mobility compared to Si, which can potentially provide higher on-current and better device performance according to equation (1.1).

There is debate about whether the high-mobility channel can increase the on-current when the channel is short enough to make carrier transport reach the ballistic limit. Counting the backscattering effect at the source edge of channel and thermal injection velocity v_T, the saturation current can be written as [18],

$$I_{dsat} = \left[\frac{C_{ox} W}{\frac{1}{v_T} + \frac{1}{\mu^0 E(0^+)}} \right] (V_g - V_{th}) \qquad (1.4)$$

where μ^0 is the low-field mobility and $E(0^+)$ is the channel electrical field. Therefore, the long channel mobility is still a critical factor to on-current and hence to transistor performance for the short channel devices.

Table 1.1 Material properties of various semiconductors

	Si	Ge	GaAs	InP	$In_{0.53}Ga_{0.47}As$	$In_{0.7}Ga_{0.3}As$	InAs
Lattice Constant (Å)	5.431	5.658	5.653	5.869	5.869	5.937	6.058
Electron Effective Mass (m^*/m_0)	0.19	0.082	0.067	0.077	0.041	0.034	0.023
Electron Affinity (eV)	4.05	4	4.07	4.38	4.5	4.65	4.9
Band-gap (eV)	1.12	0.66	1.42	1.35	0.74	0.58	0.35
n_i at R.T. (cm^{-3})	1×10^{10}	2×10^{13}	2.1×10^{6}	1.3×10^{7}	6.3×10^{11}	1.1×10^{13}	1.0×10^{15}
N_c (cm^{-3})	3.2×10^{19}	1×10^{19}	4.7×10^{17}	5.7×10^{17}	2.1×10^{17}	1.5×10^{17}	8.7×10^{16}
N_v (cm^{-3})	1.8×10^{19}	5×10^{18}	9.0×10^{18}	1.1×10^{19}	7.7×10^{18}	7.5×10^{18}	6.6×10^{18}
Electron mobility (cm^2/Vs)	1,500	3,900	8,500	4,600	12,000	20,000	33,000
Hole mobility (cm^2/Vs)	450	1,900	400	150	300	400	460
Saturation velocity at low field (cm/s)	1×10^{7}	6×10^{6}	2.1×10^{7}	2.5×10^{7}	3.1×10^{7}	6.1×10^{7}	7.7×10^{7}

Applying high-κ oxide instead of SiO_2 as the gate oxide on III-V materials can reduce the gate leakage current at the same EOT, thus reduces the power consumption. The requirements of the high-κ dielectrics [4], [19]-[20] include: 1) a large band gap for high barrier heights to both electrons and holes, 2) thermal dynamically stable and low interface trap density with substrate, 3) compatibility with gate electrode, 4) compatibility with conventional planar CMOS processing. The material properties of various gate oxide candidates are summarized in Table 1.2.

Table 1.2 Material properties of various gate oxides

Properties	SiO_2	Al_2O_3	HfO_2	ZrO_2	La_2O_3
Dielectric constant	3.9	8-9	18-25	18-30	20-36
Bandgap (eV)	9	8.8	6.0	5.8	4.3
Band offset for electrons (eV)	3.5	2.8	1.5	1.4	2.3
Band offset for holes (eV)	4.4	4.9	3.4	3.3	0.9

The key challenge for III-V MOSFETs with high-κ oxides is the lack of high quality, thermodynamically stable insulators that passivate the gate oxide/III-V interface. Recently, surface-channel inversion-mode III-V MOSFETs with atomic layer deposited (ALD) Al_2O_3, HfO_2, ZrO_2 or $LaAlO_3$ dielectrics [21]-[24], molecular beam epitaxy (MBE) $Ga_2O_3(Gd_2O_3)$ dielectrics [25]-[27] and Si, Ge, Si_xN_y, Ge_xN_y, or Al_xN_y interfacial passivation layer (IPL) and high-κ gate stacks [28]-[32]show promising results. Various interface treatment technique such as sulfur (S) compounds [33], N_2 plasma [31], HBr solution [34], PH_3 passivation [35], and fluorine treatment [36]-[37] have also been demonstrated with improved device characteristics. On the other hand, buried channel III-V MOSFETs with InAlAs barrier layer and Si interfacial passivation layer [38]-[39], or with single InP barrier layer or InP/InAlAs double barrier layer using ex-situ ALD

oxide [40]-[41], or flat band InGaAs MOSFETs with GaAs/AlGaAs barrier layer and Si δ-doping using in-situ MBE $GaGdO_x$ gate oxide [42]-[43], or MOS high-electron-mobility transistors (MOS-HEMTs) [44] demonstrate much higher channel mobility (e.g., μ_{eff} > 3800 cm^2/Vs [38]-[44]) compared to surface channel MOSFETs (e.g., μ_{eff} < 2000 cm^2/Vs [21]-[37]). Moreover, the gate leakage current density of buried channel InGaAs MOSFETs [38]-[40] can be several orders of magnitude lower than HEMTs [45] [46].

There are also other challenges for III-V MOSFETs such as small electron mass induced quantum capacitance [47], low density of states, low Γ-L valley separation, low hole mobility, and its process integration issues with Si industry. Moreover, the reported transistor characteristics, including the drive capability (saturation current and transconductance), electrostatic integrity (subthreshold swing (SS) and drain-induced-barrier-lowing (DIBL)) and the channel mobility, are still far from the satisfactory level. There is still a long way to go on successfully implementing III-V MOSFETs.

1.3 III-V TFETs with high-κ oxides

Nowadays, power and/or heat generation are the limiting factors of the down-scaling. The supply voltage reduction is becoming difficult because threshold voltage V_{th} cannot be decrease any more due to subthreshold leakage limitation (figure 1.4). Since there is a fundamental lower limit in the subthreshold swing (SS) (i.e. 60 mV/decade at room temperature) for conventional MOSFETs which rely on the thermionic emission of charge carriers over the source-to-channel barrier, the reduction of V_{th} results in increase of I_{off} and power consumption.

Inter-band tunneling field-effect-transistors (TFETs) with gate-modulated Zener tunneling junction can achieve SS < 60 mV/dec and operate at a lower supply voltage compared to MOSFETs [48]-[49], therefore they are considered potential candidates to

replace Si MOSFETs at low operating voltages for low-power digital applications. However, most of the efforts in the literature have been focused on Si and Ge based TFETs, which unfortunately exhibited a low on-current due to the high tunneling barrier [50]-[54]. III-V materials based TFETs may achieve larger tunneling currents compared to Si TFETs due to the smaller bandgap and the smaller electron mass [55]-[56]. So far, only a few reports have been published on experimental demonstrations of III-V TFETs. In Ref. [57], $In_{0.53}Ga_{0.47}As$ TFETs using 10 nm Al_2O_3 gate oxide with a saturation current of 20 μA/μm (V_g= 2 V) and a SS > 150 mV/dec were demonstrated for the first time. To successfully implement III-V TFETs, lots of efforts have to be put on to increase the on-current and decrease the subthreshold swing. The same issue of interface problems is facing by both III-V TFETs and III-V MOSFETs, thus proper interface engineering techniques can benefit both of them.

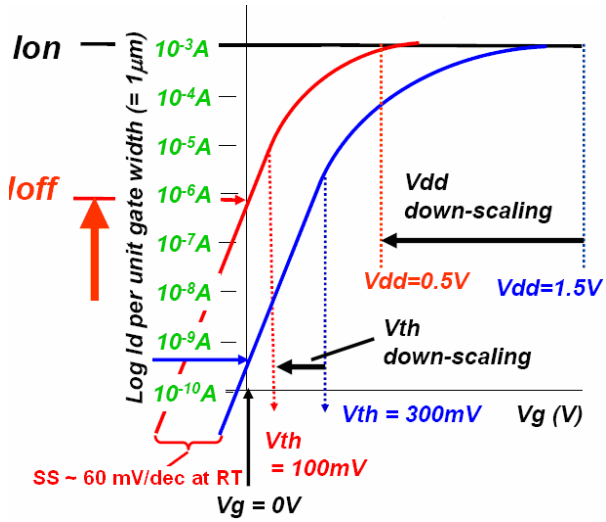

Figure 1.4 Log-scale I_d versus V_g for MOSFETs.

1.4 Outline

The motivation of this work is to explore the possibility of combining the high-κ gate dielectrics with the III-V substrates to implement high performance MOSFETs and TFETs for digital applications in the post-silicon era. To achieve this goal, various high-κ dielectrics were deposited on $In_{0.53}Ga_{0.47}As$ substrates to fabricate surface channel MOSFETs with gate-last process for good interface quality. Buried channel $In_{0.7}Ga_{0.3}As$ MOSFETs with single InP or InP/InAlAs barrier were investigated to further improve the mobility and on-current. $In_{0.7}Ga_{0.3}As$ TFETs using ALD HfO_2 with low EOT were also studied to increase the drive-current and reduce the subthreshold swing.

In chapter 2, the device performance of surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs is improved by process, substrate, interface, and oxide engineering techniques. Effects of gate-first and gate-last process on interface quality were compared. It has been found that applying gate-last process provides significant frequency dispersion reduction and interface trap density reduction for InGaAs devices compared to gate-first process. A large amount of In-O, Ga-O and As-As bonds was observed on InGaAs surface after gate-first process while no detectable interface reaction after gate-last process. By investigating the channel doping concentration and channel thickness dependence of device performance for $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD Al_2O_3 dielectrics, it has been found that undoped channel provides higher drive current compared to p-doped channel. With proper substrate doping concentration, reasonable subthreshold swing can be achieved. Thinner InGaAs channel exhibits lower off-current density. Among ALD Al_2O_3, HfO_2 and $LaAlO_3$ gate oxides, Al_2O_3 exhibits the best interface quality with InGaAs, HfO_2 exhibits the thinnest EOT, while $LaAlO_3$ gives better thickness scalability than Al_2O_3 and better interface quality than HfO_2. Inserting Al contained interfacial

dielectric between HfO_2 and InGaAs substrate has been demonstrated to effectively improve device performance including both SS and mobility.

Chapter 3 is dedicated to the buried channel InGaAs MOSFETs with single InP barrier layer with different thicknesses and InP/$In_{0.52}Al_{0.48}As$ double-barrier layer. InP barrier layer was found to provide MOSFETs with higher transconductance for both $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs, especially for $In_{0.7}Ga_{0.3}As$. $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier layer show much higher transconductance and peak mobility, and lower subthreshold swing than the ones without barrier. Devices using InP/$In_{0.52}Al_{0.48}As$ double-barrier achieve mobility enhancement at both low-field and high-field compared to the ones without barrier.

In chapter 4, a novel Ge_xN_y IPL was deposited between GaAs substrates and HfO_2 dielectric layer to improve the interface quality. Compared to Ge IPL, the Ge_xN_y IPL provides both lower slow trap density and lower trap generation rate. Moreover, effects of S passivation and post-deposition annealing (PDA) on device performance of InP gate-first inversion-type MOSFETs were investigated. Device characteristics of MOSFETs on both SI-InP substrates and p-InP substrates were compared and an asymmetric distribution of interface states along the bandgap between InP and ALD Al_2O_3 dielectric was suggested to be the reason for the difference.

In chapter 5, lateral-mode $In_{0.7}Ga_{0.3}As$ TFETs with vertical structure have been demonstrated with a high on-current of 50 μA/μm (in comparison to reported values) and a minimum SS of 86 mV/dec using ALD HfO_2 gate oxide. The tunneling diodes exhibited the gate bias dependent Esaki diode behavior with a negative differential resistance under the forward diode bias at various temperatures, which confirmed that the conduction mechanism is indeed band-to-band tunneling. The effects of EOT scaling and various temperatures on the on-current and the SS have also been investigated. By

increasing the undoped $In_{0.7}Ga_{0.3}As$ layer thickness, another >80% increase of on-current can be achieved. Using Al_2O_3/ HfO_2 bilayer gate oxide could effectively improve the SS but not the on-current. Vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs with vertical-structure have also been fabricated and characterized.

Chapter 6 summarizes the results. In addition, the future work is discussed.

Chapter 2 Surface channel InGaAs MOSFETs with ALD gate oxides

2.1 Effects of gate-first and gate-last process on interface quality of $In_{0.53}Ga_{0.47}As$ MOSCAPs using ALD Al_2O_3 and HfO_2 oxides

Source and drain (S/D) usually need to be formed by ion implantation and thermal activation for surface-channel inversion-mode MOSFETs. However, dielectric/ semiconductor interface quality may degrade during this high temperature S/D activation annealing process for III-V MOS structure.

In this section, we applied S/D activation process on metal-oxide-semiconductor capacitors (MOSCAPs) to investigate the effect of this process on oxide/III-V interface quality. We compared the interface quality of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ALD Al_2O_3 and HfO_2 oxides under three process conditions: (a) only post deposition annealing (PDA-only), no S/D activation, (b) gate-first process (S/D activated after gate stack deposition) [58], (c) gate-last process (S/D activated before gate stack deposition) [59]. It has been found that MOSCAPs with gate-last process can maintain similar interface trap density (D_{it}) as PDA-only samples, while the ones with gate-first process have much larger D_{it}. This suggests that gate-last process is more promising for surface-channel inversion-type III-V MOSFETs. Moreover, D_{it} is higher for MOSCAPs with HfO_2 oxide than with Al_2O_3. X-ray photoelectron spectroscopy (XPS) indicates that gate-first process results in a larger amount of In-O, Ga-O and As-As bonds on InGaAs surface, while gate-last process maintains similar surface chemical bonding condition as PDA-only process. MOSCAPs with HfO_2 exhibit more Ga-O bonds than the ones with Al_2O_3 and similar In or As bonding condition to Al_2O_3. Transmission electron microscopy **(**TEM) and electron energy loss spectroscopy (EELS) analysis show that MOSCAPs with HfO_2 using gate-

first process exhibit thicker interfacial layer and more intermixing between oxide and substrate than using gate-last process.

$In_{0.53}Ga_{0.47}As$ MOSCAPs were fabricated on 400nm n-type $In_{0.53}Ga_{0.47}As$ (Si-doped, $5\times10^{16}/cm^3$) epitaxially grown on n-InP substrate. Three different process conditions were applied: (a) PDA-only, (b) gate-first process (G-first), (c) gate-last process (G-last). Table 2.1 shows the process flow chart for these three processes. 6 nm Al_2O_3 (capacitance equivalent thickness (CET) =4.2 nm) or 7 nm (CET=2.1 nm) HfO_2 were deposited on different samples for gate dielectrics.

Figure 2.1 illustrates typical capacitance-voltage (C-V) characteristics of $TaN/Al_2O_3/InGaAs$ and $TaN/HfO_2/InGaAs$ MOSCAPs using PDA-only process and gate-first process. The C-V curves of MOSCAPs using gate-last process are the same as PDA-only process (data not shown), indicating similar interface quality by applying gate-last process as PDA-only process. Gate-first process exposes gate stacks on InGaAs at high temperature and degrades interface quality, thus causes higher frequency dispersion on C-V curves. Larger frequency dispersion of MOSCAPs with HfO_2 compared to Al_2O_3 indicates higher D_{it} for HfO_2 samples. D_{it} at upper half of the bandgap of MOSCAPs with different processes was measured using conductance method (figure 2.2). Low temperature (150K) measurement allows detecting D_{it} close to bandedge [60]-[61]. It is clearly seen that MOSCAPs using gate-last process have similar D_{it} as PDA-only samples, while gate-first process results in much larger value of D_{it}. MOSCAPs with Al_2O_3 have smaller D_{it} value than HfO_2.

Table 2.1 Process Flow Chart

PDA-only	G-first	G-last
1. Wafer cleaning and S passivation 2. ALD gate dielectrics 3. PDA at 500℃, 90s in N_2 4. TaN gate metal and backside metal deposition	1. Wafer cleaning and S passivation 2. ALD gate dielectrics 3. PDA at 500℃, 90s in N_2 4. TaN gate metal and backside metal deposition 5. S/D activation at 700℃, 10s in N_2	1. Wafer cleaning and S passivation 2. 10nm ALD Al_2O_3 capping layer 3. S/D activation at 700℃, 10s in N_2 4. Remove capping layer 5. Wafer cleaning and S passivation 6. ALD gate dielectrics 7. PDA at 500℃, 90s 8. TaN gate metal and backside metal

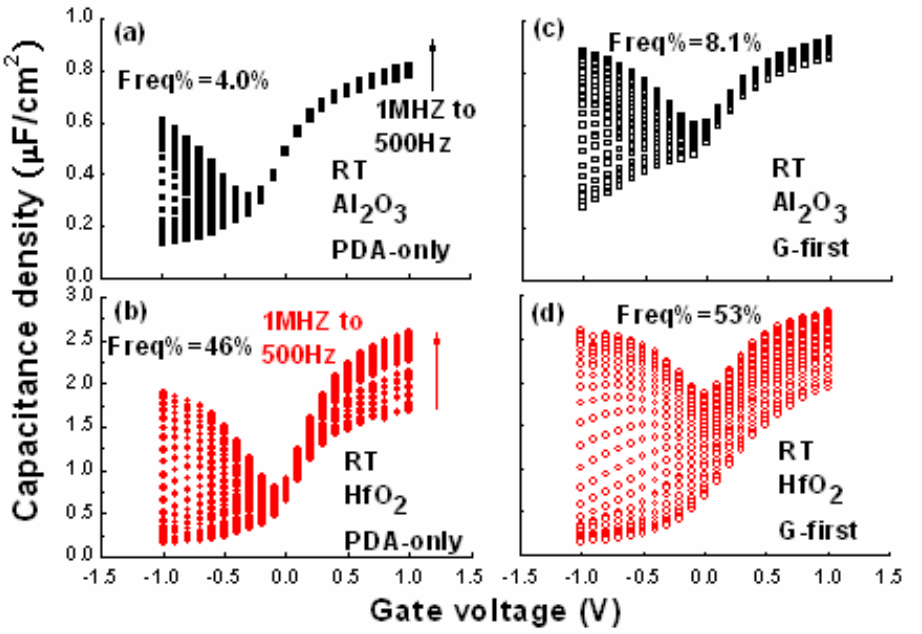

Figure 2.1 C-V characteristics of TaN/Al_2O_3/InGaAs and TaN/HfO_2/InGaAs MOSCAPs as a function of frequencies from 1 MHz to 500 Hz at room temperature using PDA-only process and gate-first process (freq%=(C_{500Hz}-C_{1MHz})/C_{1MHz}, at V_g=1 V).

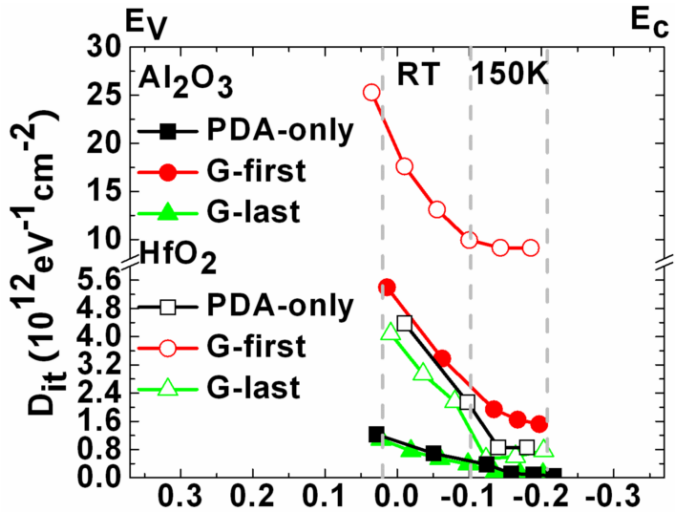

Figure 2.2 D_{it} versus energy position at bandgap for InGaAs MOSCAPs with Al_2O_3 and HfO_2 oxides using PDA-only, gate-first and gate-last process.

XPS was measured on different samples using processes including PDA-only, G-first and G-last (figure 2.3 and figure 2.4). Ga^{+3}-O bond is fitted at about 1.1 eV above Ga-As bond, Ga^{+1}-O bond and Ga-S bond [62]-[63] is under the detection limit, this might be because that we have comparably thick Al_2O_3 or HfO_2 (25 to 30Å) for our ex-situ XPS measurement. There is no As-O detected for both Al_2O_3 and HfO_2 using gate-last process and the substrate oxide self-cleaning effect during ALD oxides deposition [64]-[66] is considered to be the reason. Some As^{+3}-O bonds were detected for HfO_2 with gate-first process. The line shape for the In spectra, even for a surface that is oxygen free, is asymmetric [67]. This makes the deconvolution of In spectra exceedingly difficult, thus we only pointed out the difference in In spectra between gate-first and gate-last process. For gate-first samples, it is obvious that the excessive In oxide growth has changed the shape of In spectra dramatically. For InGaAs MOSCAPs with Al_2O_3 gate dielectrics (figure 2.3), samples with gate-last process exhibit similar amount of surface oxide components as PDA-only samples, indicating no interface reaction at Al_2O_3/InGaAs interface. On the other hand, samples with gate-first process show excessive interfacial

oxidation and increased In-O, Ga-O and As-As on the substrate surface. This explains why the samples using gate-last process can maintain similar D_{it} as the ones using PDA-only process while samples using gate-first process exhibit increased D_{it}. InGaAs MOSCAPs with HfO_2 gate dielectrics (figure 2.4) show similar trend of surface oxides condition for different processes as the ones with Al_2O_3, except that MOSCAPs with HfO_2 using gate-first process show even much larger amount of surface oxides than the ones with Al_2O_3 and those with HfO_2 using gate-last process show larger amount of Ga-O component than with Al_2O_3, which might be responsible for the higher D_{it} for MOSCAPs with HfO_2.

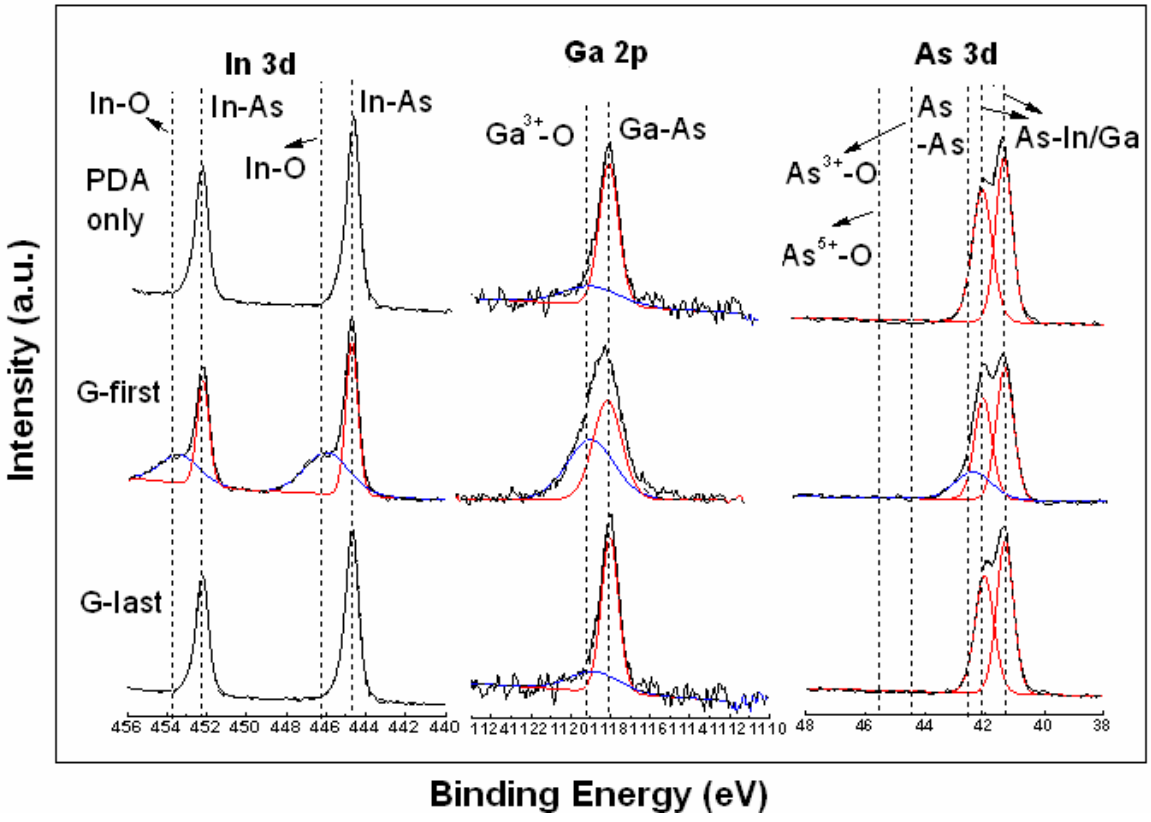

Figure 2.3 XPS spectra of In 3d, Ga 2p and As 3d after applying PDA-only, gate-first and gate-last process for Al_2O_3/InGaAs structure.

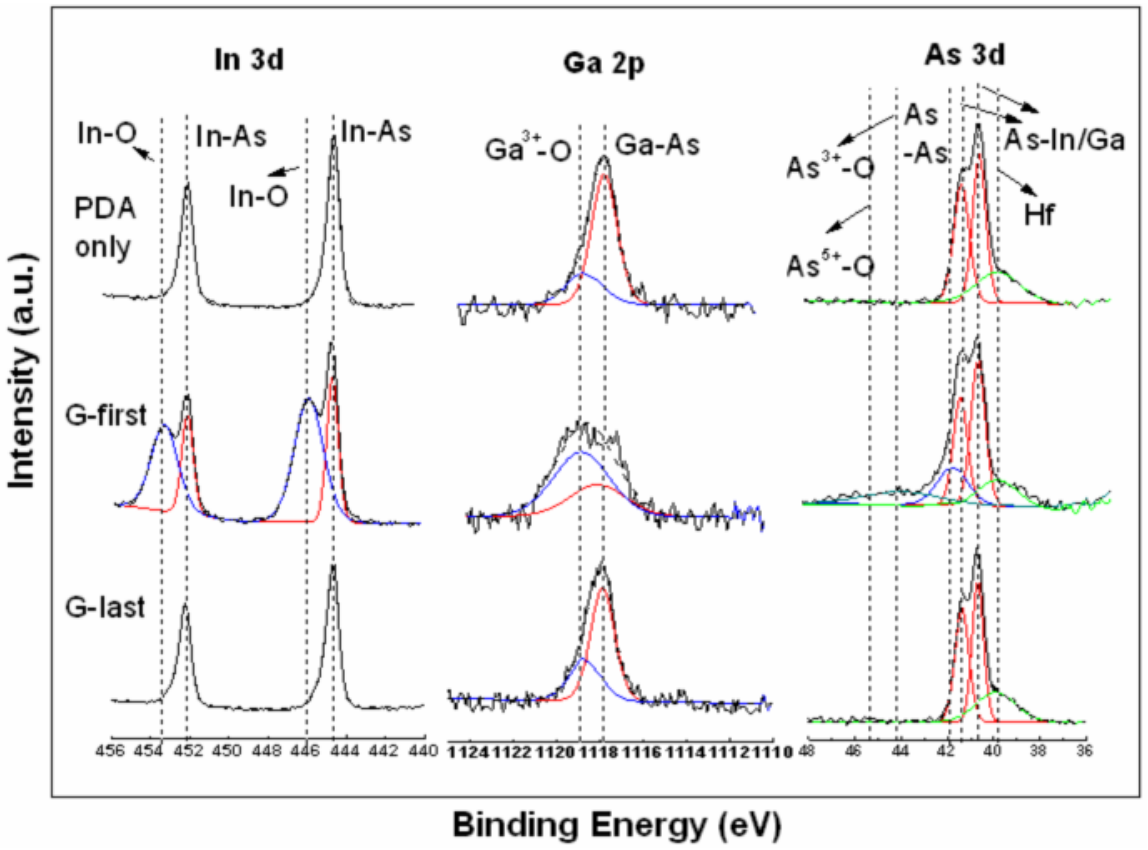

Figure 2.4 XPS spectra of In 3d, Ga 2p and As 3d after applying PDA-only, gate-first and gate-last process for HfO_2/InGaAs structure.

Figure 2.5 illustrates the high-resolution bright-field and dark field scanning TEM and EELS analysis of MOSCAPs with HfO_2 using gate-first and gate-last process. There is evidence of an interfacial layer approximately 0.5 nm thick right at the interface between InGaAs and HfO_2 using gate-first process in dark-field TEM. The interfacial oxide is still undetectable using gate-last process with dark-field TEM. The EELS analysis shows clearly that the samples with gate-first process have larger oxide/substrate interfacial mixing than with gate-last process.

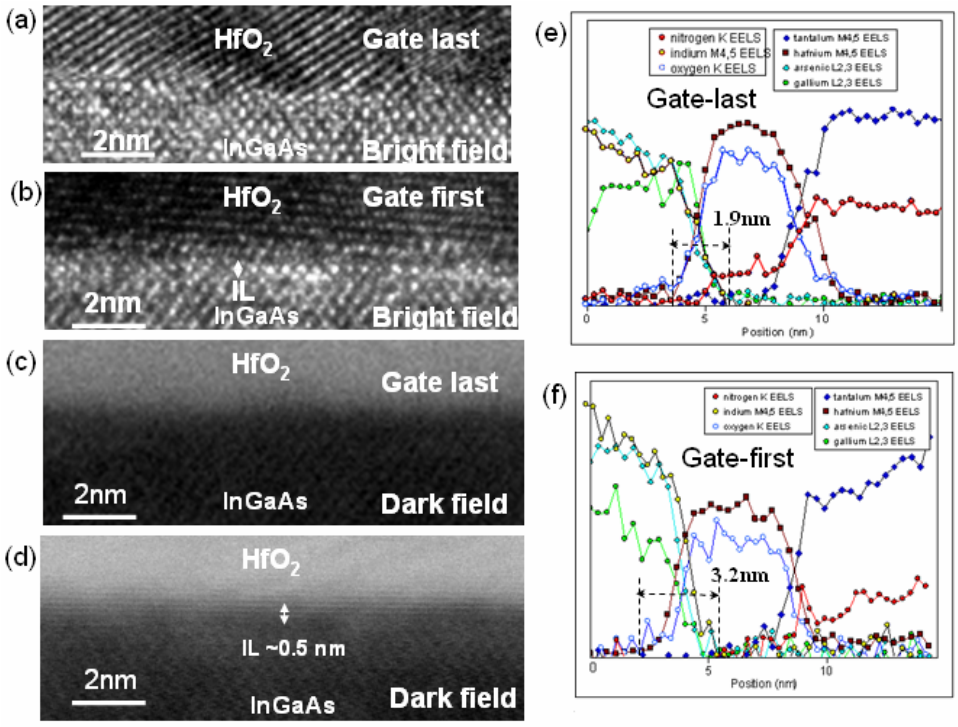

Figure 2.5 High-resolution bright-field TEM ((a)-(b)), dark-field TEM ((c)-(d)) and EELS ((e)-(f)) of MOSCAPs with HfO_2 using gate-first and gate-last process.

In conclusion, we have fabricated $In_{0.53}Ga_{0.47}As$ MOSCAPs with ALD Al_2O_3 and HfO_2 oxides by applying three different processes including PDA-only process, gate-first and gate-last process. Samples using HfO_2 oxide show larger D_{it} than Al_2O_3, which is resulted from more Ga-O bonds on HfO_2/InGaAs samples than Al_2O_3/InGaAs samples indicated by XPS spectra. MOSCAPs with gate-first process have much larger D_{it} than PDA-only process while the ones with gate-last process remain similar D_{it} value as PDA-only samples. TEM and EELS results indicate that MOSCAPs with HfO_2 using gate-first process exhibit thicker interfacial layer and more intermixing between oxide and substrate than using gate-last process. These results suggest that gate-last process is preferable over gate-first process for surface-channel inversion-type III-V MOSFETs.

2.2 Effect of channel doping concentration and thickness on device performance for $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD Al_2O_3 dielectrics

High drive current density of 400 mA/mm for 0.5 μm $In_{0.53}Ga_{0.47}As$ channel [68] and 1 A/mm for 0.4 μm $In_{0.65}G_{0.35}As$ channel [21] using ALD Al_2O_3 gate dielectric, 0.9 A/mm for 1 μm $In_{0.53}Ga_{0.47}As$ channel using MBE $Ga_2O_3(Gd_2O_3)$ gate dielectric [69] has been reported recently. The drive current is comparable to 65 nm strained Si channel technology (I_{on}=1.6 mA/μm, subthreshold swing=105 mV/dec) [70] even with much longer gate length and thicker EOT. However, InGaAs surface channel n-MOSFETs usually exhibit fairly high off current density (e.g. 5×10^{-4} mA/mm [68]) and large subthreshold swing (e.g. 179 mV/dec [71], 240 mV/dec [68], 330 mV/dec [21]). In our work, we investigate the effects of $In_{0.53}Ga_{0.47}As$ doping concentration and thickness on the MOSFETs device performance. By carefully engineering the channel doping concentration and thickness with ALD Al_2O_3 gate dielectrics, reasonable subthreshold swing of 104 mV/dec and low off-current density of 4.0×10^{-6} mA/mm have been obtained.

$In_{0.53}Ga_{0.47}As$ MOSFETs were fabricated by gate-last process on 200 nm undoped $In_{0.53}Ga_{0.47}As$ (sample (a)), or on 300 nm p-type $In_{0.53}Ga_{0.47}As$ (Be-doped, 2×10^{16} /cm^3, sample (b)), or on 30 nm p-type $In_{0.53}Ga_{0.47}As$ (2×10^{16} /cm^3, sample (c)), or on 300 nm p-type $In_{0.53}Ga_{0.47}As$ (5×10^{16} /cm^3, sample (d)). Note that sample (a) was grown on SI- InP substrate and an undoped InAlAs buffer layer was grown before InGaAs layer. Samples (b), (c) and (d) were all grown on p-InP substrates and a p-InAlAs buffer layer was grown before p-InGaAs. The surface oxides of InGaAs were removed with diluted hydrofluoric acid (HF) cleaning, then 100Å Al_2O_3 capping layer was deposited by ALD. After 35 keV, 2×10^{14} /cm^2 Si ion implantation at the source and drain (S/D) region, S/D activation annealing was performed at 700 ℃ for 10 s. The Al_2O_3 capping layer was removed using buffered oxide etch (BOE). Gate oxide (90 Å Al_2O_3) was then deposited

by ALD (EOT=4.7 nm) after HF cleaning and sulfur passivation of the surface. After 500 ℃ post-deposition annealing, TaN gate electrode was deposited by PVD and AuGe/Ni/Au S/D ohmic contact was deposited by E-beam evaporation. For p-type substrates, Cr/Au was used for back contact. The inset of figure 2.6 shows the cross section structures of sample (a) to (d).

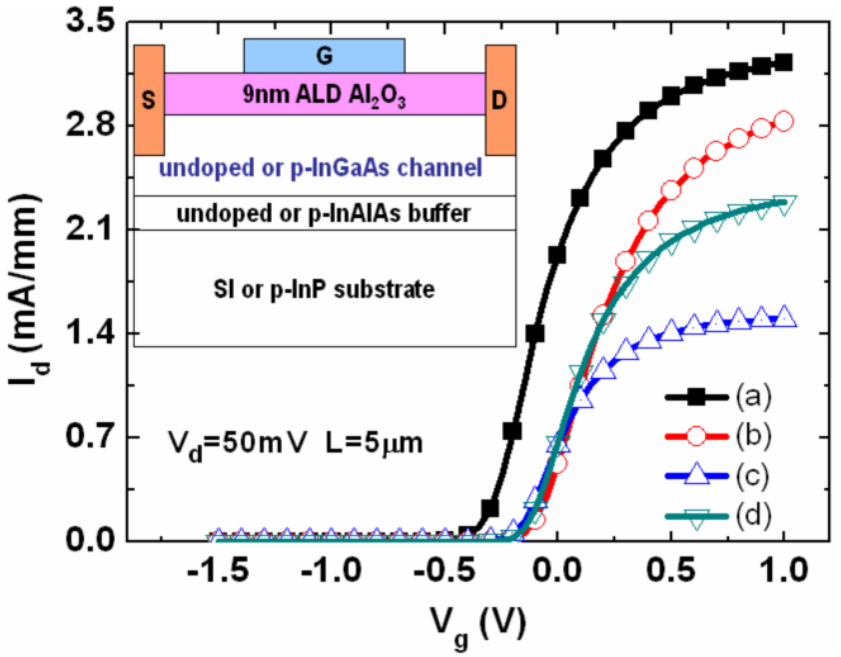

Figure 2.6 I_d-V_g characteristics at V_d=50 mV for sample (a) to sample (d) with gate width (W) of 600 μm and gate length (L) of 5 μm. (a): 200 nm undoped $In_{0.53}Ga_{0.47}As$ channel; (b): 300 nm p-type $In_{0.53}Ga_{0.47}As$ channel with 2×10^{16} /cm^3 doping concentration; (c): 30 nm p-type $In_{0.53}Ga_{0.47}As$ with 2×10^{16} /cm^3 doping concentration; (d): 300 nm p-type $In_{0.53}Ga_{0.47}As$ with 5×10^{16} /cm^3 doping concentration. Inset shows cross section structures of sample (a) to sample (d).

Table 2.2 summarizes the device performance for sample (a) to (d). Figure 2.6 and figure 2.7 compare the I_d-V_g curves at V_d=50 mV and I_d-V_d curves at different V_g values from V_{th} to V_{th}+2 V for sample (a) to (d). The gate length is 5 μm and gate width is 600 μm. Undoped InGaAs channel (sample (a)) shows the lowest threshold voltage (-

0.31 V) and the highest drive current density (125 mA/mm at V_g-V_{th}=2 V). Sample (d) (300 nm p-InGaAs, 5×10^{16} /cm^3) exhibits slightly lower drive current (80 mA/mm vs 83 mA/mm) than sample (b) (300 nm p-InGaAs, 2×10^{16} /cm^3), and sample (c) (30 nm p-InGaAs) shows the lowest drive current density (55 mA/mm). The extrinsic transconductance at V_d=50 mV (figure 2.8) shows a similar trend as the drive current density for sample (a) to (d). The maximum extrinsic transconductance is 6.5 mS/mm at V_d=0.05 V and 70.5 mS/mm at V_d=2 V for sample (a). In addition to reduced ionized impurity scattering from undoped InGaAs, the different carrier distribution is another important reason for the better current driving capability on undoped InGaAs channel. Since the "undoped" InGaAs is very lightly n-type doped (10^{14} /cm^3) in reality, MOSFETs on undoped InGaAs are actually buried channel transistors. The channel of MOSFETs on p-type InGaAs (surface channel MOSFETs) is closer to the InGaAs/Al_2O_3 interface, which will be degraded more by the interface roughness scattering and interface states.

Table 2.2. Device performances for sample (a) to (d)

Samples L=5μm W=600μm	V_{th} (V) (nonuniformity ±0.05V)	I_d @ V_g-V_{th}=2V (mA/mm)	g_{mmax} @ V_d=50mV (mS/mm)	SS (mV/ dec)	I_{off} I_d@V_g=-1V (mA/mm)	Maximum μ_{eff} (cm^2/Vs)
(a) undoped-InGaAs 200nm	-0.31	125	6.5	147	1.7×10^{-4}	1964
(b) p-InGaAs 2×10^{16}/cm^3 300nm	-0.10V	83	5.3	121	4.8×10^{-4}	1120
(c) p-InGaAs 2×10^{16}/cm^3 30nm	-0.17V	55	3.7	116	4.0×10^{-6}	847
(d) p-InGaAs 5×10^{16}/cm^3 300nm	-0.14V	80	5.0	104	6.1×10^{-5}	1066

Figure 2.8 also shows the log(I_d)-V_g at V_d=50 mV for sample (a) to (d). For undoped InGaAs(sample (a)), the off-current density is 1.7×10^{-4} mA/mm at V_g=-1 V and the subthreshold swing (SS) is 147 mV/mm. Sample (d) (300 nm p-InGaAs, 5×10^{16} /cm^3) shows the minimum subthreshold swing of 104 mV/dec while sample (b) (300 nm p-InGaAs, 2×10^{16} /cm^3) exhibits 121 mV/dec. The off-current densities are 4.8×10^{-4} mA/mm and 6.1×10^{-5} mA/mm respectively at V_g=-1 V for sample (b) and (d). Sample (c) (30 nm p-InGaAs, 2×10^{16} /cm^3) exhibits the lowest off-current of 4.0×10^{-6} mA/mm. The off-current is believed to be due to S/D junction leakage [71], and for thinner InGaAs channel sample, S/D (x_j=500 Å) diffuses into the larger band-gap InAlAs buffer region, thus resulting in lower I_{off}. Sample (d) has smaller depletion width than sample (b) due to its higher doping concentration, which leads to smaller off-current density. The high I_{off} of sample (b) degrades its subthreshold swing.

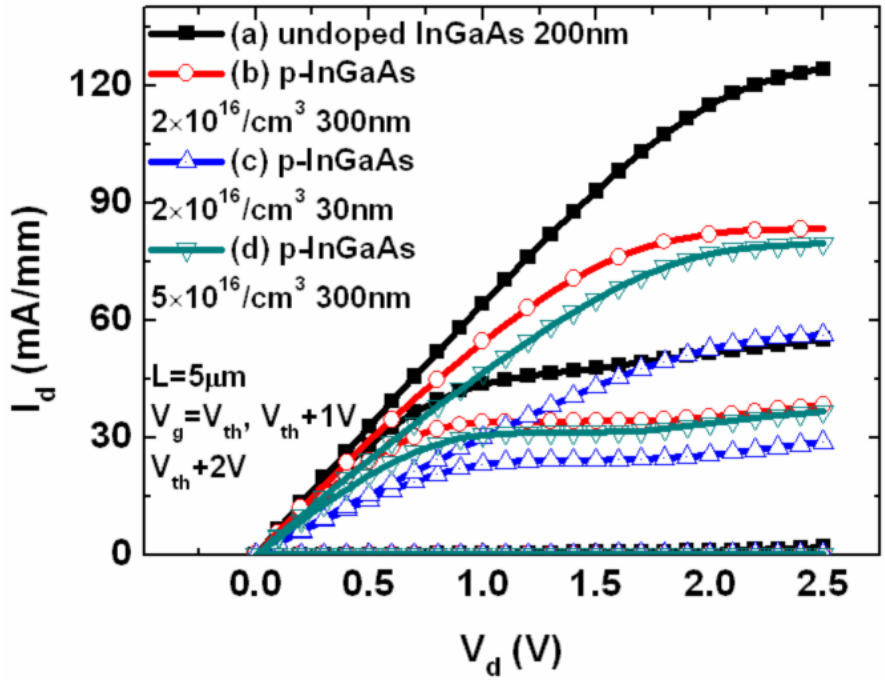

Figure 2.7 I_d-V_d characteristics at V_g=V_{th}, V_g=V_{th}+1 V, V_g=V_{th}+2 V for sample (a) to sample (d). W=600 μm, L=5 μm.

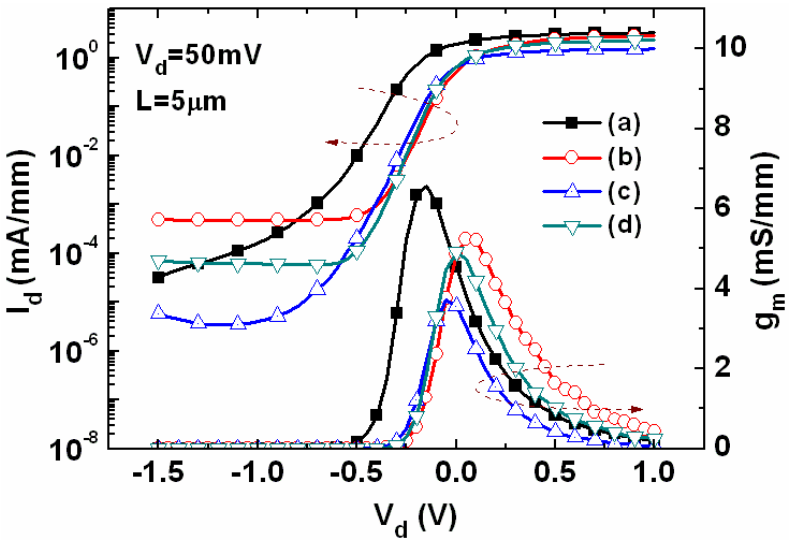

Figure 2.8 Log-scale I_d-V_g and extrinsic transconductance g_m versus V_g and at V_d=50 mV for sample (a) to sample (d). W=600 μm, L=5 μm.

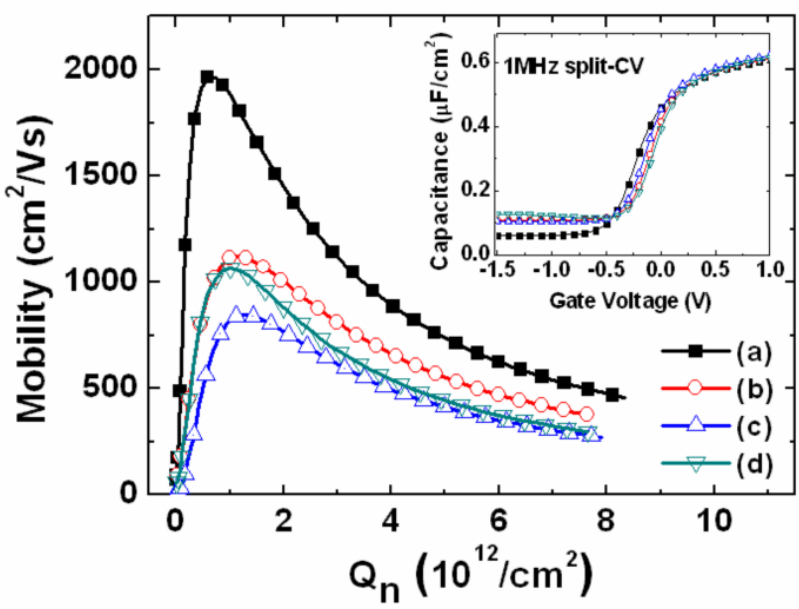

Figure 2.9 Effective channel mobility versus inversion charge density for sample (a) to sample (d). W=600 μm, L=20 μm. Inset shows 1 MHz split-CV of sample (a) to (d).

From split-CV measurement, the frequency dispersion is less than 3% at V_g=2 V from 1 MHz to 10 KHz for all four samples. The maximum mobility is 1964 cm^2/Vs,

1120 cm^2/Vs, 847 cm^2/Vs, and 1066 cm^2/Vs from sample (a) to sample (d) respectively, calculated from 1 MHz split-CV (see figure 2.9, inset shows the 1 MHz split-CV for sample (a) to (d)). Lower ionized impurity scattering and reduced interface scattering are believed to be responsible for the higher mobility of the undoped InGaAs samples.

In summary, the impact of $In_{0.53}Ga_{0.47}As$ channel doping concentration and thickness on device performance has been studied. The undoped channel provides the highest drive current but relatively poor subthreshold swing. With proper substrate doping concentration ($5\times10^{16}/cm^3$), small subthreshold swing can be achieved. Thinner InGaAs channel exhibits lower off-current density but also relatively low drive current.

2.3 $In_{0.53}Ga_{0.47}As$ n-MOSFETs with ALD Al_2O_3, HfO_2 and $LaAlO_3$ gate dielectrics

Various high-κ gate dielectrics have been demonstrated on III-V MOSFETs with high drive current density. However, MOS device performance, equivalent oxide thickness (EOT) scalability, and high-κ dielectric/III-V interface quality using different gate dielectrics on III-V substrate have not been fairly compared.

This work systematically compares the characteristics of $In_{0.53}Ga_{0.47}As$ n-MOSFETs with different gate dielectrics (Al_2O_3, HfO_2 and $LaAlO_3$) deposited by ALD. HfO_2 is demonstrated to have the best EOT scalability, while Al_2O_3 exhibits the best interface quality with InGaAs substrates. By using $LaAlO_3$, transistors can achieve smaller EOT than Al_2O_3 and accordingly smaller subthreshold swing. Al_2O_3 on $In_{0.53}Ga_{0.47}As$ shows minimum interface trap density D_{it} of 1.17×10^{12} $/cm^2$, MOSFETs with HfO_2 dielectric demonstrate the minimum EOT of 1 nm with drive current of 133.3 mA/mm for 5 μm gate length and MOSFETs with $LaAlO_3$ gate dielectric have obtained subthreshold swing of 84 mV/dec for 1.3 nm EOT.

$In_{0.53}Ga_{0.47}As$ MOSFETs were fabricated on 300 nm p-type $In_{0.53}Ga_{0.47}As$ (Be-doped, 5×10^{16} /cm^3) epitaxially grown on p-InP substrate with ring-type structure. The surface oxides of InGaAs were removed with diluted HF cleaning, then 100 Å Al_2O_3 (dummy capping layer) was deposited by ALD. After 35 keV, 2×10^{14} /cm^2 Si ion implantation at the source and drain (S/D) region, S/D activation annealing was performed at 700 ℃ for 10 s. The Al_2O_3 was removed using buffered oxides etch (BOE). Different gate oxides were then deposited by ALD including Al_2O_3 with varied thicknesses from 9 nm to 4.2 nm, HfO_2 from 7.8 nm to 4.5 nm, and $LaAlO_3$ from 5.9 nm to 3.6 nm. After 500℃ post-deposition annealing, TaN gate electrode was deposited by reactive sputter, AuGe/Ni/Au was deposited by E-beam evaporation for source and drain ohmic contact while Cr/Au for back contact.

Figure 2.10(a) shows the EOT versus physical thicknesses for different gate dielectrics. The EOT value was obtained at the inversion region from split-CV of MOSFETs. HfO_2 shows the highest dielectric constant (κ) value of 17.0 and the thinnest EOT of 1nm with 4.5 nm physical thickness. $LaAlO_3$ obtains κ value of 12.1 and Al_2O_3 shows κ value of 8.1. HfO_2 is demonstrated to have the best EOT scalability. The electron barrier height between Al_2O_3 and $In_{0.53}Ga_{0.47}As$ is usually larger than that between HfO_2 or $LaAlO_3$ and $In_{0.53}Ga_{0.47}As$ [72]-[74]. Figure 2.10(b) compares the gate leakage current density at V_g=1 V for different gate dielectrics. For similar EOT of about 2.2 nm, Al_2O_3 has larger gate leakage current than HfO_2 and $LaAlO_3$. The gate leakage current density is about 0.80 A/cm^2 for EOT of 1 nm using HfO_2, 0.2 A/cm^2 for EOT of 1.3 nm using $LaAlO_3$ and 0.48 A/cm^2 for EOT of 2.4 nm using Al_2O_3.

The threshold voltages for various gate dielectrics with different thicknesses were measured and shown in figure 2.11. For Al_2O_3 and $LaAlO_3$, the threshold voltage increases with reduced EOT, which is believed to be due to the positive fixed charges in

the dielectrics. The positive fixed charges may come from oxygen vacancies. They may also exist in HfO_2, but not as many as they are in Al_2O_3 or $LaAlO_3$.

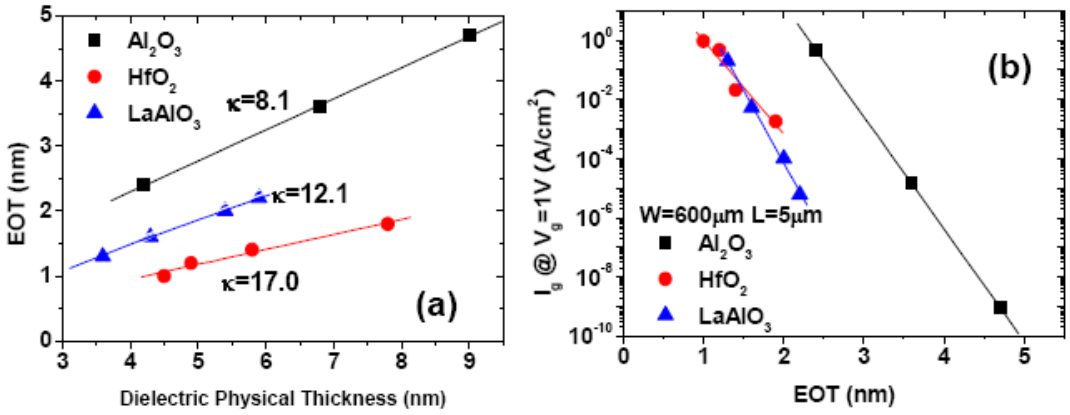

Figure 2.10 (a) EOT versus physical thicknesses for different gate dielectrics including HfO_2, $LaAlO_3$ and Al_2O_3. (b) Gate leakage current density at V_g=1 V and V_d=50 mV for MOSFETs using different gate dielectrics with various thicknesses (W=600 μm, L=5 μm).

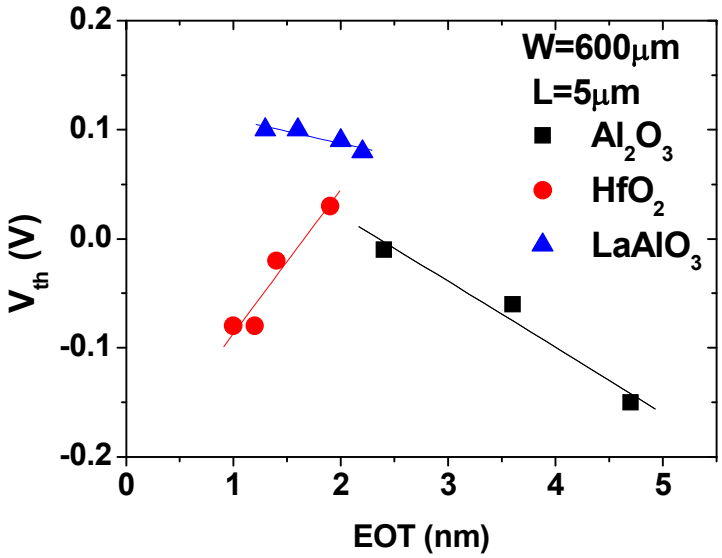

Figure 2.11 Threshold voltage for different gate dielectrics with various thicknesses.

Figure 2.12(a) and figure 2.12(b) compare the drive current capability (V_g-V_{th}=2.5 V & V_d=2.5 V) and maximum extrinsic transconductance G_{mmax} (V_d=0.05 V) for different gate dielectrics including Al_2O_3, HfO_2 and $LaAlO_3$. From the figure, for similar EOT of about 2.2 nm, Al_2O_3 has the highest drive current density and transconductance which indicates its best interface quality with InGaAs substrate among these three kinds of dielectrics. This is demonstrated by D_{it} value (figure 2.13) measured using full-conductance method at room temperature with frequency range from 100Hz to 1MHz. Full-conductance method on MOSFETs with S/D and bulk shorted provides a reliable solution to extract D_{it} with minority carrier responses for small bandgap materials [75]. From figure 2.13, we can see Al_2O_3 has the best interface quality (minimum D_{it} =1.17$\times$ 10^{12} /cm^2/eV) with InGaAs substrate; while HfO_2 has minimum D_{it} of 4.41$\times 10^{12}$ /cm^2/eV. In figure 2.13, when V_g-V_{th}=0, the position of D_{it} is close to conduction band edge (surface fermi level close to conduction band). D_{it} first decreases then increases as surface fermi level moves towards valence band (V_g-V_{th}< 0). Thus figure 2.13 illustrates an asymmetric D_{it} distribution along bandgap at high-κ dielectric/InGaAs interface, higher D_{it} near valence band is indicated. Due to the comparably high interface trap density and inadequate data for capture cross section of trap states, it is difficult to locate the position of D_{it} in bandgap accurately. V_g-V_{th} is used here to roughly indicate the location of D_{it}. Figure 2.14 shows the split-CV of MOSFETs (gate to channel capacitance) with different dielectrics at various frequencies from 1 KHz to 1 MHz. Al_2O_3 has smaller frequency dispersion value than HfO_2 and $LaAlO_3$, also indicating its better interface quality with InGaAs substrate.

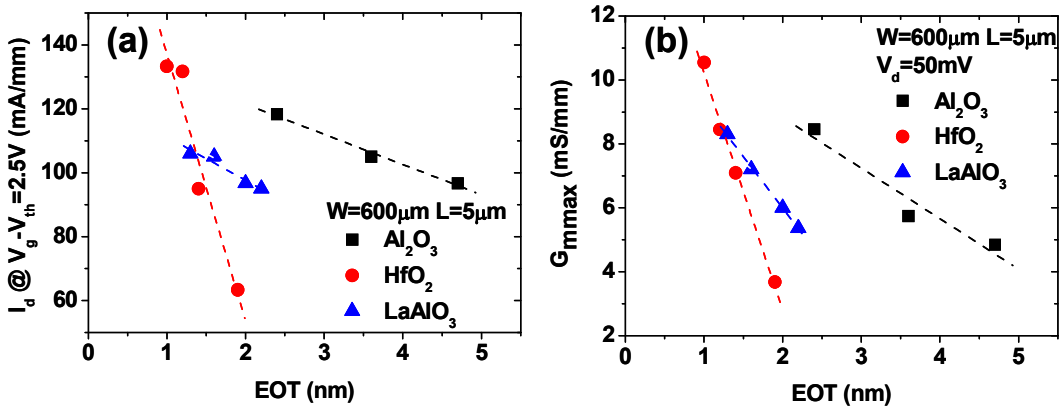

Figure 2.12 (a) Drive current density at V_g-V_{th}=2.5 V and V_d=2.5 V for MOSFETs using different gate dielectrics including Al_2O_3, HfO_2, and $LaAlO_3$ with various thicknesses. (W=600 μm, L=5 μm). (b) Maximum extrinsic transconductance for different gate dielectrics (W=600 μm, L=5 μm, V_d=50 mV).

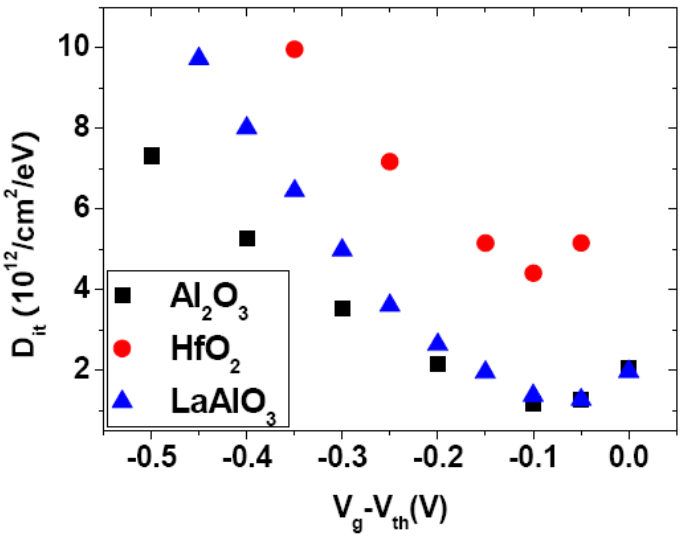

Figure 2.13 D_{it} distribution for MOSFETs with similar EOT of 2.2 nm using different gate dielectrics (Al_2O_3, HfO_2, and $LaAlO_3$).

Figure 2.15 shows the maximum effective channel mobility calculated from split-CV method for MOSFETs with different gate dielectrics. Long gate length of 20 μm was used to minimize the effect of source/drain contact resistance. As one can see, Al_2O_3 has

the highest electron mobility which is believed to be due to its best interface quality with InGaAs substrate. There is no dependence of dielectric thicknesses on effective channel mobility from figure 2.15. The differences of mobility among different EOT are believed to be due to sample variation and device non-uniformity.

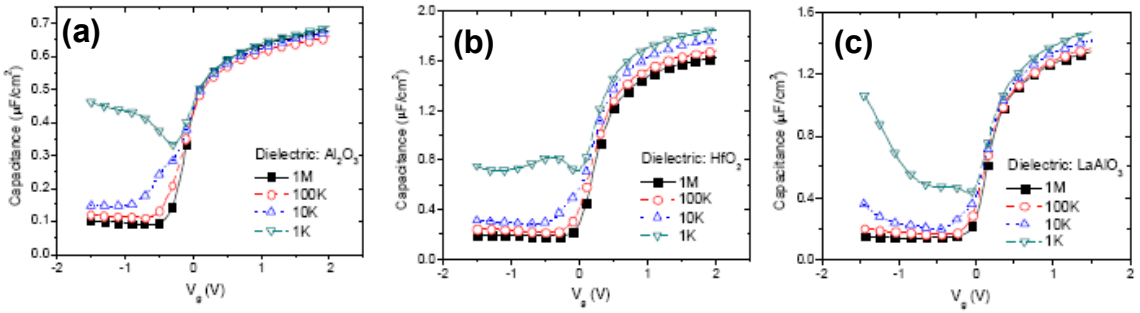

Figure 2.14 Split-CV at various frequencies from 1 KHz to 1 MHz for MOSFETs with 9 nm Al_2O_3 (a), 7.8 nm HfO_2 (b), and 5.9 nm $LaAlO_3$ (c) gate dielectrics.

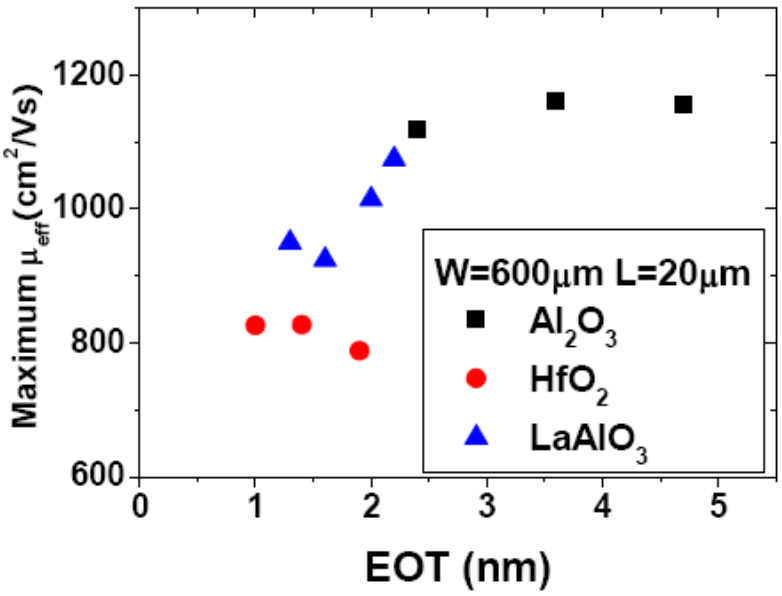

Figure 2.15 Maximum effective channel mobility for MOSFETs using different gate dielectrics including Al_2O_3, HfO_2, and $LaAlO_3$ with various thicknesses. (W=600 μm, L=20 μm).

Figure 2.16 illustrates the subthreshold swing for different gate dielectrics at V_d=50 mV. From equation

$$SS \cong \frac{kT}{q} \ln 10\{1 + \frac{C_D + C_{it}}{C_{ox}}\} \tag{2.1}$$

$$C_{it} = q \times D_{it} \tag{2.2}$$

HfO_2 has larger D_{it} value than Al_2O_3 and $LaAlO_3$ and thus larger subthreshold swing. $LaAlO_3$ can achieve smaller EOT than Al_2O_3 (larger C_{ox}) and thus smaller subthreshold swing. The minimum subthreshold swing of 84mV/dec was obtained by $LaAlO_3$ with EOT of 1.3nm. For V_d=1 V, the subthreshold swing increase by 10 to 20mV/dec due to source and drain junction leakage [76].

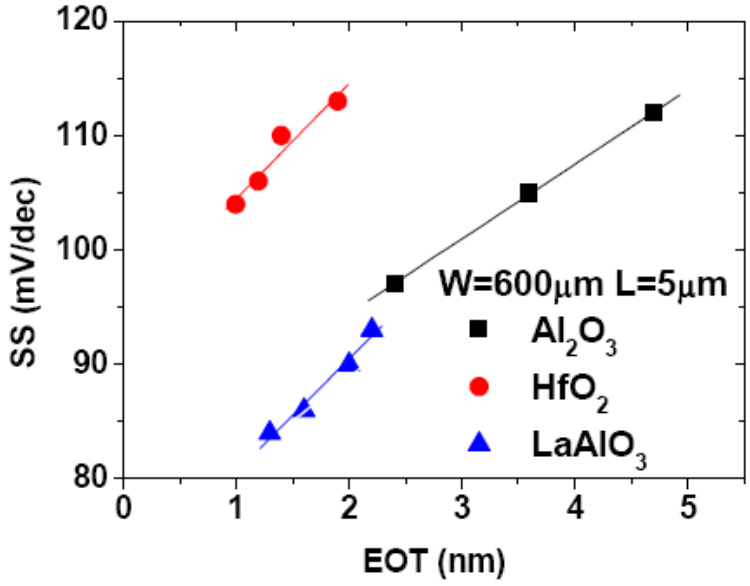

Figure 2.16 SS at V_d=50 mV for MOSFETs using different gate dielectrics with various thicknesses. (W=600 μm, L=5 μm)

Figure 2.17(a) and 2.17(b) show the characteristics of InGaAs n-MOSFETs with EOT of 1nm using HfO_2 gate dielectric. Figure 2.17(a) shows the drive current I_d, gate leakage current I_g and extrinsic transconductance g_m as a function of V_g at V_d=50 mV for 5 μm gate length. The transistor has SS of 104 mV/dec. The maximum extrinsic transconductance is 10.5 mS/mm at V_d=50 mV and 67.5 mS/mm at V_d=1 V. Figure 2.17(b) shows the I_d-V_d curves at V_g=V_{th} to V_g=V_{th}+2.5 V. High drive current density of 133.3 mA/mm at V_g-V_{th}=2.5 V was obtained for 5 μm gate length. Figure 2.18 illustrates the characteristics of InGaAs n-MOSFETs with EOT of 1.3 nm using $LaAlO_3$ gate dielectric. Figure 2.18(a) shows I_d, I_g and g_m as a function of V_g while figure 2.18(b) shows the I_d-V_d curve at various V_g value. The minimum subthreshold swing of 84 mV/dec was obtained. The maximum extrinsic transconductance is 8.8 mS/mm at V_d=50 mV and 53.8 mS/mm at V_d=1 V, respectively.

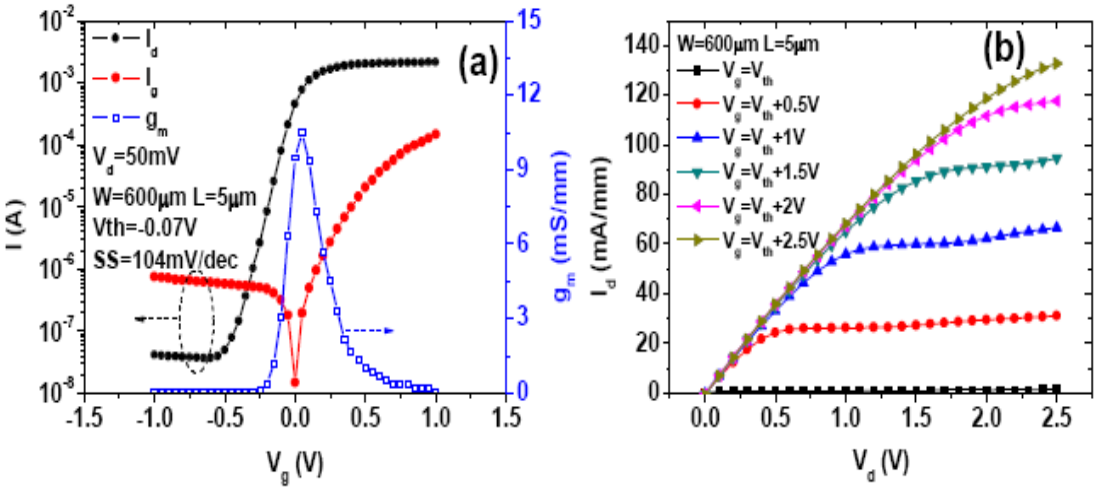

Figure 2.17 (a) I_d, I_g and extrinsic transconductance g_m as a function of V_g for MOSFETs with HfO_2 gate dielectric (EOT=1 nm) at V_d=50 mV (W=600 μm, L=5 μm). (b) I_d-V_d curves from V_g=V_{th} to V_g=V_{th}+2.5 V with a step of 0.5 V for the same device.

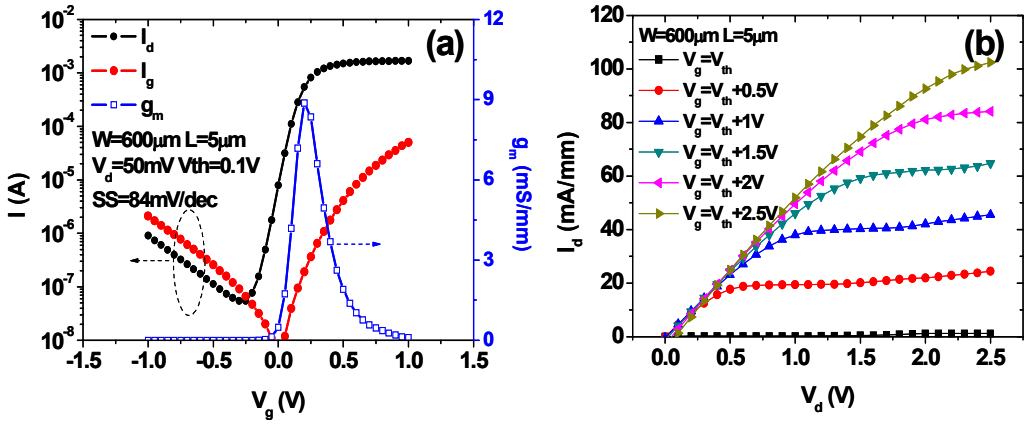

Figure 2.18 (a) Drive current I_d, gate leakage current I_g and extrinsic transconductance g_m as a function of V_g for MOSFETs with $LaAlO_3$ gate dielectric (EOT=1.3 nm) at V_d=50 mV (W=600 μm, L=5 μm). (b) I_d-V_d curve at various V_g value for the same device.

In summary, the performances for $In_{0.53}Ga_{0.47}As$ n-MOSFETs were compared among different ALD gate dielectrics including Al_2O_3, HfO_2, and $LaAlO_3$. HfO_2 shows the highest κ value and the smallest EOT while Al_2O_3 has the best interface quality with InGaAs. $LaAlO_3$ has higher κ value than Al_2O_3 and better interface quality than HfO_2, and it obtains subthreshold swing of 84 mV/dec with EOT of 1.3 nm. High drive current of 133.3 mA/mm and maximum extrinsic transconductance of 67.5 mS/mm were achieved using 4.5 nm HfO_2 gate dielectric (L=5 μm, EOT= 1 nm).

2.4 HfO_2-based $In_{0.53}Ga_{0.47}As$ MOSFETs (EOT≈10 Å) using various interfacial dielectric layers

To further improve the performance of ALD HfO_2 based InGaAs MOSFETs, stacked gate dielectrics with HfO_2 on the top and various interfacial dielectric layers at the bottom have been investigated. This work compares device performance for $In_{0.53}Ga_{0.47}As$ MOSFETs using single HfO_2 gate dielectric with stacked gate dielectrics using various interfacial layers between HfO_2 and $In_{0.53}Ga_{0.47}As$ substrate including

Al_2O_3, $HfAlO_x$, $LaAlO_x$, and $LaHfO_x$. Of the gate stacks studied, Al_2O_3/HfO_2, $HfAlO_x/HfO_2$, and $LaAlO_x/HfO_2$ bilayer gate dielectrics exhibit lower subthreshold swing, higher drive current and transconductance compared to single HfO_2 with similar equivalent oxide thickness (EOT) of about 10 Å. This is believed to be due to better interface quality between interfacial dielectrics and substrate, and confirmed by frequency dispersion and interface state density measurements.

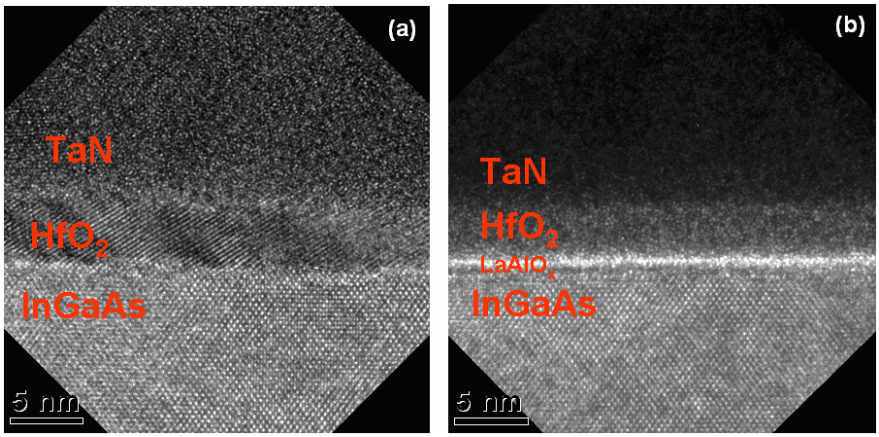

Figure 2.19 (a) Cross-section HR-TEM image for MOSFETs with 50 Å HfO_2 gate dielectric. (b) Cross-section HR-TEM image for MOSFETs with 10 Å $LaAlO_x$/ 35 Å HfO_2.

$In_{0.53}Ga_{0.47}As$ MOSFETs were fabricated on 200 nm undoped $In_{0.53}Ga_{0.47}As$ epitaxially grown on SI-InP substrate with ring-type structure by gate-last process. The surface oxides of InGaAs were removed with diluted HF cleaning. Then 100 Å Al_2O_3 (dummy capping layer) was deposited by ALD. After Si ion implantation at the source and drain region (35 keV, 2×10^{14} /cm^2), S/D activation annealing was performed at 700 ℃ for 10 sec. The Al_2O_3 capping layer was then removed using buffered oxides etch. Various gate stacks were then deposited by ALD including (a) 50 Å HfO_2, (b) 5 Å Al_2O_3/ 35 Å HfO_2, (c) 10 Å $HfAlO_x$/ 35 Å HfO_2, (d) 10 Å $LaAlO_x$/ 35 Å HfO_2, and (e) 10 Å

$LaHfO_x$/ 40 Å HfO_2. After post-deposition annealing (500 ℃ for 90 sec), TaN was deposited as gate electrode and AuGe/Ni/Au as source and drain ohmic contact. Figure 2.19(a) and figure 2.19(b) shows cross-section high-resolution TEM image at gate region for MOSFETs with 50 Å HfO_2 gate dielectric and 10 Å $LaAlO_x$/ 35 Å HfO_2 gate dielectric, respectively. The single HfO_2 gate dielectric becomes polycrystalline after PDA while the 10 Å $LaAlO_x$/ 35 Å HfO_2 bilayer gate stacks still keep amorphous.

Figure 2.20 illustrates EOT and gate leakage current density versus various bottom dielectric layers. All gate stacks show EOT of 10 Å to 12 Å. Al_2O_3/HfO_2, $HfAlO_x/HfO_2$, and $LaAlO_x/HfO_2$ exhibit more than two orders lower gate leakage current than single HfO_2 layer. Device characteristics including subthreshold swing, maximum extrinsic transconductance, threshold voltage and drive current density were measured and compared in figure 2.21 and figure 2.22. The gate width is 600 μm and gate length is 5 μm. As one can see, Al_2O_3/ HfO_2, $HfAlO_x$/ HfO_2, and $LaAlO_x$/ HfO_2 show much lower subthreshold swing and higher extrinsic transconductance and drive current density than single HfO_2. The improvement of device performance by adding Al might be related to self-cleaning effect when using Al precursor (TMA) in ALD [33], [66]. Among these three gate stacks, the last two show slightly better performance than Al_2O_3/HfO_2. This might be related to the thickness of Al_2O_3 interfacial layer, 5 Å Al_2O_3 might not be sufficient to passivate InGaAs substrate (5 Å Al_2O_3 was chosen to obtain similar EOT). $LaHfO_x$/ HfO_2 results in larger transconductance and drive current than single HfO_2 while the subthreshold swing remains approximately the same level. The enhanced current driving capability for $LaHfO_x$/ HfO_2 is believed to be due to the passivation of oxygen vacancy states in HfO_2 by La addition [77] and thereby reduce charge trapping in the high-κ dielectric layer.

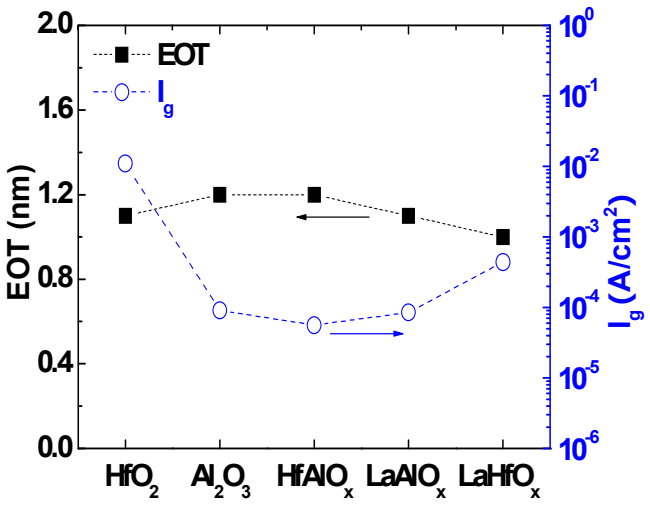

Figure 2.20 EOT and gate leakage current(I_g at V_g=1V) versus various bottom gate dielectrics.

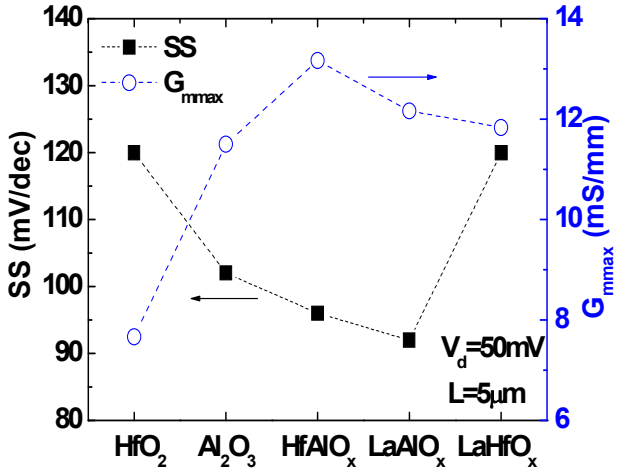

Figure 2.21 Subthreshold swing and maximum extrinsic transconductance versus various bottom gate dielectrics.

The I_d-V_g, I_g-V_g, G_m-V_g, and I_d-V_d characteristics of InGaAs MOSFETs with stacked $LaAlO_x/HfO_2$ gate dielectric were plotted in figure 2.23 to figure 2.25. High drive current density of 155 mA/mm at V_g-V_{th}=2 V (L=5 μm) and low subthreshold swing of 92 mV/dec were obtained. The maximum extrinsic transconductance is 12.3 mS/mm at

V_d=0.05 V and 76.5 mS/mm at V_d=0.5 V. To compare the interface quality of the stacked gate dielectrics with various interfacial layers, we measured the frequency dispersion between 1 MHz and 10 KHz and hysteresis at 1 MHz (V_g scan range: -1 V to 1 V) from split-CV (figure 2.26). Al_2O_3/ HfO_2, $HfAlO_x$/ HfO_2, and $LaAlO_x$/ HfO_2 exhibit smaller frequency dispersion and hysteresis than $LaHfO_x$/ HfO_2 and single HfO_2. This correlates well with the subthreshold swing characteristics (figure 2.21).

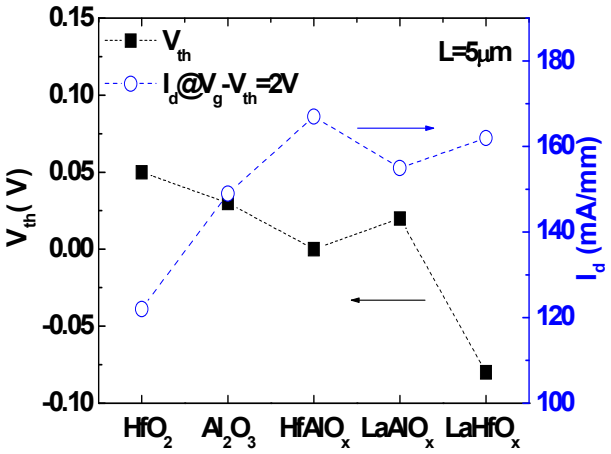

Figure 2.22 Threshold voltage and drive current versus various bottom gate dielectrics

Figure 2.27 shows frequency dispersion and hysteresis measured from split-CV for $LaAlO_x/HfO_2$, very small hysteresis of 49 mV was obtained. Interface trap density D_{it} was measured by conductance method on transistors and its distribution is shown in figure 2.28. $HfAlO_x$/ HfO_2 and $LaAlO_x$/ HfO_2 has minimum D_{it} of 1.8×10^{12} /cm^2 while single HfO_2 has 3.0×10^{12} /cm^2, the small difference on D_{it} might be related to limited measurement on D_{it} by room temperature conductance method [78].

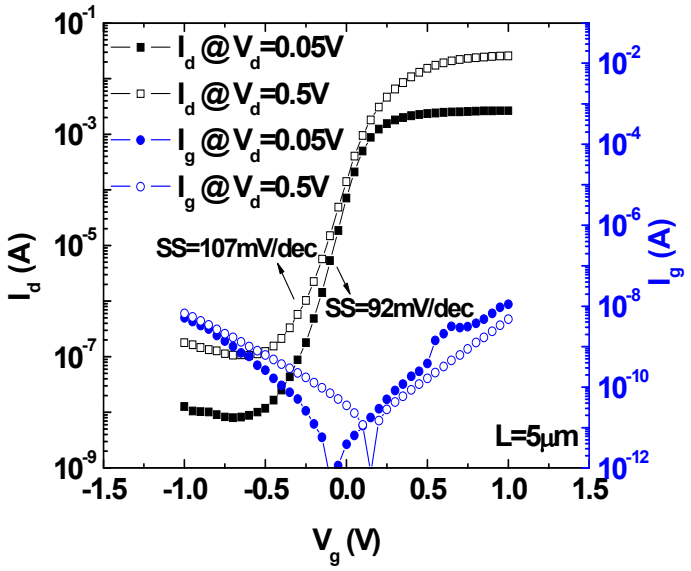

Figure 2.23 log-scale I_d-V_g and I_g-V_g at different V_d for MOSFETs with 10Å $LaAlO_x$/35Å HfO_2 gate dielectric.

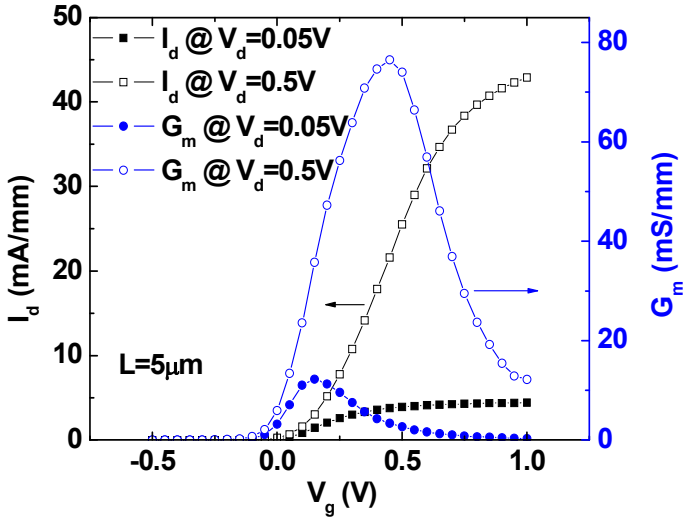

Figure 2.24 I_d-V_g and extrinsic transconductance G_m-V_g at different V_d for MOSFETs with 10 Å $LaAlO_x$/ 35 Å HfO_2 gate dielectric.

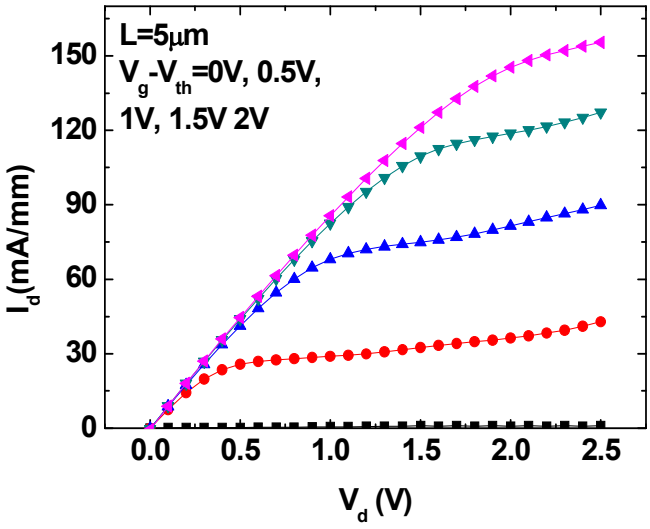

Figure 2.25 I_d-V_d at different V_g for MOSFETs with 10 Å $LaAlO_x$/ 35 Å HfO_2 gate dielectric.

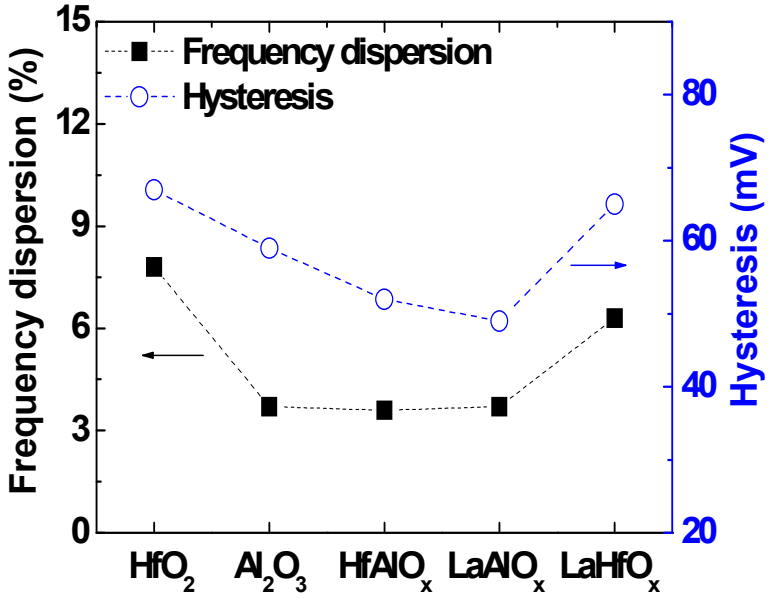

Figure 2.26 Frequency dispersion at V_g=1 V and hysteresis (V_g range: -1 V to 1 V) for different bottom gate dielectrics.

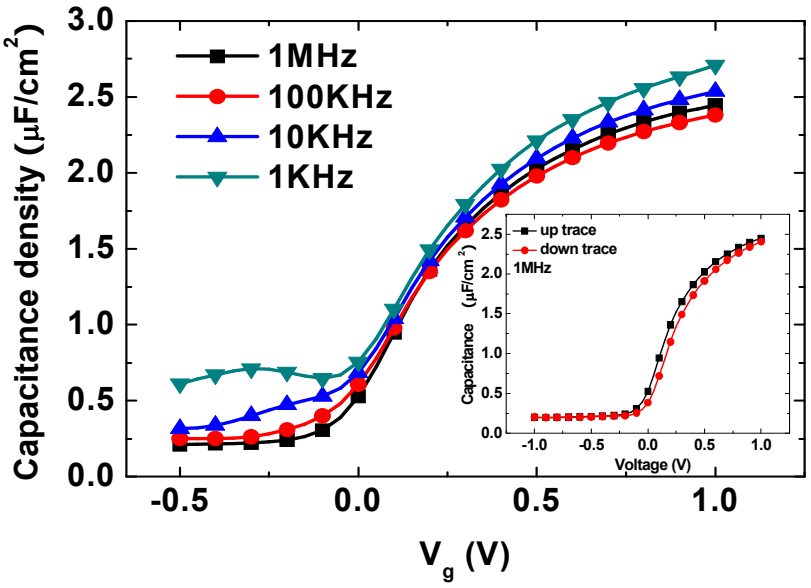

Figure 2.27 Frequency dispersion and hysteresis from split-CV for MOSFETs with 10 Å $LaAlO_x$/ 35 Å HfO_2 gate dielectric.

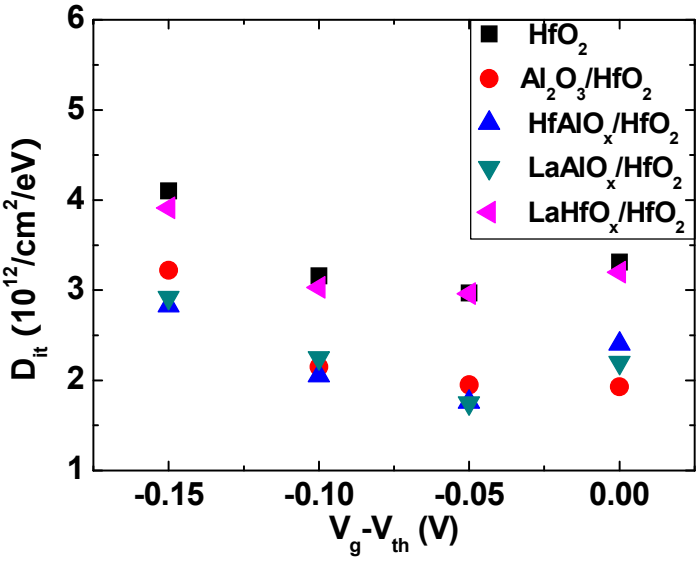

Figure 2.28 D_{it} distribution measured by conductance method on MOSFETs for various gate dielectrics.

Effective channel mobility of transistors with various gate dielectrics were measured by split-CV method and showed in figure 2.29. The maximum effective mobility of HfO_2, Al_2O_3/ HfO_2, $HfAlO_x$/ HfO_2, $LaAlO_x$/ HfO_2 and $LaHfO_x$/ HfO_2 are 787 cm^2/Vs, 1176 cm^2/Vs, 1385 cm^2/Vs, 1311 cm^2/Vs and 1034 cm^2/Vs, respectively. $HfAlO_x$/ HfO_2 and $LaAlO_x$/ HfO_2 stacked gate dielectrics achieve notable mobility enhancement than single HfO_2 layer.

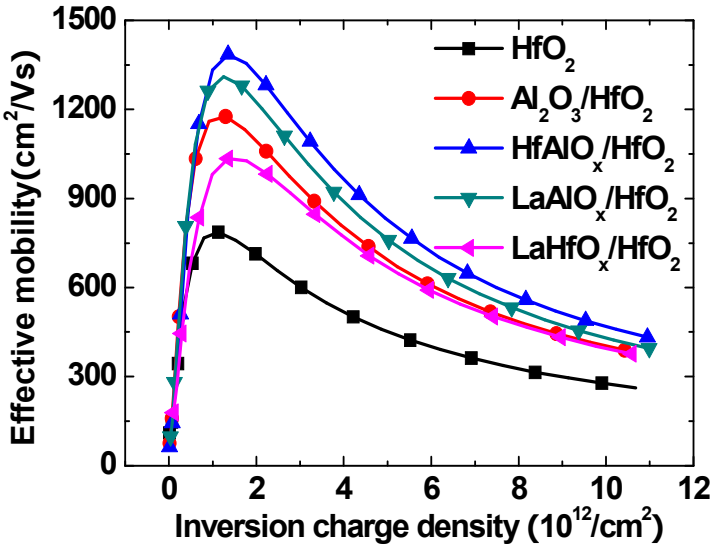

Figure 2.29 Effective mobility for different gate dielectrics.

In summary, $In_{0.53}Ga_{0.47}As$ MOSFETs using various gate dielectrics including single HfO_2, stacked Al_2O_3/HfO_2, $HfAlO_x/HfO_2$, $LaAlO_x/HfO_2$ and $LaHfO_x/HfO_2$ were fabricated and the performance was compared. Using 10 Å $HfAlO_x$ or $LaAlO_x$ as the interfacial layer between HfO_2 and InGaAs substrate reduces the interface trap density, thus achieves higher drive current, channel mobility and lower subthreshold swing than single HfO_2 layer. High drive current of 155 mA/mm, maximum mobility of 1311

cm^2/Vs and low subthreshold swing of 92 mV/dec were achieved by 10 Å $LaAlO_x$/ 35 Å HfO_2 gate stacks (EOT=11 Å, L=5 μm).

2.5 Summary

In this chapter, process engineering, substrate engineering, high-κ gate oxide engineering and interface engineering techniques have been investigated for improving the performance of surface channel InGaAs MOSFETs with ALD oxides.

It has been found that the gate-last process is more promising for surface-channel inversion-type III-V MOSFETs compared to the gate first process since InGaAs devices with gate-last process can maintain similar D_{it} as PDA-only samples, while the ones with gate-first process have much larger D_{it}. This is explained by that the gate-first process results in a larger amount of In-O, Ga-O and As-As bonds on InGaAs surface, while the gate-last process maintains the similar surface chemical bonding condition as the PDA-only process.

The impact of $In_{0.53}Ga_{0.47}As$ channel doping concentration and thickness on device performance has been studied. The undoped channel provides the highest drive current but relatively poor subthreshold swing from its depletion-mode device characteristics. With proper substrate doping concentration (5×10^{16} /cm^3), small subthreshold swing can be achieved by reducing the effect of junction leakage current on the subthreshold characteristics. Thinner InGaAs channel exhibits lower off-current density but also relatively low drive current.

Among different ALD gate dielectrics including Al_2O_3, HfO_2, and $LaAlO_3$, HfO_2 shows the highest κ value and the smallest EOT while Al_2O_3 has the best interface quality with InGaAs. $LaAlO_3$ has higher κ value than Al_2O_3 and better interface quality than HfO_2. Enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs with EOT of 10 Å using HfO_2

gate oxide have been demonstrated, which is amongst the thinnest EOT reported. $In_{0.53}Ga_{0.47}As$ MOSFETs with small SS of 84 mV/dec using $LaAlO_3$ gate oxide have also been fabricated.

It has also been found that inserting Al contained interfacial dielectrics between InGaAs channel and HfO_2 gate oxide can improve the device performance. By using $LaAlO_x/HfO_2$ bilayer stacked gate dielectrics, 67% transconductance enhancement and reduced subthreshold swing from 120 mV/dec to 92 mV/dec have been achieved.

In summary, various conditions for fabricating surface channel InGaAs MOSFETs have been investigated. The gate last process, proper channel doping concentration and thickness, and using Al contained ALD interfacial dielectrics between channel and HfO_2 gate oxide are suggested for fabricating surface channel InGaAs MOSFETs with high performance and low EOT.

Chapter 3 Buried channel InGaAs MOSFETs

3.1 High performance $In_{0.7}Ga_{0.3}As$ MOSFETs with mobility > 4400 cm^2/Vs using InP barrier layer

Even through surface channel InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and ZrO_2 dielectrics [21]-[23], molecular beam epitaxy (MBE) $Ga_2O_3(Gd_2O_3)$ dielectrics [69] and Si interfacial passivation layer (IPL) and high-κ gate stacks [29] show promising results on MOSFETs with high drive current capability, the reported effective channel mobility μ_{eff} of the surface channel devices still relatively low compared to the bulk mobility of InGaAs (e.g., $\mu_{eff} \sim 1000 - 1700$ cm^2/Vs [21], [23], [29], [69]). On the other hand, buried channel InGaAs MOSFETs with MBE InAlAs barrier layer and Si IPL [39] or flat-band InGaAs MOSFETs with GaAs/AlGaAs barrier layer and Si δ-doping using MBE GaGdO gate oxide [42] or MOS high-electron-mobility transistors (MOS-HEMTs) [44] can achieve much higher electron mobility [e.g., 3810 cm^2/Vs with Si IPL, 1280 cm^2/Vs without Si IPL [79], 5500 cm^2/Vs [25] and 4250 cm^2/Vs [44])].

The gate leakage current density of buried channel InGaAs MOSFETs or MOS-HEMTs can be several orders of magnitude lower than that of HEMTs [44], [46], [79]. Flat-band InGaAs MOSFETs and MOS-HEMTs devices in general require a Si δ-doped layer, a spacer layer and a barrier layer [25], [44], while buried channel MOSFETs only need a barrier layer [79]. Compared to MBE dielectrics, ex-situ ALD gate dielectrics are preferable due to their potential manufacturability. Furthermore, as a barrier layer, InAlAs usually has the problem of excessive aluminum oxidation for ex-situ process, while InP shows better interface quality with ex-situ ALD dielectrics than GaAs and InAlAs [80]-[81]. On the other hand, the conduction band offset between InP and InGaAs is smaller than that between InAlAs and InGaAs (0.26 eV for InP/$In_{0.53}Ga_{0.47}As$

compared to 0.47 eV for $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ [82]). In this paper, we have investigated and compared device performance for buried channel $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with InP barrier layer and surface channel $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs without InP barrier layer. High device performance including drive current of 98 mA/mm (L=20 μm), SS of 106 mV/dec and effective channel mobility of 4402 cm^2/Vs have been achieved for $In_{0.7}Ga_{0.3}As$ MOSFETs using 4 nm InP barrier layer and 5.5 nm ALD Al_2O_3 gate oxide.

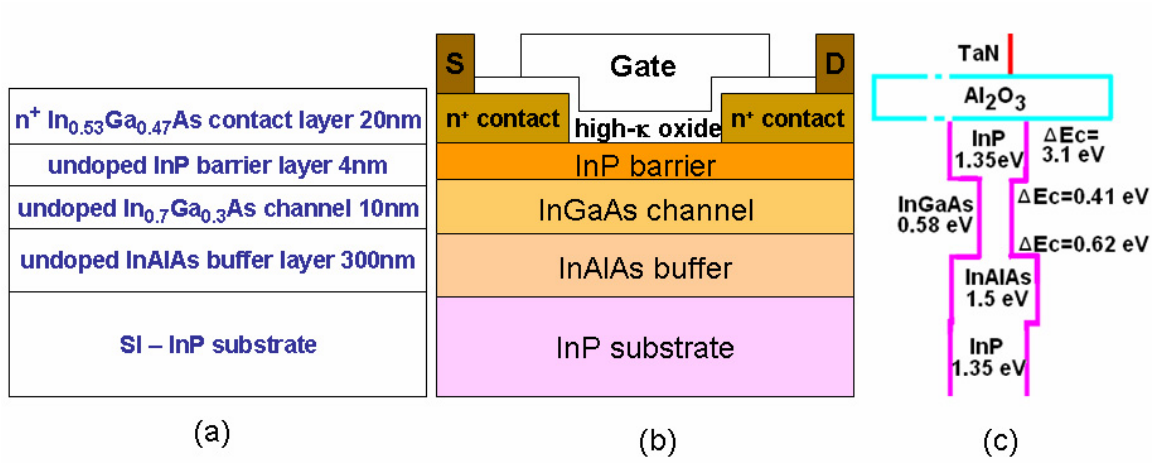

Figure 3.1 (a) Cross-section view of substrate structure for $In_{0.7}Ga_{0.3}As$ MOSFETs. (b) Cross-section view of $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with InP barrier layer. (c) Energy band diagram for $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier layer.

$In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs were fabricated on undoped InGaAs epitaxially grown on SI-InP substrate with a ring-type structure. Figure 3.1(a) shows the cross-section view of the substrate for $In_{0.7}Ga_{0.3}As$ MOSFETs. For $In_{0.7}Ga_{0.3}As$ MOSFETs, the InP barrier layer is 4 nm thick and $In_{0.7}Ga_{0.3}As$ channel layer is 10 nm thick, while for $In_{0.53}Ga_{0.47}As$ MOSFETs, the InP barrier layer is 6 nm thick and $In_{0.53}Ga_{0.47}As$ channel layer is 30 nm thick. The n^+ InGaAs contact layer at the channel region was selectively removed by citric acid based solution. For some samples, the InP

barrier layer was selectively etched by diluted hydrochloric acid. Gate oxide (5.5 nm Al_2O_3) was then deposited by ALD (EOT=3.4 nm). After that, TaN gate electrode was deposited by PVD and AuGe/Ni/Au source and drain ohmic contact was deposited by E-beam evaporation. Figure 3.1(b) shows the cross-section view of the InGaAs MOSFETs with InP barrier layer. Figure 3.1(c) shows the energy band diagram for $In_{0.7}Ga_{0.3}As$ device with InP barrier layer.

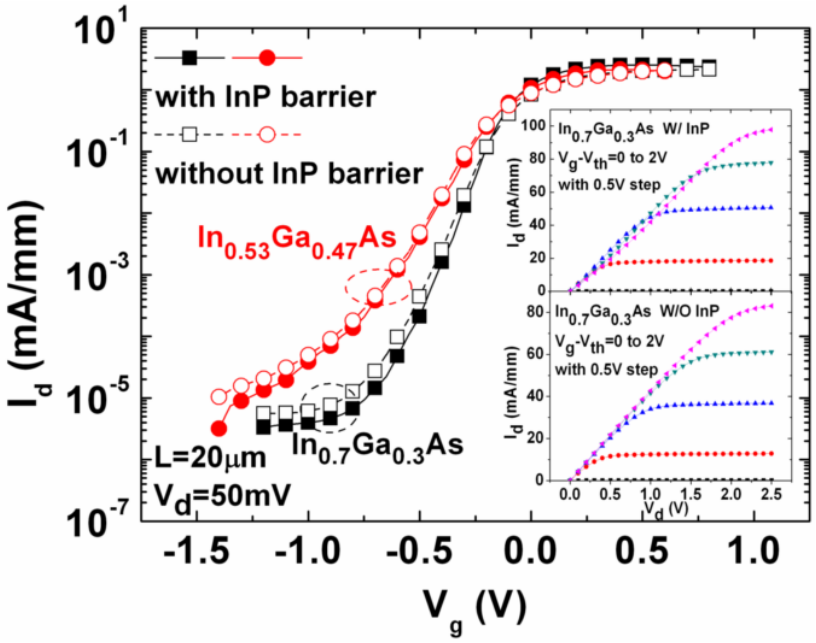

Figure 3.2 Log-scale I_d-V_g at V_d=50 mV for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer. Inset shows I_d-V_d at V_g-V_{th} from 0 V to 2 V with 0.5 V step for $In_{0.7}Ga_{0.3}As$ MOSFETs with and without InP barrier layer. The gate length is 20 μm.

Figure 3.2 illustrates the log-scale I_d-V_g characteristics of $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer. The gate leakage current density is less than 4×10^{-9}A/cm^2 at V_g-V_{th}=1V for all samples (data not shown). Compared to $In_{0.53}Ga_{0.47}As$ MOSFETs, $In_{0.7}Ga_{0.3}As$ MOSFETs show much lower subthreshold swing [106mV/dec versus 154mV/dec (figure 3.3)]. In addition to the

shorter gate-to-channel distance due to thinner InP barrier layer for $In_{0.7}Ga_{0.3}As$ MOSFETs, the thinner $In_{0.7}Ga_{0.3}As$ channel layer which is easier to be depleted by gate bias is another important reason for the lower subthreshold swing. Although InP barrier layer increases gate-to-channel distance compared to MOSFETs without InP layer, subthreshold swing for $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier layer is actually decreased. There are two interfaces from oxide to channel in $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier [Al_2O_3/InP interface and InP/$In_{0.7}Ga_{0.3}As$ interface (see figure 3.1)] compared to $In_{0.7}Ga_{0.3}As$ MOSFETs without InP barrier which has only one oxide to channel interface (Al_2O_3/$In_{0.7}Ga_{0.3}As$). Although in $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier, the ALD Al_2O_3/InP interface quality may not be as good as ALD Al_2O_3/InGaAs interface [83], the MBE grown InP/InGaAs interface is closer to channel, and we believe its excellent interface quality plays a more important role for the enhanced device characteristics. Therefore the improved subthreshold swing is believed to be due to the better MBE grown InP/InGaAs interface than ALD Al_2O_3/InGaAs interface. Figure 3.2 inset shows I_d-V_d curves at V_g-V_{th} from 0 V to 2 V with 0.5 V step for $In_{0.7}Ga_{0.3}As$ MOSFETs with and without InP barrier layer. For $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier at high V_g (1.5 V – 2 V), some channel electrons spill over into the lower-mobility InP layer. This results in the cross-over characteristics of the I_d-V_d curves. Note that the $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier layer exhibit high drive current of 98 mA/mm for gate length L=20 μm.

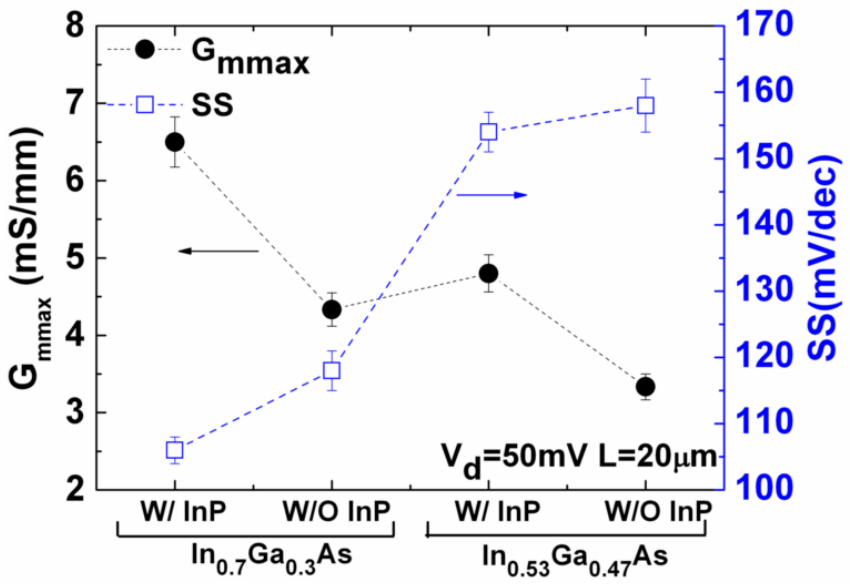

Figure 3.3 Maximum transconductance and subthreshold swing at V_d=50 mV for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer. The gate length is 20 μm.

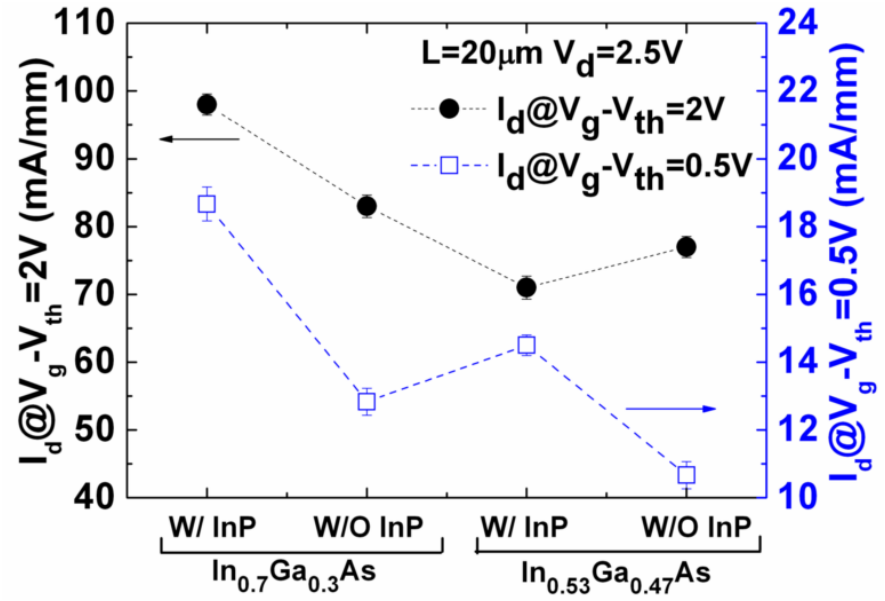

Figure 3.4 Drive current I_d at V_g-V_{th}=0.5 V and 2 V for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer. The gate length is 20 μm and V_d is 2.5 V.

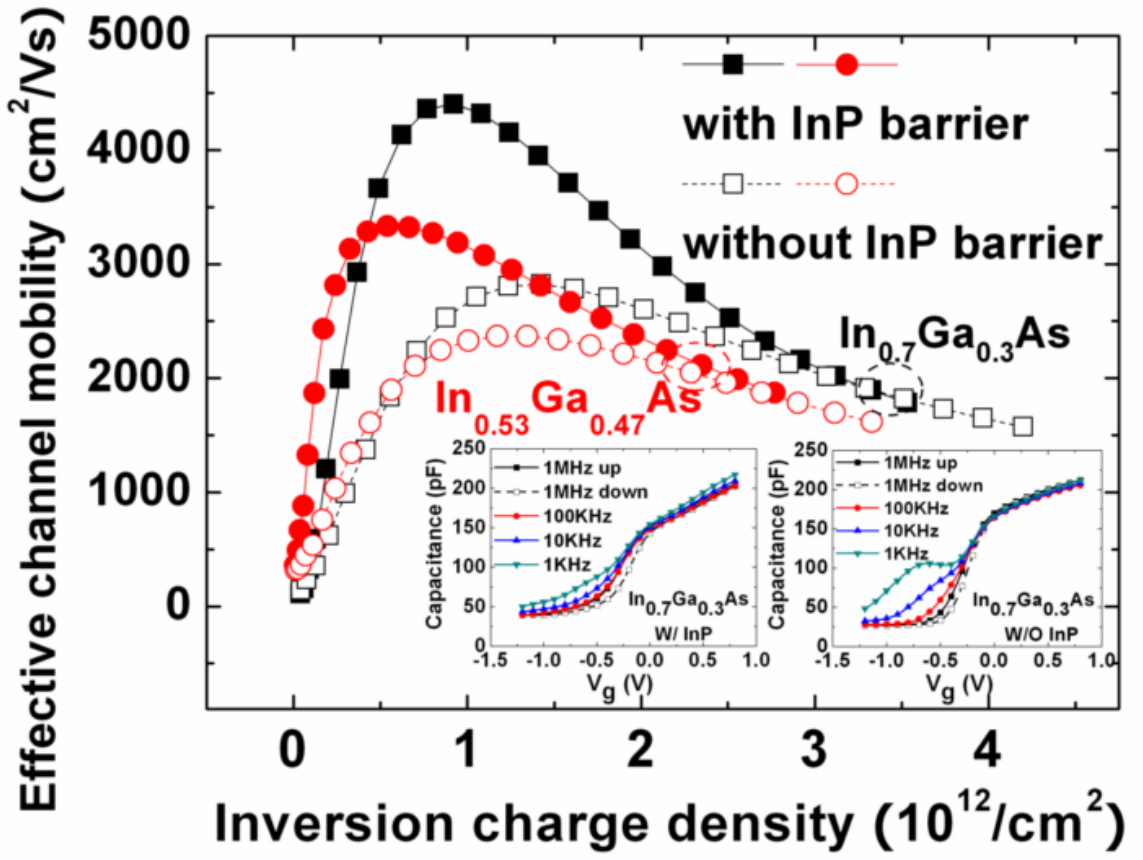

Figure 3.5 Effective channel mobility versus inversion charge density for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer. Inset shows split-CV frequency dispersion from 1MHz to 1KHz and hysteresis at 1MHz (up trace: V_g start from -1V, down trace: V_g starts from 1V) for $In_{0.7}Ga_{0.3}As$ MOSFETs with and without InP barrier layer.

Figure 3.3 and figure 3.4 compare the device performance of $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer including maximum extrinsic transconductance G_{mmax}, subthreshold swing, and drive current at different gate voltages. InP barrier provides MOSFETs with higher transconductance due to better InP/InGaAs interface close to the channel. $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier layer show much higher transconductance and much lower subthreshold swing than all other devices. This is believed to be due to higher mobility channel material and better gate-to-channel control. In figure 3.4, for V_g-V_{th}=0.5 V, $In_{0.53}Ga_{0.47}As$ MOSFETs with InP layer show

higher drive current than MOSFETs without InP layer. However, at V_g-V_{th}=2 V, the drive current for $In_{0.53}Ga_{0.47}As$ MOSFETs with InP barrier is smaller than those of $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs without InP layer. This is again because some channel electrons enter the lower-mobility InP layer. For $In_{0.7}Ga_{0.3}As$ MOSFETs with larger conduction band offset between InP and $In_{0.7}Ga_{0.3}As$ (0.41 eV versus 0.26 eV for InP/$In_{0.53}Ga_{0.47}As$), less electrons can enter InP layer at high V_g. Consequently, $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier layer show 46% and 18% enhancement in drive current than those without InP layer at V_g-V_{th}=0.5 V and 2 V, respectively. For $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier, the subthreshold swing is 106 mV/dec compared to 118 mV/dec for $In_{0.7}Ga_{0.3}As$ without InP barrier. The maximum transconductance is 50% higher (figure 3.3). These results illustrate InP is an excellent barrier layer to enhance device performance, especially for $In_{0.7}Ga_{0.3}As$ MOSFETs.

We have measured the effective channel mobility of $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer using split-CV method and plotted it in figure 3.5. The peak effective channel mobility for $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier is 4402 cm^2/Vs, which is much higher than $In_{0.7}Ga_{0.3}As$ with InAlAs barrier [e.g., 1280 cm^2/Vs without Si IPL [79]. Inset shows split-CV frequency dispersion and hysteresis for $In_{0.7}Ga_{0.3}As$ MOSFETs with and without InP barrier layer. They exhibit a small frequency dispersion and hysteresis.

In summary, we have fabricated $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs with and without InP barrier layer and compared their device performance. InP is an excellent barrier and passivation layer to enhance device current driving capability, especially for $In_{0.7}Ga_{0.3}As$ MOSFETs due to good conduction band offset. $In_{0.7}Ga_{0.3}As$ MOSFETs with InP barrier layer show much higher transconductance and lower subthreshold swing than

other MOSFETs, and exhibit high drive current of 98 mA/mm (L=20 μm), subthreshold swing of 106 mV/dec and effective channel mobility of 4402 cm^2/Vs.

3.2 Effects of barrier layers on device performance of high mobility $In_{0.7}Ga_{0.3}As$ MOSFETs

Due to the electron spill-over effect, improvement of electron mobility at high-field of buried-channel devices with InP barrier degrades as shown in the last section. In this section, double-barrier (InP/InAlAs) structures were used to significantly improve peak mobility as well as high-field mobility. Single InP barrier with different thicknesses and no barrier MOSFETs have also been studied for comparison. MOSFETs with InP/InAlAs barrier achieve high μ_{eff} of 4889 cm^2/Vs using Al_2O_3 gate oxide and 3722 cm^2/Vs using HfO_2 gate oxide, which is amongst the highest μ_{eff} reported.

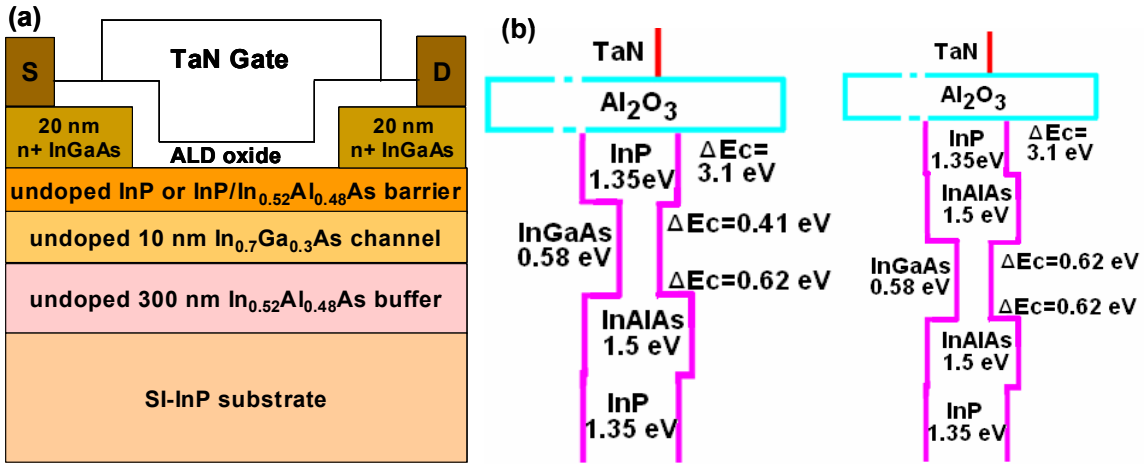

Figure 3.6 (a) Cross-sectional view and (b) band diagram of buried channel $In_{0.7}Ga_{0.3}As$ MOSFETs with single InP barrier (3nm or 5nm) or 2nm InP (top) /3nm $In_{0.52}Al_{0.48}As$ (bottom) double-barrier. InAlAs/$In_{0.7}GaAs$ shows larger ΔEc (0.62eV) than InP/$In_{0.7}GaAs$ (0.41eV).

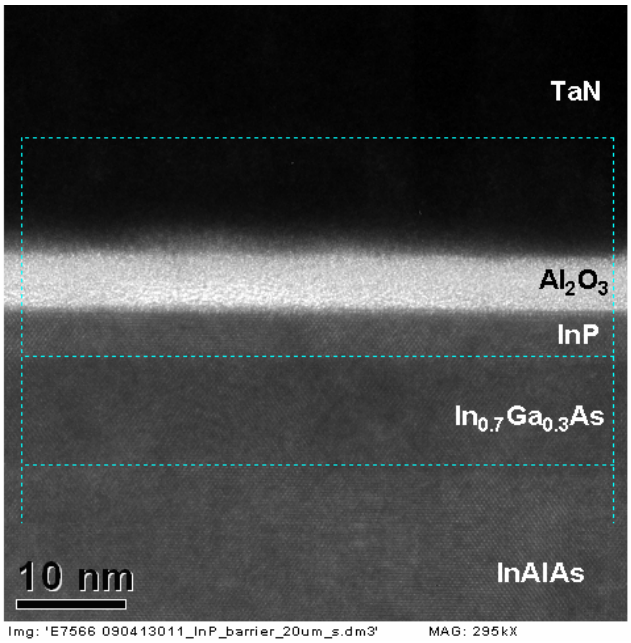

Figure 3.7 Cross-sectional high-resolution TEM for $In_{0.7}Ga_{0.3}As$ MOSFETs with 5 nm InP barrier. Sharp Al_2O_3/InP interface was observed.

Ring-type $In_{0.7}Ga_{0.3}As$ MOSFETs were fabricated on 10 nm undoped $In_{0.7}Ga_{0.3}As$ channel. Various MBE barrier layers were applied including undoped 3 nm InP, 5 nm InP and InP/InAlAs double-barrier with 2 nm InP on the top and 3 nm $In_{0.52}Al_{0.48}As$ at the bottom (figure 3.6). Various gate oxides were deposited by ALD including 4 - 8 nm Al_2O_3 (EOT: 2 nm to 4.1 nm), 5 nm HfO_2 (EOT=1.2 nm) and 1 nm Al_2O_3 (bottom) /4 nm HfO_2 (top) (EOT=1.4 nm). Sharp interface between InP barrier and Al_2O_3 is observed by TEM (figure 3.7).

In previous experiments, by comparing the performance of MOSFETs with InP barrier to those without any barrier layer using Al_2O_3 as gate oxide. MOSFETs with InP barrier achieve 56% peak effective mobility enhancement and 50% maximum extrinsic transconductance increase. They also show smaller subthreshold swing than without barrier, indicating better gate-to-channel control resulted from excellent MBE InP/$In_{0.7}Ga_{0.3}As$ interface than oxide/$In_{0.7}Ga_{0.3}As$ interface. However, effective mobility

at high inversion charge density (Q_{inv}) is similar for MOSFETs with and without InP barrier. This is because electrons spill over into the lower-mobility InP layer at high electric field for MOSFETs with InP barrier. The spill-over effect also causes the cross-over characteristics of I_d-V_d curves (figure 3.2 inset).

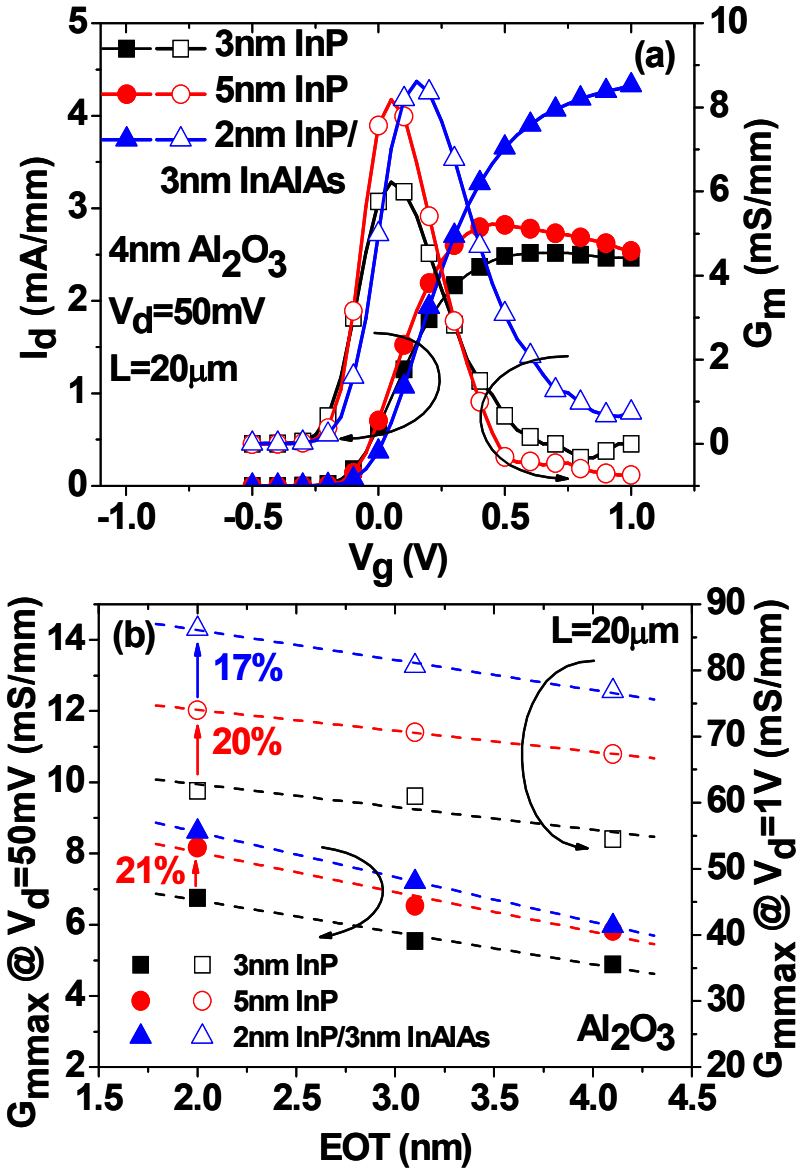

Figure 3.8 (a) MOSFETs with InP/InAlAs show much higher I_d and G_m at high V_g than InP. (b) Devices with 5 nm InP show 20% higher G_{mmax} than with 3 nm InP, MOSFETs with InP/InAlAs show 17% higher G_{mmax} than with 5 nm InP using Al_2O_3 (V_d=1 V).

Using $In_{0.52}Al_{0.48}As$ barrier with higher conduction band offset to $In_{0.7}Ga_{0.3}As$ than InP can suppress the electron spilling over effect and improve high-field mobility (figure 3.6(b)). However, InAlAs is easy to be oxidized, thus InP/InAlAs double-barrier with 2 nm InP on the top and 3 nm $In_{0.52}Al_{0.48}As$ at the bottom was used to protect InAlAs from oxidation. Figure 3.8 illustrates I_d-V_g and extrinsic G_m-V_g characteristics for MOSFETs with 3 nm InP, 5 nm InP and 2 nm InP/3 nm InAlAs barriers using Al_2O_3 gate oxide. The gate leakage current for MOSFETs with barriers and 4 nm Al_2O_3 (EOT=2 nm) is less than 1×10^{-4} A/cm^2 (data not shown). Devices with 5 nm InP show 20% maximum transconductance (G_{mmax}) increase than 3 nm InP barrier due to better passivation from oxide/III-V interface by a using thicker barrier layer. Although MOSFETs using InP/InAlAs barrier only show slightly larger G_{mmax} than 5 nm InP at V_d=50 mV, the better channel electron confinement using InP/InAlAs barrier results in 17% increase of G_{mmax} at V_d=1 V (EOT of 2 nm in figure 3.8(b)) and absence of I_d-V_d cross-over (figure 3.9(b)). Double-barrier MOSFETs also show 39% I_d increase at $V_g=V_{th}+2$ V than single 5 nm InP barrier MOSFETs (figure 3.9).

MOSFETs with InP/InAlAs barrier show larger subthreshold swing than those with single InP barrier (figure 3.10). This might be because 2 nm InP is still not sufficient to passivate InAlAs layer, and there is small amount of InAlAs oxidation, which generates donor-like defects in InAlAs layer. This does not affect I_{on} characteristics but will degrade SS [84]. Small SS of ~95 mV/dec was achieved by MOSFETs using single InP barrier and Al_2O_3 with 2 nm EOT.

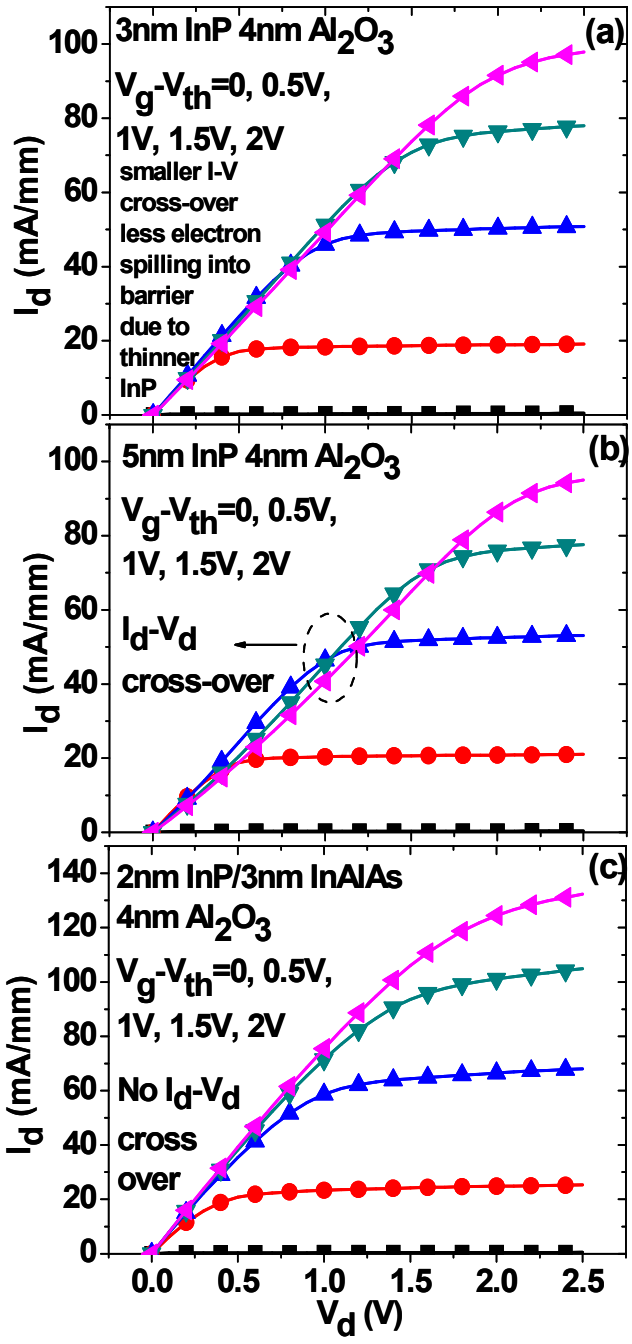

Figure 3.9 No I_d-V_d cross-over and 39% I_d increase (V_g=V_{th}+2 V) was obtained for MOSFETs with InP/InAlAs barrier (c) compared to with 5 nm InP barrier (b).

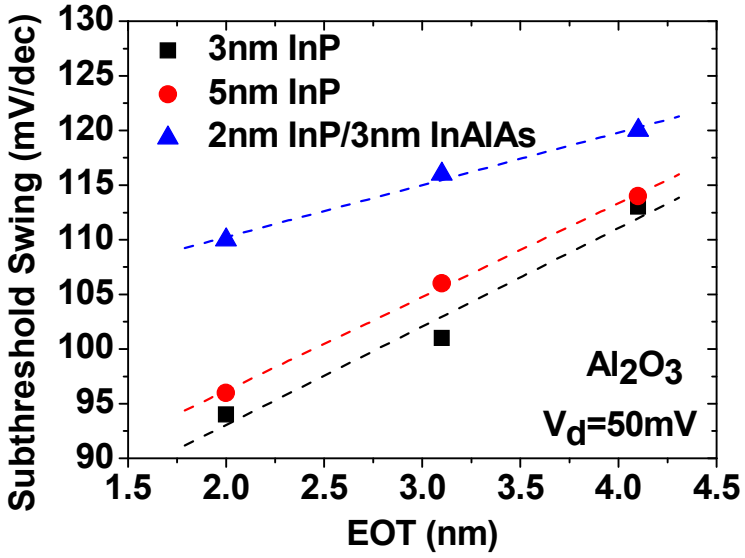

Figure 3.10 Small SS of ~95 mV/dec was achieved by MOSFETs with 3 nm or 5 nm InP barrier and Al_2O_3 with 2 nm EOT

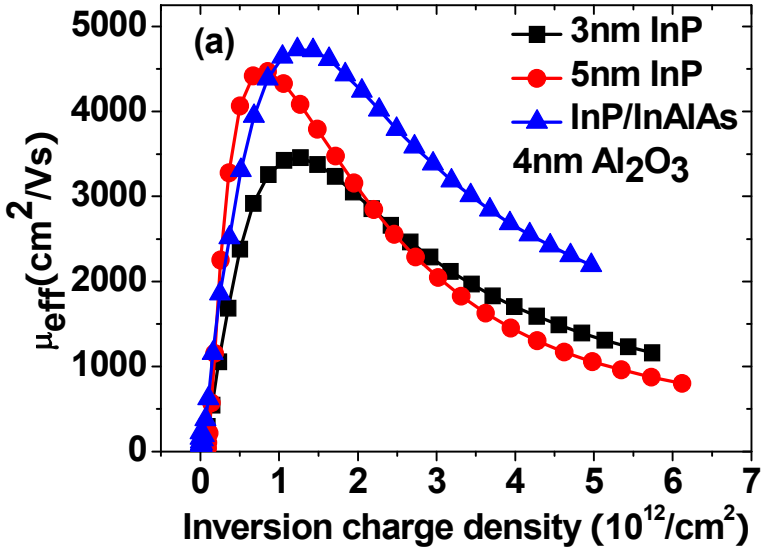

Figure 3.11 Thicker InP improves peak μ_{eff} and InP/InAlAs increases high field μ_{eff} significantly.

Devices with 3 nm InP and 5 nm InP achieve 23% and 56% peak mobility enhancement compared to no barrier, while MOSFETs with InP/InAlAs double-barrier gain both 68% peak mobility enhancement and 55% high field mobility ($Q_{inv}=4\times10^{12}$ /cm^2) enhancement compared to devices with no barrier (figure 3.11 and figure 3.12).

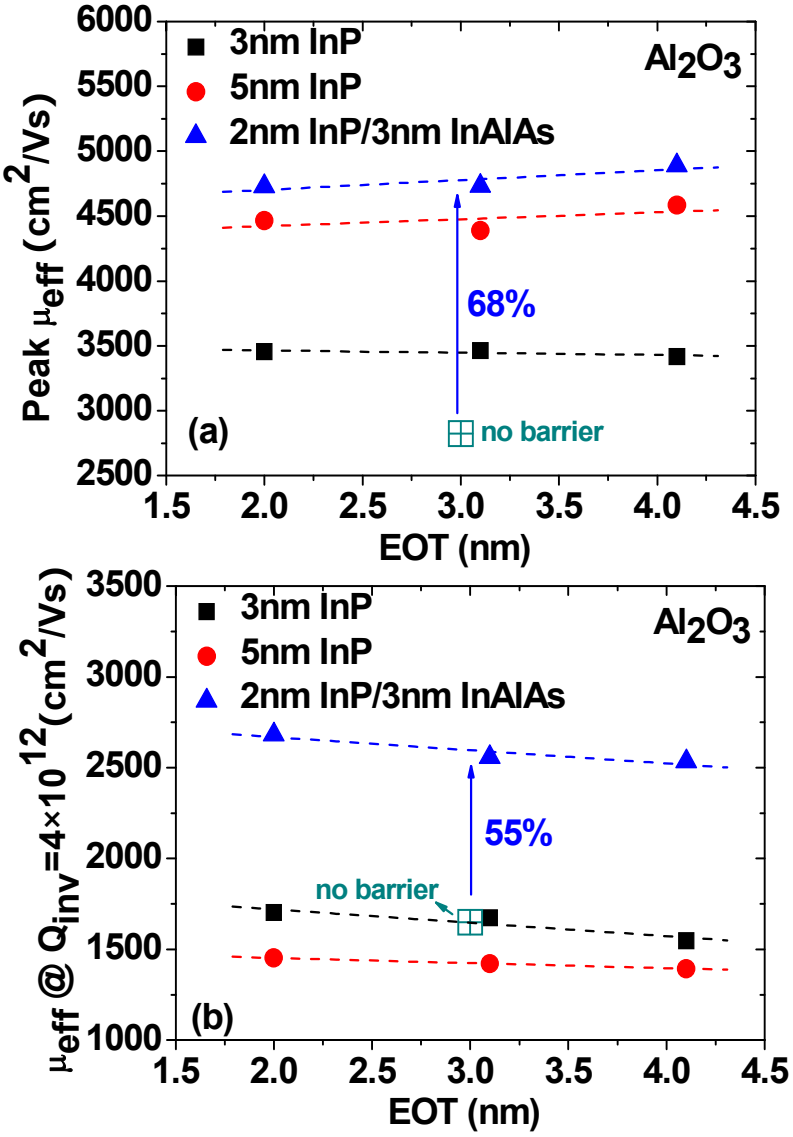

Figure 3.12 MOSFETs using Al_2O_3 with InP/InAlAs barrier show 68% higher peak μ_{eff} (a) and 55% higher high-field μ_{eff} (b) than without barrier. Single InP barrier only improve peak μ_{eff} but not high-field μ_{eff}.

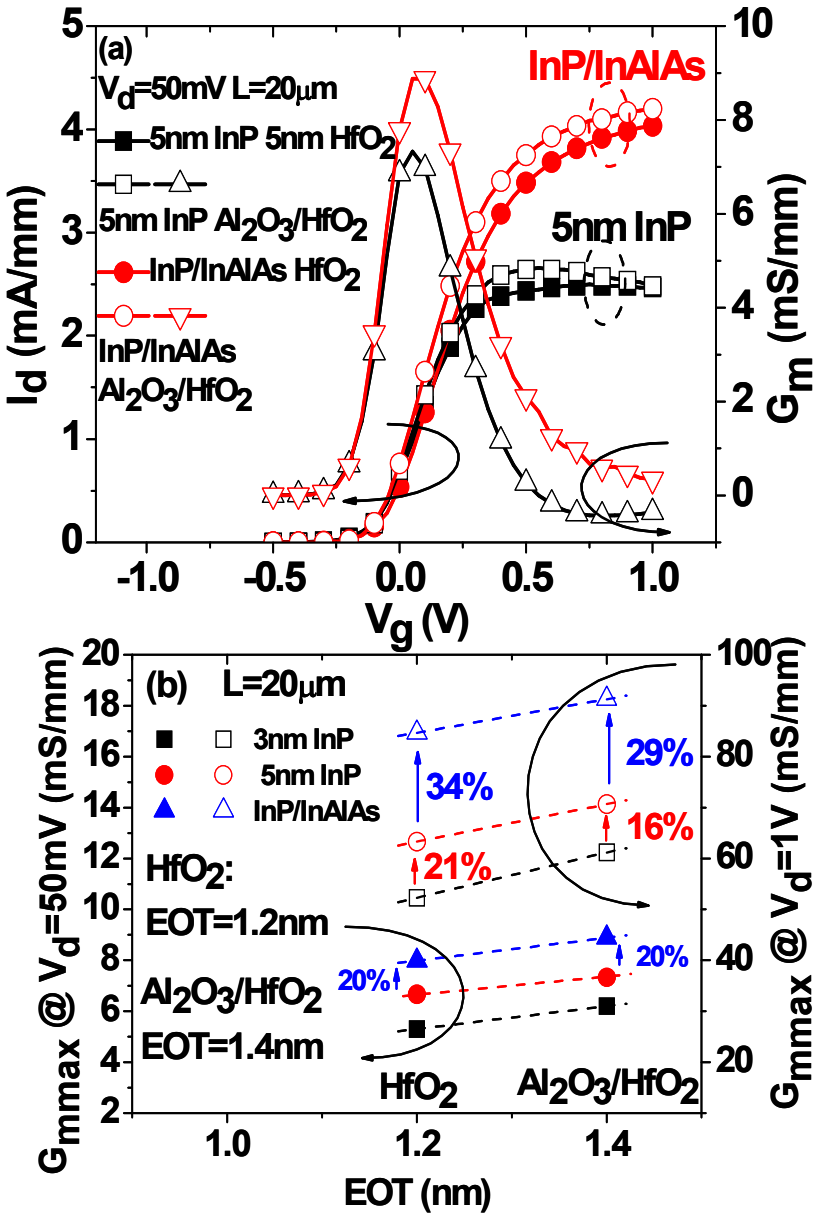

Figure 3.13 MOSFETs using HfO_2 show both 20% G_{mmax} increase at V_d=50 mV and 34% G_{mmax} increase at V_d=1 V with InP/InAlAs compared to with 5 nm InP. Al_2O_3(bottom)/ HfO_2(top) bilayer improves G_m and I_d compared to single HfO_2.

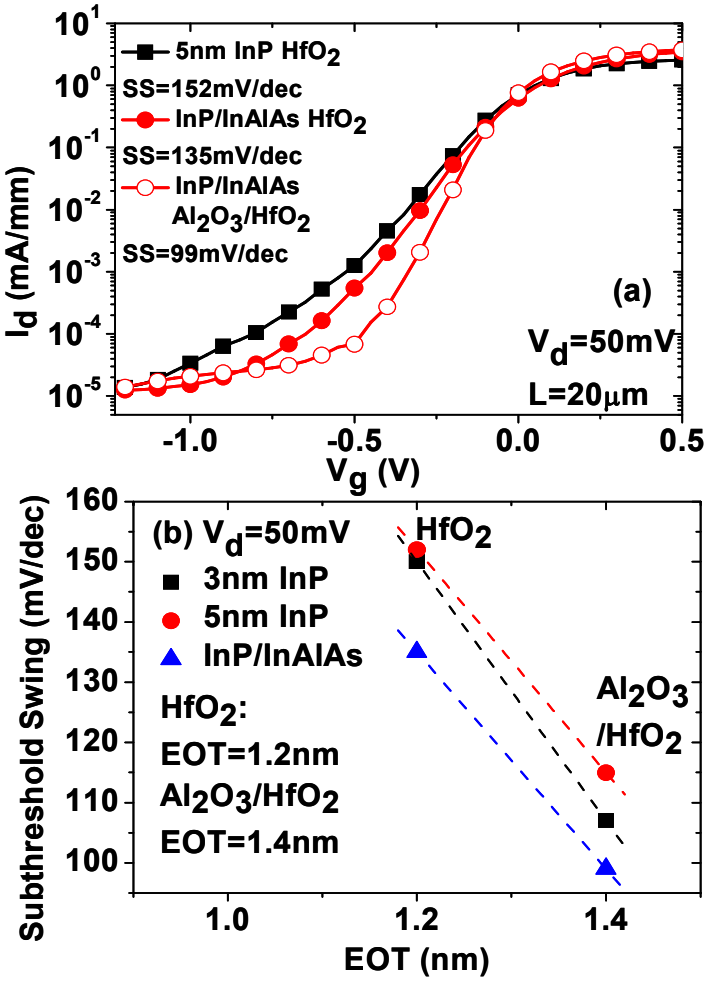

Figure 3.14 Devices using HfO_2 show smaller SS with InP/InAlAs barrier than with 5 nm InP. MOSFETs with Al_2O_3/HfO_2 bilayer achieve smaller SS than single HfO_2. Small SS of 99 mV/dec was obtained by devices with InP/InAlAs barrier and Al_2O_3/HfO_2 oxide.

To further scale down EOT, 5nm HfO_2 (EOT=1.2 nm) was applied to devices with InP and InP/InAlAs barriers. The gate leakage current for MOSFETs with barriers and 5nm HfO_2 is less than 8×10^{-5} A/cm^2 (data not shown). MOSFETs using HfO_2 with InP/InAlAs barrier show significant high-field I_d and μ_{eff} improvement (figure 3.13 to figure 3.16), as well as lower SS (135 mV/dec versus 152 mV/dec in figure 3.14) and 16% peak mobility enhancement (figure 3.16(a)) compared to those with 5 nm InP

barrier. HfO_2/InP interface shows about one order of magnitude higher D_{it} than Al_2O_3/InP interface (figure 3.17 and figure 3.18), Thus it is even more critical to reduce scattering from HfO_2/InP interface to channel electrons. The good channel electron confinement by using InP/InAlAs barrier keeps electrons far from HfO_2/InP; therefore it improves both low-field (peak μ_{eff}) and high-field characteristics compared to single InP barrier. MOSFETs with HfO_2 (EOT=1.2nm) show smaller G_m and higher SS than Al_2O_3 (EOT=2 nm) due to higher D_{it} at HfO_2/InP interface than Al_2O_3/InP interface (figure 3.17). Using Al_2O_3 (bottom) /HfO_2 (top) bilayer oxides helps to optimize oxide/InP interface thus improves G_m (figure 3.13), SS (figure 3.14), I_d (10% increase in figure 3.15) and μ_{eff} (17% increase in figure 3.16) even with slightly thicker EOT compared to single HfO_2 dielectric.

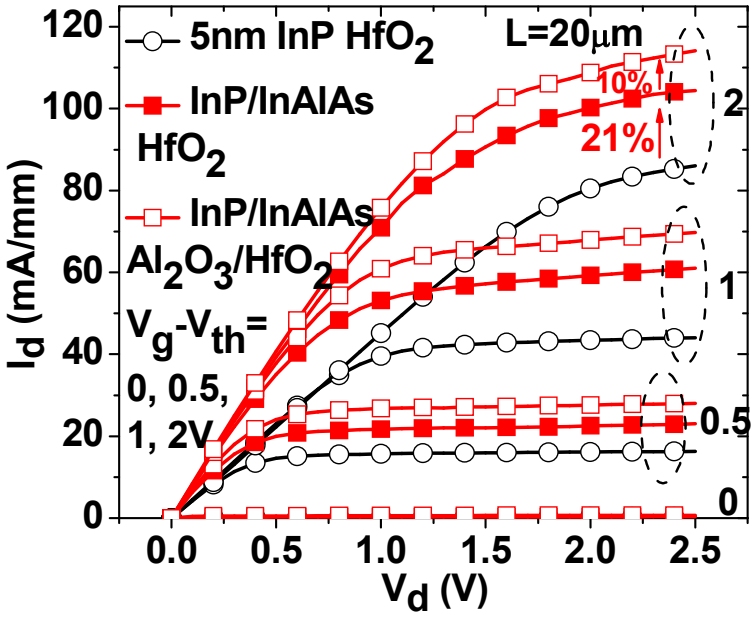

Figure 3.15 MOSFETs using HfO_2 show 21% I_d increase (V_g=V_{th}+2 V) with InP/ InAlAs barrier than with 5 nm InP barrier. MOSFETs with InP/ InAlAs barrier show 10% I_d increase using Al_2O_3/ HfO_2 oxide than HfO_2.

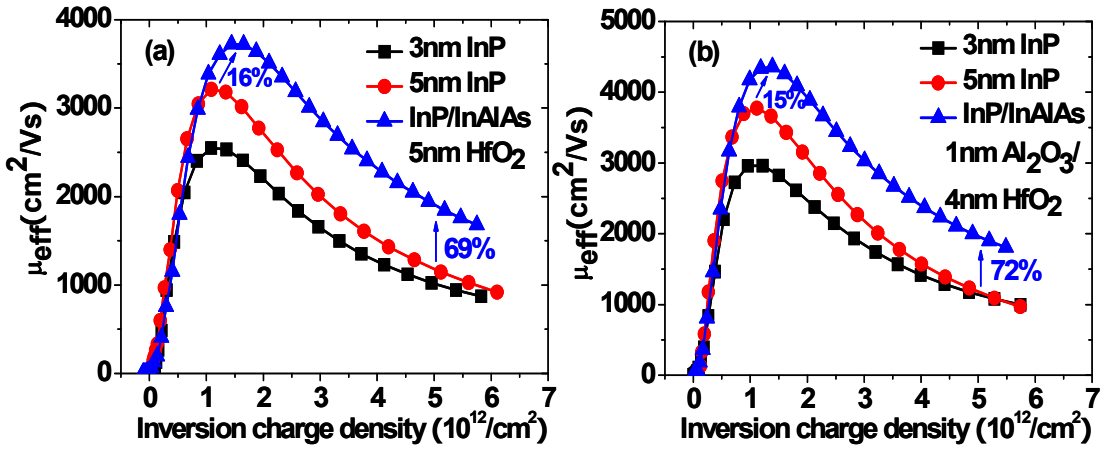

Figure 3.16(a) MOSFETs using HfO_2 show 16% higher peak μ_{eff} and 69% higher high-field μ_{eff} ($Q_{inv}=5\times10^{12}$ /cm^2) with InP/InAlAs barrier than with 5 nm InP barrier. (b) MOSFETs using Al_2O_3/ HfO_2 show 15% higher peak μ_{eff} and 72% higher high-field μ_{eff} with InP/ InAlAs barrier than with 5 nm InP barrier. MOSFETs with InP/ InAlAs barrier show 17% higher peak μ_{eff} using Al_2O_3/HfO_2 than using HfO_2.

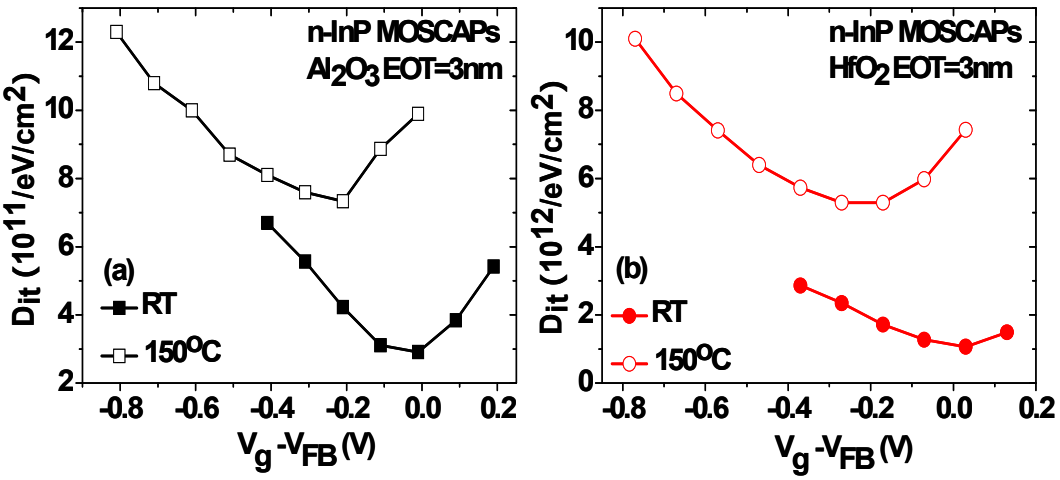

Figure 3.17 D_{it} for n-InP MOSCAPs with (a) Al_2O_3 or (b) HfO_2 gate dielectrics (same 3nm EOT) at RT and 150 ℃. 150 ℃ helps to detect D_{it} closer to mid-gap and results indicate larger D_{it} at mid-gap than closer to conduction band. MOSCAPs with HfO_2 show about one order of magnitude higher D_{it} than with Al_2O_3.

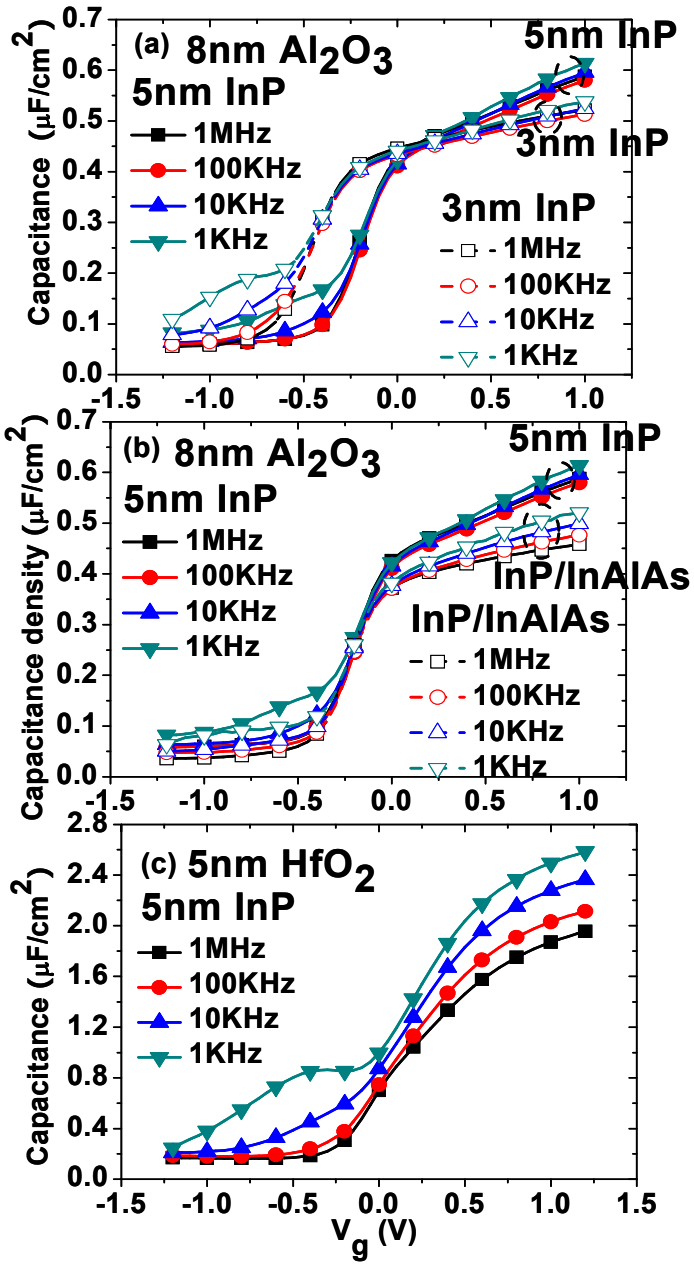

Figure 3.18 Frequency dispersion from split-CV for MOSFETs with (a) 3 nm or 5 nm InP barrier and 8 nm Al_2O_3 oxides (b) 5 nm InP barrier or InP/InAlAs barrier and 8 nm Al_2O_3 oxides (c) 5 nm InP barrier and 5 nm HfO_2 oxide. Smaller capacitance at V_g=1 V (thicker T_{inv}) for MOSFETs with 3 nm InP indicates reduced electrons spilling-over into barrier than 5 nm InP (a). Similarly, thicker T_{inv} for MOSFETs with 2 nm InP/ 3 nm InAlAs barrier than 5 nm InP shows less electrons spilling-over into barrier (b). Larger frequency dispersion for HfO_2 indicates higher D_{it} at HfO_2/InP interface than Al_2O_3 (c).

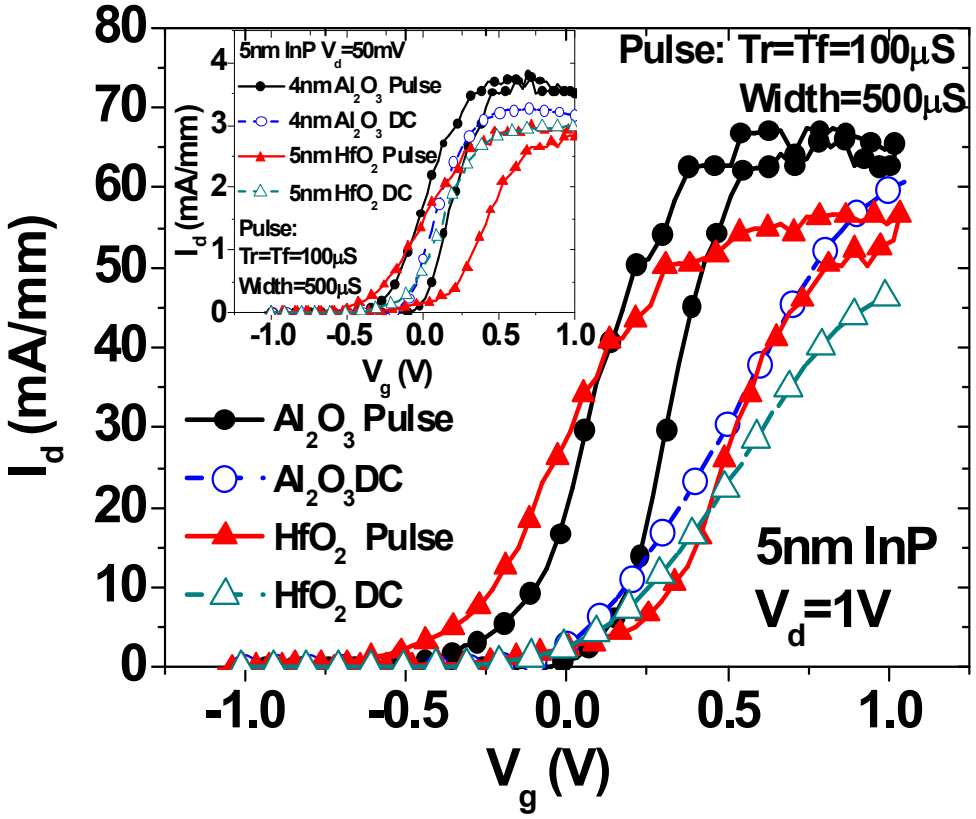

Figure 3.19 DC and pulse I_d-V_g at V_d=1 V using 5 nm InP barrier and 4 nm Al_2O_3 or 5 nm HfO_2 oxides (L=20 μm). Inset shows DC and pulse I_d-V_g at V_d=50 mV. Pulse setting: T_{rising}=$T_{falling}$=100 μS, Width=500 μS.

Figure 3.19 shows DC and pulse I_d-V_g for MOSFETs with 5 nm InP barrier and 4nm Al_2O_3 or 5 nm HfO_2. More than 2 times higher G_{mmax} was obtained using pulse I_d-V_g than DC measurement at V_d=1V, indicating transient charging effect in the gate stacks. Figure 3.20 illustrates V_{th} shift and G_{mmax} degradation after electrical stress of 7 MV/cm for MOSFETs with 3 nm or 5 nm InP barrier and various oxides. HfO_2 shows less V_{th} shift and G_{mmax} reduction than other oxides.

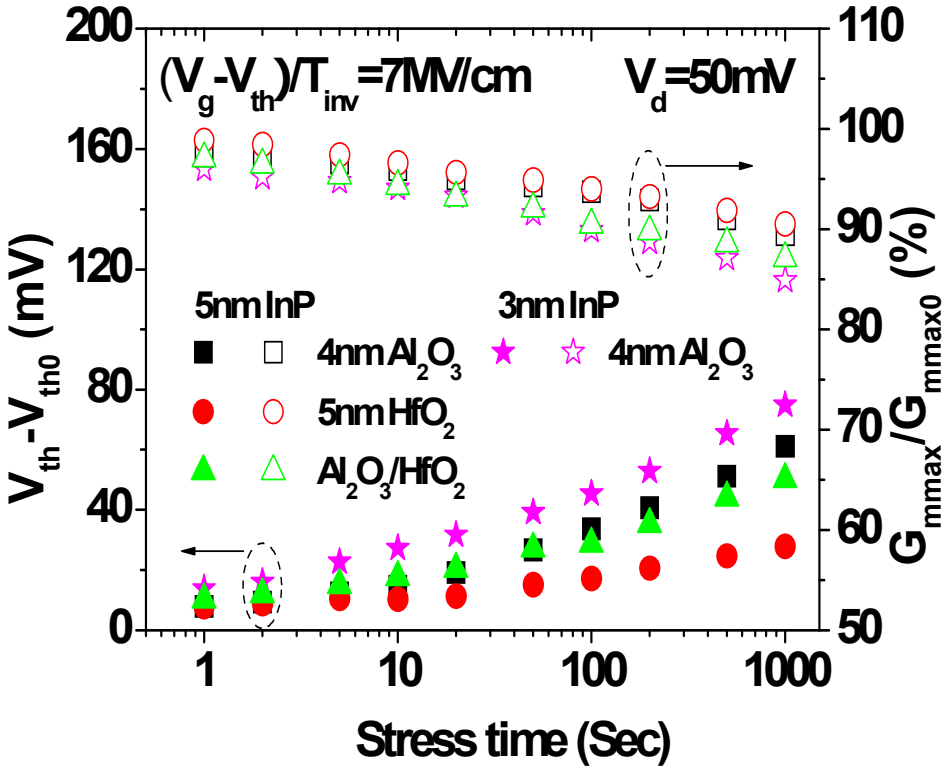

Figure 3.20 V_{th} shift and G_{mmax} degradation with electrical stress of 7MV/cm for MOSFETs with 3nm or 5nm InP barrier and various oxides (4nm Al_2O_3, 5nm HfO_2 and 1nm Al_2O_3/ 4nm HfO_2). V_{th0} and G_{mmax0} are results of fresh device

SS and on/off current were significantly improved at 115K for MOSFETs with InP/InAlAs barrier and HfO_2 oxide, highlighting the presence of scattering due to interface traps (Figure 3.21). Effective channel mobility was measured by split-CV method at various temperatures from 115K to 433K on $In_{0.7}Ga_{0.3}As$ MOSFETs with InP/ InAlAs barrier and 9 nm HfO_2 or 9 nm Al_2O_3 oxides to investigate the scattering mechanisms (Figure 3.22). Coulombic scattering and phonon scattering are the main factors affecting mobility at low electron density. Coulombic scattering (from interface and oxide charges) dominates at low temperature and optical phonon scattering (from both substrate and high-κ oxides) dominates at high temperature. At high Q_n, surface

roughness scattering also plays a role. Compared to Al_2O_3, lower mobility of MOSFETS with HfO_2 results from high interface charges and high high-κ phonon scattering.

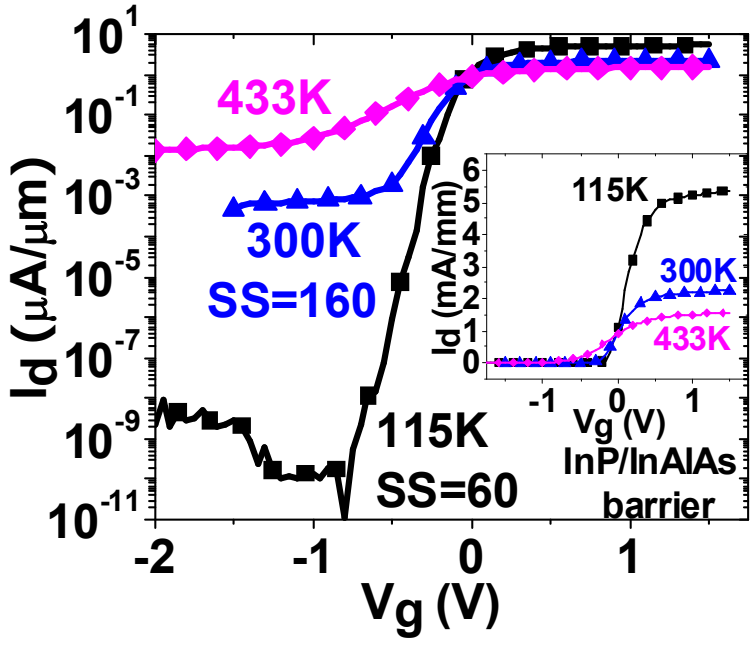

Figure 3.21 SS and I_d on/off current were significantly improved at 115K for QW MOSFETs with InP/InAlAs barrier and HfO_2 oxide, showing effect of interface traps and importance of III-V/high-κ interface (V_d=50 mV)

Figure 3.23 and figure 3.24 plot the simulated energy band diagram and carrier density for MOSFETs with 5 nm InP barrier and 4 nm Al_2O_3 (EOT=2 nm). The fermi-level in InP barrier moves toward conduction band edge and results in high electron density in InP barrier layer at V_g>1 V. This suggests that too high gate voltages should not be applied on such buried channel MOSFETs in order to gain high mobility.

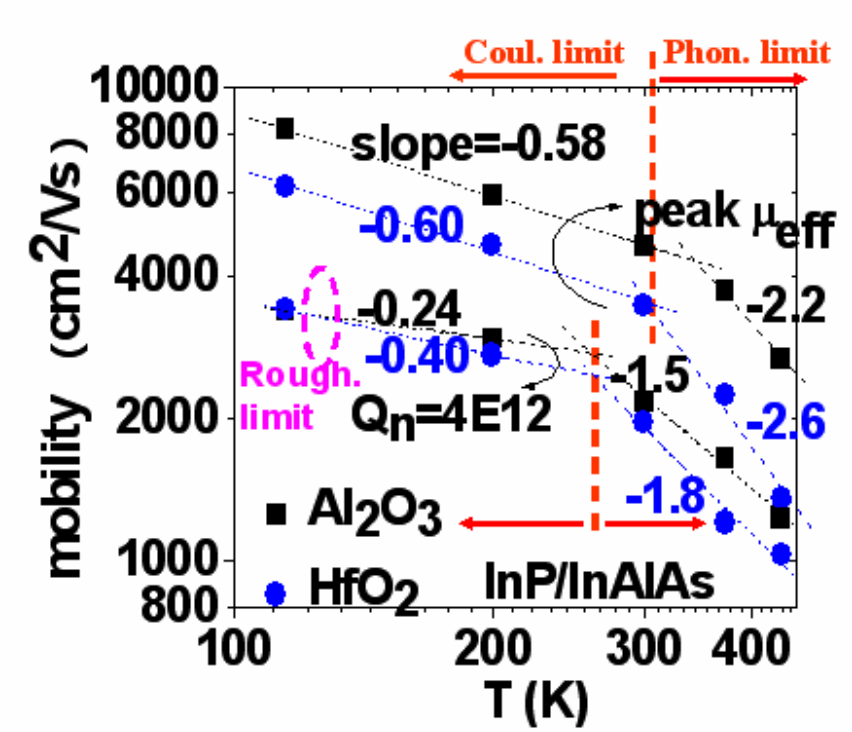

Figure 3.22 Temperature dependence mobility of QW MOSFET with HfO_2 and Al_2O_3 dielectrics at low N_{inv} (peak μ_{eff}) and high N_{inv} ($4x10^{12}$ /cm^2).Compared to Al_2O_3, lower mobility with HfO_2 result from high interface charges and high-κ phonon scattering.

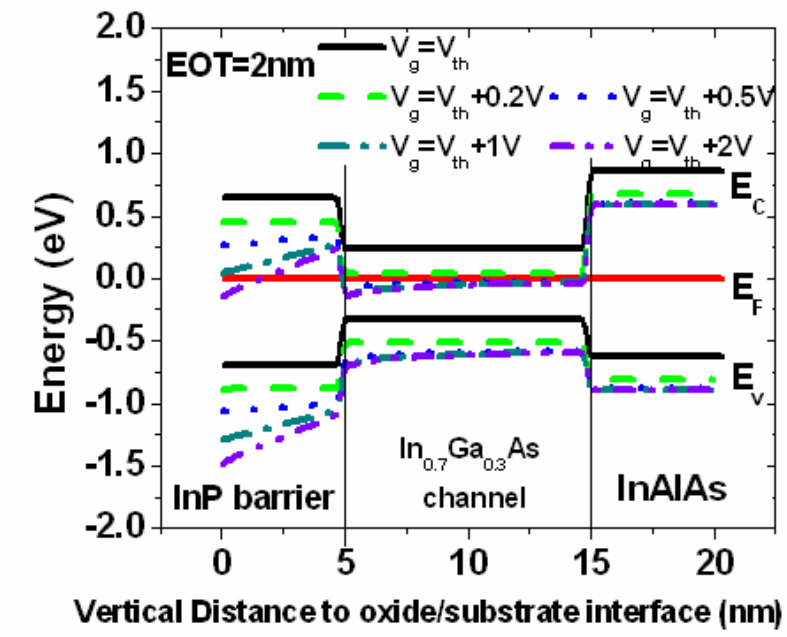

Figure 3.23 (Simulated) Energy band diagram versus substrate vertical distance at varied V_g for MOSFETs with 5 nm InP barrier and 4 nm Al_2O_3.

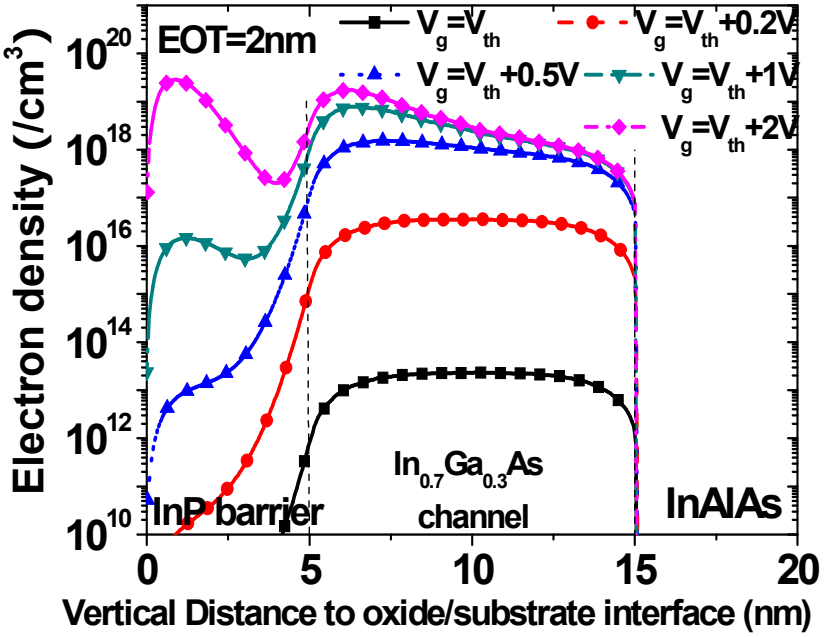

Figure 3.24 (Simulated) Carrier density versus substrate vertical distance at varied V_g for MOSFETs with 5nm InP barrier and 4nm Al_2O_3 oxide.

In conclusion, we have investigated the characteristics of $In_{0.7}Ga_{0.3}As$ MOSFETs with InP or InP/InAlAs barrier and various ALD gate dielectrics. Adding InAlAs into barrier significantly improves device performance at high field. Devices with thicker InP barrier exhibits higher μ_{eff} than with thinner InP. MOSFETs with Al_2O_3 exhibit better interface quality than HfO_2, and Al_2O_3/HfO_2 bilayer improves transistor performance compared to single HfO_2. High μ_{eff} with low gate leakage has been demonstrated owing to our novel III-V MOSFETs structure and fabrication process.

3.3 Summary

In this chapter, buried channel InGaAs MOSFETs with various barriers are fabricated to improve the channel mobility. In the effects of several MOSFETs barrier schemes, such as double-barrier (InP/InAlAs), single InP barrier and no barrier on $In_{0.7}Ga_{0.3}As$ channel are evaluated. Evaluations of high-κ dielectrics are also discussed. InP is an effective barrier to enhance InGaAs channel mobility, especially for $In_{0.7}Ga_{0.3}As$. InP/InAlAs double barrier reduces electron spilling-over effect compared to single InP barrier, thus increase both peak and high field mobility compared to devices without barrier. The InP/InAlAs double barrier architecture also significantly improves high-field mobility compared to same thickness single InP barrier. We have demonstrated significant improvement in SS, G_m and I_{on} of III-V MOSFETs.

The key factors that improve III-V MOSFETs are 1) the epitaxial InP/InAlAs double-barrier confining carriers in quantum-well channel and 2) good $InP/Al_2O_3/HfO_2$ interface with scaled EOT. Mobility was also improved by Al_2O_3 with smaller interface charge scattering and smaller soft phonon scattering.

Chapter 4 GaAs and InP MOSCAPs and MOSFETs

4.1 Motivation

Wide bandgap III-V materials such as GaAs and InP have been investigated to develop MOSFETs with high-performance during last few decades. Except for their higher bulk electron mobility compared to silicon (eg. 8500 cm^2/Vs electron mobility for GaAs, 4600 cm^2/Vs for InP and 1500 cm^2/Vs for Si), wide bandgap III-V material can provide low off-current density thus low power consumption due to reduced band-to-band tunneling and carrier generation/recombination rate. Furthermore, commercially available semi-insulating GaAs and InP substrates can be used for both n-type and p-type MOSFETs and resolve CMOS latch-up problems [85]-[86].

4.2 MOSCAPs on GaAs with germanium nitride passivation layer

The main obstacle to GaAs based MOSFET devices is the lack of high quality, thermodynamically stable insulators that passivate the interface. Recently, a few types of interfaces with dielectrics were investigated. These include in-situ passivation of GaAs interface with silicon interface control layer grown by MBE [87]-[88], in-situ MBE deposition of Ga_2O_3-Gd_2O_3 mixture or Gd_2O_3 [89]-[90], atomic layer deposition (ALD) of Al_2O_3 directly on GaAs substrate [91] and physical vapor deposited (PVD) Si or Germanium (Ge) as interfacial passivation layer (IPL) between GaAs and the dielectrics [29], [30]. A high-κ gate dielectric is a key component of future generation complimentary MOS (CMOS) devices [4]. It provides the path towards keeping the leakage current low even for low equivalent oxide thickness (EOT).

The thin EOT HfO_2 MOSCAPs with low C-V frequency dispersion have been achieved using a thin layer of sputtered Ge as an IPL and high-κ (HfO_2) material as gate dielectric films on GaAs substrate [92]. However, humps usually exist in the C-V traces near the flatband voltage at about 1KHz. These humps also appear in the Ge substrate MOSCAPs, which was explained by the slow interface trap levels [93]. In this paper, improved C-V characteristics without humps, and good interface passivation are realized using a thin reactive sputtered Ge_xN_y IPL and HfO_2 gate dielectrics on GaAs substrate.

We investigate the effect of a thin Ge_xN_y insulator IPL on the C-V and I-V characteristics of TaN/HfO_2/Ge_xN_y/GaAs MOSCAPs. Good interface between the dielectric and the semiconductor is indicated by the small C-V frequency dispersion, thin EOT (1.6 nm) with the leakage current density less than 1×10^{-5} A/cm^2 is achieved. We studied the charge trapping characteristics under constant voltage stress, it has been found that compared to Ge IPL, MOSCAPs with Ge_xN_y IPL shows smaller flatband voltage shift rate and reduced gate leakage decreasing rate due to lower trap generation rate.

MOSCAPs were fabricated on n-type GaAs (100) wafer doped with Si [$(1.5\text{-}2.5)\times10^{17}$ /cm^3]. The surface oxides were removed with the HCl clean followed by $(NH_4)_2S$ dip, resulting in a clean sulfur passivated GaAs surface. The Ge_xN_y IPL was deposited by RF reactive sputtering of Ge in N_2 and Ar ambient at 450℃. HfO_2 films were deposited by DC sputtering of Hf, followed by post deposition annealing (PDA) at 600℃ in N_2 (O_2 5%) ambient. PVD TaN was used as gate electrode. Gate patterning used reactive ion etching (RIE) based on CF_4 gas, and the gate area is 1.226 cm^2. After gate patterning, low-resistance ohmic contact was formed by using AuGe/Ni/Au alloy on the backside of the wafer. The samples were then annealed at 450℃ for 30 s in N_2. For comparison, we also fabricated GaAs MOSFET with Ge IPL using the same process except that the Ge is deposited by RF sputtering of Ge in Ar ambient.

During the IPL deposition, the thickness of Ge_xN_y IPL was varied by changing the deposition time from 10 seconds to 2 minutes. For the deposition time of 60 s, the Ge_xN_y is about 8-12 Å thick. The thickness of HfO_2 is fixed at about 10 nm. Figure 4.1 shows the typical C-V characteristics of $TaN/HfO_2/Ge_xN_y/GaAs$ MOSCAPs as a function of frequency with optimized 60 sec Ge_xN_y IPL. The inset is the C-V characteristics of $TaN/HfO_2/Ge/GaAs$ MOSCAPs with 30 s Ge IPL and 10nm HfO_2, and the thickness of the Ge IPL was also optimized, which is about 10 Å. The humps observed on the C-V curves at 1KHz with Ge IPL do not exist in the Ge_xN_y IPL structure, implying reduced slow interface trap densities due to the nitrogen effect.

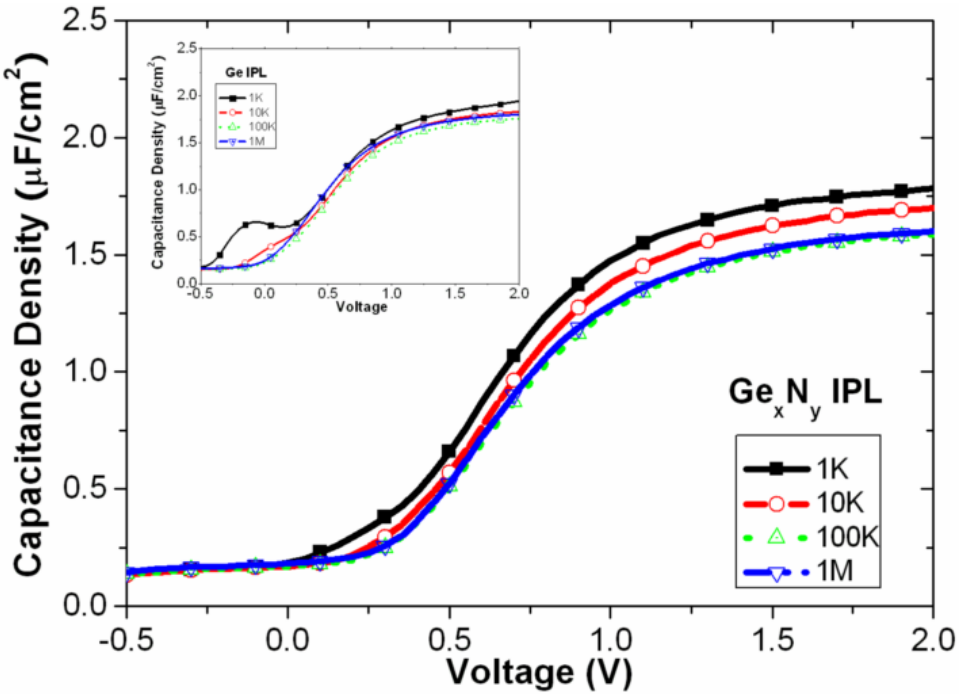

Figure 4.1. C-V characteristics of $TaN/HfO_2/Ge_xN_y/GaAs$ as a function of frequency for 60s Ge_xN_y IPL. Inset shows C-V characteristics of $TaN/HfO_2/Ge/GaAs$ for 30s Ge IPL.

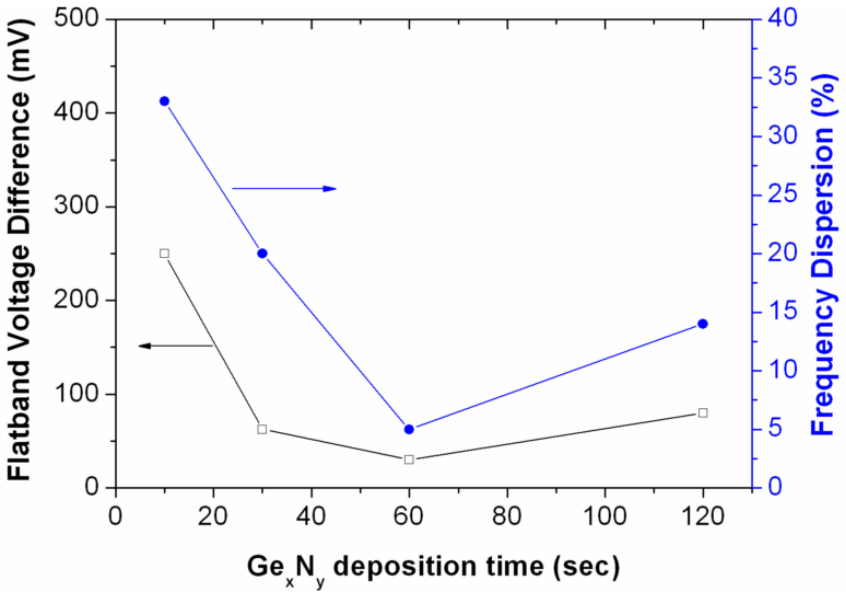

Figure 4.2 Frequency dispersion (capacitance difference (%) between 1 MHz and 10 KHz at gate voltage V_g=2 V) and flatband voltage difference between 1 MHz and 10 KHz versus Ge_xN_y deposition time.

Figure 4.2 shows the frequency dispersion which is defined by capacitance difference (%) between 1 MHz and 10 KHz at accumulation region when applied gate voltage is 2 V for varying Ge_xN_y deposition time. The flatband voltage difference between 1 MHz and 10 KHz versus Ge_xN_y deposition time is also shown. The Ge_xN_y deposition time of 60 seconds was found to result in the smallest frequency dispersion (about 5%) and the smallest flatband voltage difference (<50 mV), demonstrating low interface state density. We think that the role of Ge_xN_y IPL is to prevent the substrate from oxidizing during the thermal treatment and reduce the interface state density. With smaller Ge_xN_y deposition time, the IPL may be not thick enough to passivate the GaAs surface, while thicker Ge_xN_y may introduce more strain induced defects which will degrade the interface characteristics indicated by larger frequency dispersion and flat band voltage difference. Using conductance method, the interface state density (D_{it}) of 1-1.5×10^{12} $cm^{-2}eV^{-2}$, has been obtained for $TaN/HfO_2/Ge_xN_y/GaAs$ MOSCAPs structures,

similar to the value for GaAs MOSFET with Si IPL [94]. It is interesting to point out that Ge nitride interfacial layer has also been used on Ge substrate, and exhibited D_{it} of less than 10^{12} $cm^{-2}eV^{-2}$ [95], this implies that Ge_xN_y can provide good interface for both semiconductor substrates.

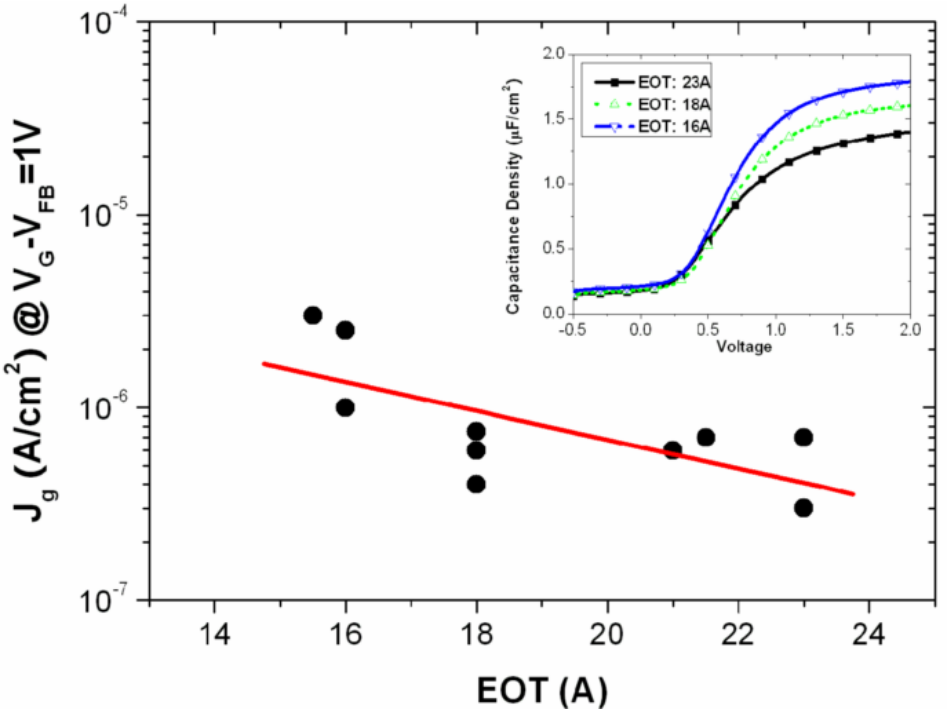

Figure 4.3 Gate leakage current at $V_g=V_{FB}+1$ V versus EOT for GaAs MOSFET with 60 s Ge_xN_y IPL. Inset shows C-V curves at 1 MHz with different EOT. V_{FB} is the flat band voltage.

For TaN/HfO_2/Ge_xN_y/GaAs MOSCAPs structure, we fixed the deposition time of Ge_xN_y at 60 s which gave the optimum interface characteristics, and we varied the HfO_2 thickness and measured their leakage currents, and we calculated the equivalent oxide thickness (EOT) values using a C-V simulation program counting the quantum effects. The gate dielectric leakage current density (J_g) obtained at gate voltage $V_g=V_{FB}+1$ V as a function of EOT is shown in figure 4.3. When the EOT is about 1.6 nm, the leakage

current density is still less than 5×10^{-6} A/cm^2. The inset is the C-V curve with different EOT value from 1.6 nm to 2.3 nm.

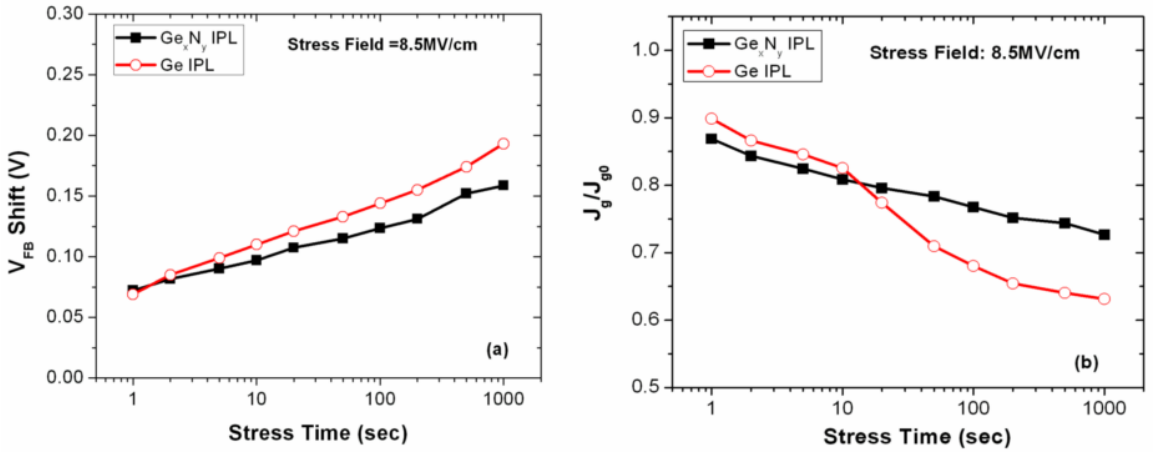

Figure 4.4 (a) Flatband voltage shift under constant voltage stress. Same stress fields (V_g-V_{FB0})/EOT=8.5 MV/cm are applied for both MOSCAPs with 60 s Ge_xN_y or 30 s Ge IPL. V_{FB0} is the flatband voltage of fresh device. (b) Normalized gate leakage at V_g=1.5 V under constant voltage stress. J_{g0} is the gate leakage current density of fresh device. Same stress fields (V_g-V_{FB0})/EOT=8.5 MV/cm are applied for both samples.

Figure 4.4 shows the flatband voltage shift and the normalized gate leakage shift under constant voltage stress. The deposition time is 60 s for Ge_xN_y and 30 s for Ge IPL, the HfO_2 is about 10 nm thick. Same stress fields (V_g-V_{FB0})/EOT=8.5 MV/cm are applied for both GaAs MOSCAPs with Ge_xN_y and Ge IPL, V_g is the gate voltage and V_{FB0} is the flatband voltage of the fresh device. From figure 4.4(a), the MOSCAPs with Ge_xN_y and Ge IPL show similar flatband shift after 1 second stress, and the MOSCAPs with Ge_xN_y IPL exhibit lower rate of flatband voltage shift which indicates reduced trap generation rate. Reduced rate of gate leakage change measured at V_g=1.5V under constant voltage stress (figure 4.4(b)) further supports lower trap generation rate for Ge_xN_y IPL.

In conclusion, GaAs MOSCAPs with Ge_xN_y IPL and HfO_2 dielectric layer was demonstrated to have low interface state density and thin EOT. Compared to GaAs

MOSCAPs with Ge IPL, the Ge_xN_y IPL provides improved C-V characteristics without humps, which indicates lower slow trap density. Moreover, the lower flatband voltage shift rate and gate leakage decreasing rate were also achieved in the TaN/HfO_2/Ge_xN_y/GaAs MOSCAPs structure compared to the MOSCAPs with Ge IPL.

4.3 Gate-first inversion-type InP MOSFETs with ALD Al_2O_3 gate dielectric

Progress has been made on inversion-type III-V MOSFETs including GaAs MOSFETs with Si or Ge passivation layer and HfO_2 dielectrics [29], [92], or with MBE Ga_2O_3 (Gd_2O_3) dielectrics [89], [90], InGaAs MOSFETs with ALD Al_2O_3 dielectrics [68], [91], or with Si passivation layer and HfO_2 dielectrics [96], or with MBE Ga_2O_3(Gd_2O_3) dielectrics [42], and InP MOSFETs with ALD Al_2O_3 dielectrics [97]. GaAs inversion-type MOSFETs usually have problems of low drive current (e.g. 162μA/mm [30], 400μA/mm [98], 500μA/mm [99]). While InGaAs MOSFETs can provide larger drive current (e.g. 400mA/mm [68], 1A/mm [21]), they also exhibit relatively high off-current density (e.g. 5×10^{-4}mA/mm [68]), small current on-off ratio (e.g. $<10^4$ [68], 150 [21]) and large subthreshold swing (e.g. 240mV/dec [68], 330mV/dec [21]). On the other hand, InP inversion type MOSFETs with ALD Al_2O_3 have showed the capability of high drive current density (e.g. 70mA/mm for 0.75μm gate length [97]), and much smaller off-current density due to larger bandgap (1.34 eV) compared to InGaAs (0.74eV for $In_{0.53}Ga_{0.47}As$). In this paper, we have systematically studied the effects of sulfur (S) passivation, post-deposition anneal (PDA) and substrate doping type on device characteristics of inversion-type InP NMOSFETs. The influence of transient and slow charge trapping in the gate stack has also been investigated.

MOSFETs were fabricated on InP (100) substrate with a ring-type structure. The native oxides were removed with a 1% HF solution, then for some samples, S passivation

was performed by dipping in a 20% $(NH_4)_2S_x$ water solution at room temperature for 10 min. After surface treatment, a 10 nm Al_2O_3 was deposited by ALD with trimethylaluminum (TMA) and H_2O as precursors at 250℃. Some samples underwent a PDA at 500℃ in N_2 for 5 minutes. After TaN gate electrode deposition and gate patterning, a Si ion implantation (1×10^{14} /cm^2 at 35 keV) was performed for n^+ source/drain extension, followed by a high temperature rapid thermal annealing (RTA) at 750℃ for 20 sec to activate the implanted dopant in nitrogen ambient. The ohmic source/drain contacts were made using the evaporation of AuGe/Ni/Au and a conventional lift-off process, followed by RTA at 450℃ for 30 sec in nitrogen ambient.

Table 4.1 Effects of Sulfur passivation and PDA on MOSFETs characteristics

	Process		MOSFETs characteristics			
	Sulfur passivation	PDA	V_{th} (V)	I_d@V_d=2 V V_g-V_{th}=2 V (mA/mm)	g_{mmax}@ V_d=0.05 V (mS/mm)	S.S. (mV/dec)
A	No	No	0.49	5.2	0.21	176
B	Yes	No	0.36	12.5	0.46	139
C	**Yes**	**Yes**	**0.21**	**15.5**	**0.65**	**134**

* W=400 μm, L=8 μm

Table 4.1 compares the characteristics of MOSFETs on SI-InP substrates with or without S passivation and PDA by listing the threshold voltage (V_{th}), drive current density (I_d), maximum transconductance (g_{mmax}) and subthreshold swing (S.S.). It has been found that transistors with S passivation show more than two times higher driver current density and much smaller subthreshold swing. These improvements probably can be attributed to the better thermal stability of the samples with S passivation [100]. PDA

at 500℃ for 5min also improves the transistor characteristics by reducing electron traps in the oxide layer during heat treatment [100].

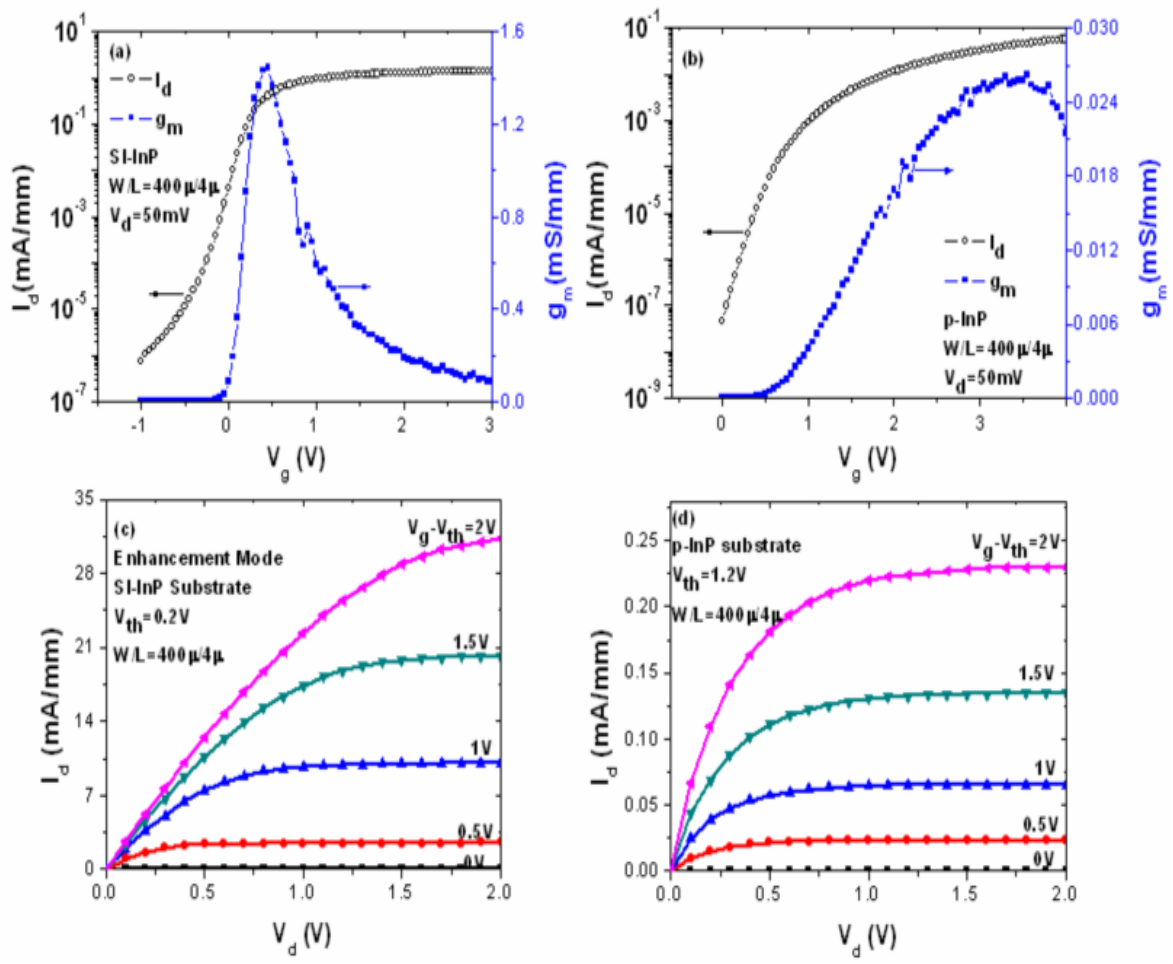

Figure 4.5 DC I_d-V_g curve and extrinsic transconductance (g_m) as a function of gate bias in the linear region (V_d=50mV) for SI-InP MOSFETs (a) and p-InP MOSFETs (b). DC I_d-V_d characteristics as a function of gate bias for SI-InP MOSFETs (c) and p-InP MOSFETs (d). The gate bias is varied from V_{th} to V_{th}+2 V with 0.5 V step.

Besides the fabrication process, substrate doping type is another determining factor for device performance. Transistor characteristics of SI- and p-InP substrate are compared in figure 4.5. Figure 4.5(a) and figure 4.5(b) illustrate the I_d-V_g curve and the transconductance as a function of gate bias at the linear region (V_d=50 mV). The V_{th} is

around 0.2 V for SI-InP substrates and 1.2 V for p-InP substrates extrapolated linearly from the maximum transconductance point. The subthreshold swings of 135 mV/dec for SI-InP and 146 mV/dec for p-InP were obtained. The off-current density is less than 1×10^{-6} mA/mm for SI-InP and 1×10^{-7} mA/mm for p-InP. The peak extrinsic transconductance is 1.5 mS/mm for SI-InP and 0.026 mS/mm for p-InP at V_d=0.05 V. Figure 4.5(c) and figure 4.5(d) show the DC I_d-V_d characteristics as a function of gate bias from the same MOSFETs in figure 4.5(a) and figure 4.5(b). The gate voltage is varied from V_{th} to V_{th}+2 V with 0.5 V step. I_d of 32 mA/mm for SI-InP and 0.23 mA/mm for p-InP were obtained (L=4 μm, V_g =V_{th}+2 V & V_d=2 V).

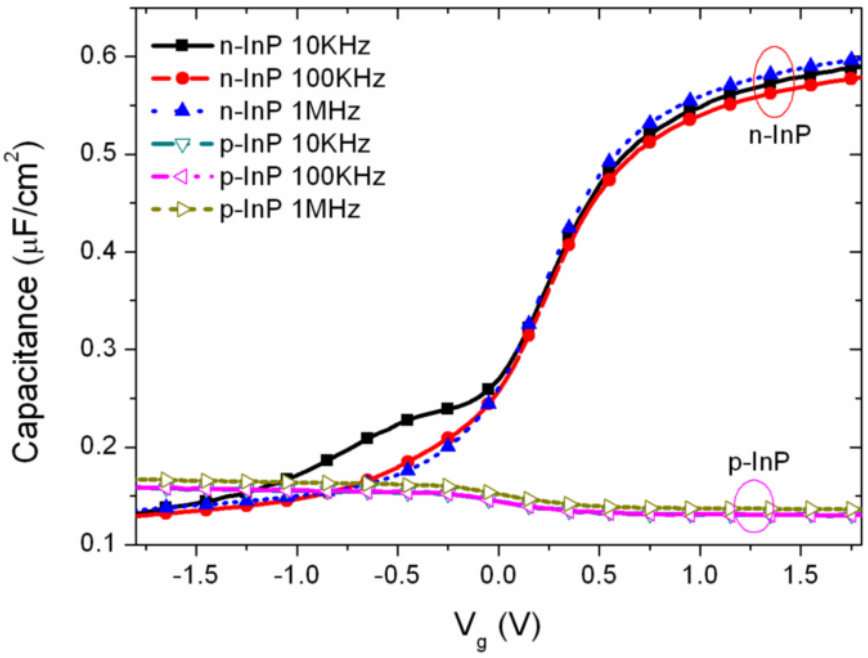

Figure 4.6 C-V characteristics of TaN/Al_2O_3/InP as a function of frequency for both n-InP substrate and p-InP substrate. The thickness of Al_2O_3 is 10 nm.

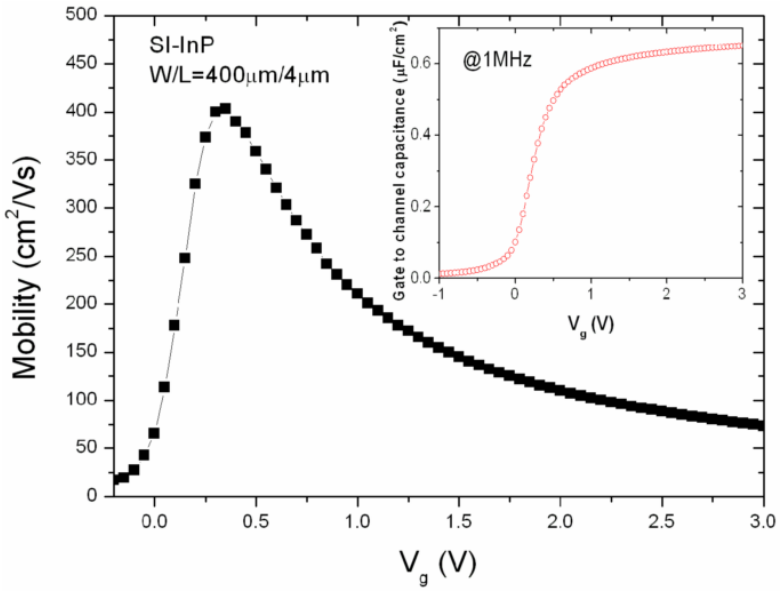

Figure 4.7 Calculated effective electron mobility as a function of gate voltage for SI-InP MOSFETs. Inset: 1MHz C-V curve between gate and channel.

We observe that SI-InP MOSFETs show much higher transconductance and drive current density than p-InP MOSFETs. To explain this difference, we plotted the typical C-V characteristics of TaN/Al_2O_3/InP MOSCAPs at different frequencies from 10KHz to 1MHz for both n-InP (Sulfur doped, 5×10^{17} /cm^3) and p-InP (Zinc doped, 5×10^{17} /cm^3) substrates in figure 4.6. The ALD Al_2O_3 is 10 nm thick. One can see that the C-V curve of n-InP substrate shows small frequency dispersion (<5%) at the accumulation region. It has a small bump in the depletion region at 10 KHz, which can be explained by slow interface trap levels [93]. The C-V curve of p-InP MOSCAPs has large stretch-out. It has been found that the C-V curve at various frequencies of n-type substrate reflects interface state density above the middle gap while for the p-type substrates, the C-V curve reflects interface state density below the middle gap [101]. Above results suggest that the ALD Al_2O_3 on InP system has asymmetric distribution of interface state along the bandgap, less interface state density above the midgap than below the midgap. This can be the main reason why SI-InP MOSFETs have much higher drive current and transconductance

than p-InP. Other mechanisms such as higher ionized impurity scattering for p-InP than for SI-InP can also result in lower drive current in MOSFETs on p-InP substrate.

The effective mobility has been calculated over entire gate voltage range using split C-V method. 1MHz C-V curve between gate and channel exhibits an equivalent oxide thickness (EOT) of 4.9 nm and the maximum electron mobility of 410 cm^2/Vs (figure 4.7) for SI-InP MOSFETs (W/L=400 μm/4 μm).

Figure 4.8 shows the threshold voltage shift and the normalized drive current drift for 400 μm/ 4 μm (W/L) MOSFETs on SI-InP substrate with constant electrical stress fields of $(V_g-V_{fb})/EOT=4$ MV/cm. The flatband voltage V_{fb} of 0.15 V is extrapolated from the 1 MHz split-CV (inset of figure 4.7). The V_{th} shift of less than 0.1 V after 1000 sec stress is obtained. The drive current shows less than 2% deduction after 1000 sec stress, indicating much more stable MOSFETs characteristics than earlier results [102].

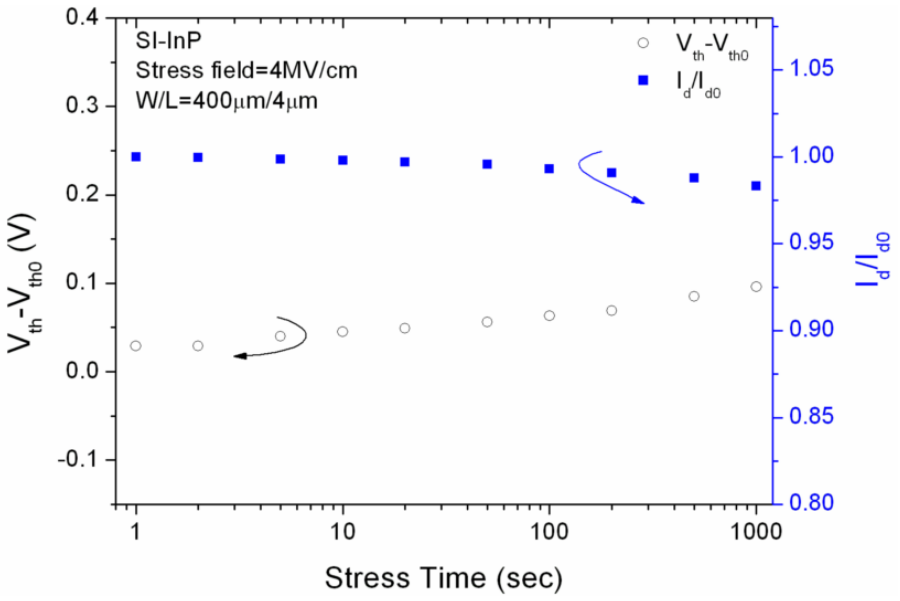

Figure 4.8 Threshold voltage shift and normalized drive current drift under constant voltage stress of $(V_g-V_{fb})/EOT=4$ MV/cm for SI-InP MOSFETs. Flatband voltage V_{fb} of about 0.15 V was extracted from 1MHz split C-V in figure 4.7. V_{th0} and I_{d0} are the threshold voltage and the drive current of the fresh devices.

To suppress the effect of interface states and bulk traps, and reveal more intrinsic device characteristics, the pulsed I_d-V_g under the 50 KHz gate pulse is compared to the DC measurement results for SI-InP MOSFETs (W/L=400 μm/4 μm) in figure 4.9. The inset shows the circuit configuration for pulse measurement. The V_d of the MOSFETs for both DC and pulse measurement was normalized to 0.1 V. In DC measurement, the gate stack traps more electrons at the interface or in the gate stack, degrading the electron mobility and drive current. The DC measurement shows peak transconductance of 2.9 mS/mm while pulse V_g provides 11.6 mS/mm.

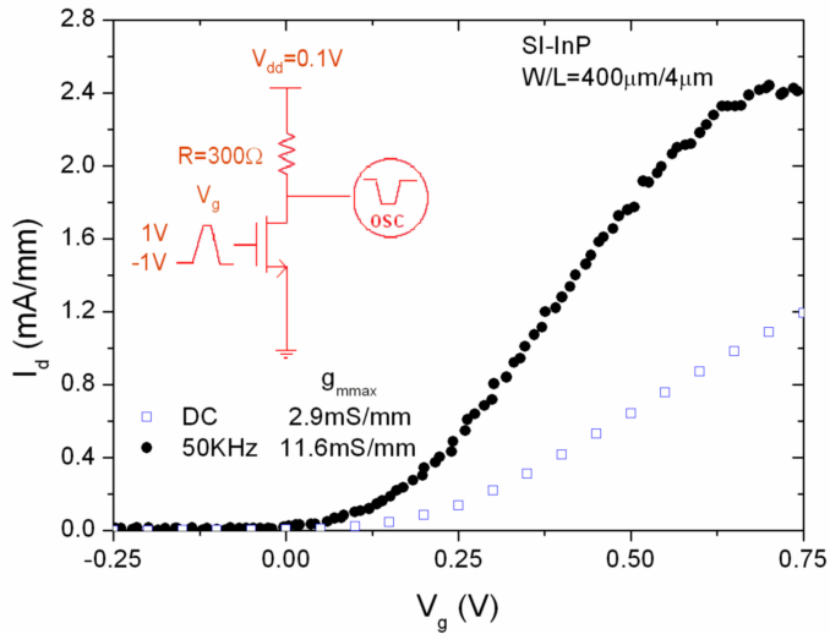

Figure 4.9 DC and pulse I_d-V_g for SI-InP MOSFETs. The frequency of gate pulse is 50 KHz.

In conclusion, gate-first n-channel enhancement-mode inversion-type MOSFETs have been demonstrated with ALD Al_2O_3 dielectric on InP substrate. Applying S passivation and PDA can improve the drive current density and subthreshold swing. The drive current densities of 32 mA/mm and 0.23 mA/mm have been obtained for SI-InP

and p-InP substrates respectively (L=4 μm, V_g-V_{th}=2 V). This difference is believed mainly due to the asymmetric distribution of interface state along the bandgap between InP and Al_2O_3 dielectric. Reliability characteristics including less than 0.1 V threshold voltage shift and less than 2% current drift are obtained for SI-InP MOSFETs after 1000 sec under 4 MV/cm electrical stress. Four times higher transconductance is observed with 50 KHz pulse I_d-V_g measurement than DC data.

Chapter 5 InGaAs TFETs with ALD oxides

5.1 $In_{0.7}Ga_{0.3}As$ TFETs with a I_{on} of 50 μA/μm and a subthreshold swing of 86 mV/dec using HfO_2 gate oxide

As MOSFETs are aggressively scaled, their performance is severely limited by short channel effects and gate leakages. In addition, high subthreshold swing (SS) and thus high operating voltage make power consumption a rising challenge [16]. TFETs with potential SS of less than 60 mV/dec [50] [52] have attracted a great deal of attention as possible alternative to conventional CMOS due to significantly reduced power consumption. III-V materials are preferred over Si due to their larger tunneling current from small electron mass and bandgap [55] [56]. In Ref. [57], $In_{0.53}Ga_{0.47}As$ TFETs using 10 nm Al_2O_3 gate oxide with a saturation current of 20 μA/μm (V_{gs}= 2 V) and a SS > 150 mV/dec were demonstrated for the first time. In this paper, the device performance was improved by fabricating TFETs on molecular beam epitaxy (MBE) $In_{0.7}Ga_{0.3}As$ tunneling junction and using a much smaller equivalent oxide thickness (EOT) with HfO_2 gate oxide. Our results show more than two times higher on-current with much better SS compared to reported $In_{0.53}Ga_{0.47}As$ TFETs [57]. Moreover, we have investigated the dependence of device performance on the EOT of gate oxide and the effects of temperature variation on the device characteristics such as I_{on}, SS, and Esaki diode behavior.

Figure 5.1(a) shows the cross-sectional view of ring-type (figure 5.1(a) inset) vertical $In_{0.7}Ga_{0.3}As$ TFETs. The tunneling junction was a p^+ $In_{0.7}Ga_{0.3}As$ (6 nm, Be doping of 2×10^{19} /cm^3)/ undoped $In_{0.7}Ga_{0.3}As$ (6 nm) hetero-structure. The channel was a 100 nm undoped $In_{0.53}Ga_{0.47}As$ layer. A layer of 30 nm n- $In_{0.53}Ga_{0.47}As$ (Si doping of 1×10^{17} /cm^3) was inserted between the n^+ and the undoped region in order to reduce the

ambipolar conduction (i.e. to suppress transistor turning-on at negative V_{gs} at the otherwise undoped/n^+ InGaAs junction). The side wall was etched by citric acid/H_2O_2 water solution, and ~120 nm p^+ $In_{0.53}Ga_{0.47}As$ was left after etching (figure 5.1(c)). Then 5 to 8 nm thick HfO_2 (κ= 16-18) was deposited by ALD at 200℃ (high κ EOT= 1.2 to 1.8 nm) as the gate oxide, followed by TaN deposited as the gate electrode (figure 5.1(b)). The drain contact was formed by e-beam evaporated AuGe/Ni/Au, and then Cr/Au was deposited on the back of the wafer as the source contact. Then the wafer was annealed at 300 ℃ in N_2 to form the source/drain ohmic contact. Figure 5.1(d) shows the secondary ion mass spectrometry (SIMS) of the substrate.

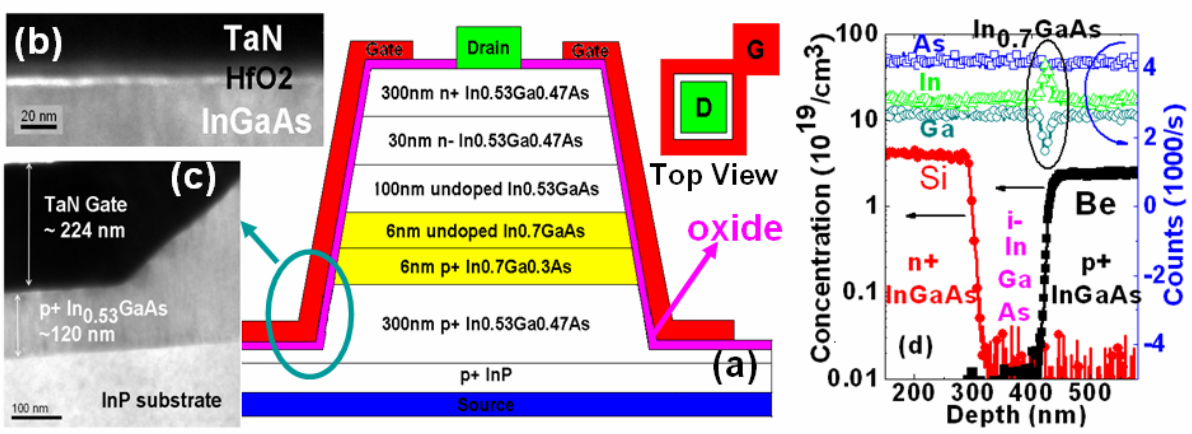

Figure 5.1 (a) Cross-sectional view of $In_{0.7}Ga_{0.3}As$ vertical TFETs with HfO_2 gate oxide and TaN gate electrode. Inset is the top view of ring-type TFETs. (b) Transmission electron microscopy (TEM) image of the TaN/HfO_2/InGaAs interface. (c) TEM image of the side wall structure. (d) Secondary ion mass spectrometry (SIMS) of the TFETs substrate.

Figure 5.2 illustrates the I_d-V_{gs} characteristics of $In_{0.7}Ga_{0.3}As$ TFETs with 5 nm HfO_2 gate oxide (EOT= 1.2 nm). The smallest SS of 86 mV/dec and 93 mV/dec were achieved at V_{ds}= 0.05 V and 1.05 V, respectively. Figure 5.2 inset shows the SS versus the drain current as a function of the drain voltage. The gate leakage current (I_g) is more

than two orders of magnitude lower compared to the drain current, and it is less than 1×10^{-4} A/cm^2 at V_{gs}= 1 V (data not shown). The $I_{dmax}/I_{dmin} > 10^6$ at V_{ds}= 0.05 V. For higher V_{ds}, the I_{dmin} was increased by the ambipolar conduction at negative V_{gs}.

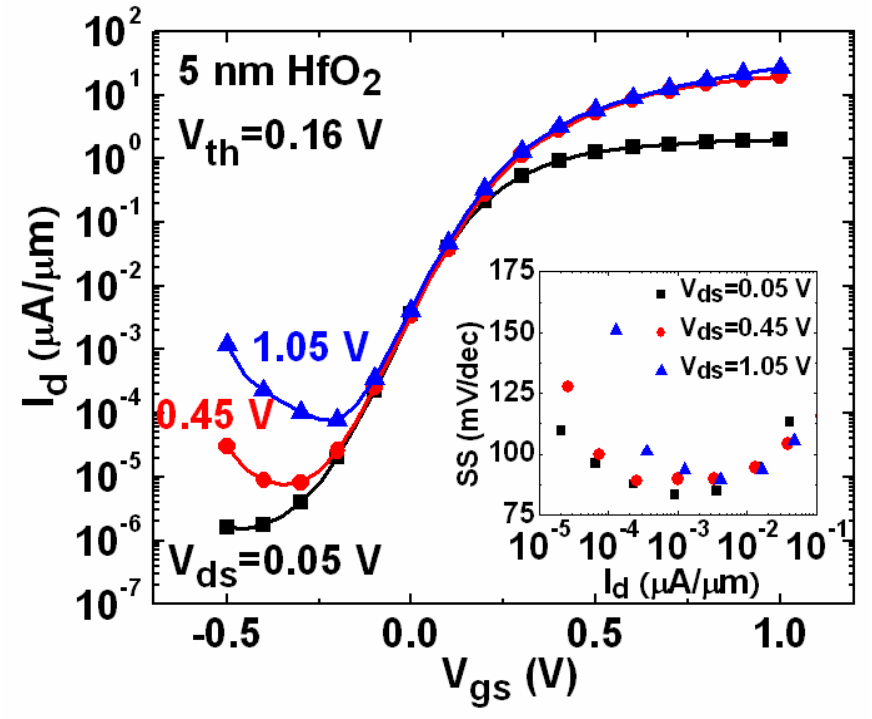

Figure 5.2 Log-scale I_d-V_{gs} characteristics of $In_{0.7}Ga_{0.3}As$ vertical TFETs with 5 nm HfO_2 gate oxide at V_{ds} from 0.05 to 1.05 V (gate width W= 560 μm and length L= 100 nm). Inset shows SS versus I_d as a function of V_{ds} for the same device.

Figure 5.3(a) shows the I_d-V_{ds} characteristics of TFETs with 5 nm HfO_2 at V_g from 0 to 2 V. The transistor on-current is about 50 μA/μm at V_{gs}= 2 V, which is more than two times higher compared to the reported value of $In_{0.53}Ga_{0.47}As$ TFETs [57], while the device still has much smaller SS of 86 mV/dec. A summary of I_{on} and SS reported for Si, Ge and InGaAs TFETs is shown in Table 5.1. One factor increasing the on-current of our TFETs is believed to be the improved Zener tunneling efficiency by using the $In_{0.7}Ga_{0.3}As$ tunneling junction with a smaller bandgap compared to that of $In_{0.53}Ga_{0.47}As$

(E_g = 0.58 eV for $In_{0.7}Ga_{0.3}As$ versus 0.74 eV for $In_{0.53}Ga_{0.47}As$). The smaller EOT by applying HfO_2 gate oxide improved the I_{on} and SS as well. The effect of bandgap on the SS is still under investigation. Figure 5.3(b) and (c) plot the log-scale $|I_d|$ versus $(-V_{ds})$ at room temperature and low temperatures. When V_{gs} is larger than V_{th}, the Esaki diode behavior [103] is shown by the negative differential resistance (NDR) region over part of the forward diode bias curves ($V_{ds} < 0$ V). This is due to the electron tunneling from the n-side conduction band to the p-side valence band when a negative V_{ds} (forward bias on diode) is applied. The Esaki diode behavior demonstrates the band-to-band Zener tunneling mechanism.

Table 5.1 Device Characteristics of TFETs

References	Channel Material	$\|V_{gs}\|$ (V)	V_{th} (V)	$\|V_{ds}\|$ (V)	SS@RT (mV/dec)	I_{on} (μA/μm)	I_{on}/I_{off}
H Zhao (this section)	$In_{0.7}Ga_{0.3}As$	2	0.16	1.05	93	50	$>10^4$
S Mookerjea [57]	$In_{0.53}Ga_{0.47}As$	2.5	~0	0.75	150-290	20	$>10^3$
T. Krishnamohan[54]	Ge	4	~0.25	1	50-60	10	10^6
T. Krishnamohan [54]	Ge	4	~0.25	3	>230	300	$>10^4$
F Mayer [50]	Ge	2		0.8	>400	4	$>10^2$
W Choi [52]	Si	1	0.12	1	52.8	12	10^4
K Bhuwalka [53]	Si	8	3	1.50	285	0.1	10^4
F mayer [50]	Si	3	~0	0.8	42-200	0.02	10^5

The SS and I_{on} of TFETs are improved by the reduced EOT as the HfO_2 thickness is decreased (Figure 5.4(a)). As the high-κ EOT is reduced from 1.8 nm to 1.2 nm, the reduction of the minimum SS from 108 to 86 mV/dec and the 67% increase of the saturation current at V_{gs} = 2 V highlight the impacts of EOT scaling in TFETs. We have

also measured the I-V characteristics of $In_{0.7}Ga_{0.3}As$ TFETs at different temperatures. The drive current at V_{gs}= 1 V and V_{ds}= 0.05 V shows ~ 10% decrease when temperature reduces from 300 K to 150 K, which might be due to increased bandgap at lower temperature. When V_{ds}= 1.5 V, the drive current exhibits ~6% decrease from 300 K to 150 K at V_{gs}= 1 V, which is believed to be caused by both bandgap increase and channel resistance decrease [104].

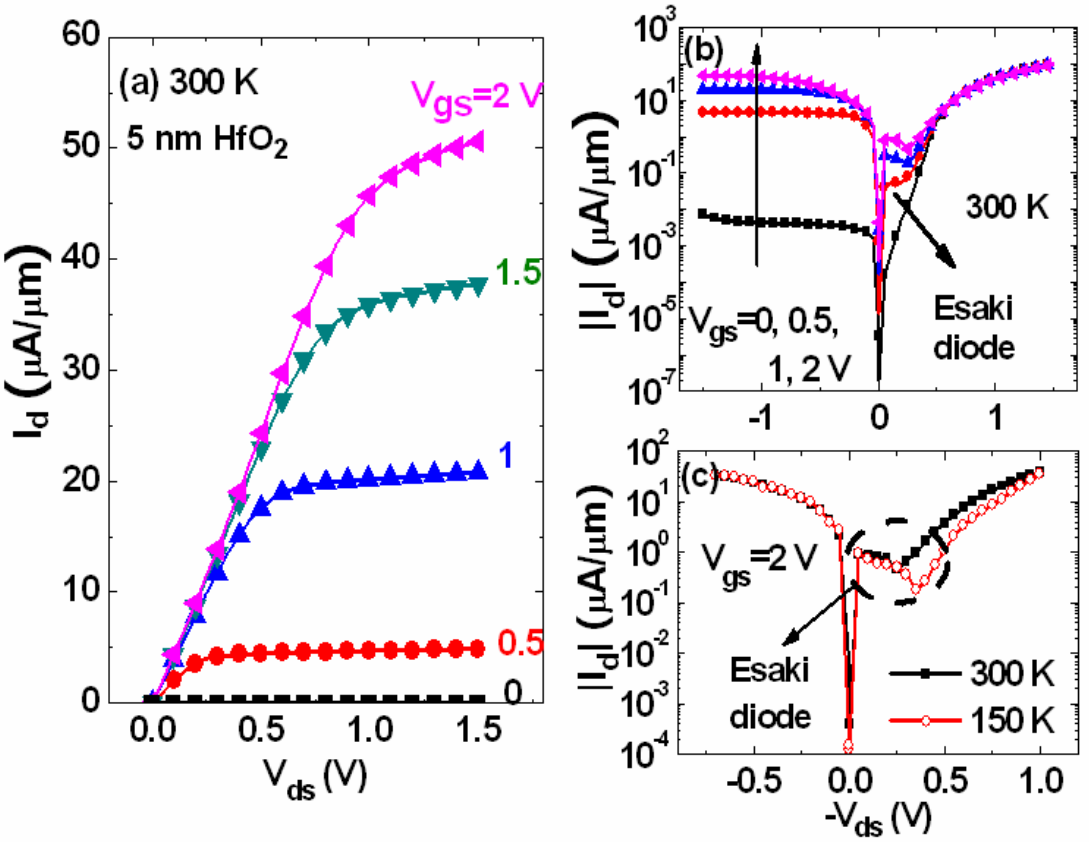

Figure 5.3 (a) I_d vs. V_{ds} at V_{gs} from 0 to 2 V with a 0.5 V step at 300 K for $In_{0.7}Ga_{0.3}As$ TFETs with 5 nm HfO_2 gate oxide. (b) Log-scale $|I_d|$ vs. $(-V_{ds})$ at V_{gs} from 0 to 2 V at 300 K (V_{gs}= 0, 0.5, 1, 2 V) for the same device. (c) Log-scale $|I_d|$ vs. $(-V_{ds})$ at V_{gs}= 2 V at 300 K and 150 K for the same device (W= 560 μm, L= 100 nm).

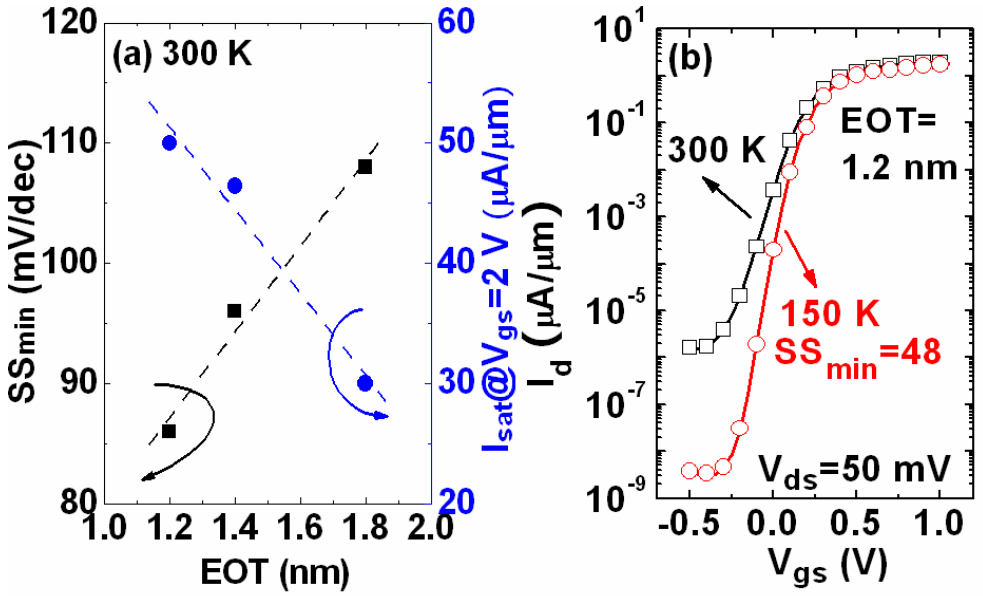

Figure 5.4 (a) The minimum SS and saturation current at V_{gs}= 2 V and V_{ds}= 1.5 V as a function of EOT for $In_{0.7}Ga_{0.3}As$ TFETs using HfO_2 gate oxides with various thicknesses. (b) Log-scale I_d-V_{gs} characteristics at 300 K (SS_{min}= 86 mV/dec) and 150 K (SS_{min}= 48 mV/dec) of $In_{0.7}Ga_{0.3}As$ TFETs with 5 nm HfO_2 gate oxide (W= 560 μm, L= 100 nm).

In Figure 5.4 (b), the SS was improved at 150 K compared to that at room temperature, and the smallest SS of 48 mV/dec was achieved at 150 K. The improved SS is believed to be due to the reduced interface trap response at 150 K in comparison to that at room temperature [23], [57]. The midgap interface trap density (D_{it}) for our ALD HfO_2 / InGaAs interface is about 4×10^{12} /eV/cm^2 measured by the conductance method [105]. These interface traps can retard the Fermi-level movement of the undoped $In_{0.7}Ga_{0.3}As$ layer controlled by the gate bias, and they can also result in the interface trap assisted tunneling and the subsequent thermal emission. These effects would lead to the degradation of SS. With the improved oxide / tunneling junction interface (Figure 5.1(b)), the SS of III-V TFETs can be further reduced. Moreover, further improvement in the MBE growth conditions to form sharper tunneling junctions with more abrupt doping profile can help improve SS. The I_{off} reduction at 150 K might be resulted from a lower

interface trap response and a lower Shockley-Read-Hall (SRH) generation/recombination induced leakage current.

In conclusion, $In_{0.7}Ga_{0.3}As$ TFETs with 5 nm HfO_2 gate oxide (EOT= 1.2 nm) have been demonstrated with an on-current of 50 μA/μm and a minimum SS of 86 mV/dec. The EOT scaling shows effective improvement on both on-current and SS for TFETs. The reduction of bandgap can effectively increase I_d while its effect on SS is still under investigation. The impacts of temperature and interface traps on the device performance were also discussed. $In_{0.7}Ga_{0.3}As$ TFETs achieved simultaneously higher I_{on} and smaller SS compared to other reported III-V TFETs results. The performance improvement paves the way for designing III-V TFETs for ultra-low power digital applications.

5.2 Improving on-current of $In_{0.7}Ga_{0.3}As$ TFETs using $p^{++}/n^{+}/i/n^{++}$ tunneling diode

$In_{0.7}Ga_{0.3}As$ TFETs have been demonstrated with an on-current of 50 μA/μm and a minimum SS of 86 mV/dec in the last section, however, the drive current is still low compared to Si technology with similar gate-length [70]. Instead of a p^{++}/i tunneling junction as in a conventional TFETs (figure 5.5 (a)), a tunneling junction formed between p^{++} region and a narrow fully depleted n^{+} layer under the gate (figure 5.5 (b)) can reduces the tunneling width and increases the lateral electric field (figure 5.6), thereby improve the tunneling efficiency and increase the on-current [106].

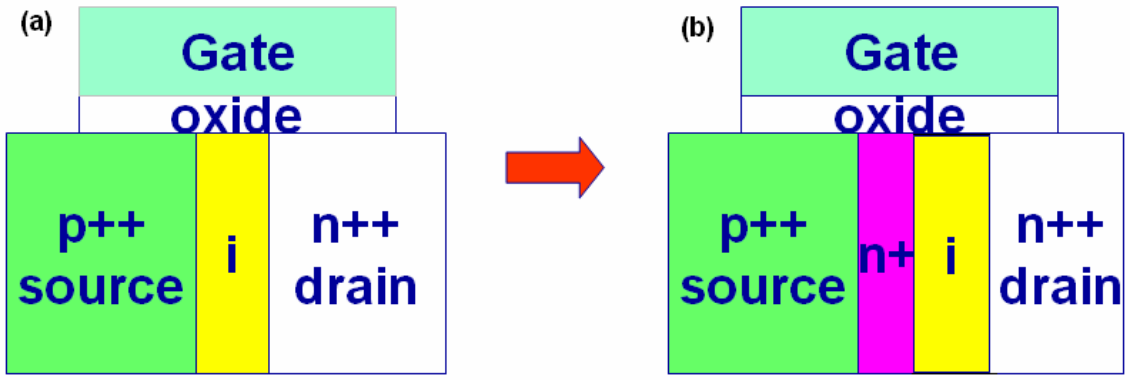

Figure 5.5 (a) Conventional TFETs with p^{++}/i tunneling diode, (b) TFETs with p^{++}/n^{+} tunneling diode.

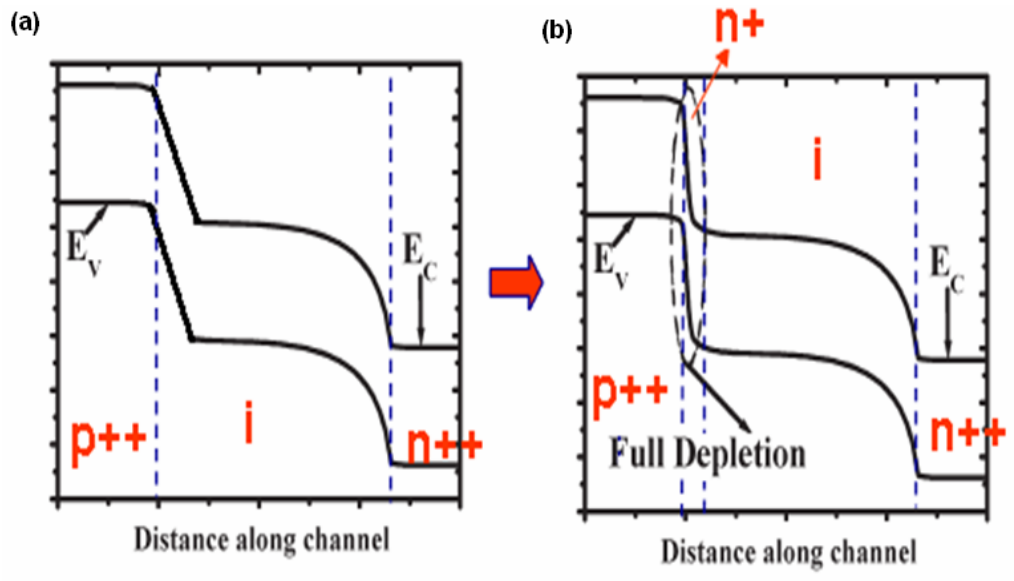

Figure 5.6 (a) Band diagram for conventional TFETs with p++/i tunneling diode, (b) Band diagram for TFETs with p++/n+ tunneling diode.

TFETs were fabricated with two types of tunneling diodes: (a) p^{++} $In_{0.7}Ga_{0.3}As$ (6 nm, Be doping of 2×10^{19} /cm^3)/ i $In_{0.7}Ga_{0.3}As$ (6 nm) and (b) p^{++} $In_{0.7}Ga_{0.3}As$ (6 nm, Be doping of 2×10^{19} /cm^3)/ n^{+} $In_{0.7}Ga_{0.3}As$ (6 nm, Si doping of 2×10^{18} /cm^3). Figure 5.7 shows the substrate structure. Thin 6 nm n^{+} $In_{0.7}Ga_{0.3}As$ with doping of 2×10^{18} /cm^3 was

used so that it can be fully depleted by p^{++} region (figure 5.7 (b)). 5 nm ALD HfO_2 was deposited as gate oxide.

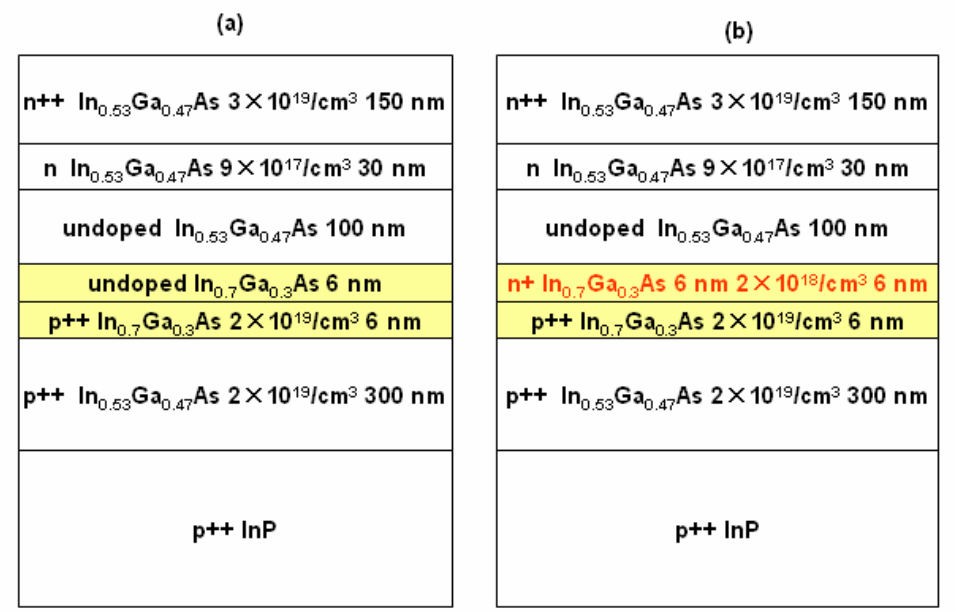

Figure 5.7 (a) Substrate structure for conventional TFETs with p^{++}/i tunneling diode, (b) Substrate structure for TFETs with p^{++}/n^{+} tunneling diode.

Table 5.2 Comparison of device performance for TFETs with p^{++}/i tunneling diode and p^{++}/n^{+} tunneling diode

Sample	SS_{min} @ V_d=0.05 V / V_d= 1 V (mV/dec)	G_{mmax} @ V_d=0.05 V (μS/μm)	V_{th} @ V_d=0.05 V (V)	I_d @ V_g=0.5 V & V_d=1.5 V (μA/μm)	I_d @ V_g=2 V & V_d=1.5 V (μA/μm)
p^{++}/i	84 / 101	7.38	0.21	7.5	49.9
p^{++}/n^{+}	84 / 99	**9.05**	0.15	**12.1**	**59.9**

Table 5.2 compares device performance for TFETs with p^{++}/i and p^{++}/n^{+} tunneling diode. It can be seen that using p^{++}/n^{+} tunneling diode provides 61% and 20% on-current increase at V_g-V_{th}=0.5 V and 2V respectively while maintaining similar SS.

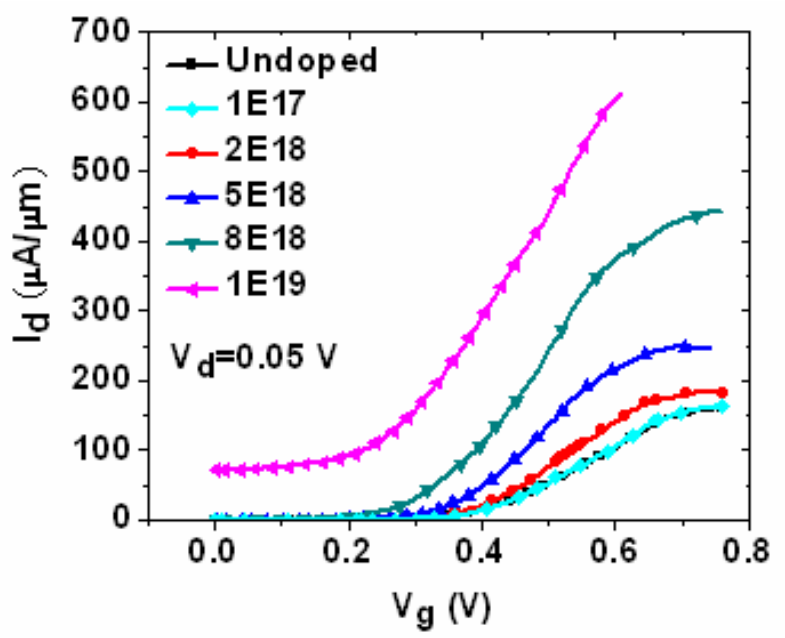

Figure 5.8 (Simulated) I_d-V_g characteristics at V_d=0.05 V for TFETs using p^{++}/n^+ tunneling junction with varied n-type doping concentration from undoped to 1×10^{19} /cm^3 in the n^+ region.

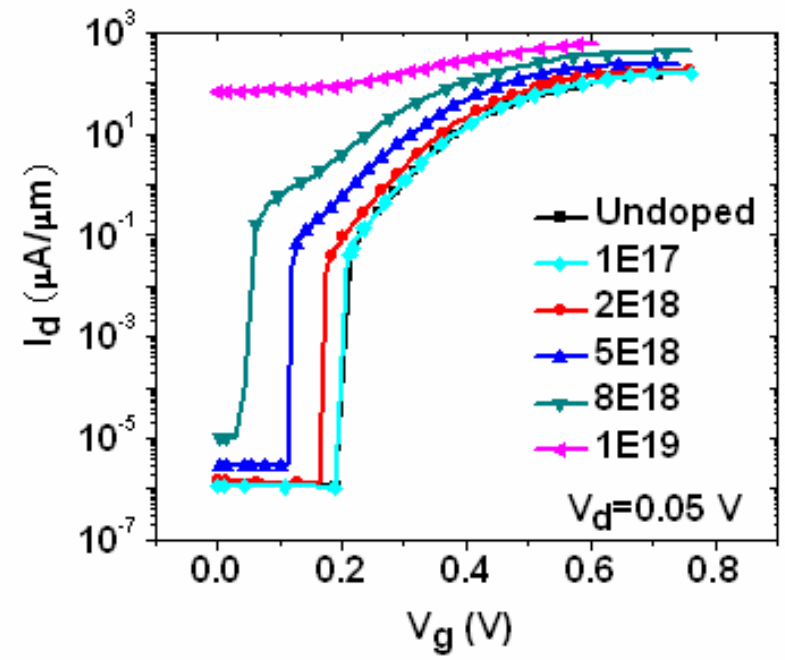

Figure 5.9 (Simulated) Log-scale I_d-V_g characteristics at V_d=0.05 V for TFETs using p^{++}/n^+ tunneling junction with varied n-type doping concentration in the n^+ region.

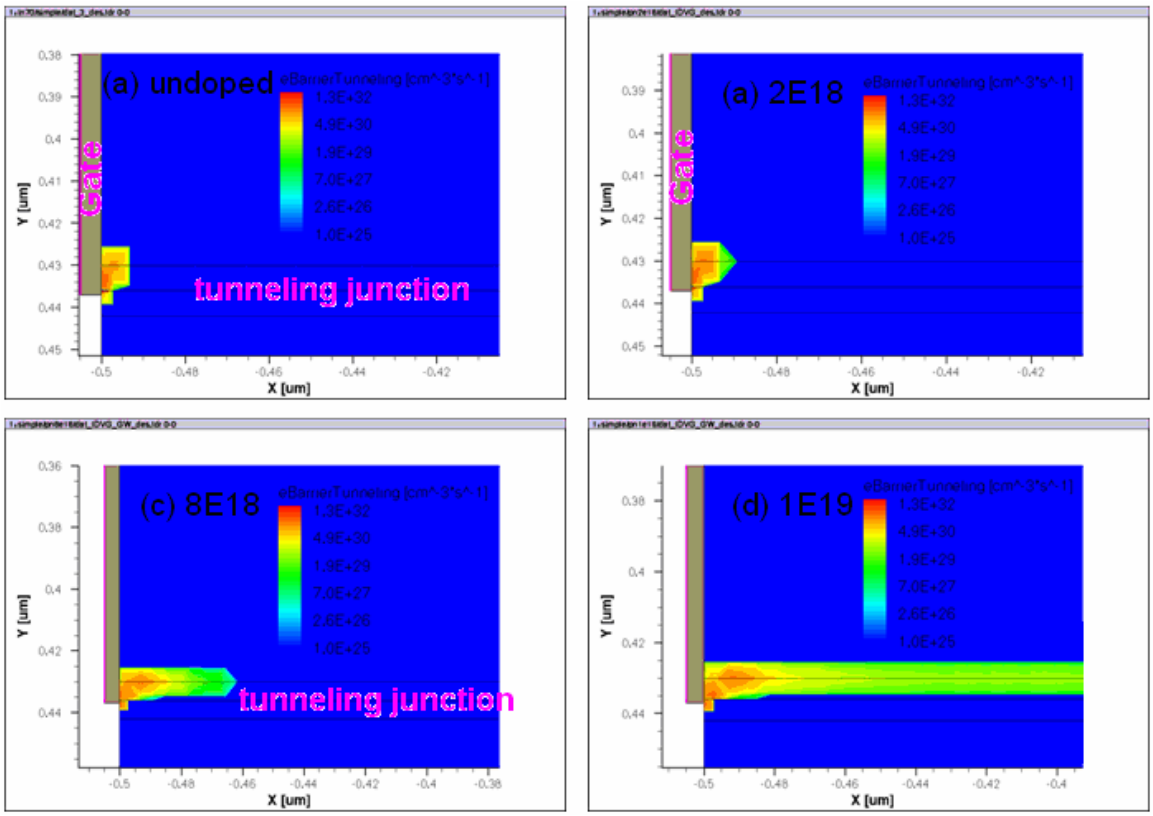

Figure 5.10 (Simulated) Electron band to band tunneling rate at V_g=0.6 V and V_d=0.05 V for TFETs using p^{++}/n^+ tunneling junction with varied n-type doping concentration in the n^+ region. (a) undoped n^+ region, (b) n^+ region with doping concentration of 2×10^{18} /cm^3, (c) n^+ region with doping concentration of 8×10^{18} /cm^3, (d) n^+ region with doping concentration of 1×10^{19} /cm^3.

To tell how much current increase should be achieved with p^{++}/n^+ tunneling diode and how much n-type doping should be used in n^+ region, device characteristics of TFETs with p^{++}/n^+ tunneling diode and various n^+ region doping concentration were simulated using non-local tunneling model [107]. Figure 5.8 illustrated simulated linear I_d-V_g curves and figure 5.9 is log-scale I_d-V_g curves at V_d=0.05 V. The device structure used is the same as shown in figure 5.7 (b) except that the doping concentration of n^+ $In_{0.7}Ga_{0.3}As$ layer is varied from undoped to 1×10^{19} /cm^3. From the simulation results, the doping concentration of n^+ $In_{0.7}Ga_{0.3}As$ layer should be set between 5×10^{18} /cm^3 to 8

$\times 10^{18}$ /cm^3. Too light doping can not effectively increase the electrical field at the tunneling junction and the band to band tunneling rate, while too heavy doping can result in tunneling happening not only at the gate region but also at the entirely p^{++}/n^+ junction region thus not well controlled by the gate bias (figure 5.10).

In summary, TFETs using p^{++}/n^+ tunneling diode with n^+ doping concentration of 2×10^{18} /cm^3 were experimentally demonstrated and they show a ~20% increase of on-current compared with TFETs using p^{++}/i tunneling diode. Simulation results indicate that a proper range of doping concentration of n^+ region should be used to provide both effective on-current enhancement and well gate-controlled tunneling characteristics.

5.3 Effect of tunneling junction thickness and gate oxides on TFETs characteristics

The SIMS results from TFETs with p^+ $In_{0.7}Ga_{0.3}As$ (6 nm, Be doping of 2×10^{19} /cm^3)/ undoped $In_{0.7}Ga_{0.3}As$ (6 nm) tunneling junction in figure 5.1(d) show a diffusion of Be into the undoped $In_{0.7}Ga_{0.3}As$ region and the diffusion length is about 3-5 nm. Since the total $In_{0.7}Ga_{0.3}As$ thickness can not be increased any more due to the lattice mismatch between $In_{0.7}Ga_{0.3}As$ layer and InP substrate, a structure with p^+ $In_{0.7}Ga_{0.3}As$ (4 nm, Be doping of 2×10^{19} /cm^3)/ undoped $In_{0.7}Ga_{0.3}As$ (8 nm) tunneling junction was fabricated to increase the effective undoped $In_{0.7}Ga_{0.3}As$ thickness at the tunneling junction thus increase the tunneling current. TFETs with p^+ $In_{0.53}Ga_{0.47}As$ / undoped $In_{0.53}Ga_{0.47}As$ tunneling junction were also fabricated as a reference. ALD HfO_2 with varied thicknesses or ALD 1 nm Al_2O_3 / 4 nm HfO_2 were deposited as gate oxide. Figure 5.11 shows the substrate structures for TFETs used in this section.

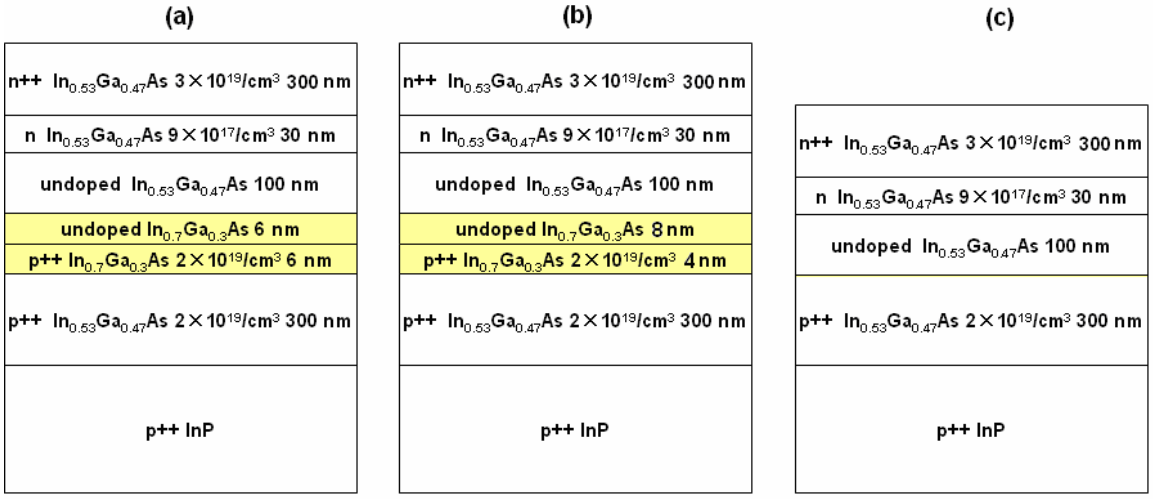

Figure 5.11 Substrate structure for TFETs with p^+ $In_{0.7}Ga_{0.3}As$ (6 nm, Be doping of 2×10^{19} /cm^3)/ undoped $In_{0.7}Ga_{0.3}As$ (6 nm) tunneling junction (a), or p^+ $In_{0.7}Ga_{0.3}As$ (4 nm, Be doping of 2×10^{19} /cm^3)/ undoped $In_{0.7}Ga_{0.3}As$ (8 nm) tunneling junction, or p^+ $In_{0.53}Ga_{0.47}As$ / undoped $In_{0.53}Ga_{0.47}As$ tunneling junction.

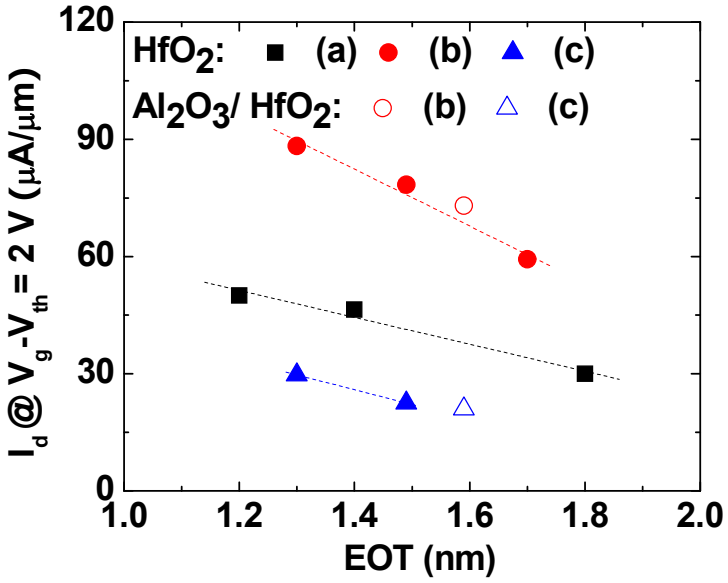

Figure 5.12 I_d at V_g-V_{th}=2 V and V_d=2 V for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ TFETs with HfO_2 or Al_2O_3/ HfO_2 gate oxides. (a): $In_{0.7}Ga_{0.3}As$ 6 nm/ 6 nm; (b): $In_{0.7}Ga_{0.3}As$ 4nm/ 8 nm; (c): $In_{0.53}Ga_{0.47}As$

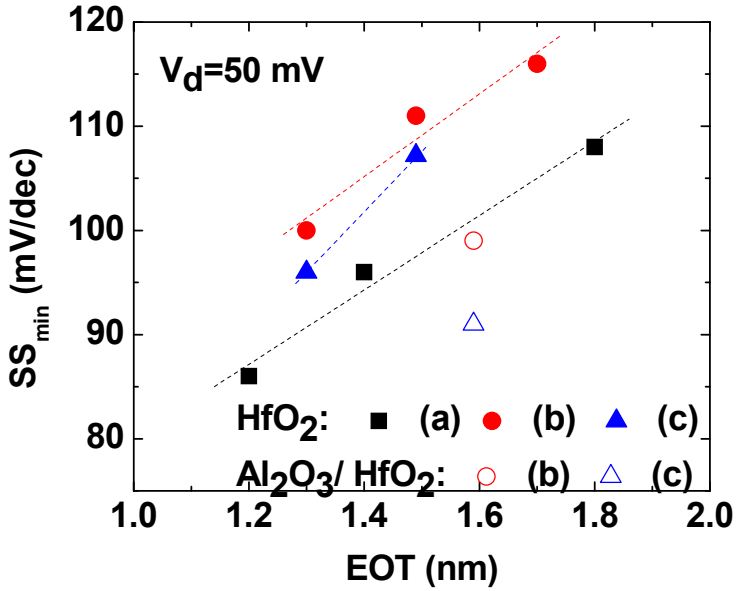

Figure 5.13 SS_{min} at V_d=0.05 V for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ TFETs with HfO_2 or Al_2O_3/HfO_2 gate oxides. (a): $In_{0.7}Ga_{0.3}As$ 6 nm/ 6 nm; (b): $In_{0.7}Ga_{0.3}As$ 4nm/ 8 nm; (c): $In_{0.53}Ga_{0.47}As$

Figure 5.12 compares the on-current for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ TFETs with HfO_2 or Al_2O_3/HfO_2 gate oxides. $In_{0.7}Ga_{0.3}As$ TFETs show a higher on-current than $In_{0.53}Ga_{0.47}As$ TFETs due to smaller bandgap. Al_2O_3/HfO_2 bilayer gate oxides do not seem to be able to effectively increase the on-current compared to HfO_2 single gate oxide for the same junction with the same EOT. This is because the on-current of TFETs depends primarily on the tunneling rate (affected by EOT) instead of the channel mobility (affected by interface quality). For $In_{0.7}Ga_{0.3}As$ TFETs, p^+ (4 nm)/ undoped (8 nm) junction provides a much higher I_{on} than p^+ (6 nm)/ undoped (6 nm) junction. This is believed to be due to a thicker undoped layer leaves a thicker effective undoped region for tunneling counting Be dopant diffusion from p^+ region thus larger tunneling current.

Figure 5.13 illustrates the minimum SS for those TFETs. Al_2O_3/HfO_2 bilayer gate oxides provide a smaller SS compared to HfO_2 single gate oxide as a result of better

InGaAs/oxide interface. $In_{0.7}Ga_{0.3}As$ TFETs using p^+ (6 nm)/ undoped (6 nm) junction show a smaller SS than $In_{0.53}Ga_{0.47}As$ TFETs due to improved tunneling efficiency from smaller bandgap. $In_{0.7}Ga_{0.3}As$ TFETs using p^+ (4 nm)/ undoped (8 nm) junction exhibit a higher SS than $In_{0.7}Ga_{0.3}As$ TFETs using p^+ (6 nm)/ undoped (6 nm) junction, this might be due to different junction doping profiles.

5.4 Vertical mode $In_{0.7}Ga_{0.3}As$ TFETs with ALD HfO_2 gate oxide

All TFETs discussed in previous sections are lateral-mode TFETs (tunneling field coming from S/D voltage), vertical-mode TFETs (tunneling field from gate voltage) with ALD HfO_2 gate oxide will be investigated in this section. Figure 5.14 plots the structure difference between lateral-mode TFETs (figure 5.14 (a)) and vertical-mode TFETs (figure 5.14 (b)) used in this chapter. In figure 5.14(b), the p^+ $In_{0.7}Ga_{0.3}As$ (8 nm, Be doping of 2×10^{19} /cm^3)/ n^+ $In_{0.7}Ga_{0.3}As$ (3 nm, Si doping of 2×10^{18} /cm^3) junction was used as the tunneling junction. The vertical tunneling was controlled by the gate and electrons tunneled to the n^+ $In_{0.7}Ga_{0.3}As$ layer were collected by the drain. The 2 nm InP layer was used as a etch-stop layer when etching the layers above the tunneling junction and removed by diluted HCl water solution afterward. The structure in figure 5.14(b) was used in our experiments rather than the ideal vertical-mode structure (figure 5.15). This is because ion implantation or secondary MBE defined lateral low-leakage p/n junction has to be formed in the ideal vertical-mode TFETs. However, for III-V materials, the ion implanted junction usually has high junction leakage [76] and a secondary MBE process is not available to us. Be noted that figure 5.15 is a simplified ideal vertical-mode TFETs structure.

Figure 5.16 illustrates the I_d-V_g and I_g-V_g characteristics of vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs using 5 nm ALD HfO_2 gate oxide. The SS (123 mV/dec) value is

much larger than the one achieved in lateral-mode TFETs (eg. 86 mV/dec). Figure 5.17 plots I_d-V_d at V_g=0 to 2.5 V for the same TFETs. They also exhibit a much lower I_{on} (12.3 μA/μm) compared to the lateral-mode TFETs in previous sections (eg. 50 μA/μm).

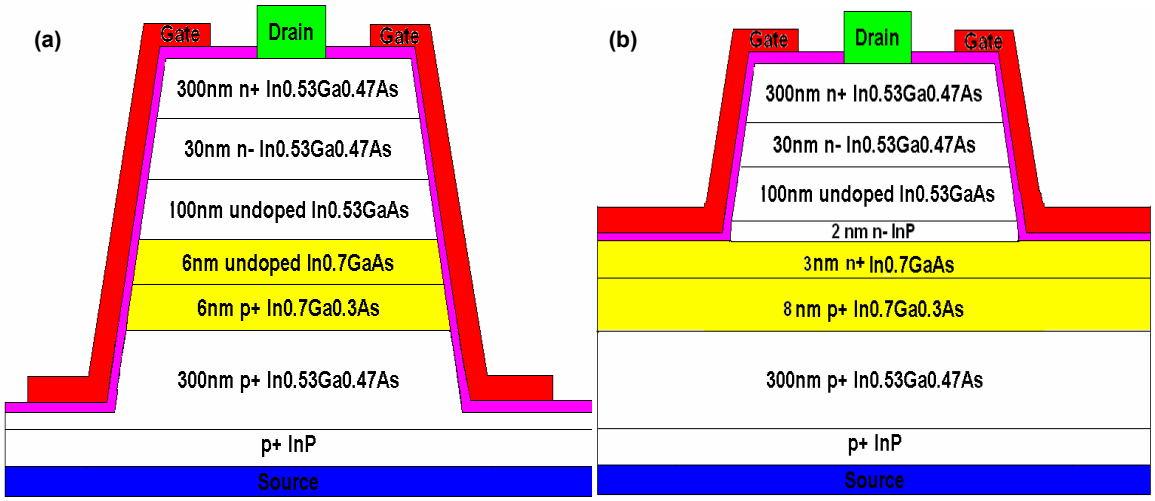

Figure 5.14 Cross-section view of lateral-mode TFETs (a) and vertical-mode TFETs (b).

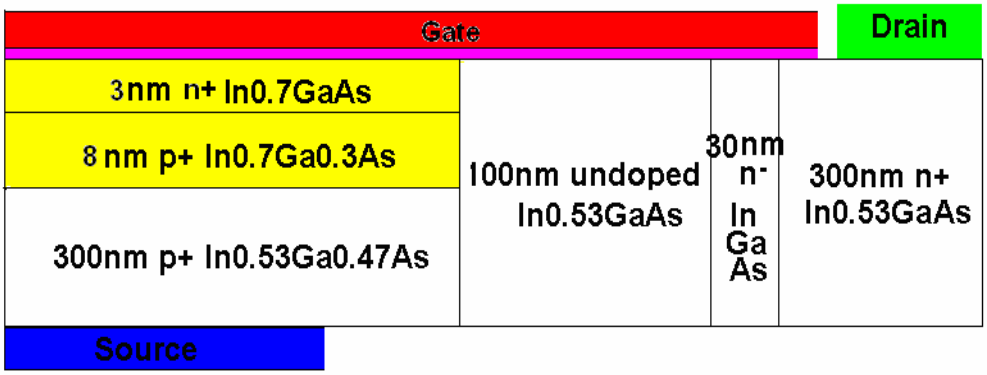

Figure 5.15 Cross-section view of ideal vertical-mode TFETs with ion implantation defined junction.

To find out the reason for the low on-current and high SS for the vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs, device characteristics of vertical-mode TFETs in figure 5.14(b) and

figure 5.15 were simulated using non-local tunneling model [109]-[110]. Figure 5.18 shows calculated electron band to band tunneling rate (a) and electron density (b) at V_g=0.6 V and V_d=0.05 V of TFETs with structure shown in figure 5.14 (b). Figure 5.19 is electron band to band tunneling rate (a) and electron density (b) of TFETs with structure shown in figure 5.15. Figure 5.19(a) illustrates a higher electron band to band tunneling rate compared to figure 5.18 (a). This is believed to be due to better electron transport using structure in figure 5.15. In figure 5.18 (b), a region of high resistance and small electron density at the gate corner can be clearly seen. This is due to drain electric field is in vertical direction and there is no lateral directional electric field to transport electrons through the corner region. This causes ineffective electron extraction by the drain and smaller electron tunneling rate at the tunneling region.

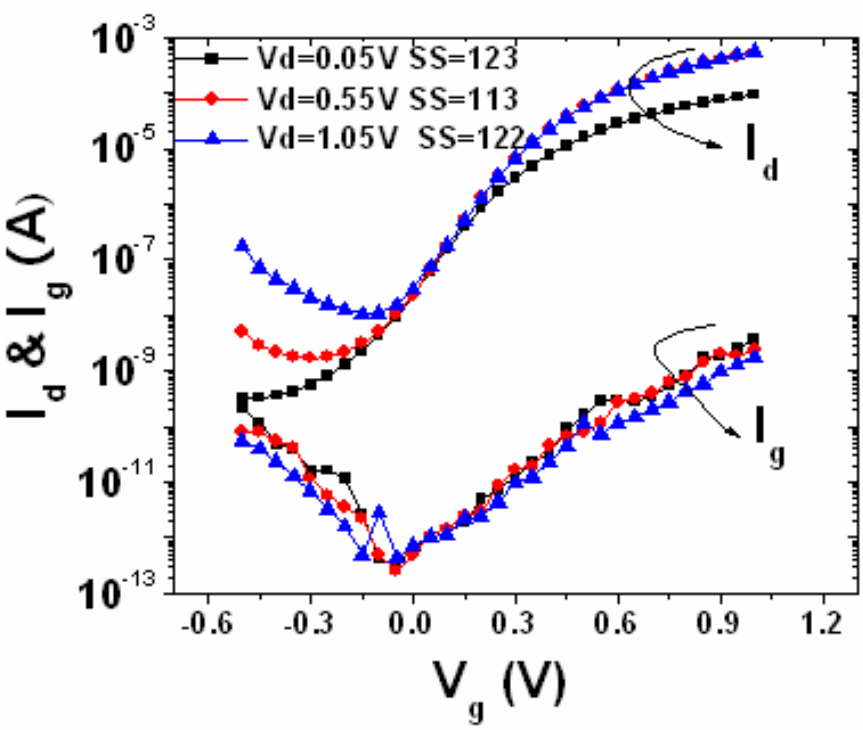

Figure 5.16 I_d-V_g and I_g-V_g characteristics of vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs using 5 nm ALD HfO_2 gate oxide (V_{th}=0.4 V).

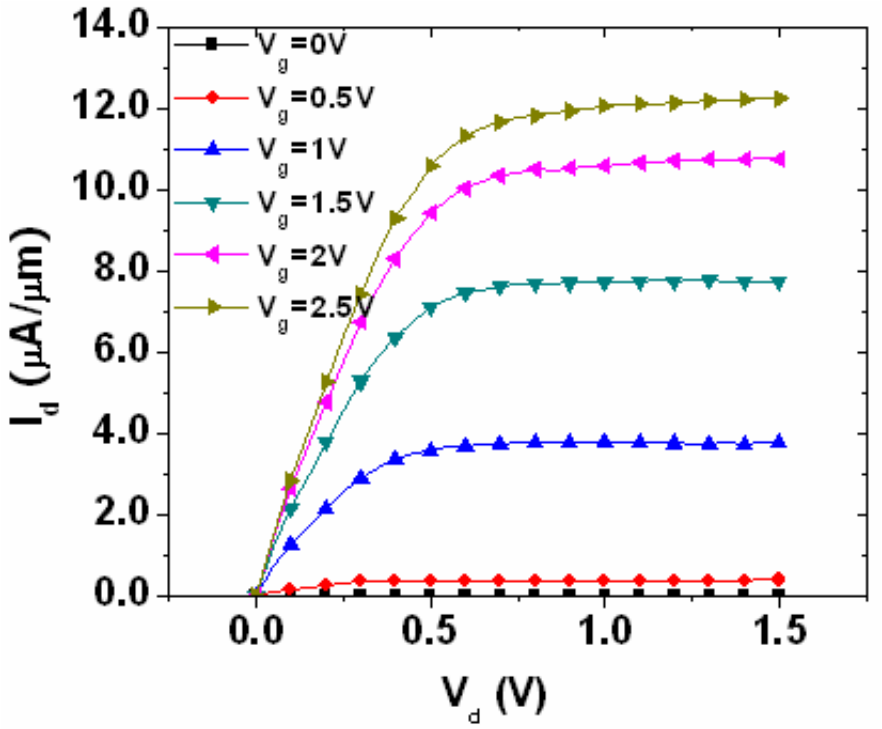

Figure 5.17 I_d-V_d curves at V_g=0 to 2.5 V of vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs using 5 nm ALD HfO_2 gate oxide.

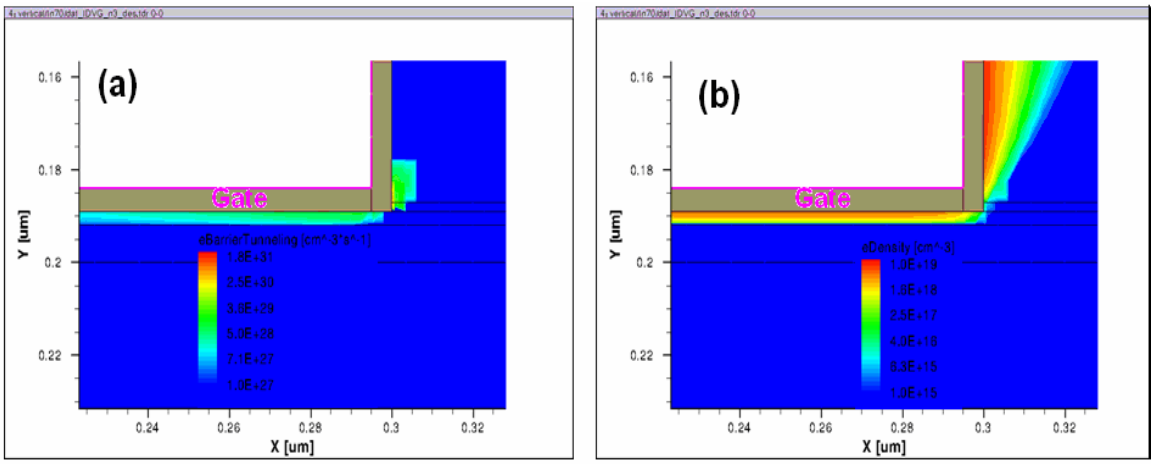

Figure 5.18 (Simulated) Electron band to band tunneling rate (a) and electron density (b) at V_g=0.6 V and V_d=0.05 V of TFETs with structure shown in figure 5.14 (b).

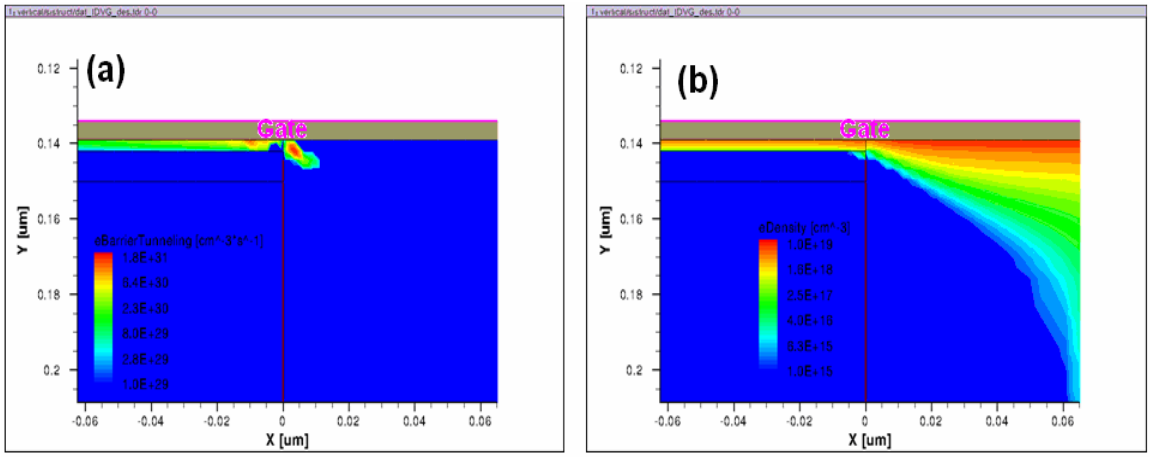

Figure 5.19 (Simulated) Electron band to band tunneling rate (a) and electron density at V_g=0.6 V and V_d=0.05 V of TFETs with structure shown in figure 5.15.

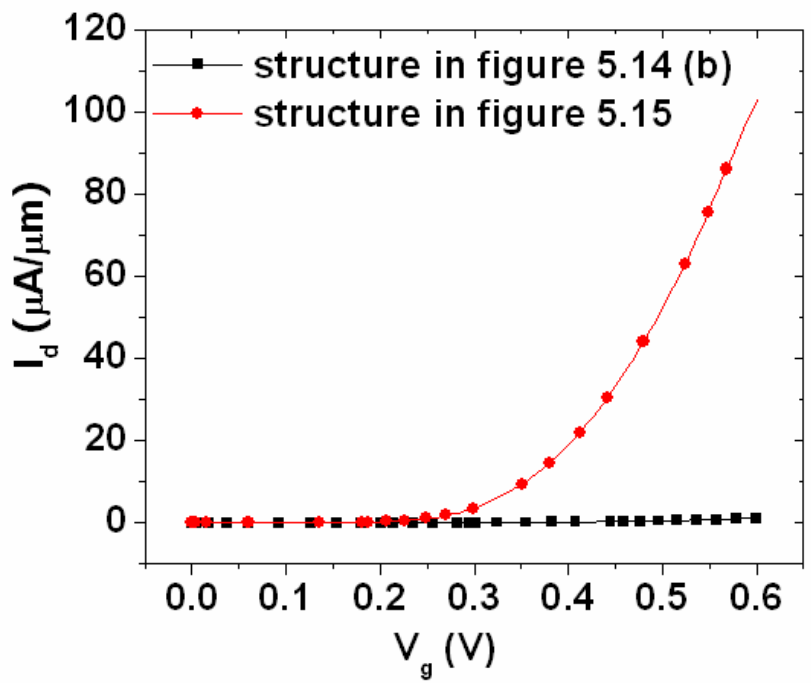

Figure 5.20 (Simulated) Linear scale I_d-V_g at V_d=0.05 V of TFETs with structure shown in figure 5.14 (b) and figure 5.15.

Figure 5.20 and figure 5.21 illustrate I_d-V_g curves calculated for TFETs with structure shown in figure 5.14 (b) and figure 5.15. With the ideal vertical-mode TFETs

structure, a much higher on-current can be achieved. This suggests that ion-implanted or MBE lateral junctions are still needed to form vertical-mode TFETs with high performance, which requires investigation on low-leakage ion implanted III-V junctions or secondary MBE lateral III-V junctions.

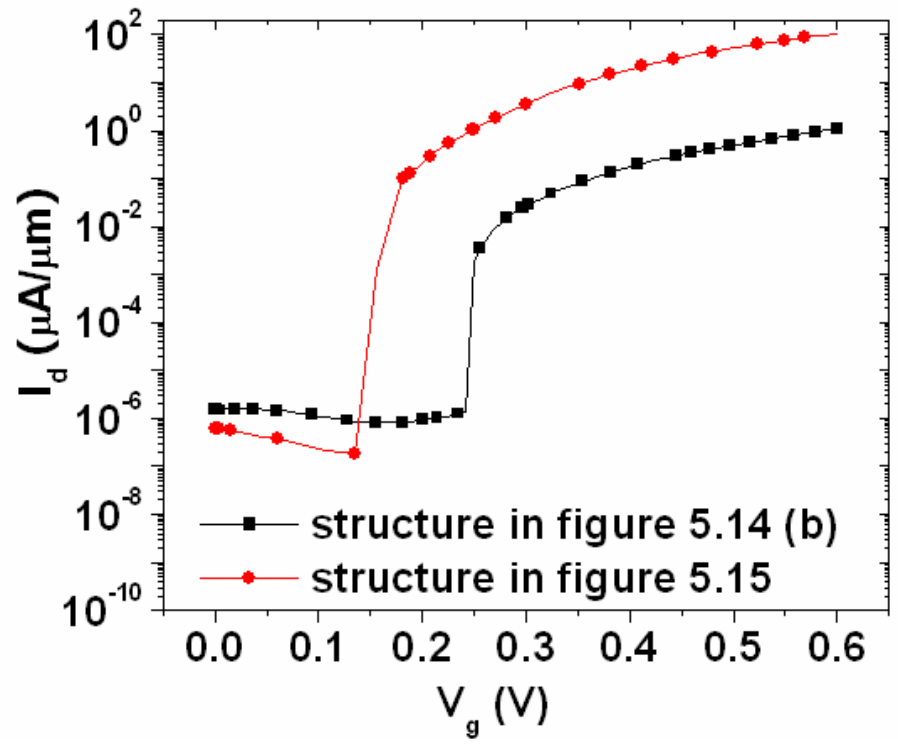

Figure 5.21 (Simulated) Log scale I_d-V_g at V_d=0.05 V of TFETs with structure shown in figure 5.14 (b) and figure 5.15.

5.5 Summary

In this chapter, InGaAs TFETs with various structures and different gate oxides have been investigated to find the optimum structures and gate stacks for TFETs with high-performance.

Firstly, lateral-mode $In_{0.7}Ga_{0.3}As$ TFETs with vertical structure have been demonstrated with a high on-current of 50 μA/μm and a minimum subthreshold swing of

86 mV/dec using ALD HfO_2 gate oxide. The tunneling diodes exhibited the gate bias dependent Esaki diode behavior with a negative differential resistance under the forward diode bias at various temperatures, which confirmed that the conduction mechanism is indeed band-to-band tunneling. The effects of EOT scaling and various temperatures on the on-current and the SS have also been investigated.

Secondly, effects of tunneling junction structure and gate oxides on lateral-mode InGaAs TFETs with vertical structure have been investigated. It has been found that $In_{0.7}Ga_{0.3}As$ TFETs with p^+ (4 nm)/ undoped (8 nm) tunneling junction provides a much higher on-current than TFETs with p^+ (6 nm)/ undoped (6 nm) junction. This is believed to be due to a thicker undoped layer leaves a thicker effective undoped layer for tunneling after dopant diffusion from p^+ region. ALD Al_2O_3/HfO_2 bilayer gate oxides provide a smaller SS compared to HfO_2 single gate oxide resulted from a better InGaAs/oxide interface. However, Al_2O_3/HfO_2 bilayer gate oxides do not show much on-current improvement compared to HfO_2 single gate oxide. This is because on-current of TFETs depends primarily on the tunneling electron density instead of the channel electron mobility.

Finally, vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs with vertical structure were fabricated but they show a much smaller on-current compared to lateral-mode $In_{0.7}Ga_{0.3}As$ TFETs with vertical structure. Simulation results indicate that the low on-current is due to the ineffective tunneling electron transportation by the vertical structure, and vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs with lateral structure would be needed to gain high on-current.

Chapter 6 Summary and future work

6.1 Summary

With the end of CMOS roadmap looming, there has been tremendous research in order to identify promising technologies to continue the historical trend of performance scaling. This thesis mainly explored the device characteristics of III-V MOSFETs and TFETs with various substrate structures and gate oxides, aiming to realize high-performance III-V devices by improving the device structures and interfaces.

Firstly, the proper fabrication process for $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD oxides has been identified by comparing device characteristics from gate-first and gate-last process. It has been found that applying the gate-last process provides significant smaller interface trap density compared to the gate-first process. This is due to the less interface oxides growth from the gate-last process in comparison with the gate-first process. By investigating the dependence of device performance on the channel doping concentration and the channel thickness for $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD Al_2O_3 dielectrics, p-type InGaAs substrates with proper doping concentration and sufficient thickness are identified to be the optimum substrates for both high drive current and small subthreshold swing. Since ALD Al_2O_3 exhibits better interface quality while ALD HfO_2 has better EOT scalability, by inserting Al contained interfacial dielectrics between HfO_2 and InGaAs substrate, device performance for InGaAs MOSFETs with ~10 Å EOT has been effectively improved including both SS and mobility.

Secondly, the buried channel InGaAs MOSFETs using single InP barrier layer with different thicknesses and $InP/In_{0.52}Al_{0.48}As$ double-barrier layer have been investigated to increase the channel mobility and drive current. InP barrier layer was found to be an effective barrier to improve the low-field mobility of $In_{0.7}Ga_{0.3}As$

MOSFETs. The InP/$In_{0.52}Al_{0.48}As$ double-barrier architecture significantly improves high-field mobility compared to same thickness single InP barrier and provide >50% improvement compared to surface channel devices.

Thirdly, a novel Ge_xN_y IPL was deposited between GaAs substrates and HfO_2 dielectric layer to improve the interface quality. Low interface state density and thin EOT have been achieved by this gate stack. Compared to Ge IPL, the Ge_xN_y IPL provides both lower slow trap density and lower trap generation rate. On the other hand, effects of S passivation and PDA on InP gate-first inversion-type MOSFETs were investigated and demonstrated to improve the drive current density and subthreshold swing. An asymmetric distribution of interface state along the bandgap between InP and ALD Al_2O_3 dielectric was identified by comparing device characteristics of MOSFETs on both SI-InP substrates and p-InP substrates.

Finally, lateral-mode $In_{0.7}Ga_{0.3}As$ TFETs with vertical-structure have been demonstrated using ALD HfO_2 gate oxide with a much higher on-current and a much smaller SS compared to reported results. By increasing the undoped $In_{0.7}Ga_{0.3}As$ layer thickness, another >80% on-current increase can be achieved. Al_2O_3/HfO_2 bilayer could effectively improve the SS but not the on-current. Vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs with vertical-structure have also been investigated. However, they show a low on-current due to the ineffective tunneling electron transportation. Vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs with lateral-structure are suggested to gain high on-current.

6.2 Suggestions for future work

6.2.1 Surface channel III-V MOSFETs

How to reduce the interface state density and improve the interface quality is always a challenge for III-V surface channel MOSFETs. ALD Al_2O_3 and MBE $GaGdO_x$

are demonstrated with low interface state density on InGaAs (high 10^{11} /cm^2/eV to high 10^{12} /cm^2/eV [105]). However, future improvement would be required for implementation of III-V surface channel MOSFETs with high mobility. Novel high-κ materials such as $LaLuO_3$ and Gd_2O_3 might have better passivation of III-V interface and their high-κ value (eg. κ value of $LaLuO_3$ is 32 [108]) is also good for future EOT scaling down. Fabricating surface channel III-V MOSFETs with those high-κ materials might be able to provide both high mobility and extremely small EOT.

The high off-current of InGaAs surface channel MOSFETs is mainly caused by junction leakage current [76], which will degrade the subthreshold characteristics and increase the power consumption. To reduce the off-current, a systematic investigation on the ion implantation process and dopant activation process for III-V materials should be conducted.

6.2.2 Buried channel III-V MOSFETs

For the buried channel III-V MOSFETs, it would be very useful to investigate the device characteristics with short channels and ultra-thin barrier layers. Since short channel devices require ultra-thin barrier layers to reduce the short channel effects, the barrier layer structure and thickness could be different from the long-channel devices. One the other hand, because the carriers should be kept outside of the barrier layer to avoid mobility degradation due to the low mobility of the barrier layer, a barrier layer with high band offset with the channel layer is preferred. When the barrier layer was made extremely thin (eg. 10- 20 Å), barriers with larger lattice mismatch but also larger conduction band offset with the channel such as AlAs can be used.

Furthermore, the process of using MBE grown n^+ S/D contact layer on the whole wafer and then etching back to expose the gate region results in high resistance between

the channel and the drain contact (~20 Ω). This would not be a big problem for long channel devices and would have negative effects on the short channel devices. To solve this problem, a secondary MBE process to form the S/D n^+ contact with a low contact resistance might be needed.

6.2.3 III-V TFETs

An abrupt tunneling junction is preferred over a junction with dopant diffusion for TFETs. Using carbon as p-type dopant rather than Be could provide shaper p^+/undoped junction interface due to its smaller thermal diffusion coefficient. Thus TFETs with higher on-current and better SS can be expected.

To fabricate vertical-mode $In_{0.7}Ga_{0.3}As$ TFETs with high performance, a lateral-structure is suggested by both the experimental and simulation results. Either secondary MBE lateral III-V p/n junctions or good ion implanted III-V p/n junctions with small junction leakage would be needed for this structure.

To really achieve III-V TFETs with high on-current and <60 mV SS, interface quality between III-V materials and gate oxides must be further improved. A new high-κ oxide with a better interface with III-V materials or surface treatment techniques such as nitridation or fluorine treatments might help.

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