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Thermal and Mechanical Analysis of Interconnect Structures in 3D Stacked Packages

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Thermal and Mechanical Analysis of Interconnect Structures in 3D Stacked Packages

by

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Dedication

To my father, for his emphasis on education

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Thermal and Mechanical Analysis of Interconnect Structures in 3D Stacked Packages

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Physical scaling limits of microelectronic devices and the need to improve electrical performance have driven significant research and development into 3D architecture. The development of die stacks in first level packaging is one of the more viable short-term options for improved performance. Placement of memory die above or below processors in a traditional flip chip C4 package with through-silicon vias (TSVs) has significant benefits in reducing data and power transmission paths. However, with the electrical performance benefits come great thermal and mechanical challenges. There are two key objectives for this work. The first is understanding of the die-die interface resistance, R_{dd}, composed of the back end of line (BEOL) layers and micro-C4 interconnects. The interfacial resistance between BEOL material layers, the impact of TSVs and the impact of strain on R_{dd} are subtopics. The second key objective is the understanding of package thermal and mechanical behavior under operating conditions, such as local thermal disturbances . To date, these topics have not been adequately addressed in the literature. It is found that R_{dd} can be affected by TSVs, and that the

interfacial contributions predicted by theoretical sub-continuum models can be significantly different than measurements. Using validated finite element models, the significance of the power distribution and R_{dd} on the temporal responses of 2D vs. 3D packages is highlighted. The results suggest local thermal hotspots can greatly exacerbate the thermal penalty due to the R_{dd} and that no peaks in stress arise in the transient period from power on to power off. .

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Chapter 1: Background and Motivation

1.1 INTRODUCTION

The ever approaching physical scaling limits of microelectronic devices and a desire to maintain electrical performance trends have driven significant research and development into 3D architecture. One of the shorter-term practical approaches for 3D microelectronics has been the development of die-stacks in first level packaging. Placement of memory die above or below processors in a traditional flip chip C4 package with through-silicon vias (TSVs) has significant benefits in reducing data transmission paths. With the electrical performance benefits, however, come great thermal and mechanical challenges. The reader is referred to an abundance of work describing the general benefits and manufacturing challenges of 3D stacked packages [1-12]. The focus of most 3D packaging related studies is the manufacturability and reliability of TSVs [13-16]. Thermo-mechanical modeling studies of 3D structures under steady state and/or uniform temperature conditions are numerous [17-23].

Figure 1.1 shows the traditional 2D flip chip package with C4-attached die on an organic laminate. The ball grid arrays (BGAs) provide I/O fan-out to the card while the backside of the die makes an ideal contact surface for a heat spreader or heat sink. The main thermal challenge for traditional 2D flip-chip packages has been to reduce the thermal interface material (TIM) resistance between die and heat spreader while maintaining reliability. Today, the TIM thermal resistance for low power, cost sensitive applications can be 100Cmm^2/W or more, while higher-end, high-power consumer applications can be 20Cmm^2/W or less.

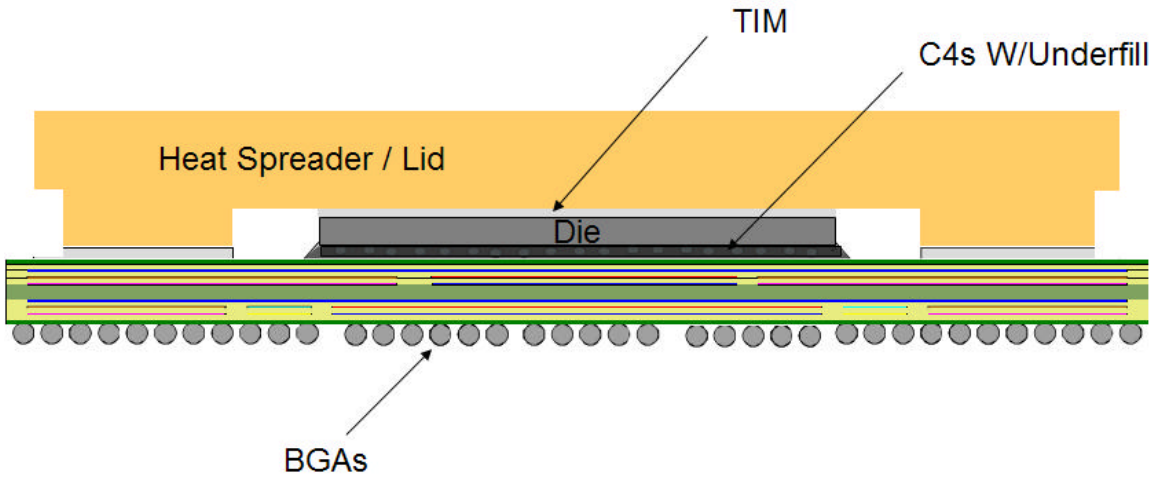


Figure 1.1 Typical 2D flip chip package.

Figure 1.2 shows a 3D stacked flip chip package, the focus of this study. The stacked package contains a thinned die in one layer, typically 100µm or less to enable through silicon via processing. The TSVs allow signal and power interconnection from the laminate to the upper die in this case. Figure 1.3 shows details of the die-die interface components, including the back end of line (BEOL) layers of the upper die and the micro-C4 interconnection between die. Although a variety of die-die bonding techniques can be used, this study will focus on the micro-C4 interconnects. Micro-C4s are similar to traditional C4s but scaled down to much smaller pitches and diameters, <100µm and <50µm, respectively. As will be shown, the additional thermal resistance of the die-die interface, (R_{dd}), can be of the same order as the TIM thermal resistance, effectively doubling the overall resistance for a two layer stack over the traditional 2D package. The impact of this additional thermal resistance is exacerbated by the non-uniform power maps of typical processors.

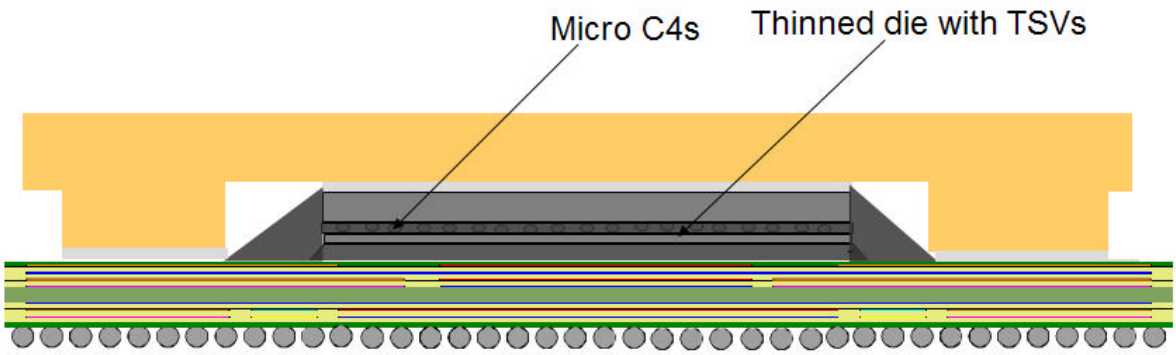


Figure 1.2 3D stacked package with thinned die on bottom containing TSVs for I/O from laminate to top die, with a micro-C4 layer in between.

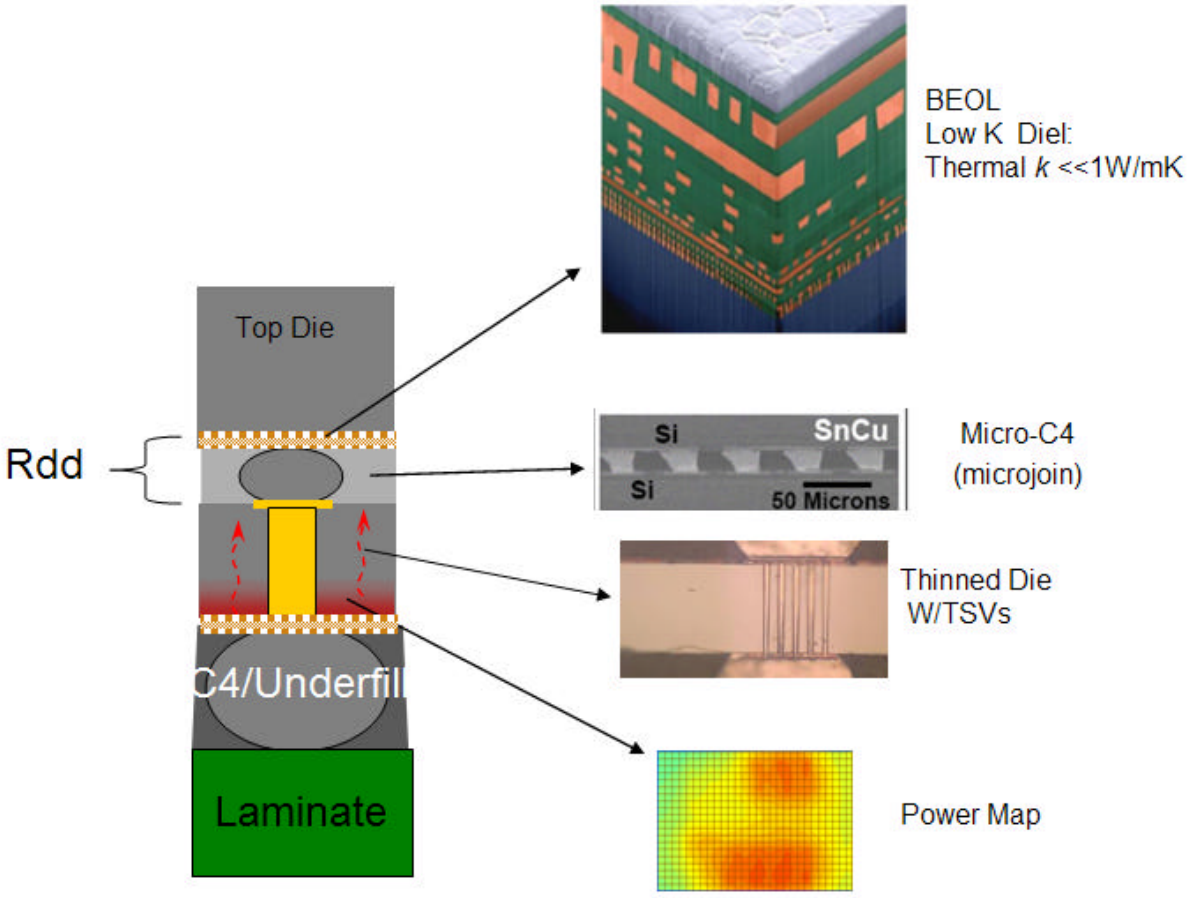


Figure 1.3 Details of stacked die-die interface components and heat transfer path from lower die.

Most of the previous thermal studies on the BEOL have focused on joule heating in interconnect structures [24-28]. Few studies have attempted to quantify the net thermal resistance increase from the lower die to the heat sink. Wakil [29] highlighted the inadequacy of simple models to accurately estimate total BEOL stack resistance without the need for detailed modeling. The conclusions of that study are summarized in Chapter 2. No known studies have evaluated the interfacial contributions of BEOL materials or the impact of strain on BEOL material conductivities. Neither have any known studies compared the transient thermo-mechanical behavior of traditional 2D and stacked-die packages under operating conditions.

1.2 Objectives and Organization of Work

The objectives of this work involve two interrelated topics. The first is understanding of the total die-die interface resistance, R_{dd}. Subtopics in this category include the impact of TSVs, contribution of interfacial resistance between BEOL material layers, and the impact of strain on the total resistance. The second main category is the understanding of the transient thermal and mechanical behavior under operating conditions with various power distributions.

The organization of the work is depicted pictorially in Figure 1.4. The next section contains a brief theoretical background of the fundamental thermal and mechanical field equations, and assumptions and simplifications used. Chapter 2 addresses the first main topic, understanding R_{dd} and its dependencies. Chapter 3 is a supporting chapter and describe the model and experimental validation. The reader can skip the validation chapter without loss of continuity, although geometry and model details will be missed. Chapter 4 describes the thermal comparison of 2D and 3D stacks, with R_{dd} as a parameter. Chapter 5 compares the mechanical behavior.

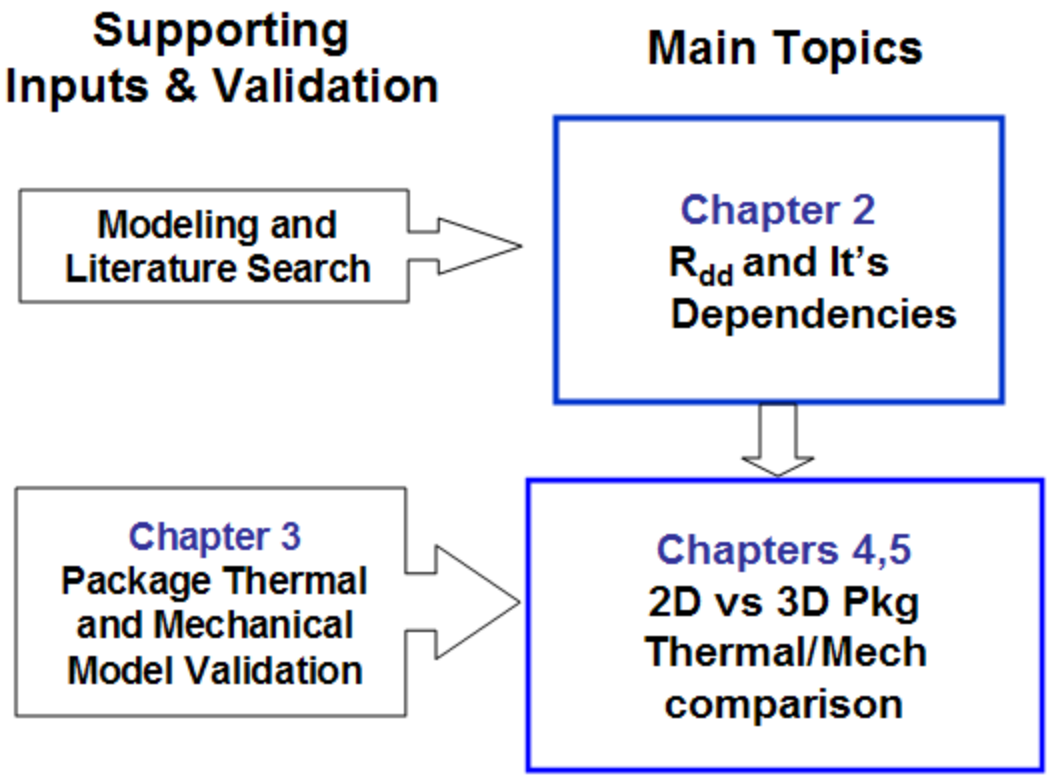


Figure 1.4 Outline of the main topics and supporting chapters.

1.3 THEORETICAL BACKGROUND

The commercially available finite element code ANSYS^{TM} was used for this work. The finite element model solves the fundamental equations for thermo-elasticity. For static analysis and isotropic materials, the fundamental equations in index notation are [11]:

Stress-strain relation;

$$\varepsilon_{ij} = \frac{(1+\nu)\sigma_{ij}}{E} - \frac{\nu\sigma_{kk}}{E}\delta_{ij} + \alpha(T - T_o)\delta_{ij} \qquad (1.1)$$

The strain-displacement relation;

$$e_{ij} = \frac{1}{2}\left(\frac{\partial(u_i)}{\partial j} + \frac{\partial(u_j)}{\partial i} \right). \qquad (1.2)$$

Heat conduction equation;

$$\frac{\P}{\P x_i}\left(\frac{\P T}{\P x_i} \right) + \frac{\dot{q}}{k} = \frac{1}{\tilde{a}} \frac{\P T}{\P t} + T_0 C \frac{\partial e_{ii}}{\partial t} \qquad (1.3)$$

Equilibrium relation;

$$\sigma_{ij,j} + F_i = 0 \qquad (1.4)$$

where: ε = total strain

σ = stress

δ = 0 if i≠j, or 1 if i=j

α = Coefficient of Thermal Expansion (CTE)

$\tilde{a}$ = thermal diffusivity

T = T(x,y,z) = temperature field

T_o = T_o(x,y,z)=reference temperature field

ν = Poisson ratio

E = Young's modulus

u = displacement

k = thermal conductivity

q = heat generation

C = material constant

F = force

The last term in (1.3) is the temperature-strain coupling term (where C is a constant related to the material elastic constants and thermal conductivity). The coupling term represents viscous energy dissipation and is typically neglected if the strain/deformation rate is sufficiently small (less than speed of sound in the material). This assumption will be used, and its validity addressed when analyzing the final results. The temperature field can thus be solved independently. The thermo-elasticity problem then involves finding sixteen unknowns: σ_{ij}, $\varepsilon_{ij,}$ u_i, T, using eqs. (1.1-1.4) (which give sixteen relations) along with appropriate boundary conditions. Appropriate thermal boundary conditions for the current analysis are heat transfer coefficients on package and card surfaces determined from validation experiments. Mechanical boundary conditions include surfaces with heat sink loads or free surfaces. More details of the modeling and boundary conditions used will be given in the model validation Chapter 3 and with analysis of each topic.

Chapter 2: BEOL and Micro-C4 Resistance, R_{dd}

2.1 INTRODUCTION

As mentioned in Chapter 1, much of the previous thermal analysis on back end of line (BEOL) structures has been focused on the Joule heating within interconnect structures. A new concern that has arisen with the advent of 3D flip chip stack packages is the additional thru-plane thermal resistance created by the BEOL and die-die interconnect layer in the primary heat flow path of the lower die, as shown in Figure 2.1. The figure shows a worst case scenario where a high-power processor is placed below the memory die, which contacts the heat sink. There is now an additional resistance due to the BEOL of the upper die and interconnects between the die, which for this study are assumed to be micro-C4s. The objective of this chapter is to identify and quantify the subcomponents of this die-die resistance (R_{dd}), and its influencing parameters.

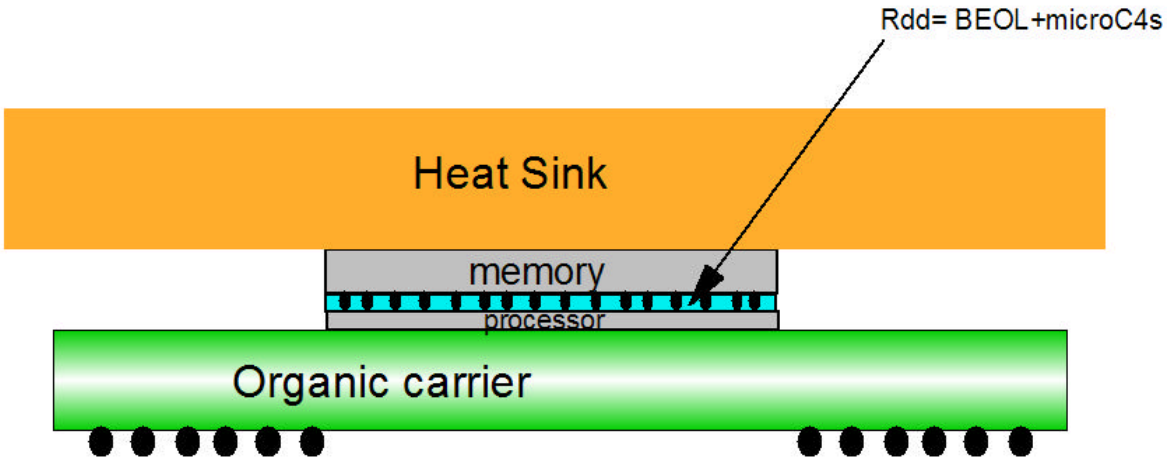


Figure 2.1. Schematic of 3D stacked flip chip package with high power processor below memory.

2.2 BEOL THRU-PLANE THERMAL RESISTANCE

A previous study by the author [29] attempted to quantify the BEOL thermal resistance and address the dependence of the effective thermal resistance of the structures on the geometric details of the BEOL structures. A four layer BEOL as shown in Figure 2.2 was modeled using finite elements. The structure of the interconnect lines and vias were varied, keeping material properties constant. Eleven different designs were modeled, the results of which are shown in Table 2.1. The total metal fraction as well as the metal fraction for the line and via layers are specified. Of particular interest were cases in which the metal fractions were the same but gave different thermal resistances based on the via/line placements (i.e. cases A2 and B2).

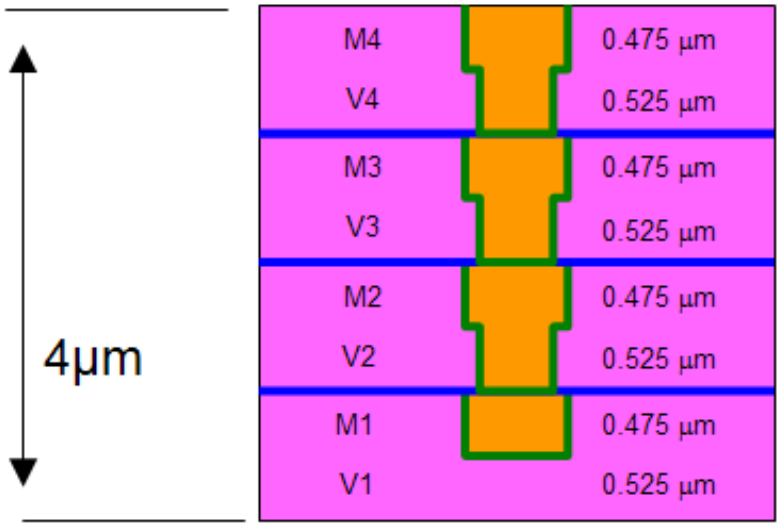


Figure 2.2. Four layer pair BEOL modeled to evaluate effective thermal resistance of the stack for different geometries and metal fractions. From [29].

Table 2.1. Thermal resistance of four layer BEOL for different configurations of vias and lines. k_{diel}=0.54W/mK, k_{met}=380W/mK. From [29].

Case	Via Desc	Lines/Space	Metal fraction: Total / Line layer / via layer	%Via Area	Out of Plane Resistance
A1	Stacked	0.28/0.28um	0.239/.5/.0031	0.31	2.9 Cmm²/W
A2	Stacked	0.28/0.28um	0.262/.5/.0625	6.25	1.2
B1	Connected staggered	0.28/0.28um	0.239/.5L/.0031	0.31	2.6
B2	Connected staggered	0.28/0.28um	0.262/.5/.0625	6.25	1.3
C1	Isolated staggered	0.28/0.28um	0.239/.5/.0031	0.31	3.6
C2	Isolated staggered	0.28/0.28um	0.262/.5/.0625	6.25	1.8
D1	Isolated staggered	0.28/1.4um	0.081/.167/.0031	0.31	4.9
E1	No vias	0.28/1.4um	0.079/.167/0	NA	5.7
E2	No vias	0.28/0.28um	0.239/.5/0	NA	4.1
F1	Stacked (small spacing)	0.28/0.28um	0.24/.5/.0069	0.69	2.9
F2	Stacked (larger spacing)	0.28/0.28um	0.24/.5/.0069	0.69	3.0

The FEM results were compared to approximations using the Maxwell model [31] eq. (2.1) and the parallel series approximation eq. (2.2).

$$\frac{k_{eff}}{k_a} = C_o + C_1\Phi_b + C_2\Phi_b^2 + C_3\Phi_b^3 + ... \tag{2.1}$$

$$\left(L/k\right)_{eff} \approx N\left(\frac{L_{lines}}{\Phi_{lines}^{met} k_{lines}^{met} + \Phi_{lines}^{diel} k_{lines}^{diel}}\right) + V\left(\frac{L_{vias}}{\Phi_{vias}^{met} k_{vias}^{met} + \Phi_{vias}^{diel} k_{vias}^{diel}}\right) \tag{2.2}$$

where Φ is the volume fraction, k the conductivity, N the number of line layers and V the number of via layers, L, the thickness of respective layers. The Maxwell model constants *C1*, *C2* were obtained from calibration with finite element results and were thus

inherently design specific, whereas the parallel/series approximation used no design information.

Figure 2.3 plots the percent error from the FEM results for the thermal resistances calculated by the Maxwell model (eq 2.1) and the parallel/series approximation (eq. 2.2). The results suggested simple averaging schemes without accounting for actual geometric details would not be sufficiently accurate.

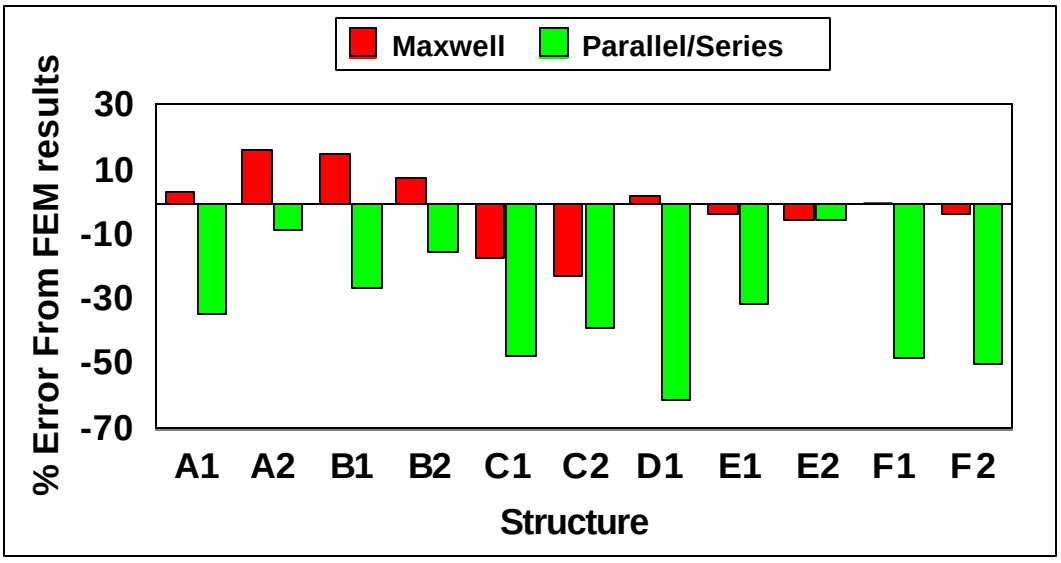


Figure 2.3. Percent error from FEM results for the Maxwell and Parallel/Series models

5.3 MICRO-C4 THERMAL RESISTANCE

The micro-C4 joint is similar to traditional C4 solder joint technology except scaled down to meet electrical I/O requirements. The joints can be encapsulated in underfill epoxy for improved cycling reliability. Previous thermal studies of micro C4s are limited but include Lloyd [32] who measured thermal conductivity and diffusivity of lead free solder using an iterative inverse method. Szekely [33] used structure functions for a cylindrical heat propagation scenario to model solder joint heat propagation.

The ANSYS^{TM} software was used to model a micro-C4 unit cell. The objective was to compare FEM results to a parallel/series resistance model. The ANSYS conduction model is shown in Figure 2.4. The model consisted of a single solder joint and surrounding underfill layer. Also modeled were 5µm layers with effective conductivities of 15.0 (W/mK) in-plane, and 1.0 thru-plane which represented BEOL layers on prescribed sides of the joint. For the face-to-face joining condition (in which the active sides of each die would be facing each other) the BEOL was modeled on each side of the joint. For the face-to-back condition (in which the active side of one die would be attached to the back of the other), the BEOL was modeled on only one side of the joint. A no-BEOL case was also modeled. 100µm of Silicon was modeled to represent the die on each side of the joint. The thermal resistance of the micro-C4 layer was calculated by finding the total resistance of the structure, and then subtracting the Silicon and BEOL contributions. For comparison, the parallel resistance model results were obtained by using the one-layer version of eq. (2.2).

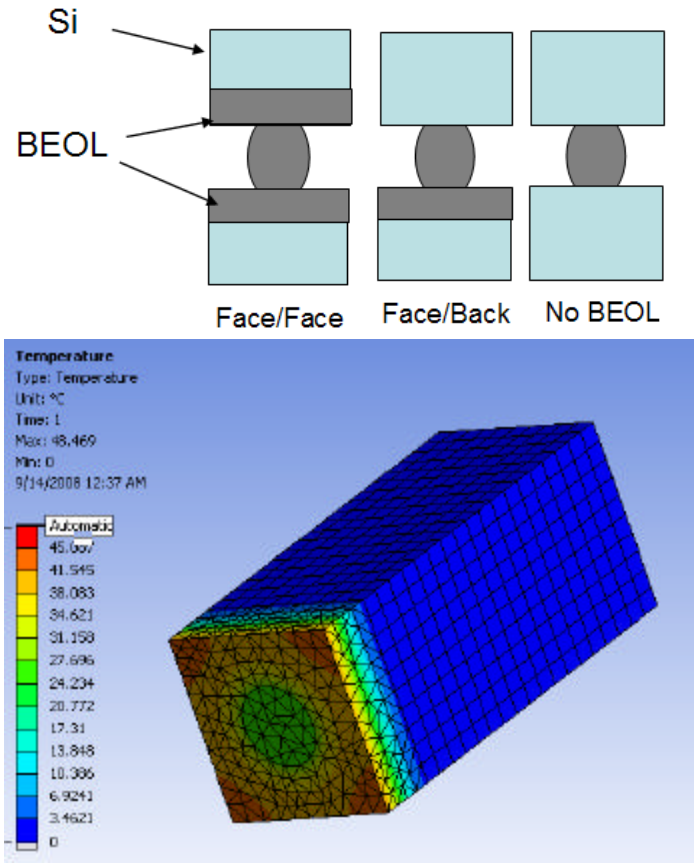
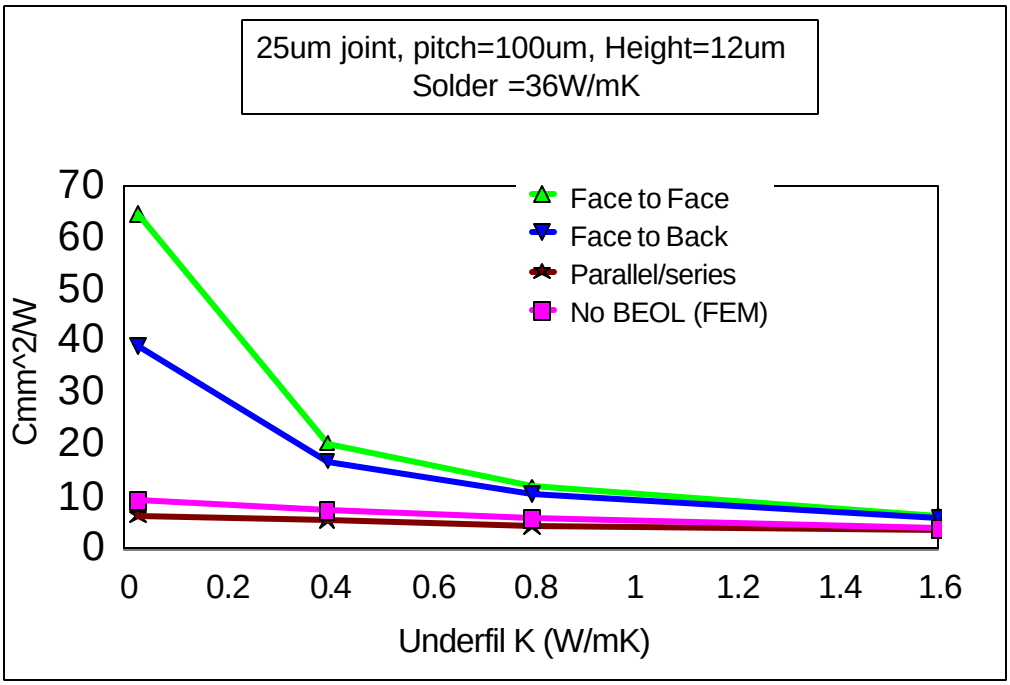
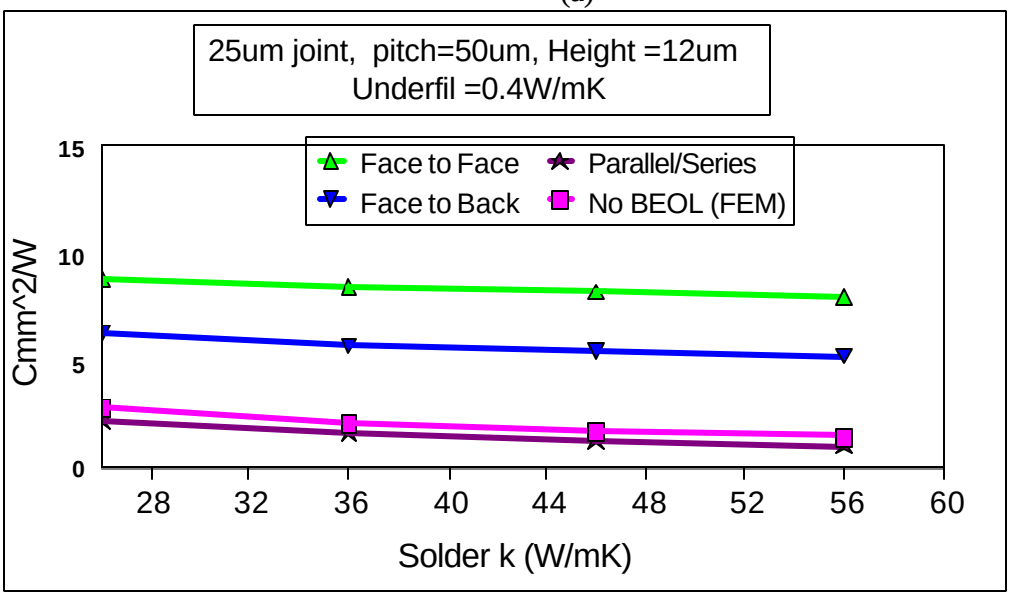


Figure 2.4. Structures modeled (top) and ANSYS^{TM} thermal conduction model (bottom) of a micro-C4 unit cell, showing one side of the model.

Figure 2.5 shows plots of the micro-C4 thermal resistance as a function of underfill conductivity (a) and solder joint conductivity (b) for 100µm and 50µm pitches, respectively, with 25µm diameter joints, 12µm tall. Also compared are the no-BEOL case, and the parallel/series approximations which obviously do not consider the surrounding BEOL. The results reveal significant difference between the face-to-face, face-to-back, and no BEOL configurations. It can be concluded that the BEOL adjacent to the micro-C4s greatly impacts the results due to spreading resistance and that independent analysis of the micro-C4 and BEOL is not possible. Subsequent analysis will include the BEOL and micro-C4 layer resistance together as R_{dd} (die-die resistance).



(a)



(b)

Figure 2.5. Micro-C4 layer thermal resistance as a function of underfill conductivity (a), solder conductivity (b), and micro-C4 pitch for the face to face and face to back BEOL configurations.

2.4 IMPACTS OF THROUGH-SILICON VIAS (TSVS)

An important design feature that affects BEOL and micro-C4 thermal resistance is the through-silicon via (TSV). TSVs are designed for power delivery or signal I/O and can penetrate one or more layers of the BEOL as well as the bulk Silicon, as shown in Figure 2.6. The goal of this section is to determine the impact of Cu TSVs on R_{dd}. As concluded from the previous section, micro-C4 thermal resistance is strongly dependent on the adjacent BEOL resistance and therefore the two features cannot be analyzed separately.

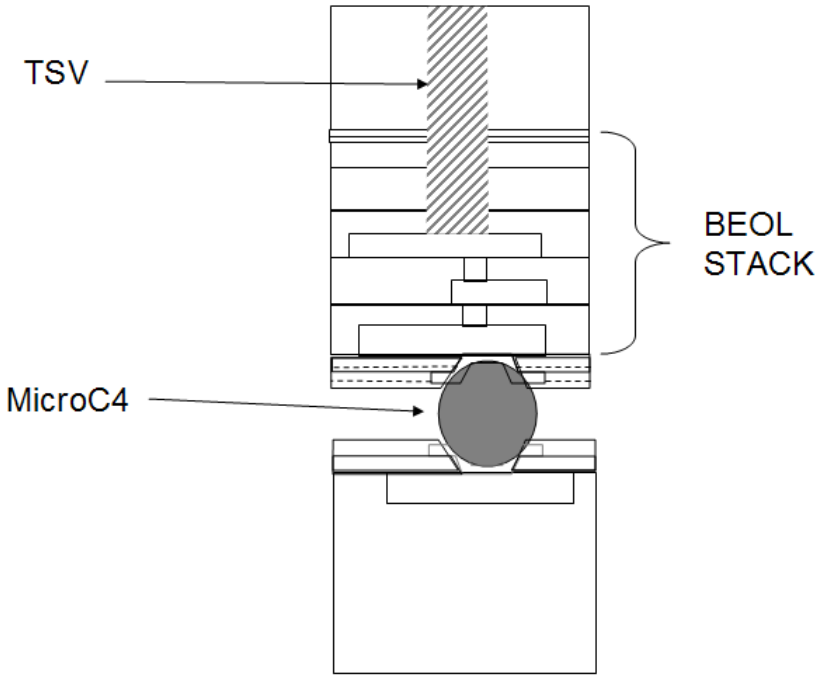


Figure 2.6. Example die stack with micro-C4 and TSV penetrating a portion of the BEOL stack.

A simple four-layer BEOL with micro-C4 layer was modeled in ANSYS as shown in Figure 2.7. The model was used to compare the four layer BEOL with TSVs

penetrating various numbers of layers and aligned with the miroC4 vs. non-aligned. Additional Si layers were modeled upon which heat source and heat sink boundary conditions were applied. The resistance of these silicon layers was subtracted from the total to get the BEOL+micro-C4 composite resistance, R_{dd}. This geometry would be representative of a face-to-back design described in the previous section.

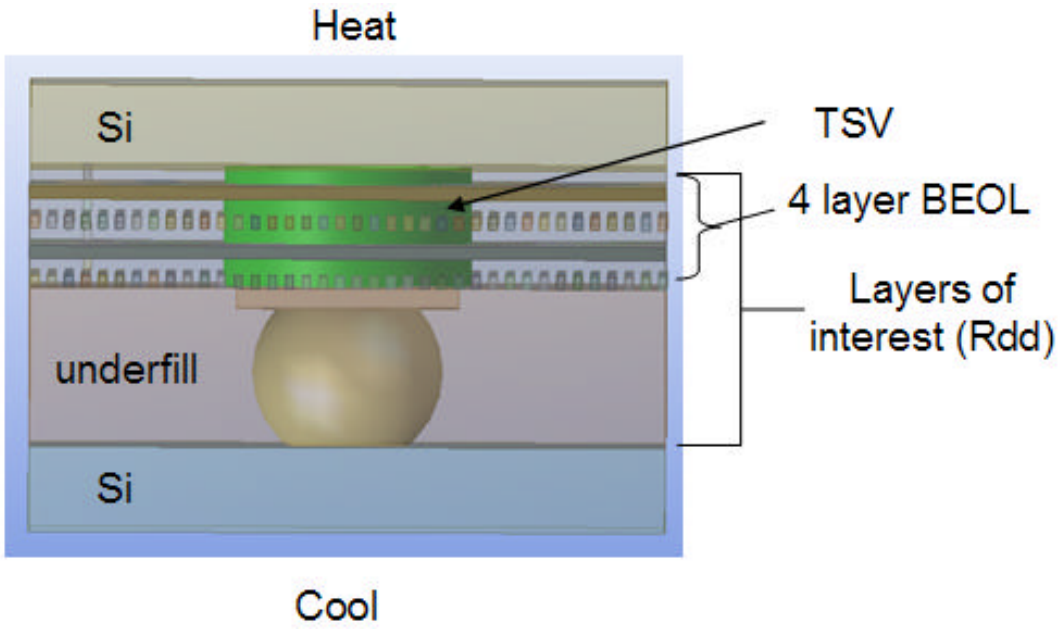


Figure 2.7. BEOL and micro-C4 model used to evaluate the effect of TSVs.

Figure 2.8 shows R_{dd} as a function of the TSV pitch. The micro-C4s (also referred to as microjoins or ujoins) are assumed 14µm tall, 18µm in diameter, with an underfill conductivity of 1 w/mK. The TSVs are assumed to be not directly aligned with the micro-C4s. The legend designates the scale of lines/spaces modeled and the number of layers the TSV penetrates. 8X-1L designates 8X scale layers with one layer of TSV penetration. The table above the figure shows the dimensions used for 8X and 2X scale lines. The dots indicate the infinite TSV pitch (no TSVs). The first observation from Figure 2.8 is that the TSV pitch primarily affects the larger 8X layer structures. The

second observation is that beyond ~150µm pitch, the TSVs become basically ineffective in providing thermal enhancement

	Line/space (µm)	Line height (µm)	Via layer height (µm)
8X	0.8	1.2	1.6
2X	0.14	0.25	0.25

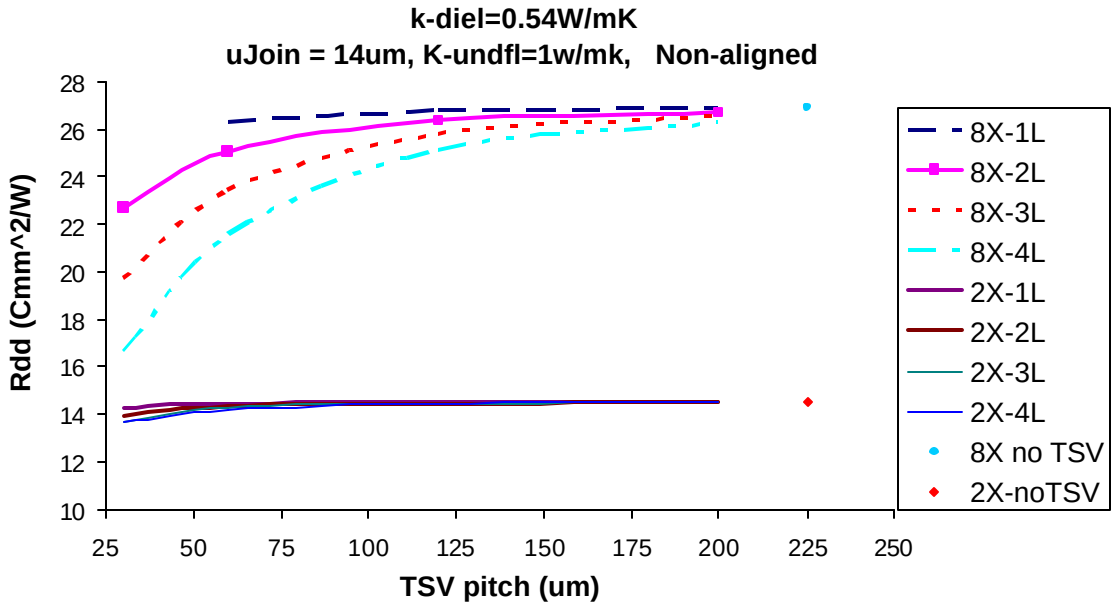


Figure 2.8. BEOL + micro-C4 thermal resistance (R_{dd}) as a function of TSV pitch for TSVs not aligned with the micro-C4s.

Figure 2.9 shows R_{dd} as a function of the dielectric thermal conductivity with 8X layers, 200µm TSV pitch and 14µm micro-C4 height with 1 W/mK underfill conductivity. The TSVs are non-aligned with the micro-C4s. The three curves compare TSV through all four layers, no TSV but with 5% area microvias connecting the layers, and no TSV nor vias. The main conclusion from Figure 2.9 is that 5% microvias without TSVs is significantly better than having TSVs at this large pitch. It must be noted that

the TSV at 200um pitch equates to less than 1% Cu. The second observation is that the dielectric conductivity in this range has minimal affect on the structures with 5% vias.

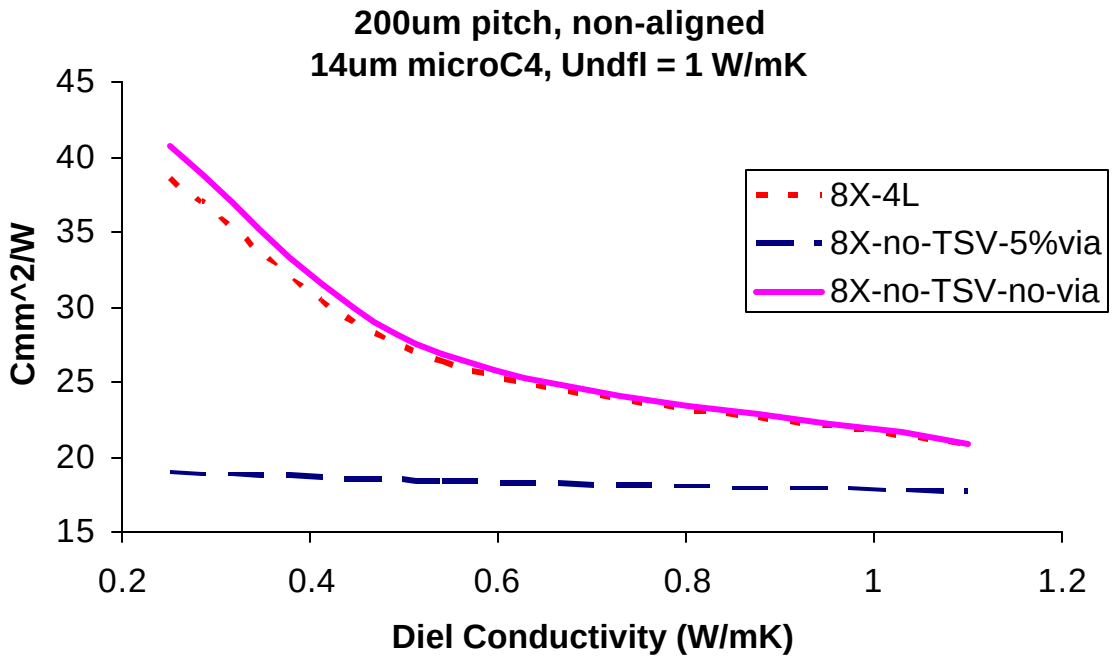


Figure 2.9. BEOL+micro-C4 thermal resistance (R_{dd}) as a function of dielectric conductivity for 200µm TSV pitch, with 14µm tall micro-C4s and underfill conductivity of 1W/mK.

Figures 2.10 and 2.11 compare aligned (with micro-C4) vs. non-aligned TSVs for two and four layer TSV penetrations, for 200µm and 30µm TSV pitches, respectively. The main observation is that the four layer penetration aligned TSV is the only significantly different result. At the larger pitch, all the non-fully-penetrated TSV structures are approximately the same regardless whether aligned or not. The difference is more obvious for the smaller pitch of Figure 2.11. Here, one can see that the aligned cases have lower resistance than the non-aligned..

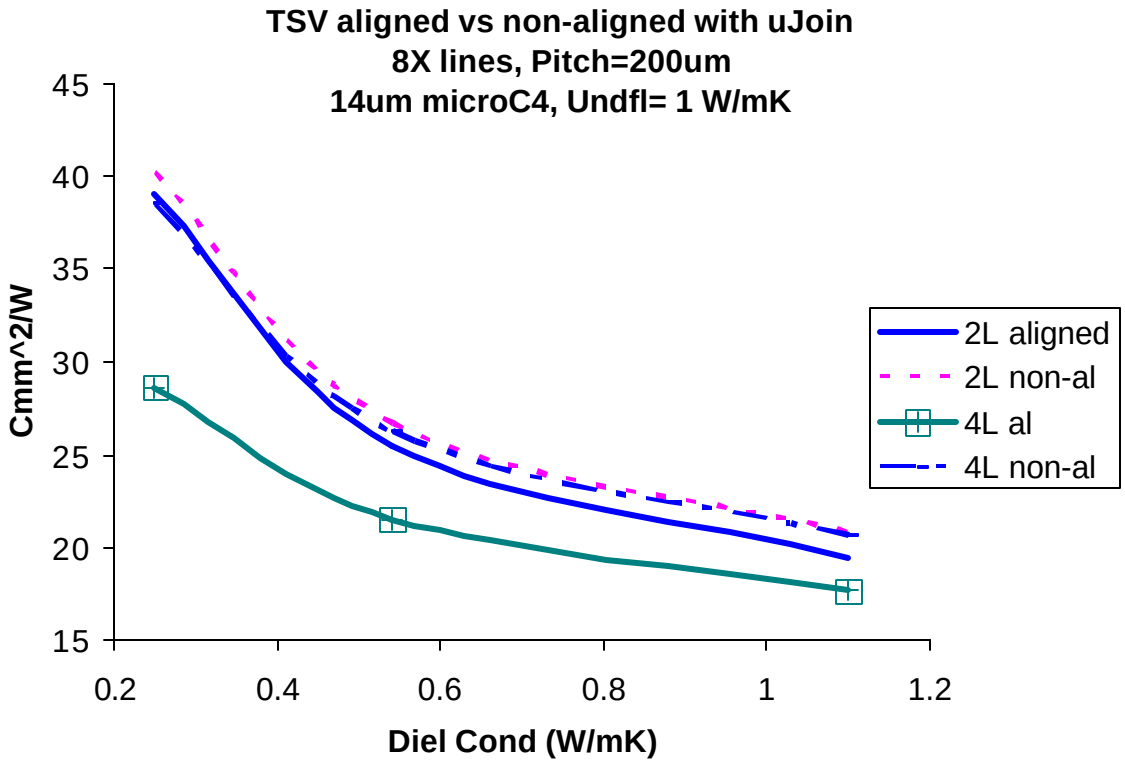


Figure 2.10. BEOL+ micro-C4 thermal resistance (R_{dd}) as a function of dielectric conductivity for 200µm TSV pitch, with 14µm tall micro-C4s and underfill conductivity of 1W/mK.

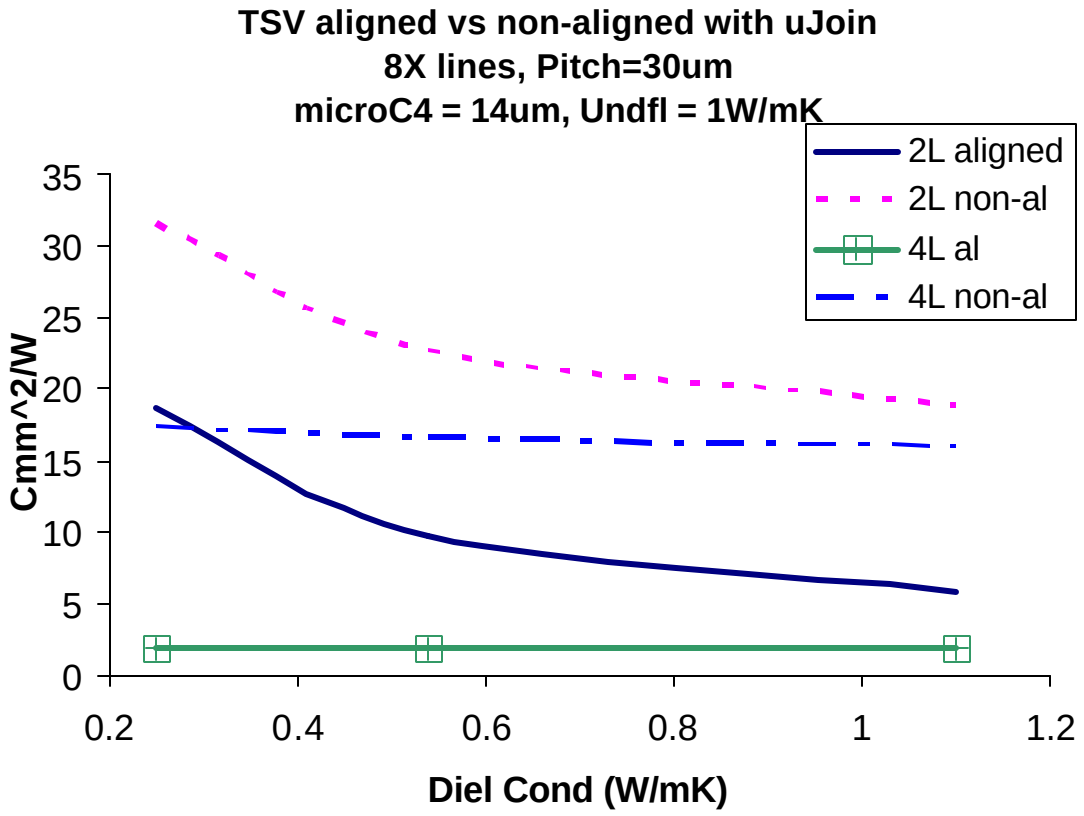


Figure 2.11. BEOL+micro-C4 thermal resistance (R_{dd}) as a function of dielectric conductivity for 30µm TSV pitch, with 14µm tall micro-C4s and underfill conductivity of 1W/mK.

As a rough comparison with the results of Figures 2.8-2.11, measurements were made on a stacked test vehicle containing two die, with an interface consisting of 200µm pitch, 70µm tall underfilled C4 joints. Figure 2.12 shows the test vehicle and cross section revealing the die stack (more details of the thermal measurements will be given in Chapter 3 as part of the package macro model validation). The BEOL of the top die was a five-layer stack, consisting of two 10X and 2X layers; and one 1X, containing no TSVs. The lower die contained heaters and sensors which could be powered to measure temperatures on the lower die, and a thermocouple to measure the lid temperature. By

measuring the two-die stack chip-to-lid resistance and comparing to a single die layer package with the same thermal interface material (TIM) bond line, it was possible to extract the R_{dd}. The results revealed $R_{dd} \simeq 95 Cmm^2/W$. Assuming the C4 layer comprised a majority of the R_{dd} resistance and linearly extrapolating to 14µm layer height resulted in ~$19 Cmm^2/W$ for R_{dd}. This is consistent with results shown in Figures 2.8 and 2.9, for no TSV (or very large pitch), with underfill and dielectric conductivities in the ranges analyzed.

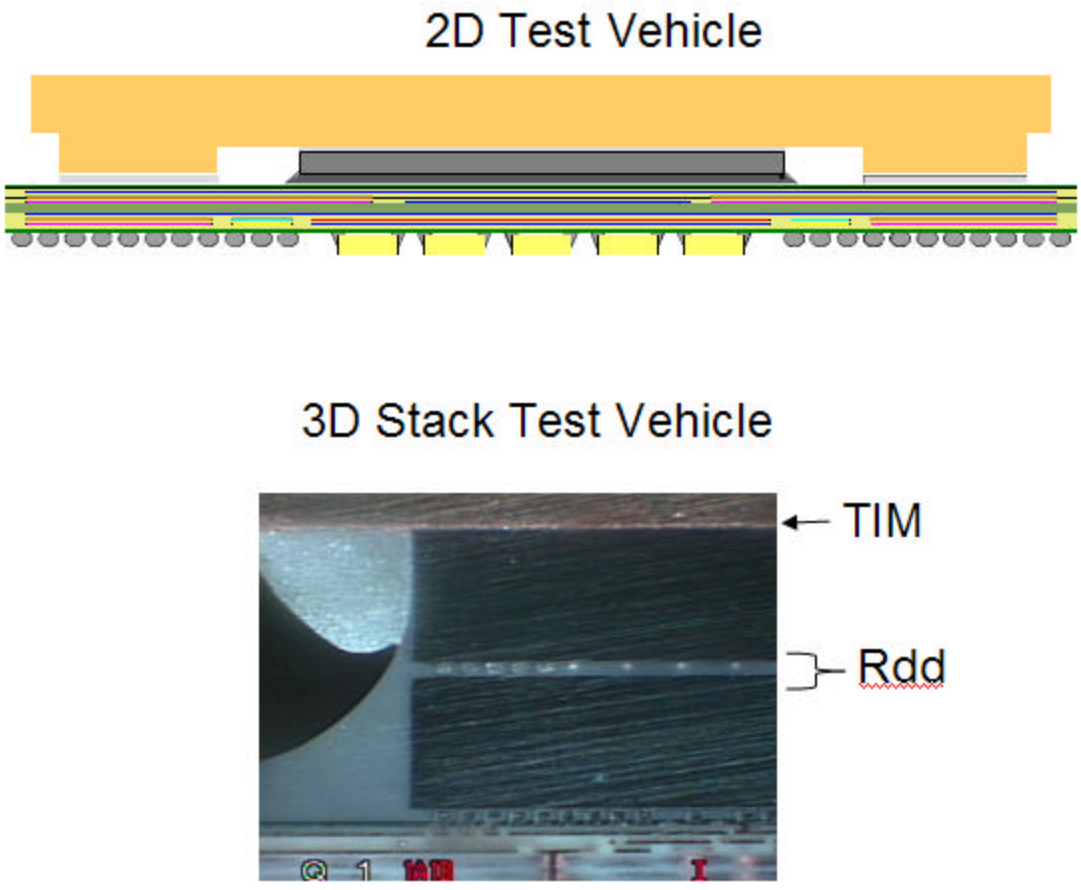


Figure 2.12. 2D test vehicle and cross section of 3D stack test vehicle used to extract R_{dd} for 70µm tall C4s, 200µm pitch with underfill.

2.5 INTERFACIAL RESISTANCE CONTRIBUTION

Implicit in the previous sections was that the interfacial resistances between material layers, especially the many BEOL layers, were negligibly small. The thermal resistance at the interface of dissimilar materials has long been a focus of study by researchers. Examples include Kanuparthi [34] who attempted to decipher the thermal resistance contributions from interfacial and particle randomness in thermal interface materials by using a hierarchal meshless analysis method. It was concluded that the particle randomness and distribution played a more significant role than interfacial resistances. Nan [35] looked at SiC composites with whiskers and measured total effective resistance, from which the individual resistance components were back-calculated. The interfacial resistance component was bounded to be roughly 0.001 to 0.1 Cmm^2/W. Molecular dynamics based studies include Yang [36] who used a coupled molecular dynamics/finite element method to model the interfacial and continuum characteristics at an interface. Wang [37] used the diffuse mismatch model (DMM) to look at 1250 different material interfaces. The results ranged from 0.001 to 0.1Cmm^2/W for most cases. The interfacial resistances correlated with the ratios of average material sound velocities. Figure 2.13 plots the interfacial thermal resistances as a function of the ratio of average sound velocities of the mating materials. It must be noted that the diffuse mismatch model is a rough approximation and is in fact not valid for interfaces between very similar materials.

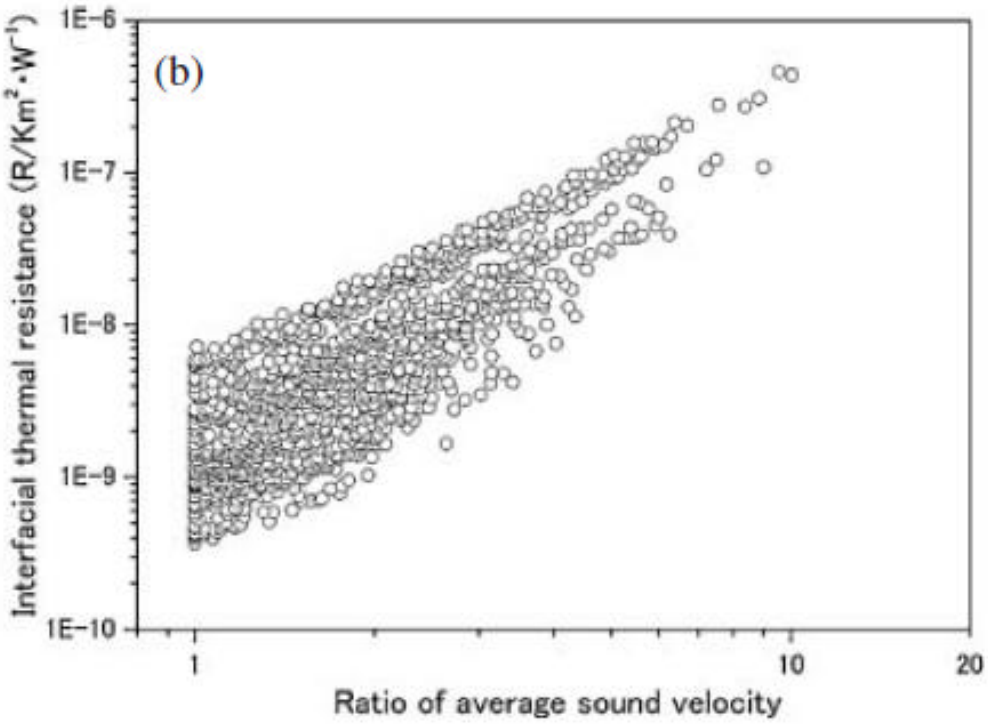


Figure 2.13. Interfacial thermal resistance as a function of ratio of average sound velocities for various material pairs. Reprinted with permission from [37].

It was attempted to use the relationship developed by Wang to estimate the interface resistance of typical BEOL material pairs. The results are shown in Figure 2.14. The left axis shows the ratio of sound velocities for the material pairs, and the right axes shows the interface resistance using the sound velocity ratio relationship of Wang. The materials listed are typical BEOL materials used in sub 90nm device generations, including low-k dielectrics and barrier layers. The sound velocities were calculated as follows:

$$u_{avg} = \frac{u_L + 2u_T}{3}$$
$$u_L = \sqrt{\frac{C_{11}}{r}} \quad , \quad u_T = \sqrt{\frac{C_{44}}{r}} \qquad (2.3)$$

where *C11, C44* and r are the Young's modulus, shear modulus and density of the material, respectively. Based on Figure 2.13 the uncertainties can be as high as an order of magnitude for the lower sound velocity ratios.

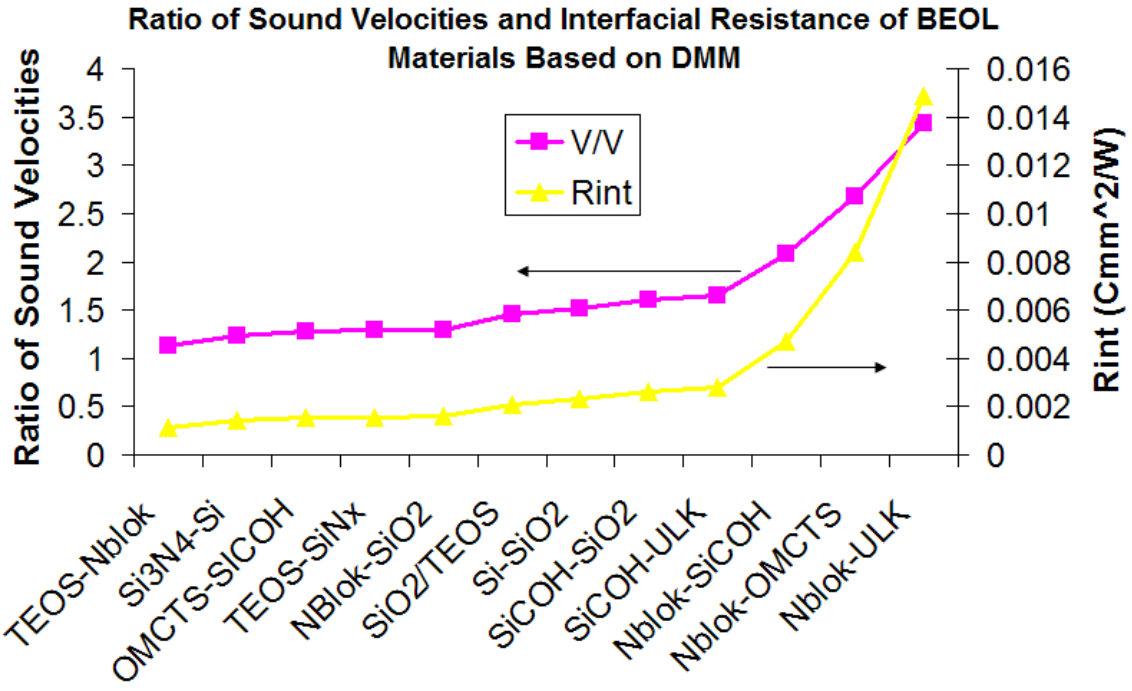


Figure 2.14. Ratio of sound velocities (left axes) and interface resistance (right axes) for common BEOL material pairs estimated using the $R_{interface}$-to-sound velocity ratio relationship of Wang [37]

Table 2.2 shows the numbers of such interfaces in a typical IBM BEOL stack and the value of the total interfacial thermal resistance contribution of a stack in a sub-90nm generation microelectronic technology. The number of interfaces and estimated resistance per interface are shown. As can be seen, the total theoretical interfacial

contribution (~0.17Cmm^2/W) is quite small relative to the thermal resistance values discussed in the previous sections.

Table 2.2. Number of interfaces and interface resistances per interface for a typical 90nm BEOL stack.

Interfaces	# interfs.	Rint per interface (Cmm^2/W)
TEOS-Nblok	6	0.001156
OMCTS-SICOH	1	0.001563
TEOS-Si_3N_4	1	0.001569
NBlok-SiO2	4	0.001592
SiO2/TEOS	1	0.002089
SiCOH-SiO_2	4	0.00261
SiCOH-ULK	7	0.002783
Nblok-SiCOH	1	0.004715
Nblok-OMCTS	1	0.008365
Nblok-ULK	7	0.014891
Total resistance		~0.17

Another method to estimate the interfacial thermal resistance is extrapolation of resistance vs. film thickness measurements as was done by Lambropoulos [38] who summarizes thermal conductivity measurements of thin films. Figure 2.15 shows the thermal conductivity of oxide films as a function of thickness, summarized from other sources by Lambropoulos. The interfacial resistances are quite large for SiO_2 to Si and Si_3N_4 to Si (>2Cmm^2/W). These values are roughly three orders of magnitude larger than the theoretical values shown in Figure 2.13 based on the DMM methodology and suggest significant imperfections at the interface.

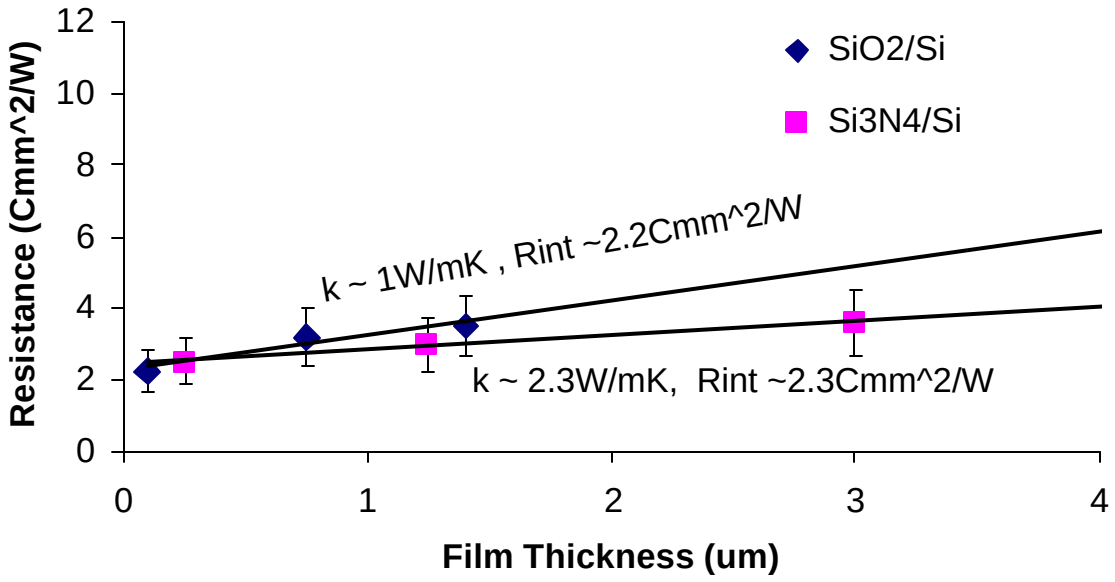


Figure 2.15. Interfacial resistances extrapolated from resistance vs. film thickness for SiO_2 on Si. Data from [38].

Such large interface resistances as in Figure 2.15 are not the norm for SiO_2 and Si_3N_4 to Si interfaces. Lee et. al. [39] measured the interface resistance of PECVD deposited SiO_2 and Si_3N_4 on Si and measured approximately 0.02Cmm^2/W for both using the 3 omega method. This seems to be within at least an order of magnitude of the DMM results. The same method was used by Hu et. al [40] who studied the interface of polymeric low-k materials to Si and measured 0.04-0.2Cmm^2/W for four different organic materials. The results were typically within 50% of both acoustic mismatch (AMM) and DMM model predictions. Alvarez-Quintana et. al. [41] Also used the 3 omega method to measure the interface between $Si0_2$/a-Ge/Si and published values of 0.02Cmm^2/W for the interfaces.

The metal dielectric interface was analyzed by Chien [42] who used a sandwich structure of different metal layers between two dielectric oxide layers and compared

measured thermal resistance to phonon/electron non-equilibrium based theoretical results. The extracted interfacial resistances were about an order of magnitude higher than those predicted by the two-fluid model [42]:

$$R_{SiO_2-m} = \left(\frac{d}{k_e + k_p}\right)\left(\frac{k_e}{k_p}\right)\left[\frac{e^{\frac{L}{d}} - 1}{e^{\frac{L}{d}} + 1}\right] \qquad (2.4)$$

Where: L=thickness of metal layer,

$$d = \sqrt{\frac{k_e k_p}{G(k_e + k_p)}}$$

G=electron-phonon coupling factor

k_e=related by Wiedemann-Franz law

k_p=Cvl/3

C from Dulogn-Petit law

l assumed to be 2X lattice constant

The modeled and measured results are summarized in Table 2.3.

Table 2.3. Interface resistance between metal and SiO_2 calculated using two fluid model and measurements. Data from [42].

Metal-SiO_2 Interface	Two fluid model Cmm^2/W	Measurement Cmm^2/W
Cr	7.1x10-4	2.4x10-2
Ti	3.9x10-4	3.4x10-2
Al	1.3x10-3	3.5x10-2
Ni	8.1x10-4	3.5x10-2
Pt	1.6x10-3	3.8x10-2

Chien explained the model/measurement discrepancies as imperfections at the interfaces, such as voiding. Other studies of metal to dielectric interface resistance include Cahill, et. al., [43] who summarized the measurements of several dielectric materials to metals ranging from 0.005 to 0.03Cmm^2/W, although the comparative DMM results were always somewhat smaller. Bai et. al. [44] used a thermo-reflectance technique to measure 0.012Cmm^2/W for the interface between Si_3N_4 and Au. Lee et. al. [45] used the 3 omega method to measure the interface resistances of SiO_2 and MgO sandwiched between a metal and Si. For the combination of metal + Si interfaces, they reported values of 0.016Cmm^2/W for SiO_2 and 0.04Cmm^2/W for MgO. These values are certainly within the range of values from the DMM or two fluid models.

In summary, the review of prior work on the interfacial resistance between dissimilar materials reveals a wide range between measurements by different researchers and techniques. Disparity also exists between theoretical perfect-bond models and experimental results, although some researchers have been able to get decent agreement. The differences between the theoretical models and experiments can only be explained by imperfections at the interface caused by sample preparation or measurement techniques. Even after neglecting extreme values, an order of magnitude difference between measured and perfect-bond models is not uncommon. Modeling the resistance caused by imperfections such as voids or impurities at the interface is another field in itself. (An interesting study by Prasher [46] attempted to relate the higher interface thermal resistance due to imperfections to the materials' adhesion energy). Ultimately, these types of studies provide a different way of measurement, not necessarily a way to understand the causes of the imperfections or how to incorporate them into the theoretical models. Process variability and sample preparation will certainly affect any results. The

R_{dd} extracted from the 3D stack test vehicles (see pages 33-34 and Chapter 3), suggests imperfections in an actual BEOL stack are not as alarmingly high as the measurements from Lambropoulos [38] for example (page 39) might suggest.

In conclusion, the results from all theoretical models suggest the thermal resistance for a perfect bond between dissimilar materials would be negligible for most macro-level analysis of BEOL stacks. Therefore a standardized, large-sample-size measurement technique is necessary for determining the resistance of BEOL stacks with variable interface resistance due to process variability.

2.6 STRAIN EFFECT

Another factor seldom considered in calculation of overall thermal resistance is the impact of strain. Picu [47] used a monatomic Lennard-Jones solid assumption and a molecular dynamics simulation to calculate the thermal conductivity of the solid under plane strain and plane stress conditions. They found that the plane strain condition affected thermal conductivity, but plane stress had a negligible impact. Hydrostatic strain had the largest impact. The results of the plane strain and hydrostatic strain are shown in Figure 2.16. The effects are due to change of phonon group velocities and mean free paths caused by the strains. As can be seen, the plane strain condition makes the thermal conductivity anisotropic. Focusing on the range of less than 2% strains, averaging hydrostatic and in-plane results and linearizing, one can conclude that the ratio of strained to unstrained thermal conductivity is approximately:

$$k/k_o \simeq 1\text{-}0.21(\%e), \qquad \text{for } e = 2\% \qquad (2.5).$$

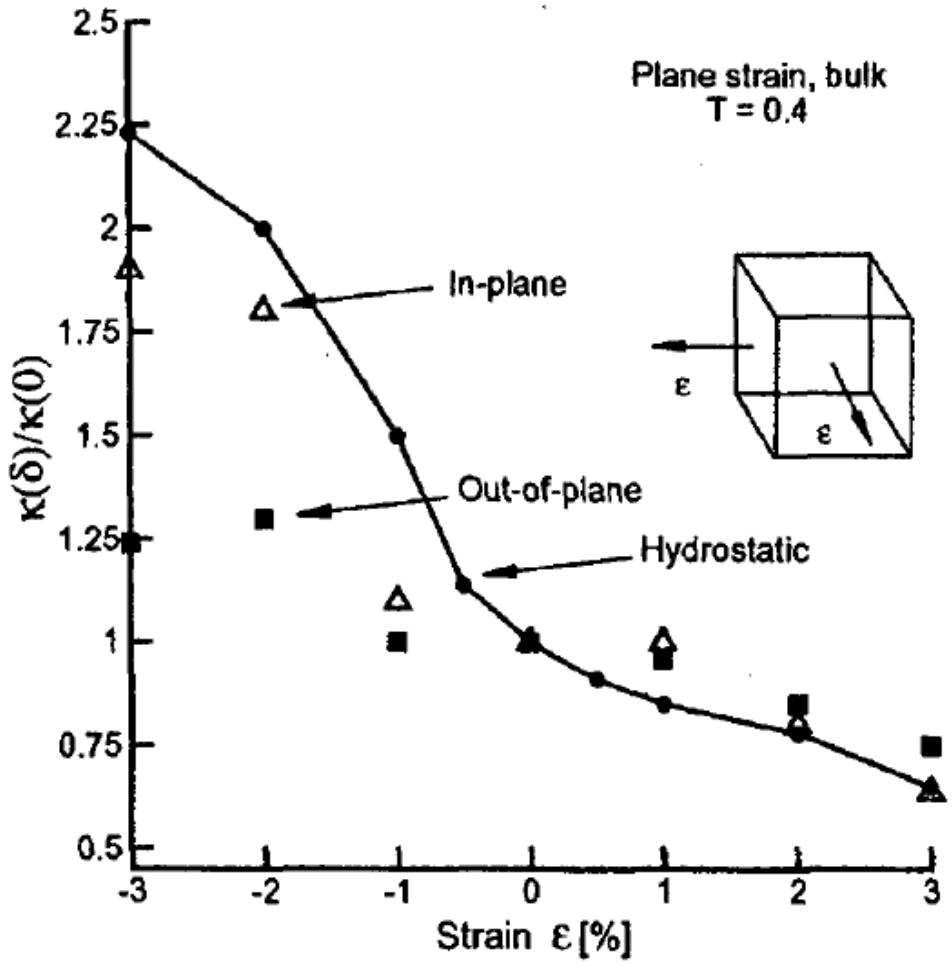


Figure 2.16. Effect of strain on thermal conductivity of a Lennard-Jones solid. Both hydrostatic (lines) and in-plane strain components are shown. Reprinted with permission from [47]

Bhowmick [48] also explained the strain dependence of thermal conductivity as manifested in the group velocity (speed of sound) and relaxation time. However, the only strain condition analyzed was hydrostatic strain. In the work, the phonon frequency was related to strains, and compared with a molecular dynamics simulation showing good comparison. The relaxation time was related to temperature and strain as follows [48]:

$$t \sim \frac{1}{T} e^{-g} \qquad (2.6)$$

where g is a material constant. The relationship of group velocity to strain based on their results was approximately:

$$\frac{u}{u_0} \approx 1 - 4(\%e) \qquad (2.7)$$

resulting in a strained to unstrained thermal conductivity ratio of approximately:

$$k/k_o \simeq 1\text{-}0.20(\%e) \qquad (2.8)$$

which is fairly close to that extracted from Picu (eq 2.5). Using the above relationship, it was desired to find the impact of strain on the thermal conductivities of typical BEOL materials. As a test case, the strains developed in a six layer stack arising from the thermal loading from deposition temperatures were analyzed using ANSYS. In an actual BEOL structure, the strain fields would be much more complicated, due to the metal lines, vias, and package influences. It is obvious from Figure 2.17 that there would be some layers in tension and others in compression. For the highest strain shown in Figure 2.17, the k/k0 would be ~0.8. However, a majority of the layers are either in compression or unstrained. It is therefore argued that while design dependent, the net effect of the strain on thermal resistance of the BEOL (and hence R_{dd}) would likely be negligibly small. However, localized regions could be affected more significantly.

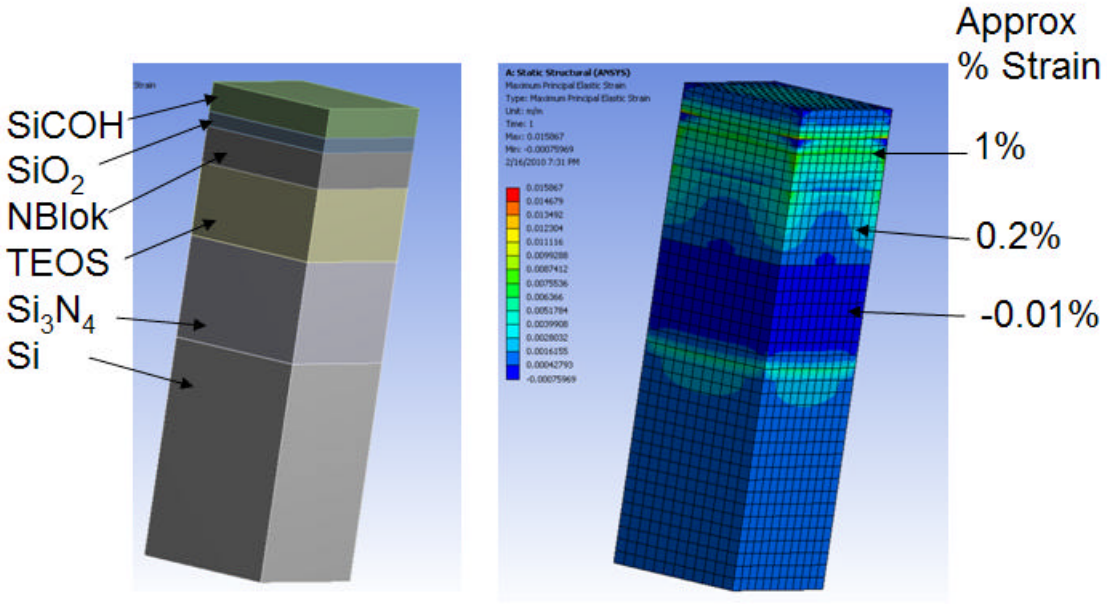


Figure 2.17. ANSYS model of BEOL material stack on Si and resulting max principle strains due only to thermal loading from deposition temperatures to room temperature.

2.7 SUMMARY AND CONCLUSIONS

The primary objectives of this chapter were to quantify the added thermal resistance (R_{dd}) due to the BEOL, and micro-C4 layers for 3D stacked packages and identify the major and minor contributions. The study revealed the micro-C4 interconnects are significantly impacted by the adjacent BEOL resistance and could not be analyzed separately due to spreading resistance. Analysis of the impact of copper through-silicon vias on the total die-die interface resistance, R_{dd}, revealed that only for pitches below ~150µm and for TSVs directly aligned with micro-C4s and which penetrated a significant portion of the BEOL layers would there be significant impact. The interfacial resistance of BEOL materials was evaluated based on the work of others, and revealed some disparity between experimental results of different researchers and

between theoretical perfect-bond models and experimental results. The impact of strain on the thermal resistance of BEOL layers was analyzed and suggested a difficult-to-quantify but negligibly small impact over large areas, and possibly a higher concern for local regions.

Chapter 3: Thermal and Mechanical Validation of Package Macro Model

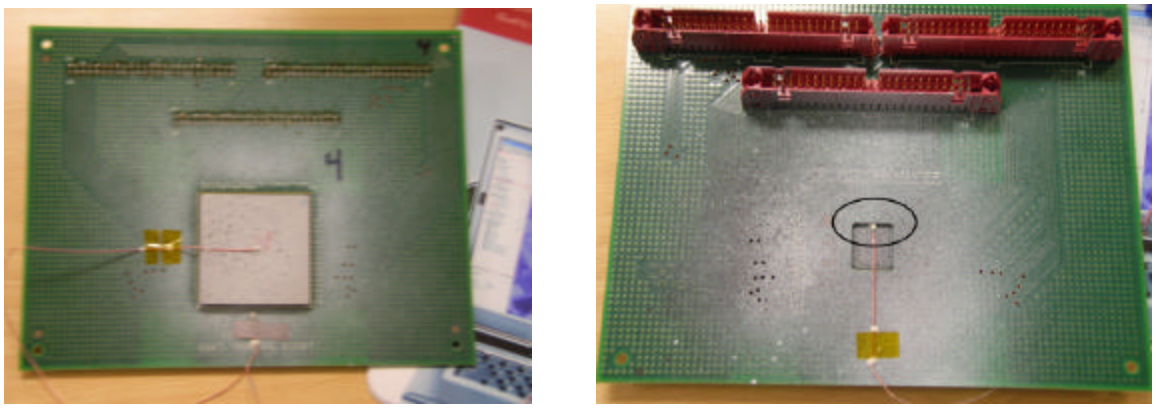
3.1 INTRODUCTION

An ANSYS^{TM} finite element model was used to evaluate the steady state and transient thermo-mechanical response of 2D and 3D packages. The first task was to properly validate the models using test vehicles. This chapter will describe the thermal and mechanical measurements made to validate the package macro level thermo-mechanical model. The macro level model consisted of the package on a printed circuit board (PCB), or card, with the appropriate boundary conditions to simulate the heat transfer from the package surfaces and the mechanical load from the heat sink. The thermal validation will be described in Section 3.2, with details of the thermal test vehicles, description of the thermal model and comparison of measured and modeled results. Section 3.3 will contain similar details for the mechanical model validation.

3.2 THERMAL VALIDATION OF PACKAGE MACRO MODEL

3.2.1 Thermal Validation Test Vehicles

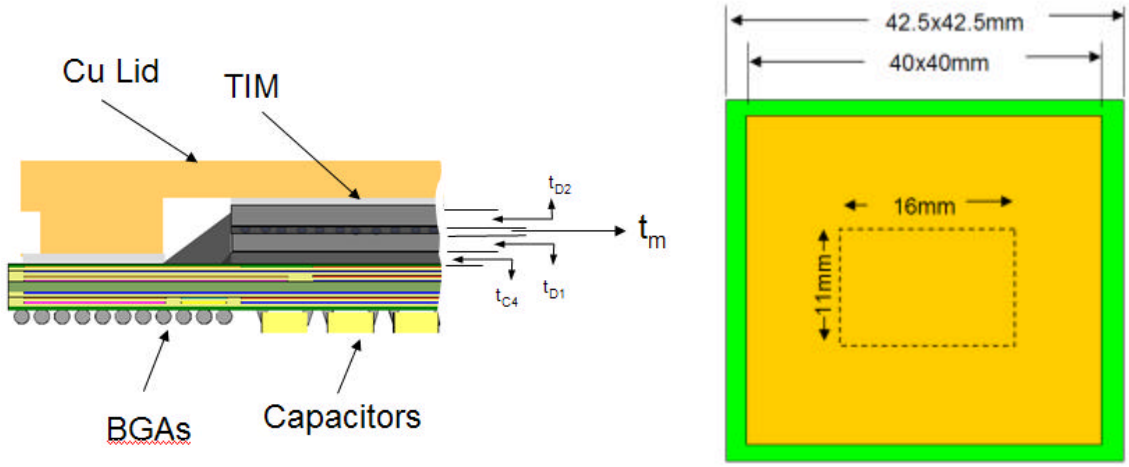
Three different test vehicles were used for thermal validation, 3D stacks containing dummy die adhered to the back surface of functional test die, and a standard 2D test vehicle containing a single functional die. A picture of a test module on card is shown in Figure 3.1. Thermocouples used in thermal measurements were attached to the lid and card as shown.



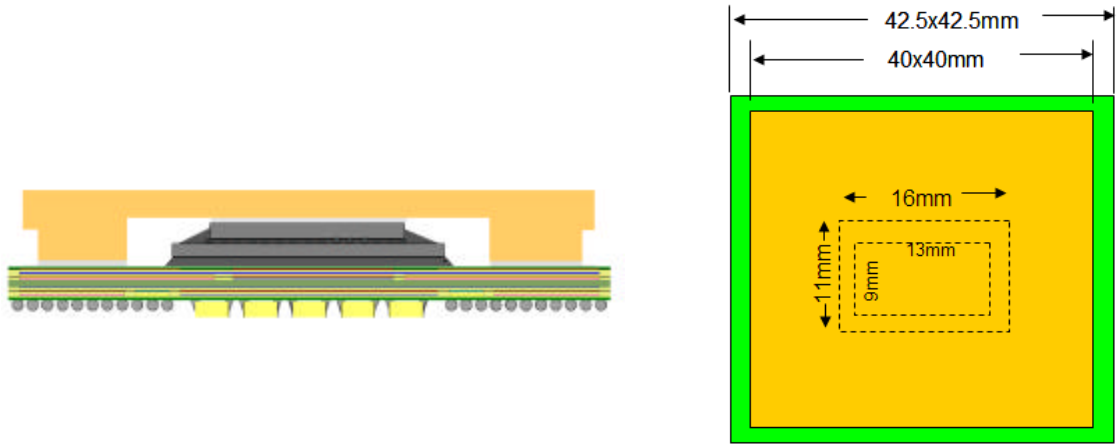
(a) (b)

Figure 3.1. Picture of thermal validation vehicle on card, module side (a) and card backside (b) showing thermocouples attached to the lid and card.

Figure 3.2 shows the dimensions and components of the two 3D stack test vehicles. 3.2a shows a test vehicle with two 11x16mm die. The left side figure shows half the module, highlighting the bottom die (D1), top die (D2), die-die micro-C4 (m) and C4. Also highlighted are the Cu lid, thermal interface material (TIM), BGAs and capacitors. (The capacitors served no purpose for this study). Figure 3.2b shows a similar stack test vehicle with a smaller (9x13mm) dummy die on top. The thicknesses for the die and joining layers are summarized in Table 3.1. In addition, a standard 2D package (not shown) with all similar components but without the top die was used for comparison.



(a)



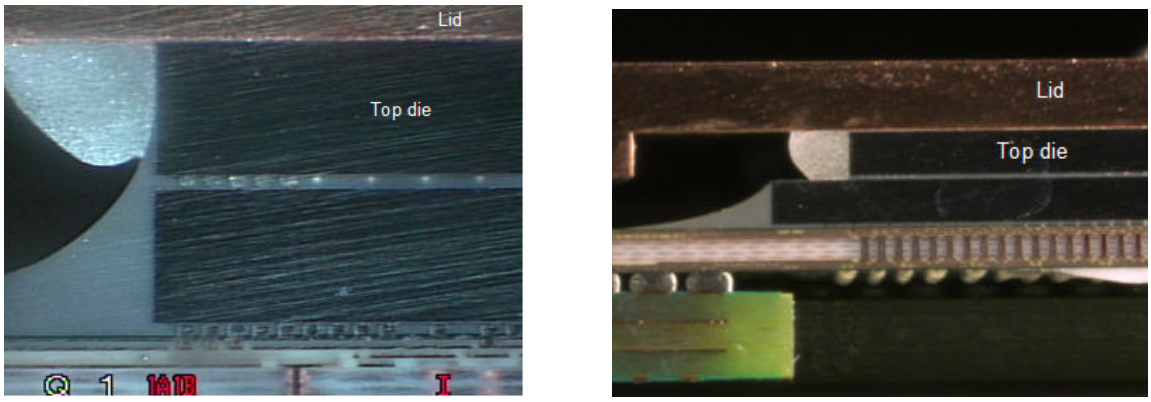
(b)

Figure 3.2. Schematic showing the module components and dimension for the same size die stack (a) and smaller-die-on-top stack (b)

Table 3.1 Thickness of C4 (t_{C4}), micro-C4 (t_m), bottom die (t_{D1}) and top die (t_{D2}), and TIM (t_{TIM}). All dimensions in µm.

	Same size die stack	Smaller die-on-top	2D
t_{TIM} (µm)	26	32	28
t_{D1} (µm)	770	766	770
t_{D2} (µm)	764	758	NA
t_m (µm)	68	68	NA
t_{C4} (µm)	60	54	58

Figure 3.3 shows cross sections of the 3D samples. 3.3a shows the same-size-die stack test vehicle at the die edge. A slightly larger field of view is shown for the smaller-top-die test vehicle in 3.3b.



(a) (b)

Figure 3.3. Cross section of same size die stack (a), and smaller-die-on-top stack (b).

3.2.2 Assembly Process For Validation Test Vehicles

Standard bare die 2D flip chip test vehicles were used to create the 3D stacks by bonding a non-functional die to the backside of the test die using a conventional epoxy based underfill. The underfill was dispensed on the back of the lower (functional) die which was previously C4-reflowed to the laminate using standard manufacturing lead-free reflow temperature profiles and underfilled with a conventional capillary-flow

underfill. The top die was placed centrally on the lower die and fixtured with adequate weight during the curing process of 150ºC for 90mins. After adequate cleaning of the die surfaces, the TIM was dispensed on the top die, a lid adhesive was dispensed on the laminate to adhere to the lid seal, and cured again at 150C for 90mins. Several debug samples were built and cross-sectioned to ensure expected bondlines and minimal voiding in the underfill and TIM.

Although several attempts were made to minimize the void levels in the die-die interface, zero voiding was never achieved. Figure 3.4 shows a Sonoscan image of typical voiding in the die-die interface. The TIM interface and C4 interface between bottom die and laminate were essentially void free based on similar Sonoscan measurements.

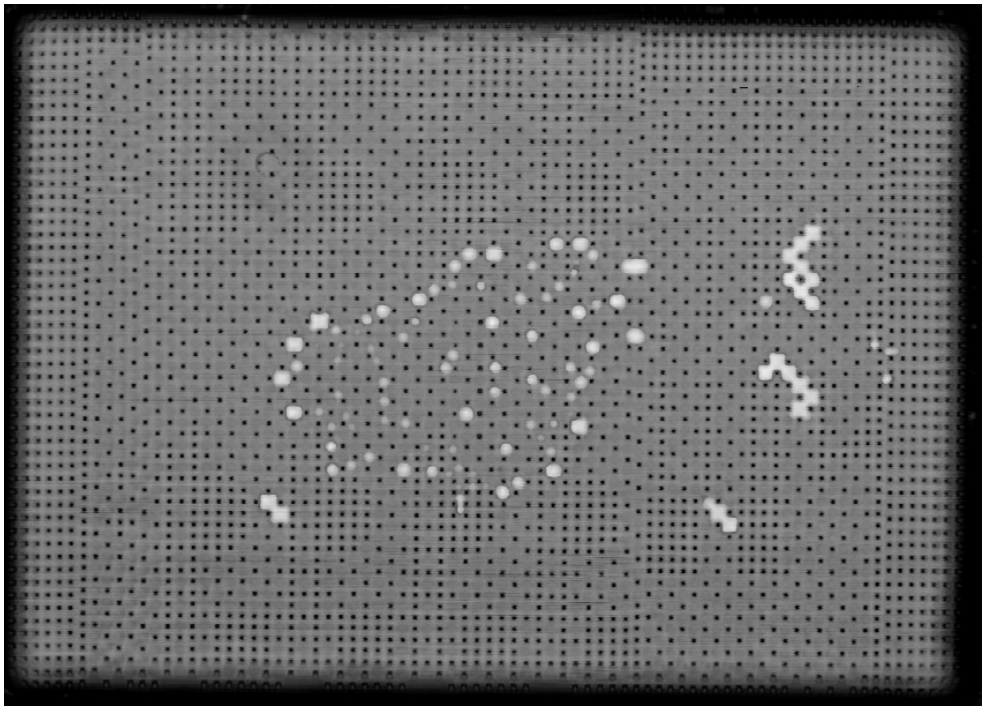


Figure 3.4 Sonoscan of die-die interface showing some voiding (white regions).

3.2.3 Thermal Test Die Description

Figure 3.5 shows the details of the functional thermal test die used in the 2D and 3D packages. The die consisted of four primary heaters that could be powered to provide uniform power to the die. Smaller secondary and tertiary heaters were also available on the die, but not used for this study. All heaters were made of serpentine electrically resistive metal lines. The die contained fourteen temperature sensors placed throughout the die to measure chip temperatures. The sensors were made of electrically resistive elements which could be calibrated in an oven to measure the chip temperatures during operation.

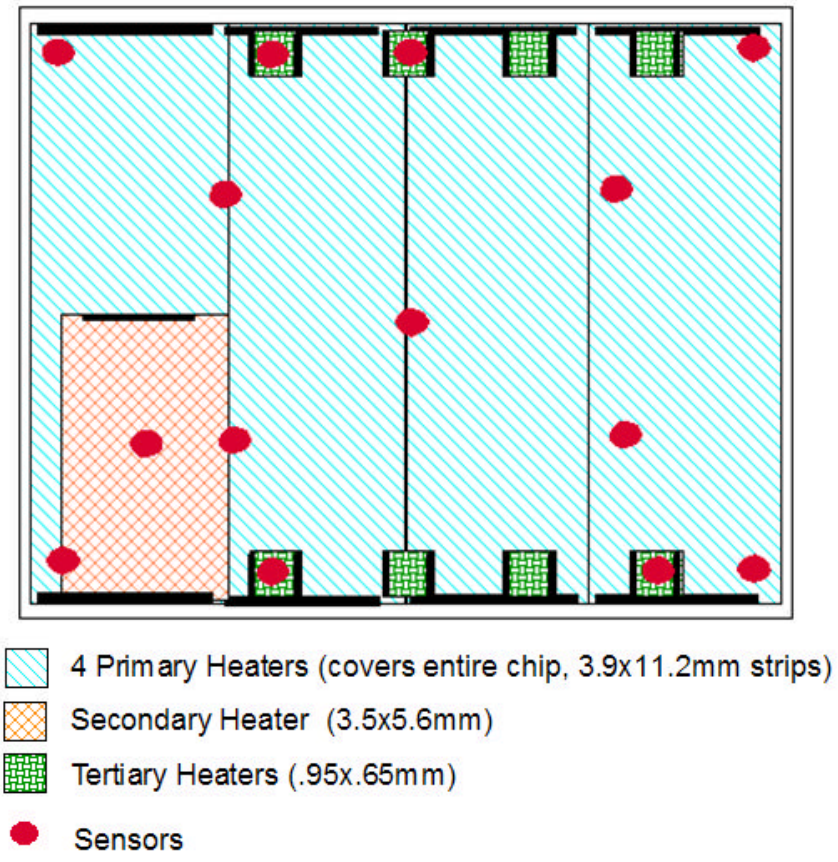


Figure 3.5. Thermal test die used in thermal validation test vehicles.

3.2.4 Thermal Test Procedure

36-gauge Type T thermocouples were used for measuring surface temperatures. The thermocouple beads were placed on the lid and card as shown previously in Figure 3.1. A commercially available thermally conductive epoxy (k ~1W/mK) was used for attachment of the thermocouple bead.

The temperature sensing resistors were calibrated in an oven to get the resistance-to-temperature relationship using a multiplexed constant current source and voltage meter. Testing was conducted on a cold plate as shown in Figure 3.6. The package was mounted on the cold plate with the lid in intimate contact with the cold plate. A thermally conductive oil was used to minimize interface resistance to the cold plate. A groove in the cold plate accommodated the thermocouple bead and wire and allowed flush mounting of the lid. An insulating foam was used on the backside of the card to reduce heat loss from the back. Maintaining the cold plates at an adequately low temperature and reducing contact resistance ensured negligible losses through the package sides and back of the board. These boundary conditions could be representative of high-powered processors with high-end heat sinks in actual applications. The heaters were powered and temperature sensor voltages and lid temperatures were recorded continuously as steady state was reached. The power was then shut off and temperatures tracked as the package cooled to the cold plate temperature.

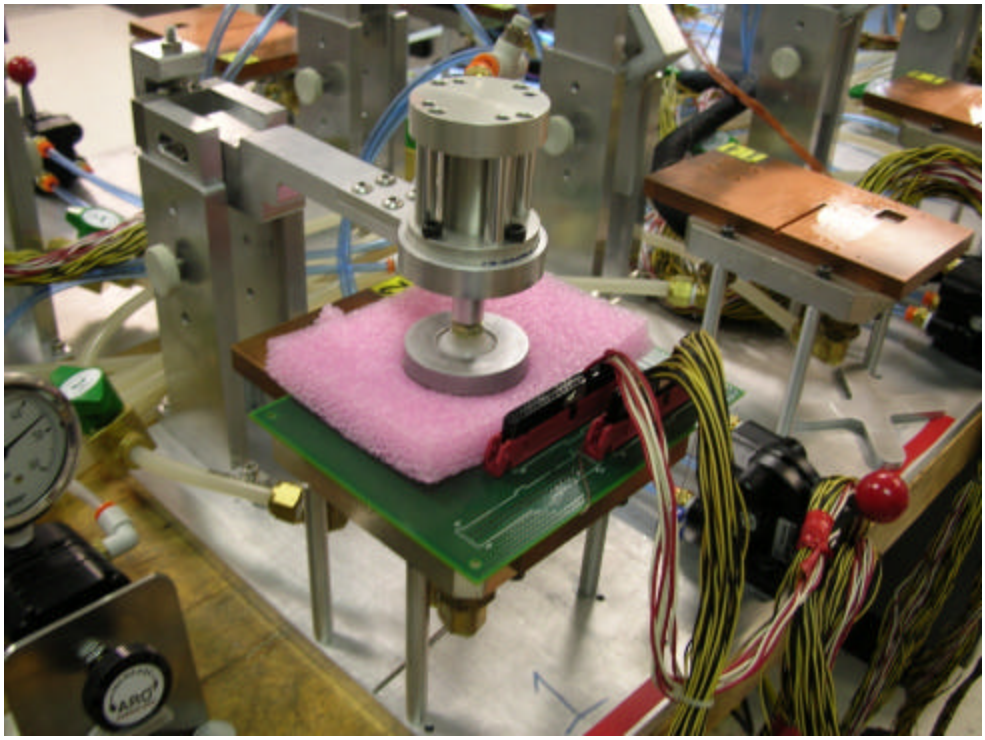


Figure 3.6. Testing on a cold plate

3.2.5 Thermal Model Description

Figure 3.7 shows the ANSYS^{TM} quarter-symmetry model used for package thermal and mechanical analysis. The model contained roughly 100,000 nodes and 60,000 elements. Both brick and tetrahedral elements were used for balancing mesh size and simplicity of creation, and a higher density of elements were used in the die region being analyzed. The thermal model parameters were validated as follows:

1. 2D die-to-lid steady state measurements to determine TIM resistance
2. 3D stack steady state die-to-lid resistance measurements to determine die-die interface resistance using TIM values obtained from step 1 and bondline information from cross sections.

3. Lidded cold plate transient measurements to determine appropriate conductivities and thermal diffusivities for rest of components

The heat transfer coefficients for the cold plate measurements were determined from steady state die-to-ambient measurements. Values were determined for each measurement to give the correct chip center temperature at steady state, and held constant for the rest of the transient analysis to determine thermal diffusivities. Typical values ranged from 4500-5500 W/m^{2}K applied to the lid top surface (representing the cold plate and oil interface), all other vertical surfaces of the package and card were fixed at 30W/m^{2}K and the horizontal surfaces at 10W/m^{2}K

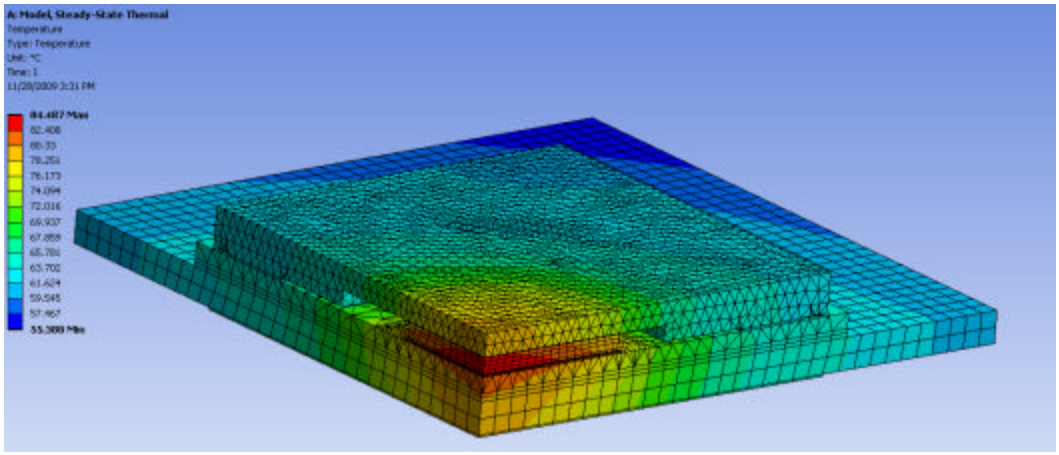


Figure 3.7. ANSYS^{TM} package thermal conduction model.

3.2.6 Thermal Validation Results

Table 3.2 summarizes the die center-to-lid thermal resistance (theta-jc) values for the 2D and 3D packages. The TIM thermal resistance was adjusted to match the 2D test vehicle thermal measurements. Assuming the TIM resistance to be the same for all test vehicles (based on the similarities of the TIM bondlines measured in cross sections, see Table 3.1), the die-die interface resistance (R_{dd}) could then be extracted from the model.

Table 3.2 Measured theta-jc of 2D and 3D packages and TIM resistance and R_{dd} extracted from model.

	Measured Theta-jc	TIM Interface Resistance	R_{dd} Assuming same TIM Resistance
2D	0.08C/W	~12 Cmm^2/W	
11x16 on 11x16mm	0.60 C/W		110Cmm^2/W
9x13 on 11x16mm	0.65 C/W		95Cmm^2/W

Figure 3.8 shows the model/experiment comparison for the standard 2D package as the powered package (60W) at steady state cools down to the cold plate temp of 30C after power shut-off. The lines represent modeled results, and dots of the same color the corresponding experimental data. The three temperature points are the die center (Die cent), card top approximately 5mm from the package edge (card), and backside capacitor temperature (decap). Figure 3.9 shows similar results for the 11x16 on 11x16mm die stack package, and Figure 3.10 shows the 9x13 on 11x16mm die stack results. Figure 3.10 also includes the chip corner temperatures on the lower die which are not covered by the top die. As can be seen from all three figures, the model to experiment agreement is excellent. Both the steady state power (time <0) and transient temperatures are within ~10% agreement at worse. The temperature measurement uncertainty is approximately 1C, and about the size of the markers used for in the plots. The resulting material properties used in the model are shown in Table 3.3

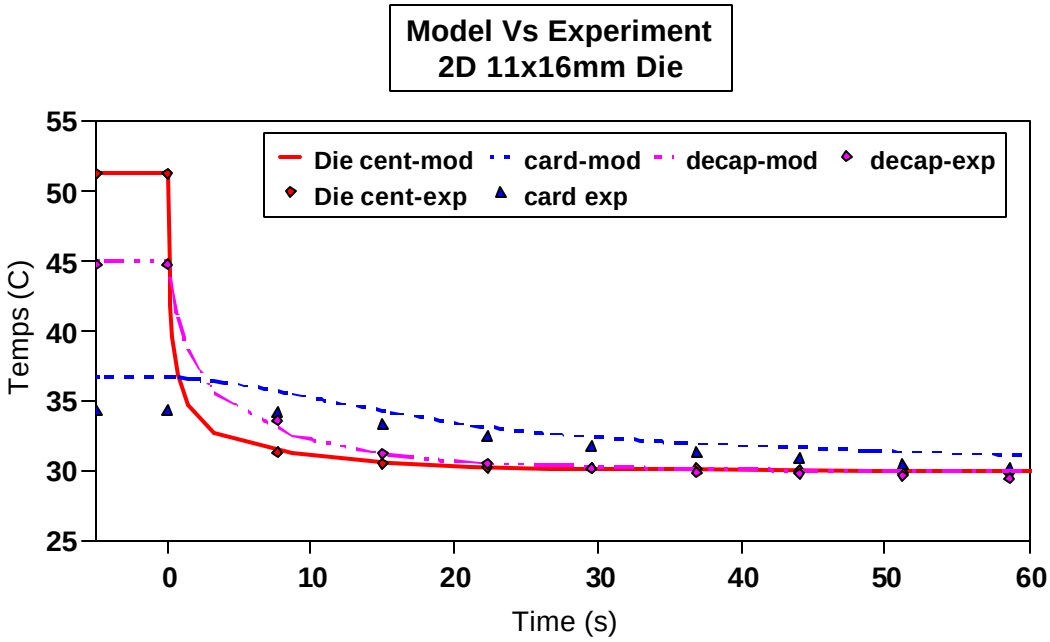


Figure 3.8. Model/experiment comparison for 2D package, showing die center, card, and backside capacitor temperatures during cool down from powered state.

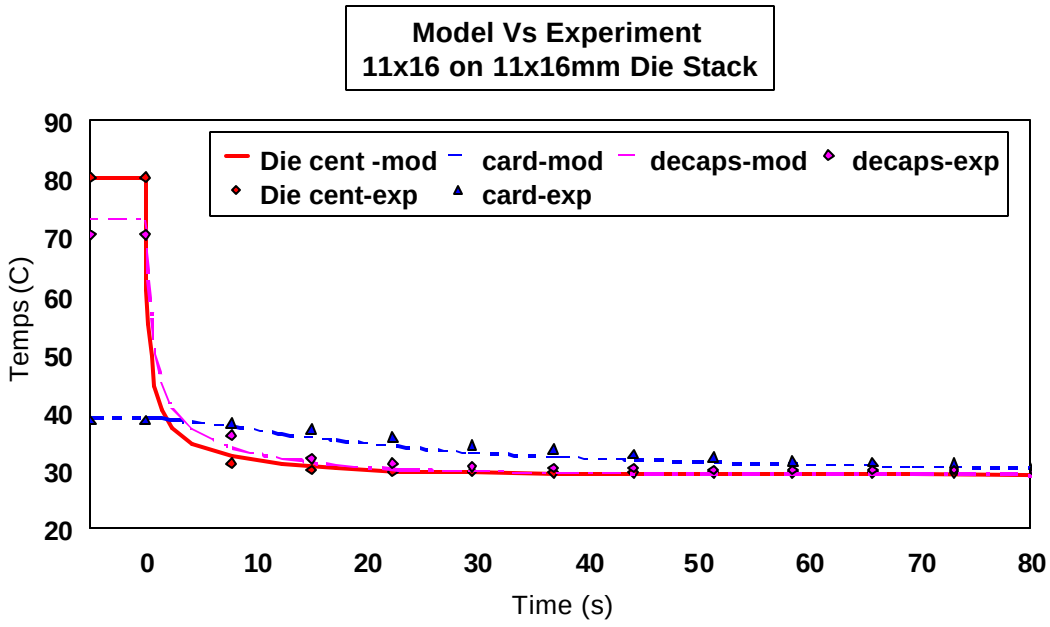


Figure 3.9 Model/experiment comparison for same size die stack package, showing die center, card, and backside capacitor temperatures during cool down.

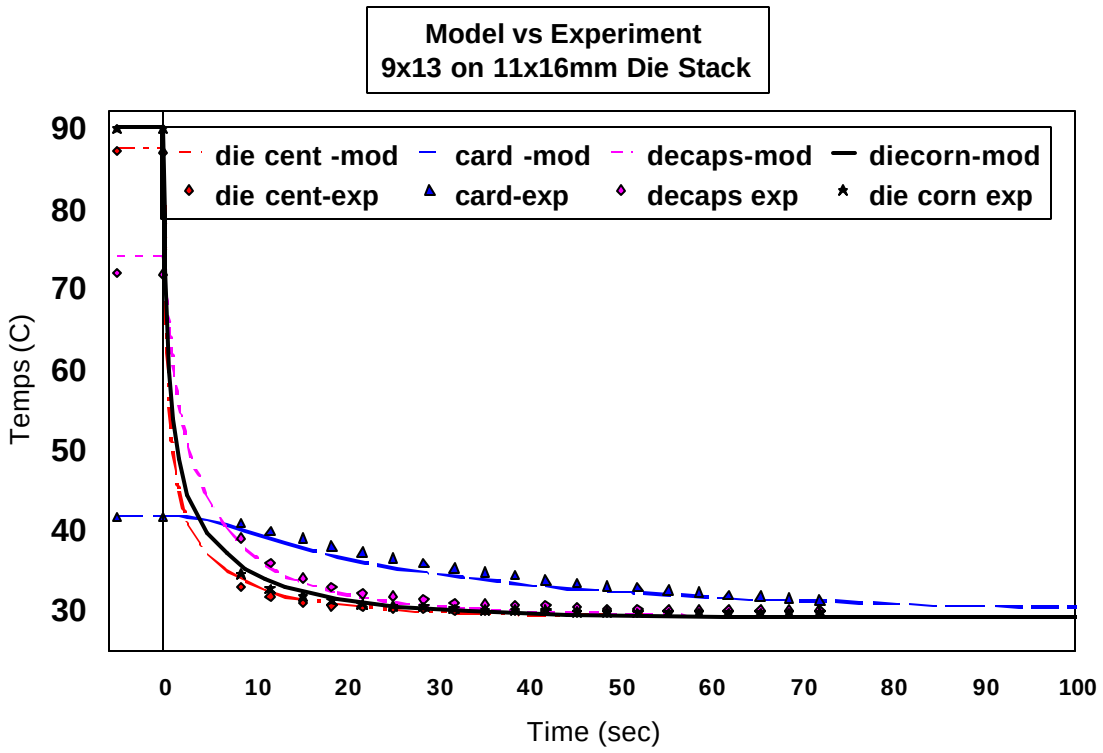


Figure 3.10. Model/Experiment comparison for 9x13mm on 11x16mm die stack package, showing die center, card, backside capacitor and die corner temperatures. Cooling from 60W powered state. Measurement uncertainty is approximately 1C.

Table 3.3. Thermal material properties resulting from validation experiments.

	Therm. Cond. (W/mK)	Spec. Heat (J/kgK)	Den (kg/m^3)
C4/Underfill	1	1000	1700
Card	3xy, 1z	2000	1700
Lid	380	385	8300
Laminate	75xy, 6z	1600	1700
Die-Die interf	1	1000	1700
Si	130	700	2330
BGA layer	0.34xy, 8z	134	5500
Lid Adhesive	1	500	2000
TIM	2.5	500	2000

3.3 MECHANICAL VALIDATION OF PACKAGE MACRO MODEL

3.3.1 Test Vehicles Used For Measurements

Figure 3.11 shows the variety of test vehicles used for the mechanical model validation, and Table 3.4 gives details for each type of test vehicle. Most of the packages were essentially the same as those used for the thermal validation described in the previous section. The test vehicles included lidded and bare-die versions however. The assembly process and die thicknesses were essentially the same as those described in Sec. 3.2. One test vehicle which was not used in the thermal validation was one which contained a 75um interposer under a standard thickness die. This test vehicle contained thru-silicon vias (TSVs) and was also used for the TSV micro model validation to be described in Chapter 4.

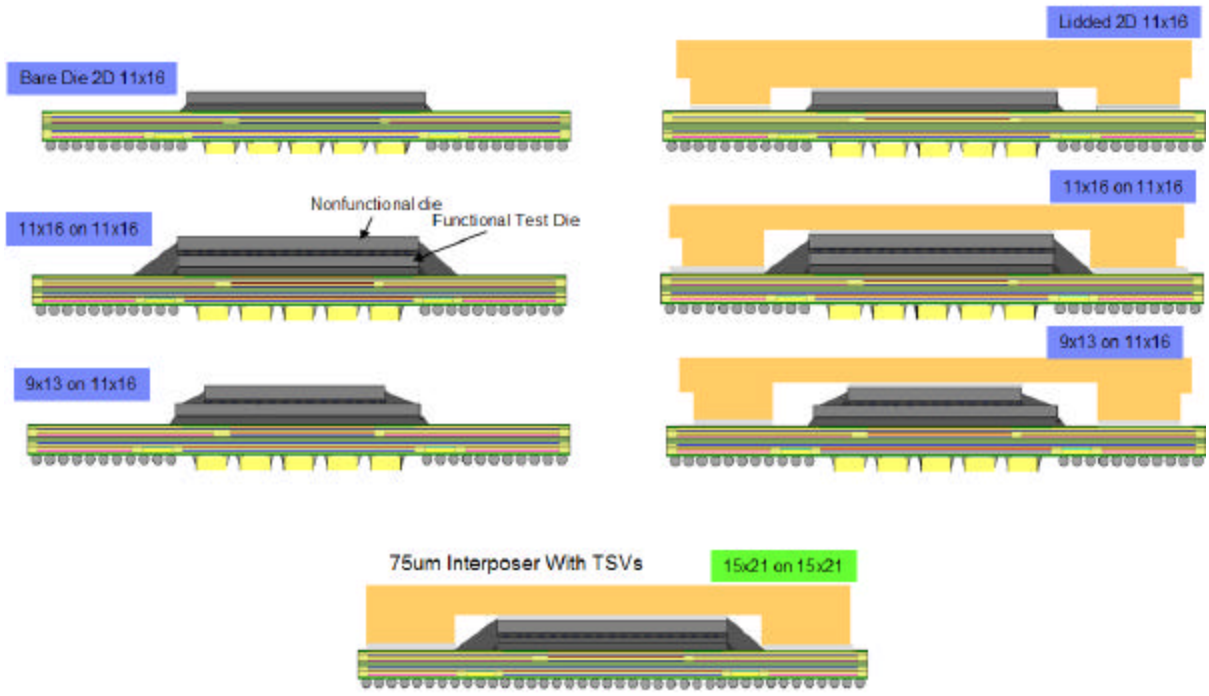


Figure 3.11 Test vehicles used for macro mechanical model validation.

Table 3.4. Mechanical test vehicle details.

TV	Description	Bottom Die (mm)	Top Die (mm)	Card (mm)	Lid (mm)
2D-BD	2D Bare die module on card	11x16x0.77	none	165x124x1.6	none
2D-LD	2D Lidded module	11x16x0.77	none	165x124x1.6	40x40x2
2D-BD-NC	2D Bare die no card	11x16x0.77	none	none	none
3D-1	Bare die same size die stack	11x16x0.77	11x16x0.77	none	none
3D-2	Lidded same size die stack	11x16x0.77	11x16x0.77	none	40x40x2
3D-3	Bare die same size die stack	11x16x0.77	11x16x0.77	40x40x2	none
3D-4, 10	Lidded stack	11x16x0.77	9x13x0.77	40x40x2	40x40x2
3D-6	Bare die stack	11x16x0.77	9x13x0.77	40x40x2	none
3D-7	Lidded stack	11x16x0.77	11x16x0.77	40x40x2	40x40x2
3D-8	Lidded stack	11x16x0.77	9x13x0.77	none	40x40x2
3D-9	Lidded w/interposer	15x21x0.08	15x21x0.77	none	40x40x2

3.3.2 Digital Image Correlation Measurements

The digital image correlation (DIC) system ARAMIS^{TM} by GOM mbH was used in this study to validate the mechanical properties for the macro model. The system is based on collecting digital images before, during or after deformation, assigning coordinates to the image pixel groups (facets), and tracking the pixels to calculate deformation. Unlike Moire Inteferometry, DIC does not require a grating to be placed on the surface of measurement. However, for optically homogenous surfaces with few distinctive features, a color spray pattern is applied to provide the necessary contrasts. This spray is typically significantly easier to apply and less time consuming than a Moire grating. The following sections give brief descriptions of the measurement technique and theory. For detailed descriptions, the reader is referred to the ARAMIS user manual [43].

For 3D warpage measurements, two cameras are required. The initial step is to determine the necessary measurement volume. A setup and measuring volume are shown in Figure 3.12. The measurement and distance between cameras is based on the camera lenses used and the angle a results when both cameras view the same point.

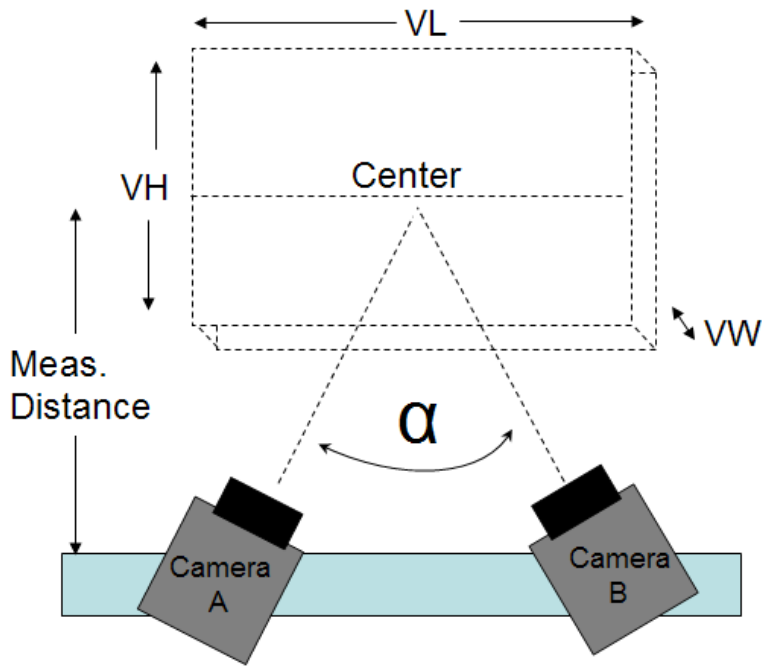


Figure 3.12. Camera setup and measurement volume for 3D DIC measurement.

Calibration objects containing predetermined object distances are used to ensure dimensional consistency of the measuring system. Calibration objects consist of panels or crosses containing scale bars and precise dimensional information. Figure 3.13 shows an example. The ARAMIS^{TM} system has instructional programs with systematic steps to rotate and move the calibration objects and capture images for various configurations. From this set of images the distances and angles between the ARAMIS^{TM} sensors are precisely determined.

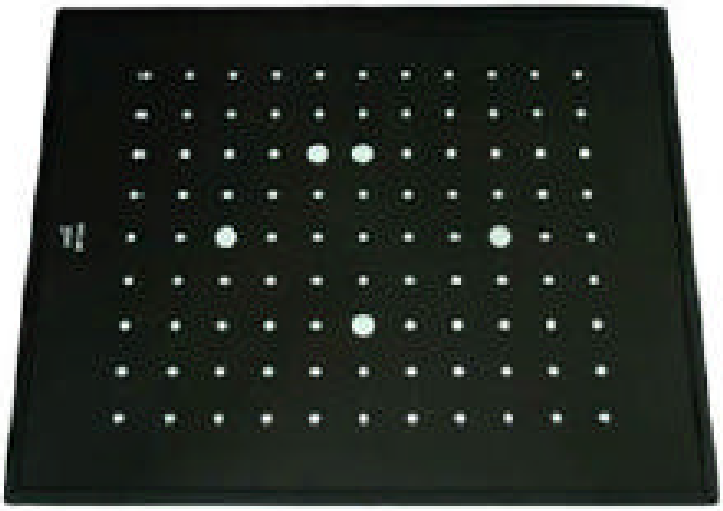


Figure 3.13. Example of calibration panel used to calibrate the ARAMIS^{TM} measurement system [43].

ARAMIS^{TM} uses facets, which are user defined groupings of pixels that are tracked by the software. Each facet determines a calculation point in the image. Larger facets means higher accuracy per point, but fewer points overall. The overlapping of pixels in a facet determines the density of calculations points. Higher overlapping means more calculation points per unit area. As expected, larger facets and higher overlapping results in increased accuracy at the cost of computation time. For 3D measurements, the images from the right and left sensors along with the calibration data are used to calculate 3D coordinates of the facets. The coordinates of the facets are tracked through the deformation stages. The software essentially runs a minimization routine for the difference between a point and its surroundings at its old coordinates versus new coordinates. Rigid body motions can be subtracted out.

Figure 3.14 shows a picture of the system used in this study. The figure shows the two cameras mounted on a fixture, which is viewing a sample inside a temperature

chamber through a view-glass (not visible in picture) from above. Fluorescent lights are used to illuminate the sample.

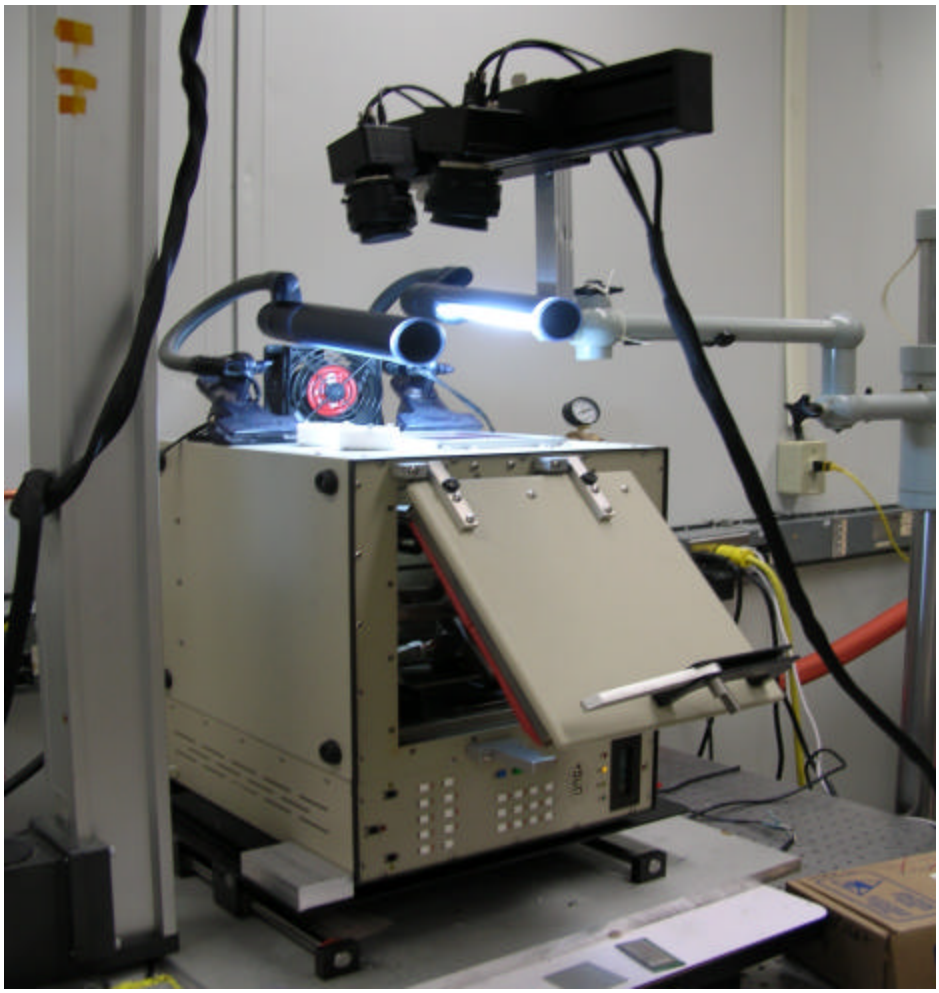


Figure 3.14. The Digital Image Correlation (DIC) setup used for measuring module warpage and in-plane deformation for mechanical model validation.

Figure 3.15 shows a sample warpage measurement of the underside of a laminate. In the upper left are line scan profiles and on the right is a contour plot of warpage. Figure 3.16 shows an example of in-plane X field contours on the cross section of a package. The measurement accuracy for the system is approximately ±5um for 3D

measurements, and theoretically an order of magnitude better for in-plane measurements, however, based on repeatability measurements it is believed to be closer to ±2um for in-plane.

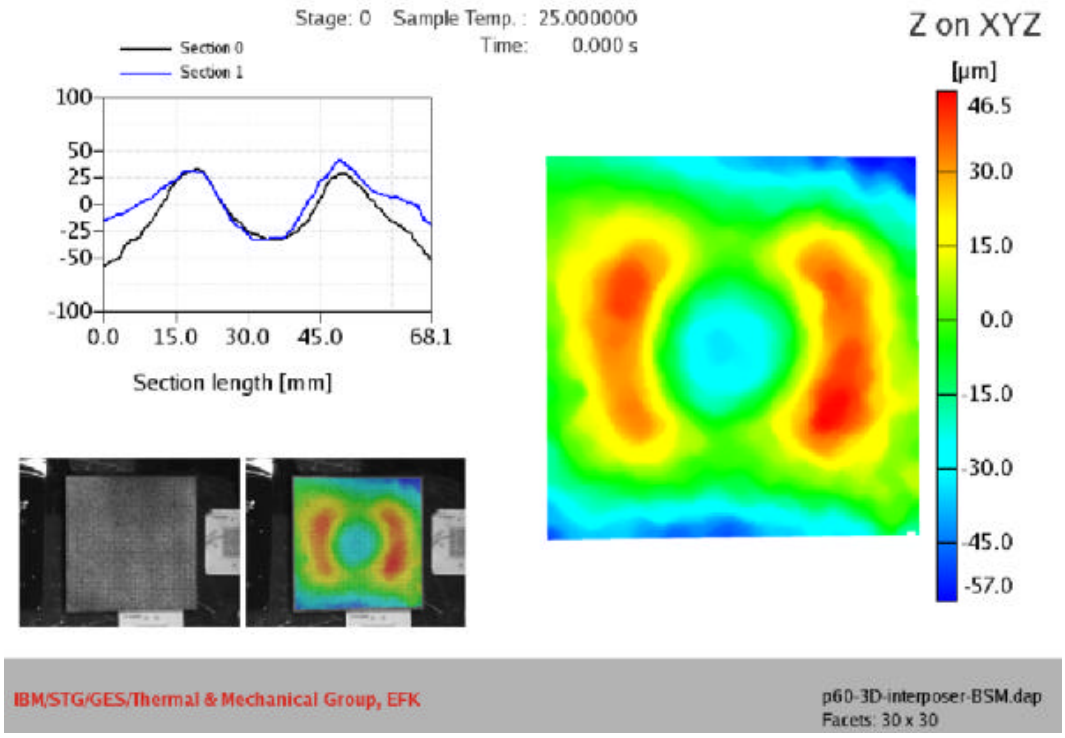


Figure 3.15. Example of DIC warpage measurement.

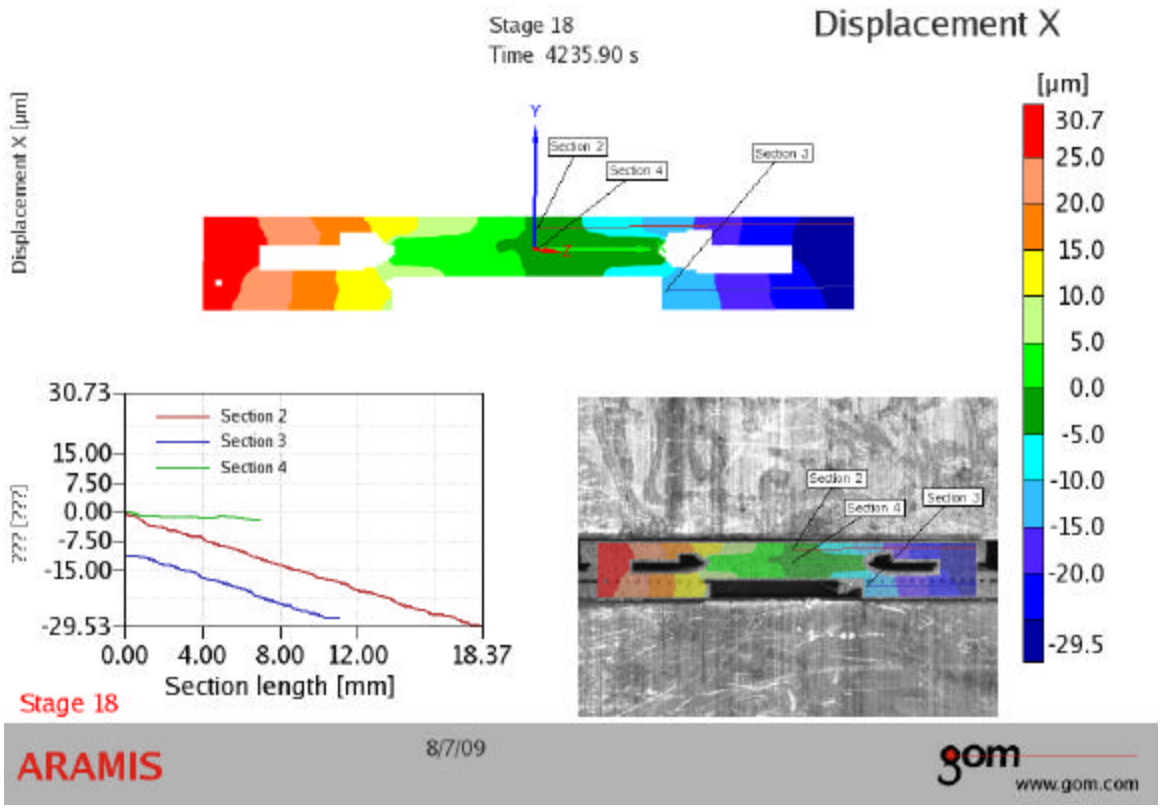


Figure 3.16. Example DIC in plane X-displacement measurement.

3.3.3 Mechanical Model Validation Strategy

Figure 3.17 depicts the strategy for validating the various components of the mechanical model. A systematic approach was used wherein samples ranging from bare-die-on-laminate to fully assembled modules on card were used to fix the properties for various components of the package. For all materials, initial values based on previous characterization or vendor data were used, and then adjusted to match the measurement results. First, a bare die flip chip module (2D-BD-NC in Table 3.4) was used to fix the laminate and underfill/C4 layer properties. Next a two-die stack without lid or card (3D-1) was used to fix the die-to-die interface properties. Next, 3D lidded packages (3D-2, 8,

9) were used to fix the TIM and lid adhesive properties. Finally, a 2D bare die package on card (2D-BD) was used to fix the card and BGA layer properties.

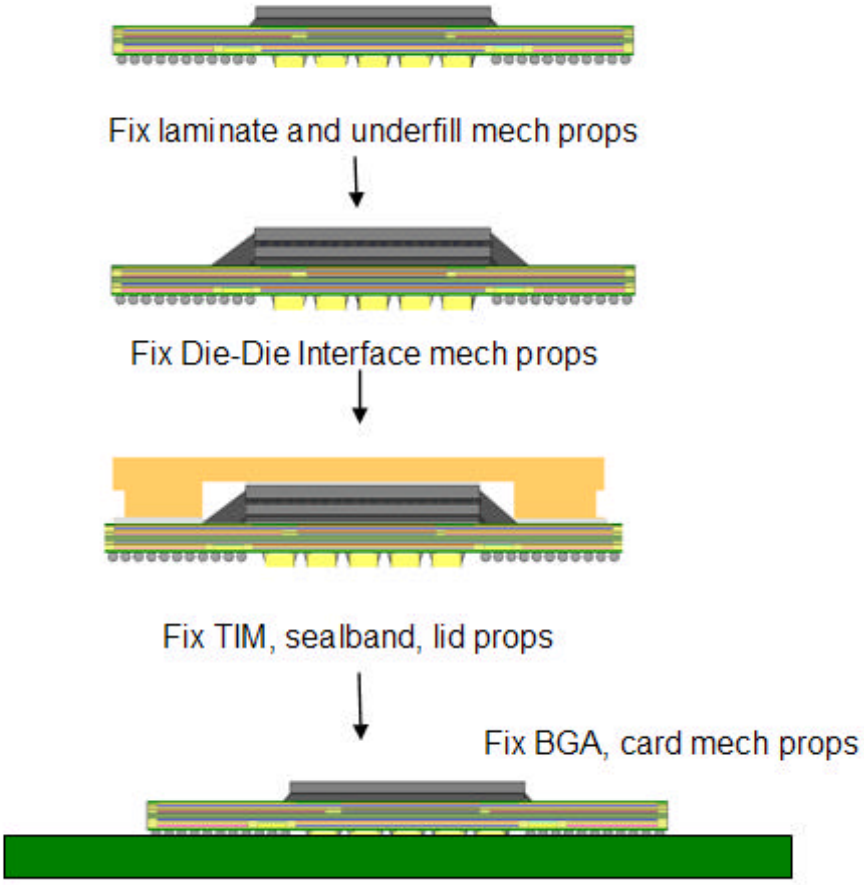
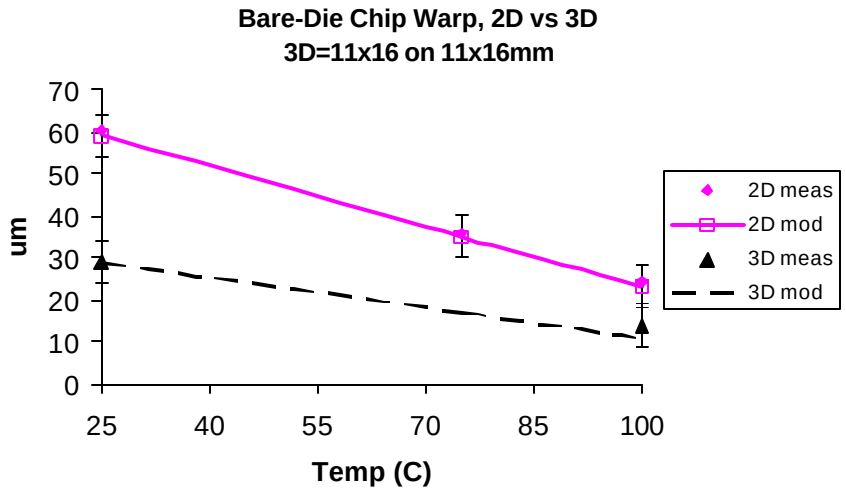


Figure 3.17. Mechanical property validation strategy.

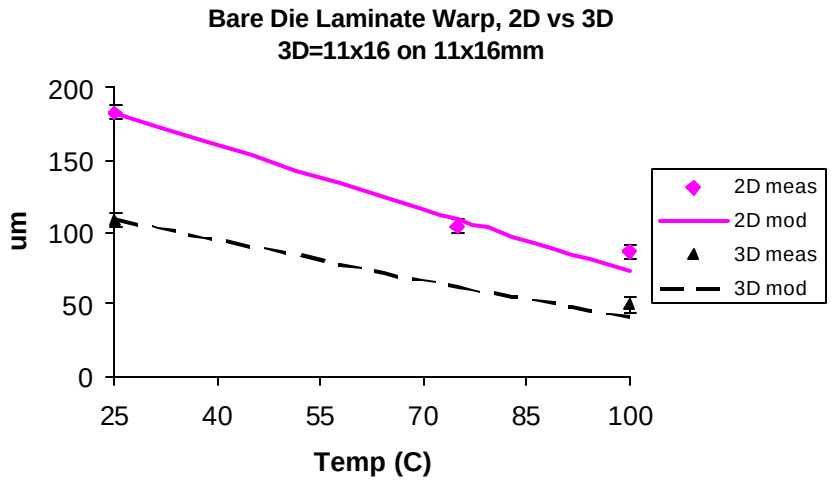
3.3.4 Measurement/Modeling Comparison

The same model used for the thermal validation and described previously in Sec 3.2 was used for the mechanical property validation. All properties were assumed linearly elastic. The primary purpose of the experimental validation was to generate greater confidence in this simplified modeling approach.

Figures 3.18 shows the bare die module without card chip (a) and laminate bottom (b) warpage measurements (dots) and model results (lines) as a function of temperature. The figure shows the 2D module as well as the 11x16 on 11x16mm 3D die stack. As can be seen, the model and measurements are in close agreement. Figure 3.19 shows the chip warpages for bare die modules assembled on cards.



(a)



(b)

Figure 3.18. Module level chip (a) and laminate backside (b) warpages as function of temperature, measured and modeled, for bare die modules without card.

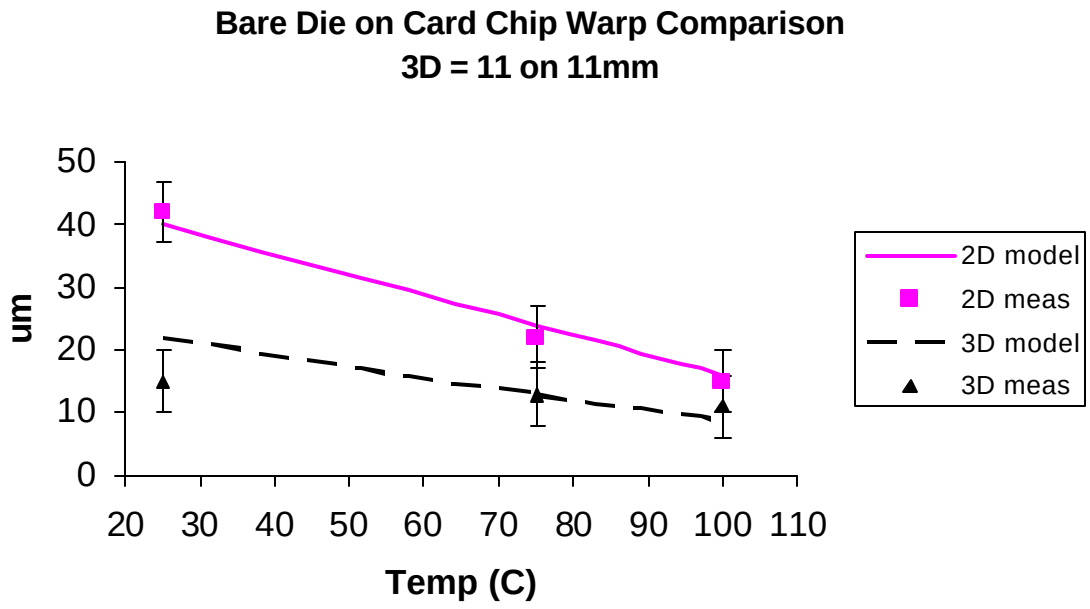


Figure 3.19 Chip warpage for bare die module on card.

Figure 3.20 shows the laminate warpage comparison for one of the lidded 3D packages without card (3D-8). Here, significant difference can be observed between the measurements and models. This was a consistent trend with all the samples and believed to be due to non-flatness of the lid and non-idealities in the lid attach process. In general, this is not believed to affect the accuracy of the model for the purposes of this work.

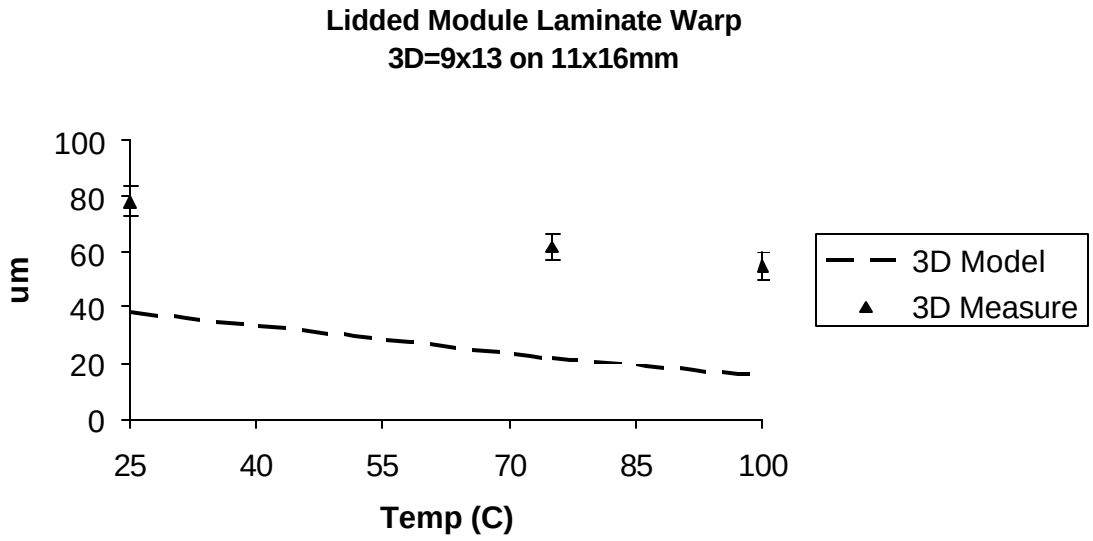


Figure 3.20 Module level laminate warpage for lidded 3D stack module.

Figure 3.21 shows the 150→25C in-plane X-field deformation on the center cross section of the 2D lidded package on card. Two line scans are plotted, one along the center of the lid and one along the center of the laminate. The upper schematic in Figure 3.21 explains the locations of measurements. The measurement results are shown as dots, the model as lines. Figure 3.22 shows both X and Y field measurements for 150C→25C for the 3D package with 70um interposer. As can be seen, the model and measurement results are in close agreement. Figure 3.23 shows the 150→100C X and Y fields for the 11x16 on 11x16mm die stack package. Finally, Figure 3.24 shows the X and Y field deformations to room temperature for the 9x13 on 11x16mm die stack package. A common observation from Figs 3.20-3.24 is that the X-field predictions of the model are typically better than the Y-field. As was the case for the warpage measurements, the difference is believed due to the lid and assembly process non-

idealities which affect the Y-direction deformations primarily and would not be captured by the model.

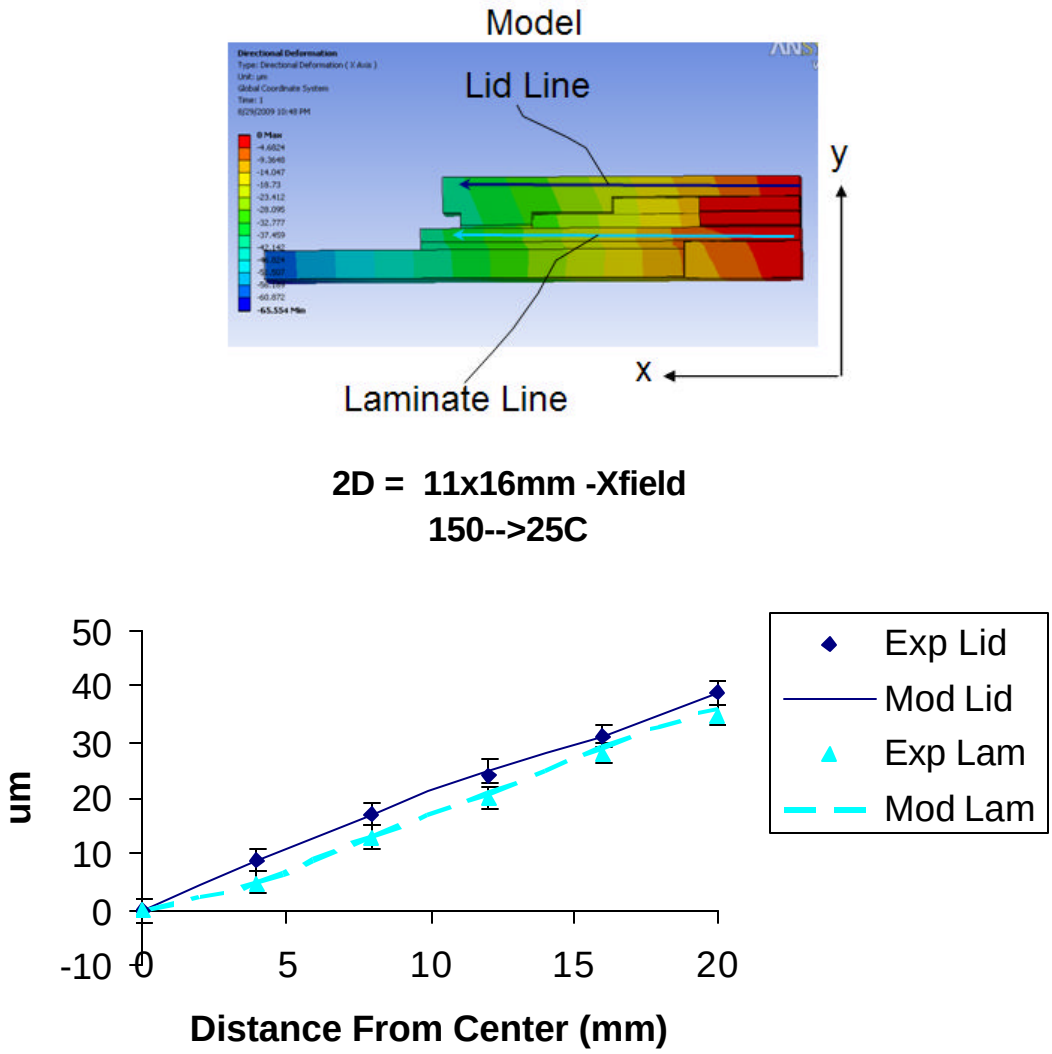
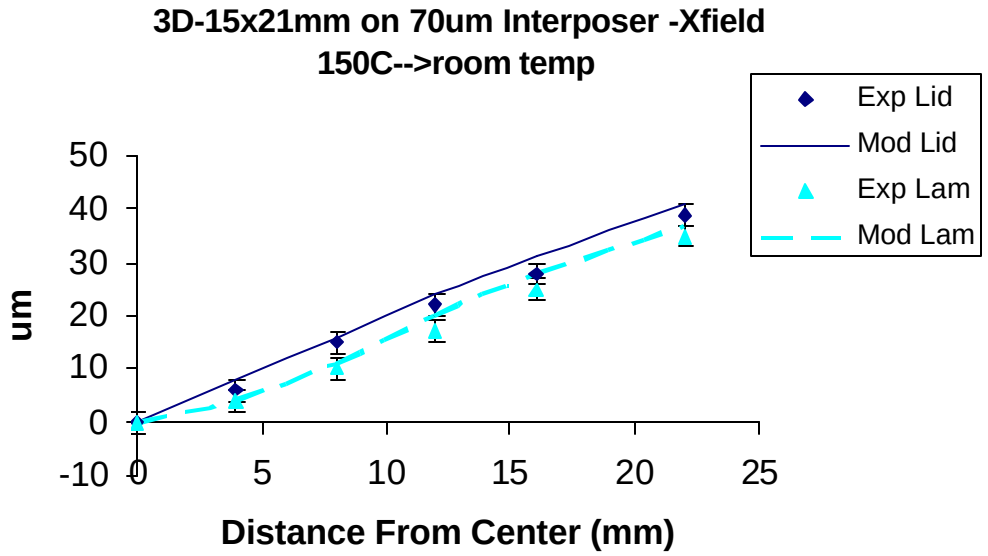
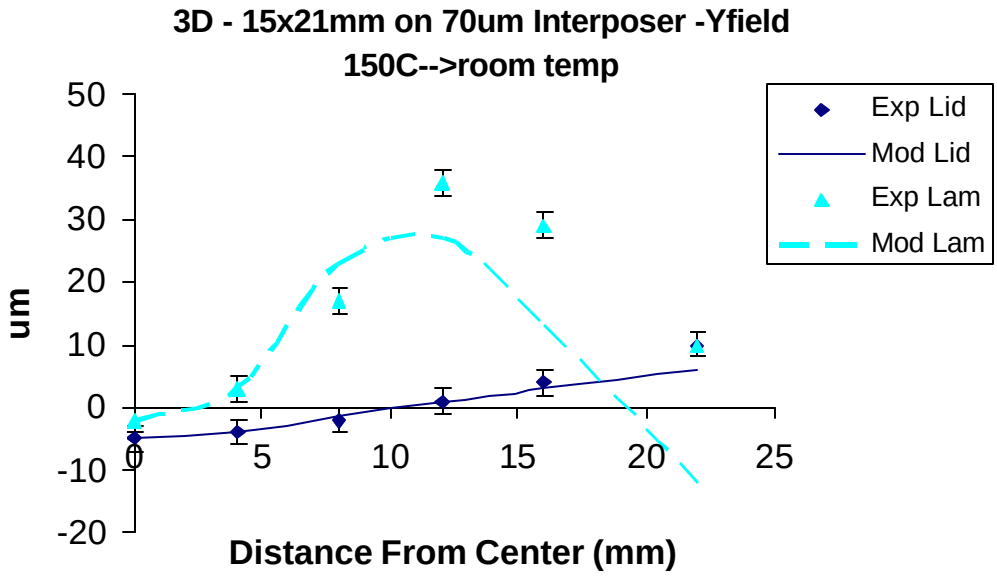


Figure 3.21. X-field deformation of 2D package from 150ºC to room temperature. The top schematic depicts the lid and laminate trace lines for the results

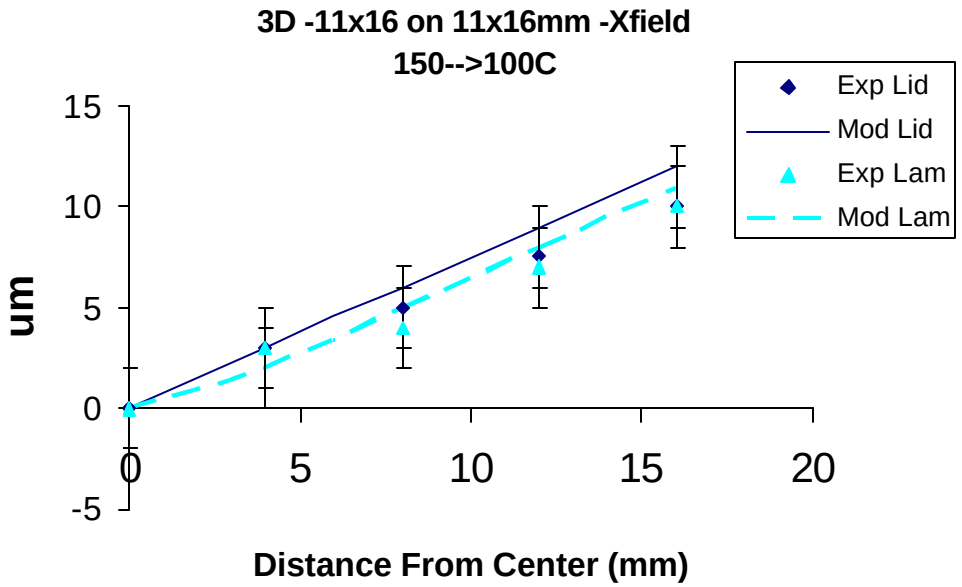


(a)

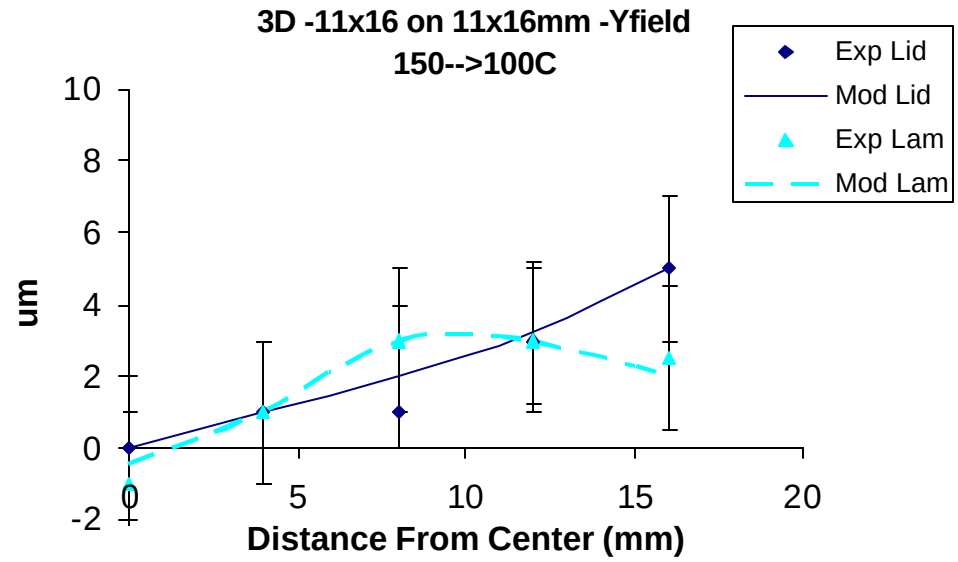


(b)

Figure 3.22 X (a) and Y (b) field deformation of 70µm interposer package from 150C to room temperature.

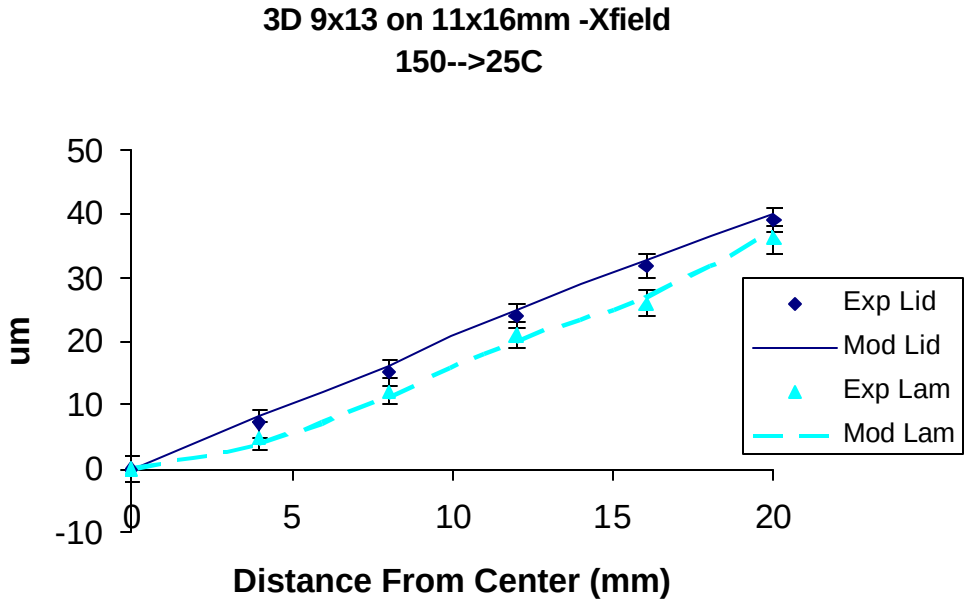


(a)

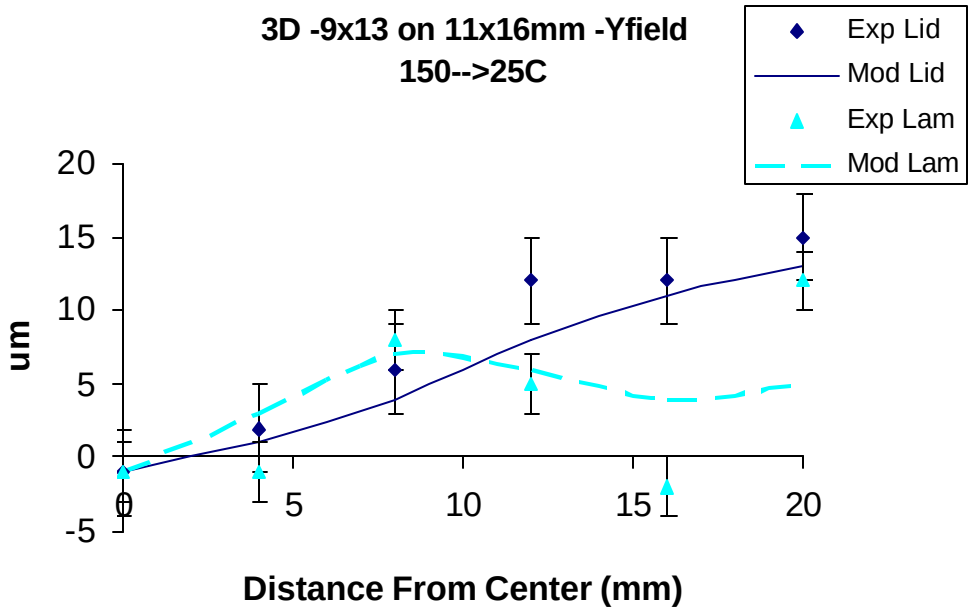


(b)

Figure 3.23 X (a) and Y (b) field deformation from 150ºC to 100ºC for the 11x16 on 11x16mm die stack package.



(a)



(b)

Figure 3.24 X (a) and Y (b) field deformation for 150ºC→25ºC for the 9x13 on 11x16mm die stack package.

Table 3.5 summarizes the elastic mechanical properties generated from the validation measurement results just described.

Table 3.5. Mechanical material properties resulting from validation experiments.

	CTE (ppm/C)	Youngs Modulus (GPa)	Poisson Ratio
C4/Underfill layer	27	12	0.4
Card	17	15	0.2
Lid	16	110	0.34
Laminate	16	25	0.3
Die-Die interf	27	12	0.4
Si	3.5	150	0.28
BGA layer	83	0.4	0.3
Lid Adhesive	240	0.001	0.45
TIM	250	0.00025	0.49

Chapter 4: 2D vs. 3D Package Thermal Response

4.1 OBJECTIVES AND INPUTS

The two objectives of the package thermal analysis were to compare steady state and transient temperature distributions of 2D and 3D packages and compare thermal time constants. The die-die thermal resistance (R_{dd}), and input power distribution were parameters in the study. The validated (see Chapter 3) ANSYS^{TM} conduction model was used for the analysis. Table 4.1 gives the dimensions of the package used for this analysis, which contained an 11x16mm full thickness die on an 11x16x0.07mm high-power die. The thermal boundary conditions were heat transfer coefficients based on typical applications for which the given uniform power distribution resulted in a die average temperature of ~85ºC in a standard 2D package. Table 4.2 summarizes the heat transfer coefficients used. Other assumptions of the analysis were:

- all power was dissipated in the lower thinned die, assumed to be a processor
- all thermal boundary conditions were constant
- all material properties were constant
- the TIM bondline between the top die and the lid for the 3D package was the same as for the 2D case, and based on the validation described in chapter 3.

Table 4.1 Package dimensions modeled.

Card	100x100x1.6mm
Pkg Laminate	42.5x42.5x0.77mm
Pkg Lid	40x40x1.2mm
D1 (bottom die)	11x16x0.07mm
D2 (top die)	11x16x0.78mm
t_{TIM}	30µm
t_m	20µm
t_{C4}	70µm
$t_{\text{lid adhesive}}$	120µm
T_{BGA}	420µm

Table 4.2 Thermal boundary conditions used for the thermal model.

Surface	HTC (W/m^2K)	T-amb (C)
Package Top	1000	29
Other lateral surfaces	10	29
Other vertical surfaces	30	29

4.2 2D VS 3D TEMPERATURE RESPONSE

Figure 4.1 shows the steady state power distributions modeled. Three different scenarios are modeled; a uniform power of $0.34W/mm^2$, a 3X hotspot of 2x2mm at center, and a 10X power density hotspot of 2x2mm at die center.

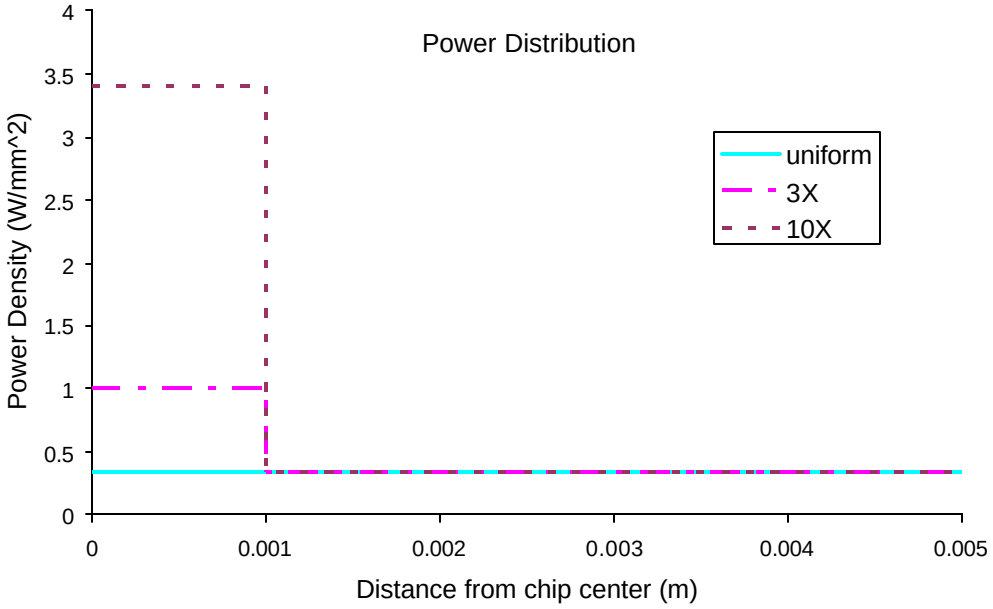
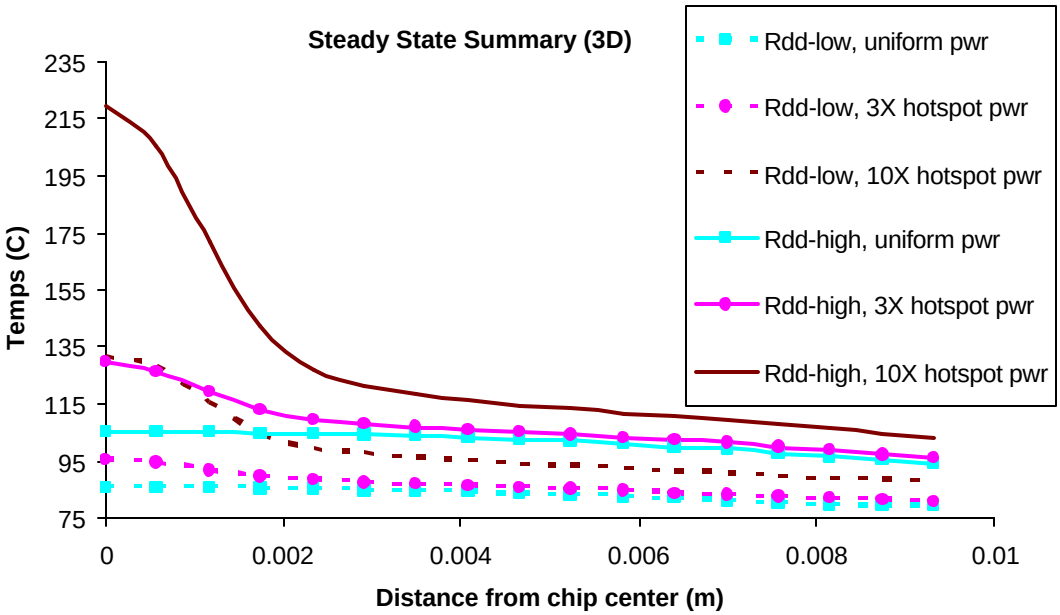
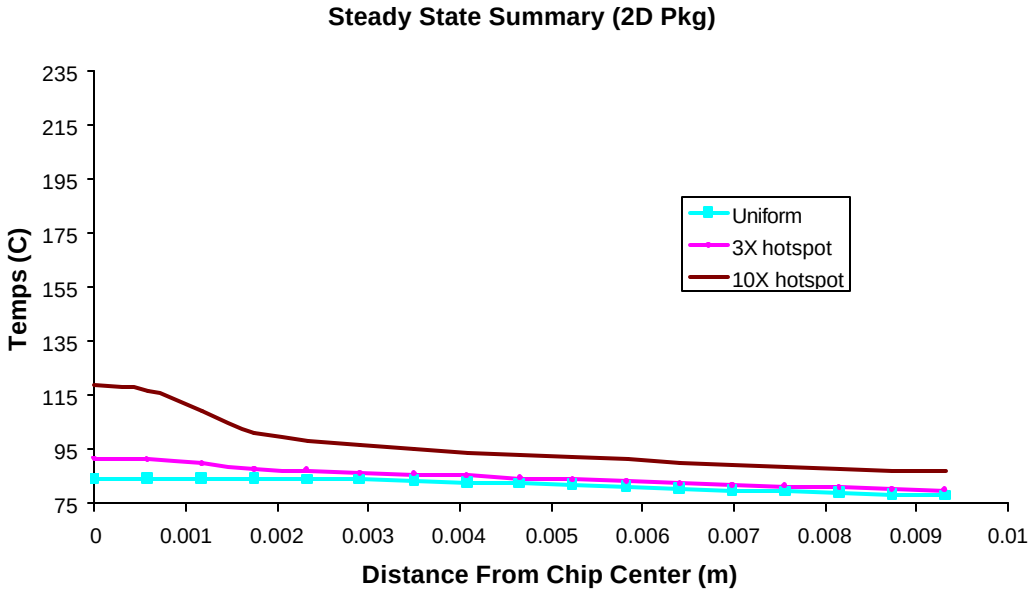


Figure 4.1. Power density distributions modeled on lower die active surface.

The resulting steady state temperature distributions are shown in Figure 4.2a for 3D packages and Figure 4.2b for 2D. The temperatures are for the lower (processor) die for the 3D cases. Two different resistances for the die-die interface (R_{dd}) are modeled for the 3D cases, a low value of 5Cmm^2/W and a high value of 80Cmm^2/W. R_{dd} represents both the BEOL and micro-C4s between the die. The resistance values used represent extreme ranges of resistances for solder joints of 20µm and the BEOL in series. Underfilled micro-C4s or direct copper bonding would be closer to the low end, and non-underfilled micro-C4s would be closer to the high end. The dotted lines represent the low R_{dd} results, while the solid ones are for the high. The first conclusion for the 3D packages is that the low R_{dd} produces significantly lower overall temperatures, as expected. The higher power density hotspot temperatures are proportionally much higher with the high R_{dd}. The lowest temperatures for each power distribution are for the 2D package, as expected.



(a)



(b)

Figure 4.2. Steady state temperature distributions resulting from the power profiles of Figure 4.2 for 3D (a) and 2D (b) packages. R_{dd} low =5Cmm^2/W, R_{dd} high = 80Cmm^2/W.

A 'radius of hot spot influence' is defined as the farthest distance from the hotspot center at which the temperature is still perturbed by the hotspot. This is arbitrarily designated as the point at which the lateral special temperature gradient starts to deviates significantly from the one resulting from uniform power. Figure 4.3 shows the temperature gradients for the 10X hotspot case. The radius of hot spot influence is approximately ~3mm for the 2D case as compared to ~4mm for the 3D with high R_{dd}.

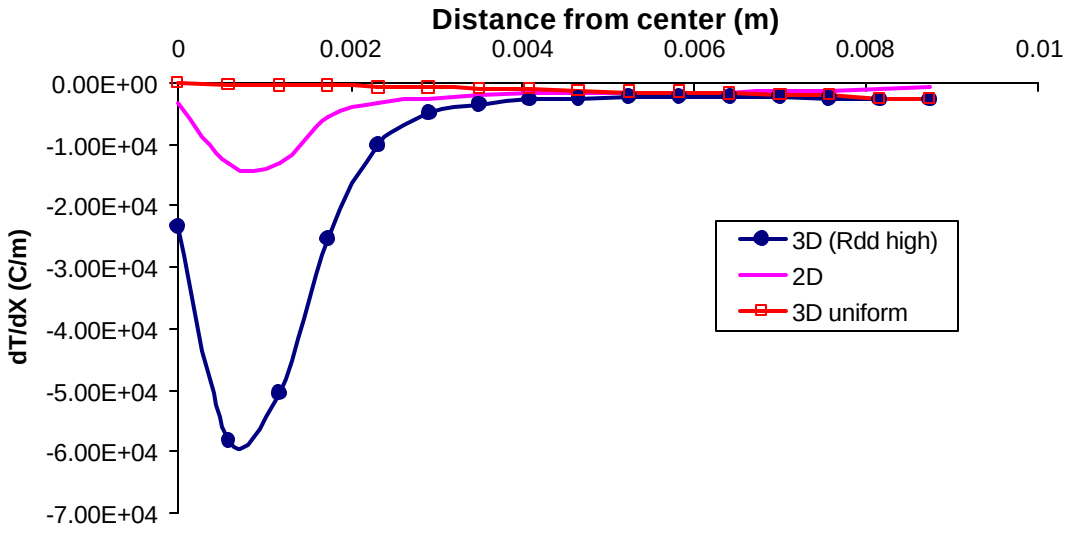
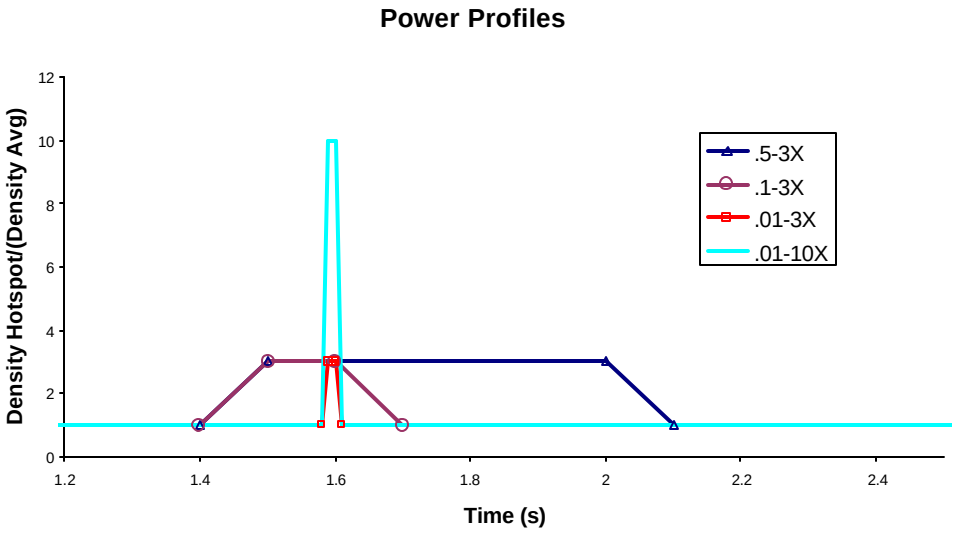


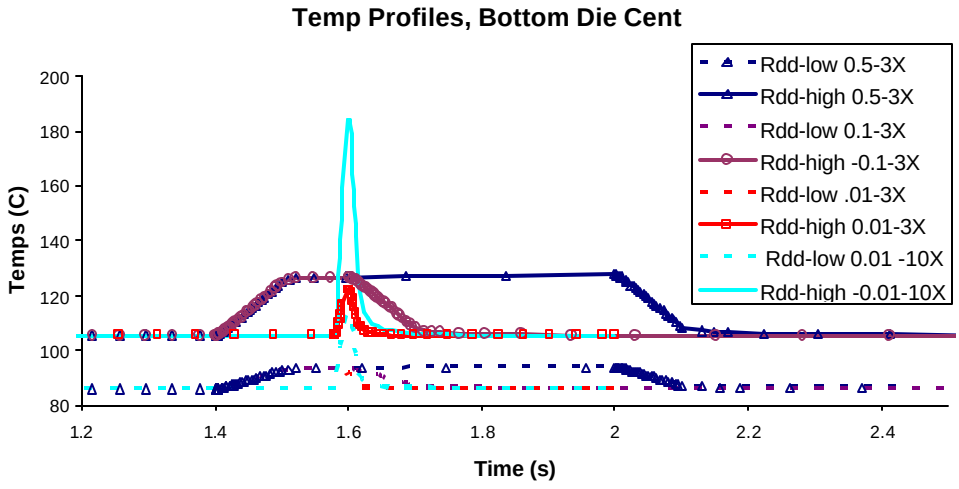
Figure 4.3. Temperature radius of influence comparing 2D and 3D with 10X hotspot vs. 3D with uniform power.

Several different transient temperature profiles were also modeled. In each case, the hotspot was turned on and off for different time periods. Figure 4.4a shows the hotspot power density ratio vs. time profiles. The legend designations are pulse duration and power density increase over the uniform case. For example, 0.5-3X implies a pulse of 0.5secs with a hotspot power density 3X that of the rest of the chip. The time steps used in the modeling were always two orders of magnitude smaller than the pulse duration during the power transient, to ensure adequate capture of the temperature

response. The resulting temperature responses for the center of the lower die are shown in Figure 4.4b. Again, the low R_{dd} cases are shown as dotted lines, and those with high resistance are solid. Clearly the 10X power spike produces a significant temperature rise that is well beyond the increase for the uniform power case (before 1.4 secs).



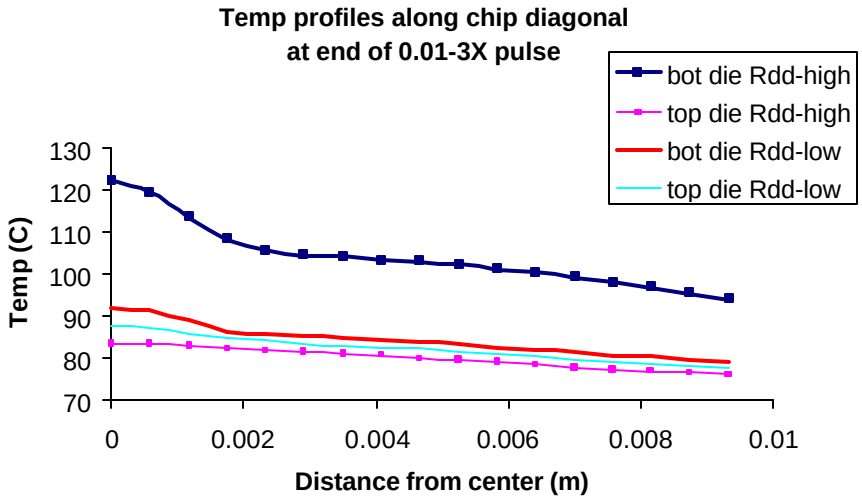
(a)



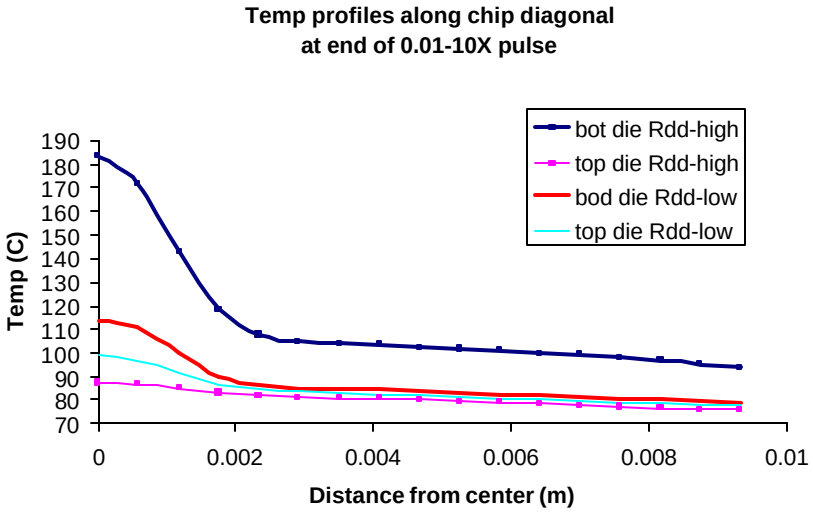
(b)

Figure 4.4. Transient power profiles (a) and max temperature responses (b).

Figures 4.5a and 4.5b show the temperature distribution at the end of the 3X and 10X power density spikes, respectively, for the bottom and top die, with high and low R_{dd}. As can be seen, the top die temperature is lower with high R_{dd}, and the temperature non-uniformity is also less due to the thermal insulative effect of the R_{dd} below the die.



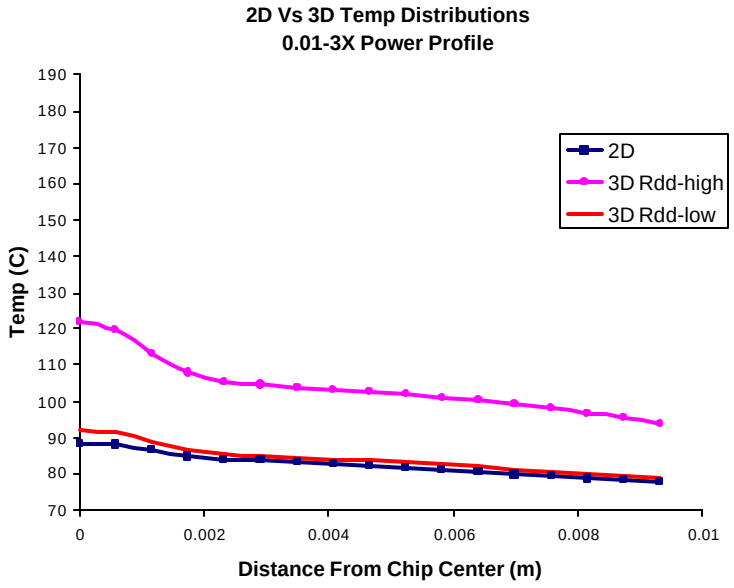
(a)



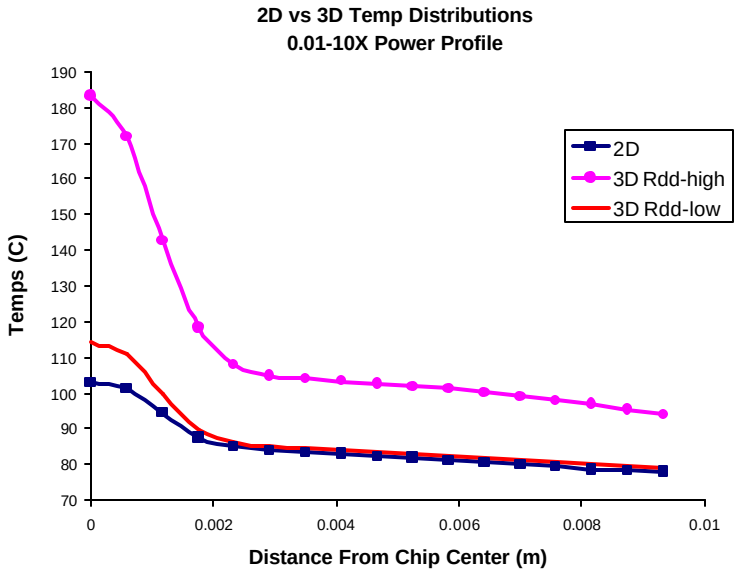
(b)

Figure 4.5 Temperature profiles along chip diagonal at the end of 3X (a) and 10X (b) power density hotspot spike, showing bottom and top chip temperatures

Figures 4.6 and 4.7 compare the 2D and 3D temperature distributions to 0.01-3X and 0.01-10X input hotspot power densities. The temperature distributions are shown at the end of the power spike in Figure.4.6 and vs. time for the max temperature in 4.7

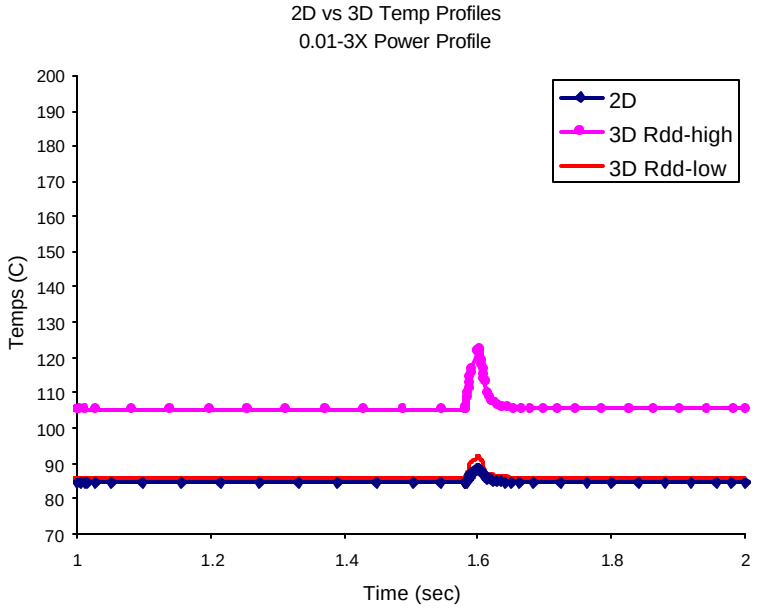


(a)

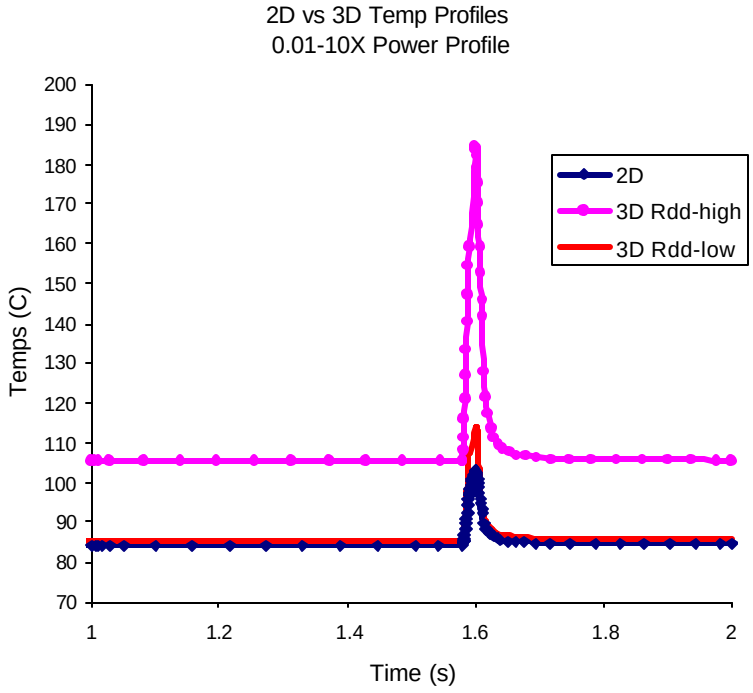


(b)

Figure 4.6. Comparison of 2D and 3D temperature distributions at the end of 0.01-3X hotspot power spike (a) and 0.01-10X (b).



(a)



(b)

Figure 4.7. Comparison of 2D and 3D temperature responses to hotspot power spike of 0.01-3X (a) and 0.01-10X (b).

4.3 TIME CONSTANT ANALYSIS

The time to reach 63.2% of peak temperature rise was analyzed for the 3D and 2D packages. Figure 4.8 shows the temperature/time response when the whole chip is powered uniformly to X=0.34W/mm^2. The 3D cases are modeled with high (80Cmm^2/W), medium (20Cmm^2/W) and low (5Cmm^2/W) R_{dd}. Figure 4.9 summarizes the time constants calculated from the uniform power step response. As can be seen, the time constants decrease with increasing R_{dd}, and are highest for the 2D case. Note that the range of values for all the cases studies is ~6-9 seconds. Also note that a larger time constant is desired in general for power management.

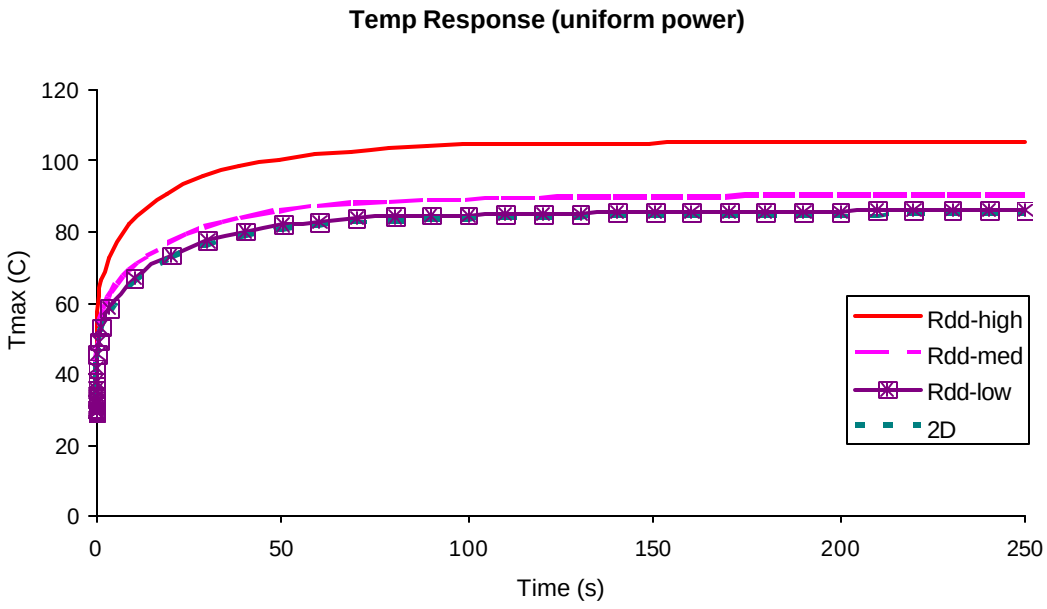


Figure 4.8. Temperature response with uniform power applied to entire chip, with different die-die interface resistances R_{dd} for the 3D cases.

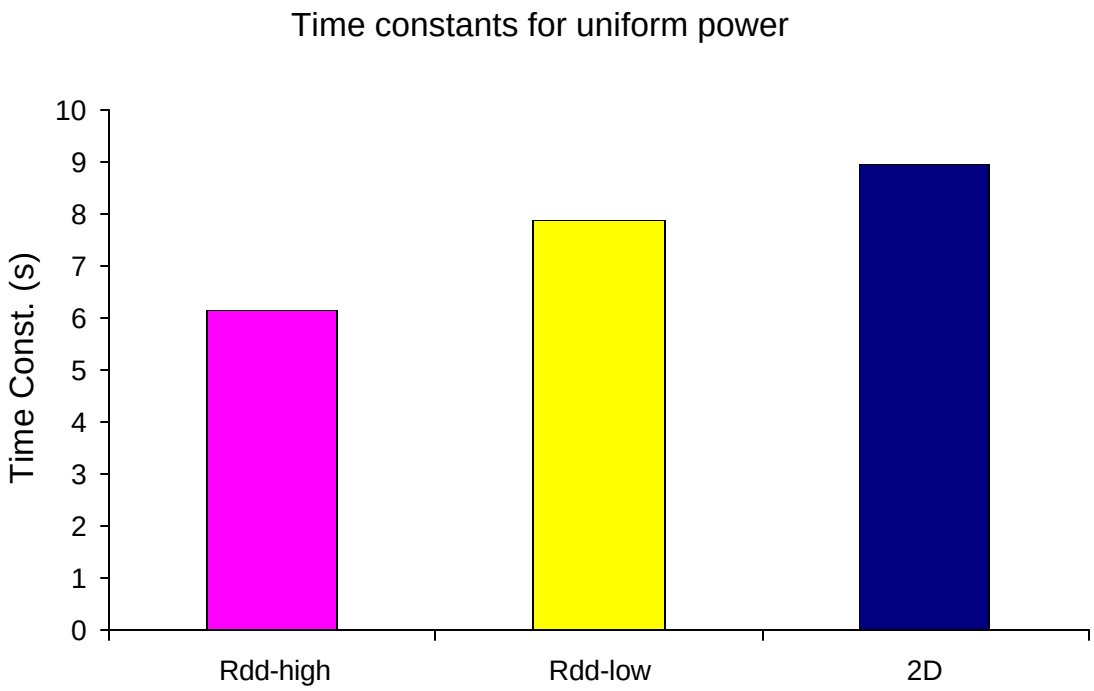


Figure 4.9. Time constants calculated with uniform power over entire chip.

The time constants in which the hotspot was powered for the 2D and 3D cases are shown in Figure 4.10. The hotspot region is 2x2mm at die center, as discussed previously. It is clear that the lower R_{dd}, the higher the time constant, and that the impact of R_{dd} and percent difference between the cases is greater than in the uniform power case. The 3D case with high R_{dd} has the smallest time constant. The time constants for the hotspots are in the millisecond range, as opposed the full chip power cases which are more than two orders of magnitude larger.

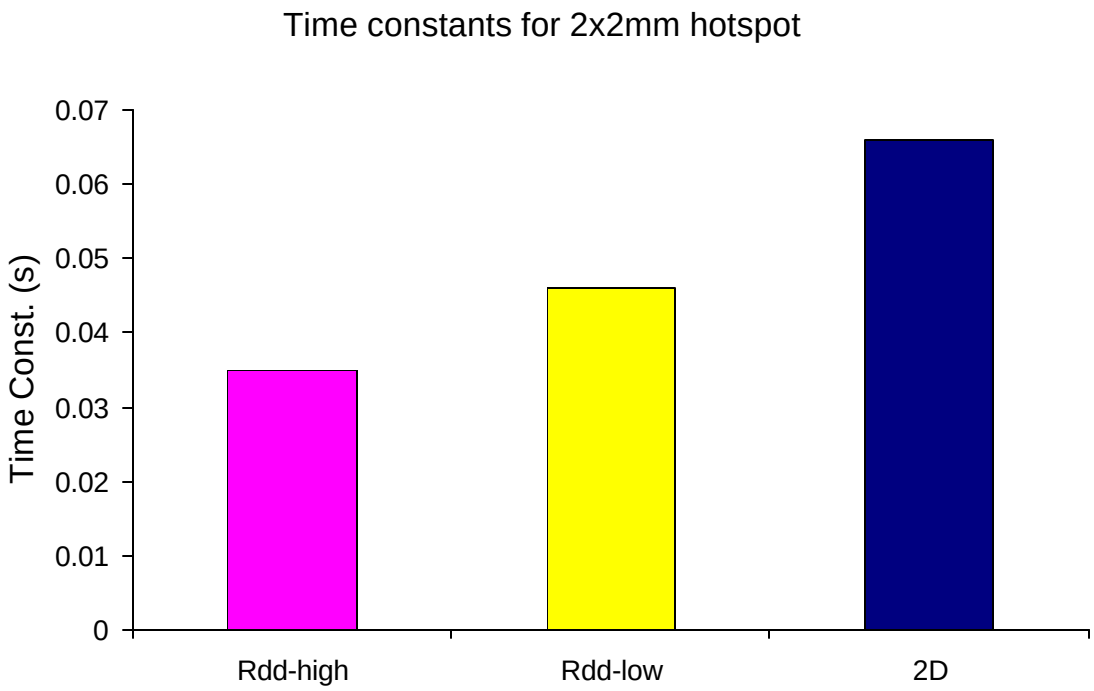


Figure 4.10. Time constants for the hotspot with various die-die interface resistances.

4.4 CONCLUSIONS

The results showed significant difference in 2D vs. 3D temperature responses in which the 3D package contained a high die-die interface resistance R_{dd}. This difference was exacerbated when hotspots or short term power transients were involved. The time constants showed significant range for different levels of heating area under consideration. Thermal-awareness (both spatially and temporally) is a key consideration at the design time for 3D microprocessor architectures. The results suggest local effects and time constants need to be considered in addition to the typical steady state temperature rise in a uniformly heated 3D package.

Chapter 5: 2D vs. 3d Package Mechanical Analysis

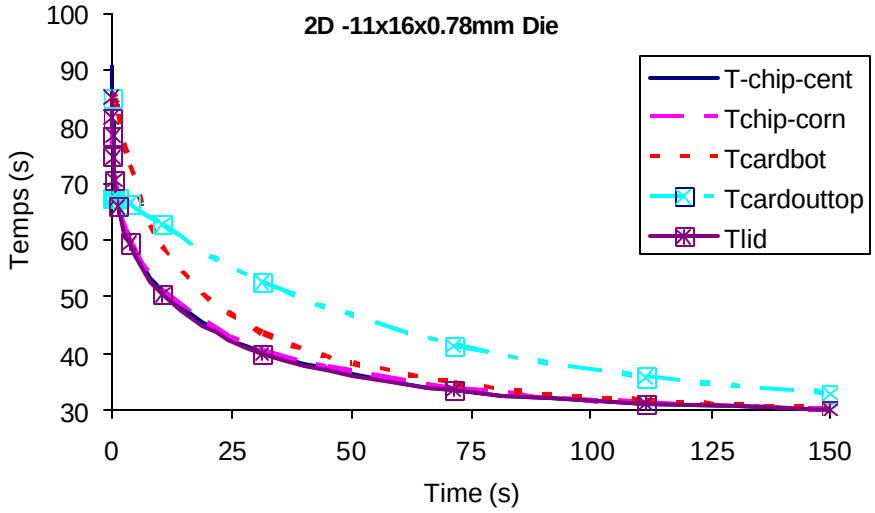
5.1 OBJECTIVES AND INPUTS

The objectives of the package mechanical analysis were to compare 2D vs. 3D TIM strains, chip/package interaction and warpage during the cool down stage from a powered condition. Of particular interest were any peaks in stress or strain that could be missed in the powered or room-temperature-only analysis. The main parameters in the study were the die and micro-C4 layer thicknesses.

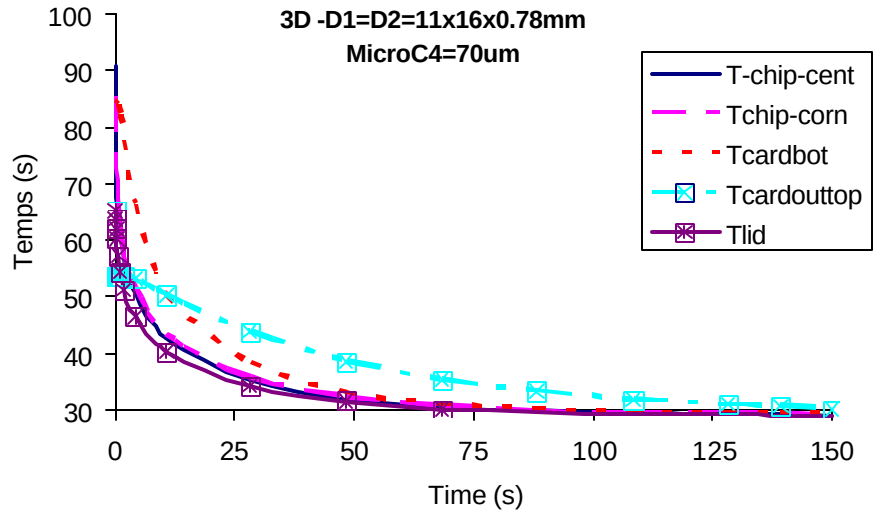
The validated model described in Chapter 3 was used, with the material properties described in Table 3.5. The same package design was used as for the thermal analysis of chapter 5 (see Table 5.1 for dimensions). The mechanical boundary conditions included a 100 Newton heat sink load on the package and a zero displacement constraint at die center. The following general assumptions were used:

- The thermal boundary conditions for each scenario were heat transfer coefficients which resulted in chip average temperatures of approximately ~85ºC, an arbitrary but realistic temperature for electronic devices.
- The system cooling was maintained as the die power was shut off.
- All material properties were constant.

Figure 5.1 shows sample temperature profiles for the 2D (a) and a two-layer 3D stack (b). The die center and corner, card bottom and car outside top, and lid temperatures are shown. As can be observed, the 3D package has a faster cool down rate due to the lower external thermal resistance necessary for the 3D stack to maintain the same chip temperatures during operation. The 3D case has a worse case die-die interface resistance based on the 70µm micro-C4 (or microjoin) height which would correspond to the R_{dd} = high value (~80Cmm^2/W) as designated in Chapter 5.



(a)



(b)

Figure 5.1 Temperatures while cooling down from power-on state for 2D package (a) and 3D stack (b) with two 785µm die layers, and micro-C4 =70µm tall.

5.2 RESULTS

Figures 5.2-5.3 show the die warpage during the cool down process as a function of time, die thickness, and micro-C4 layer thickness. Different top die (TD), bottom die (BD) and micro-C4 (microjoin or mj) thicknesses are evaluated. It can be observed that in relation to the different 3D designs, the 2D has one of the highest die warpages. The lowest warpages are for the thinnest and thickest combination of top die + bottom die + micro-C4s (70+70+7µm as well as 785+785+70µm).

Figure 5.3 plots the die warpage as a function of die thickness (a) and micro-C4 layer thickness (b) for three different time periods in the cool down process: 0 secs = power on, 4 secs = transition, 120 secs = ~ power off (uniform temp). The X-axis in 5.3a is the top die thickness if the bottom die is kept constant (at 785um), or the bottom die if the top die is constant. In 5.3b, the top and bottom die are constant at 785 and 70um, respectively, while the micro-C4 thickness is varied (X-axis). From 5.3a it can be seen that the die warpage reduces as either of the chip thicknesses is increased and makes little difference which one is thinner or thicker (comparison of dotted and solid lines). From 5.3b we observe the micro-C4 thickness has negligible impact on die warp.

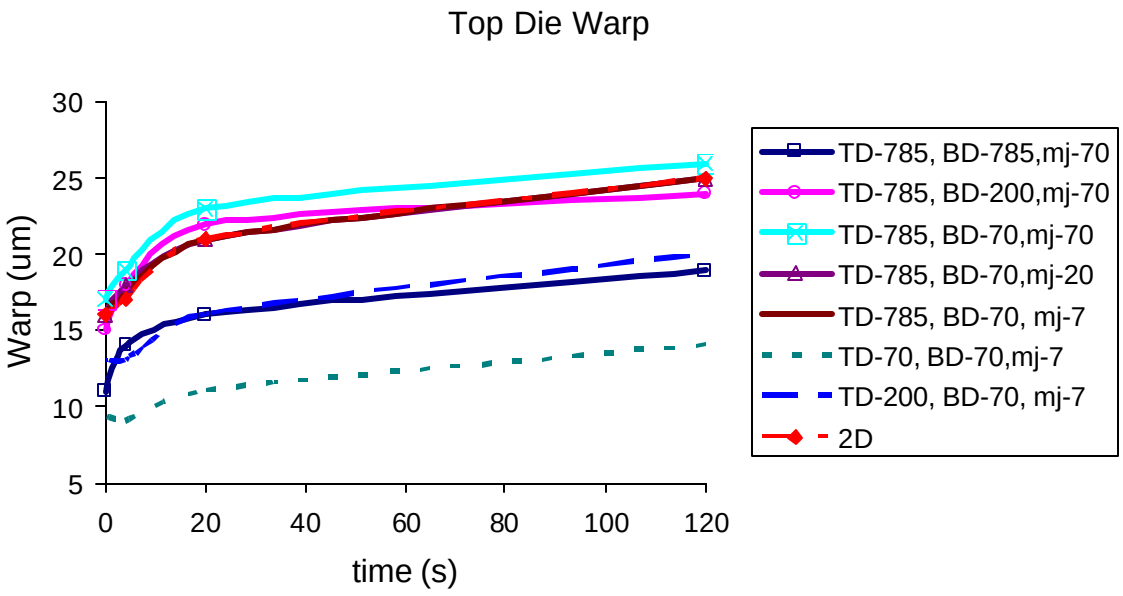
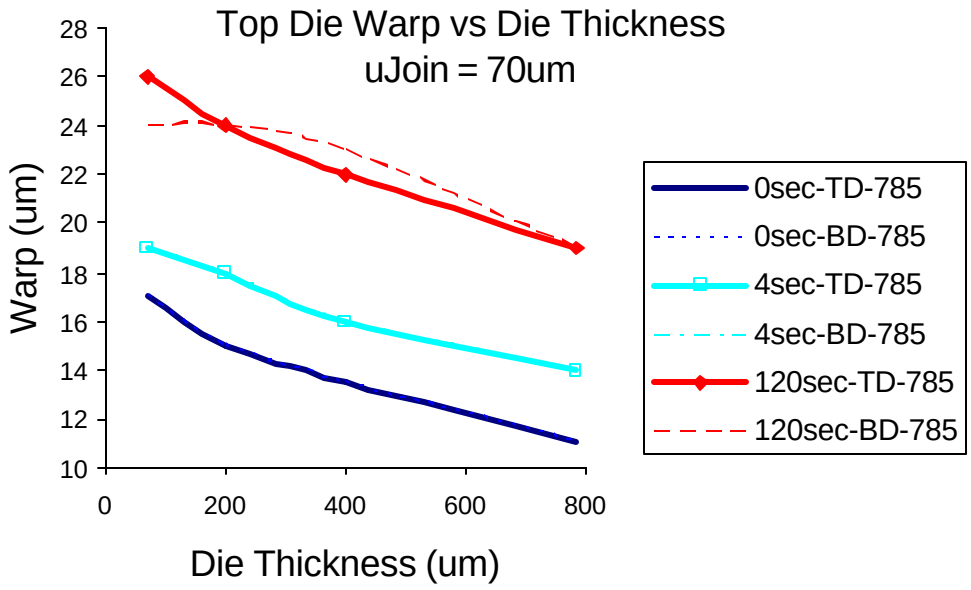
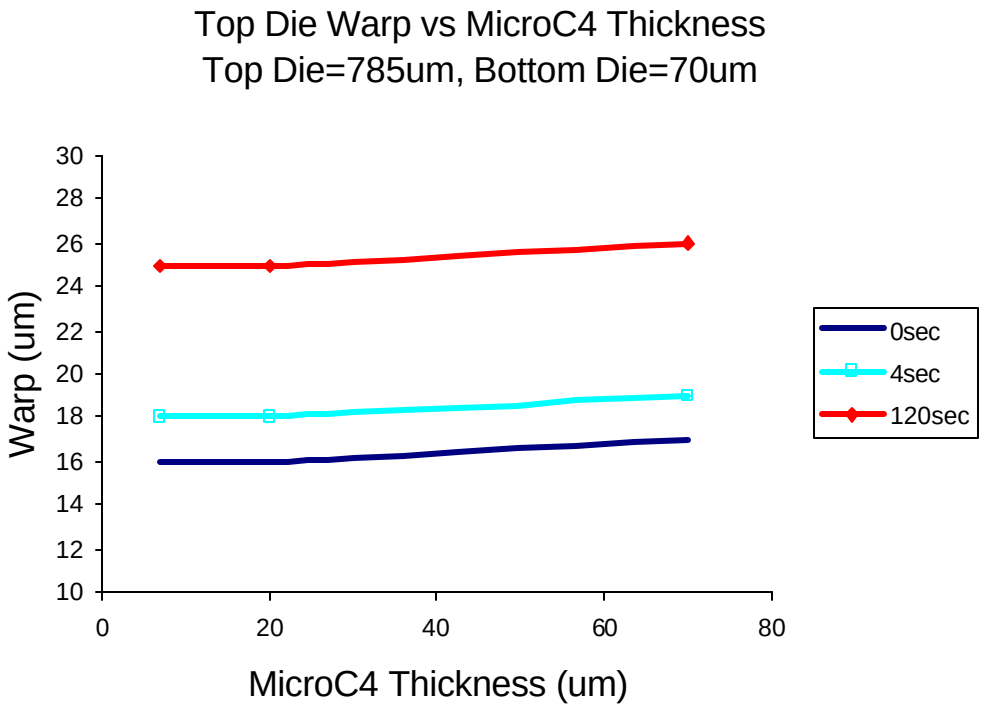


Figure 5.2 Top die warp as a function of time for the cool down ramp shown in Fig. 5.1. TD=top die, BD=bottom die, mj=microjoin or micro-C4.



(a)



(b)

Figure 5.3. Die warpage for 3D stacks as a function of die thickness (a) and micro-C4 thickness (b).

Figures 5.4-5.5 have similar information for the laminate warpage. Figure 5.4 shows laminate warpage as a function of time, comparing the 2D case to 3D stacks with different component thicknesses. As can be seen, all the 3D stack configurations have lower laminate warpages than the 2D, with the lowest being the thickest and thinnest stacks. Figures 5.5a and 5.5b show the same information but as a function of die thickness (a) and the micro-C4 thickness (b). Again, three different time periods are plotted. One observation from 5.5a is that there seems to be some influence as to which die (top or bottom) is thinner or thicker (comparing dotted curves to solid curves). In general, if the bottom die is thinner, the laminate warpages are slightly higher than if the top is thinner. It can also be observe from 5.5b that although the power-off (~120 sec) condition has the highest laminate warpage as expected, the transition stage (4 sec) is actually lower than the initial power-on state. The micro-C4 thickness does not seem to impact the laminate warpage significantly.

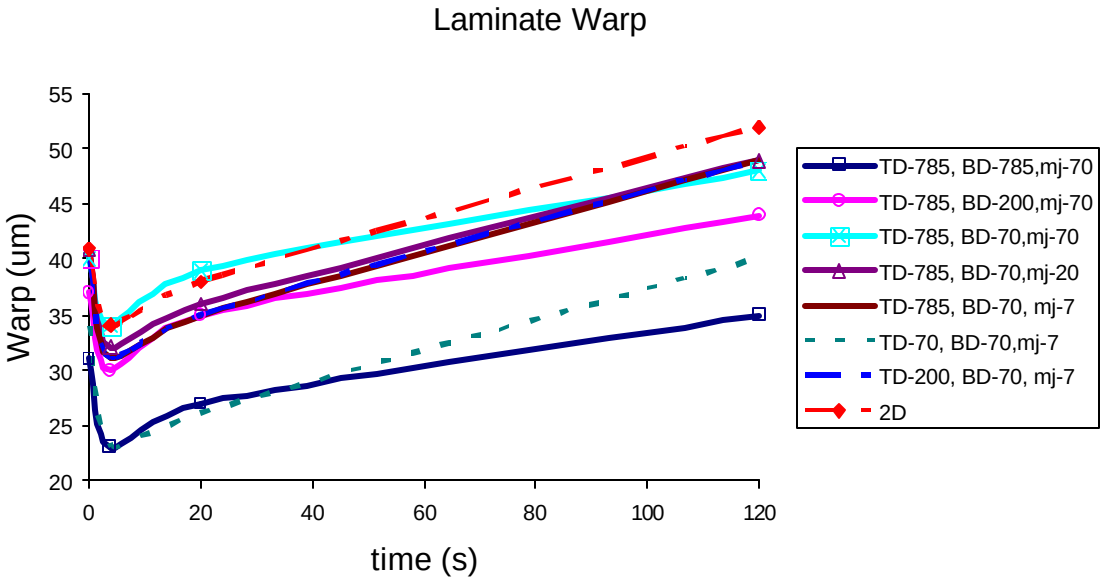
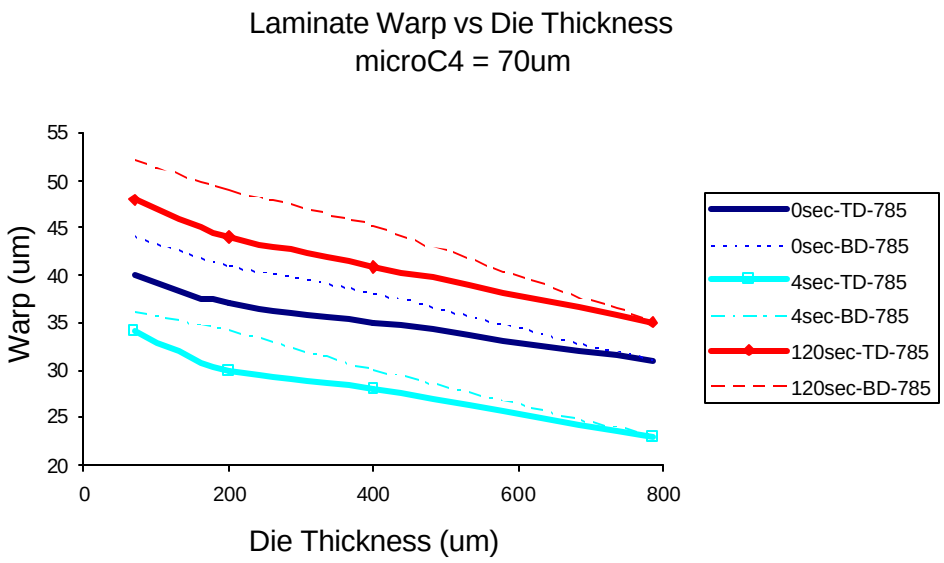
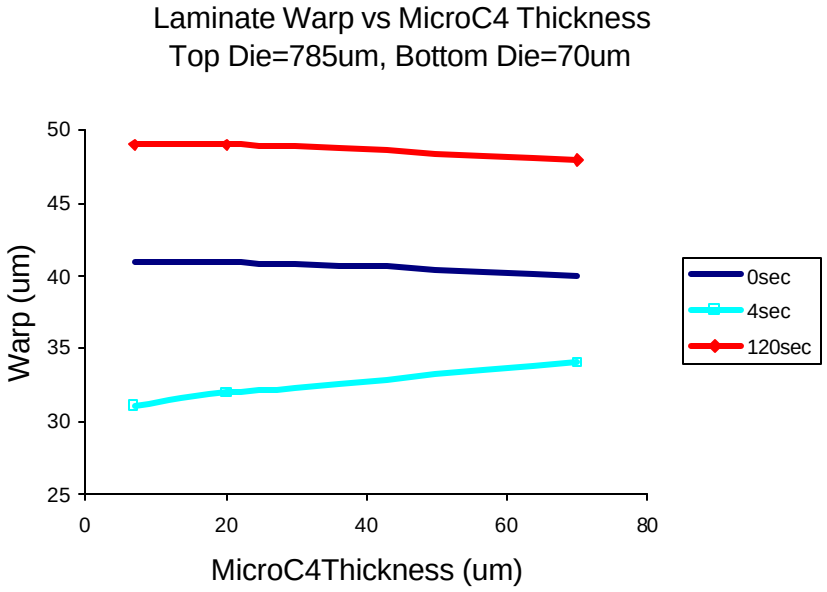


Figure 5.4 Laminate warpage as a function of time for the cool down process shown in Fig. 5.1. TD=top die, BD=bottom die, mj=microjoin or micro-C4.



(a)



(b)

Figure 5.5. Laminate warpage as a function of die thickness (a) and micro-C4 thickness (b).

Figures 5.6-5.7 show the TIM equivalent strain results during the cool-down stage. It is interesting to note from Figure 5.6 that although the die and laminate warpages were lower for the 3D stacks as compared to the 2D, the TIM strains are in fact higher for most of the 3D cases. This can be explained by the lower lid warpage (not shown) and emphasizes the point made in the chapter introduction, that these results are somewhat design dependent. A change in the lid design could alter the conclusions. The only 3D cases with lower TIM strains are the two lowest overall thickness stacks. Figures 5.7a and 5.7b show the same information, but now as a function of die thickness and micro-C4 thickness. From 5.7a, for the cases where the top die is thinner (dotted lines, BD=785µm), the TIM strain has a linear increase with die thickness. For cases where the bottom die is thinner (solid lines, TD=785µm), there is a minimum warp around 200um for the powered-off state (~120 sec). From 5.7b, the powered-off state TIM strain decreases slightly with increasing micro-C4 thickness, while for the power-on and transition stages it increases.

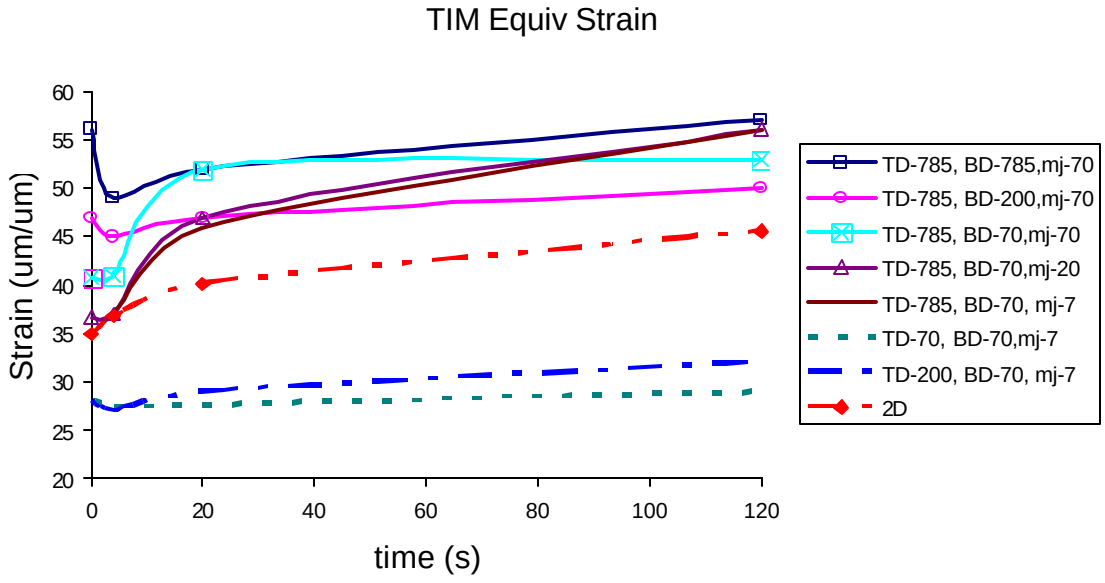
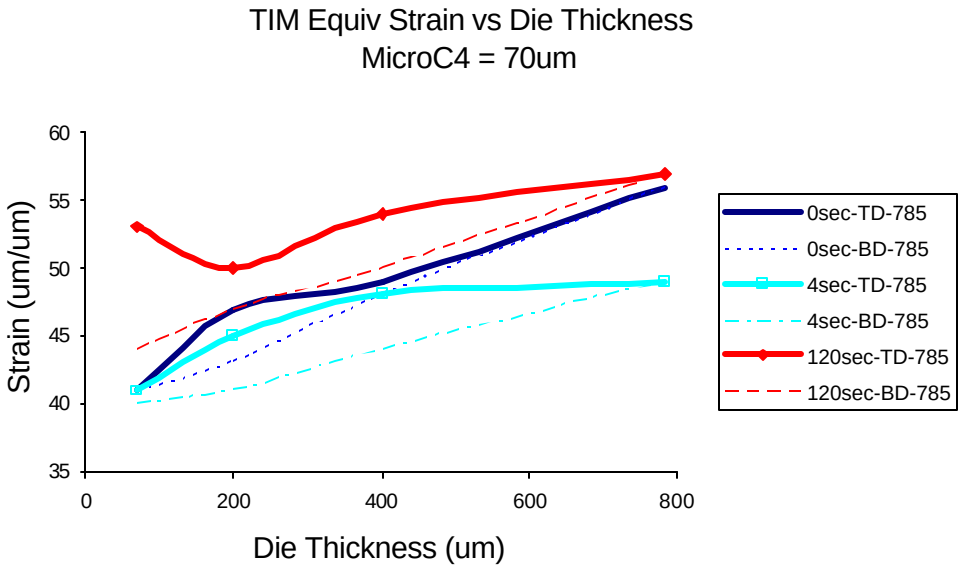
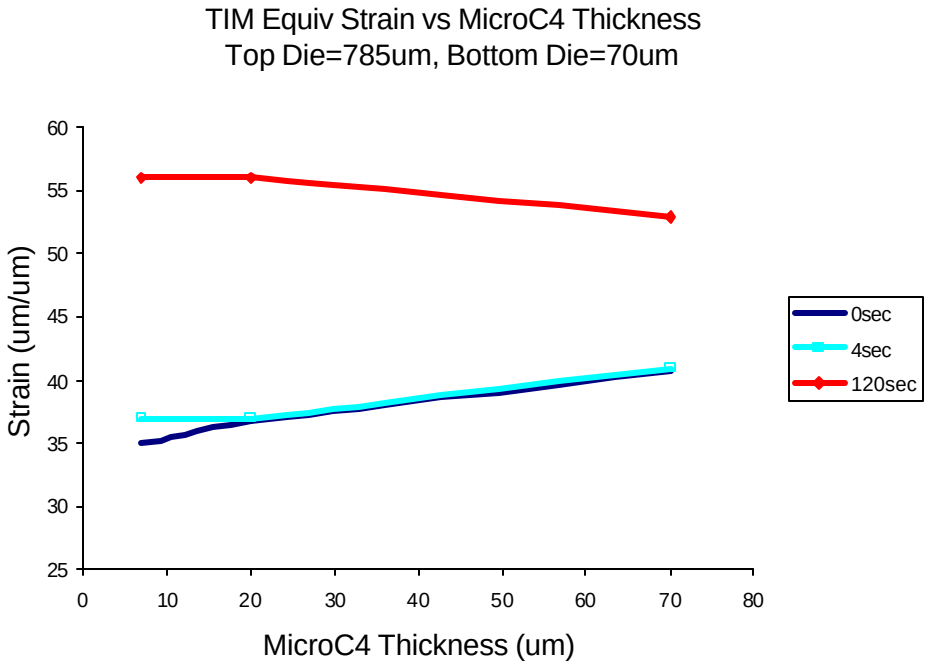


Figure 5.6 TIM equivalent strain as a function of time for the cool down ramp shown in Fig. 5.1. TD=top die, BD=bottom die, mj=microjoin.(micro-C4).



(a)



(b)

Figure 5.7. TIM equivalent strain as a function of die thickness (a) and micro-C4 thickness (b).

Figure 5.8 shows the bottom die shear (on the lower surface), which can be used as a metric for assessing chip package interaction (CPI) reliability. Here it can be concluded that all 3D cases should have lower CPI concerns than the 2D. It can also be noted that the thinnest stacks have the least die shear stress and thus CPI concern. Figures 5.9a and 5.9b show the same information but as a function of the die thickness and micro-C4 thickness for three time periods. From 5.9a we observe that the die-bottom shear increases with die thickness and is not influenced by the micro-C4 thickness in the range studied.

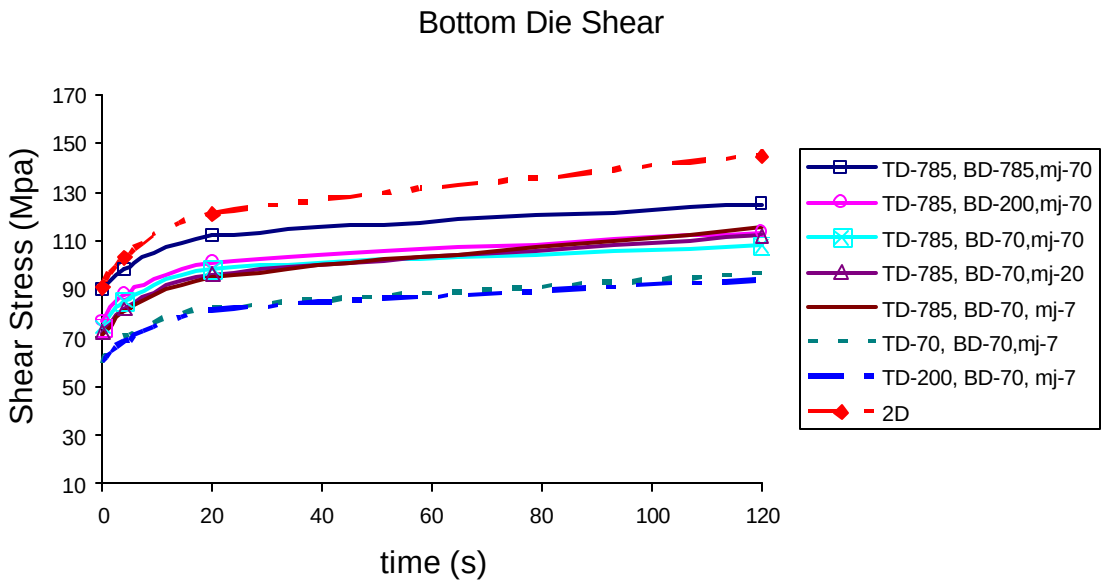
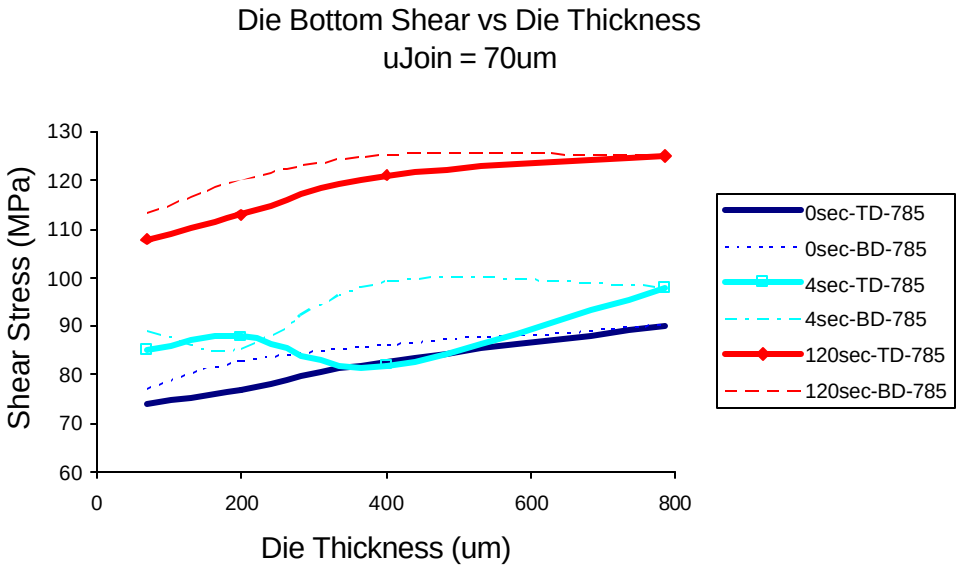
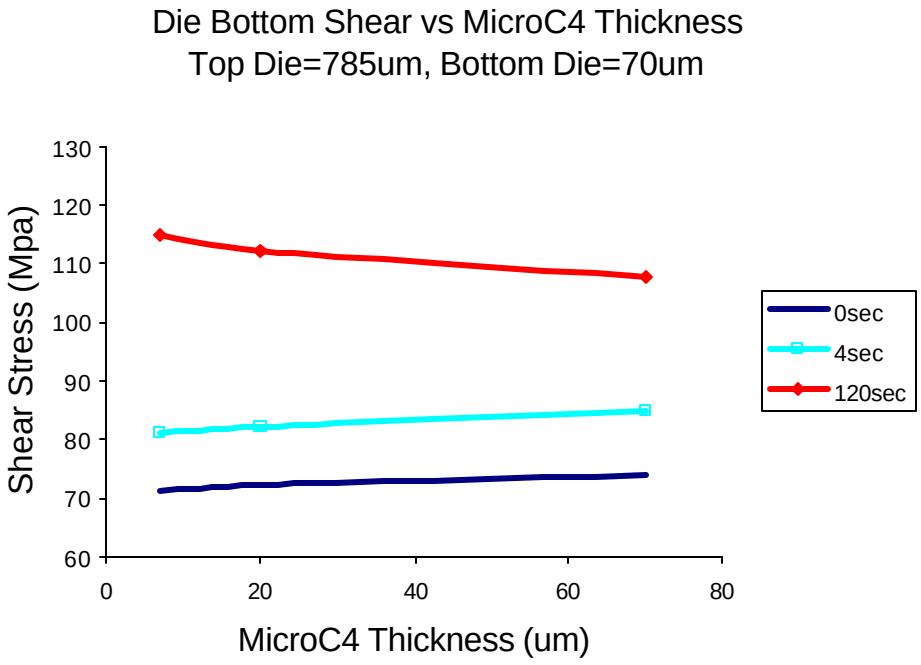


Figure 5.8 Die bottom shear as a function of time for the cool down ramp shown in Fig. 5.1. TD=top die, BD=bottom die, mj=microjoin.



(a)



(b)

Figure 5.9. Die bottom shear stress as a function of die thickness (a) and micro-C4 thickness (b).

5.3 CONCLUSIONS

This analysis served as an example of the contrast between 2D and 2D mechanical behavior under transient conditions. Although dependent on the geometry chosen for comparison, such as laminate and lid design of the package, the following conclusions can be drawn:

- The fact that die and laminate warpages are lower for 3D stacks does not necessarily indicate lower TIM strains.
- The lower warpages do indicate less stress on the laminate-die interface and reduction in CPI stress for 3D stacks compared to 2D
- No significant peaks were observed in the stresses and strains analyzed during the transition period from power-on to power-off as compared to the steady state periods

References

1. Newman, M., et al., "Fabrication and Electrical Characterization of 3D Vertical Interconnects", Proceedings, 2006 Electronic Components and Technology Conference.

2. Wu, L. et al, "The Advent of 3-D Package Age", Proceedings, 2000 IEEE/CPMT Symposium.

3. Mohammed, I, et al, "A Design and Performance Study of 3D Packaging for High Performance Memory Applications", Proceedings, 2003 IEEE/CPMT/SEMI Symposium.

4. Pozder, S. et al, "Exploration of the Scaling Limits of 3D Integration", Proceedings, Material Research Society Symp. Vol 970, 2007.

5. Wunderle, B. et al, " Thermo-mechanical Reliability of 3D-Integrated Microstructures in Stacked Silicon", Proceedings, MRS Symposium, Vol. 970, 2007.

6. Morrow, et. al, "Design and Fabrication of 3D Microprocessors", Proceedings, MRS Symposium, Vol 970, 2007.

7. Takahashi, K., et al., "Process Integration of 3D Chip Stack with Vertical Interconnection", Proceedings, 2004 Electronic Components and Technology Conference.

8. De Moor, P. et al., "Recent Advances in 3D Integration at IMEC", Proceedings, MRS Symp. Vol 970, 2007.

9. Topper, M., et al., "Technology Requirements for Chip-On-Chip Packaging Solutions", Proceedings, 2005 Electronic Components and Technology Conference.

10. Miettinen, et al., "System design issues for 3D system-in-package (SiP)" Proceedings, 2004 Electronic Components and Technology Conference.

11. Li, J. et al., "Post-placement Thermal Via Planning for 3D Integrated Circuit", Proceedings, 20006 IEEE APCCAS Conference.

12. Black, B. et al. "Die Stacking (3D) Microarchitecture", Proceedings, 2006 IEEE/ACM International Symp. On Microarchitecture, MICRO-39.

13. Ranganathan, N., et all, "High Aspect Ration Through-Wafer Interconnect for Three Dimensional Integrated Circuits", Proceedings, 2005 Electronic Components and Technology Conference.

14. Hon, R. et al, "Multi-stack Flip Chip 3D packaging with Copper Plated Through Silicon Vertical Interconnection", Proceedings, 2005 Electronic Components and Technology Conference.

15. Bower, C., et. al., "High Density Vertical Interconnects for 3-D Integration of Silicon Integrated Circuits", Proceedings, 2006 Electronic Components and Technology Conference.

16. Lo, W., et al, "Development and Characterization of Low Cost Ultrathin 3D Interconnet", Proceedings, 2005 Electronic Components and Technology Conference.

17. Hossain, M., et al., "Reliability of Stack Packaging Varying the Die Stacking Architectures for Flash Memory Applications", Proceedings, 2006 IEEE Semitherm Symposium.

18. Noritake, C., Thermal Cycle Reliability of 3D Chip Stacked Package Using Pb-free Solder Bumps: Parameter Study by FEM Analysis", Proceedings, 2006 EuroSimE Conference.

19. Gerlack, D and Y Joshi, "Parametric Thermal Modeling of 3D stacked Chip Electronics with Interleaved Solid Heat Spreaders", Proceedings, 2006 IEEE Intersociety Conf on Thermal.

20. Wong, E., et al., "Effective Thermal Via and Decoupling Capacitor Insertion For 3D System-On-Package", Proceedings, 2006 Electronic Components and Technology Conference.

21. Saini, M., "Theoretical Model Based Thermal Studies on Stacked Dies", Proceedings, 2006 IEEE Intersociety Conf on Thermal.

22. Mao, C.Y., et al, "Packaging Parameter Analysis on Solder Joint Reliability for Twin Die Stacked Packages by Variance in Strain Energy Density of Each Solder Joint", Proceedings, 2006 IEEE Electronics System Integration Tech. Conference.

23. Khan, N. et al, "Development of 3D Stack Package Using Silicon Interposer for High Power Application", Proceedings, 2006 Electronic Components and Technology Conference.

24. Gill,J., et. al., "Joule Heating Considerations in Metallization Reliability and the Impact of Thermal Conductivity", Proceedings, 2004 Advanced Metallization Conference.

25. Chiang, T., et. al., "Effect of Via Separation and Low-k Dielectric Materials on the Thermal Characteristics of Cu Interconnects", IEEE-IEDM 2000.

26. Chiang, T. et al., "Closed-form Analytical Thermal Model for Accurate Temperature Estimation of Mulitlevel ULSI Interconnects", 2004 Symposium on VLSI Circuits Digest of Technical Papers.

27. Chiang, T., et. al., "Analytical Thermal Model for Multilevel VLSI Interconnects Incorporating Via Effect", IEEE Electron Device Letters, Vol. 23, No. 1, Jan 2002.

28. Harmon, D., et. al., "Thermal Conductance of IC Interconnects Embedded in Dielectrics", IRW Final Report, IEEE, 1998.

29. Wakil, J. et. al., "BEOL Thermal Characterization for 3-D Packaging", Proceedings, 2008 IMAPS Conference.

30. Kovalenko, A. D., *Thermoelasticity*, Wolters-Noordhoff Publishing Groningen, The Netherlands, 1969, Chs. 1-2.

31. Gebhart, B. "Heat Conduction and Mass Diffusion", McGraw-Hill, Inc, NY, 1993

32. Lloyd, J. R., "Measurements of Thermal Conductivity and Specific Heat of Lead Free Solder", IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium, 1995.

33. Szekely, V., et. al., "Calculating Effective Board Thermal Parameters From Transient Measurements", IEEE Trans. On Comp. and Pack. Tech. Vol. 24, No4, Dec 2001.

34. Kanuparthi, S., et. al., "Full-Field Simulations of Particulate Thermal Interface Materials: Separating the Effects of Random Distribution from Interfacial Resistance", IEEE publications, IBM Market Insights, 2006

35. Nan, C., et., al., "Inverse Problem For Composites With Imperfect Interface: Determination of Interfacial Thermal Resistance, Thermal Conductivity of Constituents, and Microstructural Parameters", Journal of the American Ceramic Society, Vol 83, Issue 4, 2000

36. Yang, P., and Ningbo Liao, "Physical Mechanism of Interfacial Thermal Resistance in Electron Packaging Based on Mixed MD/FE Model", IEEE Trans. On Advanced Packaging, Vol. 31, No. 3, Aug 2008

37. Wang, H., et. al., "Computation of Interfacial Thermal Resistance by Phonon Diffuse Mismatch Model", Materials Trans. Vol 48, No. 9, 2007

38. Lambropoulos, J. and S Hwang, "Interface Contributions to Localized Heating of Dielectric Thin Films", Journal of Adhesion, Vol 67, 1998

39. Lee, S. and D. Cahill, “Heat Transport in Thin Dielectric Films”, Journal of Applied Physics, Vol. 81, Issue 6, Mar. 1997.

40. Hu, C. et. al., “Thermal Conductivity and Interfacial Resistance of Polymeric Low-K Films”, Applied Physics Letters, Vol 79, #25, Dec. 2001.

41. Alverez-Quintana, J. and J. Rodriguez-Viejo, “Interfacial Effects on the Thermal Conductivity of a-Ge Thin Films Grown on Si Substrates”, Journal of Applied Physics, Vol 104, Issue 7, Jun 2009.

42. Chien, H., et. al., “Measurement and Evaluation of the Interfacial Thermal Resistance Between a Metal and a Dielectric”, Applied Physics Letters, 93, 2008

43. Cahill, D. et. al. “Thermometry and Thermal Transport in Micro/Nanoscale Solid-State Devices and Structures”, Journal of Heat Transfer, Vol. 124. Apr. 2002.

44. Bai, S. “Thermal Characterization of Si3N4 Thin Films Using Transient Thermoreflectance Technique”, IEEE Transactions on Industrial Electronics, Vol. 56, NO. 8, Aug., 2009.

45. Lee, S. and D. Cahill, “Influence of Interface Thermal Conductance on the Apparent Thermal Conductivity of Thin Films”, Microscale Thermophysical Engineering, Vol. 1, Issue 1, Mar. 1997.

46. Prasher, R. “Acoustic Mismatch Model for Thermal Contact Resistance of van der Waals Contacts”, Applied Physics Letters 94, 041905, 2009

47. Picu, R. C., et. al., ‘Strain and Size Effects on Heat Transport in Nanostructures:” Journal of Applied Physics, Vol. 93, No. 6, Mar. 2003

48. Bhowmick, S. and V. B. Shenoy, “Effect of Strain on the Thermal Conductivity of Solids”, The Journal of Chemical Physics, Vol. 125, 2006

49. ARAMIS v6 User Manual, GOM mbH, Germany, 2007

Vita

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