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Energy-Efficient Design Techniques for High Speed Continuous Time Delta Sigma Modulators

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Energy-Efficient Design Techniques for High Speed Continuous Time Delta Sigma Modulators

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Dedicated to my parents.

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Energy-Efficient Design Techniques for High Speed Continuous Time Delta Sigma Modulators

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The University of Texas at Austin, 2020

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Continuous Time Delta Sigma Modulators (CTDSMs) with high sampling rates are becoming increasing popular in wideband communication applications. Conventional CTDSMs use operational transconductance amplifier (OTA)-based active RC integrators to realize the loop filter. In addition to being power-hungry, high DC-gain OTAs are difficult to realize in ultra-deep submicron CMOS processes. This dissertation addresses techniques to realize high sampling rate CTDSMs in advanced CMOS processes, without using OTA-based active RC integrators. Instead, the author investigates techniques to implement the loop filter using more energy-efficient, open-loop building blocks, namely passive integrators and passive summers, Gm-C integrators and voltage controlled oscillator (VCO)-based integrators. The efficacy of the proposed techniques is supported by silicon measurement results of three different CTDSMs which have been fabricated in 40 nm CMOS.

The first part of this dissertation attempts to explore power efficient design techniques for single-bit quantizer based CTDSMs in scaled CMOS processes. A single-bit quantizer is typically implemented as a latched comparator whose outputs regenerate to the supply rails. By deliberately ensuring a small voltage swing at the input of the single-bit quantizer, a large effective gain can be obtained from the quantizer. This helps to significantly relax the DC gain requirements of the loop filter, thereby permitting the use of low DC gain active integrators and even passive integrators within the loop filter. Exploiting this principle, the first segment of this dissertation introduces a 3rd order single-bit quantizer-based CTDSM with a hybrid active-passive loop filter and finite-impulse-response (FIR) DAC. The jitter suppression capability of the FIR DAC is combined with the superior out-of-band quantization noise filtering capability of a passive integrator, thereby enabling the use of an energy efficient Gm-C integrator at the front-end. Most of the DC loop gain is obtained from the single-bit quantizer. The prototype chip has been fabricated in 40 nm CMOS and achieves signal-to-noise-and-distortion-ratio (SNDR), signal-to-noise-ratio (SNR) and dynamic range (DR) of 65.6 dB, 66.7 dB and 67.3 dB respectively in a 5 MHz bandwidth at a sampling rate of 1 GS/s.

The second section of this dissertation switches gear to exploring low power design techniques for multibit quantizer based CTDSMs using a voltage controlled oscillator (VCO) as the quantizer and integrator. The most common implementation of a VCO based quantizer employs a transconductor (Gm) stage driving a current controlled oscillator (CCO). However, when

using such Gm-CCO based quantizers in closed loop CTDSMs at GHz sampling rates, a major challenge is the VCO's voltage-to-frequency (V-F) parasitic pole, which causes excess loop delay (ELD) and degrades loop stability. To address this challenge, the second segment of this dissertation introduces a high speed closed-loop capacitive-input VCO-based CTDSM using a novel fully differential VCO topology which virtually eliminates its V-F parasitic pole. The mitigation of the parasitic pole is achieved by splitting the VCO's input transconductor into a set of distributed input transistors. Capacitive input and capacitive DAC result in a very low thermal noise front end, besides ensuring that there is no additional pole caused due to the VCO's input capacitance. The prototype 1st-order VCO based CTDSM is fabricated in 40 nm CMOS and occupies a core area of 0.02 mm^2 while achieving 63.1 dB DR in 480 kHz to 20.48 MHz bandwidth at 1 GS/s. This is the first work to mitigate the parasitic pole in a fully differential VCO, without relying on any additional active circuits. To the authors' best knowledge, this is also the first work to demonstrate capacitive input in a high speed CTDSM, without using chopping.

The capacitive-input CTDSM presented in the previous section had only 1st order quantization noise shaping and hence its in-band performance was limited by quantization noise. Moreover, it could not digitize signals near DC. To address these limitations, the final section of this dissertation introduces a 2nd order VCO-based CTDSM which uses the distributed-input VCO of the previous section as the second stage (back-end) integrator and

quantizer. Due to the more aggressive noise shaping, this modulator's in-band performance is dominated by thermal noise, resulting in a significantly better measured power efficiency (figure-of-merit). Since the modulator has a resistive input, it can digitize signals from near DC. The combination of a Gm-C integrator and a resistor DAC yields a low-power front-end. The loop filter uses a capacitive-π network to break the constraint between the size of the modulator's inner capacitive DAC and the factor by which the front-end Gm-C integrator is impedance scaled. This, in turn, helps to significantly reduce both analog and digital power. The prototype chip has been fabricated in 40 nm CMOS and achieves SNDR, SNR and DR of 71.8 dB, 72.9 dB and 74.5 dB respectively in a 10 MHz bandwidth at 655 MS/s, yielding an SNDR-based Walden figure-of-merit (FoM) of 45.6 fJ/step.

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Chapter 1

Introduction

Noise-shaping analog-to-digital converters (ADCs) are becoming widely popular in integrated radio receivers. As compared to their discrete time counterparts, noise shaping (oversampled) ADCs that are implemented in continuous time are significantly more power efficient primarily because the internal integrator outputs do not need to accurately settle within a fraction of the sampling clock period. Moreover, continuous time noise shaped ADCs, also commonly referred to as continuous time delta-sigma modulators (CTDSMs), possess intrinsic anti-aliasing capability and are also easier to drive as compared to discrete time (switched-capacitor based) modulators. All these factors make CTDSMs very attractive for wideband communication applications.

Demand for wider conversion bandwidth translates to increased sampling rates, which in turn, increases the unity-gain bandwidth requirement for the integrators within the CTDSM's loop filter. Traditionally, the integrators within a CTDSM's loop filter have been implemented as closed-loop operational-transconductance amplifier (OTA)-based active RC integrators due to their excellent linearity. Since the open-loop unity gain bandwidth of an OTA-based active-RC integrator needs to be several times higher

than its closed-loop unity gain bandwidth, higher ADC sampling rates directly translate to increased OTA power. In addition to poor power efficiency, high DC-gain OTAs are also difficult to implement advanced CMOS processes. The focus of this dissertation is to explore low power design techniques for high-sampling rate CTDSMs by replacing the OTA-based active RC integrators with more energy efficient, open-loop integrators. Two main directions are explored in this dissertation – (1) Single-bit quantizer-based CTDSM design using a combination of passive and active filters (2) Multibit quantizer based CTDSM design using a wideband voltage controlled oscillator (VCO) as the integrator and quantizer. The efficacy of the proposed techniques is demonstrated through silicon measurement results of three different CTDSM designs which have been fabricated in 40 nm CMOS.

A major advantage of single-bit quantizer based CTDSMs is the fact that their feedback DAC is inherently linear, which obviates the need for DAC calibration or dynamic element matching (DEM) circuits. However, compared CTDSMs with multibit quantizers, single-bit quantizer based CTDSMs require higher oversampling ratio (and hence higher sampling rates) for the same conversion bandwidth. Since the power of an OTA-based active RC integrator is directly proportional to the CTDSM's sampling rate, single-bit quantizer based CTDSMs with active RC integrators are typically plagued by high loop filter power consumption. By virtue of their open-loop nature, Gm-C integrators are significantly more power efficient than OTA-based active-RC integrators. However, owing to their relatively poor linearity, Gm-C integrators are

rarely used as the CTDSM's front-end integrator. Moreover, since the front-end integrator mostly processes high-pass shaped quantization noise, the large quantization error of a single-bit quantizer-based CTDSM exacerbates the effect of the Gm-C integrator's non-linearity. Due to the rail-to-rail transitions of the effective feedback DAC waveform, sensitivity to clock jitter is another problem associated with single-bit quantizer based CTDSMs.

To address the challenges associated with single-bit quantizer based CTDSMs, the first part of this dissertation introduces a 3rd order single-bit quantizer based CTDSM with a hybrid active-passive loop filter. This work uses a 2-tap FIR DAC to reduce the effect of clock jitter. A front-end continuous-time passive integrator helps to heavily filter the out-of-band quantization noise, thus significantly relaxing the linearity requirement of the subsequent Gm-C integrator. Unlike a multibit quantizer whose effective gain is approximately 1, the effective gain of a single-bit quantizer is inversely proportional to the voltage swing at the quantizer's input. In our proposed design, the voltage swing at the quantizer's input is designed to be very small and hence, a large effective gain is obtained from the single-bit quantizer. This large quantizer gain helps to compensate for the passive integrator's low DC gain, thus ensuring that the overall in-band loop gain is adequate to meet the desired signal-to-quantization-noise-ratio (SQNR). The prototype CTDSM has been fabricated in 40 nm CMOS and occupies a core area of 0.034 mm^2. The measured peak SNDR, SNR and DR are 65.6 dB, 66.7 dB and 67.3 dB respectively in a 5 MHz bandwidth.

The second half of this dissertation switches gear to multibit quantizer based CTDSMs. Since multibit quantizer based CTDSMs can digitize the same conversion bandwidth with a lower sampling rate, they are becoming increasing popular over their single-bit quantizer-based counterparts in wide-band communication applications. However, the rapidly shrinking core supply voltage in ultra-deep submicron processes makes it difficult to realize high resolution multibit voltage domain quantizers. For CTDSMs with very high sampling rates, a flash quantizer is the most popular voltage domain multibit quantizer since it offers a single-step conversion, unlike a successive approximation register (SAR) quantizer. However, the diminishing supply voltages in ultra-deep submicron processes imposes very stringent constraints on the offset mismatch requirements of the individual comparators within a flash quantizer, in turn mandating comparator offset mismatch calibration which increases circuit complexity. To overcome these problems associated with voltage domain quantizers, there has been increasing interest in *time domain* signal processing. Owing to its scaling friendly nature, a voltage controlled oscillator (VCO) is an ideal candidate for a time domain quantizer. A VCO offers several attractive features, namely, (1) the outputs of all inverters in a ring VCO collectively provide a natural multi-level quantization of the oscillator's phase. The LSB of this phase quantization is not limited by supply voltage (2) A VCO also acts as a voltage to phase integrator with infinite DC gain. This implies that a VCO can be used to replace both the multibit quantizer as well as the active integrator in a CTDSM.

The most common implementation of a VCO based quantizer employs a transconductor (Gm) stage driving a current controlled oscillator (CCO). However, when using such Gm-CCO based quantizers in closed loop CTDSMs at high sampling rates, a major challenge is the VCO's voltage-to-frequency (V-F) parasitic pole, which causes excess loop delay (ELD) and degrades loop stability. To cancel the effect of the VCO's pole, prior works have used additional active circuits in the loop filter, thereby increasing circuit complexity and power consumption. To address this parasitic pole problem without consuming extra power, the second segment of this dissertation introduces a novel fully differential VCO topology which is inherently devoid of a V-F parasitic pole. By splitting the VCO's input transconductor into a set of distributed input transistors, our proposed 'distributed-input' VCO can virtually eliminate its V-F parasitic pole. A detailed explanation for the parasitic pole mitigation mechanism is provided in this dissertation. To ensure that the VCO's gate capacitance does not cause any additional pole in the loop filter, the modulator proposed in this section uses capacitive input and capacitive DAC. Our modulator possesses an intrinsic clock level averaging (CLA) mechanism which naturally up-modulates DAC mismatch errors to even multiples of the VCO's center frequency. This obviates the need for DAC calibration or explicit DEM circuits. To our best knowledge, this is the first published work to demonstrate capacitive input in a high speed CTDSM, without using chopping. The prototype first order VCO-based CTDSM has been fabricated in 40 nm CMOS and occupies a core area of 0.02 mm^2. The fabricated chip achieves 63.1 dB

dynamic range in 480 kHz to 20.48 MHz bandwidth at a sampling rate of 1GS/s.

Despite its merits, our capacitive-input VCO-based CTDSM had certain architectural shortcomings. Firstly, it was capable of only first order quantization noise shaping. The in-band performance was limited by quantization noise, resulting in limited power efficiency (figure-of-merit). Secondly, due to capacitive input, it could not digitize from DC. To leverage the full potential of our distributed-input VCO, the final segment of this dissertation introduces a second order CTDSM that uses the distributed-input VCO as the second stage integrator and quantizer. By virtue of more aggressive noise shaping, this proposed modulator's in-band performance is limited by thermal noise, resulting in a significantly improved measured figure-of-merit. Moreover, since this proposed work uses resistive input, it can digitize signals from near DC. Similar to the first order VCO-based CTDSM proposed in the previous segment, this second order CTDSM also possesses intrinsic CLA and hence does not require any DAC calibration or explicit DEM circuits. Our proposed modulator uses a pair of low power inner capacitor DACs for ELD compensation. When using a front-end Gm-C integrator to directly drive a capacitor DAC, the major challenge is to allow the Gm-C integrator to be impedance scaled up for thermal noise without simultaneously sizing up the inner capacitor DAC. This work demonstrates the use of a capacitive-π network to make the capacitor DAC's feedback coefficient independent of the Gm-C integrator's load capacitance. This allows us to use small-size DAC unit capacitors resulting in

significant savings in both analog and digital power. The prototype ADC has been fabricated in 40 nm CMOS and occupies a core area of 0.064 mm^2. Operating at a sampling rate of 655 MS/s, the measured SNDR, SNR and DR are 71.8 dB, 72.9 dB and 74.5 dB respectively in a 10 MHz bandwidth, resulting in an SNDR-based Walden FOM of 45.6 fJ/step, SNDR-based Shreier FOM of 167.2 dB and DR-based Shreier FOM of 169.9 dB.

The subsequent three chapters will provide relevant analysis, implementation details and measurement results for the three CTDSMs that we discussed. Chapter 5 concludes this dissertation.

Chapter 2

A 1 GS/s Continuous Time $\Delta\Sigma$ ADC with a Passive Front-End Integrator and FIR Feedback DAC in 40 nm CMOS

2.1 Introduction

Sensitivity to clock jitter and stringent linearity requirements for the front-end integrator are major challenges associated with the design of single-bit quantizer based CTDSMs. An FIR DAC [Shettigar and Pavan [2012]; Sukumaran and Pavan [2014]] can address both these issues. Gm-C integrators are inherently more energy efficient than their active RC counterparts, for the same integrator gain-bandwidth product. However, if we were to use (an inherently non-linear) front-end Gm-C integrator in a 1-bit quantizer based CTDSM with an FIR DAC, a very large number of FIR taps would then be required to adequately suppress the transconductor's input voltage swing, thereby incurring larger digital power and increased area.

This work uses a front-end continuous-time passive integrator to heavily suppress the voltage swing at the input of the subsequent Gm-C integrator, thereby significantly relaxing the transconductor's linearity requirements [Das et al. [2005]; Song et al. [2008]; Balachandran et al. [2010]; Srinivasan et al. [2012]; de Melo et al. [2015] Nowacki et al. [2016]]. This allows the

front-end FIR DAC to use only as few taps as necessary to achieve the desired jitter suppression, thus saving digital power and area. By designing the quantizer's input voltage swing to be very small, a large effective gain can be obtained from the 1-bit quantizer, thereby compensating for the passive filter's low DC-gain in a power-efficient and scaling-friendly fashion. Unlike [Balachandran et al. [2010]; Srinivasan et al. [2012]] which employ a current steering (CS) FIR DAC to drive the front-end passive filter, this work uses an FIR resistor DAC (RDAC) which generates lesser noise and can operate under reduced supply voltage. When designing CTDSMs with passive (leaky) integrators, additional constraints arise between SQNR, quantizer's gain, thermal noise and distortion. This chapter includes a thorough analysis of these system-level design constraints and considerations. Interestingly, the use of passive/low DC gain integrators can extend the maximum stable amplitude of a 1-bit quantizer based CTDSM. This chapter also includes an analysis of this phenomenon. Fabricated in 40 nm CMOS, the prototype CTDSM occupies a core area of 0.034 mm^2 and achieves SNDR, SNR, DR of 65.6 dB, 66.7 dB, 67.3 dB respectively in a 5 MHz bandwidth at 1 GS/s.

2.2 Architecture and Circuit Implementation

Fig. 2.1(a) shows the (single-ended equivalent) architecture of the proposed 3rd order CTDSM comprised of a front-end passive integrator, two subsequent Gm-C integrators and a 2-tap FIR feedback DAC for jitter suppression. The voltage swing at the input of the 1-bit quantizer is designed to

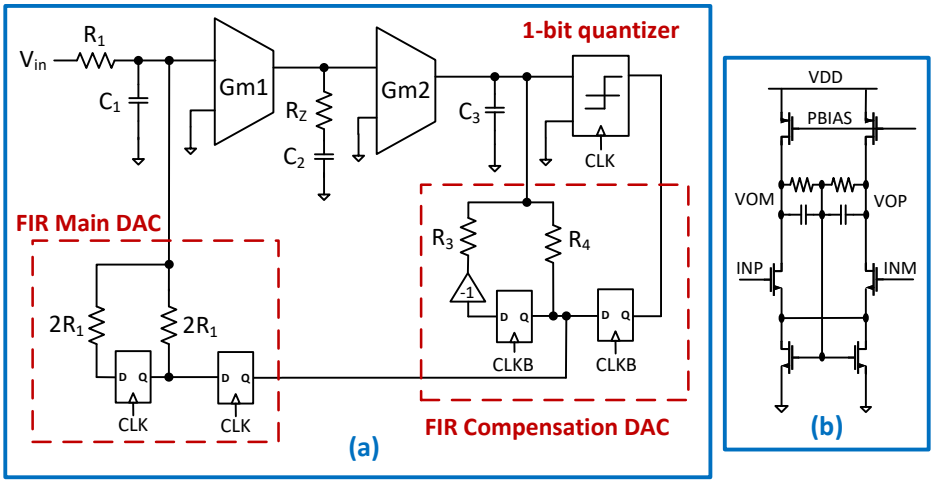

Figure 2.1: (a) Architecture of proposed CTDSM (b) Schematic of Gm1 and Gm2

be very small, thereby resulting in a large effective quantizer gain. Since the front-end passive integrator (R_1, C_1 in Fig. 2.1(a)) heavily filters most of the out-of-band quantization noise, the voltage swing at the input of the subsequent Gm-C integrator is very small. This relaxes the linearity requirement of the Gm-C integrator. The resistor R_Z helps to create a left half plane zero, thus effectively realizing a feedforward path at high frequencies. An inner 2-tap FIR DAC (formed by R_3, R_4 in Fig. 2.1(a)) is used for compensating excess loop delay (ELD). The 1-bit quantizer is implemented by a standard Strong-Arm latch followed by an RS latch. Fig. 2.1(b) illustrates the schematic of both transconductors in the loop filter. Since the voltage swing at the comparator's input is designed to be very small, there is a potential for metastability in the comparator. The inner FIR DAC is retimed with half clock cycle delay. The errors introduced by the outer FIR DAC have a much greater impact on the

system performance compared to the inner DAC's errors. Therefore, the data driving the outer DAC is obtained by sending the inner DAC's input data through another D-Flip Flop which is triggered after an additional half clock cycle (as shown in Fig. 2.1(a)). In presence of quantizer metastability, successive regeneration through a cascade of two Flip-flops significantly reduces the probability of data-dependent delay in the outer FIR DAC.

2.3 Jitter Suppression by FIR DAC

This work uses a 2-tap FIR DAC for jitter suppression. Intuitively, a 2-tap FIR DAC converts the bi-level output of a 1-bit quantizer into a tri-level feedback DAC waveform. This reduces the transition height of the effective DAC waveform, thereby reducing the area of the jitter pulses. Assuming the quantization error to be uncorrelated with the input signal, for a quantizer whose output is ± 1, the in-band jitter-induced noise (J) for a 2-tap FIR DAC can be derived [Reddy and Pavan [2007]] to be

$$J = (\frac{\sigma_{\Delta t}^2}{T^2})(\frac{1}{12\pi OSR}) \int_0^{\pi} |(1 - e^{-j2\omega}) NTF(e^{j\omega})|^2 d\omega \tag{2.1}$$

where ($\sigma_{\Delta t}$/T) represents the fractional clock jitter. Unlike the case of a standard NRZ DAC without FIR feedback, the expression within the integral of Eq. (2.1) contains a notch at $f_s/2$. This is because the outer FIR DAC's transfer function ($= 0.5(1 + z^{-1})$) contains a notch at $f_s/2$. This explains why a 2-tap FIR DAC results in lesser in-band jitter noise compared to an NRZ DAC without FIR feedback. Although a higher number of FIR taps can even further suppress the in-band jitter noise, only two FIR taps are chosen for this

design to minimize complexity and save digital power. Behavioral simulations with a 2-tap FIR DAC and 0.5% fractional clock jitter indicate that the 2-tap FIR DAC provides between 7 dB to 9.5 dB reduction in in-band jitter noise power across input signal amplitude, as compared to a standard bi-level NRZ DAC without FIR feedback.

2.4 Analysis of Design Trade-offs

The linear model of the proposed CTDSM is shown in Fig. 2.2, wherein the transconductors' output resistances are assumed to be infinite for simplicity. However, all our analyses include the finite output resistance of Gm1 and Gm2. In Fig. 2.2, k_1 and k_2 represent scaling factors and are solely used for the purpose of analysis in the subsequent sections.

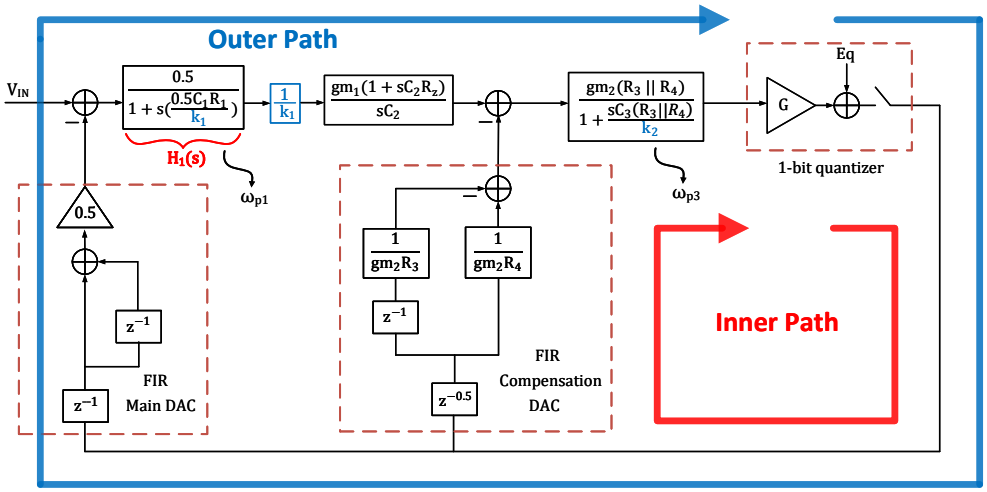

Figure 2.2: Linear model of the proposed CTDSM highlighting the inner and outer paths of the loop gain

2.4.1 Quantizer's Gain

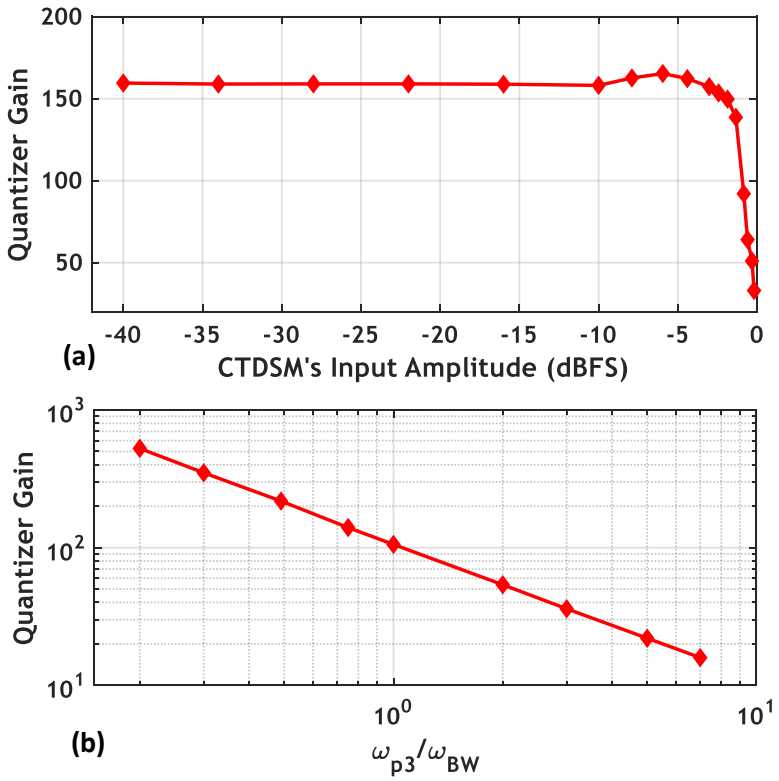

Figure 2.3: Quantizer gain vs (a) CTDSM's input signal amplitude (b) ω_{p3}/ω_{BW}

The gain (G) of a 1-bit quantizer whose output is ± 1 is statistically defined as $G = E[|y|]/E[y^2]$, where y is the input of the 1-bit quantizer. Fig. 2.3(a) plots the quantizer's gain vs the modulator's input signal amplitude. Fig. 2.3(a) indicates that the quantizer's gain is largely independent of the modulator's input signal amplitude except when the modulator's input signal is near the maximum stable amplitude (MSA). This implies that, unless the

modulator's input is very close to the MSA, the overall (peak-to-peak) voltage swing at the quantizer's input (and hence the quantizer's gain) is a weak function of the modulator's input and is mostly determined by quantization noise (which is concentrated at high frequencies). The loop's inner path (labeled in Fig. 2.2) has greater high-frequency gain as compared to the loop's outer path. Hence, it is the high-frequency gain of the loop's *inner path* that determines the voltage swing at the quantizer's input (and consequently sets the quantizer's gain). Fig. 2.3(b) plots the quantizer's gain vs ω_{p3}/ω_{BW} where ω_{p3} is the 3rd integrator's pole (created by C_3 in Fig. 2.1) and ω_{BW} is the signal bandwidth. The analysis of Fig. 2.3(b) assumes constant DC gain for the 3rd integrator while ω_{p3} is scaled by a factor k_2 (labeled in Fig. 2.2). Scaling up ω_{p3} by k_2 (>1) increases the 3rd integrator's high-frequency gain and hence scales up the voltage swing at the quantizer's input by the same factor k_2. This consequently scales the quantizer's gain by $1/k_2$, resulting in an inverse relationship between ω_{p3} and the quantizer's gain (as seen in Fig. 2.3(b)).

2.4.2 SQNR Dependence on Loop Filter's Poles

The SQNR depends on the low frequency (in-band) gain of the loop's outer path (labeled in Fig. 2.2). The front-end passive integrator's pole ω_{p1} and the 3rd integrator's pole ω_{p3} can be considered design variables since their values are determined by passive resistors. Fig. 2.4(a) plots the SQNR vs ω_{p1}/ω_{BW} while maintaining the same DC gain for the front-end passive integrator. For the analysis of Fig. 2.4(a), whenever ω_{p1} is scaled by some

factor k_1 (labeled in Fig. 2.2), the Gm-C integrator following the front-end passive filter is deliberately scaled by $1/k_1$ to preserve the same high frequency loop gain (and hence same out-of-band NTF). When $\omega_{p1}/\omega_{BW} \ll 1$, scaling ω_{p1} by a factor k_1 scales the "average" in-band gain of the front-end passive filter by approximately the same factor k_1. However, since the subsequent Gm-C integrator is being simultaneously scaled by $1/k_1$, the average in-band loop gain stays the same resulting in almost no change in in-band SQNR. On the contrary, when $\omega_{p1}/\omega_{BW}>1$, further increasing ω_{p1} by a factor k_1 (>1), does not change the in-band gain of the passive filter. But since the subsequent Gm-C integrator is being simultaneously scaled by the reciprocal ($=1/k_1$), the average in-band loop gain decreases, resulting in loss of SQNR, as seen in Fig. 2.4(a).

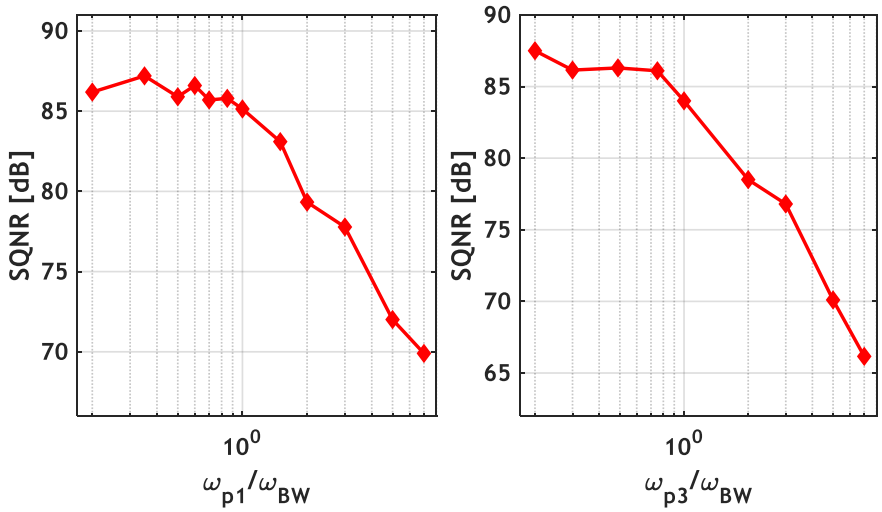

Figure 2.4: SQNR vs (a) ω_{p1}/ω_{BW} (b) ω_{p3}/ω_{BW}

Fig. 2.4(b) plots the SQNR vs ω_{p3}/ω_{BW} while maintaining the same DC gain for the 3rd integrator. Similar to the previous case, when $\omega_{p3}/\omega_{BW}>1$, further increasing ω_{p3} by a factor k_2 (>1), does not change the 3rd integrator's in-band gain. However, since the quantizer's gain G is inversely proportional to ω_{p3}, scaling up ω_{p3} by k_2 implicitly scales G by $1/k_2$ thus resulting in a lower overall in-band loop gain (and consequently a loss of SQNR). Fig. 2.4(a) and 2.4(b) indicate that, for the same target out-of-band NTF, ω_{p1} and ω_{p3} must be within the signal bandwidth to prevent loss of SQNR.

2.4.3 Thermal Noise and Distortion

The ADC's in-band thermal noise is dominated by the input resistors, outer resistor-DAC and the first Gm-C integrator ($Gm1$ in Fig. 2.1). The ADC's in-band input referred thermal noise spectral density is,

$$S_{in} \approx 16kTR_1 + 4S_{Gm1}|1 + s\frac{R_1C_1}{2}|^2 \tag{2.2}$$

where R_1, C_1 correspond to the front-end passive filter and S_{Gm1} is the input referred noise of $Gm1$. As is evident from Eq. (2.2), lowering ω_{p1}/ω_{BW} tends to amplify the noise of $Gm1$ when referred to the ADC's input.

During system-level design, the voltage swing at the quantizer's input should be nominally designed to be several times higher than the quantizer's input referred thermal noise, in order to ensure that the quantizer's gain is not a function of its own thermal noise. This requirement sets the upper limit on the maximum achievable quantizer gain.

To evaluate the effect of the first transconductor's distortion, Gm1's output current is modeled as $i_o = g_1 v_i - g_3 v_i^3$, where $g_1 = 0.7\ mA/V$ and $g_3 = 12.6\ mA/V^3$. This amount of distortion is typical for differential pairs biased in weak sub-threshold. Although our design's Gm1 is biased in strong inversion (and is hence more linear), the following analysis assumes such a relatively large non-linearity just to consider the worst-case distortion scenario. Fig. 2.5(a) plots the third harmonic distortion (HD3) vs ω_{p1}/ω_{BW}. For the analysis of Fig. 2.5(a), whenever ω_{p1} is scaled by a factor k_1 (labeled in Fig. 2.2), the subsequent Gm-C integrator is deliberately scaled by $1/k_1$ to preserve the same high frequency loop gain. Lowering ω_{p1} reduces the voltage swing at the input of $Gm1$, thereby resulting in lesser distortion, as confirmed by Fig. 2.5(a).

Considering all the above-mentioned tradeoffs, the optimal design choice for ω_{p1}/ω_{BW} is around 1. Since ω_{p3}/ω_{BW} has weaker effect on the ADC's performance, it is sufficient to only ensure $\omega_{p3}/\omega_{BW} < 1$ (to prevent loss of SQNR) but it should not be made too small either (to prevent excessively amplifying the quantizer's input referred thermal noise).

2.4.4 Stability for Input Near Full Scale

An interesting consequence of using low DC gain integrators (or even passive integrators) is an increase of the MSA, thus extending the ADC's dynamic range. This fact is also supported by measurement results of the prototype chip. To qualitatively understand this phenomenon through a linear

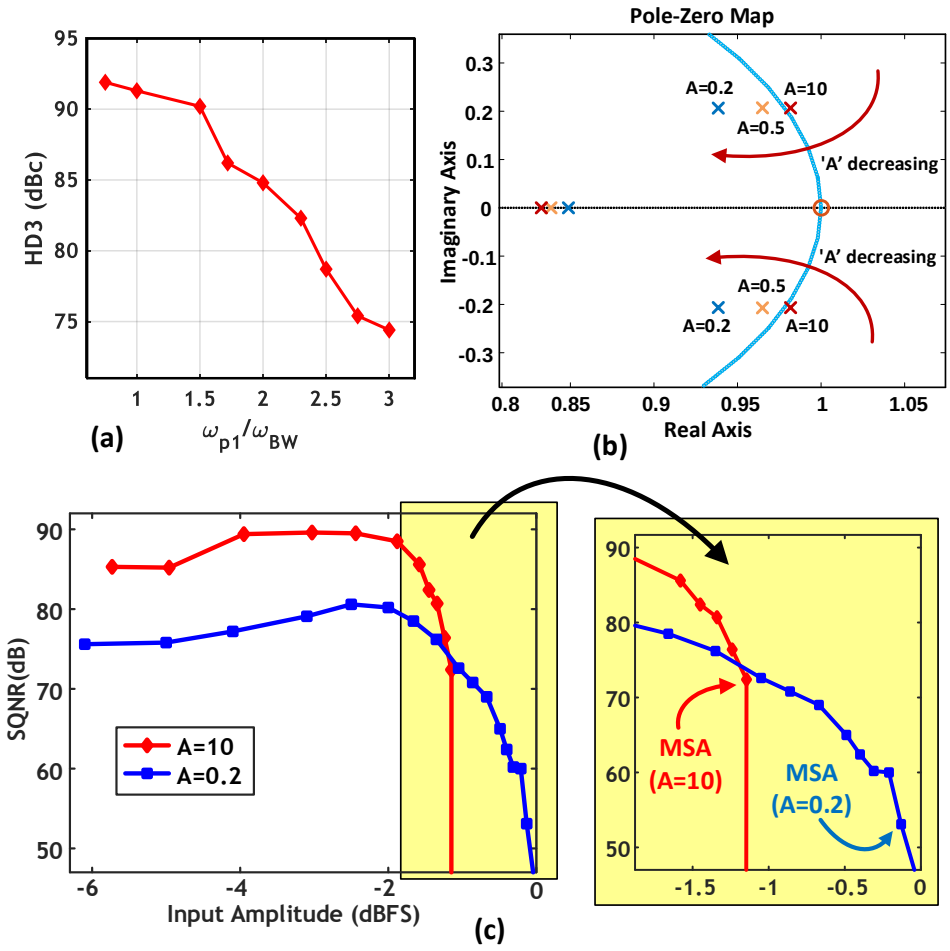

Figure 2.5: (a) HD3 vs ω_{p1}/ω_{BW} in presence of Gm_1 non-linearity (b) Loci of NTF's poles for different values of A, with $G = 30$ (c) SQNR vs modulator's input signal amplitude for $A = 10$ and $A = 0.2$

model, the transfer function of the front-end integrator, marked as $H_1(s)$ in Fig. 2.2, can be re-written as

$$H_1(s) = \frac{A}{1 + \frac{sA}{UGB}} \tag{2.3}$$

where A is the DC gain and UGB is the unity-gain-bandwidth of $H_1(s)$. For $\omega_{p3}/\omega_{BW} = 0.65$, the quantizer's gain G is nominally 160 when the modulator's input signal amplitude is small. However, as shown in Fig. 2.3(a), G is greatly reduced with a larger input signal at the modulator's input. Hence, for this analysis, the value of G in the modulator's linear model has been set 30 to mimic a scenario wherein a large signal at the modulator's input (near MSA) has significantly decreased the quantizer's gain. Under such a scenario, we now proceed to show that a low DC gain integrator can still ensure stability.

While maintaining the same UGB, the DC gain A is lowered from 10 to 0.2. The pole-zero plot of Fig. 2.5(b) shows the loci of the NTF's complex conjugate poles as a function of A, with G fixed at 30. Fig. 2.5(b) demonstrates that the poles are outside the unit circle for larger values of A. However, as A is decreased considerably below 1, the poles move back inside the unit circle. This first-order analysis therefore confirms that a low DC gain integrator can improve stability even when G is greatly reduced (due to the presence of a large signal at the modulator's input). Fig 2.5(c) plots the SQNR vs the modulator's input signal amplitude for $A = 10$ and $A = 0.2$, wherein it is evident that a lower A can extend the MSA.

2.5 Measurement Results

The proof-of-concept ADC has been fabricated in 40 nm CMOS and has a core area of 0.034 mm^2. Fig. 2.6 shows the die photo of the fabricated chip. The measured SNDR, SNR and DR are 65.6 dB, 66.7 dB and 67.3 dB

respectively in a 5 MHz bandwidth at f_s =1.024 GHz. The total measured power consumption is 787 μW of which is 653 μW is from analog and 134 μW is from the digital circuits. The ADC's full scale voltage, analog and digital supplies are all 1.2 V.

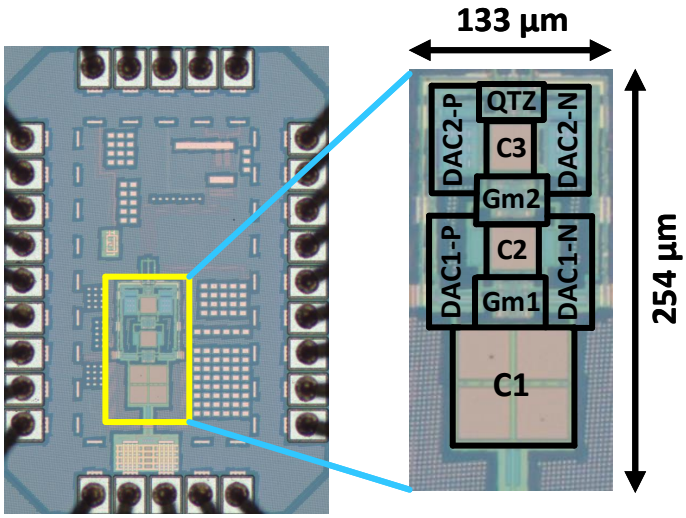

Figure 2.6: Die photo of the fabricated chip

Fig. 2.7 depicts the measured spectrum for a -3 dBFS, 500 kHz input wherein the measured SFDR is -82.6 dBc. Fig. 2.8 shows the measured SNDR/SNR vs input signal amplitude (for a 500 kHz input). The measured MSA is -0.5 dBFS, thus confirming our claim of stability with nearly full-scale input. This prototype chip is designed mainly for proof-of-concept. Its performance can be further improved with more schematic and layout optimizations. Table 2.1 compares the performance of the fabricated chip with state-of-the-art CTDSMs. Since the DC loop gain is mostly obtained from the quantizer, our proposed architecture is inherently scaling-friendly and low-power.

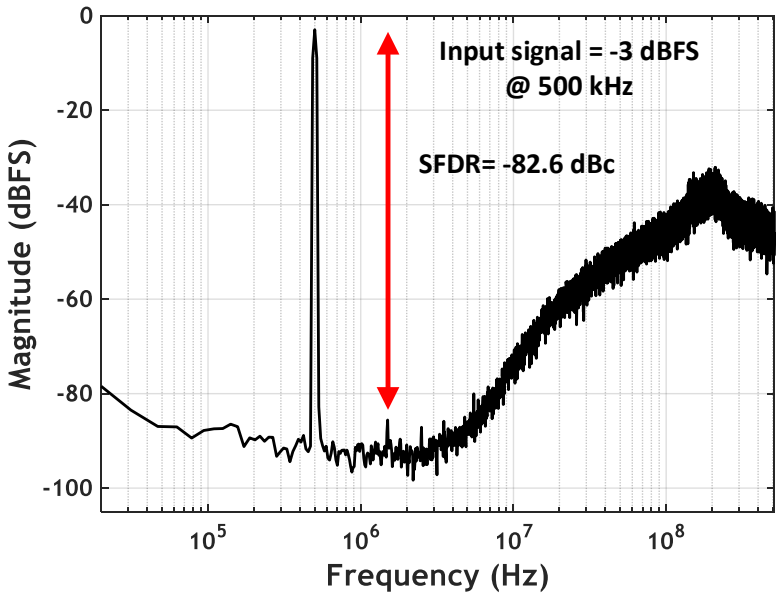

Figure 2.7: Measured 65,536 point spectrum with a 500 kHz, -3 dBFS input

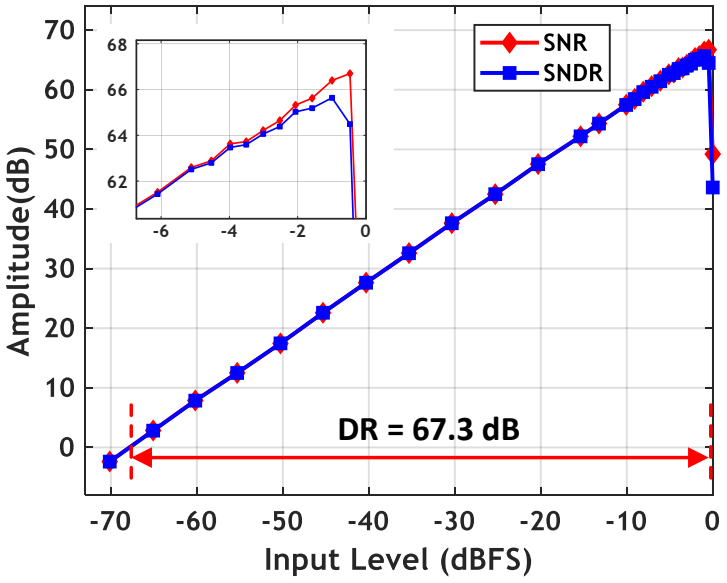

Figure 2.8: Measured SNDR/SNR vs input amplitude

Table 2.1: Performance comparison for proposed 1-bit 3rd order CTDSM

	VLSI 2015 Kao	VLSI 2017 Jang	CICC 2018 Maniv-annan	VLSI 2014 Weng	JSSC 2017 Babaie-Fishani	**This Work**
Order	4th	4th	4th	3rd	3rd	**3rd**
Process [nm]	16	28	65	90	65	**40**
Area [mm^2]	0.115	0.1	0.62	0.12	0.01	**0.034**
Fs [MHz]	832	320	128	300	1600	**1024**
BW [MHz]	19	10	1	8.5	10	**5**
SNDR [dB]	71.6	74.4	75.7	67.2	65.7	**65.6**
DR [dB]	78.5	80.8	–	69.3	71	**67.3**
SFDR [dBc]	75	94.2	84.5	72	75.5	**82.6**
Supply [V]	–	1.1/1.2	1.2/2.5	1.2/1.4	1/1.2	**1.2**
Power [mW]	6.2	4.2	2.2	4.3	3.7	**0.79**
FOMw*[fJ]	52.5	49.3	220.8	135	117	**51**

*$FoMw = Power/(2*BW*2^{ENOB})$, $ENOB = (SNDR-1.76)/6.02$

Chapter 3

A 1 GS/s 20 MHz-BW Capacitive-Input Continuous Time $\Delta\Sigma$ ADC Using a Novel Parasitic Pole-Free Fully Differential VCO in 40 nm CMOS

3.1 Introduction

In this chapter[1], we switch gear to exploring multibit quantizer based delta-sigma ADCs using *time domain* signal processing.The benefits of technology scaling have fuelled significant interest in realizing time domain quantizers. Owing to its scaling friendly nature, a voltage controlled oscillator (VCO) is an ideal candidate for a time domain quantizer. At any instant, output voltage of all inverters in a ring VCO collectively provide a quantized snapshot of the oscillator's revolving phase. The least-significant-bit (LSB) of this phase quantization depends only on the number of inverters in the ring VCO and is hence independent of the supply voltage. Thus, an equivalent

[1]This chapter is a partial reprint of the publication: Abhishek Mukherjee, Miguel Gandara, Biying Xu, Shaolan Li, Linxiao Shen, Xiyuan Tang, David Pan, and Nan Sun, "A 1-GS/s 20 MHz-BW capacitive-input continuous-time $\Delta\Sigma$ ADC using a novel parasitic pole-mitigated fully differential VCO," in *IEEE Solid-State Circuits Letters*, Vol. 2, No. 1, Jan. 2019. I am the main contributor in charge of circuit design, layout, and chip validation.

phase quantizer can be realized simply by sampling the output voltage of all the inverters in a ring VCO. However, since the VCO's phase is an integral of its control voltage, to quantize the VCO's control *voltage*, it necessary to differentiate the quantized phase output of the VCO. As demonstrated by Straayer and Perrott [2008], this differentiation can be performed in digital domain using XOR gates, thereby resulting in a quantization noise transfer function (NTF) which has a perfect null at DC.

However, when used as a quantizer, the VCO processes nearly full-scale input voltage. This can potentially cause significant harmonic distortion since the VCO's voltage-to-frequency (V-F) tuning curve is severely non-linear. To mitigate the effects of the VCO's V-F non-linearity, [Taylor and Galton [2010]; Taylor and Galton [2013]; Rao et al. [2014]] used digital background calibration. However, in addition to increasing circuit complexity and digital power, these background calibration schemes also possess the disadvantage of requiring a well-matched replica VCO, which may be difficult to guarantee in practice. To avoid the need for non-linearity calibration, Straayer and Perrott [2008] embedded the VCO quantizer within a $\Delta\Sigma$ modulator loop, thus relying on the front-end active RC integrator to suppress the non-linearity of the VCO quantizer. However, due to limited gain of the front-end integrator near the upper edge of the signal band, the ADC's overall performance was still limited by the VCO's non-linearity. Alternatively, [Reddy et al. [2012]; Xing and Gielen [2015]] mitigated the VCO's non-linearity by using the VCO as a fine quantizer in a two-step/sub-ranging architecture. However, these

architectures are sensitive to DAC mismatch, gain errors and delay mismatch between the different paths. Realizing that a VCO provides lossless integration from frequency to phase, Park and Perrott [2009] proposed using the VCO both as a voltage-to-phase *integrator* as well as a phase *quantizer* within a closed loop. When using a VCO as a voltage-to-phase integrator in closed loop, the input signal component at the VCO's input is inherently first-order high pass shaped, thereby significantly reducing the VCO's harmonic distortion. This type of linearization does not incur the extra circuit complexity of previous schemes and is hence used in the CTDSM proposed in this chapter.

As reported in most publications on VCO-based ADCs, the most common VCO implementation involves a transconductor (Gm) driving a current controlled oscillator (CCO). However, a major drawback of such Gm-CCO structures is the current-to-frequency parasitic pole that is inherently formed at the CCO's lumped control node. When such Gm-CCO based quantizers are used within a closed loop CTDSM, the excess loop delay (ELD) caused by the CCO's parasitic pole can degrade loop stability. Moreover, the frequency of this parasitic pole decreases with increase in the number of inverters in the ring CCO, thus making it difficult to simultaneously achieve high quantizer resolution and high ADC sampling rate in a closed loop implementation. To compensate for this parasitic pole, Reddy et al. [2012] used a source follower driving a feedforward capacitor to introduce a left-half plane (LHP) zero. Similarly, Huang et al. [2017] created additional LHP zeros in the VCO driver and loop filter to cancel the phase lag of the VCO's parasitic pole. Instead of trying

to create LHP zeros in the loop filter, Reddy et al. [2015] used an opamp-based active adder to directly drive the oscillator's lumped control node, thus absorbing the VCO's parasitic pole into the opamp's output parasitic pole. All these prior works used active circuits to mitigate the VCO's parasitic pole and hence increased power dissipation. Adopting an alternative approach, instead of trying to cancel the effect of the CCO's parasitic pole, Li and Sun [2017] exploited the CCO's parasitic pole to realize a passive integrator, thus achieving an extra order of quantization noise shaping. However, the creation of a passive integrator in the loop filter introduces additional constraints, thereby potentially complicating the design and optimization of the loop filter.

All these prior works that we discussed so far have used conventional VCO/CCO topologies and have chosen to deal with the VCO's parasitic pole through architectural (system-level) modifications, thus unfortunately incurring extra architectural complexity. Recognizing the need for transistor-level innovation within the VCO itself, this chapter introduces a novel fully differential distributed-input VCO topology that inherently eliminates the VCO's voltage-to-frequency (V-F) parasitic pole. Thus, the effect of the VCO's parasitic pole is mitigated without any extra power consumption. To prevent the VCO's gate capacitance from causing any additional pole in the loop, our proposed modulator uses capacitive input and capacitive DAC. This in turn results in an inherently low thermal noise front-end. To the author's best knowledge, this is the first published work to demonstrate capacitive input in a high speed CTDSM, without using chopping. Our prototype 1st order

63-stage VCO based CTDSM occupies a core area of only 0.02 mm^2 while achieving 63.1 dB dynamic range in 480 kHz to 20.48 MHz bandwidth at a sampling rate of 1 GS/s in 40 nm CMOS.

3.2 Distributed-Input VCO

Fig. 3.1 introduces the 63-stage differential VCO used in this work and contrasts its functionality with the conventional Gm-CCO topology [Tu et al. [2017b]; Tu et al. [2017a]]. Fig. 3.1(a) depicts the commonly used Gm-CCO topology, whereas Fig. 3.1(b) depicts the proposed VCO topology with distributed input transistors. Being a hybrid of the Gm-CCO topology and the current starved inverter-based VCO [Park and Perrott [2009]], the proposed VCO topology combines the merits of both. In the Gm-CCO topology (Fig. 3.1(a)), a step change in the VCO's input voltage first changes the voltage at the lumped control node of the CCO (V_{MID1} in Fig. 3.1(a)), which *subsequently* permits the CCO's frequency to settle to the correct value. This mechanism, which can be coarsely approximated as a two-step process, provides time-domain intuition of the parasitic pole that is inherent in the conventional Gm-CCO topology. In contrast, the proposed topology of Fig. 3.1(b) avoids this two-step process by splitting the input transconductor into a set of distributed transistors. Due to the absence of an intermediate lumped control node, the proposed VCO's input voltage can *instantaneously* change its frequency, thereby eliminating the parasitic pole in voltage-to-frequency conversion. The transistor-level simulation in Fig. 3.1(c) compares the spec-

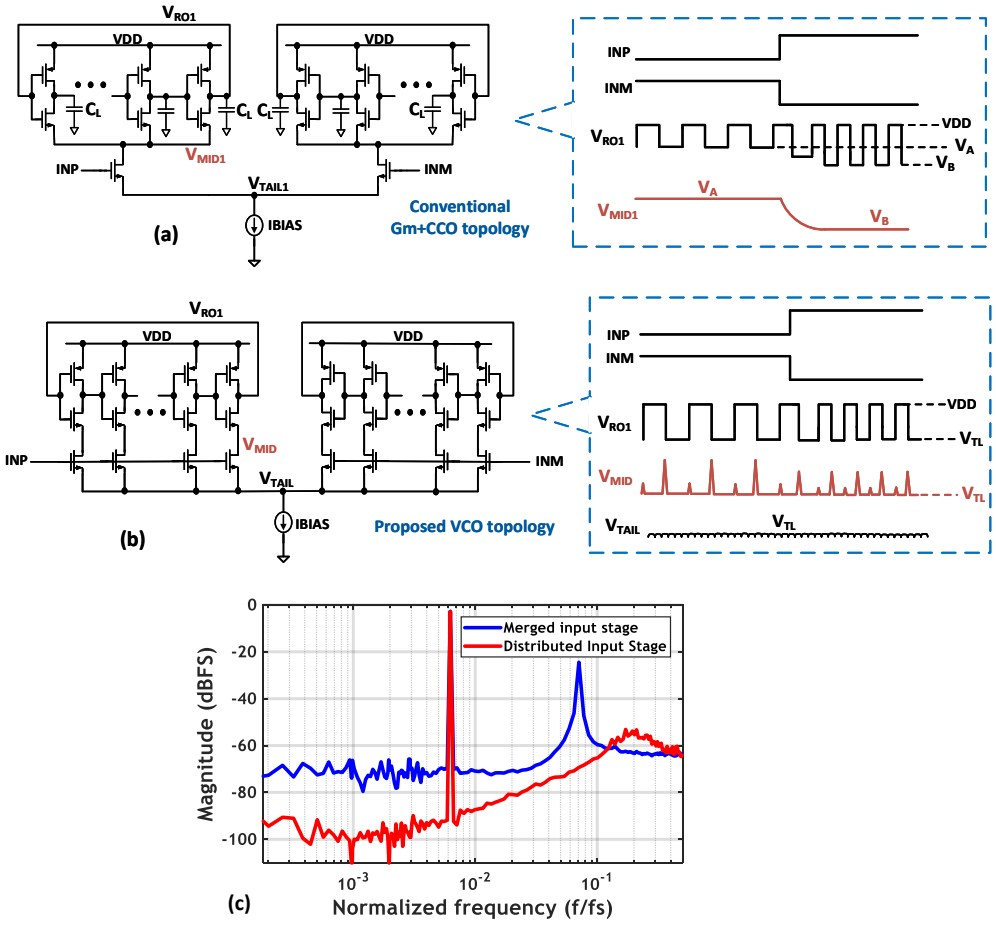

Figure 3.1: (a) Conventional Gm+CCO with a single input transconductor; (b) Proposed VCO with distributed input transconductors; (c) Transistor-level simulation comparing a 1st order VCO-based CTDSM's spectrum when designed with the conventional Gm+CCO (blue curve) and the proposed distributed-input VCO (red curve) respectively, with $ELD = 0.5$ clock cycle

trum between two 1st-order VCO-based CTDSMs designed using the Gm-CCO topology and the proposed distributed-input VCO topology. As is evident from Fig. 3.1(c), the absence of peaking in noise transfer function (NTF)

confirms the absence of a parasitic pole in the proposed VCO topology. Half clock cycle uncompensated ELD and 63 VCO stages are used for both cases that are compared in Fig. 3.1(c). Unlike the current starved inverter based VCO, the proposed topology possesses fully differential operation. Thus, for the proposed topology, the center frequency as well as the frequency difference between the two oscillators are less sensitive to input common mode variations.

3.3 Mechanism of Parasitic Pole Mitigation

In this section, we provide a detailed time domain explanation as to why our proposed distributed-input VCO of Fig. 3.1(b) is capable of virtually eliminating its parasitic pole. In the distributed-input VCO of Fig. 3.1(b), since the VCO's input transistors do not have a steady operating point, performing a static small signal modeling would be tedious and unsuitable. We therefore proceed to analyze the problem in time domain. We will attempt to use a simple (yet completely rigorous) 'thought experiment' to prove that the distributed-input VCO topology is significantly more wideband than the conventional Gm-CCO topology [Tu et al. [2017a]; Tu et al. [2017b]] with a lumped control node.

Fig. 3.2 shows the single-ended unit slice of the distributed-input VCO (left) and the associated timing diagram of our proposed thought experiment (right). In Fig. 3.2, C_L and C_{MID} represent parasitic capacitances at the respective nodes. Before delving into our thought experiment, it is crucial to first understand the time-domain behavior of the internal nodes of the

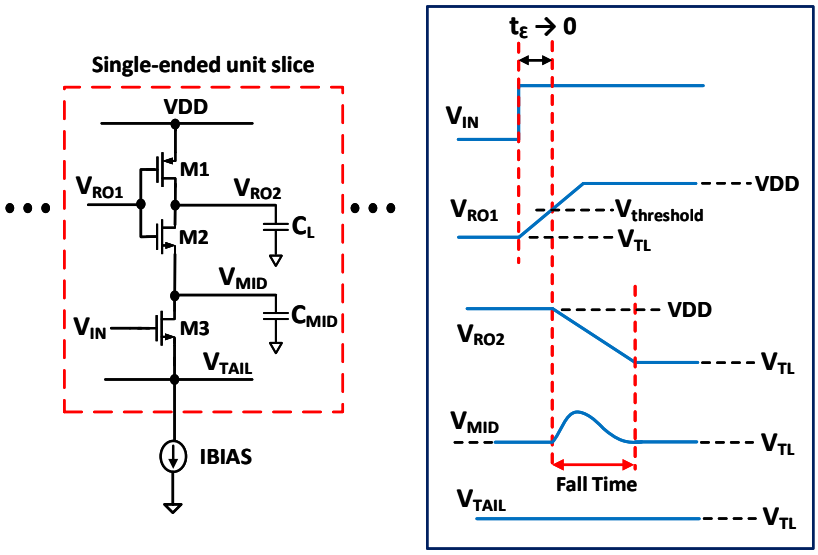

Figure 3.2: Single ended unit slice of the distributed-input VCO (left) and timing diagram for our proposed thought experiment (right)

distributed-input VCO, as illustrated by the waveforms on the right side of Fig. 3.2. Since the VCO is driven in a fully differential manner, the drain of the tail current source (V_{TAIL} in Fig. 3.2) always stays at a constant value (labeled as V_{TL} in Fig. 3.2), very similar to the tail node of a fully differential amplifier. The output of each VCO delay stage (labeled as V_{RO2} in Fig. 3.2) oscillates between VDD and V_{TL}. When any individual delay stage is not transitioning, the corresponding internal node (labeled V_{MID} in Fig. 3.2) remains at the tail voltage, V_{TL} and thus the drain-source voltage (V_{DS}) of the corresponding input transistor M3 will be zero when there is no transition. When the inverter input, V_{RO1} is falling, it turns off M2 and turns on PMOS, M1, which then charges up the inverter output (V_{RO2}) to VDD. During the charging up (rising transition) of V_{RO2}, since M2 is mostly turned off, therefore, to the first order,

the rising transition delay (or rise time) is independent of the VCO's input signal (V_{IN} in Fig. 3.2). It is only the falling delay which is a function of V_{IN}. Therefore, in our subsequent analysis we shall only focus on the falling delay. The falling transition of V_{RO2} is initiated when V_{RO1} rises beyond a certain threshold value (labeled as $V_{threshold}$) in Fig. 3.2. The PMOS M1 starts turning off, NMOS M2 starts turning on. The internal node V_{MID} charges up a little from its initial value of V_{TL} until the drain-source voltage (V_{DS}) of the input transistor, M3 is sufficiently large for M3 to be able to sink the discharging current. Subsequently, M3 simultaneously discharges both C_L and C_{MID}, and by the end of the falling transition, V_{RO2} and V_{MID} nodes are both discharged to the tail voltage V_{TL}. As highlighted in Fig. 3.2, it is crucial to note that the internal node V_{MID} starts with a value of V_{TL} at the beginning of *each* falling transition of V_{RO2} and returns to the same value, V_{TL} at the end of the falling transition.

We now introduce the setup for our thought experiment. In our proposed thought experiment, we let the VCO run stand-alone (in an open loop fashion) and apply a small differential input step at the VCO's inputs (INP and INM in Fig. 3.1(b)). In principle, the VCO's inputs could change at any arbitrary time. But, as shown in Fig. 3.2, in this thought experiment we will assume that the input step is applied just before V_{RO1} crosses $V_{threshold}$, i.e., we apply the input step just before V_{RO2} is about to start discharging. In Fig. 3.2, this is illustrated as $t_\varepsilon \to 0$. Let the fall time associated with this particular falling transition be denoted as T_{d0}. We will subsequently use the phrase 'first

falling transition' to refer to this falling transition that takes place just after the input step is applied. Now consider any other falling transition at a much later time (i.e., at $t \rightarrow \infty$) when the VCO has presumably reached steady state. We shall refer to the fall time corresponding to this falling transition (i.e., at $t \rightarrow \infty$) as the steady state falling delay and denote it as $T_{d,ss}$.

At this point, we state that the dynamics of the falling transition (including the falling delay) for any arbitrary VCO delay stage, is solely dependent on the *initial value* (value at the beginning of the transition) of the corresponding node voltages (namely nodes V_{RO1}, V_{RO2}, V_{IN}, V_{MID} and V_{TAIL}) in Fig 3.2. Furthermore, we make the crucial observation that the nodes V_{RO1}, V_{RO2}, V_{IN}, V_{MID} and V_{TAIL} have exactly the same voltages at the beginning of the falling transition at $t \rightarrow \infty$ as well as at the beginning of the falling transition which occurred just after the input step was applied (first falling transition). In other words, the dynamics of the falling transition at $t \rightarrow \infty$ are *indistinguishable* from that of the first falling transition (and consequently, $T_{d,ss} = T_{d0}$), simply because the corresponding node voltages have the same values at the beginning of the respective transitions. But, according to the setup of our thought experiment, the first falling transition was defined to be the falling transition that occurred $just\ after$ the input step was applied to the VCO's input terminals. Therefore, our thought experiment enables us to conclude that a differential step input to the VCO is potentially capable of *almost instantaneously* changing the falling transition delay to its steady state value. This time domain analysis confirms that VCO's V-F parasitic

pole has been virtually moved to very high (almost infinite) frequency. This analysis is independent of the number of inverter stages in the ring VCO.

In summary, by splitting the input transconductor of the conventional Gm-CCO topology into a set of distributed transconductors, the distributed-input VCO topology manages to isolate the internal nodes of the different stages. This isolation *prevents memory effects* from propagating between successive falling transitions, thereby ensuring that all falling transitions have the same initial conditions (i.e., same values of involved node voltages at the beginning of the respective transitions) in our proposed thought experiment. This is the time domain explanation of why the distributed-input VCO can virtually eliminate its V-F parasitic pole, regardless of the number of inverter stages in the ring VCO.

For the sake of completeness, we will next analyze the parasitic-pole for the conventional Gm-CCO topology of Fig. 3.1(a). For this VCO topology, since the input transistor is always in saturation, small signal modeling is relatively more straightforward and has already been explained in [Reddy et al. [2012]]. Based on the analysis in [Reddy et al. [2012]], Fig. 3.3 shows the well-known small signal model for the conventional Gm-CCO topology (left) and the exponential settling behavior of the lumped control node (right). In Fig. 3.3, R_{eq} represents the input resistance of the CCO and C_{eq} denotes the effective capacitance at the lumped control node, V_{MID1}. Let C_L denote the parasitic capacitance at the output of each inverter in the ring CCO. Each inverter's output oscillates between VDD and V_{MID1}. Thus, every inverter

whose output is in 'logic low' state has its output parasitic capacitance (C_L) directly connected to the lumped node (V_{MID1}) through the on-switch resistance of the corresponding NMOS transistor. Thus, for an N-stage ring CCO, $C_{eq} \approx (N/2)C_L$ in Fig. 3.3. Consequently, it is evident that greater number of inverters in the ring CCO will add more capacitance at the lumped node, thus lowering the parasitic pole ($1/R_{eq}C_{eq}$) even further. In fact, it has been reported in [Reddy [2014]] that this parasitic pole happens to be quite close to the oscillator's center frequency.

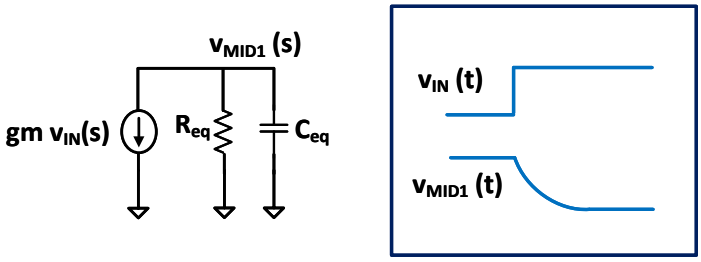

Figure 3.3: Small signal model of the conventional Gm-CCO (left) and exponential settling behavior of the lumped control node (V_{MID1})

We now analyze the conventional Gm-CCO using same time domain approach that we had used for the distributed-input VCO. Let us consider a scenario wherein the conventional Gm-CCO topology has a very large number of inverters in the ring CCO. In response to a differential step applied at the VCO's inputs, the lumped node V_{MID1} will take a relatively long time to settle. During the time that V_{MID1} is in the process of settling, there could be several falling transitions of the CCO. For each of these falling transitions, the transition delay (falling time) will be different because one of the state

variables involved in the transition, namely V_{MID1}, would have a different value at the beginning of each of those falling transitions. It is only $after$ V_{MID1} has completely settled, will all the fall transitions have identical delay (the steady state transition delay). This is the time domain interpretation of the V-F parasitic pole inherent in the conventional Gm-CCO.

3.4 Architecture of Proposed ADC

Fig. 3.4 shows the architecture of our proposed capacitive-input 1st-order CTDSM which uses the distributed-input VCO as an integrator and quantizer. XOR gates are used to measure the phase difference between two 63-stage ring VCOs which are driven in a fully differential fashion. This type of phase detection scheme benefits from intrinsic clock level averaging (CLA) which up-modulates (PWM modulates) DAC mismatch errors to even multiples of the VCO's center frequency, thus eliminating the need for explicit DEM circuitry, as explained in [Lee et al. [2015]; Li et al. [2017]]. Since the modulator is only 1st order, it is comfortably stable despite the uncompensated 50% clock cycle ELD used for data retiming. Since capacitors are noiseless, the system has inherently low thermal noise.

To set the bias voltage at the VCO's inputs ($V_{XP/M}$ in Fig. 3.4), if we were to directly connect nodes $V_{XP/M}$ to a DC voltage using large resistors, then the loop would saturate due to the absence of DC negative feedback. Till date, capacitive input CTDSMs have been demonstrated only in low speed applications such as sensor interfaces [as in Tu et al. [2017b]] wherein chop-

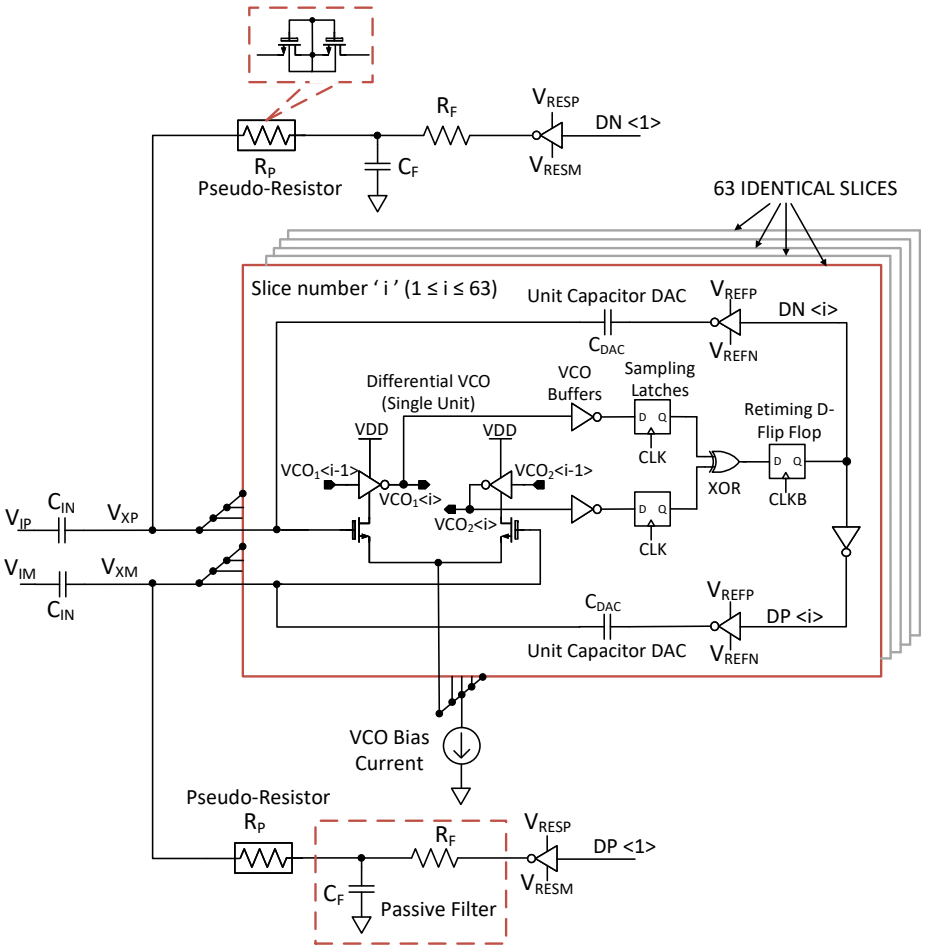

Figure 3.4: Architecture of proposed CTDSM with 63-stage differential ring VCO

ping has been used to provide DC negative feedback in addition to flicker noise suppression. However, chopping is not an efficient solution for providing DC negative feedback in high-speed capacitive-input CTDSMs due to extra power in driving the chopping switches, additional ISI, and quantization noise folding that chopping introduces. This work demonstrates the use of a pseudo-resistor between the VCO's input and the ADC output to provide DC negative

feedback in the modulator. In order to feedback the ADC output (D_{OUT} in Fig. 3.5(a)) to the VCO input, it may appear that we need to use 63 pairs of pseudo-resistors to connect each retimed XOR output pair (DN/P <i> in Fig. 3.4) and the VCO's input ($V_{XP/M}$ in Fig. 3.4). However, using 63 pairs of pseudo-resistors would lead to increased area overhead. Interestingly, owing to the dual VCO's quantization property [Lee et al. [2015]], *each* DN/P <i> contains a linear PWM modulated version of D_{OUT}. Taking advantage of this property, this work uses only a *single* pair of pseudo-resistors for DC negative feedback (as shown in Fig. 3.4), which, in turn helps to save area. Unlike the spectrum of any *individual* comparator's output in a traditional flash quantizer, the spectrum of *each* DN/P <i> in the proposed scheme does not contain any signal harmonics within the modulator's bandwidth and consequently, the modulator's THD is not degraded when using a *single* pair of pseudo-resistors.

The DAC reference voltages, $V_{REFP/N}$ are 1.2 V/0 V. DN <1>and DP <1>are the retimed outputs of the first XOR gate and its complement. The inverter driving the DC negative feedback path is operated between two separate reference voltages, labeled as $V_{RESP/M}$ in Fig. 3.4. The common mode voltage at the VCO's inputs ($V_{XP/M}$) is the average of V_{RESP} and V_{RESM}. $V_{RESP/M}$ are nominally set as 1.2 V/0.3 V. If pseudo-resistors R_P were to be directly connected to inverters' outputs, they would not be able to correctly set the common mode voltage at $V_{XP/M}$ because pseudo-resistors are highly nonlinear in presence of large voltage swings. Therefore, a passive filter formed

by R_F and C_F is placed before the pseudo-resistors to suppress the signal swing at the driven end of the pseudo-resistor. The pole formed by R_F and C_F is around 85 kHz. The modulator's conversion bandwidth is chosen to begin from 480 kHz to ensure that the input signal component in DN <1>and DP <1>is sufficiently suppressed by the passive filter. Although the signal transfer function (STF) has a null at DC, the STF magnitude increases to 1 at frequencies beyond $1/(2\pi R_P C_{IN})$, which is well below the 480 kHz lower cutoff frequency of the input signal bandwidth. The STF also has nulls at the sampling rate (f_S) and its multiples, thus retaining anti-aliasing property.

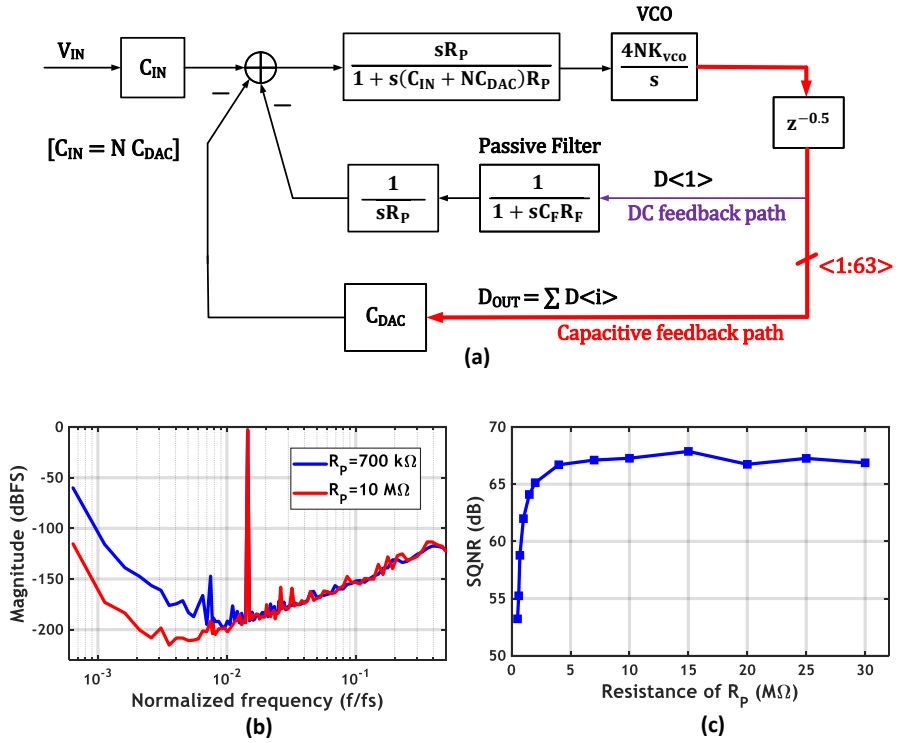

Figure 3.5: (a) Linear model of proposed CTDSM; (b) Behavioral simulation comparing spectrum with pseudo-resistor value, R_P=700 kΩ and R_P=10 MΩ; (c) Variation of SQNR with R_P

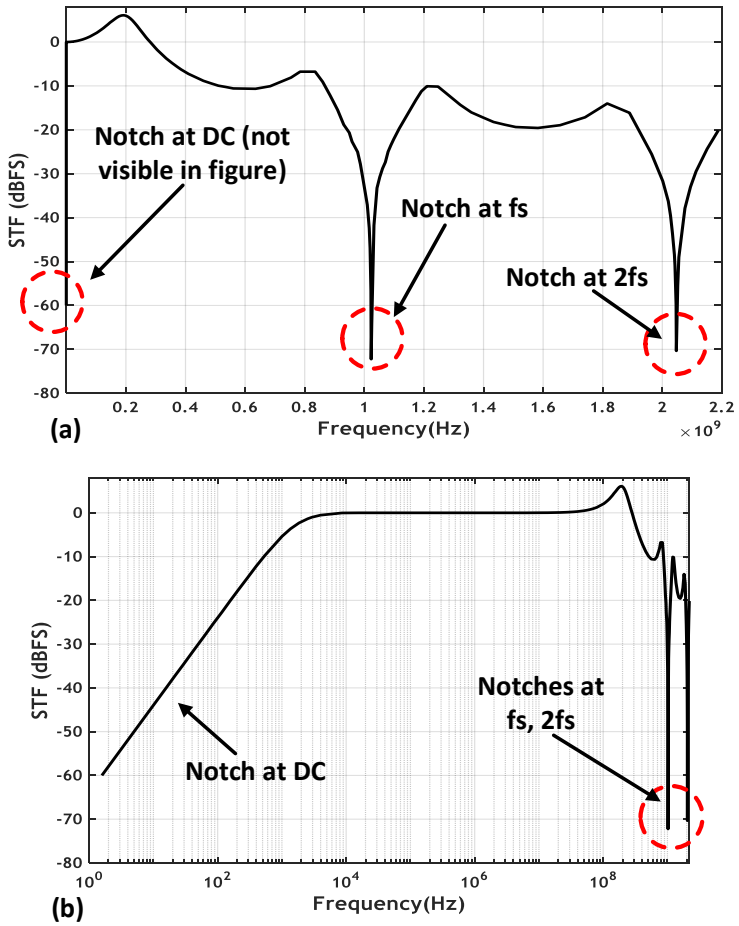

Figure 3.6: Simulated STF (a) plotted on a linear scale (b) plotted on a logarithmic scale

Fig. 3.5(a) shows the linear model of the system, where $N = 63$ and the differential input full scale is normalized to 1. In Fig. 3.5(a), D <1>denotes the retimed output of the first XOR gate and this path is used for DC feedback. D_{OUT} represents the overall output of the modulator and is denoted as the summation of all retimed XOR outputs. Since only a single pair of

pseudo-resistors is used, this asymmetry causes low frequency quantization noise to increase, as illustrated through behavioral simulations in the spectra of Fig. 3.5(b). However, as demonstrated by Fig. 3.5(c), this low frequency quantization noise injection does not affect the modulator's SQNR within the input signal bandwidth as long as the pseudo-resistor is greater than 5 MΩ, which is guaranteed by design. Fig. 3.6(a) and Fig. 3.6(b) plot the simulated STF on a linear scale and logarithmic scale respectively. The STF null at DC is clearly visible from Fig. 3.6(b).

3.5 Circuit Implementation

The output of every stage in the ring oscillator is buffered by a skewed inverter and then sensed by a standard single-ended latch, as shown in Fig. 3.4. Errors due to mismatch among the VCO's transistors are up-modulated (PWM modulated) to the VCO's center frequency (fc) and its multiples. Since $fc = 70$ MHz nominally, these up-modulated mismatch errors do not affect the ADC performance within the 20 MHz signal bandwidth. Moreover, since mismatch among VCO's transistors shows up as an additive error in *phase* quantization, therefore, in addition to being PWM modulated, these errors will also be shaped by the NTF. Although the VCO's input capacitance is increased in presence of multiple input transistors, the choice of capacitive input and capacitive DAC ensures that the VCO's input parasitic capacitance only causes an attenuation instead of a pole in the loop's transfer function.

The VCO's input transistors are thick oxide devices to prevent gate

leakage. R_F is a 450 kΩ poly-resistor and C_F is implemented by a thick-oxide MOSCAP with a MOM capacitor stacked above it. Each DAC unit capacitor is an 8 fF MOM capacitor and the ADC's input capacitance (C_{IN} in Fig. 3.4) is 504 fF. Pseudo-resistor R_P is implemented by thick oxide transistors with deep N-well to prevent undesirable leakage currents from flowing towards the VCO's input nodes, $V_{XP/M}$. Retiming is performed using TSPC DFFs to save clocking power. Except the pseudo-resistor and passive filter, the rest of the modulator's core is laid out in a modular fashion. As highlighted in the die photo of Fig. 3.7, a single slice in the modular layout has a width of only 2.9 μm and consists of a vertical stack of unit differential input and DAC capacitors, a single pair of VCO input transistors and associated digital circuits. The core is constructed by placing 63 such identical slices horizontally next to one another.

3.6 Measurement Results

The prototype modulator is fabricated in 40 nm CMOS. The core area, including passive filter, is 0.02 mm^2. The differential full-scale input voltage is 2.4 V. Fig. 3.7 shows the die photo and the layout of an individual slice of the core. At $f_S = 1.024$ GHz, the measured SNDR, SNR and DR are 59.1 dB, 62.1 dB and 63.1 dB respectively in a 20 MHz bandwidth (480 kHz to 20.48 MHz).

Fig. 3.8 plots measured SNR/SNDR versus input amplitude and measured power breakdown. The total power is 2.5 mW, of which 2.06 mW is

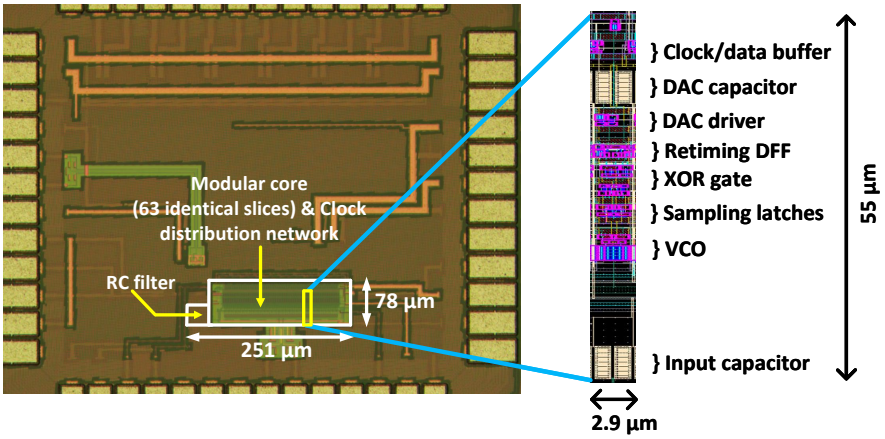

Figure 3.7: Die photo (left) and layout of individual slice (right)

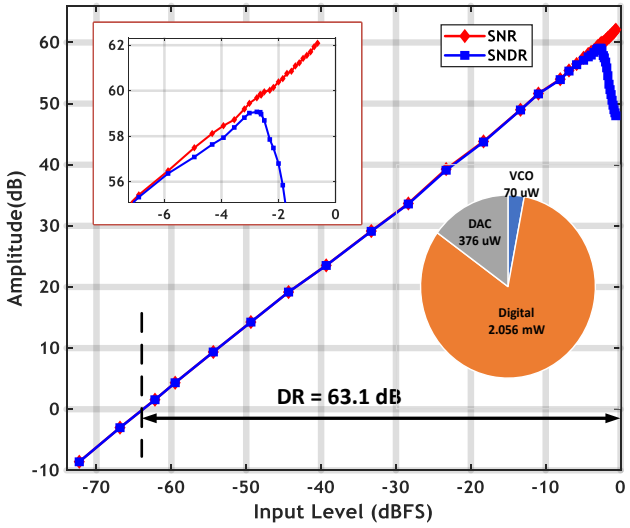

Figure 3.8: Measured SNR/SNDR vs input amplitude and power breakdown

from digital circuits, 0.38 mW from DAC references, and 0.07 mW from VCO. It is to be noted that the thermal-noise dominant VCO consumes only 3% of the total power. The digital circuits (inverters, XOR, DFFs) consume 80%,

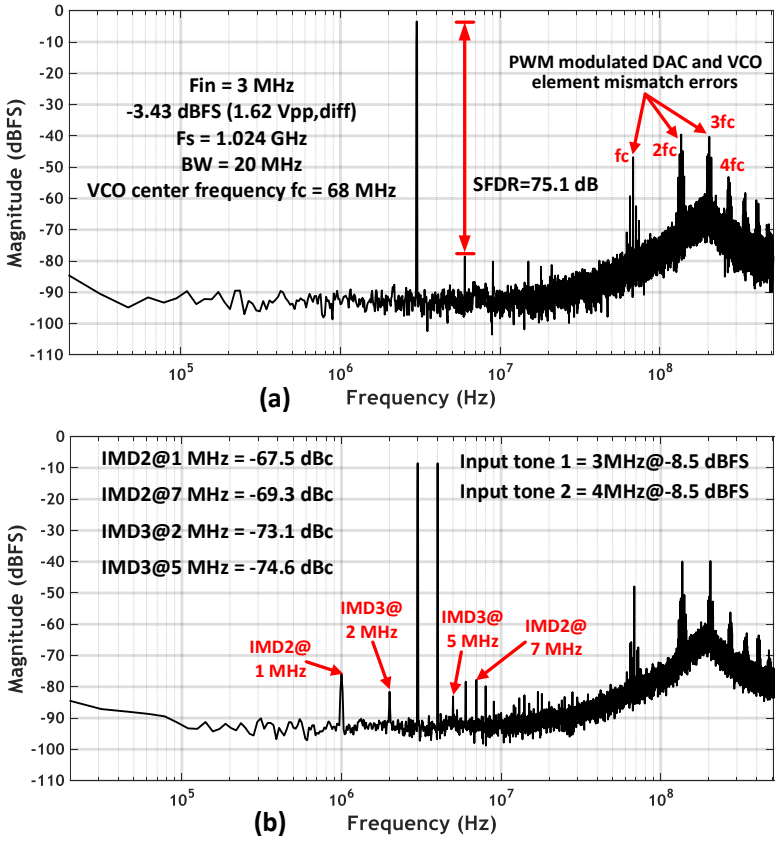

Figure 3.9: (a) Measured spectrum with a 3 MHz, −3.43 dBFS input signal (b) Measured spectrum with two in-band tones at 3 MHz and 4 MHz, each having amplitude of −8.5 dBFS

but their power would significantly decrease if implemented in a better process (e.g., 16 nm CMOS as in Huang et al. [2017]).

The performance is mostly limited by quantization noise. Fig. 3.9(a) shows the measured spectrum with a 3 MHz, −3.4 dBFS input signal. Fig. 3.9(b) shows the measured spectrum with two tones at 3 and 4 MHz, each of

Table 3.1: Performance comparison for proposed 1st order VCO-based ADC

	VLSI 2012 Taylor	ISSCC 2012 Reddy	VLSI 2014 Young	VLSI 2013 Rao	VLSI 2015 Reddy	ISSCC 2017 Huang	**This work**
OTA Free	Yes	No	No	Yes	No	No	**Yes**
Calibration/ DEM Free	No	No	Yes	No	No	No	**Yes**
Noise shaping order	1st	2nd	3rd	1st	4th	4th	**1st**
Process(nm)	65	90	65	90	65	16	**40**
Area(mm^2)	0.075	0.36	0.49	0.16	0.5	0.217	**0.02**
Fs(GHz)	1.3	0.6	1.28	0.64	1.2	2.15	**1.024**
BW(MHz)	20.3	10	50	5	50	125	**20**
OSR	32	30	12.8	64	12	8.6	**25**
SNR(dB)	70	83	71	75.4	71.7	72.6	**62.1**
SNDR(dB)	69	78.3	64	73.9	71.5	71.9	**59.1**
DR(dB)	71	83.5	75	77	72	74.8	**63.1**
Supply(V)	0.9	–	1.5/1.2	1.2/1	–	1.35/1.5/1	**1.1**
Power(mW)	11.5	16	38	4.1	54	54	**2.5**
FOMw** (fJ/step)	123	120	294	101	176	67.2	**85**

$^{**}FoMw = Power/(2^{*}BW^{*}2^{ENOB})$, $ENOB = (SNDR-1.76)/6.02$

−8.5 dBFS amplitude. The measured IMD2 are −67.5/−69.3 dBc at 1 MHz/7 MHz, and measured IMD3 are −73.1/−74.6 dBc at 2 MHz/5 MHz. Table 3.1 compares the performance of the fabricated chip with the state-of-the-art. As highlighted in Table 3.1, to the authors' best knowledge, this work is the first capacitive-input CTDSM with sampling rate greater than 1 GHz. It replaces the OTA by a scaling-friendly and parasitic pole-mitigated VCO, achieving a Walden FOM of 85 fJ/step.

Chapter 4

A 74.5 dB Dynamic Range 10 MHz BW CT-$\Delta\Sigma$ ADC with Distributed-Input VCO and Embedded Capacitive-π Network in 40 nm CMOS

4.1 Introduction

This chapter presents significant architectural improvements over the first order VCO based ADC presented in the previous chapter. In the previous chapter, we introduced a fully differential distributed-input VCO topology that virtually eliminates the VCO's voltage-to-frequency (V-F) parasitic pole [Mukherjee et al. [2019]]. By using a VCO that *inherently* alleviates the effect of the V-F parasitic pole, no additional active circuits were required for parasitic pole mitigation, thus making this type of VCO an ideal candidate for wideband closed loop CTDSMs. However, the previous chapter demonstrated the use of the distributed-input VCO in a first order modulator which had a limited quantization noise shaping capability. To adequately suppress the quantization noise within a relatively wide bandwidth, the previous chapter's modulator [Mukherjee et al. [2019]] used a 63-stage ring VCO (which is equivalent to a 6-bit quantizer), resulting in very large digital power consumption (digital circuits accounting for 80% of the overall power). Despite such a high

quantizer resolution, the in-band spectrum of the previous chapter's modulator was still dominated by quantization noise, thus limiting the overall power efficiency (FoM) of the CTDSM. Since the distributed-input VCO has a relatively large input gate capacitance, the previous chapter's modulator used capacitive input and capacitor DAC to drive the VCO, in order to ensure that the VCO's input gate capacitance caused no additional pole in the loop. However, the downside of capacitively coupling the input was that the modulator could not digitize low frequency inputs. In fact, the previous chapter's modulator could only digitize input signals higher than 480 kHz. In summary, despite the merits of the distributed-input VCO topology, deficiencies in the *modulator's architecture* limited the application space and overall power-efficiency of the previous chapter's modulator.

This chapter attempts to leverage the full potential of the distributed-input VCO topology that we introduced in the previous chapter, by using the distributed-input VCO as the back-end (second-stage) integrator and quantizer within a power-efficient second order modulator architecture. As compared to the previous chapter's modulator which possessed only first order noise shaping, the more aggressive (second order) noise shaping of our proposed CTDSM relaxes the requirement of the VCO quantizer's resolution, thus lowering digital power. Our proposed modulator's in-band spectrum is dominated by thermal noise, resulting in a significantly better measured FoM as compared to the previous chapter's modulator. Since our proposed CTDSM uses resistive input, it can digitize signals from close to DC, unlike the previous chapter's

modulator. Choosing 31 stages in the ring VCO greatly reduces the voltage swing of the quantization noise that is processed by our modulator's front-end integrator. This, in turn, relaxes the linearity requirement of the front-end integrator, thereby permitting the use of an energy-efficient Gm-C integrator at the front-end. Since the gate capacitance of the distributed-input VCO is absorbed within the load capacitance of the Gm-C integrator, no additional parasitic pole is formed due to the VCO's gate capacitance.

Our proposed modulator uses a pair of low power inner capacitor DACs for ELD compensation. When using a front-end Gm-C integrator to directly drive a capacitor DAC, the major challenge is to allow the Gm-C integrator to be impedance scaled up for thermal noise *without* simultaneously sizing up the inner capacitor DAC. A key highlight of this chapter's CTDSM is that we demonstrate the use of a capacitive-π network to make the capacitor DAC's feedback coefficient independent of the Gm-C integrator's load capacitance. This allows us to use small-size DAC unit capacitors resulting in significant savings in both analog and digital power, as will be explained later in this chapter. Similar to the previous chapter's CTDSM, this chapter's modulator also possesses intrinsic clock level averaging (CLA) [Lee et al. [2015]] which naturally up-modulates DAC mismatch errors out-of-band. Consequently, our prototype CTDSM does not require any DAC calibration or explicit DEM circuits. The prototype second order CTDSM proposed in this chapter has been fabricated in 40 nm CMOS and occupies a core area of 0.064 mm^2. The measured SNDR, SNR and DR are 71.8 dB, 72.9 dB and 74.5 dB respectively

in a 10 MHz bandwidth at 655 MS/s, resulting in an SNDR-based Walden FoM of 45.6 fJ/step, SNDR-based Shreier FoM of 167.2 dB and DR-based Shreier FoM of 169.9 dB.

4.2 Architecture and Implementation of Proposed CTDSM

4.2.1 Conceptual Evolution of Architecture

This section explains the conceptual evolution of our proposed 2nd order CTDSM architecture which uses the distributed-input VCO both as the second stage (voltage-to-phase) integrator as well as the phase quantizer. Since the resolution of a VCO-based quantizer is not constrained by the supply voltage, we try to fully leverage this property by targeting a high resolution from the VCO quantizer. This design uses a 31-stage ring VCO, which effectively translates to a 5-bit internal quantizer. A relatively high quantizer resolution lowers the LSB of the quantization error, thereby relaxing the linearity requirement of the front-end integrator. Consequently, the front-end integrator can be implemented as a Gm-C integrator which is inherently more energy efficient than its active RC counterpart. Since the distributed-input VCO can potentially have a relatively large input capacitance, a Gm-C integrator seems to be a natural choice to drive the VCO since the VCO's input capacitance can be absorbed within the transconductor's load capacitance and hence no additional pole is formed due to the VCO's input capacitance.

As shown in Fig. 4.1(a), it might seem intuitive to directly connect the output of the transconductor (Gm-stage) to the VCO's input. In Fig. 4.1(a),

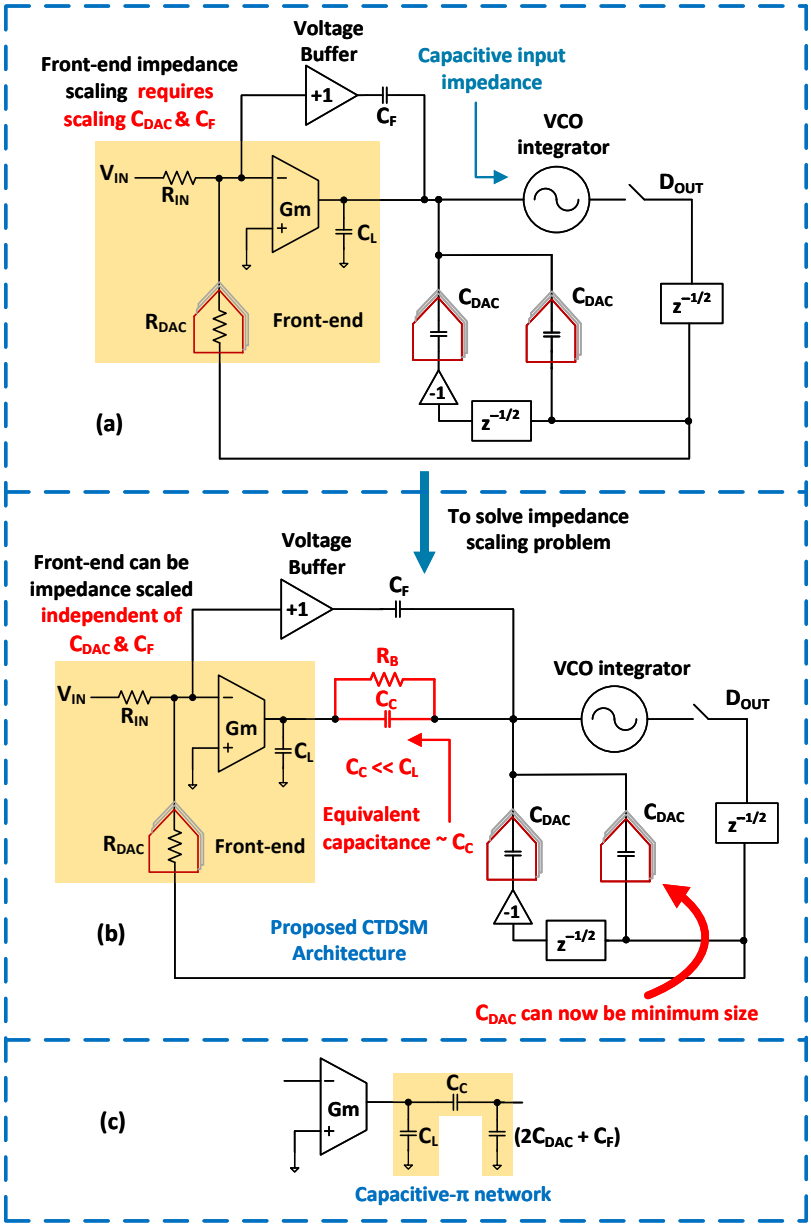

Figure 4.1: Conceptual evolution of the proposed 2nd order CTDSM architecture: (a) Intuitive starting point (b) Proposed CTDSM with embedded capacitive-π network (c) Constitution of the capacitive-π network

ELD compensation is achieved by differentiating the modulator's output with capacitor DACs (C_{DAC} in Fig. 4.1(a)) in a semi-analog fashion and injecting it in front of the VCO integrator to equivalently realize a direct path around the quantizer [Mitteregger et al. [2006]; Bolatkale et al. [2011]]. The loop filter's first order (1/s) path is realized by a unity-gain voltage buffer driving a feedforward capacitor (C_F). The capacitive input impedance of the VCO enables the use of a low power and inherently wideband passive (capacitive) adder to perform signal summation at the VCO's input [Bolatkale et al. [2011]]. The outer DAC is chosen to be a resistor DAC (R_{DAC} in Fig. 4.1(a)) since resistor DACs generate lesser noise, have better matching and can operate under a lower supply voltage compared to current steering DACs ($I_{DAC}s$). Furthermore, unlike an I_{DAC}, using an R_{DAC} reduces the voltage swing at the input of the Gm-stage by half, thus further relaxing the Gm-C integrator's linearity requirement. For the architecture of Fig. 4.1(a), the capacitive feedforward coefficient (α_F) and the capacitive DAC feedback coefficient (α_D) are expressed as follows:

$$\alpha_F = \frac{C_F}{C_L + C_F + 2C_{DAC}} \tag{4.1}$$

$$\alpha_D = \frac{C_{DAC}}{C_L + C_F + 2C_{DAC}} \tag{4.2}$$

The architecture of Fig. 4.1(a) however suffers from one major limitation. In order to meet any arbitrary thermal noise specification, impedance scaling up the modulator's front-end would include scaling up both Gm and

C_L. But scaling up C_L in Fig. 4.1(a) would require the feedforward capacitor C_F and the capacitor DACs C_{DAC} to be *simultaneously scaled up* by the same factor in order to preserve the same capacitive feedforward coeffcient (α_F) and capacitor DAC feedback coefficient (α_D). Scaling up C_{DAC} would proportionately increase the (charging/discharging) power of the C_{DAC}. Moreover, larger C_{DAC} unit capacitors would have to be driven by stronger inverters, which in turn would demand greater driving strength from the preceding digital circuits (such as the C_{DAC} retiming latches), thereby leading to a significant increase in overall digital power. Furthermore, scaling up C_F would demand more power in the voltage buffer for the following reason. C_F and the voltage buffer's finite output resistance together form a pole which introduces a delay in the loop's first order path. To maintain the same pole frequency in presence of a higher C_F, the voltage buffer's output resistance would have to be reduced, thus necessitating higher bias current in the buffer. Therefore, for the architecture of Fig. 4.1(a), an attempt to lower the front-end noise would eventually require an increase in both analog as well as digital power, making the architecture of Fig. 4.1(a) practically infeasible.

The solution to this problem is demonstrated in Fig. 4.1(b). The solution involves coupling the Gm-stage output to the VCO's input through a capacitor C_C. As highlighted in Fig 4.1(c), a capacitive-π network is hence formed by C_L, C_C and the remaining equivalent capacitance at the VCO's input. A large resistor R_B biases the VCO's input and also ensures DC feedback in the loop. As shown in Fig. 4.1(b), the series combination of C_C and C_L is

the equivalent capacitance that loads C_{DAC} and C_F. With C_C being chosen to be much smaller than C_L, the capacitor DACs and C_F are loaded by an approximately constant capacitance ($=C_C$). This therefore permits Gm and C_L to be impedance scaled up to any arbitrary extent, without attenuating the feedforward and C_{DAC} feedback factors. This implies that, regardless of how large C_L is, we can still use very small size C_{DAC} unit capacitors (and consequently a smaller C_F), thus significantly reducing the power consumption of the voltage buffer, the C_{DAC}s and the digital circuits driving the C_{DAC}s. Owing to the capacitive feedforward path (realized by C_F), the output voltage of the Gm-stage is devoid of any input signal component, thus lowering the Gm-C integrator's harmonic distortion. Fig 4.1(b) thus represents the architecture of the modulator proposed in this work. In our final design, $C_L \approx 1pF$ and $C_C \approx 100fF$.

4.2.2 Modulator Implementation

Fig. 4.2(a) shows the fully differential implementation of the proposed second order CTDSM in which a 31-stage fully differential VCO is used as the second stage integrator and quantizer. This work adopts the dual VCO scheme [Lee et al. [2015]; Li et al. [2017]] which uses XOR gates to measure the phase difference between two oscillators which are driven in a fully differential fashion. The outputs of the 31 XOR gates represent the modulator's quantized phase output. The two oscillators are nominally frequency-locked with respect to each other, with the oscillation frequency being determined by the

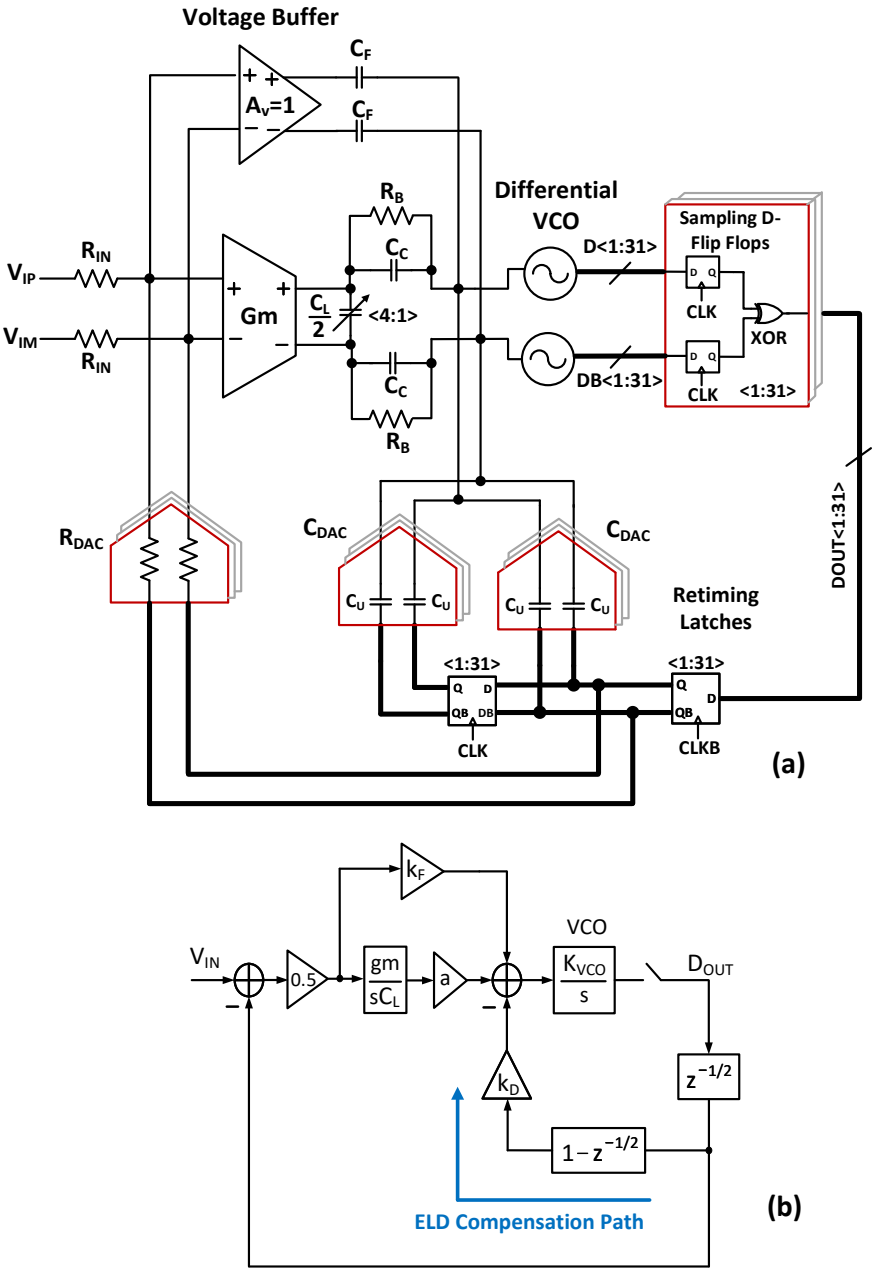

Figure 4.2: (a) Fully differential schematic of the proposed 2nd order CTDSM (b) Linear model of the proposed CTDSM

differential VCO's tail current. This type of phase detection scheme possesses intrinsic clock level averaging (CLA) [Lee et al. [2015]] which up-modulates DAC mismatch errors to even multiples of the VCO's center frequency. Consequently, our modulator does not require any DAC calibration or explicit DEM circuitry.

In addition to making the C_{DAC} unit capacitance unconstrained with respect to front-end impedance scaling, the coupling capacitor C_C provides the secondary benefit of suppressing the differential component of the VCO's kickback noise and C_{DAC} switching transients, when referred to the Gm-stage output. The Gm-C integrator's differential load capacitance ($C_L/2$ in Fig. 4.2(a)) is implemented as a digitally programmable bank of MOM (metal-oxide-metal) capacitors with ±45% trimming range. All DACs are NRZ (non-return-to-zero) type. The unity-gain voltage buffer and the Gm-C integrator both operate under 1.2 V supply. The reference voltage for all DACs (outer R_{DAC} and two inner C_{DAC}s) is 1.1 V. The VCO supply and the digital supply are also 1.1 V. Fig. 4.2(b) shows the linear model of the proposed CTDSM, wherein the factors a, k_F and k_D represent capacitive attenuation caused by C_C, C_F and C_{DAC} respectively.

We next investigate the effect of the VCO's bias resistor (R_B in Fig. 4.2(a)) on the modulator's stability. The out-of-band NTF (and hence the modulator's stability) is predominantly determined by the faster paths in the loop, namely, the first order and direct paths. To qualitatively understand the effect of R_B on stability, we therefore analyze the impulse response of the

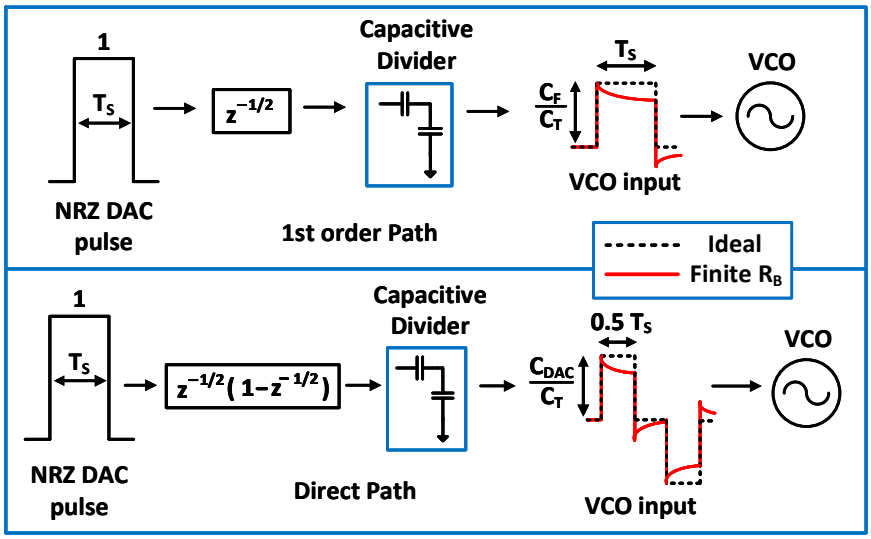

Figure 4.3: Comparison of impulse response waveforms for the loop's 1st order and direct paths with infinite R_B (dotted line) and finite R_B (solid red line).

loop's first order and direct paths. Fig. 4.3 compares the impulse response waveforms of the first order and direct paths for a finite R_B and for infinite R_B. In Fig. 4.3, C_T represents the total capacitance at the VCO's input. When R_B is infinite (dotted line in Fig. 4.3), the NRZ DAC pulse appears as a scaled pulse at the VCO's input, with the scaling factor being determined by the corresponding capacitor divider. However, a finite R_B causes the pulse response at the VCO's input to exponentially decay with a time constant which is determined by R_B, as indicated by the solid line in Fig. 4.3. It is evident that the resulting error in the sampled impulse response would become negligible only if $R_B C_C \gg T_S$, where $T_S = 1/f_S$ is the ADC's sampling interval.

A commonly used technique to realize a very large effective resistance with a small area is to use a pseudo-resistor, which is basically a transistor

operating in cutoff region (as shown in Fig. 3.4 of the previous chapter). The effective resistance of a pseudo-resistor could even be in the GΩ range. However, when such a large R_B is directly connected to the VCO's gate, the gate leakage current of the VCO's input transistors could potentially cause a substantial DC voltage drop across R_B. In fact, the gate leakage current is not negligible in the core devices of the 40 nm CMOS process that is used for our fabricated chip. To minimize the gate leakage current, the only solution would then be to use thick oxide devices for the VCO's input transistors. But, compared to core devices, thick oxide devices are bulkier with greater parasitic capacitances and hence yield lower VCO tuning gain (K_{VCO}) for the same device size. In our design, we use core devices for the VCO's input transistors to achieve the desired K_{VCO} with smaller sized transistors. We implement R_B as a 400 kΩ poly-resistor. Simulations show that the gate leakage current of our VCO's input transistors causes negligible voltage drop across the 400 kΩ poly-resistor. Since $C_C \approx 100$ fF in our design, $R_B C_C \approx 40$ ns which is still much greater than our modulator's sampling interval T_S of 1.5 ns.

4.2.3 Gm-C Integrator and Voltage Buffer

Fig. 4.4(a) shows the schematic of the Gm-stage of the front-end Gm-C integrator. The degeneration resistance ($2R_D$ in Fig. 4.4(a)) is implemented as a digitally programmable bank of poly-resistors with ± 20 % trimming range. Pmos cascode devices (M3, M4 in Fig. 4.4(a)) are used to increase the DC gain. The VCO's input is biased by the Gm-C integrator's output common

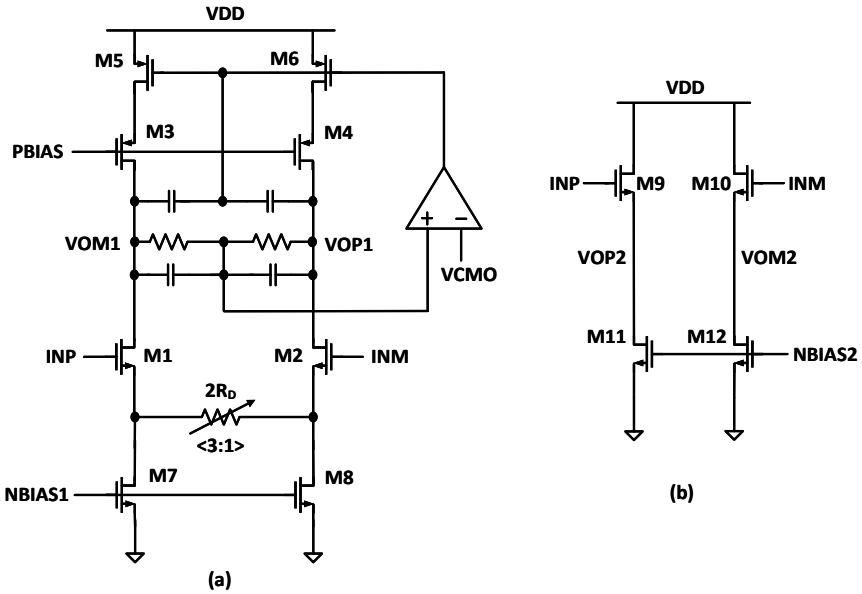

Figure 4.4: (a) Gm-stage (b) Voltage buffer implemented as source follower

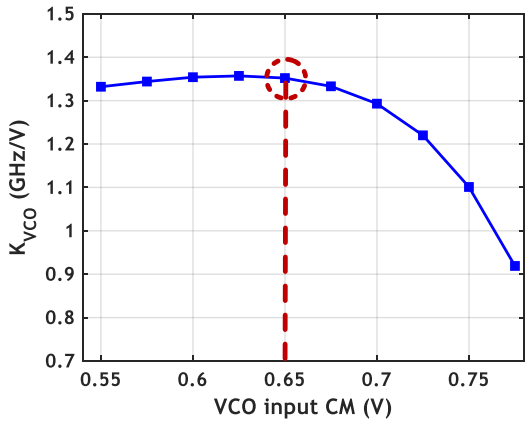

Figure 4.5: K_{VCO} vs VCO's input common mode voltage (VCMO)

mode voltage (VCMO). Fig. 4.5 shows the VCO's tuning gain (K_{VCO}) as a function of the VCO's input common mode voltage (VCMO). For our design, we choose VCMO to be 650 mV. As depicted in Fig. 4.5, using larger values of

VCMO (around 750 mV or higher) lowers K_{VCO} and also makes K_{VCO} more sensitive to variations in VCMO. Hence, we do not use NMOS cascode devices in the Gm-C integrator since doing so would require a higher VCMO. The loop filter's unity-gain voltage buffer is implemented by a pair of source followers as shown in Fig. 4.4(b). The source followers' in-band noise and distortion are first-order high-pass shaped when referred to the ADC's input and hence the voltage buffer has very little effect on the in-band performance. However, the finite output resistance of the source follower causes an additional pole in conjunction with capacitor C_F. Thus, the source follower's bias current is primarily determined by its output resistance specification. The effect of the voltage buffer's output resistance on the modulator's stability will be discussed in detail in Section 4.3.1.

4.2.4 VCO

Fig. 4.6 shows the implementation details of the VCO along with the sampling D-Flip Flops. The VCO uses the distributed-input topology with a very small degeneration resistance for linearization. Fig. 4.7 plots the waveforms of the VCO's internal nodes when a small differential input step is applied at the VCO's inputs (INP and INM in Fig. 4.6). Fig. 4.7 shows that when a differential step is applied to the VCO, the tail nodes V_{TAIL1} and V_{TAIL2} tend to follow the respective gate voltages, thereby effectively lowering the gate-source voltage (V_{GS}) of the input transistors and resulting in a more linear V-F conversion. However, V_{TAIL1} and V_{TAIL2} take a finite time

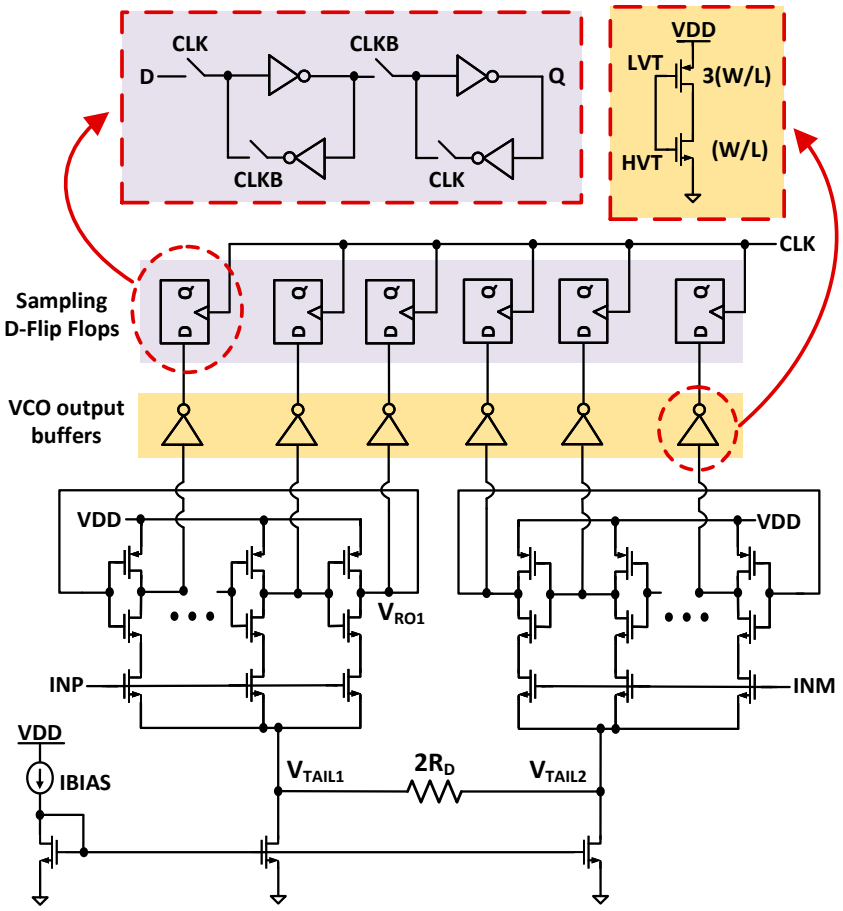

Figure 4.6: Schematic of VCO including VCO's output buffers and sampling D-Flip Flops

to respond to the VCO's input step. The transition delays (fall times) of the VCO's individual inverter stages (and hence the overall oscillation frequency) can reach their steady state values only $after$ V_{TAIL2} and V_{TAIL2} have settled. Thus, V_{TAIL1} and V_{TAIL2} cause memory effects to propagate across successive inverter transitions, thereby re-introducing the VCO's V-F parasitic pole.

The parasitic pole (f_p) associated with nodes V_{TAIL1}, V_{TAIL2} in Fig.

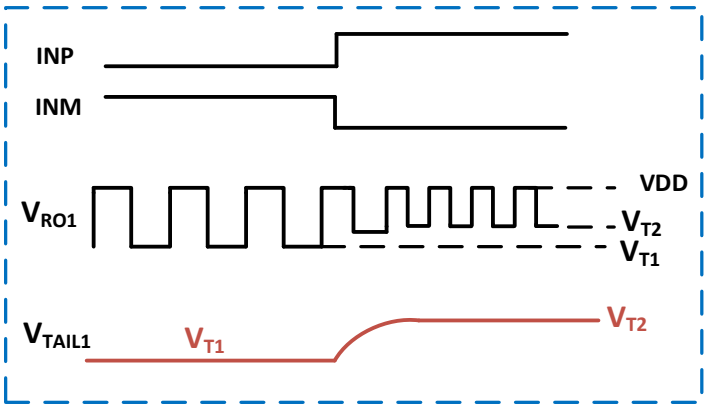

Figure 4.7: Waveforms of internal nodes for the resistively degenerated distributed-input VCO of Fig. 4.6 in response to a differential input step

4.6 can be expressed as,

$$f_p \approx \frac{1}{2\pi(R_{CCO}\|R_D)\frac{N}{2}C_L} \tag{4.3}$$

where C_L denotes the parasitic capacitance at the output of each inverter in the ring VCO.

As shown in Eq (4.3), the equivalent resistance at V_{TAIL1}, V_{TAIL2} is the parallel combination of R_D and the resistance looking up into the oscillator (R_{CCO}). Therefore, the degeneration resistor ($2R_D$ in Fig. 4.6) can be used as a 'tuning knob' to trade-off the VCO's V-F linearity and its parasitic pole frequency, while maintaining the *same center frequency*. The center frequency is set by tail current and is not a function of R_D. Thus, unlike the conventional Gm-CCO (Fig. 3.1(a) in the previous chapter) whose V-F parasitic pole frequency is always near the center frequency, the resistively degenerated

distributed-input VCO of Fig. 4.6 enables the parasitic pole frequency to be controlled independent of the VCO's center frequency. As $R_D \to 0$, $f_p \to \infty$ and the circuit returns to the original distributed-input VCO topology (Fig. 3.1(b) of the previous chapter).

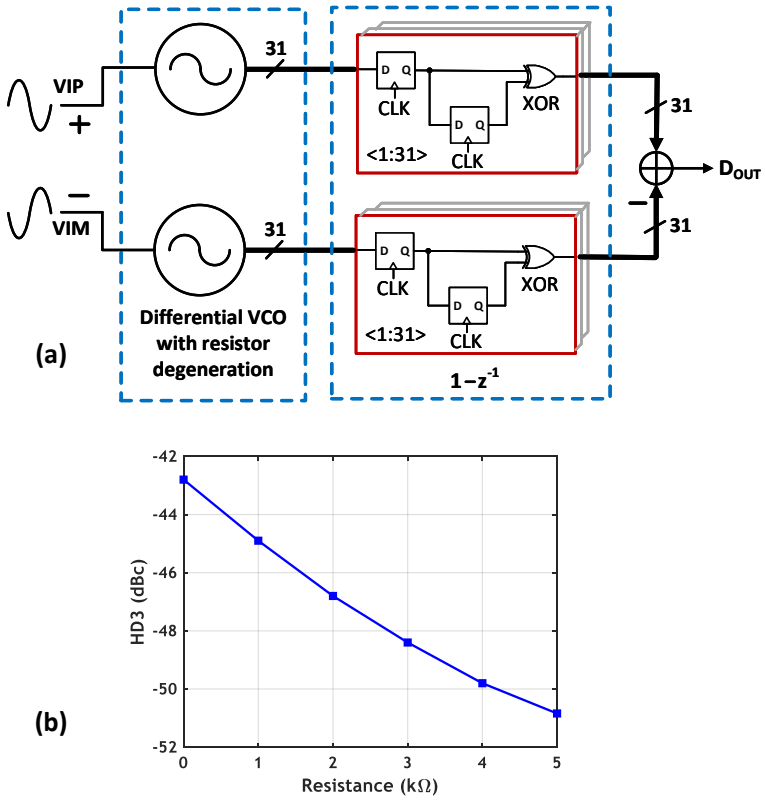

Figure 4.8: (a) Simulation setup for evaluating the linearity of the resistively degenerated distributed-input VCO (b) HD3 in D_{OUT} vs VCO's degeneration resistance

Fig. 4.8(a) shows the simulation setup for evaluating the linearity of the resistively degenerated distributed-input VCO. A 31-stage differential VCO is driven by a 160 mV differential peak-to-peak sinusoidal input while running in

an open loop fashion. The output phase of each oscillator is first digitally differentiated with XOR gates [Straayer and Perrott [2008]] and then subtracted, thus effectively using the VCO as an open-loop voltage to frequency converter. Fig. 4.8(b) plots the third harmonic distortion (HD3) in the digitized differential output of the open-loop VCO (D_{OUT} in Fig. 4.8(a)) as a function of the VCO's degeneration resistance. The linearization is evident from Fig. 4.8(b) which shows that increasing the VCO's degeneration resistance helps to lower the HD3. Although not a key focus of the ADC presented in this chapter, the concept of linearization through resistor degeneration is a useful extension of our previously developed distributed-input VCO topology and hence merits discussion in this section.

It is however important to note that, since our proposed modulator uses the VCO as an integrator in closed loop, the voltage swing at the VCO's input is inherently very small, thus greatly relaxing the VCO's linearity requirement. Moreover, the front-end Gm-C integrator further helps to suppress the VCO's non-linearity when referred to the modulator's input. Consequently, our proposed CTDSM does not demand linearization of the VCO and hence, a small VCO degeneration resistance $2R_D$ of only 1 kΩ (implemented as a poly-resistor) has been used in the fabricated chip.

To protect the ring oscillator from kick-back from the sampling D-Flip Flops, each ring oscillator output is buffered by an additional inverter (labeled as 'VCO output buffers' in Fig. 4.6). Each ring oscillator output oscillates between VDD (1.1 V) and the drain voltage of the NMOS tail current sources

(nodes V_{TAIL1}, V_{TAIL2} in Fig. 4.6). The nominal voltage of V_{TAIL1}, V_{TAIL2} is around 200 mV. Due to the nearly rail-to-rail voltage swing of the ring oscillator, the VCO's output buffer is simply implemented as a skewed inverter which operates between VDD and ground. As highlighted in Fig. 4.6, the skewing of the VCO's output buffer is achieved by using a high threshold voltage (HVT) device for the NMOS transistor and using a 3-times wider, low threshold voltage (LVT) device for the PMOS transistor, similar to [Tu et al. [2017a]]. This makes the VCO buffer's PMOS much stronger than its NMOS, thereby compensating for the PMOS transistor's slightly lower on-state $|V_{GS}|(= VDD - V_{TAIL1,2})$. Since the VCO buffer's output is exactly rail-to-rail, it can be sampled by a standard single-ended master-slave D-Flip Flop, as highlighted in Fig. 4.6. The cross-coupled inverters in the master-slave D-Flip Flop are capable of providing regeneration which is especially useful when sampling voltages near $VDD/2$.

4.2.5 DACs

Each R_{DAC} unit element has a resistance of 62 kΩ. To minimize area of the overall R_{DAC} array, each R_{DAC} unit element is implemented as a single segment whose dimensions are 41 μm x 0.4 μm. The dimensions of the overall differential R_{DAC} array (consisting of 31 differential unit elements and additional dummy units) is (41 μm x 134 μm). The resistance and dimensions of the R_{DAC} unit element are chosen after balancing several trade-offs including noise, R_{DAC} power and mismatch. Since our modulator has intrinsic

CLA, our design does not use any DAC calibration or explicit DEM circuits. The mismatch considerations for the R_{DAC} as well as the optimization of the R_{DAC}'s noise/power trade-offs will be analyzed in detail in the next section (in Sections 4.3.3 and 4.3.4). In addition to experiencing intrinsic CLA, the C_{DAC} mismatch errors are also first order high-pass shaped by the front-end Gm-C integrator. Consequently, C_{DAC} mismatch is less critical as compared to R_{DAC} mismatch.

Ideally, the NTF should remain unchanged when C_{DAC}, C_F and C_C are simultaneously scaled. However, in practice, owing to the presence of a constant parasitic capacitance at the VCO's input, lowering the C_{DAC} unit capacitance degrades the C_{DAC} feedback coefficient (k_D in the linear model of Fig. 4.2(b)) and the loop filter's feedforward coefficient (k_F in Fig. 4.2(b)). The expressions for k_F and k_D are as follows:

$$k_F = \frac{C_F}{C_F + 2C_{DAC} + C_C + C_{PAR}} \tag{4.4}$$

$$k_D = \frac{C_{DAC}}{C_F + 2C_{DAC} + C_C + C_{PAR}} \tag{4.5}$$

where C_{PAR} is the total parasitic capacitance at the VCO's input. In the above equations, $C_{DAC} = 31C_U$, where C_U represents a unit capacitor of each C_{DAC}. C_{PAR} consists of the VCO's gate capacitance (C_{VCO}), the wiring parasitics (C_{WIRE}) and the substrate parasitic capacitance of the MOM capacitor plates that are connected to the VCO's inputs (C_{MOM}). That is,

$$C_{PAR} = C_{VCO} + C_{WIRE} + C_{MOM} \tag{4.6}$$

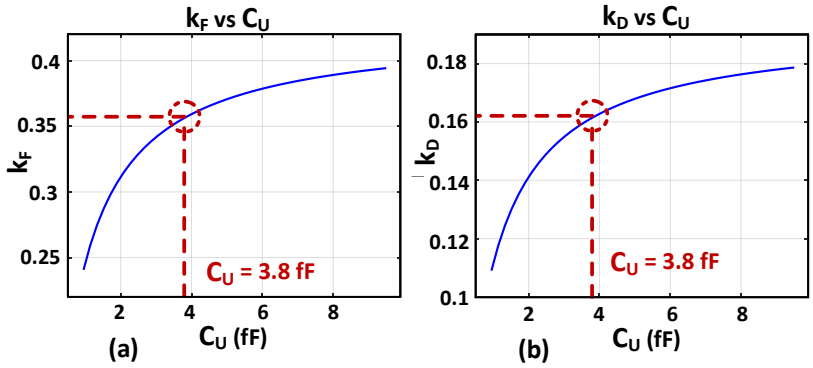

Figure 4.9: (a) k_F vs C_U when C_U, C_F and C_C are scaled together (b) k_D vs C_U when C_U, C_F and C_C are scaled together

Since the VCO's input voltage swing is very small, the non-linearity of the VCO's gate capacitance (C_{VCO}) can be ignored in our analysis. Fig. 4.9 plots k_F and k_D as a function of C_U wherein C_F, C_C and C_U are simultaneously scaled by the same factor. Upon scaling C_F, C_C and C_U, the MOM capacitor substrate parasitic capacitance C_{MOM} also scales proportionately. However, the two other components of C_{PAR}, namely C_{VCO} and C_{WIRE} do not scale upon scaling the MOM capacitors. Consequently, as confirmed by plots in Fig. 4.9, the values of k_F and k_D tend to decrease upon decreasing C_U. Furthermore, k_F and k_D vary more sharply when C_U is very small, implying a greater sensitivity of the loop filter coefficients in presence of process variations. On the other hand, a larger C_U would also demand a larger C_F, thereby increasing power consumption in the C_{DAC}s, the C_{DAC}s' preceding digital circuits and also in the source followers (assuming that we want to maintain the same frequency for the source followers' output pole). Hence, as a trade-off between power

consumption and robustness against process variations, we choose the nominal value of the C_{DAC} unit capacitance to be 3.8 fF in our design, as highlighted in Fig. 4.9. In our design, the constant component of the parasitic capacitance (namely, $C_{VCO} + C_{WIRE}$) accounts for 16% of the total capacitance connected at the VCO's inputs.

In order to reduce the substrate parasitic capacitance of the MOM capacitors at the VCO's inputs (C_{MOM} component of C_{PAR}), we asymmetrically custom layout each C_{DAC} unit MOM capacitor to have lesser substrate parasitic capacitance on the plate facing the VCO's inputs and greater substrate parasitic capacitance on the plate driven by the retiming latch. The 1σ mismatch of a 3.8 fF MOM capacitor is estimated to be 0.36%. After incorporating 0.36% mismatch between C_{DAC} unit elements in our modulator's behavioral model, simulations show that the worst-case SQNR is 85 dB (which is only 2 dB below the ideal SQNR of 87 dB) across 500 Monte Carlo runs.

4.3 Analysis of Design Trade-offs

4.3.1 Effect of Voltage Buffer's Output Resistance

In this section, the effect of the voltage buffer's finite output resistance is analyzed. Fig. 4.10 shows the three different paths of the loop gain with the voltage buffer's output resistance denoted as R_{BUF}. The lumped parasitic capacitance at the VCO's input is denoted as C_{PAR}. The following analysis assumes that $C_C \ll C_L$. We also assume that $R_B C_C \gg T_S$ and thus, the effect of VCO's bias resistor R_B can be safely ignored in the foregoing analysis. The

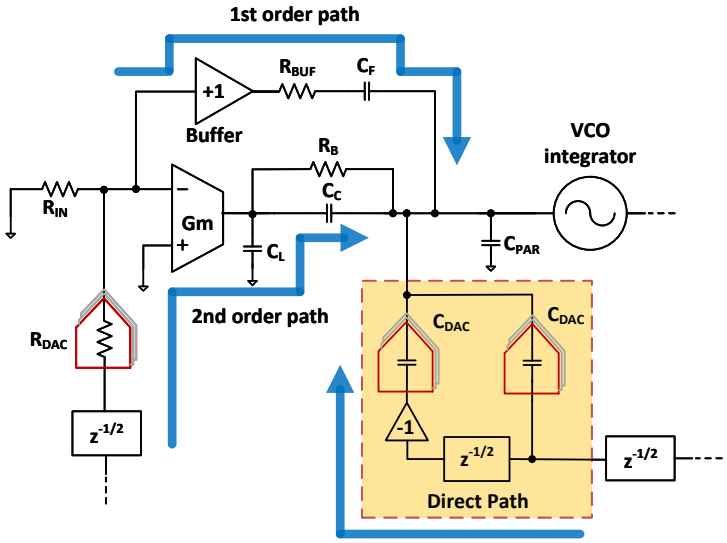

Figure 4.10: The three different paths of the loop gain

total equivalent capacitance at the VCO's input (C_T) is expressed as

$$C_T = C_F + 2C_{DAC} + C_C + C_{PAR} \tag{4.7}$$

In order to account for the buffer's finite output resistance (R_{BUF}) while evaluating the NTF, the ideal transfer functions of the 2nd order, 1st order and direct paths of the loop gain (as highlighted in Fig. 4.10) need to be multiplied by transfer functions $H_2(s)$, $H_1(s)$ and $H_0(s)$ respectively, where

$$H_2(s) = H_0(s) = \frac{1 + \frac{s}{\omega_{BUFF}(1-\frac{C_F}{C_T})}}{1 + \frac{s}{\omega_{BUFF}}} \tag{4.8}$$

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_{BUFF}}} \tag{4.9}$$

and ω_{BUFF} represents the pole associated with R_{BUF} and is expressed as,

$$\omega_{BUFF} = \frac{1}{R_{BUF}C_F(1 - \frac{C_F}{C_T})} \tag{4.10}$$

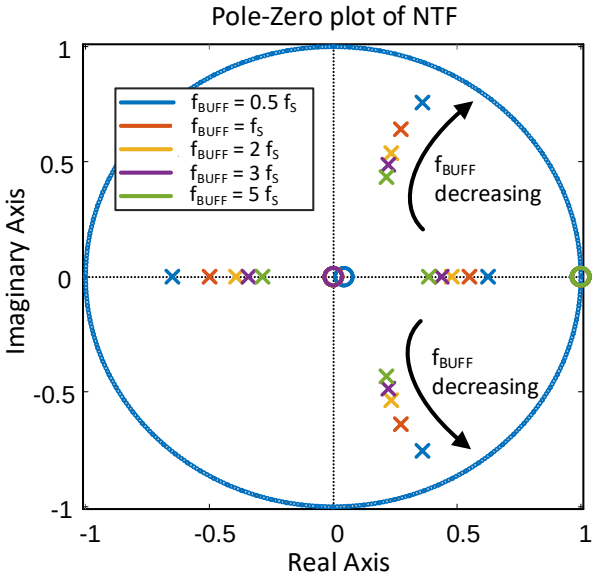

Figure 4.11: Loci of the NTF's poles and zeros as a function of f_{BUFF}

In our design, $C_F/C_T = k_F = 0.36$. Equations (4.8) and (4.9) show that the effect of R_{BUF} is the creation of a pole in the loop's 1st order path and a pole-zero pair in the loop's 2nd order and direct paths. Fig. 4.11 shows the loci of the NTF's poles and zeros as a function of the buffer's output pole (f_{BUFF}) where $f_{BUFF} = \omega_{BUFF}/2\pi$. Ideally, the NTF is designed to have only one pair of complex-conjugate poles. As can be observed in Fig. 4.11, a finite R_{BUF} causes extra real poles in the NTF. Upon progressively decreasing the buffer's output pole (f_{BUFF}), all NTF poles move towards the unit circle. However, it is the NTF's *complex-conjugate* pole-pair that *first* reaches the unit circle. Therefore, to assess the system's stability with respect to variations in f_{BUFF}, it is sufficient to only evaluate the magnitude of the NTF's complex-conjugate

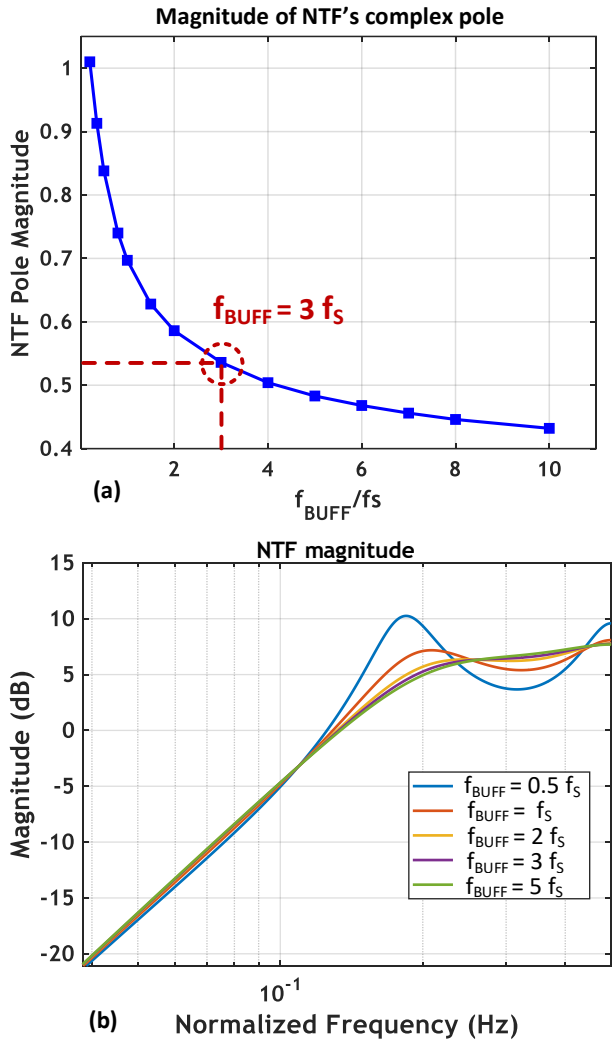

Figure 4.12: (a) Magnitude of NTF's complex pole as a function of normalized buffer output pole (f_{BUFF}/f_S) (b) Out-of-band NTF magnitude

poles.

Fig. 4.12(a) plots the magnitude of the NTF's complex-conjugate pole as a function of the buffer's output pole normalized with respect to the sam-

pling rate (f_{BUFF}/f_S). The slope of this curve indicates the modulator's sensitivity with respect to variations in f_{BUFF}. As a trade-off between power consumption and robustness against variations in f_{BUFF}, we have chosen $f_{BUFF} = 3f_S$ for this design (as highlighted in Fig. 4.12(a)). This translates to $R_{BUFF} = 330\ \Omega$. Fig. 4.12(b) shows the out-of-band NTF magnitude for different values of f_{BUFF}.

4.3.2 Stability in presence of K_{VCO} variation

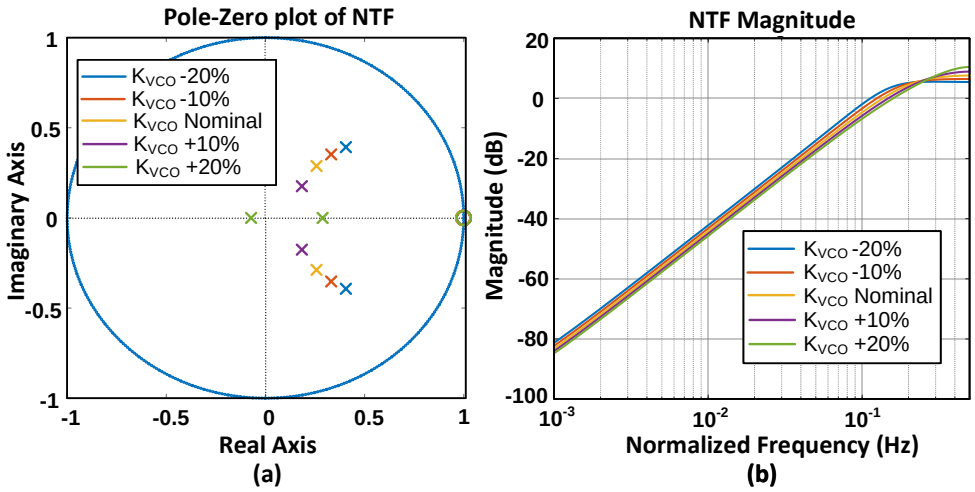

Figure 4.13: (a) Loci of NTF poles and zeros with ±20% K_{VCO} variation (b) NTF magnitude with ±20% K_{VCO} variation

Although the Gm-C integrator's load capacitor is made digitally trimmable, no such digital trimming option is included in the VCO in order to simplify the VCO's design. Simulations show that the variation in the VCO's tuning gain (K_{VCO}) across corners and temperature is within ±20%. Fig. 4.13(a) plots the loci of the NTF's poles and zeros in presence of ±20% K_{VCO} varia-

tion. Fig. 4.13(b) plots the NTF's magnitude as K_{VCO} varies by ±20%. Fig. 4.13(a) and Fig. 4.13(b) confirm that the modulator remains reliably stable in presence of ±20% K_{VCO} variation.

4.3.3 Noise and Power Breakdown

In our design, 17% of the total in-band noise is allocated to quantization noise and the remaining 83% is allocated to electronic noise (thermal and flicker noise). Out of the total electronic noise, about 75% is allocated to the front-end (Gm-C integrator, input resistor and resistor DAC) and the remaining 25% is allocated to the back-end (VCO, VCO's bias resistors and source followers).

Fig. 4.14 shows the total front-end power (power of the Gm-C integrator and resistor DAC) as a function of the modulator's input resistance, while maintaining the same total front-end noise (noise from the Gm-stage, input resistor and R_{DAC}). In other words, whenever the input resistor is scaled in Fig. 4.14, the Gm-C integrator is simultaneously scaled in a manner that keeps the total front-end noise constant. From Fig. 4.14, it is evident that the optimum is quite shallow. For this design, we choose the input resistance to be 2 kΩ, as highlighted in Fig. 4.14. This results in R_{DAC} unit element resistance of 62 kΩ. Choosing a higher value of input resistance would in turn result in a larger value for the R_{DAC} unit element resistance. Assuming the same resistor segment width, this would then translate to a physically larger R_{DAC} unit element size, thus resulting in greater R_{DAC} area. More importantly, a bulkier R_{DAC} unit element would also suffer from increased distributed para-

sitic capacitance, resulting in slower DAC rise/fall transitions.

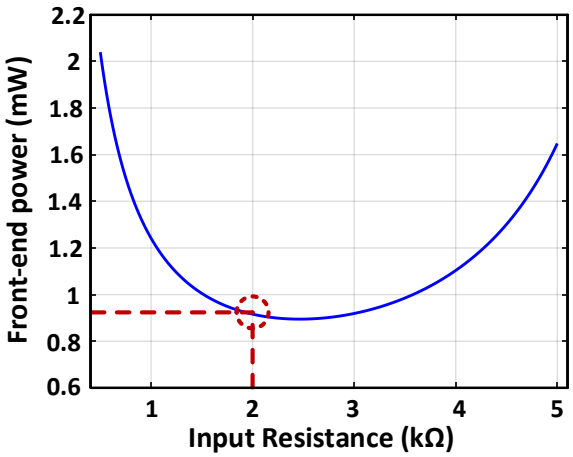

Figure 4.14: Front-end power vs input resistance for a constant front-end noise

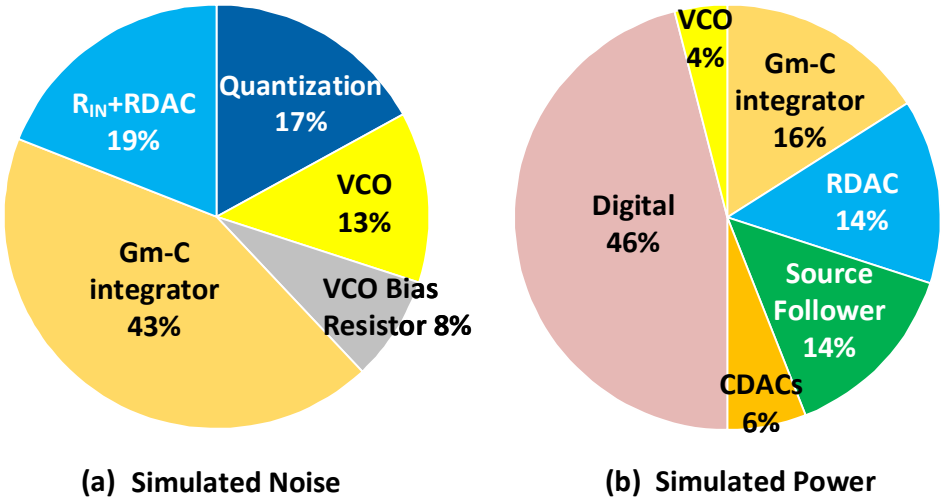

Figure 4.15: (a) Simulated noise breakdown (b) Simulated power breakdown

Fig. 4.15(a) shows the simulated noise breakdown for our design. In Fig. 4.15(a), the in-band noise has been integrated from 1 kHz to 10 MHz.

Resistive degeneration in the Gm-stage increases the Gm-C integrator's input-referred noise. However, we can compensate for this by lowering the resistance of the input resistor and resistor DAC, and allocating more noise to the Gm-C integrator. Such an approach would be infeasible for an OTA based active RC integrator because lowering an active RC integrator's input resistance demands more current to be sourced by the OTA, thereby degrading the OTA's linearity. However, since the linearity of our Gm-C integrator is not constrained by the modulator's input resistance, we can lower the input and DAC resistance, thus allocating more noise budget to the Gm-C integrator. As confirmed by Fig. 4.15(a), the Gm-C integrator contributes more than twice the noise of the input and DAC resistance combined.

The noise spectral density contributed by both source followers, referred to the modulator's input ($S_{buf,in}$) is given by

$$S_{buf,in} = 2S_{buf}(\frac{C_F}{C_T})^2|H_{VCO}(s)|^2 \tag{4.11}$$

where S_{buf} is the noise spectral density of each source follower referred to its own input and C_T is the total capacitance at the VCO's input. H_{VCO}(s) is the transfer function by which the VCO's noise is suppressed when referred to the modulator's input and exhibits first order high pass shaping within the signal bandwidth. As revealed by Eq. (4.11), the capacitive attenuation by $(C_F/C_T)^2$ further reduces the source followers' noise contribution as compared to the VCO. As such, the source followers contribute a negligible fraction of the total in-band noise and hence their contribution is not explicitly depicted in Fig.

4.15(a). Fig. 4.15(b) illustrates the simulated power breakdown. The Gm-C integrator consumes 16%, the resistor DAC consumes 14%, the two source followers together consume 14%, the two capacitor DACs together consume 6% and the VCO consumes 4% of the total simulated power. The remaining 46% is contributed by digital circuits. The measured power breakdown will be shown in Section 4.4.

4.3.4 Mismatch in Resistor DAC

As already mentioned, the R_{DAC} possesses intrinsic CLA and hence its mismatch errors are up-modulated to even multiples of the VCO's center frequency. The nominal value of the VCO's center frequency has been chosen to be 190 MHz in our design. To evaluate the efficacy of the intrinsic CLA, behavioral simulations are run with 1σ R_{DAC} mismatch ranging from 0.1% to 0.5%. Fig. 4.16(a) shows the worst-case SQNR (across 100 runs) as a function of 1σ R_{DAC} mismatch. Fig. 4.16(a) reveals that even when 1σ R_{DAC} mismatch is as large as 0.5%, the worst-case SQNR (across 100 runs) is still better than 80 dB (the ideal SQNR being 87 dB).

As already explained in the previous section, our modulator's input resistance has been chosen to be 2 kΩ since this value minimizes the modulator's front-end power for the target front-end noise. Choosing 2 kΩ for the input resistance yields a unit DAC resistance of 62 kΩ. Since 62 kΩ is a relatively large resistance, to limit R_{DAC} area, each R_{DAC} unit element is implemented as a single segment with minimum segment width (0.4 μm). This yields (41

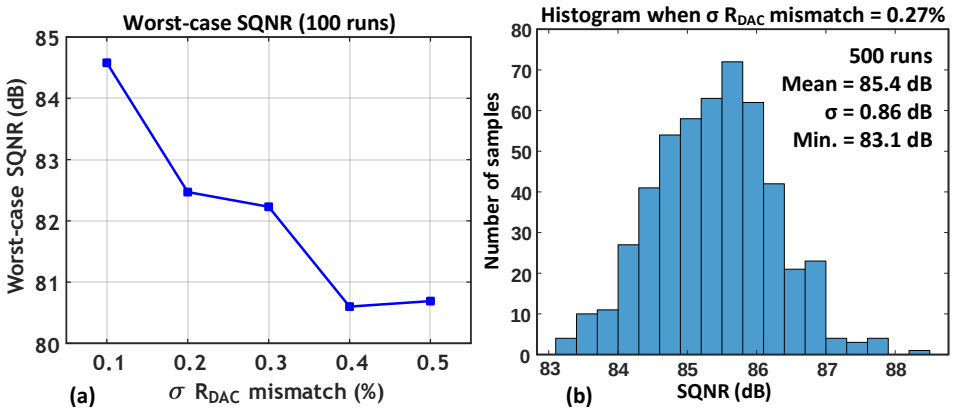

Figure 4.16: (a) Worst-case SQNR (across 100 runs) vs 1σ R_{DAC} mismatch (b) Histogram of SQNR when 1σ R_{DAC} mismatch = 0.27 % (which is the case for our design)

μm x 0.4 μm) as the dimensions of a single 62 kΩ resistor. With these dimensions of R_{DAC} unit element, Monte Carlo simulations indicate that the 1σ R_{DAC} unit element mismatch is 0.27%. After including 0.27% 1σ R_{DAC} unit element mismatch in our modulator's behavioral model, simulations show that the mean SQNR and worst-case SQNR across 500 simulation runs are 85.4 dB and 83.1 dB respectively. Fig. 4.16(b) shows the histogram of SQNR with 0.27% 1σ R_{DAC} unit element mismatch.

4.4 Measurement Results

The prototype ADC has been fabricated in 40 nm CMOS and occupies a core area of 0.064 mm^2. Fig. 4.17 shows the die photo of the fabricated chip. The differential full-scale voltage is 2.2 V. With a 1 MHz input signal, the measured peak SNDR, peak SNR and DR are 71.8 dB, 72.9 dB and 74.5

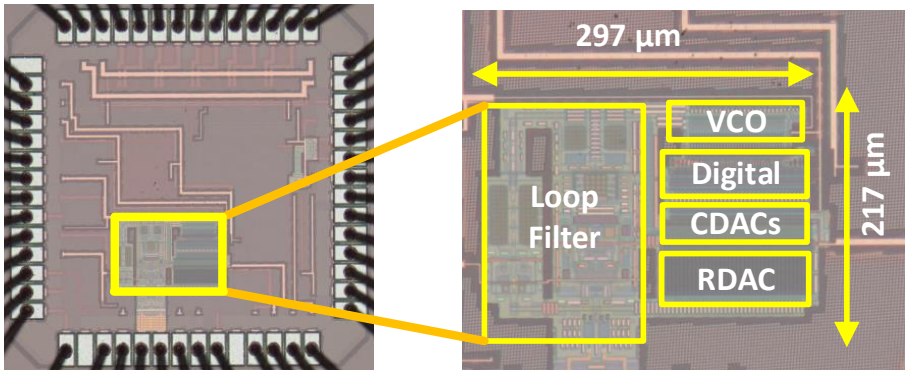

Figure 4.17: Die photo of fabricated chip

dB respectively in 10 MHz bandwidth at 655 MS/s. Fig. 4.18 shows the 65,536-point measured spectrum with a 1 MHz, -3 dBFS input signal wherein the measured SFDR is -86.6 dBc. Fig. 4.19 shows the two-tone measurement result with two input tones at 3 and 4 MHz, each of -8.5 dBFS amplitude. The measured IMD2 are -89.5/-80.9 dBc at 1 MHz/7 MHz, and measured IMD3 are -87.4/-82.1 dBc at 2 MHz/5 MHz.

Fig. 4.20 plots the measured SNDR and SNR vs input amplitude with a 1 MHz input. Fig. 4.20 shows that the peak SNDR is obtained at -3.1 dBFS input amplitude. Fig. 4.21(a) plots the measured SFDR and SNDR vs input frequency (input frequency ranging from 500 kHz to 4 MHz) with the input signal amplitude fixed at -3.1 dBFS. Fig. 4.21(a) shows that the measured SFDR is always better than -82 dBc across different input frequencies, with the peak SFDR being -90 dBc (for a 500 kHz input). Moreover, the measured SNDR varies by only 0.7 dB (from 71.9 dB to 71.2 dB) across different input

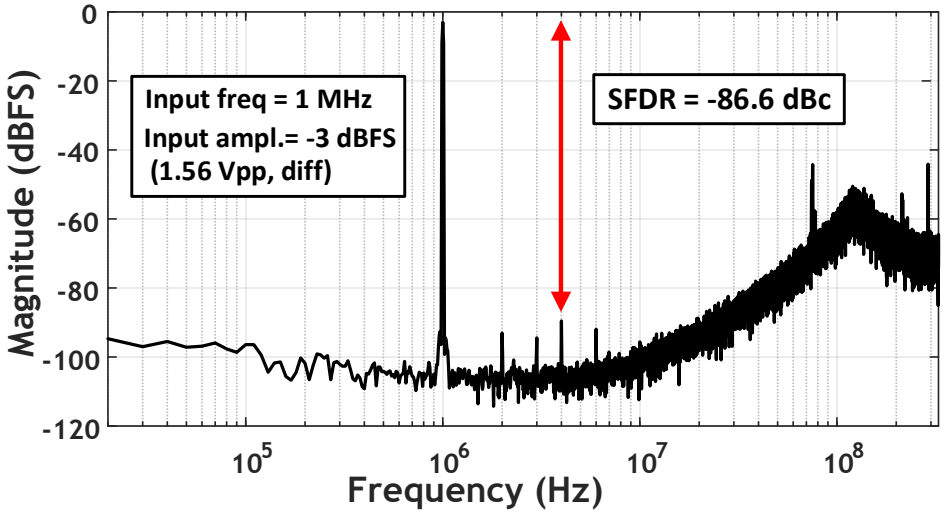

Figure 4.18: Measured 65,536-point spectrum with a 1 MHz, -3 dBFS input signal

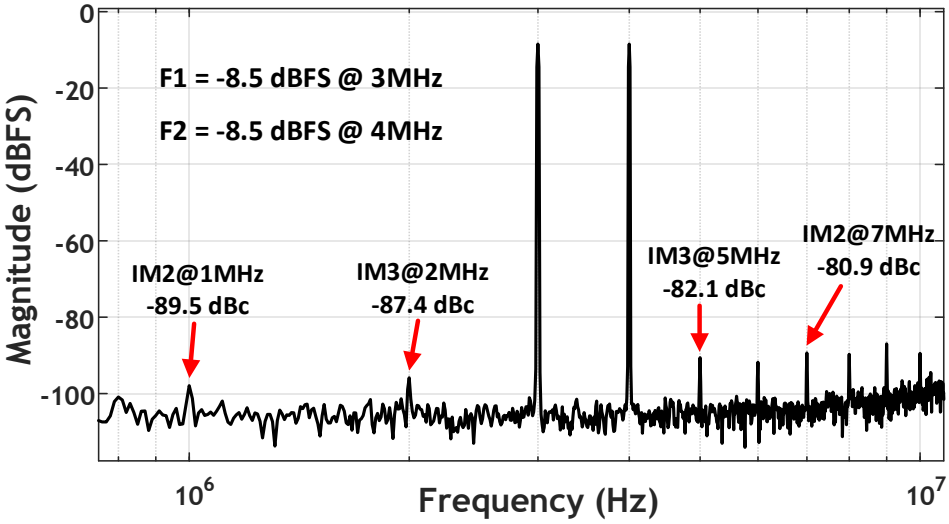

Figure 4.19: Two-tone measurement with input tones at 3 MHz and 4 MHz, each having -8.5 dBFS amplitude

frequencies, thus confirming that our fabricated ADC's in-band performance is limited by thermal noise. Fig. 4.21(b) shows the measured power breakdown with a 1 MHz input. The Gm-C integrator and voltage buffer consume 0.98 mW, the R_{DAC} and C_{DAC}s together consume 0.44 mW, the VCO consumes 0.19 mW and digital circuits consume 1.29 mW, resulting in a total power consumption of 2.9 mW.

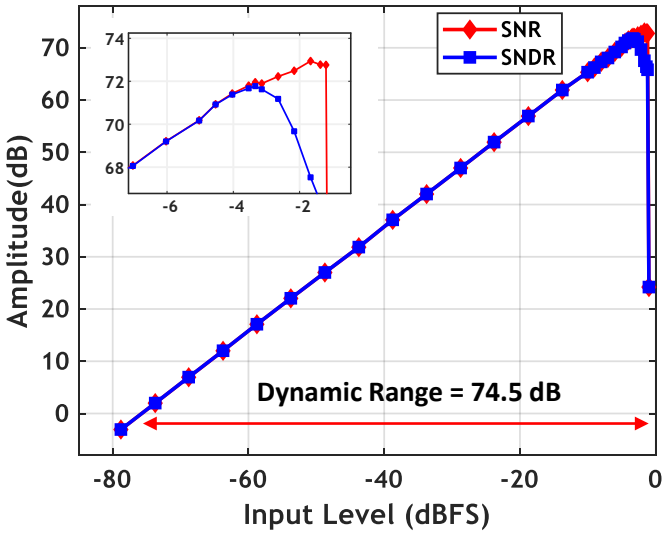

Figure 4.20: Measured SNDR/SNR vs input amplitude with a 1 MHz input

Despite not using any DAC calibration or explicit DEM circuits, the prototype ADC can achieve SNDR-based Walden FoM of 45.6 fJ/step, SNDR-based Shreier FoM of 167.2 dB and DR-based Shreier FoM of 169.9 dB, with a 1 MHz input signal. Table 4.1 compares the performance of the prototype chip with state-of-the-art CTDSMs. Table 4.1 confirms that the measured performance of our proposed CTDSM is competitive not only among VCO-based

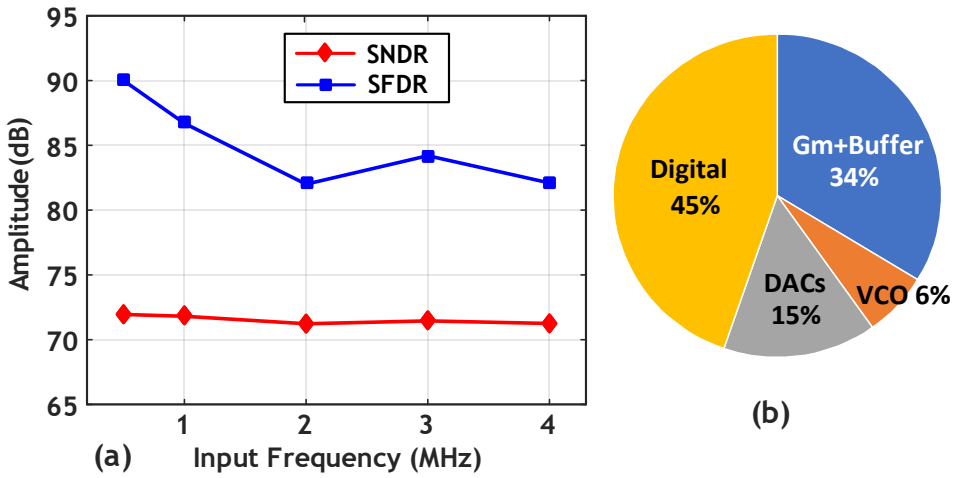

Figure 4.21: (a) Measured SNDR and SFDR vs input signal frequency, with -3.1 dBFS input amplitude (b) Measured power breakdown

ADCs but also among conventional CTDSMs having bandwidth of 10 MHz or higher. Since nearly half of the total measured power is consumed by digital circuits, our design's power efficiency can be improved even further if implemented in a more advanced process. Our proposed CTDSM is constructed using open-loop building-blocks, namely Gm-C integrator, source follower and VCO, which, together with a passive (capacitive) summing stage, results in an inherently power-efficient CTDSM architecture suitable for wideband applications in scaled CMOS processes.

Table 4.1: Performance comparison for proposed 2nd order VCO-based ADC

	This Work	JSSC 2017 Babaie	JSSC 2015 Xing	VLSI 2015 Reddy	VLSI 2017 Jang	VLSI 2015 Kao	ISSCC 2016 Wu	JSSC 2014 Zeller
Quantizer Type	**VCO based**	VCO based			SAR based	–	SAR based	1.5bit quant.
DEM/DAC Calibration Free?	**Yes**	Yes	Yes	No	No	–	No	Yes
Front-end Integrator	**Gm-C**	VCO	VCO	Active RC	Active RC	Active RC	Active RC	Active RC
Noise Shaping Order	**2nd**	3rd	1st	4th	4th	4th	6th	3rd
Tech.(nm)	**40**	65	40	65	28	16	65	65
Area (mm^2)	**0.064**	0.01	0.017	0.5	0.1	0.115	0.16	0.039
Fs (MHz)	**655**	1600	1600	1200	320	832	900	650
BW (MHz)	**10**	10	40	50	10	19	45	10
SNR (dB)	**72.9**	66.2	60.7	71.7	–	–	78.5	69.3
SNDR (dB)	**71.8**	65.7	59.5	71.5	74.4	71.6	75.3	68.6
DR (dB)	**74.5**	71	–	72	80.8	78.5	82.5	71.2
Supply (V)	**1.1/ 1.2**	1/ 1.2	0.9	–	1.1/ 1.2	–	–	1.1
Power (mW)	**2.9**	3.7	2.57	54	4.2	6.2	24.7	1.82
FoM_W*(fJ)	**45.6**	117	42	176	49.3	52.5	57.7	41.4
FoM_S**(dB)	**167.2**	160	161.4	161.2	168.1	166.5	167.9	166

*$FoM_W = Power/(2BW2^{ENOB})$, $ENOB = (SNDR - 1.76)/6.02$
**$FoM_S = SNDR + 10log_{10}(BW/Power)$

Chapter 5

Conclusion

This dissertation has discussed low power and scaling friendly design techniques for CTDSMs with high sampling rates. Traditional implementations of CTDSMs typically use OTA-based active RC integrators in the loop filter due to the excellent linearity of active RC integrators. However, since the power of the active RC integrator is directly proportional to the CTDSM's sampling rate, the OTA power typically becomes the energy bottleneck for CTDSMs with high sampling rates. This dissertation has discussed techniques to replace the CTDSM's power-hungry OTA-based active RC integrator with more energy-efficient, open-loop integrators such as passive integrators, Gm-C integrators and VCO-based (phase domain) integrators. When using such open-loop integrators, additional challenges and constraints arise. This dissertation proposed solutions to address these challenges. The efficacy of our proposed techniques has been supported by silicon measurement results of three different CTDSM designs which have been fabricated in 40 nm CMOS.

The initial segment of this dissertation was dedicated to the design of low power single-bit quantizer based CTDSMs. Chapter 2 discussed the design of a 3rd order single-bit quantizer based CTDSM with a hybrid active-

passive loop filter and FIR feedback DAC for jitter suppression. A front-end continuous time passive filter heavily suppressed the out-of-band quantization noise, thereby permitting the subsequent active integrator to be implemented as a power-efficient Gm-C integrator. By deliberately ensuring a small voltage swing at the quantizer's input, a large effective gain was obtained from the single-bit quantizer. This large quantizer gain helped to compensate for the passive filter's low DC gain. Since most of the DC loop gain was obtained from the 1-bit quantizer, our design was inherently scaling friendly. The prototype CTDSM was fabricated in 40 nm CMOS and achieved SNDR, SNR and DR of 65.6 dB, 66.7 dB and 67.3 dB respectively in a 5 MHz bandwidth at a sampling rate of 1 GS/s.

The second section of this dissertation switched gear to exploring low-power design techniques for high sampling rate CTDSMs with multibit time domain (phase domain) quantizers. A VCO is capable of acting both as a voltage-to-phase integrator with infinite DC gain as well as a multibit phase domain quantizer. The most common implementation of a VCO based quantizer employs a transconductor (Gm) stage driving a current controlled oscillator (CCO). However, when using such Gm-CCO based quantizers in closed loop CTDSMs with GHz sampling rates, a major challenge is the VCO's voltage-to-frequency (V-F) parasitic pole which causes excess loop delay and degrades loop stability. To address this challenge, Chapter 3 introduced a high speed capacitive-input VCO-based CTDSM using a novel fully differential 'distributed-input' VCO topology that is inherently devoid of a V-F para-

sitic pole. The proposed CTDSM used capacitive input and capacitor DAC to ensure that the VCO's input gate capacitance does not cause any additional pole in the loop filter. The prototype first order VCO based CTDSM was fabricated in 40 nm CMOS and occupied a core area of 0.02 mm^2 while achieving 63.1 dB DR in 480 kHz to 20.48 MHz bandwidth at 1 GS/s. This was the first work to mitigate the parasitic pole in a fully differential VCO, without relying on any additional active circuits. To our best knowledge, this was also the first work to demonstrate capacitive input in a high speed CTDSM, without using chopping.

Despite its merits, the modulator of Chapter 3 possessed some limitations. Firstly, it could only provide first order quantization noise shaping. Secondly, due to capacitive input, it could not digitize signals near DC. To address these limitations, Chapter 4 discussed the design of a second order VCO-based CTDSM which used the distributed-input VCO (introduced in Chapter 3) as the second stage (back-end) integrator and quantizer. Due to the more aggressive noise shaping, this modulator's in-band performance was dominated by thermal noise, thereby resulting in a significantly better measured power efficiency (as compared to the modulator of Chapter 3). Since this proposed second order modulator had resistive input, it could digitize signals from near DC. The high resolution of the VCO quantizer relaxed the linearity of the front-end Gm-C integrator. A capacitive-π network helped to indefinitely impedance scale up the front-end Gm-C integrator for thermal noise without simultaneously requiring the inner capacitor DAC and feedforward

capacitor to be scaled up. Consequently, even with a large load capacitance for the Gm-C integrator, we still could use very small unit capacitors in the inner capacitor DAC, resulting in significant power savings. The prototype chip was fabricated in 40 nm CMOS and achieved SNDR, SNR and DR of 71.8 dB, 72.9 dB and 74.5 dB respectively in a 10 MHz bandwidth at 655 MS/s, yielding an SNDR-based Walden FoM of 45.6 fJ/step.

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Vita

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