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Device and process development of SiC lateral power devices

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Device and process development of SiC lateral power devices

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Dedication

Dedicated to the reader

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Abstract

Device and process development of SiC lateral power devices

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RESURF (Reduced Surface Field) technology is one of the most widely used methods used for designing lateral high-voltage, low on-resistance devices for Si power integrated circuits. However, these Si devices operate in a range of few volts to a few hundred volts in reverse blocking voltage. Silicon carbide (SiC) possesses a high breakdown field of 4×10^6 V/cm, high saturated electron drift velocity of 2×10^7 cm/s and excellent thermal conductivity of 4.9 W/cm · K, attributing from its wide bandgap. This makes it an ideal choice for future SiC power integrated circuits, e.g. integrated gate driver circuits for ultra-high voltage SiC discrete devices, which can operate in higher voltage class.

In this research study, the concept of RESURF, which utilizes 2-dimensional depletion (vertical and lateral junction direction), is demonstrated with 4H-SiC material to achieve high blocking capability. The RESURF structure consists of a lateral P^+/N^- epitaxial junction component and a vertical P^-substrate/N^- epitaxial junction component. One of the key features in this concept is the electric field distribution at the surface of the RESURF device will display a parabolic shape with peaks at both lateral and vertical junction ends after full depletion. As a result, the lateral electric field at the lateral P+/N^- epitaxial junction is greatly reduced compared to the one-dimensional diode, and device blocking capability is significantly increased.

The objective of this research is to both design and fabricate 600V Lateral RESURF Schottky diodes and MESFETs using a silicon carbide wide-bandgap semiconductor material.

Numerical simulation was performed using Sentaurus Device TCAD Simulator by Synopsys to both verify and optimize the performance of these two devices. The SiC wafer with multiple epi layers, encompassing different polarities, has been specifically designed for optimal performance of these lateral devices. Critical process technology, such as ohmic contacts with low specific contact resistance (ρ_c), N^+ ion implant process with effective activation procedure, and sloped field plate structure with low leakage current, was developed. The fabricated devices have shown improved trade-off between specific on-resistance and blocking capability over conventional vertical SiC devices.

Some of the notable contribution in establishment of fabrication process flow and critical process development are development of alternative cap layer other than carbonized photoresist for SiC activation, by encapsulating both front and backside of sample with 1um SiO_2 layer. The activation process at 1500℃, 30min shows sufficient implanted phosphorus to be activated for low sheet resistance necessary for quality ohmic contact. The experimentally evaluated TLM measurements show specific contact resistance ρ_C as low as $1.746 \times 10^{-6}\ \Omega \cdot cm^2$ using original ohmic metal stacks recipe of Ti/Ni/Ti/Au=20nm/90nm/6nm/120nm annealed at 1050℃ for 2 min in N_2 ambient with 200nm-box profile phosphorous implant. Also, we have developed, and applied contact open etch process utilizing multiple wet and dry etch techniques to form a 30°degree angle sloped field plate structure to further ensure electric field distribution uniformity at the contact edges. This sloped field plate structure is effective in mitigating high electric field crowding at electrode edges for all lateral SiC devices to be fabricated in the future.

Two lateral devices, lateral RESURF 4H-SiC Schottky barrier diodes and MESFETs were successfully developed and fabricated, and the best performing diode shows specific on-resistance of 10.226 $m\Omega \cdot cm^2$ with breakdown voltage of 575V. The MESFET achieved the best forward performance at V_{GS}=0.6V with specific on-resistance of 5.699$m\Omega \cdot cm^2$ (Drain-Gate only) and 35.621$m\Omega \cdot cm^2$ (Drain-Source, the whole device area). This device achieved a breakdown voltage of 525V at V_{GS}=-3.2V.

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Chapter 1. Introduction

1.1 Background

Majority of integrated circuits and power devices that semiconductor industries offer today for applications such as advanced computers, consumer electronics, communication networks, and industrial and military systems have been almost exclusively based on silicon (Si) technology. These trends are changing as the requirements of future electronics demands more emphasis on greater power density and energy efficiency, which can only be achieved by the development of new devices designed with new semiconductor materials. It is now widely believed that silicon technology is coming to its fundamental physical limits and there are urgent needs to come up with new design protocols and innovative packaging techniques to utilize the full potential of these new wide-bandgap semiconductor materials. These new materials will not only enable meeting devices' electrical requirements such as voltage, current, and power rating, but also further advance operational environment of the power systems in scenes where radiation, extreme temperature exposure, wide-range of thermal cycling are present; That is basically where conventional silicon-based systems are incapable of surviving or efficient operation.

1.2 Material advantage of 4H-SiC for power semiconductor device

In general, efficiency of power conversion and conditioning is mainly limited by the performance of power semiconductor devices used as switches in these applications. During the past years, silicon (Si) has been the most widely used material in these fields because of its abundance, and the ease to manufacture large high-quality single crystals that could be processed to form large diameter wafers. Although the performance of Si power devices has significantly improved over the years through the development of innovative devices such as vertical power metal oxide semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs), its material properties are now facing physical limitations, especially for high voltage (>600 V) applications where the device internal electric field exceeds the order of ~MV/cm. The need for faster devices with high voltage and high switching frequency capability is growing, and emerging novel power semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN) are highly expected to replace existing Si power semiconductor devices.

Silicon carbide (SiC) is a wide-bandgap semiconductor with superior physical and electrical properties than those of Si, which can be the next fundamental building block material for high voltage, low power loss semiconductor device for future power electronics applications. The large bandgap of 4H-SiC (roughly three times larger than that of Si) enables device operation at increased temperatures and low-leakage currents compared to Si devices. SiC can also withstand high electric fields, ten times greater than Si, and at a much higher current density before it can break down. The large electrons saturation drift velocity enables SiC to generate high power at high frequencies. Moreover, SiC has excellent thermal conductivity, which makes it suitable for high-power operation when multiple dies are packaged into a single module. Its strong chemical and thermal stability have notable advantages for devices intended to operate under severe conditions or harsh environments, such as applications in aerospace or automotive industries. Also SiC is the only compound semiconductor where insulating material, SiO_2, can be grown through thermal oxidation like Si which makes it possible to fabricate MOS-based (metal-oxide-semiconductor) electronics in SiC [1].

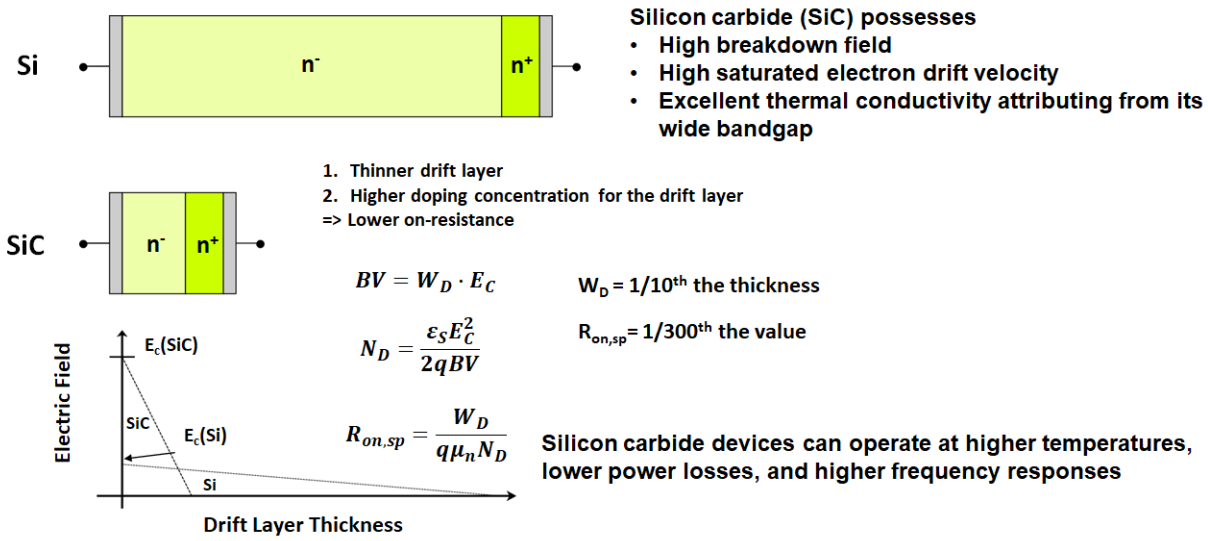


Fig. 1.1 Explanation of advantage of SiC over Si material through comparison of Schottky barrier diode structures

1.3 Replacing Si-IGBTs to SiC MOSFETs for Three Phase Inverter Applications

Currently, SiC-MOSFETs are regarded to provide benefits from voltages of 600 V and higher, and strongly preferred in 1 kV and higher applications. Si-IGBTs have been the mainstream device structure in these voltage classes where the device design uses minority carriers for conductivity modulation to supplement high on-resistance coming from the thick epitaxial layer. SiC-MOSFETs offer significantly reduced turn-off losses compared with IGBTs, and a smaller-size setup can be realized from the reduced component size from higher frequency operation. Compared with Si SJ-MOSFETs (super-junction MOSFETs) with comparable rated voltage, ON-resistance values are even lower, and so reduced chip areas and greatly reduced recovery losses are possible from the same ON-resistance.

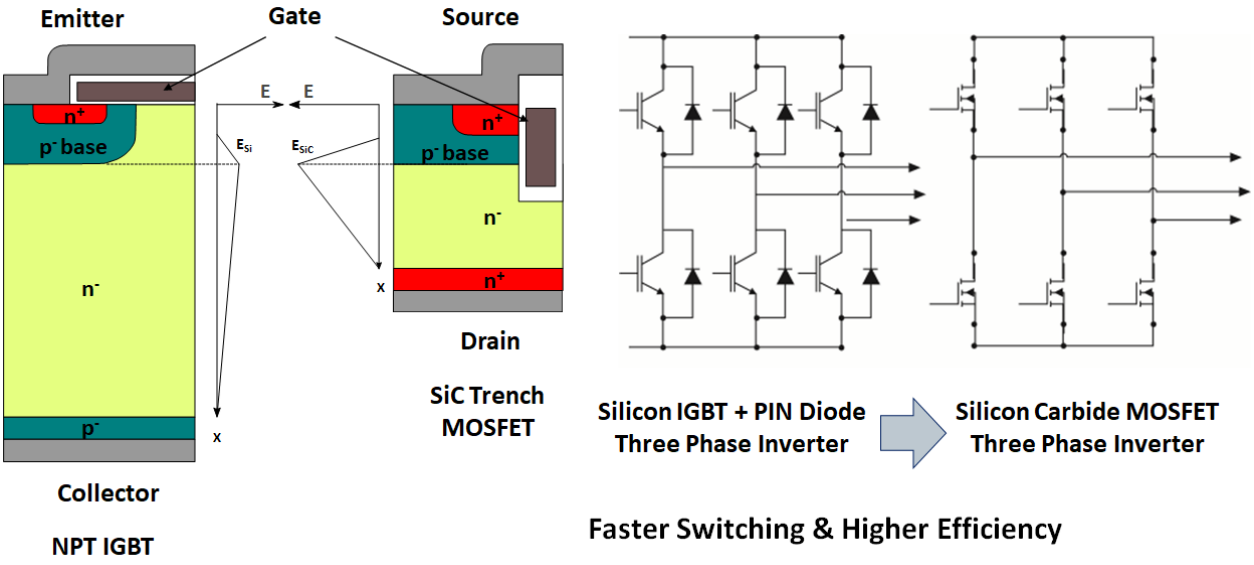


Fig. 1.2 Replacing conventional silicon IGBT devices to all-SiC power devices

1.4 Monolithic power IC technology basics and challenges

Power semiconductor device are traditionally designed to handle large current and power vertically using the whole chip area for conduction and available only as discrete package. A higher breakdown voltage in vertical devices usually requires a thicker and lower doping concentration epitaxial layer. On the other hand, much of the power electronics applications now require compact and cost-effective power management design where lateral integrated one-chip solutions are becoming the mainstream. Power devices can be developed laterally where all terminals are on the surface and the current flows laterally at the surface of thin epitaxial layer. Unit cells of individually designed power devices (Lateral MOSFETs & diodes) can be placed side by side on the chip and can be simply connected in parallel. This is a common method to achieve a high current conduction capability and is especially used for high current lateral power devices. Additionally, there are also techniques that allow the use of vertical structures in planar environments. The vertical current is commonly collected by a highly doped buried layer. These collected carriers are transported to the top surface using sinker structures

Packaging of the SiC power device is also a pressing problem. Packaging reliability will be a key factor affecting the performance of the circuits once the material and process-related challenges are overcome. Packaging reliability is also important when devices operate at high temperatures (≥ 200°C). It is important to increase the power handling capability through innovative package design to reduce cooling cost. Thus, new package materials for high temperature application are necessary.

2 Review of Lateral power device

2.1 LDMOSFETs (Laterally-Diffused Metal-Oxide Semiconductor Field Effect Transistors)

2.1.1 Si LDMOS

LDMOS is one of the primary devices used in power ICs. For Si LDMOS, the channel region is created by the difference of diffusion length of p-type body and n-type source, much like a vertical double-diffused MOS (VDMOS). A well-designed LDMOS will have high breakdown voltage, low on-resistance, and a small gate to drain capacitance which could be easily integrated to each other.

2.1.2 State of the art Si LDMOS on silicon-on-insulator wafer (SOI-LDMOSFET)

Si LDMOS can be designed and fabricated on not just bulk silicon but on silicon-on-insulator (SOI) wafers as well. This is a favorable solution to incorporate in terms of reducing leakage currents and isolation separation between devices, which can greatly improve high temperature performance. The buried oxide layer in the SOI wafer helps support high electric field during reverse blocking state which results in a higher breakdown voltage of the device. One of the drawbacks of using SOI wafers is that the device's operation is limited by self-heating effects during switching and short circuit faults. Because the buried oxide underneath the device is a good thermal insulator, the temperature rise inside SOI power devices can be much higher than that of bulk silicon devices. To overcome this thermal disadvantages, researchers have employed partial SOI (PSOI) technology, which can still increase breakdown voltage and reduce self-heating effects due to its Si window as shown in the bottom Figure 2.1. Inversion charges located in the trenches also enhance the electric field of the buried layer during blocking state, modulating the electric field in the drift region for higher breakdown voltage.

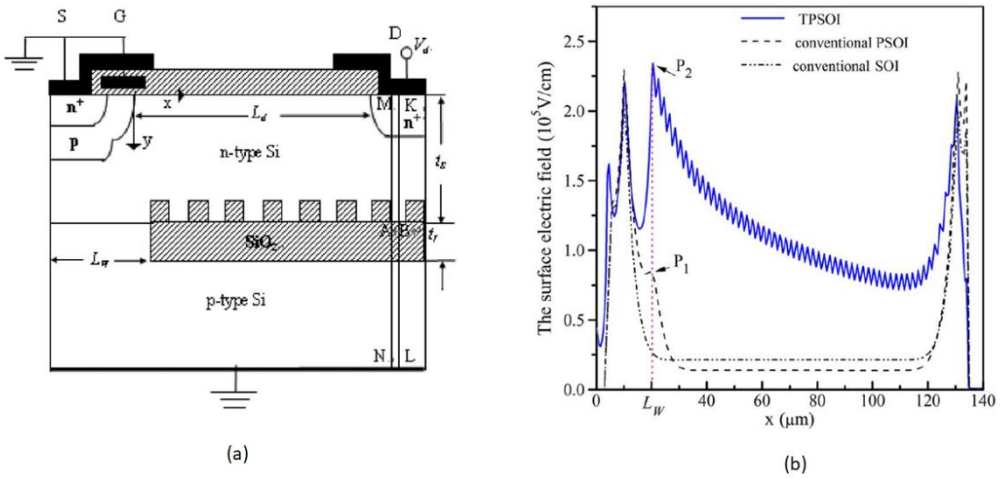


Fig. 2.1 Cross-section of partial SOI-LDMOSFET with charge trenches (a) and surface electric field simulation comparison (b)[2]

2.2 Silicon Carbide lateral MOSFETs

Lateral SiC DMOSFETs were first fabricated in 1998 with a breakdown voltage of 2.6 kV [3] as shown in Figure 2.2. The concept of this structure was to construct a lateral MOSFET on a semi-insulating SiC substrate. In this structure, when drain bias is applied while the gate is closed, the depletion region around the p-well will first deplete the n-type epi layer underneath to the semi-insulating substrate, then move laterally toward the drain. Therefore, the lateral extent of the depletion region is not limited by the thickness of the epi layer.

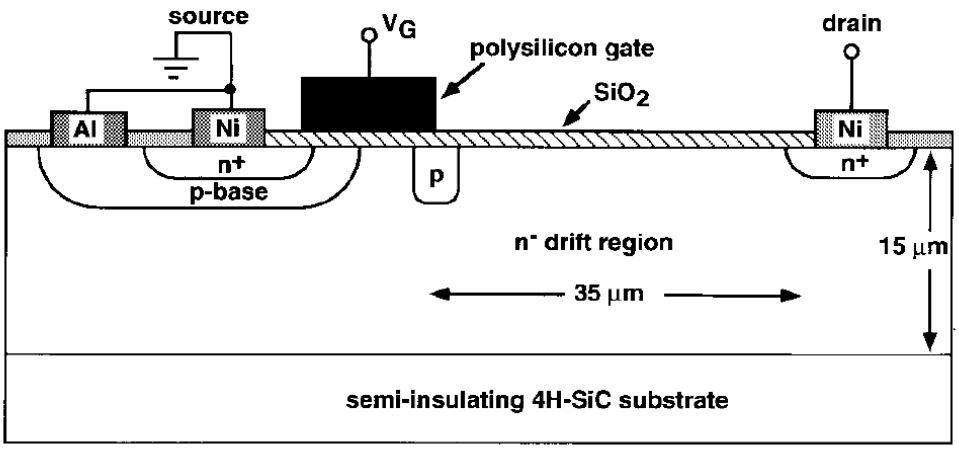


Fig.2.2 Cross-section of first fabricated 4H-SiC LDMOS power transistor

The fabricated SiC LDMOS device had a 35um drain-to-guard-ring spacing which corresponds to the drift region length, 10um channel length, and 130um channel width. The device blocked 2.6 kV and specific on-resistance of 200m$\Omega \cdot cm^2$ was recorded, which was innovative in this era when silicon carbide was still considered as new material. Since then the performance of SiC LDMOS have improved greatly through employing RESURF and double RESURF design principles. On-resistance have reduced order-of-magnitudes by higher doping concentration and shorter drift region length benefiting from the RESURF concept. Blocking capability of SiC LDMOS has also improved through implementation of high breakdown-field dielectric such as Si_3N_4 for passivation layer and improved field plate structure.

2.2.1 State of the art SiC lateral MOSFET

Table 2.1 Performance characteristics overview of SiC lateral MOSFET and diode technologies and publications

Material	Device type	Implemented key technology	Drift region thickness /Dose	Channel Mobility	Specific on-resistance	Breakdown voltage	Year published	Ref.
4H-SiC	Lateral MOSFET	RESURF through ion implantation	0.5um/ 2×10^{13} cm^{-2}	2cm^2/v·s	4Ω·cm^2	1200V	2000	[4]
4H-SiC	Lateral MOSFET	RESURF through ion implantation	0.5um/ 5×10^{13} cm^{-2}	14cm^2/v·s	0.5Ω·cm^2	900V	2001	[5]
4H-SiC	Lateral MOSFET	Two RESURF zones with NO annealing	0.5um/ 5×10^{13} cm^{-2}	25cm^2/v·s	170mΩ·cm^2	930V	2004	[6]
6H-SiC	Lateral MOSFET	Two RESURF zones	0.4um /4×10^{12} cm^{-2}	40cm^2/v·s	130mΩ·cm^2	1300V	2002	[7]
4H-SiC	Lateral MOSFET	Two RESURF zones	0.6um/ 2.4×10^{12} cm^{-2}	25cm^2/v·s	67mΩ·cm^2	1330V	2005	[8]
4H-SiC	Lateral MOSFET	Double-RESURF	0.5um/ 9×10^{12} cm^{-2}	17cm^2/v·s	66mΩ·cm^2	1380V	2007	[9]
4H-SiC	Lateral MOSFET	Double-RESURF	0.5um/ 8×10^{12} cm^{-2}	36cm^2/v·s	40mΩ·cm^2	1580V	2009	[10]

Material	Device type	Implemented key technology	Research type	Drift region thickness /concentration	Specific on-resistance	Breakdown voltage	Year published	Ref.
3C-SiC	Lateral Schottky diode	RESURF 3C-SiC on p-type Si substrate	TCAD simulation	4um/ 1×10^{16} cm^{-3}	4mΩ·cm^2	1200V	2014	[11]
4H-SiC	Lateral Schottky diode	RESURF Epi grown	Experimental Fabrication	0.5um/ unknown	626mΩ/mm	331V	2018	[12]
4H-SiC	Lateral PN diode	Two RESURF zones	TCAD simulation	0.5um/ 1.6×10^{16} cm^{-3} 2.6×10^{17} cm^{-3}	unknown	8000V	2012	[13]

Above Table 2.1 summarize the literature review of published SiC lateral MOSFETs/diodes and its performance characteristics. Various key technologies have been implemented to improve both forward and reverse performance, as well as channel mobility. Example of implemented key technologies are the two RESURF zones method and double-RESURF structure.

Two RESURF zones method is a technique to optimize and reduce the electric filed crowding at the drain edge and in the gate oxide by applying different dose for RESURF and lightly doped drain (LDD) regions as shown in Figure 2.3 . RESURF and lightly doped drain (LDD) regions are set 10um long and 0.6um deep and dose of 2.4×10^{12} cm^{-2} and 7.8×10^{12} cm^{-2} were used, respectively. By this

optimization, the device exhibited a high breakdown voltage of 1330 V, and an on-resistance of $67m\Omega \cdot cm^2$.

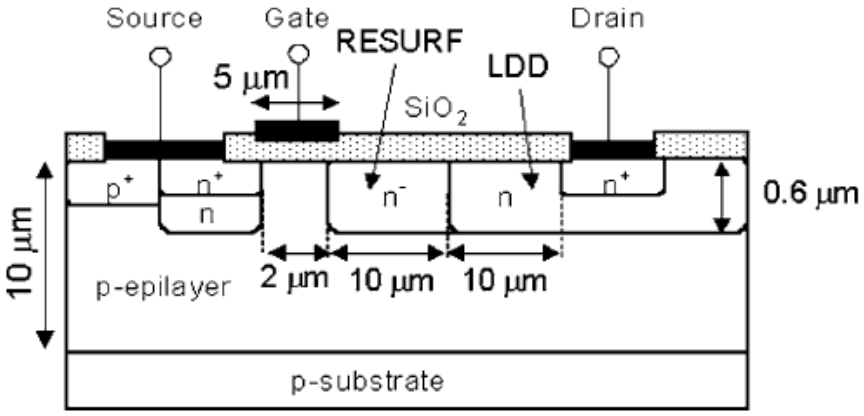


Fig.2.3 Cross-section of SiC lateral MOSFET with two RESURF zones [8]

Additional RESURF effect can be achieved by incorporating an additional layer of the opposite polarity (p+ top region) on the top of the n- drift layer. In this structure, the vertical depletion of the n- drift layer occurs from the two junctions: p- epi layer/ n- drift and p+ top layer/ n- drift. This device structure is referred to as double-RESURF structure, and because of this two-sided vertical depletion, the total integrated n- drift layer charge can be significantly increased to twice as much value compared to single-RESURF device as shown in Figure 2.4. This corresponds to lower on-resistance performance of the device.

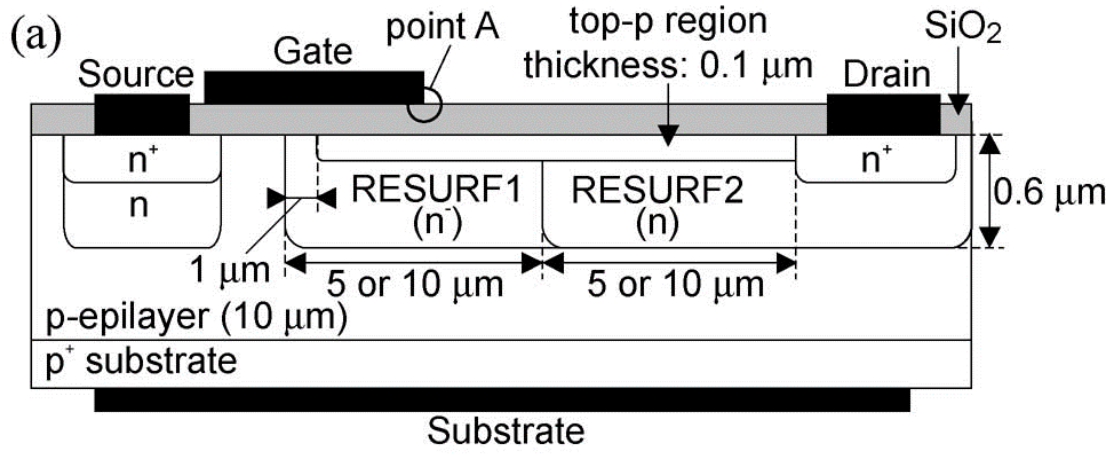


Fig.2.4 Cross-section of double-RESURF SiC lateral MOSFET [9]

2.2.2 Challenges for SiC lateral MOSFETs

There are two primary challenges associated with SiC lateral MOSFETs that need addressing. These are the low electron mobility in the inversion channel layer and gate oxide reliability with high electric field and temperature. Special gate oxidation technologies are needed to eliminate the SiC/SiO_2 interface defects and increase the mobility of the electron in the inversion layer, such as the post oxidation annealing in NO or N_2O environment. As shown in the above Table 2.1, the mobility in the channel start to improve once NO annealing was introduced around year 2004. Since SiC has a band gap of 3.3eV and critical electric field of 2.5×10^6 V/cm, internal electric field could get extremely high even during normal operation for both vertical and lateral SiC MOSFETs (Figure 2.5). Gate oxide reliability is a concern as internal electric field can reach as high as the gate oxide's critical value of 1×10^7 V/cm. Device designers have made efforts by adding P+ shield layer or making use of trench gate structure to secure additional reliability to the point of existing Si power MOSFET technology.

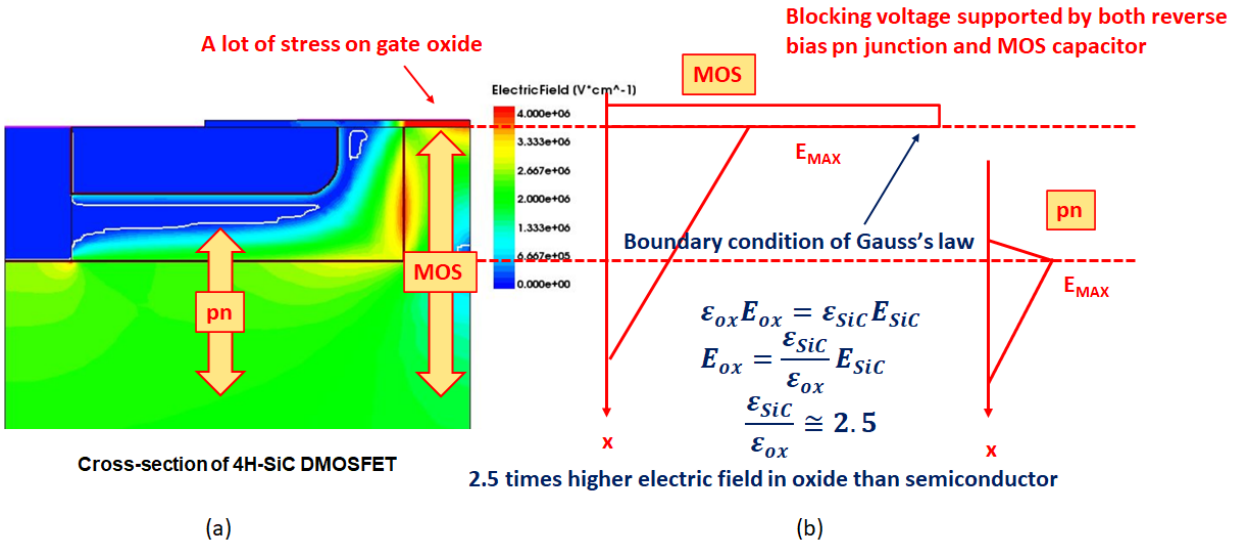


Fig.2.5 Electric field distribution inside the vertical DMOSFET cell structure (TCAD simulation) (a) and electric field diagram in vertical DMOSFET in blocking state (b)

2.3 LIGBTs (Lateral Insulated Gate Bipolar Transistors)

2.3.1 Silicon lateral IGBTs

The major limitation of Si LDMOS is their relatively high specific on-resistance when used in power switching application that require high current and voltages. Much like vertical devices, for the LDMOS to block high voltages, especially for Si material, the device requires longer drift region length for depletion which results in poor forward performance due to majority carrier conduction mechanism. Lateral IGBTSs or LIGBTs are designed to overcome these high on-state losses of LDMOS through incorporating conductivity modulation in the structure. The specific on-resistance of an LIGBT can be much lower than that of LDMOS and for the same current and voltage rating, the chip size or active area occupied in monolithic chip can be also be reduced. These are the advantages of LIGBT over LDMOS, but much like vertical IGBTs, trade-off relationship between on-resistance and turn-off time exist as well. IGBTs, either vertical or lateral structure, posses a longer turn-off time due to existence of minority carriers which are removed from the drift region through recombination. The turn-off time of LIGBT is dependent on the lifetime of the minority carriers. Therefore, LIGBT is especially effective in applications that require high current density and slow switching speed. For low current density and fast switching applications, LDMOS is the better choice.

2.2.2 State of the art Si HVIC using Si LIGBTs [14]

One of the highest power level Si HVIC chip was demonstrated using Si LIGBT by Toshiba in 1999 which is shown in Figure 2.7(a). The chip size of this one chip inverter IC is $7.1\times5.2mm^2$, which integrates six silicon lateral IGBT (LIGBT) (Figure 2.6) and diodes with a driver IC. Although this work was published in 1999, the paper demonstrates the highest power handling capability of a single chip HVIC that has been achieved using Si material. As shown in Figure 2.7 (b), each LIGBT has a unit cell dimension of 140 um which can achieve a breakdown voltage of 520V. Each device has a forward voltage drop of 3V at $175A/cm^2$, which is equivalent to specific on-resistance of 17 $mohm\cdot cm^2$. The power device rating reached is 500V/3A per switch for this three-phase inverter HVIC. The output power of this inverter is, therefore, less than 1 kW. No publications following this demonstration has been made in terms of the amount of power that a single chip Si HVIC can achieve. This is due to slow switching speed of the Si LIGBT and researchers preferring faster switching LDMOS instead. This will result in even more limitation of power handling capability of LDMOS based HVIC since current conduction capability is limited by the on-resistance and breakdown voltage trade-off relationship of Si LDMOS requiring long drift region length. On the other hand, Si LDMOS

based HVIC solution is preferred in higher switching frequency applications such as flyback converters at 80 to 100 kHz range.

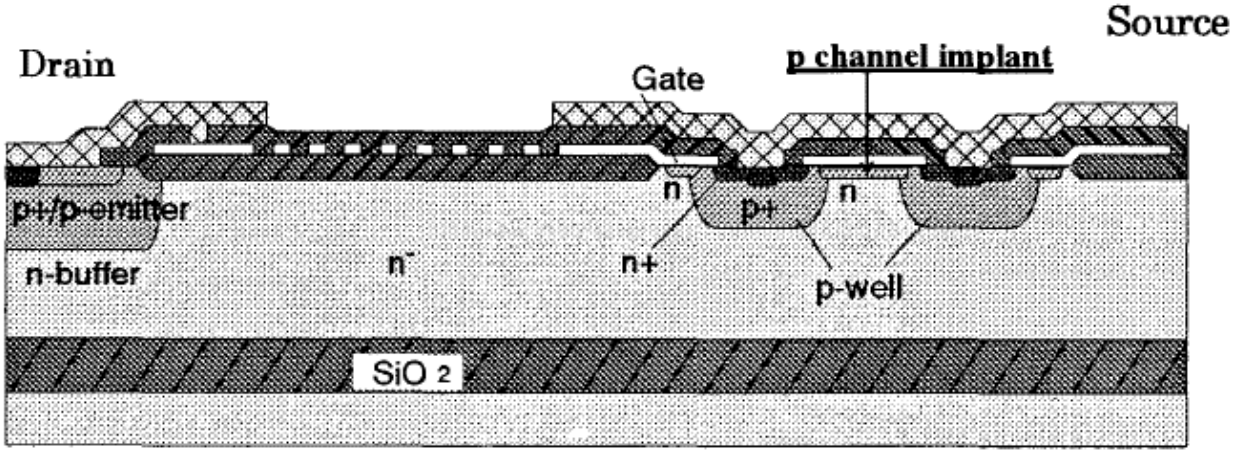


Fig.2.6 Cross-section of multi-channel lateral IGBT used in one chip inverter HVIC

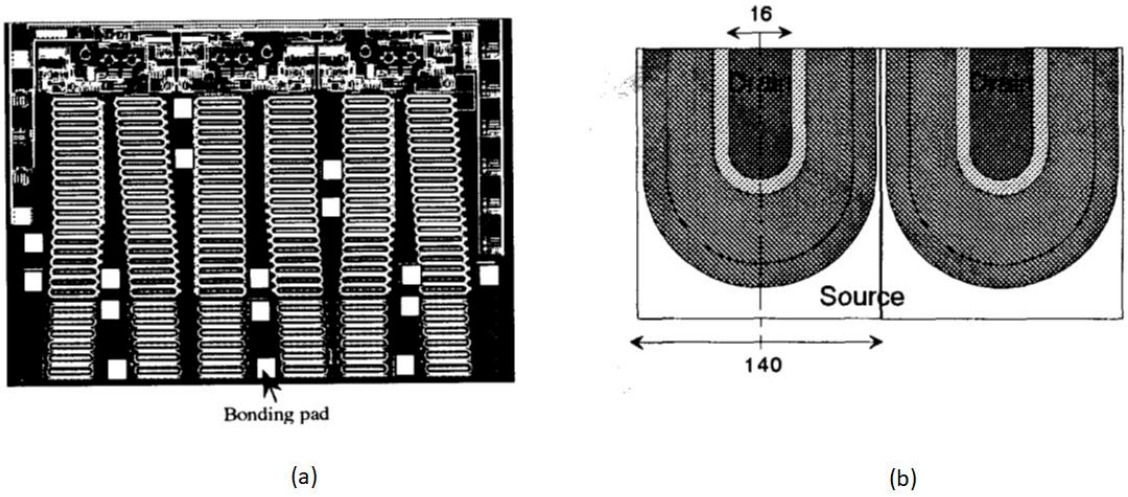


Fig.2.7 Top view of 500V 3A one chip inverter HVIC (a) and two units of LIGBT cells used in the layout (b)

2.4 Silicon carbide lateral IGBTs

There are reports on SiC vertical IGBTs but reports on SiC lateral IGBTs are limited. Vertical n- and p-channel SiC IGBTs have been successfully realized with a breakdown voltage of 12kV and a specific on-resistance of 18.6m$\Omega \cdot cm^2$. This corresponds to a forward voltage drop of 5.3V at a current density of 100A/cm^2, which is much smaller than that of a 10kV rated SiC MOSFETs. The cross-section diagram of SiC lateral IGBT is shown in Figure 2.8 [15]. The device was fabricated on a p-type epitaxial layer grown on a 4H-SiC semi-insulating wafer which serves as the p-base. A n-buffer layer was placed between the p^+ collector and the p-base to prevent punch-through.

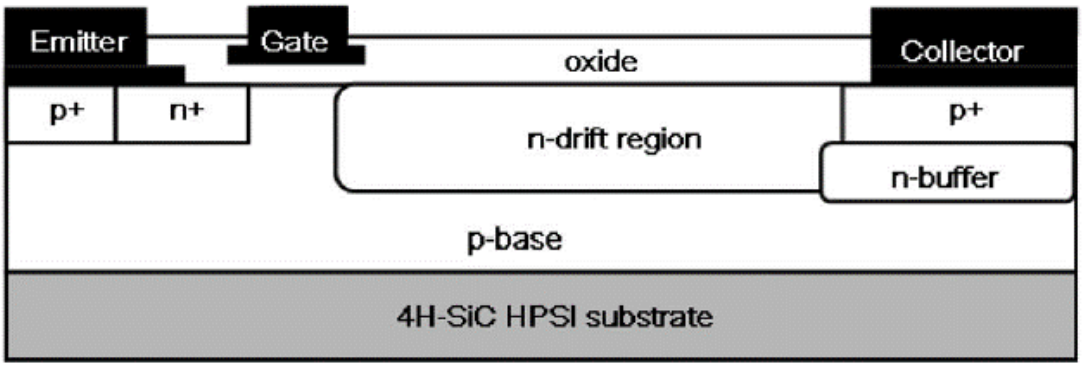


Fig. 2.8 Cross-section of a lateral 4H-SiC IGBT

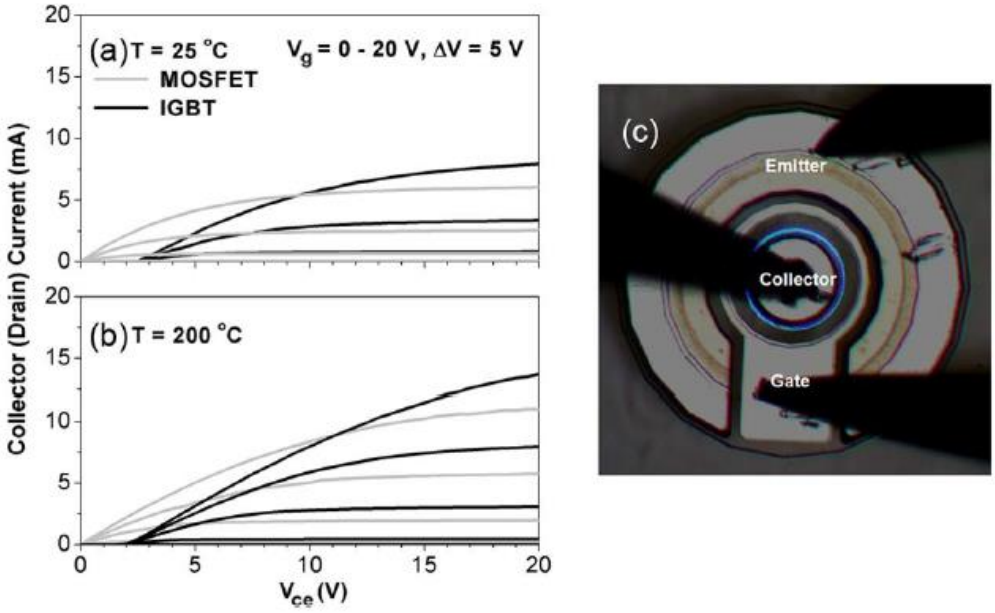


Fig.2.9 Experimental forward performance results of lateral 4H-SiC IGBT in comparison with counterpart test MOSFET fabricated simultaneously

Experimental results shown Figure 2.9 indicates that the differential on-resistance of a lateral IGBT is smaller than that of a counterpart test lateral MOSFET fabricated simultaneously, as a result of the injection of minority carriers from the p^+ collector into the drift region. The performance of lateral IGBT is further improved at 200 ℃ evaluation. Injection of minority carrier injection is further proven through the confirmation of electroluminescence when the IGBT turns on as shown in Figure 2.9 (c).

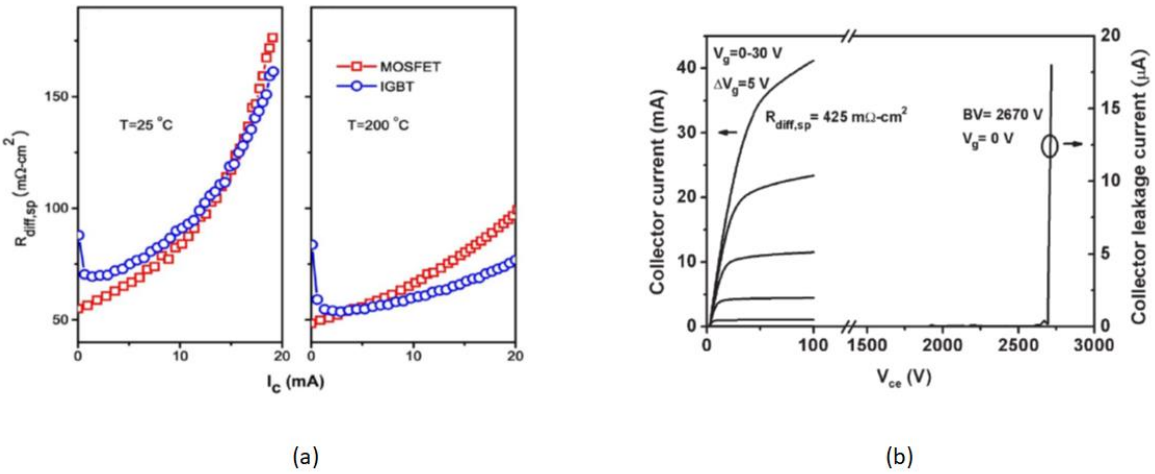


Fig.2.10 Differential on-resistance of lateral 4H-SiC IGBT in comparison with counterpart test MOSFET fabricated simultaneously at a V_g of 30 V at room temperature and 200℃ (a) and forward and reverse performance lateral IGBT with L_{ch} of 5um and an L_d of 80um

As shown in Figure 2.10 (a), at room temperature, the $R_{diff,sp}$ of LIGBT is lower than that of the MOSFET when I_c is larger than 15 mA, implying partial conductivity modulation in the drift region of LIGBT. The crossover point is reduced to 3.7 mA at 200 ◦C, which is attributed to the increase in minority carrier lifetime in the drift region, and the improved injection efficiency of holes at high temperatures for the LIGBT. Figure 2.10 (b) shows the blocking capability of the lateral 4H-SIC IGBT is high as 2670V for a device with 80um drift region length. The reported results illustrate that 4H-SiC lateral IGBTs are promising candidates for future power integrated circuit applications where further power handling capability is required above lateral SiC DMOSFETs operational range.

2.5 Silicon carbide vertical and lateral JFETs

There are different types of vertical channel SiC JFETs which have been reported through publications but the recessed gate JFET shown in Figure 2.11 is a widely known structure. This structure is especially innovative because it offers the lowest achievable on-resistance value from a SiC unipolar device. This is from the small cell pitch and its primary current conduction is dominated by the high bulk mobility of the electron compared to a MOSFET device where the mobility of the electron is referred to as the "surface mobility". Also, the device's on-resistance has a positive temperature coefficient, which is desirable when paralleling multiple devices for higher current conduction applications. In order to fully utilize this device's properties and performance, it is preferred to design it as normally-on operation. Normally-off design is also possible but, in most cases, the fabrication process window is relatively small where gate control requires accurate doping concentration and thickness decided from the built-in potential between the P^+ gate and n-channel region. The same vertical gate structure is also applied to lateral double RESURF JFETs where the planer gate structure is insufficient to close the highly doped n-drift region. The device is commonly known as normally off vertical channel lateral double RESURF JEFTs as shown in Figure 2.12.

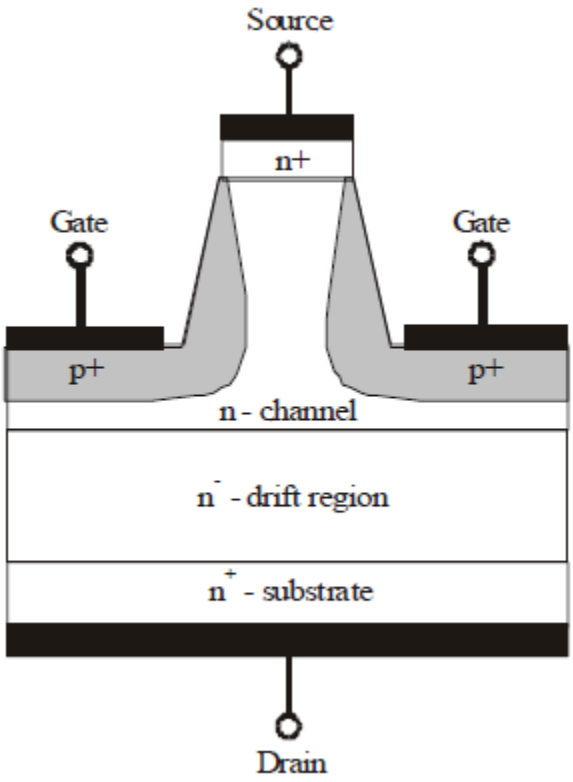


Fig. 2.11 Cross-section diagram of vertical channel recessed gate SiC JFET

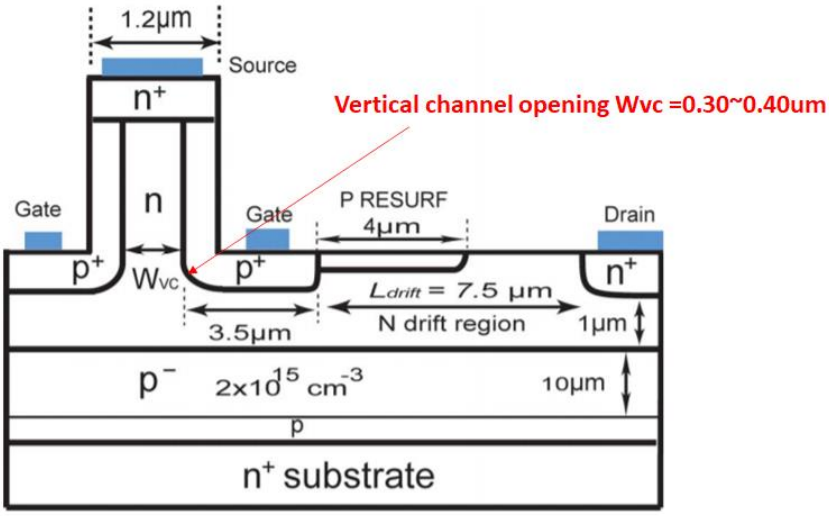


Fig. 2.12 Cross-sectional diagram of the 4H- SiC normally off VC-LJFET with RESURF structure [16]

2.6 Challenges for SiC power IC applications

One of the challenges in integrating existing lateral SiC MOSFETs and diodes in to one monolithic chip is the complexity of fabrication process flow. Much of the device reviewed utilize multiple ion implantation method in forming n- drift region on p-type epitaxial wafer. This requires precise control of the dose and implant energy to achieve the blocking voltage necessary. Same applies to the additional top-p region for double RESUF structure. One way to avoid this small process window is by preparing epitaxial grown RESURF and drift region layers. The blocking capability of lateral RESURF device is determined by the bottom p-type layer and its vertical junction breakdown. Then drift region length can be varied in order to achieve the necessary blocking voltage within this vertical breakdown value. Variation in both blocking voltage and forward current capability can be designed by varying the drift region length, and number /length of fingers in the layout. This method is effective when there are multiple lateral power device of different current/voltage ratings are necessary in a monolithic one chip solution. The following dissertation research will start out by designing the optimum epitaxial wafer specifications for a 600V SiC lateral power device development and fabrication.

2.7 Advantage of thin drift layer used in RESURF structure and isolation

For high voltage power device to be integrated into monolithic chip, isolation structure between neighboring devices play an important role. This is especially important when there are low-voltage circuitries, such as driver IC that requires protection from high voltage operating power devices that are integrated in to one chip. Some of different isolation methods employed are:

1) Self-isolation
2) Junction isolation
3) Dielectric isolation
4) Mesa-etch isolation

An example of self-isolation method is found in a conventional CMOS structure where the device inherently forms reverse-biased junction though the n-well structure on p-type substrate. The problem with this method is flexibility of the circuit is reduced since for the isolation to be effective, the pn-junctions between the devices need to be permanently reverse-biased.

Junction isolation method is additional doped area of the opposite polarity introduced between devices to ensure electrical isolation. These regions are formed either by diffusion for Si devices or ion implantation for SiC devices. For p-type substrates with n-type epitaxial layers, for example, p-doped regions from the surface down to the substrate are used.

Dielectric isolation method is using dielectric material such as SiO_2 layer to separate neighboring devices. This leads to much lower ohmic and capacitive coupling compared to junction isolation techniques. There are no parasitic devices between the transistors since there are no additional pn-junctions. SOI (Silicon-on-insulator) devices are an example of dielectric isolated structure where devices benefit in form of higher temperature operation, and lower leakage and parasitic capacitance. Trench etched isolation filled with passivation is another form of dielectric isolation.

Finally, the mesa-etch isolation method is the simplest and most effective way in separating neighboring devices. This method is to simply etch an “island” where devices are formed. The area between adjacent devices can be filled with additional passivation layer to further enhance the isolation. This method is especially applicable for SiC lateral RESURF structure where drift regions are thin. It is important that this mesa etch reaches the depth up to the natural depletion layer of the n- epi layer /p- layer junction underneath to restrict the current flow. So, having a thin drift layer simplify the mesa etching process. The following dissertation research on thin RESURF lateral device employs this mesa-

etch isolation method in separating neighboring devices. Example of integrated lateral RESURF all 4H-SiC half-bridge circuit using mesa-etch isolation is shown in Figure 2.13 and 2.14.

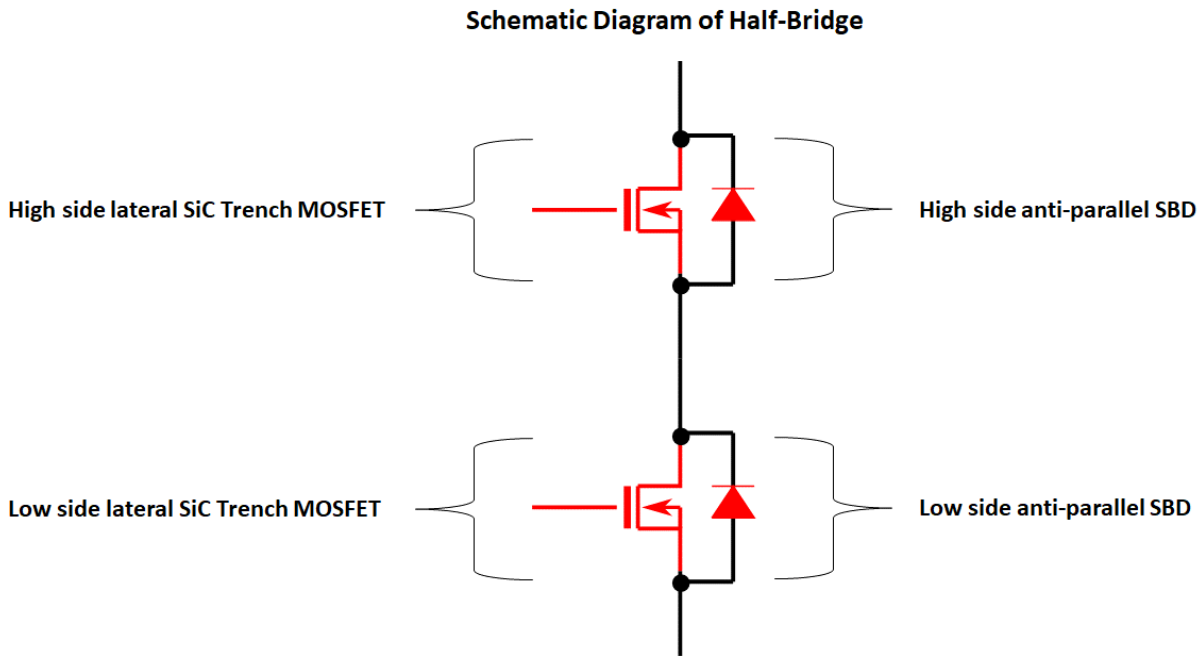


Fig. 2.13 Schematic of conventional half-bridge circuit diagram using SiC MOSFET and Schottky barrier diode

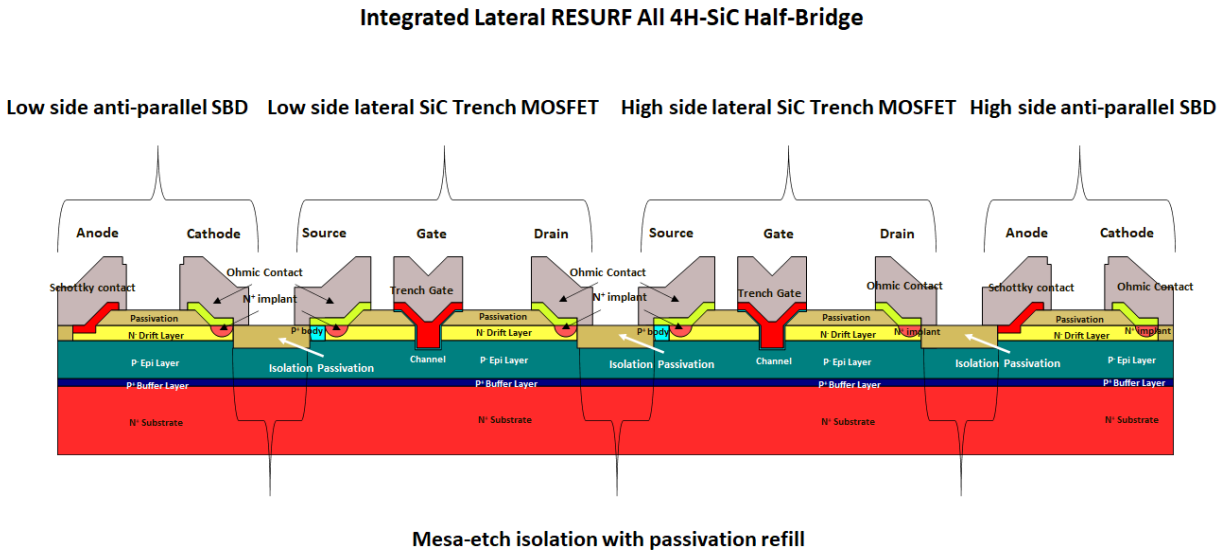


Fig. 2.14 Cross-section diagram of integrated lateral RESURF all 4H-SiC half-bridge circuit

2.8 Objectives of the Dissertation Research

The objective of the research is to develop lateral RESURF devices that could be integrated in to a monolithic 4H-SiC power IC chip in the near future. By experimentally demonstrating through fabrication and development of simple 2-terminal lateral RESURF SiC Schottky diodes and 3-terminal lateral RESURF SiC MESFETs, the basis of essential devices that could lead to a novel SiC power integration technology for high temperature, high frequency, and high voltage applications can be realized. The large bandgap of 4H-SiC (roughly three times larger than that of Si) enables integrated devices to operate at increased temperatures and low-leakage currents compared to Si devices. SiC can also withstand high electric fields, ten times greater than Si, and at a much higher current density before it can break down. The large electrons saturation drift velocity enables SiC to generate high power at high frequencies. All of these advantages of the SiC material enables monolithic 4H-SiC power IC chip to go beyond the operation environment of conventional Si electronics and power IC chips.

In order to demonstrate lateral 4H-SiC devices based monolithic power IC technology, critical technology on device and epitaxial wafer design, photolithography mask layout, robust fabrication flow, and evaluation and analysis of device characteristics, will be addressed. Specifically, the identified essential elements for the development and fabrication of the devices are:

1) Design and simulation of 4H-SiC lateral RESURF power device through TCAD (Technology computer-aided design) to attain optimal design specification for RESURF epitaxial wafer for process fabrication.
2) Photolithography mask layout strategy to capture performance trends according to design splits made. Test patterns such as TLM (Transmission line measurement) and vertical breakdown patterns are incorporated for necessary device performance analysis.
3) Develop a robust fabrication process flow for SiC lateral devices. This includes addressing of critical process issues, such as ohmic contacts with low specific contact resistance (ρc), N^+ ion implant process with effective activation procedure, and sloped field plate structure to mitigate electric field crowding that occurs during lateral current conduction and voltage blocking.
4) Evaluation of forward and reverse characteristics of the fabricated devices, as well as capacitance – voltage evaluation are conducted for analysis of both static and dynamic performance of lateral device compared to conventional vertical devices.
5) Simulation analysis of obtained electrical characterization results for further optimization of wafer and device design and process flow modifications.

Chapter 3. DESIGN AND SIMULATION OF 4H-SIC LATERAL RESURF POWER DEVICE

3.1 Simulation model and method

The 2D device simulator used for optimal RESURF epitaxial wafer and device design is the Sentaurus Device TCAD Simulator by Synopsys. Poisson's equation and continuity equations for electrons and holes were solved, and a drift-diffusion model was used to solve transport equations to calculate specifications of the designed epitaxial wafer and predict both forward conduction and blocking performance of the device. In addition, in order to accurately simulate the electrical characteristics of the various 4H-SiC lateral RESURF power device structure, the following physical models were activated in the simulation: Recombination (Auger, SRH (Doping Dependence and Temperature Dependence), and Avalanche (OkutoCrowell)), Mobility (Doping Dependence, High Field Saturation, and Incomplete Ionization), Incomplete Ionization, and Effective Intrinsic Density (OldSlotboom). First, the advantages of lateral RESURF structure were theoretically calculated from an on-resistance point of view. Then, optimal epitaxial wafer design specification was determined through 2D numerical simulation using a lateral RESURF p-n diode cell. Finally, lateral RESURF Schottky barrier diode and MESFET structure with optimum sloped field plate structure was simulated and analyzed before fabrication.

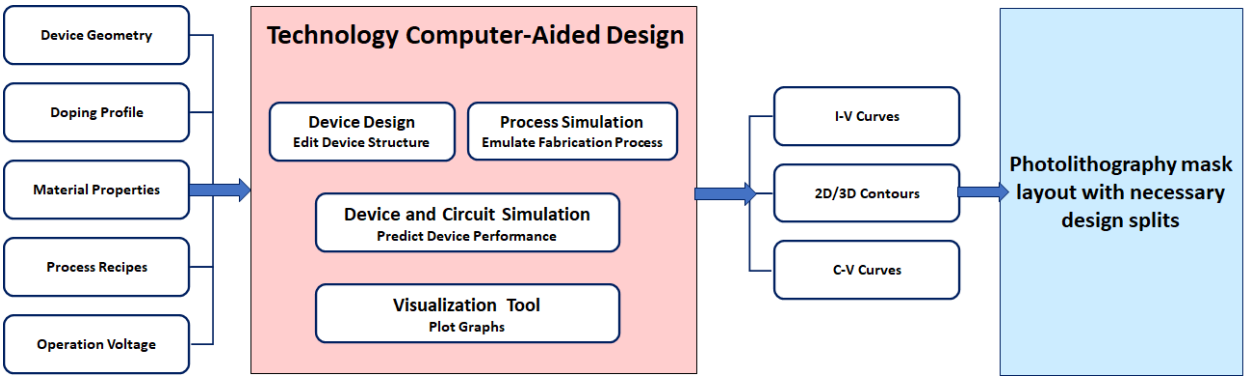


Fig. 3.1 Design and simulation flow using TCAD explaining principle tools and its input/output files

3.2 RESURF device figure of merit (FOM)

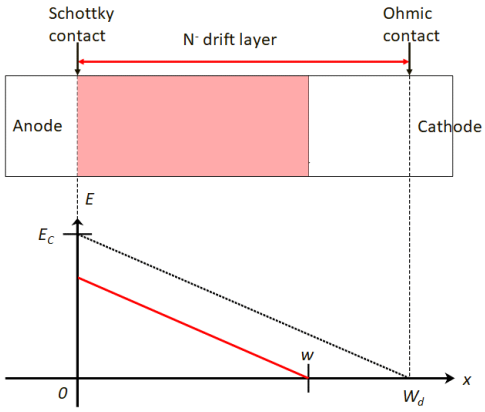


Fig. 3.2 Electric field distribution of a conventional vertical diode

As shown in Figure 3.2, the electric field distribution of a conventional vertical diode has a triangular shape. The breakdown voltage BV of the device is expressed by the equation given below (Eq.3.1):

$$BV = \frac{1}{2} W_D \cdot E_C \tag{3.1}$$

The depletion width W_D under breakdown condition is given by:

$$W_D = \frac{2BV}{E_C} \tag{3.2}$$

where E_C is the critical electric field at breakdown for the semiconductor material. Resistivity ρ is expressed with majority carrier mobility μ, electron charge q, and doping concentration in the drift region N_D using the following equation.

$$\rho = \frac{1}{q\mu_n N_D} \tag{3.3}$$

Thus, the specific resistance of the drift region $R_{on,sp}$ is obtained using Eq. (3.3) as follows:

$$R_{on,sp} = \frac{W_D}{q\mu_n N_D} \tag{3.4}$$

The doping concentration in the drift region required to obtain the above breakdown voltage BV is given by:

$$N_D = \frac{\varepsilon_S E_C^2}{2qBV} \tag{3.5}$$

Combining Eq. (3.2), Eq. (3.4), and Eq. (3.5), the specific resistance $R_{on,sp}$ is expressed with the breakdown voltage BV of the device in Eq. (3.6)

$$R_{on,sp} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \tag{3.6}$$

The denominator $\varepsilon_S \mu_n E_C^3$ is commonly referred to as Baliga's figure of merit of power device [17].

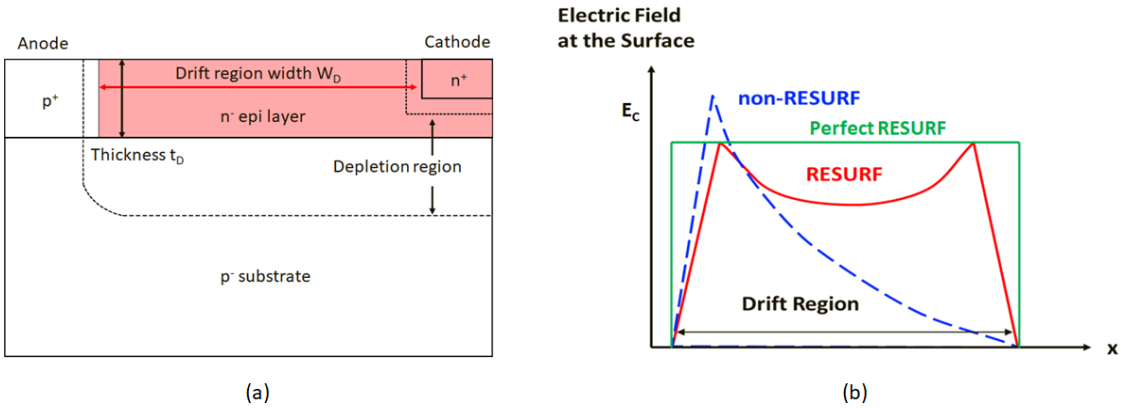


Fig. 3.3 Electric field distribution of a lateral RESURF PIN diode

The concept of the RESURF is to utilize 2-dimensional depletion using lateral p^+ / n^- epitaxial junction and vertical p^- substrate/ n^- epitaxial junction to reduce the surface electric field of the device. The optimized lateral surface electric field distribution of a RESURF device is shown by the red curve in Figure 3.3 (b) which is close to a rectangular uniform electric field of perfect RESURF (green). By making this approximation, the breakdown voltage BV of an ideal REDURF device is:

$$BV = W_D \cdot E_C \tag{3.7}$$

Where W_D is the lateral drift layer width. The specific on-resistance of the drift layer is given by (3.8) if the drift layer thickness is defined as t_D

$$R_{on,sp} = \frac{W_D^2}{q\mu_n N_D t_D} \tag{3.8}$$

Total charge ionized Q_n in the drift region is expressed by Eq. (9) using Gauss's law:

$$Q_n = q \cdot N_D \cdot t_D = \varepsilon_S \cdot E_C \tag{3.9}$$

Where t_D is the thickness of the drift layer. Combining (3.7) and (3.9) into (3.8),

$$R_{on,sp} = \frac{BV^2}{\varepsilon_S \mu_n E_C^3} \cong 0.0283 m\Omega \cdot cm^2 \ (SiC\ 600V\ Rating) \tag{3.10}$$

Comparing Eq. (3.10) and Eq. (3.6), in theory, an ideal lateral RESURF device will perform 4 times better in on-resistance over conventional vertical device. When the surface of electric field is not a uniform rectangular shape, the breakdown voltage will be lower than Eq. (3.7), therefore the actual specific on-resistance will be higher than Eq. (3.10). The design objective of a RESURF power device to ensure the electric field is like that of the red curve in Fig. 3.3. This is typically done by optimizing the RESURF charge Q_n shown in equation Eq. (3.9) to maximize the breakdown voltage.

3.2.1 RESURF effect and maximum charge

Optimum charge for a lateral RESURF device is defined as the $Q_{optimum}$ which maximize the breakdown voltage once W_D and t_D are fixed. According to Eq. (3.9), the optimal charge is

$$Q_{optimum} = \frac{\varepsilon_S E_C}{q} = 1.34 \times 10^{13} cm^{-2} \tag{3.11}$$

Where E_C=2.5 × 10^6 V/cm and ε_S=9.7 × 8.85 × 10^{-14} F/cm for SiC material.

3.3 1st attempted epitaxial design (original design epi) analysis

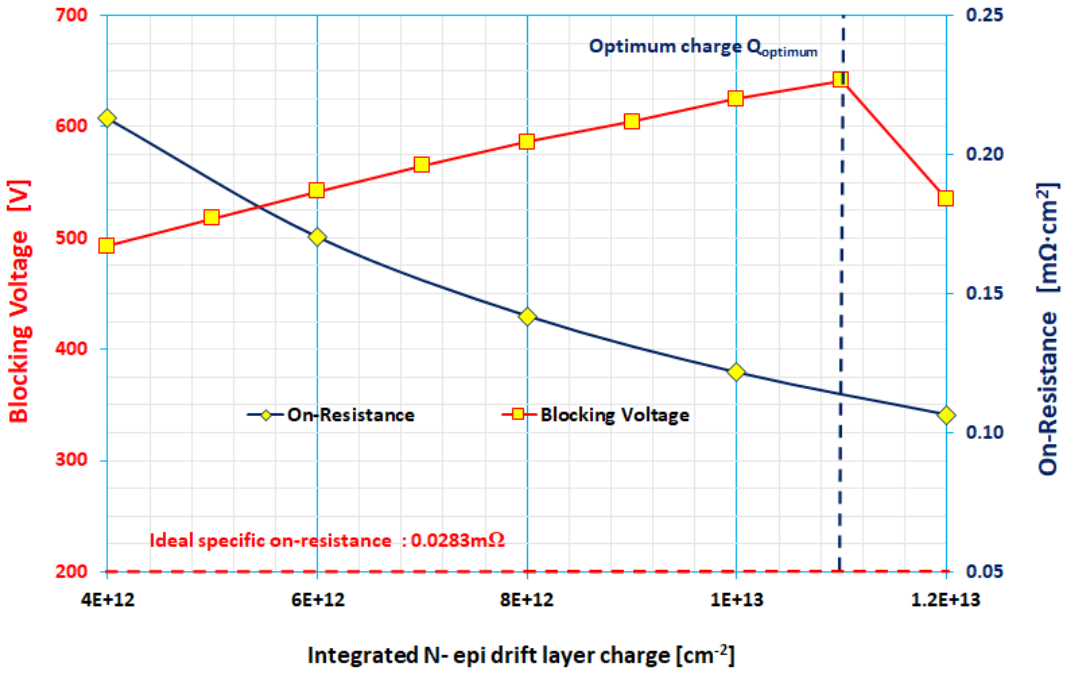
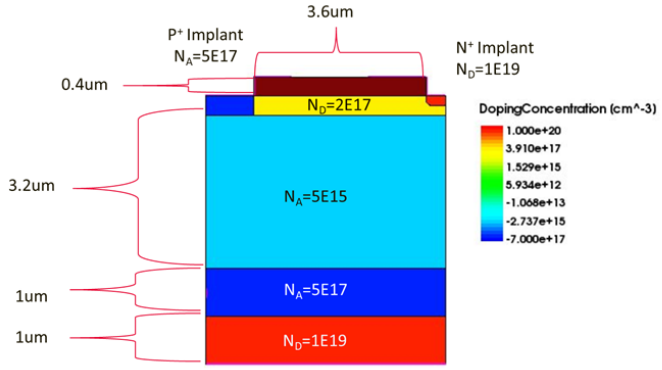


Fig. 3.4 Blocking voltage and on-resistance of lateral RESURF p-n diode cell in relationship with integrated N⁻ drift layer charge

Figure 3.4 is a plot of blocking voltage and on-resistance (calculated from equation(3.8) using the doping concentration and thickness from the simulation) of the lateral RESURF p-n diode cell simulated using TCAD in relationship with integrated N^- drift layer charge. The peak in the blocking voltage curve indicates optimal charge for the N^- drift layer, which matches closely to the calculation in Eq. (3.11). Since there is a sudden drop in the breakdown voltage of the device past the maximum charge peak, the doping concentration of the N^- drift region was set to $2\times10^{17}cm^{-3}$ (total charge of $8E12cm^{-2}$) to assure $\pm 5\times10^{16}cm^{-3}$ variance in doping concentration during actual epi growth using a CVD reactor. P^- epi layer thickness and doping concentration was set to 3.2um and $5\times10^{15}cm^{-3}$ respectively to assure > 600V vertical blocking voltage through a punch-through design of the vertical P^- epitaxial/ N^- epitaxial junction.



(a)

Parameters	Values
N^- Epi Drift Concentration	2×10^{17} cm^{-3}
P^- Epi Concentration	5×10^{15} cm^{-3}
P^+ Buffer Concentration	5×10^{17} cm^{-3}
N^- Epi Drift Thickness	0.4um
P^- Epi Thickness	3.2um
P^+ Buffer Thickness	1um

(b)

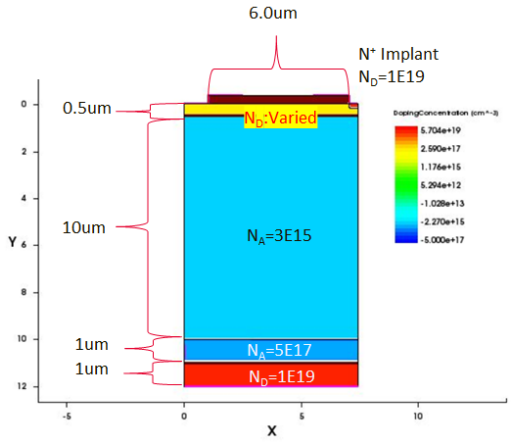
Fig. 3.5 Model of lateral RESURF p-n diode cell used in simulation (a) to determine optimum epitaxial design (b)

3.3.1 Problem with 1st attempted epitaxial design (original design epi)

The first attempted epitaxial design was set very aggressively to achieve both forward and reverse performance to the limit of the epi wafer design. The doping concentration for the N^- drift layer was set close to the maximum possible extent, and drift length was set to the minimum length for better forward performance. The most critical parameter of the design that presented a challenge was the lack of margin in the vertical blocking capability which only had little over 600V (simulated vertical breakdown of 691.3V in 2D simulation). Since all simulation for the design of the epitaxial wafer was done in 2D simulation, much of the 3D electric field crowding was not considered. The vertical breakdown of the actual fabricated device only had 400V~550V vertical blocking capability, which was insufficient for the actual lateral RESURF device to block the required 600V rating. Thus, two new designs of epitaxial wafer and a new photolithography mask for the final fabrication run were required.

3.4 New epitaxial design with thick and lighter doped P⁻ epi layer (Design 1 and Design 2)

The primary objective of the newly designed epi wafer is to increase the vertical blocking voltage by increasing the p⁻ epi layer thickness and applying a lighter doping concentration. As shown in the bottom Figure 3.6, the thickness was increase from 3.2um to 10um and doping concentration from $5\times10^{15}cm^{-3}$ to $3\times10^{15}cm^{-3}$. From these modifications, the vertical blocking voltage have increased double the amount from 691.3V to 1423V through TCAD simulation. Once the vertical breakdown voltage is set, thickness and doping concentration is varied to find the optimum integrated charge for maximum RESURF effect.



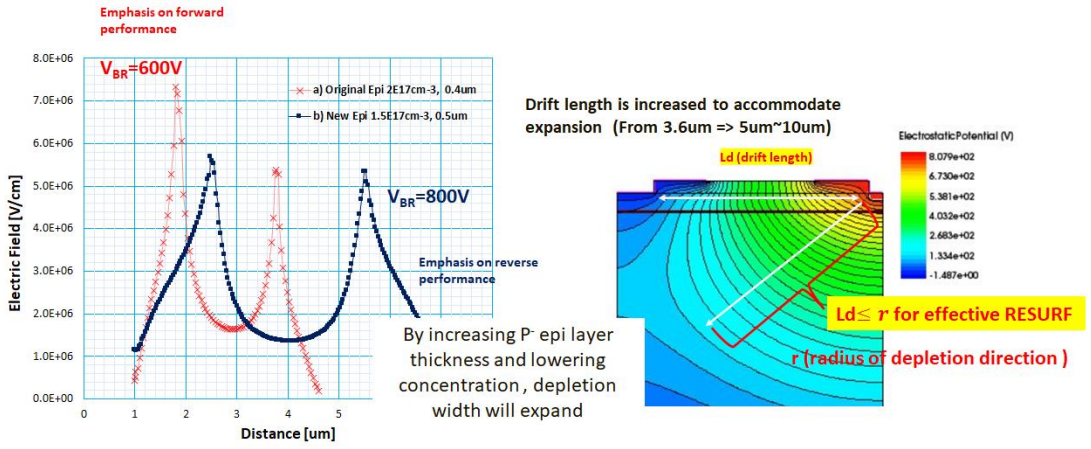
(a)

New epi wafer design parameters

Parameters	Original Values	Punch-through design with higher vertical blocking voltage
N⁻ Epi Drift Concentration	2×10^{17} cm^{-3}	9×10^{16} cm^{-3} (Initial)
P⁻ Epi Concentration	5×10^{15} cm^{-3}	3×10^{15} cm^{-3}
P⁺ Buffer Concentration	5×10^{17} cm^{-3}	5×10^{17} cm^{-3}
N⁻ Epi Drift Thickness	0.4um	0.5um
P⁻ Epi Thickness	3.2um	10um
P⁺ Buffer Thickness	1um	1um
Vertical Blocking Voltage	691.3V	1423V

(b)

Fig. 3.6 Model of lateral RESURF Schottky diode cell with thick P⁻ epi layer (a) to determine optimum epitaxial design with higher blocking voltage (Design 1) (b)



(a) (b)

Fig. 3.7 Surface electric field cut comparison of lateral diodes with different epi parameters (a) cross section with electrostatic potential indicating expansion of depletion layer from thicker P⁻ epi layer (b)

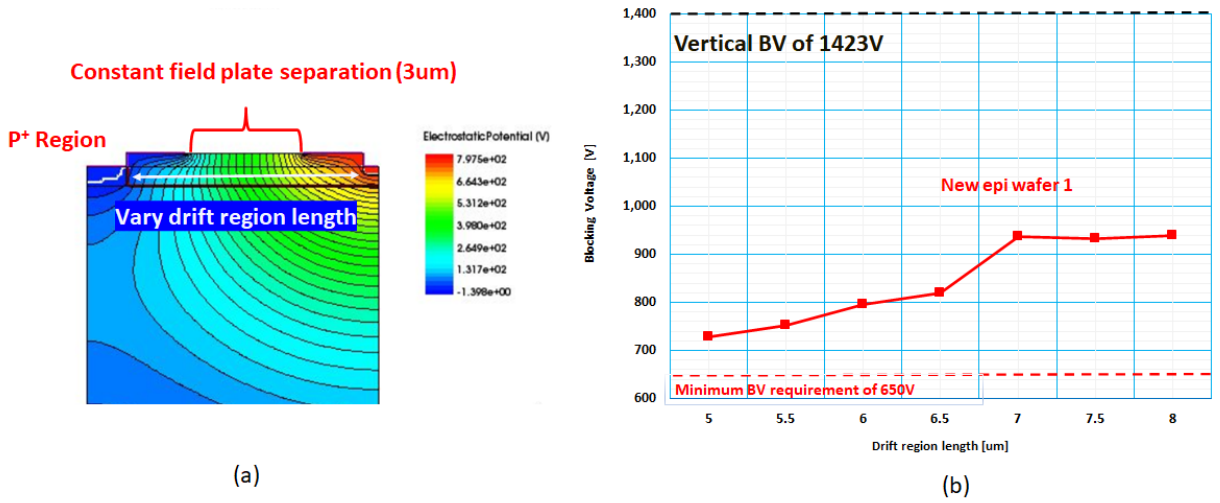


Fig. 3.8 Varying the drift region length with constant field plate separation (a) Breakdown voltage in relationship with drift region length variation (b)

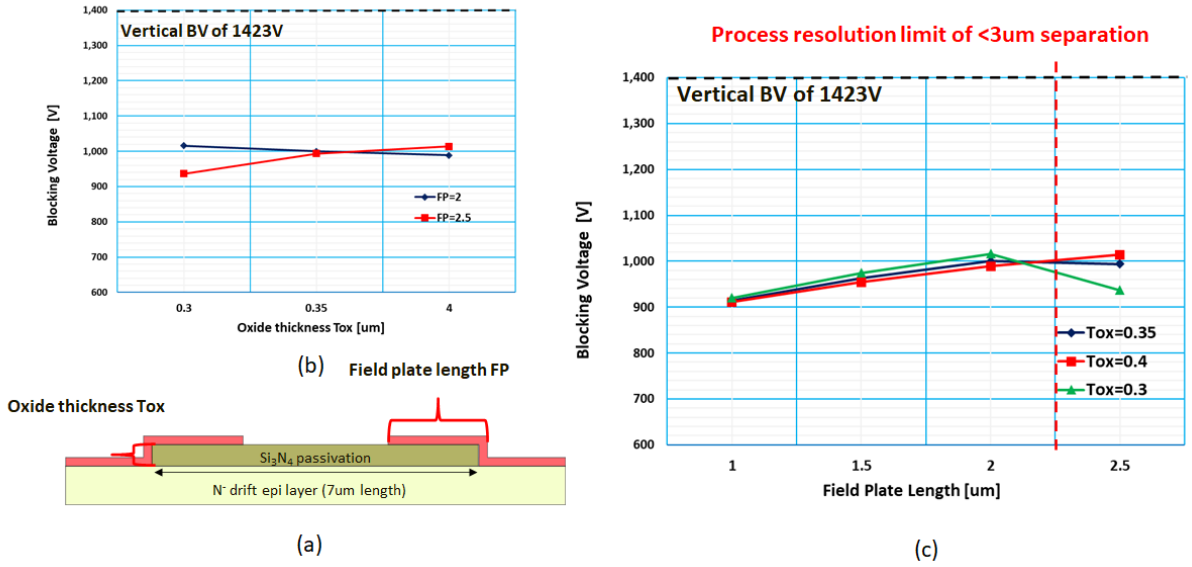


Fig. 3.9 Optimization of field plate structure (definition) (a) thickness dependence (b) field plate length dependence

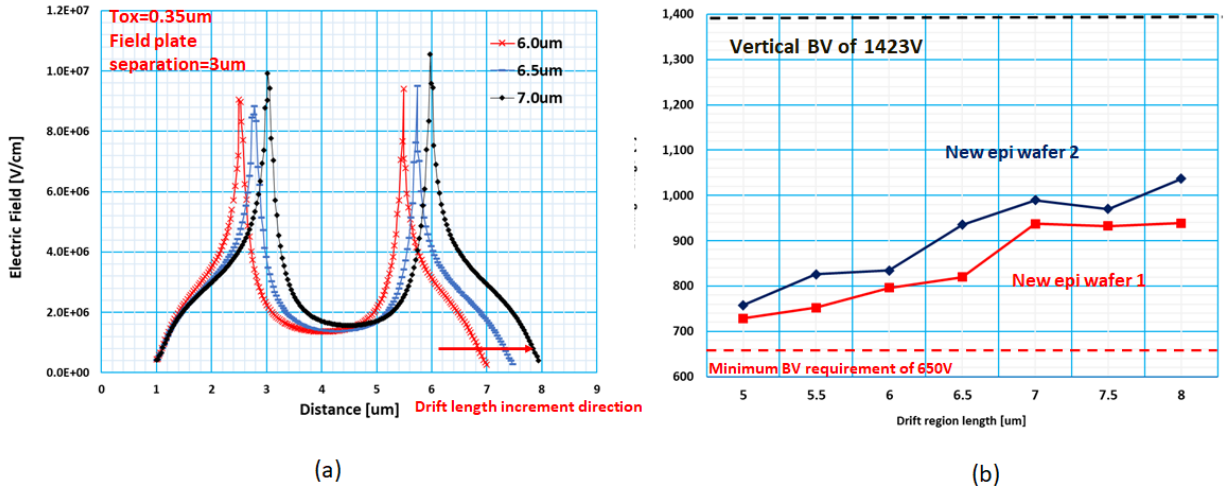
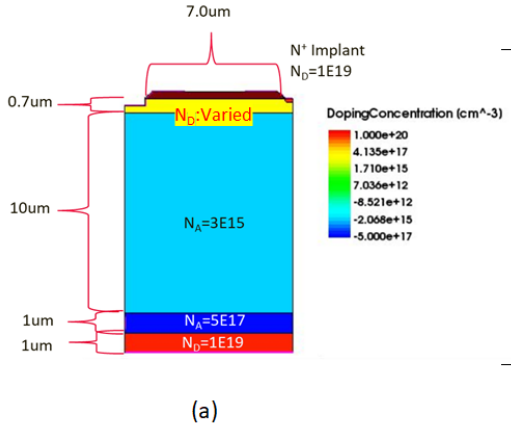


Fig. 3.10 Varying the drift region length with constant field plate separation surface electric field cut (a) Breakdown voltage in relationship with drift region length variation (b)



New epi wafer design parameters

Parameters	Original Design	Design 1	Design 2
N⁻ Epi Drift Concentration	2×10^{17} cm^{-3}	**9×10^{16} cm^{-3} (Initial)**	**7×10^{16} cm^{-3} (Initial)**
P⁻ Epi Concentration	5×10^{15} cm^{-3}	3×10^{15} cm^{-3}	3×10^{15} cm^{-3}
P⁺ Buffer Concentration	5×10^{17} cm^{-3}	5×10^{17} cm^{-3}	5×10^{17} cm^{-3}
N⁻ Epi Drift Thickness	0.4um	**0.5um**	**0.7um**
P⁻ Epi Thickness	3.2um	**10um**	**10um**
P⁺ Buffer Thickness	1um	1um	1um
Vertical Blocking Voltage	691.3V	1423V	1423V

(b)

Fig. 3.11 Model of lateral RESURF Schottky diode cell with thick P⁻ epi layer (a) to determine optimum epitaxial design with higher blocking voltage (Design 2) (b)

Epitaxial Wafer Design 1 (t_{epi}=0.5um, N_d= $1.5\times10^{17}cm^{-3}$)

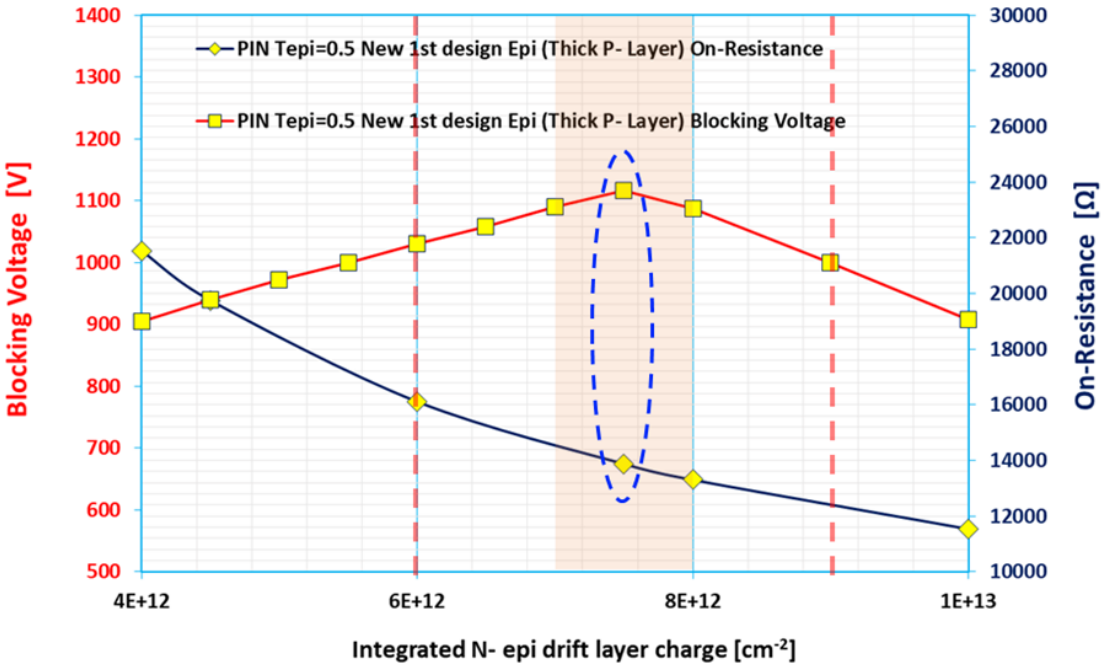


Fig. 3.12 Epi wafer design 1. Blocking voltage and on-resistance of lateral RESURF p-n diode cell in relationship with integrated N^- drift layer charge Tolerance of ± 50nm for thickness and ± 3E16 cm^{-3} for doping concentration
(On-resistance is for a unit cell with Z direction dimension of 1 um)

Epitaxial Wafer Design 2 (t_{epi}=0.7um, N_d= $1.2\times10^{17}cm^{-3}$)

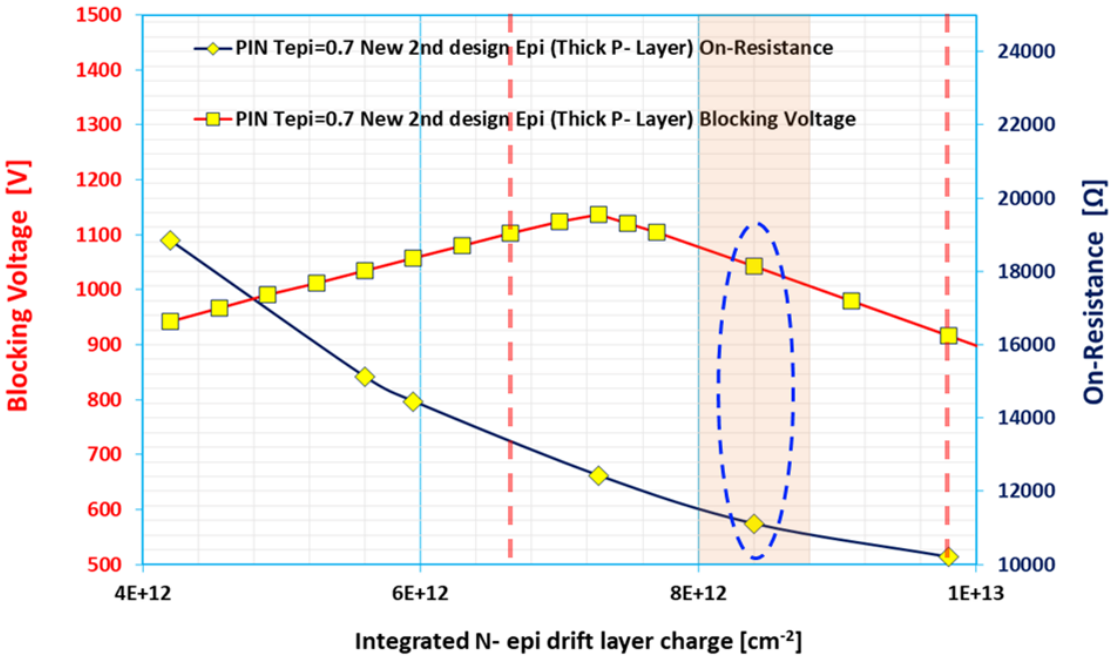


Fig. 3.13 Epi wafer design 2. Blocking voltage and on-resistance of lateral RESURF p-n diode cell in relationship with integrated N^- drift layer charge Tolerance of ± 50nm for thickness and ± 2.5E16 cm^{-3} for doping concentration
(On-resistance is for a unit cell with Z direction dimension of 1 um)

Table 3.1 Epitaxial wafer design parameters

Parameters	Design 1	Design 2
N^- Epi Drift Concentration	$1.5\times 10^{17}\ cm^{-3}$	$1.2\times 10^{17}\ cm^{-3}$
P^- Epi Concentration	$3\times 10^{15}\ cm^{-3}$	$3\times 10^{15}\ cm^{-3}$
P^+ Buffer Concentration	$5\times 10^{17}\ cm^{-3}$	$5\times 10^{17}\ cm^{-3}$
N^- Epi Drift Thickness	0.5um	0.7um
P^- Epi Thickness	10um	10um
P^+ Buffer Thickness	1um	1um

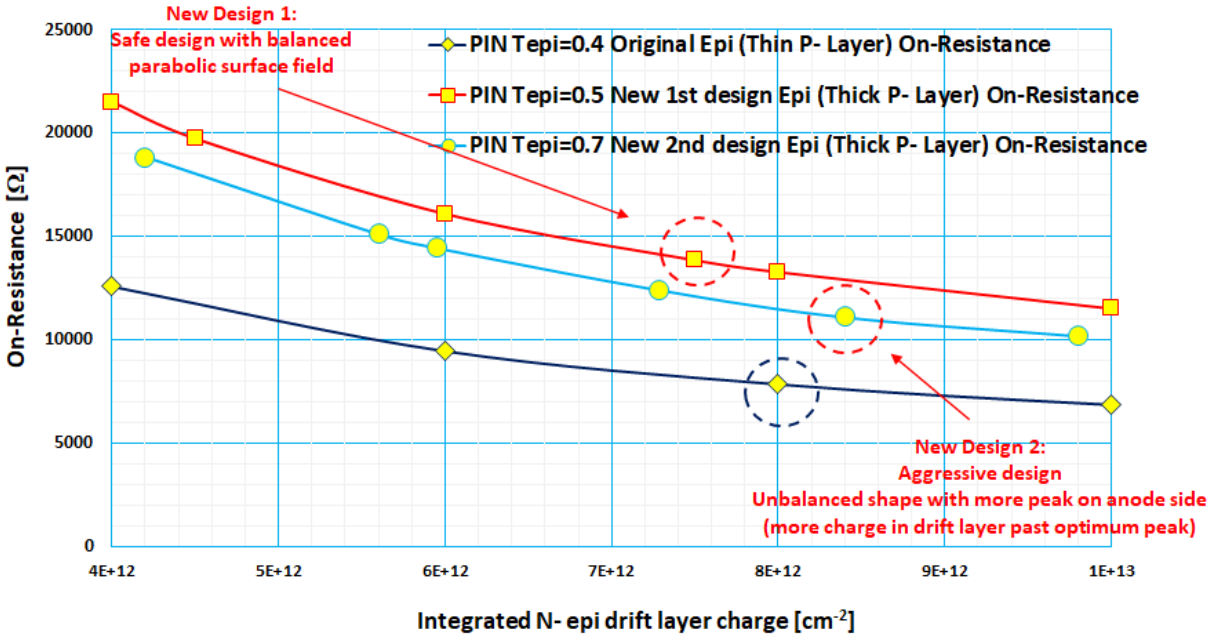
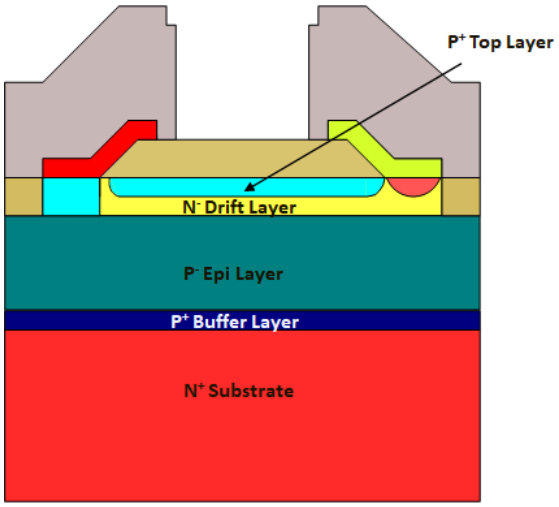


Fig. 3.14 On-resistance versus different integrated N- epi drift layer charges and thickness (Comparison of 3 different epi design)

The final design specification of the 2 new epi wafer is shown in the above table 3.1. As shown in Figure 3.6, newly designed epitaxial wafer 1 has the n^- drift thickness of 0.5um and its doping concentration was chosen in correspondence to the maximum RESURF effect achieved at its optimum charge of $7.5\times10^{12}cm^{-2}$. It can be said that Design 1 is a safe design with balanced parabolic surface electric field. On the contrary, newly designed epitaxial wafer 2 has the n^- drift thickness of 0.7um and its doping concentration was chosen past the optimum charge peak at $8.4\times10^{12}cm^{-2}$. As a result, Design 2 is an aggressive design in terms of forward performance where the surface electric field will be an unbalanced shape with move peak on the anode side. 2 pieces of 4-inch SiC epitaxial wafer with above Table 1 design parameter were order from Ascatron AB for the final fabrication.

3.5 Double RESURF concept and analysis of its benefits and disadvantages through additional TCAD simulation

Additional RESURF effect can be achieved by incorporating an additional layer of the opposite polarity (p^+ top region) on the top of the n^- drift layer. In this structure, the vertical depletion of the n^- drift layer occurs from the two junctions: p^- epi layer/ n^- drift and p^+ top layer/ n^- drift. This device structure is referred to as double-RESURF structure, and because of this two-sided vertical depletion, the total integrated n^- drift layer charge can be significantly increased to twice as much value compared to single-RESURF device. The on-resistance will decrease according to the integrated charge in the p^+ top RESURF layer. It is required that both p^+ top region and n^- drift layer be fully depleted in order to maintain high breakdown voltage in double-RESURF devices.



(a)

Double RESURF PIN diode design parameters

Parameters	Values
Drift region length	7um
Field plate length	2um
Passiavation Thickness	0.4um
N^- Epi Drift Concentration	**3×10^{17} cm^{-3}**
P^- Epi Concentration	3×10^{15} cm^{-3}
P^+ Buffer&Anode Concentration	5×10^{17} cm^{-3}
P^+ Top RESURF Concentration	**5×10^{17} cm^{-3}**
P^+ Top RESURF Depth	**0.2um**
N^- Epi Drift Thickness	0.7um
P^- Epi Thickness	10um
P^+ Buffer Thickness	1um

(b)

Fig. 3.15 Cross-section of a lateral double RESURF 4H-SiC PIN diode (a) and optimum epitaxial design specification (b)

Theoretical calculation for optimum double RESURF can be calculated the same way as the single RESURF considering the charge balance requirements. First, more accurate theoretical calculation of maximum charge for single RESURF device is calculated considering the relationship between the vertical junction depletion extension d_{nepi} and the thickness of the n^- epi layer t_{epi}. Same concept applies with the double RESURF as well, but this time both p^+ top region and n^- drift layer need to be fully depleted before the lateral diode breaks down for the maximum RESURF effect.

3.5.1 More accurate theoretical calculation of maximum charge for single RESURF device

Lateral diode breakdown voltage of the single RESURF p-i-n diode in figure 3 can be expressed,

$$BV_{Lateral} = \frac{\varepsilon_{SiC} E_C^2}{2qN_D} \tag{3.12}$$

Vertical junction (P^- epi /N^- epi) depletion extension d_{nepi} into n^- epi drift region at an applied reverse bias V_R is expressed as following:

$$d_{nepi}(V_R) = \sqrt{\frac{2\varepsilon_{SiC} V_R N_A}{qN_D(N_D+N_A)}} \tag{3.13}$$

For a RESURF effect to work, vertical full depletion of the n^-epi drift region needs take place before the lateral diode breaks down,

$$d_{nepi}(BV_{Lateral}) \geq t_{epi} \tag{3.14}$$

Where, $V_R = \frac{\varepsilon_{SiC} E_C^2}{2qN_D}$

$$Q_n = N_D \cdot t_{epi} = N_D \cdot \sqrt{\frac{2\varepsilon_{SiC} V_R N_A}{qN_D(N_D+N_A)}} \tag{3.15}$$

$$Q_n = \frac{\varepsilon_{SiC} E_C}{q} \cdot \sqrt{\frac{N_A}{(N_D+N_A)}} \tag{3.16}$$

Theoretical limit of Q_n happens when $N_D = N_A$

$$Q_{n,max} = \frac{\varepsilon_{SiC} E_C}{q\sqrt{2}} \tag{3.17}$$

So, for SiC material, the maximum charge for the single RESURF device is 9×10^{12} cm^{-2}

3.5.2 Theoretical calculation of maximum charge for double RESURF device

Similarly, for the double-RESURF structure shown in Figure 9, it is essential that the doping concentration of the P-top layer be such that $N_{ATOP} > N_D > N_A$. This time the weakest breakdown point we need to consider is at the lateral N^+/P-top junction with breakdown voltage given by

$$BV_{Lateral} = \frac{\varepsilon_{SiC} E_C^2}{2qN_{ATOP}} \tag{3.18}$$

To achieve high breakdown voltages in double-RESURF structures, full depletion of the P-top and n^- epi drift region is required. Just as with the case of single-RESURF devices, full depletion should occur before the lateral N^+/P-top junction breaks down. Therefore, in the double-RESURF case, the following conditions must be met:

i)

$$d_{ptop}(BV_{Lateral}) \geq t_{ptop} \tag{3.19}$$

where d_{ptop} is the vertical depletion extension into P-top region at an applied reverse bias $BV_{Lateral}$ and t_{ptop} is the junction depth (thickness) of the P-top region.

ii)

$$d_{nepi1}(BV_{Lateral}) + d_{nepi2}(BV_{Lateral}) \geq t_{epi} \tag{3.20}$$

where d_{nepi1} is the vertical depletion extension into the n^-epi drift region from the P-top/ N^- epi junction and d_{nepi2} is the vertical depletion extension into the n^-epi drift region from the P^- epi / N^- epi junction. The condition i) prevents the structure from breaking down prematurely at the lateral N^+/P-top junction, whereas the condition ii) guarantees the prevention of a premature breakdown at the lateral P^+/ N^- epi junction. As a result, an expression for the optimal P-top integrated charge $Q_p = N_{ATOP} \times t_{ptop}$ and the optimal n^-epi drift region integrated charge $Q_n = N_D \times t_{epi}$ can be determined as follows:

$$Q_p = \frac{\varepsilon_{SiC} E_C}{q} \cdot \sqrt{\frac{N_D}{(N_{ATOP}+N_D)}} \tag{3.21}$$

$$Q_n = \frac{\varepsilon_{SiC} E_C}{q} \cdot \left[\sqrt{\frac{N_D}{(N_{ATOP}+N_D)}} + \sqrt{\frac{N_A \cdot N_D}{(N_{ATOP} \cdot (N_A+N_D)}}\right] \tag{3.22}$$

Based on (7) and (8), an upper bound for Q_p and Q_n can be determined as

$$Q_{p,max} = \frac{\varepsilon_{SiC} E_C}{q\sqrt{2}} \tag{3.23}$$

$$Q_{n,max} = \frac{2\varepsilon_{SiC} E_C}{q\sqrt{2}} \tag{3.24}$$

For SiC material, maximum charge for the double RESURF device and P-top layer are as follows,

$$Q_{p,max} = \frac{\varepsilon_{SiC} E_C}{q\sqrt{2}} = 9 \times 10^{12} cm^{-2}$$

$$Q_{n,max} = \frac{2\varepsilon_{SiC} E_C}{q\sqrt{2}} = 1.8 \times 10^{13} cm^{-2}$$

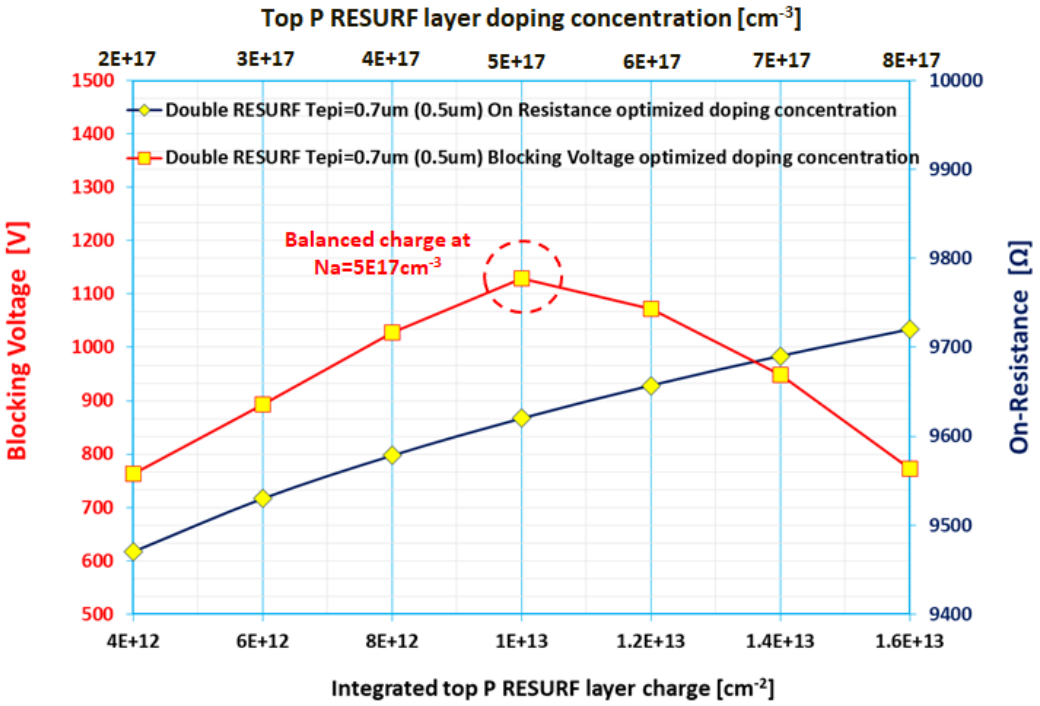


Fig.3.16 Epi wafer design 2. Blocking voltage and on-resistance of lateral RESURF p-n diode cell in relationship with integrated Top P RESURF layer charge (On-resistance is for a unit cell with Z direction dimension of 1 um)

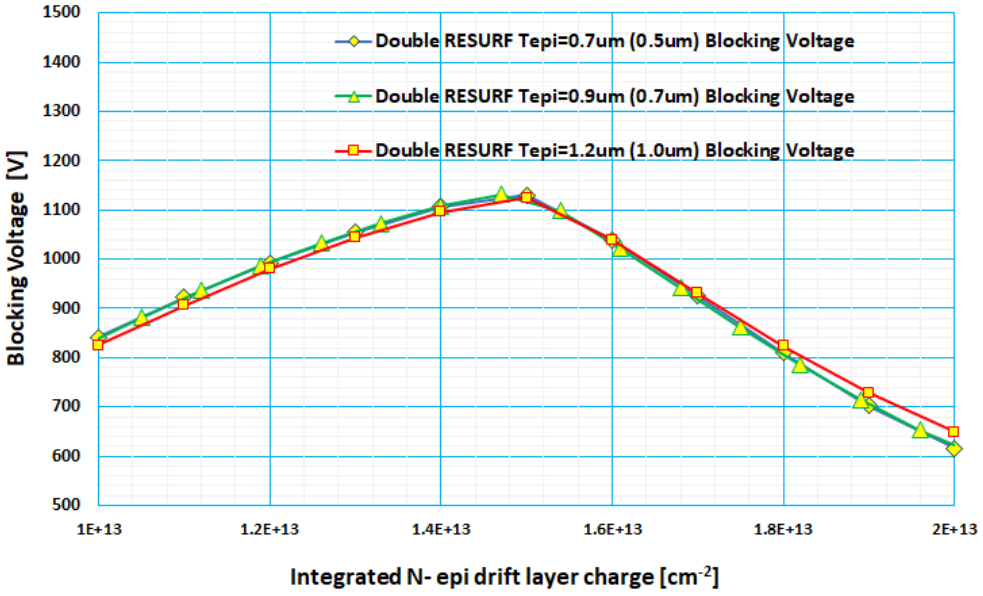


Fig. 3.17 Double RESURF PIN diode Blocking voltage in relationship with integrated N^- drift layer charge and thickness

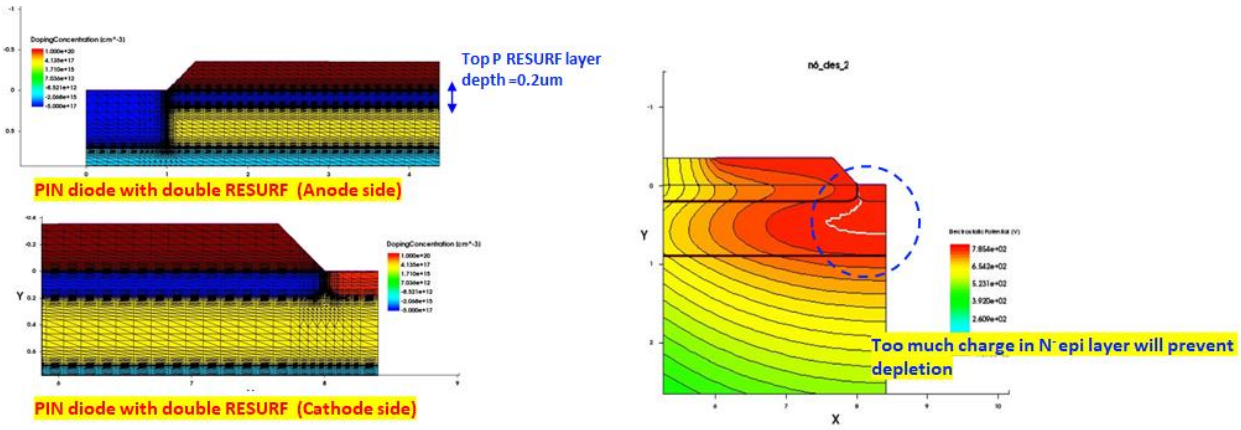


Fig. 3.18 Cross section of a lateral double RESURF PIN diode TCAD model indicating undepleted region from excessive charge in the N^- drift layer

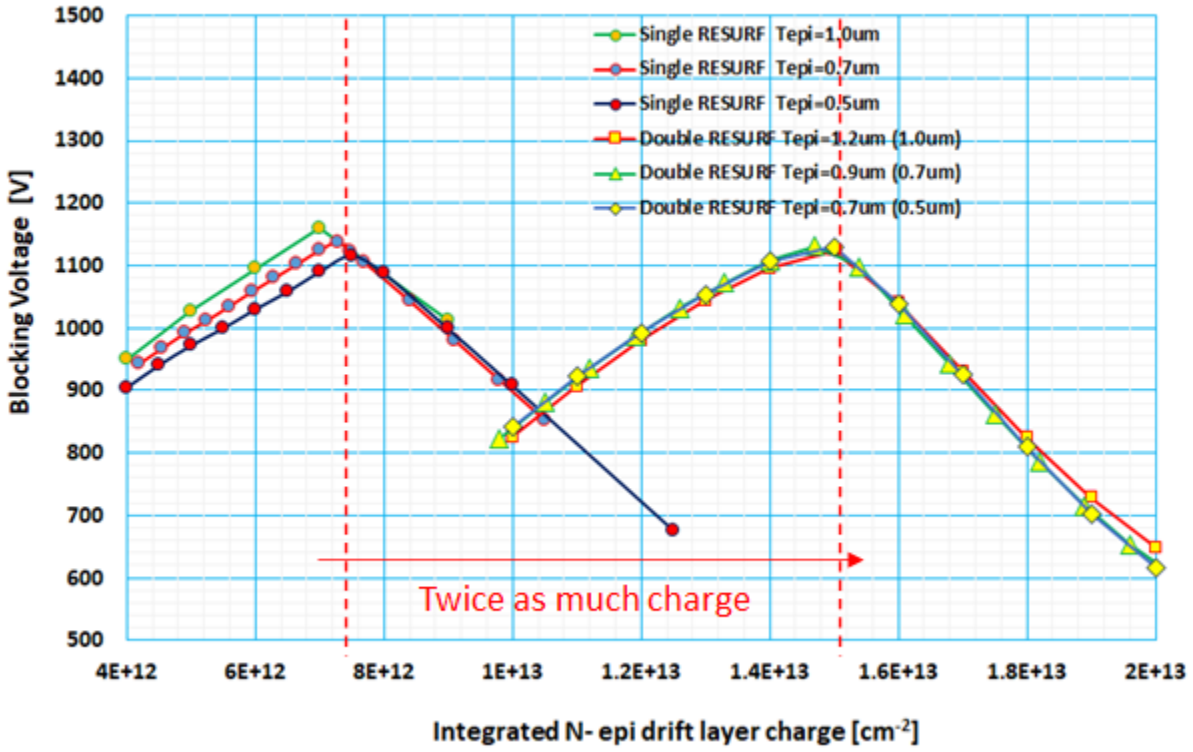


Fig. 3.19 Comparison of Single and double RESURF PIN diode blocking voltage in relationship with integrated N- drift layer charge and thickness

As is evident by the above figure and the theoretical calculation, the presence of the P-top layer in double-RESURF structures allows the total charge in the N^- drift region to be increased by twice as much as that in single-RESURF, leading to a much lower on-resistance in forward performance.

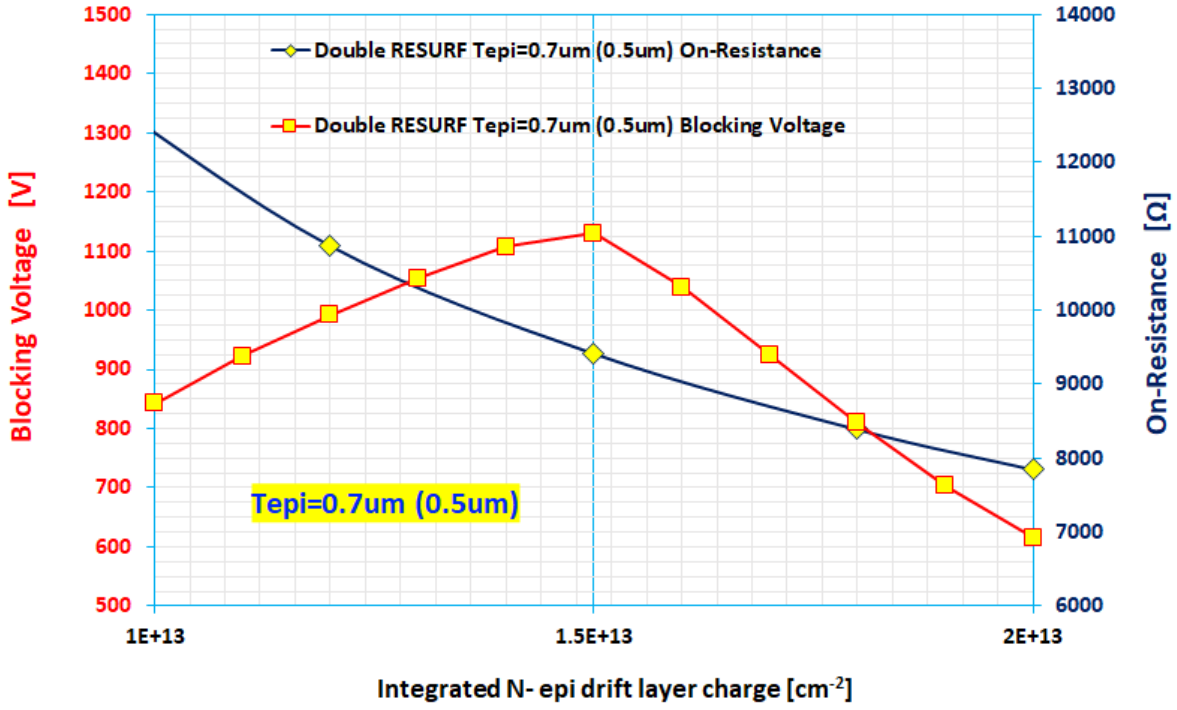


Fig. 3.20 Double RESURF PIN diode blocking voltage and on-resistance in relationship with integrated N- drift layer charge (Thickness 0.7um with 0.2um P- top layer)

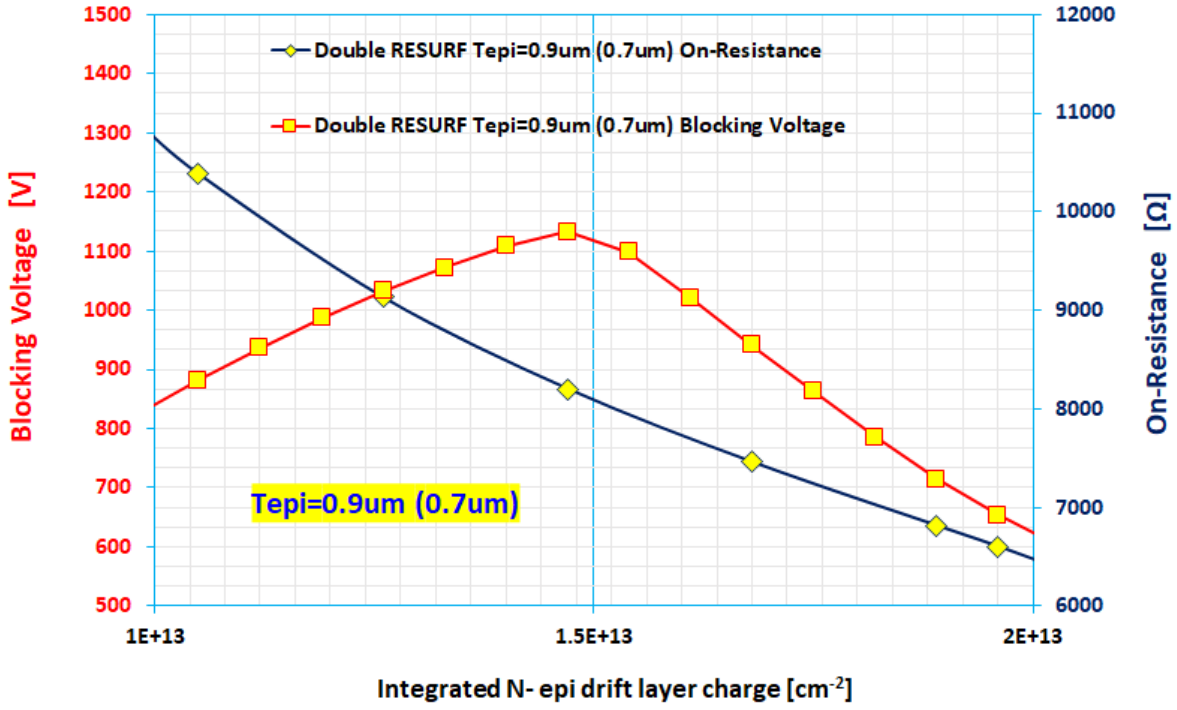


Fig. 3.21 Double RESURF PIN diode blocking voltage and on-resistance in relationship with integrated N- drift layer charge (Thickness 0.9um with 0.2um P- top layer)

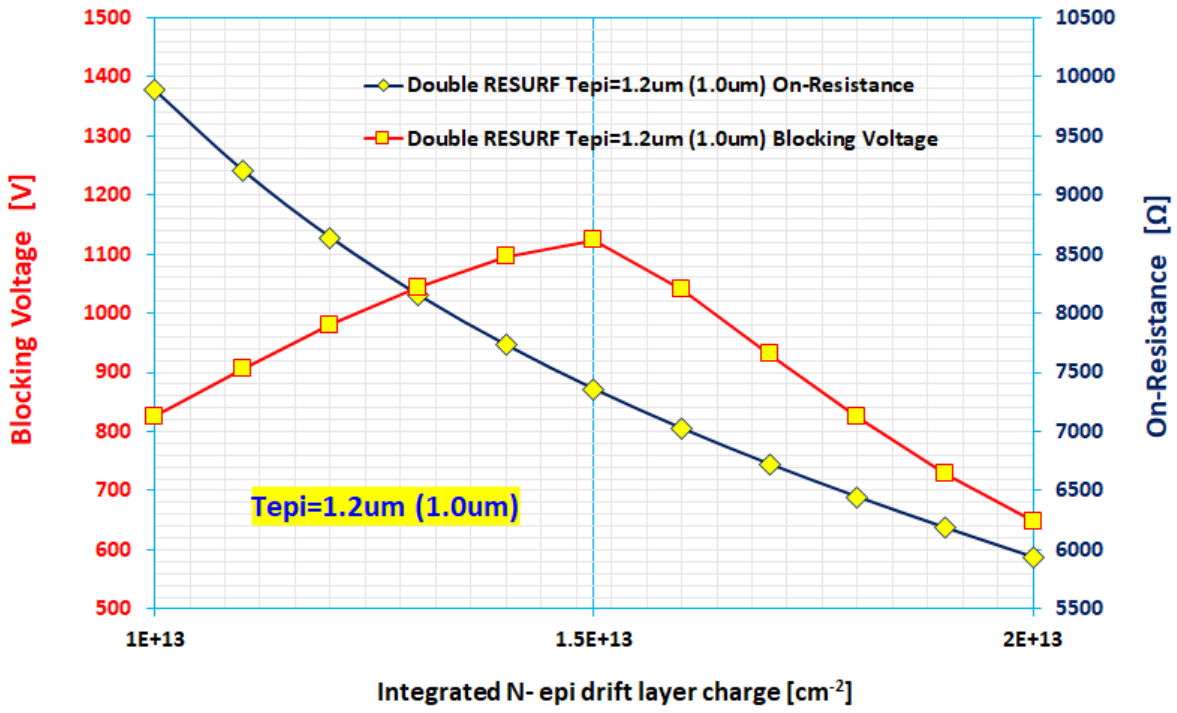


Fig. 3.22 Double RESURF PIN diode blocking voltage and on-resistance in relationship with integrated N- drift layer charge (Thickness 1.2um with 0.2um P- top layer)

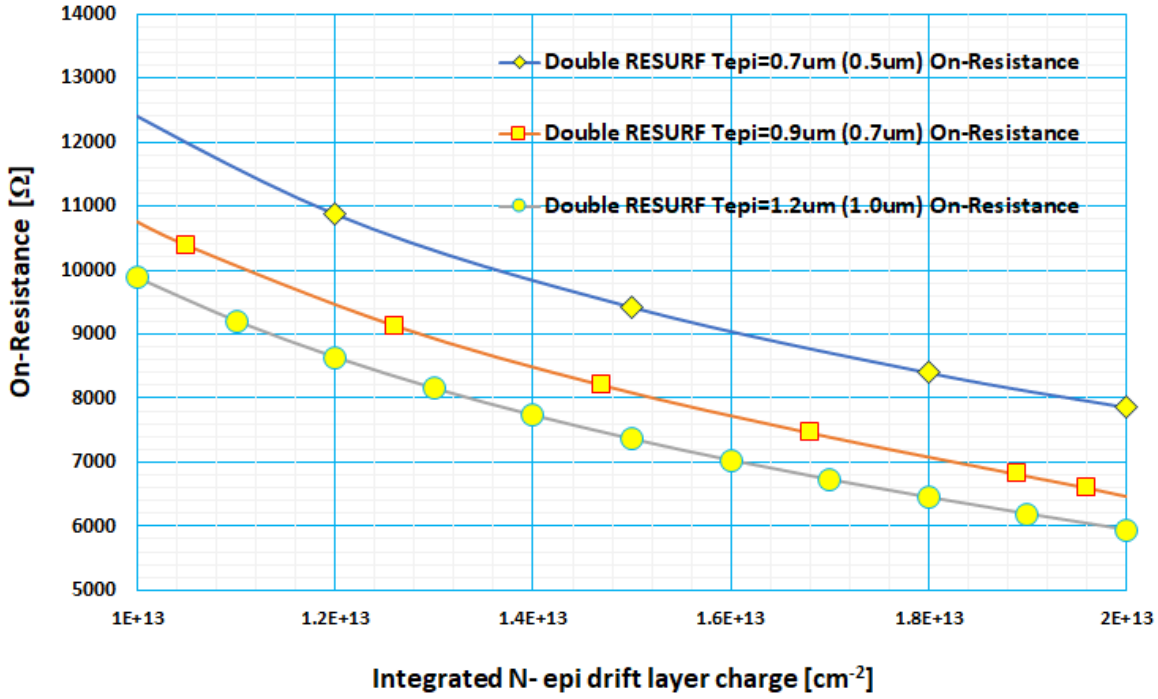
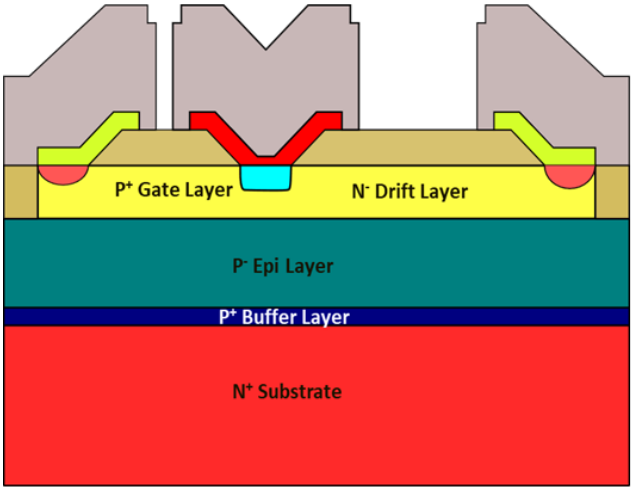


Fig. 3.23 On-resistance versus different integrated N- epi drift layer charges and thickness of double RESURF PIN diode (Comparison of 3 different epi design)

3.6 Additional TCAD simulation of lateral 4H-SiC RESURF JFET and double RESURF JFET using new epitaxial wafer design 2



Single RESURF JFET device design parameters

Parameters	Values
Drift region length	8um
D-S length (gate)	17um (4um)
Gate Field plate length	2.5um
Passiavation Thickness	0.35um
N^- Epi Drift Concentration	7×10^{16} cm^{-3}
P^- Epi Concentration	3×10^{15} cm^{-3}
P^+ Buffer Concentration	5×10^{17} cm^{-3}
P^+ Gate Concentration	1×10^{19} cm^{-3}
P^+ Gate Depth	0.35um
N^- Epi Drift Thickness	0.7um
P^- Epi Thickness	10um
P^+ Buffer Thickness	1um

(a) (b)

Fig. 3.24 Cross-section of a lateral RESURF 4H-SiC JFET with P^+ gate (a) and optimum epitaxial design specification (b)

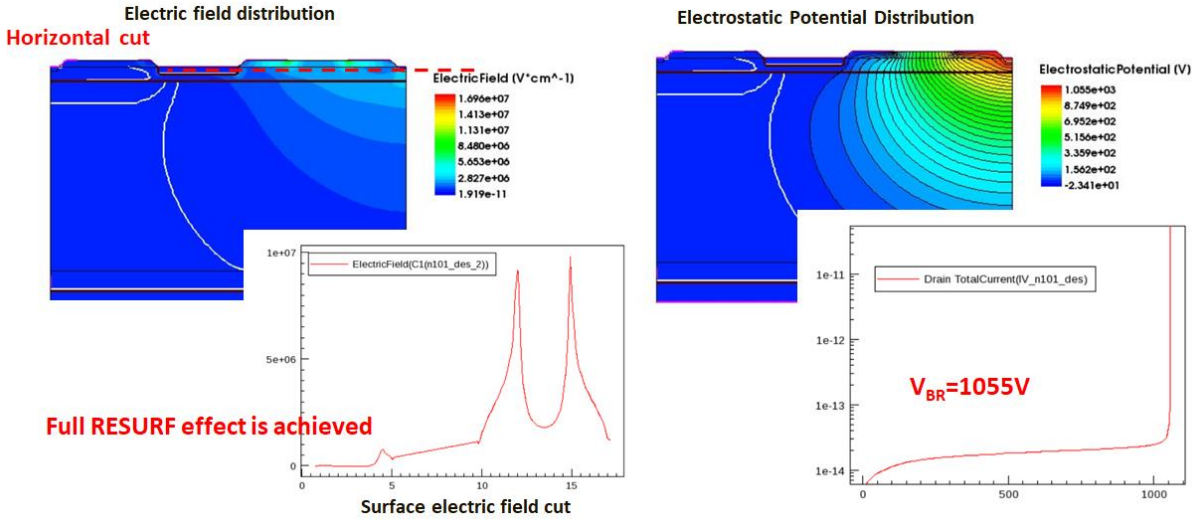
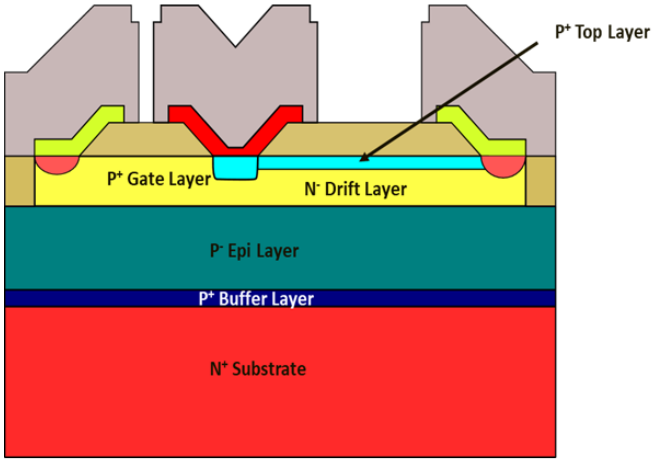


Fig. 3.25 Electric field distribution of the simulated lateral RESURF 4H-SiC JFET (a) and electrostatic potential distribution



(a)

Double RESURF JFET device design parameters

Parameters	Values
Drift region length	8um
D-S length (gate)	17um (4um)
Gate Field plate length	2.5um
Passiavation Thickness	0.35um
N^- Epi Drift Concentration	**1.5×10^{17} cm^{-3}**
P^- Epi Concentration	3×10^{15} cm^{-3}
P^+ Buffer Concentration	5×10^{17} cm^{-3}
P^+ Gate Concentration	1×10^{19} cm^{-3}
P^+ Top RESURF Concentration	**5×10^{17} cm^{-3}**
P^+ Gate Depth	0.35um
P^+ Top RESURF Depth	**0.2um**
N^- Epi Drift Thickness	0.7um
P^- Epi Thickness	10um
P^+ Buffer Thickness	1um

(b)

Fig. 3.26 Cross-section of a double lateral RESURF 4H-SiC JFET with P^+ top RESURF layer (a) and optimum epitaxial design specification (b)

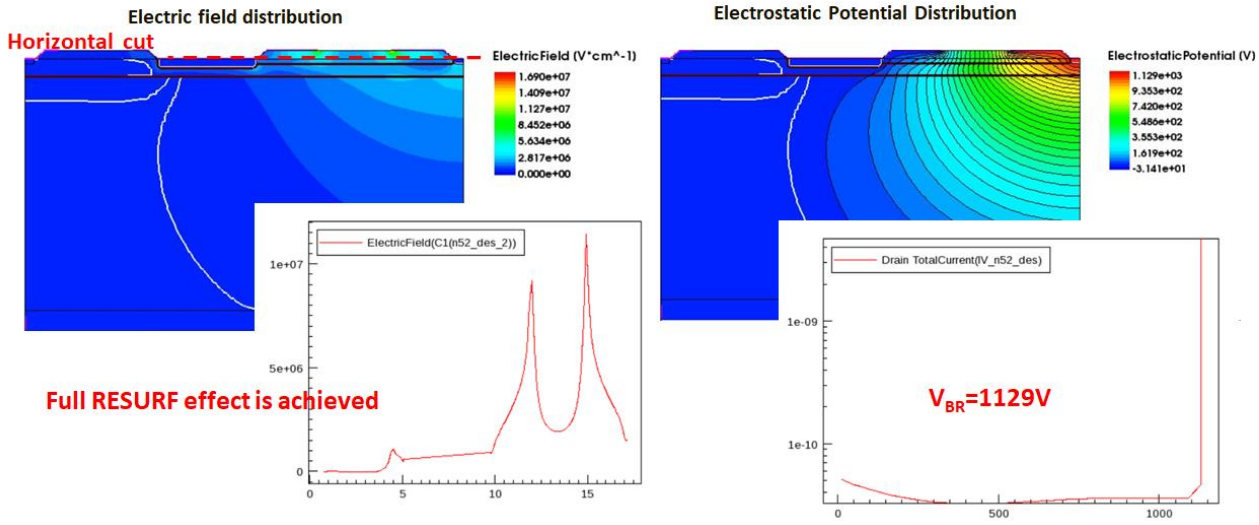


Fig. 3.27 Electric field distribution of the simulated lateral double-RESURF 4H-SiC JFET (a) and electrostatic potential distribution

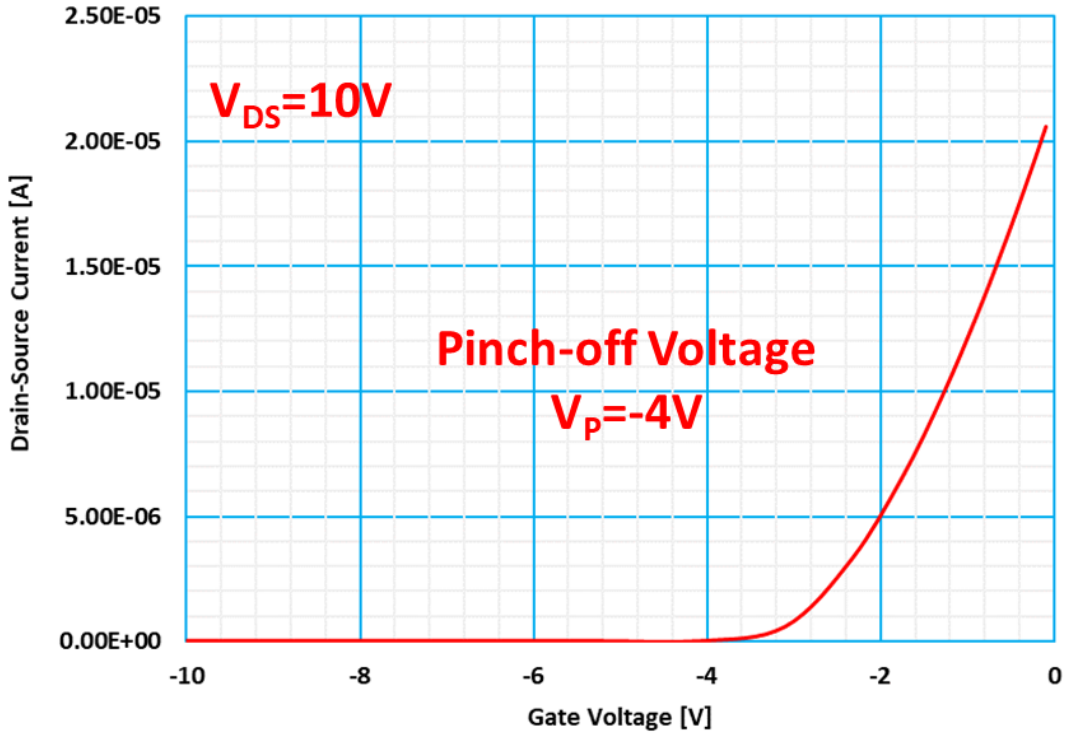


Fig. 3.28 Forward I_D-V_{GS} characteristics of lateral RESURF 4H-SiC JFET using epi wafer design 2 (unit cell with Z direction dimension of 1 um)

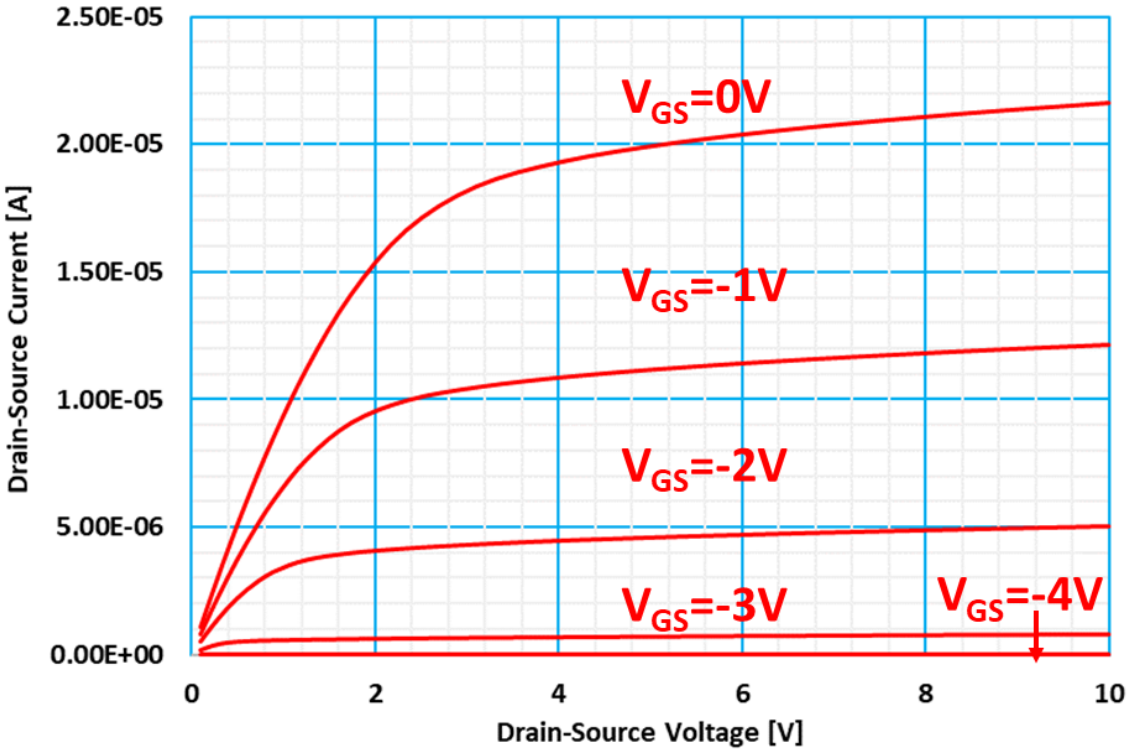


Fig. 3.29 Forward I_D-V_{DS} characteristics of lateral RESURF 4H-SiC JFET using epi wafer design 2 (unit cell with Z direction dimension of 1 um)

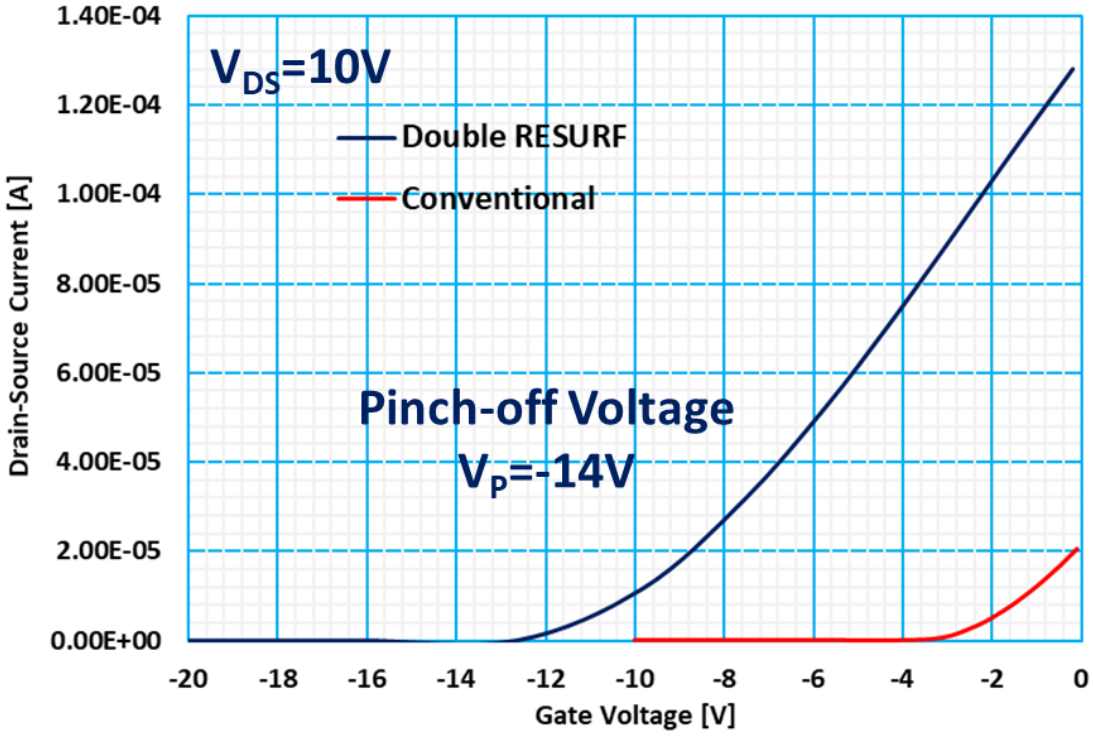


Fig. 3.30 Forward I_D-V_{GS} characteristics of lateral double-RESURF 4H-SiC JFET in comparison with conventional design (unit cell with Z direction dimension of 1 um)

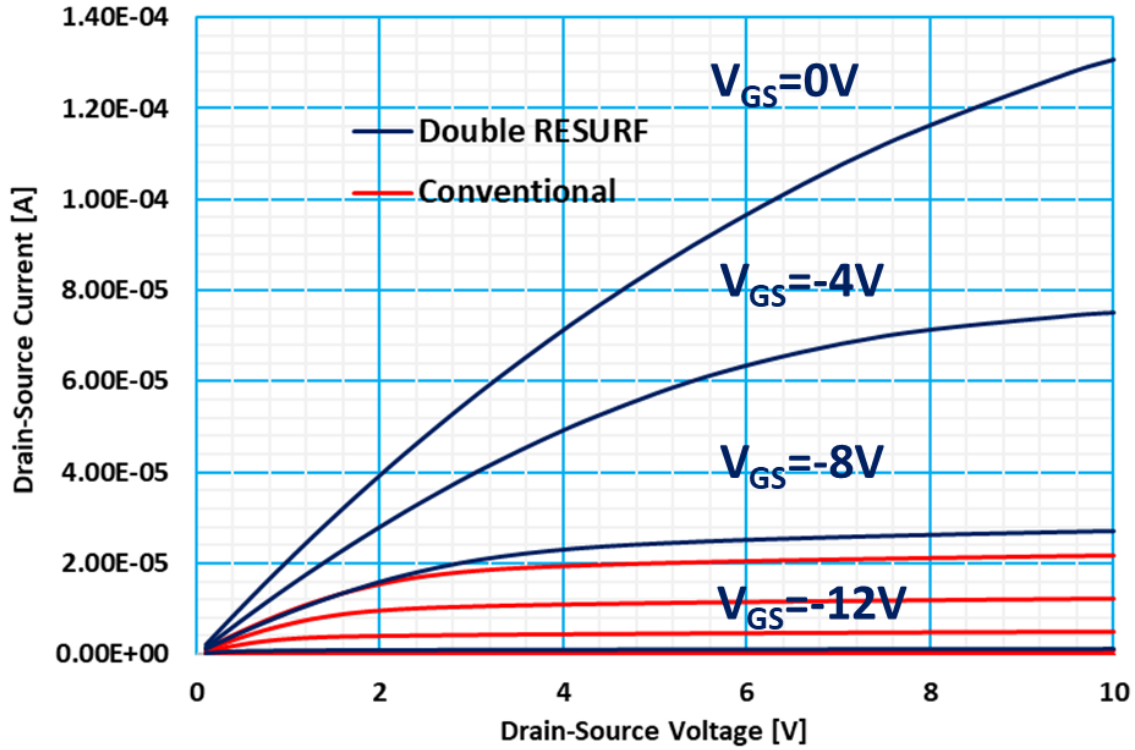


Fig. 3.31 Forward I_D-V_{DS} characteristics of lateral double-RESURF 4H-SiC JFET in comparison with conventional design (unit cell with Z direction dimension of 1 um)

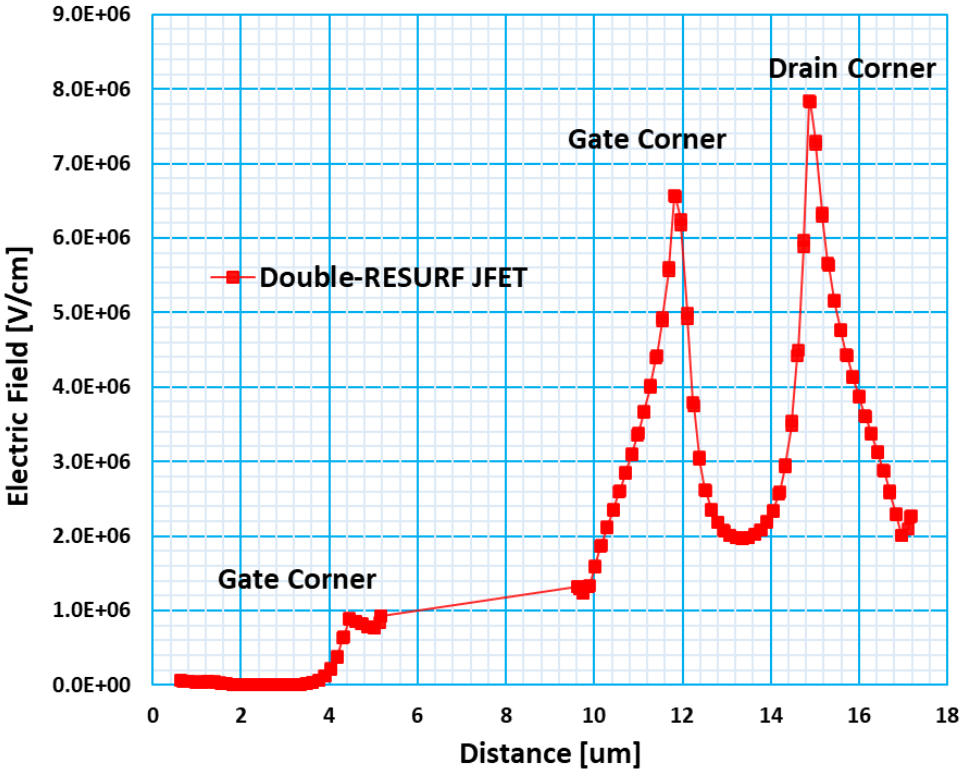


Fig. 3.32 Surface electric field cut of lateral double-RESURF 4H-SiC JFET

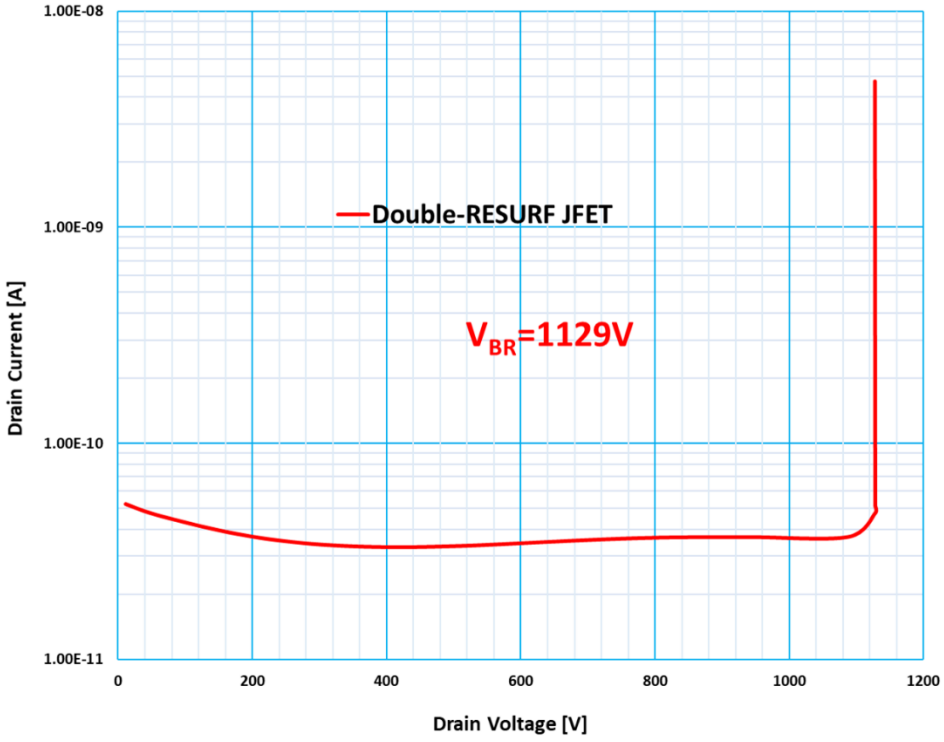


Fig. 3.33 Breakdown voltage simulation of lateral double-RESURF 4H-SiC JFET

3.6.1 Disadvantage of Double RESURF JFET Structure over Conventional RESURF JFET

Although double RESURF structure offers advantages such as increased charge in the N^- drift region for better on-resistance performance, this increased charge can cause difficulty for the gate to close in JFET, which is also seen with MESFET structure. As shown in Figure 3.30, the increased doping concentration in the N^- drift layer from the optimum double RESURF design causes a significant increase in the pinch-off voltage, indicating difficulty in depleting the channel. For this reason, additional design modification to the gate, such as shallow recess etch or vertical mesa etched gate structure, is necessary for double RESURF JFET structure.

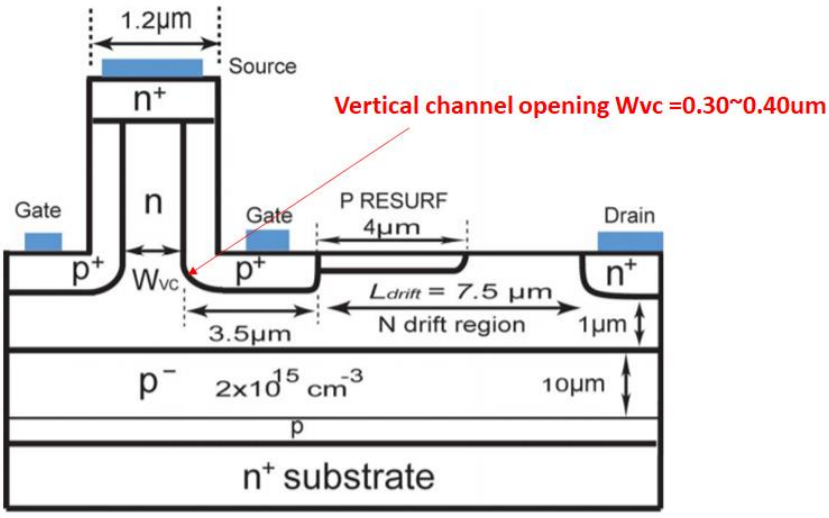


Fig. 3.34 Cross-sectional view of the 4H- SiC normally off VC-LJFET with RESURF structure [16]

Figure 3.34 illustrates an example of double RESURF JFET structure with double gate vertical channel structure for normally-off operation. It is worth noting that this device has a vertical channel opening of 0.30um~0.40um, which fully depletes by the gate to source potential with no applied voltage. This design is popular as conventional normally-on JFETs, despite their excellent on-resistance performance, are not accepted by the market due to system safety issues. Normally-off JFETs, on the other hand, require narrow and relatively low doping at the channel to ensure the normally-off function, thus sacrificing the on-state performance.

3.7 Photolithography mask design and layout

The mask layout of the designed lateral RESURF 4H-SiC Schottky barrier diodes and MESFETs device consists of 7 layers (i.e., Isolation, Recess Etch/P Implant, N Implant, Contact Open, Ohmic, Schottky, and Conduction Metal). Layout variation consist of 2 types of layout (i.e., finger type and circular type) for both the lateral RESURF Schottky diodes and the lateral RESURF MESFETs. Split variations have been made in the mask layout for the drift region length, field plate length, finger length, finger numbers, and contact width to further confirm optimization of device design.

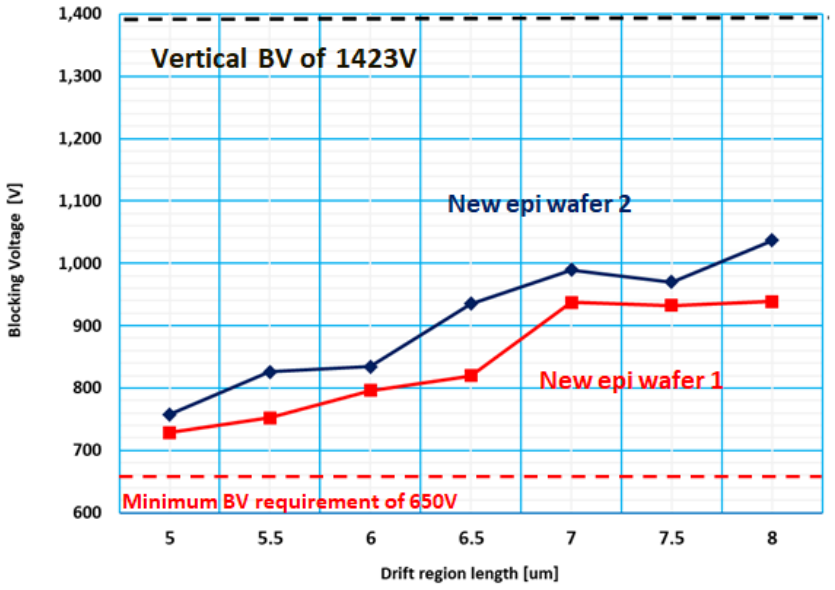


Fig. 3.35 Simulation result of breakdown voltage in relationship with drift region length variance

Table 3.2 Design splits included in the mask layout

Device type /Layout type	Targeted breakdown voltage	Drift region length	Necessary field plate length
Schottky diode/Finger and Circular type layout	1000V	10um	3.5um
	900V	9um	3.0um
	800V	8um	2.5um
	700V	7um	2.0um
	600V	6um	1.5um
	500V	5um	1.5um
MESFETs/Finger and Circular type layout	1000V	10um	3.5um
	900V	9um	3.0um
	800V	8um	2.5um
	700V	7um	2.0um
	600V	6um	1.5um
	500V	5um	1.5um

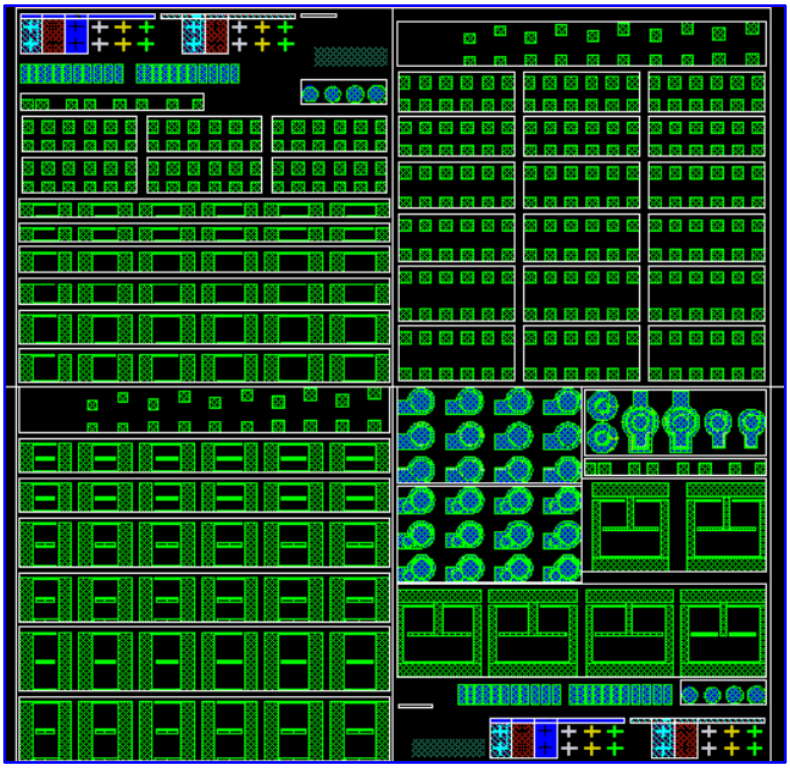


Fig. 3.36 Reticle layout design for Lateral RESURF 4H-SiC Schottky diode, MESFET, PIN diode and JFET

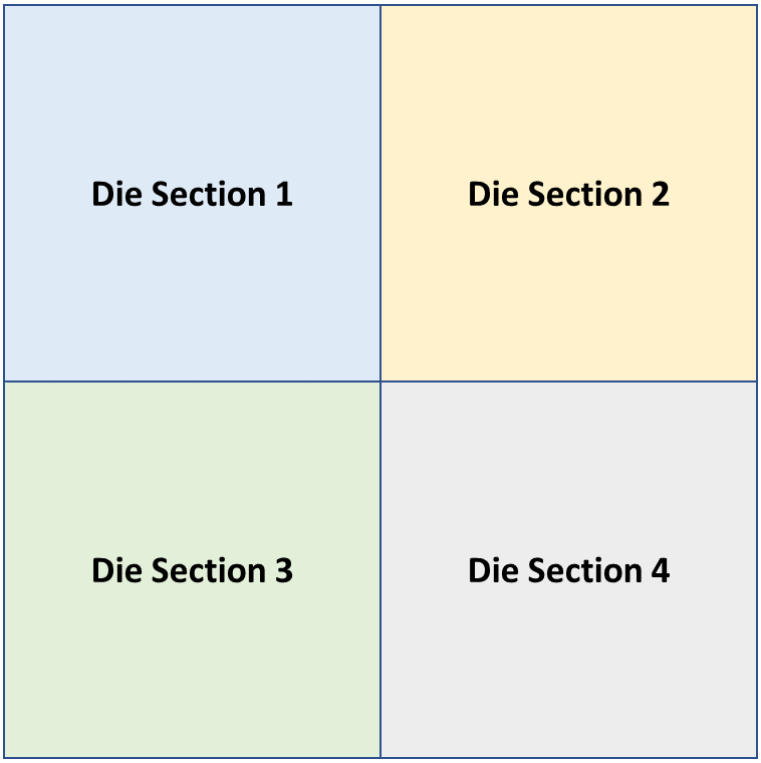


Fig. 3.37 Die shot section classification for cell identification

List of cell variation (name /description) in final photolithography mask

Section		Cell Module Name	Description
Die Section 1	Test Patterns	Alingment_Key_Isolation3rd	Standard Alingment Marker for MA6 (Against Isolation)
		Alingment_Key_Contact3rd	Standard Alingment Marker for MA6 (Against Contact)
		3rd_Litho_Resolution	Resolution pattern (5um, 4um, 3um 2um)
		3rd_Litho_L_Bar	L Bar resolution pattern (5um, 4um, 3um 2um)
		TLM_Line_Test_Pattern	Contact resistance measurement for ohmic contact
		TLM_Line_Test_Pattern_schottky	Contact resistance measurement for schottky contact
		VerticalBreakdownPattern	Vertical P-/N- Junction breakdown evaluation pattern
		Isolation_Pattern	Isolation voltage breakdown evaluation pattern (50um, 100um, 150um, 200)
	3 Finger Schottky/PIN diode (50um)	3FD50W50LD150LP8CV1	50um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		3FD50W60LD150LP8CV1	50um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		3FD50W70LD200LP8CV1	50um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		3FD50W80LD250LP8CV1	50um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		3FD50W90LD300LP8CV1	50um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		3FD50W100LD350LP8CV1	50um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		3FD50W50LD150LP8CV2	50um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		3FD50W60LD150LP8CV2	50um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		3FD50W70LD200LP8CV2	50um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		3FD50W80LD250LP8CV2	50um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		3FD50W90LD300LP8CV2	50um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		3FD50W100LD350LP8CV2	50um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	2 Finger Schottky/PIN diode (50um)	2FD50W50LD150LP8CV1	50um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		2FD50W60LD150LP8CV1	50um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		2FD50W70LD200LP8CV1	50um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		2FD50W80LD250LP8CV1	50um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		2FD50W90LD300LP8CV1	50um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		2FD50W100LD350LP8CV1	50um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		2FD50W50LD150LP8CV2	50um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		2FD50W60LD150LP8CV2	50um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		2FD50W70LD200LP8CV2	50um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		2FD50W80LD250LP8CV2	50um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		2FD50W90LD300LP8CV2	50um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		2FD50W100LD350LP8CV2	50um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	1 Finger Schottky/PIN diode (50um)	1FD50W50LD150LP8CV1	50um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		1FD50W60LD150LP8CV1	50um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		1FD50W70LD200LP8CV1	50um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		1FD50W80LD250LP8CV1	50um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		1FD50W90LD300LP8CV1	50um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		1FD50W100LD350LP8CV1	50um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		1FD50W50LD150LP8CV2	50um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		1FD50W60LD150LP8CV2	50um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		1FD50W70LD200LP8CV2	50um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		1FD50W80LD250LP8CV2	50um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		1FD50W90LD300LP8CV2	50um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		1FD50W100LD350LP8CV2	50um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	10 Finger Schottky/PIN diode	10FD100W50LD150LP8CV1	100um length 10 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		10FD100W60LD150LP8CV1	100um length 10 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		10FD100W70LD200LP8CV1	100um length 10 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		10FD100W80LD250LP8CV1	100um length 10 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		10FD100W90LD300LP8CV1	100um length 10 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		10FD100W100LD350LP8CV1	100um length 10 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		10FD100W50LD150LP8CV2	100um length 10 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		10FD100W60LD150LP8CV2	100um length 10 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		10FD100W70LD200LP8CV2	100um length 10 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		10FD100W80LD250LP8CV2	100um length 10 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		10FD100W90LD300LP8CV2	100um length 10 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		10FD100W100LD350LP8CV2	100um length 10 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
		10FD200W50LD150LP8CV1	200um length 10 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		10FD200W60LD150LP8CV1	200um length 10 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		10FD200W70LD200LP8CV1	200um length 10 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		10FD200W80LD250LP8CV1	200um length 10 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		10FD200W90LD300LP8CV1	200um length 10 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		10FD200W100LD350LP8CV1	200um length 10 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		10FD200W50LD150LP8CV2	200um length 10 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		10FD200W60LD150LP8CV2	200um length 10 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		10FD200W70LD200LP8CV2	200um length 10 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		10FD200W80LD250LP8CV2	200um length 10 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		10FD200W90LD300LP8CV2	200um length 10 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		10FD200W100LD350LP8CV2	200um length 10 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
		10FD300W50LD150LP8CV1	300um length 10 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		10FD300W60LD150LP8CV1	300um length 10 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		10FD300W70LD200LP8CV1	300um length 10 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		10FD300W80LD250LP8CV1	300um length 10 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		10FD300W90LD300LP8CV1	300um length 10 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		10FD300W100LD350LP8CV1	300um length 10 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		10FD300W50LD150LP8CV2	300um length 10 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		10FD300W60LD150LP8CV2	300um length 10 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		10FD300W70LD200LP8CV2	300um length 10 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		10FD300W80LD250LP8CV2	300um length 10 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		10FD300W90LD300LP8CV2	300um length 10 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		10FD300W100LD350LP8CV2	300um length 10 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)

List of cell variation (name /description) in final photolithography mask (continue)

Section		Cell Module Name	Description
Die Section 2	3 Finger Schottky/PIN diode (100um)	3FD100W50LD150LP8CV1	100um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		3FD100W60LD150LP8CV1	100um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		3FD100W70LD200LP8CV1	100um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		3FD100W80LD250LP8CV1	100um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		3FD100W90LD300LP8CV1	100um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		3FD100W100LD350LP8CV1	100um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		3FD100W50LD150LP8CV2	100um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		3FD100W60LD150LP8CV2	100um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		3FD100W70LD200LP8CV2	100um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		3FD100W80LD250LP8CV2	100um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		3FD100W90LD300LP8CV2	100um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		3FD100W100LD350LP8CV2	100um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	2 Finger Schottky/PIN diode (100um)	2FD100W50LD150LP8CV1	100um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		2FD100W60LD150LP8CV1	100um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		2FD100W70LD200LP8CV1	100um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		2FD100W80LD250LP8CV1	100um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		2FD100W90LD300LP8CV1	100um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		2FD100W100LD350LP8CV1	100um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		2FD100W50LD150LP8CV2	100um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		2FD100W60LD150LP8CV2	100um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		2FD100W70LD200LP8CV2	100um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		2FD100W80LD250LP8CV2	100um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		2FD100W90LD300LP8CV2	100um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		2FD100W100LD350LP8CV2	100um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	1 Finger Schottky/PIN diode (100um)	1FD100W50LD150LP8CV1	100um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		1FD100W60LD150LP8CV1	100um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		1FD100W70LD200LP8CV1	100um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		1FD100W80LD250LP8CV1	100um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		1FD100W90LD300LP8CV1	100um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		1FD100W100LD350LP8CV1	100um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		1FD100W50LD150LP8CV2	100um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		1FD100W60LD150LP8CV2	100um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		1FD100W70LD200LP8CV2	100um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		1FD100W80LD250LP8CV2	100um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		1FD100W90LD300LP8CV2	100um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		1FD100W100LD350LP8CV2	100um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	3 Finger Schottky/PIN diode (200um)	3FD100W50LD150LP8CV1	100um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		3FD100W60LD150LP8CV1	100um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		3FD100W70LD200LP8CV1	100um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		3FD100W80LD250LP8CV1	100um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		3FD100W90LD300LP8CV1	100um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		3FD100W100LD350LP8CV1	100um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		3FD100W50LD150LP8CV2	100um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		3FD100W60LD150LP8CV2	100um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		3FD100W70LD200LP8CV2	100um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		3FD100W80LD250LP8CV2	100um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		3FD100W90LD300LP8CV2	100um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		3FD100W100LD350LP8CV2	100um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	2 Finger Schottky/PIN diode (200um)	2FD100W50LD150LP8CV1	100um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		2FD100W60LD150LP8CV1	100um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		2FD100W70LD200LP8CV1	100um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		2FD100W80LD250LP8CV1	100um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		2FD100W90LD300LP8CV1	100um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		2FD100W100LD350LP8CV1	100um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		2FD100W50LD150LP8CV2	100um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		2FD100W60LD150LP8CV2	100um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		2FD100W70LD200LP8CV2	100um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		2FD100W80LD250LP8CV2	100um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		2FD100W90LD300LP8CV2	100um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		2FD100W100LD350LP8CV2	100um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	1 Finger Schottky/PIN diode (200um)	1FD100W50LD150LP8CV1	100um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		1FD100W60LD150LP8CV1	100um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		1FD100W70LD200LP8CV1	100um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		1FD100W80LD250LP8CV1	100um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		1FD100W90LD300LP8CV1	100um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		1FD100W100LD350LP8CV1	100um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		1FD100W50LD150LP8CV2	100um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		1FD100W60LD150LP8CV2	100um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		1FD100W70LD200LP8CV2	100um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		1FD100W80LD250LP8CV2	100um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		1FD100W90LD300LP8CV2	100um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		1FD100W100LD350LP8CV2	100um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)

List of cell variation (name /description) in final photolithography mask (continue)

Die Section 2 (Continue)	3 Finger Schottky/PIN diode (300um)	3FD100W50LD150LP8CV1	100um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		3FD100W60LD150LP8CV1	100um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		3FD100W70LD200LP8CV1	100um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		3FD100W80LD250LP8CV1	100um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		3FD100W90LD300LP8CV1	100um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		3FD100W100LD350LP8CV1	100um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		3FD100W50LD150LP8CV2	100um length 3 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		3FD100W60LD150LP8CV2	100um length 3 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		3FD100W70LD200LP8CV2	100um length 3 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		3FD100W80LD250LP8CV2	100um length 3 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		3FD100W90LD300LP8CV2	100um length 3 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		3FD100W100LD350LP8CV2	100um length 3 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	2 Finger Schottky/PIN diode (300um)	2FD100W50LD150LP8CV1	100um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		2FD100W60LD150LP8CV1	100um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		2FD100W70LD200LP8CV1	100um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		2FD100W80LD250LP8CV1	100um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		2FD100W90LD300LP8CV1	100um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		2FD100W100LD350LP8CV1	100um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		2FD100W50LD150LP8CV2	100um length 2 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		2FD100W60LD150LP8CV2	100um length 2 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		2FD100W70LD200LP8CV2	100um length 2 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		2FD100W80LD250LP8CV2	100um length 2 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		2FD100W90LD300LP8CV2	100um length 2 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		2FD100W100LD350LP8CV2	100um length 2 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	1 Finger Schottky/PIN diode (300um)	1FD100W50LD150LP8CV1	100um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		1FD100W60LD150LP8CV1	100um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		1FD100W70LD200LP8CV1	100um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		1FD100W80LD250LP8CV1	100um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		1FD100W90LD300LP8CV1	100um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		1FD100W100LD350LP8CV1	100um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		1FD100W50LD150LP8CV2	100um length 1 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		1FD100W60LD150LP8CV2	100um length 1 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		1FD100W70LD200LP8CV2	100um length 1 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		1FD100W80LD250LP8CV2	100um length 1 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		1FD100W90LD300LP8CV2	100um length 1 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		1FD100W100LD350LP8CV2	100um length 1 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	MESFET/JFETs	3FM100W50LD150LP8CV1	100um length 3 finger MESFET/JFET with 5um drift length 1.5um FP
		3FM100W60LD150LP8CV1	100um length 3 finger MESFET/JFET with 6um drift length 1.5um FP
		3FM100W70LD200LP8CV1	100um length 3 finger MESFET/JFET with 7um drift length 2.0um FP
		3FM100W80LD250LP8CV1	100um length 3 finger MESFET/JFET with 8um drift length 2.5um FP
		3FM100W90LD300LP8CV1	100um length 3 finger MESFET/JFET with 9um drift length 3.0um FP
		3FM100W100LD350LP8CV1	100um length 3 finger MESFET/JFET with 10um drift length 3.5um FP
		3FM200W50LD150LP8CV1	200um length 3 finger MESFET/JFET with 5um drift length 1.5um FP
		3FM200W60LD150LP8CV1	200um length 3 finger MESFET/JFET with 6um drift length 1.5um FP
		3FM200W70LD200LP8CV1	200um length 3 finger MESFET/JFET with 7um drift length 2.0um FP
		3FM200W80LD250LP8CV1	200um length 3 finger MESFET/JFET with 8um drift length 2.5um FP
		3FM200W90LD300LP8CV1	200um length 3 finger MESFET/JFET with 9um drift length 3.0um FP
		3FM200W100LD350LP8CV1	200um length 3 finger MESFET/JFET with 10um drift length 3.5um FP

List of cell variation (name /description) in final photolithography mask (continue)

Section		Cell Module Name	Description
Die Section 3	MESFET/JFETs	3FM100W50LD150LP8CV1	100um length 3 finger MESFET/JFET with 5um drift length 1.5um FP
		3FM100W60LD150LP8CV1	100um length 3 finger MESFET/JFET with 6um drift length 1.5um FP
		3FM100W70LD200LP8CV1	100um length 3 finger MESFET/JFET with 7um drift length 2.0um FP
		3FM100W80LD250LP8CV1	100um length 3 finger MESFET/JFET with 8um drift length 2.5um FP
		3FM100W90LD300LP8CV1	100um length 3 finger MESFET/JFET with 9um drift length 3.0um FP
		3FM100W100LD350LP8CV1	100um length 3 finger MESFET/JFET with 10um drift length 3.5um FP
		3FM200W50LD150LP8CV1	200um length 3 finger MESFET/JFET with 5um drift length 1.5um FP
		3FM200W60LD150LP8CV1	200um length 3 finger MESFET/JFET with 6um drift length 1.5um FP
		3FM200W70LD200LP8CV1	200um length 3 finger MESFET/JFET with 7um drift length 2.0um FP
		3FM200W80LD250LP8CV1	200um length 3 finger MESFET/JFET with 8um drift length 2.5um FP
		3FM200W90LD300LP8CV1	200um length 3 finger MESFET/JFET with 9um drift length 3.0um FP
		3FM200W100LD350LP8CV1	200um length 3 finger MESFET/JFET with 10um drift length 3.5um FP
	20 Finger Schottky/PIN diode	20FD100W50LD150LP8CV1	100um length 20 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		20FD100W60LD150LP8CV1	100um length 20 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		20FD100W70LD200LP8CV1	100um length 20 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		20FD100W80LD250LP8CV1	100um length 20 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		20FD100W90LD300LP8CV1	100um length 20 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		20FD100W100LD350LP8CV1	100um length 20 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		20FD100W50LD150LP8CV2	100um length 20 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		20FD100W60LD150LP8CV2	100um length 20 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		20FD100W70LD200LP8CV2	100um length 20 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		20FD100W80LD250LP8CV2	100um length 20 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		20FD100W90LD300LP8CV2	100um length 20 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		20FD100W100LD350LP8CV2	100um length 20 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
		20FD200W50LD150LP8CV1	200um length 20 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		20FD200W60LD150LP8CV1	200um length 20 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		20FD200W70LD200LP8CV1	200um length 20 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		20FD200W80LD250LP8CV1	200um length 20 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		20FD200W90LD300LP8CV1	200um length 20 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		20FD200W100LD350LP8CV1	200um length 20 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		20FD200W50LD150LP8CV2	200um length 20 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		20FD200W60LD150LP8CV2	200um length 20 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		20FD200W70LD200LP8CV2	200um length 20 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		20FD200W80LD250LP8CV2	200um length 20 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		20FD200W90LD300LP8CV2	200um length 20 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		20FD200W100LD350LP8CV2	200um length 20 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
		20FD300W50LD150LP8CV1	300um length 20 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		20FD300W60LD150LP8CV1	300um length 20 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		20FD300W70LD200LP8CV1	300um length 20 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		20FD300W80LD250LP8CV1	300um length 20 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		20FD300W90LD300LP8CV1	300um length 20 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		20FD300W100LD350LP8CV1	300um length 20 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		20FD300W50LD150LP8CV2	300um length 20 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer cathode)
		20FD300W60LD150LP8CV2	300um length 20 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		20FD300W70LD200LP8CV2	300um length 20 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		20FD300W80LD250LP8CV2	300um length 20 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer cathode)
		20FD300W90LD300LP8CV2	300um length 20 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		20FD300W100LD350LP8CV2	300um length 20 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)

List of cell variation (name /description) in final photolithography mask (continue)

Section		Cell Module Name	Description
Die Section 4	Test Patterns	Alingment_Key_Isolation3rd	Standard Alingment Marker for MA6 (Against Isolation)
		Alingment_Key_Contact3rd	Standard Alingment Marker for MA6 (Against Contact)
		3rd_Litho_Resolution	Resolution pattern (5um, 4um, 3um 2um)
		3rd_Litho_L_Bar	L Bar resolution pattern (5um, 4um, 3um 2um)
		TLM_Line_Test_Pattern	Contact resistance measurement for ohmic contact
		TLM_Line_Test_Pattern_schottky	Contact resistance measurement for schottky contact
		VerticalBreakdownPattern	Vertical P-/N- Junction breakdown evaluation pattern
		Isolation_Pattern	Isolation voltage breakdown evaluation pattern (50um, 100um, 150um, 200)
	40 Finger Schottky/PIN diode	40FD300W50LD150LP8CV1	300um length 40 finger Schottky/PIN diode with 5um drift length 1.5um FP (Outer anode)
		40FD300W60LD150LP8CV1	300um length 40 finger Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		40FD300W70LD200LP8CV1	300um length 40 finger Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		40FD300W80LD250LP8CV1	300um length 40 finger Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		40FD300W90LD300LP8CV1	300um length 40 finger Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		40FD300W100LD350LP8CV1	300um length 40 finger Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
	Cicular Schottky/PIN diode	CircularDiode50LD125LPV1	Circular Schottky/PIN diode with 5um drift length 1.25um FP (Outer anode)
		CircularDiode60LD150LPV1	Circular Schottky/PIN diode with 6um drift length 1.5um FP (Outer anode)
		CircularDiode70LD200LPV1	Circular Schottky/PIN diode with 7um drift length 2.0um FP (Outer anode)
		CircularDiode80LD250LPV1	Circular Schottky/PIN diode with 8um drift length 2.5um FP (Outer anode)
		CircularDiode90LD300LPV1	Circular Schottky/PIN diode with 9um drift length 3.0um FP (Outer anode)
		CircularDiode100LD350LPV1	Circular Schottky/PIN diode with 10um drift length 3.5um FP (Outer anode)
		CircularDiode50LD125LPV2	Circular Schottky/PIN diode with 5um drift length 1.25um FP (Outer cathode)
		CircularDiode60LD150LPV2	Circular Schottky/PIN diode with 6um drift length 1.5um FP (Outer cathode)
		CircularDiode70LD200LPV2	Circular Schottky/PIN diode with 7um drift length 2.0um FP (Outer cathode)
		CircularDiode80LD250LPV2	Circular Schottky/PIN diode with 8um drift length 2.5um FP (Outercathode)
		CircularDiode90LD300LPV2	Circular Schottky/PIN diode with 9um drift length 3.0um FP (Outer cathode)
		CircularDiode100LD350LPV2	Circular Schottky/PIN diode with 10um drift length 3.5um FP (Outer cathode)
	Cicular MESFET	Circular_MESFET_50LD125LPV1	Circular MESFET/JFET with 5um drift length 1.25um FP (Outer anode)
		Circular_MESFET_60LD150LPV1	Circular MESFET/JFET with 6um drift length 1.5um FP (Outer anode)
		Circular_MESFET_70LD200LPV1	Circular MESFET/JFET with 7um drift length 2.0um FP (Outer anode)
		Circular_MESFET_80LD250LPV1	Circular MESFET/JFET with 8um drift length 2.5um FP (Outer anode)
		Circular_MESFET_90LD300LPV1	Circular MESFET/JFET with 9um drift length 3.0um FP (Outer anode)
		Circular_MESFET_100LD350LPV1	Circular MESFET/JFET with 10um drift length 3.5um FP (Outer anode)
		Circular_MESFET_50LD125LPV1	Circular MESFET/JFET with 5um drift length 1.25um FP (Outer cathode)
		Circular_MESFET_60LD150LPV1	Circular MESFET/JFET with 6um drift length 1.5um FP (Outer cathode)
		Circular_MESFET_70LD200LPV1	Circular MESFET/JFET with 7um drift length 2.0um FP (Outer cathode)
		Circular_MESFET_80LD250LPV1	Circular MESFET/JFET with 8um drift length 2.5um FP (Outer cathode)
		Circular_MESFET_90LD300LPV1	Circular MESFET/JFET with 9um drift length 3.0um FP (Outer cathode)
		Circular_MESFET_100LD350LPV1	Circular MESFET/JFET with 10um drift length 3.5um FP (Outer cathode)
	3 Terminal	NPNBipolar	Vertical NPN bipolar test pattern
		PNPBipolar	Vertical PNP bipolar test pattern
		Thyristor	Vertical GTO thyristor test pattern

3.7.1 3, 2, 1 Finger Device Lateral Schottky Diode Variation (Mask Splits)

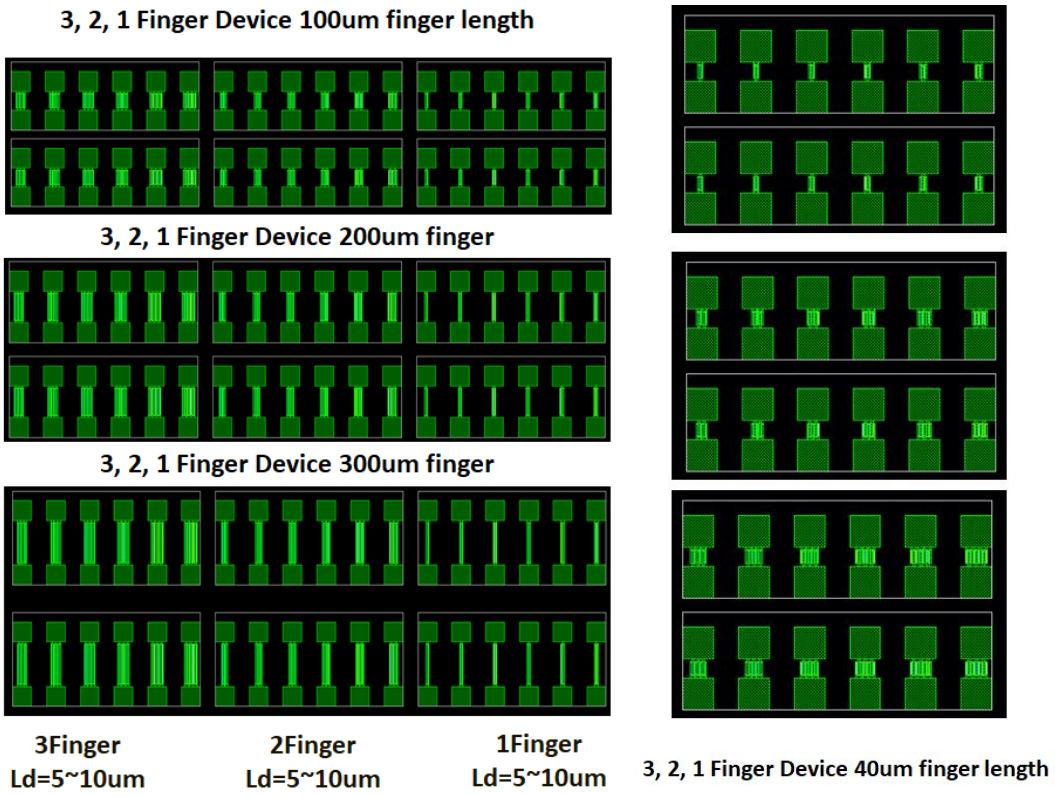


Fig. 3.38 3,2,1 Finger Device with varied drift region and finger length and 2 types of finger layout

3.7.2 Finger type MESFET (Mask Splits)

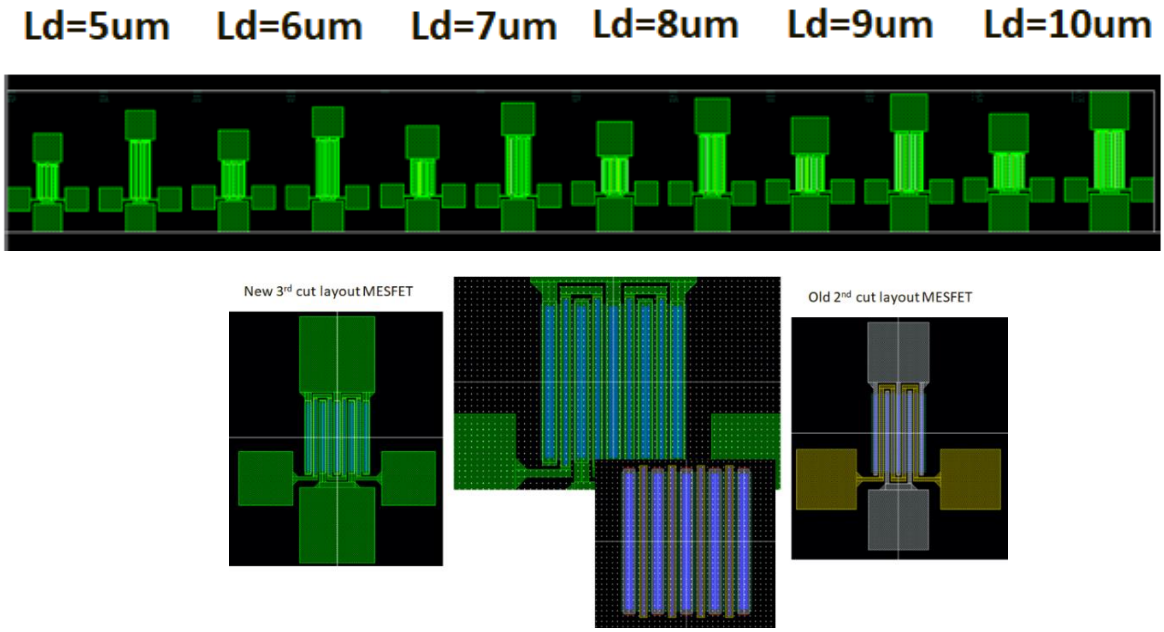


Fig. 3.39 2 Finger MESFETs with varied drift region and finger length

3.7.3 10 Finger Device Lateral Schottky Diode Variation (Mask Splits)

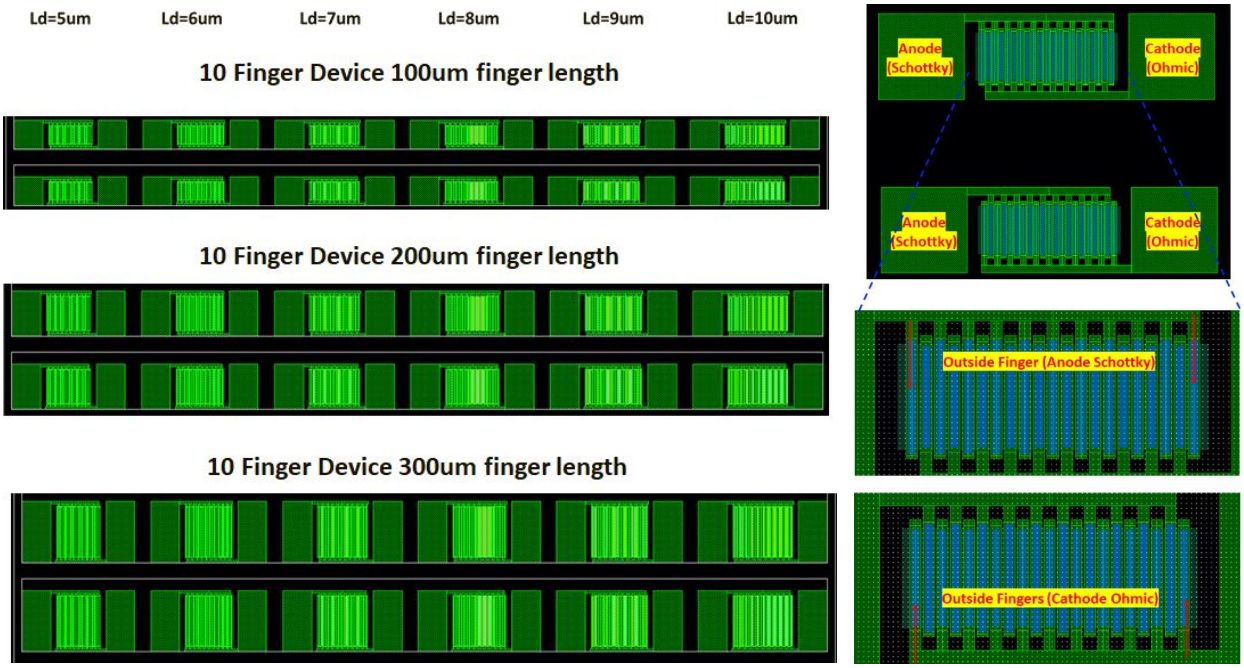


Fig. 3.40 10 Finger Device with varied drift region and finger length and 2 types of finger layout

3.7.4 20 Finger Device Lateral Schottky Diode Variation (Mask Splits)

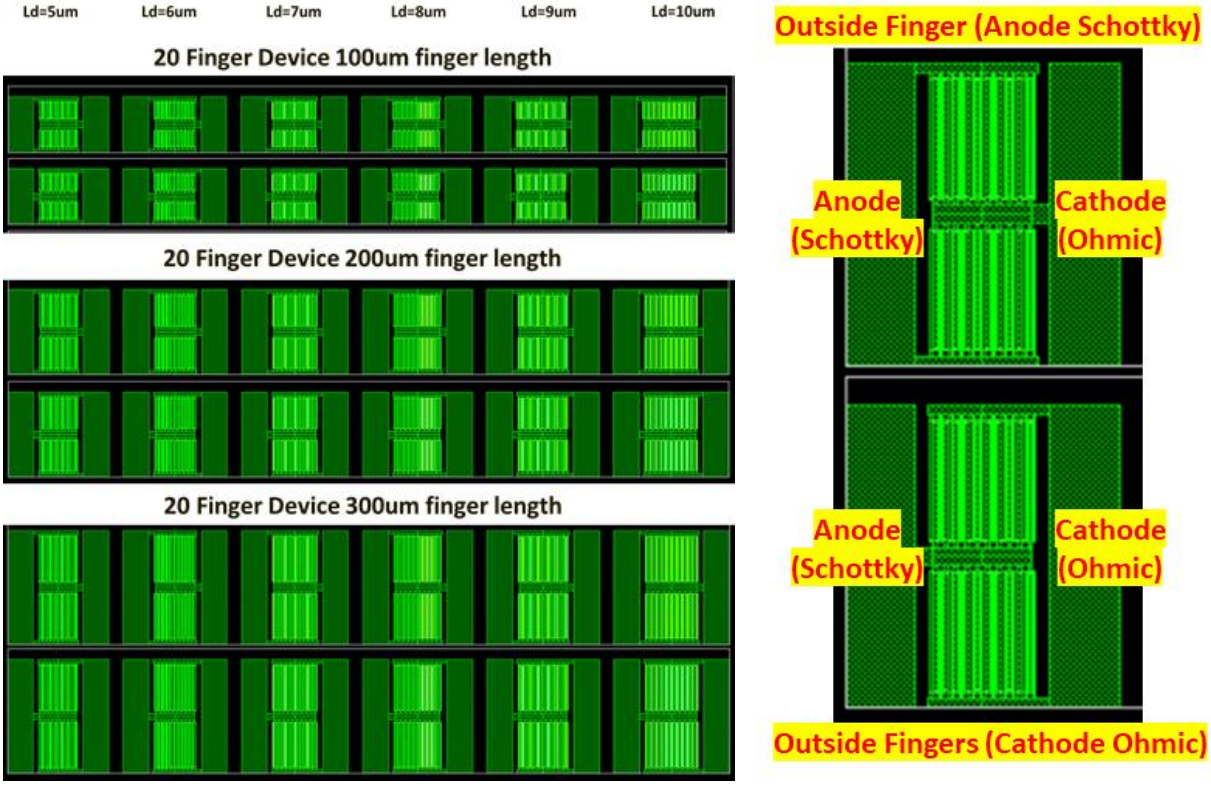


Fig. 3.41 20 Finger Device with varied drift region and finger length and 2 types of finger layout

3.7.5 40 Finger Device Lateral Schottky Diode Variation (Mask Splits)

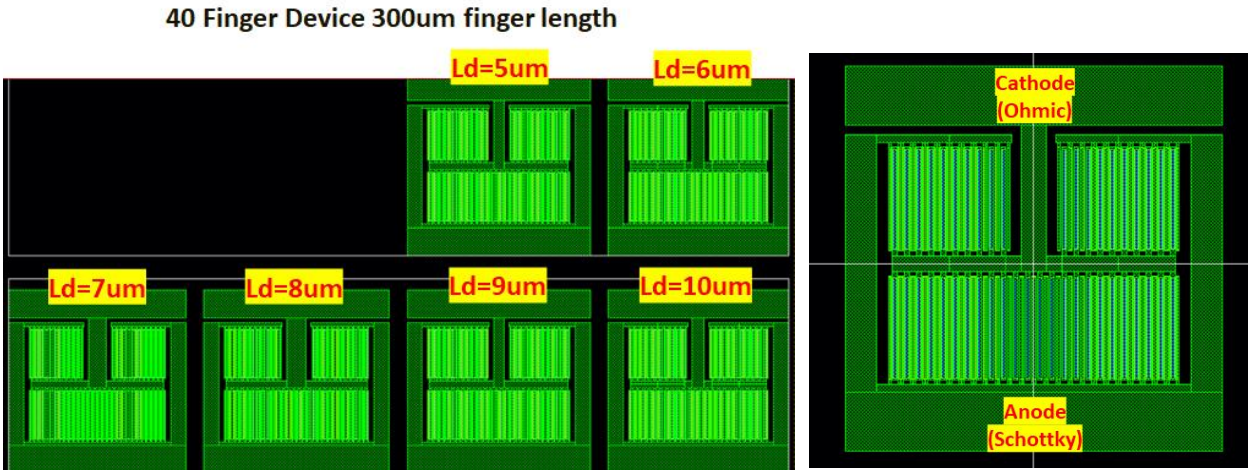


Fig. 3.42 40 Finger Device with varied drift region and finger length and pad layout explanation

3.7.6 Circular Lateral Schottky Diode and MESFET Variation (Mask Splits)

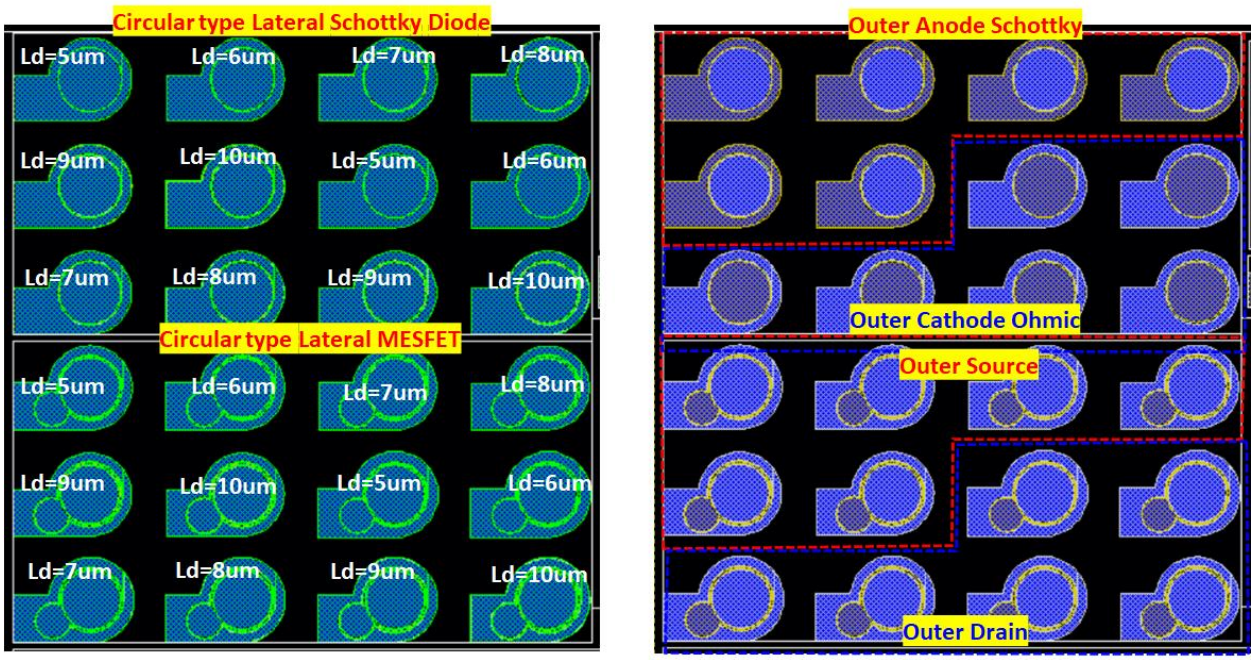


Fig. 3.43 Circular lateral Schottky diode and MESFET variation and pad layout explanation

3.7.7 Various Test Patterns

Bipolar test patterns

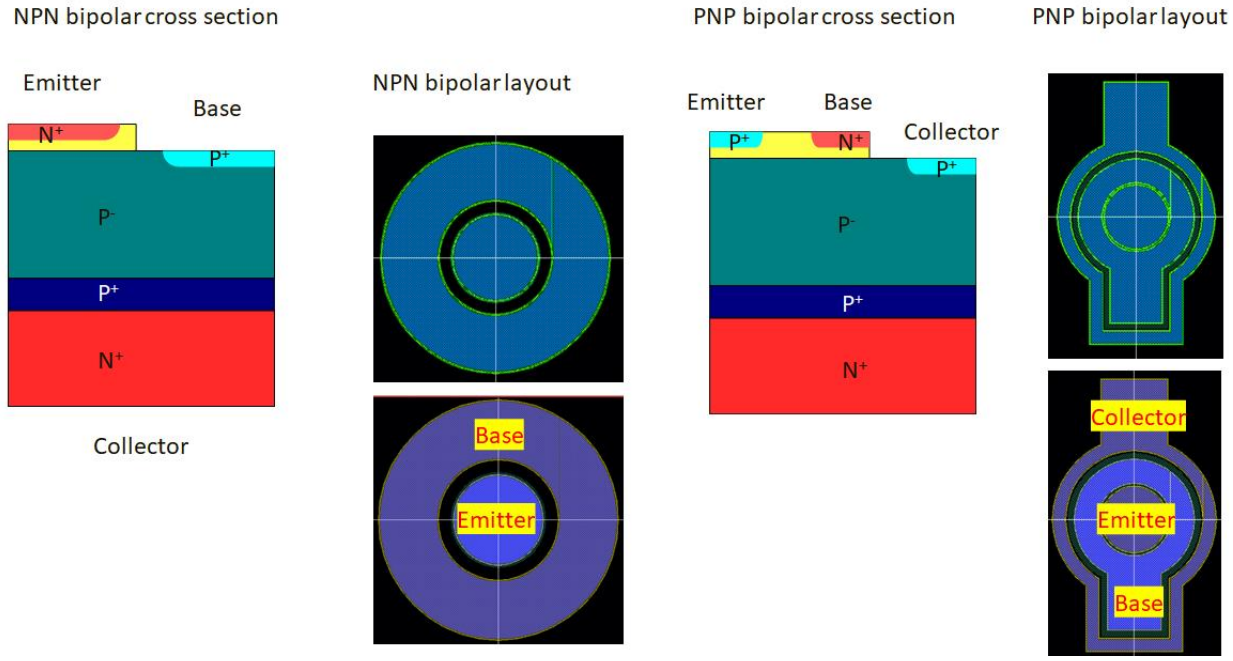


Fig. 3.44 Circular NPN and PNP bipolar test pattern

GTO (Gate Turn-off Thyristor) test patterns

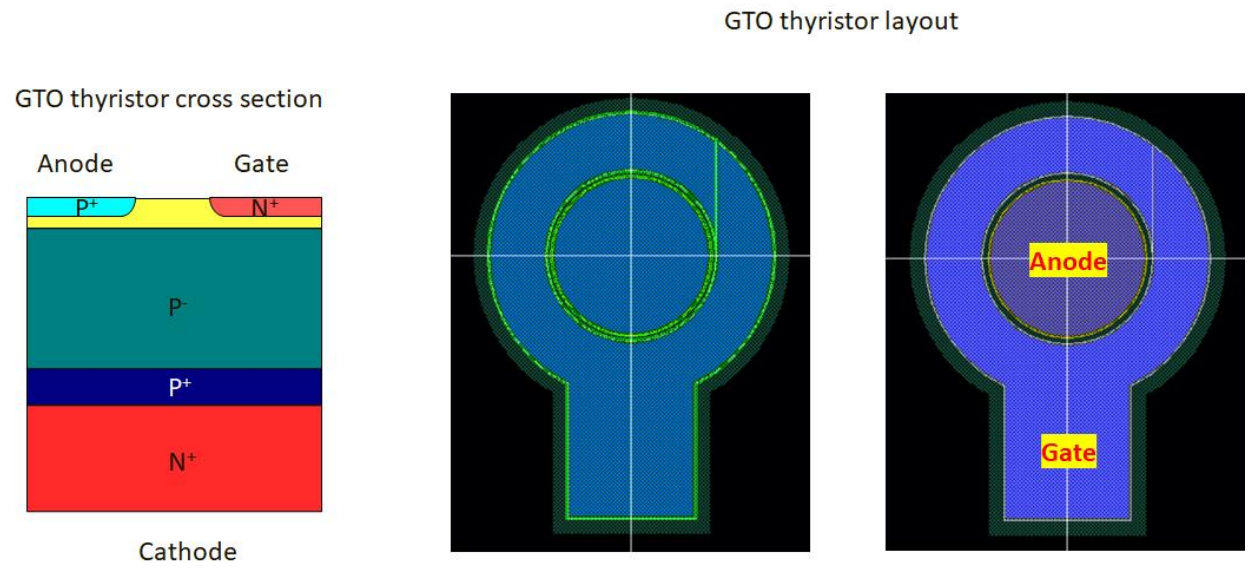
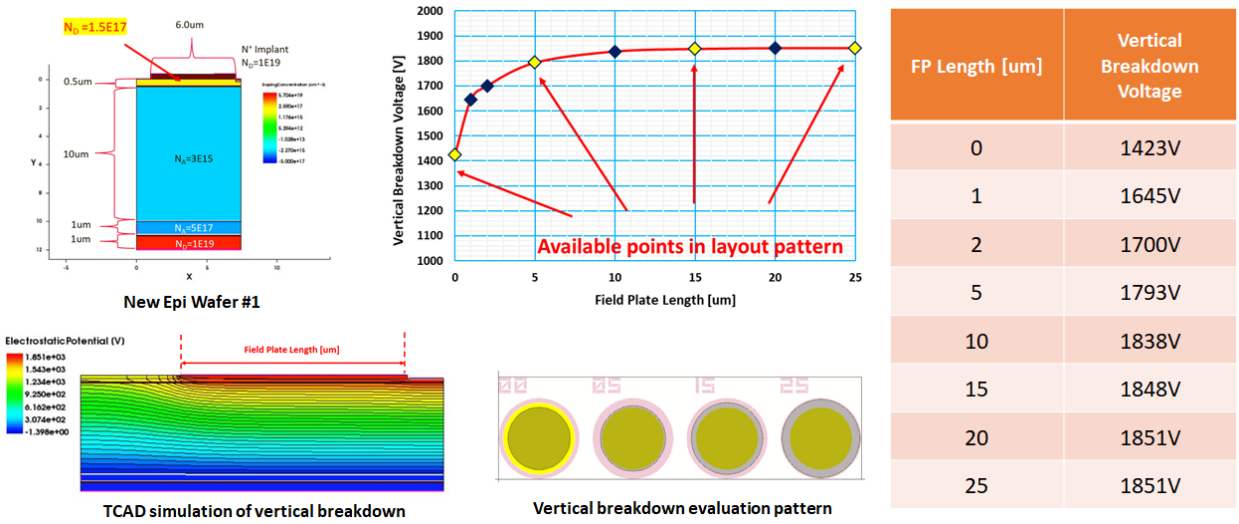


Fig. 3.45 Circular GTO (Gate turn-off thyristor) test pattern

Vertical breakdown test patterns



FP Length [um]	Vertical Breakdown Voltage
0	1423V
1	1645V
2	1700V
5	1793V
10	1838V
15	1848V
20	1851V
25	1851V

Fig. 3.46 Vertical breakdown test pattern

3.7.8 Alignment sequence of the 7 layer mask process

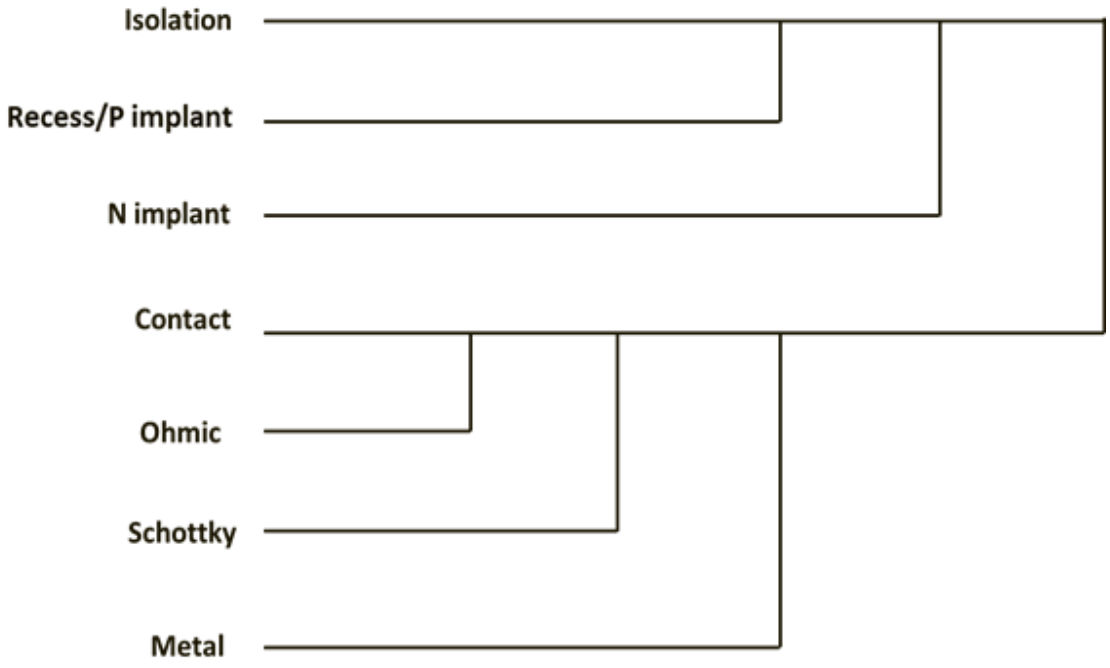
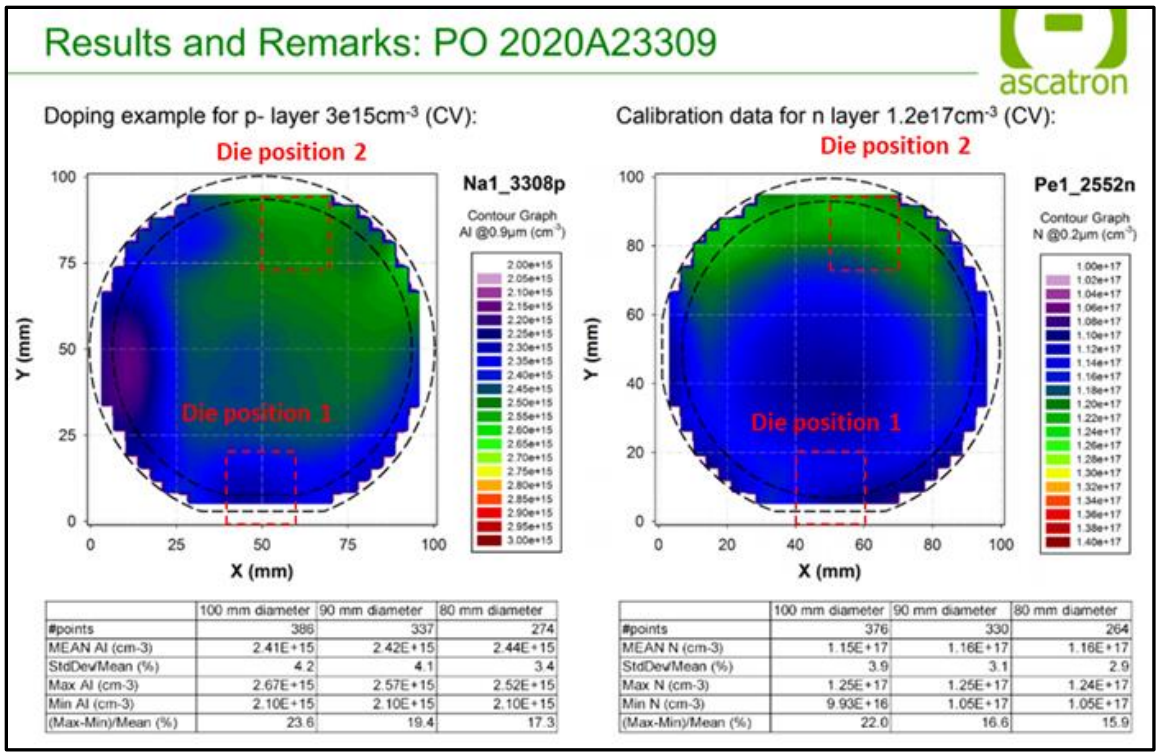


Fig. 3.47 Alignment sequence of the 7 layer mask process of lateral RESURF 4H-SiC Schottky barrier diodes and MESFETs

Chapter 4. Fabrication and Characterization of 4H-SiC Lateral RESURF Schottky Barrier Diode and MESFET

4.1 Epitaxial growth results from Ascatron AB

Ascatron AB is a power semiconductor device manufacturer company which also provides SiC epitaxy services to customers. Their epitaxy growth service offered, range in wafer size of 76mm, 100mm, 150 mm wafers (3-inch, 4-inch, and 6-inch size) with best in class uniformity. The *in-situ* doping concentration for both *n*-type and *p*-type range in order of 10^{14} ~10^{19} cm^{-3} with thickness ranging from 0.1um ~ 250um. Both *n*-type and *p*-type SiC epitaxial layers are grown using single wafer epitaxy LPE PE106, Aixtron VP508 in its individual CVD reactor, with doping concentration and thickness calibrated for each growth to form the multi-layer structure needed for lateral RESURF device.



	100 mm diameter	90 mm diameter	80 mm diameter
#points	386	337	274
MEAN Al (cm-3)	2.41E+15	2.42E+15	2.44E+15
StdDev/Mean (%)	4.2	4.1	3.4
Max Al (cm-3)	2.67E+15	2.57E+15	2.52E+15
Min Al (cm-3)	2.10E+15	2.10E+15	2.10E+15
(Max-Min)/Mean (%)	23.6	19.4	17.3

	100 mm diameter	90 mm diameter	80 mm diameter
#points	376	330	264
MEAN N (cm-3)	1.15E+17	1.16E+17	1.16E+17
StdDev/Mean (%)	3.9	3.1	2.9
Max N (cm-3)	1.25E+17	1.25E+17	1.24E+17
Min N (cm-3)	9.93E+16	1.05E+17	1.05E+17
(Max-Min)/Mean (%)	22.0	16.6	15.9

Fig. 4.1 Calibration C-V measurement data of doping concentration map for p^- epi layer (left) and n^- epi layer (right) grown on 4H-SiC substrate at Ascatron AB

Table 4.1 Expected device performance from doping concentration variance across the grown epi wafer

Design specification	Die position 1 (lightest doping from CV map)	Die position 2 (heaviest doping from CV map)
$Na= 3\times10^{15}cm^{-3}$	$Na=2.3\times10^{15}cm^{-3}$	$Na=2.6\times10^{15}cm^{-3}$
$N_d=1.2\times10^{17}cm^{-3}$	$N_d=1.12\times10^{17}cm^{-3}$	$N_d=1.24\times10^{17}cm^{-3}$
$V_{BR}=1043V$	$V_{BR}=1062V$ (Expected)	$V_{BR}=999.3V$ (Expected)
$R_{on}=11,115.82\Omega$	$R_{on}=11,598.16\Omega$	$R_{on}=10,945.14\Omega$

Figure 4.1 shows the calibration *C-V* measurement data of doping concentration map for p^- epi layer (left) and n^- epi layer (right) grown on 4H-SiC substrate at Ascatron AB. The delivery specification sheet guarantees tolerance of ± 50nm for thickness and ± $3\times10^{16}cm^{-3}$ for doping concentration of the grown epi layer. The *C-V* measurements indicates that the actual doping variance is much tighter and both guaranteed value (in red dotted line) and actual distribution (shaded region) are ploted with the blocking voltage and on-resistance with relataive integrated charge in the n^- epi layer in the bottom figure.

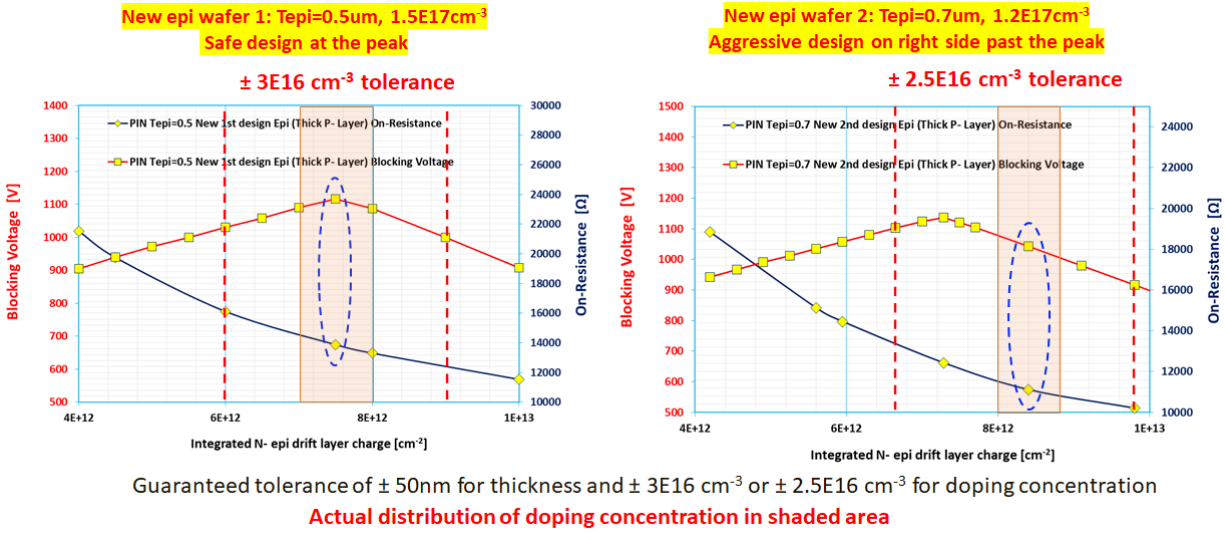
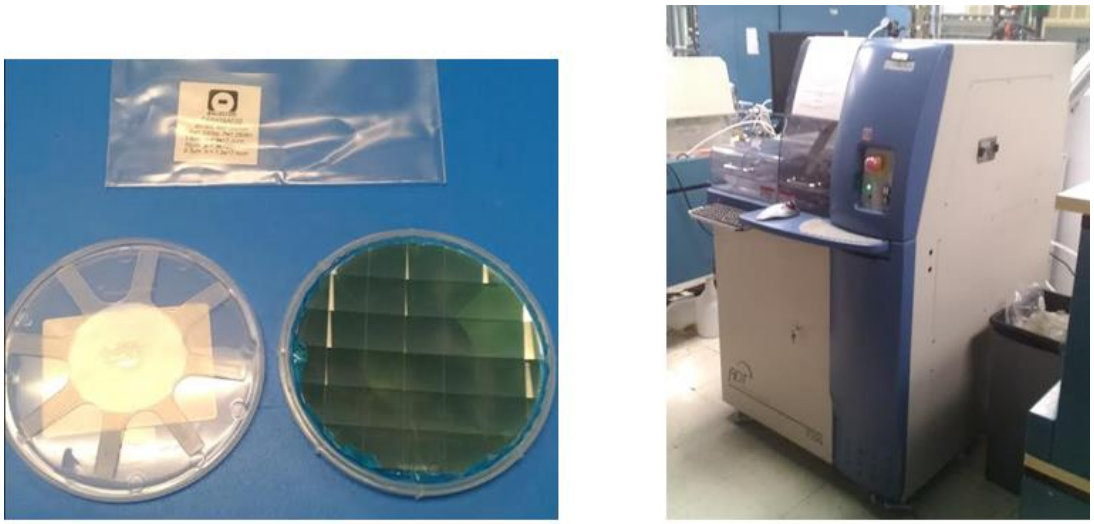


Fig. 4.2 Blocking voltage and on-resistance of lateral RESURF p-n diode cell in relationship with integrated N- drift layer charge with distribution of actual doping concentration of the C-V measurement

From table 4.1, it is confirmed that even the heaviest doped region in the grown epi wafer will have the capability to block 1kV and lightest doped region will still have a competitive forward on-resistance performance. From the delivery specification sheet and the calibration *C-V* measurement data from Ascatron AB, it can be said that the grown RESURF epitaxial wafer meets the required specificaiton and tolerance to deliver designed performance of the simulated lateral RESURF Schottky barrier diode and MESFETs.

4.2 SiC Wafer Dicing

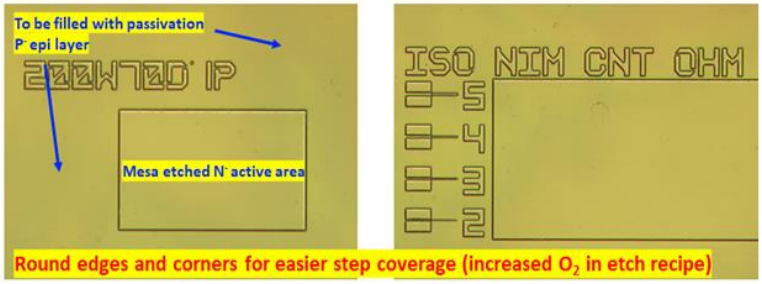
Dicing SiC wafers are difficult task since they are almost as hard as the diamond blade they cut with. It is estimated that SiC's hardness is 96 percent that of a diamond and because of this, blade wear is approximately 100 to 500 times higher than for silicon. Cutting with a saw blade is slow, tedious, and can generate a lot of heat. Since the material is also brittle, chipping is also a common problem. Resin bonded blades which are normally used for dicing SiC wafers, have excellent cutting ability that helps reduce chipping, fractures, and achieve smooth surface finish.



(a) (b)

Fig. 4.3 Image of diced 4 inch SiC epitaxial wafer (a) and ADT 7100 dicing saw (b)

4.3 Silicon Carbide Plasma Etching



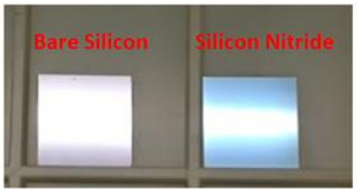
ICP Oxford 100 SiC etch recipe
SF_6 flow: 9sccm, O_2 flow: 6sccm
Pressure: 5mtorr
RF power: 100W
ICP power: 800W
Etch time : 630sec (10.5min)

Fig. 4.4 Image of mesa isolation etched SiC epi wafer and standard etch recipe

Since conventional wet etch used in silicon such as KOH etching is not practical in etching silicon carbide material, much of the device patterning is performed through plasma-based dry etching. Dry etching capability in clean facilities of Microelectronics Research Center at University of Texas at Austin is one of the top in nation with 12 different chambers using fluorine and chlorine based gas chemistries. Of all the dry etch equipment, OXFORD ICP is the most suitable etcher for etching hard materials such as SiC and other III-V compound semiconductor materials. Oxford Instruments Plasmalab System 100 ICP-RIE is a plasma-chemical etching system equipped with inductively coupled plasma source. This system allows to independently vary the energy and density of ions which are bombarded to react with the surface of the processed material. The operating pressure (2~5mTorr) of these ICP tools is much lower than in RIE systems (10-300mTorr), with much higher ion fluxes ($\geq 10^{11} cm^{-3}$ compared to $\geq 10^{9} cm^{-3}$). The high ion energy (typically ≥ 200eV) is effective and useful in breaking the strong bonds in the SiC material but as a consequence could result in photoresist burn, mask erosion, and residual lattice damage. Also, the temperature of the substrate holder can be varied in the range of -150 °C to 300 °C in order to achieve a smooth clean surface. SiC epi wafer was mesa isolation etched ~0.6um deep with a SF_6+O_2 gases mixture and the standard etch recipe is shown above Figure 4.4. The oxygen content was increased in the gas mixture to keep the surface clean, as well as to increase the curvature at the edges for easier step coverage for the upcoming passivation deposition and metal process. Mesa isolation etch acts as an edge termination for lateral power device since the active area of the n^- drift layer is selectively islanded with passivation surrounding the edges. This prevents 2D electric field crowding from happening so that lateral depletion can occur along the whole drift region length. All masks up to the contact open mask are aligned to the alignment marks etched during this process, then metal masks are aligned to the contact open mask.

4.4 Using Silicon Nitride (Si_3N_4) as Dielectric Passivation Layer

The main concern in fabricating RESURF devices in SiC is that the field in the oxide passivation can become quite high and lead to oxide rupture. Silicon nitride is a suitable candidate for passivation since owing from its higher dielectrc constant compared to silicon oxide, can withstand high electric fields during operation. As shown in the bottom Figure 4.5, the dielectric constant of Si_3N_4 is 7.5, while dielectric constant of SiO_2 is 3.9. This means that an electric field of 7.5×10^6 V/cm in oxide would correspond to a field of around 3.9×10^6 V/cm in silicon nitride. Since both passivation material's dielectric strength is 10^7 V/cm, more reliable device with passivation breakdown margin can be fabricated using silicon nitride over silicon oxide as passivation. Also, more electric field can be supported by field plate structure using silicon nitride as passivation and with appropriate optimization of the doping concentration and thickness of the epitaxial wafers and the corresponding device design, higher blocking voltage capability can be achieved as shown in the following TCAD simulation figures.



Properties	SiO_2	Si_3N_4
Dielectric Constant	3.9	7.5
Dielectric Strength (V/cm)	10^7	10^7
Refractive Index	1.46	2.05
Etch Rate in Buffered HF (angstroms/min)	1000	5 - 10

Fig 4.5 Properties of high-k dielectric silicon nitride (Si_3N_4) compared to SiO_2

Nitride (Si_3N_4) deposition recipe

Parameter	Value
RF Power	20W
Pressure	400mTorr
NH_3 Flow	2sccm
N_2 Flow	25sccm
SiH_4 Flow	20sccm
Temperature	250 °C

Fig 4.6 Plasmatherm 790 PECVD and standard recipe for silicon nitride depostion

Plasmatherm model 790 plasma enhanced chemical vapor deposition system was used to deposit both oxide (SiO_2) and silicon nitride (Si_3N_4) dielectric films as shown in above Figure 4.6. The system uses a capacitively-coupled 13.56 MHz source excitation to produce the plasma between two parallel aluminum plates. The gas is injected over the sample through a 6" diameter showerhead and chemically reacts to form thin dielectric films. The samples are placed on the system anode which is heated to 200-250°C to form a denser film. Thickness and refractive index for evaluating the quality of film was conducted using the Ellipsometer J.A. Woollam M-2000 DI.

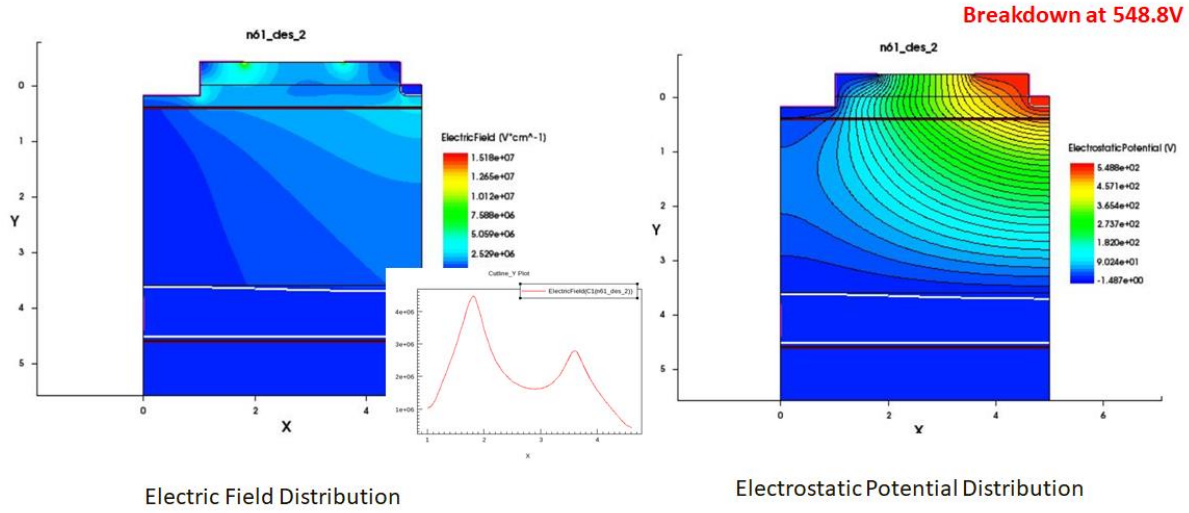


Fig. 4.7 Simulation of lateral RESURF 4H-SiC Schottky barrier diode with SiO_2 as passivation layer

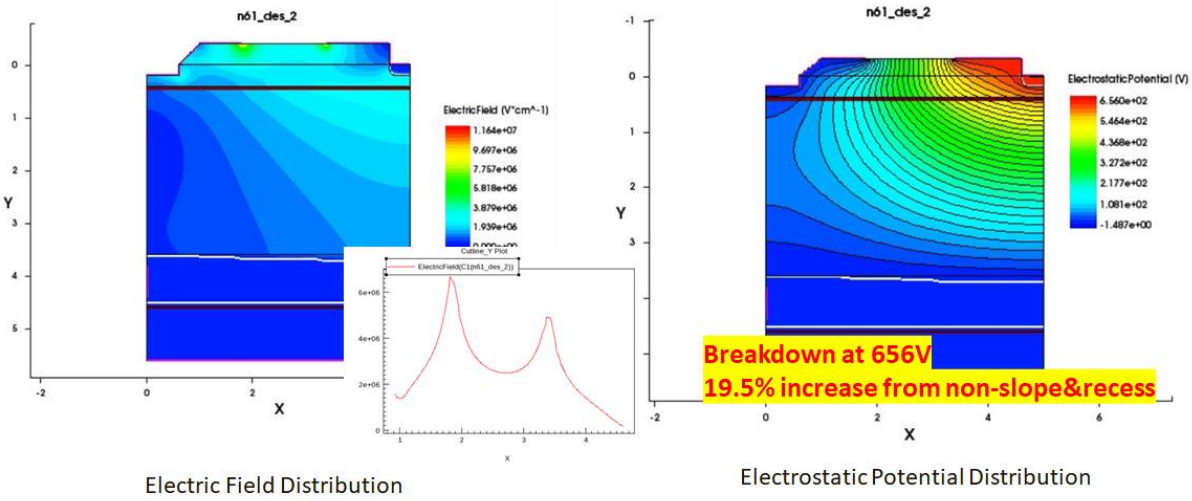


Fig. 4.8 Simulation of lateral RESURF 4H-SiC Schottky barrier diode with Si_3N_4 as passivation layer

4.5 Contact Open Etch Process

Passivation contact open process involves a mixture of wet and dry etch technique to achieve the finest resolution and the necessary slope in the structure. Both SiC epi wafer and passivation (SiO_2 or Si_3N_4) are semi-transparent materials, which cause "double-exposure" problems when reflecting UV light is not controlled during photolithography. 55nm of Ti was used as an "anti-reflective coat" to control scattering reflected UV light. Once fine resolution had been achieved for contact open photo against a positive photoresist, wet etch of the Ti layer was conducted with BOE (buffered oxide etchant). This wet etch process will produce an undercut, which defines the length of the slope. Then anisotropic dry etch, using Plasmatherm 790 RIE, was performed with a CF_4+O_2 gas mixture followed by another BOE wet etch so as to completely remove passivation residues. After PR removal, the remaining Ti layer was selectively removed using a piranha solution, which left a clean layer of passivation with defined drift length, contact width, and taper angle for effective sloped field plate.

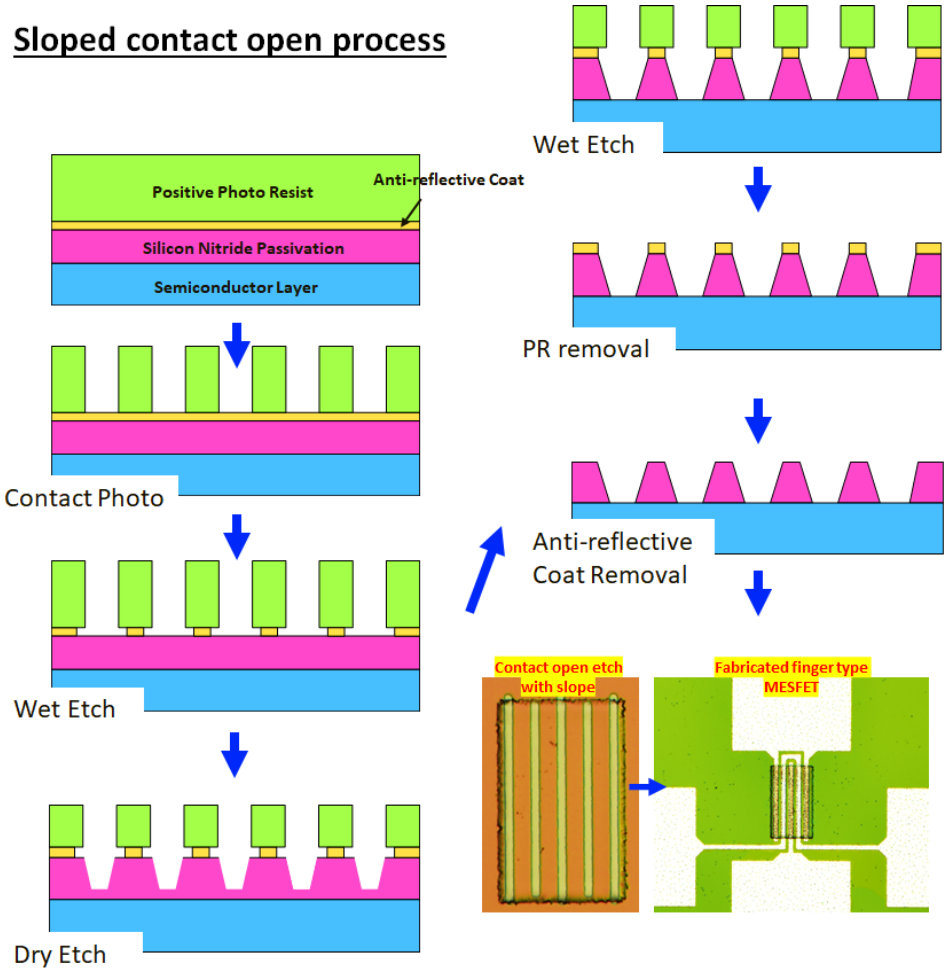


Fig. 4.9 Fabrication process step for sloped passivation contact open

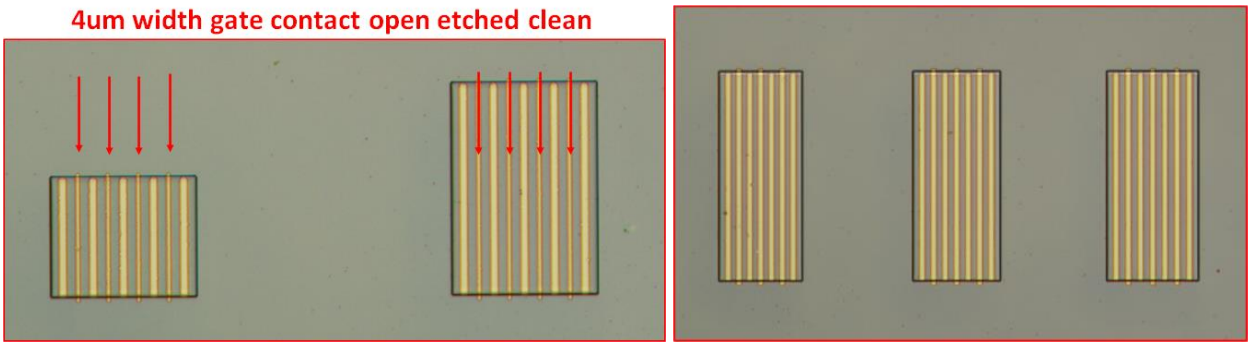


Fig. 4.10 Example of microscope image of contact open etch to finger-type devices

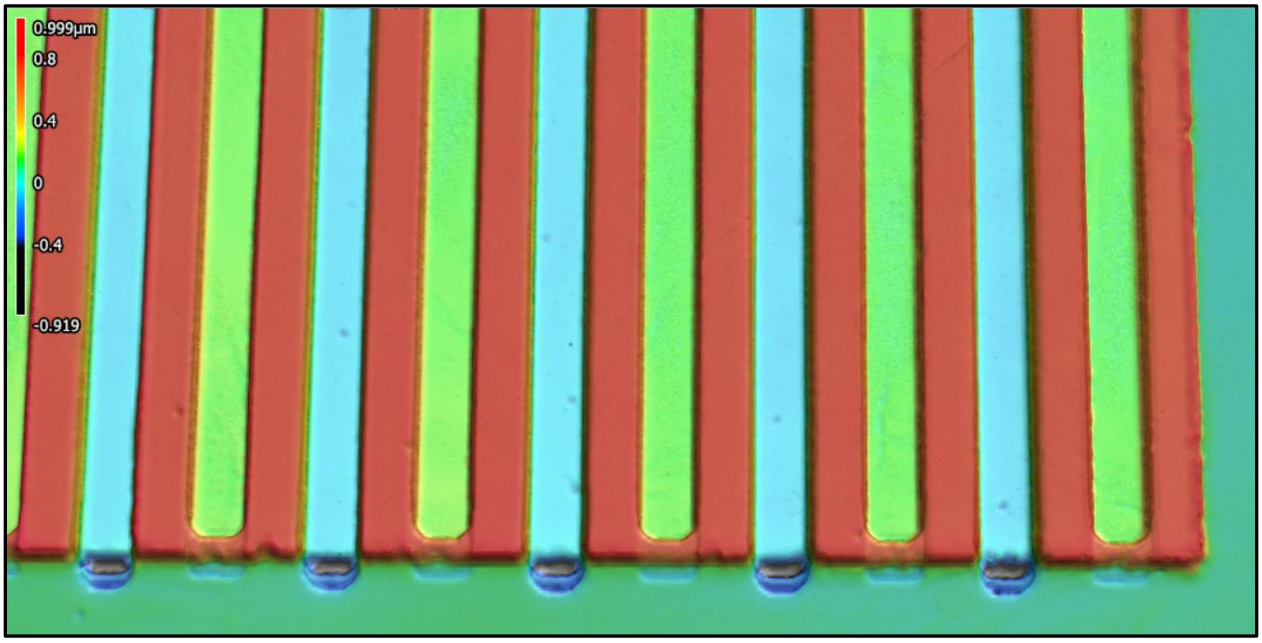


Fig. 4.11 Keyence optical profilometer image of the fabricated finger-type device after contact open etch

The evaluated angle of the contact open etch in the passivation is roughly 30° degrees as shown on Figure 4.13. Although the intended angle from the TCAD simulation is 45° degrees, 30° degrees is still sufficient in spreading out the electric field away from the contact periphery and reduce the magnitude. The purpose of the sloped field plate structure is to ensure further electric field distribution uniformity at the contact edges by having metal contact overlapping on a dielectric passivation layer. This structure is similar to a MOS capacitor and produces the same effect as introducing positive charges in the drift layer which spreads out the electric field.

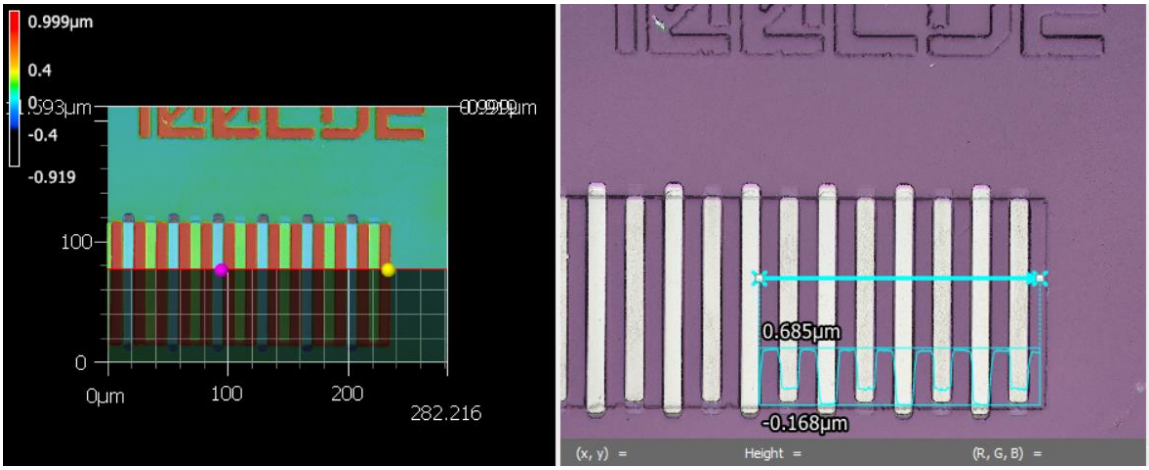


Fig. 4.12 Keyence optical profilometer image of the fabricated finger-type device after contact open etch indicating height scan direction

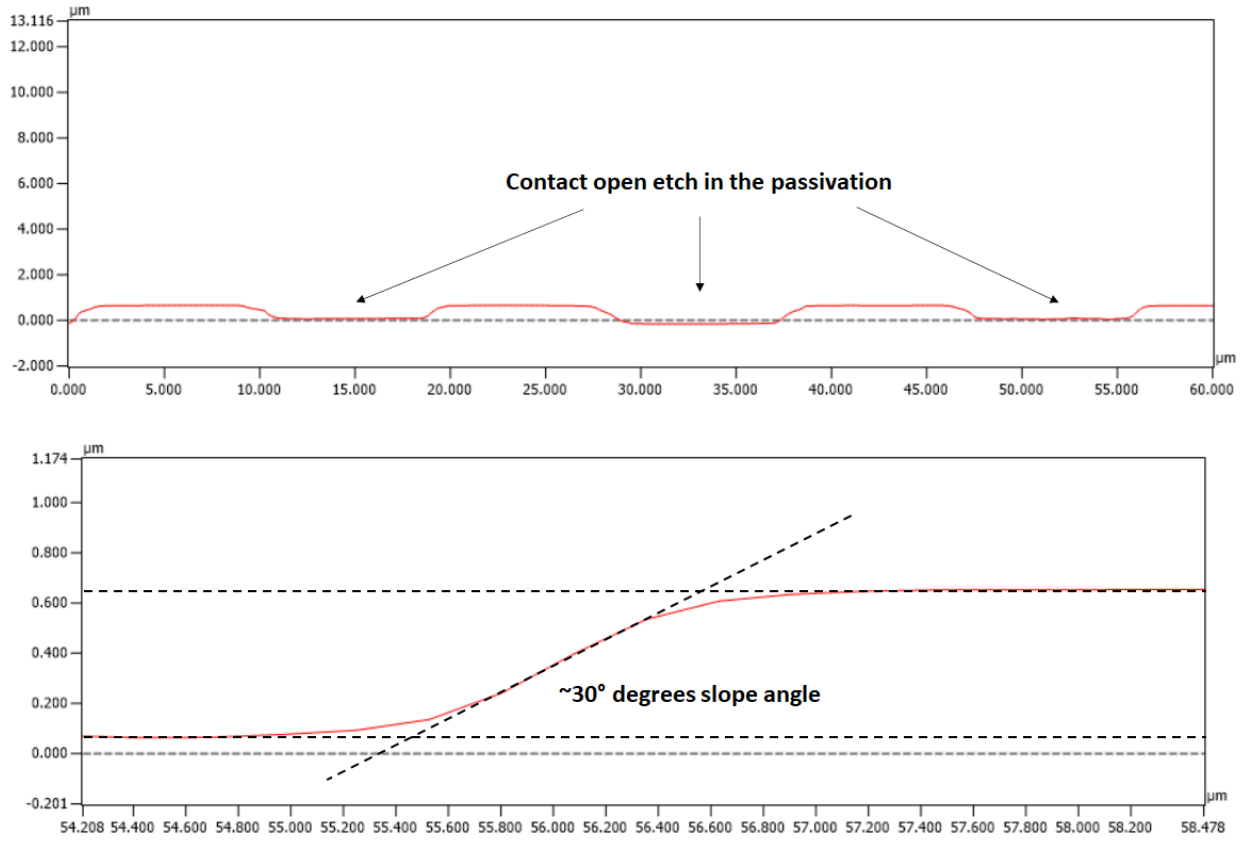


Fig. 4.13 Scanned height profile of the sloped passivation contact open (top) and close-up image of the slope with measured angle (bottom)

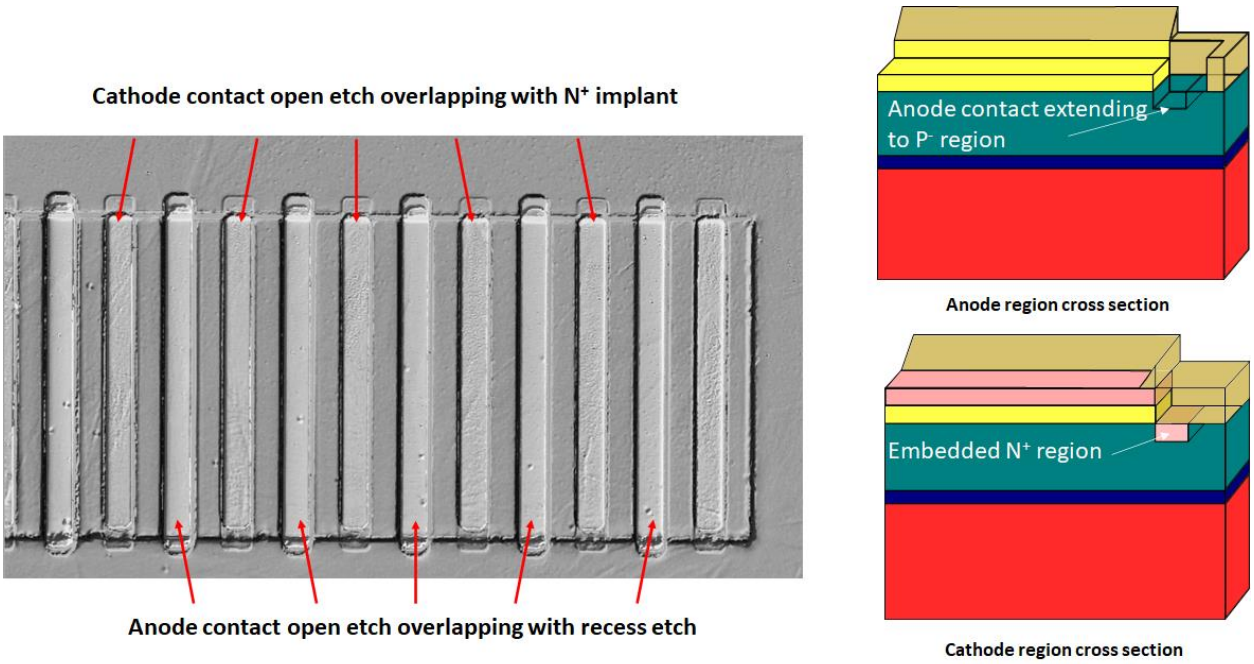


Fig. 4.14 Contact open etch laser microscope image indicating alignment against N^+ implant region and recess etch

The above Figure 4.14 image proves quality mask alighnment was achieved during the contact open etch process against the prior N^+ implant and recess etch process. Horizontal misalignment is barely noticable, while there is a slight vertical misalignment of the contact open photo being little upward against the mesa isolation etch. Still, the cathode region contact open do not surpass the mesa isolation edge, so the intended 1D structure to minimize electric field crowding is achieved.

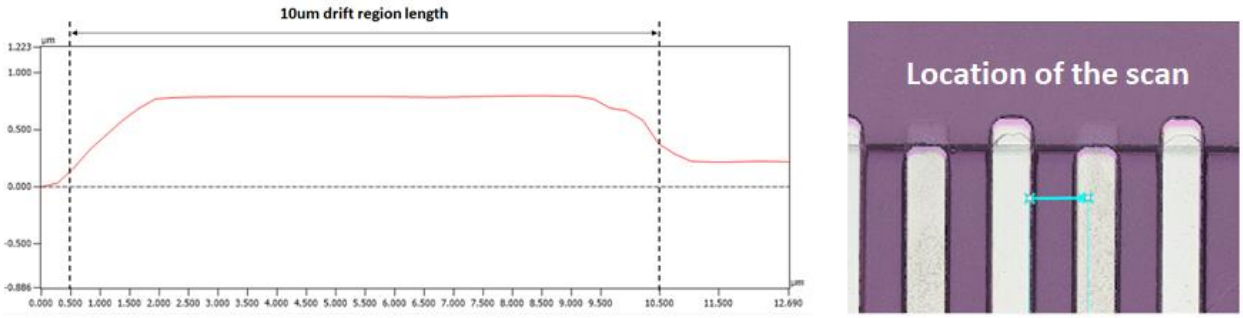


Fig. 4.15 Scanned height profile of the sloped passivation contact open confirming necessary drift region length

As confirmed from the height scan in Figure 4.15, contact widening from the isotropic wet etch is suppressed to the minimum and the necessary drift length according to mask dimension is achieved.

4.6 Ohmic contact to *n*-type SiC

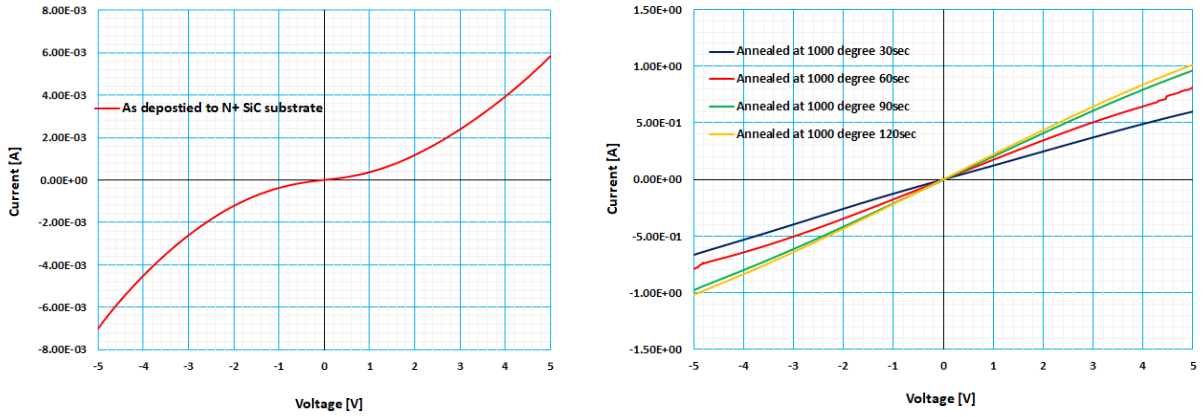


Fig. 4.16 Comparison of current conduction of ohmic metal stacks between as deposited and annealed at 1000°C with different duration

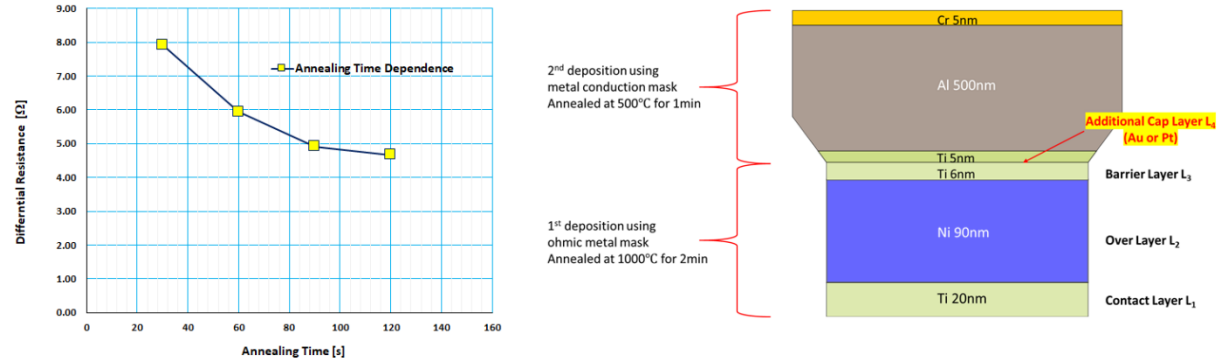


Fig. 4.17 Annealing time dependence of the differential resistance obtained and schematic diagram of ohmic metal stacks

Ohmic metal stacks of Ti/Ni/Ti =20nm/90nm/6nm were deposited with e-beam evaporator and patterned through a lift-off process. The above figures describe the effect of annealing at high temperature for a formation of ohmic contacts to a N^+ highly doped SiC substrates. A high temperature, preferably higher than 900°C, is required to form a sufficent nickel silicide (Ni_2Si) layer to achieve an ohmic behavior. The metal stacks were annealed using RTA (AG Associates, Model: Heat pulse 610) at a temperature of 1000°C for 2min in 99.99% pure nitrogen (N_2) ambient. Normally, for high temperature annealing, an additional cap layer using nobel metals such as Au or Pt is required to prevent oxidization and deterioration, especially when annealing in atmospheric pressure. The top 6nm of the Ti layer oxides easily but remains conductive and prevents further oxidization of the bottom Ni layer. The ohmic metal stacks can be summerized into four essential layers. The first metal layer is

refferred to as the contact layer L_1, which requires low work function and good adhesion to the highly doped SiC. The second layer is the overlayer L_2, which is able to form intermetallic compounds such as Ni_2Si connecting the top and bottom layers. The third metal layer, barrier layer L_3, serves the purpose of limiting the in-diffusion of the upper metal layer and out-diffusion of the bottom metal layers. The fourth cap layer acts as a protective layer to prevent the oxidation of underlying metals.

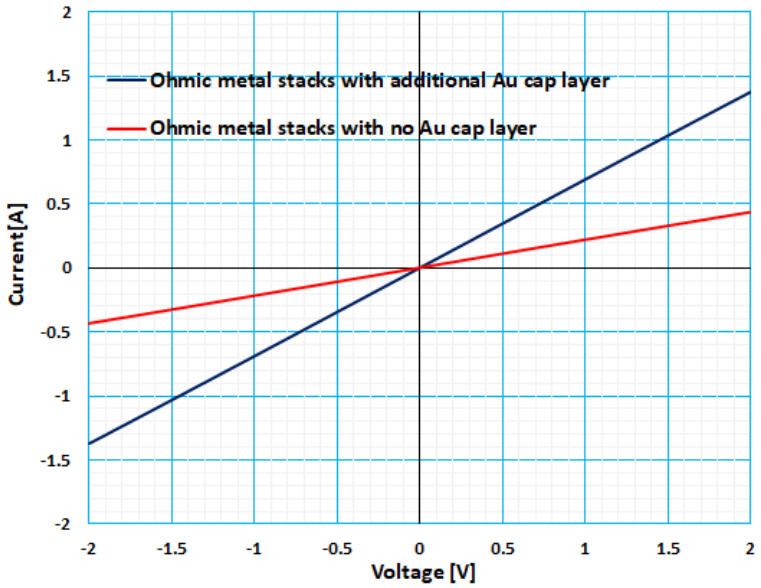


Fig. 4.18 I-V plot showing improvement of current conduction with additional Au cap layer to ohmic contact metal

For the final fabrication process, Au cap layer with thickness of 120nm was added to the previous ohmic contac metal recipe. As shown in Figure, Au cap layer is effective in reducing contact resistance. The current conduction capability is ×3 times more than previous ohmic metal contact stacks and this process recipe was applied to the final device fabrication with N^+ implant. Surface roughness is also supressed using Au as the cap layer and clean etch of Al is possible in the subsequent process step.

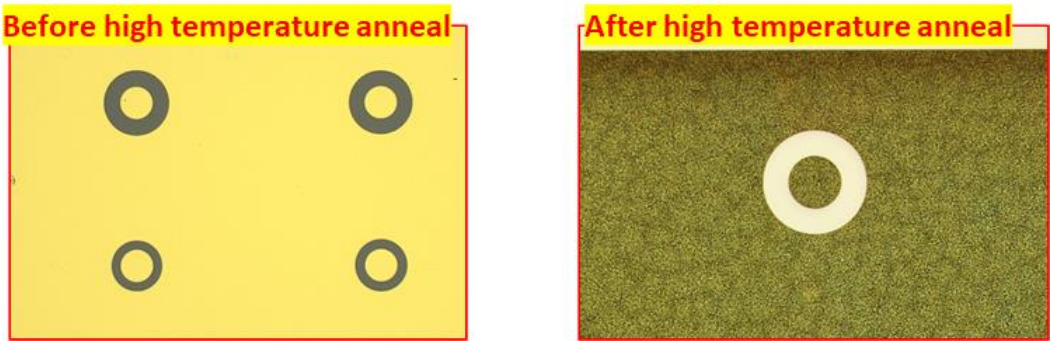


Fig. 4.19 Microscope image of CTLM pattern with ohmic metal stacks and Au as cap layer (Before and after annealing)

4.7 Schottky contact to *n*-type SiC and confirming field plate structure

Schottky metal stacks of Ni/Al/Ni =50nm/50nm/20nm were deposited with e-beam evaporator to form the anode region of the lateral Schottky barrier diodes and gate region of the lateral MESFETs. Nickel was chosen as the Schottky contact metal layer because of its high metal work function (5.01eV) needed in forming high barrier height Φ_{BN} to suppress reverse leakage current during reverse operation. The downside of using a high metal work function is forward voltage drop V_F will be high which will lead to high conduction loss during forward operation. After each metal contacts were deposited and patterned, formation of field plate structures was confirmed through microscope image. Slight misalignment between the contact mask and ohmic/Schottky mask can lead to insufficient field plate length. As shown in the bottom figure, Schottky metal formed an even field plate structure on both sides, while the ohmic metal has slightly longer field plate on the left side from small misalignment.

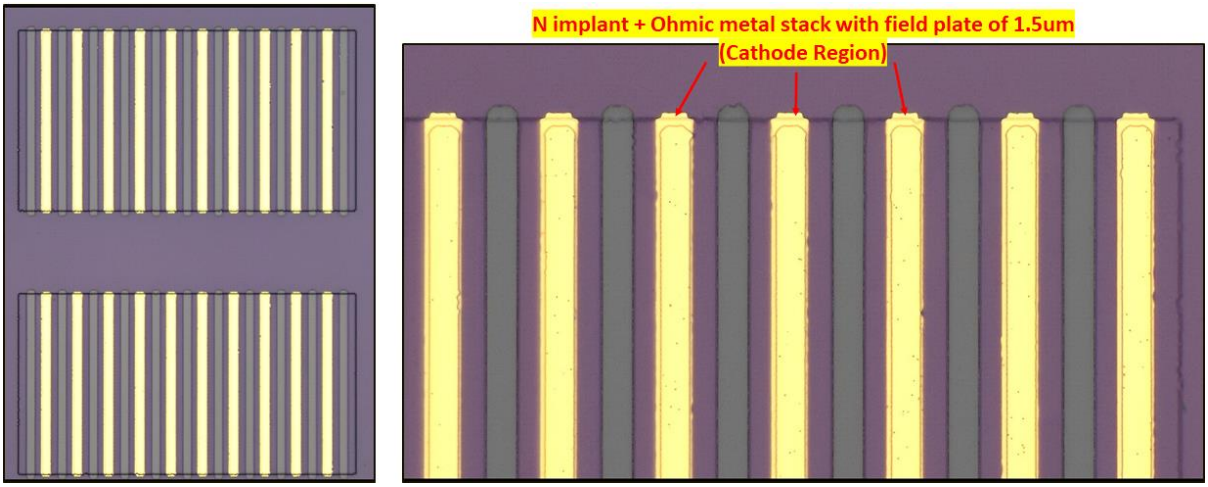


Fig.4.20 Microscope image confirmation of field plate structure from ohmic metal contact and contact open overlap

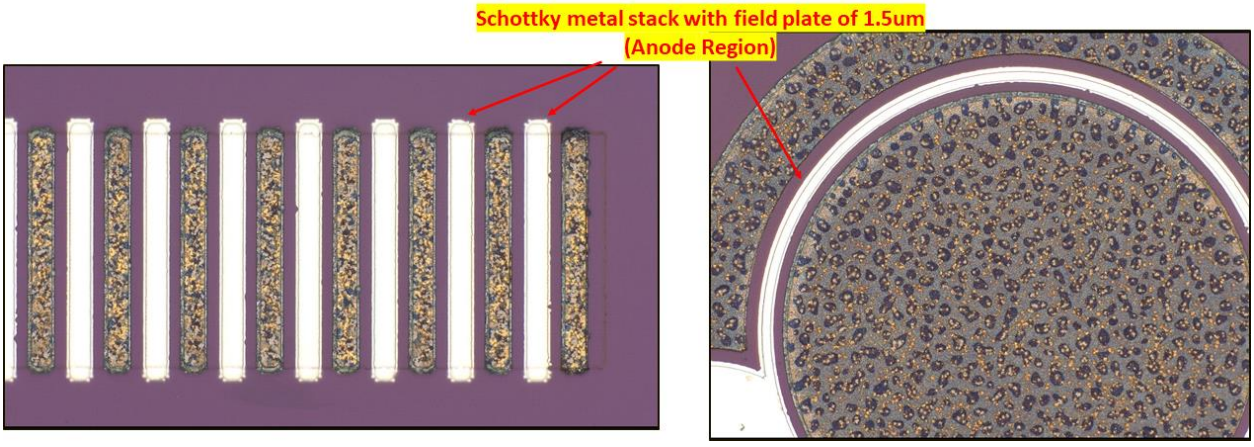


Fig. 4.21 Microscope image confirmation of field plate structure from Schottky metal contact and contact open overlap

4.8 Thick Aluminum Process

For the lateral device fabrication, thick metal conduction layer is essential for minimizing resistance during forward conduction, since current runs along the surface of the whole area of the device instead of vertically through the thickness of the epitaxial wafer. Aluminum was chosen as the conduction metal layer because of its ease to deposit thick layers at a relatively inexpensive cost. Aluminum can be patterned in multiple ways, such as lift-off process using negative photoresist, dry etch using chlorine based chemistries, and wet etch using aluminum etchant such as "Aluminum etch 16:1:1:2". For our current needs, metal stack of Ti/Al/Cr=5nm/500nm/10nm were deposited using an e-beam evaporator and then patterned using a dry/wet etch process. The titanium layer is used as adhesive layer, aluminum as the conductive layer, and chromium (Cr) as the cap layer. The top Cr layer acts as an anti-reflective coat during the photolithography process, minimizing reflection for possible "double-exposure" problems. Patterning was performed using BCl_3 dry etch, then finished off with a wet etch. During the final wet etch process, the top Cr layer is resistant to the aluminum etchant, thus minimizing a possible undercut being formed. As shown in Figure 4.22, a combination of a dry and wet etch process with the top Cr layer enables to retain a thick line width necessary for fabricating long finger devices with fine resolution during the whole metal process.

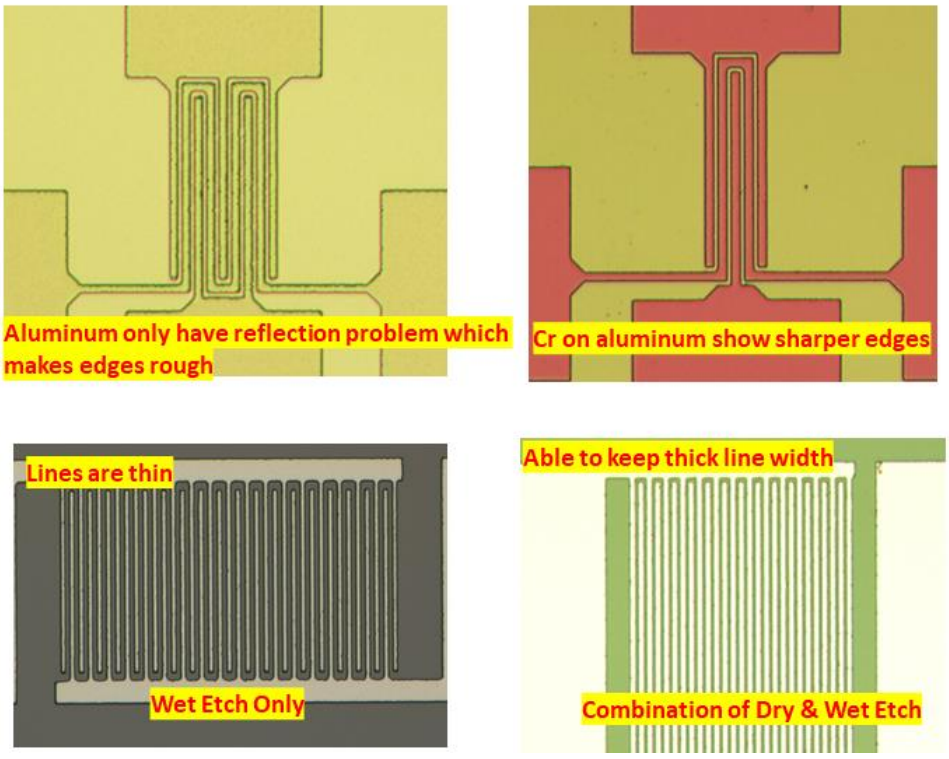


Fig.4.22 Thick Al metal fabrication process (dry & wet etch)

4.9 N^+ ion implant and activation process

4.9.1 *n*-type Doping of SiC

Phosphorus and nitrogen have been extensively studied for the n-type doping of SiC, due to their relatively low activation energies as shown in Table 1 below.

Table 1. Ionization Energies of Nitrogen and Phosphorus Impurities in 4H-SiC and 6H-SiC

Polytype	Impurity	Ionization energy in hexagonal site (meV)	Ionization energy in cubic site (meV)
4H-SiC	*Nitrogen*	85	140
	Phosphorus	80	110
6H-SiC	*Nitrogen*	50	92
	Phosphorus	53	93

Nitrogen is especially used as an *n*-type dopant for *in-situ* doping during epitaxial growth. The element also has lower atomic mass; thus, less damage is created to the crystal when it is ion implanted. On the other hand, phosphorus has recently been used increasingly for SiC MOSFET fabrication in order to achieve lower contact resistance for source/drain ohmic contact due to its higher solubility in SiC material. Moreover, phosphorus has a higher activation rate at lower temperature activation, which could be beneficial if the availability of furnace equipment and cap layer material is limited.

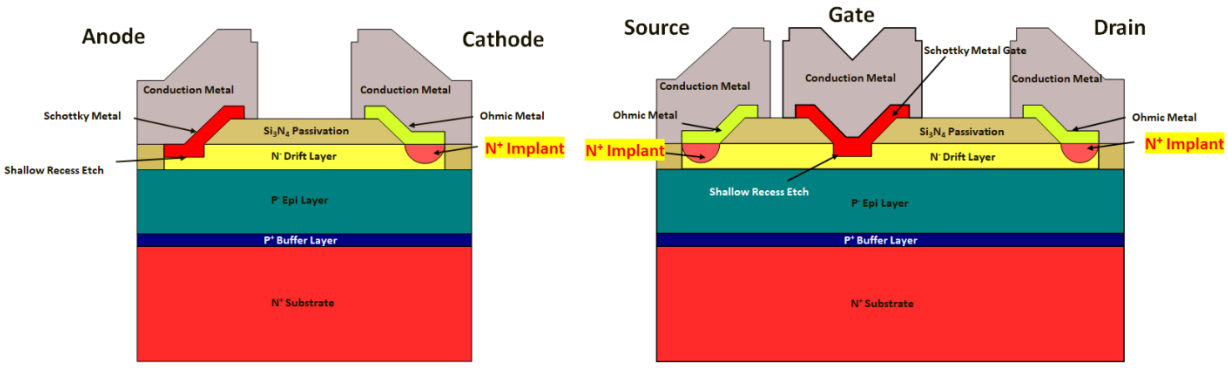


Fig. 4.23 Schematic illustration of fabricated lateral RESURF SiC Schottky barrier diode and MESFETs indicating N^+ implanted cathode, source, and drain region

As shown in Figure 1, phosphorus implant was performed to all cathode contact of lateral Schottky barrier diodes and source/drain contact of the lateral MESFETs in the final fabrication so as to reduce contact resistance and improve forward performance.

Table 2. Anode/Drain/Source Implantation Series

Dopant	Dose	Energy	Angle/Twist
Phosphorus	$2.7\times10^{15}cm^{-2}$	200keV	Tilt 7 degrees, Twist 23 degrees
Phosphorus	$1.4\times10^{15}cm^{-2}$	100keV	Tilt 7 degrees, Twist 23 degrees
Phosphorus	$9.0\times10^{14}cm^{-2}$	50keV	Tilt 7 degrees, Twist 23 degrees

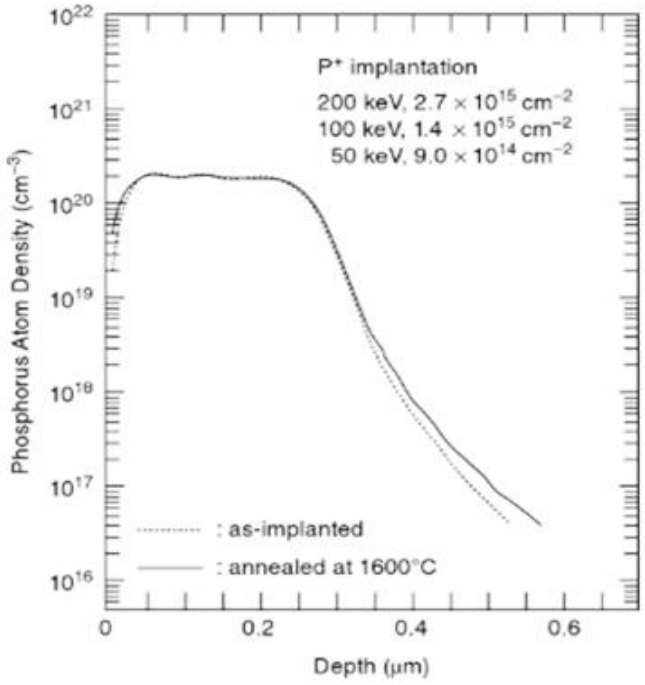


Fig. 4.24 Depth profiles of a 200nm-deep box profile phosphorus atoms multistep energy implant process [18]

The above figure illustrates the depth profile of phosphorus implanted with the implantation series shown in Table 2 which was performed at Nissin Ion Equipment Co. LTD. As indicated, the three multiple energy implants, which gave the highest energy of 200keV and the lowest energy of 50keV, will form a 200-nm-deep box profile. Furthermore, channeling effects can be suppressed by setting the implantation tilt angle to 7° and twist to 23°. Obtaining a good box profile with high doping concentration is necessary in achieving quality ohmic contact with low contact resistance.

Nissin Ion Equipment Co. LTD. is a tool manufacturer company which also provides ion implant service. They offer standard dopants used for silicon process, as well as N and Al for SiC. Compatible substrate size ranges from a small piece of 15mm × 15mm to 300mm sized wafer. Their ion implanters are capable in energy range from 5keV to 960keV with multiple charge. Their newest ion implanter, IMPHEAT®, has the capability to conduct hot implantation at a temperature as high as 500℃.

4.9.2 Post-implantation annealing

Post-implant annealing is required for the following reasons:

1) Restoring the crystal structure damage created by ion implantation
2) Electrically activating the implanted dopants

Post-implantation annealing is generally performed at temperatures ranging between 1200℃ and 1700℃. The ion implantation doping technique, compared to *in-situ* doping through epitaxial growth, generates a substantial amount of crystal damage during the process. The damage can range from point defects by single collision at low implant doses to complete amorphization at high doses. Although much of the implant-induced damage can be removed at 1200℃, hot implantation is recommended where the sample is heated to ~500℃ during high-dose implantation to reduce damage and induce fast crystal recovery.

4.9.3 Effect of Using SiO_2 as a Cap Layer for Dopant Activation [19]

After ion implantation, the dopants must be thermally activated using high temperature annealing within a range of 1400~1700℃. The presence of severe surface roughening is observed on SiC implanted with P or N followed by high temperature annealing as a substantial amount of Si evaporates outward from the SiC substrate. A rough surface deleteriously affects the specific on-resistance of SiC power devices. In order to preserve surface morphology, cap layers, such as pyrolyzed negative photoresist [20] and AlN [21], have been traditionally used during implant activation. Dopant activation using pyrolyzed negative photoresist as a cap layer requires a complex furnace setup, where inert gasses, such as Ar or N_2, are needed to prevent the cap layer from oxidizing and evaporating. The deposition of a thick AlN layer requires a DC sputtering system where a 3-inch AlN sputtering target could cost over $500~. The AlN cap layer also requires KOH etch for removal after activation, which can also etch the SiC layer underneath. Although both pyrolyzed negative photoresist and AlN layers have been known to be effective in protecting surface morphology, in this research study, the use of a thick SiO_2 layer is proposed as a protective layer. While SiO_2 only withstands temperatures of up to ~1200°C when deposited over Si, it withstands higher temperatures of up to ~1500°C on SiC owing to the lower vapor pressure of Si over SiC. As shown in Figure 3, if there is sufficient thickness (>1um) of SiO_2, the surface is protected from the deterioration caused by high temperature, and surface roughness is suppressed to the minimum.

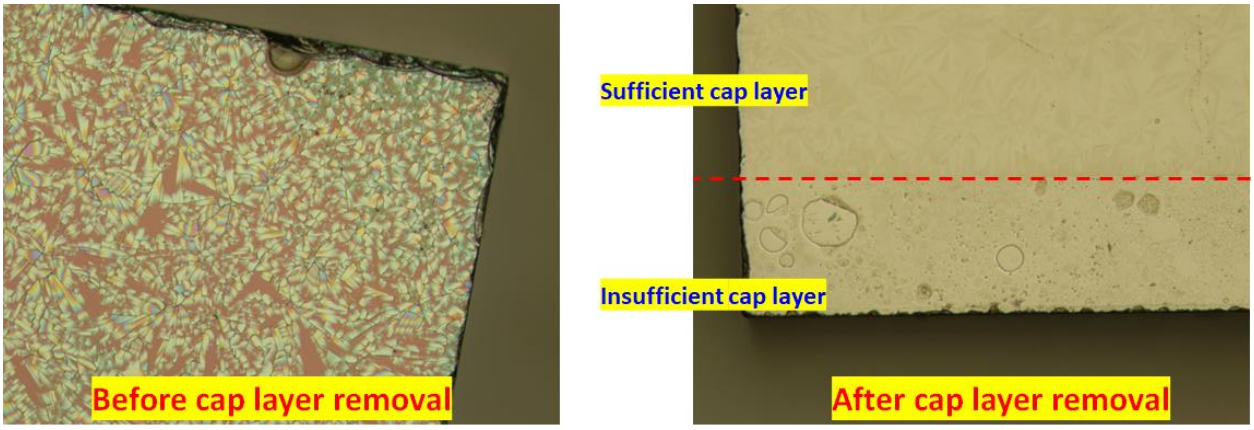


Fig. 4.25 A microscope image of the SiO_2 cap layer after 1500℃ activation and SiC surface after removal

4.9.4 Thermal Processes in SiC Device Fabrication and Necessity of High Temperature Furnace

SiC power device fabrication requires several thermal processes, some of which are:

- Activation of dopants after ion implantation
- Thermal oxidation with dry or wet oxygen
- Deposition of LPCVD-oxide from TEOS (Tetraethoxysilane)
- Deposition of Oxynitride
- Post deposition annealing of evaporated metal layers
- Short-term contact annealing

Table 3. Example of Required Temperature for SiC Device Fabrication

Thermal process in SiC fabrication	Furnace type	Required maximum temperature
Activation	High Temperature Furnace	2000℃
Oxynitriding	High Temperature LPCVD Furnace	1400℃
TEOS-Deposition	High Temperature LPCVD Furnace	1350℃
Thermal Oxidation	Vertical Furnace	1200℃
Post Deposition Annealing	RTA	1100℃
Contact Annealing	RTA	1000℃

As illustrated in the above table, typical quartz furnaces, with a maximum operating temperature of 1200℃ used in the Si device fabrication process, cannot be employed for thermal

processes for SiC device fabrication. Hence instead, we have prepared a high temperature tube furnace (MHI industry, model H18-40HT) fitted with an alumina tube for the ion implant activation process. This furnace has an alumina tube with an outside diameter of 50 mm and an inner diameter of 44 mm, which can handle small SiC pieces and withstand temperatures of up to 1760 °C.

Fig. 4.26 An image of Micropyretics Heaters International H18-40HT high temperature furnace with detached alumina furnace tube

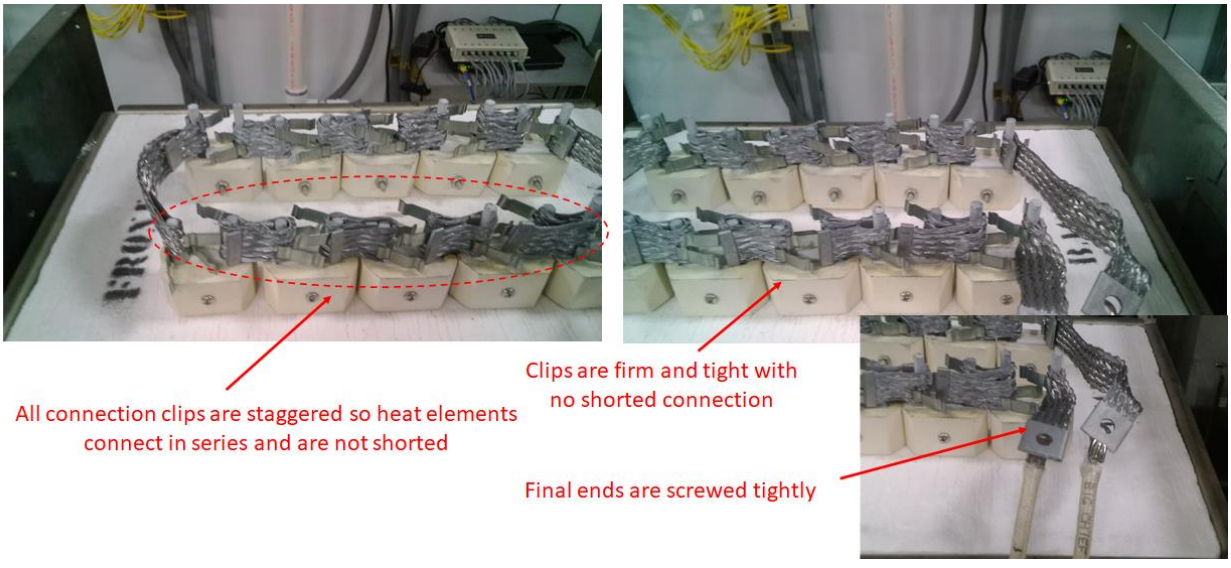


Fig. 4.27 Installation of ((Molybdenum Disilicide) heat elements to Micropyretics Heaters International H18-40HT high temperature furnace

MHI industry, model H18-40HT high temperature furnace, requires 10 sets of $MoSi_2$ (Molybdenum Disilicide) heating elements, which are known for their ability to quickly attain and sustain high temperatures, thus suitable for the needed application. Resistivity of a $MoSi_2$ heating element increases dramatically when temperature rises. Even though they appear robust, they are glasslike material with low mechanical shock resistance. Heating elements have a molybdenum core coated with quartz glass which nearly becomes liquid as they approach maximum temperature. The glass surface reacts with the oxygen in the air to form a renewed coating of protective glass on the element surface after every usage. These elements will eventually lose their thickness and need replacing. The advantage of these heat elements is that resistance of a $MoSi_2$ does not drop over time during usage, and new and old elements can be mixed together. As shown in Figure 4.28, we have purchased 10 new sets of heat elements and installed them as illustrated in Figure 4.27.

Fig. 4.28 An image of replacement $MoSi_2$ heating elements and alumina boat used in the activation experiment

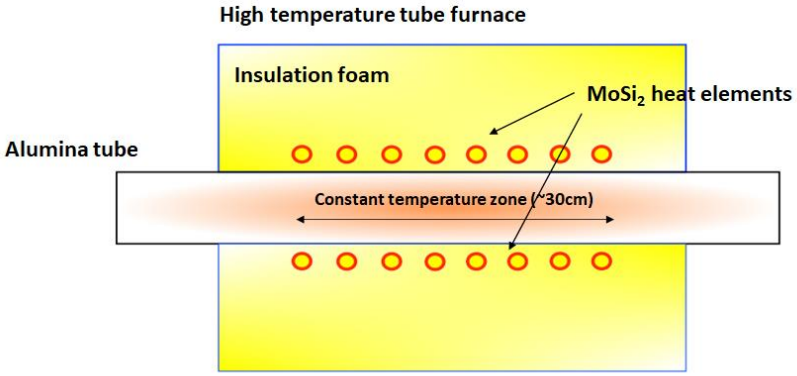


Fig. 4.29 Schematic illustration of high temperature tube furnace with $MoSi_2$ heat elements

The temperature in the constant temperature zone is the highest, equivalent to the temperature that was set using the controller. As illustrated above, the temperature decreases when extended away from the constant temperature zone. Boat was placed in the constant temperature zone for the activation experiment.

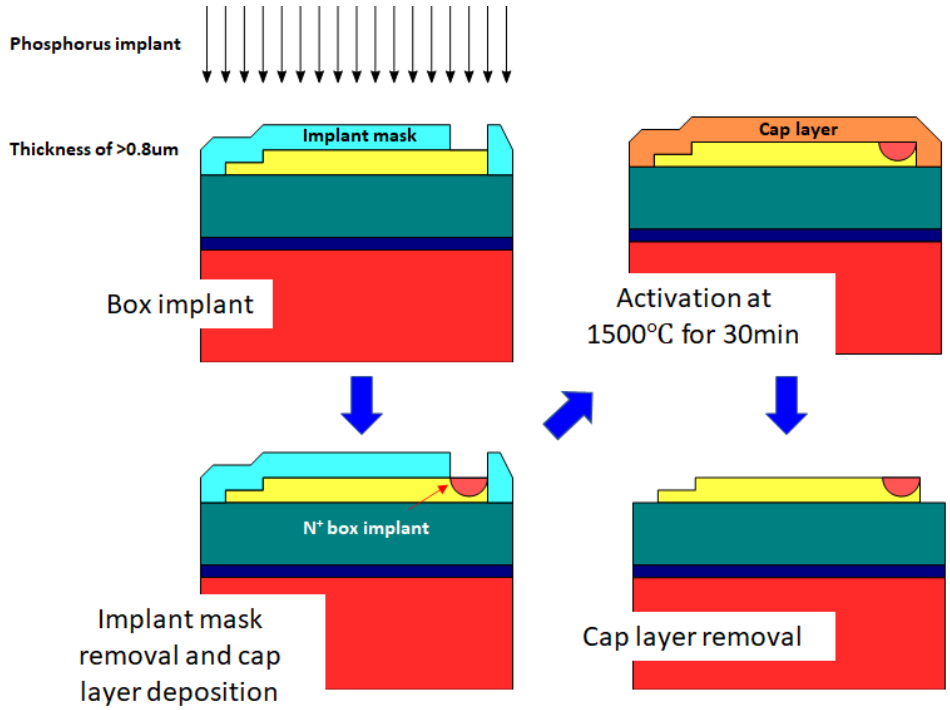


Fig. 4.30 The process flow of ion implantation and activation for cathode ohmic contact

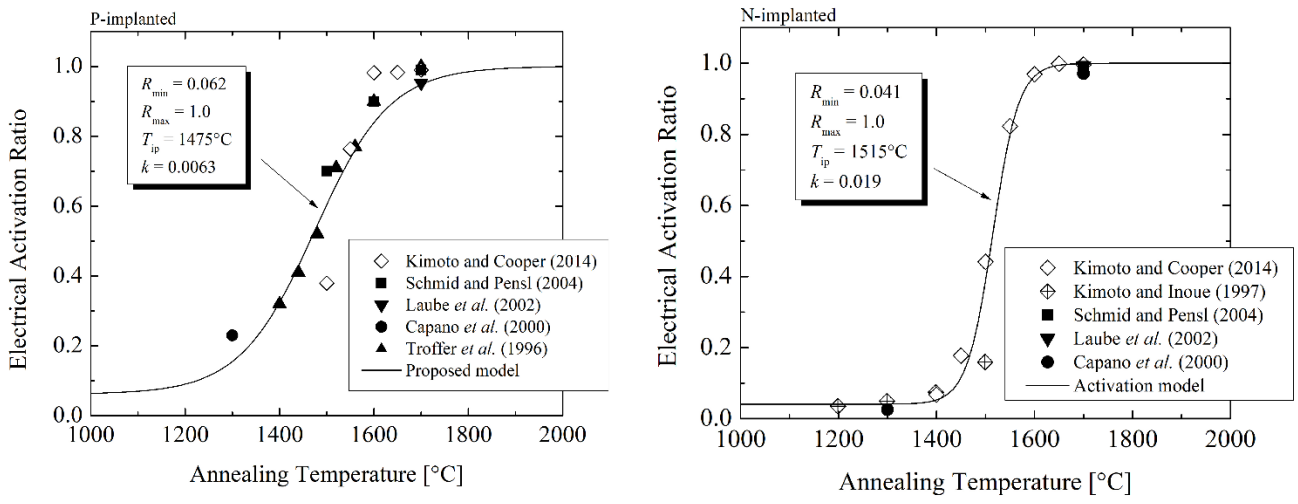


Fig. 4.31 Electrical activation ratios of phosphorus and nitrogen dopants as a function of the annealing temperature [22]

Post implantation annealing at a temperature higher than 1400°C is necessary for dopants to become "electrically active" by taking position in a proper lattice site. As shown in the above electrical activation ratio curve, phosphorus has a lower activation temperature, where dopants start to get activated at 1200°C and the activation ratio continuously increases with temperature. On the other hand, nitrogen activation in SiC is similar to a step function, requiring a temperature above 1500°C to secure

a sufficient activation ratio. In this research study, we have chosen phosphorus as the dopant species and a temperature of 1500 °C as the activation temperature due to the following reasons:

- High temperature furnace has no gas line equipped for Ar or N_2 ambient annealing and activation was done in air ambient.
    - 1um thick SiO_2 was chosen as the cap layer. (Pyrolyzed photoresist will oxidize and evaporate). The temperature limit for the SiO_2 cap layer is around 1500°C where it will start to deteriorate.
- Phosphorus has higher solubility; thus, higher concentration needed for quality ohmic contact can be achieved.
- Phosphorous has a higher activation rate at lower temperature activation which is beneficial since the high temperature furnace is unstable at the maximum operational temperature of 1600~1700°C.
- Phosphorus implanted doping profile is easier to detect through SIMS analysis against a constant nitrogen background doping of the implanted n^- drift region.

4.9.5 Two-contact two-terminal pattern for confirmation of activation process

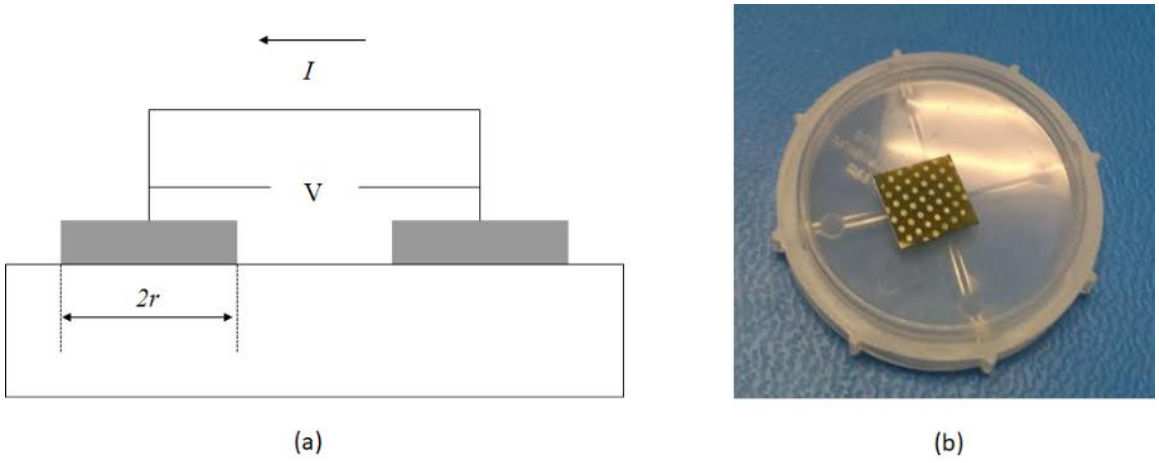


Fig. 4.32 Cross section view (a) and actual fabricated two-contact two terminal pattern on SiC epi with implanted N^+ region activated at varied activation temperature (b)

The plots in Figure 11 show the current conduction capability of a two-contact two-terminal pattern of an N^+ implanted epitaxial layer with an activation temperature of 1300°C and 1500°C, compared with a non-implanted epitaxial layer. A nitrogen doped n^- epilayer with a doping concentration of $2\times10^{17}cm^{-3}$ and thickness of 0.4um was used. Ti/Ni/Ti/Au=20nm/90nm/6nm/120nm metal stacks deposited with

an e-beam evaporator using a circular shadow mask were used as ohmic contacts. The fabricated pattern will have a cross section as shown in Figure 10 (a) and actual die is shown in (b)

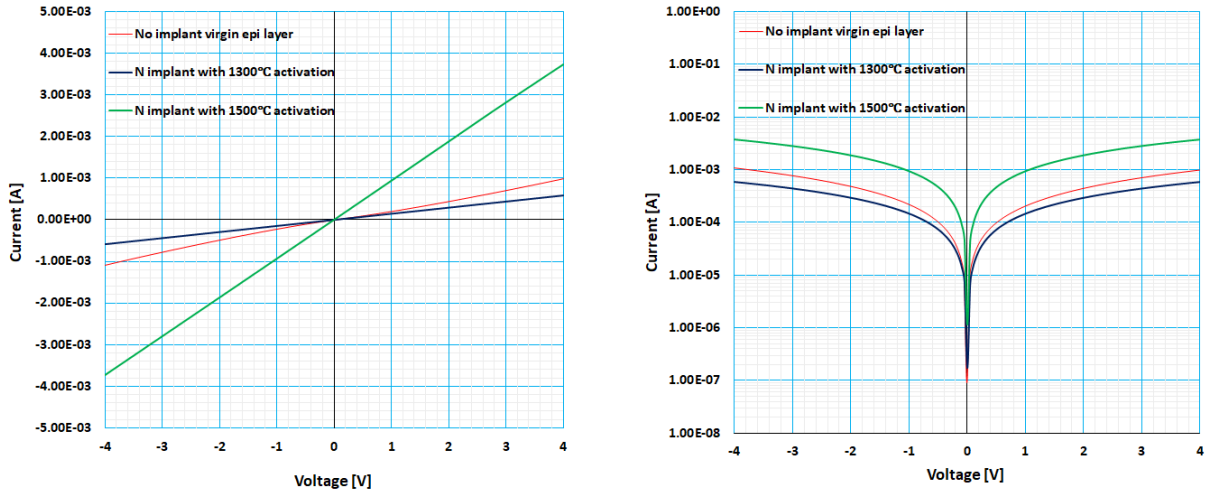


Fig.4.33 I-V plots (linear & semi-log scale) of an evaluated two-contact two-terminal pattern of an N^+ implanted sample at varying activation temperature

As shown in Figure 11, with 1300°C annealing, the activation ratio is about 20% and increase in current conduction cannot be seen. While with 1500°C annealing, the activation ratio is about 70% and we see 4 times more current conduction than the non-implanted epi sample. After sufficient activation of dopants are confirmed, the optimized process conditions for N^+ implant and activation process were integrated to the actual fabrication of the device die for better forward performance. In the upcoming chapter, we will discuss the analysis of specific contact resistance ρ_C through transmission line measurement method. This method is an effective method in evaluating the resistivity of contacts to thin semiconductor layers and extracted specific contact resistance ρ_C value will be an indication of how well ohmic contacts are formed and improved through the N^+ implant and activation process. Typically, a quality ohmic contact is defined as ~10^{-5} $\Omega \cdot cm^2$ range or lower for *n*-type 4H SiC.

5.1 Keyence VK-X1100 Optical Profilometer Evaluation

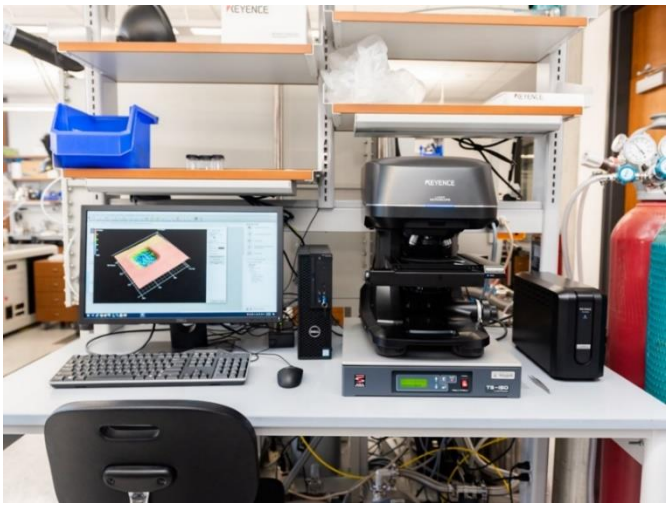


Fig. 5.1 Keyence VK-X1100 Optical Profilometer at TMI facilities

The microscope combines optical microscope image with laser profilometry for a high resolution 3D optical image which can be scanned for height profile and surface roughness. Any type of material can be used for evaluation, but semi-transparent and transparent materials tend to confuse the measurement of the laser profilometry under low magnifications. This microscope is especially suited for soft and fragile material where traditional stylus profilometry would damage the samples. This microscope is especially appropriate for the needs of this research project, compared to SEM (Scanning Electron Microscope) and the evaluation of our lateral device since it can laterally scan the needed large area while still being able to evaluate the necessary height and thickness of the device structure.

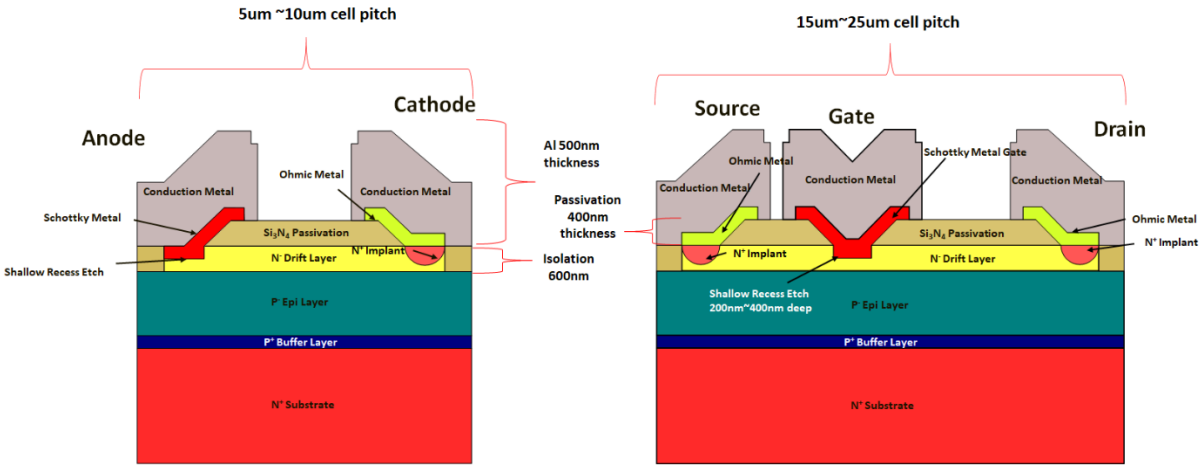


Fig. 5.2 Keyence VK-X1100 Optical Profilometer at TMI facilities

Compared to cross section SEM, the evaluation is non-destructive evaluation where no cuts or polishing is necessary, and fabrication results can be analyzed in each process step. As shown in Figure 5.2, the fabricated device has minimum structure thickness vertically where a cross section analysis is necessary, while laterally structural change spans in large area.

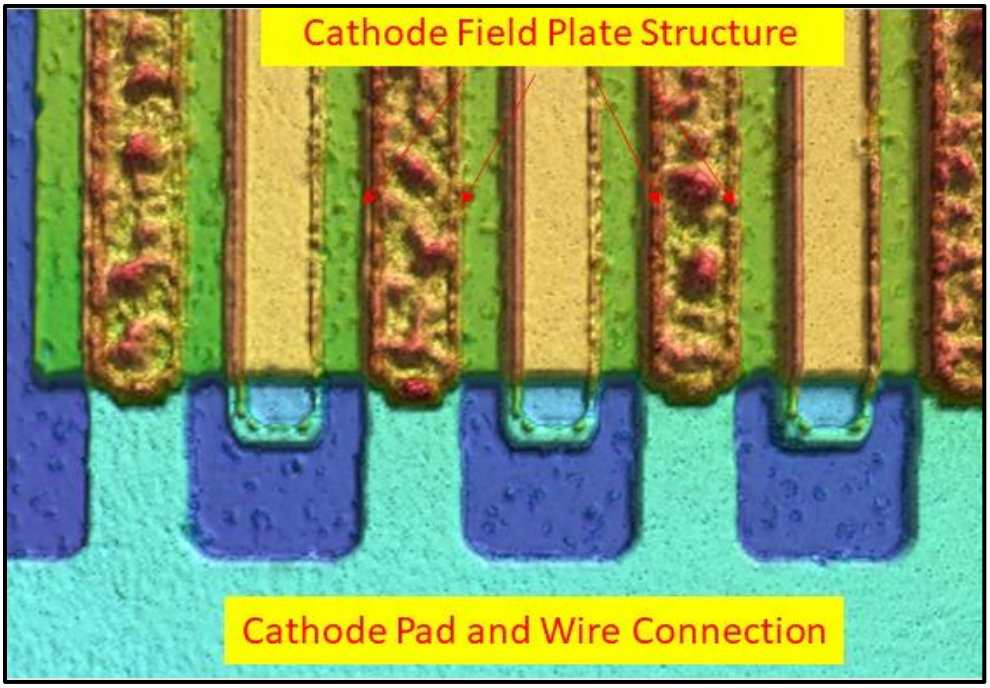


Fig. 5.3 Keyence Optical Profilometer cathode pad area of the fabricated device with effective field plate structure

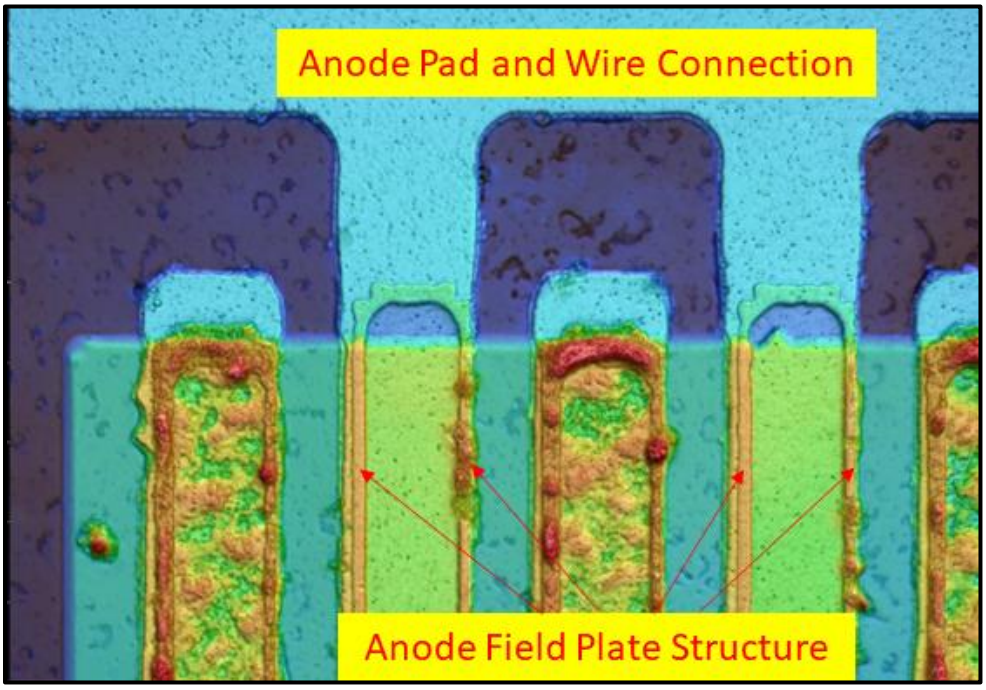


Fig. 5.4 Keyence Optical Profilometer anode pad area of the fabricated device with effective field plate structure

5.1.2 Device Dimension Confirmation of the Final Fabricated Device Using Keyence VK-X1100 Optical Profilometer

Table 5.1 Comparison of targeted design value to actual fabricated device measurement

Design parameters	Targeted design value	Measurement from actual fabricated device
Isolation etch depth	700nm	680nm
Recess etch depth	350nm	375nm
Passivation thickness	400nm	505nm (before annealing)
Passivation slope angle	45° degrees	30° degrees
Drift region length	10um	10.2um
Contact open to isolation alignment	0um misalignment	0.8um misalignment vertically
Ohmic metal thickness	236nm	253nm
Ohmic metal field plate length	1.5um	1.6um(left)/1.1um(right)
Schottky metal thickness	120nm	154nm
Schottky metal field plate length	1.5um	1.2um both sides
Conduction metal (Al) thickness	500nm	475nm
Conduction metal field plate length	3.5um	3.0um(left)/2.8um(right)

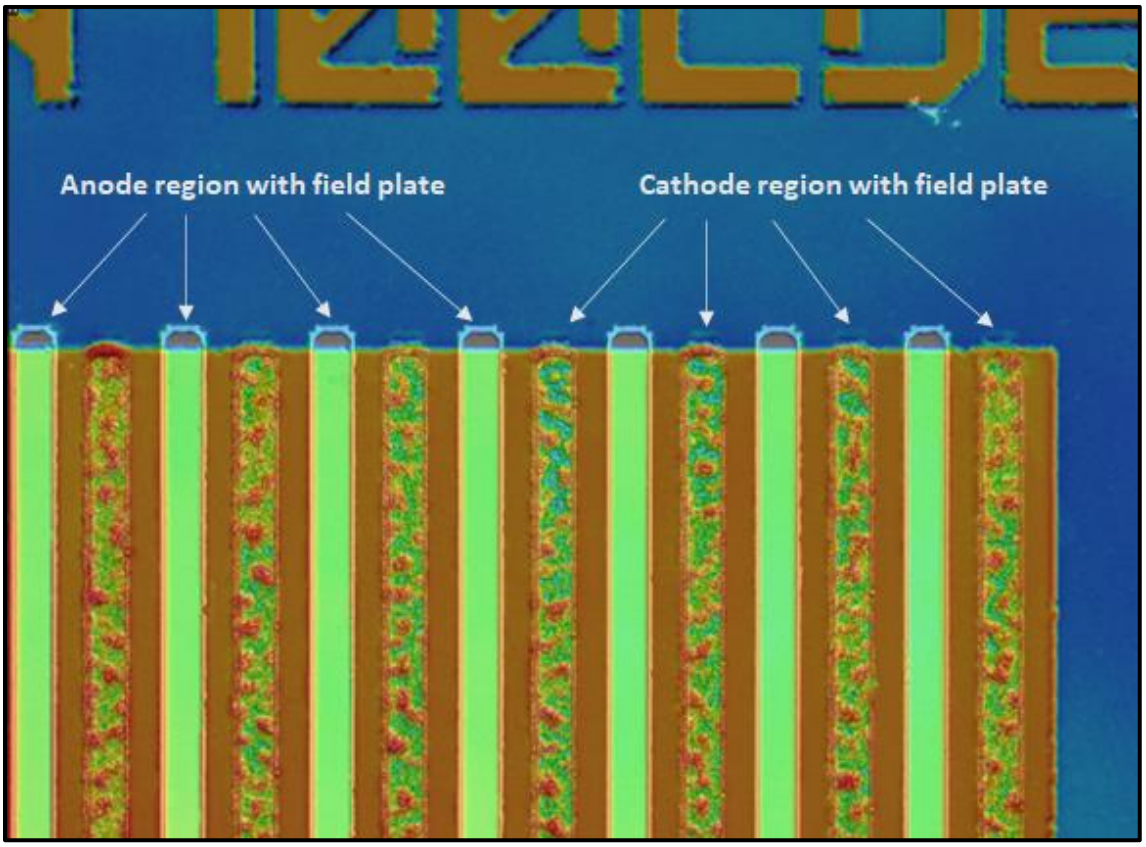


Fig. 5.5 Keyence Optical Profilometer image of fabricated finger device up till Schottky metal lift-off for device dimension analysis

5.2 Transmission Line Measurement (TLM) Method

The Transmission Line Measurement or TLM method is widely used to determine the specific contact resistivity of metal-semiconductor interface in the semiconductor industry and research. The total resistance R_T between two contacts with a length L, width W, and separation distance d can be plotted as a function of d.

5.2.1 Specific Contact Resistance ρ_C Extraction

I-V measurement is carried out on each adjacent contact and the resistance is obtained through extracting the average value of the slope of the measured line. The resistance is then plotted as a function of the contact spacing d as shown in Figure 1 below.

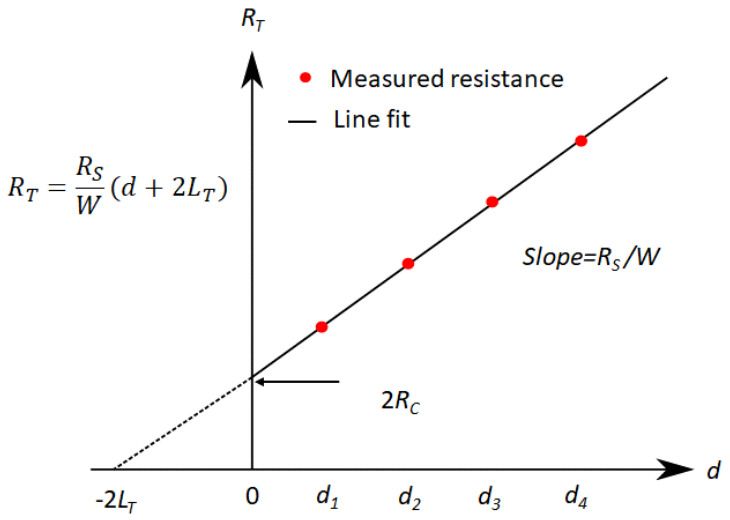


Fig. 5.6 Example of line fit against a plot of total resistance R_T as a function of TLM pad spacing d

The schematic diagram in Figure 5.8 (a) of the TLM pattern indicates that the total resistance R_T between adjacent pads is given by:

$$R_T = 2R_C + R_{semi} \tag{5.1}$$

Where R_C is the contact resistance associated with the metal/semiconductor interface and R_{semi} is the semiconductor resistance between the two adjacent pads.

The semiconductor resistance R_{semi} can be expressed using sheet resistance R_s, width of TLM pad W, and TLM pad spacing d

$$R_{semi} = R_s \frac{d}{W} \tag{5.2}$$

Hence, Equation (5.1) becomes:

$$R_T = \left(\frac{R_S}{W}\right) d + 2R_C \tag{5.3}$$

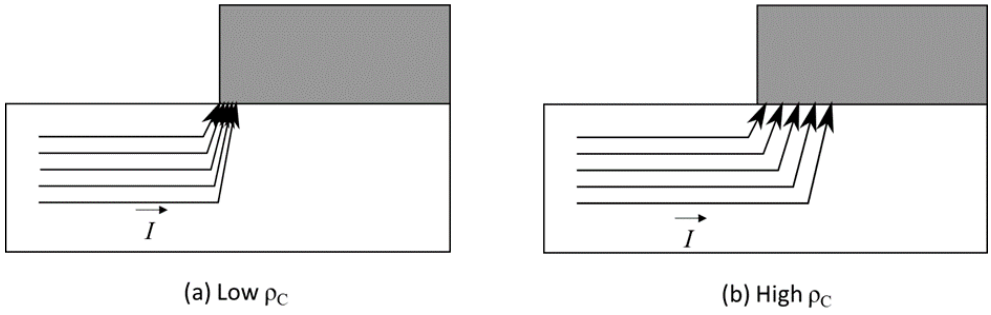


Fig. 5.7 Current flow into the contact for low and high ρ_C

The current flowing laterally through the semiconductor is uniform; however, the flow into the contact is not. At the edge of the contact, current density will be significantly high due to current crowding; however, at the opposite edge, the current drops until there is not any. Current crowding decreases in an exponential function with length L_T, known as the transfer length. This length can be described as the effective length of the contact. Hence, it can be said that the transfer length L_T is the average distance that an electron travels in the semiconductor beneath the contact before it flows up into the contact.

This can be expressed by the following equation:

$$L_T = \sqrt{\frac{\rho_C}{R_S}} \tag{5.4}$$

Where ρ_C is the specific contact resistance having a unit of $\Omega \cdot cm^2$ for standard quantity for comparison between different geometries and sizes. The relationship between specific contact resistance ρ_C and transfer length L_T is shown in Figure 2 with schematic illustration of the current flow. As the Figure 5.8 (a) indicates, the effective area of the contact can be expressed as $L_T \cdot W$ and then contact resistance R_C is:

$$R_C = \frac{\rho_C}{L_T \cdot W} = \frac{R_S L_T}{W} \tag{5.5}$$

Hence, Equation (5.3) becomes:

$$R_T = \frac{R_S}{W}(d + 2L_T) \tag{5.6}$$

When fitting a linear line using the above equation, against experimentally obtained plot of total resistance R_T as a function of spacing d, sheet resistance R_S, transfer length L_T, contact resistance R_C, and specific contact resistance ρ_C of the evaluated sample can be extracted.

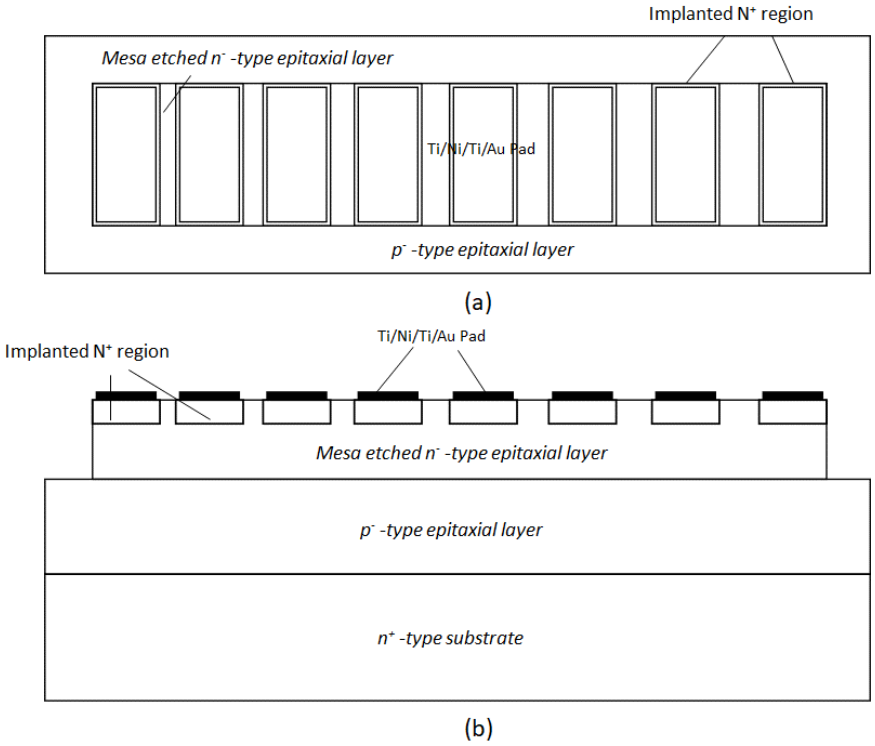


Fig. 5.8 Top view (a) and cross section (b) of fabricated TLM structure with implanted N^+ region

The structure of the linear TLM pattern used in this study is shown in Figure 5.8 (a) the top view and 3(b) the cross section. The TLM structure consists of eleven TLM contacts (260µm × 100µm) in a row with a different range of spacing: 5, 10, 15, 20, 25, 30, 35, 40, 45 and 50µm as shown in Figure 5.9. The contacts are patterned on to a rectangular mesa etched island in a dimension of 1375 µm ×260µm. It is important that this mesa etch reaches the depth up to the natural depletion layer of the n^- epi layer /p^- layer junction underneath to restrict the current flow only laterally between the intended distance of the pad separation.

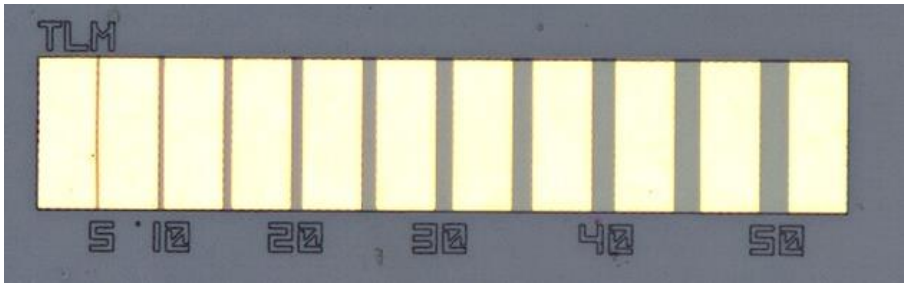


Fig. 5.9 A microscope image of fabricated TLM pattern for N^+ ohmic contact before 1050°C contact annealing

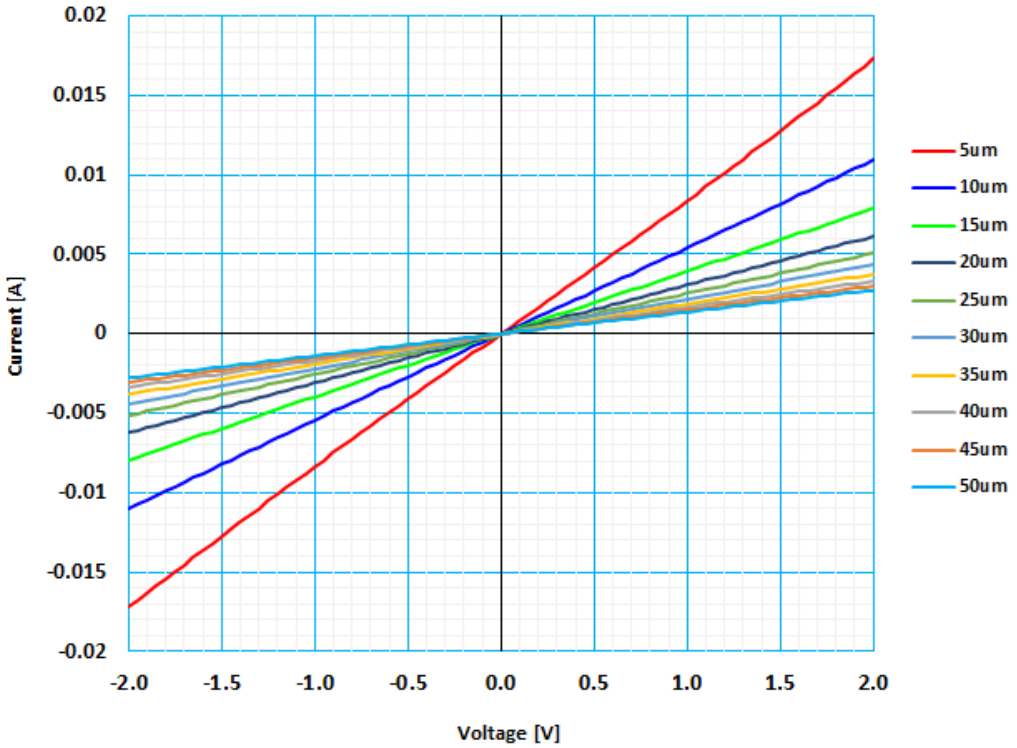


Fig. 5.10 I-V plots of evaluated TLM structures on old design epi with N^+ implant and activation at 1400°C

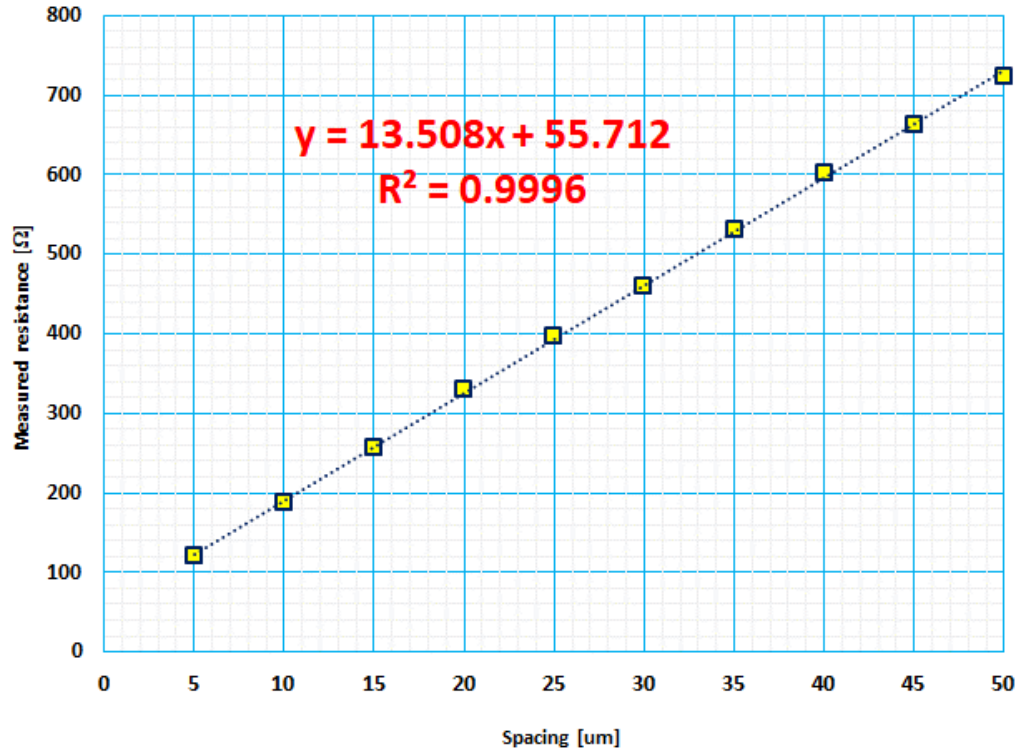


Fig. 5.11 Plots of the measured total resistance as a function of the contact electrode spacing with fitted line (old design epi at 1400°C activation)

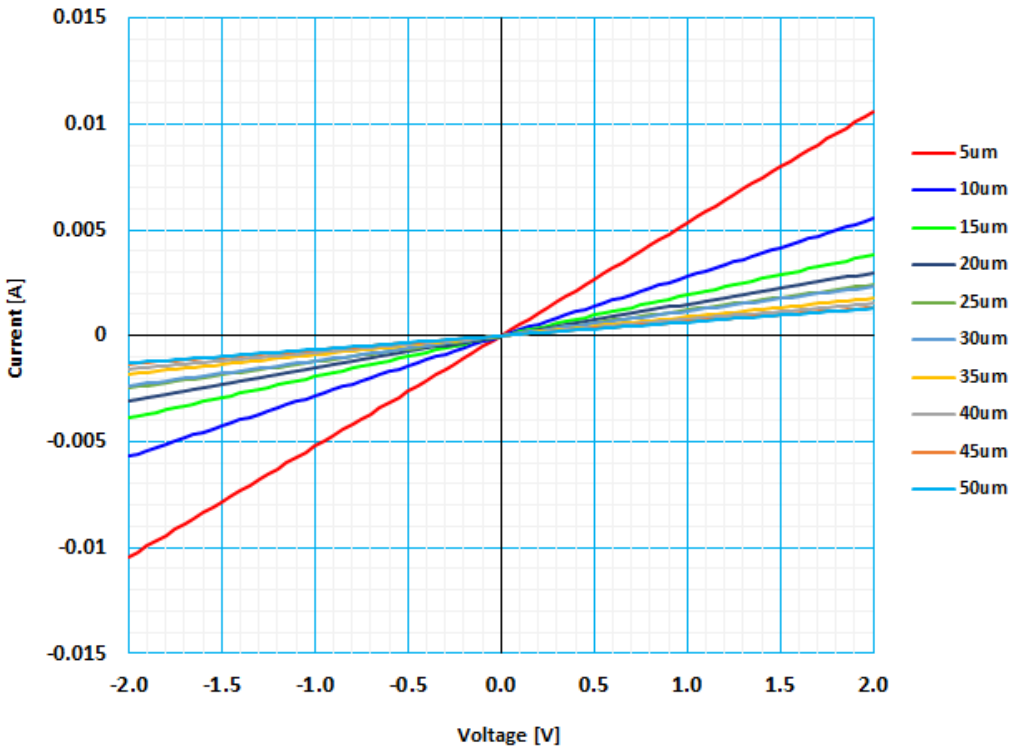


Fig. 5.12. I-V plots of evaluated TLM structures on old design epi with N^+ implant and activation at 1500°C

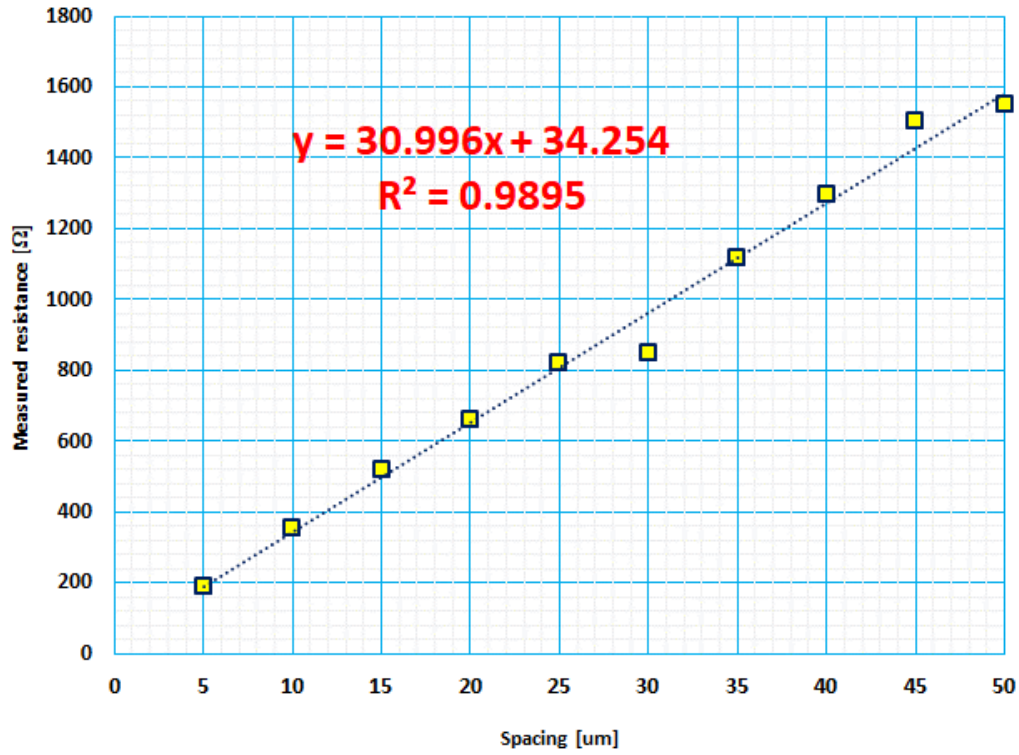


Fig. 5.13 Plots of the measured total resistance as a function of the contact electrode spacing with fitted line (old design epi at 1500°C activation)

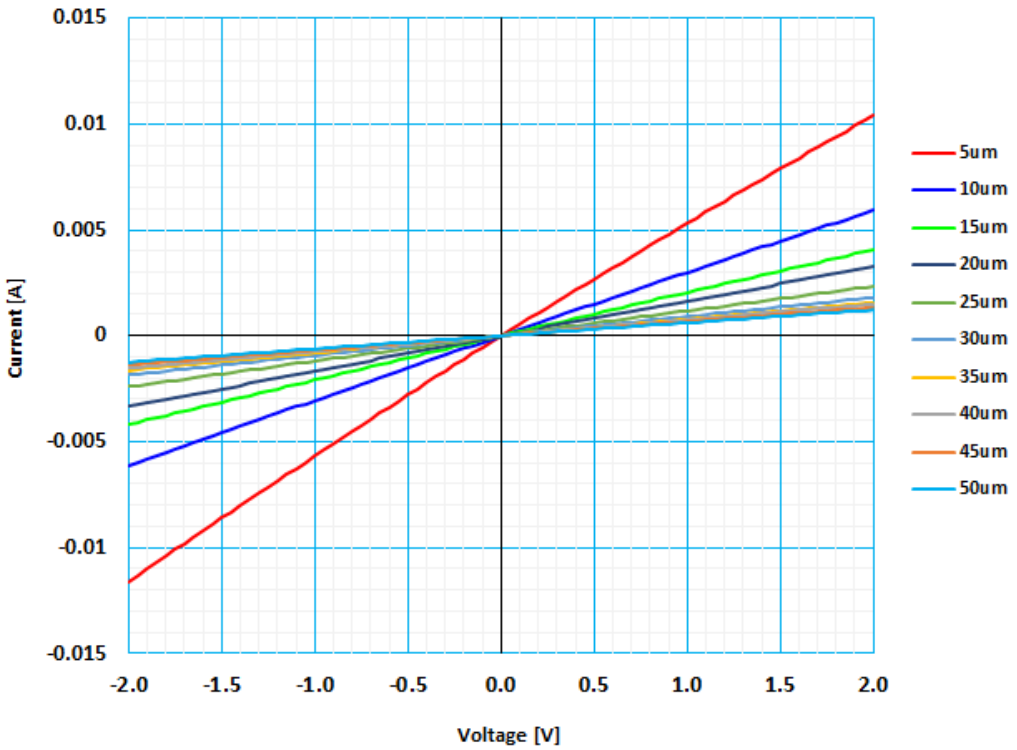


Fig. 5.14 I-V plots of evaluated TLM structures on Design 1 epi with N^+ implant and activation

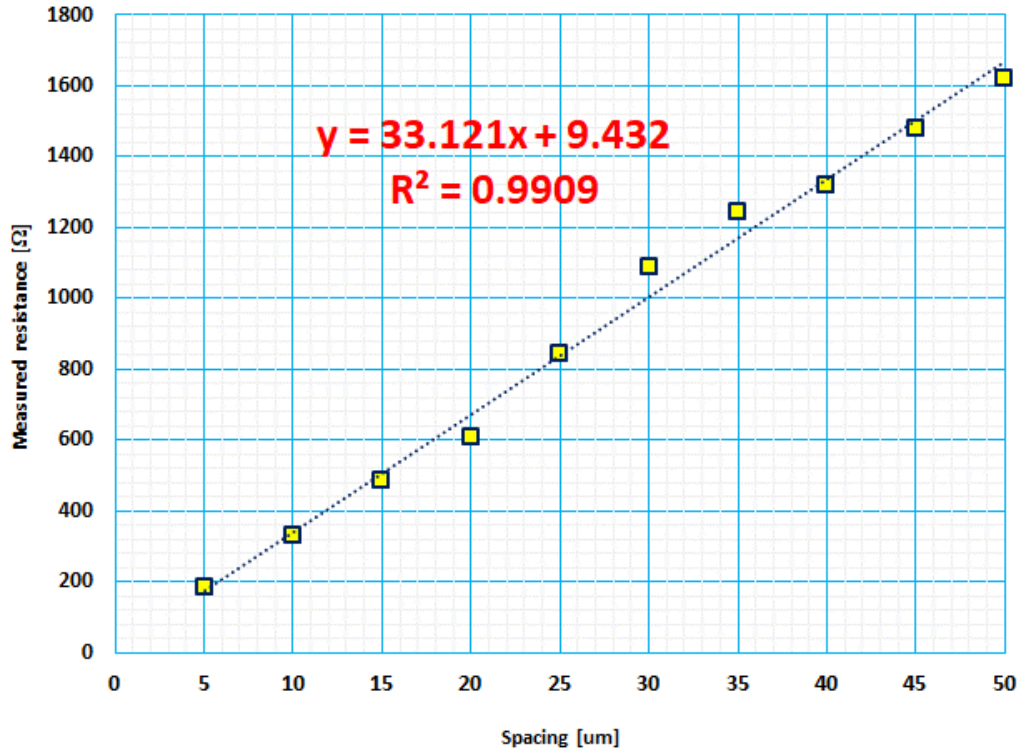


Fig. 5.15 Plots of the measured total resistance as a function of the contact electrode spacing with fitted line (Design 1 epi)

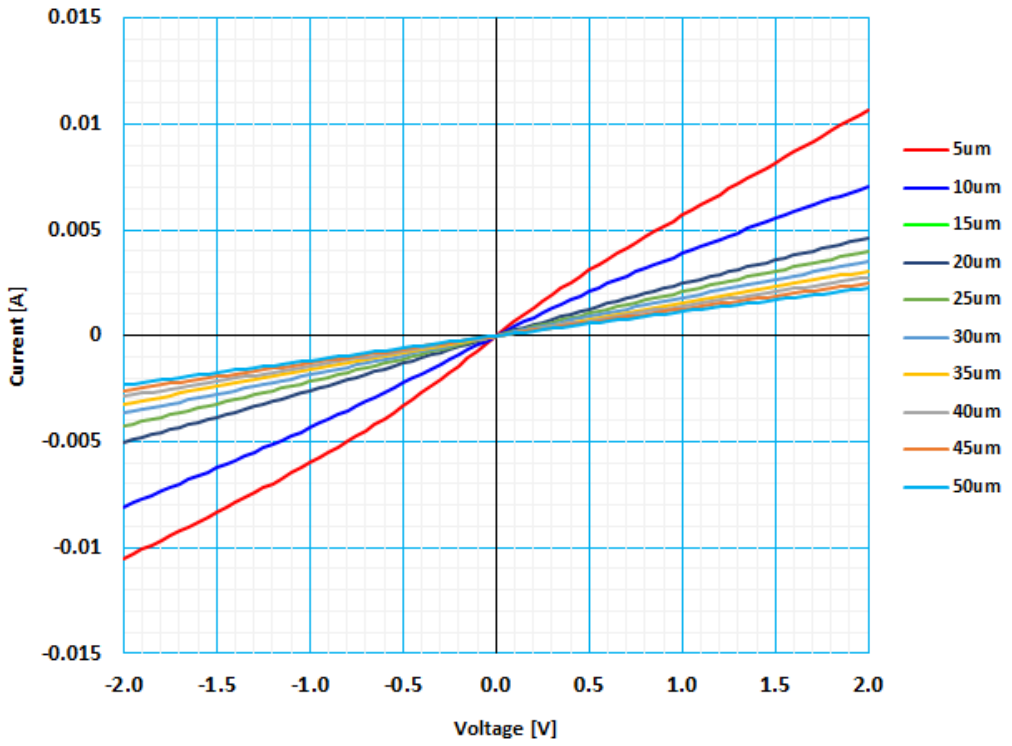


Fig. 5.16 I-V plots of evaluated TLM structures on Design 2 epi with N^+ implant and activation

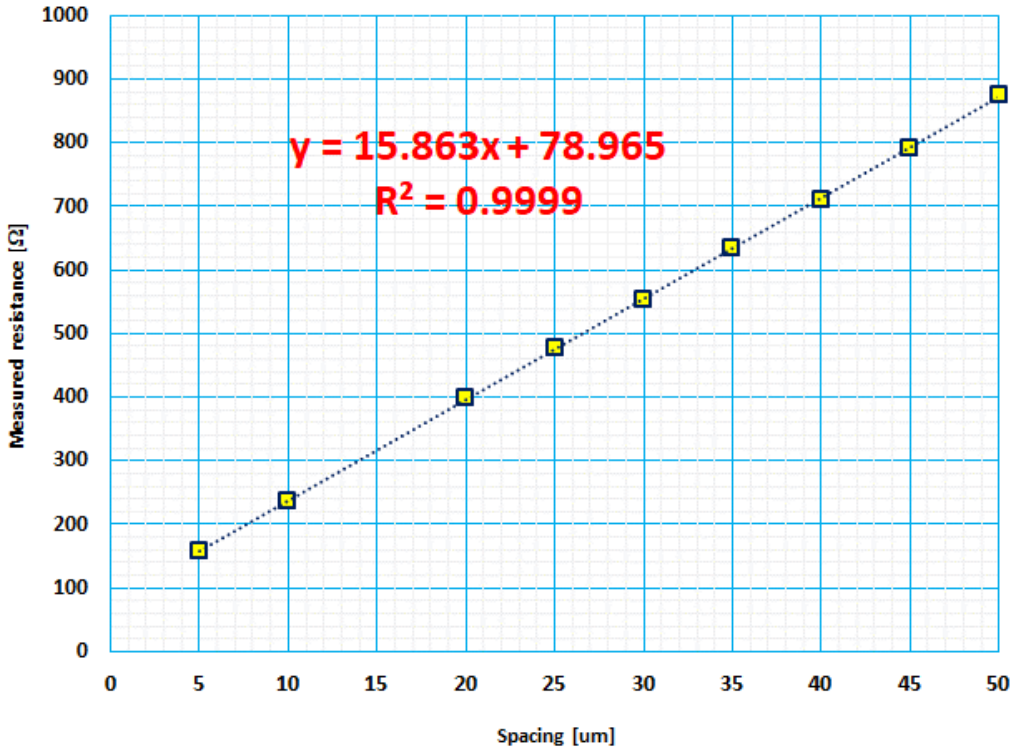


Fig. 5.17 Plots of the measured total resistance as a function of the contact electrode spacing with fitted line (Design 2 epi)

Table 5.2 Summary of parameters extracted from TLM measurement (Old Design Epi Activation at 1400℃)

Epi Specification	**Value**
Doping concentration	$2\times10^{17}cm^{-3}$
Thickness	0.4um
Parameter	**Value**
Contact Resistance R_C	27.86Ω
Sheet Resistance R_S	3512.08Ω/□
Transfer length L_T	2.062um
Specific contact resistance ρ_C	$1.494\times10^{-4}\Omega\cdot cm^2$
Bulk resistivity ρ	0.1405Ω·cm

Table 5.3 Summary of parameters extracted from TLM measurement (Old Design Epi Activation at 1500℃)

Epi Specification	**Value**
Doping concentration	$2\times10^{17}cm^{-3}$
Thickness	0.4um
Parameter	**Value**
Contact Resistance R_C	17.13Ω
Sheet Resistance R_S	8058.96Ω/□
Transfer length L_T	0.5526um
Specific contact resistance ρ_C	$2.461\times10^{-5}\Omega\cdot cm^2$
Bulk resistivity ρ	0.3224Ω·cm

Table 5.4 Summary of parameters extracted from TLM measurement (Design 1 Epi)

Epi Specification	**Value**
Doping concentration	$1.5\times10^{17}cm^{-3}$
Thickness	0.5um
Parameter	**Value**
Contact Resistance R_C	4.716Ω
Sheet Resistance R_S	8611.46 Ω /□
Transfer length L_T	0.1424um
Specific contact resistance ρ_C	$1.746\times10^{-6}\Omega\cdot cm^2$
Bulk resistivity ρ	0.4306Ω·cm

Table 5.5 Summary of parameters extracted from TLM measurement (Design 2 Epi)

Epi Specification	**Value**
Doping concentration	$1.2\times10^{17}cm^{-3}$
Thickness	0.7um
Parameter	**Value**
Contact Resistance R_C	39.48Ω
Sheet Resistance R_S	4124.38Ω/□
Transfer length L_T	2.489um
Specific contact resistance ρ_C	$2.555\times10^{-4}\Omega\cdot cm^2$
Bulk resistivity ρ	0.2887Ω·cm

5.2.2 Analysis of measured specific contact resistance ρ_C and TLM constraints and accuracy

The semiconductor layer thickness is not needed nor measured in by TLM and this leads to inaccuracy in measuring TLM on very thick layers or even on bare substrates. Thickness is the key parameter in measuring specific contact resistance ρ_C accurately. Also, from the extracted value, samples with higher sheet resistance between the 2 separated contacts tends to have lower contact resistance such as design 1 epi and old design epi activated at 1500℃. These 2 samples have thin top N^- epi layer thus resistance increase according to separation distance is high, thus bigger slope in fitted line equation. When there is an inaccuracy in some of the measurements for these bigger slope fitted lines, the y intercept (contact resistance) can mistakenly be interpreted smaller than the actual value. On the other hand, samples with thick top N^- epi layer tends to show higher specific contact resistance ρ_C than the actual value.

5.3 Evaluation and analysis of Lateral RESURF 4H-SiC Schottky Barrier Diodes

After fabricating both lateral RESURF Schottky barrier diode and MESFETs, DC *I-V* characteristics were measured using Keithley 2600-PCT-4B high voltage/ high current curve tracer connected to a micromanipulator probe station. For the lateral RESURF 4H-SiC Schottky barrier diode, forward *I-V* was evaluated with more accurate DC mode since the current ratings of the diodes are low and device self-heating is not a concern. Reverse *I-V* was evaluated in pulse mode.

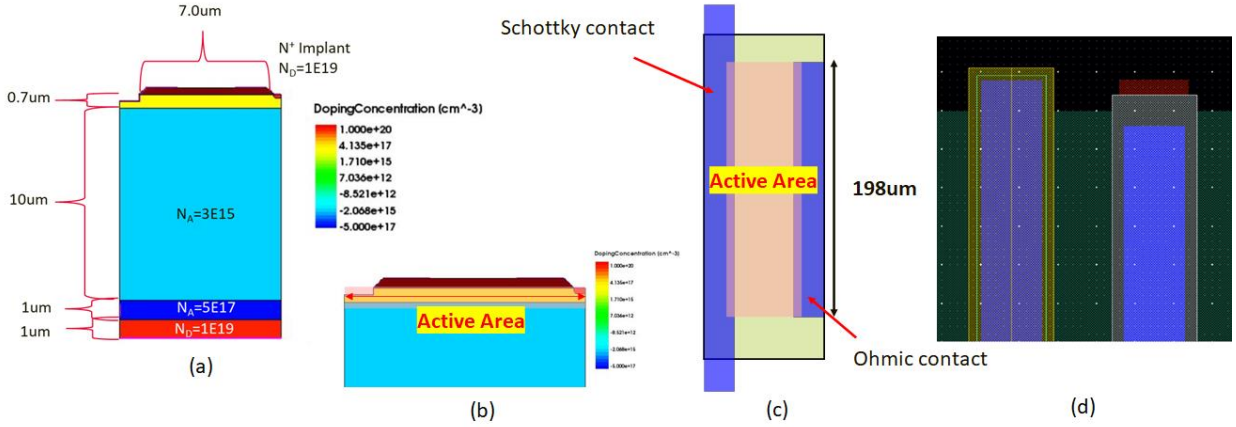


Fig. 5.18 Definition of active area for on-resistance calculation. unit cell from TCAD simulation (a) Active area length in simulated cell (b) same active area in mask layout diagram(c)and actual mask layout data

In above figures, the definition of active area for the calculation of the specific on-resistance RonAa is explained. Figure 5.18(a) and (b) from the TCAD simulation unit cell defines the length of the active area as drift region length + 0.5um contact width on both anode and cathode ends. Figure 5.18 (c) shows the width of the active area is defined as the length of the ohmic contact open. On-resistance is calculated from the differential resistance of the forward current with lowest point in the curve being extracted for specific on-resistance calculation.

Figure 5.19 shows the summary plot of on-resistance vs breakdown voltage of the fabricated lateral RESURF Schottky diode from the best performing epi wafer 2 sample. As known, because on-resistance and breakdown voltage are in a trade-off relationship, much of the high breakdown devices possess a higher on-resistance in the evaluated spectrum of the batch. There are few samples with on-resistance in the 1-digit mΩ order which show breakdown voltages around 400V. The evaluated highest vertical breakdown of the die is 675V and in theory it is unlikely that there will be a device that exceed this breakdown voltage. The evaluated vertical breakdown test pattern results are plotted in Figure 5.20. The optimum field plate length experimentally is at 5um length and the pattern without passivation and field plate shows increase in leakage current when electric field crowding is present.

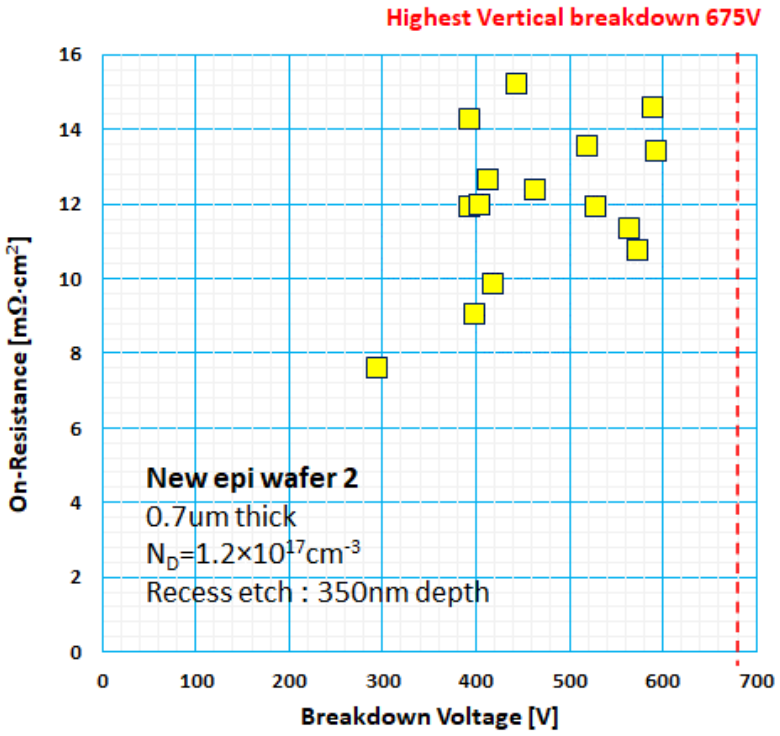


Fig. 5.19 Summary plot of on-resistance vs breakdown voltage of the fabricated lateral RESURF Schottky diode from the best performing epi wafer 2 sample

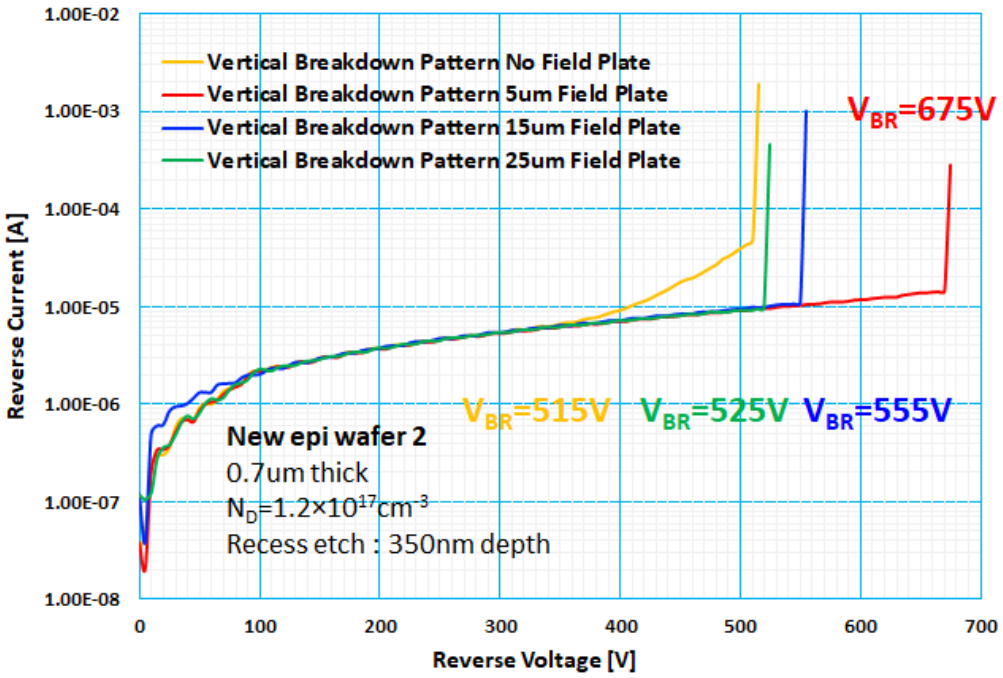


Fig. 5.20 Summary plot of vertical breakdown test pattern from newly designed epi wafer 2

5.3.1 Current conduction capability and number of fingers/widths of finger relationship

The vast majority of the discrete power devices (i.e., non-integrated) in the market today are vertical devices where the current conductions happen vertically for higher current density. Current rating of the device is proportional to its area, and the voltage blocking capability is achieved by the thickness of the vertical epitaxial region. To achieve the same current conduction capability with lateral power device, one needs to increase the number and the width of finger cells. Higher current rating lowers the on-resistance due to greater numbers of parallel cells, but this will increase the overall capacitance and slows down the switching speed. In figure 5.21 (a) shows the correlation of number of fingers (100um width) and current conduction capability of fabricated devices evaluated from epi wafer 2. In figure 5.21 (b) shows the correlation of width of fingers and current conduction capability of fabricated devices evaluated from epi wafer 2. From the projection from the fitted line, 1A current rating device will require 230 fingers of 100um width finger cells or 77 fingers of 300um width finger cells. The advantage of lateral device is that all device terminal will be formed on the top of the epitaxial wafer integration of multiple high-voltage power device will at ease. But to conduct as much current as vertical power device, lateral power device requires much larger surface area.

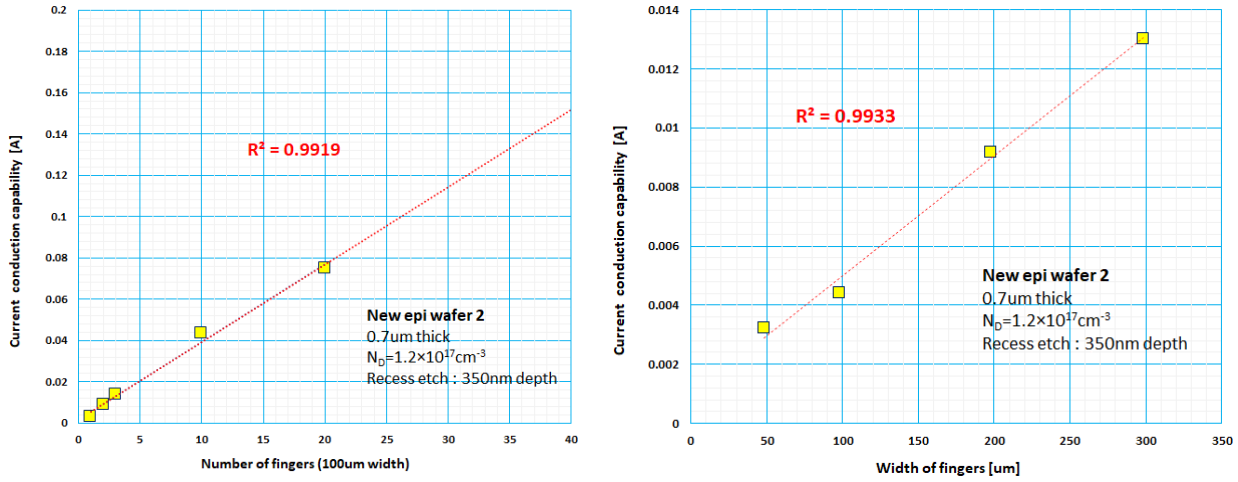


Fig. 5.21 Correlation of number of fingers (100um width) and current conduction capability from epi wafer 2 (a) and correlation of width of fingers and current conduction capability from epi wafer 2 (b)

5.3.2 Best performing lateral RESURF 4H-SiC Schottky barrier diode

In the following Figure 5.25~5.28, we present the best performing lateral RESURF 4H-SiC Schottky barrier diodes fabricated. Of the batch of fabricated device evaluated from the best epi wafer 2 sample, 2 samples showed the best reverse *I-V* performance or best forward *I-V* performance with the other complementary trade-off performance in acceptable value. The summaries are,

- Best forward performing diode: Specific on-resistance of 10.226 $m\Omega \cdot cm^2$ with breakdown voltage of 575V (Device name: 1FD200W100LD350FPC8V1)
- Best reverse performing diode: Specific on-resistance of 14.713 $m\Omega \cdot cm^2$ with breakdown voltage of 595V (Device name: 2FD40W90LD300FPC8V1)

There are many other attributes of evaluated results other than the above extracted value that are worth pointing. Compared to previous fabrication run, majority of evaluated *I-V* curves show clean and smooth curves with minimum noise observed during evaluation. This is from the modification made on the final Al metallization dry and wet etch process. During the final process, photoresist was kept on (Figure 5.22) during electrical evaluation check so that it was possible to do additional etch/cleaning of the Al residue after noises were observed. DC power for the etch recipe was lowered so that long duration cleaning was possible with minimum damage done to the Si_3N_4 passivation underneath. As seen in Figure 5.22, multiple microscope image and electrical evaluation check were performed to insure there were no unetched residue which shorted the finger Al lines. The underneath passivation remains smooth from the soft low power dry etch performed for cleaning.

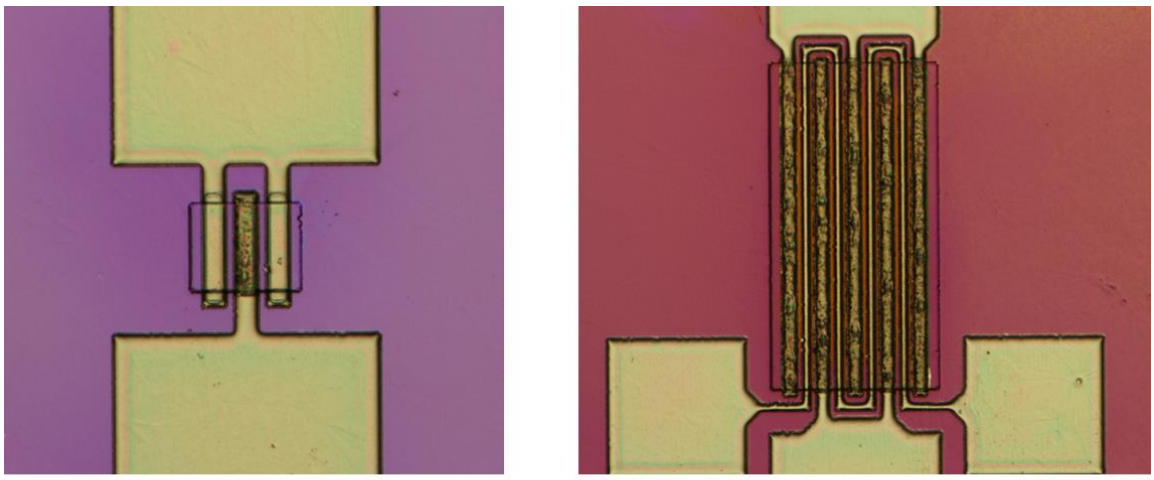


Fig. 5.22 Microscope image of final fabricated device after Al metallization etch with photoresist finger Schottky barrier diode (a) and finger MESFET (b)

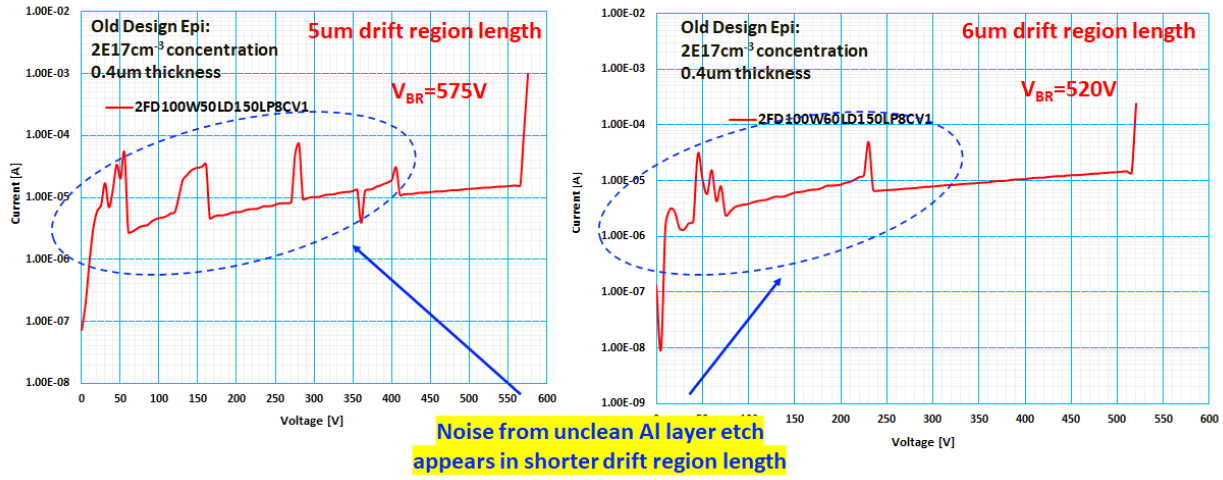


Fig. 5.23 Example of noise observed from previous fabrication during reverse I-V evaluation when Al metallization residue is not cleaned

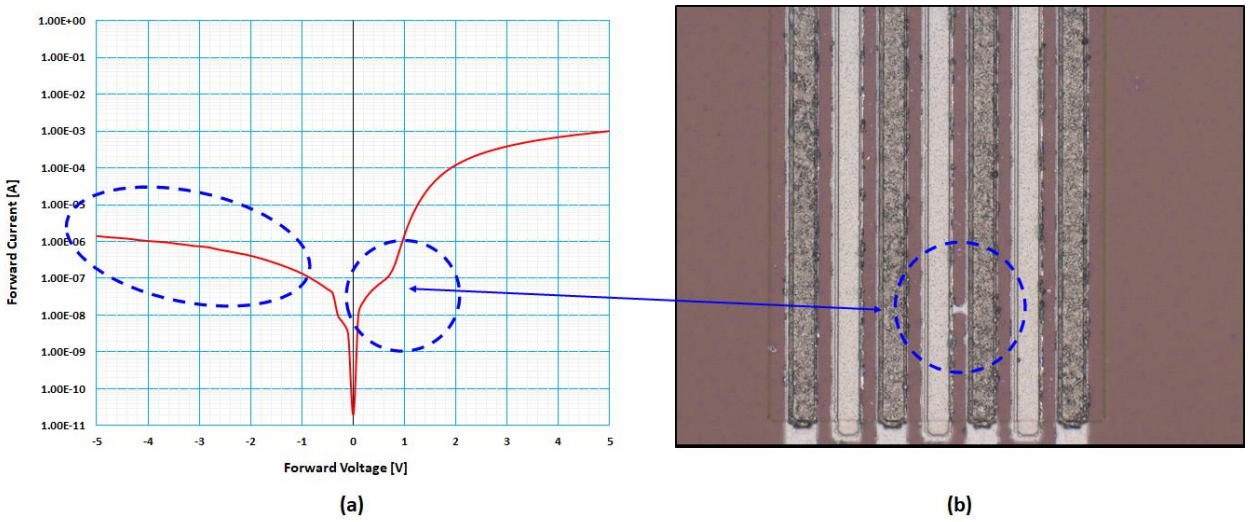


Fig. 5.24 Example of shorted device from unclean photoresist development leading to high leakage I-V (a) and microscope image of problematic spot (b)

Another attribute is forward current conduction of devices fabricated with epi wafer 2 have an influence of the "JFET effect" from the underneath p^- epi layer. When positive bias is applied to the anode Schottky contact, the n^-drift region/p^- epi layer depletes and the effective thickness of the n- drift region for current conduction slightly decreases. This can be seen at forward voltage of around 2V as shown in Figures 5.25 and 5.27 as a slight curvature in the forward *I-V* curve. Epi wafer 2 has the lightest doping in the n- drift region of all epitaxial wafer ordered. As the result this influence is seen strongly from the fabricated devices from epi wafer 2 sample.

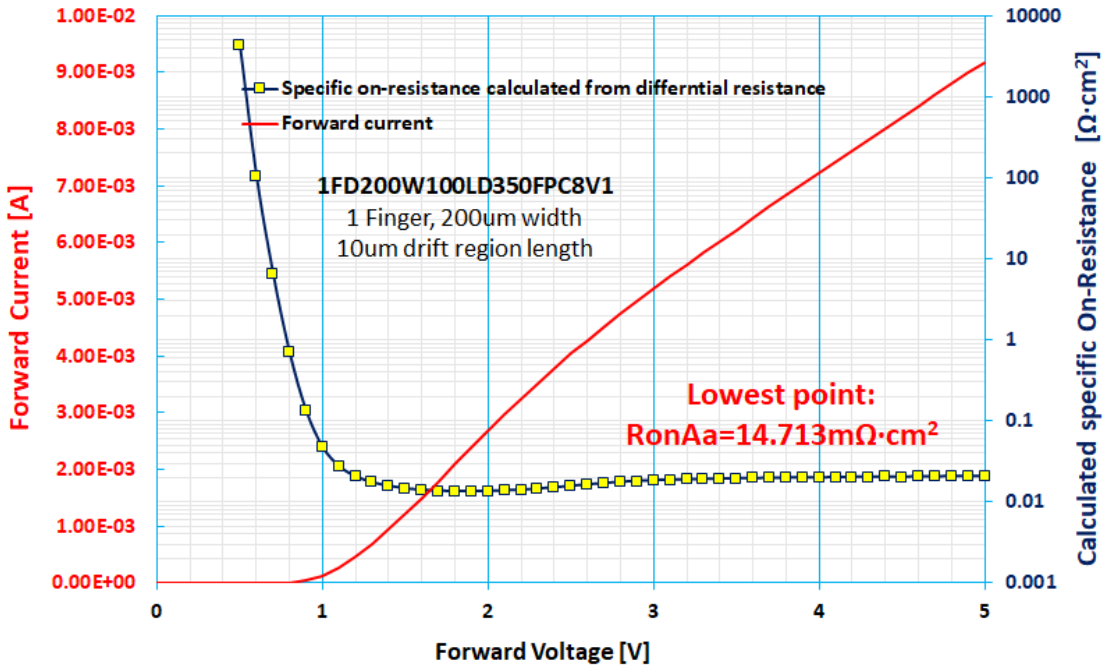


Fig. 5.25 Forward I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (1FD200W100LD350FP8V1) and calculated specific on-resistance

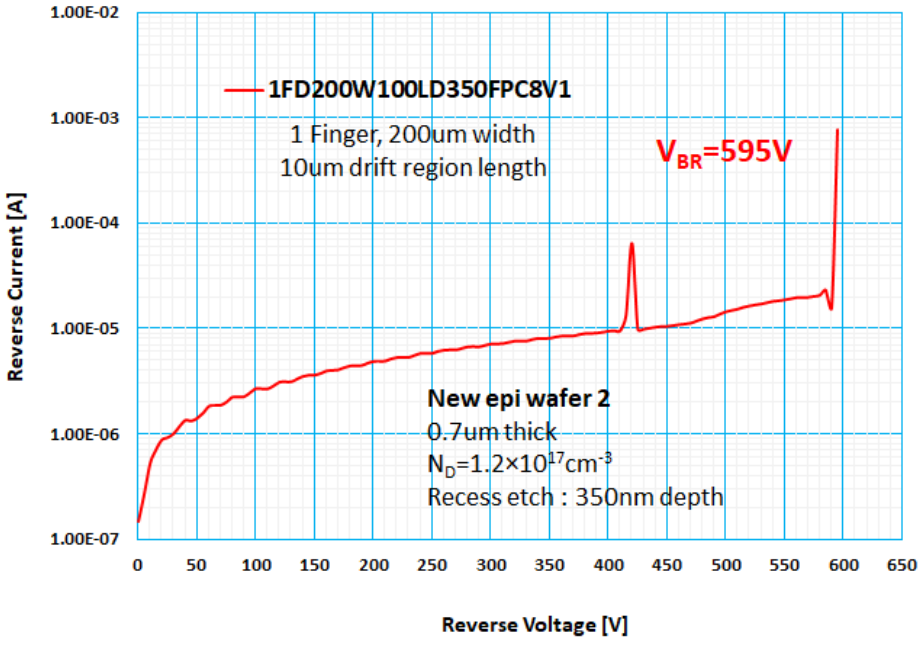


Fig. 5.26 Reverse I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (1FD200W100LD350FP8V1)

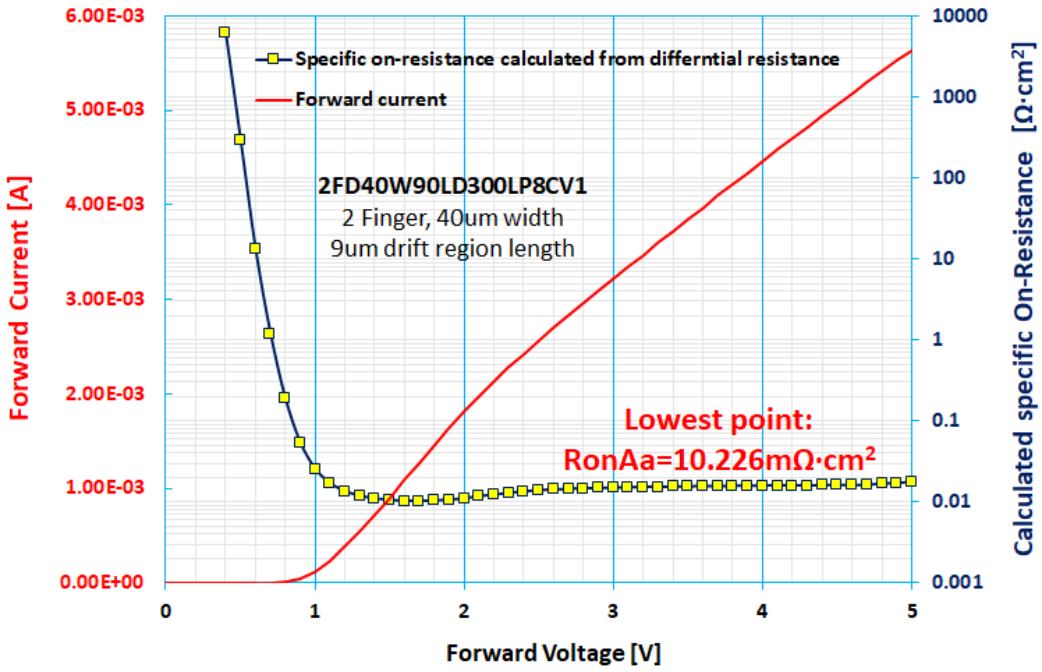


Fig. 5.27 Forward I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (2FD40W90LD350FP8V1) and calculated specific on-resistance

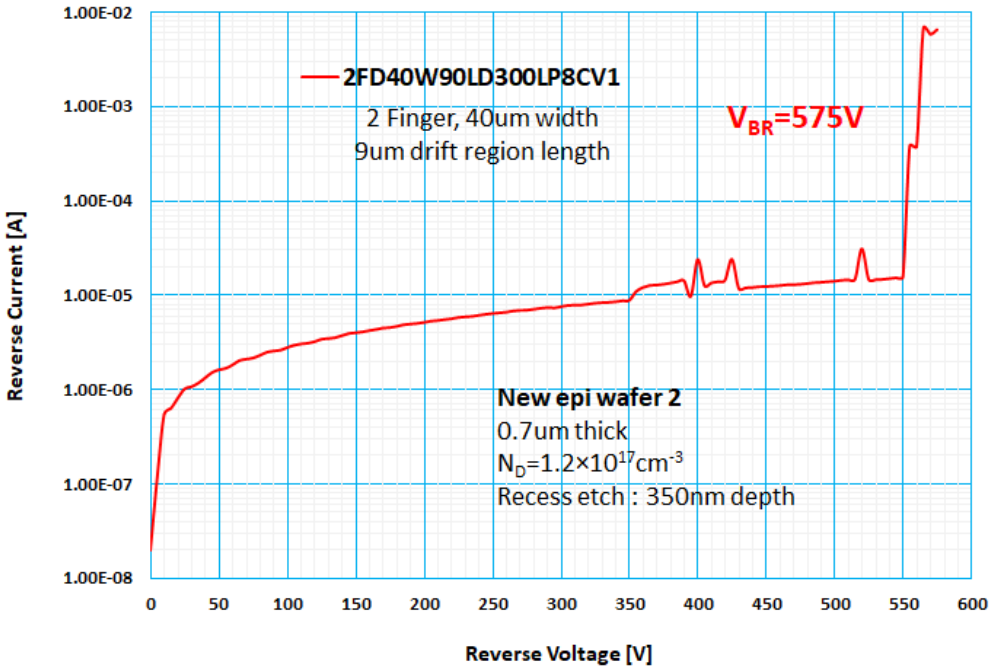


Fig. 5.28 Reverse I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (2FD40W90LD350FP8V1)

5.3.3 Comparison of N^+ implanted and non-implanted devices among different epitaxial wafers

In this section, we compare the impact of N^+ implant process to both forward and reverse performance of the device between different epi wafer specifications. The comparison is conducted using the same mask patterned device for the N^+ implanted and non-implanted device. From the high phosphorus implant on the cathode region, the contact resistance is reduced significantly, and current conduction improves by a factor of more than 100. While in both cases of the epi wafer variation, the breakdown voltage decreases by ~200V after the N^+ implant is performed. There is no significant leakage current increase in both cases of the epi wafer variation indicating that crystal damage may not be the primarily reason in the breakdown voltage lowering. Further analysis for lowering of vertical voltage blocking capability after N^+ implant is discussed in chapter 6 using SIMS analysis of the implanted doping profile. Overall, new epi wafer 1 tends to block better since it possess a thicker p^- epi layer for higher vertical breakdown, while the original epi wafer has a better forward performance from the higher doping concentration of the n^- drift region.

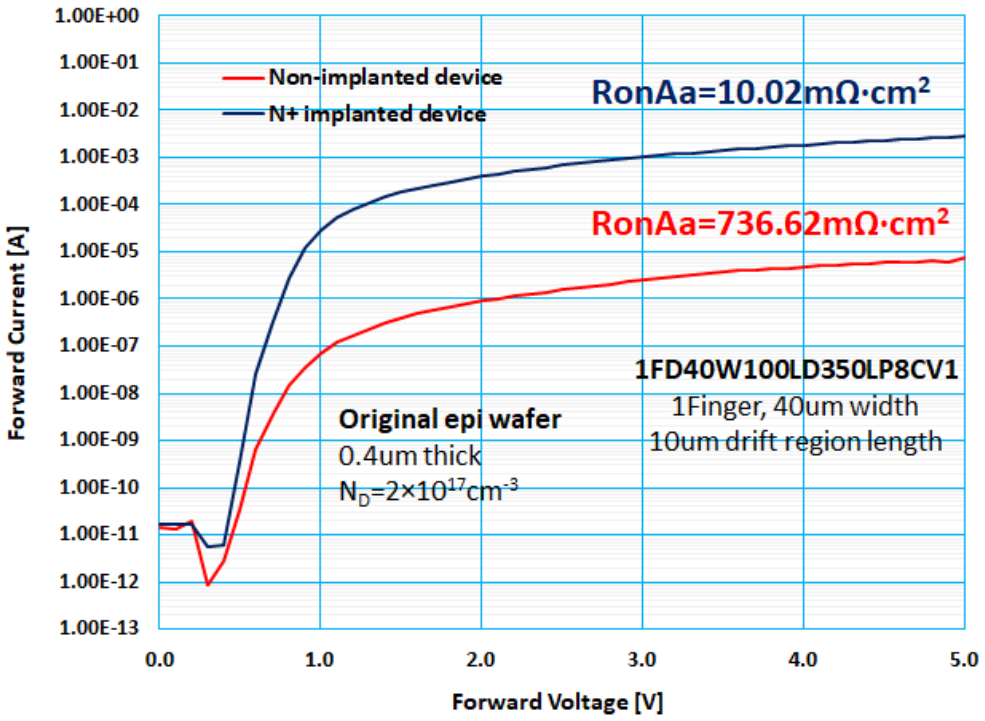


Fig. 5.29 Comparison of forward I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (1FD40W100LD350FP8V1) with and without N^+ implant and calculated specific on-resistance

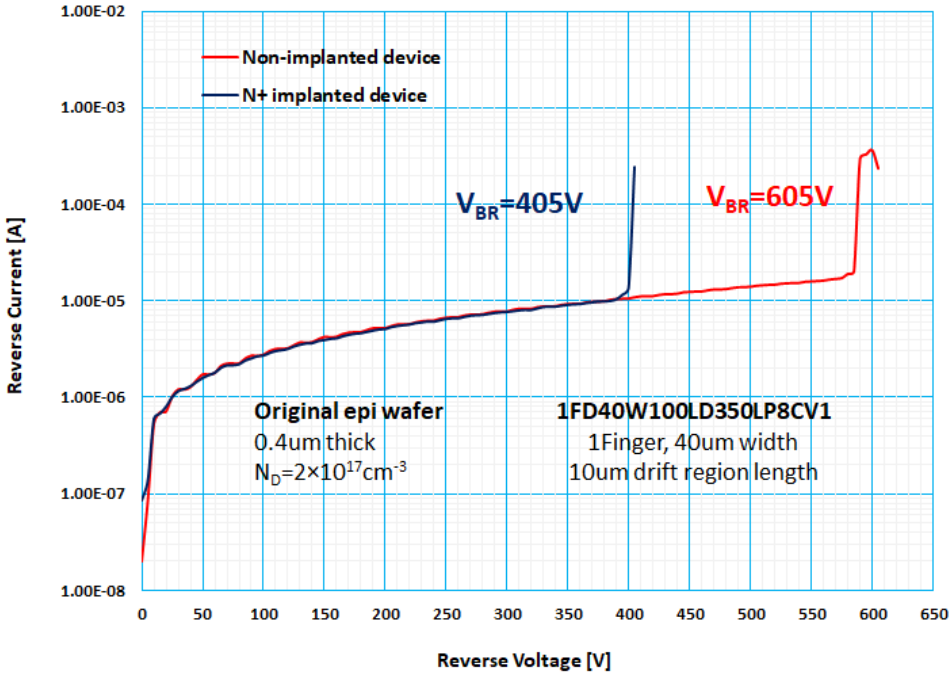


Fig. 5.30 Comparison of forward I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (1FD40W100LD350FP8V1) with and without N^+ implant and calculated specific on-resistance

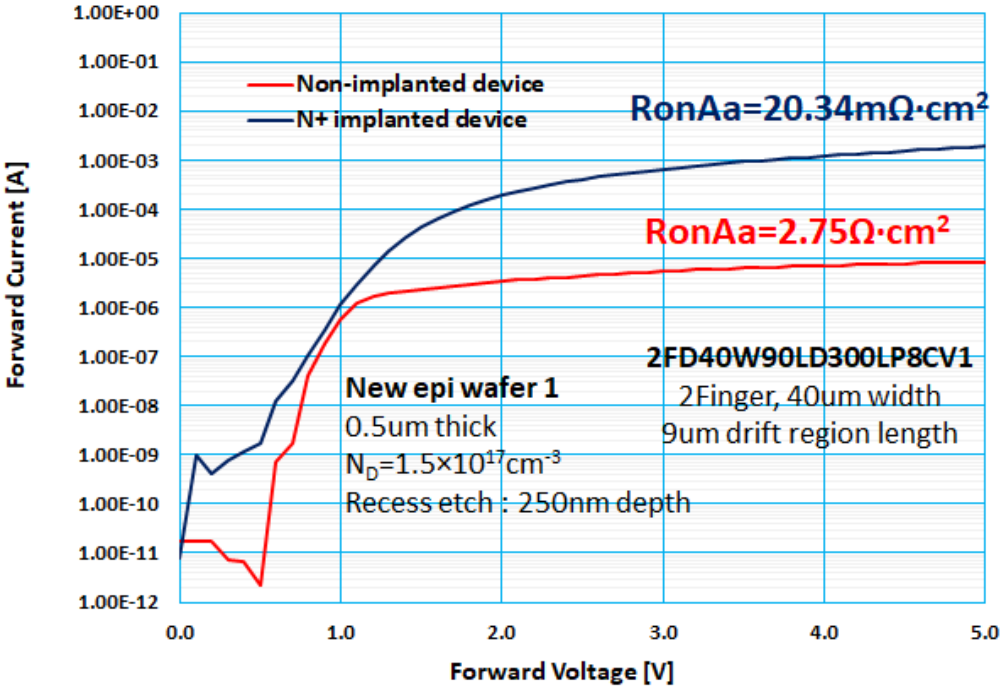


Fig. 5.31 Comparison of forward I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (2FD40W90LD300FP8V1) with and without N^+ implant and calculated specific on-resistance

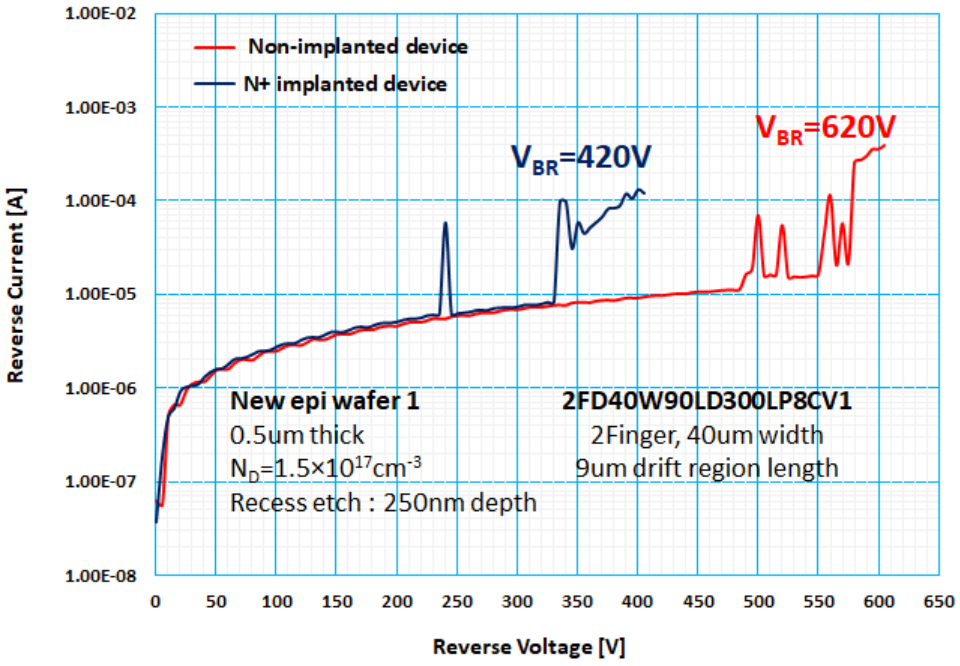


Fig. 5.32 Comparison of forward I-V characteristics of fabricated Lateral RESURF Schottky barrier diode (1FD40W100LD350FP8V1) with and without N^+ implant and calculated specific on-resistance

5.4 Experimental Determination of the Schottky Barrier Height

The Schottky barrier height of Ni/SiC contact can be experimentally determined by either current-voltage (*I-V*) or capacitance-voltage (*C-V*) measurements. In this research project, the barrier height will be calculated by extrapolating the saturation current I_s from semi-log plot of the forward *I-V* curve. If thermionic emission (TE) dominates the carrier transport mechanism, the Schottky diode current *I* will be given by:

$$I = AA^*T^2 e^{-\frac{q\Phi_{BN}}{kT}}\left(e^{\frac{qV}{nkT}} - 1\right) \tag{5.7}$$

The latter parameter expresses all the effects that make the contact non-ideal (e.g. inhomogeneity of the barrier height, etc.)

When the diode is forward-biased, for V>>kT/q, the above equation (5.7) can be written as follows:

$$I = AA^*T^2 e^{-\frac{q\Phi_{BN}}{kT}} e^{\frac{qV}{nkT}} = I_S e^{\frac{qV}{nkT}} \tag{5.8}$$

A is the device area, and A* is the effective Richardson constant for silicon carbide and has a value of 146 $A \cdot cm^{-2} \cdot K^{-2}$. I_s is the saturation current for the Schottky contact. q is the electron charge, k is the Boltzmann constant, T is the absolute temperature and n is the ideality factor.

By plotting the forward *I-V* characteristics in a semi-log scale, it becomes possible to fit the above equation (5.8) to the experimental data in the linear portion of the curve. This allows determining the saturation current I_s by extrapolating this fitted line to the y axis intercept or to zero volts. Saturation current I_s is expressed as:

$$I_s = AA^*T^2 e^{-\frac{q\Phi_{BN}}{kT}} \tag{5.9}$$

From the above equation, Schottky barrier height Φ_{BN} can be calculated as follows:

$$\Phi_{BN} = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_s}\right) \tag{5.10}$$

The obtained value for the barrier height is 1.236eV. It is known that Schottky barrier height Φ_{BN} is independent to the donor concentration N_D of the epi layer for most cases. Only image force lowering of the barrier $\Delta\Phi_{BN}$ is dependent on N_D and with $N_D=1.2\times10^{17}$ cm^{-3} being high for the fabricated diode, it agrees that the obtained barrier height Φ_{BN} is smaller than the reference value (Table 5.6).

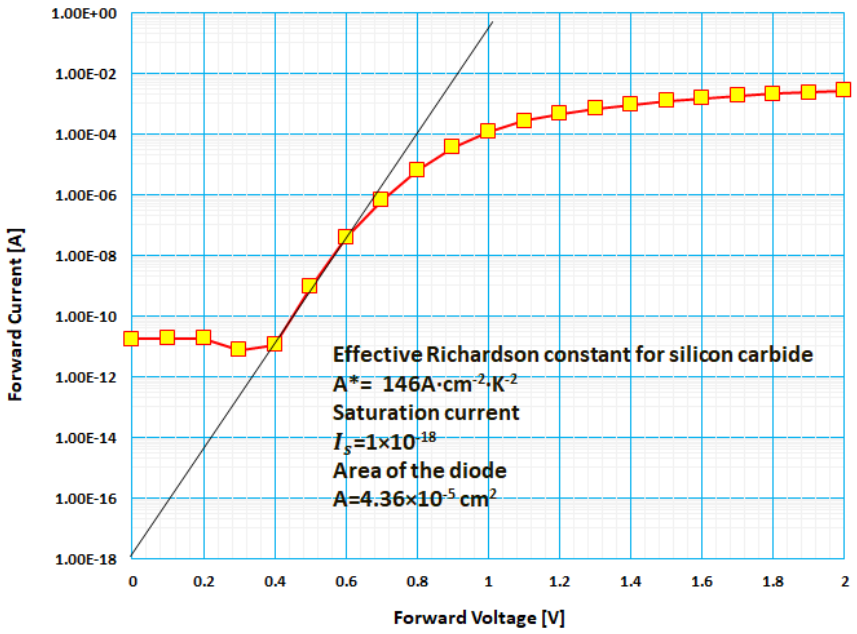


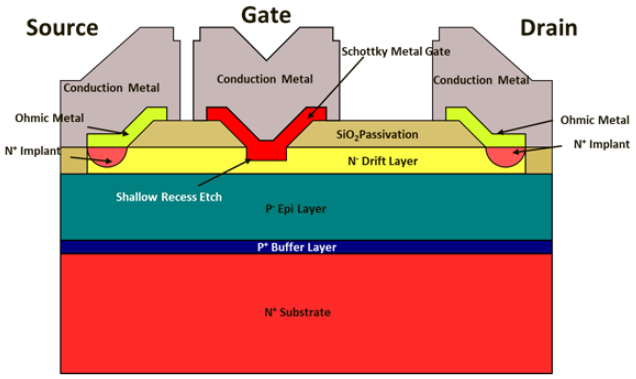
Fig.5.33 Extraction of the Schottky barrier height from the linear fit of the forward *I-V* characteristics of a fabricated lateral RESURF 4H-SiC Schottky diode in a semi-log scale

Table 5.6 Schottky barrier height ($q\Phi_{BN}$) for major metals on *n*-type 4H-SiC (0001)

Schottky barrier height on *n*-type 4H-SiC (0001)					
Metal	$q\Phi_{BN}$ (eV)		n	Annealing Temperature	Ref.
Ti	1.10	1.15	1.03	As deposited	[23]
Ti	1.20		1.23	As deposited	[24]
Ti	1.20	1.21	1.03	400℃	[25]
Ti	1.23	1.32	1.02	500℃	[26]
Ti	1.27		1.04	N.A.	[27]
Ni	1.32			As deposited	[28]
Ni	1.40		1.10	As deposited	[29]
Ni	1.45	1.65	1.10	As deposited	[30]
Ni	1.60	1.70	1.01	As deposited	[31]
Au	1.73	1.80	1.08	As deposited	[30]
Pt	1.39		1.01	Sputtering at 200℃	[32]
Pt	1.817	1.883	1.08	As deposited	[33]

* The majority of above Schottky barrier diodes were fabricated on epitaxial layer with doping concentration in the order of 10^{15}~10^{16}cm^{-3}

5.5 Evaluation and analysis of 4H-SiC Lateral RESURF MESFETs



(a)

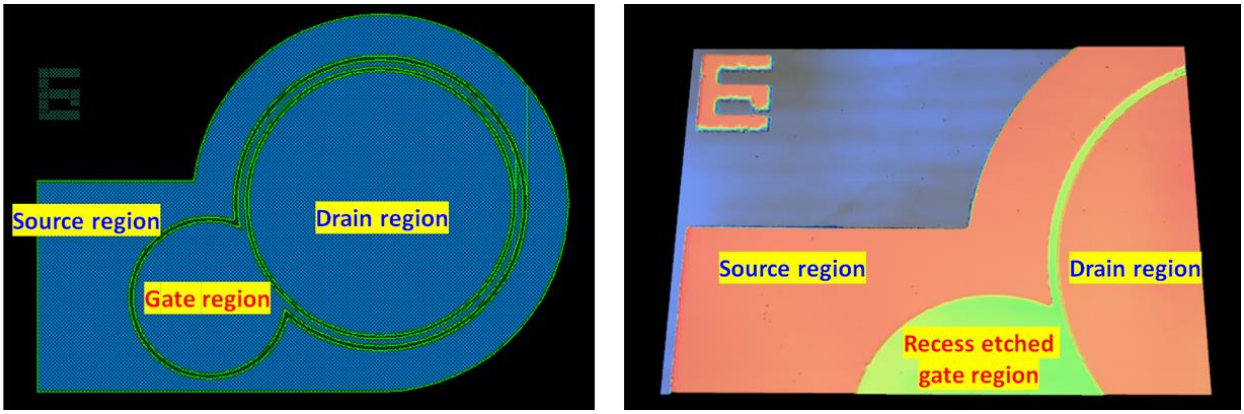
MESFET device design parameters

Parameters	Values
Drift region length	4um
D-S length (gate)	12um (4um)
Field plate length	1um
Passiavation Thickness	0.4um
N^- Epi Drift Concentration	2×10^{17} cm^{-3}
P^- Epi Concentration	5×10^{15} cm^{-3}
P^+ Buffer Concentration	5×10^{17} cm^{-3}
N^- Epi Drift Thickness	0.4um
P^- Epi Thickness	3.2um
P^+ Buffer Thickness	1um

(b)

Fig. 5.34 Cross section of proposed lateral RESURF 4H-SiC MESFET with recessed gate (a) and optimum epitaxial design specification (b)

Figure 5.34 shows the proposed lateral RESURF 4H-SiC MESFET with recessed gate structure. Shallow recess etch under the gate is an effective method to reduce pinch-off voltage of the device, especially when the channel region is doped heavily from the intended RESURF design.



(a) (b)

Fig. 5.35 Circular type mask layout of proposed lateral RESURF 4H-SiC MESFET (a) and Keyence optical profilometer image of the device after recess etch (b)

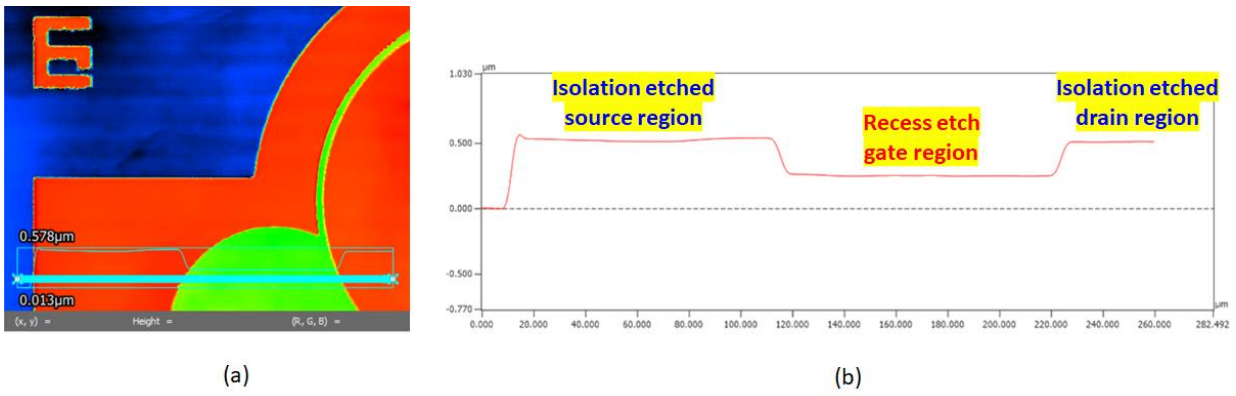


Fig. 5.36 Keyence optical profilometer image of the device after recess etch (a) and scanned height profile along the recess etch gate region

5.5.1 Pinch-off voltage of MESFET and necessary recess etch depth

By applying a bias to the gate junction, the depletion depth and therefore the resistance of the current flow between the source and drain and the saturation current can be controlled. If a large enough negative gate bias is applied, the depletion region depth will reach the channel depth, and the channel will be pinched off. This gate bias is called the internal pinch-off voltage V_{p0} and is given by the following equation;

$$V_{p0} = \frac{qN_d d^2}{2\varepsilon_s} \tag{5.11}$$

where, q is the electron charge, N_D is the doping concentration in the drift region, d is the hight of the channel , ε_0 is permittivity of free space, ε_r is relative dielectric constant, and $\varepsilon_s = \varepsilon_r \times \varepsilon_0$.

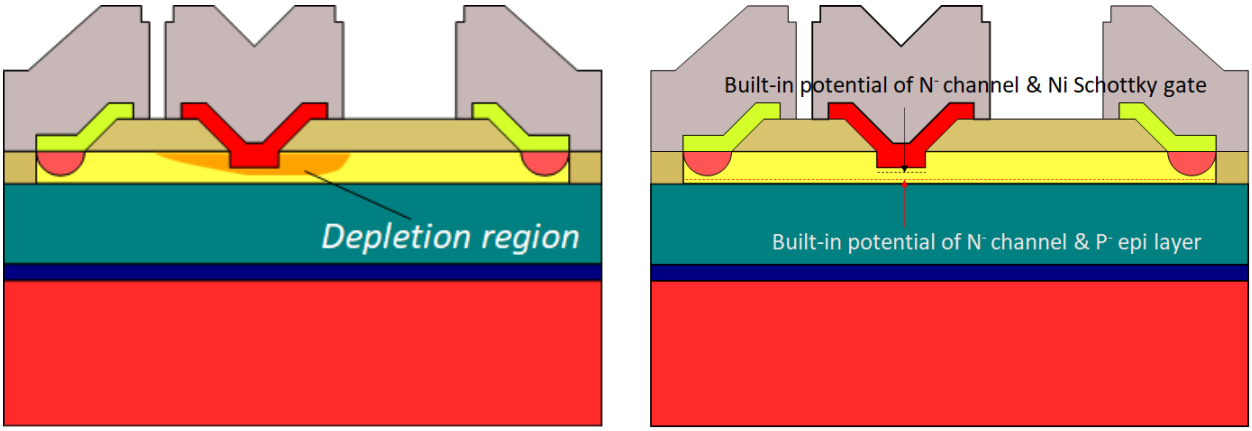


Fig. 5.37 Cross section diagram of lateral RESURF 4H-SiC MESFET explaining built-in potential and gate operation

Besides this internal pinch-off voltage, our lateral RESURF 4H-SiC MESFETs have built in potential barriers forming from both top Schottky barrier gate and bottom p^- epitaxial layer at thermal equilibrium as shown on above figure. Considering these potentials as 2nd and 3rd terms in the calculation of pinch off voltage, the equations can be expressed as the following.

Built-in potential barrier from n^- channel and p^- epi layer is expressed as follows,

$$V_{bi(bottom)} = \frac{kT}{q} ln\left(\frac{N_A \cdot N_D}{{n_i}^2}\right) \tag{5.12}$$

where N_A is the doping concentration of the bottom p^- epi layer, N_D is the doping concentration of the n^- channel layer, and n_i is the intrinsic carrier concentration, k is the boltzmann constant, and T is the temperature in kelvin.

Built-in potential barrier from n^- channel and Ni Schottky gate is expressed as follows,

$$V_{bi(bottom)} = \Phi_{Bn} - V_n \tag{5.13}$$

where Φ_{Bn} is the barrier height of Ni Schottky gate and V_n can be expressed,

$$V_n = \frac{kT}{q} ln\left(\frac{N_C}{N_D}\right) \tag{5.14}$$

where N_C is the conduction band density of states. The final pinch-off voltage V_p is expressed as following,

$$V_p = V_{p0} - V_{bi(bottom)} - V_{bi(top)}$$

$$V_p = \frac{qN_d d^2}{2\varepsilon_s} - \frac{kT}{q} ln\left(\frac{N_A \cdot N_D}{{n_i}^2}\right) - \Phi_{Bn} - \frac{kT}{q} ln\left(\frac{N_C}{N_D}\right)$$

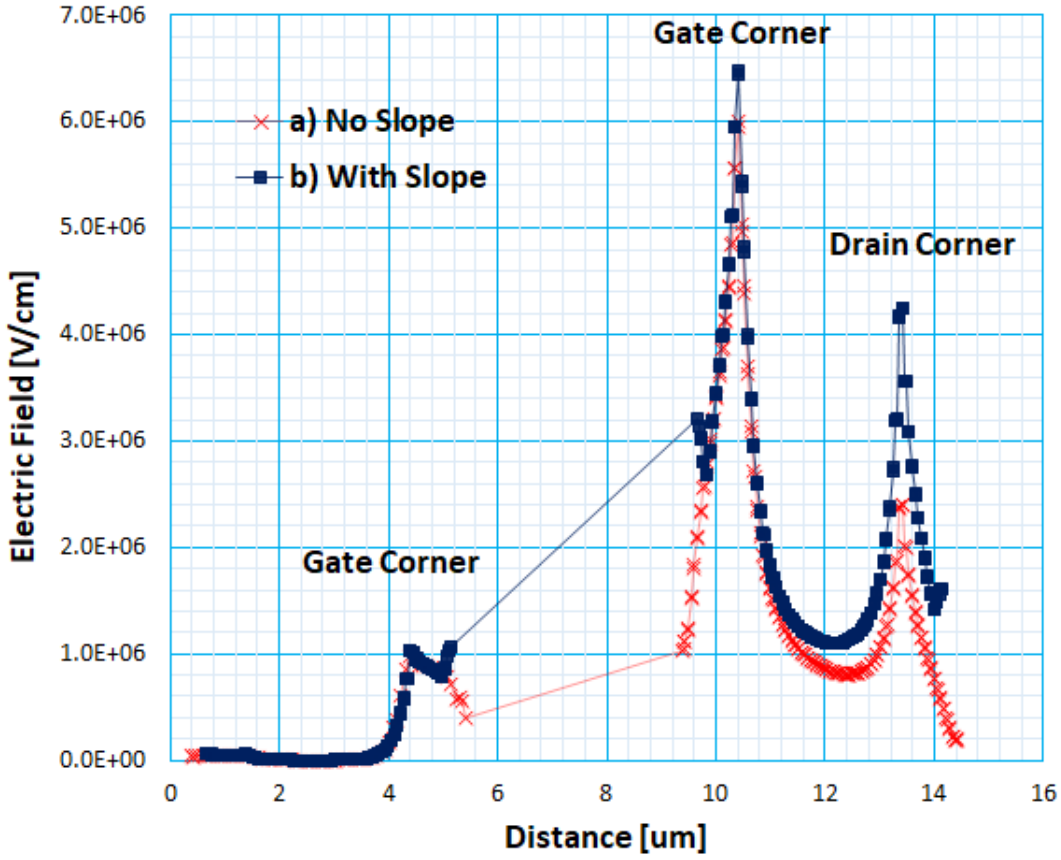


Fig. 5.38 Surface electric field cut comparison of a conventional MESFET and MESFET with sloped field plate structure

Figure 5.38 shows the surface electric field of the lateral RESURF MESFET, with and without sloped passivation as shown in Figure 5.39. The channel length L_{ch} is 4um to accommodate the lithography capability of the cleanroom facility. For a conventional field plate structure, breakdown, initiated by impact ionization, occurs at the gate corner near the drain side due to the electric field crowding. Figure 5.38a illustrates unbalanced peaks in the parabolic shape of the surface electric field cut, resulting from incomplete RESURF effect. These peaks can be balanced out by changing the doping concentration of the N^- epi drift region. For the gate corner having a higher peak, lower doping concentration will deplete the drift region faster, resulting in a more electric field on the drain side to balance the RESURF effect. The negative effect of this approach is the fact that on-resistance is sacrificed by the increased drift region resistance. To achieve maximum trade-off characteristics of breakdown and forward performance, a slope field plate structure is introduced to mitigate electric field crowding. As a result, almost full RESURF effect (balanced parabolic shape) is achieved while keeping the same high doping concentration in the drift region as shown in Figure 5.38b.

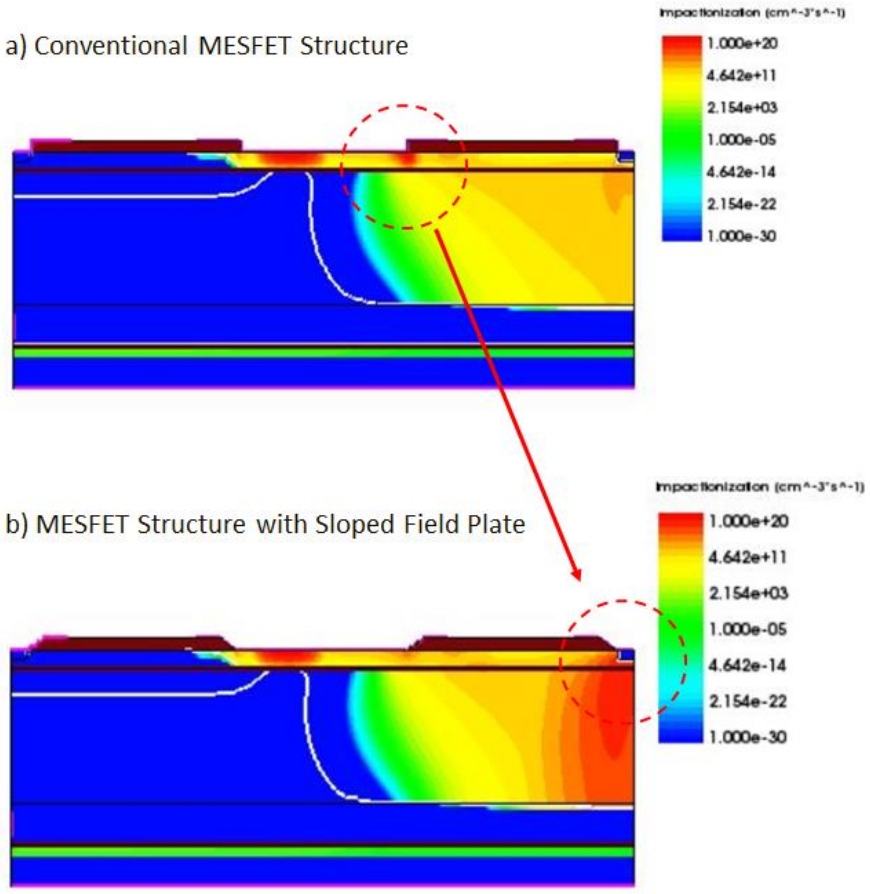


Fig. 5.39 TCAD simulation of impact ionization spots at breakdown for conventional MESFET and MESFET with sloped field plate structure

Figure 5.39 shows the impact ionization spot changing from the drain side gate corner to vertical P^- epitaxial/ N^- epitaxial junction when the sloped field plate structure is incorporated. Therefore, in order to achieve the highest possible breakdown in a RESURF design, it is required that the N^- epi drift region is fully depleted vertically before the lateral electric field has reached a critical value. The impact ionization of the sloped structure occurs at the vertical junction where the blocking capability of the device is originally defined by design.

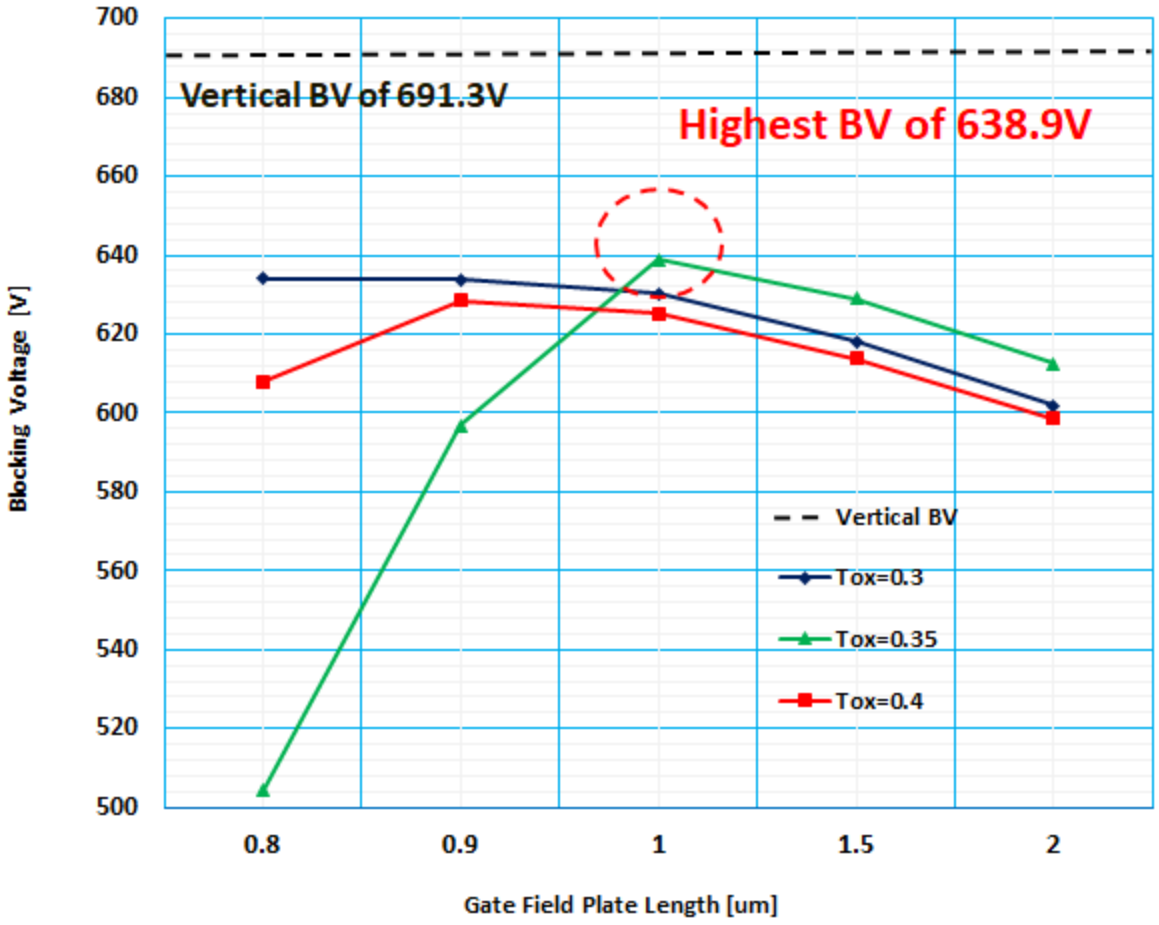


Fig. 5.40 Gate field plate length versus breakdown voltage with varied passivation thickness

Figure 5.40 indicates the optimum design of the gate field plate structure to achieve the highest possible breakdown voltage. As the gate bias increases towards pinch-off, high electric field is formed under the gate. This combined with high electric field at the edge of gate near drain limit the breakdown of MESFET, thus careful control of field crowding at this area is necessary.

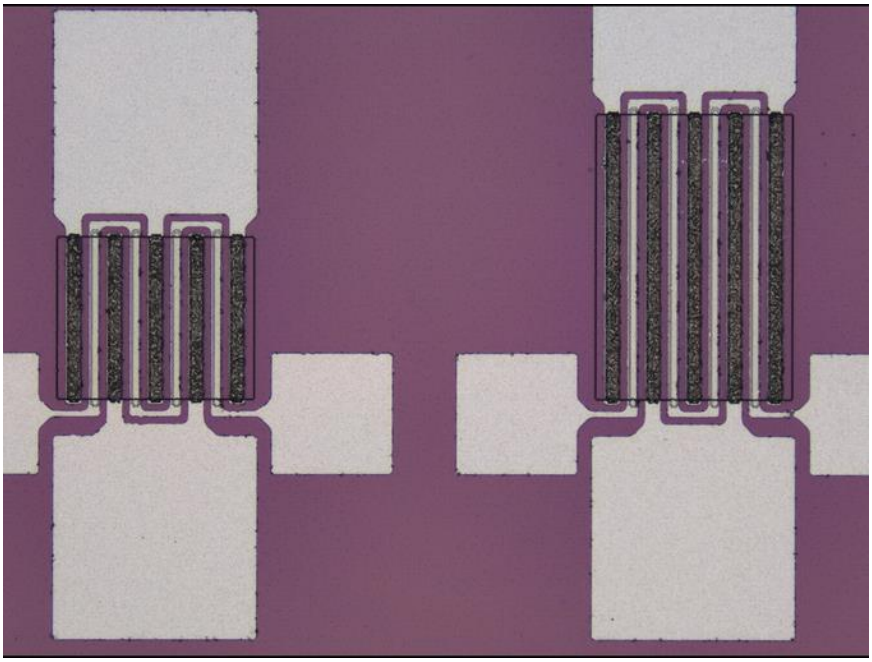


Fig.5.41 Microscope image fabricated finger-type Lateral 4H-SiC MESFETs

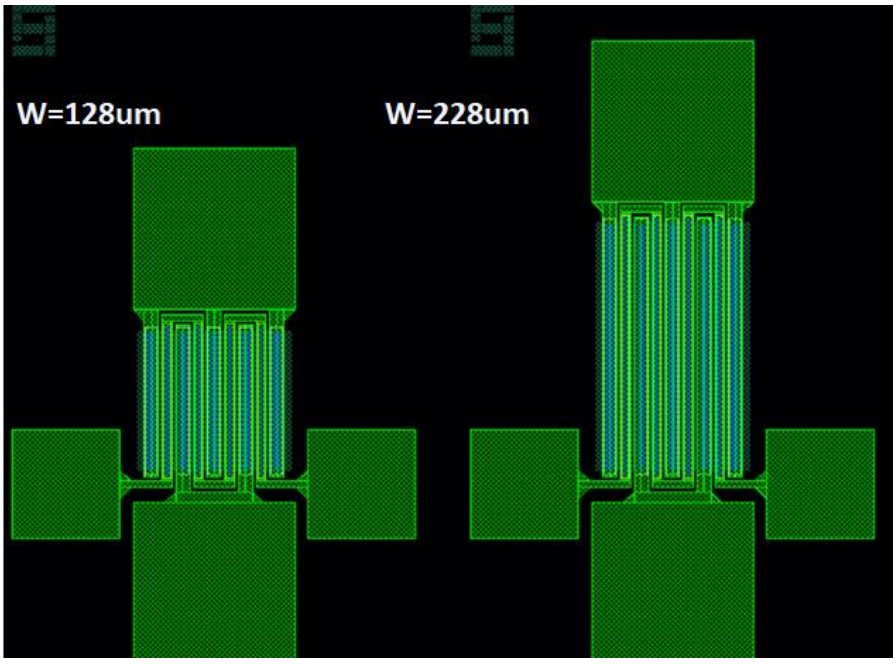


Fig.5.42 Mask layout of finger-type Lateral 4H-SiC MESFETs

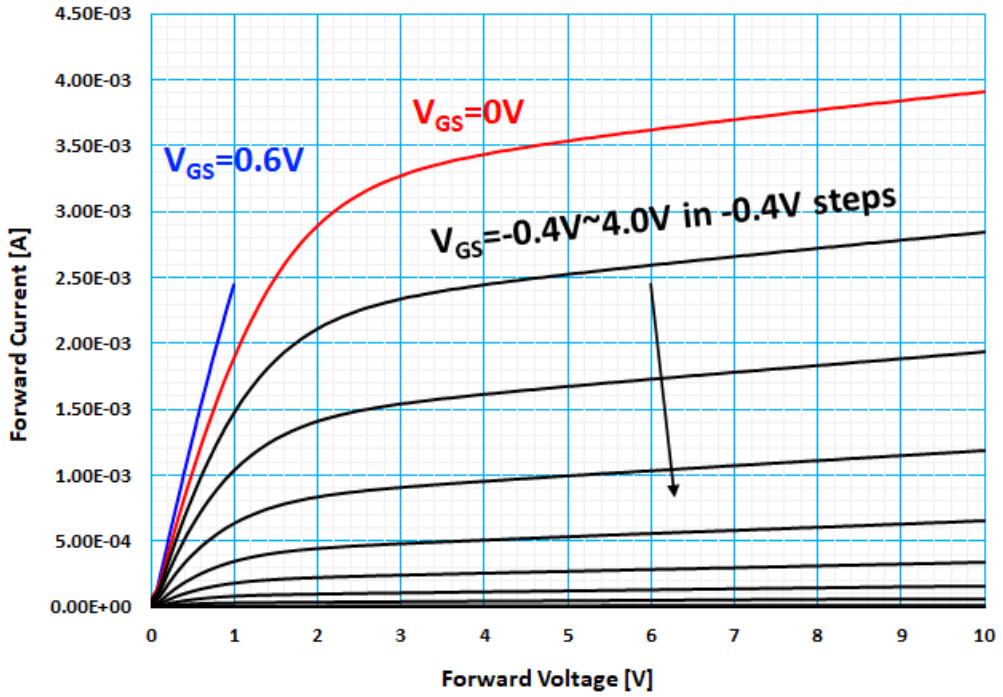


Fig. 5.43 Forward I-V of fabricated SiC MESFET with indicating on-resistance calculation at V_{GS}=0.6V and V_{GS}=0V

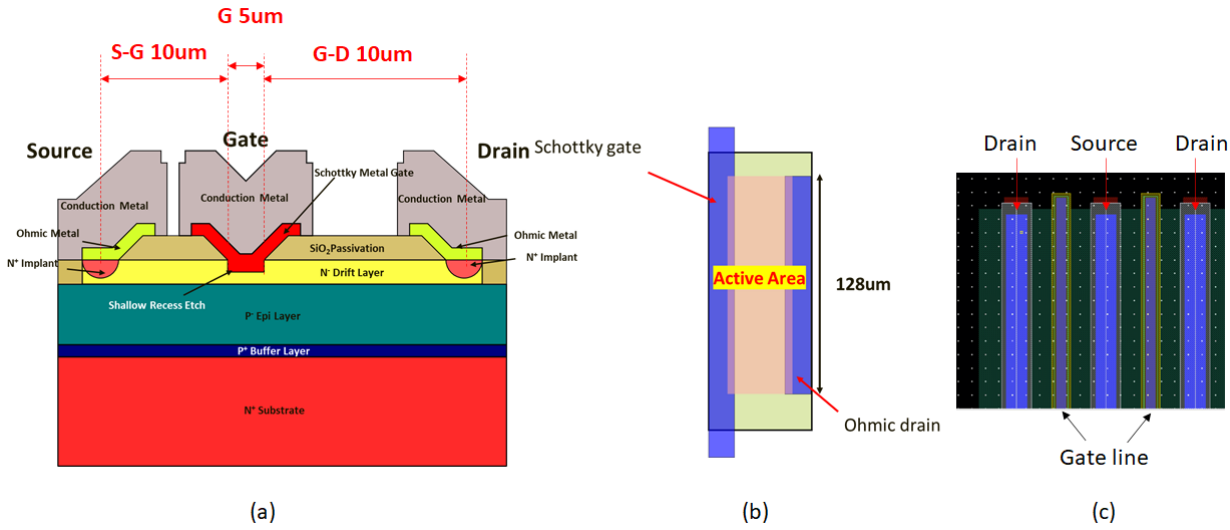


Fig.5.44 Definition of active area: cross section of MESFET (a) Unit cell in layout (b) Actual mask layout (c)

Table 5.7 Extracted specific on-resistance from the I_{DS}-V_{DS} curve of fabricated SiC MESFET

Calculated on-resistance	V_{GS}=0.6V	V_{GS}=0V
Drain-Gate (10um)	5.699mΩ·cm^2	9.548mΩ·cm^2
Drain-Source (25um)	35.621mΩ·cm^2	59.677mΩ·cm^2

The disadvantage of the MESFET structure is that the gate is controlled by a Schottky metal contact. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. This turn-on voltage is typically around 0.7 V for Ni/SiC Schottky diodes. The threshold voltage, therefore, must be lower than this turn-on voltage. As a result, it is more difficult to fabricate an enhancement-mode MESFET than a normally off JFET where the mesa-etched thin vertical channel fully depletes by the gate to source potential with no applied voltage. As shown in the above figure, the highest current conduction occurs at forward bias of 0.6V, just below the turn-on voltage of the Schottky diode, is applied to the Schottky gate. Specific on-resistance was both calculated at V_{GS}=0.6V and V_{GS}=0V for both active areas considering only the drain-gate length and the full drain-source length. The drain-source length is 2.5 times longer than that of the drain-gate. This means the evaluated drain-source on-resistance will be 2.5 times higher than that of the drain-gate, and the specific on-resistance (*RonAa*) will be 2.5 × 2.5 = 6.25 times larger for the drain-source where the value in the chart matches with the calculations.

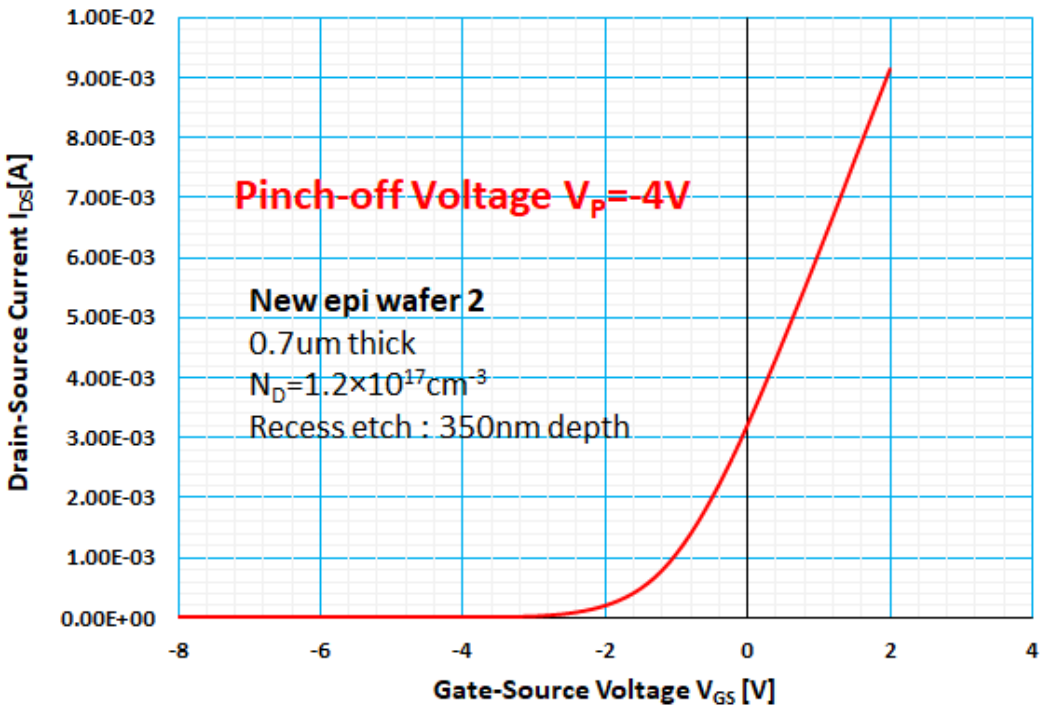


Fig.5.45 Transfer characteristics (I_D-V_{GS}) of fabricated SiC MESFET

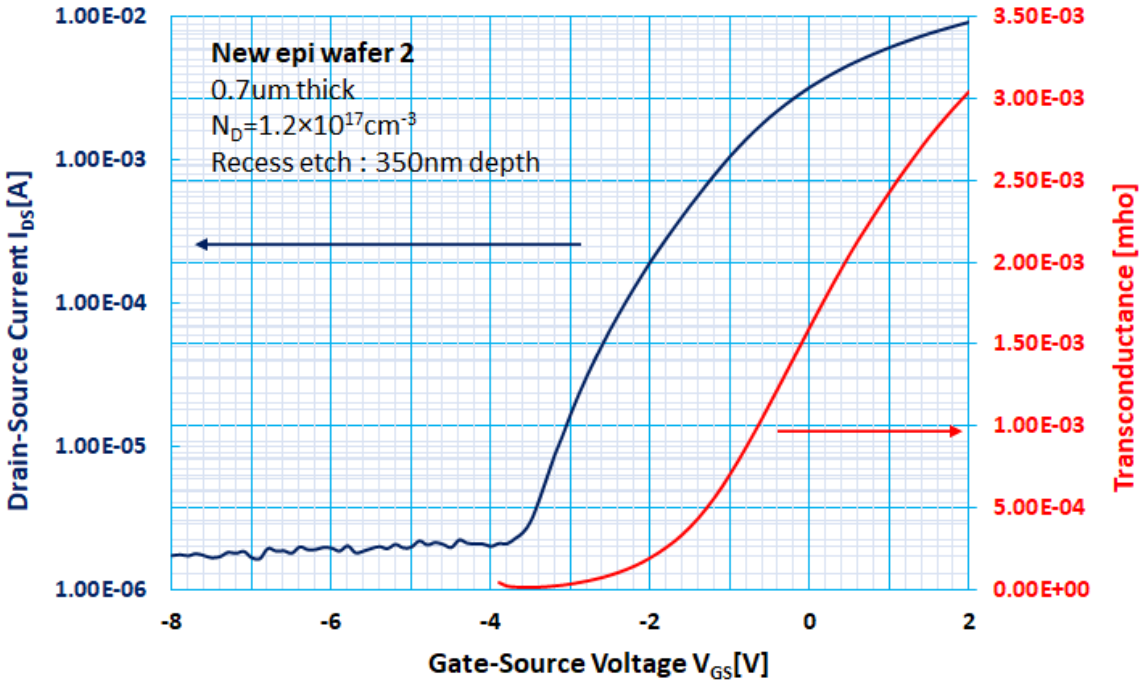


Fig. 5.46 Transfer characteristics (I_D-V_{GS}) and transconductance (mho) of fabricated SiC MESFET in semi-log scale

The key advantage of the MESFET is the higher mobility of the carriers in the channel as compared to the MOSFETs. Because the minority carriers of electron located in the inversion channel layer of a MOSFET have a wavefunction, which extends into the oxide, their mobility referred to as "surface mobility", is less than half of the mobility of bulk material. For MESFETs, because the depletion region separates the carriers from the surface, their mobility is close to that of bulk material. The higher mobility leads to a higher current, transconductance and transit frequency of the device. As shown in figure 5.46, high current conduction leads to high transconductance, which relates directly to the voltage gain of the device. Compared with GaAs MESFETs, the poor low-field electron mobility of SiC and substantial contact resistance of the device result in a still lower transconductance compared with typical values for GaAs MESFETs. The low electron mobility of the SiC material results in a large on-resistance and a low transconductance, however the wide bandgap of SiC enables the device to operate under high electric field with greater advantage in power density.

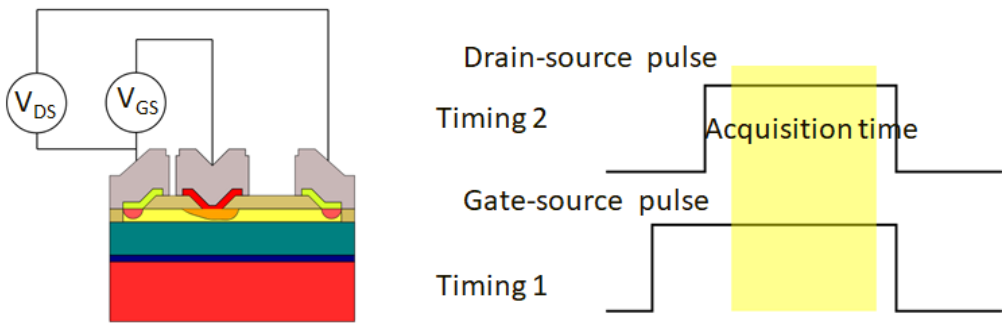


Fig. 5.47 Timing chart for MESFET breakdown evaluation using pulse mode

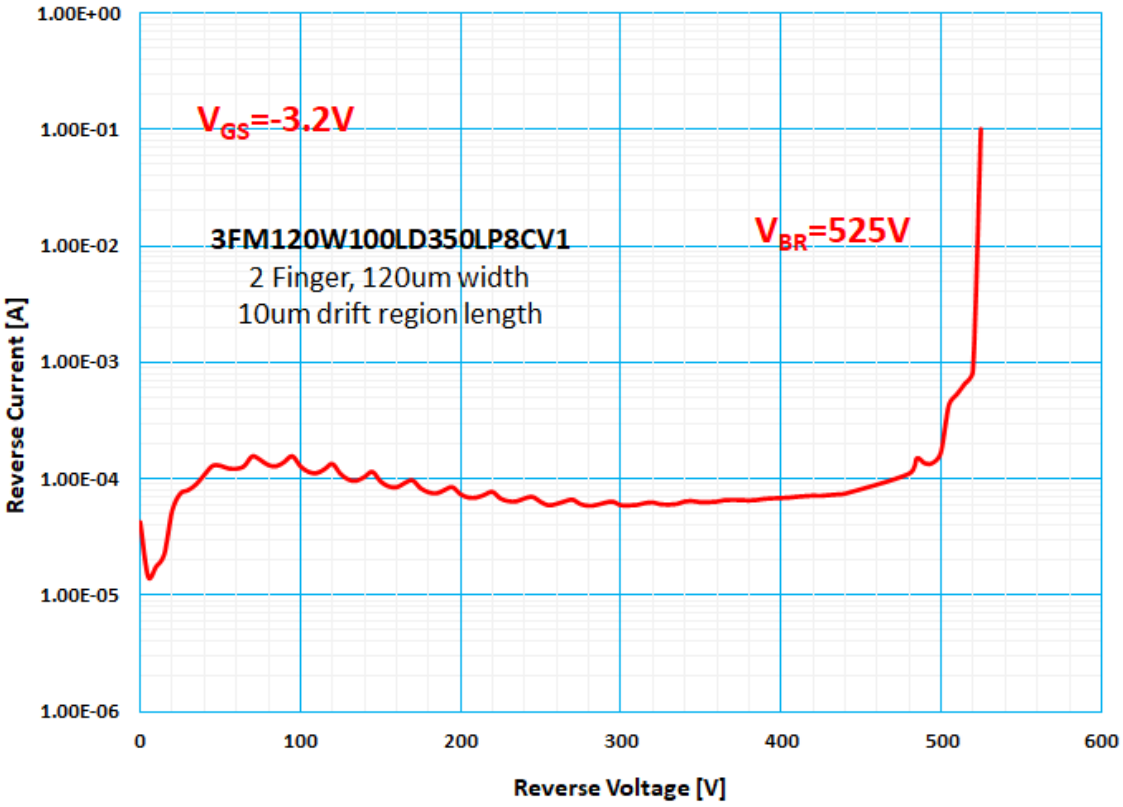


Fig. 5.48 Reverse I-V breakdown evaluation of fabricated SiC MESFET using pulse mode

All measurement of the fabricated lateral 4H-SiC MESFETs was done in pulse mode using Keithley 2600-PCT-4B high voltage/ high current curve tracer connected to a micromanipulator probe station. Pulsed measurements with short pulse width (~µs) is required to avoid device self-heating especially for high current at medium voltage bias such as forward *I-V* curve shown in Figure 5.43. It is also considered a much safer method in measuring high voltage breakdown evaluation where negative gate bias is being applied to close the gate. Figure 5.47 shows the timing chart for MESFET breakdown

evaluation using pulse mode measurement. By using timing 1 pulse to close the gate by applying negative bias, drain-source bias can be pulse measured using timing 2 pulse. The evaluated reverse *I-V* breakdown curve of the fabricated lateral 4H-SiC MESFET is shown in Figure 5.48. The breakdown voltage of the fabricated lateral 4H-SiC MESFET is 525V, which matches closely with the blocking capability of the lateral 4H-SiC Schottky barrier diode with the same drift region length.

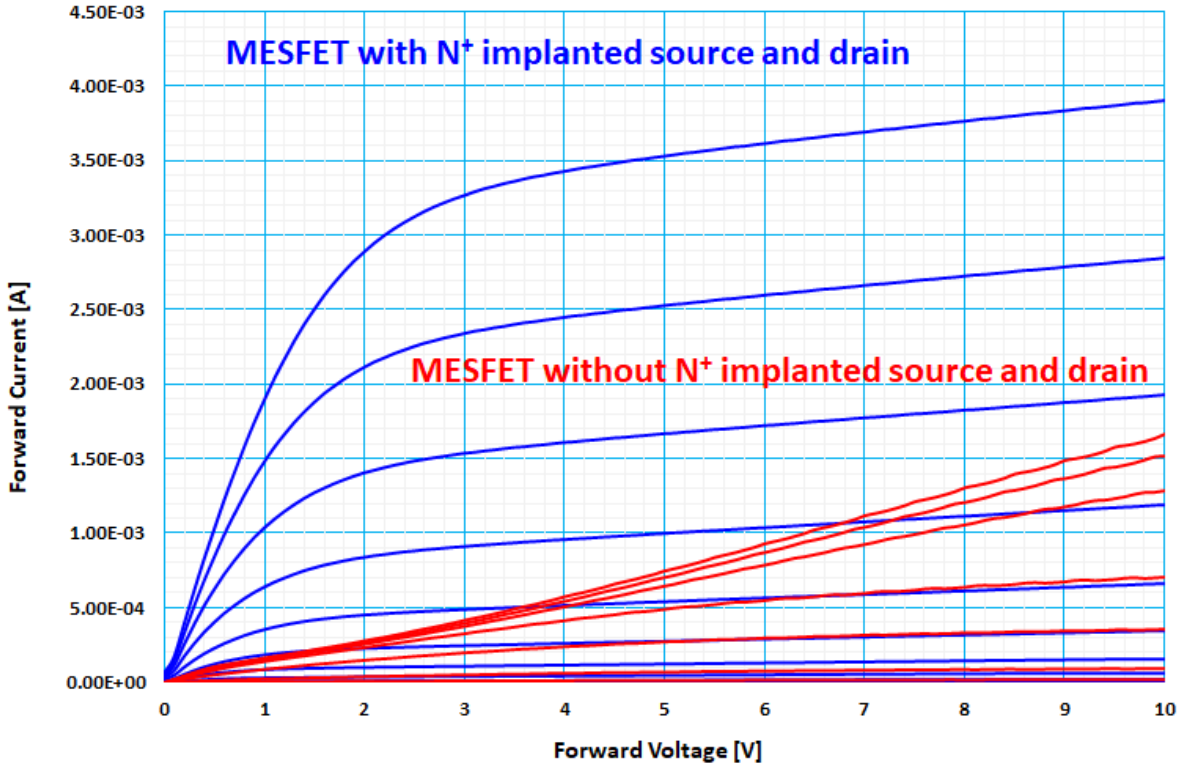


Fig. 5.49 Comparison of MESFETs with and without N^+ implanted source and drain

Figure 5.49 shows the benefits of performing N^+ ion implantation process to source and drain region to form quality ohmic contact. Compared to conventional MESFET with channel-recessed structure where highly doped N^+ cap layer is used for drain and source, this implantation procedure to decrease the source and drain contact resistance is beneficial in terms of reducing dry etch damage to the channel region. As we can see in the blue line forward *I-V* , both linear region ($0 \leq V_{DS} \leq (V_{GS} - V_P)$) and saturation region ($0 \leq (V_{GS} - V_P)) \leq V_{DS}$) can be clearly distinguished. It is also worth noting that I_{DS} increase slightly with increased drain-source voltage in the saturation region. This is because the effective channel length decreases with increasing V_{DS} above pinch-off. This effect is called the "channel-length modulation."

5.6 Evaluation of vertical breakdown pattern

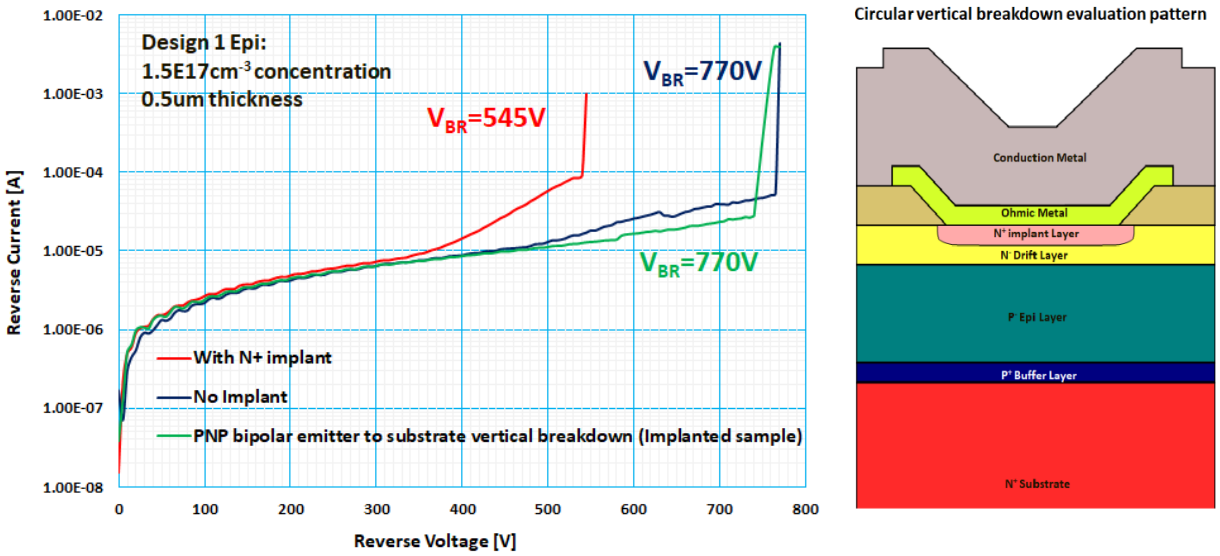


Fig. 5.50 Comparison of vertical breakdown (left) and cross section diagram of circular vertical breakdown pattern

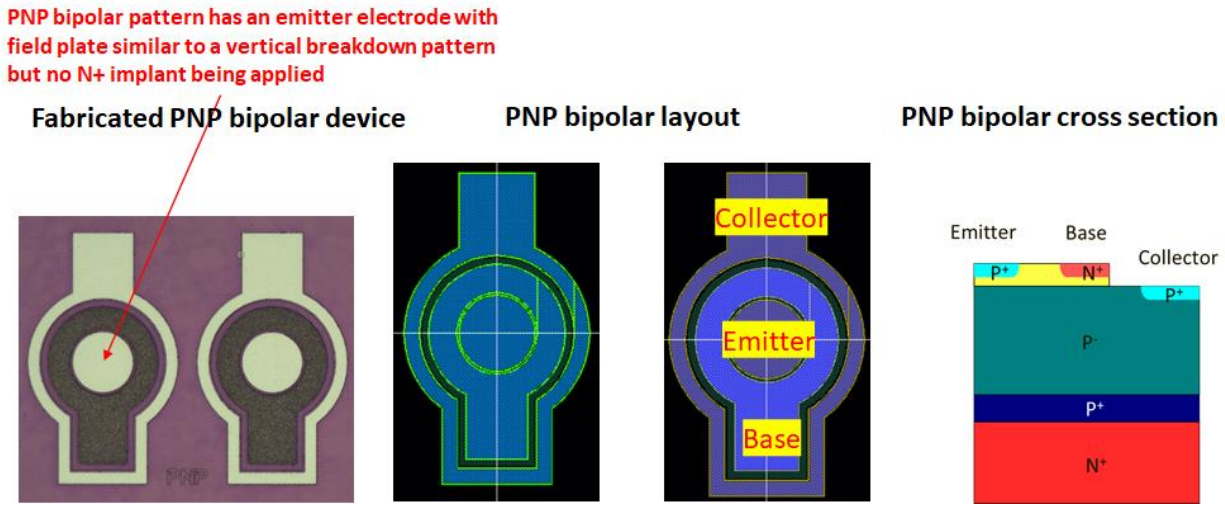


Fig. 5.51 Emitter electrode of PNP bipolar pattern used as vertical breakdown evaluation comparison

1st fabrication run with the new epitaxial wafers and new set of masks showed blocking voltage as high as 900V without N^+ implant. Although 2nd fabrication run with N^+ implant process of the same above design showed greatly improvement in on-state performance, there was a significant decrease (~200V or so) in breakdown voltage. As shown in the above Figure 5.50, the device's decrease in blocking capability comes from the decrease in vertical breakdown influenced by the N^+ implant process. The new epitaxial wafer 1 has 770V vertical breakdown with no implant, while the vertical pattern with N^+ implant decreases to a value of 545V. The N^+ implanted die goes through activation

process and HF wet etch cap layer removal, but the non-implanted region still retains the vertical blocking capability as proved by the evaluation of PNP bipolar test pattern. The green curve in Figure 5.50 is the evaluation result of the vertical breakdown of the emitter electrode of the PNP bipolar test pattern from the same N^+ implanted die. Emitter electrode has a similar field plate structure as the circular vertical pattern but without the N^+ implant and shows a vertical breakdown of 770V as well. It is evident that the N^+ implant itself has significant influence on the blocking capability of the fabricated lateral RESURF device.

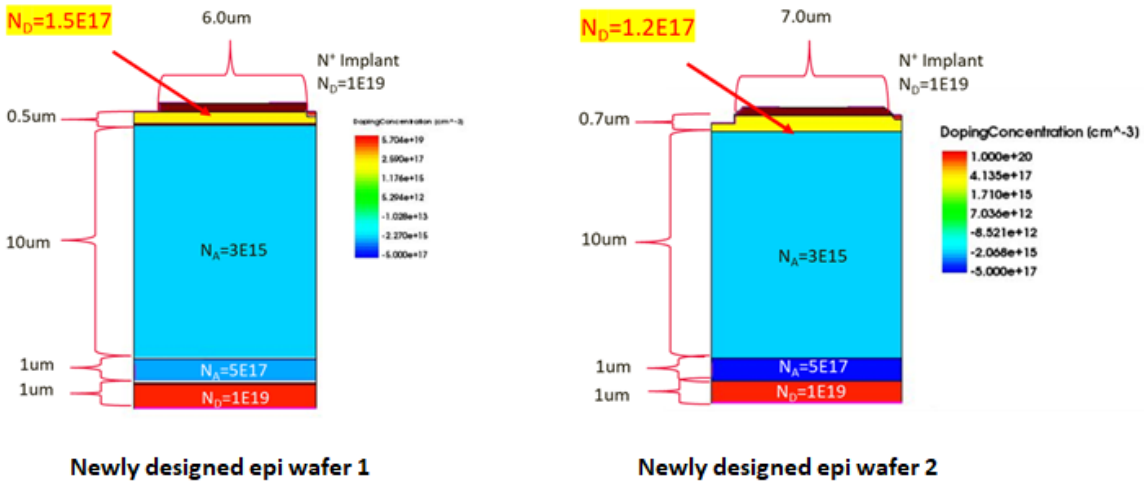


Fig. 5.52 Comparison of newly designed epi wafers with different thickness and doping concentration

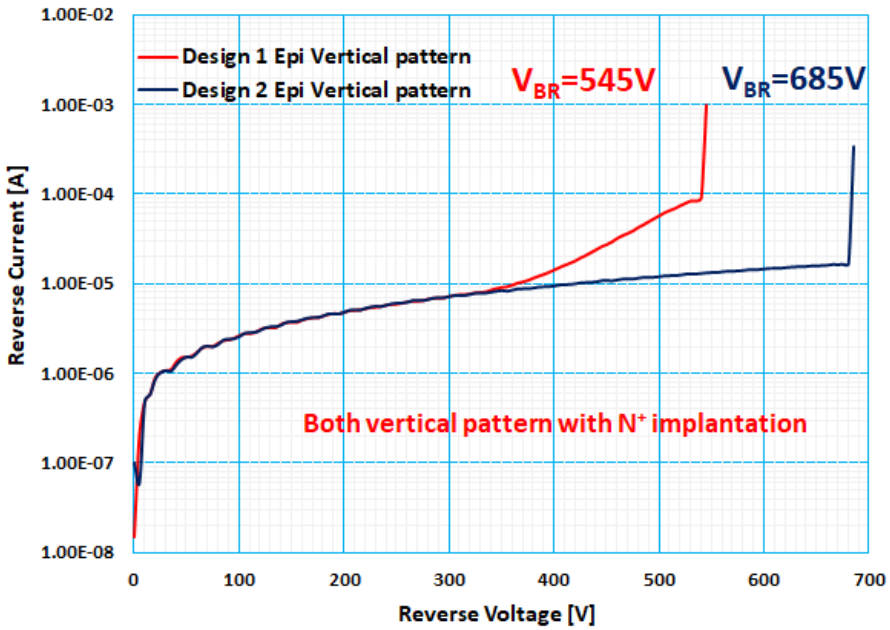


Fig. 5.53 Comparison of vertical breakdown of the newly designed epi wafers with N^+ implant

As shown in the above Figure 5.53 newly designed epi wafer 1 and 2 were designed with similar vertical breakdown of > 1kV yet, only design 2 is able to retain vertical blocking capability over 600V. Leakage current of design 1 starts to increase past 300V and eventually reaching premature breakdown around 545V. N^+ ion implant process have more impact on design 1 epi wafer because of thinner top n^- drift epi layer, possibly the tail of the high energy phosphorous implant penetrating into the p^- epitaxial layer underneath.

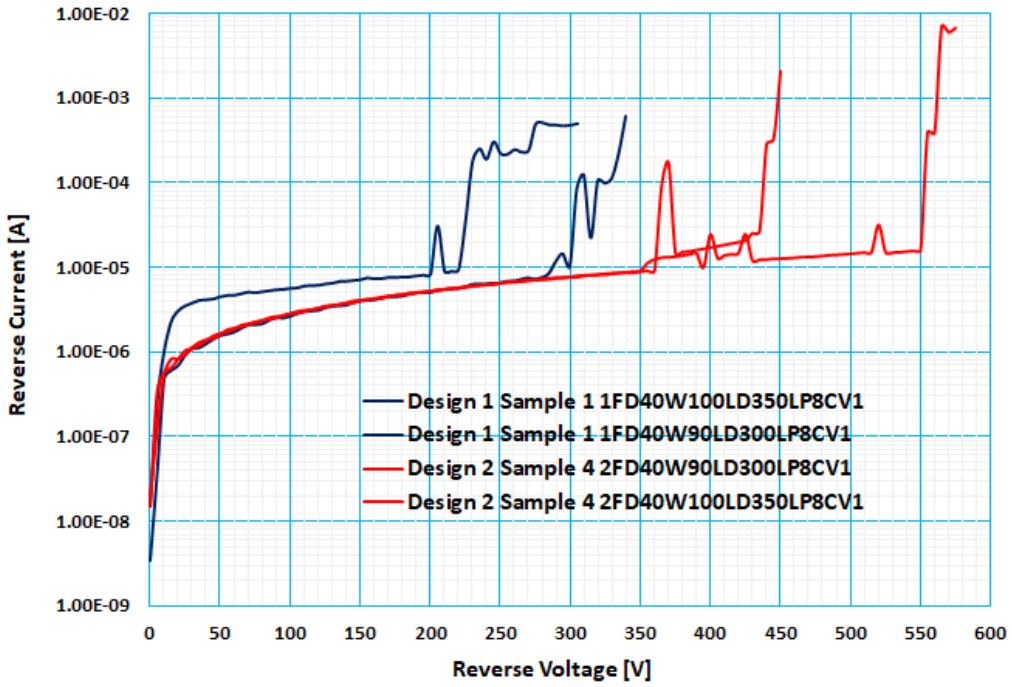


Fig. 5.54 Comparison of vertical breakdown of the newly designed epi wafer with N^+ implant

As a consequence, comparing actual lateral RESURF Schottky barrier diode breakdown, newly designed epi wafer 2 samples show higher breakdown compared to newly designed epi wafer 1 sample as shown in Figure 5.54. There is no significant increase in leakage current between implanted and non-implanted sample or between different wafer specs, so the possibility of crystal damage induced by implantation should not be our primary concern.

5.7 Secondary-Ion Mass Spectrometry (SIMS) Analysis

Secondary-ion mass spectrometry (SIMS) is a technique used to analyze the composition of solid surfaces and thin films by sputtering the surface of the sample with a focused ion beam and collecting and analyzing emitted secondary ions. A SIMS measurement gives the chemical composition of the samples with extremely high accuracy. Using sputtering for material removal, it is possible to obtain a depth profile within a resolution of ~1 nm or less. It is a widely used method to analyze the dopant and impurity depth profile in semiconductor material where junctions are formed through ion implantations or diffusions for device operation. However, reference samples are needed to calibrate the detectors for each measurement so as to obtain an accurate concentration of the impurities, which makes this technique rather expensive. Due to the experimental need in this research to analyze the cathode, drain, and source N^+ implant profile, the full amount of phosphorus will be detected, and the amount of electrically active and inactive phosphorus cannot be distinguished. The uncertainty in the concentration is estimated to be within ±10 %.

Fig. 5.55 Time of Flight Secondary-Ion Mass Spectrometer (TOF.SIMS 5) at TMI facilities

A SIMS analysis was conducted using the University of Texas at Austin, Texas Materials Institute's Time-of-Flight Secondary-Ion Mass Spectrometry (TOF-SIMS) (refer to Figure 5.55). TOF-SIMS is a technique in which an ion beam (primary ion) is irradiated on a solid sample and mass separation of the ions emitted from the surface (secondary ions) is performed using the difference in time-of-flight (time-of-flight is proportional to the square root of the weight). The limitation of this equipment is that it is required to collect and analyze large amounts of data for a single depth profile. Also, every point of an image produced by ToF-SIMS contains a full mass spectrum. Thus, it may take hours, days, or

even weeks to fully analyze a single dataset. Below Figure 5.56 shows the analyzed phosphorous profile according to sputtering time. The analysis took 2 days because of very slow sputtering rate of SiC. The profile was acquired with a Bi^+ analysis beam (30kV, 4pA, reading 100um × 100um) and a Cs^+ sputtering beam (500V, 40nA, sputtering 300um × 300um centered over the Bi+ analysis area) in noninterlaced mode, that is, sequential sputtering and analysis. All detected ions had negative polarity. The sputtering time 20000sec where the evaluation ends correspond to a depth of ~0.4um. Nitrogen and aluminum atoms have positive polarity in this analysis, thus with our current setup could not detect accurately.

Table 5.8 Implantation Series for SIMS analyzed sample

Dopant	Dose	Energy	Angle/Twist
Phosphorus	$2.7\times10^{15}cm^{-2}$	200keV	Tilt 7 degrees, Twist 23 degrees
Phosphorus	$1.4\times10^{15}cm^{-2}$	100keV	Tilt 7 degrees, Twist 23 degrees
Phosphorus	$9.0\times10^{14}cm^{-2}$	50keV	Tilt 7 degrees, Twist 23 degrees

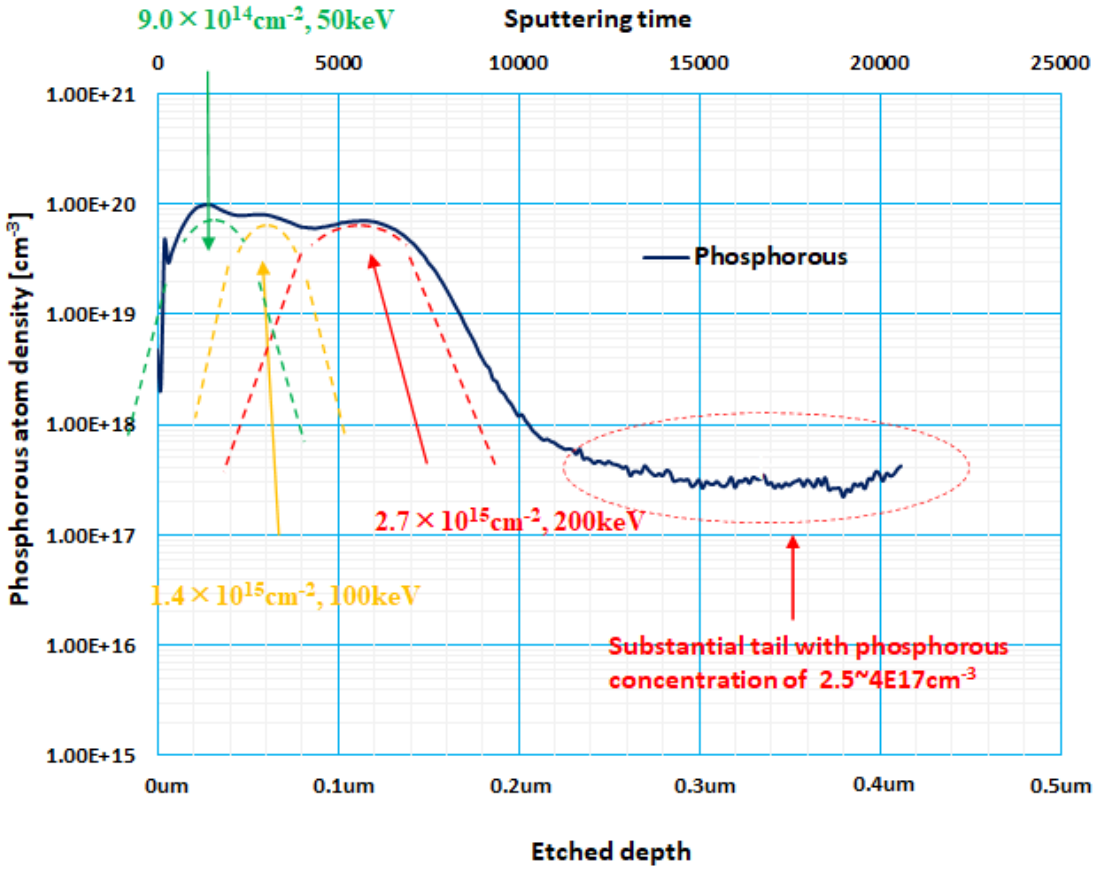


Fig. 5.56 Semi-log plot of the SIMS analysis of phosphorous implant profile over sputtering time (etched depth)

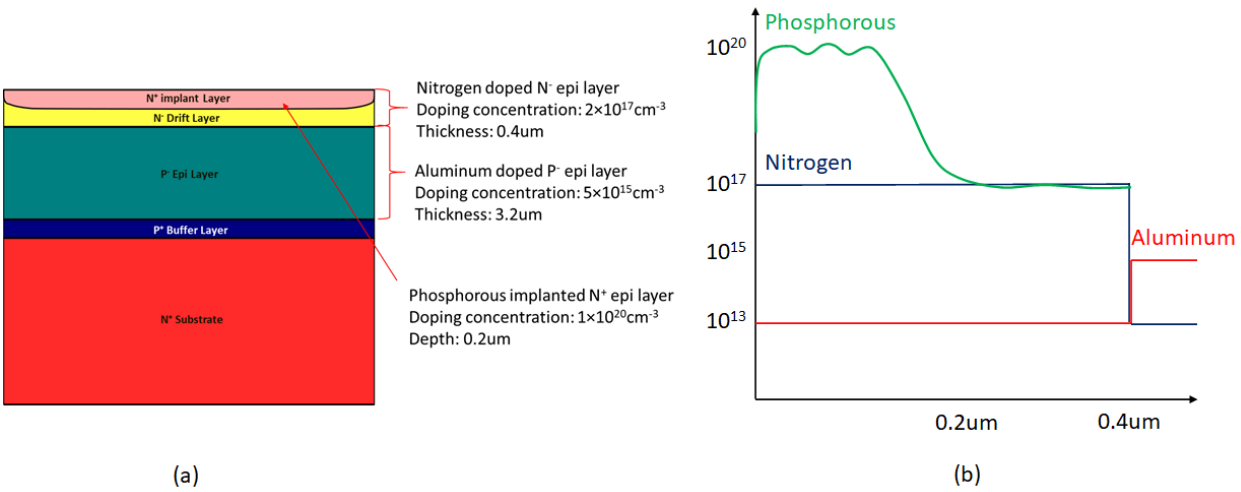


Fig. 5.57 Semi-log plot of the SIMS analysis of phosphorous implant profile over sputtering time (etched depth)

The tail of the implanted 200-nm-deep box profile seems to extend well past the 0.4um interface of the N^- drift epi layer /P^- epi layer with substantial phosphorous concentration ranging from $2\sim4\times10^{17}$ cm^{-3}. The background n-type doping for the initial 0.4um depth is nitrogen, so any phosphorous detected is from the ion implant process. Although the effect is not severe, the long tail is the result of "channeling effect". This is when implanted ions travel considerable distance with little energy because its velocity is parallel to the major crystal orientation. Countermeasures are taken to suppress this channeling effect such as setting angles and twists to avoid major crystal orientation and deposition of thin oxide layer as the "screening oxide" to further randomize the direction of the implanted ions to the crystal.

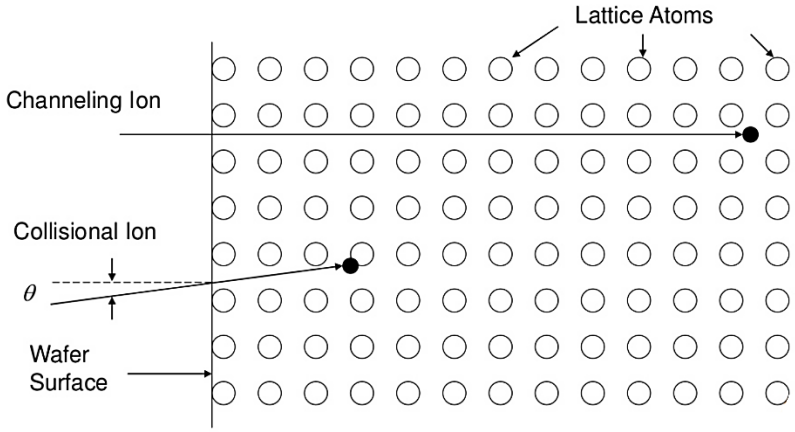


Fig. 5.58 Diagram explaining "channeling effect"

5.8 Capacitance-voltage curves for figure of merit comparison between vertical and lateral device

Table 5.9 Comparison of vertical and lateral device TCAD simulation results

	Vertical SiC Schottky barrier diode	Lateral SiC Schottky barrier diode
On-resistance R_{on} [Ω]	13161Ω	10869
Area S [cm^2]	8.40×10^{-8} (8.4um cell pitch z=1um)	8.40×10^{-8} (8.4um cell pitch z=1um)
Ron·Aa [mΩ·cm^2]	1.106	0.913
Junction capacitance C_j [F]	1.5×10^{-16} @1000V	5.825×10^{-17}@1000V
Junction capacitance C_j [nF/cm^2]	1.786 @1000V	0.6935 @1000V
FOM1 Ron× C_j	**1.975**	**0.6332**
Junction charge Q_j [C]	1.957×10^{-13}	1.500×10^{-13}
Junction charge Q_j[nC/cm^2]	2.330	1.786
FOM2 Ron× Q_j	**2.577**	**1.631**

Advantages of lateral RESURF device structure can be proven through comparison with vertical device using various figure of merit calculation. Above table is the TCAD simulation of both vertical punch-through SiC Schottky barrier diode with P^+ guard ring structure and the proposed lateral RESURF SiC Schottky barrier diode as shown in the bottom Figure 5.59. Each unit cell has a cell pitch of 8.4um. The calculated specific on-resistance indicates the performance of the device at static state being both devices are designed to block V_{BR}=1000V. The junction capacitance and charge represent the dynamic performance of each device as these values are required to charge and discharge during on to off state transition. By multiplying on-resistance Ron against junction capacitance C_j or on-resistance Ron against junction charge Q_j overall performance of 2 different devices can be compared. From the figure of merit 1 and 2 calculations, it can be concluded that lateral RESURF Schottky barrier diode performs 1.58~3.12 times better than vertical Schottky barrier diode.

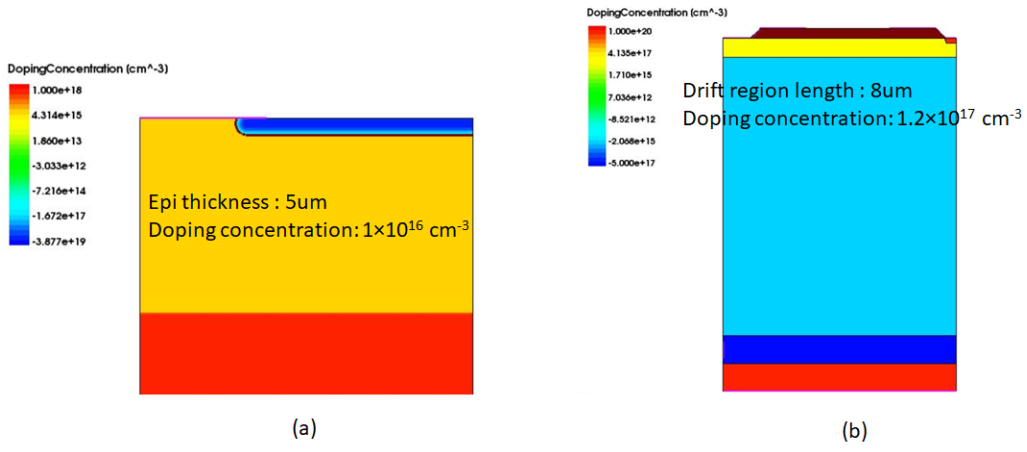


Fig.5.59 Unit cell structure of simulated vertical punch-through SiC Schottky barrier diode with P+ guard ring structure and lateral RESURF 4H-SiC Schottky barrier diode

Previous theoretical calculation indicated that lateral device would perform up to 4 times better than the vertical device. The vertical device in comparison at this section is a punch-through design where the electric field possess a trapezoid shape instead of a triangular shape, suitable for attaining lower on-resistance while maintaining the required blocking capability. It is simulated with P^+ guard ring structure, much like the edge termination necessary for an actual fabricated device which will enhance its blocking capability. While the lateral RESURF Schottky barrier diode structure is optimized for its best performance, its electric field distribution is still a parabolic shape compared to an ideal square shape used for theoretical calculation comparison. Above reasons are why the figure of merit comparison difference is smaller than 4 times from the previous theoretical calculations.

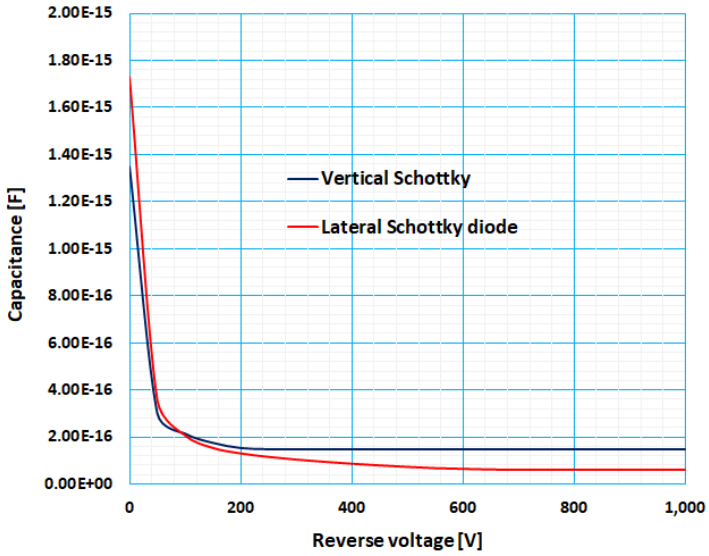


Fig.5.60 Capacitance simulation comparison of vertical and lateral SiC Schottky diode

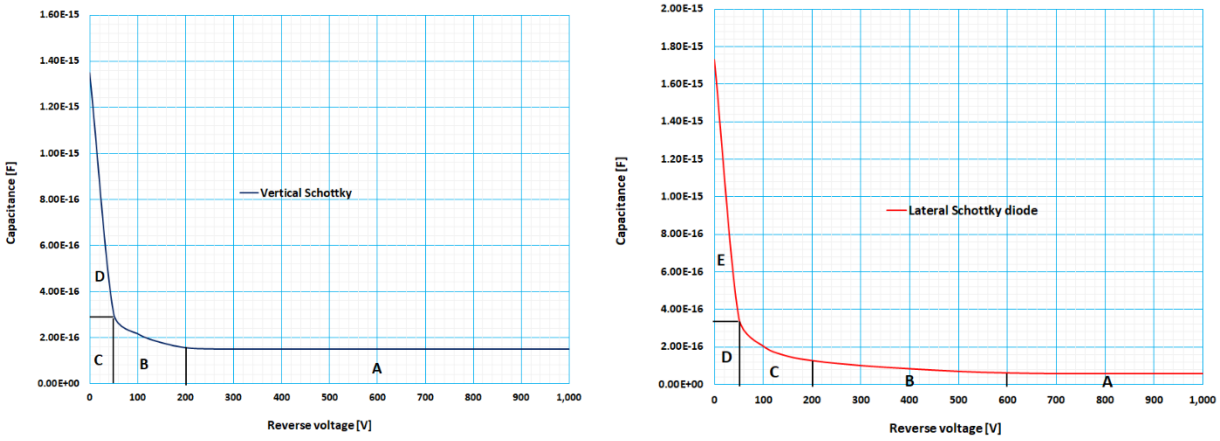


Fig.5.61 Capacitance simulation of vertical and lateral SiC Schottky diode with labeled region for charge calculation

Integral calculation of junction capacitance for charge values

Vertical Schottky barrier diode:

Region A: 1.5E-16 [F] × 800 [V] =1.20E-13 [C]

Region B: (3.03E-16 + 1.56E-16)/2[F]× 150 [V] = 3.44E-14 [C]

Region C: 3.03E-16 [F]×50[V]= 1.52E-14 [C]

Region D: (1.35E-15-3.03E-16) [F] ×50[V] / 2= 2.61E-14 [C]

Total= 1.20E-13+3.44E-14+1.52E-14+2.61E-14= 1.957E-13 [C]= 0.1957 [pC]

Lateral Schottky barrier diode:

Region A: 5.83E-17 [F] × 400 [V] =2.33E-14 [C]

Region B: (6.25E-17 + 1.28E-16)/2 [F]× 400 [V] = 3.82E-14 [C]

Region C: (1.28E-16 + 3.56E-16)/2 [F]× 150 [V] = 3.63E-14 [C]

Region D: 3.56E-16 [F]×50[V]= 1.78E-14 [C]

Region E: (1.73E-15-3.56E-16) [F] ×50[V] / 2= 3.44E-14 [C]

Total= 2.33E-14 + 3.82E-14 + 3.63E-14 + 1.78E-14 +3.44E-14 = 1.500E-13 [C]= 0.1500 [pC]

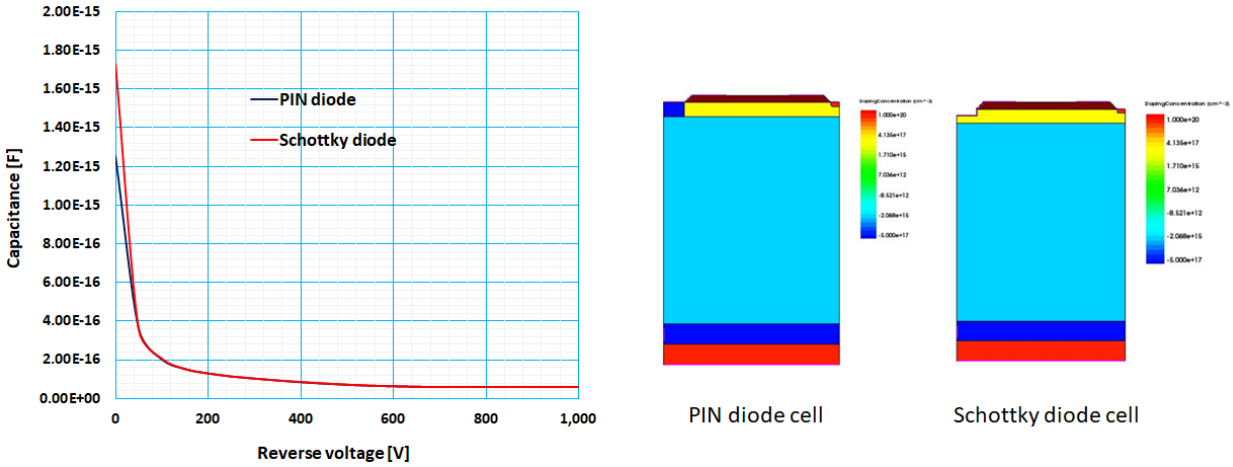


Fig.5.62 C-V simulation of 2 terminal device using proposed RESURF epitaxial wafer specifications

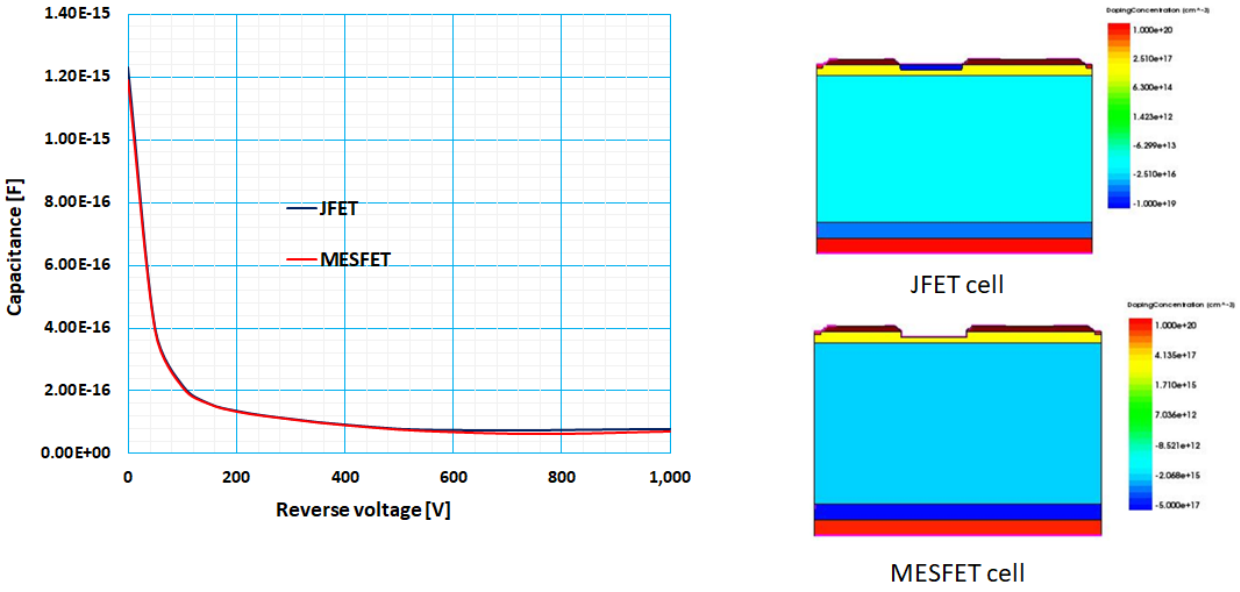


Fig.5.63 C-V simulation of 3 terminal device using proposed RESURF epitaxial wafer specifications

5.8.1 Experimental measurements of capacitance-voltage curves

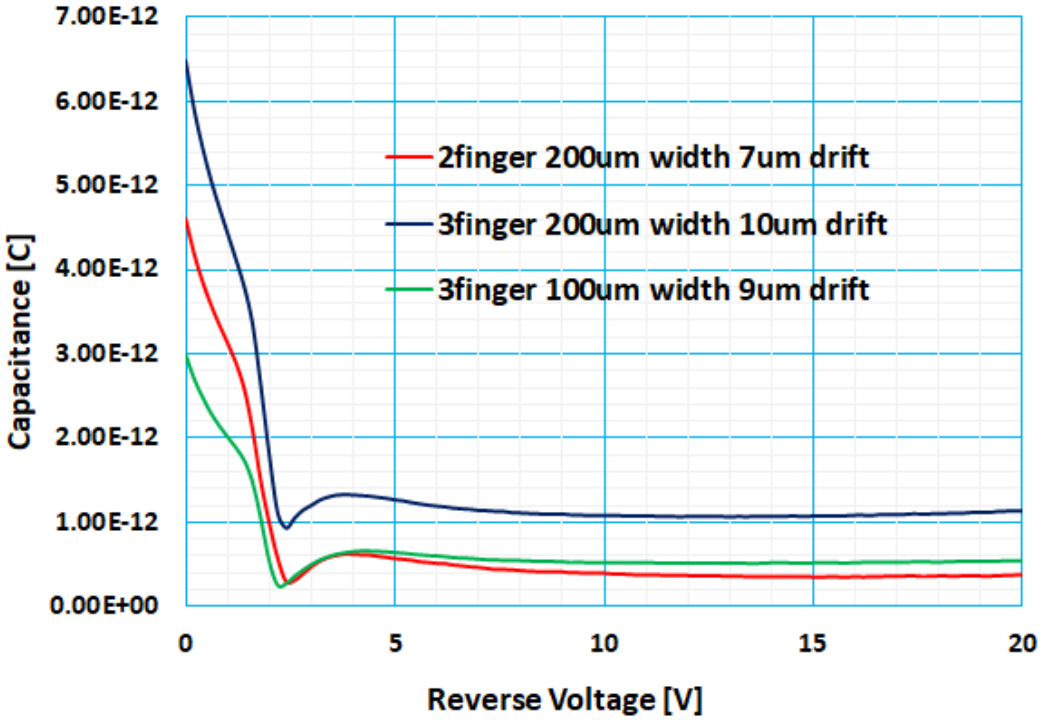


Fig.5.64 C-V measurement of fabricated lateral RESURF 4H-SiC Schottky barrier diode with different active area size

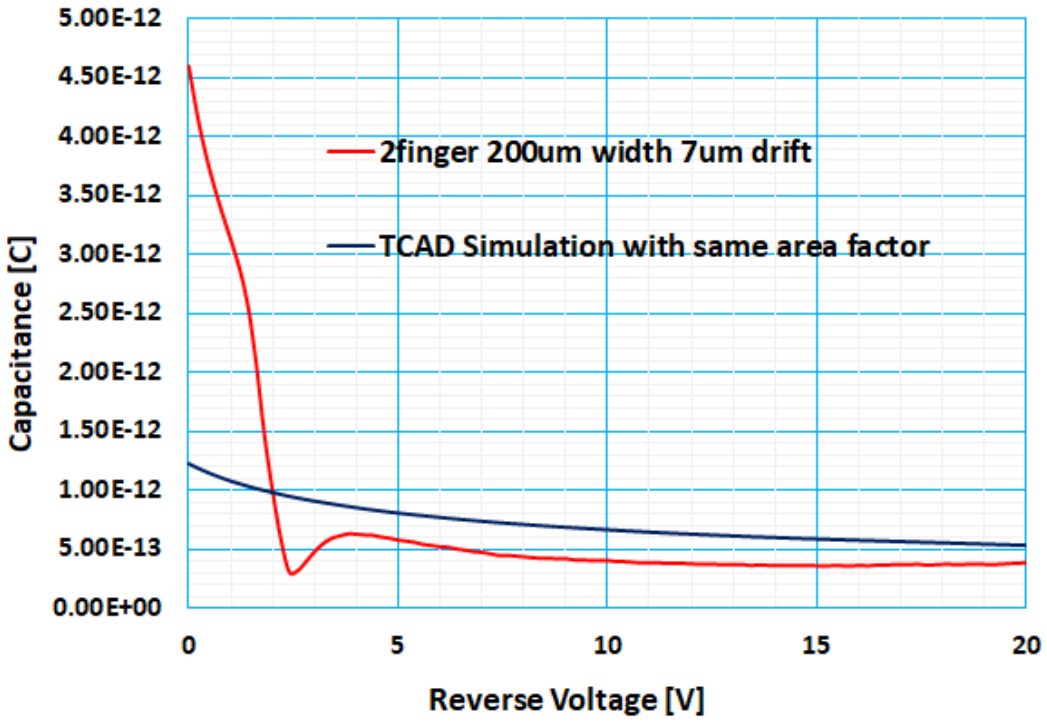


Fig.5.65 C-V measurement of fabricated lateral RESURF 4H-SiC Schottky barrier diode compared with TCAD simulation of device with same area factor size

In Figure 5.64 shows the *C-V* measurement of the fabricated lateral RESURF 4H-SiC Schottky barrier diode. As the area of the device gets bigger (number of fingers × width of finger × drift region length), the value of parasitic capacitance increases. As shown in Figure 5.65, it is possible to simulate the capacitance of actual fabricated device size by utilizing the TCAD simulation command "Area Factor". In this case, the area factor was set to the number of fingers × both sides of finger × width of finger to simulate the actual active area of the fabricated device. The figure indicates that the actual *C-V* measurement matches in similar order of capacitance to that of the simulation results with same area factor. Possessing a smaller parasitic capacitance is one of the advantages of lateral RESURF devices over vertical device, and through simulation and experimental *C-V* measurement, it has been proven that lateral RESURF devices is capable of performing better in both static and dynamic characteristics.

Chapter 6. Conclusion

6.1 Analysis for Lowering of Vertical Voltage Blocking Capability after N^+ Implantation Using 3D TCAD Simulation

Much of the device simulation using Synopsys TCAD was performed using a 2D model. Through each simulation, optimal epitaxial layer thickness and doping concentration was decided for the final fabrication design. While the 2D model is easier to compute due to having less mesh, it does not take into account every physical phenomenon that happens in actual fabricated device. One of the main concerns is at the edge of the device, where electric field crowding occurs more severely in the form of 3D coming from all three directions, lowering the voltage blocking capability from the intended value. In this section, we will analyze the reason why the fabricated device showed lower blocking capability after the N^+ ion implantation process by simulating the vertical voltage blocking pattern using a 3D model. Figure 6.1 below shows the 3D TCAD model of the vertical breakdown voltage pattern using cylindrical coordinates.

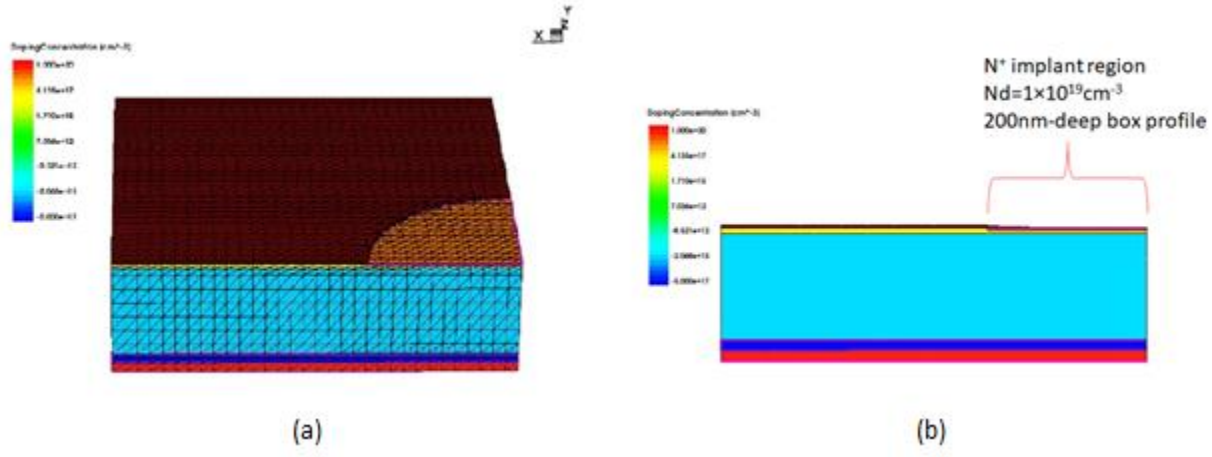


Fig. 6.1 3D TCAD model of the vertical breakdown voltage pattern using cylindrical coordinates Top view (a) and cross section (b)

The model has a 0.4um thick passivation with a circular contact open for top metal contact. The first n^- epitaxial layer has a doping concentration of 1.5×10^{17} cm^{-3} and a thickness of 0.5um, reflecting the same value as the Design 1 Epi. Whereas the second p^- epitaxial layer has a doping concentration of 3×10^{15} cm^{-3} and a thickness of 10um, which is intended to block more than 1kV vertically through a punch-through design. The top n^- layer has a highly doped region where the contact open is present with a doping concentration of 1×10^{19} cm^{-3} and a depth of 200nm. This region reflects the 200nm-deep box profile created by the N^+ ion implant process. The vertical breakdown voltage will be simulated

by applying positive bias to the top contact with the bottom substrate contact grounded in the simulation, similar to how you would evaluate the lateral RESUF Schottky diodes by applying positive bias to the cathode electrode in an experimental setup.

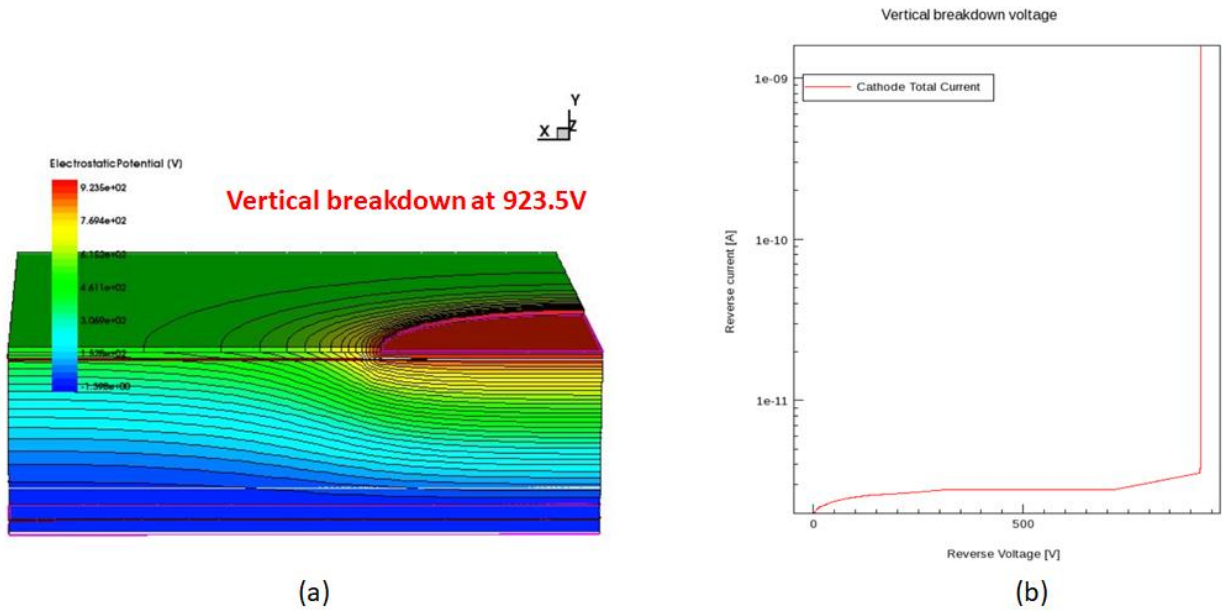


Fig. 6.2 3D TCAD model of the vertical breakdown voltage pattern using cylindrical coordinates electrostatic potential distribution (a) and breakdown I-V curve from simulation (b)

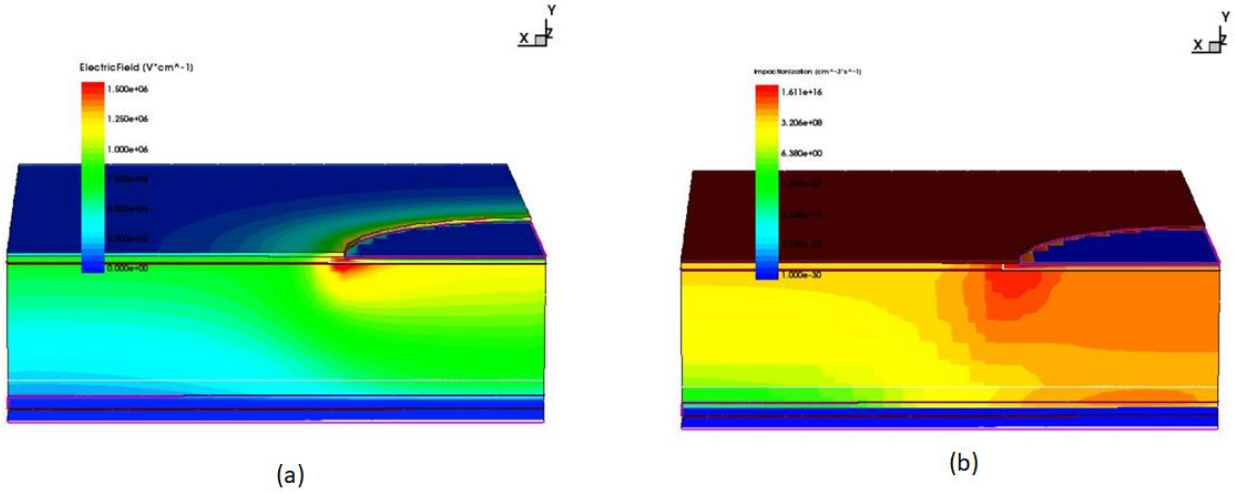


Fig. 6.3 3D TCAD model of the vertical breakdown voltage pattern using cylindrical coordinates electric field distribution (a) and Impact ionization distribution (b)

Table 6.1 Comparison Between Simulated Vertical Breakdown Voltages Obtained from 2D and 3D Simulation Models

Simulated vertical breakdown pattern model	Breakdown Voltage
2D simulation model	1423V
3D simulation model without N^+ implant region	1121V
3D simulation model with N^+ implant region	**923.5V**

As illustrated in Figure 6.3 (a), high electric field is observed at both the corner of the N^+ implant region, as well as the n^-/p^- vertical junction below. These combined high electric fields reach a critical electric field value at an earlier stage initiating impact ionization before the intended breakdown of the punch-through design n^-/p^- vertical junction to block over 1kV.

6.1.1 Simulating with the HF etch damage caused through activation and cap layer removal process

Through N^+ implant activation and SiO_2 cap layer removal process, the surface of SiC epitaxial layer was substantially damaged, especially where the N^+ implanted area took place by HF chemical etch. 1um thick SiO_2 cap layer was removed by immersing the sample in HF solution for 5 min. This duration was necessary not only to remove the thick cap layer, but to also remove small crystallized thermal oxide that began to develop between the SiC epitaxial layer and the SiO_2 cap layer. These thermal oxides tend to grow selectively more on where the phosphorus was implanted and chemical attack from the HF removed 50~75nm of epi layer as indicated Figure 6.4 (a) and (b)

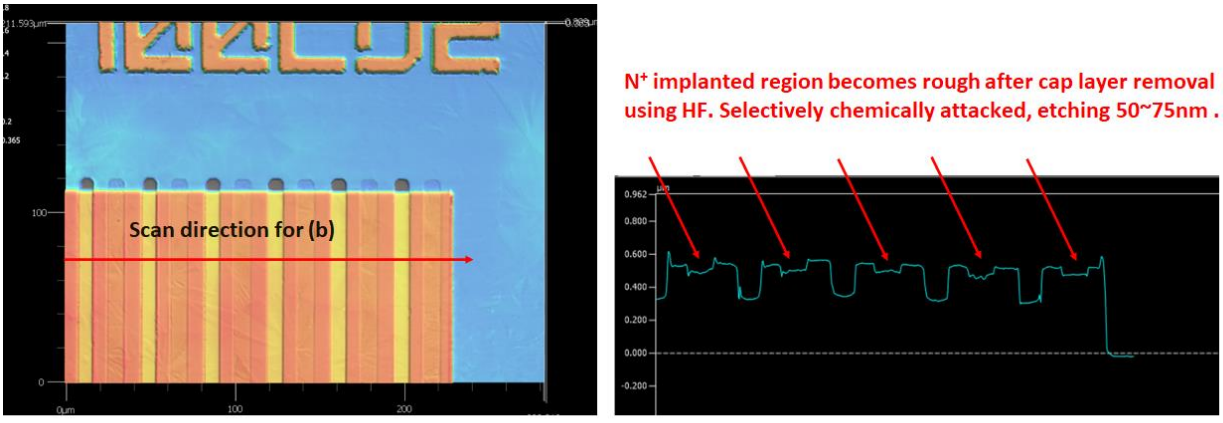


Fig. 6.4 Keyence Optical Profilometer image of the active area of the fabricated device after activation and cap layer removal (a) and scanned height profile (b)

Figure 6.4 (a) is the image of the active area of the fabricated finger device after dopant activation and cap layer removal. The image contains the anode line with recess etch in dark yellow indicating that the depth of this region is lower than the mesa etched top. The cathode line is lighter orange indicating that it is slightly deeper than the red mesa etched top resulting from the HF etch induced damage. As shown in the scanned height profile, there is a recess in depth of 50~75nm deep at the N^+ implanted region. In this section, we will simulate the effect of this loss in thickness which will results in reduction in charge in the n^- epi region and ultimately lowering of the vertical blocking voltage.

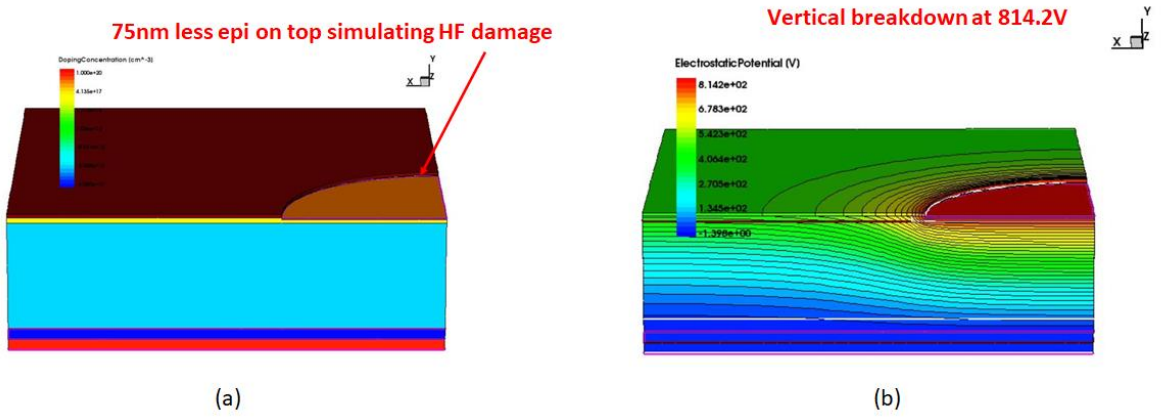


Fig. 6.5 3D TCAD model of the vertical breakdown voltage pattern with 75nm less epi on top simulating HF damage Top view (a) and electrostatic potential distribution (b)

Figure 6.5(a) shows the same vertical breakdown voltage pattern as the previous section but with 75nm less epi on top simulating HF damage. The n^- epilayer loses noticeable amount of charge and depletes quicker than the intended vertical breakdown of the punch-through designed thick p^- epi layer. As shown in Figure 6.5(b), the vertical breakdown happens at even lower voltage of 814.2V.

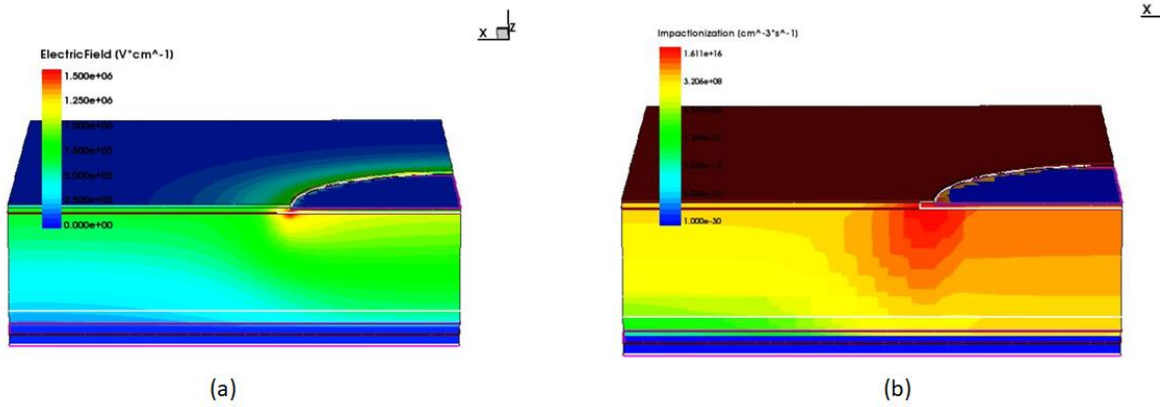


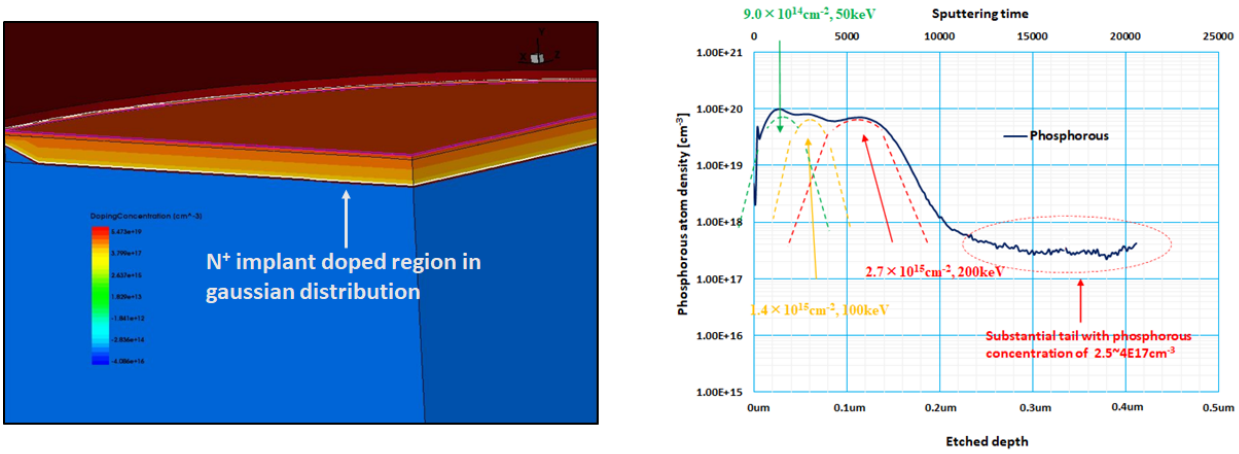
Fig. 6.6 3D TCAD model of the vertical breakdown voltage pattern with 75nm less epi on top simulating HF damage electric field distribution (a) and Impact ionization distribution (b)

Table 6.2 Comparison Between Simulated Vertical Breakdown Voltages Obtained from 2D and 3D Simulation Models

Simulated vertical breakdown pattern model	Breakdown Voltage
2D simulation model	1423V
3D simulation model without N^+ implant region	1121V
3D simulation model with N^+ implant region	923.5V
3D simulation model with N^+ implant region and HF damage	**814.2V**

6.1.2 Simulating with analytical doping profile modeling long implant tail going into p^- epi layer

As shown in the SIMS analysis from the previous section, actual phosphorous ion implant profile possesses a substantial amount of tail. This tail has 2~3 times more concentration than the background doping of the n^- drift epi layer and extends into the p^- epi layer. In this section, we will simulate the effect of this tail using analytical doping profile features in the TCAD simulation. In figure 6.7 (a) shows the TCAD model with contour change in doping profile modeling the actual implant profile obtained by the SIMS analysis. The top 200nm have a constant doing in ~1×10^{20} cm^{-3} equivalent to the obtained box profile. As the tail extends inward to the p^- epi layer, the doping concentration gradually becomes lighter with the final tail value being 1×10^{17} cm^{-3} in form of gaussian distribution.



(a) (b)

Fig. 6.7 3D TCAD model of the vertical breakdown voltage pattern with analytical doping profile simulating actual implant profile with long tail(a) and phosphorous ion implant profile from SIMS analysis (b)

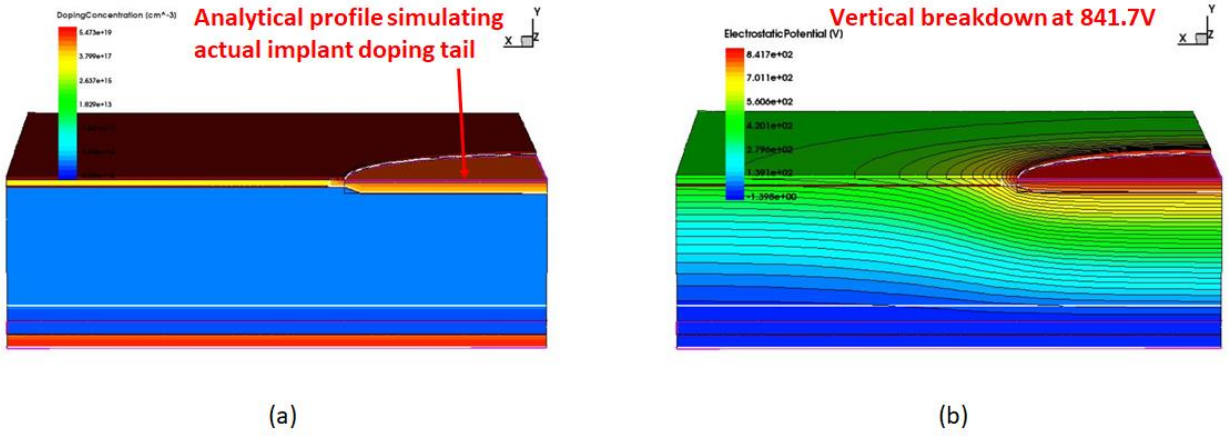


Fig. 6.8 3D TCAD model of the vertical breakdown voltage pattern with analytical doping profile simulating actual implant profile with long tail doping top view(a) and electrostatic potential distribution (b)

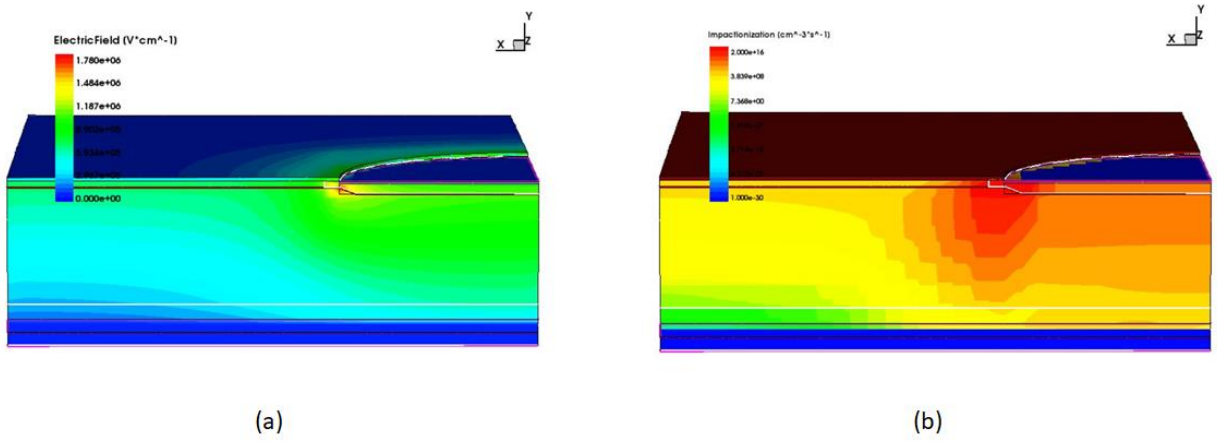


Fig. 6.9 3D TCAD model of the vertical breakdown voltage pattern with analytical doping profile simulating actual implant profile with long tail doping electric field distribution (a) and Impact ionization distribution (b)

Table 6.3 Comparison Between Simulated Vertical Breakdown Voltages Obtained from 2D and 3D Simulation Models

Simulated vertical breakdown pattern model	Breakdown Voltage
2D simulation model	1423V
3D simulation model without N^+ implant region	1121V
3D simulation model with N^+ implant region	923.5V
3D simulation model with N^+ implant region and HF damage	814.2V
3D simulation model with N^+ implant region with analytical doping profile and long tail	**841.7V**

Analytical profile simulation shows that the vertical breakdown voltage starts to drop when substantial amount of phosphorus tail goes into the p^- layer, forming a "linearly graded junction" where the impurity distribution varies linearly across the junction comparted to the original design of having an abrupt junction. Although it is known that linearly graded junctions have lower peak electric field compared to the abrupt junctions, much of the vertical blocking voltage is still supported by the p^- epitaxial layer thickness. Losing the necessary thickness in the p^- layer from the high energy, high dose N^+ ion implantation seems to be one of the reasons why the RESURF epitaxial wafer cannot retain the designed vertical blocking capability.

6.2 Major Contributions

This dissertation has covered theory calculations, TCAD device simulation, the mask layout technique, and fabrication processes required to fabricate lateral RESURF 4H-SiC Schottky barrier diodes and MESFETs.

The major contributions of this dissertation are laid out as follows:

1. Thorough TCAD device simulations and theory calculations were carried out to design and optimize n^- epi layer /p^- epi layer /p^+ substrate epitaxial wafer in terms of thickness and doping concentration for lateral RESURF device fabrication. First epi wafer and mask design were targeted aggressively to achieve the best forward performance at breakdown voltage of 600V, without sufficient vertical breakdown voltage margin.

2. A second design and process iteration of the proposed 600V lateral RESURF 4H-SiC Schottky barrier diodes and MESFETs with newly designed epitaxial wafers with vertical blocking capability of >1kV was conducted. The first run with this new epitaxial wafer and new set of masks showed blocking voltage as high as 900V without N^+ implant.

3. A second run with N^+ implant process of the same design above was conducted. The measured diodes showed greatly improved on-state performance compared to the previous run without N+ implant.

4. The final fabricated lateral RESURF 4H-SiC Schottky barrier diode with the best performance are set as follows:
    - Best forward performing diode: Specific on-resistance of 10.226 $m\Omega \cdot cm^2$ with a breakdown voltage of 575V.
    - Best reverse performing diode: Specific on-resistance of 14.713 $m\Omega \cdot cm^2$ with a breakdown voltage of 595V.

    The final fabricated lateral RESURF 4H-SiC MESFET with the best performance is:
    - Best forward performance at V_{GS}=0.6V with specific on-resistance of 5.699$m\Omega \cdot cm^2$ (Drain-Gate only) and 35.621$m\Omega \cdot cm^2$ (Drain-Source, the whole device area). The breakdown voltage of the above device was 525V at V_{GS}=-3.2V.

5. Successfully achieved quality ohmic contacts to *n*-type SiC. The experimentally evaluated TLM measurements showed specific contact resistance ρ_C as low as $1.746\times10^{-6}\ \Omega\cdot cm^2$. With the combination of N^+ implant and originally developed recipe for ohmic metal stacks (Ti/Ni/Ti/Au=20nm/90nm/6nm/120nm annealed at 1050 ℃ for 2 min in N_2 ambient), the ohmic contact fabrication process in forming cathode and source/drain region of lateral SiC device was established.

6. An alternative cap layer other than carbonized photoresist for SiC activation was developed, by encapsulating both front and backside of the ion-implanted sample with 1um-thick SiO_2 layer. The activation process at 1500 ℃, 30 min showed sufficient implanted phosphorus to be activated for low sheet resistance necessary for quality ohmic contact.

7. Had the abandoned model H18-40HT high temperature furnace in working order by replacing the required ten sets of $MoSi_2$ (Molybdenum Disilicide) heating elements. This furnace is currently the only furnace at Microelectronics Research Center/University of Texas at Austin that can operate at a high temperature of ~1600 ℃.

8. Experimentally verified that MESFETs with shallow recess etch underneath the gate have improved pinch-off voltage as low as -4V compared to MESFETs without shallow etch which have pinch-off voltage of -14V.

9. Developed and applied the contact open etch process utilizing multiple wet and dry etch techniques to form a 30°-degree angle sloped field plate structure in order to further ensure electric field distribution uniformity at the contact edges.

10. Converted the old micromanipulator probe station so as to be connected to the Keithley 2600-PCT-4B high voltage/high current digital curve tracer for measurements of fabricated power semiconductor devices at wafer/die level. Replacement parts for four probe manipulators were bought and restored so that the three vertical and lateral terminal devices can be evaluated.

6.3 Proposed Future Work

In this section details several suggested modifications and improvements to further increase the blocking capability of the proposed and fabricated lateral RESURF 4H-SiC Schottky barrier diodes and MESFETs. The fabricated results show roughly 200V less breakdown voltage than the intended design.

6.3.1 Layout modification

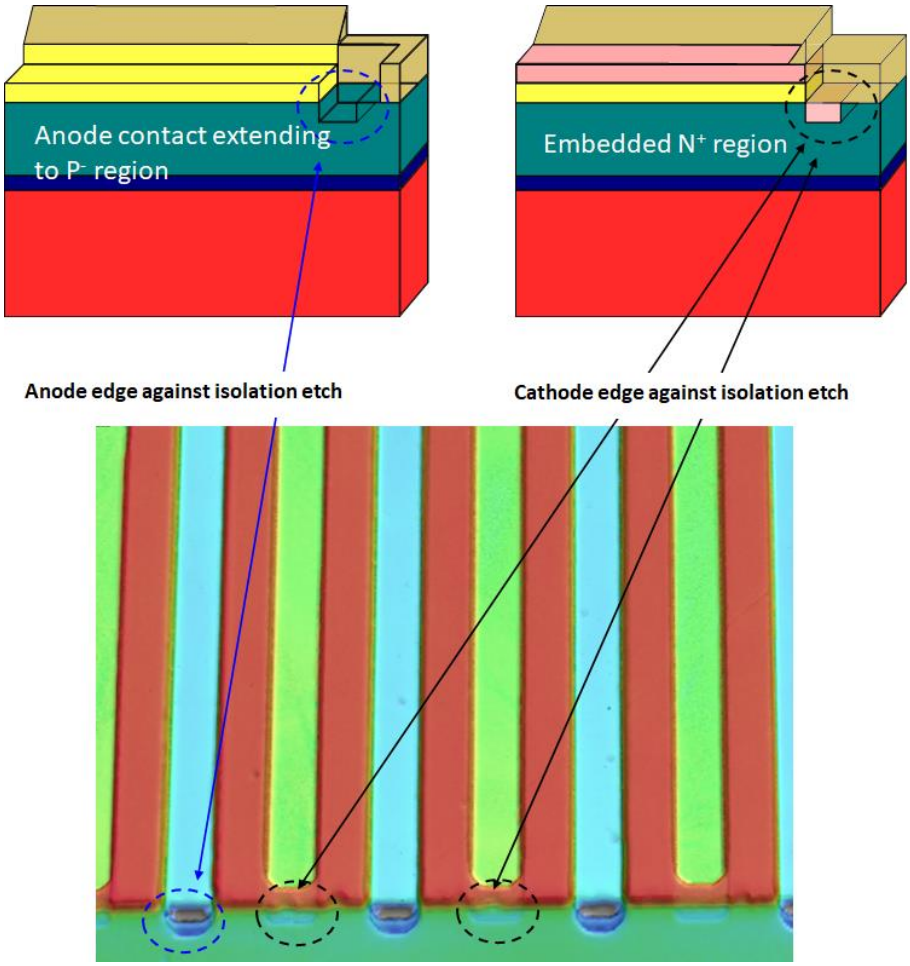


Fig.6.10 Explanation of anode and cathode region edge against the mesa isolation etch

There are still concerns in how both anode and cathode region extend to the mesa isolation edge. Having the recess etch and contact open overlapping against the mesa isolation is necessary in reducing 2D electric field crowding. The extended anode region makes contact to the bottom p^- layer forming a P-i-N diode structure. This may affect the forward *I-V* characteristics but should not cause problems in blocking capability of the device. On the other hand, overlapping of the N+ implant region

to the mesa isolation edge forms embedded N^+ regions which may affect the vertical blocking capability of the device at this edge. In the bottom figures are other proposed edge termination technique for lateral RESURF devices. If the thickness of the n- drift region is 1um or less, common effective edge termination is applying a box P^+ ion implant to completely surround the active region as shown in Figure 2. Applying positive bias in the active area will further deplete the P+ edge termination/n- active area junction and all current conduction is confined within the active area of the isolated island. Another simple but effective method is performing an isolation trench etch around the whole device structure as shown in Figure 3. This isolation etch can also act as a contact to the bottom p^- layer for the bottom gate operation in double gate JFET.

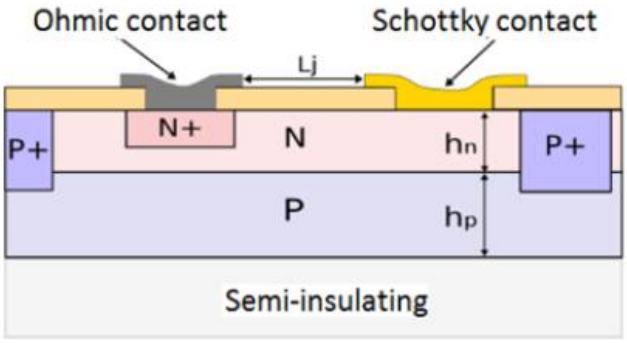


Fig. 6.11 Lateral REURF Schottky barrier diode with vertical box P^+ implant for isolation [34]

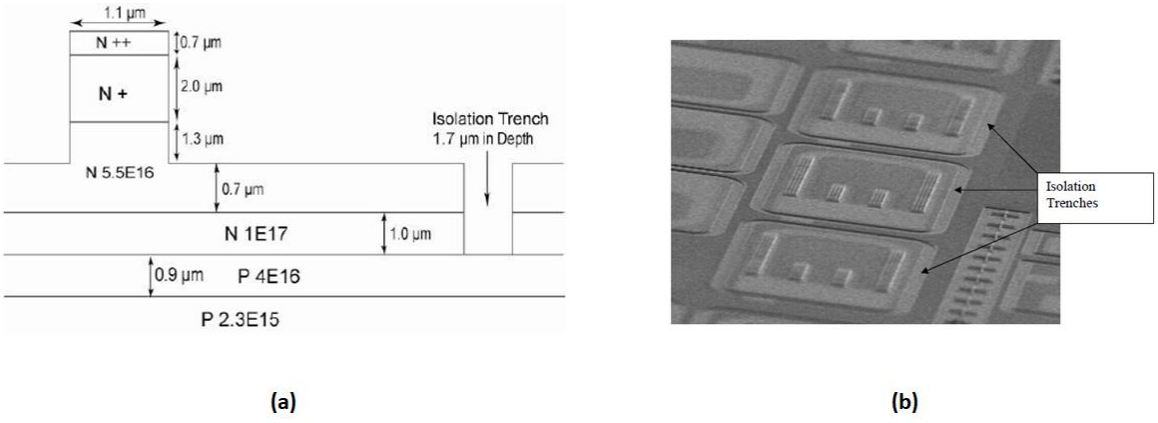


Fig. 6.12 Lateral REURF JFET with isolation trench [35]

6.3.2 Ion implantation and activation process modification

Shallow junction with minimum channeling effect and damage to the crystal is essential to retain the designed vertical blocking capability of the epi layers. Although phosphorous has a higher "solubility" in SiC material and is able to achieve higher active dopant concentration with lower activation temperature, nitrogen inflicts less damage to the crystal coming from smaller atomic mass as well as channeling effect occurs less frequently with this dopant. Heating during implantation or "hot implantation" helps avoid partial crystal recovery from high dose (> 3×10^{14} cm^{-3}) implantation which can cause complete amorphization of the crystal. As shown in the figure below, hot implantation is effective in further reducing sheet resistance at high implant dose. Equipment, such as IMPHEAT from Nissin, has the capability to perform ion implantation at an elevated temperature of 300℃ ~500 ℃

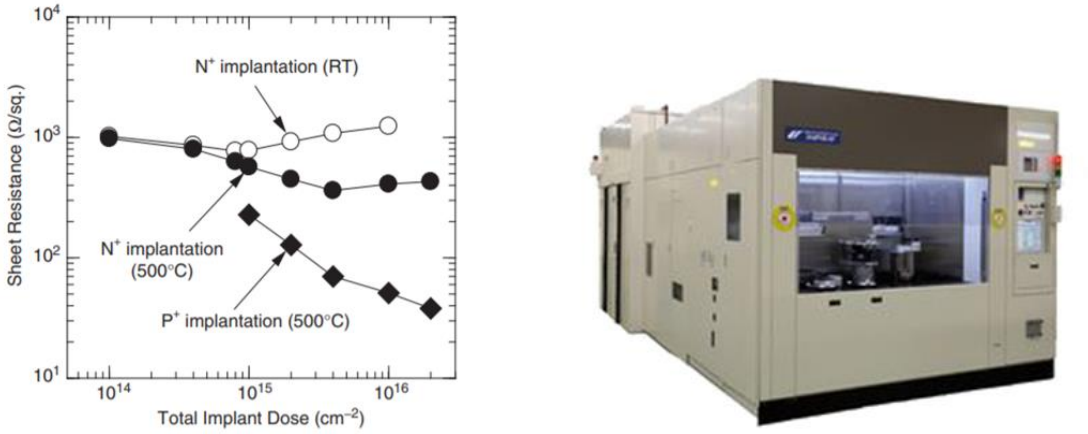


Fig.6.13 Sheet resistance versus the total implant dose for nitrogen- or phosphorus-implanted 4H-SiC (0001) annealed at 1700 ∘C for 30 min. (a) IMPHEAT® from Nissin capable of processing elevated temperature ion implantation(b)

6.3.3 Suggested Modification in Process Fabrication to Achieve Higher Blocking Voltage

- Nitrogen implant at lighter dose & lower energy to form shallower N^+ junction Hot ion implantation at 500 ℃ will further reduce crystal damage and improve ohmic contact.
- A thicker N^- drift epi layer (~1um) with same total integrated charge (lighter doping concentration) will make the effect of the N^+ junction depth irrelevant to the vertical breakdown of the designed RESURF epitaxial wafer.

- Less surface damage during the activation process, is also suggested, by modifying high temperature furnace setup, cap layer material, and improving cap layer removal method.

6.3.4 Choice of Cap Layer Material

Although using thick SiO_2 as the cap layer during the activation process was adequate for the current furnace setup proposed in this research project, pyrolyzed photoresist is still the standard material used widely today. For this carbonized photoresist to be effective, additional modifications are necessary, such as adding argon gas lines and vacuum pump to this high temperature furnace setup. By performing the activation annealing in vacuumed pressured Ar ambient, oxidation of both the cap layer and SiC sample can be suppressed. The cap layer will retain throughout the entire activation process and can be removed through the use of remover PG and O2 ashing with minimum damage to the sample compared to HF immersion. At these high temperatures of post-implantation annealing, the carbon cap layer will minimize Si out-diffusion (step-bunching) and will be capable of keeping an even smoother surface. Modification of the high temperature furnace can be costly, time consuming, and safety precautions need to be considered.

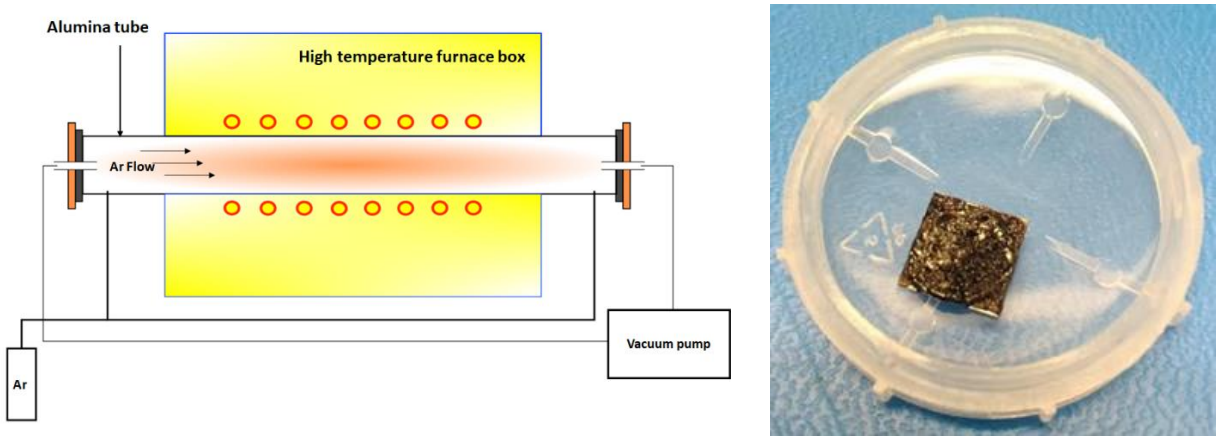


Fig. 6.14 Modified high temperature furnace with Ar gas line and vacuum pump for high vacuum Ar ambient annealing (a) SiC ion implanted sample with carbonized photoresist cap layer (b)

Fig. 6.15 Vacuum Sealing Assembly (Flange Lip I.D. 104 mm) with Vacuum Gauge and Valves for Alumina Tube (a) Edwards RV8 6.9 CFM Dual-Stage Vacuum Pump (b)

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Appendix A. Lateral RESURF 4H-SiC Schottky Diode and MESFET Fabrication Flow (With N^+ implant)

Integration Module	Process step	Process Module	Tool	Recipe details	Purpose	Comments
Wafer Preparation	Wafer dicing (MRC 2.406 room)	Dicing	Dicing Saw ADT	SiC epi and sub diced to 16mm x 16mm, with PR coated	Minimum half cut for furnace process	PR cover to prevent surface damage
	PR remove	Clean	Solvent Hood	70°C Remover PG, 10 min	Protection PR removal	
	Solvent clean	Clean	Solvent Hood	1) Acetone 2) IPA 3) Methanol 4) DI water	Remove organic residue	3000rpm/30 sec for each step
	Piranha clean	Clean	Acid Hood	H_2SO_4: H_2O_2 = 40 ml: 20ml for 15 min	Remove surface residue	
	BOE clean	Clean	Acid Hood	BoE etch for 30 sec	Remove native oxide	
Mesa Isolation (MA6 and ICP Oxford 100)	Solvent clean	Clean	Solvent Hood	1) Acetone 2) IPA 3) Methanol 4) DI water	Remove organic residue	3000rpm/30 sec for each step
	Piranha clean	Clean	Acid Hood	H_2SO_4: H_2O_2 = 40 ml: 20ml for 15 min	Remove surface residue	
	BOE clean	Clean	Acid Hood	BoE etch for 30 sec	Remove native oxide	
	Pre-photo clean	Clean	MARCH Asher	O2 plasma descum 30sec (descum recipe)		
	HMDS treatment	Photo	L10 Hood Spinner	Contact with surface 10sec->3000 rpm/30sec	Improve PR adhesion	MCC Primer 80/20 Use petri dish and pipette
	Bake	Photo	Oven	Bake at 110°C for 120sec		
	PR coating	Photo	L10 Hood Spinner	AZ 1518 5000RPM, 60sec		AZ 1518 stock positive photo resist
	Soft bake	Photo	Oven	Bake at 100°C for 60sec		
	Mask 1 - Isolation	Photo	MA-6	Exposure time: **7sec**		Use Si carrier piece with double-sided tape CH2 10W (Vac Purge 2, Full Vac 8, Pre 4) Vac Wec/CONT Mode
	Develop	Photo	Developer	50sec developing		
	Hard bake	Photo	Oven	110°C for 120sec		
	SiC mesa etch	Etch	ICP Oxford 100	ICP Oxford 100- SiC etch recipe SF6 =9sccm, O2=6sccm Pressure=5mtorr RF Power =100W ICP Power=800W Etch time= 630sec (10.5min)		0.4um etch with clean surface (increased oxygen reduces C-F bonds) Use cotton swab for backside oil placement
	PR remove	Clean	Solvent Hood	70°C Remover PG, 10 min		
	Piranha clean	Clean	Acid Hood	H_2SO_4: H_2O_2 = 40 ml: 20ml for 15 min	Remove surface residue	3000rpm/30 sec for each step
	BOE clean	Clean	Acid Hood	BoE etch for 30 sec	Remove native oxide	
Shallow Recess Etch (MA6 and ICP Oxford 100)	Solvent clean	Clean	Solvent Hood	1) Acetone 2) IPA 3) Methanol 4) DI water	Remove organic residue	3000rpm/30 sec for each step
	Piranha clean	Clean	Acid Hood	H_2SO_4: H_2O_2 = 40 ml: 20ml for 15 min	Remove surface residue	
	BOE clean	Clean	Acid Hood	BoE etch for 30 sec	Remove native oxide	
	Pre-photo clean	Clean	MARCH Asher	O2 plasma descum 30sec (descum recipe)		
	HMDS treatment	Photo	L10 Hood Spinner	Contact with surface 10sec->3000 rpm/30sec	Improve PR adhesion	MCC Primer 80/20 Use petri dish and pipette
	Bake	Photo	Oven	Bake at 110°C for 120sec		
	PR coating	Photo	L10 Hood Spinner	AZ 1518 5000RPM, 60sec		AZ 1518 stock positive photo resist
	Soft bake	Photo	Oven	Bake at 100°C for 60sec		
	Mask 2 - Recess	Photo	MA-6	Exposure time: **7sec**		Use Si carrier piece with double-sided tape CH2 10W (Vac Purge 2, Full Vac 8, Pre 4) Vac Wec/CONT Mode
	Develop	Photo	Developer	50sec developing		
	Hard bake	Photo	Oven	110°C for 120sec		
	SiC mesa etch	Etch	ICP Oxford 100	ICP Oxford 100- SiC etch recipe SF6 =9sccm, O2=6sccm Pressure=5mtorr RF Power =100W		0.2um etch with clean surface (increased oxygen reduces C-F bonds) Use cotton swab for backside oil placement

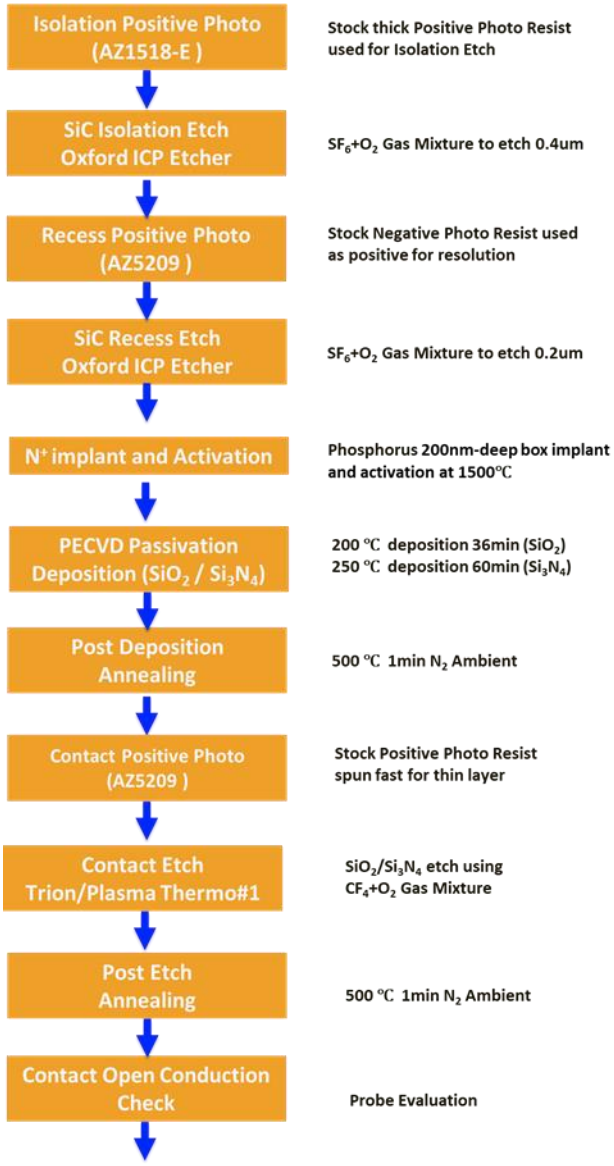
				ICP Power=800W Etch time= 630sec (10.5min)		
	PR remove	**Clean**	**Solvent Hood**	70°C Remover PG, 10 min	Protection PR removal	
	Piranha clean	**Clean**	**Acid Hood**	H_2SO_4: H_2O_2 = 40 ml: 20ml for 15 min	Remove surface residue	3000rpm/30 sec for each step
	BOE clean	**Clean**	**Acid Hood**	BoE etch for 30 sec	Remove native oxide	
N^+ implant (Nissin) and Activation	**HMDS treatment**	**Photo**	**L10 Hood Spinner**	Contact with surface 10sec->3000 rpm/30sec	Improve PR adhesion	MCC Primer 80/20 Use petri dish and pipette
	Bake	**Photo**	**Oven**	Bake at 110°C for 120sec		
	PR coating	**Photo**	**L10 Hood Spinner**	AZ 1518 5500RPM, 60sec		AZ 1518 stock positive photo resist
	Soft bake	**Photo**	**Oven**	Bake at 100°C for 60sec		
	Mask 3 – N implant	**Photo**	**MA-6**	Exposure time: 6.5**sec**		No carrier wafer needed CH2 10W (Vac Purge 2, Full Vac 8, Pre 4) Vac Wec/CONT Mode
	Develop	**Photo**	**Developer**	40sec developing		
	Hard bake	**Photo**	**Oven**	110°C for 120sec		
	Phosphorus implant	**Ion Implant**	**Ion Implant at Nissin**	$2.7\times10^{15}cm^{-2}$ 200keV Tilt 7 degrees, Twist 23 degrees		200nm-deep box profile implant
				$1.4\times10^{15}cm^{-2}$ 100keV Tilt 7 degrees, Twist 23 degrees		
				$9.0\times10^{14}cm^{-2}$ 50keV Tilt 7 degrees, Twist 23 degrees		
	PR remove	**Clean**	**Solvent Hood**	70°C Remover PG, 10 min		
	O2 ashing	**Clean**	**March Asher**	O2 plasma descum 600sec (descum recipe)		Remove carbonized PR from implant
	Activation	**Activation**	**High Temperature Furnace**	1500°C 30min Activation using 1um SiO_2 cap layer		
	Cap layer removal	**Clean**	**Acid Hood**	HF etch for 5min		
Passivation Deposition (PECVD)	**Light Etch Clean**	**Clean**	**March Asher**	O2 plasma descum 30sec (descum recipe)		
	Passivation dielectric deposition	**PECVD**	**PECVD 790 Plasma Therm #1**	400nm for 60min (JJCF402 for clean, SiN-AS.prc for deposition) NH3=2sccm, N2=25sccm, SiH4=20sccm, Pressure=400mTorr, RF Power = 20W, Temperature = 250°C	Passivation Layer	Adjust time from 60min~70min to achieve 0.4um thickness
	Dielectric anneal (PDA)	**RTA**	**RTA Allwin610 III-V**	Post deposition anneal 500 °C 1min in N2 ambient		Carrier wafer needed
Contact Open (MA6 and Plasma Thermo#1)	**HMDS treatment**	**Photo**	**L10 Hood Spinner**	Contact with surface 10sec->3000 rpm/30sec	Improve PR adhesion	MCC Primer 80/20 Use petri dish and pipette
	Bake	**Photo**	**Oven**	Bake at 110°C for 120sec		
	PR coating	**Photo**	**L10 Hood Spinner**	AZ 1518 5500RPM, 60sec		AZ 1518 stock positive photo resist
	Soft bake	**Photo**	**Oven**	Bake at 100°C for 60sec		
	Mask 4 - Contact	**Photo**	**MA-6**	Exposure time: 6.5**sec**		No carrier wafer needed CH2 10W (Vac Purge 2, Full Vac 8, Pre 4) Vac Wec/CONT Mode
	Develop	**Photo**	**Developer**	40sec developing		
	Hard bake	**Photo**	**Oven**	110°C for 120sec		
	SiN etch	**Etch**	**Plasma Therm #1**	Nitride etch recipe (80mTorr, 75W, CF4=40sccm, O2=1sccm,960sec)		Program: ASCF42.prc Finish off with BOE wet etch
	PR remove	**Clean**	**Solvent Hood**	70°C Remover PG, 10 min		
	O2 ashing	**Clean**	**March Asher**	O2 plasma descum 30sec (descum recipe)		
	Post ash RTA	**RTA**	**RTA Allwin610 III-V**	Post etch anneal 500 °C 1min in N2 ambient		Carrier wafer needed
Ohmic Contact Metal	**Solvent clean**	**Clean**	**Solvent Hood**	1) Acetone 2) IPA 3) Methanol 4) DI water	Remove organic residue	3000rpm/30 sec for each step
	Pre-photo clean	**Clean**	**MARCH Asher**	O2 plasma descum 30sec (descum recipe)		
	HMDS treatment	**Photo**	**L10 Hood Spinner**	Contact with surface 10sec->3000 rpm/30sec	Improve PR adhesion	MCC Primer 80/20 Use petri dish and pipette
	Bake	**Photo**	**Oven**	Bake at 110°C for 120sec		

	PR coating	**Photo**	**L10 Hood Spinner**	AZ 5209-E 4000RPM, 60sec		AZ 5209-E stock negative photo resist
	Soft bake	**Photo**	**Oven**	Bake at 100°C for 60sec		
	Mask 5 – Ohmic	**Photo**	**MA-6**	Exposure time: **3.4sec**		Use Si carrier piece with double-sided tape CH2 10W (Vac Purge 2, Full Vac 8, Pre 4) Vac Wec/CONT Mode
	Post exposure bake	**Photo**	**Oven**	120°C for 120 sec		Image reversal step
	Flood exposure	**Photo**	**MA-6**	Exposure time: **28sec**		
	Develop	**Photo**	**Developer**	35sec developing		
	Pre-metal clean	**Clean**	**MARCH Asher**	O2 plasma descum 30sec (descum recipe)		
	Cathode (Ti/Ni/Ti/Au)	**Metal**	**EVAP (CHA#1)**	Ti/Ni/Ti/Au=20nm/90nm/6nm/120nm		
	Metal lift-off	**Clean**	**Solvent hood**	Acetone (10 min) 70°C PG remover + Sonicator (< 1 min) Leave for 5~6 hours		Metal lift-off process
	Post metal annealing	**RTA**	**RTA Allwin610 III-V**	N2 Anneal 1000 °C for 2min (4 sets of 30sec)		Program: WT1000N.RCP
Schottky Contact Metal	**Solvent clean**	**Clean**	**Solvent Hood**	1) Acetone 2) IPA 3) Methanol 4) DI water	Remove organic residue	3000rpm/30 sec for each step
	Pre-photo clean	**Clean**	**MARCH Asher**	O2 plasma descum 30sec (descum recipe)		
	HMDS treatment	**Photo**	**L10 Hood Spinner**	Contact with surface 10sec->3000 rpm/30sec	Improve PR adhesion	MCC Primer 80/20 Use petri dish and pipette
	Bake	**Photo**	**Oven**	Bake at 110°C for 120sec		
	PR coating	**Photo**	**L10 Hood Spinner**	AZ 5209-E 4000RPM, 60sec		AZ 5209-E stock negative photo resist
	Soft bake	**Photo**	**Oven**	Bake at 100°C for 60sec		
	Mask 6 – Schottky	**Photo**	**MA-6**	Exposure time: **3.4sec**		Use Si carrier piece with double-sided tape CH2 10W (Vac Purge 2, Full Vac 8, Pre 4) Vac Wec/CONT Mode
	Post exposure bake	**Photo**	**Oven**	120°C for 120 sec		Image reversal step
	Flood exposure	**Photo**	**MA-6**	Exposure time: **28sec**		
	Develop	**Photo**	**Developer**	35sec developing		
	Pre-metal clean	**Clean**	**MARCH Asher**	O2 plasma descum 30sec (descum recipe)		
	Anode (Ni/Al/Ni)	**Metal**	**EVAP (CHA#2)**	Ni/Al/Ni=50nm/50nm/20nm		
	Metal lift-off	**Clean**	**Solvent hood**	Acetone (10 min) 70°C PG remover + Sonicator (< 1 min) Leave for 5~6 hours		Metal lift-off process
	Post metal annealing	**RTA**	**RTA Allwin610 III-V**	N2 Anneal 500 °C for 10 sec		Program: JJ500.RCP
Conduction Metal	**Solvent clean**	**Clean**	**Solvent Hood**	1) Acetone 2) IPA 3) Methanol 4) DI water	Remove organic residue	3000rpm/30 sec for each step
	Conduction Metal (Ti/Al/Cr)	**Metal**	**EVAP (CHA#2)**	Ti/Al/Cr=5nm/1000nm/10nm		
	Solvent clean	**Clean**	**Solvent Hood**	1) Acetone 2) IPA 3) Methanol 4) DI water	Remove organic residue	3000rpm/30 sec for each step
	Pre-photo clean	**Clean**	**MARCH Asher**	O2 plasma descum 30sec (descum recipe)		
	HMDS treatment	**Photo**	**L10 Hood Spinner**	Contact with surface 10sec->3000 rpm/30sec	Improve PR adhesion	MCC Primer 80/20 Use petri dish and pipette
	Bake	**Photo**	**Oven**	Bake at 110°C for 120sec		
	PR coating	**Photo**	**L10 Hood Spinner**	AZ 5209-E 8000RPM, 60sec		AZ 5209-E stock negative photo resist used as positive
	Soft bake	**Photo**	**Oven**	Bake at 100°C for 60sec		
	Mask 7 – Metal	**Photo**	**MA-6**	Exposure time: 9.5**sec**		No carrier wafer needed CH2 10W (Vac Purge 2, Full Vac 8, Pre 4) Vac Wec/CONT Mode
	Develop	**Photo**	**Developer**	25sec developing		
	Hard bake	**Photo**	**Oven**	110°C for 120sec		

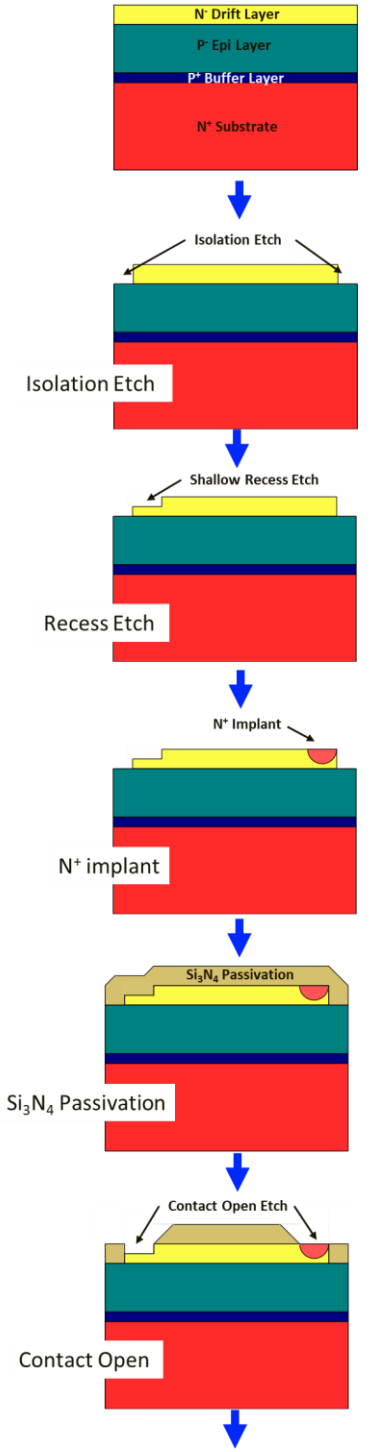
	Al etch	**Etch**	**Plasma Therm #1**	Aluminum etch recipe (60mTorr, 100W, BCl3=15sccm,480sec~720sec)		Program: ASBCL.prc Finish off with Al wet etchant
	Post metal annealing	**RTA**	**RTA Allwin610 III-V**	N2 Anneal 500 ℃ for 10 sec		Program: JJ500.RCP

Appendix B SiC lateral RESURF Schottky diode process flow

Simplified process flow and conditions



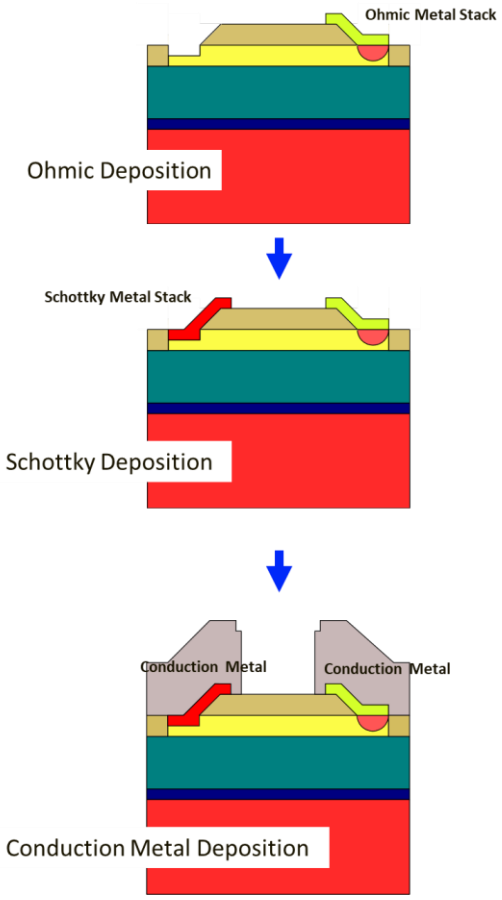
Simplified process flow figures



Simplified process flow and conditions (continued)

Ohmic Metal Photo (AZ5209)	Stock Negative Photo for Metal lift-off
Ohmic Metal Deposition CHA#1	Ohmic Metal Stack 116nm thickness
Post Metal Deposition Annealing	1000 ℃ 2min N2 Ambient
Schottky Metal Photo (AZ5209)	Stock Negative Photo for Metal lift-off
Schottky Metal Deposition CHA #1	Schottky Metal Stack 120nm thickness
Post Metal Deposition Annealing	500℃ 10sec N2 Ambient
Aluminum Deposition CHA#1 or Sputtering	Aluminum 1um thickness
Conduction Metal Layer Photo (AZ5209)	Stock Negative Photo Resist used as positive for resolution
Aluminum Dry/Wet Etch (RIE/Chemical)	Anisotropic Etch
Electrical Evaluation	

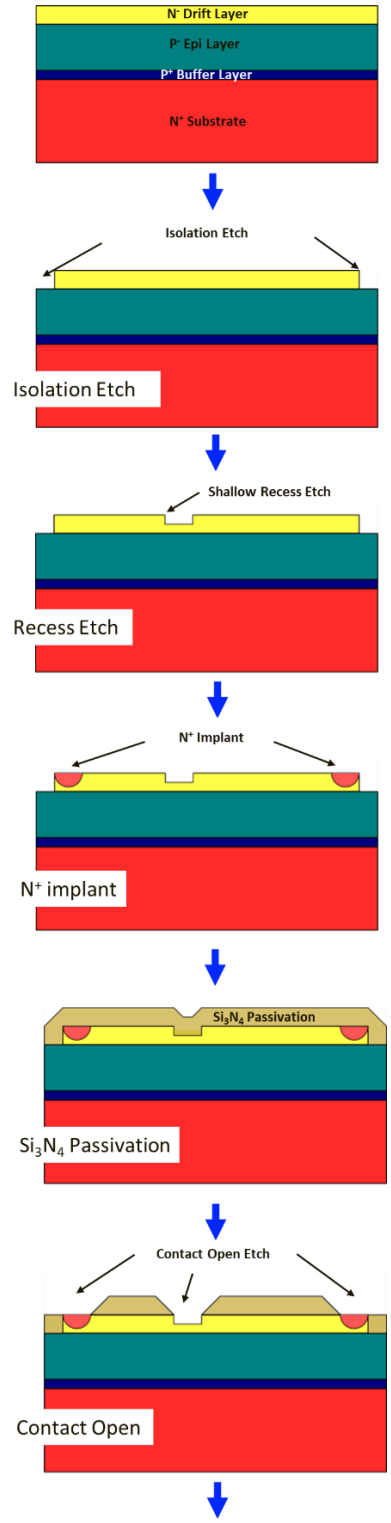
Simplified process flow figures (continued)



Simplified process flow and conditions

Isolation Positive Photo (AZ1518-E)	Stock thick Positive Photo Resist used for Isolation Etch
SiC Isolation Etch Oxford ICP Etcher	SF_6+O_2 Gas Mixture to etch 0.4um
Recess Positive Photo (AZ5209)	Stock Negative Photo Resist used as positive for resolution
SiC Recess Etch Oxford ICP Etcher	SF_6+O_2 Gas Mixture to etch 0.2um
N^+ implant and Activation	Phosphorus 200nm-deep box implant and activation at 1500℃
PECVD Passivation Deposition (SiO_2 / Si_3N_4)	200 ℃ deposition 36min (SiO_2) 250 ℃ deposition 60min (Si_3N_4)
Post Deposition Annealing	500 ℃ 1min N_2 Ambient
Contact Positive Photo (AZ5209)	Stock Positive Photo Resist spun fast for thin layer
Contact Etch Trion/Plasma Thermo#1	SiO_2/Si_3N_4 etch using CF_4+O_2 Gas Mixture
Post Etch Annealing	500 ℃ 1min N_2 Ambient
Contact Open Conduction Check	Probe Evaluation

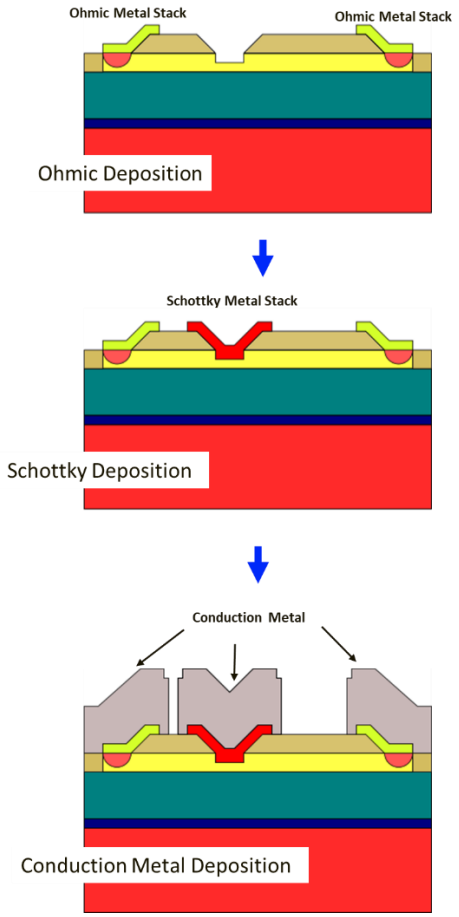
Simplified process flow figures



Simplified process flow and conditions (continued)

Ohmic Metal Photo (AZ5209)	Stock Negative Photo for Metal lift-off
Ohmic Metal Deposition CHA#1	Ohmic Metal Stack 116nm thickness
Post Metal Deposition Annealing	1000 ℃ 2min N2 Ambient
Schottky Metal Photo (AZ5209)	Stock Negative Photo for Metal lift-off
Schottky Metal Deposition CHA #1	Schottky Metal Stack 120nm thickness
Post Metal Deposition Annealing	500℃ 10sec N2 Ambient
Aluminum Deposition CHA#1 or Sputtering	Aluminum 1um thickness
Conduction Metal Layer Photo (AZ5209)	Stock Negative Photo Resist used as positive for resolution
Aluminum Dry/Wet Etch (RIE/Chemical)	Anisotropic Etch
Electrical Evaluation	

Simplified process flow figures (continued)



Publishing Lists

- **Atsushi Shimbori** and Alex Q. Huang, "A Novel 500V Lateral RESURF 4H-SiC MESFET with Sloped Field Plate for High Power and High Frequency Applications," IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA-Asia) 2020. (Oral presentation)

  Abstract—Silicon carbide (SiC) possesses a high breakdown field of 4×10^6 V/cm, high saturated electron drift velocity of 2×10^7 cm/s and good thermal conductivity of 4.9 W/cm·K attributing from its wide bandgap. These characteristics specifically make this material attractive for incorporating new approaches in device design such as the RESURF (Reduced Surface Field) technology, which is an innovative method for designing lateral high-voltage, low onresistance devices. In this research project, we have presented a 500V Lateral RESURF 4H-SiC MESFET with sloped passivation with measured specific on-resistance of 7.88m$\Omega\cdot cm^2$ and a breakdown voltage as high as 560V, which shows significantly higher power density over conventional RF GaAs devices and silicon LDMOS transistors.

- **Atsushi Shimbori**, Hiu Yung Wong, and Alex Q. Huang, "Fabrication and Analysis of Novel High Voltage Heterojunction p-NiO/n-Ga_2O_3 Diode," 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD). (Poster presentation)

  Abstract—A novel heterojunction NiO/β-Ga_2O_3 diode was fabricated using p-type NiO deposited by ion-assisted e-beam evaporation on n-type β-Ga_2O_3 epitaxial wafer. The fabricated diodes exhibited excellent rectifying current-voltage characteristics, with a rectifying ratio greater than 10^6 at ±4V. The breakdown voltage of the heterojunction diode was 525V for an un-terminated device. The measured specific on-resistance is 2.90m$\Omega\cdot cm^2$. The leakage current demonstrates one order of magnitude lower value than that of the comparison Ni/ β-Ga_2O_3 Schottky barrier diode. The breakdown voltage of the heterojunction NiO/β-Ga_2O_3 diodes is 4.5 times higher than that of the Ni/ β-Ga_2O_3 Schottky barrier diode.

- **Atsushi Shimbori**, Hiu Yung Wong, and Alex Q. Huang, **"**Comprehensive Comparison of Fabricated 1.6-kV Punch-Through Design Ni/n-SiC Schottky Barrier Diode with Ar^+ Implant Edge Termination and Heterojunction p-NiO/n-SiC Diode" IEEE International Electron Devices Meeting 2020 (Submitted)

  Abstract—A comprehensive comparison of a punch-through Ni/SiC Schottky diode with Ar^+ implant edge termination and heterojunction NiO/SiC diode was conducted through fabrication, electrical evaluation, TCAD simulation analysis and reverse recovery evaluation. Both fabricated diodes exhibited high breakdown voltage of 1595V, utilizing a punch-through design. The heterojunction NiO/SiC diode has shown ×0.5 less reverse leakage current than the Ni/SiC Schottky diode due to higher barrier height. The Ni/SiC Schottky diode, on the other hand, has shown 90% less reverse recovery time, indicating a small degree of minority carrier injection for the heterojunction NiO/SiC diode.

Teaching/Mentoring/Internship Experience

2019 Research Experiences for Undergraduates " Fabrication and Optimization of a Schottky Diode Utilizing Field Plate Termination," William Bennett, Mentor: **Atsushi Shimbori**

Power Semiconductor Device Research Engineer Internship, Ford Motor Company, June 2020 – August 2020
A member of power electronics team for research and development of traction invertor for automotive applications.

Power Module Characterization Internship, Wolfspeed/Cree Inc., May 2017–Aug 2017
A member of the design service of SiC power module.

Teaching Assistant (Lab Instructor) for ECE200 (Introduction to Signals, Circuits and Systems) at NCSU for five semesters and ECE331 (Principles of Electrical Engineering I) for one semester.

Teaching Assistant for EE394V (Power Semiconductor Devices) at UT Austin for one semester.