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Analysis of Electromigration in Single- and Dual-Inlaid Cu Interconnects

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Analysis of Electromigration in Single- and Dual-Inlaid Cu Interconnects

by

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Dedication

To my mother for her unwavering support.

To my father for his sage influence. To Robin for her kinship.

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Analysis of Electromigration in Single- and Dual-Inlaid Cu Interconnects

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The continual downward scaling of devices and increases in drive current have required an ever shrinking interconnect pitch and higher current densities. In order to overcome both the higher signal delay, as well as reliability concerns, new metallization technologies like Cu interconnects and low-k interlevel dielectrics have been developed. The implementation of inlaid Cu interconnects introduces a new set of material systems and structures which will result in new mass transport and failure mechanisms under electromigration. This study focuses on the characterization and understanding of electromigration induced failures in these advanced, 0.18 μm, Cu interconnects. Structures designed to test both the upper and lower interfaces associated with a Cu via will be used to understand the role of void formation and interconnect geometry in EM behavior. The effect of interconnect geometry is also examined using varying line width and

length structures. New statistically based methodologies, using multi-link test structures, will be developed and used to further understand the reliability of these advanced interconnects. These new statistical methodologies will be applied to EM tests on both single and dual-inlaid test structures.

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Chapter 1: Introduction

For the past twenty years semiconductor device scaling has resulted in many changes to interconnect technology. The continual downward scaling of devices and increases in drive current have required an ever shrinking interconnect pitch and higher current densities. The ever smaller interconnects now pose a significant delay to signal propagation in a chip [1] and are also much more susceptible to process defects as well as reliability issues. In order to overcome both the higher signal delay [2,3] as well as reliability concerns new metallization technologies like Cu interconnects and low-k interlevel dielectrics have been developed. With these new metallization technologies come new reliability concerns. Paramount amongst these reliability concerns is electromigration (EM) induced failure. Electromigration in interconnects has been studied since the late 1960's when it was first observed in wide Al based interconnects. This study will first focus on characterizing Cu / FTEOS based interconnects in terms of their integration, microstructure, and basic EM behavior. Furthermore, a statistical approach employing multi-link test structures will be used to better characterize the EM performance of a large population of interconnects such as the ones present on many modern semiconductor products. The improved characterization will yield more accurate extrapolations to use conditions as well as show greater sensitivity to process defects or early failure mechanisms. A brief history and overview of electromigration theory and its

application to sub-micron interconnects will be given in this introduction as well as an overview of the experimental work done in this study.

1.1 THEORY OF ELECTROMIGRATION

Electromigration describes the diffusion of metal ions aided by an electric current when an electric field is applied. Net atomic transport of metal ions arises under an applied electric field because of two effects. The first of these effects is the interaction of the applied electric field and the metal ions. This electrostatic force contains the interaction of the ion with valence Z and applied field as well as any electrostatic shielding from the surrounding electrons. The electrostatic force can be written as

$$\begin{aligned} F_{es} &= Z(1-k)e\vec{E} \\ &= Z_{es}{}^{*}\, e\vec{E} \quad \text{with } Z_{es}{}^{*} = Z(1-k) \end{aligned} \tag{1.1}$$

where k describes the electrostatic shielding and Z_{es}^{*} is the effective charge caused by the electrostatic force F_{es}^{*}.

The second contribution to the total force, F, arises from the momentum transferred to the ions from the electrons. This contribution is often referred to as the 'electron wind' force. The electron wind force, F_{wd}, contribution can be written as

$$\vec{F}_{wd} = -Z_{wd}{}^{*}\, n\lambda_d \sigma_d \tag{1.2}$$

\

where n is the electron density, λ_d is the electron mean free path between collisions, and σ_d is the cross-section of the electron-ion collision.

The total force, F, is simply the sum of these two components.

$$\begin{aligned} \vec{F} &= \vec{F}_{es} + \vec{F}_{wd} \\ &= (Z_{es}^{*} + Z_{wd}^{*})e\vec{E} \\ &= Z^{*}e\vec{E} \end{aligned} \tag{1.3}$$

where Z^* is the effective charge number for the migrating metal ions described in this system.

The atomic flux can then be obtained through the relation $J = \mu F$ where μ is the atomic mobility. The atomic mobility can also be expressed in terms of the diffusion coefficient according to the Nernst-Einstein equation, $\mu = nD/kT$ where n is the mass density of the metal, k is Boltzman's constant and T is the absolute temperature. By substituting the applied electric field with the product of the current density, j, and the metal resistivity, ρ, the following equation is derived.

$$\begin{aligned} J_e &= n(D/kT)Z^{*}e\rho j \\ &= nv_e \end{aligned} \tag{1.4}$$

where , J_e, is the atomic flux due to electromigration and v_e is the drift velocity due to electromigration.

1.2 ELECTROMIGRATION IN INTERCONNECTS

The interconnects of modern semiconductor products are highly dense and intricate networks containing millions of line segments terminating with vias and contacts. These line segments vary in length and width depending on their function in the circuit. Each interconnect level can also vary in the minimum dimensions allowed as well as many processing details. In Figure 1.1 we can see a cutaway SEM micrograph of a typical interconnect stack showing the density and complexity of these structures. In Figure 1.2 we see a closer view of a interconnect structure showing a metal line terminating with a via. In a typical semiconductor device it only takes the failure of one of these metal line segments or vias to cause the entire chip to fail. So it is not only important to study how individual lines fail but also how the survival of the entire chip is related to these fundamental mechanisms. Because the chip is made of a large number of varying width and length interconnects it is important to gain an understanding of the role of interconnect geometry on the electromigration reliability. It is also important to address the large number of interconnect segments through the use of statistical analysis of the electromigration failure.

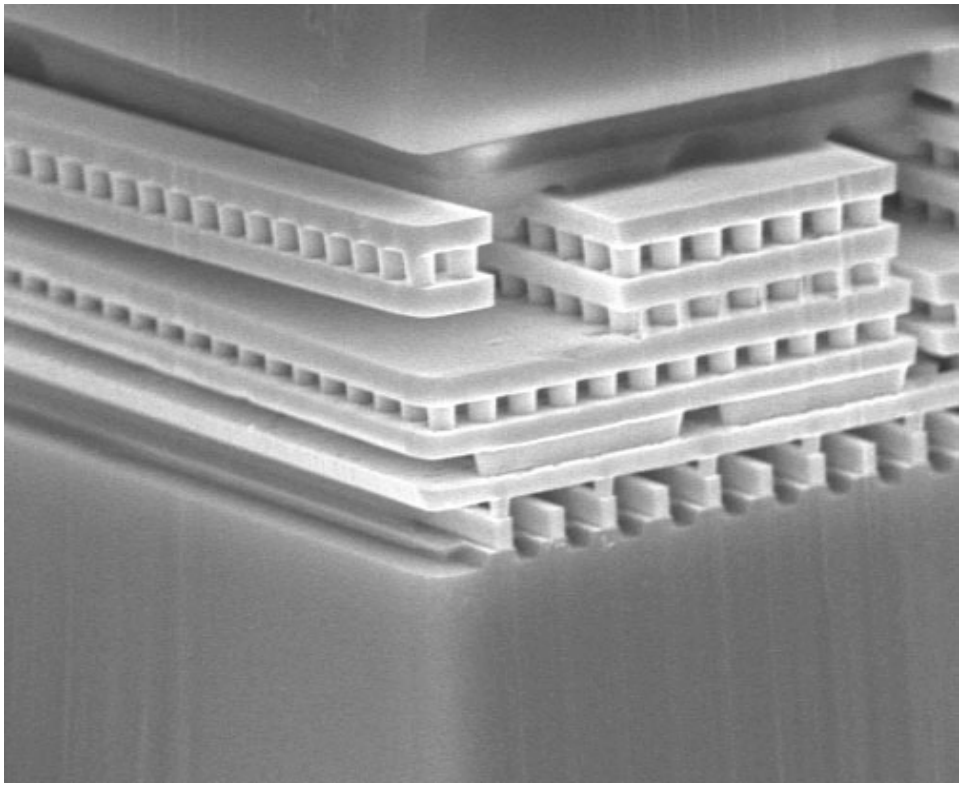


Figure 1.1: (a) The interconnects of a typical semiconductor chip. The chip has been etched away to reveal several levels of the metal line segments and vias.

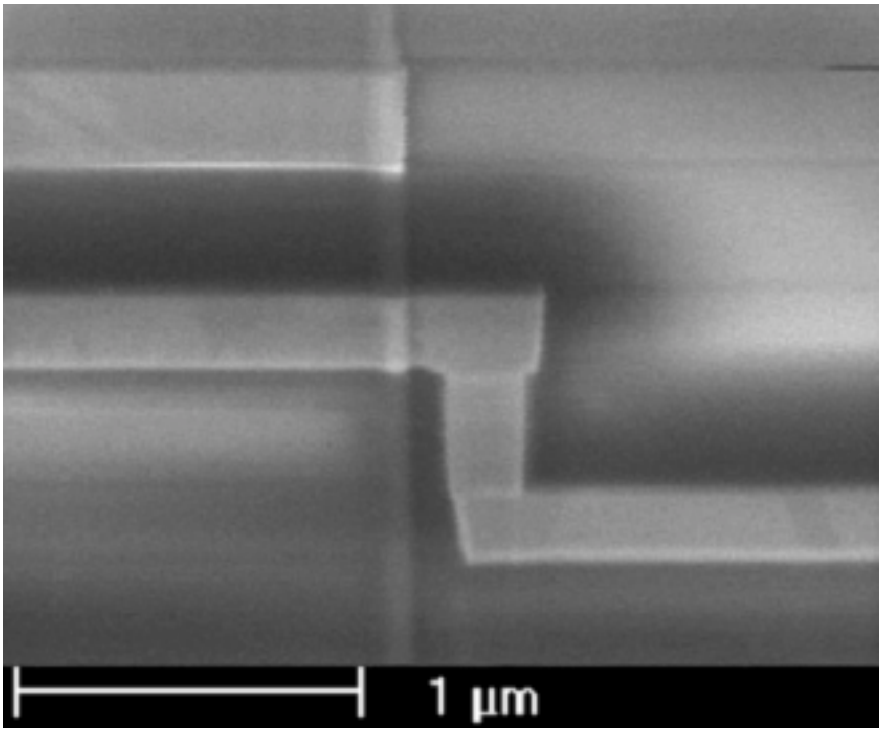


Figure 1.2: (a) A close up view of a metal segments connected by a via. A third metal level can be seen in the top of the picture. The fold in the middle of the image is a result of the FIB sample preparation technique.

The most fundamental aspects of EM are those that relate to the mechanisms of diffusion in the metal lines and vias. Electromigration in interconnects can occur through several different diffusion paths. These paths include diffusion through the bulk, grain boundaries, dislocations, and interfaces. The effective diffusivity can be written as the sum of the diffusivities associated with different paths. The following equation shows the effective diffusivity written as the sum of the bulk, grain boundary, interfacial, and dislocation pipe diffusivities.

$$D_{eff} = D_b + \sum_j^n D_{gb,j}(\frac{\delta_{gb,j}}{d}) + D_i\left[2\delta_i\left(\frac{1}{w}+\frac{1}{h}\right)\right] + D_p\rho_{disl}d^2 \qquad (1.7)$$

where D_{eff} is the effective diffusivity, δ is the diffusion pathway cross section for the various pathways, and *d* is the width of the grain boundary, *w* is the width and *h* is the height of the interconnect. In the case of interconnect structures the most important terms are the grain boundary diffusion and interfacial diffusion. The bulk term can be ignored because the temperatures used for accelerated testing are too low for this mechanism to contribute. The dislocation pipe term can be ignored because the dislocation density is too low for this mechanism to account for much diffusion. For Cu interconnects the model can be further described by identifying the critical interfaces and flux divergence points.

The drift velocity Cu under electromigration can be expressed as

$$v_d = D_{eff}Z_s^* e\rho j / kT \qquad (1.8)$$

where D_{eff} is the effective diffusivity, Z_s^* is a coefficient based on momentum transfer from electrons to Cu atoms, e is the electrical charge, ρ is the resistivity, j is the applied current density, k is Boltzman's constant, T is the temperature in Kelvin. Electromigration failure is caused when enough Cu has drifted from the via in order to form a fatal void. The time required to form these fatal voids can be expressed as a function of the drift velocity in the following way

$$TTF = l_v / v_d \tag{1.9}$$

where l_v is the length of the fatal void. This equation forms the basis of another important equation in the analysis of electromigration, Black's equation [4]. Black's equation links the median time to failure to the applied stressing conditions, current and temperature. Black's equation in general terms is listed below:

$$MTTF = AJ^{-n} e^{E_a/kT} \tag{1.10}$$

where *MTTF* is the median time to failure, *A* is constant containing many of the terms from Equation 1.8, *N* is the current density exponent, E_a is the activation energy, *J* is the applied current density, *K* is the Boltzman constant, *T* is the temperature in Kelvin

In more specific terms Black's equation contains the activation energy for the diffusion mechanism and the other constants associated with that mechanism incorporated into the constant A. It is based on drift velocity equations and includes a current exponent term that in the case of Cu interconnects should be equal to 1.

Another important consideration of EM in interconnects is that of the stress-induced back flow, or 'Blech' effect [5]. If the particular metal line of interest is embedded in a stiff dielectric material like SiO_2 a third force is created

which opposes the two previously described forces. This third force arises as atoms are depleted from the cathode and accumulate at the anode. This net electromigration flux creates a stress gradient opposite to the direction of the electromigration flux. The net flux equation, which includes this 'back-stress' is expressed as

$$\begin{aligned} J_{net} &= nv_d = n(v_e - v_b) \\ &= n(D/kT)(z^* e\rho j - \Delta\sigma\Omega_a / L) \end{aligned} \tag{1.11}$$

Where V_d is the net drift velocity, $\Delta\sigma$ is the stress gradient, Ω_a is the atomic volume, and L is the line length.

The back-stress affect can improve the electromigration resistance of metal lines if the product of the current density, j, and line length, l, is equal to or less then a threshold value, Γ. If the current density is held constant then there arises a critical length, L_c, below which there will be no net electromigration flux. The threshold value and the critical length are expressed as

$$\Gamma = jL_c = \Delta\sigma\Omega_a / Z^* e\rho \tag{1.12}$$

The back-stress effect is an important consideration from a reliability stand point, because designers can create interconnect layouts that are mostly electromigration resistant by keeping the majority of lines below the critical length. But if the insulator material that surrounds the metal lines is not as stiff as

the metal there may not be a back-stress. The presence of a back stress will also act to slow the electromigration damage formation in lines that are longer then the critical length.

Special consideration must be given to whether the interconnects are made with a single- or dual-inlaid process scheme when discussing the critical length. The development of the compressive stress gradient that is essential to the critical length is largely dependent on the amount of mass that is accumulated at the anode. In the case of dual-inlaid structures, a flux divergence point exists at the bottom of the via which can cause fatal voiding at that location. This voiding can create an open without displacing much Cu and result in EM failure before enough Cu has migrated to the anode to create the compressive stress gradient. The result of this is that for Dual-inlaid Cu interconnects the existence of a critical length product is largely dependent on void location and morphology.

1.3 OVERVIEW OF WORK

This work focuses on the characterization and understanding of electromigration induced failures in advanced Damascene, or inlaid, Cu interconnects. This effort is broken up into four components. In the first part the Cu interconnect test structures are characterized in terms of their design and manufacture as well as their microstructure. This was done in order to fully understand the role of design or process details on the EM performance of the structures. Secondly, the basic EM characteristics are examined. These basic studies will look into the fundamental properties of EM in Cu interconnects including temperature acceleration, diffusion mechanism, and void formation, and lognormal failure statistics. The basic studies will provide the empirical base for the following two sections of this work.

The third section will examine how interconnect geometry impacts the EM performance. The geometry study will examine structures of varying length and width. For the last section a new statistically based methodology, using multi-link test structures, will be developed and used to further understand the reliability of these advanced interconnects. In this fourth section, samples made with single-Damascene fabrication methods will be examined using the new statistical methodology. This new methodology will be shown to improve both early fail detection as well as statistical confidence. The improved statistical confidence will result in more realistic lifetime extrapolations that are essential to accelerated testing. Also, in the fourth section, samples made with a dual-Damascene process scheme will be examined using the same methodology. As in the case of the

single-inlaid structures, the new methodology will be shown to greatly improve the sensitivity to multi-modal failure. This heightened sensitivity is critical to identifying process induced failure mechanisms, which in turn can help process development. These structures have been manufactured at the Motorola Advanced Products Research and Development Lab (APRDL). All of the EM testing and characterization work in this study was conducted at APRDL.

Chapter 2: Experimental Techniques

In the following section all of the experimental techniques used in this work including microstructure characterization and electromigration testing will be described. The theory behind each technique as well as the fundamental aspects of its use will be briefly described followed by a section detailing the technique's use specific to this work. This chapter will act to familiarize the reader with the experimental aspects of this work in order to create a basis of understanding the results sections to follow.

2.1 MICROSTRUCTURE CHARACTERIZATION

Microstructural analysis was conducted on representative samples in order to determine the distribution of Cu grain sizes in the minimum width interconnect structures. Transmission Electron Microscopy (TEM) images were taken of special test structures that contain a large amount of parallel interconnect lines. Although these structures are generated using a different photo mask set then the structures used for EM testing, the geometry and process steps were the same. These parallel line structures were used instead of the EM test structures because they provide many more lines in a viewing area. Figure 2.1 shows a schematic cross-section of the parallel line structures used for grain size determination. The details of the stack geometry and materials are the same as those of the EM test structures.

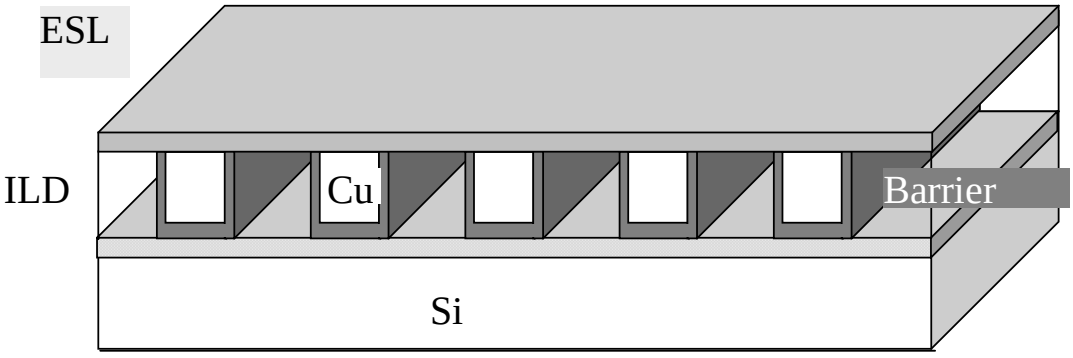


Figure 2.1: Schematic cross section of the parallel line structure used for grain size analysis.

In order to obtain the grain size distribution in these 0.18μm wide lines, plan view TEM samples were prepared. The samples were first prepared using a wedge polishing technique using a tripod holder and polishing wheels. Once the sample wedge had been prepared the sample was further thinned by ion-milling, which resulted in a sufficiently large area that is transparent in the TEM.

The TEM imaging was done with a JEOL 2010™ set to 200kV accelerating voltage. The TEM transparent region was then imaged at zero sample tilt condition. The plan view images created from the zero tilt were used as the reference for the analysis described later. The transparent region was then imaged with a series of different sample tilt angles. By changing the sample tilt angle the electron diffraction conditions are changed leading to different amounts of grain contrast. The sample tilt also allows for the identification of grain boundaries that might not be apparent at the zero tilt condition. Many twins can also be identified with the varying tilt angles. These twins were not counted as

separate grains as the twin boundary is not likely to contribute to Cu diffusion or voiding.

With all of the images collected, the grain size was determined by tracing the outlines of the grains found at the zero-tilt condition. Grain boundaries found at the other tilt conditions were added to the original grain boundary trace. The grain boundary trace was then analyzed using the ImageProPlus™ microstructure analysis software package. The grain boundary traces allowed for simplified grain area analysis using the automated software package. The grain areas were then converted to a linear dimension (diameter) by mapping the grain areas to circles and determining these circles diameter. This diameter value was used as the measure for grain size.

2.2 ELECTROMIGRATION TESTING

Electromigration testing is essentially accelerated testing of interconnects using heat and electrical current as the accelerating factors. Electromigration, being a diffusion-controlled phenomenon, is thermally activated, allowing for the acceleration of testing through increased temperature. The lifetime of the interconnects will have an Ahhrenius dependence on temperature as shown in the prior chapter. In this study the EM tests are conducted at temperatures ranging from 250^{o}C. to 350^{o}C. As in any accelerated testing, it is important to conduct the tests in a range of temperatures that allow for the same failure mechanisms one might see at operating conditions (65^{o}C. to 150^{o}C).

The applied current can also be used as an accelerating factor during EM testing. This is true because the rate of drift of Cu ions, and hence the interconnect lifetime, is dependent on the current density. In this study, no current density acceleration was used. This is due to the fact that at higher current densities Joule heating can occur and confound the results. Global Joule heating resulting from high current densities will result in higher test structure temperatures and an increase in the Ohmic resistance. These changes can easily be dealt with by fully characterizing the level of joule heating and incorporating it into lifetime extrapolations. The problem lies in local Joule heating that can occur in thinned Cu sections or stretches of exposed barrier during EM failure. The impact of this local joule heating is difficult to characterize and as a result is not treated in this work.

2.2 EM SAMPLE PACKAGING

All of the EM testing conducted for this study was done using package level testing with the use of wirebonded die. Package level experiments differ from wafer level experiments in several ways. In wafer level EM experiments, a wafer is placed on a hot-chuck, and microprobes are leveled into contact with the test structure. The advantage of this method is that it does not require the expense of packaging the test structures. However, the technique is severely limited in that it can not effectively test a large sampling of test structures. Wafer level experiments were used in this work to measure the amount of joule heating in a small number of structures.

Package level testing was used in this study because it allows for the sampling of a large number of devices under test (DUTs). In package level testing the wafers are first diced using a diamond saw to provide die that contain the test structure. These die are then bonded to IC package, like the 16-Pin dual inline package (DIP) packages used in this work. In Figures 2.1 and 2.2 a typical ceramic DIP package used in this study is shown. The package consists of two rows of 8 pins that correspond to bonding posts that surround the well of the package. In order to connect the test structure to the tests system wirebonds are connected to the bond pads of the test structure to the bonding posts of the package as seen in Figure 2.1. The wirebonded packages are then loaded into socket boards, which then are loaded into an EM testing oven. The electrical connections are made through the socket boards, to the packages and then through the wirebonds to the structure. The main advantage of this technique is that it allows for testing of great number of samples simultaneously.

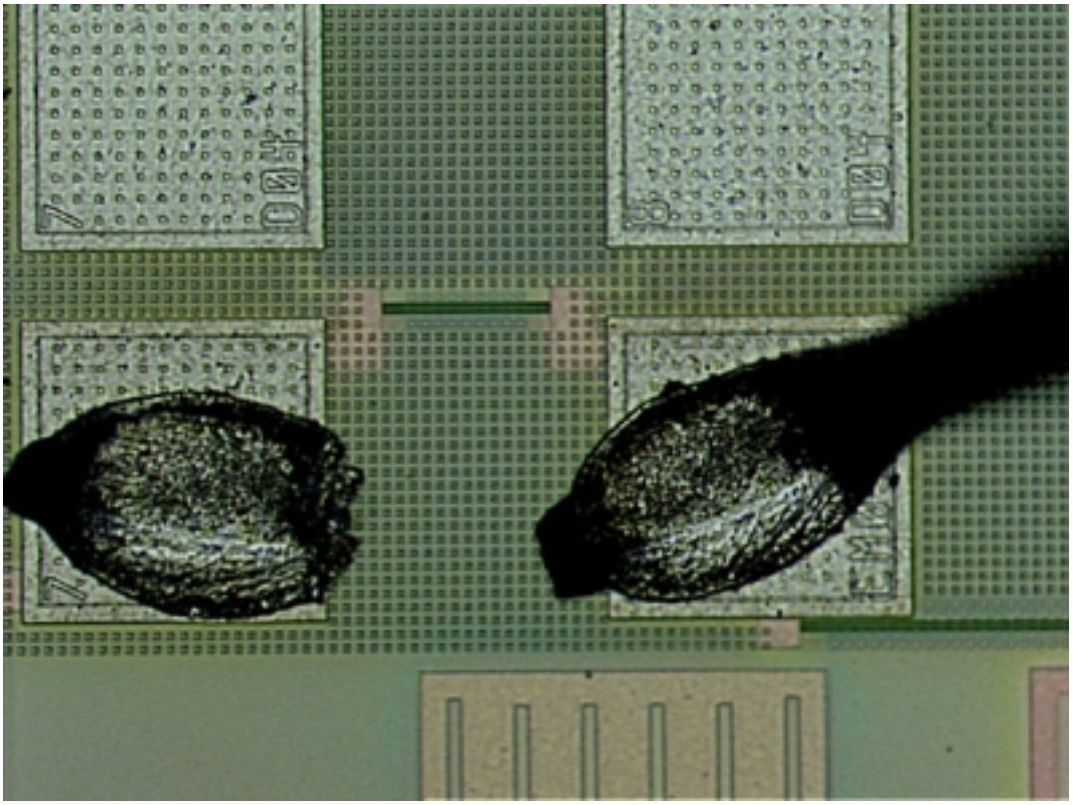


Figure 2.2 A view of 50μm long test structure located between two bond pads. Wirebonds can be seen on both of the pads.

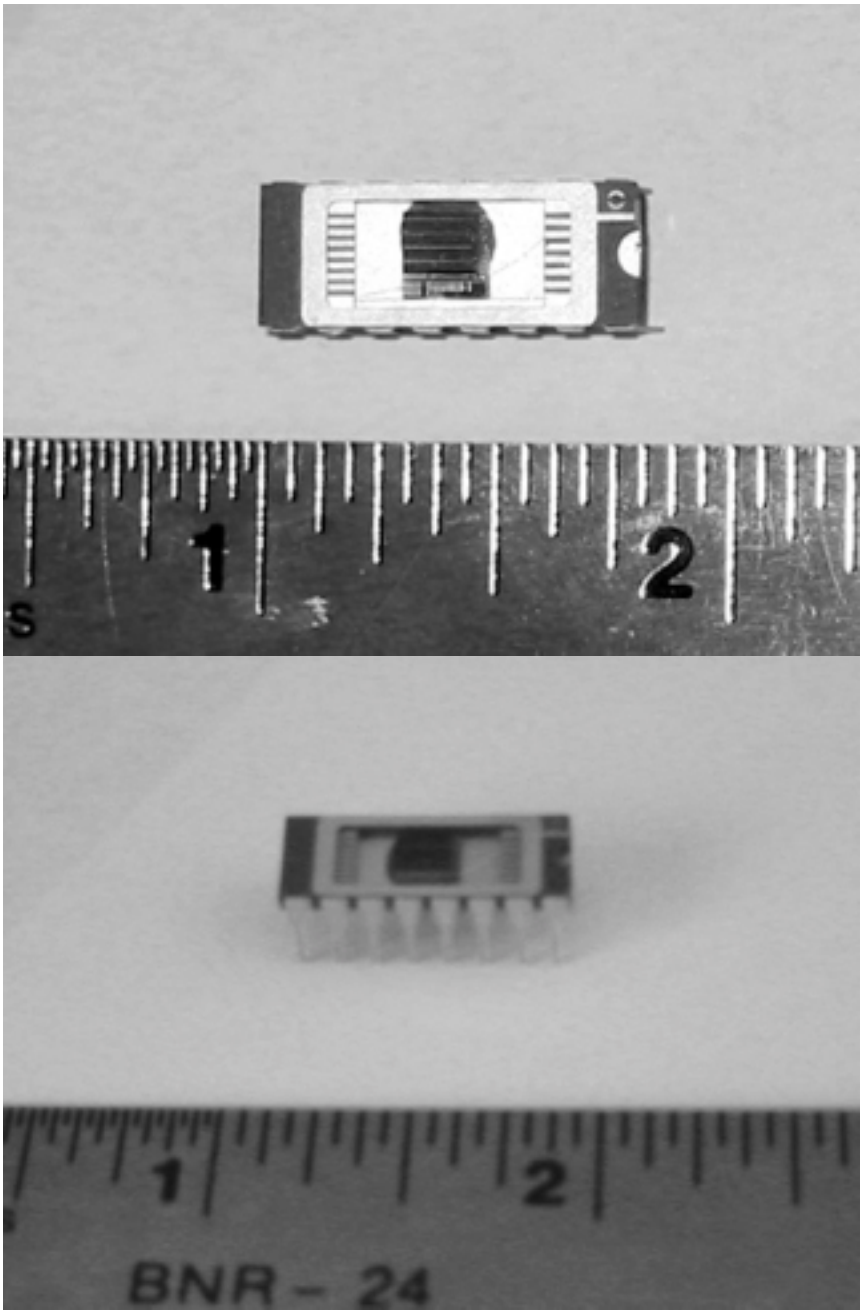


Figure 2.3 (a) A top-down picture of the 16-pin dual inline package. In this view the die sitting in the die well can be seen. The wirebond posts are seen on the right and left side of the well. (b) A perspective view showing a row of 8 pins.

2.3 EM TEST SYSTEM DETAILS AND SPECIFICATIONS

EM testing in this work was done using 5 Qualitau™ semiconductor reliability testing systems. These systems are based on 2 - 4 ovens containing slots for 10 high temperature socket cards. In Figure 2.3 two of these socket cards are shown. The cards are similar to typical printed circuit boards (PCBs) but are based on steel boards with insulating materials surrounding them. This design is necessary to allow the cards to operate at high temperatures. The socket cards' function is to connect the pins of the DIP packages to the electronics of the test system. The removable design allows for easy loading and unloading. Each of these sockets cards can hold 6 or 12 DIP packages of various pin counts and sizes for a total of 60 sockets per oven. For the systems based on 2 ovens, each socket can hold 2 individual devices under test (DUT). For the systems based on 4 ovens, only one DUT can be tested per socket. Either way, each test system can test a total of 240 DUT's at a time. The two different arrangements allow for flexibility when it comes to the number of DUT's per test as well as the packaging arrangement. Having two DUT's per package allows for more efficient use of wafers as well as reduced packaging costs, and the smaller capacity ovens allow for testing a smaller sampling of parts at a wide range of temperatures without impacting the remaining testing capacity.

Each of the 5 test systems has similar performance specifications. The oven temperatures can range up to 350^{o}C with or without a N_2 ambient. The electronic performance of these systems depends on which of the two available power supply units is engaged. For all of the EM testing done in this work the

high current power supply module was used. This power supply module can deliver a fixed DC current with a total voltage compliance of about 9 volts in the range of currents used in this study.

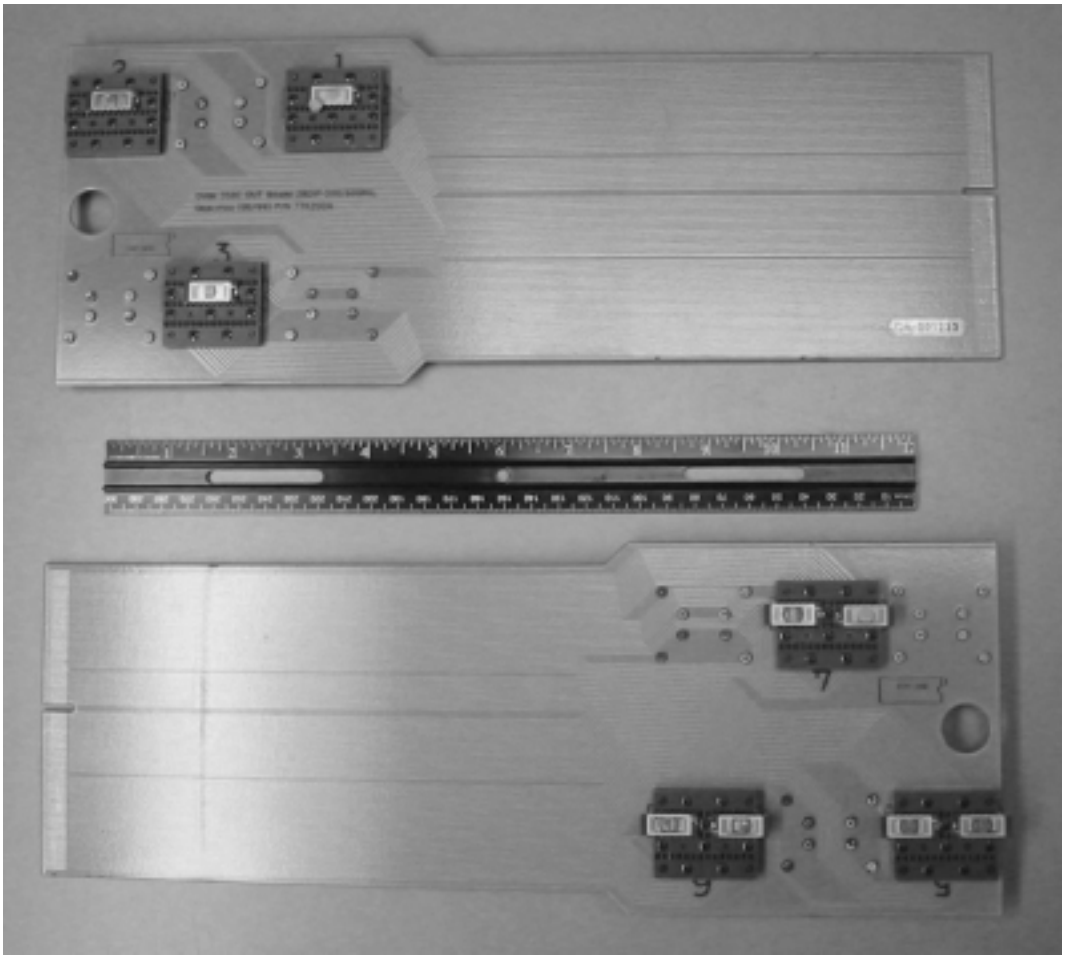


Figure 2.4 A picture of two Qualitau™ socket boards. Each board contains six sockets, which can hold 1 or 2 DIP packages depending on the system. The boards have a maximum use temperature of 350C.

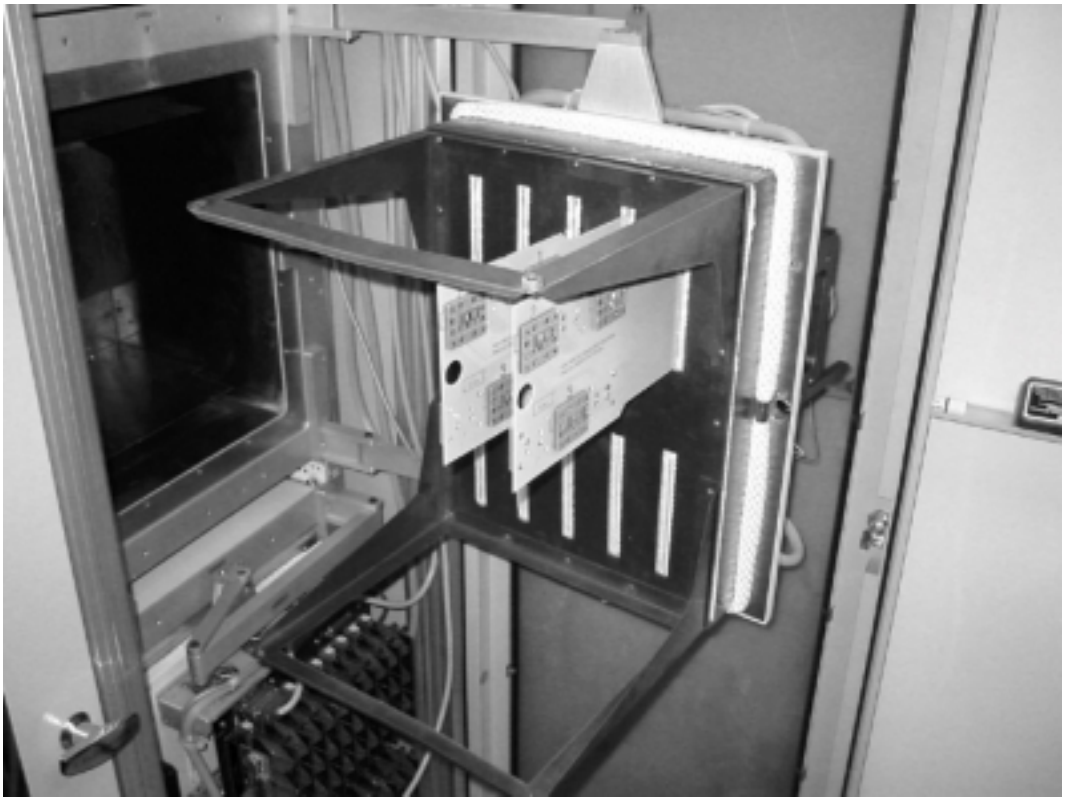


Figure 2.5 A picture of an open Qualitau™ oven. Each oven contains slots for 10 socket cards. The cards are loaded into the oven so that they make electrical contact at the face of the oven.

2.3 WAFER LEVEL JOULE HEATING TESTS

Wafer-level tests were conducted to measure the amount of joule heating created with different levels of stressing current. A workbench with a vacuum wafer chuck and probe needles was used in conjunction with a Hewlett Packard 4156A™ Precision Semiconductor Parameter Analyzer. The wafer is held in place on the chuck with the use of vacuum slots and holes. Electrical contact was from the test system to the bond pads of the test structure using Karl Suss™ adjustable probe needles. Several identical structures located in different die were

then stressed with varying amounts of current. A 4-point resistance measurement was made at the different current levels in order to determine the joule heating of the structure at specific stressing currents.

Chapter 3: Characterization of Test Structures

The design and creation of the electromigration test structures is a critical part of the experimental work of this study. The design and lay-out of the test structures will determine the type of specific behavior measured by testing them, and so it is important to understand the test structure design in order to have a basis of understanding the EM results obtained from them. Just as it is important to understand the design of test structures it is also important to understand the processes and process integration that are responsible for creating the test structures. The following sections will describe both the processing and design of the test structures used in this study.

3.1 INTERCONNECT PROCESSING

Modern semiconductor logic devices can contain as many as seven levels of interconnects. Each level of these Cu interconnects is made with complex processes that involve many steps as well as many different materials. The overall integration of these processes results in complex interactions between processes. These interactions will have a significant impact on the reliability of interconnects. The following section, the processing of the test structures used in this work will be surveyed. A description of the Cu damascene process and how it differs from Al interconnects will be given. The differences in the processing

of dual- and single-inlaid interconnects will be examined as well as the different approaches to making dual-inlaid interconnects.

3.1.1 Damascene Process

The damascene process differs from Al metallization processing in the order in which the metal and dielectric are deposited. Al interconnects are made by depositing the metal first and then patterning it and finally be depositing the dielectric. Figure 3.1 depicts the process steps for Cu metallization in which the dielectric material is deposited first. Cu metallization also differs from Al metallization in that Cu does not create a stable passivating layer like Al. In order to protect the devices from damage by the diffusion of Cu, the trenches formed in the dielectric layer must be coated with a diffusion barrier. This diffusion barrier material must both provide a seal in which Cu cannot migrate into the interlevel dielectric (ILD) and a surface to which the Cu seed can be deposited. The barrier material used in this study was Ta, as it provided the best process characteristics while meeting the requirements above. After the diffusion barrier is deposited a thin Cu seed is deposited by PVD. This seed layer provides a preferred surface to which Cu can be plated using an electrolysis method. The trench is then filled with Cu by this electroplating process. Once the Cu trench and/or via is filled, the excess Cu must be removed with a chemical-mechanical polishing (CMP) technique. Once the newly formed interconnect level is planarized by CMP, an etch stop layer (ESL) comprised of Si_3N_4 is deposited. The process is then repeated for each interconnect level.

3.1.2 Dual Inlaid and Single Inlaid Vias

Two types of the damascene process were used, Single-Inlaid and Dual inlaid. The basic elements of the process as described above do not differ much from single-inlaid to dual-inlaid. The difference is that in the dual-inlaid process the Via and trench above are created with a single barrier deposition and Cu fill process. In Figure 3.1 the single-inlaid process is outlined and for comparisons sake the outline of the dual-inlaid process is shown in Figure 3.2 Figure 3.3a depicts the resultant line and via structure from single and dual inlaid processes. In the single inlaid process, an encapsulated via is created that is resistant to EM damage formation. In the dual inlaid process the via is open to the trench above, and therefore susceptible to EM damage. In Figure 3.3b we can see a schematic view of a V1M1 and V1M2 interface resulting from a dual-inlaid process. In the V1M1 structure there is typically a single mode of EM failure but in the V1M2 structure multiple-modes of failure exist. In a single-inlaid V1M2 structure voiding in the vias is prevented leading to a single mode of failure. In Figures 3.4a and 3.4b focused ion beam (FIB) images of the actual single-inlaid and dual-inlaid interfaces are shown.

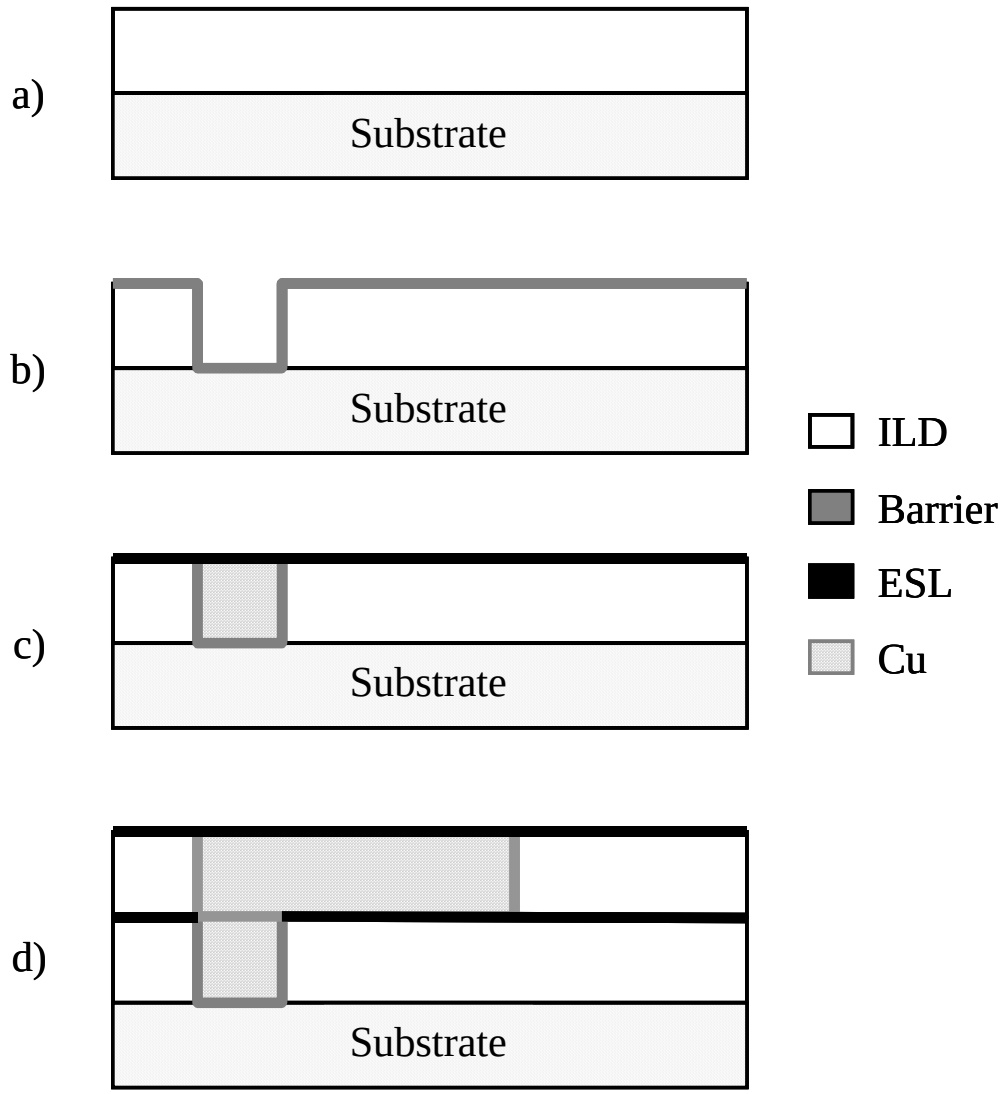


Figure 3.1: A schematic summarizing the major aspects of the single-inlay process. (a) The first interlevel dielectric (ILD) layer is deposited on the substrate. (b) The via is etched and the barrier and seed are deposited. (c) Cu is electroplated to fill the via and the etch stop layer (ESL) is deposited. (d) The process is repeated for the metal level above.

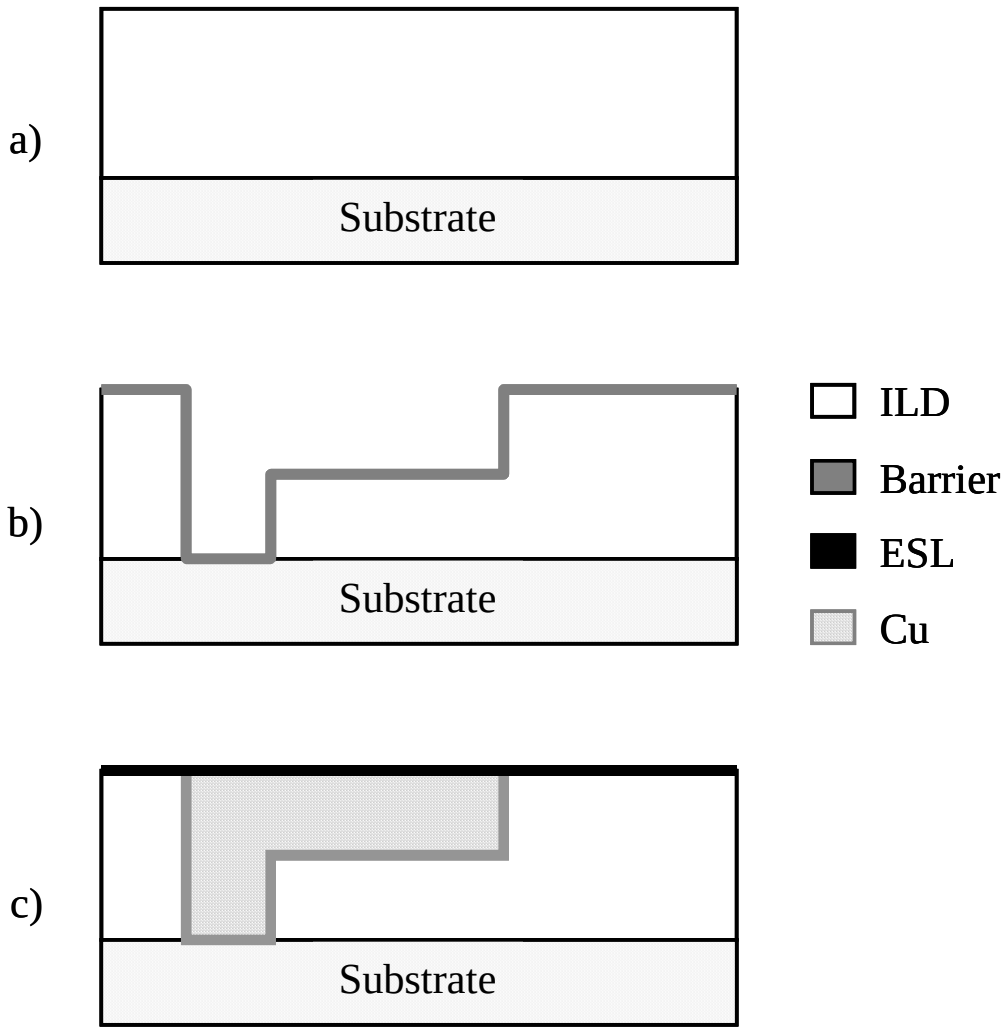


Figure 3.2: A schematic summarizing the major aspects of the dual-inlay process. (a) A thick interlevel dielectric (ILD) layer is deposited on the substrate. (b) The via and trench are etched suing either via-first-trench-last (VFTL) or trench-first-via-last (TFVL) and the barrier and seed layers are deposited (c) Cu is electroplated to fill both the via and trench and the etch stop layer (ESL) is deposited.

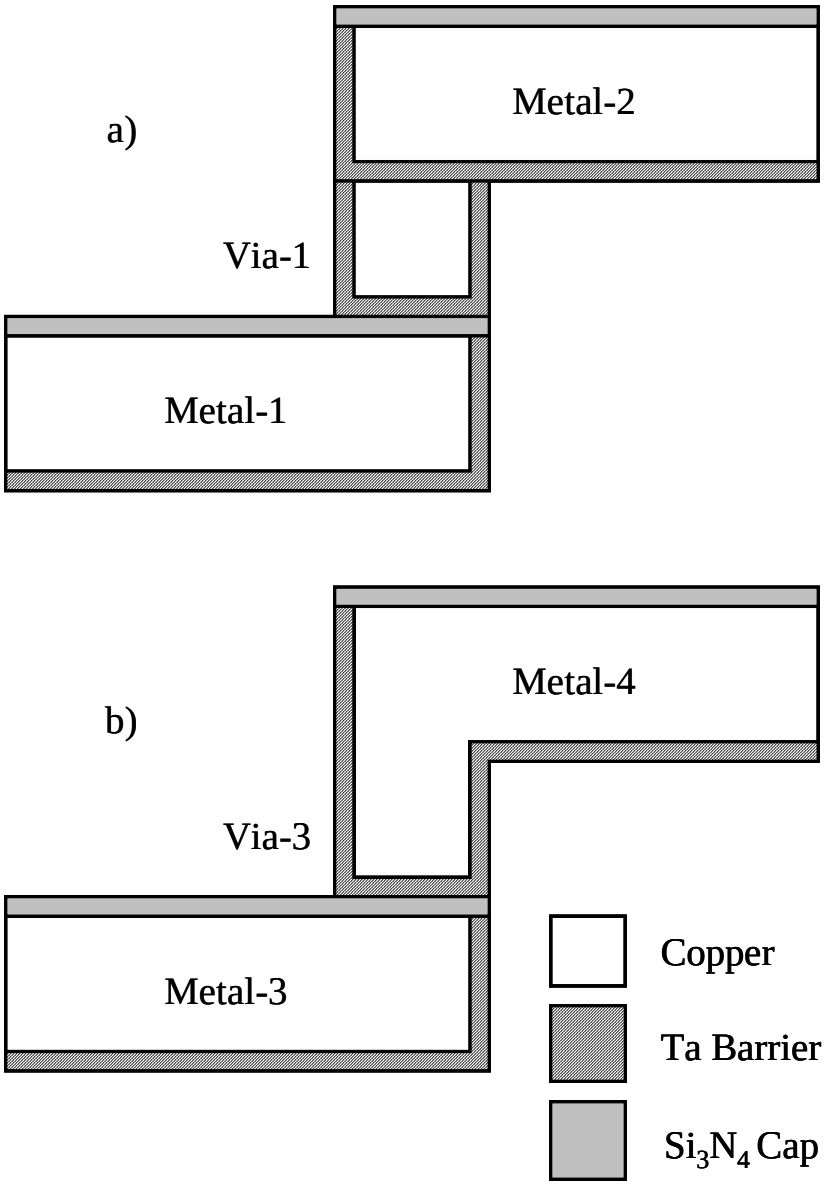


Figure 3.3: (a) A schematic depicting the resultant via structures from a single-inlaid processes. In the single-inlaid case the via and metal line are separated by the Ta barrier. (b) A schematic depicting the resultant via structure from a dual-inlaid process. In the dual inlaid case the metal of the via is continuous with the metal in the line.

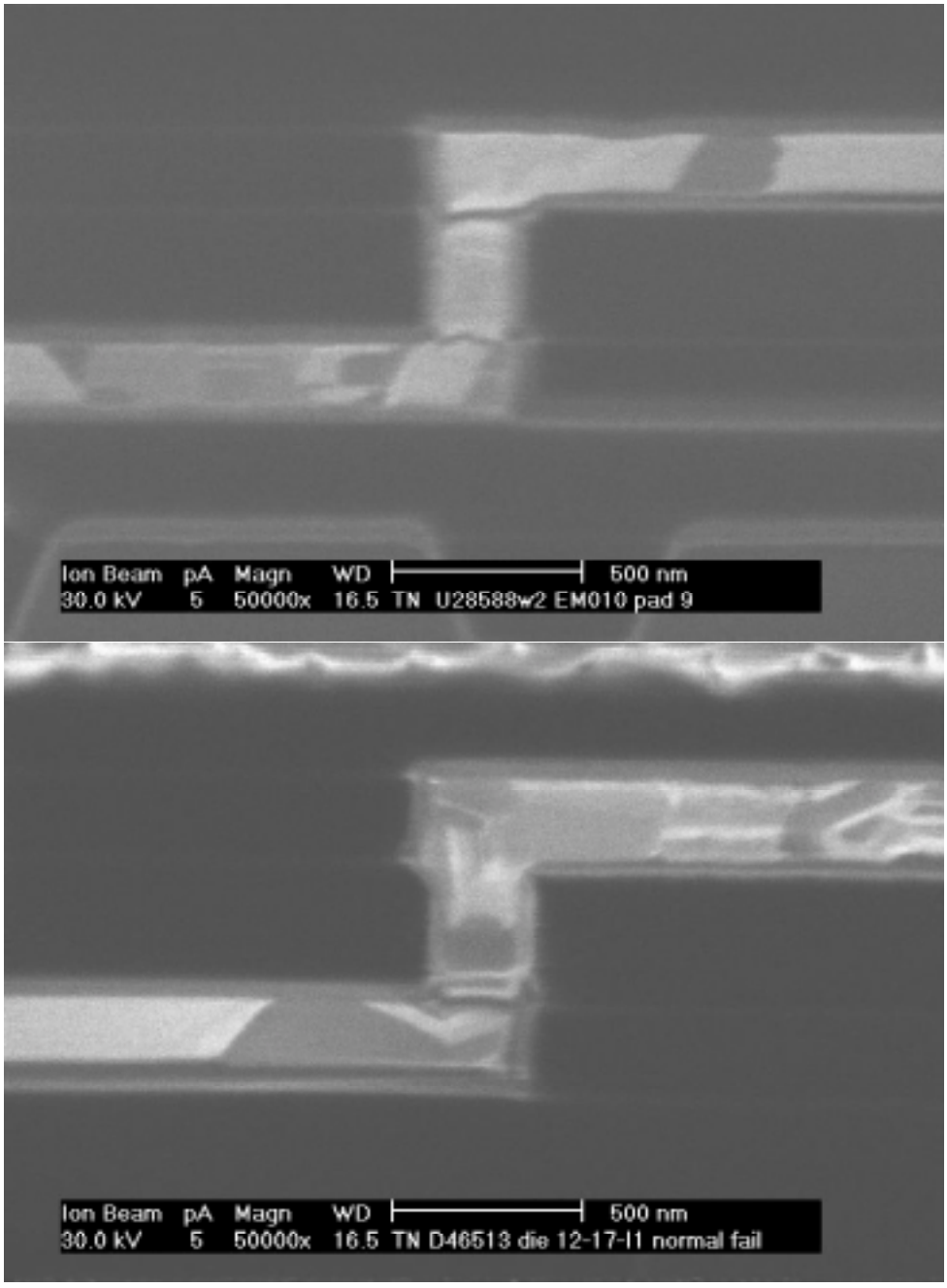


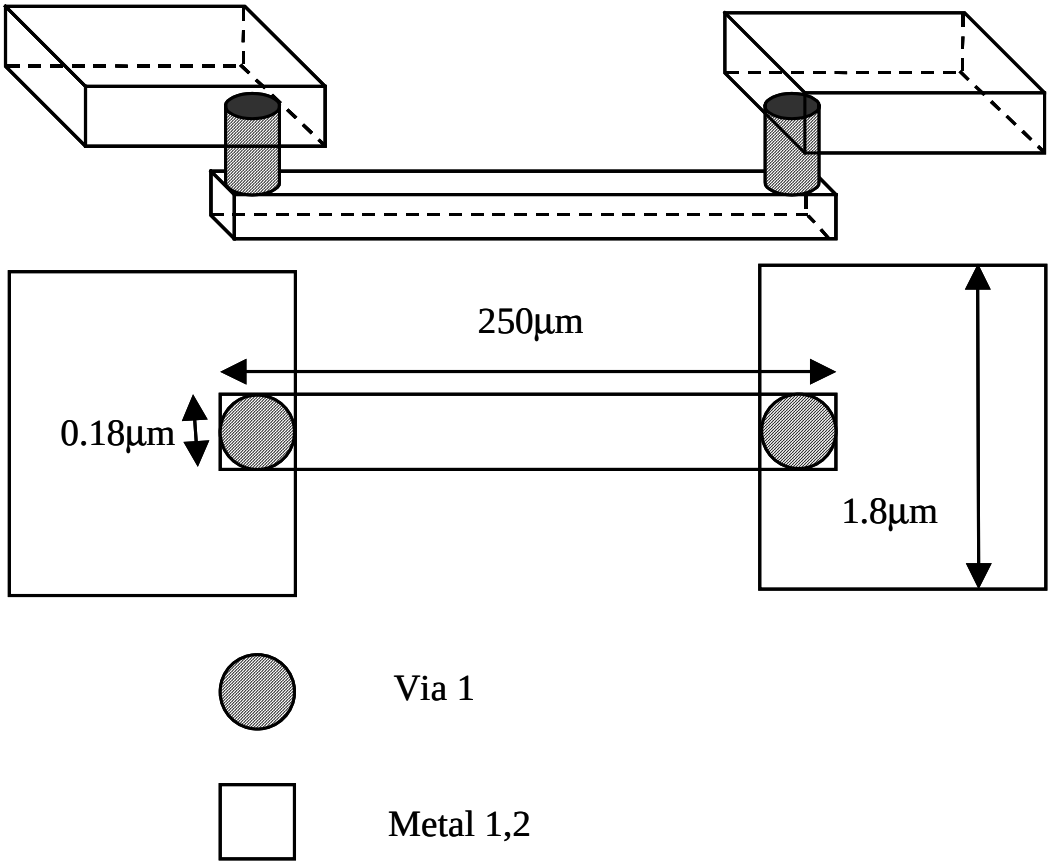
Figure 3.4: (a) An FIB micrograph of single-inlaid metal-via-metal stack. The via is completely encased in the barrier. (b) An FIB micrograph of dual-inlaid metal-via-metal stack. The via is continuous with the metal line.

3.1.3 Via-First Trench-Last Process Integration

The interconnects used in this study were made by a Via-First-Trench-Last (VFTL) DI process. In (VFTL) integration the via is etched first and then filled with a removable slug. Then the trench is formed and the slug removed. In the Trench-First-Via-Last (TFVL) process the trench is formed first and then a very large aspect ration via is etched. The differences between the two process integrations is not examined as part of this study.

3.2 TEST STRUCTURE DESIGN

The design and creation of the electromigration test structures is a critical part of the experimental work of this study. The design and lay-out of the test structures will determine the type of behavior measured by testing them, and so it is important to understand the test structure design in order to have a basis of understanding the EM results obtained from them. The test structures used in this study, although different in many ways, adhere to a set of design rules which govern the layout of interconnects depending on the level in which they reside. In Figure 3.5 and 3.6 the layout of the basic V1M1 and V1M2 EM test structures are shown. In Figure 3.7 the layout of the Dual-inlaid EM test structure at the V3M4 interface is shown. The line width of 0.18μm is particular to the Metal 1 and Metal 2 levels. In Table 3.1 the particular line width and via dimensions are shown for the various metal levels used in this study. The following sections will describe the design of the varying types of test structures used in this study.



Via 1

Metal 1,2

Figure 3.5: A schematic of the basic V1M1 EM test structure used in this study. The Metal line is terminated in vias at either end that connect to wider supply lines. These supply lines are routed to the wire bond pads. The dimensions shown are those of the Metal 1 or Metal 2 interconnect levels.

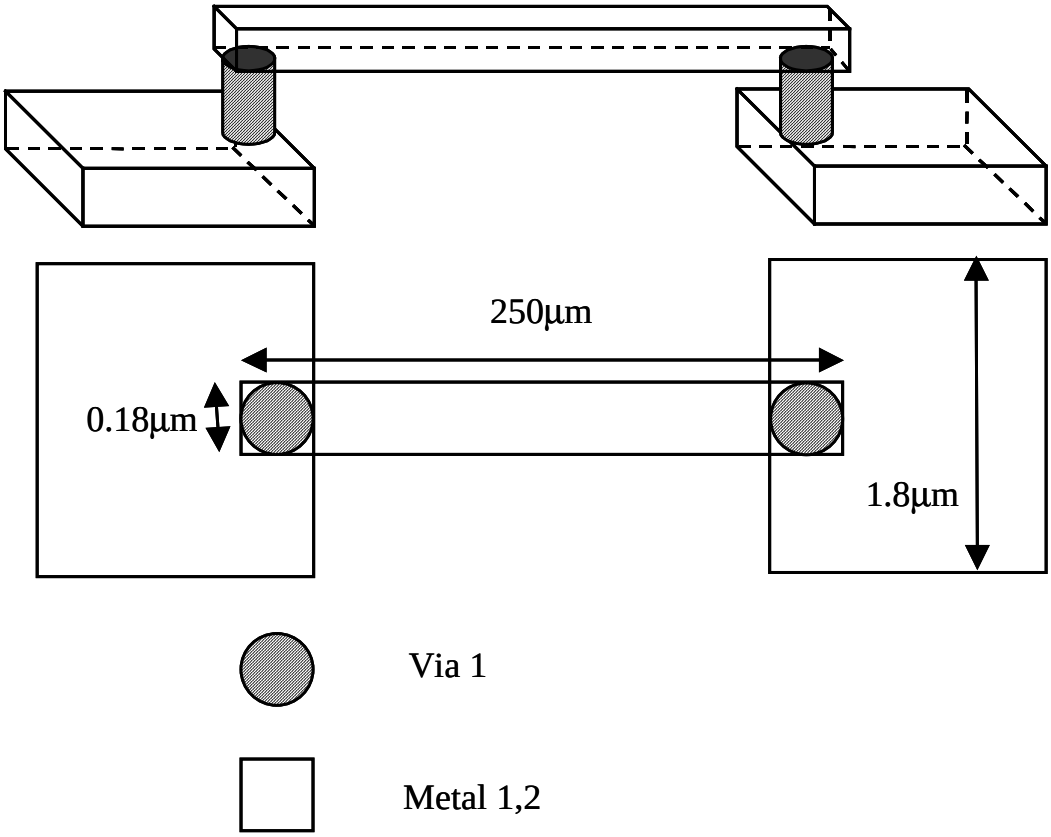


Figure 3.6: A schematic of the basic V1M2 EM test structure used in this study. The Metal line is terminated in vias at either end that connect to wider supply lines. These supply lines are routed to the wire bond pads. The dimensions shown are those of the Metal 1 or Metal 2 interconnect levels.

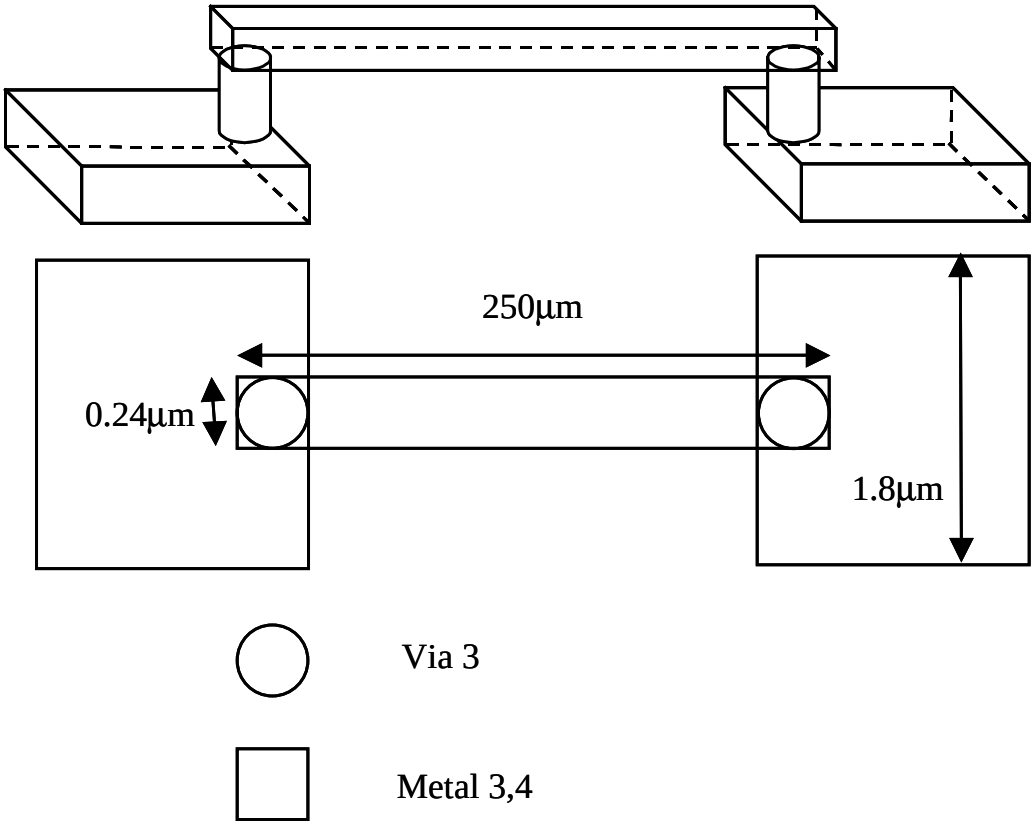


Figure 3.7: A schematic of the basic V3M4 EM test structure used in this study. The Metal line is terminated in vias at either end that connect to wider supply lines. These supply lines are routed to the wire bond pads. These structures were used to examine the EM behavior of the Dual-inlaid process.

Table 3.1: Minimum metal line widths and via diameters in microns for the various interconnect levels used in this study.

Metal Level / Via	Width/Diameter (μm)	Spacing (μm)	Pitch (μm)
Metal-1	0.18	0.18	0.36
Via-1	0.18	0.18	0.36
Metal-2	0.18	0.18	0.36
Metal-3	0.24	0.24	0.48
Via-2	0.24	0.24	0.48
Metal-4	0.24	0.24	0.48

Figures 3.8 and 3.9 depict the two types of multi-link structures designed to test both sides of the Via – Metal interface. The two interfaces are named V1M1, in which the electron flow is down through the via and into the metal line below, and V1M2, in which the current flows up into the metal line above. (V3M3 and V3M4 in the case of the Dual Inlaid structures). The varying width structures make use of both interfaces just as the basic EM structures. The other studies in this work will make use of only one interface.

3.2.1 Multi-Link Structures

The multi-link test structures used in this study are made up of chains of metal line segments connected with vias. The chain segments are made up of long-narrow and short-wide segments. The short-wide segments are designed to be EM resistant and act to link the long metal chains in series. The long metal segments are the failure elements and these will be located on Metal-1 for the

V1M1 structures and Metal-2 for the V1M2 structures. In Figure 3.8 the basic layout of a V1M1 multi-link structure can be seen and in Figure 3.9 the layout of the 1-link and 10-link V1M2 structures is shown.

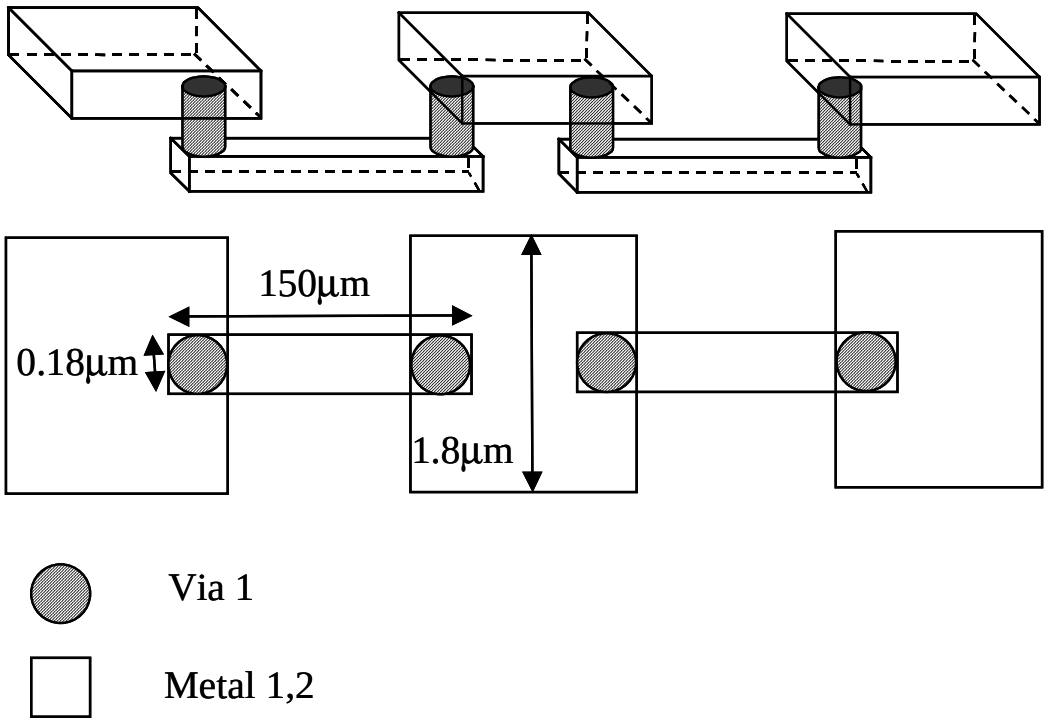


Figure 3.8: A schematic depicting the 2 of the serial links of the 10 or 100-link V1M1 structures. The Metal-2 segments are kept short and wide to insure EM damage occurs in the Metal 1 line segments, which are 150µm long.

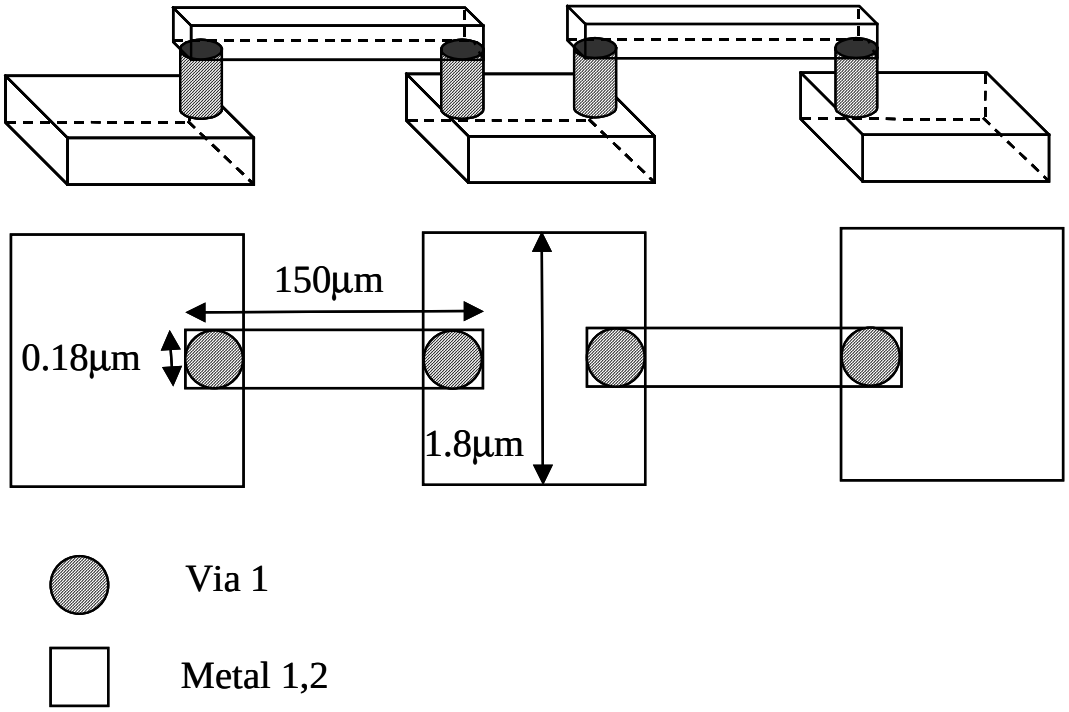


Figure 3.9: A schematic depicting the 2 of the serial links of the 10 or 100-link V1M2 structures. This structure is the same as the previous but with the long, 150µm, segments on Metal-2.

Structures containing 1, 10 and 100 failure elements were used in this study. The number of failure elements was limited to a maximum of 100 due to the voltage compliance limits of the EM test system. In addition the length of the metal links is 150µm compared to 250µm used for the basic EM test structures. The reason for the shorter length is to keep the electrical resistance of the structure down so that the compliance limits of the test system would not be exceeded. The purpose of the multi-link structures is to allow for the testing of a large number of interconnect segments. By testing a large number of interconnects one gains statistical sensitivity, which improves the lifetime

extrapolation and is needed to detect secondary or extrinsic failure modes. The structures are designed to detect the lifetime of the first element to fail. The structures are in a serial arrangement so that the entire structure will fail when the first interconnect segment fails.

The multi-link structures were used to examine EM on both SI and DI integrations. The same basic design of the multi-link test structures was used for both the single inlaid integration as well as the dual inlaid integration. While the overall design of these two test structures is similar they differ in their dimensions as well as their physical location in the stacking sequence. The SI test structures are located on the Metal-1, Via-1, and Metal-2 layers, and have dimensions consistent with the design rules for those layers. As can be seen in Table 3.1, the pitch of the SI multi-link structures is 0.36μm and the length of each segment is 150μm. The dual inlaid test structures are located on the Metal-3, Via-3, and Metal-4 layers, and have a pitch of 0.48μm and a length of 150μm.

3.2.2 Varying Width Structures

Structures of varying width were created to measure the impact of scaling the dimensions on the EM failure mechanism. Wide interconnects have both more interface area as well as a different Cu microstructure, both of which will likely affect EM performance. The varying width test structures consist of 8 specific structures. Four of the structures are at the V1M1 interface while the remaining four are at the V1M2 interface. Both interfaces were examined because it is anticipated that the EM behavior of the two interfaces will behave

differently when different line widths are used. As can be seen in Figure 3.10, these structures consist of 1x, 2x, and 3x wide varieties. These three structures are connected to the bond pad through a single via. A fourth structure, which contains a 3x wide metal line as well as 2 connection vias, was designed to measure the impact of multiple vias.

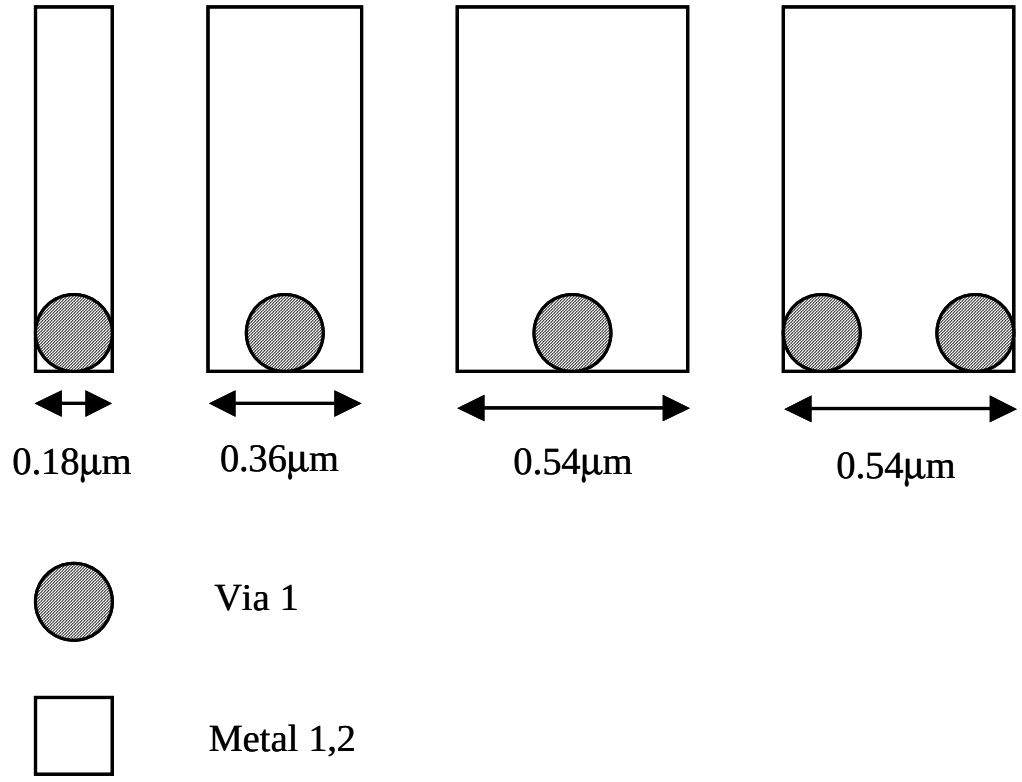


Figure 3.10: (a) A schematic depicting the varying line width structures. The width ranges from 0.18 to 0.54 microns. The widest structure also has 2 versions, one containing a single via, and another terminating in two vias.

3.2.3 Varying Length Structures

The last type of test structure to be described here are the varying length, or critical length structures as they are sometimes called. The purpose of these structures is to determine the critical length – current density product as described in section 1B. Interconnects that are shorter then this critical length are immune to EM failure and are therefore important in chip design. By measuring the lifetimes of these structures it is possible to calculate the JLc product. These structures, much like the varying width structures described above, contain failure elements of varying dimensions connected to pads through single vias. In this case the length of the structures is varied while the width is kept constant. 6 types of structures, with lengths of 5, 10, 20, 50, 100, and 250μm were designed in order to determine the critical length with varying process and test conditions. All of the structures are based on a 0.18μm wide Contact - Metal-1 (CaM1) test structure. The contacts are made of Tungsten (W) plugs. Figure 3.11 shows the basic layout of the CaM1 test structure.

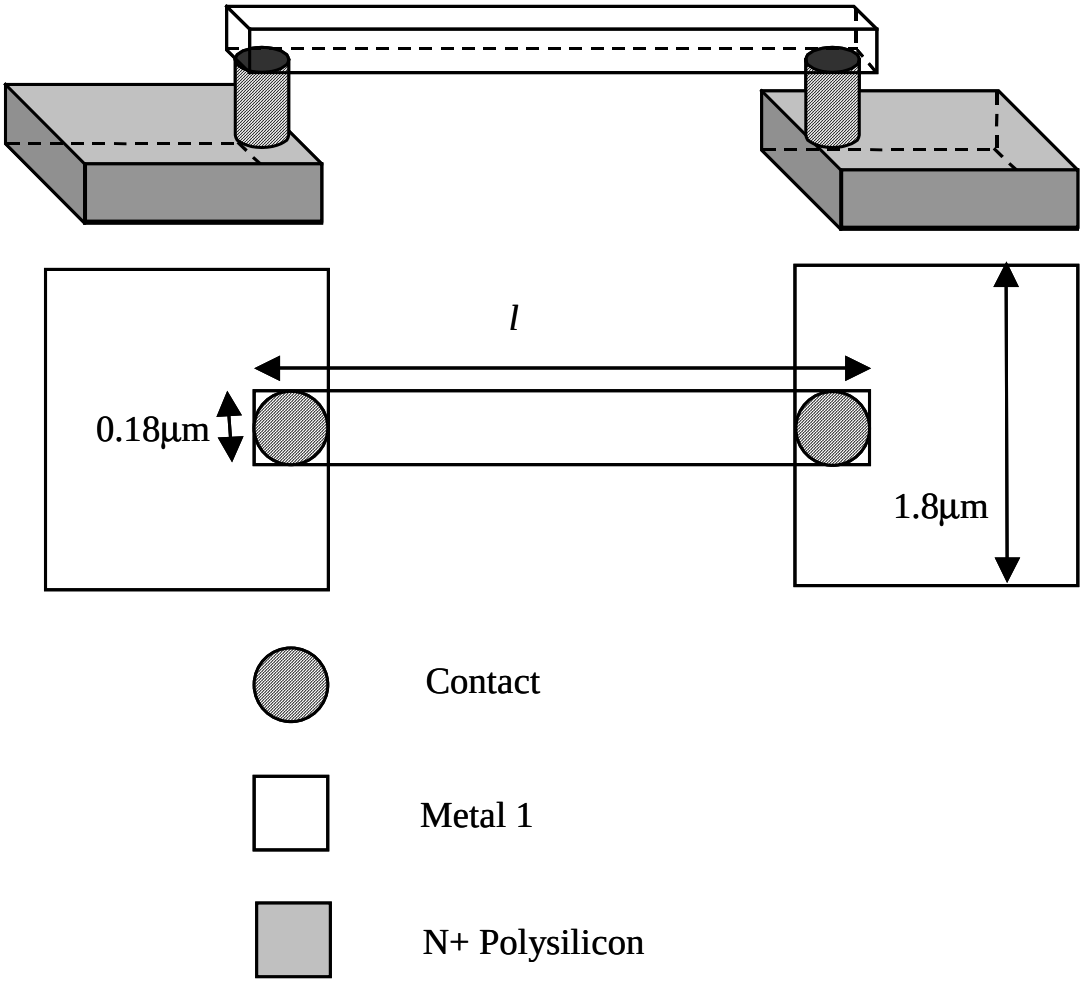


Figure 3.11: a) A schematic showing the layout of the CaM1 varying length tests structures. The current is supplied from a polysilicon region through a contact and into the metal line.

3.3 GRAIN SIZE CHARACTERIZATION

The influence of the grain size on the EM behavior of Cu interconnects has long been a topic of study. In the previous generations of Al(Cu) interconnects grain boundaries were found to be a significant contributor to Cu migration. The larger the grains were, the more bamboo-like the grain structure would become, and the fewer grain boundaries would contribute to Cu migration. With the introduction of Cu interconnect technology, the role of grain size in EM induced Cu migration has once again become a prime topic of study. Many researchers have found that the contribution of grain boundaries to the mass flux in Cu interconnects is not as significant as it was in Al(Cu) interconnects. The critical diffusion pathway has repeatedly shown to be the top interface between the Cu metal and the nitride etch stop layer (ESL) [7, 8, 12-16]. So in this way the grain size of the interconnects was not expected to impact the EM performance of the Cu interconnects. However, it is still important to characterize the grain size distribution so that the void formation mechanisms can be better understood.

The size of discreet Cu grains was determined by the TEM imaging of plan-view interconnect structures as described in Chapter 2. In Figure 3.12 an example of a zero-tilt TEM image taken at 40,000x magnification is shown. In this figure several parallel Cu interconnect lines can be seen. The lines are 0.18μm wide and extend well out of the imaging area. Grain boundaries, twins, and the Ta diffusion barrier can clearly be seen in this image. Figure 3.13 shows a similar TEM image at 50,000x magnification.

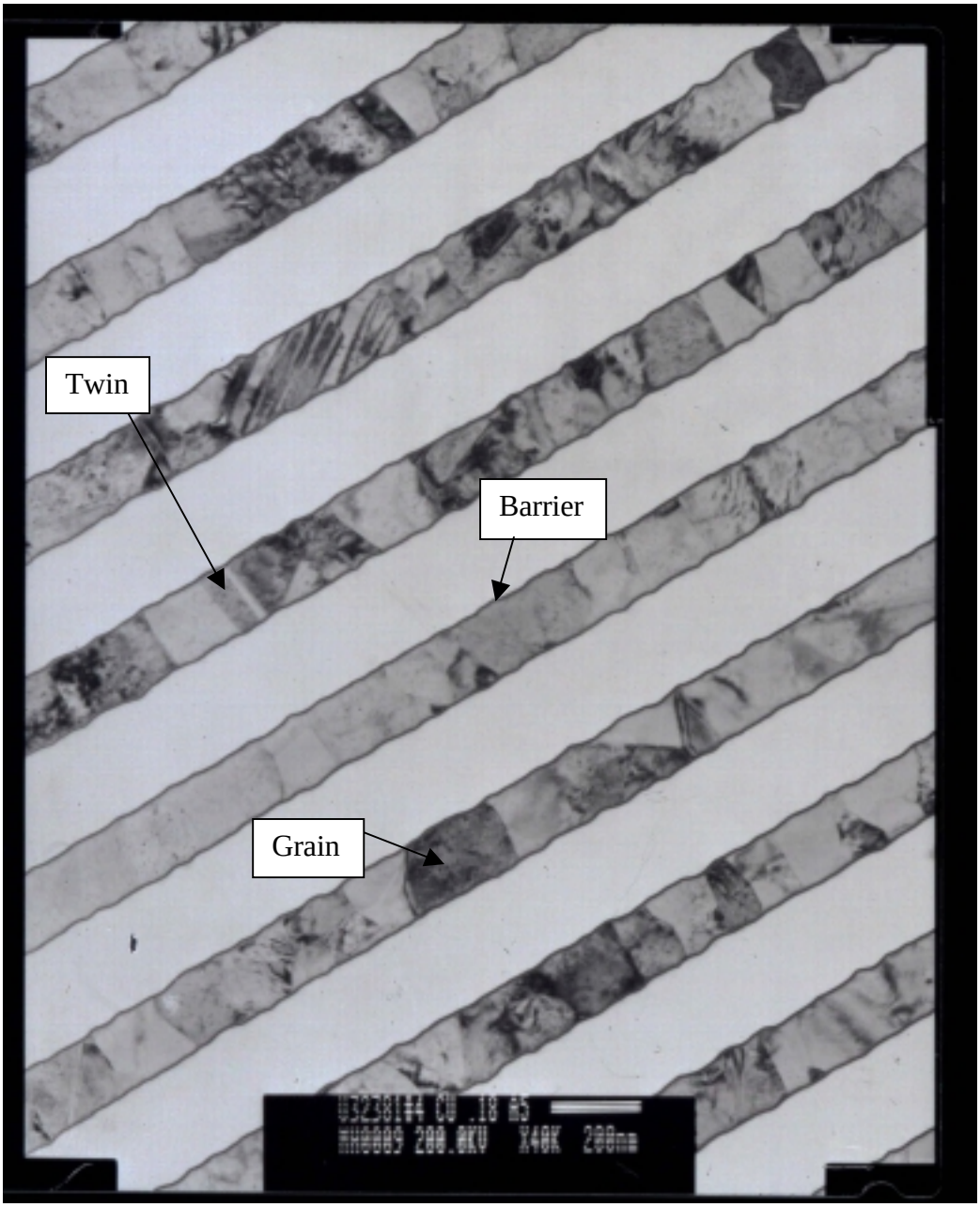


Figure 3.12: A plan-view TEM image showing the grain structure of several parallel Cu interconnect lines at 40,000x magnification.

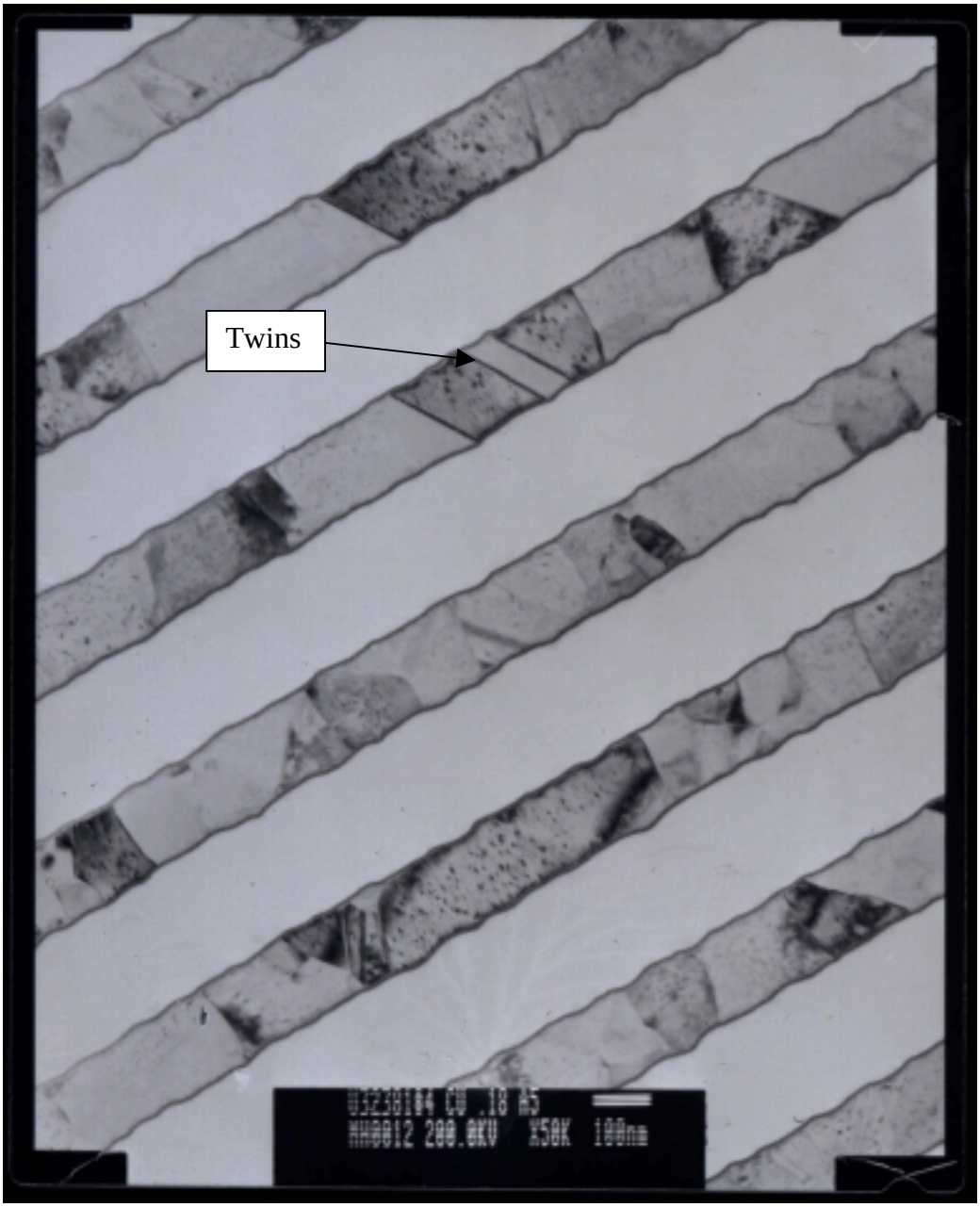


Figure 3.13: Another plan-view TEM image showing the grain structure of several parallel Cu interconnect lines at 50,000x magnification. Two pairs of twin boundaries can clearly be seen in the third line from the top.

A total of 283 discreet grains were identified and measured using the images shown above. The resulting grain size distribution is shown in Figure 3.14. The mean grain size was found to be approximatly 0.15μm with a lognormal sigma of 0.38. The mean grain size is below the line width, 0.18μm, but is close enough to suggest the presence of some bamboo like grains like the one indicated in Figure 3.12. The grain size distribution shown in Figure 3.14 is fit with a lognormal line. By comparing the data to the fitting line the kink in the grain size distribution at the 50^{th} percentile can be seen. This kink in the distribution occurs at a grain size of 018μm.

The bend in the distribution is result of the maximum grain size limit in the perpendicular direction imposed by the width of the interconnect line. While the grains are not limited in their size in the direction of the interconnects there is a maximum limit to their size in the perpendicular direction. The result of the line width on the grain size distribution is to shift the distribution to the left at grain sizes above the 0.18μm limit, resulting in a bimodal distribution.

The other important result from the grain size analysis, is that the grain structure has been shown to be not entirely bamboo like. A typical interconnect line resulting from this process will likely contain mostly sub-line-width grains with a few grains spanning the entire width. As a result, EM-induced void formation in the cathode end of the interconnect structures is likely to occur in region containing many smaller grains, which will result in a more uniform void formation process.

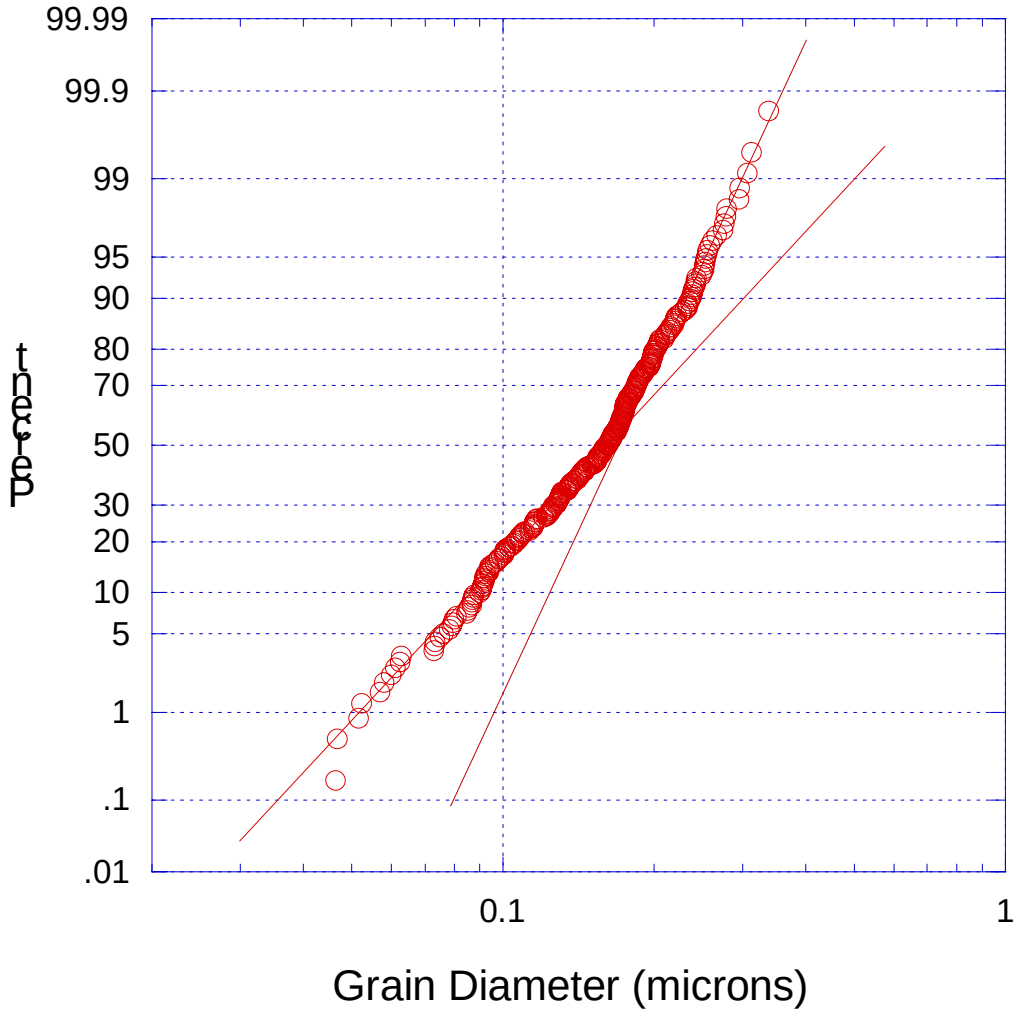


Figure 3.14: A lognormal plot of the grain diameters as determined from the TEM images above. A good lognormal fit is seen with a slight kink in the distribution at 0.18μm.

3.4 JOULE HEATING CHARACTERIZATION

Joule heating caused by the higher current density in interconnects can significantly accelerate EM by increasing the temperature of structure [6]. The amount of joule heating present in the sample can be calculated by first determining α, the coefficient of thermal resistivity of the test structure. The resistance of the test structure can be written as a function of the temperature as in Equation 3.1.

$$R = R_o(1 + \alpha\Delta T) \tag{3.1}$$

Secondly, resistance of the structure as a function of applied current must be measured. This was done using wafer level tests as described in section 2.2.3. The data was collected on 8 different V1M1 and V1M2 structures. Three different line width structures from each interface were used. In addition, a variant of the 3x wide structure with two vias was used in order to determine the effect of via count. From these two tests, the change in temperature as a result of increased current density could be determined. In Figure 3.15, the results from the V1M1 samples show that the wider structures have higher joule heating. The effect of the second via in the 3x wide structures is negligible. In Figure 3.16 the V1M2 data shows the same trends as the V1M1 structures. However, the amount of joule heating at the EM test condition, 1.5 MA/cm^2, is small so that the difference in Joule heating is negligible. In Table 3.2 the change in temperature for the various structures is shown for a current density of 1.5MA/cm^2.

Table 3.2 The change in temperature, ΔT, for all structures stressed with a current density of $1.5MA/cm^2$

Interface	1x (0.18μm)	2x (0.36μm)	3x (0.54μm)	3x (w. 2 vias)
ΔT_{V1M1} (^oC)	0.1	0.4	0.5	0.5
ΔT_{V1M2} (^oC)	0.1	0.5	0.5	0.4

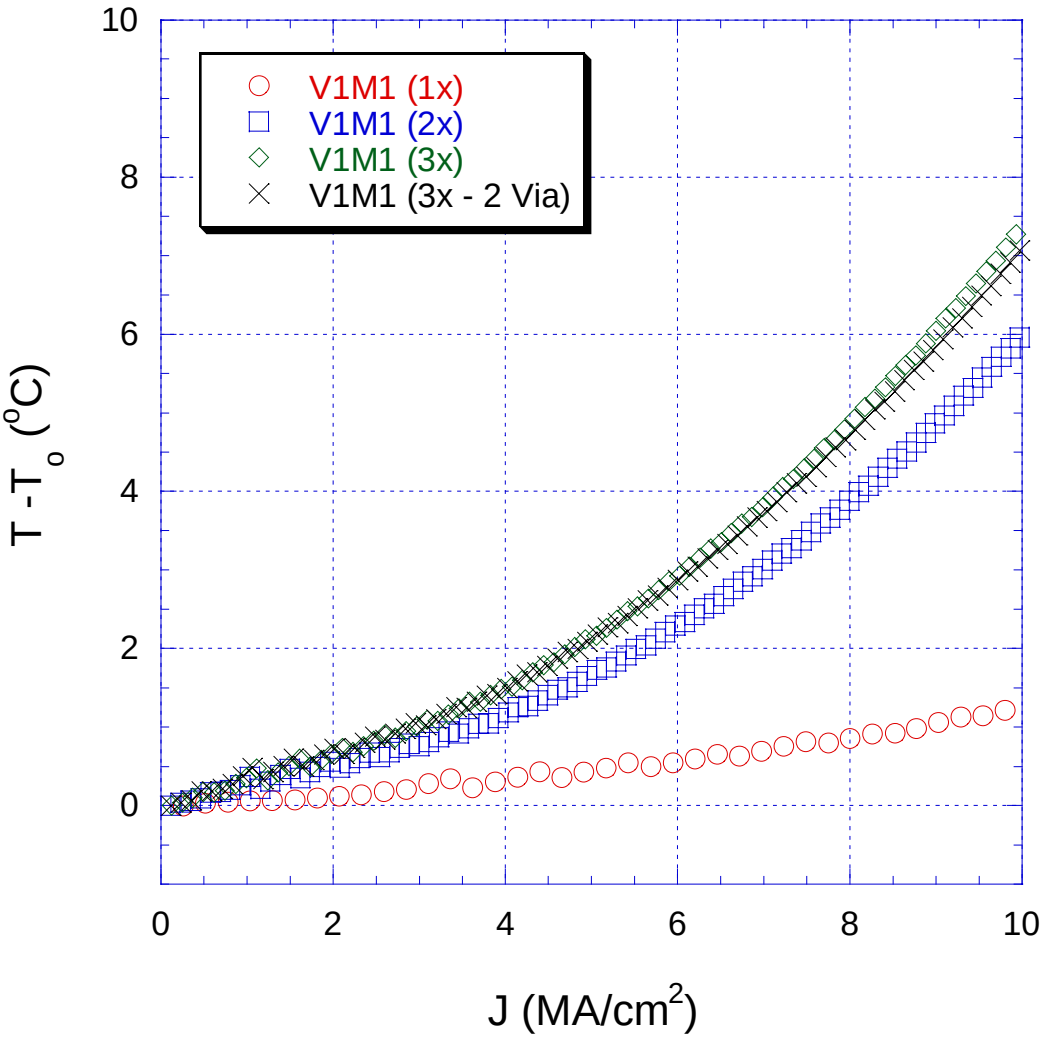


Figure 3.15: The change in temperature of varying line width V1M1 structures as a function of current density. The 2x and 3x have higher joule heating for a fixed current density, but at the testing current, 1.5MA/cm^2 the difference is negligible.

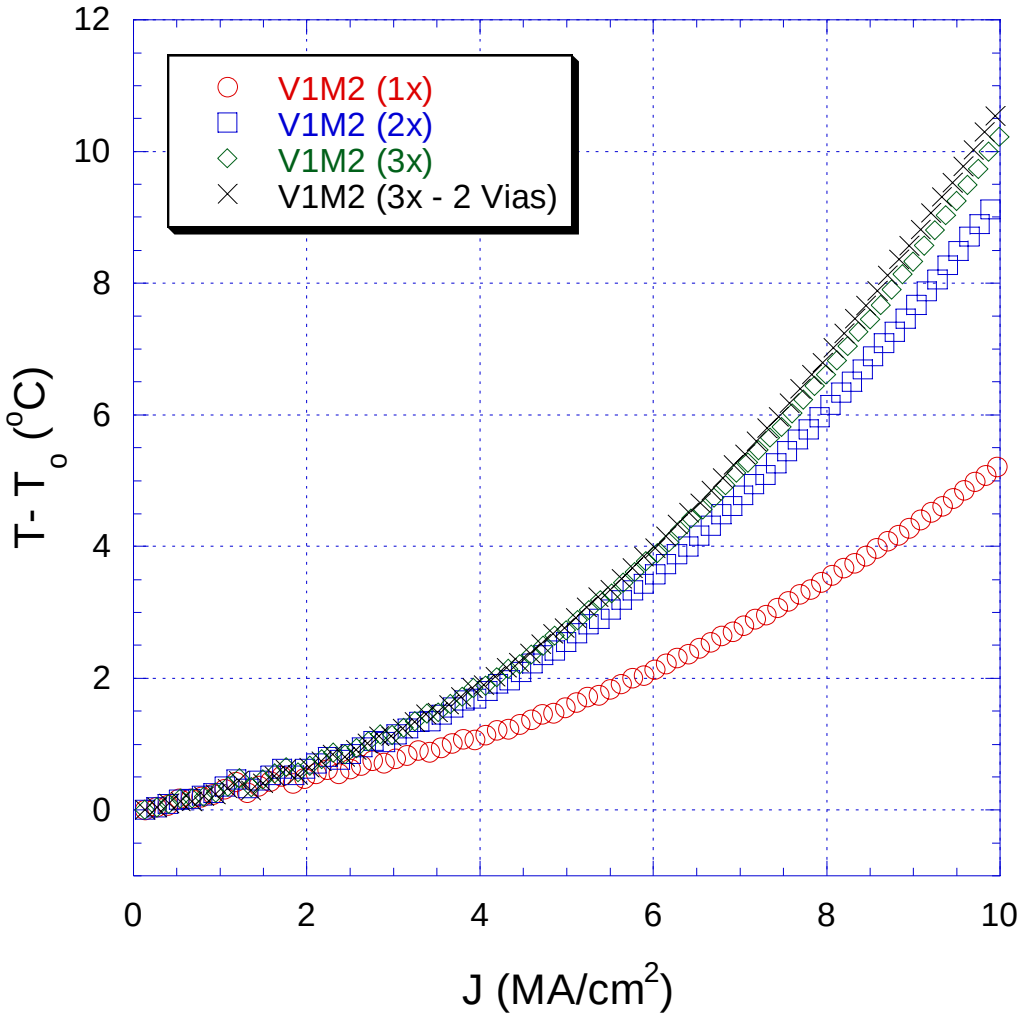


Figure 3.16: The change in temperature of varying line width V1M2 structures as a function of current density. These structures exhibit the same behavior as the V1M1 structures.

Chapter 4: Fundamental EM Phenomena in Cu Interconnects

An understanding of the fundamental mechanisms responsible for EM in interconnects forms the basis for accurate determinations of reliability of actual devices. In this way the basic EM behavior of a single interconnect structure needs to be studied so that more complicated tests can be interpreted correctly. The diffusion pathways responsible for the flux of Cu ions, the positions of barriers and the morphologies of fatal voids are all important factors in determining when a interconnect will fail under EM. The drift velocity of Cu ions under electromigration can be expressed as

$$v_d = D_{eff} Z_s^* e \rho j / kT \tag{4.1}$$

where the terms have the same meanings as in Equation 1.10. It is possible to refine the effective diffusivity, D_{eff} by assuming that the dislocation and bulk diffusion do not play a role in Cu interconnects. Several researchers, including C.-K. Hu et. al. [7] and E. T. Ogawa et. al. [8], have found that the grain boundary diffusion is also secondary to the interfacial or surface diffusion [7-9]. So by elimination all of these terms, the effective diffusivity of a Cu interconnect can be expressed as

$$D_{eff} = D_i \left[2\delta_i \left(\frac{1}{w} + \frac{1}{h} \right) \right] \tag{4.2}$$

where D_i is the interfacial diffusion. This construction is not strictly correct as the diffusivities of the Cu / Ta interface are likely different then that of the Cu / PEN interface. Further refinement of this transport equation will be reserved for a later section.

The net flux of Cu atoms from anode to cathode will cause voiding to occur at the anode of the interconnect. A schematic of a voided V1M1 and V1M2 structure showing the void length terms is depicted in Figure 4.1. In single-inlaid interconnects, in which the via is not susceptible to EM damage, the void must grow past the via in order to cause failure. The void must go past a length of l_o in order to have a detectable impact on the resistance. The length in which the void grows past the via determines the amount of resistance increase as described in Equation 4.3 as

$$\Delta R \propto \Delta l_v \tag{4.3}$$

where Δl_v is the void distance past the via. By normalizing the terms by the line length and resistance and expanding the equation it is possible to write the following expression

$$\left(\Delta R / R\right) = K_{eff}\left(\Delta l_v / l\right) \tag{4.4}$$

where K_{eff} is constant based on the resistivity of the Cu metal and Ta barrier. If the sidewalls and bottom barrier are assumed to contribute to electrical conduction, K_{eff} can be written as

$$K_{eff} = (\rho_B h) \Big/ (\rho_{Cu} t_B (2h/w + 1)) \tag{4.5}$$

in which ρ_B is the resistivity of the barrier, ρ_{Cu} is the resistivity of the Cu metal, t_B is the thickness of the barrier and h and w are the height and width of the interconnect. If only the bottom of the barrier is assumed to contribute to electrical conduction then K_{eff} can be simplified and written as

$$K_{eff} = (\rho_B h) \Big/ (\rho_{Cu} t_B) \tag{4.6}$$

This type of analysis is similar to methods applied to Al(Cu) interconnects by Korhonnen, *et. al* [10]. In Korhonnen's studies the Al line sat atop a shunt layer consisting of TiN. In this study the Cu lines are encased by a thin Ta barrier. The difference in resistivity between the Cu metal and Ta barrier is much greater than that of Al(Cu) and TiN. The result is this is that a Cu void will not need to extend past the via as far in order to cause failure.

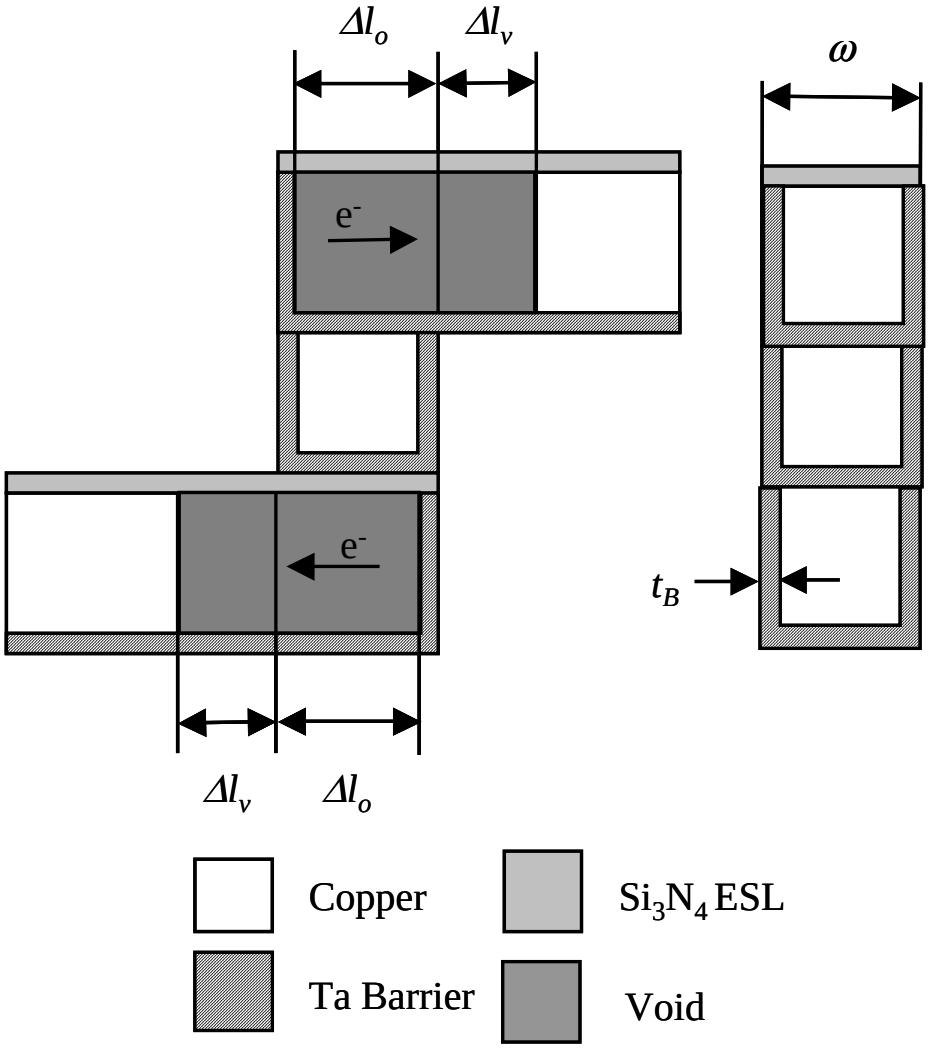


Figure 4.1: A schematic of voided V1M1 a V1M2 interconnects. The terms used in Equation 4.3 – 4.5 are given. Only when a void extends past L_0 does it begin to affect the resistance of the line.

In these tests, the time to 10% resistance increase was used as the failure criteria. It is also important to note that the stressing current is shut off after a 30% increase in resistance is detected. The amount of resistance increase will determine the length of the voids. The 30% resistance current cut-off value is

important because it will determine the size of the voids seen in failure analysis. In Table 4.1 the void length past the via, $\Delta L_{v,}$ as calculated from Equations 4.5 and 4.6 is shown for interconnects of varying length.

Table 4.1 The void length past the via, $\Delta L_{v,}$ as calculated from Equations 4.5 and 4.6. The void size is controlled by the fact that the stressing current is shut off after the structure has reached a 30% resistance increase.

L	ΔL_v from Eq. 4.5 (nm)	ΔL_v from Eq. 4.6 (nm)
`250	313.1	104.4
150	187.9	62.6
50	62.6	20.9
25	31.3	10.4
10	12.5	4.2

4.1 BASIC ELECTROMIGRATION BEHAVIOR

The fundamental EM behavior of single-inlaid interconnects was studied by examining the EM behaviors of both the V1M1 and the V1M2 interface. EM tests were done at a range of temperatures from 250^{o}C to 342^{o}C with a stressing current of 0.67mA. The stressing current used in this section translates to a current density of 1.5MA/cm^2, which is the same used for all of the tests in the following sections. In Table 4.2 a list of the median times to fail (MTTF) at the five different testing temperatures for both of the structure types is presented. The lifetimes of the V1M2 structures are consistently higher then that of the V1M1 structures. The cause of this disparity is result of the location of void formation in

relation to the fast diffusion interface in the different structures. A more detailed description of this effect will be given later in this section when the failure results are discussed.

Table 4.2 The Median Time to Fail (MTTF) in hours for the V1M1 and V1M2 structures at the 5 testing temperatures. The V1M2 structures have nearly twice the lifetime as the V1M1 structures under the same conditions.

Temperature (^{o}C)	V1M1 MTTF (hrs)	V1M2 MTTF (hrs)
342	26.7	46.8
325	45.0	70.4
300	94.0	171.4
269	278.1	478.2
250	630.2	1155

In figures 4.1 and 4.5 the typical resistance traces are shown for the V1M1 and V1M2 structures respectively. In both cases the resistance remains flat until the resistance spikes. A failure criteria of 10% resistance increase was used for these tests because it would make little difference to the data and can be easily automated as part of the Qualitau test system. In Figures 4.2 and 4.6, the failure time distributions for the V1M1 and V1M2 structures are shown at the different test temperatures. The data is fit with a lognormal distribution with upper and lower 90% confidence bounds. Both data sets have a good lognormal fit with a trend of increasing sigma at lower temperatures. This behavior is consistent with

the findings of W. Nelson that conclude that higher stressing conditions tend to lower the sigma of the distribution [11].

The quality of the lognormal fit can also be seen in Figures 4.3 and 4.7 in which the lognormal plots of the standardized residuals for the pooled data are shown. The standardized residuals have been calculated according to a maximum likelihood analysis method used by the Minitab™ software suite. The standardized residuals provide a measure of the deviation from ideal lognormal behavior. The plots show that for both the V1M1 and V1M2 structures the data is fit well by the lognormal trend with only small amounts of deviation towards the bottom of the plots. This data is also bracketed by the 90% confidence bounds just as the failure distribution plots shown before were.

In Figures 4.4 and 4.8 Arrehnius plots of the time to failure (TTF) are show for the V1M1 and V1M2 structures respectively. The individual fail times are shown at each testing temperature and the fitted line runs through the median value. The activation energy described in Blacks' Equation, Eq. 1.10, can be determined by the slope of these lines and is described later in this section. Below the fail time data and the fitted median line is a fitted line based on the first time to fail in 1,000,000 interconnects, or the 0.000001% failure. These fail times are calculated by solving for percentage value of 0.000001% instead of calculating based on a percentage of 50% as is done with the median values. This type of calculation is useful when making a statement about the reliability of a large population based on a smaller sampling of tested parts. It is a way to extrapolate

the EM behavior for number of parts just like the behavior is extrapolated in temperature with accelerated testing.

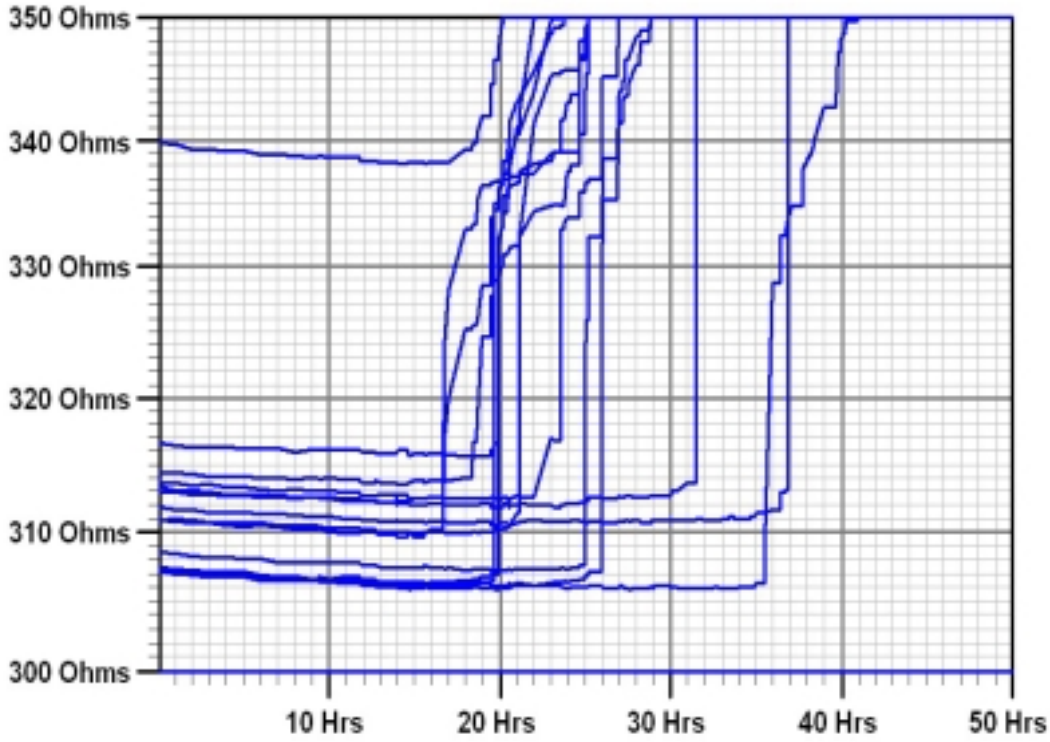


Figure 4.1: Resistance traces of V1M1 structures tested at 342C with 0.67mA stressing current. The resistance remains more or less constant until a sudden jump in resistance causing failure.

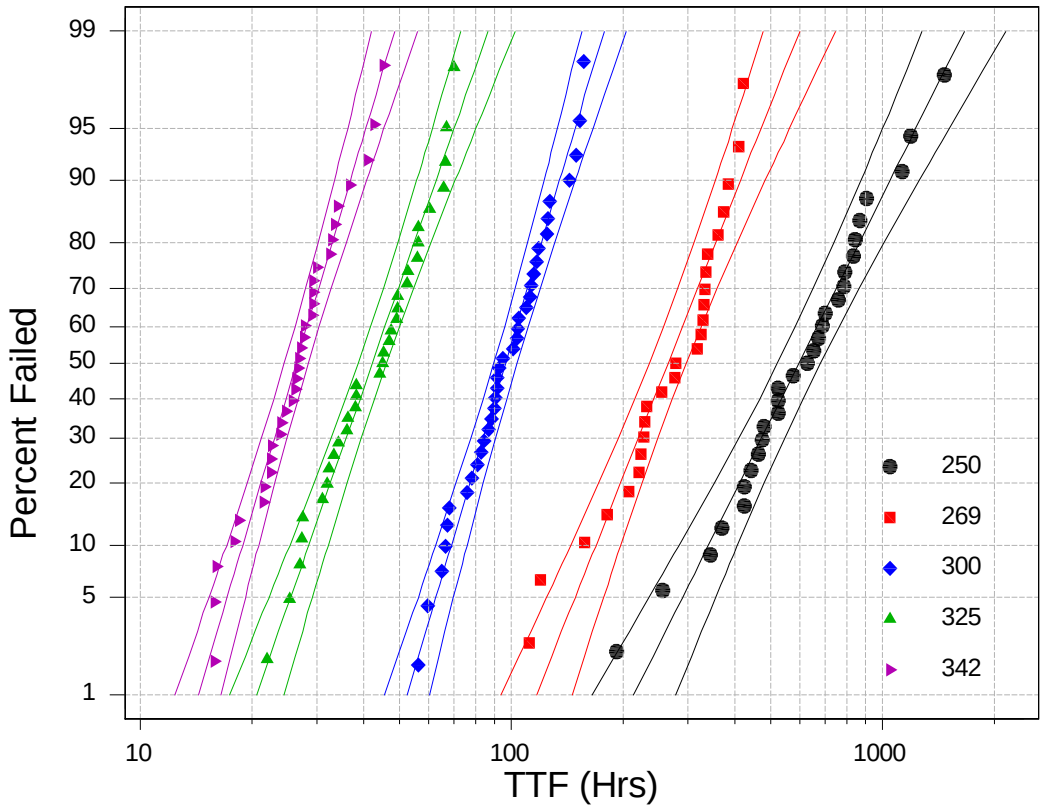


Figure 4.2: Failure distributions of the V1M1 structures tested in a range of temperatures from 250 to 342C. The distributions are fitted and bounded by 90% confidence intervals.

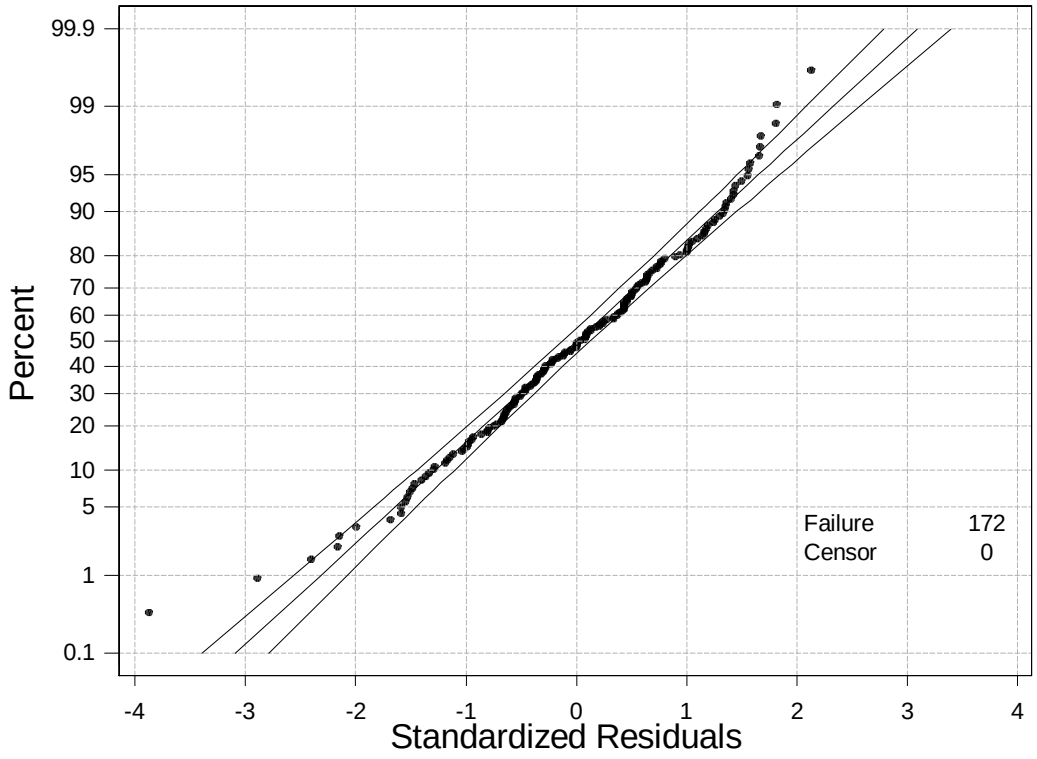


Figure 4.3: A plot of the distribution standardized residuals for the lognormal fit of the V1M1 structures tested in a range of temperatures from 250 to 342C. The plot indicates that the lognormal distribution fits the data well.

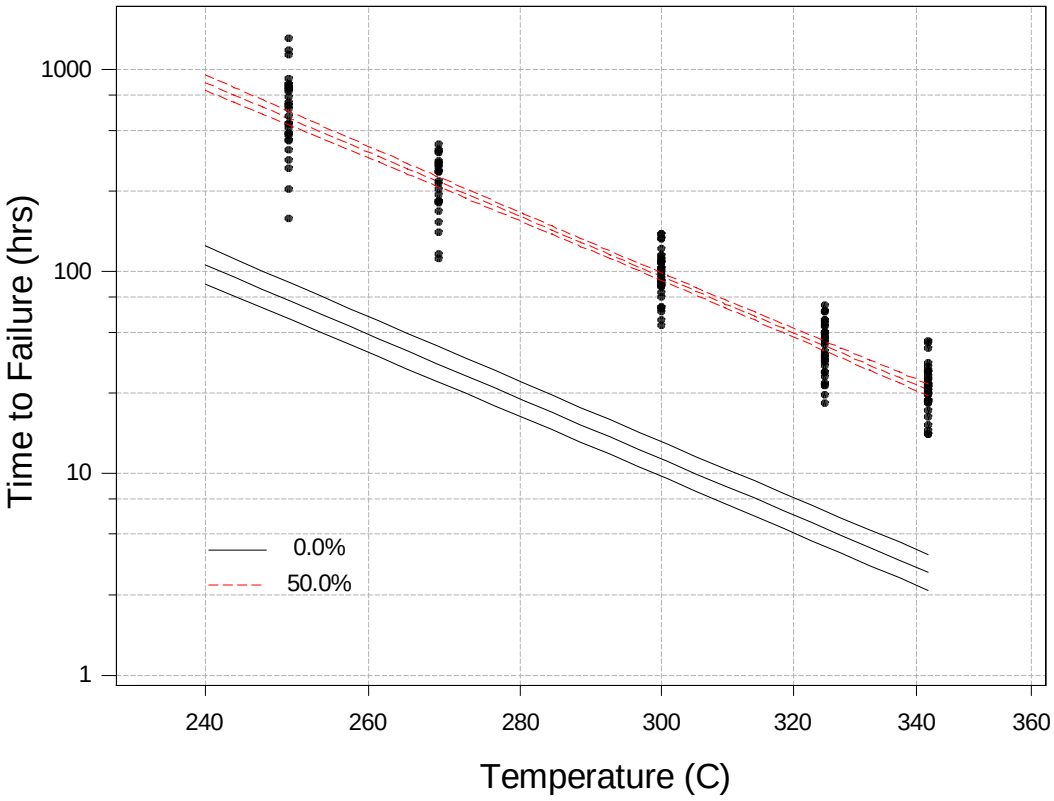


Figure 4.4 An Arrhenius plot of the V1M1 structure fail times tested in a range of temperatures from 250 to 342C. The data is fitted based on the MTTF of the distributions and includes the upper and lower 90% confidence bounds. The Arrhenius fit based on the first failure in 1 million samples (0.000001% value) is also shown below.

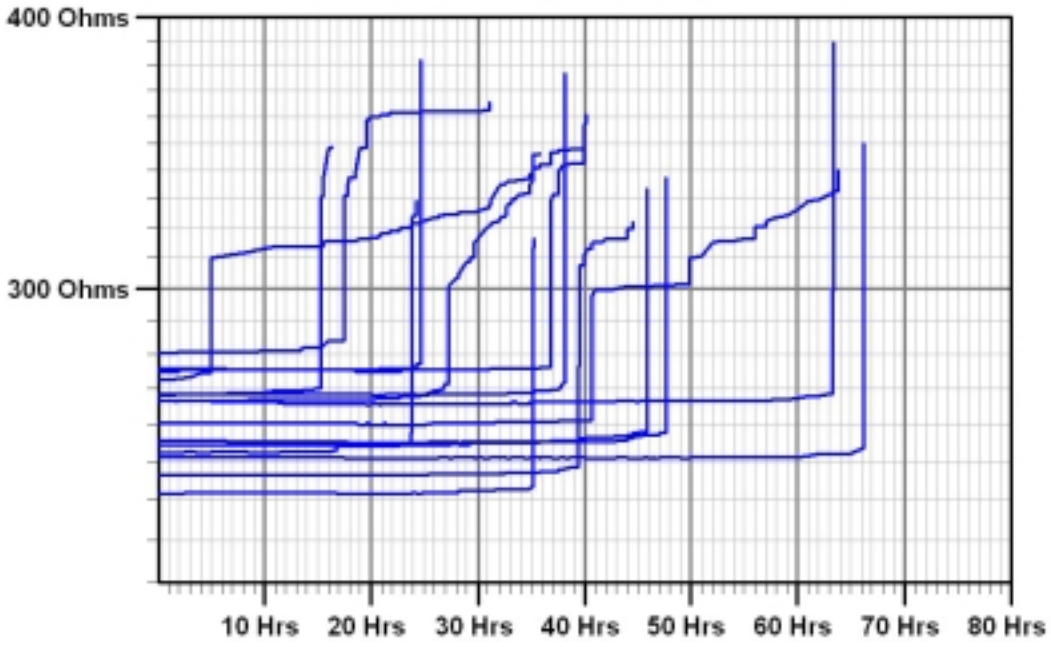


Figure 4.5: Resistance traces of V1M2 structures tested at 342C with 0.67mA stressing current. These traces look similar to those of the v1M1 structures. Some of the samples show a period of slow drift after the initial jump in resistance.

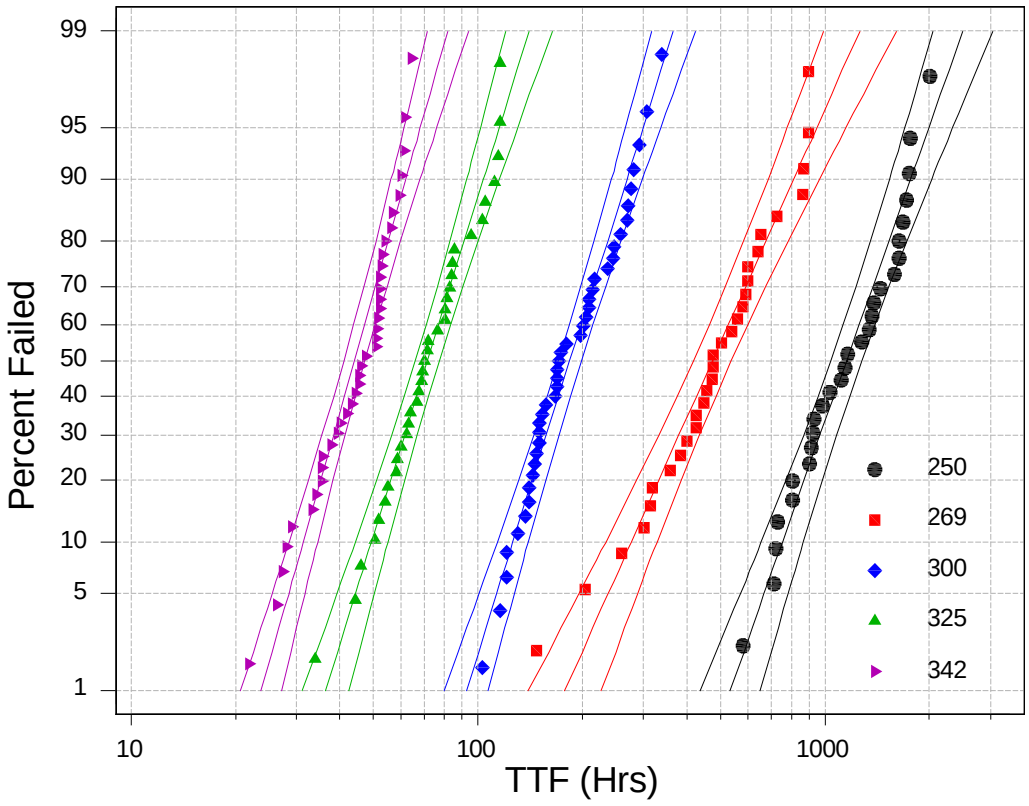


Figure 4.6: Failure distributions of the V1M2 structures tested in a range of temperatures from 250 to 342C. The distributions are fitted and bounded by 90% confidence intervals.

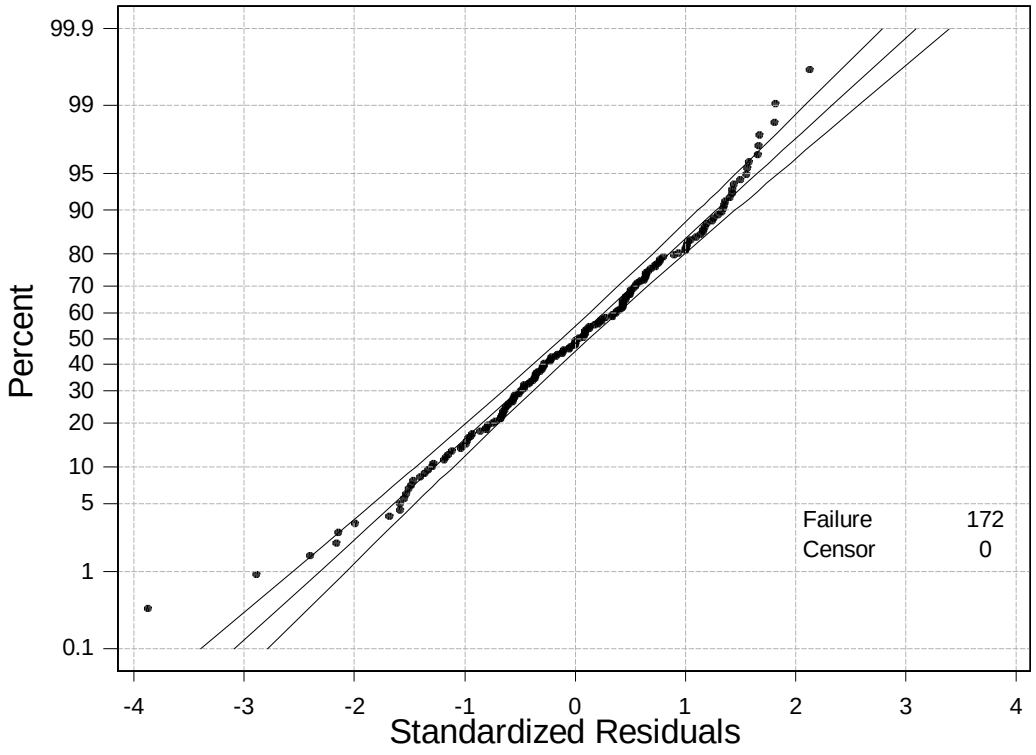


Figure 4.7: A plot of the distribution standardized residuals for the lognormal fit of the V1M2 structures tested in a range of temperatures from 250 to 342C. The plot indicates that the lognormal distribution fits the data well.

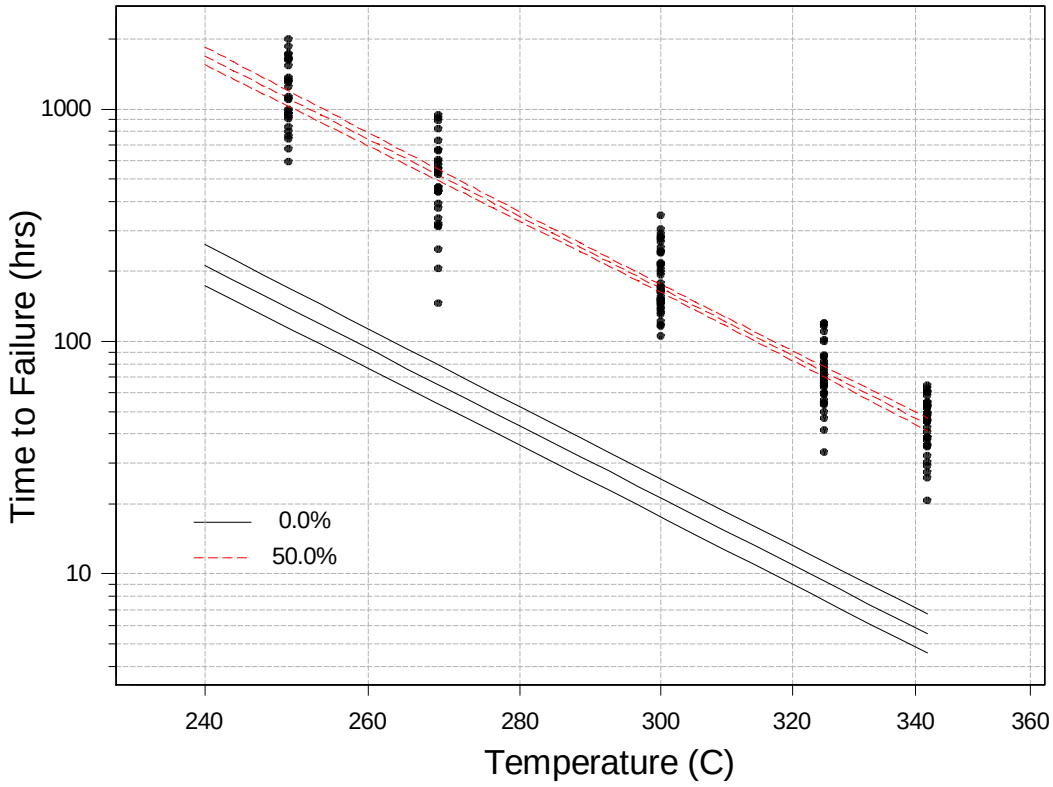


Figure 4.8 An Arrhenius plot of the V1M2 structure fail times tested in a range of temperatures from 250 to 342C. The data is fitted based on the MTTF of the distributions and includes the upper and lower 90% confidence bounds. The Arrhenius fit based on the first failure in 1 million samples (0.000001% value) is also shown below.

Failure analysis was conducted on all selected samples using the techniques described in the failure analysis section of the experimental techniques chapter. In Figures 4.7a and 4.7b SEM micrographs of V1M1 structures tested at 325^{o}C are shown. In both pictures the void location and shape is the same and indicates that the Cu - Si_3N_4 interface is where the diffusion takes place. This is typical for EM in Cu interconnects and has been reported by many researchers [7, 8, 12-16] including. Hu et. al. [7] and Arnaud *et al.* [14,15]. In Figures 4.10a and

4.10b SEM micrographs of V1M2 structures tested at 325^{o}C are shown. The voids in these V1M2 structures have the same slope up to the top Cu - Si_3N_4 interface that the V1M1 structures do indicating that electromigration induced diffusion happens primarily along this interface for both structures. Unlike the V1M1 structures the voids in the V1M2 structures have different locations. Some samples show voiding away from the via as in Figure 4.10a, and some extend over the via as in Figure 4.10b. These results indicate that void formation occurs at different locations in the V1M2 structures or that voids are initially away from the via but then grow towards the via.

The latter explanation is supported by the fact that the void formation would be away from the compressive stresses found down wind from the via. Evidence of void growth in the direction opposite to the direction of electron flow can be seen in Figure 4.11. In this figure the effect of a Cu reservoir can be seen, with the void clearly extending from the W-contact into the reservoir.

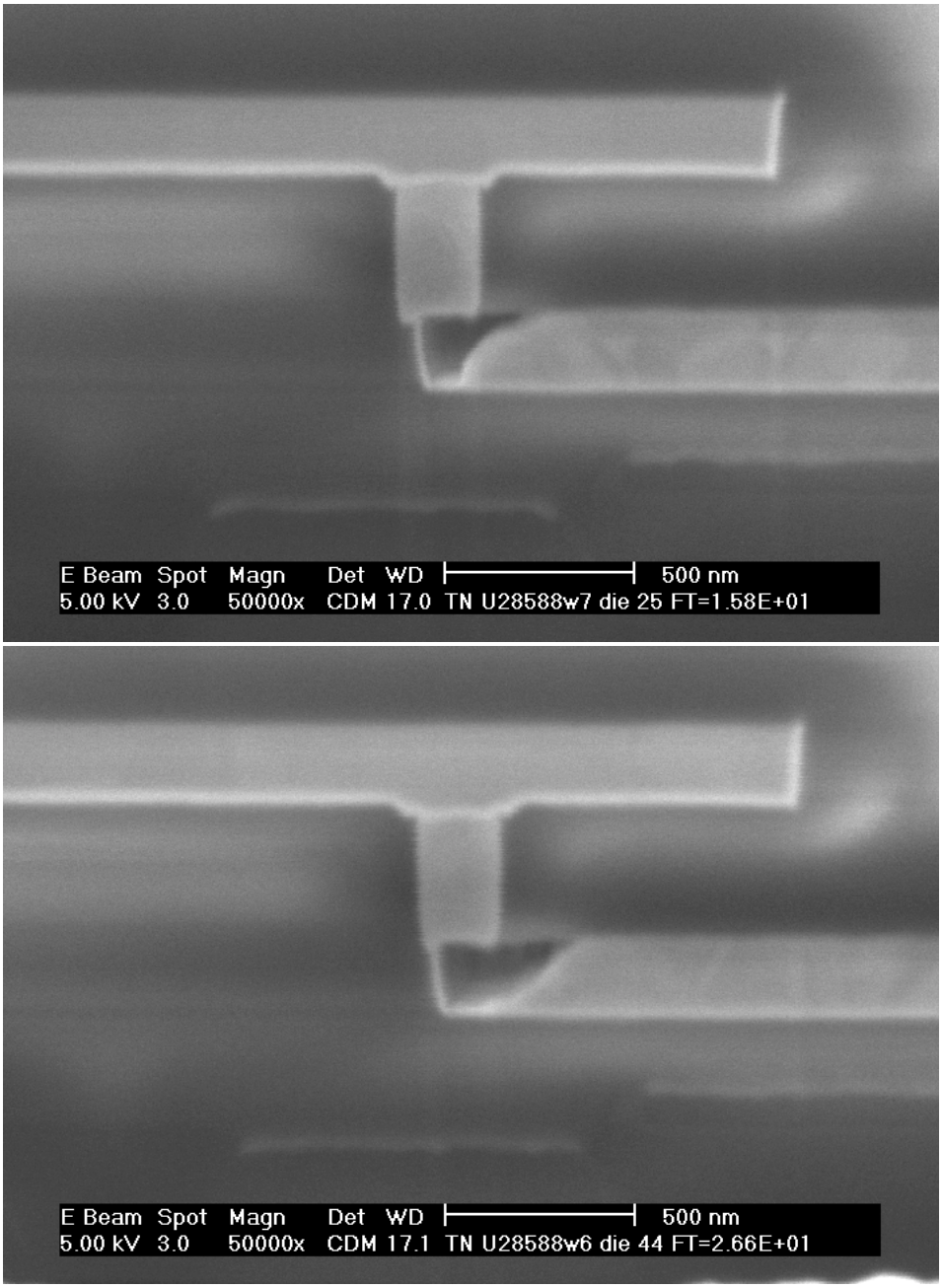


Figure 4.9: (a) SEM micrograph showing the cross sections of V1M1 test structures after EM testing at 325C. The shape of the void suggests that diffusion occurs primarily along the top interface. (b) A similar SEM micrograph taken from a sample tested at 300C.

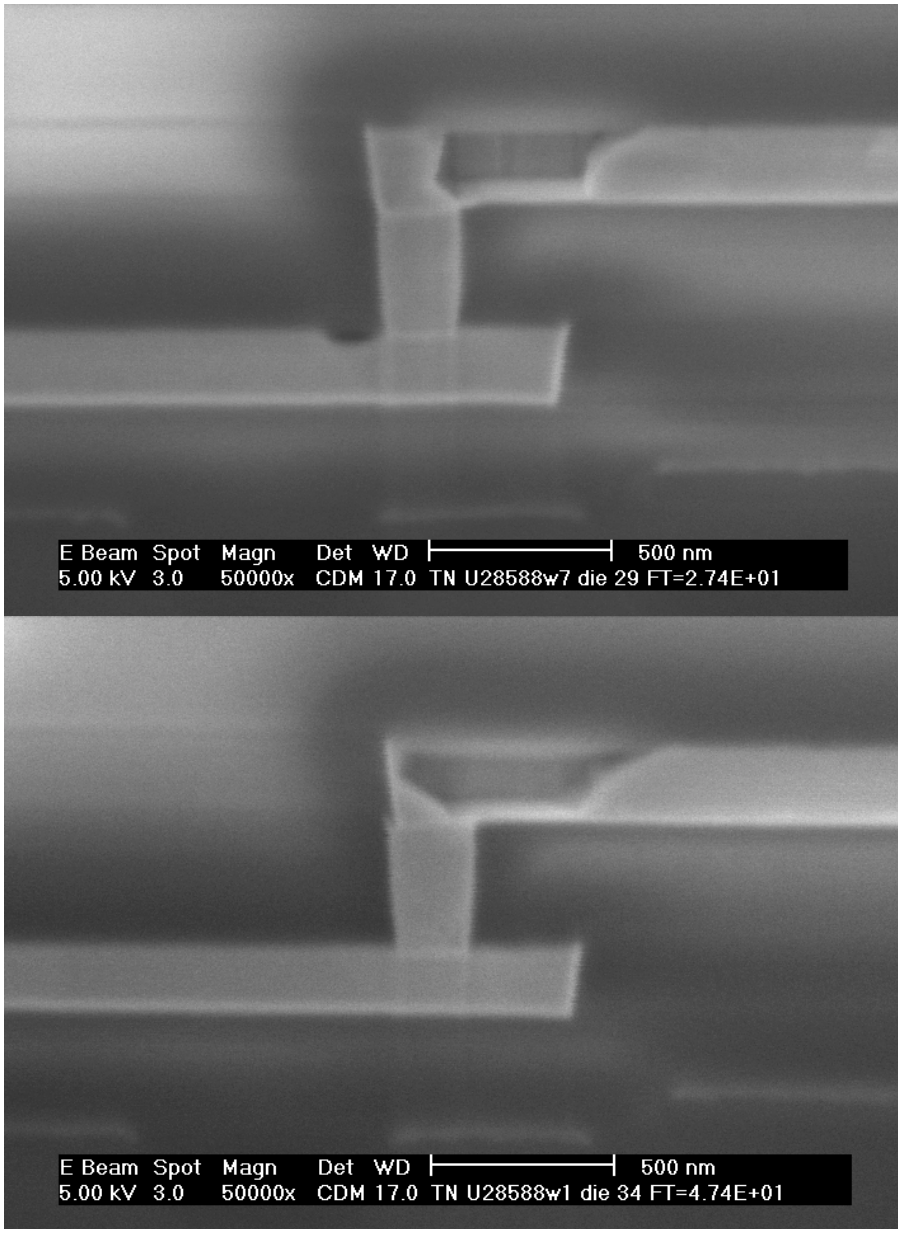


Figure 4.10: (a) SEM micrograph showing the cross sections of V1M2 test structures after EM testing at 325C. The void is downwind from the via and the void front suggests that diffusion occurs primarily along the top interface. (b) A similar SEM micrograph taken from a sample tested at 350C with the void extending over the via.

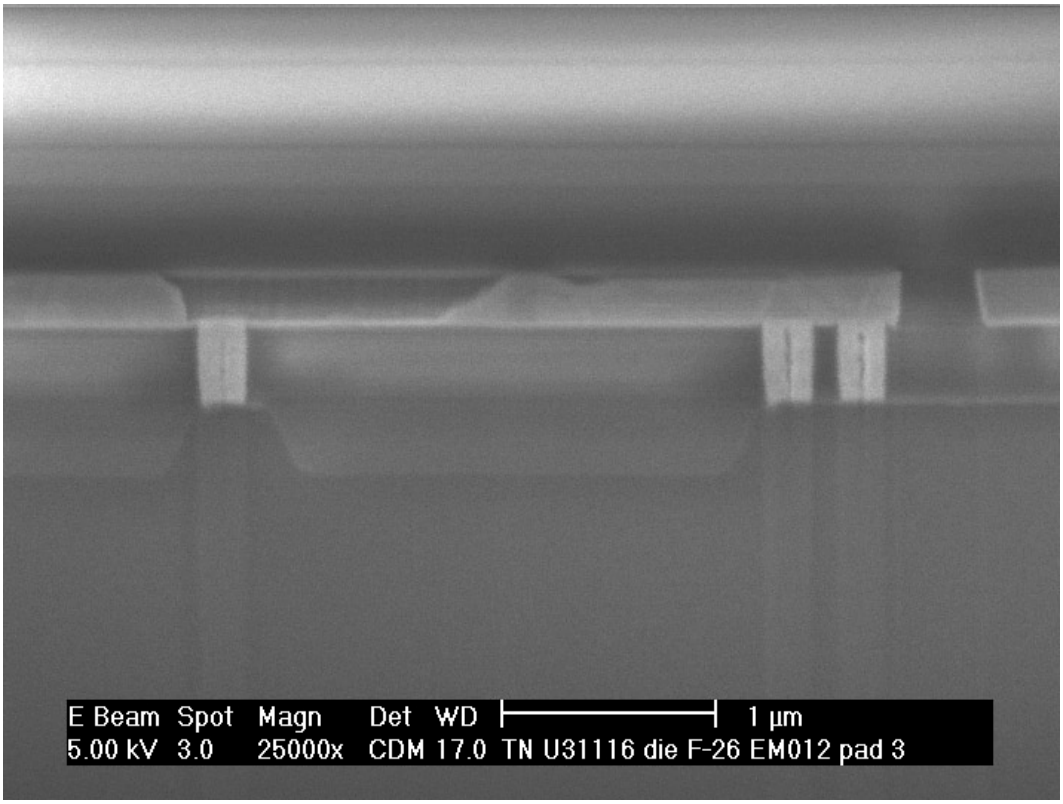


Figure 4.11: SEM micrographs showing the cross sections of Metal 1 test structures after EM. The electron flow was from the single W contact on the left to the left. The void extends away from the contact opposite to the direction of electron flow.

In Table 4.3 the EM activation energy and the lognormal sigma calculated from these tests are shown. The sigma listed is that of the pooled results such as that presented in the plots of the standardized residuals. The two different structures have similar values of E_a implying that both are controlled by the same diffusion mechanism. This is supported by the fact that the failure analysis pictures indicate that the electromigration is controlled by diffusion along the top ESL – Cu interface. With the same diffusion mechanism controlling both

samples they should have the same E_a but not necessarily have the same fail times or lognormal sigma. In this case both structures have similar sigmas but with very different fail times. On average across the 5 testing temperatures the V1M2 samples last almost twice as long (1.9x) as the V1M1 samples do. This drastic difference in lifetime can be explained by the difference in location and morphology of fatal voids in the two samples. In the case of the V1M1 samples the fatal voids will tend to form directly under the via along the Cu – ESL interface. Figures 4.12a,b,c show a schematic of the typical progression of void formation in the V1M1 structures. Because the voids form in a position that is coincident with the fast diffusion interface, the size of the void need not be very big to cause interconnect failure. Put another way, not a lot of Cu needs to be diffused away to cause a large resistance increase.

Table 4.3 The activation energy and lognormal sigma calculated form the results described above. The error rate is also listed for both the E_a and σ in terms of ± value.

Structure	Activation Energy (eV)	Lognormal σ
V1M1	0.94 ± 0.04	0.33 ± 0.03
V1M2	0.94 ± 0.04	0.33 ± 0.03

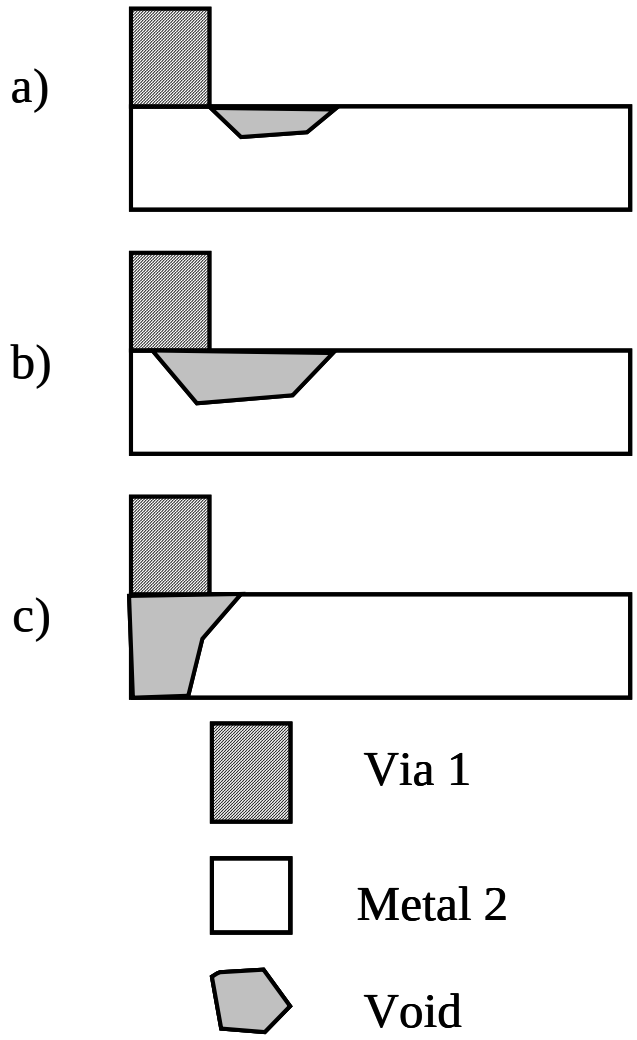


Figure 4.12: A schematic showing the typical void growth in a V1M1 structure. a) The first stage of void formation in which little or no resistance increase is observed. b) The second stage of void formation in which the void grows in the direction of the via. c) A fatal void

In the case of the V1M2 structures the fatal voids typically form over the entire via in a similar fashion as the V1M1 parts. Figures 4.13a,b,c show a schematic of the typical progression of void formation in the V1M2 structures.

Unlike the V1M1 structures the surface of the via where fatal voids will form is not coincident with the fast diffusion interface. The result of this separation is that a void must grow to be significantly larger in order to cause failure. This means that more material must be diffused away from the via area in order to get a significant resistance increase. A simple comparison can be made in order to determine if the drift rate and hence the diffusion mechanism is the same for these two parts. If the drift rate as described in Eq. 4.1 is the same for both samples the ratio of their void size must be equivalent to that of their lifetime. By taking rough estimates of the void size using image analysis software the ratio of the void sizes of these samples was determined to be 1.8. This is nearly the same as the ratio of 1.9 found for their lifetimes and it indicates that the diffusion mechanism for both samples is the same, and their different EM performance is merely a result of their geometry.

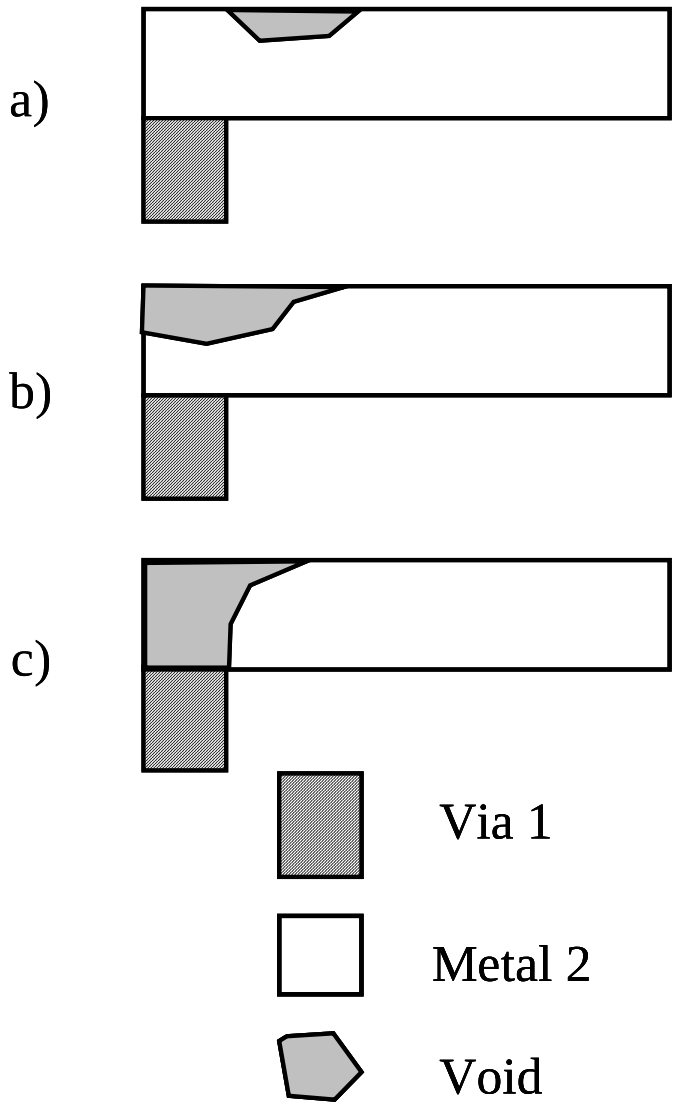


Figure 4.13: A schematic showing the typical void growth in a V1M2 structure. a) The first stage of void formation in which little or no resistance increase is observed. b) The second stage of void formation in which the void grows in the direction of the via. c) A fatal void

Chapter 5: Interconnect Geometry and Electromigration

The impact of interconnect geometry on EM reliability is of critical concern to design of advanced semiconductor devices. Both the width and length of interconnect pathways will be determined by the design with a set of design rules that define dimension limits on the interconnect design. Unlike the width and length, the height of interconnect is not determined by the design, but rather is determined by the process and tuned according to the resistance and capacitance requirements of the design. The electromigration reliability of interconnects is also a function of several process, integration, and design variables. Modern semiconductor devices with identical processing and integration can have drastically different reliability due to differences in the design. Semiconductor products contain interconnects of different length with the shortest of these often being EM resistant due to the Blech effect. Interconnects of different width are also used depending on the amount of current the interconnect must carry. In order to understand the relationship between interconnect geometry and EM reliability kinetic models for the drift rate and void-size as a function of interconnect dimensions were created. EM tests on structures of different length and width were performed and failure mechanisms and resultant void morphology were also examined by failure analysis. The results of which were used to confirm the behavior described in the kinetic models.

5.1 EFFECT OF INTERCONNECT LINE WIDTH

The line width is expected to affect the EM behavior by changing the dimensions of the top and bottom interfaces. The line width impact on microstructure and, as a result, the grain boundary diffusion is not considered here because grain boundary diffusion has been shown not to contribute significantly to EM flux [7, 8, 12-16]. It has been shown that for dual-inlaid interconnects the bottom interface between the Cu metal and the Ta barrier can also contribute to EM flux [17]. Because these samples are made with a single-inlaid process the bottom interface between the Cu metal and the Ta barrier is assumed to not contribute significantly to EM flux [18]. The top interface between Cu and the plasma enhanced Si_3N_4 (PEN) has been shown repeatedly to contribute to EM diffusion the most [7, 8, 12-16]. These interfaces act as fast diffusion pathways in which the Cu moves from anode to cathode.

By assuming that the Cu / PEN interface is the most important surface through which EM occurs it is possible to approximate the effective surface as [18]

$$\delta_{eff} = \delta_s w / wh = \delta_s / h \tag{4.3}$$

where δ_s is the surface width coefficient of the Cu / PEN interface, w is the width of the line and, h is the height of the line. The drift velocity of the line can be written as a function of the effective surface thickness in the following way

$$v_d = \delta_{eff}(1/h)D_s Z_s^* e\rho j / kT \quad (4.4)$$

where D_s is the diffusivity of the Cu / PEN surface and Z_s^*, e, ρ, and j have the same meanings as described in Equation 1.2. In this way the drift velocity and as a result the lifetime of a damascene Cu-interconnect is not a function of the line width when the current density is kept constant.

The effect of interconnect line width on EM behavior was studied using structures based on the basic structures used above but with varying line width. Structures with line widths in multiples of the minimum line width dimension of 0.18μm were used. In addition to the 0.18μm structures, 0.36 μm and 0.54μm were used in this study. In order to comply with the interconnect design rules these structures are terminated in a single via which sits in the center of the line. For the widest structures, the 0.54μm lines, a variant of the structure with two vias was tested as well in order to determine the impact of multiple vias on the EM performance. All of the structures were designed to be long enough to avoid any back stress effect. The structures used in this section are all 250μm long.

Both the V1M1 and V1M2 interfaces were tested with all four structures because the two interfaces could show different line width-dependent behavior. As was discussed in the previous section the V1M1 and V1M2 interfaces fail differently, and this difference might impact how changes in line width will affect the fatal void formation mechanism.

The structures were tested with a constant current density of 1.5MA/cm^2 so that the impact on time to fail and activation energy could be more precisely

gauged. The stressing current was scaled with the increasing line width according to the values shown in Table 5.1. Although the current density through the via does not remain constant in these tests, the vias in these single-inlaid structures are not susceptible to EM damage formation. The tests were conducted at 300^{o}C and 350^{o}C in order to obtain an activation energy for each structure. About 30 samples were tested under each condition in order to provide adequate statistical confidence in the performance of each structure type.

Table 5.1 A summary of the stressing conditions used for the four different line width structures. Both the stressing current, I, and the resultant current density, J, are shown.

Structure	I (mA)	J (MA/cm^2)
0.18 μm	0.67	1.50
0.36 μm	1.33	1.50
0.54 μm (1 via)	2.00	1.50
0.54 μm (2 via)	2.00	1.50

5.1.1 V1M1 Results

The time-to-fail distributions from the varying width V1M1 structures are shown in Figures 5.1 and 5.2. In Figure 5.1 the results from the 300^{o}C tests are shown. The distributions of the single via structures overlap a lot, indicating the line width does not impact the lifetime significantly. The failure distribution of the 2-via 0.54μm structures is off to the right at higher lifetimes indicating the number of vias has a major impact on the lifetime of the V1M1 interface. In

Figure 5.2 the results from the 350°C are shown. There is more spread in the failure distributions at the higher temperature, but the same trends as seen in the 300 °C tests are seen here too. The 0.36μm failure distribution has what seems to be an early fail tail extending to the left. Failure analysis revealed no clear evidence of a different failure mechanism responsible for the early fail tail.

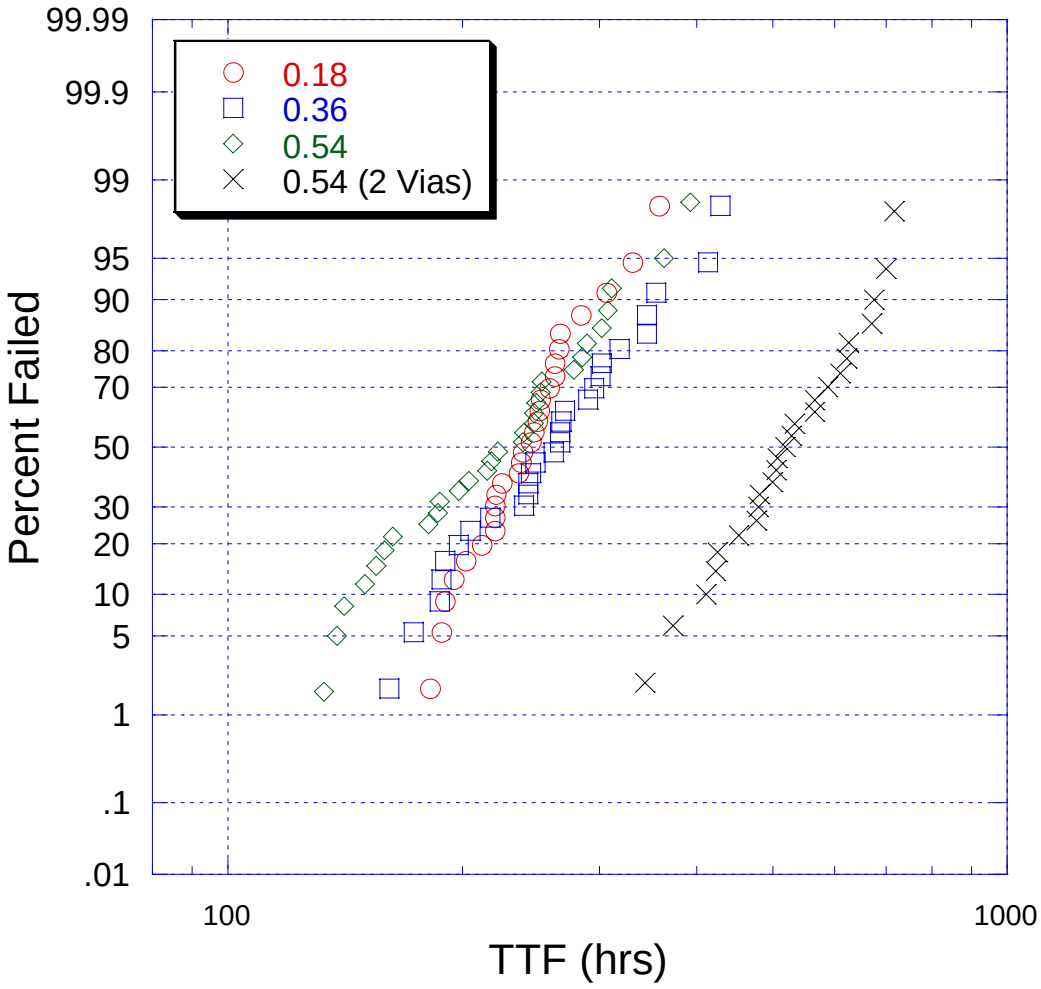


Figure 5.1: The failure distributions of the varying width V1M1 test structures tested at 300°C. The distributions of all of the single via structures line up well, the distribution of the 2-via 0.54μm structures is off to the right at higher lifetimes.

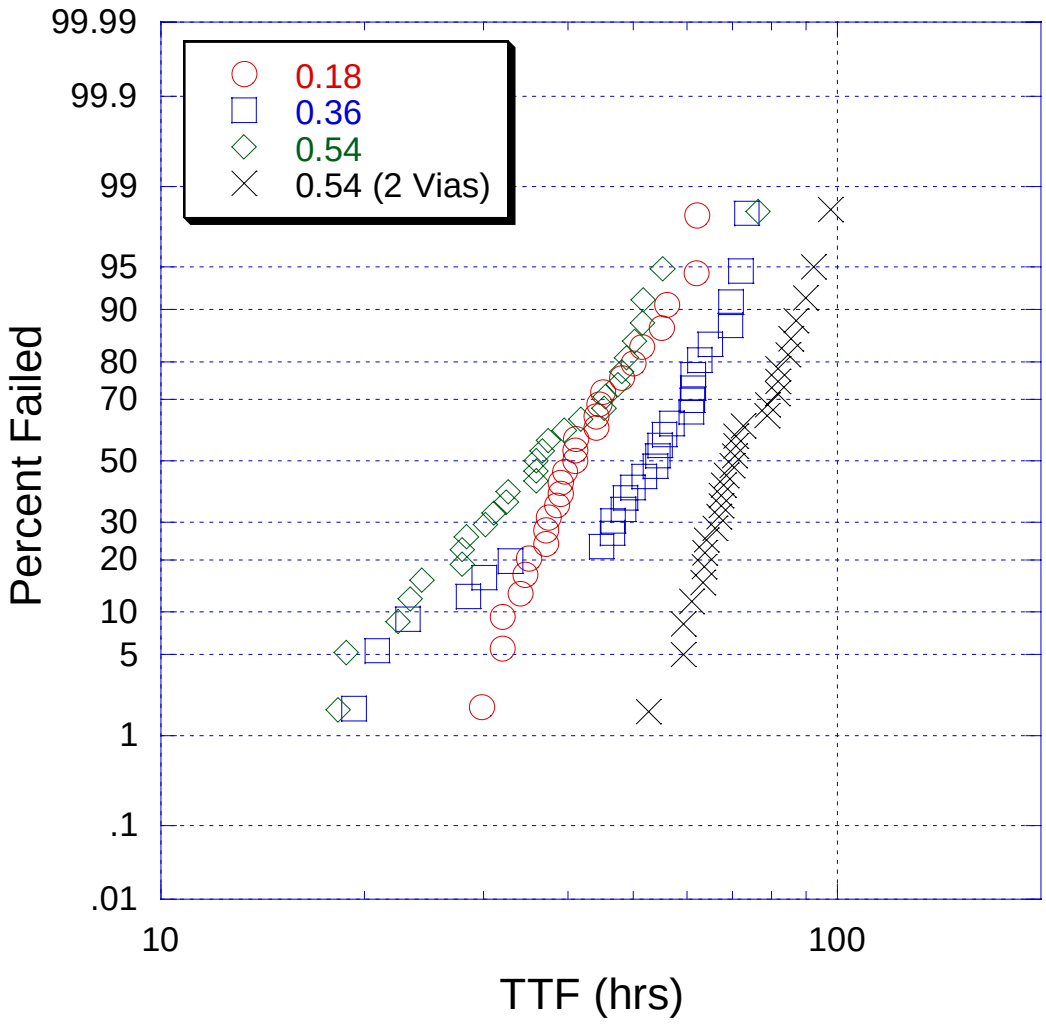


Figure 5.2: The failure distributions of the varying width V1M1 test structures tested at 350°C. There is more spread in the distributions here, but the lifetime of the 2-via 0.54μm structures is still much greater than that of the rest of the structures.

The results for the V1M1 interface are summarized in Table 5.2, in which the activation energy, lognormal sigma, and the median times to failure at 300 ^{o}C and 350^{o}C are shown. The variation of the median time to failure with the line width is shown graphically in Figure 5.3. In this plot the median time to fail (MTTF) at 300^{o}C is shown with a bar indicating the spread of the fail times measured for that test. The MTTF does not show any significant trend with the varying line width at either of the two testing temperatures. The consistency of the median time to failure suggests that either the fatal void volume of these samples does not change or that the void volume does change but the drift rate also scales with the increasing line width. In order to determine which of the two scenarios is in fact true, the dependence of activation energy on line width and size and location of the voids needs to be determined. The MTTFs of the 0.54μm appear to be slightly lower than the others and this is likely the result of some small amount of joule heating in the via which receives a current density of over 4.5MA/cm^{2}. The resultant heating caused a slight dip in the lifetime of these structures.

In Figure 5.4 the variation of activation energy with the line width is shown. The EM activation energy also does not have a significant dependence on the line width. The reason for this is that the diffusion mechanism responsible for electromigration in these parts does not change with varying line width. The result suggests that the drift rate of these samples does not change with increasing line width, which supports the argument that the fatal void size of these samples remains unchanged. In order to confirm that this in fact the case, failure analysis

needs to be conducted to determine the size and location of the voids in these samples.

Figures 5.5 – 5.7 show the results of failure analysis conducted on representative samples from each V1M1 structure. In Figure 5.5 cross-sections of the 0.18μm (1x) and 0.36μm (2x) structures reveal similar void shapes and sizes. In Figure 5.6(a) the 0.54μm (3x) structure also shows similar void shape and size. The voids of the 1x, 2x and 3x structures are assumed to be roughly equivalent in length and are assumed not to expand the entire width of the line in the case of the 2x and 3x structures. In Figure 5.6(b) a cross-section in the middle of the 3x structure with 2 vias is shown. There is no via in the center of this structure but the void is clearly present. In Figure 5.7 cross-sections taken at the two via locations of the 3x-2via structure are shown. The void is clearly present in both of these images indicating that the void extends the entire width of the line.

Table 5.2 A summary of the results from the V1M1 varying line width tests. The activation energy, lognormal sigma, and Median times to failure at 300 and 350°C are included. The error rate is also listed for both the E_a and σ in terms of ± value.

Width (μm)	E_a (eV)	σ	$MTTF_{300}$ (hrs)	$MTTF_{350}$ (hrs)
0.18	1.08 ± 0.05	0.18 ± 0.03	241.0 ± 13.0	43.6 ± 3.3
0.36	1.05 ± 0.08	0.30 ± 0.05	258.6 ± 21.8	47.9 ± 5.6
0.54	1.18 ± 0.08	0.18 ± 0.03	221.0 ± 20.6	36.0 ± 4.0

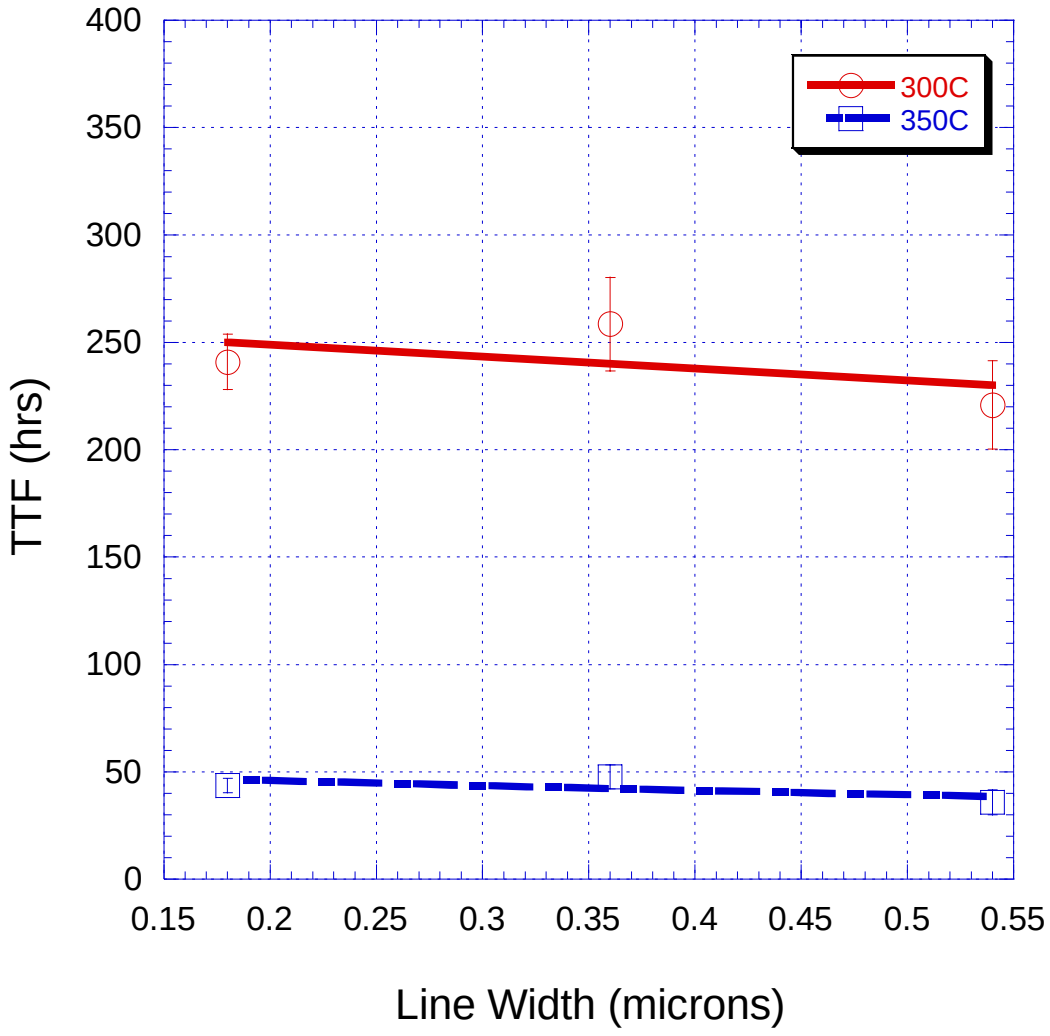


Figure 5.3: A plot of the median time to fail of the V1M1 structures as a function of interconnect line width. The V1M1 fail times are constant with varying line width in a range of 0.18 to 0.54 microns at both 300C and 350C. The error bars represent the spread of the fail times recorded in this test.

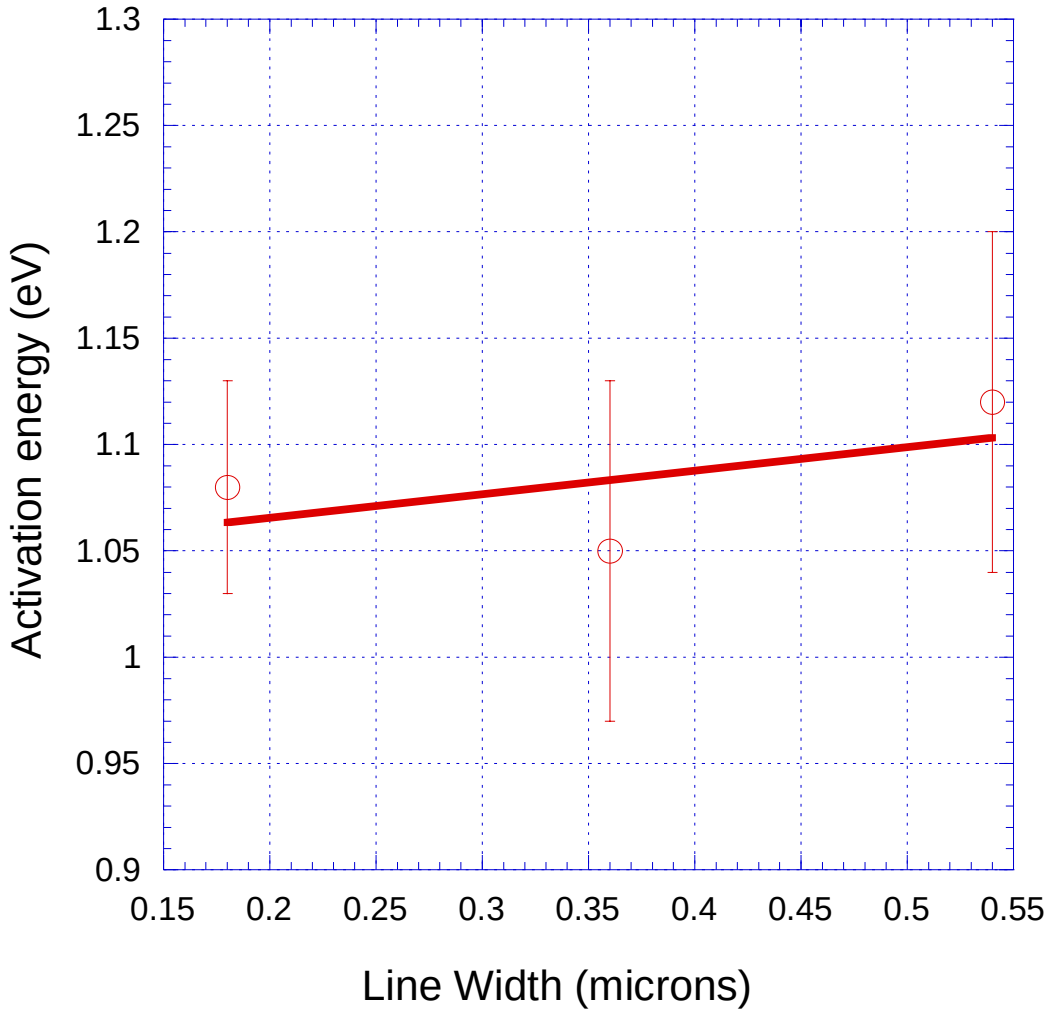


Figure 5.4: A plot of activation energy of the V1M1 structures as a function of interconnect line width.

The impact of multiple vias was also investigated using the 0.54μm wide structures. Table 5.3 lists a summary of the results including the activation energy, lognormal sigma, and MTTF at 300 and 350^{o}C. The activation energies calculated for the structures show the same scatter as the previous tests did and

the results are inconclusive. It is in the MTTF that the impact of the additional vias can clearly be seen. The 2-via structure had fail times almost twice that of the single via structure. The reasons for this can clearly be seen in Figures 5.8, in which a schematic of the voiding in the two structures is shown. In order for void to become fatal in the 2-via structure it must typically grow to encompass the entire line width. In the single via structure a void becomes fatal when it encompasses the relatively small area beneath the via and it need not span the width of the interconnect. The results show that incorporating additional vias in wide Metal 1 interconnects will have a beneficial effect on the EM performance of the V1M1 interface.

Table 5.3 A summary of the results from the V1M1 0.54μm varying via tests. The activation energy, lognormal sigma, and median times to failure at 300 and 350^{o}C are included. The error rate is also listed for both the E_a and σ in terms of ± value.

# of Vias	E_a (eV)	σ	$MTTF_{300}$ (hrs)	$MTTF_{350}$ (hrs)
1	1.18 ± 0.08	0.18 ± 0.03	221.0 ± 20.6	36.0 ± 4.0
2	1.22 ± 0.05	0.17 ± 0.03	547.2 ± 44.8	72.1 ± 3.4

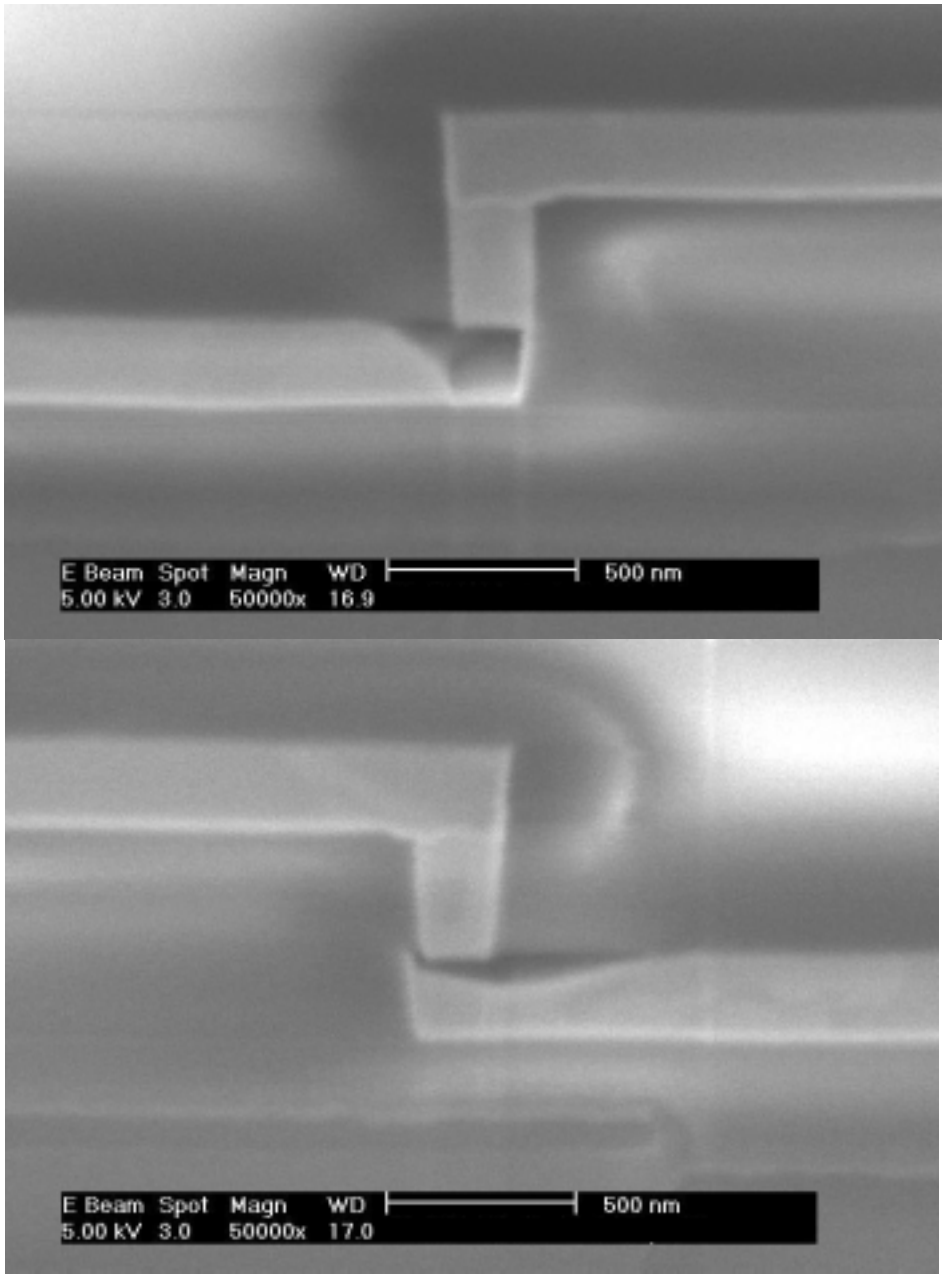


Figure 5.5: (a) SEM micrograph showing the cross sections of the 0.18μm V1M1 test structure after EM testing at 300C. (b) SEM micrograph showing the cross sections of the 0.36μm V1M2 test structure.

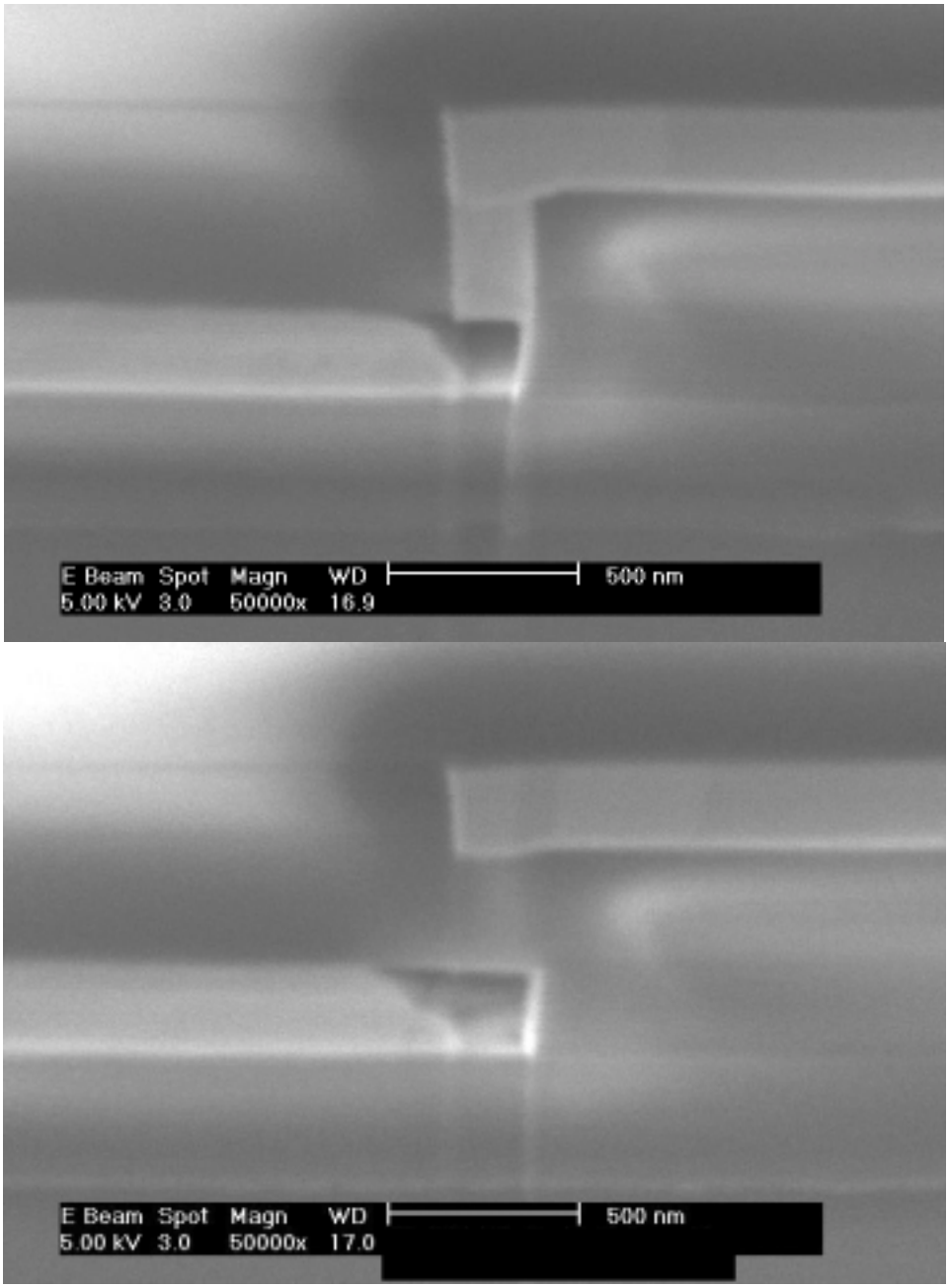


Figure 5.6: (a) SEM micrograph showing the cross sections of the 0.54μm V1M1 test structures after EM testing at 300C. (b) SEM micrograph showing the center cross section of the 0.54μm 2-via V1M1 test structures after EM testing at 300C.

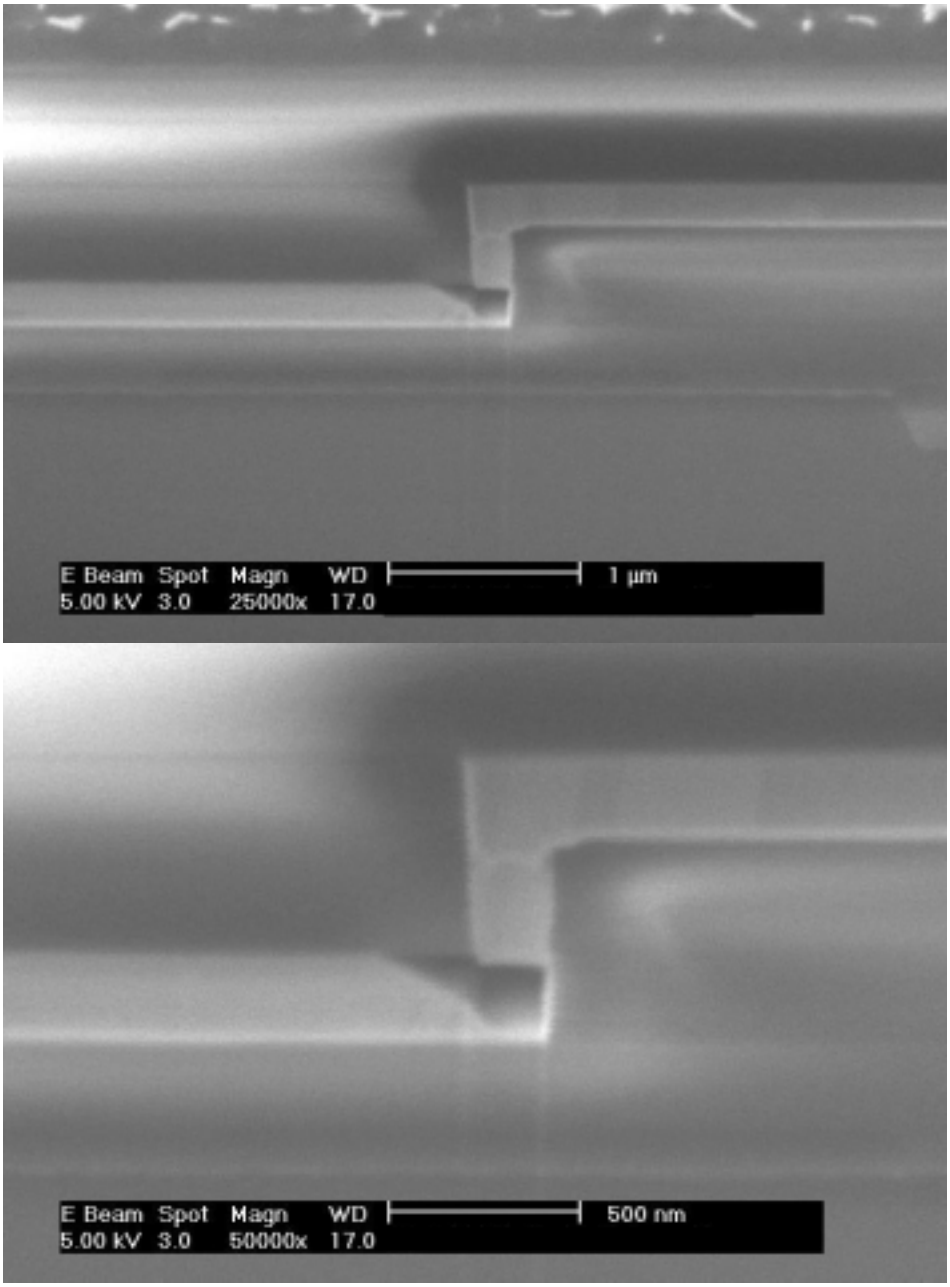


Figure 5.7: (a) SEM micrograph showing the cross sections of the 0.54µm V1M1 test structures after EM testing at 300C. (a) SEM micrograph showing the cross sections of the 0.54µm V1M2 test structures after EM testing at 300C.

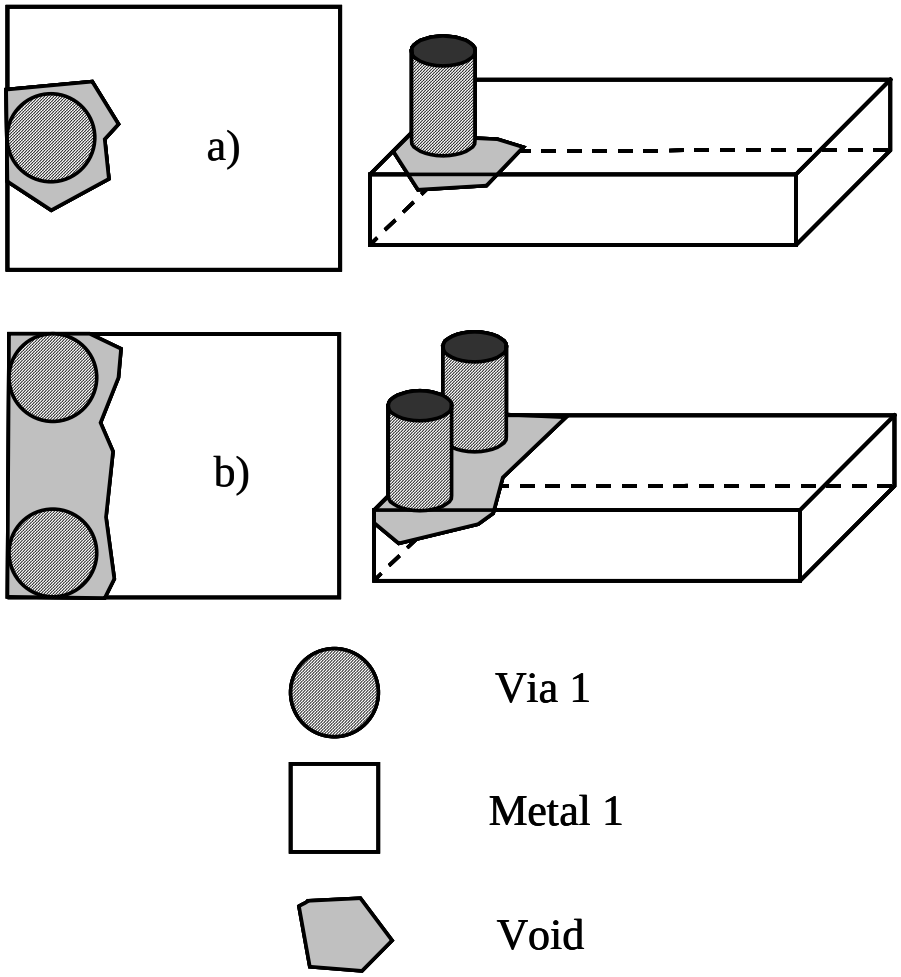


Figure 5.8: a) A schematic showing a typical fatal void in the V1M1 0.54μm single via structure. b) A schematic showing the larger fatal void growth in the V1M1 0.54μm twin via structure.

5.1.2 V1M2 Results

The time-to-fail distributions from the varying width V1M2 structures are shown in Figures 5.9 and 5.10. In Figure 5.9 the results from the 300^{o}C tests are shown. The distributions of all of the structures overlap a lot except for the 0.18μm structures, which failed at consistently lower lifetimes. The distributions of the single and double via 0.54μm structures are nearly identical indicating that the number of vias does not impact the EM lifetime of the V1M2 interface. In Figure 5.10 the results from the 350^{o}C tests are shown. Just as in the V1M1 interface, the failure distributions at the higher temperature show more spread. In this case the 0.18μm structures line up well with the other distributions. Again no difference is seen between the 0.54μm structures with one or two vias.

The results for the V1M2 interface are summarized in Table 5.4, in which the activation energy, lognormal sigma, and the median times to failure at 300 ^{o}C and 350^{o}C are shown. The variation of the median time to failure with the line width is shown graphically in Figure 5.11. In this plot the median time to fail (MTTF) at 300^{o}C is shown with a bar indicating the spread of the fail times measured for that test. Just as was the case for the V1M1 structures, the MTTF does not show any significant trend with the varying line width at either of the two testing temperatures.

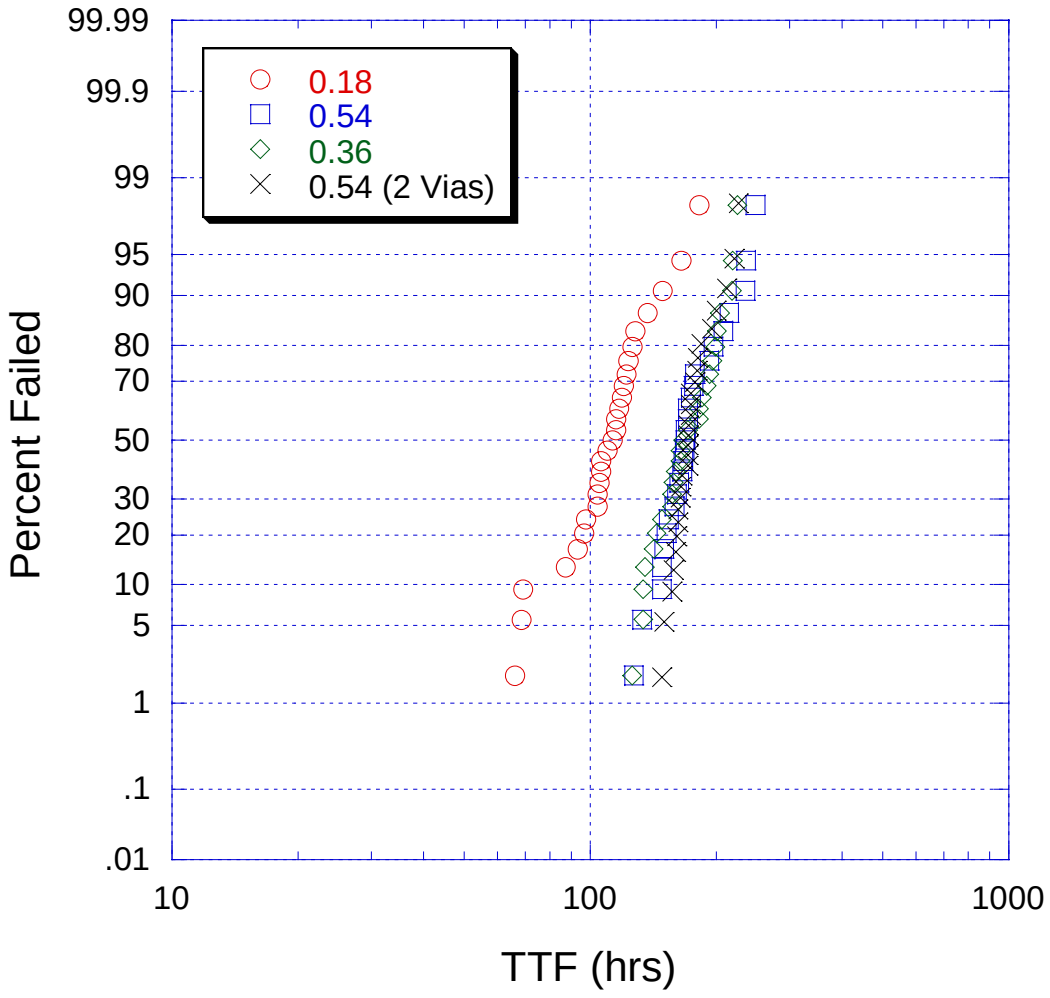


Figure 5.9: The failure distributions of the varying width V1M2 test structures tested at 300°C. The distributions of all of the single via structures line up well except for the 0.18μm structures, which failed somewhat earlier than the others.

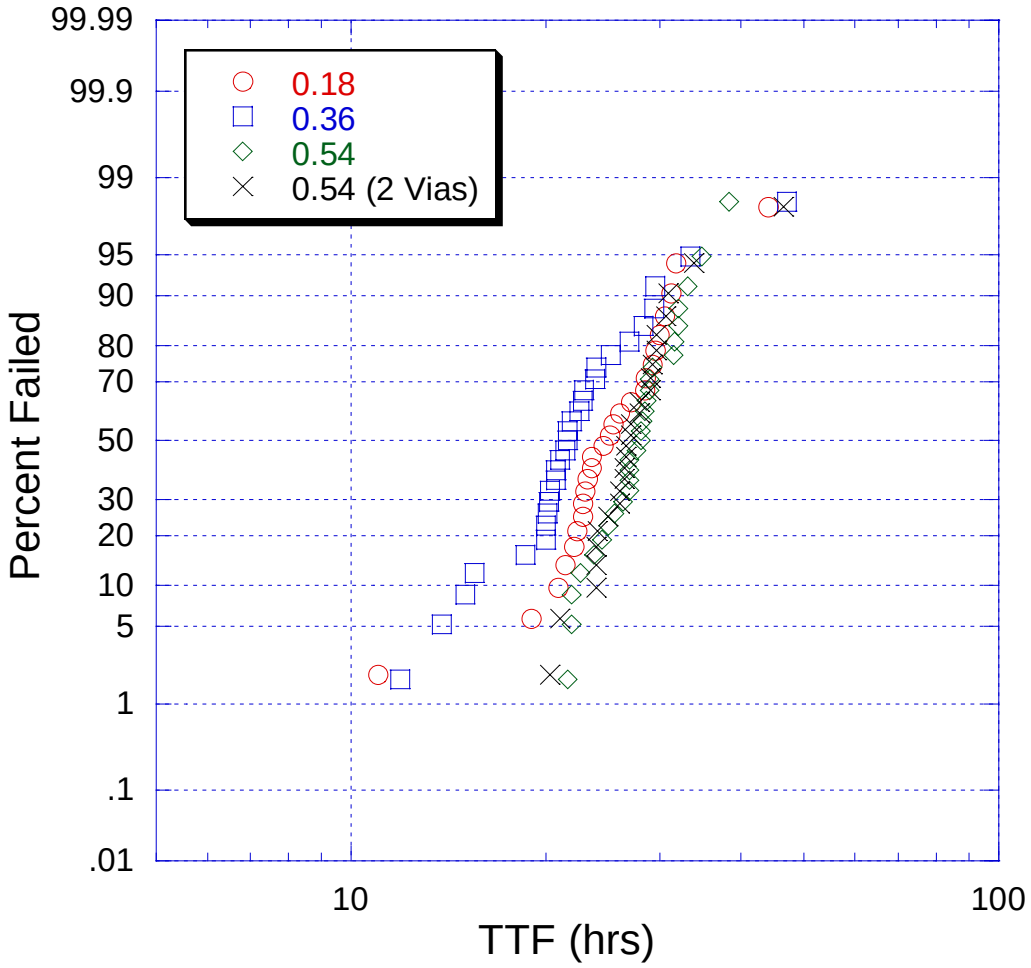


Figure 5.10: The failure distributions of the varying width V1M2 test structures tested at 35°C. The distributions of all of the single via structures line up well.

In Figure 5.12 The variation of activation energy with the line width is shown. The activation energies calculated for these samples don't show any sort of consistent trend. Just as in the case of the V1M1 structures the EM activation energy does not have a significant dependence on the line width. Again, the diffusion mechanism in this case, along the Cu – PEN interface, remains

unchanged with varying line width and hence the activation energy remains unchanged.

Failure analysis was conducted on representative samples from each of the V1M2 structures. Figures 5.13 – 5.15 show the results of failure analysis conducted on representative samples from each V1M2 structure. In Figure 5.13 cross-sections of the 0.18μm (1x) and 0.36μm (2x) structures reveal similar void shapes and sizes. In Figure 5.14(a) the 0.54μm (3x) structure also shows similar void shape and size. In Figure 5.14(b) a cross-section in the middle of the 3x structure with 2 vias is shown. There is no via in the center of this structure but the void is clearly present. In Figure 5.15 cross-sections taken at the two via locations of the 3x-2via structure are shown. The void is clearly present in both of these images indicating that the void extends the entire width of the line just as in the V1M1 structure.

Table 5.4 A summary of the results from the V1M2 varying line width tests. The activation energy, lognormal sigma, and Median times to failure at 300 and 350°C are included. The error rate is also listed for both the E_a and σ in terms of ± value.

Width (μm)	E_a (eV)	σ	$MTTF_{300}$ (hrs)	$MTTF_{350}$ (hrs)
0.18	0.93 ± 0.05	0.17 ± 0.03	113.0 ± 8.7	24.8 ± 1.7
0.36	1.22 ± 0.05	0.18 ± 0.03	180.2 ± 9.6	22.0 ± 1.9
0.54	1.13 ± 0.03	0.12 ± 0.02	174.3 ± 5.9	27.7 ± 1.3

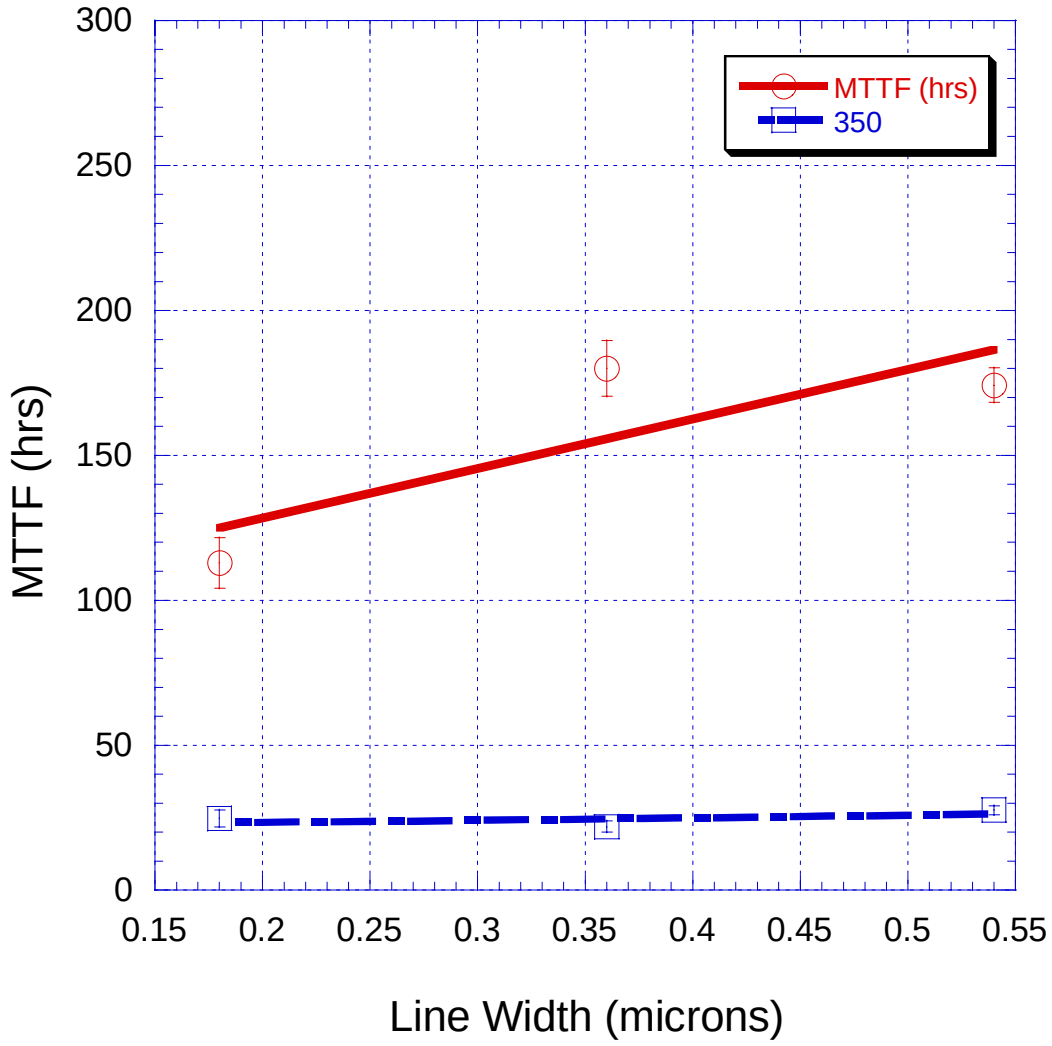


Figure 5.11: A plot of the median times to fail of the V1M2 structures as a function of interconnect line width. The V1M2 fail times increase with the increasing line width in a range of 0.18 to 0.54 microns. The error bars represent the spread of the fail times recorded in this test.

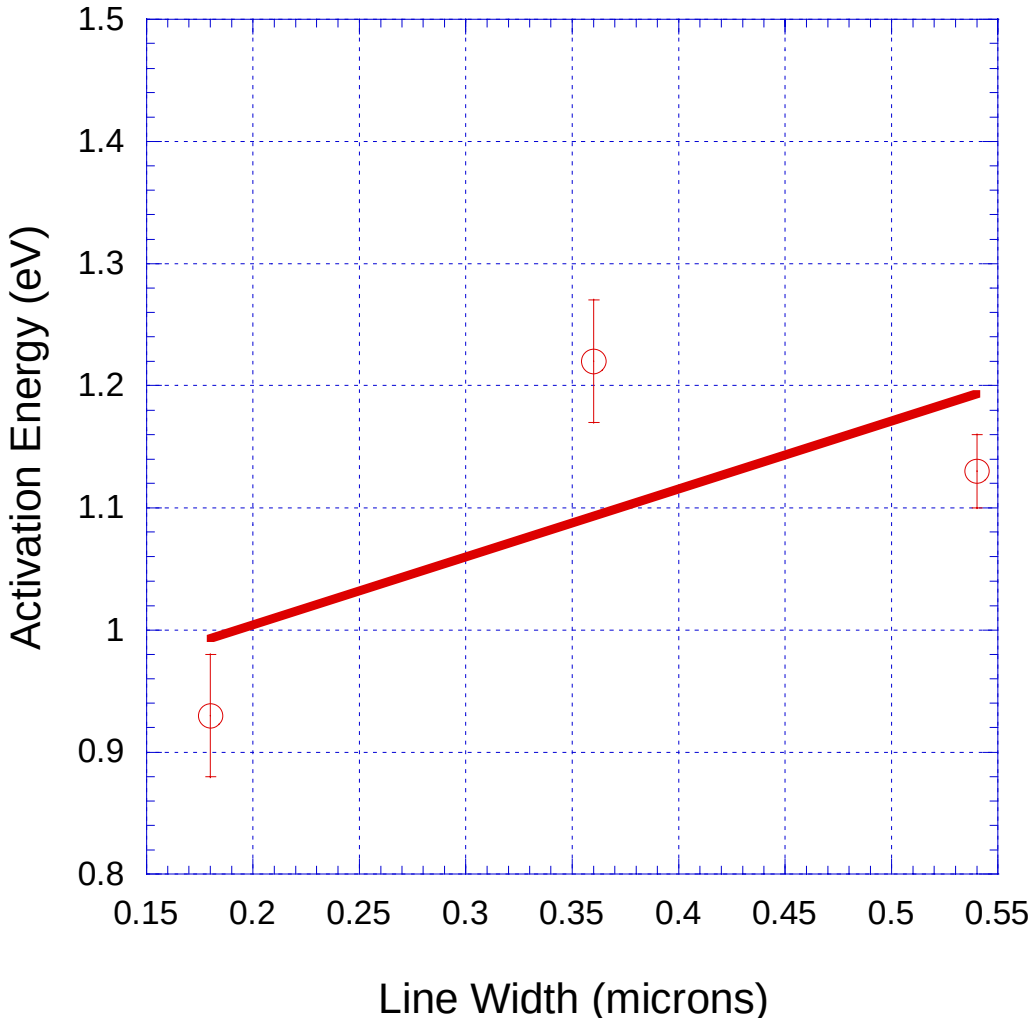


Figure 5.12: A plot of activation energy of the V1M2 structures as a function of interconnect line width.

The impact of multiple vias was also investigated using the 0.54μm wide structures. Table 5.5 lists a summary of the results including the activation energy, lognormal sigma, and MTTF at 300 and 350°C. The activation energies calculated for the structures show the same scatter as the previous tests did and

the results are inconclusive. Unlike the V1M1 structures, the MTTF of the V1M2 structures does not show any dependence on the number of vias. The reason for this non-dependence is related to how fatal voids form in V1M2 structures. This void formation is described section 4.1.2. Because the fast diffusion surface and the flux divergent point in the V1M2 parts are not coincident fatal voids are only formed when the voiding along the top interface grows to meet the top of the via as seen in Figure 4.10. These voids tend to span the entire width of the interconnect line regardless of whether or not there are one or two vias present. Figure 5.16 shows a schematic of the two structures in which voids spanning the entire width of the line in both single and 2-via structures are shown. The results indicate that the addition of vias in wide Metal 2 lines will not impact the EM performance of the V1M2 interface.

Table 5.5 A summary of the results from the V1M2 0.54μm varying via tests. The activation energy, lognormal sigma, and Median times to failure at 300 and 350°C are included. The error rate is also listed for both the E_a and σ in terms of ± value.

# of Vias	E_a (eV)	σ	$MTTF_{300}$ (hrs)	$MTTF_{350}$ (hrs)
1	1.13 ± 0.03	0.12 ± 0.02	174.3 ± 5.9	27.7 ± 1.3
2	1.11 ± 0.04	0.14 ± 0.02	173.1 ± 9.6	28.4 ± 1.7

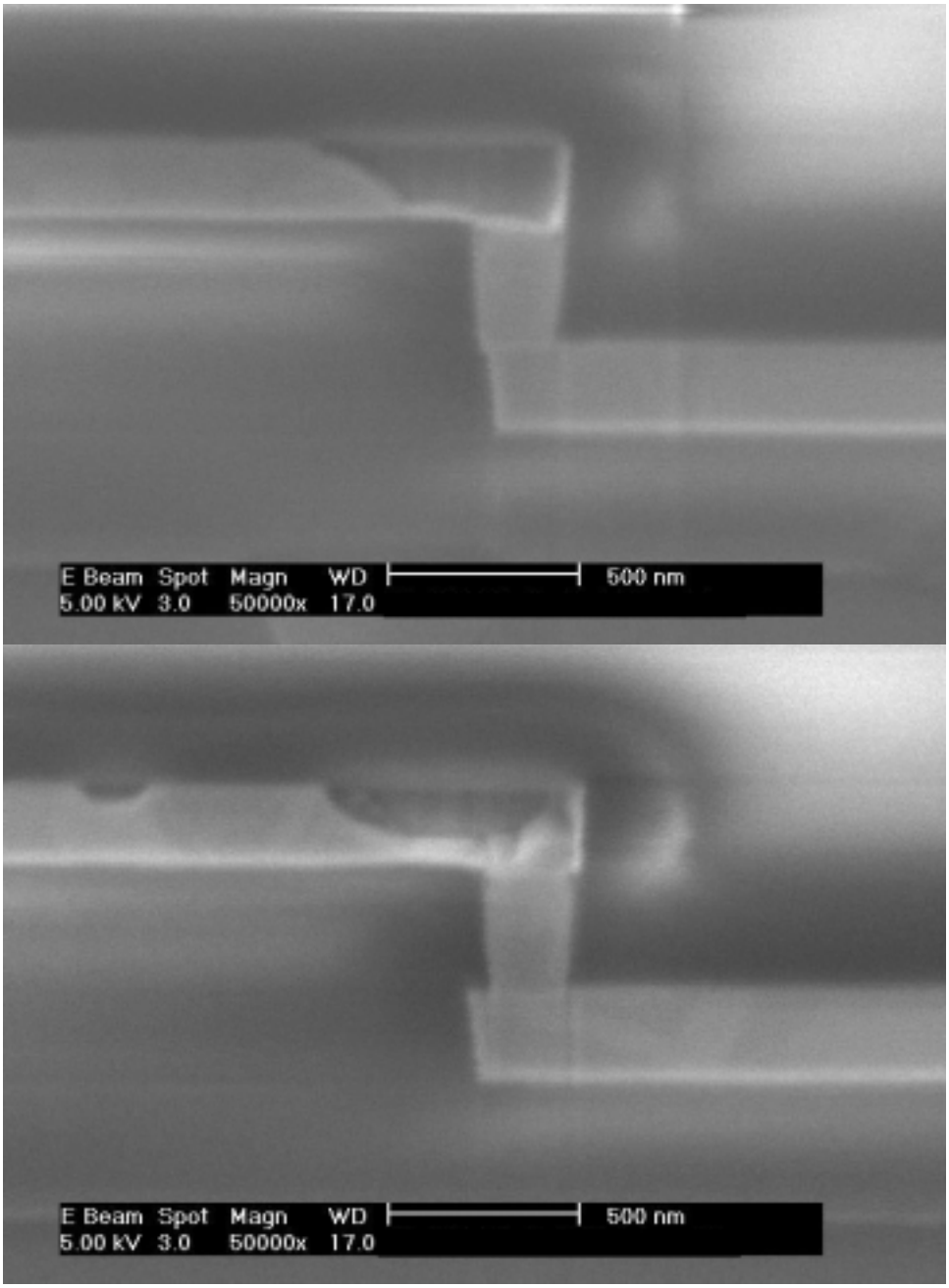


Figure 5.13: (a) SEM micrograph showing the cross sections of the 0.18µm V1M2 test structure after EM testing at 300C. (b) SEM micrograph showing the cross sections of the 0.36µm V1M2 test structure.

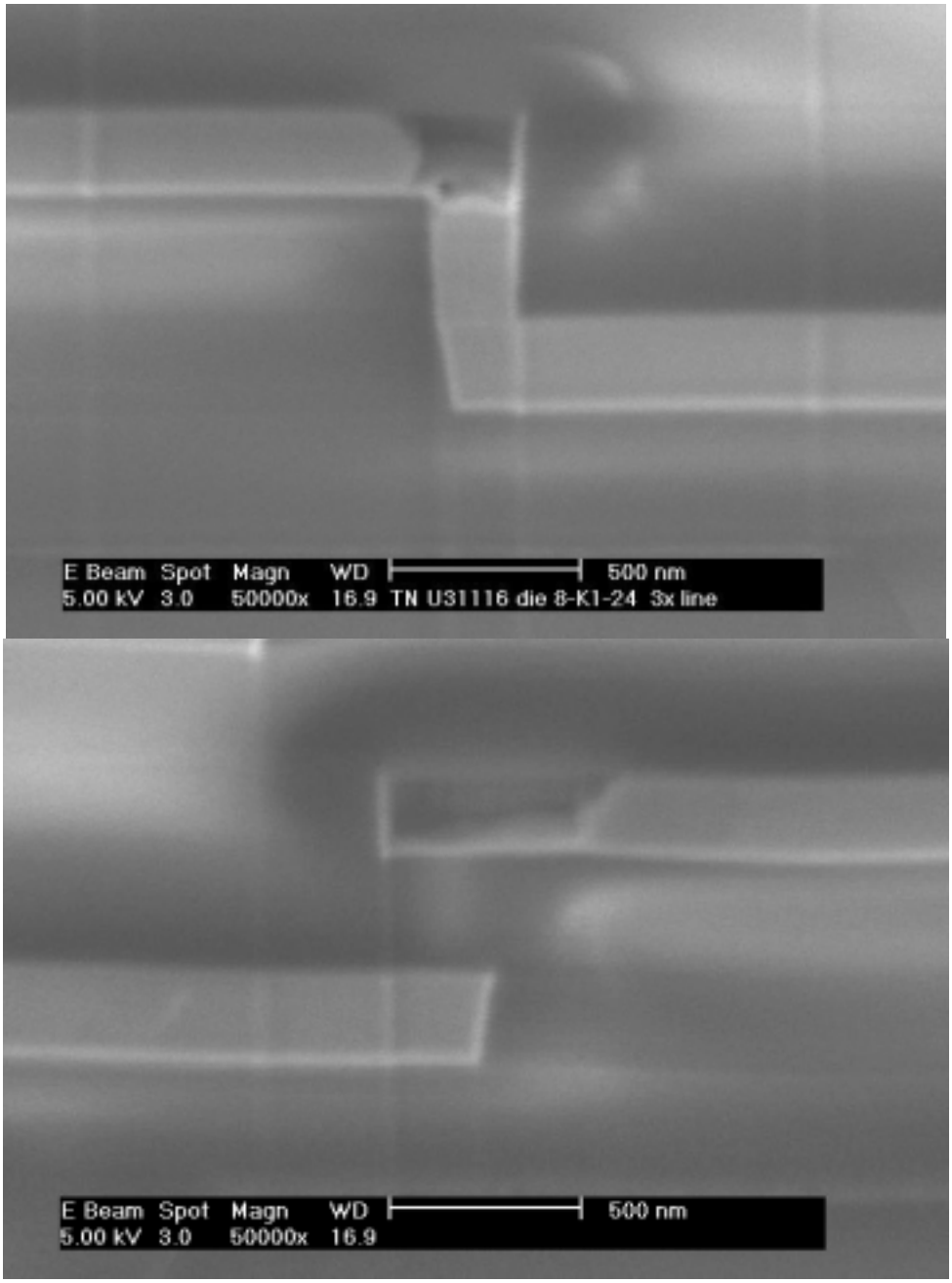


Figure 5.14: (a) SEM micrograph showing the cross sections of the 0.54μm V1M2 test structures after EM testing at 300C. (a) SEM micrograph showing the cross sections of the 0.54μm V1M2 test structures after EM testing at 300C.

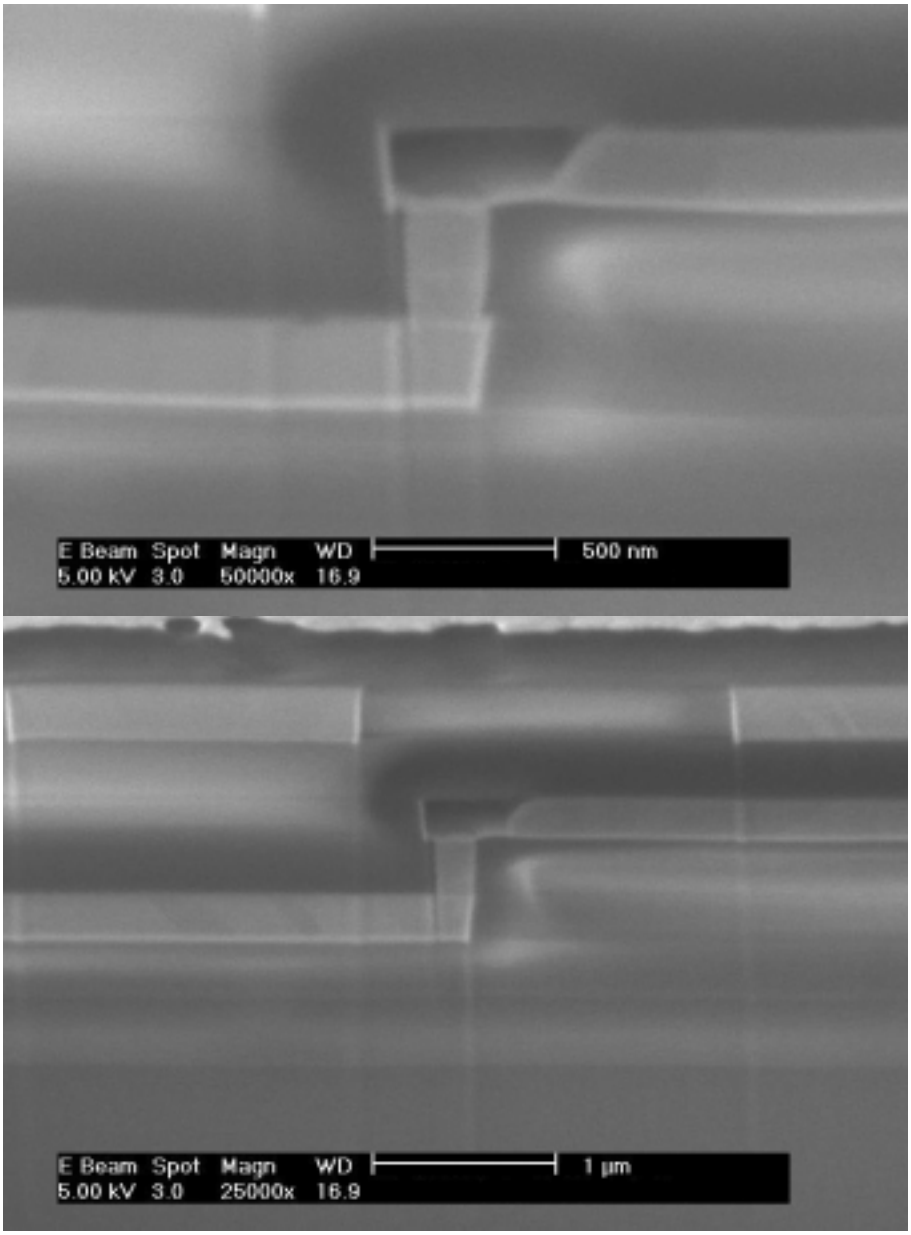


Figure 5.15: (a) SEM micrograph showing the cross sections of the 0.54µm V1M2 test structures after EM testing at 300C. (b) SEM micrograph showing the center cross section of the 0.54µm 2-via V1M2 test structures after EM testing at 300C.

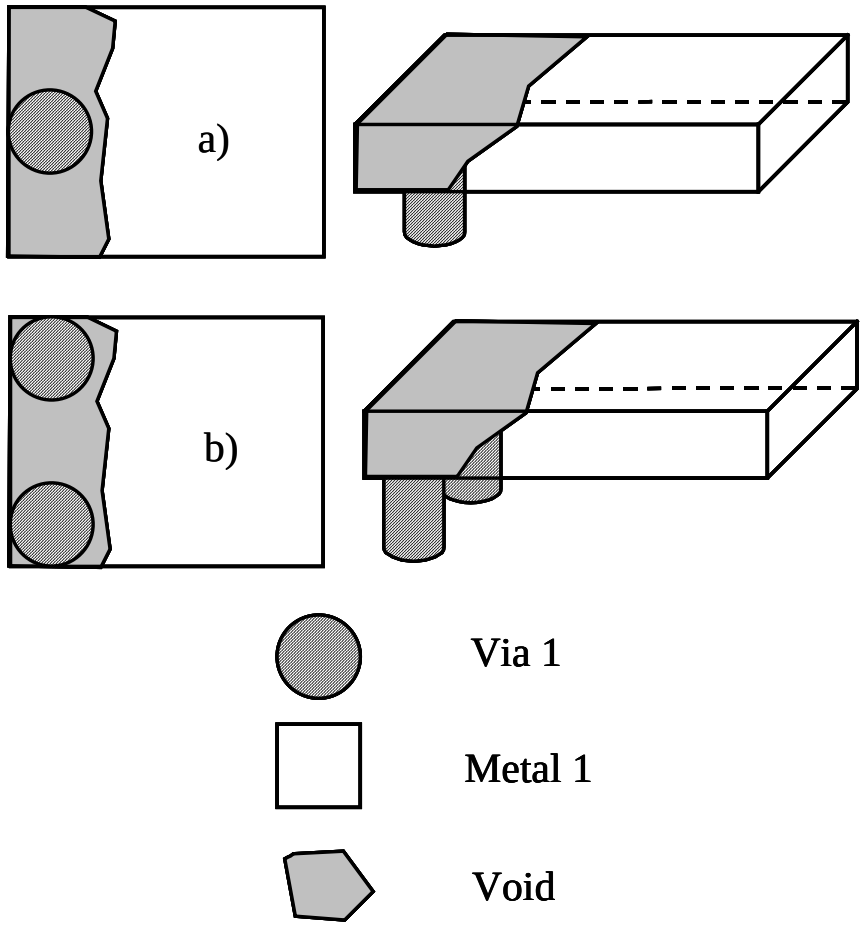


Figure 5.16: a) A schematic showing a typical fatal void in the V1M2 0.54μm single via structure. b) A schematic showing the same fatal void in the V1M2 0.54μm twin via structure.

5.2 EFFECT OF INTERCONNECT LINE LENGTH

The line length is expected to affect the EM behavior by the phenomenon known as the Blech effect in which the flux of material from the anode to the cathode creates a compressive stress gradient [5, 19]. This gradient acts in opposition to the electron wind force, and in certain conditions it can stop the flow of mass altogether. In Equation 4.5 the net flux of Cu atoms, J_{net}, is shown as a function of these two forces.

$$\begin{aligned} J_{net} &= nv_d = n(v_e - v_b) \\ &= n(D/kT)(z^* e\rho j - \Delta\sigma\Omega_a / \Delta L_{eff}) \end{aligned} \tag{4.5}$$

Where v_d is the net drift velocity, $\Delta\sigma/L$ is the stress gradient, Ω_a is the atomic volume, and L_{eff} is the effective line length. The effective length is used to account for the reduction in length as a result of void growth, it is defined in the equation below.

$$\Delta L_{eff} = L - \Delta L_{void} \tag{4.6}$$

Figure 5.17a shows a schematic of an interconnect with plot of the hydrostatic stress state of the line before voiding begins. At the anode, greater tensile stresses are created as a result of the depletion of Cu atoms from this

portion of the line. As material is relocated down-wind, compressive stresses develop and a stress gradient from anode to cathode is created. This gradient acts to reduce the driving force for mass flux and slows electromigration. For an unvoided line the gradient will evolve until there is an uniform stress gradient along the line. This stress evolution is seen in Figure 5.17a. For short lines the gradient is much larger, and as a result the driving force for electromigration is often reduced to zero. At the critical length condition as described below,

$$v_d = 0 \text{ when } jL \leq jL_c \tag{4.6}$$

the net drift velocity becomes zero, and there is no further failure in the interconnect. A similar situation arises for interconnects after a lot of material has moved to the cathode, the compressive stress gradient will increase and eventually create the same critical length condition. In this situation void growth will eventually stop and the resistance will saturate. This resistance saturation effect was often seen in Al(Cu) interconnects, in which a TiN layers acts as a shunt layer allowing for the formation of large voids.

Recently, more sophisticated models of the line length effect in confined lines have been established by Korhonen *et al.* [20]. These models are based on the following equivalence

$$dC/C = -d\sigma/B \tag{4.7}$$

in which dC/C is the change in the number of available lattice sites per unit volume and $d\sigma$ is the change in stress and B is the effective bulk elastic modulus. In the case of Cu interconnects B will be very sensitive to the geometry of the line, as well as the thickness of the barrier and capping layers. In the situation in which the jl product is higher then the jl* value voiding can occur. In this case the void will nucleate and grow in a tensile stress field located at the cathode. The local tensile stresses will be relatively low in the region of the void due to the constant flux of Cu atoms acting to reduce the stress state and create a vacancy equilibrium [20]. The flux of Cu atoms does, however, create large compressive stresses that cover most of the line and that peak at the anode end of the line. In Figure 5.17b the stress gradient in a Cu line is shown after the void has begun to form. As the void growth continues the front of the compressive stress field will move towards the growing void and the tensile stresses in the void region will drop [21]. Eventually the Cu flux caused by this compressive stress field will counter the electromigration flux and the void will stop growing. In Al(Cu) interconnects, this situation would result in resistance saturation in which the EM induced resistance increase saturates. This phenomenon is seen in Figure 5.18 in which the resistance trace of an EM test on an Al-Cu test structure is seen [22]. In Cu interconnects the result is somewhat more complicated because of the lack of an effective shunt layer. Once the void extends pass the length of the via and electrical connectivity of the line is maintained solely through the thin Ta barrier the resistance will increase drastically. The result is that resistance saturation in

Cu interconnects is difficult to observe and was in fact never observed in the course of this study.

Table 5.6 The void length past the via at 30% resistance increase for the various line length structures.

L	ΔL_v from Eq. 4.5 (nm)	ΔL_v from Eq. 4.6 (nm)
250	313.1	104.4
150	187.9	62.6
50	62.6	20.9
25	31.3	10.4
10	12.5	4.2

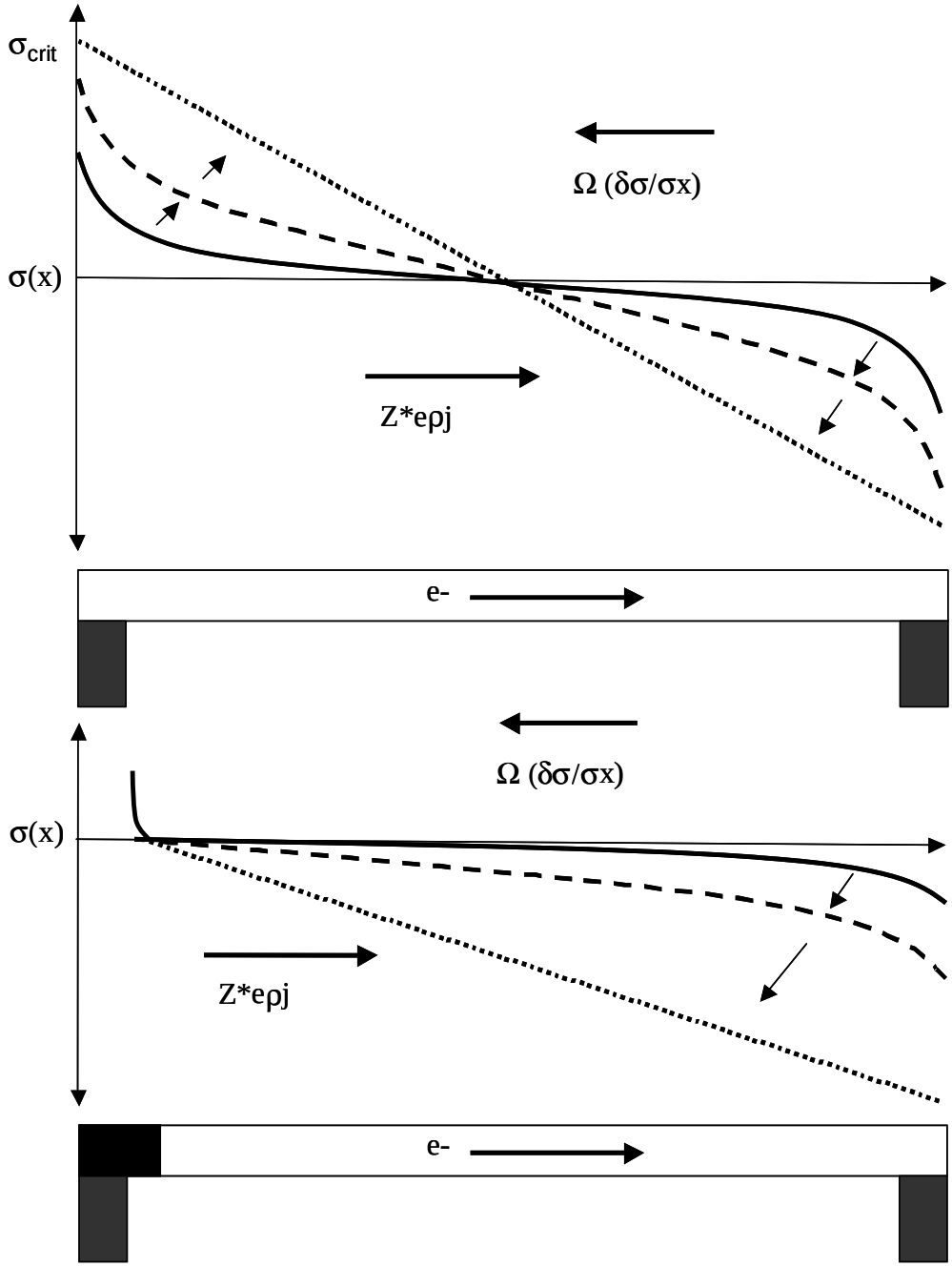


Figure 5.17: (a) A schematic showing the stress state during void growth in a contact (CaM1) test structure. The stress state in an pre-voiding interconnect. (b) The stress state with a void present. The tensile stress region is limited to the voided region once voiding occurs.

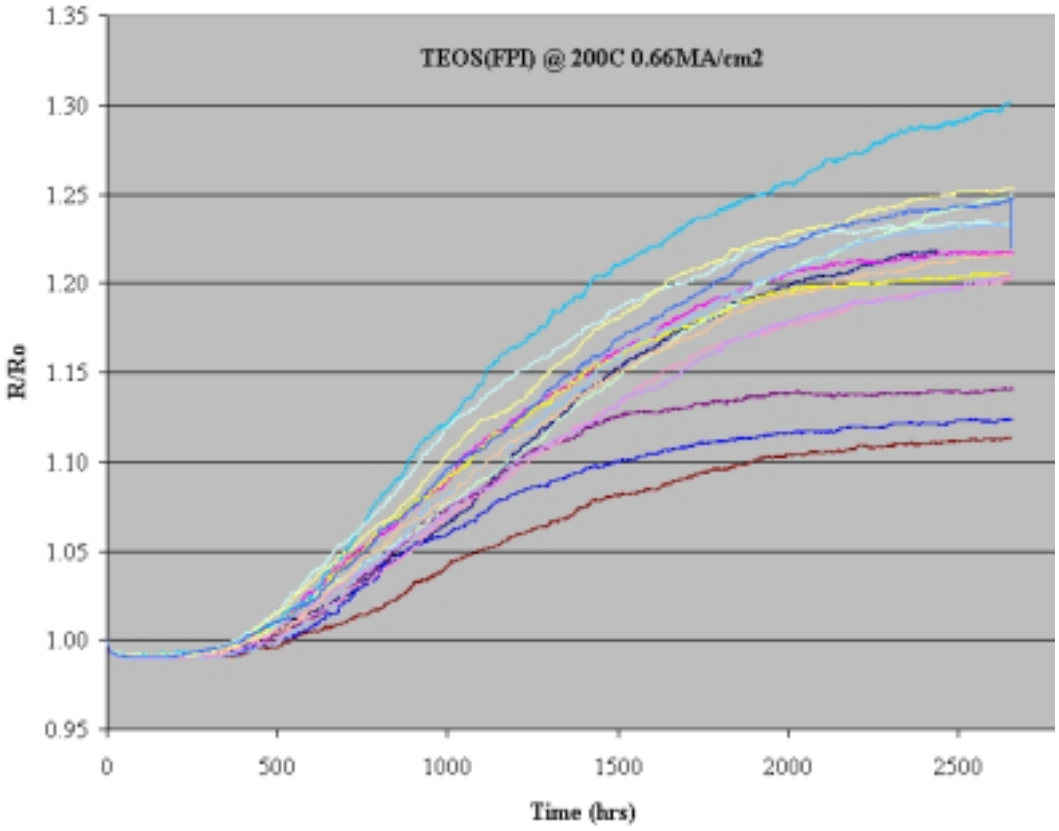


Figure 5.18: Resistance saturation as seen in Al(Cu) – TEOS interconnects. The effective TiN shunt layer allows for current to still effectively pass through the structure allowing for the observation of resistance saturation.

5.2.1 Results

The effect of interconnect line length on EM behavior was studied using structures based on the basic structures used above but with varying line length. Structures with line lengths of 250, 150, 50, 25 ,10, and 5μm were used. All of the structures are based on a 0.18μm wide Contact - Metal-1 (CaM1) test structure. Two rounds of EM testing were conducted to first roughly estimate the critical length and then to determine it more precisely. The first round of tests were done using a constant current density with varying length structures to determine a range of jl*. Each of the structures was stressed at 300^{o}C and 350^{o}C with an applied density of 1.5MA/cm^{2}. The second round of tests were done using the 25μm and 50μm structures with varying current density to precisely determine jl*.

The time to fail distributions from the first round of tests are shown in Figures 5.18 and 5.19. In Figure 5.18 the results from 300^{o}C show failure distributions for the 50 and 150μm structures are shown. None of the shorter structures failed after 500 hours of testing suggesting that they were below the jl* threshold. In Figure 5.19 the results from the 350^{o}C show failure distributions for the 25, 50 and 150μm structures. Less than half of the 25μm structures failed after 500 hours of testing. The median time to failure of the data was determined using a least squares fit method to fit the data with a lognormal distribution and extending this lognormal distribution to the 50th percentile.

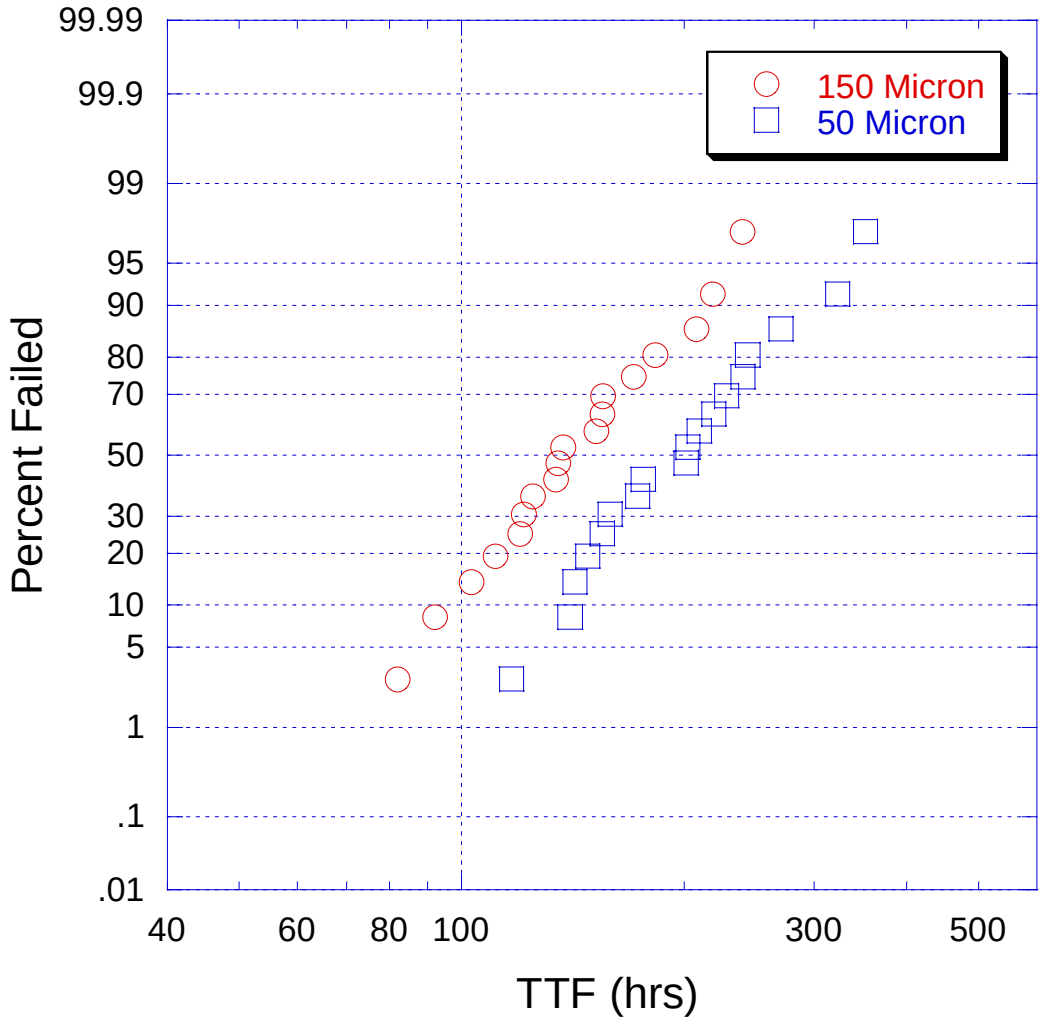


Figure 5.19: The failure distributions of the 50 and 100µm structures tested at 300°C. These were the only two structures to fail after 500hours of testing.

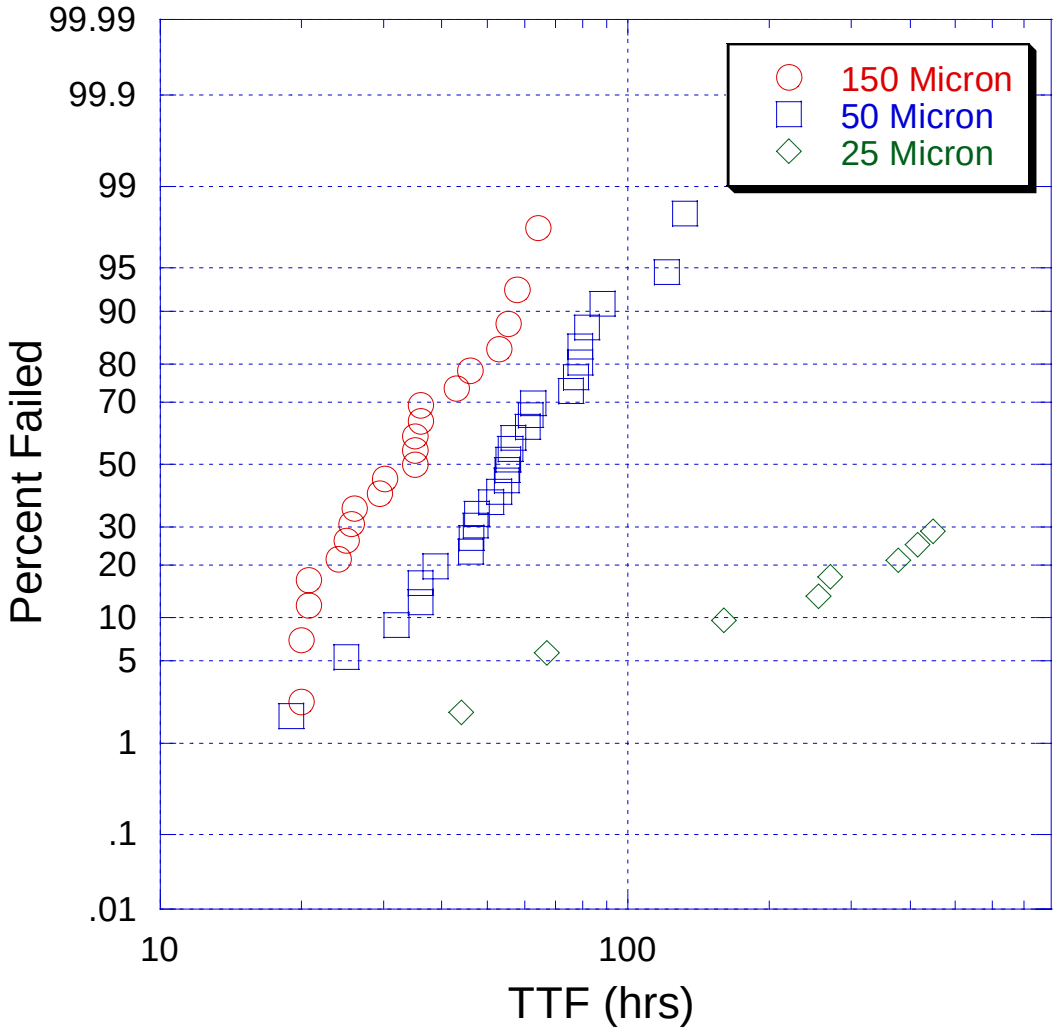


Figure 5.20: The failure distributions of the 25, 50, and 100µm structures tested at 300°C. The 25µm data is incomplete because only 8 of 30 parts failed after 500 hours of testing.

The results for the varying length structures are summarized in Tables 5.7 and 5.8, in which the median times to failure and lognormal sigma are shown for each of the six different structures tested at 300°C and 350°C. The median time to failure and the lognormal sigma both increase as the line length decreases. At

350°C, less than half of the 25μm structures fail, resulting in a large extrapolated value of median time to failure.

Table 5.7 The Median Time to Fail (MTTF) in hours for varying length CaM1 structures tested at 350°C.

Line Length (μm)	$MTTF_{350}$ (hrs)	σ
5	-	-
10	-	-
25	1432.4 ± 1009.9	1.82 ± 1.00
50	55.0 ± 7.8	0.44 ± 0.11
150	32.9 ± 4.7	0.38 ± 0.11

Table 5.8 The Median Time to Fail (MTTF) in hours for varying length CaM1 structures tested at 300°C.

Line Length (μm)	$MTTF_{350}$ (hrs)	σ
5	-	-
10	-	-
25	-	-
50	197.0 ± 23.1	0.31 ± 0.10
150	141.2 ± 18.0	0.31 ± 0.10

The results summarized above can be explained by examining the back-stress effect on the drift velocity and resultant time to failure. As the line length becomes shorter, the amount of back stress increases. From Equation 1.9 the

MTTF can be seen as being proportional to the inverse of drift velocity as is written below.

$$MTTF \propto 1/v_d \tag{4.8}$$

Equation 4.6, which describes the drift velocity in terms of jl*, can then be re-written with MTTF in the following way.

$$MTTF \rightarrow \infty \text{ when } jL \rightarrow jL_c \tag{4.9}$$

So as the jl* threshold is approached the drift velocity will approach zero and the time to failure will become infinite.

The inverse MTTF as a function of line length was plotted in Figure 5.21. The drift velocity at both temperatures becomes zero near the 25μm length suggesting that the critical length at the stressing current density of 1.5MA/cm^2 is near 25μm. This would equate to a jl* of approximately 3400 A/cm. From this data the jl* was estimated as being between 3000 and 4000 A/cm. This estimate is consistent with findings from other researchers who have measured the jl* product on similar single-inlaid test structures [23,24].

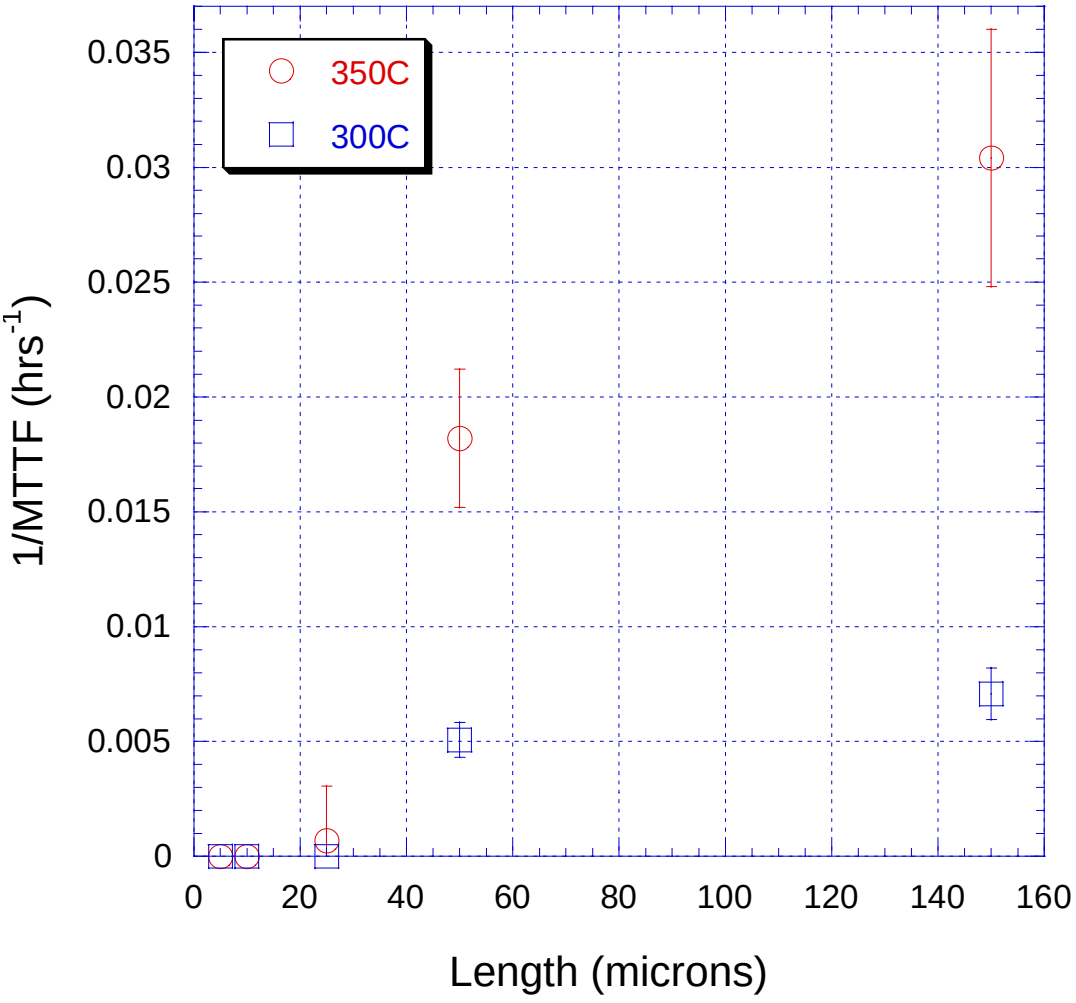


Figure 5.21: The inverse of the median time to failure ($MTTF^{-1}$) plotted against the structure length. Both the 300 and 350°C curves intersect the x-axis at roughly the same value. This plot is used to estimate jl*.

In the second round of tests the 25 and 50μm structures were tested with a range of currents from 0.45mA to 1.35mA at a temperature of 350°C. These two lengths were selected because they were the two shortest structures to have failed in the previous round of tests. The currents were selected so that at all conditions jl* is exceeded allowing failure to occur. In Figure 5.21 the results from the

second round of tests on the 50μm structures are shown. The distribution of the low current data is wide compared to the other data. Just as in Figure 5.19 the lognormal sigma of the failure distribution increases rapidly as the critical length condition is approached. In Figure 5.23 the 25μm data is shown. The data taken from the first round of tests at 0.67mA is also included.

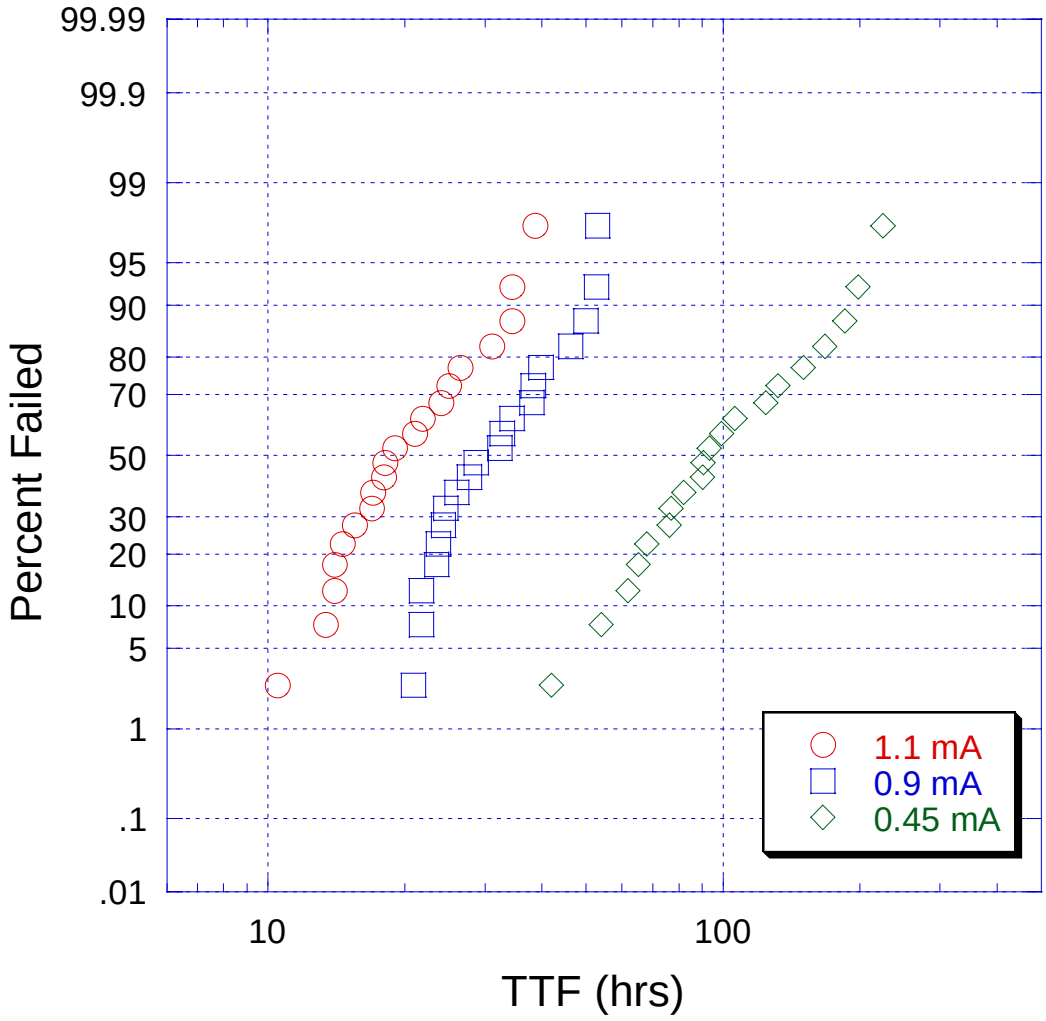


Figure 5.22: The failure distributions of the 50 μm structures tested at 350°C with a range of currents.

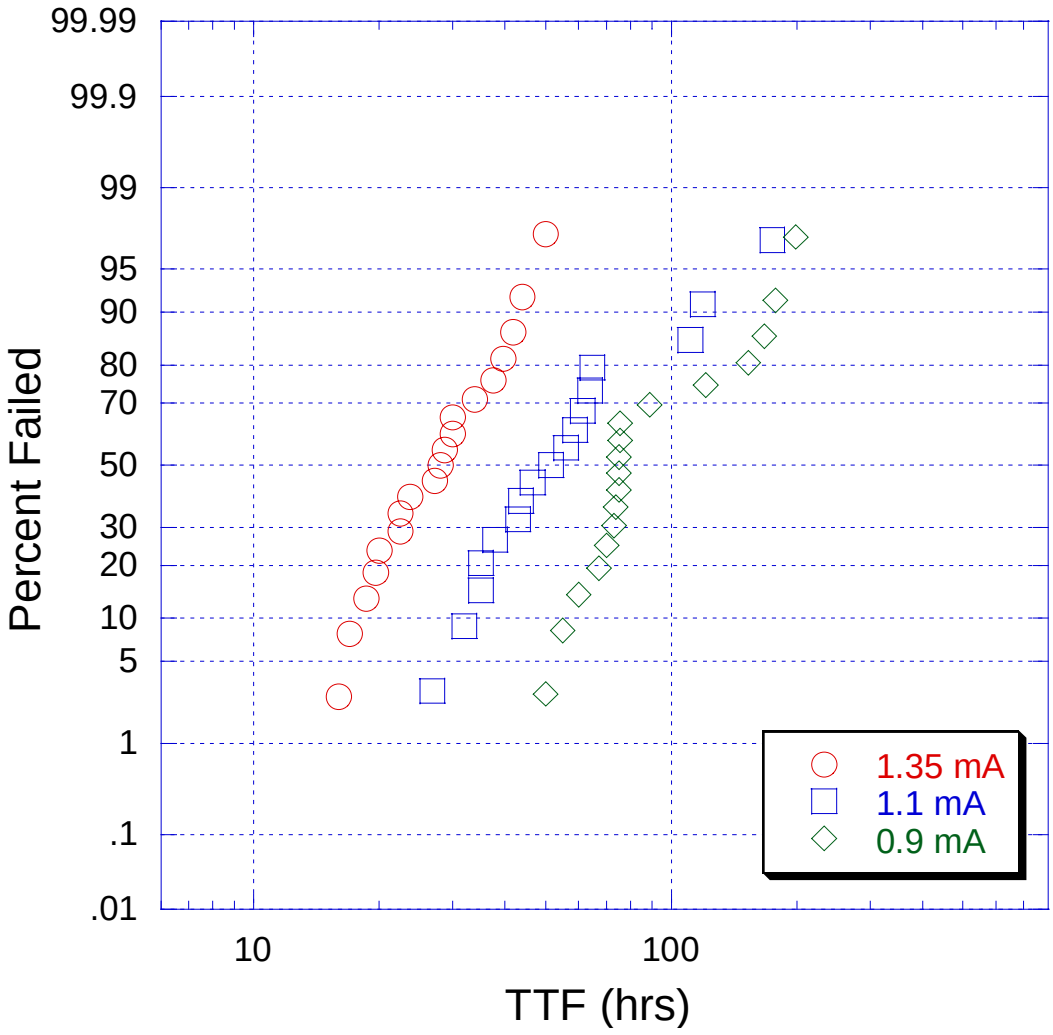


Figure 5.23: The failure distributions of the 25μm structures tested at 350°C with a range of currents.

The results from the second round of tests are summarized in Tables 5.9 and Table 5.10. In these tables the median times to failure and lognormal sigma are shown each of the stressing currents for both the 25 and 50μm structures tested at 350°C. Data from the first round of tests done with a stressing current of

0.67mA are also included. Error bounds that are shown are calculated from the 90% confidence interval of the lognormal fit of the data.

In both cases as the current decreases and the critical length condition is approached the lognormal sigma increases rapidly. Small differences in the geometry, barrier thickness, stress state, and/or grain structure result in differences in the effective bulk modulus, B. As reported by. Hau-Reige the fraction of failed lines will increase monotonically with jl^2/B [21]. When a population of devices under test exhibit a range in B, the result is that some of the interconnects will be immortal. In order to determine the median time to fail the immortal samples are right-censored resulting in misleading sigma values for the lifetime distribution.

Table 5.9 The Median Time to Fail (MTTF) in hours for 50 μm CaM1 structures tested at 350°C with a range of currents.

Current (mA)	$MTTF_{350}$ (hrs)	σ
0.45	97.1 ± 9.4	0.45 ± 0.07
0.67	55.0 ± 7.8	0.44 ± 0.11
0.90	31.5 ± 4.6	0.32 ± 0.10
1.10	20.1 ± 3.0	0.37 ± 0.11

Table 5.10 The Median Time to Fail (MTTF) in hours for 25 μm CaM1 structures tested at 350°C with a range of currents.

Current (mA)	$MTTF_{350}$ (hrs)	σ
0.67	1432.4 ± 1009.9	1.82 ± 1.00
0.90	83.2 ± 12.7	0.32 ± 0.11
1.10	54.7 ± 4.6	0.51 ± 0.16
1.35	29.4 ± 5.2	0.45 ± 0.13

5.2.2 Critical Length Determination

Just as with the first round of tests the inverse of the median time to failure, $MTTF^{-1}$, is used as a measure of the drift velocity. In this case it is plotted against the stressing current. The Cu drift velocity has a linear dependence with the applied current as is shown in Equation 1.4 and as a result it is possible to extrapolate to the zero drift condition in order to determine the precise jl* value. In Figure 5.24 the $MTTF^{-1}$ is shown as a function of stressing current for both the 25 and 50μm structures. The data is fit linearly and the critical current value is calculated. By multiplying the critical current by the structure length, jl* is determined. In Table 5.11 the results from the jl* determination are listed. The error bounds are calculated from the 90% confidence limit of the lognormal fit. These finding are consistent with the findings of other researchers on single inlaid structures using similar methodologies [23,24]. These findings are also similar to those of Lee et. al. using a failure statistics approach to determine the jl* product on dual-inlaid structures [17].

Table 5.11: The critical current density as determined in Figure 5.20, the structure length, and the jl* threshold.

J* (A/cm^2)	Length (μm)	jl* (A/cm)
1.50	25	3800
0.73	50	3800

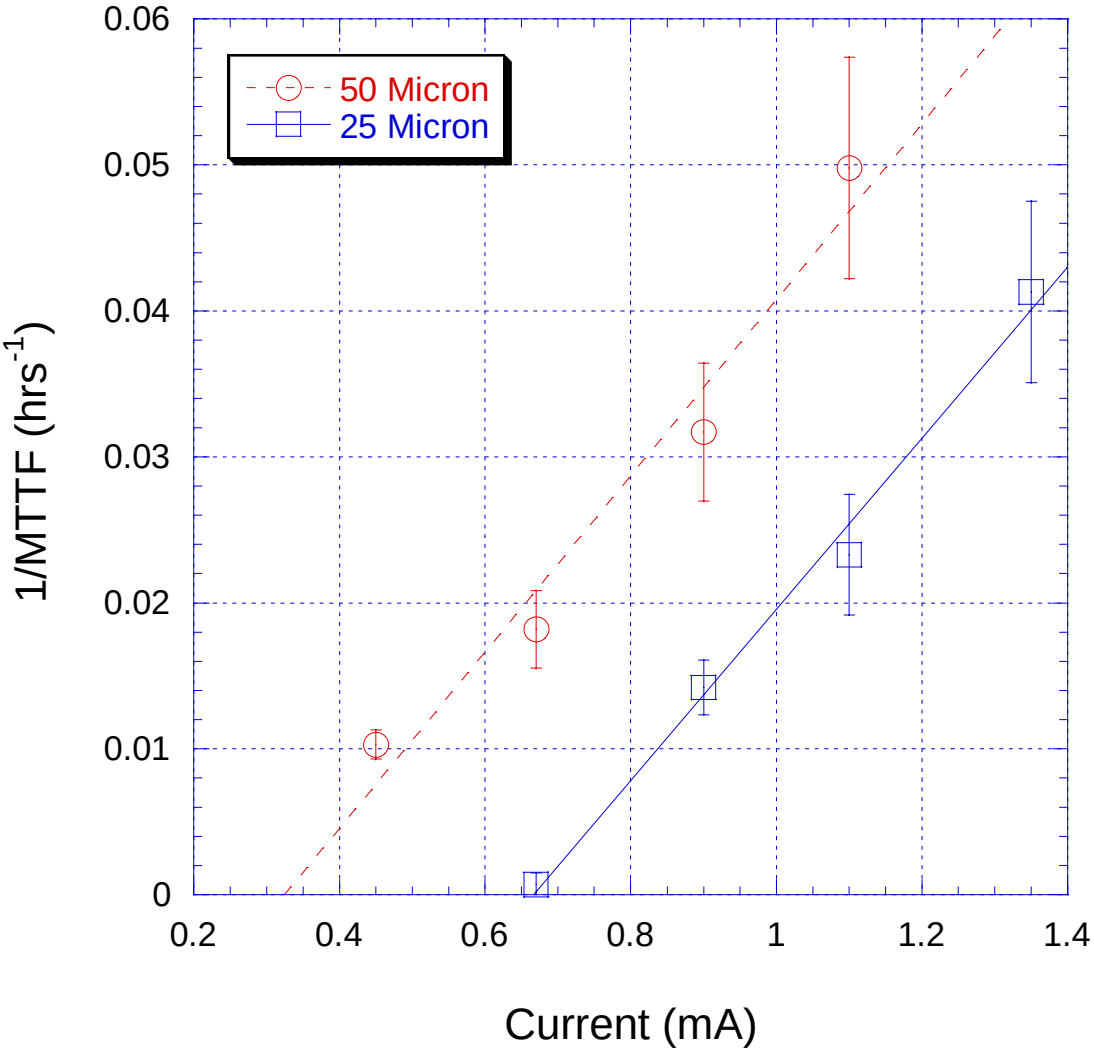


Figure 5.24: The inverse of the median time to failure ($MTTF^{-1}$) plotted against the stressing current.

5.2.3 Current Density Exponent determination

In Figure 5.25 the median time to fail is plotted against the stressing current. The data is fit with power function that is printed on the graph. From Black's Equation as described in Equation 1.10 the median time to failure is

related to the current density by an exponential term. For Al(Cu) alloy interconnects the current density exponent, n, was determined to be approximately 2 [29]. The current density exponent of Cu interconnects is a matter of some divergence. Some findings suggest that it is 2 just as in Al (Cu) but other findings suggest that it is nearly 1. Because Cu interconnects are not alloyed, and do not experience 2-stage EM, so the MTTF should have an inverse relation with the stressing current.

Some recent findings suggest that the current density exponent is larger than 1 because of Joule heating [25]. Global Joule heating in which the entire structure is heated is easy to account for by adjusting the recorded temperature appropriately. Local Joule heating effects would be difficult to account for because the heating would only occur in a small area and possibly only after some voiding has occurred.

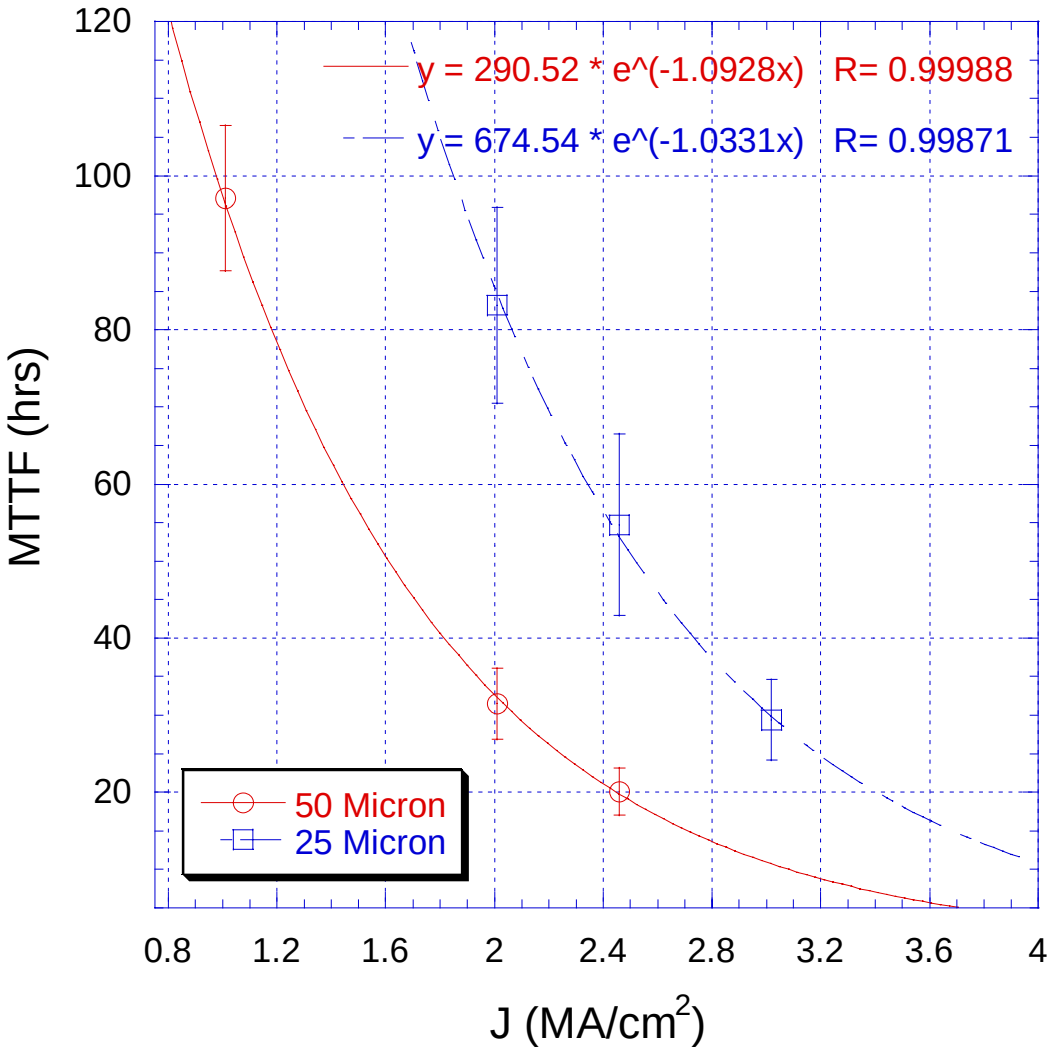


Figure 5.25: The median time to fail plotted against the stressing current density for the 25 and 50µm long test structures. The data is fitted with a power function that is printed on the top of the graph.

Chapter 6: Statistical Analysis of Cu / FTEOS Interconnects

Typical semiconductor products such as processors or memory chips are made from as many as hundreds of millions of discreet devices. In order to link these devices together processors and memory chips will incorporate a complex interconnect structure containing millions of line segments terminating with vias and contacts. If just one of these interconnect structures fails due to EM, the entire semiconductor device can fail. This basic fact has lead to the use of 'weakest-link' [11] statistical analysis methods for EM testing [29]. It is therefore important to model the behavior of a large population of interconnects as opposed to just one or a small sampling.

Typically in EM testing, a relatively small number of individual interconnect segments are tested. These tests are limited in size due to the expense of creating the packaged parts and testing these parts. So as a result, EM tests typically will test between 10 and 30 parts per condition [8,17,25,26]. These results represent just a small sampling of what is a much larger population of interconnects in each semiconductor product. The small sampling of results must be used to accurately gauge the reliability of the entire population, and this is why the use of statistical analysis is critical. In addition, these EM tests are typically done at accelerated conditions to minimize the testing time of the samples. So the results of these tests must also be extrapolated to use conditions as well as made to model the behavior of a large population.

In this study, multi-link test structures were used to enhance the statistical resolution of the EM testing in order to improve the reliability predictions. Multi-link test structures were first used by M. Gall et. al. to further the statistical resolution of EM test on Al(Cu) interconnects [28,29]. Since then, researchers such as, E. T. Ogawa et. al., have demonstrated the use of similar structures and methods to investigate EM failure in Cu interconnects [8]. The use of multi-link structures made it possible to analyze the performance of a large sampling of structures without having to test a large number of test structures. In the following sections the statistical models used to describe EM failure behavior will be reviewed, as well as several aspects of the testing and data analysis methodology will be described. Finally, the results of the EM tests on both single- and dual-inlaid structures will be explored.

6.1 STATISTICS MODELS AND METHODOLOGY

Typically, the lifetime data from EM tests has been fitted with the log-normal distribution. The distribution of EM lifetime data has been repeatedly shown to be best described by the lognormal distribution [30]. The log-normal distribution is essentially a normal distribution of the log of the variable, in this case, the time-to-failure. The normal distribution's probability density function (PDF) can be written as:

$$\text{PDF(x)} = \frac{1}{\sqrt{2\pi}} \exp(-\frac{1}{2} x^2), \tag{6.1}$$

where *x* is the measured variable.

The exponential dependence of interconnect lifetime on temperature results as seen Equation 1.10 results in this lognormal dependence. The probability density function (PDF) of the log-normal distribution can be written as:

$$\text{PDF(t)} = \frac{1}{\sigma t\sqrt{2\pi}} \exp(-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2}), \tag{6.2}$$

where t is the variable time, t_{50} is the median time to failure, and σ is the standard deviation expressed in log-time. The cumulative failure distribution (CFD) is expressed by taking the integral of the PDF from the limits 0 to 1. The CFD can be described as:

$$F(t) = \int_0^t f(u)du = \int_{-\infty}^{z} \frac{1}{(2\pi)^2} \exp(-v^2/2)dv, \qquad (6.3)$$

where $z = \frac{\ln(t) - \ln(t_{50})}{\sigma}$ and t>0. The preceding equations describe statistics of EM failure of a sampling of single interconnect structures with log-normal distribution. Data in the form of a lognormal distribution can be plotted by either its probability density function (PDF) or the cumulative failure distribution (CFD). Typically in engineering work the CFD is preferred because it allows for easy examination of the sigma of the distribution and lognormal fit. In Figure 6.1a we can see a data characterized by a single lognormal distribution plotted by its PDF. In Figure 6.1b the CFD of the same data is shown.

Often the lifetime data obtained through EM experiments shows multiple modes of behavior that can be represented as two overlapping distributions. In Figure 6.2a the PDF of two distributions is shown, one with a median value of 1 and the other with a median value of 10. The same data is shown in a CFD plot in Figure 6.2b. In this CFD plot the early fail tail that is created by the second distribution can clearly be seen as deviating from the trend of the first distribution.

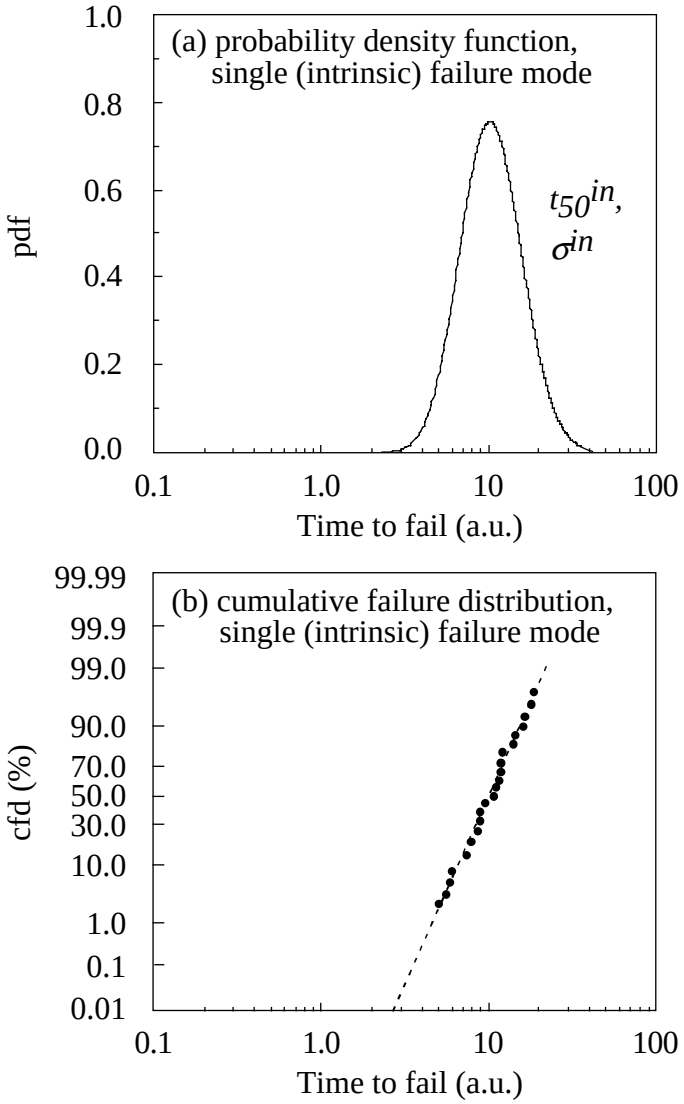


Figure 6.1: (a) A single lognormal probability density function with a f t_{50} of 10. The distribution is centered at 10 and spreads according to it characteristic σ. (b) The cumulative failure distribution (CFD) of the same lognormal distribution. Using the lognormal plot the CFD is straight with a single monomodal distribution.

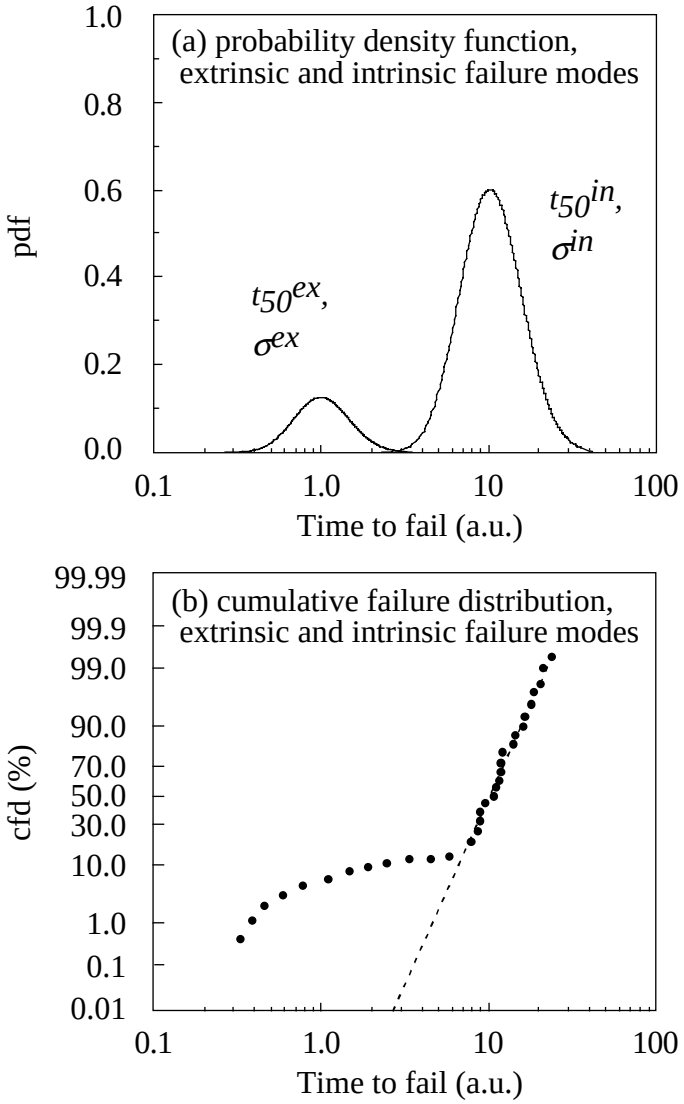


Figure 6.2: (a) Two lognormal probability density functions plotted together. One distribution is the same as shown in Figure 6.1a, the other has a t_{50} of 1 and its own characteristic σ. (b) The cumulative failure distribution (CFD) of the same pair of lognormal distributions. The second mode of failure can clearly be seen by the 'early fail tail it creates.

6.1.1 Monte-Carlo Simulations

Monte-Carlo simulations were conducted in order to demonstrate the utility of statistical analysis using multi-link test structures, and to determine the sensitivity of the technique to detect extrinsic failure populations. A random number generator was used to create lognormal distributions of specific sigmas and median values. In some cases multiple distributions were created and combined to model the behavior of interconnects with multiple EM failure modes. The combined data were then plotted in CFD plots to determine how this multi-modal behavior looks and under what conditions it could be detected.

The behavior of a sampling of X number of single-link EM structures was modeled by a single log-normal distribution of X data points. Each data point signifies the fail time of an EM test structure. In order to model the structure containing 10 and 100 links a more complicated approach is needed. A population of X number of 10-link structure was modeled by creating a lognormal distribution of 10X data points. The data was then grouped into bins of 10 random data points. The lowest value in these bins of 10 was then used to signify the failure time of that 10-link structure. This method is based on the weakest link assumption (WLA) in which the structure lifetime is determined by the weakest link within it. The WLA is often used to model large populations of data such as the case of an actual semiconductor chip in which there are millions of potential failure links. Modeling the behavior of the 100-link structures used the same approach as with the 10-link structures, but in this case the bins consisted of 100 values. Figure 6.3 shows a CFD plot of the simulation of 1, 10, and 100-link

failure time distributions. The distributions of the 10 and 100-link structures are shifted to lower median values and have progressively larger slopes. The 100-link data was limited to only 10 points in this study due to size constraints on the parent distribution. In Figure 6.4 the same data is shown after it deconvoluted so that the failure times of the multi-link structures are shown at the appropriate percentile or number of standard deviations (NSD). Instead of being plotted using lognormal charts the data is plotted according to the number of standard deviations. The 10 and 100 link data extend to lower NSD values reflecting the fact that a large number of actual links were sampled. Both the 10 and 100-link data extend to the same NSD values since both sets of data were obtained from a total of 1000 elements.

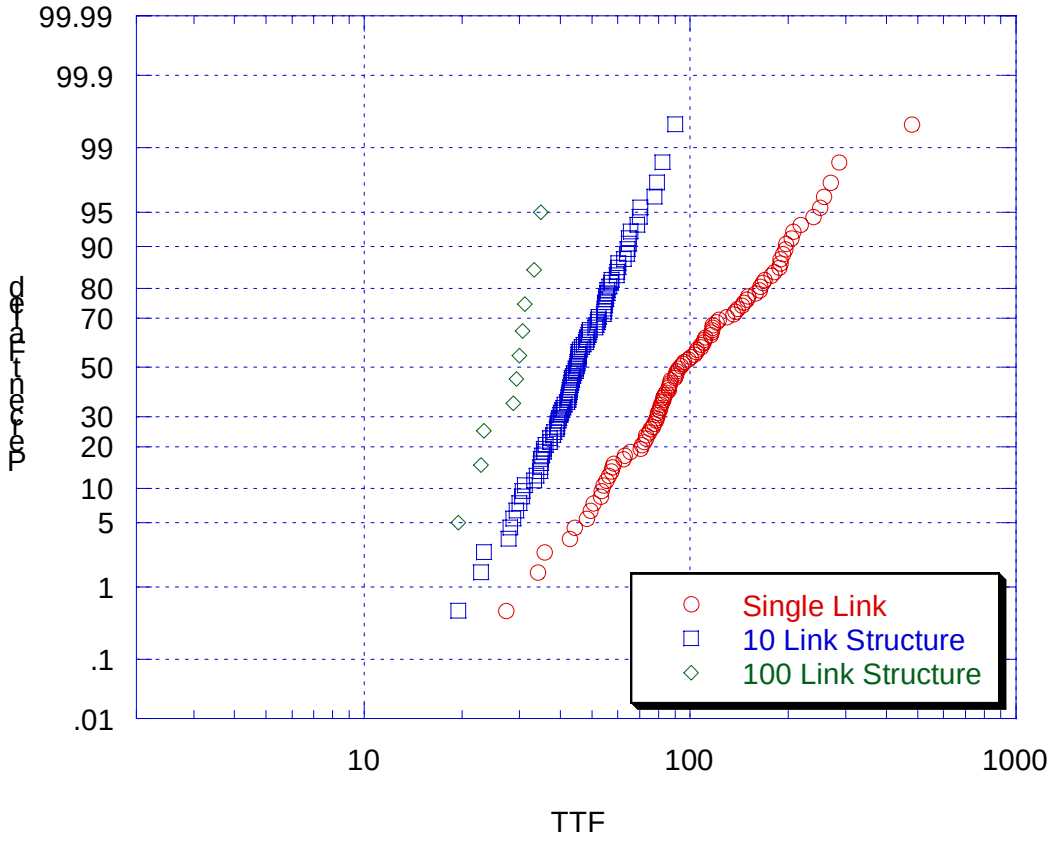

99.99
99.9
99
95
90
80
70
50
30
20
10
5
1
.1
.01
10
100
1000
TTF
Single Link
10 Link Structure
100 Link Structure

Figure 6.3 Monte-Carlo simulation of 1, 10, and 100-link structures failing according to the same lognormal distribution. The median time to failure for the 10 and 100 link structures is low due to weakest link assumption. The apparent sigmas of the distributions also decrease with increased link count.

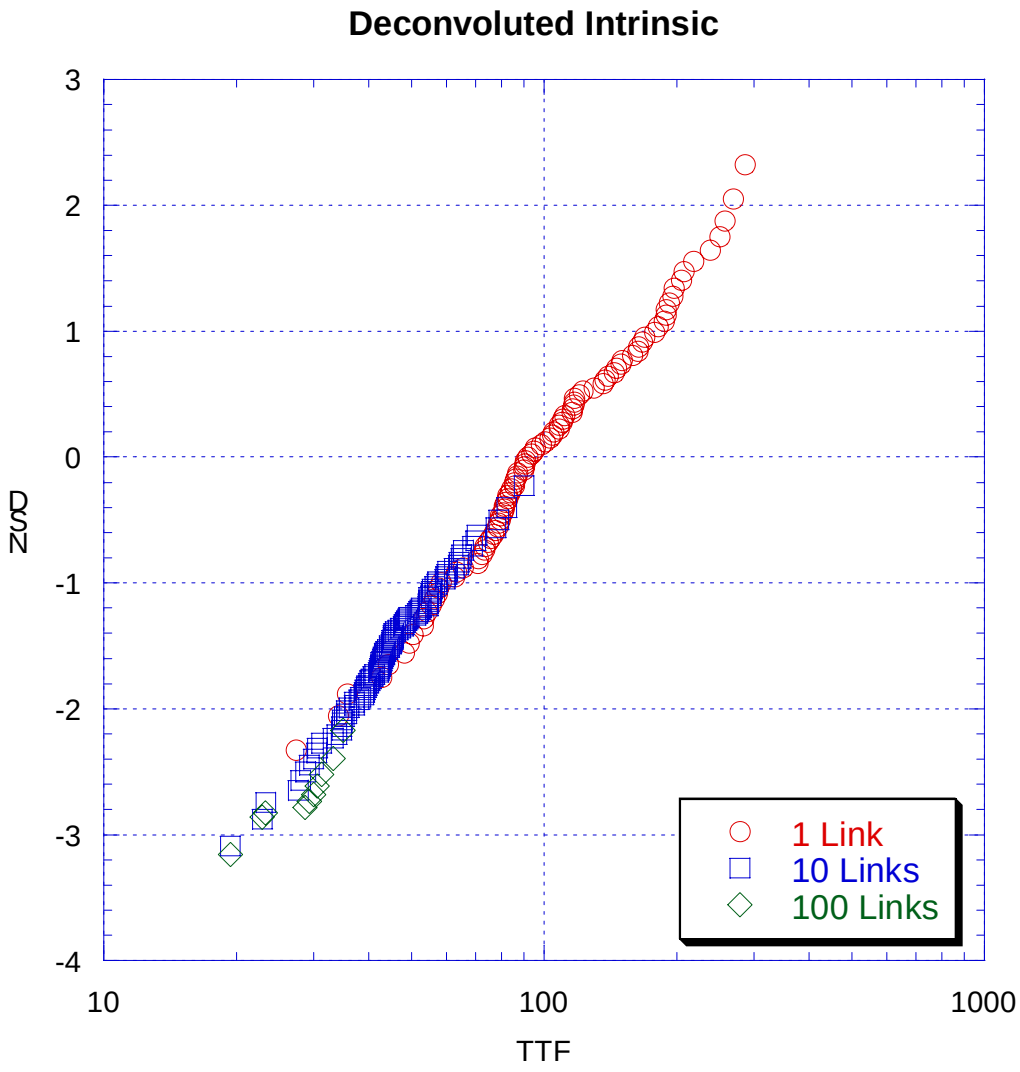


Figure 6.4 Monte-Carlo simulation of 1, 10, and 100-link structures failing according to the same lognormal distribution. The three distributions have been deconvoluted using the weakest link approximation so that they line up.

Simulations were also conducted with multiple distributions. The same initial distribution with median value of 100 was used together with a new distribution with a median value of 10. Both distributions had a sigma of 0.5 for this simulation. In the first case 1% of the intrinsic population was compared to a random value from the extrinsic population. In every case the extrinsic value was the lowest and therefore used to represent the fail time of that structure. In the second case 10% of the values were compared, and in this case almost all of the extrinsic values were used. In Figure 6.5 we can see the results of the 1% early fail rate on the distributions of the 1, 10 and 100 link structures. The early fail population is clearly evident in the 10-link data but not the single link data. With only 10 points it also difficult to detect the early fails in the 100-link data also. In Figure 6.6 the results of the 10% early fail simulation are shown. In this case the early fail population is evident in both the single and 10 link data. Figure 6.7 shows the distributions of 100 link data with 100 points. In this plot it can be seen that the 100-link structures show clear signs of an early fail population at a rate of 1%, and at 10% the distribution is dominated by the extrinsic data. The sensitivity of the various structures to varying early fail population is important to note as even large 100-link structures have limitations on their sensitivity.

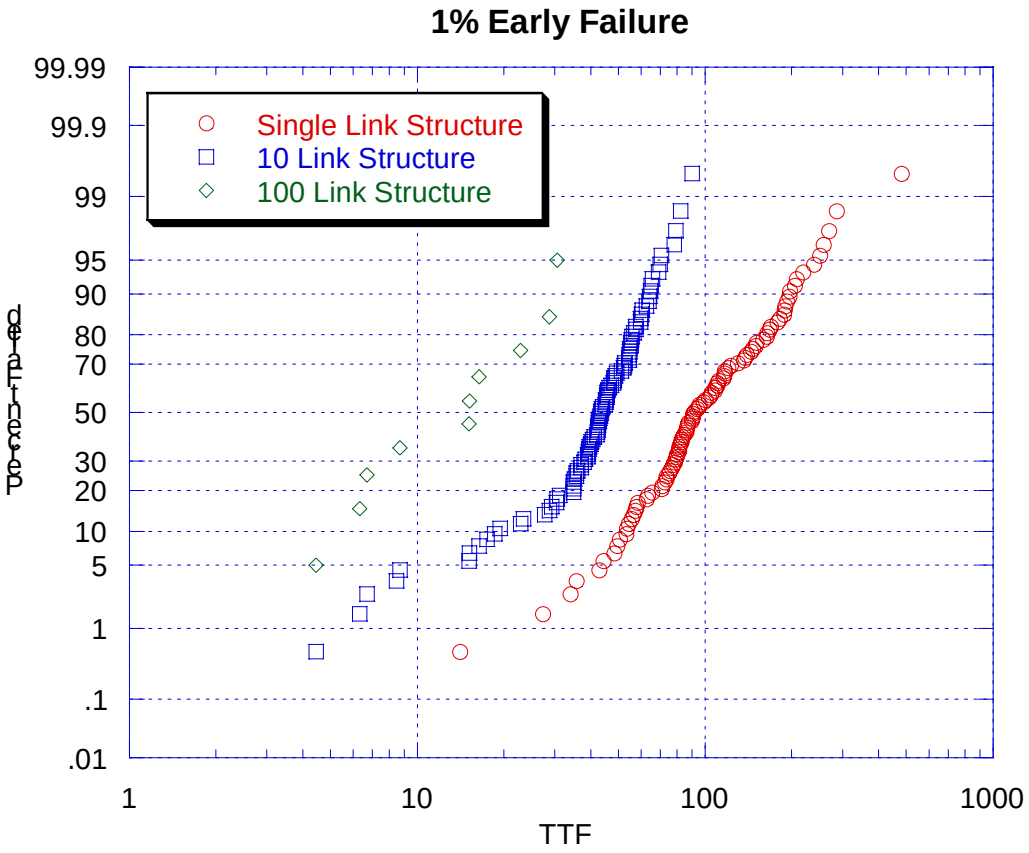


Figure 6.5 Monte-Carlo simulation of 1, 10, and 100-link structures failing according to a combination of two lognormal distributions. The added distribution has a median value of 10, and accounts for 1% of the entire population. The early fail population is not evident in the single link data but is made obvious in the 10-link data by the early fail tail.

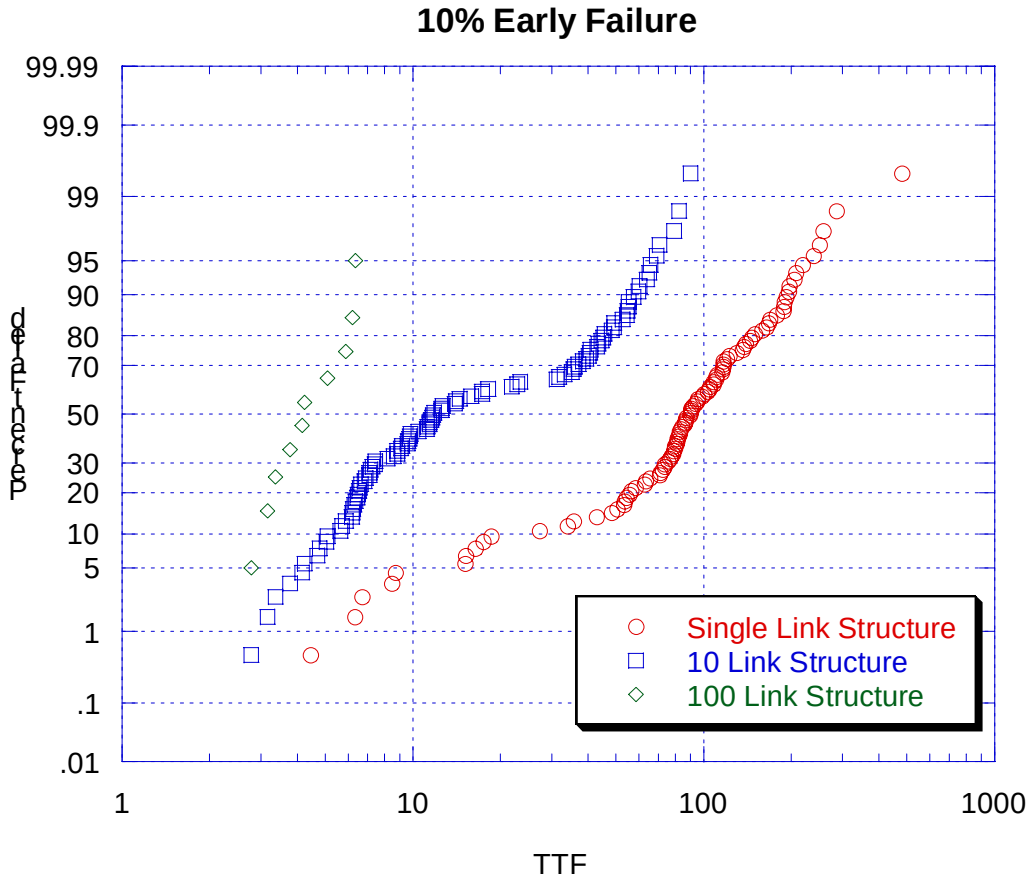


Figure 6.6 Monte-Carlo simulation of 1, 10, and 100-link structures failing according to a combination of two lognormal distributions. The added distribution has a median value of 10, and accounts for 10% of the entire population. The early fail population is now evident in both the 1 and 10-lnk structure, but not in the 100-link structures.

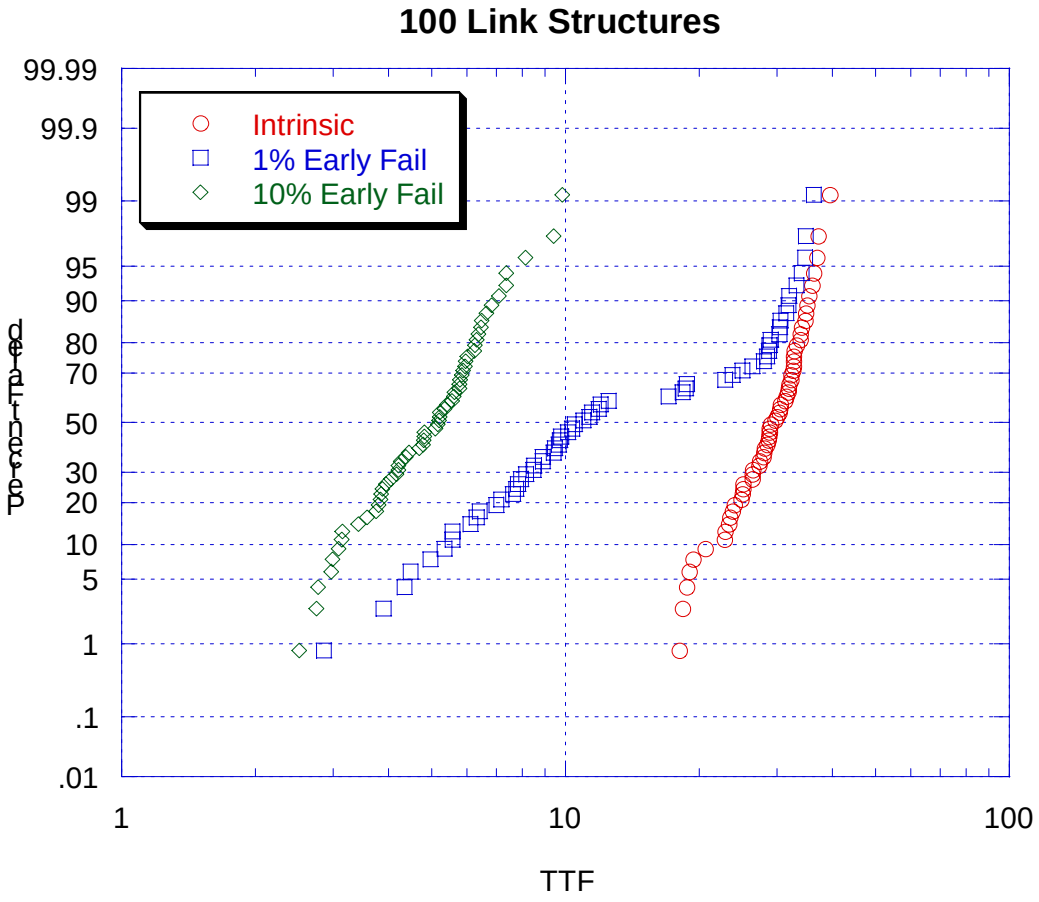


Figure 6.7 Monte-Carlo simulation a larger population of 100-link structures. The additional data makes the trends much more clear. With a 10% early fail population the 100-link structures are only sensitive to the early failures.

6.1.2 Failure Criteria Selection

In order to analyze the data from the multi-link data properly, an appropriate failure criteria must be selected. Typically, in EM testing the time to 10% resistance increase is used as the failure criteria. This works fine when

testing only single link data or when comparing multi-link data from structures containing the same number of elements, but it breaks down when comparing data from structures containing different numbers of elements. The reason for this is that the 10% criterion is insensitive to the amount of ohmic increase found in the samples. 10% resistance increase in a 100 link sample would equate to 100 times the ohmic increase in a single link structure. In order to avoid this situation it is important to use a failure criteria based on a set value of resistance increase. In this study the use of two different failure criteria, a 5-Ohm increase and a time to first resistance increase (TTFI), was investigated. The criteria were selected because they do not scale with the structure size and they are both relatively low. By keeping the resistance level of the failure criteria low potential aberrant behavior found later in resistance traces does not impact the failure distributions. In Figure 6.8 the deconvoluted failure distributions of the V1M2 structures tested at 325^{o}C are shown. In this case the 5 Ohm failure criteria was used and the result is that the alignment of the 1, 10 and 100-link data is not very good. In Figure 6.9 deconvoluted failure distributions of the V1M2 structures tested at 300^{o}C are shown when a TTFI failure criteria is used. The data from the three structures line up extremely well in this case. The difference in the two failure criteria results from the fact that there are often small resistance jumps that occur before catastrophic failure. These jumps are often smaller then 5 ohms and as a result not picked up by the 5 Ohm failure criteria. If the parts consistently failed with a sharp resistance spike any failure criteria could be used with success, but when there are noncatastrophic resistance increases, the TTFI criterion should be used.

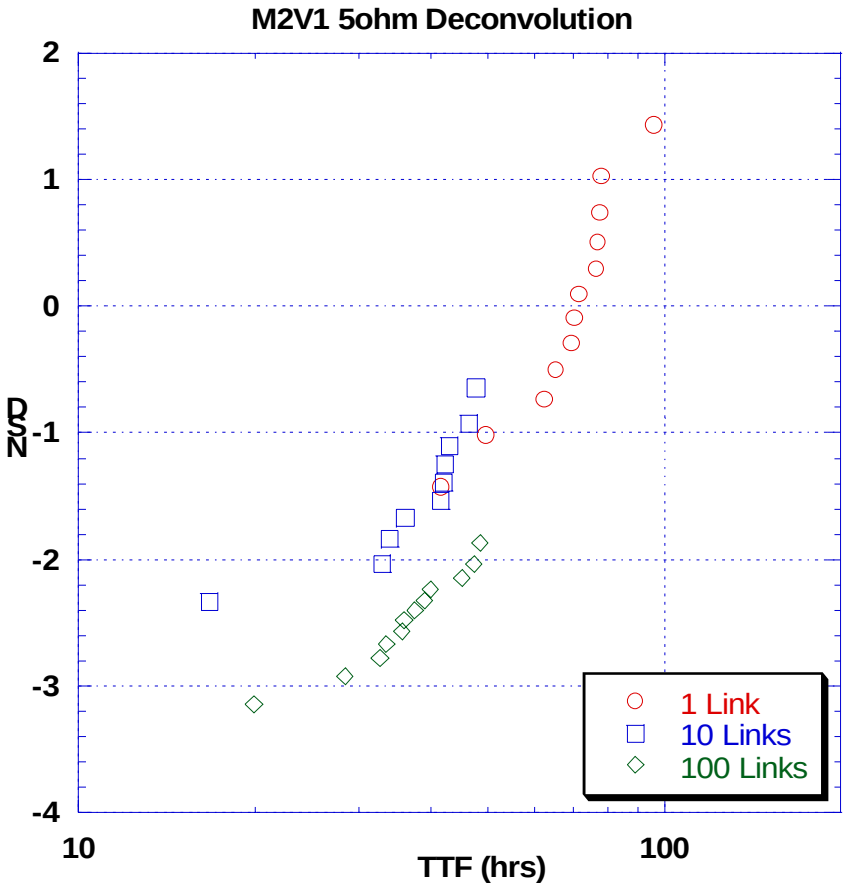


Figure 6.8 Results from a 325 °C V1M2 EM test obtained by using the time to 5% resistance increase failure criteria. The 100 link data is off to the right at higher lifetimes.

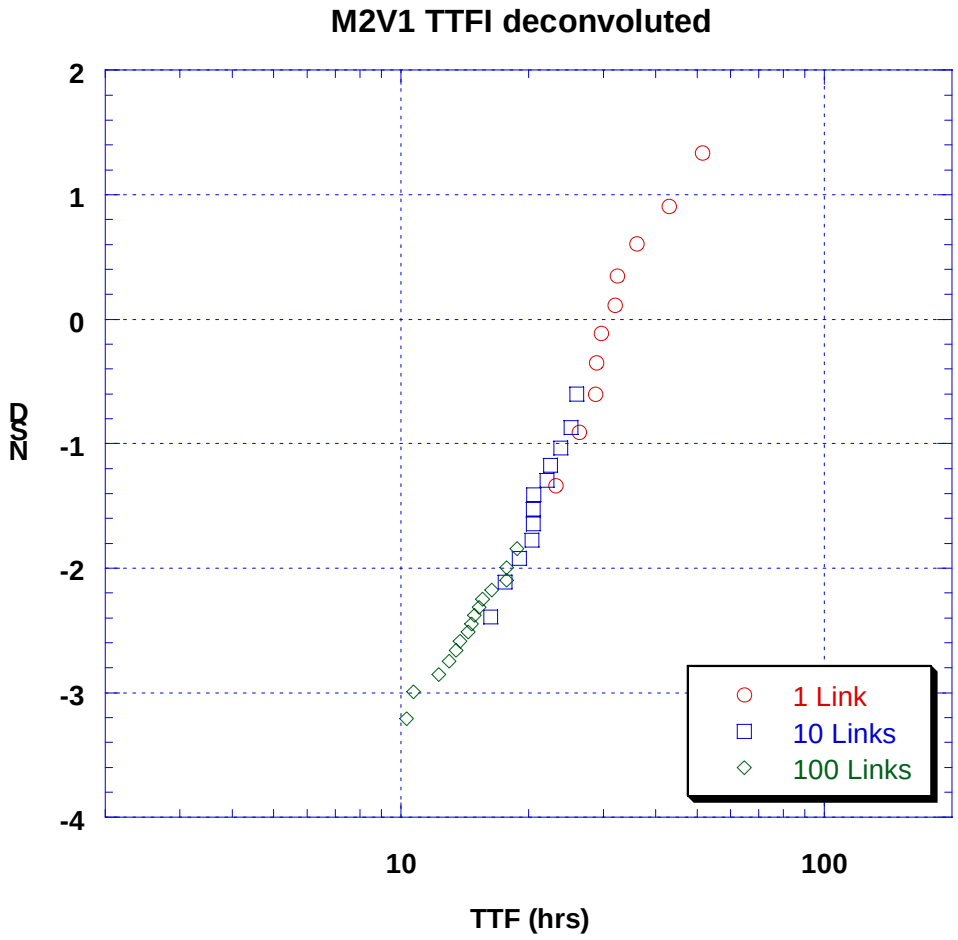


Figure 6.9 Results from a 325 °C V1M2 EM test obtained by using the time to first resistance increase (TTFI) failure criteria. In this case the data from each of the three structures line up very well.

The resistance traces of the multi-link structures often show multiple distinct failure 'events' in the form of sharp resistance jumps. The times of these resistance jumps can be used to represent the failure of multiple elements within the structure. In Figure 6.10 a few resistance traces of a single link structure are shown. In these traces the resistance remains stable until the DUT fails with a

sudden resistance spike. In Figure 6.11 a couple of resistance traces from a 10-link structure are shown. In this case the resistance stays constant until the resistance jumps anywhere from 50 to 100Ohms. Then a short time later another similar jump occurs. This process continued until it reaches a 30% resistance increase. At this value the test system shuts off the applied current preserving the structure for failure analysis. In Figure 6.12 a similar process is seen for the 100 link structures but in this case many more jumps are seen before the samples reach the 30% mark.

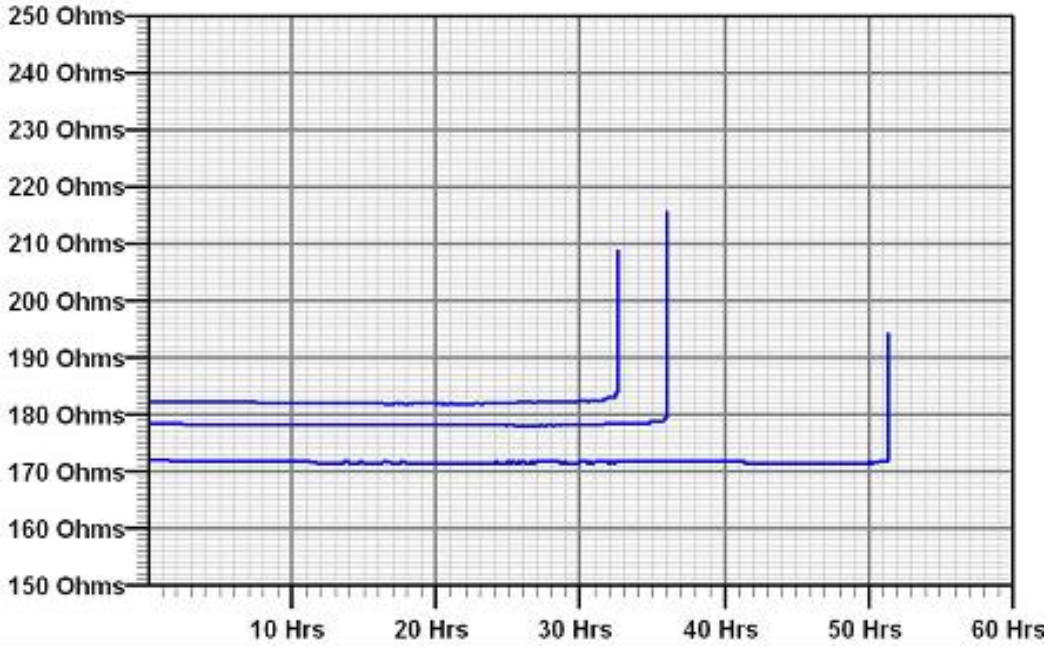


Figure 6.10 Resistance traces from V1M2 single link structures tested at 300C with an applied current of 0.67mA. The resistance of the DUTs remains roughly constant until the parts fail with an abrupt resistance spike.

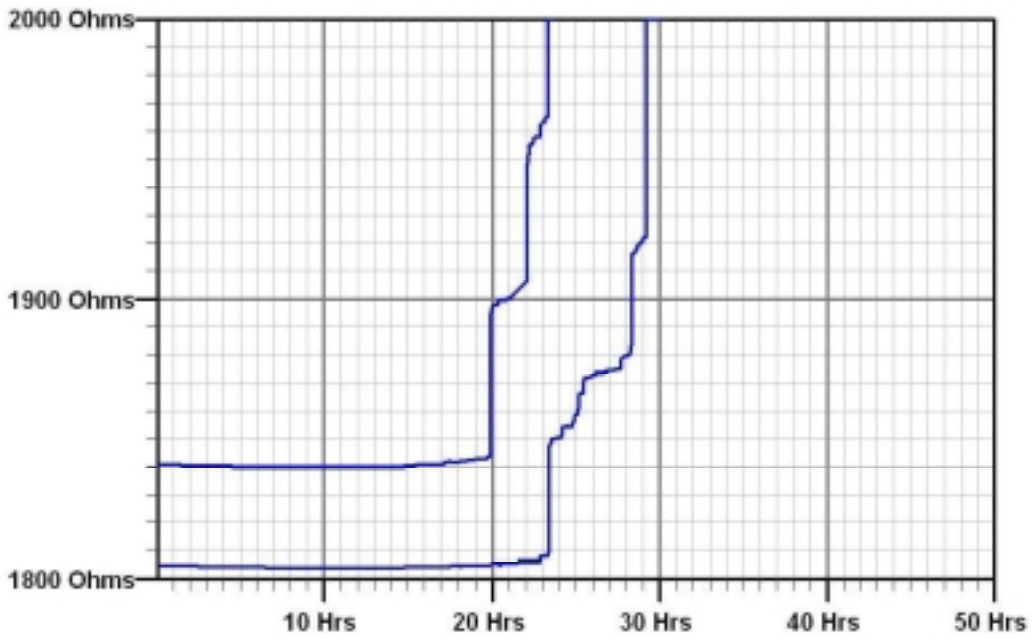


Figure 6.11 Resistance traces from V1M2 10-link structures tested at 300C with an applied current of 0.67mA. Like the previous example the resistance of the DUTs remains roughly constant until the parts fail with an abrupt resistance jump of about 50 Ohms. A short time later, additional resistance jumps can be seen.

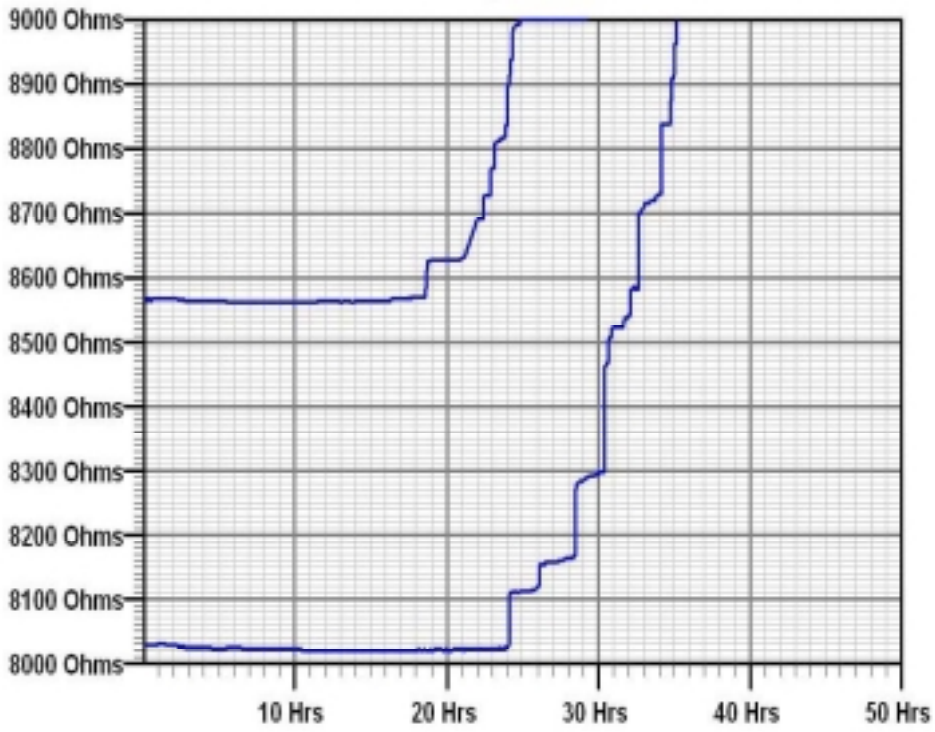


Figure 6.12 Resistance traces from V1M2 100-link structures tested at 300 ^{o}C with an applied current of 0.67mA. These structures behave similarly to the 10-link structures but have many more resistance jumps.

By recording the times of each of these resistance jumps it is possible to measure not just the fail time of the weakest link, but additional links as well. Typically two or three fail times were recorded for each 10-link structure and any where from 2 to 5 times recorded for the 100 link structures. The additional data points were employed in a censored data approach. For each multi-link structure the recorded fail times are used and the remaining number of elements are right-censored. The data censoring is based on a maximum likelihood analysis (MLA) method that is used to fit the distributions. The failure times of the subsets of

interconnects such as the 100 links in a particular structure can then be estimated by the fail time of the structure itself. The result of the analysis is very similar to the results obtained form the weakest link approach. This censored data approach is very sensitive to the small number of fail times recorded and can be thrown wildly off by any unusual data or uncensored data. As a result the multiple fail times were only used selectively when the resistance trace was unambiguous and clearly showed consecutive resistance jumps. This was done to avoid a situation in which a failure jump was taken to be the third element failing but in reality was the trace from the forth or fifth element to fail. The results of this situation would be to artificially shift the distribution to later times. When collected carefully the additional data increases the uncensored data count and allows for better extrapolations to use conditions by tightening the statistical confidence bounds.

6.2 STATISTICAL ANALYSIS OF SINGLE-INLAID INTERCONNECTS

Electromigration testing and data analysis were conducted using the methodologies described in the preceding sections on interconnect structures made with a single-inlaid process. The single inlaid process results in an encapsulated via that is resistant to electromigration behavior. The EM testing on both sides of the via with V1M1 test structures to test the lower interface and V1M2 structures to test the upper interface. As reported in Chapter 4, it is expected that the diffusion and hence the electromigration of these structures will likely occur and therefore be controlled by the upper interface. By using the multi-link structure the statistical sensitivity is improved so that additional failure modes might be identified.

6.2.1 V1M1 Experimental Results

The V1M1 multi-link structures were tested in much the same way as the single link structures described in Chapter 4 under two of different conditions. The length of the metal segments studied in this chapter was 150μm as opposed to the 250μm long structures described earlier. The difference in length is not expected to affect the EM behavior of the structures as both values are well above the critical length of 25μm with a current density of 1.5MA/cm^2. As seen in section 4.3 the EM activation energy and drift rate will not be affected by the difference in length.

The other significant difference in the testing is the failure criteria used. Earlier a 10% resistance criterion was used in order to facilitate fast data collection. In this case a time to first resistance increase criteria, which has been demonstrated to be appropriate for Cu EM [8], was used. This was done in order to address the fact that many samples have small resistance steps before the larger resistance jumps that indicate failure. Single link structures rarely show these jumps, but they are common in the 100 link structures. In order to get the 1, 10, and 100 link failure distributions to align, the resistance increase onset criteria was chosen.

The V1M1 tests structures were tested at three temperatures, 300, 325, and 350^{o}C in order to obtain an activation energy as well as to study the failure distributions at different temperatures. A single stressing current if 0.67mA, or 1.5MA/cm^2 was used for all of the testing. In Figure 6.13 the failure distributions of the combined 1, 10, and 100 link structures are shown at the three testing temperatures. The three distributions are separated equally suggesting that the activation energy is constant in this range of temperatures. The 300^{o}C distribution has some deviation from lognormal behavior at high failure times. This deviation is also reflected in Figure 6.14, which depicts a lognormal plot of the standardized residuals. Overall, the data is fit well by the lognormal and do not indicate any additional failure mechanisms or bimodal behavior. In this figure the number of recorded fail times, 196, and the number of censored data points, 4986, are indicated.

In Figure 6.15 an Arrhenius plot of the same data is shown. A good spread in the distributions at the different temperatures indicating a reasonable high value of activation energy.

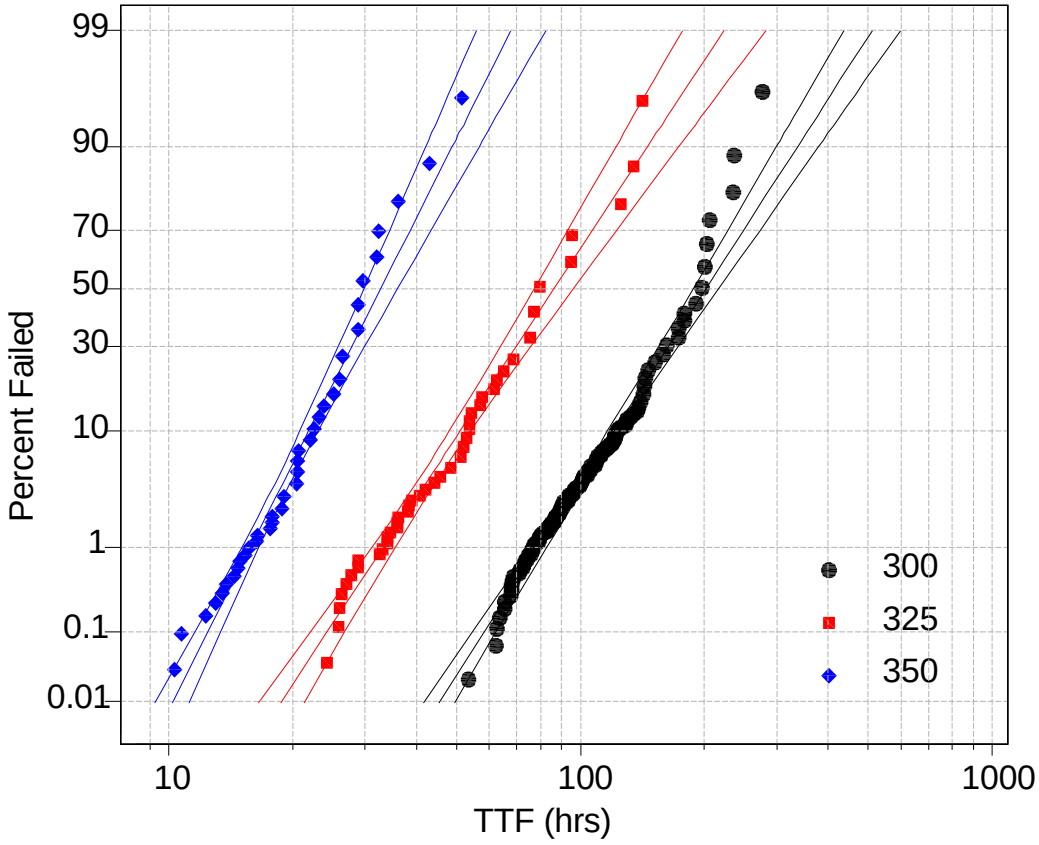


Figure 6.13 Failure distributions of the 1, 10, and 100-link V1M1 structures tested in a range of temperatures from 300 to 350C. The distributions are fitted and bounded by 90% confidence intervals.

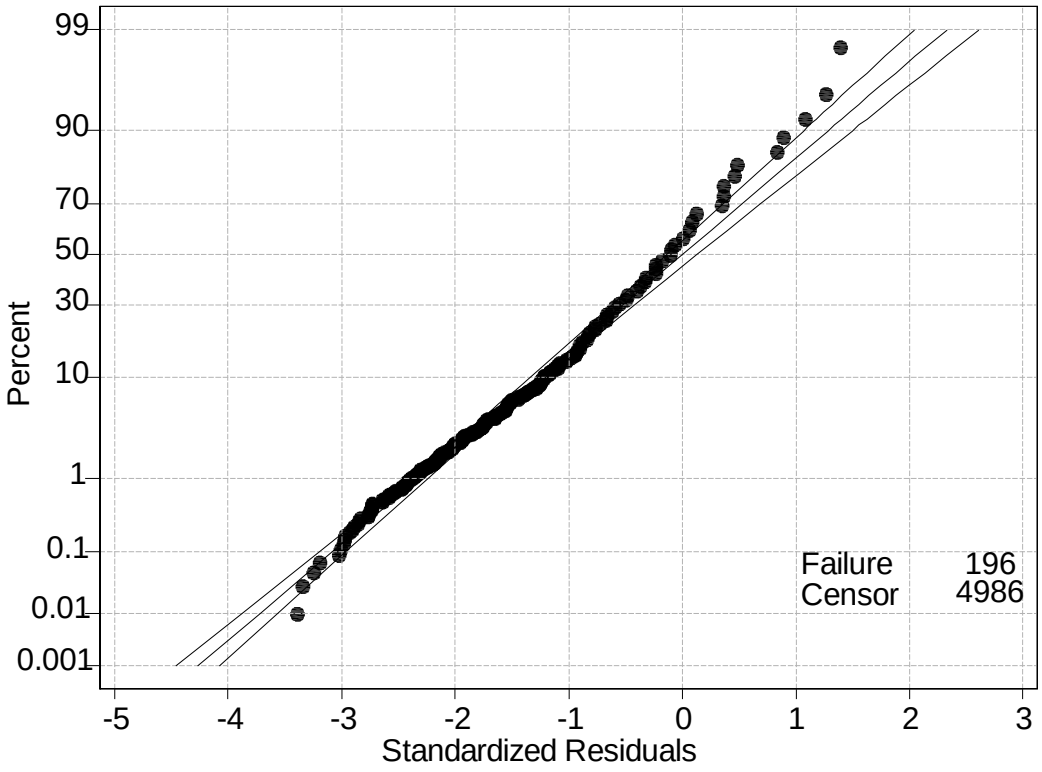


Figure 6.14: A plot of the distribution of standardized residuals for the lognormal fit of the 1, 10, and 100-link V1M1 structures tested in a range of temperatures from 300 to 350C. The plot indicates that the lognormal distribution fits the data well. The data is based on 196 measured data points and 4986 censored data points.

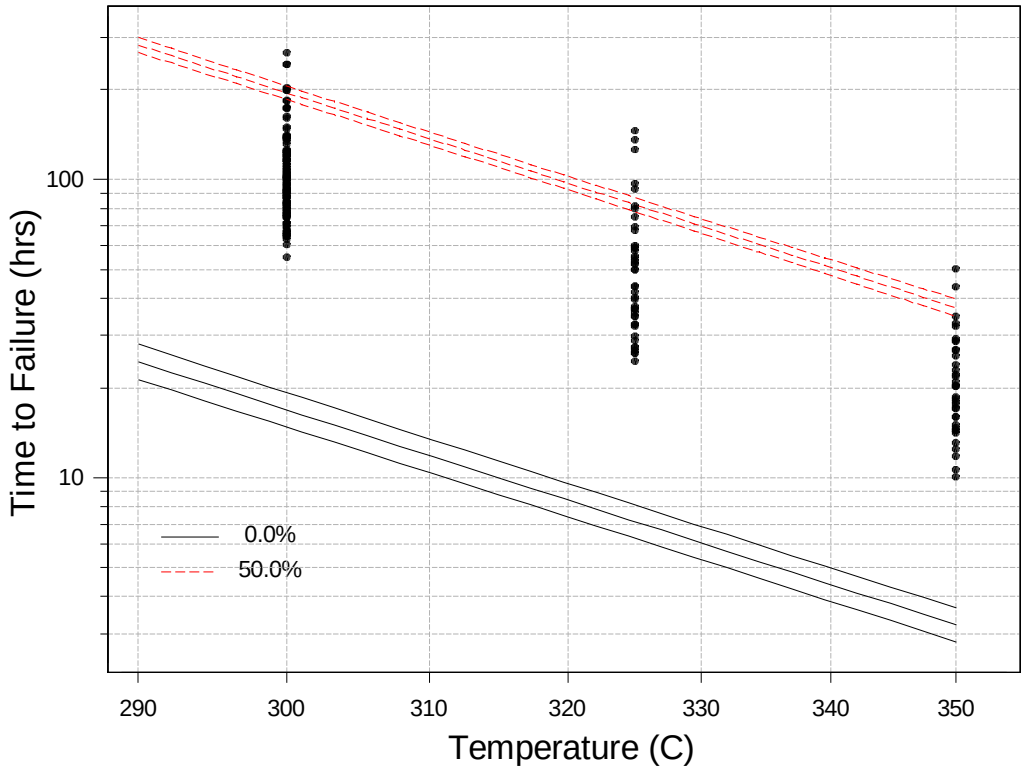


Figure 6.15: An Arrhenius plot of the 1, 10, and 100-link V1M1 structure fail times tested in a range of temperatures from 300 to 350C. The data is fitted based on the MTTF of the distributions. The data extends well below the median (50%) value due to the censored data included in the analysis. The Arrhenius fit based on the first failure in 1 million samples (0.000001% value) is also shown below.

Table 6.1 The activation energy and lognormal sigma calculated form the V1M1 results described above. The error rate is also listed for both the E_a and σ in terms of ± value. The median times to fail (MTTF) of the single link structures for the three testing temperature are also listed.

E_a (eV)	Lognormal σ	$MTTF_{300}$ (hrs)	$MTTF_{325}$ (hrs)	$MTTF_{350}$ (hrs)
1.02 ± 0.04	0.38 ± 0.03	146.0	75.5	27.1

Failure analysis was conducted on all selected samples using the techniques described in the failure analysis section of the experimental techniques chapter. In Figures 6.16 through 6.18 SEM micrographs of 10-link V1M1 structures tested at 325^{o}C are shown. In Figure 6.16 the layout of the structure with the short M2 connecting link is shown. In Figure 6.17 a collage of vias in a 10-link structure that failed relatively early are shown. These were the only voids found in the 10 links of this structure. The void shape is the same as was seen in the single link results from the previous chapter. The sloping void front indicates that the Cu - Si_3N_4 interface is where the diffusion takes place. Figure 6.18 shows all 10 links of a structure that failed relatively late. Because the structure was stressed for a long time all of the links had time to form voids. The cells of this collage are arranged in order of the degree of void formation.

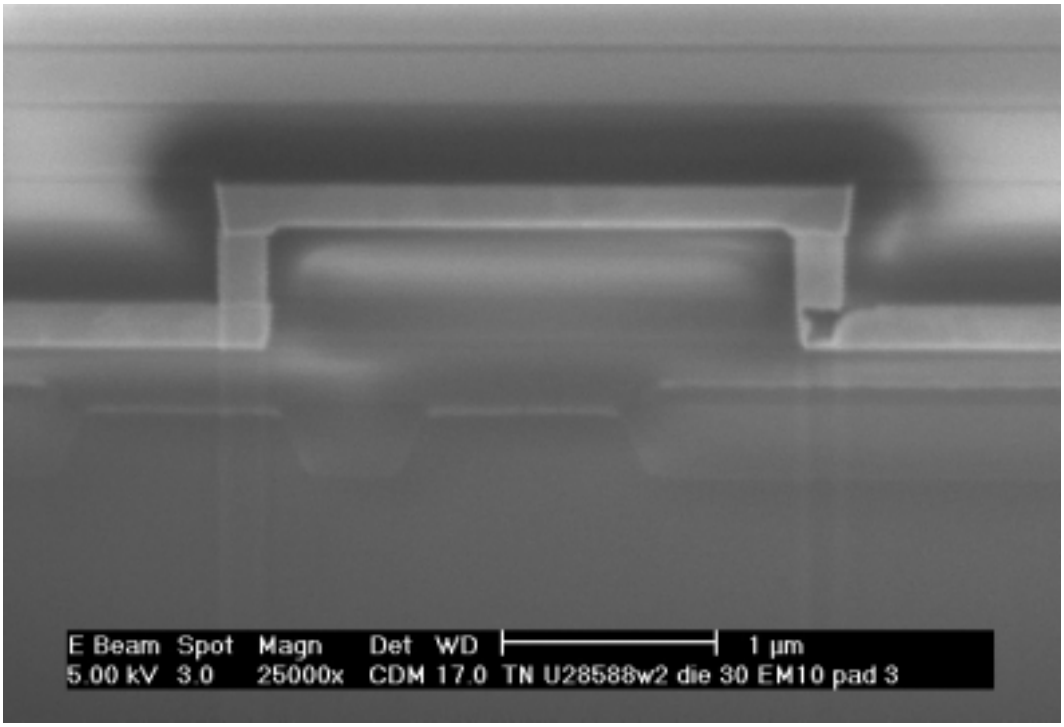


Figure 6.16 SEM micrograph showing the cross section of part of a 10-link V1M1 test structures after EM testing at 300C. A short Metal –1 connecting line is seen in the center. The void is one of three similar voids found in this structure.

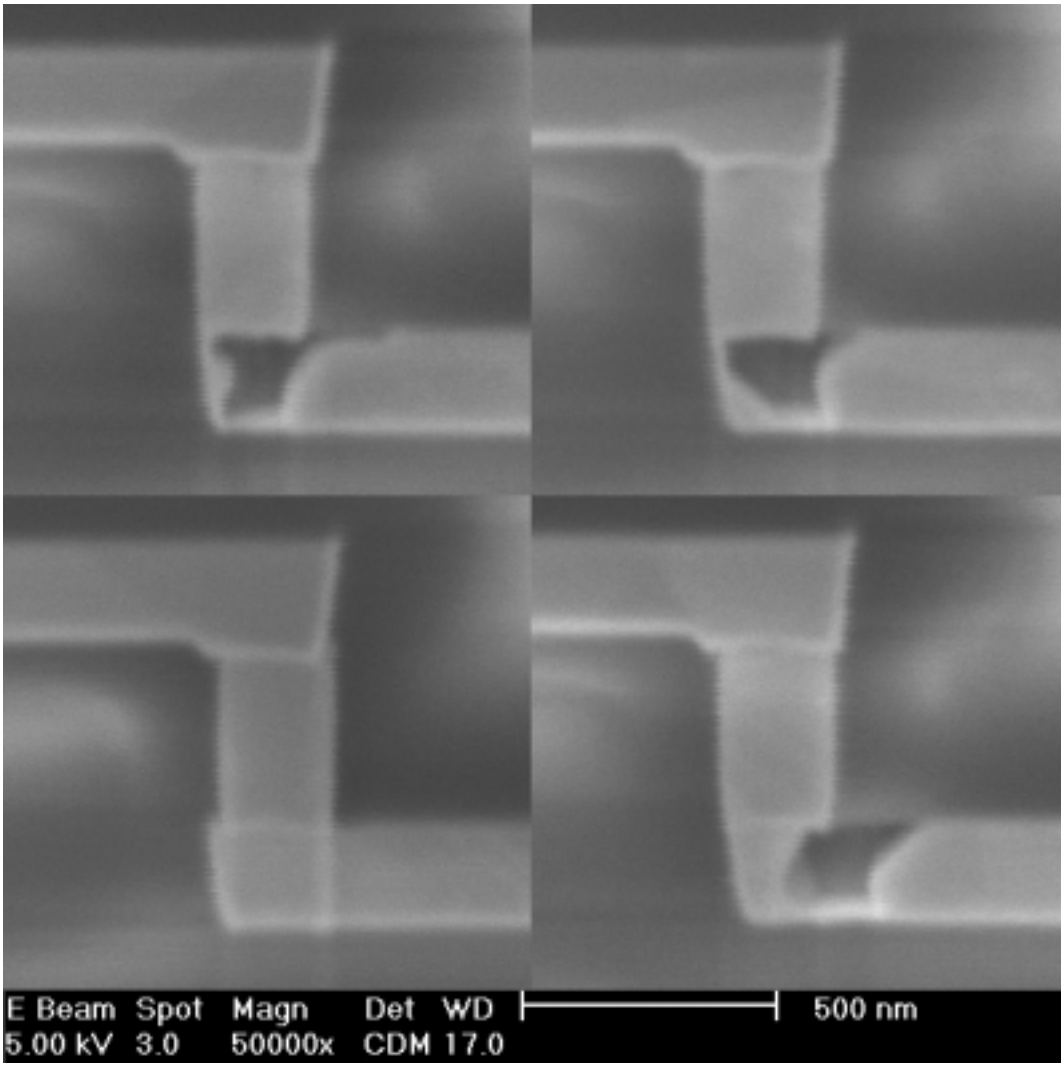


Figure 6.17 Collage of 4 SEM micrographs showing cross-sections of individual links in a 10-link V1M1 test structures after EM testing at 300C. The void shown in the upper left is the same as in Figure 6.21. Only two other voids were found in this structure and both are similar to the one shown prior.

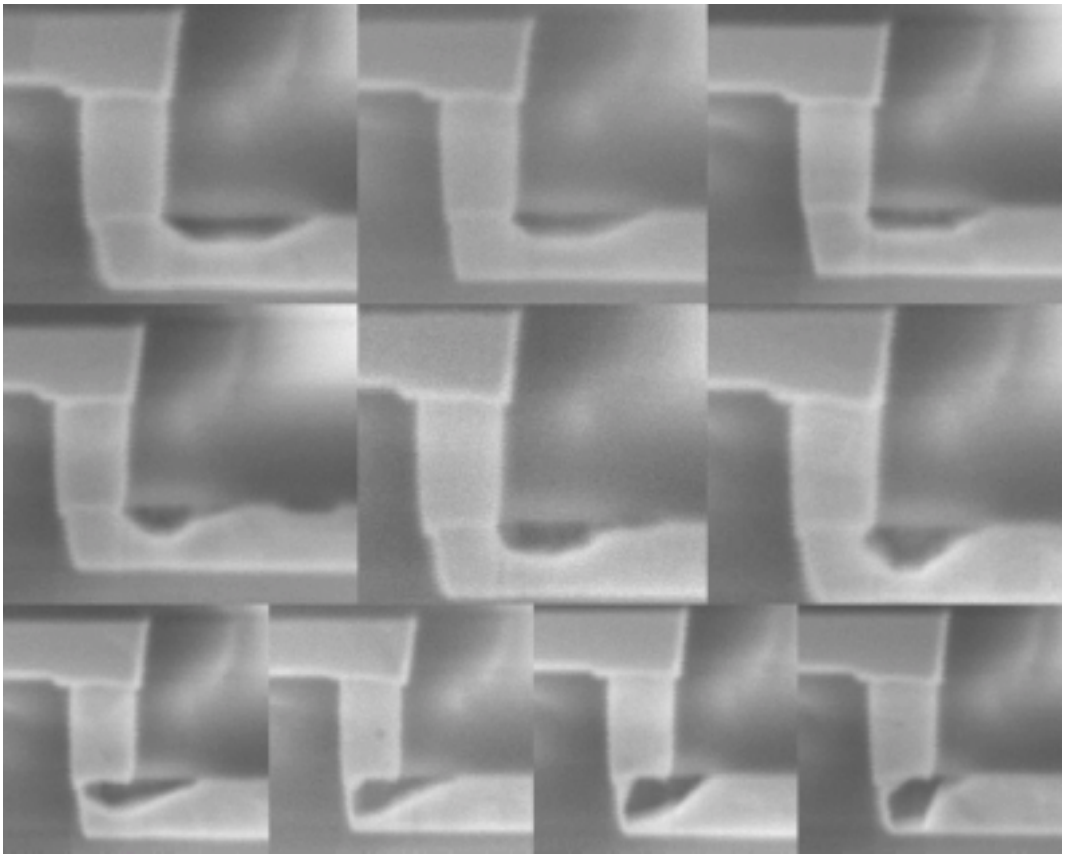


Figure 6.18 A second collage of all 10 SEM micrographs showing cross-sections of individual links in a 10-link V1M1 test structures after EM testing at 300 ^{o}C. The images are placed in order according to the void growth process.

6.2.2 V1M2 Experimental Results

The EM testing of the V1M2 multi-link structures was done in the same way as the V1M1 structures were. The results are also laid-out in much the same way. In Figure 6.19 the failure distributions of the combined 1, 10, and 100 link structures are shown at the three testing temperatures. As with the V1M1 structures the three distributions are separated equally suggesting that the

activation energy is constant in this range of temperatures. Unlike the V1M1 case the failure time distributions are not all linear on the lognormal plot. The 350 ^{o}C data does have a good lognormal fit, but both the 300 and 325 ^{o}C data have clear early fail tails. The 325^{o}C data also forms what appear to be three distinct groups. Each one of these groups are made up of data from one of the three structure types. The data on the right (longer lifetimes) is from the single link structures, the data in the middle is from the 10-link structures, and the low lifetime data to the left, including the early fail tail is from the 100-link structures. In this case the failure analysis reported later did not show a clear reason for the early fail distributions seen in the V1M2 structures. In Figure 6.20 a lognormal plot of the standardized residuals of the V1M2 failure time distributions is shown. The early fail tail seen in the 325 and 300 ^{o}C data before can clearly be seen here as well.

In Figure 6.21 an Arrhenius plot of the same data is shown. A good spread in the distributions at the different temperatures indicating a reasonably high value of activation energy.

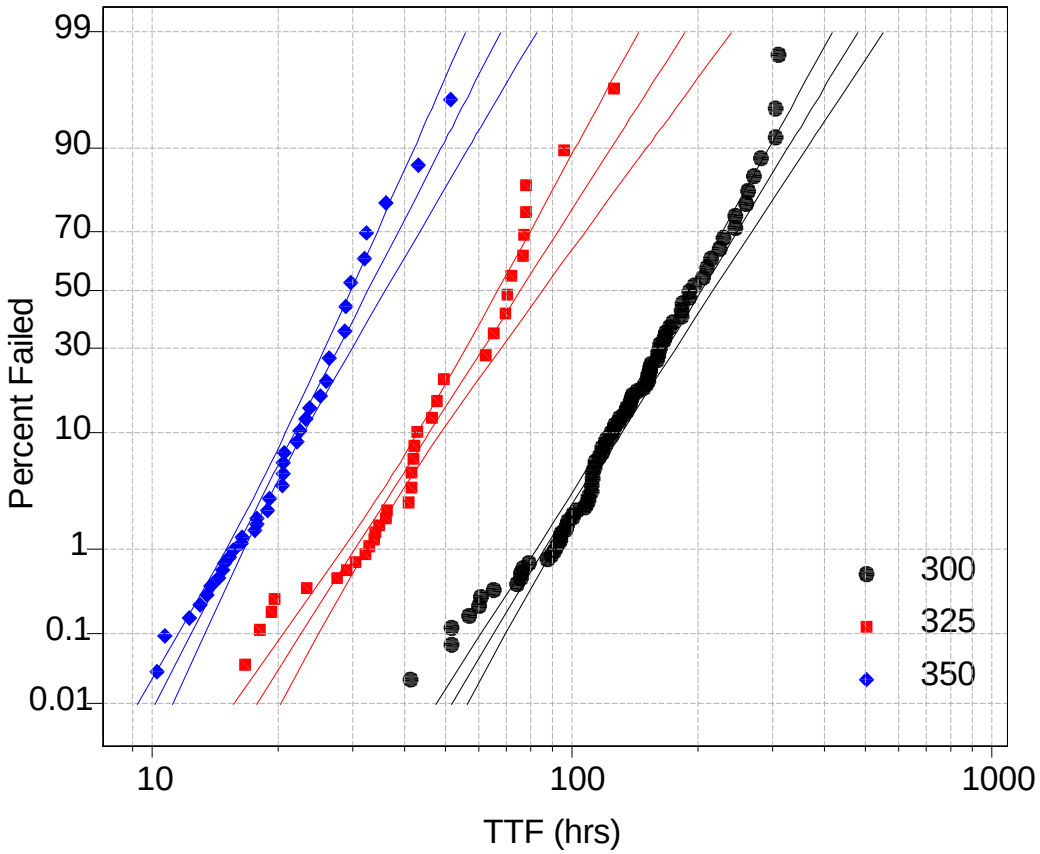


Figure 6.19 Failure distributions of the 1, 10, and 100-link V1M2 structures tested in a range of temperatures from 300 to 350 °C. The distributions are fitted and bounded by 90% confidence intervals. The 300 and 325 °C data show some deviation from log normal behavior.

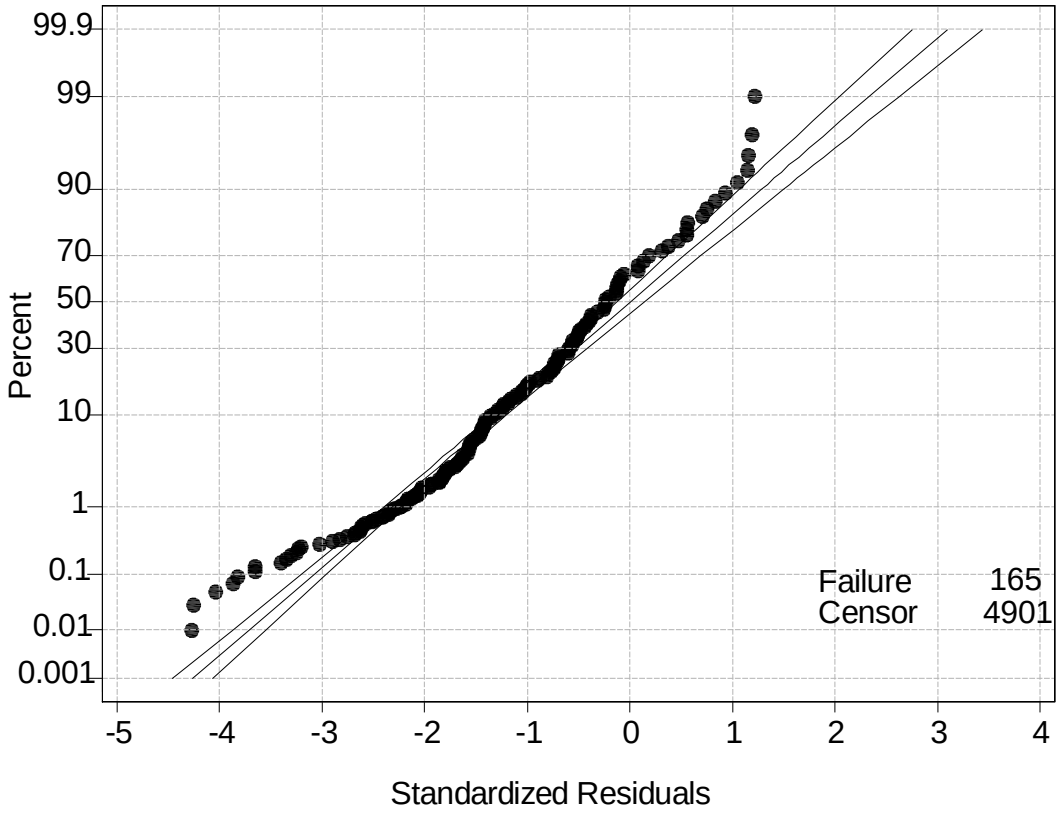


Figure 6.20 A plot of the distribution standardized residuals for the lognormal fit of the 1, 10, and 100-link V1M2 structures tested in a range of temperatures from 300 to 350 ^{o}C. The plot indicates that the lognormal distribution fits the central portion of the data well. At both low and high percentages the data deviates from lognormal behavior. The data is based on 165 measured data points and 4901 censored data points.

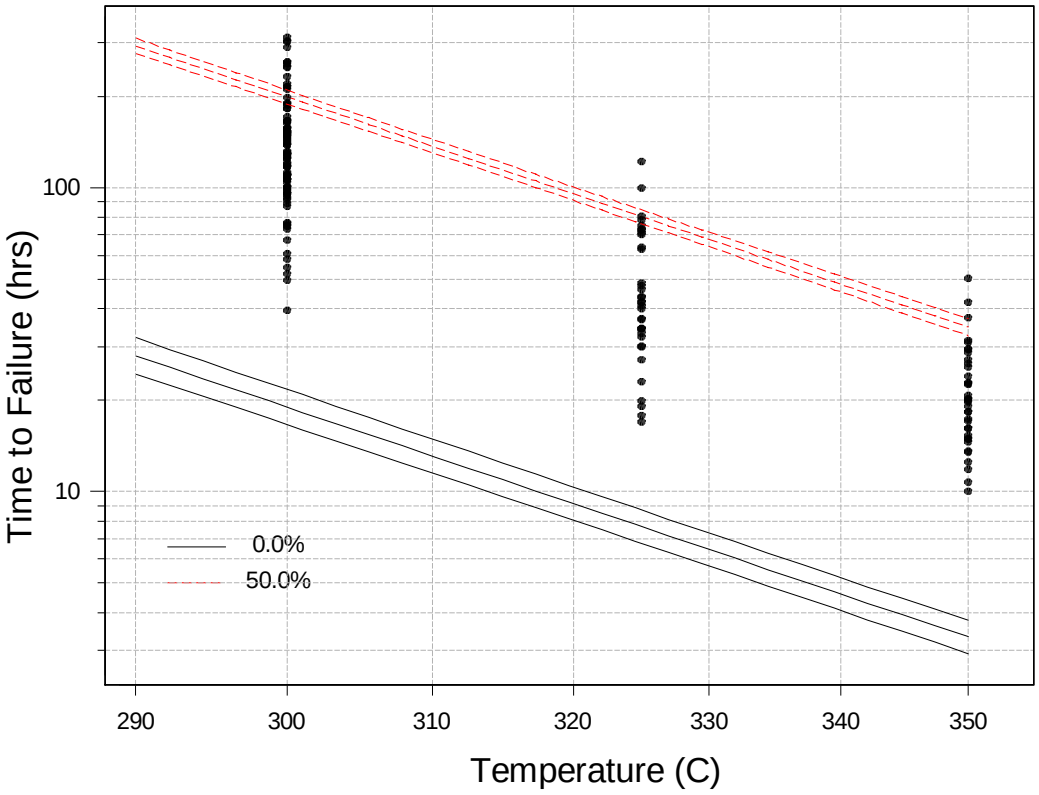


Figure 6.21 An Arrhenius plot of the 1, 10, and 100-link V1M2 structure fail times tested in a range of temperatures from 300 to 350 °C. The data is fitted based on the MTTF of the distributions. The data extends well below the median (50%) value due to the censored data included in the analysis. The Arrhenius fit based on the first failure in 1 million samples (0.000001% value) is also shown below.

Table 6.2 The activation energy and lognormal sigma calculated form the results described above. The error rate is also listed for both the E_a and σ in terms of ± value. The median times to fail (MTTF) of the single link structures for the three testing temperature are also listed.

E_a (eV)	Lognormal σ	$MTTF_{300}$ (hrs)	$MTTF_{325}$ (hrs)	$MTTF_{350}$ (hrs)
1.07 ± 0.04	0.37 ± 0.03	213.9	71.6	30.9

Failure analysis was conducted on selected samples using the techniques described in the failure analysis section of the experimental techniques chapter. In Figures 6.20 and 6.21 SEM micrographs of 10-link V1M2 structures tested at 325^{o}C are shown. In Figure 6.20 the layout of the structure with the short M2 connecting link is shown. In Figure 6.21 a collage of vias in a 10-link structure that failed relatively early are shown. The failures in this case are similar to those found for the basic structures tested in the previous chapter. Both critical voids that span the via region and non-critical voids that form along the top interface were found. The non-critical voids show a large amount of voiding along the Cu – Si_3N_4 interface that dues not significantly impact the resistance of the structure. Failure analysis of the 100-link structures that exhibited early fail times was also conducted. Unfortunately, the failure analysis could only be conducted on a small fraction (10%) of the 100-links and as a result did not show any unusual failure mechanism.

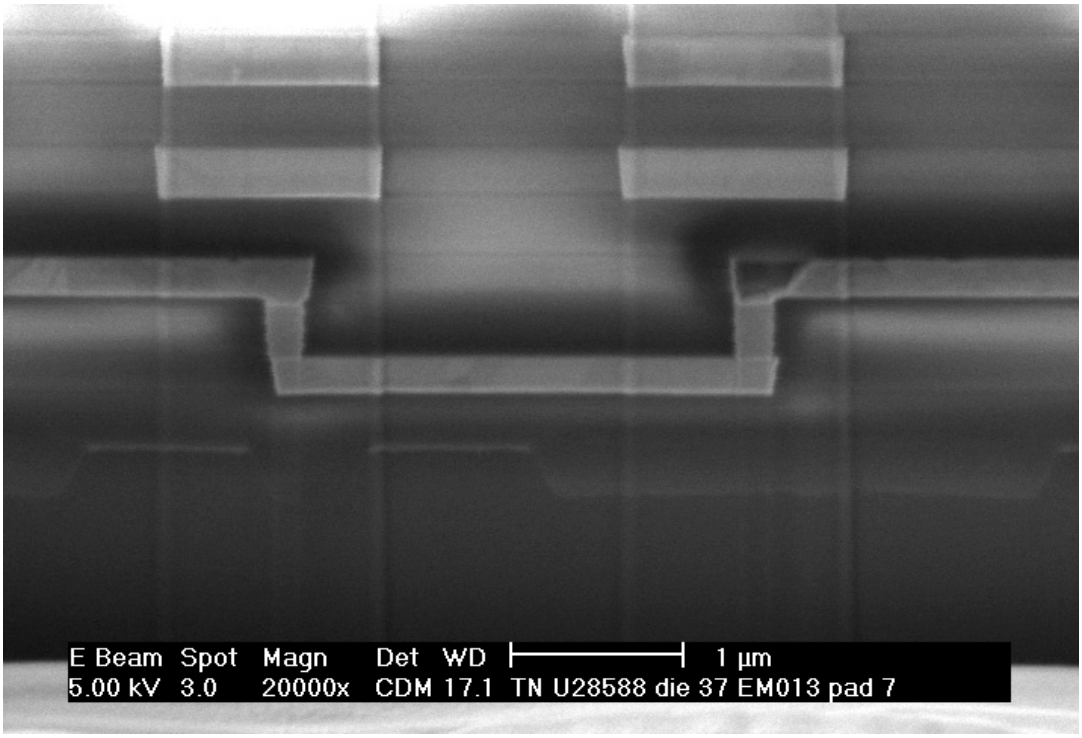


Figure 6.20 SEM micrograph showing the cross section of part of a 10-link V1M2 test structures after EM testing at 325 ^{o}C. A short Metal –1 connecting line is seen in the center. The void on the right has likely caused the failure of the structure.

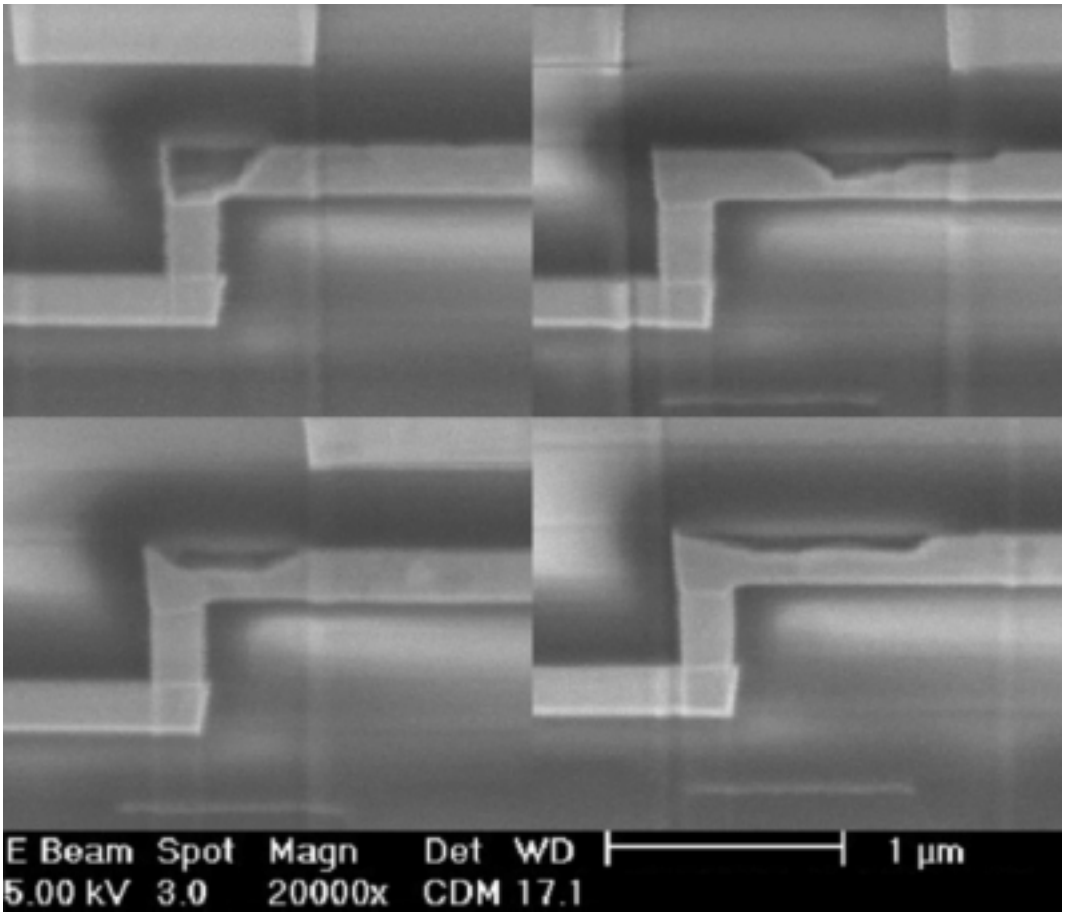


Figure 6.21 Collage of 4 SEM micrographs showing cross-sections of individual links in a 10-link V1M2 test structures after EM testing at 325 ^{o}C. The void shown in the upper left is the same as in Figure 6.19. The other three voids do not seem to be fatal and are likely indicative of the voiding on the remaining six segments.

6.3 STATISTICAL ANALYSIS OF DUAL-INLAID INTERCONNECTS

Electromigration testing and data analysis were conducted using the methodologies described in the preceding sections on interconnect structures made with a dual-inlaid process. Unlike the single-inlaid process, the dual-inlaid process results in a via that is continuous with the metal line and results in a via that is susceptible to EM damage formation.

6.3.1 Bimodal Behavior

In Figure 6.22 a schematic is shown depicting the potential voiding sites associated with a single- and dual-inlaid via. In the single-inlaid via the voiding is confined to the metal line above the via, just as in the results of the previous sections have shown for the V1/M2 interface. In the dual-inlaid via voids can potentially form in the via as well as in the trench. The void formation in the via has been shown to occur primarily at the bottom of the via [8, 31, 32] where the presence of the diffusion barrier creates a mass flux divergence point. The additional failure mechanism can complicate the statistical methods used to make reliability predictions based on accelerated testing of a small population of interconnects. The additional failure mechanism can result in two competing modes of failure that result in net distributions that are better described as a bimodal or separated and treated as separate log-normal distributions.

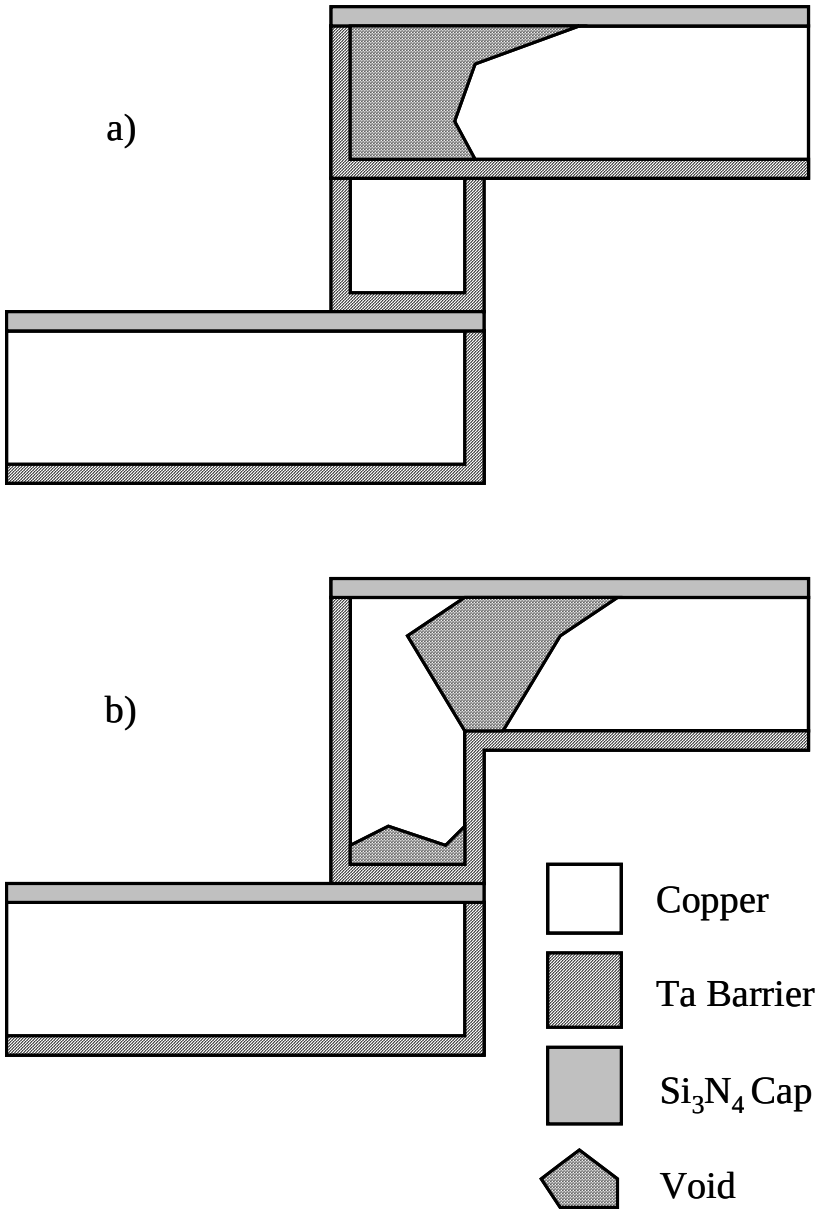


Figure 6.22: (a) A schematic depicting the potential failure location in single-inlaid V1M2 interface. (b) A schematic depicting the potential failure locations in a dual-inlaid V1M2 structure.

6.3.2 Experimental Results

The EM experiments reported in this section were done in the same way as the previous, Single-Inlaid, section. EM tests were done at three temperatures, 300, 325 and 350^{o}C in order to determine the activation energy, E_a. Three different structures containing 100, 10, or 1 links were used for greater statistical sensitivity. The physical dimensions of the metal line and via are larger for these V3M4 structures. A slightly larger current, 0.89mA, was required to meet 1.5MA/cm^2 current density. In this case the EM testing was done only on the dual-inlaid V3M4 interface and was not done on the V3M3 because the dual inlaid process is not expected to affect the EM performance of the lower interface.

In Figure 6.23 the failure distributions of the combined 1, 10, and 100 link structures are shown at the three testing temperatures. The failure times and appropriate percentiles of the multi-link structures are addressed in the same manner as the single-inlaid structures described in the previous sections. A single fail time was recorded for each of these structures and the rest of the links were treated as right-censored data from the single fail time. Maximum likelihood analysis of the censored data produced the failure distributions seen in Figures 6.23 and 6.24.

The failure distributions of the dual-inlaid structures all show significant early fail tails that extend beyond the 10th percentile. The presence of the early fail tail is indicative of a second mode of failure that is responsible for the lower portion of the distributions. As other researchers have done, the two failure

mechanisms, or modes of failure, will be referred to as the 'strong' mode and the 'weak' mode. The strong mode refers to the upper portion of the distributions and the weak mode refers to the mode responsible for the lower portion of the distributions. The spacing of both the top and bottom portions of the distributions are all spaced roughly equally suggesting that the activation energy for the strong mode and weak mode are similar.

In Figure 6.24 a lognormal plot of the standardized residuals of the pooled time to failure distributions is shown. The early fail tail seen in Figure 6.23 can also clearly be seen here too extending to the left at lower percentiles. The large censored data count of 6628 data points is a result of the maximum likelihood analysis done using right censored data points. The number of actual recorded lifetimes is only 234 which equals the number of samples tested in this study. A small jog in the data can be seen at the 8^{th} percentile which reflects similar data seen in each of the three separate failure distributions.

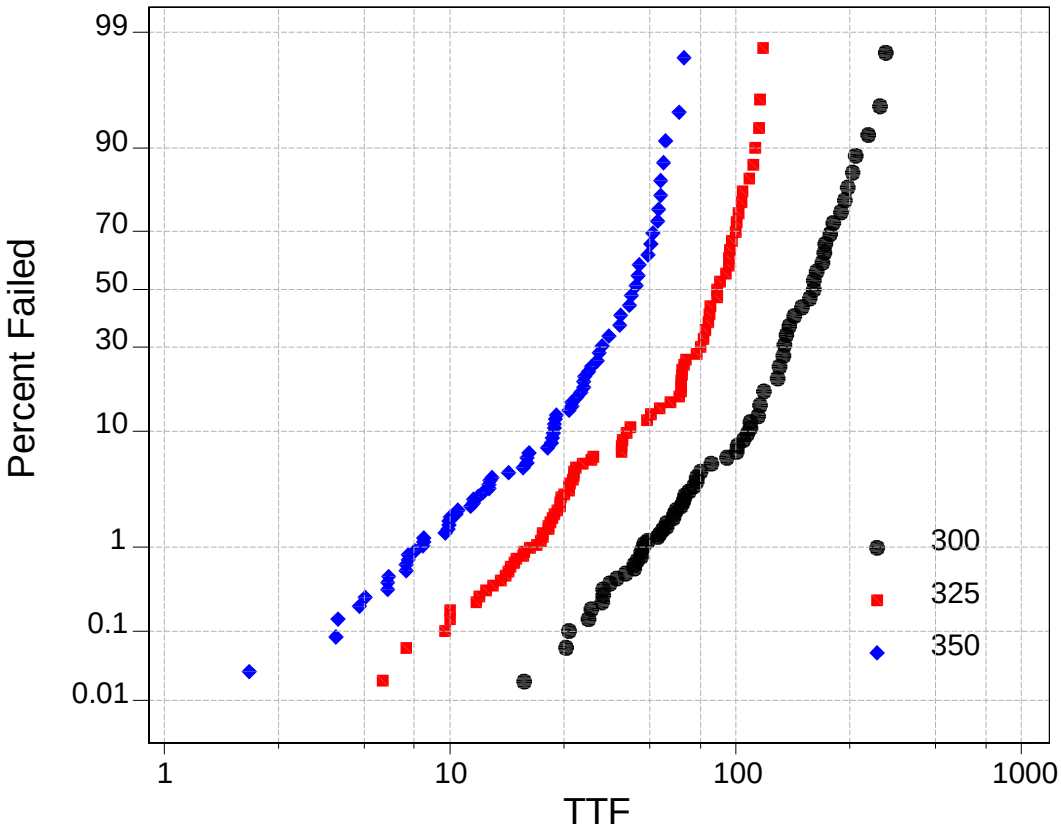


Figure 6.23 Failure distributions of the 1, 10, and 100-link V3M4 structures tested in a range of temperatures from 300 to 350 °C. The data shows bimodal behavior at all three temperatures.

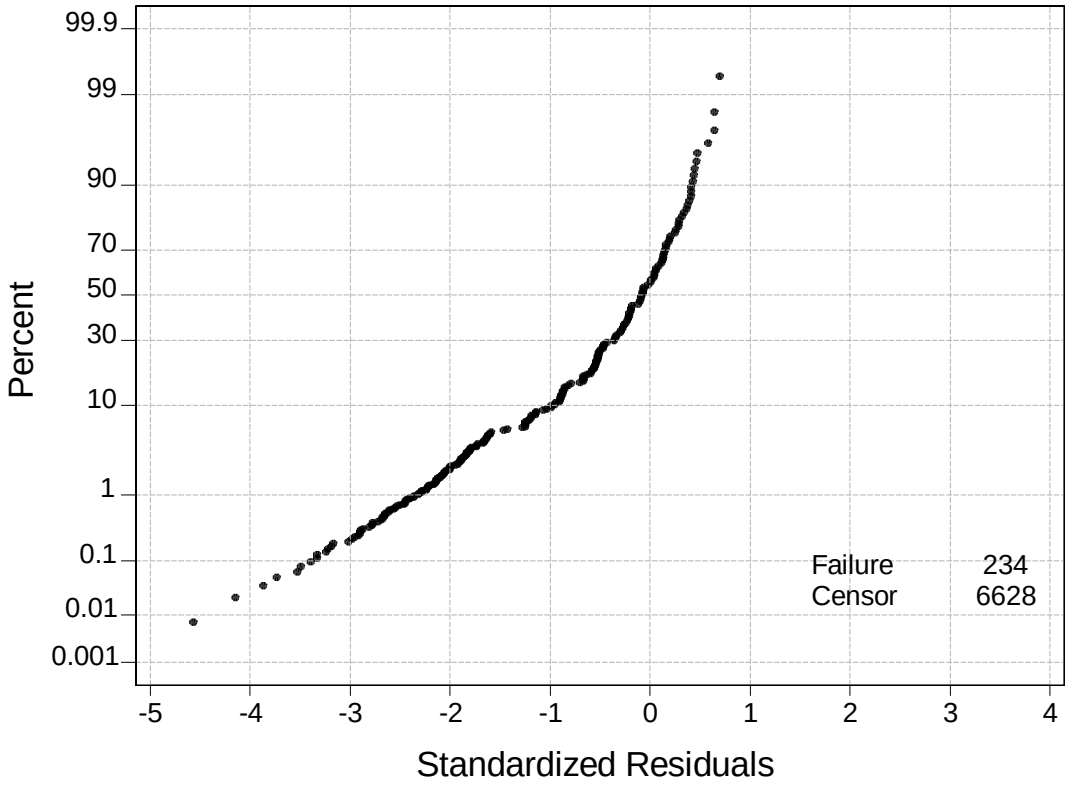


Figure 6.24: A plot of the distribution of standardized residuals for the lognormal fit of the 1, 10, and 100-link V3M4 dual-inlaid structures tested in a range of temperatures from 300 to 350 ^{o}C. The early fail tail is clearly seen in this figure extending to the left.

The failure distributions of the dual-inlaid samples were further analyzed by separating the two distributions. The distributions were separated using an iterative technique in which the distribution was first cut in half at about the 10th percentile. Data points were then removed from the bottom of the strong mode distribution and from the upper portion of the weak mode distribution until the

two distributions were straight. In Figure 6.25 the failure distributions of the weak mode are shown at the three testing temperatures. The distributions are fit by a lognormal and bounded by the 90% confidence intervals. The good temperature separation seen in 6.23 is also evident here. In Figure 6.25 the distribution of standardized residuals of the weak mode is shown. Again the lognormal fit is seen with the 90% confidence bounds. The figure reveals a good lognormal fit extending below the 0.001 percentile. The quality of the fit allows for a confident characterization of the weak mode failure. The censored data count indicated in this figure, 6453, is the result of the weak mode distribution being comprised of 10 and 100-link structures. These distributions are comprised almost entirely of 100 and 10 link structures because these structures are more susceptible to minority modes of failure. The relative percentage of the two modes of failure will be investigated later in this chapter.

The MTTFs, activation energy and lognormal sigma calculated from the weak mode distributions are listed in Table 6.3. The activation energy found for the weak mode was found to be consistent with the findings from the single-inlaid structures. The similarity in activation energy suggests that the diffusion mechanism responsible for EM failure in these parts is the same as in the single-inlaid structures. The lognormal sigma of the weak mode is large which indicates there is a great amount of variability in the kinetics of failure for the individual links.

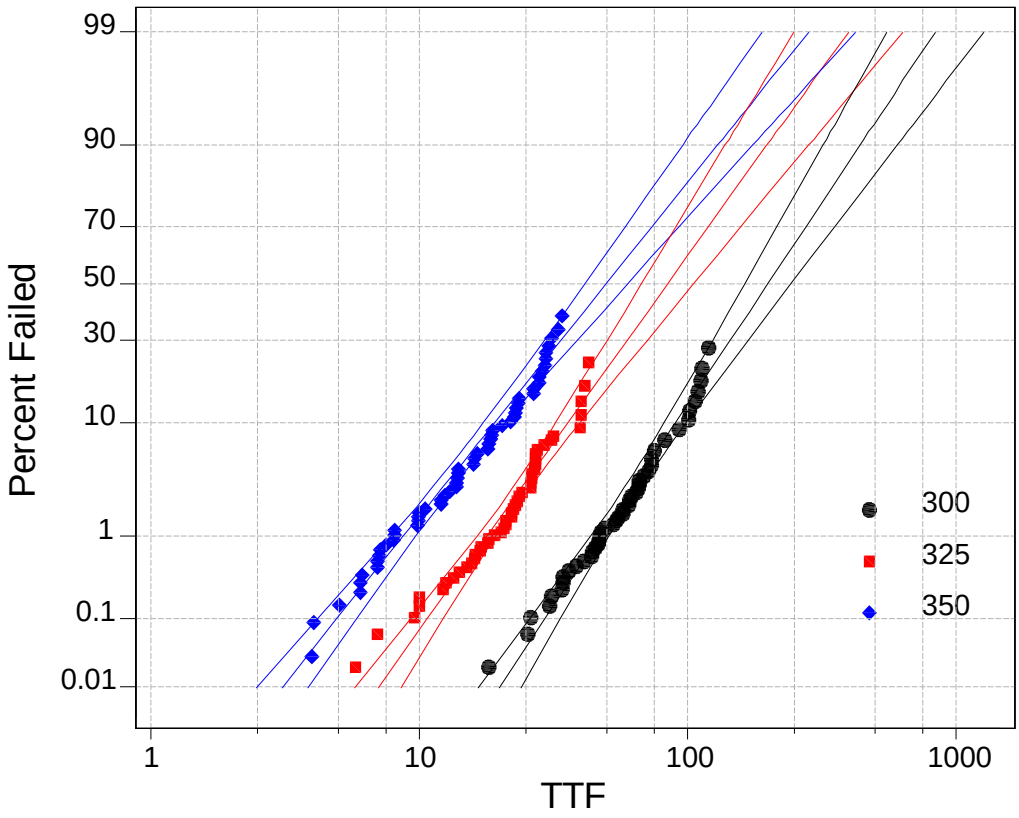


Figure 6.25 Failure distributions of the lower portion of the data. The data includes the 1, 10 and 100 link structures.

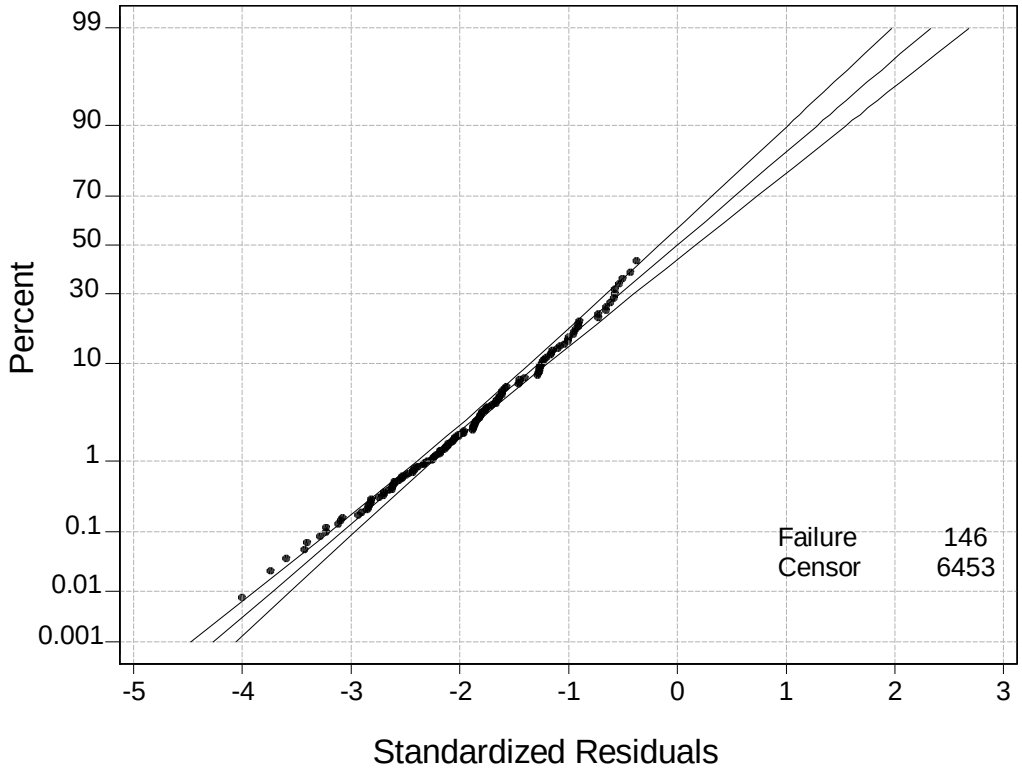


Figure 6.26: A plot of the distribution of standardized residuals of the lower portion of the data. The data has a good lognormal fit. The large amount of censored data is due to the 100 and 10 link test structures.

Table 6.3 The activation energy and lognormal sigma calculated form the lower portion of the results described above. The error rate is also listed for both the E_a and σ in terms of ± value. The median times to fail (MTTF) based on a maximum likelihood analysis (MLA) are listed for each of the three temperatures.

E_a (eV)	Lognormal σ	$MTTF_{300}$ (hrs)	$MTTF_{325}$ (hrs)	$MTTF_{350}$ (hrs)
1.01 ± 0.07	0.70 ± 0.06	198.2 ± 29.2	83.8 ± 17.0	49.5 ± 7.5

In Figure 6.27 the separated strong mode failure distributions are shown for the three testing temperatures. As in the previous example the distributions are fit by a lognormal and bound by the 90% confidence bounds. The distributions are straight and well separated as in Figure 6.25. The distributions in this case are roughly symmetric about the median line because they are comprised of mostly single-link structures. In Figure 6.28 the distribution of standardized residuals of the strong mode is shown. The pooled distribution of the residuals reveals a good lognormal fit extending down to the 1 percentile. The MTTFs, activation energy and lognormal sigma calculated from the strong mode distributions are listed in Table 6.4. Surprisingly, the activation energy of the strong mode is actually slightly lower than that of the weak mode, but when the error bound are taken into consideration it is quite similar. The other surprising result is that the median times to failure at the three testing temperatures are similar to those of the weak mode. Due to the similarity on fail times, it would be inappropriate to refer to the weak mode failures as ‘early fails’. The lognormal sigma found for the strong mode was significantly lower then that of the weak mode and was consistent with the single-inlaid findings.

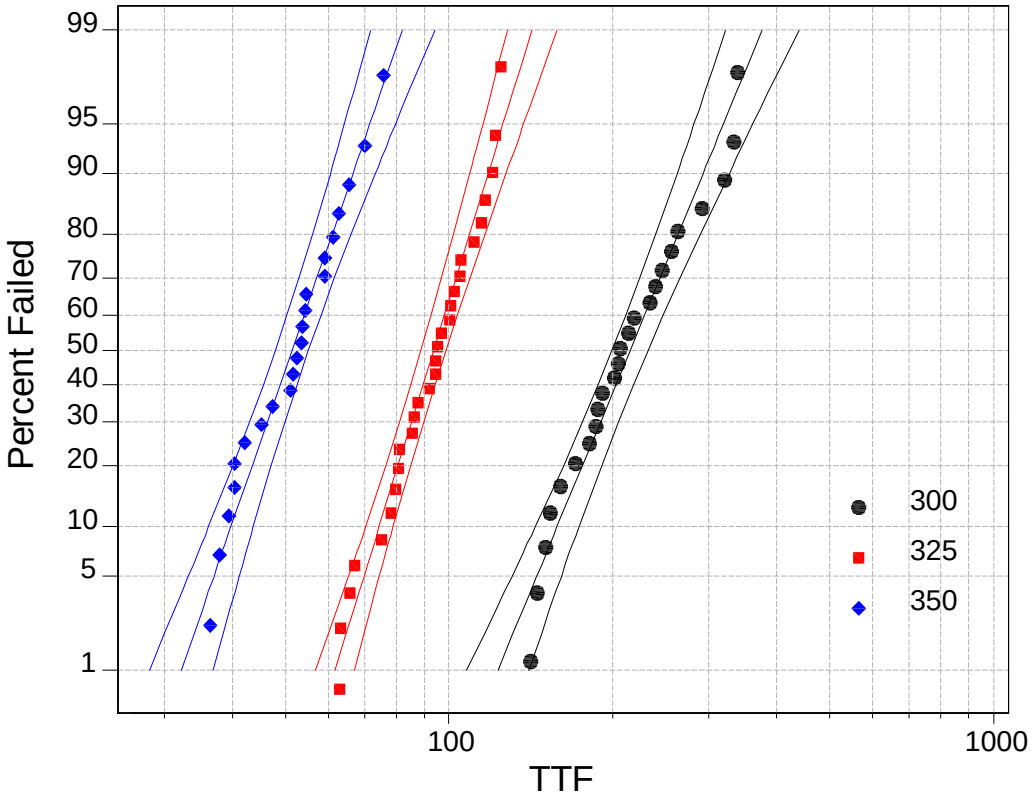


Figure 6.27 Failure distributions of the lower portion of the data. The data includes the 1, 10 and 100 link structures.

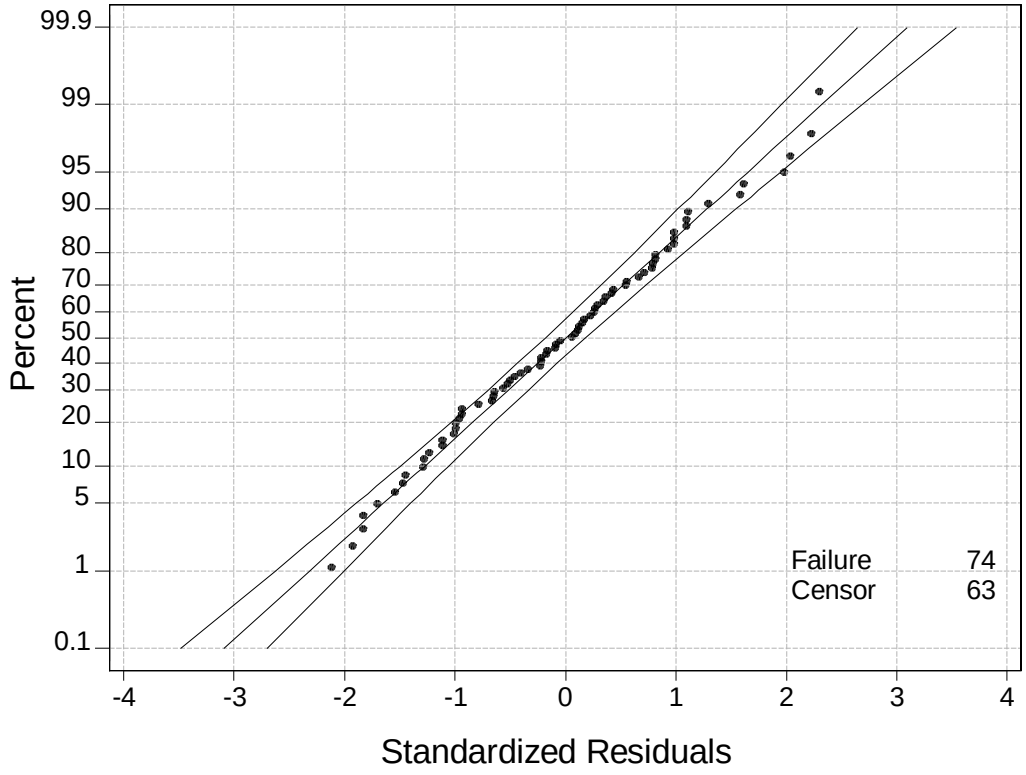


Figure 6.28 A plot of the distribution of standardized residuals of the upper portion of the data. The data has a good lognormal fit. The small amount of censored data is the result of the 10-link structures.

Table 6.4 The activation energy and lognormal sigma calculated form the upper portion of the results described above. The error rate is also listed for both the E_a and σ in terms of $\pm$ value. The median times to fail (MTTF) based on a maximum likelihood analysis (MLA) are listed for each of the three temperatures.

E_a (eV)	Lognormal σ	$MTTF_{300}$ (hrs)	$MTTF_{325}$ (hrs)	$MTTF_{350}$ (hrs)
0.88 ± 0.06	0.21 ± 0.02	204.8 ± 8.1	90.7 ± 5.4	53.9 ± 2.5

In Figures 6.29 and 6.30 Arrehnius plots of the median time to failure for the strong mode and weak mode failure are shown. In both cases the same trend is seen with the 325^{o}C time being lower then the trend line. The error bounds are much greater for the weak mode failure shown in Figure 6.30 due to the large sigmas for the fail time distributions. In the 300 and 350 ^{o}C tests thermocouples verified the testing temperature to be within ± 1^{o}C of the set temperature. The 325 ^{o}C test however, did not make use of thermocouples, making temperature correction of this test difficult. The consistency of the data is an indication that the actual temperature of the 325^{o}C was actually somewhat higher than the set point. The MTTF of the center data point does not influence the slope of the fitted line and as a result does not have any bearing on the activation energy calculated from these results. Because the 325^{o}C value does not impact the activation energy, no attempt was made to correct for the offset testing temperature.

In Figure 6.31 the lognormal sigmas for the strong and weak modes are shown as a function of test temperature. It is interesting to note that the trend of the lognormal sigmas with temperature is different for the two failure modes. As the temperature is increased the strong mode sigma decreases as has been reported by other researchers. Interestingly, the sigma of the weak mode distribution increases with increasing temperature.

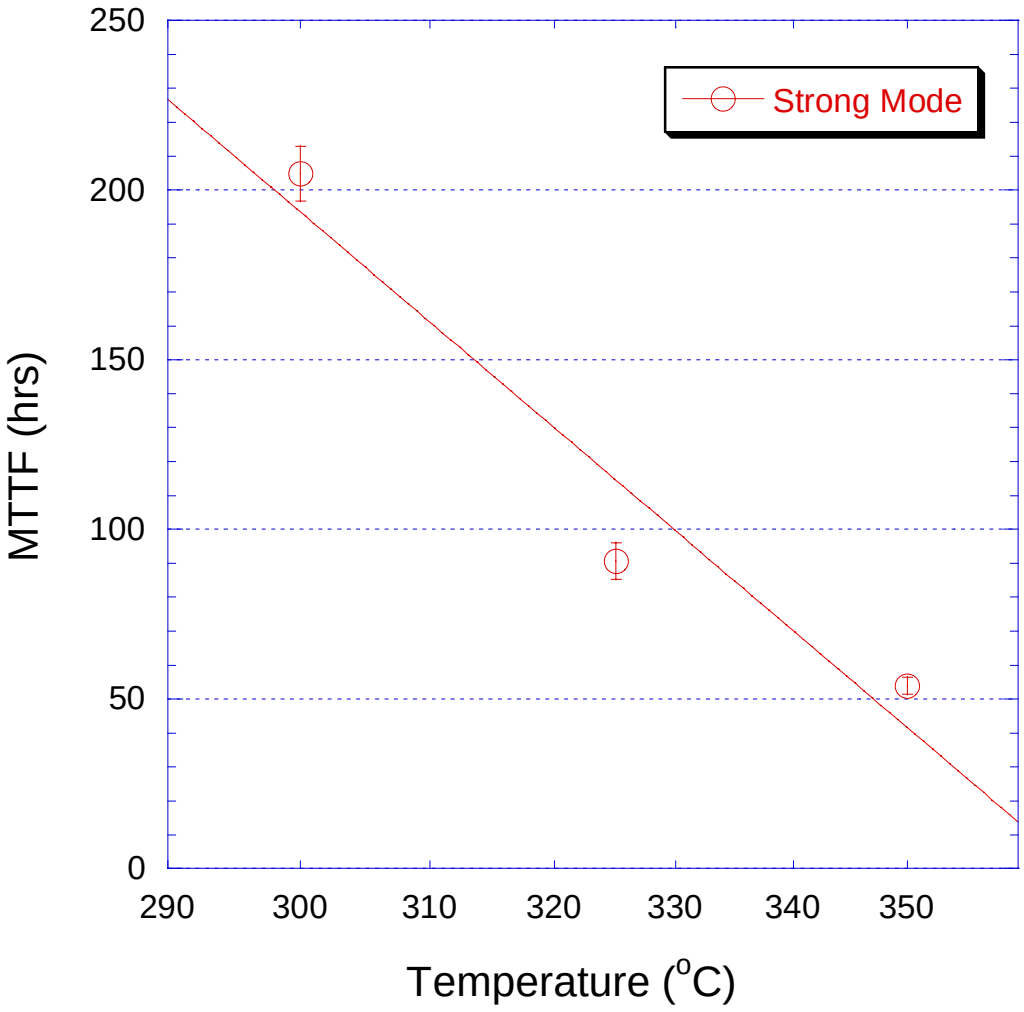


Figure 6.29: A log plot of the Median Time to Failure (MTTF) from the upper portion of the data, or the strong mode.

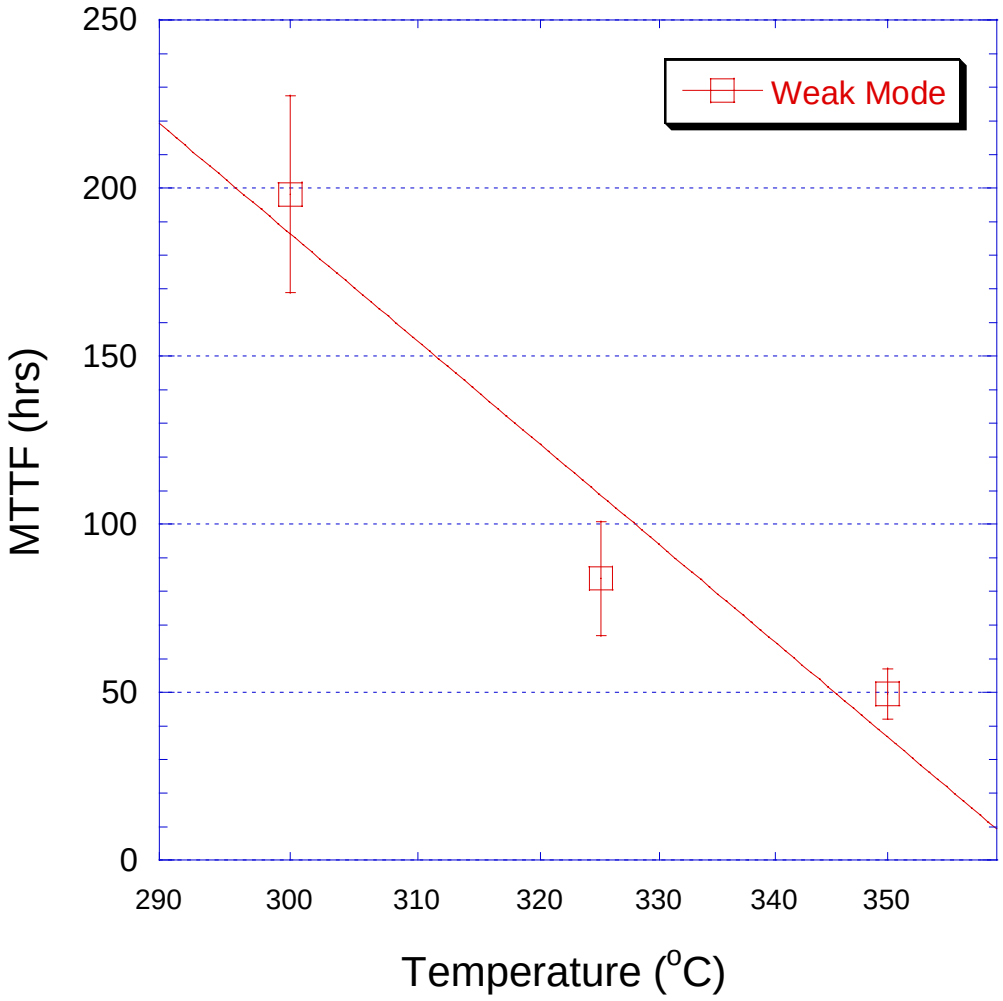


Figure 6.30: A log plot of the Median Time to Failure (MTTF) from the lower portion of the data, or the weak mode.

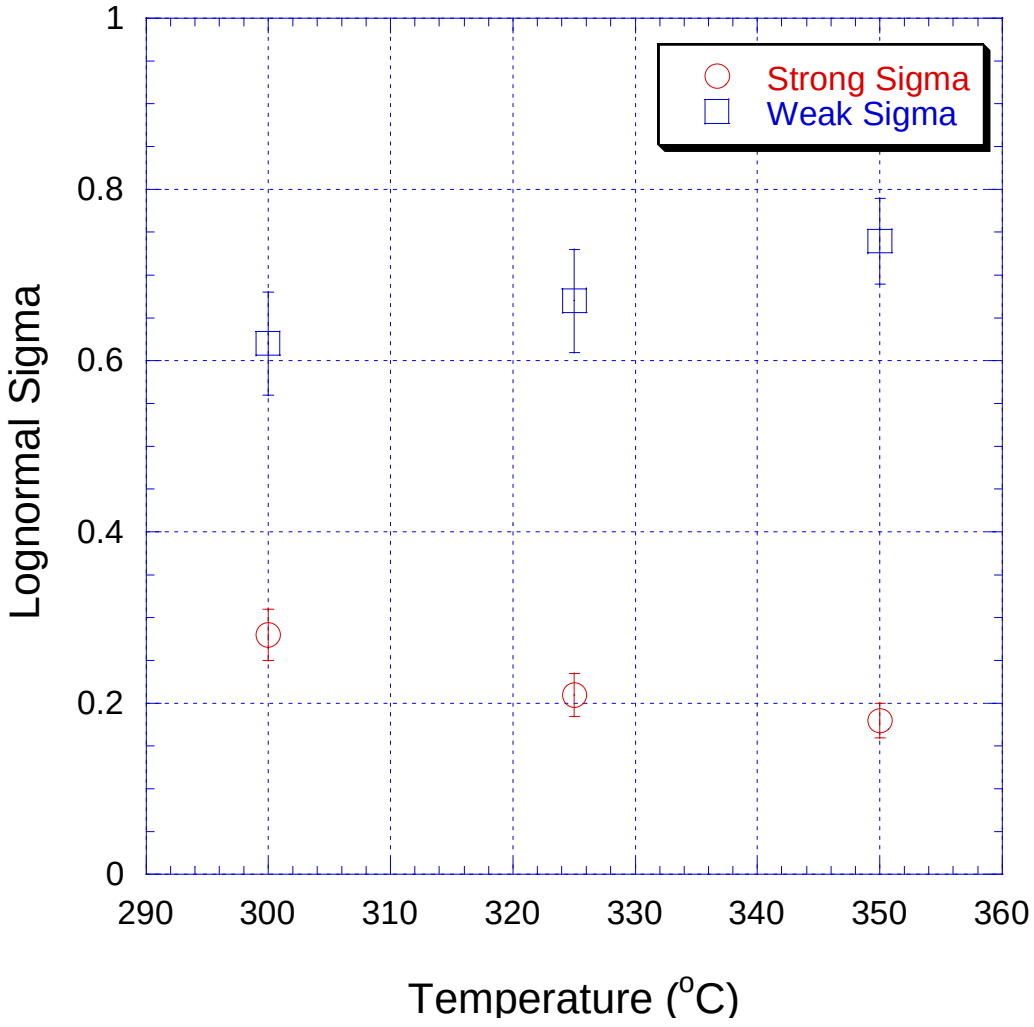


Figure 6.31: The lognormal sigma for the Strong-Mode and Weak-Mode as a function of temperature.

Once the weak and strong modes had been identified and characterized the next step is to determine the degree of mode mixing in the EM failures for the dual-inlaid structures. In order to determine the proportions of mode mixing the bimodal failure distributions seen in Figure 6.23 must be modeled with Monte-Carlo simulations. The Monte-Carlo simulations were conducted using a random

number generator that is part of the Mintab™ statistical software package. Six different types random log-normal distributions were created; one for the strong and weak modes at each of the testing temperatures. The lognormal distributions were specified by the median time to fail as written in tables 6.3 and 6.4, as well as the sigma for the specific temperature as seen in Table 6.5.

Table 6.5 The lognormal sigma for the strong and weak mode at each of the three testing temperatures.

Temperature (^{o}C)	Strong Mode σ	Weak Mode σ
300	0.28 ± 0.03	0.62 ± 0.05
325	0.21 ± 0.02	0.67 ± 0.06
350	0.18 ± 0.02	0.74 ± 0.06

The first step in fitting the observed data with the simulation data was to create the strong mode base. For the 300^{o}C data the 1, 10 and 100-link structures were modeled by three different distributions. Each of these distributions was created with the same MTTF and sigma values as measured for the strong mode results at 300^{o}C. 50 data points were created to model the single link structures. Than a distribution of weak mode fails was created. The size of this distribution was originally set to be 10% of that of the strong mode failure implying 10% weak mode mixing. The 5 weak mode data points were then compared to 5 random data points of the strong mode distribution. Whichever of the two values was lower was used for the new fail time. For the 10 link structures, 500 strong mode points, and 50 weak mode points were created initially. The 50 weak mode

points were compared to 50 random strong mode points, and the lower value was kept. While in random order the combined data sets were assigned to bins of 10 data points. The lowest value in each of these bins was than used to simulate the fail time of a 10-link structure. The 100 link structures were modeled in much the same way, except 5000 data points were originally created and a bin size of 100 was used.

The same procedure was repeated for each of the three testing temperatures. The fit of the simulations based on a 10% weak mode population did not fit the observed distributions very well. The observed distributions had significantly higher percentage of weak mode fails than was simulated. The same procedures were repeated with higher weak mode populations until the simulations fit the observed data. In Figures 6.32 – 6.34 the simulated results are plotted with the experimental results. In each case the fit of the simulated data is excellent with only very small deviations observed. In Table 6.6 the proportions of strong and weak mode failure for each of the testing temperatures are listed. The amount of weak mode mixing needed to achieve the quality fits was much higher than anticipated, 40-50% compared to the expected value of 10%. The large percentage of weak mode failure is a result of the fact that the median times to failure for the weak and strong mode were quite similar. The result of this is that when the two distributions are mixed, there is a lot of overlap so that much of the upper portion of the weak mode distribution does not impact combined fail distribution. The amount of overlap is also greatly increased due to the large

sigma of the weak mode distribution. The large sigma results in many long lifetime data points that also do not impact the combined distribution.

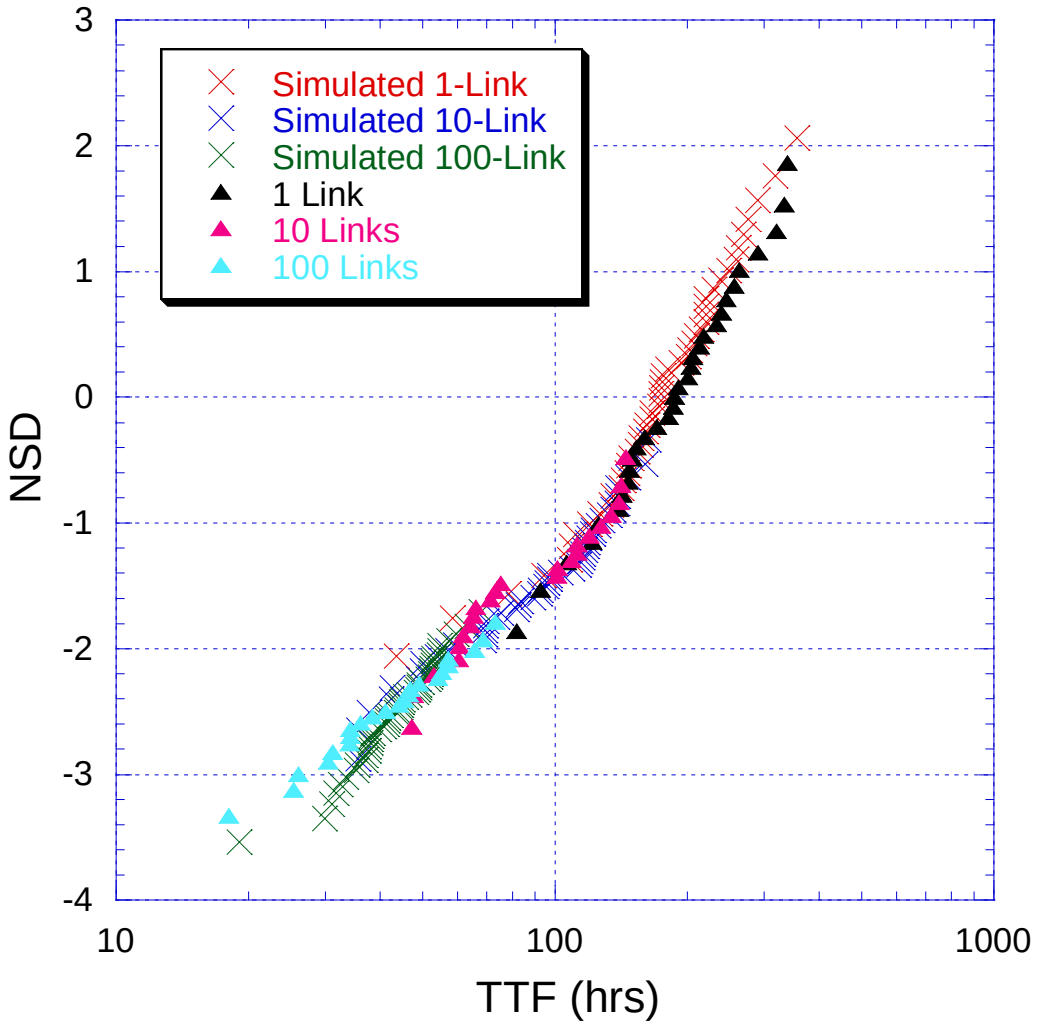


Figure 6.32 Failure distributions of the 1, 10, and 100-link V3M4 structures tested at 300°C and the results of the Monte-Carlo simulation. Good agreement is seen between the two data sets.

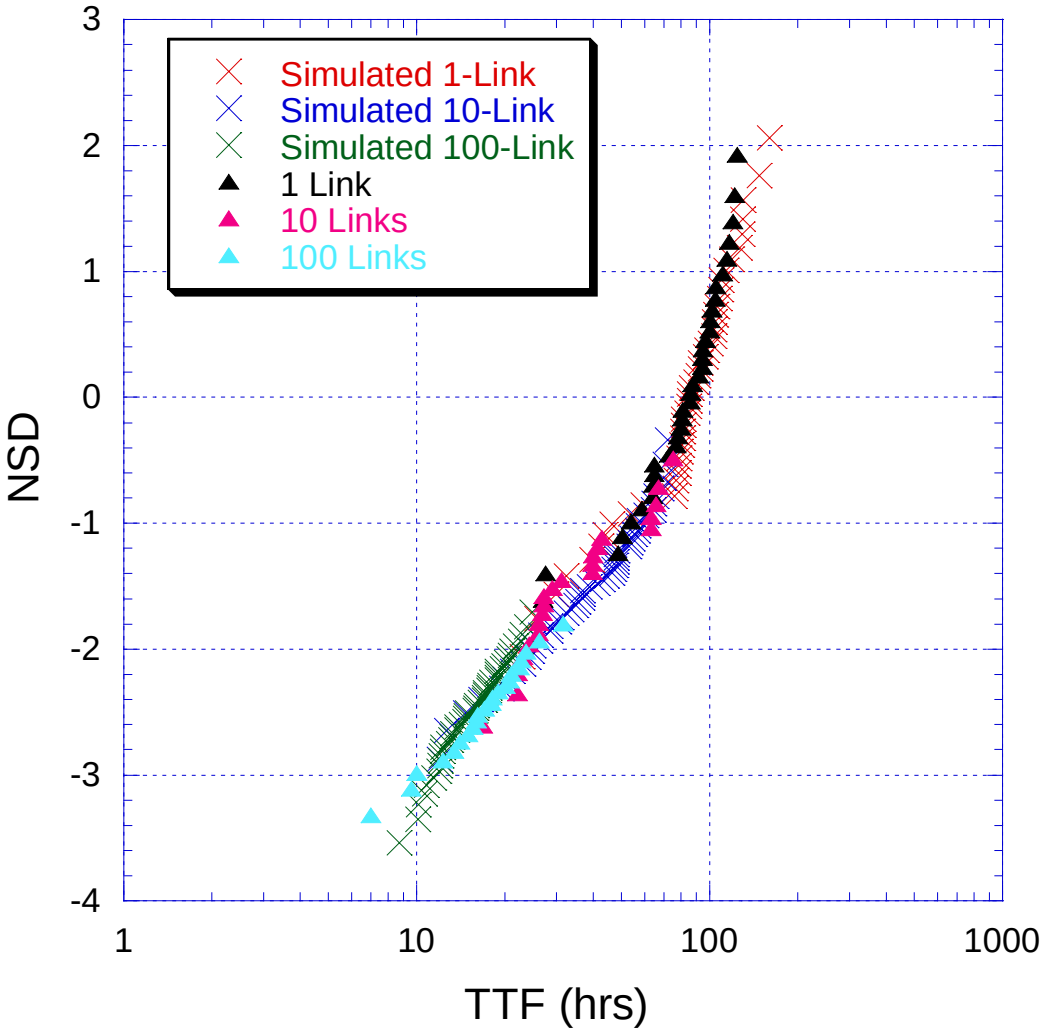


Figure 6.33 Failure distributions of the 1, 10, and 100-link V3M4 structures tested at 325°C and the results of the Monte-Carlo simulation.

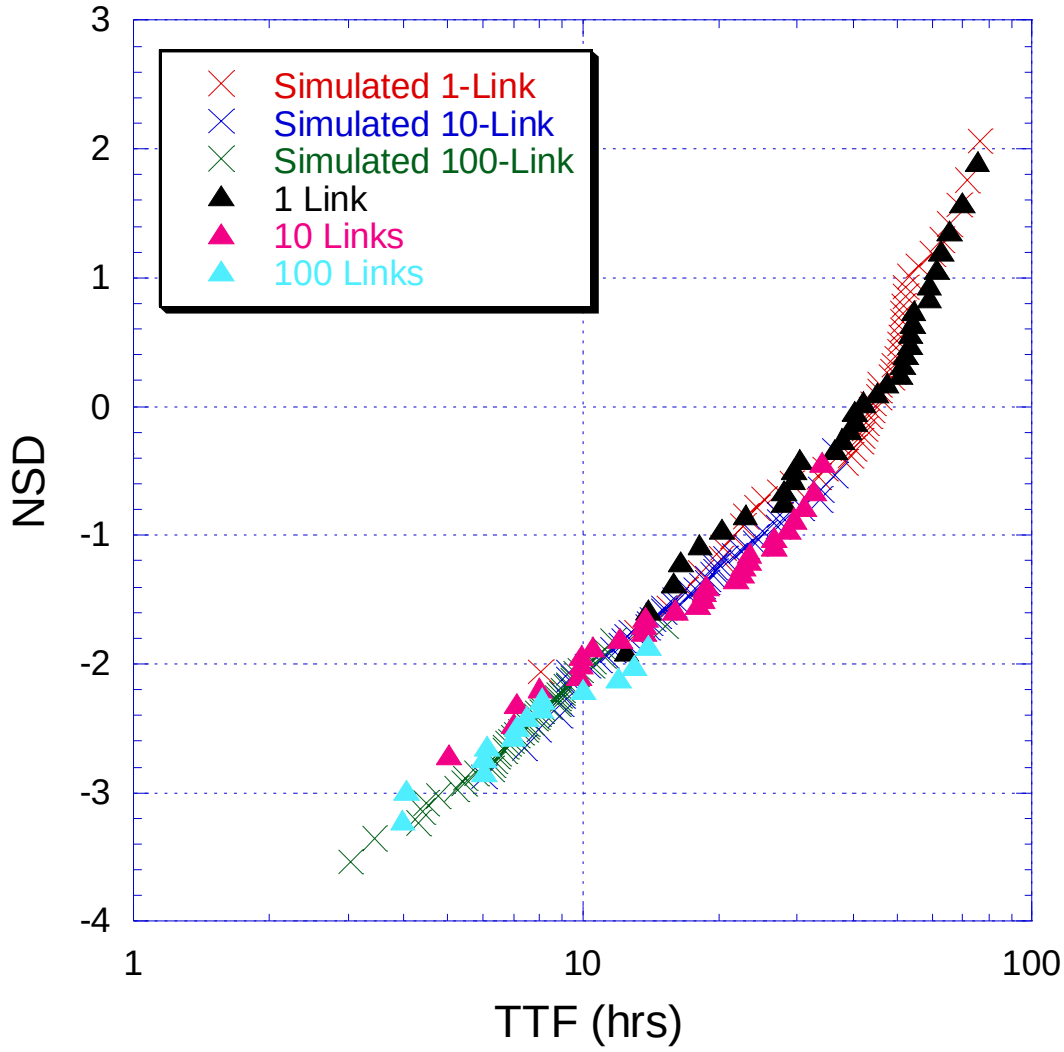


Figure 6.34 Failure distributions of the 1, 10, and 100-link V3M4 structures tested at 350°C and the results of the Monte-Carlo simulation.

Table 6.6 The percentage of strong and weak mode failures used to create the Monte-Carlo simulation. The percentage of weak mode failures is much higher then the combined distribution would suggest.

Temperature (^{o}C)	Strong Mode	Weak Mode
300	60%	40%
325	55%	45%
350	50%	50%

Failure analysis was conducted on single link structures to determine the causes of the bimodal behavior seen in the EM testing of the dual-inlaid structures. The failure analysis was done in much the same way as the failure analysis discussed in previous sections, in which a trench next to the via of interest was cut with an FIB. SEM and FIB micrographs were than taken of the cross sections.

In Figure 6.35 two images of the anode of a single link structure which failed according to the weak mode. The failure occurs at the top of the via as opposed to the bottom of the via as other researchers have reported. The weak mode failure as described by other researchers occurs at the bottom of the via due to the flux divergence created by the diffusion barrier. In this case the weak mode failure does not appear to be caused by the flux divergence at the bottom of the via but rather by a process defect that induces failure at the corner of the via and line intersection. In Figure 3.4b a similar FIB cross section of an unstressed sample is shown. The barrier appears to be either extremely thin or discontinuous at intersection corner. If the barrier is continuous it is possible that it does not

contribute to any accelerated failure. If the barrier becomes discontinuous it can contribute to early failure by allowing for preexisting voids. These preexisting voids are created when the Cu seed does not have a continuous barrier layer in which to form one. The electroplating fill process depends on a complete seed layer to completely fill the interconnect trench and via. With gaps in the seed layer it is likely the Cu fill process was compromised leading to early EM failure in some structures.

In Figure 6.36 the failure analysis results from the strong mode failure are seen. In Figure 6.36a a failure that is very similar to the single-inlaid V1M2 failure seen in Figures 4.10, 5.20, and 5.21. In this case the via remained undamaged just as if it were encapsulated by the diffusion barrier. In Figure 6.36b the void is seen extending into the via. In this case it is likely that the void formed along the top interface (Cu / PEN) and grew towards the anode end and into the via. In none of the failure analysis conducted on these dual-inlaid samples was a typical via failure as reported by other researchers observed. In these samples the multi-modal EM behavior is the result of a process defect and is not associated with the inherent nature of the dual-inlaid interface.

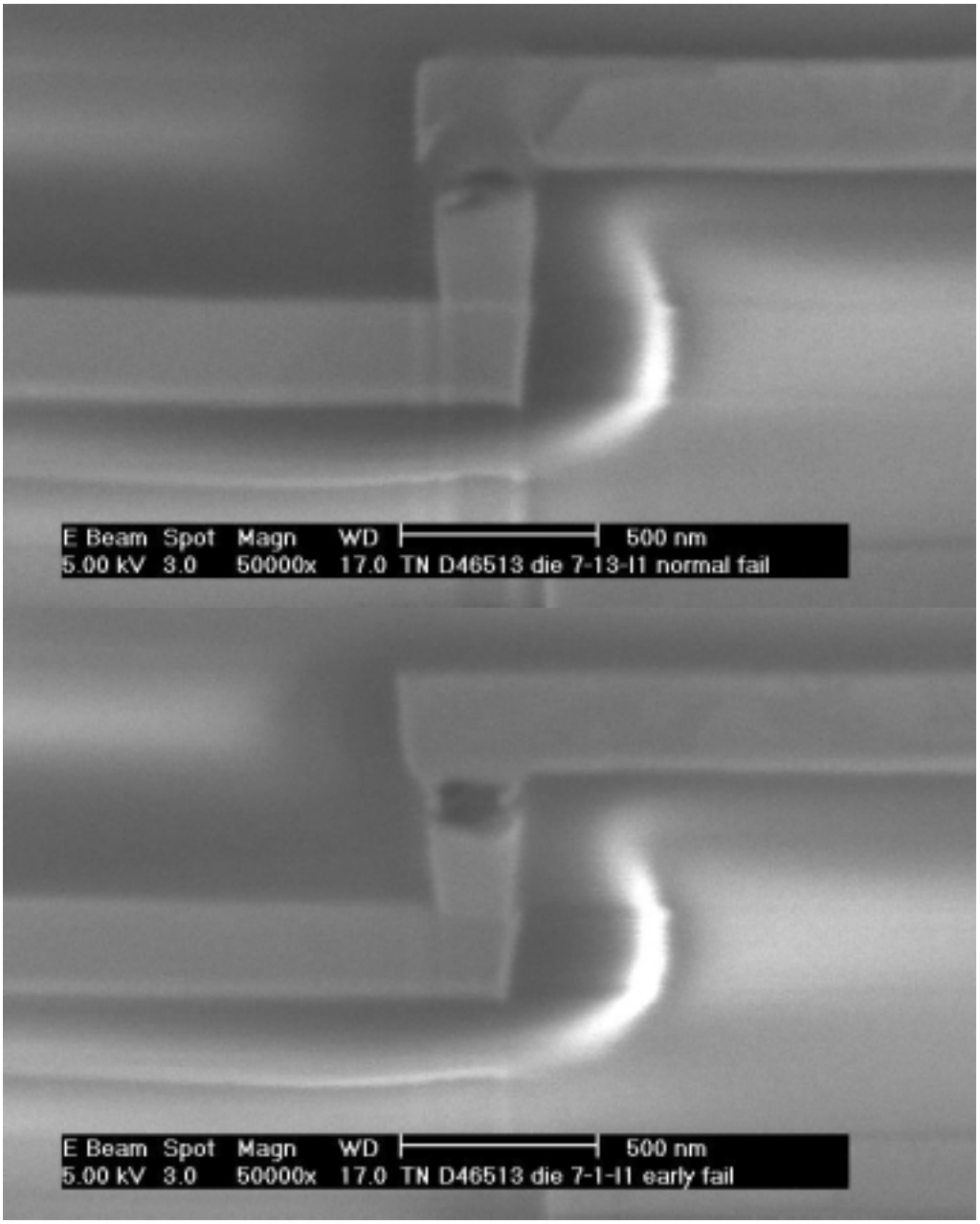


Figure 6.35 (a&b) SEM micrographs showing the cross section of part of two early fail dual-inlaid test structures after EM testing at 325 ^{o}C. A short Metal –1 connecting line is seen in the center. These two structures failed according to the weak mode mechanism.

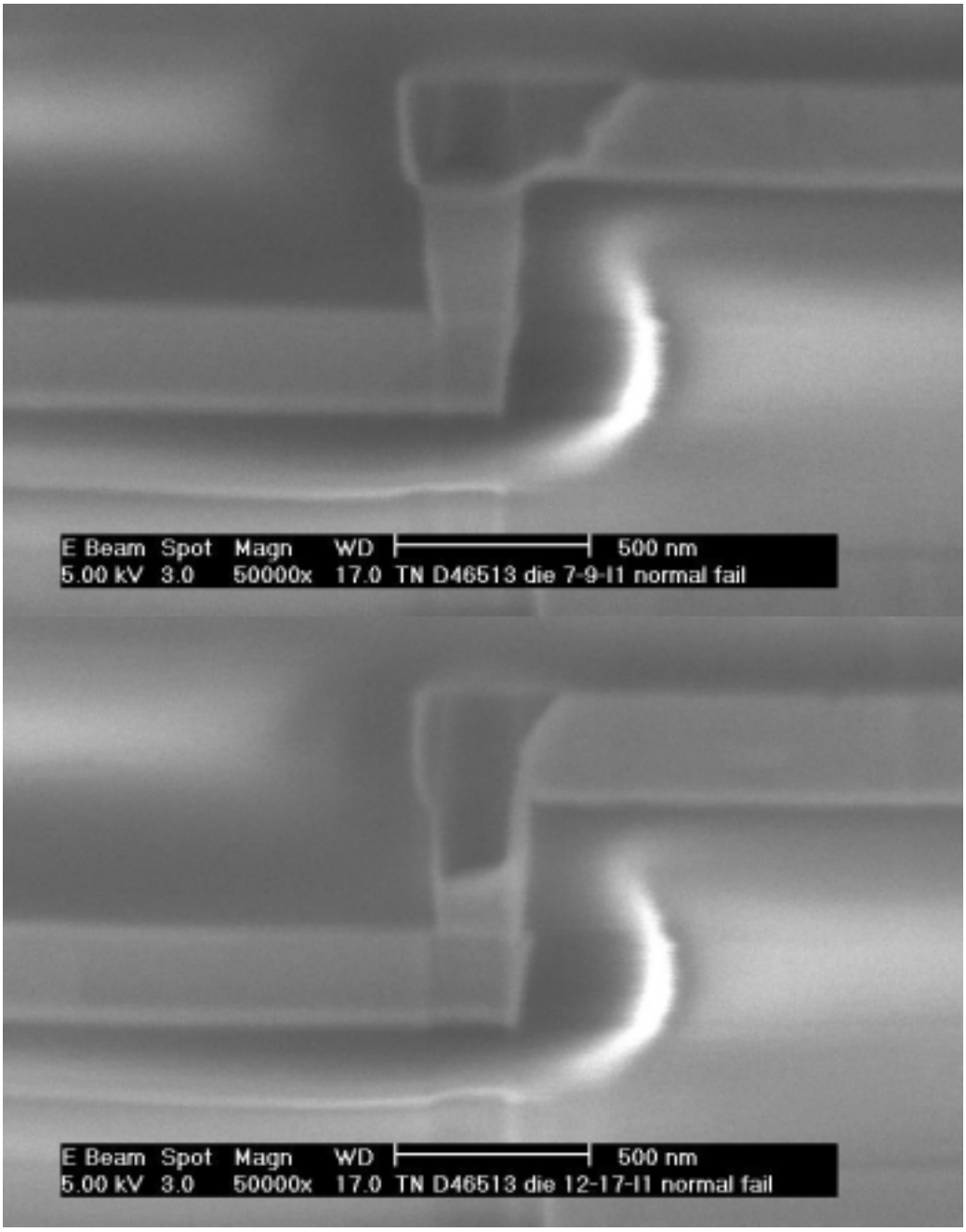


Figure 6.36 (a&b) SEM micrographs showing the cross section of part of two normal fail dual-inlaid test structures after EM testing at 325 ^{o}C. A short Metal –1 connecting line is seen in the center. These two structures failed according to the weak mode mechanism.

Chapter 7: Summary and Conclusions

The results of this study have confirmed several recently developed models describing electromigration behavior in Cu interconnects. Electromigration studies conducted on single-inlaid test structures have shown that the electromigration induced voiding occurs at flux divergent interfaces created by non-diffusing layers. Two types of interfaces were studied in this work, the upper via / metal interface, V1M2 and the lower via / metal interface, V1M1. The results of this study indicate that the fundamental failure mechanisms of these interfaces are different and results in longer lifetimes for the V1M2 interface but equivalent activation energies of about 1.0eV.

The impact of interconnect geometry was also examined in this work. The impact of interconnect line width was studied using single-inlaid test structures with 1x, 2x and 3x width structures. The results indicate that the EM lifetime of both interfaces does not depend on line width when the current density is kept constant. Another interesting result indicated that the EM lifetime of the 3x V1M2 structure was not affected by the addition of a second via, where as the equivalent 2 via-V1M1 significant increase in lifetime. The effect of interconnect line length and the 'Blech' effect was studied on contact-metal, CaM1, structures. The Blech length, jl*, was determined to be 3800 A/cm, but the resistance saturation effect seen in Al-Cu interconnects was not seen. This was likely the result of the thin highly resistive barrier layers used in these Cu interconnect which do not act as effective shunt layers.

The statistical nature of electromigration failure was also studied in both single- and dual-inlaid interconnects using multi-link test structures. In single inlaid Cu interconnects the statistical analysis showed that the EM failure distributions of both the V1M1 and V1M2 were primarily mono-modal with the failure mechanisms reflecting the observations of single link interconnects. The EM tests on the multi-link structures were sensitive enough to observe the resistance jumps associated with individual line segments failing in the structures. The statistical analysis of the single-inlaid parts also highlighted the improved failure statistics that multi-link structures provide.

The statistical analysis of dual-inlaid structures highlights the other major advantage to using multi-link structures. In this case the V3M4 EM structures were found to fail with a distinct bi-modal failure distribution. Had only traditional single-link structures been used the EM tests might not have been sensitive to the multi-modal failure. The cause of the bimodal behavior was determined to be a process induced defect in which there was not complete barrier coverage at the top of the via.

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Vita

Patrick Ryan Justison was born in Tucson, Arizona on August 26th 1973, to Paul and Ann Justison. After completing high school in California, Patrick packed his things and headed off to Pennsylvania and Lehigh University. While there Patrick exemplified the study hard, party hard ethic. After completing his undergraduate degree in Materials Science Patrick moved on to a brief stint at IBM in Endicott, NY where he studied conductive polymers to be used in the microlectronics industry. Shortly after his work at IBM, Patrick decided the next step was graduate school, so he enrolled in the University of Texas to continue his study of materials science. Shortly after beginning at the Univ. Of Texas Patrick started a summer internship with Motorola, where he continues to work to this day.

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