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Capacitive Shear Stress Sensor with DC Sensing Capability for Fluid Flow Measurements

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Capacitive Shear Stress Sensor with DC Sensing Capability for Fluid Flow Measurements

by

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Abstract

Capacitive Shear Stress Sensor with DC Sensing Capability for Fluid Flow Measurements

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The University of Texas at Austin, 2017

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In this work, the design, simulation, fabrication, and characterization of a shear stress sensor based on a differential capacitive sensing scheme are presented. The sensor is an adaptation of previous generations that utilized piezoelectric sensing techniques. The present generation of the device replaces the piezoelectric with a dielectric film, converting the sensing mechanism of the device from piezoelectric to capacitive. The motivation for this adaptation is to create a shear stress sensor capable of sensing static shear stresses, such as those generated by a constant flow across a surface. The sensors consist of an array of unit sensing cells, each of which contains three electrodes: two resting on the substrate, and a third resting on top of the dielectric, between the bottom electrodes. This configuration creates a resting capacitance between the top electrode and either bottom electrode that varies when the top surface of the device experiences shear stress and thus deflection of the top electrode. The departure from the resting capacitance is monitored by applying a sinusoidal signal to the bottom electrode, and observing the change in amplitude of the signal at the top electrode as the surface shears. The device is

first modeled analytically and numerically to estimate the sensitivity for the device, which is used as the figure of merit in evaluation of these shear sensors. Sensitivity is defined in this context as the change in capacitance per Pascal [$\Delta C/Pa$]. The fabrication and testing of the device are described, through which a measurement of the sensitivity of the sensors is obtained and found to be in agreement with the predicted sensitivity via simulation.

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Chapter 1: Introduction

For several decades, the ability to measure shear stress with high spatial and temporal accuracy has been of interest in the field of fundamental fluid dynamics research. The research is applicable to various industries – biomedical, aerospace, automotive, and others. Many of the existing sensors suffer from the effects of thermal drift, device vibration, and scaling limitations. Differential capacitive sensing offers an alternative technique that can mitigate some of the ailments of the existing technologies.

The ability to accurately measure a shear force is a relatively recent development, gaining significant traction in the 1970s and 1980s, prior to which researchers relied heavily upon FEA models to estimate tangential forces on a surface [12]. The capability to measure shear forces directly is an attractive complement to computer modeling to countless industries. Generally speaking, being able to measure shear force enables users to learn about the viscosity of the given fluid. This principle has significant impact on the health care industry. Some studies suggest the existence of a connection between blood viscosity and certain cardiovascular issues, and MEMS devices are often targeted for use in measuring these bio-parameters [2]. Continuous in-vivo measurements of a patient's blood viscosity could offer monitoring abilities for physicians to detect early warning signs of ailments such as Acute Coronary Syndrome, as investigated by Lee et al. [3]. Many other industries such as the paints and coatings, oil and gas, and food and beverage [5] often require close monitoring of process control values, such as product viscosity. In [4], for example, Maroto et al. utilize shear measurements for evaluation of the weight of petroleum oils, while in [5], Sharma et al. focus on the viscosity of mozzarella cheese. The use of shear sensors to continuously monitor these production processes for quality control is also a realistic application. In addition to viscosity, a shear stress sensor can

supply data about tactile interaction with its environment. Consumer electronic devices, such as touch screens or video game controls with variable force controls, can all benefit from the use of shear stress sensors.

Aside from the above mentioned applications of shear force measurement, there are significant applications in automotive, watercraft, aircraft, and spacecraft industries. In many situations, the designs of each type of these vessels target highly aerodynamic shapes as to minimize drag. Measuring the shear stress at any point on the outer surface of a vehicle, which is usually carried out in a wind tunnel, allows researchers to determine which regions of a surface may be negatively impacting the aerodynamics of the vessel. Robust shear stress sensors can be mounted flush on the surface of any vessel in great numbers to gain a picture of the shear stress experienced at many different locations on the vessel. As the sensors are made smaller, the possibility to increase the spatial resolution of these measurements increases, improving designers' abilities to optimize the shape of the given vehicle with even greater accuracy. This is essential to creating safer spacecraft, which undergo extreme shear stress environments and can sustain critical damage from heating of regions that are subject to extreme shear stress. The same principle aids the creation of more fuel-efficient automobiles, aircraft, and watercraft. Moreover, in the racing sector of these industries, where experts endlessly labor to reduce drag on their craft, a high spatial resolution shear sensor offers the possibility to accurately identify and pinpoint areas that may be contributing more drag. When the capabilities of the vehicle become more extreme, such as aircraft and space craft that can achieve Mach numbers in the range of 0.8-5, the drag and friction on the boundary layer of the vehicle become even more critical. In these extreme flow conditions, temperatures can reach levels up to 1,200 K (926 °C). In these applications, it becomes even more important to accurately measure the flow over a surface of the

vehicle as to prevent any safety malfunctions and to maximize aerodynamics and energy efficiency.

The primary motivation for the research presented in this document comes from the Air Force Office of Scientific Research (AFOSR). This device is part of a broader research project to address the lack of sensors capable of direct measurement of shear stress in extreme flow conditions experienced by many Air Force systems. The ultimate goal of the project is to develop a shear sensor that can measure shear stress from 5-1500 Pascals, exhibit a frequency response of 0-1MHz, can operate at 1,200 K, and has a sensor head size less than 3mm by 3 mm [29]. The device described in this document specifically addresses the need for direct static shear stress measurement at a frequency of 0 Hz, henceforth referred to as DC measurement. A previous generation of the senor is described later in this introduction addresses measuring dynamic shear stress at frequencies from 1Hz to 1MHz, or AC. This device, as well as the previous generation, have a device size of 1.8mm by 1.8mm, satisfying the size requirement as well. While the previous generation device utilized piezoelectric effects to measure the frequency dependent shear stress, the device in this document utilizes differential capacitive sensing to measure the DC shear stress. It is also important to note that this device is not limited to DC shear stress measurement. The design allows for AC measurement as well, however, the primary focus was on the DC capability in this project.

The operating principle of a sensor utilizing differential capacitive sensing is as follows: a device has a resting position in which two or more electrodes are placed in close proximity so as to have a characteristic capacitance. The capacitor is subjected to an environment in which one of the parameters, which include electrode spacing and material between electrodes, varies. In the realm of measuring physical forces, the natural variation for the capacitor is spacing. Particularly, the electrodes are arranged such that

one may move in relation to the other, and this causes a variation from the characteristic capacitance. The change in capacitance can be related to the displacement of the moving electrode, which can in turn be related to the shear stress applied to the device. The focus of this document is a device capable of measuring the DC shear stress of the device's sensing surface through differential capacitive sensing.

1.1 Existing Direct Shear Stress Sensor Technology

Direct measurement with shear stress sensors is frequently based on a floating element model, in which the element has specified length, width, and thickness, and is suspended by mechanical springs with a designed stiffness. The suspended element, when subjected to flow across the surface, deflects and allows transduction to occur. Depending on the construction of the spring elements, the transduction can occur in different ways. Using piezoelectric materials to fabricate the springs, the piezoelectric effect can be utilized to convert the mechanical deflection of the floating element into an electrical signal. Alternatively, if the floating element is equipped with electrodes, and the stationary portion of the device also has electrodes, the movement of the floating element provides the means for a differential capacitive sensing configuration, as previously described. The floating element has a characteristic capacitance in its resting position, and a positive or negative departure from this characteristic impedance occurs when the floating element deflects, moving the electrode mounted on the floating element closer to or further from the stationary electrode. A schematic diagram of such a device developed by Jonathan Naughton and Mark Sheplak is shown below in Figure 1.1 [1,7].

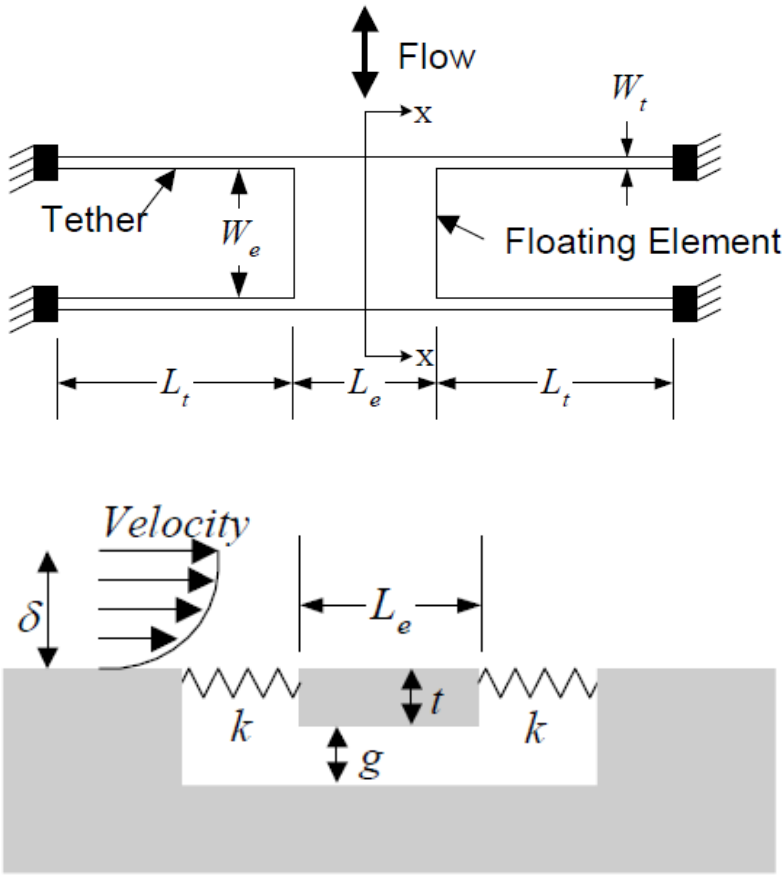


Figure 1.1. Typical schematic of a floating element shear stress sensor (top) top view and (bottom) cross section view. [1,7]

In another variation of the floating element sensor, also in [1] from Sheplak et al., an optical sensing scheme is used as the sensing mechanism. Several different configurations can be used in which the floating element interacts with a coherent light source. In this family of designs, the resting position of the floating element in the coherent light source provides the resting position parameters. The interaction between the light and the floating element can be transduced by various methods. In [9] from Horowitz et al., the element is equipped with an optical grating, and a second optical grating is below the grating on the stationary region of the device. When deflected by

flow, the floating element grating and the stationary grating create an interference pattern that can be captured by a charge-coupled device (CCD) camera. The image of the produced Moiré pattern can determine the deflection and thus the shear force. In another optical transduction technique, presented by Padmanabhan et al. in [8] and represented by Sheplak et al, in [1], the floating element serves as a shutter between the light source and photodiodes mounted below. When deflected, the photodiodes are exposed to greater illumination, increasing leakage current that is proportional to the amount of the displacement. Diagrams showing such devices can be seen below in Figure 1.2.

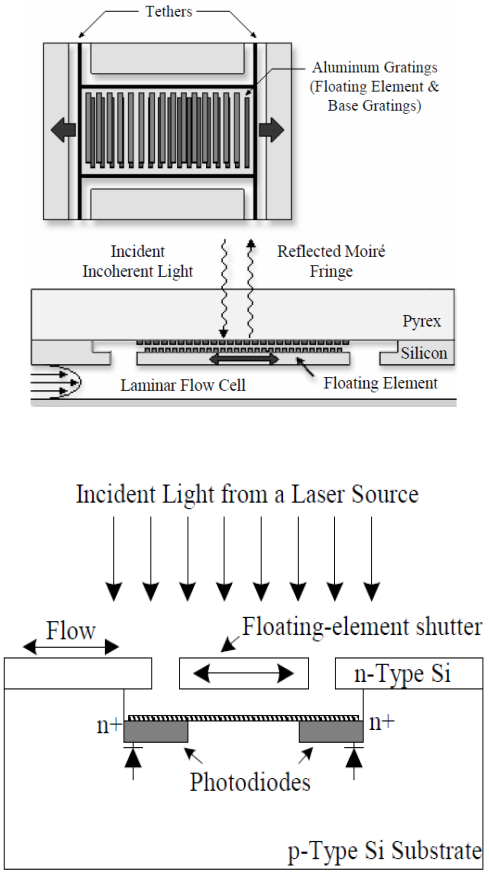


Figure 1.2. Representative schematics of optical floating element shear sensors. (Top) Moiré pattern-generating configuration (Bottom) Photodiode enabled embodiment [1,8,9].

Optical floating element shear stress sensors offer high levels of accuracy, but can become impractical to implement due to commonly bulky packaging and the need for an included coherent light source. Additionally, if the light source is not rigidly mounted to the device base, outside vibration can cause unintended signal generation.

Another family of shear stress sensors operate based on thermal principles and are commonly known as hot-film shear stress sensors. The core mechanism of these devices is the transduction of the heat transfer rate to voltage. The flow of particles across a boundary layer includes friction between the boundary and the flow particles, and thus there is heat generated as the particles interact with the boundary surface. A thermal shear stress sensor is composed of a given material with well-known relationships between temperature and resistance. In an ambient temperature environment, the material has a characteristic resistance, but when subjected to flow that exerts a shear stress on the device, it heats, causing a departure from the characteristic resistance. A schematic diagram of the hot-film sensing mechanism is shown below in Figure 1.3.

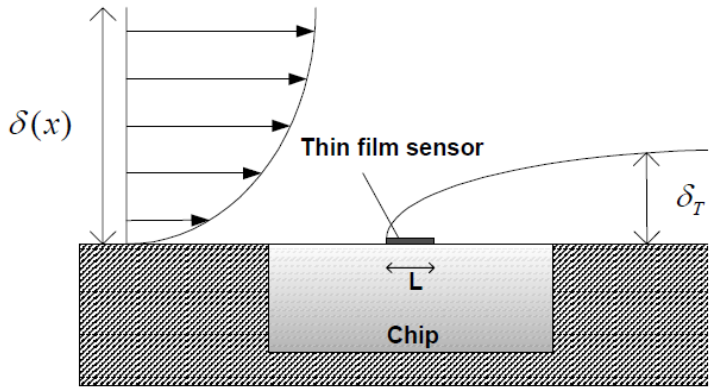


Figure 1.3. Basic diagram of functional mechanism for a hot-film shear stress sensor [1].

Unfortunately, there isn't a direct relationship between the shear force applied and the heating of the resistive element, and so it must be a measured empirical relationship [1]. These sensors also suffer from ambient temperature drift that can corrupt measurements, as well as interference from conductive heating of the device substrate. Further, thermal sensors can cause the unintended heating of the flow intended to be measured. Heating the flow particles can induce flow perturbations, causing additional measurement errors, as explained by Liu et al. in [10].

1.2 DC Shear Stress Sensor Operating Principle

The shear stress sensor developed in this document utilizes the following sensing mechanism: the device contains an array of "unit cells" or "sensing pixels" that are each comprised of three electrodes, two of which rest on the device substrate, and a third electrode resting on a thin, compliant dielectric film separating it from the bottom two electrodes. The third electrode's rest position is located between the two bottom electrodes such that there is a characteristic capacitance, C_1, between the top electrode and the first bottom electrode, and another characteristic capacitance, C_2, between the top electrode and the second bottom electrode (See Figure 1.4, below). In the ideal case, C_1 and C_2 are equal. When subjected to a shear force perpendicular to the electrode length, the compliant dielectric displaces, moving the top electrode closer to one of the bottom electrodes, causing a change in the capacitance, ΔC. The capacitances between the top electrode and the bottom electrodes change to $C_1 \pm \Delta C$ and $C_2 \mp \Delta C$. Since we anticipate small stresses and strains on the dielectric, we allow this simplified linear relationship of the capacitance changes.

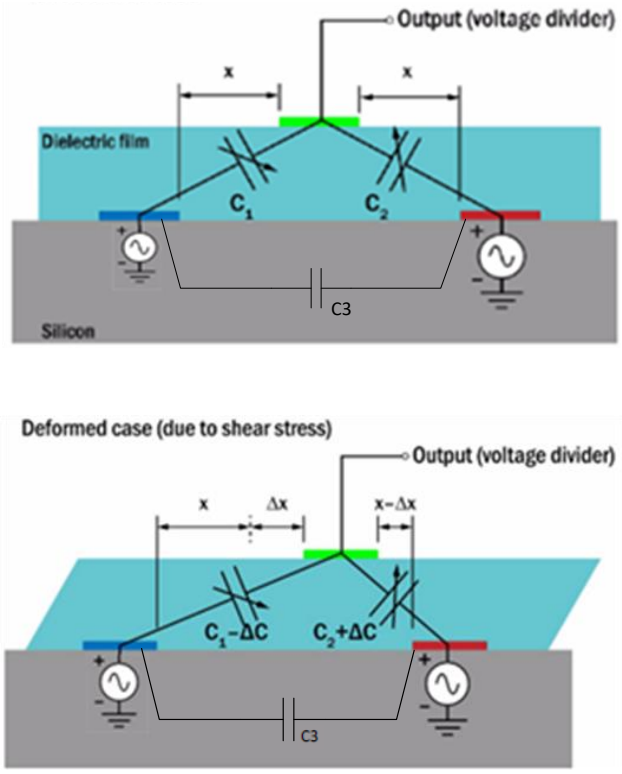


Figure 1.4. Schematic of DC shear stress sensor. (Top) Device in resting condition (bottom) Device under shear stress load.

To directly measure the shear stress of the device, the bottom two electrodes are biased with an alternating voltage, $+V_{ac}$ and $-V_{ac}$. These signals are labeled with the subscript "ac" to emphasize that they are alternating voltage signals, specifically sinusoidal signals, but could have also sensibly been labelled $+V_{bias}$ and $-V_{bias}$ to indicate their function as bias voltage signals. Assuming ideal alignment and equal characteristic capacitances C_1 and C_2, exactly half of the voltage drop will occur across the first capacitor, and the other half of the voltage drop will occur across the second capacitor, leaving a value of $\frac{1}{2}(+V_{ac} + -V_{ac}) = 0$ at the top electrode. However, when the shear force is applied, the top electrode displaces, causing the C_1 and C_2 values to increase or decrease slightly. This means that the voltage drop across the two capacitors is no longer

equal, and that a zero voltage is not expected at the top electrode. If sinusoidal signals $+V_{ac}$ and $-V_{ac}$ are applied to the bottom electrodes as previously described, and the top electrode is displaced, the voltage division is no longer equal and a sinusoidal signal would be expected at the top electrode output. A circuit model depiction of this mechanism is shown below in Figure 1.5. The value C_3 is the value of the capacitance between the two bottom electrodes via the silicon dioxide layer, and will also later include the peripheral wiring scheme's capacitance. When the wiring scheme is included, C_3 will be referred to as $C_{parasitic}$. These parasitic capacitances degrade device quality, but don't significantly alter the core functional mechanism of the sensor.

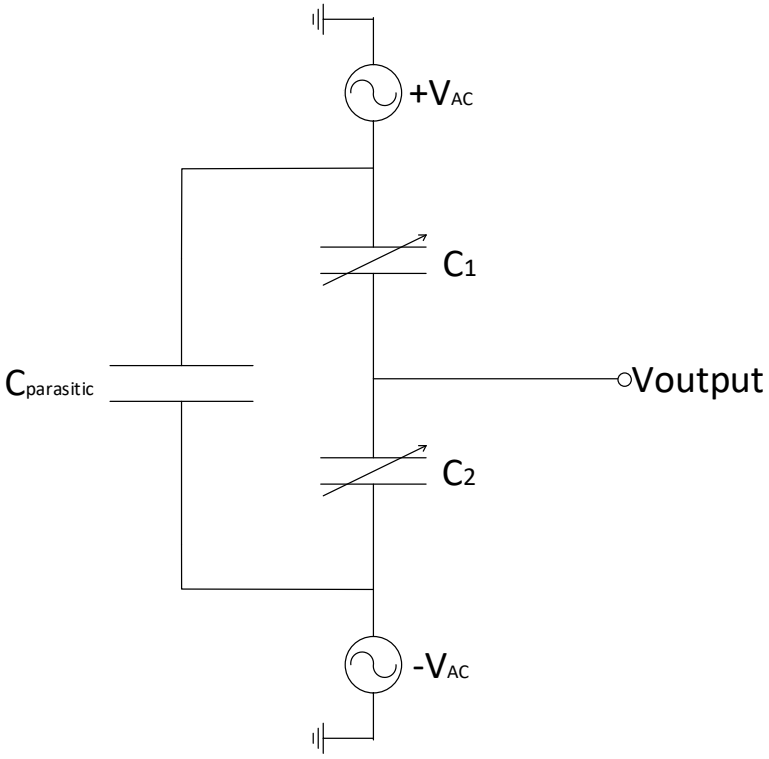


Figure 1.5. Circuit diagram used to model DC shear stress sensor behavior.

Alternatively, the positive electrode can be biased at V_{ac}, while the second bottom electrode can be grounded. When the same signal is applied, the voltage at the top electrode output will be the same waveform as V_{ac}, with half of the amplitude. Under shear, the top electrode signal would $\frac{1}{2}(V_{ac} \pm \Delta V)$, where ΔV is the change in voltage drop due to the non-equal capacitances due to deflection of the top electrode.

1.3 Previous Work on Shear Stress Sensor

The University of Texas Acoustic MEMS group has also developed two previous generations of the shear stress sensor device, and the device reported in this document is the third generation. The first and second generation devices both utilized piezoelectric sensing, and the primary advance from the first to second generation device was the decrease in the device dimensions from roughly 1cm by 1cm to 1.8mm by 1.8mm. In the rest of this document, comparisons will refer to the current third generation device to the second generation device, as these two devices share the same design and dimensions, but differ in materials and transduction mechanisms, as will be further detailed in Chapter 2. Both devices are comprised of unit capacitance cells, each of which has three electrodes. Two of the electrodes rest on the silicon substrate, while the third electrode rests situated between the bottom electrodes on top of a thin film. The previous device's electrodes were separated by a film of piezoelectric PZT-5H, thus enabling piezoelectric sensing. The current device's electrodes are separated by a compliant, dielectric film made of SU-8 photoresist, which enables differential capacitive sensing. Physically, the operational mechanisms are similar: a wall shear stress causes deformation and displacement of the top electrode from the resting position, however the transduction mechanisms are quite different. In the piezoelectric device, this deformation causes an electrical polarization directed between electrodes. The elongation of the piezoelectric

material causes an electrical potential signal that is proportional to the amount of shear stress at the surface of the device, as described by R.P. Williams et al. in [11]. An important aspect of the previous devices was the selectivity to normal pressure. As illustrated below in Figure 1.6, shear stress induces polarization in the piezoelectric film, while normal stress on the device does not produce a comparable output signal. This is due to the polarizations between the top electrode and each of the bottom two electrodes are of opposite polarity, such that normal stress generates potentials equal and opposite in value, cancelling the total signal. When developing future generations of the sensor, it was desirable to preserve this beneficial attribute.

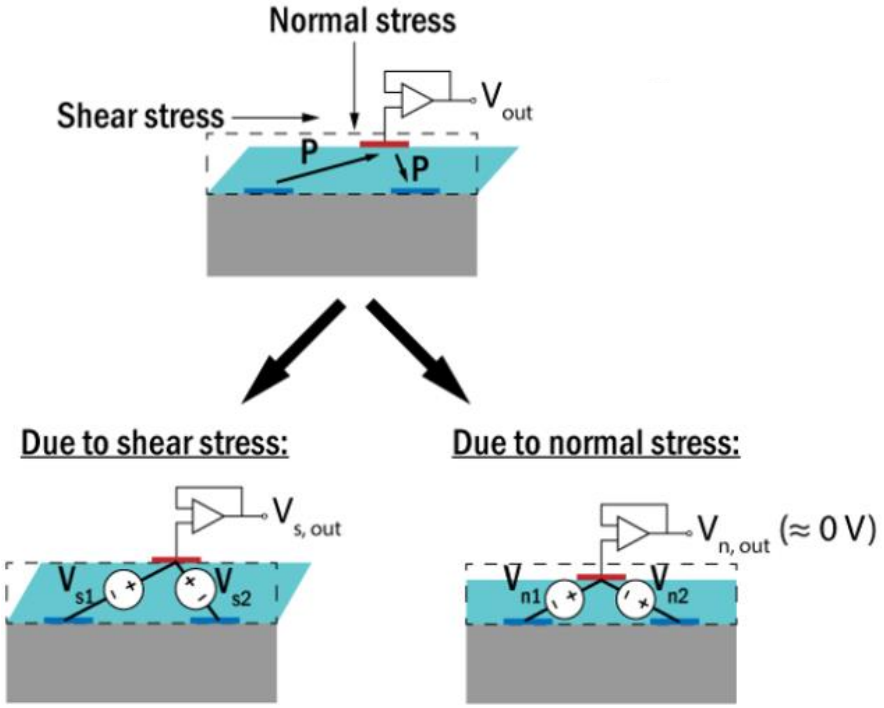


Figure 1.6. Diagram depicting shear stress sensor selectivity to shear stress and rejection of normal pressure [11].

The use of a piezoelectric film specializes the device to measure frequency-dependent wall shear stress. The design of the current generation device would be adapted to incorporate a dielectric film instead of a piezoelectric film, enabling a differential capacitive sensing mechanism in the third generation device, which is the subject of this document. By enabling the differential capacitive sensing scheme, we lose the benefit of the piezoelectric effect, but gain the ability to sense static DC shear stress. DC sensing was not possible with the previous generations that could only detect dynamic AC shear stresses, thus providing the motivation for the third generation device capable of differential capacitive sensing.

1.4 Organization of Thesis

This thesis is organized with the following structure: in Chapter 2, the design considerations and simulation efforts for the shear stress sensor are described and explained. In Chapter 3 provides a detailed description of the development of a viable fabrication process, concluding with the final successful fabrication recipe. Additionally, Chapter 3 describes the packaging of the devices for testing purposes. Chapter 4 then describes the testing method in which the device characteristics and performance were evaluated to characterize the device behavior and compare to the models' simulated behavior. Finally, Chapter 5 recaps the work conducted and outline the future work that will logically follow the successful implementation of this particular shear stress sensor.

Chapter 2: Design and Simulation

As mentioned in the introduction, a large amount of work had previously been done on MEMS shear sensors in the UT Austin Acoustics MEMS research group. The first generation of the device was a piezoelectric shear sensor that could measure dynamic shear stress. In the second generation of the device, the motivation was to scale down the device as to have a smaller overall footprint while maintaining the same functionality. This would also allow for greater spatial resolution in shear stress measurements. The original device measured about 1cm on a side, and the second generation device measured just 1.8mm on a side. Moving from the second generation to the third generation, the focus of this document, the goal was to emphasize differential capacitive sensing in order to enable the measurement of the static, or DC, shear stresses. From a high-level design standpoint, this simply meant swapping the piezoelectric PZT-5H layer out and replacing it with a suitable dielectric. Furthermore, the dimensions of the second generation device were satisfactory from a footprint standpoint. This meant that the photolithography mask set created for the second generation device could also serve as the mask set for the new, third generation differential capacitive shear stress sensor. The new device would therefore be a derivative of the second generation piezoelectric shear stress sensor. This defined the starting point for design and constrained the design parameters to materials selection and dielectric thickness. The new sensing mechanism also made it very important to correctly model and analyze the behavior of the device.

2.1 EXISTING DEVICES

The existing mask set contains six device variants that would be fabricated. The length and orientation of the unit sensing cell arrays differ among the three different shear sensor designs, but all of the devices employ 2µm or 4µm electrode traces, separated by a lateral distance of 2µm (See Figure 2.1). These three device variants with a 2µm or 4µm options constitute the six device variants that were fabricated. The first type of device, dubbed the "small area" device, simply consisted an array of unit cells connected in parallel, all running in the same direction for a length of 1300µm. As mentioned previously, a unit cell consists of two separate electrodes on the substrate, separated by a third electrode located between the two bottom electrodes, but separated by the dielectric film layer (See Figure 1.4). The variations on this type of device contained either 24 unit cells, with electrode traces 2µm in width, or contained 17 unit cells, with electrode traces 4µm wide. The schematic diagram of these devices can be seen below in Figure 2.2.

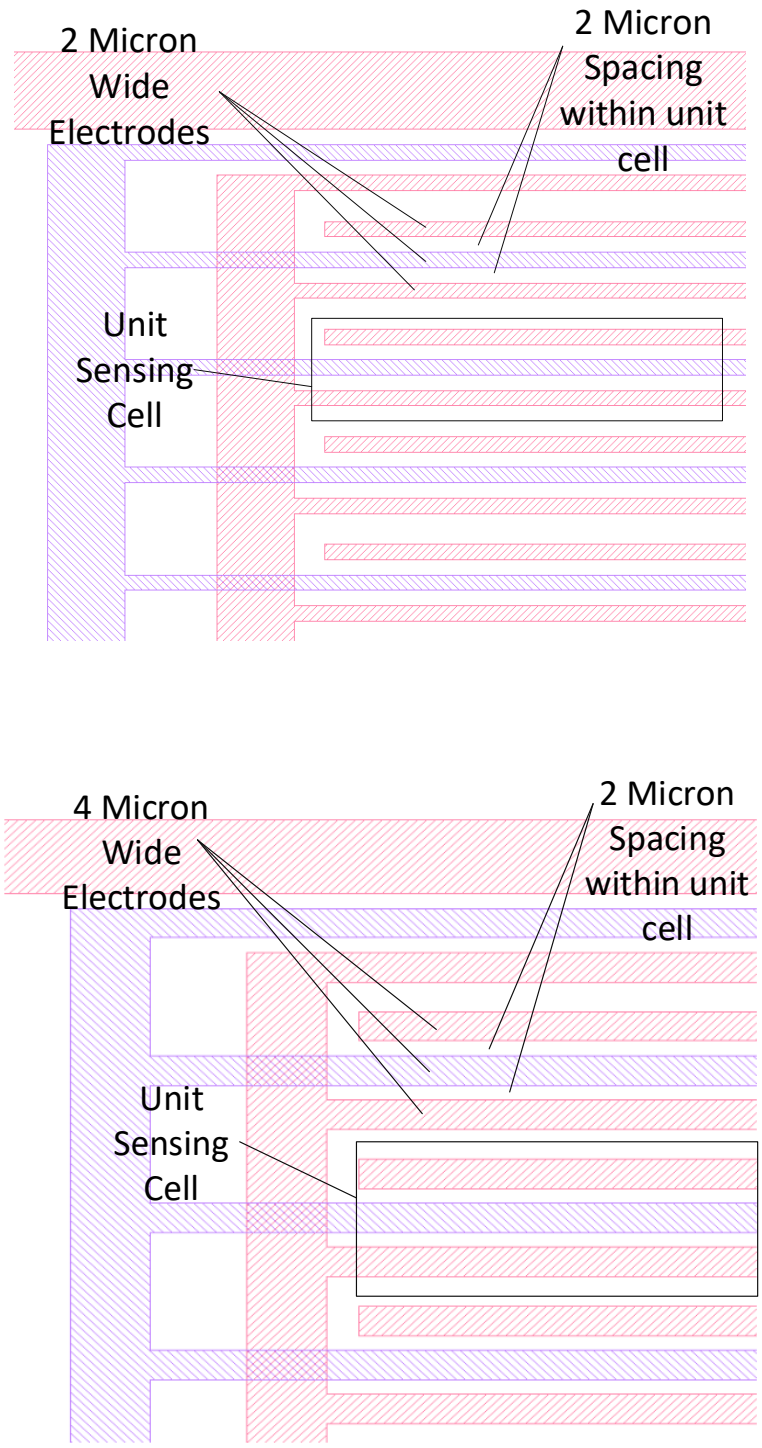


Figure 2.1. Sample sections of device schematic showing 2µm traces (top) and 4µm traces (bottom)

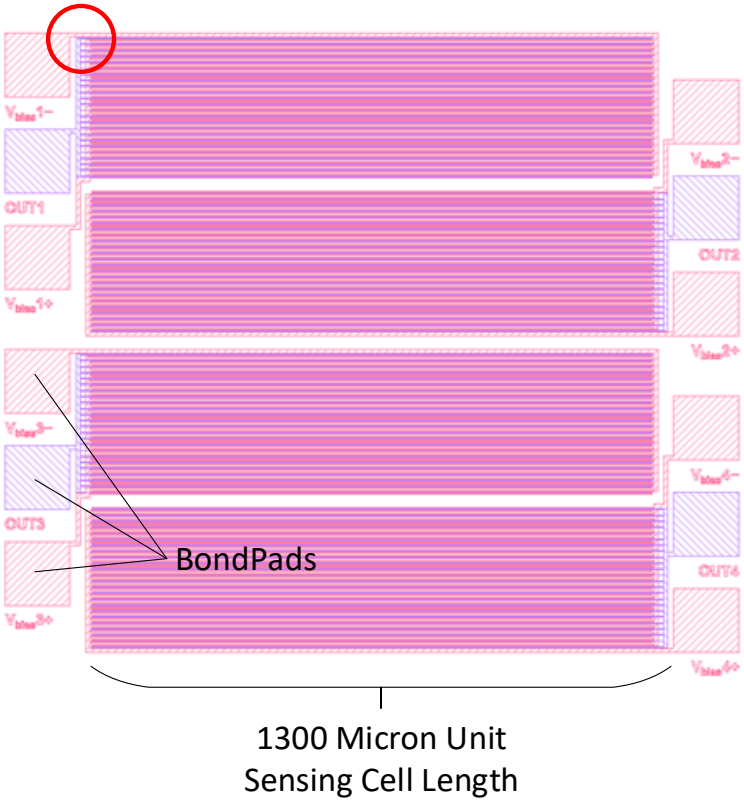


Figure 2.2. Schematic diagram of small area device. Note that there are four separate devices fabricated per die of this device. Circled in red is the region detailed in Figure 2.1.

The next device variant available in the second generation mask set was known as the "bidirectional" device, which consisted of quadrants of unit cells, with two such quadrants oriented perpendicular to the others, allowing for measurement of shear stress in two orthogonal directions. The two unit cell directions have their own separate electrical read out capabilities, meaning the device could be used to only measure one direction of shear stress if desired. This type of device has unit sensing cells 584µm in length. The bidirectional shear stress sensor schematic can be seen below in Figure 2.3.

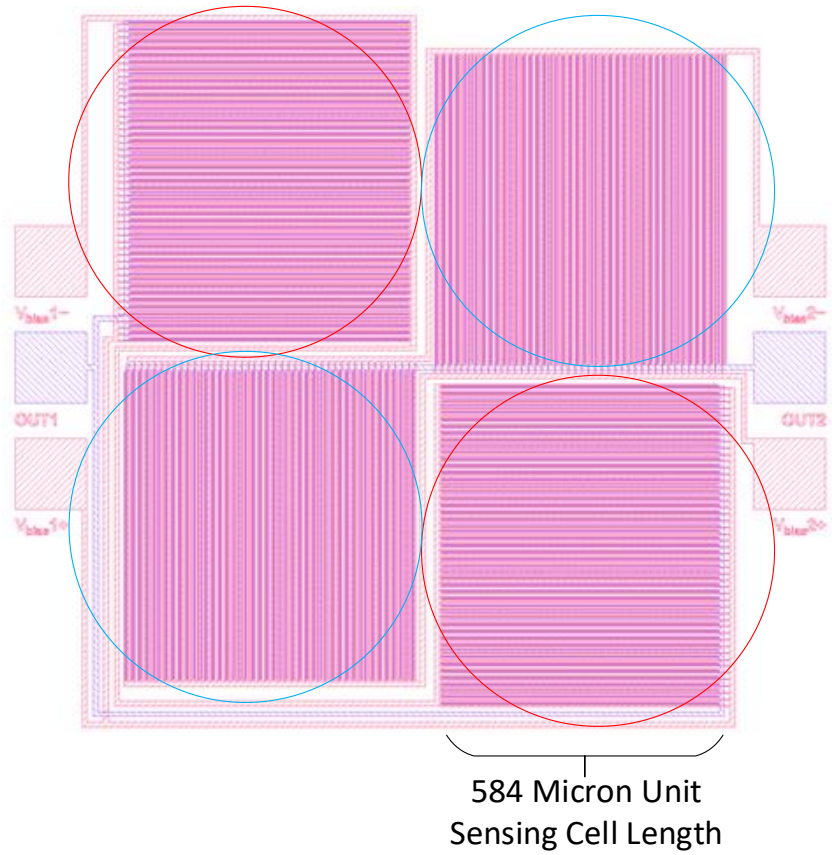


Figure 2.3. Bidirectional shear stress sensor capable of simultaneously measuring shear stress in two dimensions. Blue circles indicate cells for sensing first direction, and Red circles indicate regions for sensing second orthogonal direction.

The third and final shear stress sensor variant in the existing mask set, known simply as the "dot device", included a pressure sensor embedded into the device. The pressure sensor is located directly in the center of the device, and consists of two circular plates, one on the silicon substrate and one on top of the dielectric surface. Applied pressure causes the thickness of the dielectric to change, thus altering the capacitance of the capacitor formed by the two circular plates. This capacitor is surrounded by an array of unit capacitance cells, all of which are oriented in a single direction and are 1300µm in length. Although the pressure sensor was originally intended to be used with piezoelectric

films, the functionality is preserved with a dielectric film, and so these devices pose as viable candidates for fabrication as well.

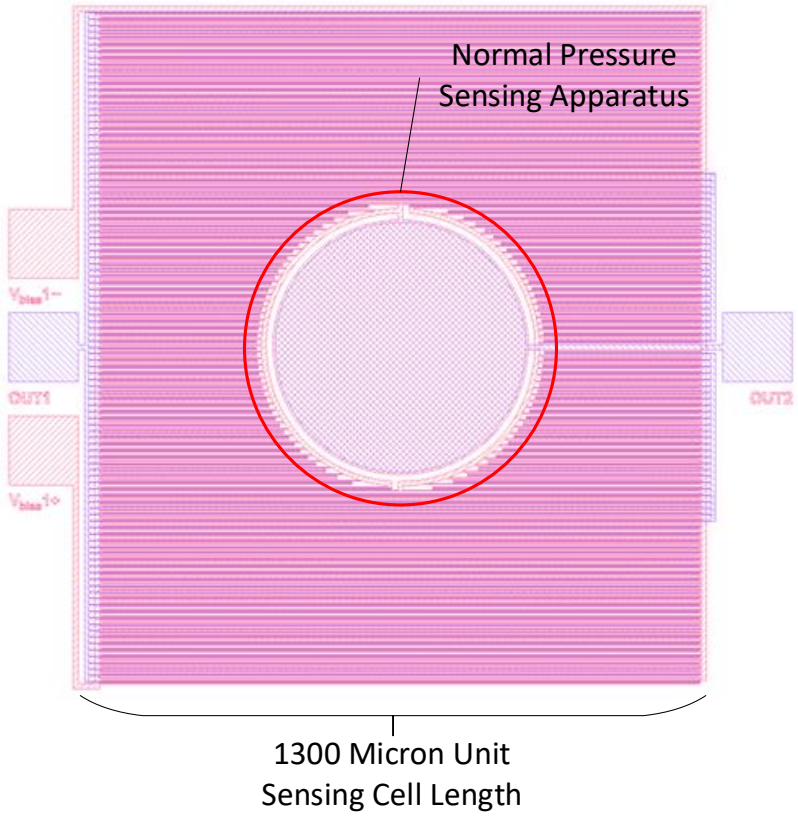


Figure 2.4. Shear stress sensor with added capability of measuring normal pressure. Circled in red is the area of the device used for sensing normal pressure.

In addition to the devices listed so far, the mask set included a simple parallel plate capacitor consisting of two circular plates roughly 1mm in diameter. These devices allow for accurate estimation of the relative dielectric constant of the film existing between the devices due to their consistency with the analytical solution for capacitance of a parallel plate capacitor. To allow proper characterization of the devices, the relative dielectric constant of the dielectric film material, SU-8 3005 negative photoresist, would

later be determined and validated using these devices. This information is presented in Chapter 4. A schematic of these devices can be seen below in Figure 2.5.

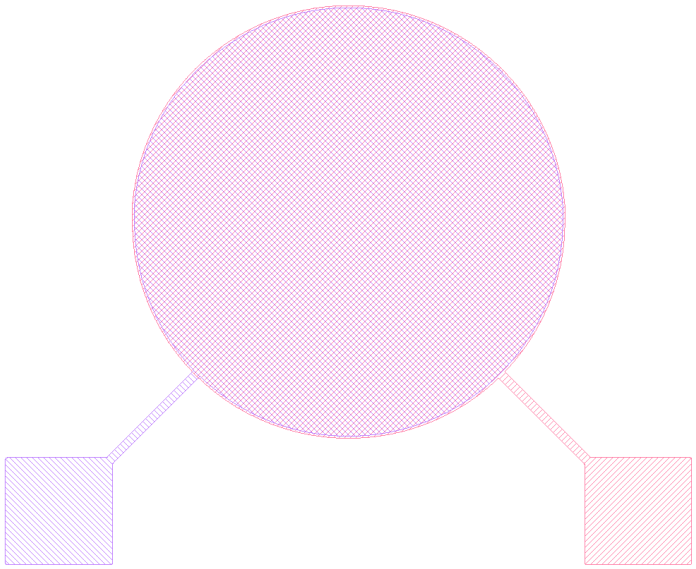


Figure 2.5. Basic schematic drawing of circular parallel plate capacitor used to measure relative dielectric constant.

2.2 Predicted Behavior

In order to determine the viability of the existing mask set as the mask set for a differential capacitive shear stress sensor, it was necessary to first thoroughly model the device. In particular, it was critical to obtain an estimate of the capacitance that would result from the devices being fabricated with a specific dielectric. Additionally, it was imperative to estimate how such a dielectric would deflect under a given shear force, and if the resulting change in capacitance due to the shear stress would be great enough to be detected.

The well-known equation for a parallel plate capacitor is the following:

$$C = \varepsilon_r * \varepsilon_o * \frac{A}{d}. \tag{2-1}$$

In this equation, C is the capacitance in Farads, A is the surface area of the device in square meters, d is the separation between the plates in meters, ε_0 is the permittivity of free space, 8.854×10^{-12}F/m, and ε_r is the dimensionless relative dielectric constant of the material between the capacitor plates. Given that pre-determined dimensions from the existing mask set were used, the value of A was fixed. However, the plate separation, d, and the relative dielectric constant, ε_r could be altered in our design based on material selections. In particular, a material that could provide a high ε_r and could be fabricated to a very thin separation would be optimal for maximizing the capacitance in our design. A familiar and readily available material in the UT Acoustic MEMS research group was MicroChem SU-8 photoresist, particularly the SU-8 3005 material. SU-8 is an epoxy-based negative photoresist that has the potential to be used as a permanent structure due to its ability to fully cross-linked via a hard baking process. The SU-8 3005 negative photoresist is designed to provide coatings with a thickness of 4-10μm, and the manufacturer offers the values of ε_r = 3.28 at 1GHz, a Young's Modulus of 2.0 GPa, and a Poisson's ratio, ν, of 0.22, which is needed to model the shear stress in the material [6, 13]. Although the dielectric constant was quoted at a frequency far greater than our anticipated biasing signal frequency, the value was still used as a starting point with the intention of later being replaced with a measured value from our own devices. Using SU-8 3005 as the dielectric film, a single unit capacitive cell was modeled to analyze the electrical properties. A nominal value of 4μm was used for the SU-8 thickness d in the above equation, as this would be the target thickness for the film to maximize the capacitance capability in the thickness range of 4-10μm.

2.2.1 Analytical Model

Prior to fabricating a device, it was necessary to predict the behavior of the devices via different modeling methods. This was achieved using both analytical and numerical modeling techniques. An analytical model has the goal of using known ideal equations to get a realistic estimate, accurate at least to the correct order of magnitude, of the resting capacitance, top electrode displacement, and sensitivity values associated with the devices. Given the complex geometry of the sensors, there is no exact analytical model for predicting their behavior, and so an idealized equation is used to create a simplified model with knowledge that it will not exactly predict the device's behavior. To supplement the imperfect analytical model, a finite element analysis (FEA) numerical model is helpful in accurately predicting behavior and validating the analytical models. The numerical model is presented in the subsequent section.

In the case of the shear sensor devices, the resting capacitance was the first value we were interested in predicting. From there, it was necessary to predict the deflection of the top surface of the dielectric SU-8 film under a given shear stress. With the electrode deflected, the analytical model can then predict a new capacitance. The change in capacitance, ΔC, is the difference between the resting capacitance and the capacitance when the device is deformed. The figure of merit for the devices is the sensitivity, M, and it is defined as:

$$M = \frac{\Delta C}{\tau} \tag{2-2}$$

In this expression, ΔC is measured in Farads, and τ is the shear stress on the device in Pascals. The first step in predicting the device behavior was to use an idealized analytical model that represents the capacitor-based devices. Because there is no analytical expression for a parallel plate capacitor in which the edges of the plates are not aligned, several methods were necessary to estimate the capacitance of such a

configuration. Every unit cell consisting of three electrodes had two capacitors of interest, but modelling a single capacitor was sufficient, as the other capacitor was expected to exhibit equal and opposite behavior under a given load. The first and most crude analytical model was to approximate the device capacitors as parallel plate capacitors that were in fact aligned, while preserving the separation of the plates as oriented in the real device. This approximation is illustrated below in Figure 2.6.

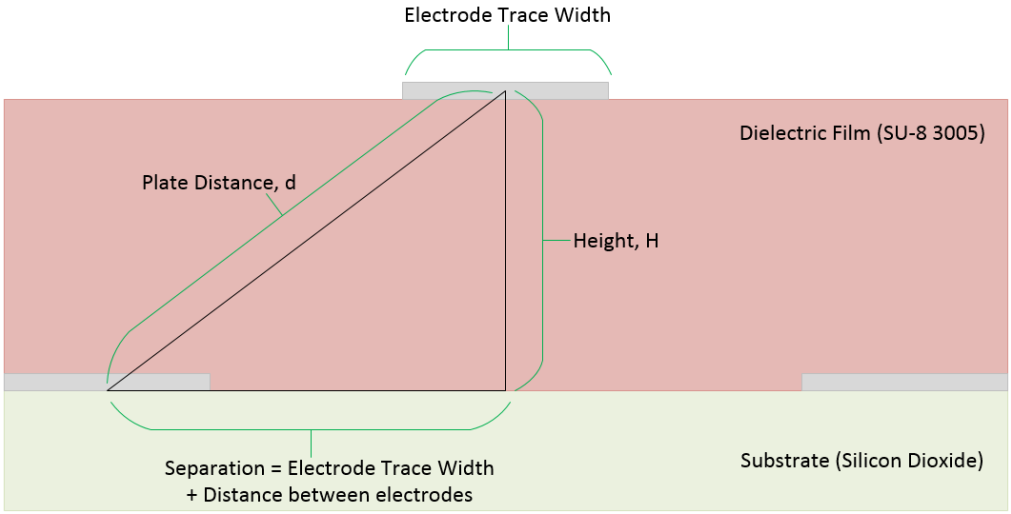


Figure 2.6. Unit sensing cell with labeled dimensions to be applied to ideal parallel plate capacitor capacitance expression.

In this model, the capacitance is given by the equation (2-2), where the area, *A*, is the region of the top electrode making contact with the SU-8 film, which is equal to the electrode trace width multiplied by the length of the unit cell. The separation distance, *d*, is distance from the center of the bottom electrode to the center of the top electrode. This model has the benefit of simplicity and ease of calculation, but fails to account for the offset orientation of the electrodes, as well as the non-uniform charge distribution that

results from the electrode orientation. Table 2.1 below shows the results for the analytical model for the devices on the existing mask set. The capacitance were calculated based on a single unit capacitance cell, then extrapolated to the specific orientation of the given device geometry. These predictions reflect the actual thickness of the SU-8 that was achieved in fabrication, 4.8 microns, rather than the original targeted value of 4 microns. Additionally, the measured SU-8 dielectric constant of 3.8 was used in place of the manufacturer's quoted value of 3.28 [6]. The MATLAB code used to calculate these values is given in Appendix A.

Device Type and Trace Width	Capacitance per Unit Cell [F]	Length of Unit Cell [μm]	Number of Unit Cells	Total Device Capacitance (Resting) [pF]
Small Device 2μm	1.400e-14	1300	24	0.336
Small Device 4μm	2.277e-14	1300	17	0.387
Bidirectional Device 2μm	6.289e-15	584	98	0.616
Bidirectional Device 4μm	1.023e-14	584	68	0.696
Pressure Enabled Device 2μm	1.400e-14	1300	105	1.470
Pressure Enabled Device 4μm	2.277e-14	1300	73	1.662

Table 2.1 Capacitances Calculated for Parallel Plate Capacitor Analytical Model

The next analytical model used was a parallel plate capacitor formed from a projection of the electrodes in their true orientation to the plane perpendicular to a line connecting the centers of the electrodes, slightly correcting for the misalignment that was

ignored in the initial model by adjusting the effective area of the interacting parallel plates. This projection is illustrated below in Figure 2.7.

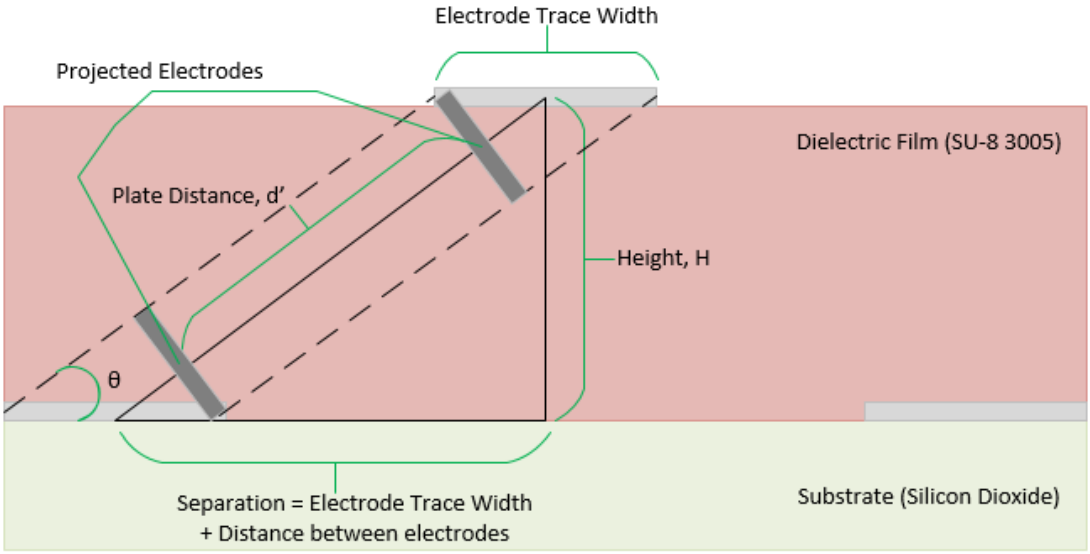


Figure 2.7. Schematic with "projected" capacitor plates and dimensions for model labeled.

Using this method, a new parallel plate capacitor is formed, in which the area of the plate, *A*, is given by:

$$A = L * W * \sin\theta \text{ ,} \tag{2-3}$$

Where L is the length of the unit cell into the page and W is the width of the electrode trace. The new distance between the plates, d', replaces d in equation (2-2) and is given in terms of the original separation, d, by the equation:

$$d' = d - (W * \cos\theta) \text{ .} \tag{2-4}$$

With these projected values, the original equation can be used to determine the capacitance of the imagined parallel plate capacitor. The benefit of this theoretical model is that it takes into account a smaller area of the electrode, which represents the effective area contributing to the capacitance. However, the charge distribution is still not taken

into account, and the electric field not directly between the plates is ignored. Despite these departures from the true device, the predicted values closely relate to those ultimately measured on the devices. Table 2.2 below shows the expected capacitances based on the projected parallel plate capacitor model for the different devices.

Device Type and Trace Width	Capacitance per Unit Cell [F]	Length of Unit Cell [µm]	Number of Unit Cells	Total Device Capacitance (Resting) [pF]
Small Device 2µm	1.353e-14	1300	24	0.325
Small Device 4µm	2.370e-14	1300	17	0.407
Bidirectional Device 2µm	6.077e-15	584	98	0.596
Bidirectional Device 4µm	1.077e-14	584	68	0.732
Pressure Enabled Device 2µm	1.353e-14	1300	105	1.420
Pressure Enabled Device 4µm	2.400e-14	1300	73	1.750

Table 2.2 Capacitances Calculated for Projected Parallel Plate Capacitor Analytical Model

Another alternative method for analytically predicting the capacitances of the device electrodes is to treat each electrode as a cylindrical wire with radius *a* and separation between wires *d*. The known equation for capacitance between two parallel wires of length *l* is given by the following:

$$\frac{\pi\varepsilon l}{\operatorname{arcosh}\left(\frac{d}{2a}\right)} = \frac{\pi\varepsilon l}{\ln\left(\frac{d}{2a} + \sqrt{\frac{d^2}{4a^2} - 1}\right)} \tag{2-5}$$

The most obvious fault in this model applied to the shear stress sensors is that the electrodes are not cylindrical in shape. Rather, they are rectangular with a nominal thickness of 0.1µm and a width of 2µm or 4µm. Thus, there is not a radius associated with this shape – using the thickness of the electrode greatly reduces the estimated size of the wire, while using the width greatly over estimates the size of the wire. As a compromise, the average of the two dimensions was used as the radius in our approximations. Despite this model's overt inaccuracies, it is helpful in assuring that our calculations are reasonable for the other models nonetheless. The estimated resting capacitances for the wire model are given below in Table 2.3.

Device Type and Trace Width	Capacitance per Unit Cell [F]	Length of Unit Cell [µm]	Number of Unit Cells	Total Device Capacitance (Resting) [pF]
Small Device 2µm	7.616e-14	1300	24	1.828
Small Device 4µm	1.082e-13	1300	17	1.840
Bidirectional Device 2µm	3.421e-14	584	98	3.353
Bidirectional Device 4µm	4.862e-14	584	68	3.306
Pressure Enabled Device 2µm	7.616e-14	1300	105	7.996
Pressure Enabled Device 4µm	1.082e-13	1300	73	7.900

Table 2.3 Capacitances Calculated for Wire Capacitor Analytical Model

The next step in estimating the sensitivity, *M*, of the devices was to investigate the expected deflection of the dielectric film under a given shear force. The relationship between the shear stress and the shear strain is given by:

$$\tau = \gamma * G \,, \tag{2-6}$$

$$G = \frac{E}{2(1+\nu)} \,, \tag{2-7}$$

and

$$\tau = \frac{F}{A} \,. \tag{2-8}$$

Here, τ is the average shear stress in Pascals, γ is the shear strain in radians, G is the shear modulus in Pascals, E is the Young's Modulus in Pascals, and ν is Poisson's ratio. For SU-8 3005, which was ultimately used to fabricate the devices, the Young's Modulus is 2.0 GPa and the Poisson's ratio is ν = 0.22, which yields a shear modulus of μ = 8.197×10^8, or 81.97 GPa. Setting τ equal to 1 Pascal, the shear strain γ is found to be 3.34×10^{-4} radians. The deflection of the top surface of the SU-8 3005, where the top electrode is located, is related to the tangent of the shear strain via the following equation:

$$\tan\gamma = \frac{\delta x}{H} \tag{2-9}$$

In this equation, δx is the deflection of the top surface of the dielectric film and H is the thickness of the film. Because the SU-8 is expected to deflect only a small amount and the resulting shear strain angle will be small, the small approximation for tangent can be used, where $\tan X \approx X$. This simplifies equation (2-9) to:

$$\gamma = \frac{\delta x}{H} \tag{2-10}$$

From which the deflection of the top surface of the SU-8 dielectric film can easily be seen to be:

$$\delta x = \gamma * H \tag{2-11}$$

If the thickness H of the SU-8 is assumed to be 4.8 microns (the true fabricated thickness, rather than the target thickness of 4.0 microns), the deflection due to 1 Pascal

of shear stress gives a shear strain angle of 1.22×10^{-9} radians and a deflection of 5.856×10^{-15} m, or 5.856 femtometers. This estimation is illustrated below in Figure 2.8.

Figure 2.8. Diagram labeling values used to determine the deflection of the top surface of the dielectric film due to shear stress.

With an estimated deflection due to a shear stress of 1 Pascal, it is possible to calculate a new capacitance of the device. The deflection is assumed to be in the direction perpendicular to the length dimension of the electrodes, meaning the top electrode has deflected towards one of the bottom electrodes by an amount δx. This new location of the top electrode slightly alters the capacitance between the top electrode and either of the bottom electrodes. In our model, we focus on the capacitance of the separation that increased by δx. To calculate the new capacitance, each of the analytical models was used again, taking into account the new separation distances of the electrodes including the deflections. Once the new capacitances for each analytical model were obtained, it is easy to calculate ΔC as the difference between the original capacitance and the new

capacitance. Finally, by trivially dividing by 1 Pascal, we can obtain the sensitivity for each analytical model. These results are listed below in Table 2.4.

Device Type and Trace Width	Parallel Plate Sensitivity [F/Pa]	Projected Parallel Plate Sensitivity [F/Pa]	Wire Model Sensitivity [F/Pa]
Small Device 2um	2.016e-22	3.675e-22	6.416e-22
Small Device 4um	2.304e-22	5.447e-22	1.010e-21
Bidirectional Device 2um	3.698e-22	6.741e-22	1.177e-21
Bidirectional Device 4um	4.139e-22	9.788e-22	1.815e-21
Pressure Enabled Device 2um	8.820e-22	1.608e-21	2.807e-21
Pressure Enabled Device 4um	9.892e-22	2.339e-21	4.338e-21

Table 2.4 Sensitivity Estimations for Analytical Models

With these expected sensitivity values, we were able to benchmark the viability of a differential capacitive shear stress sensor using our existing mask set and SU-8 3005 as the dielectric film. At first glance, a sensitivity on the order of 10^{-21} does not appear to be reasonable for any usable device. However, for testing purposes, it is easy to generate shear stresses on the order of kilopascals or even megapascals with a quite small object, due to the small cross sectional area of the sensing surface. Producing a shear stress on the order of 10^{6} Pascals is expected to yield a change in capacitance on the order of 10^{-15} F. While still quite small, this is not an unreasonable change as far as detection

capabilities go, as found by Ashrafi and Golnabi in [30], for example. In light of these analytical model predictions, we confirmed feasibility of a usable sensor and proceeded. Before fabrication, however, it was important to consult a more powerful representative model to validate the analytical predictions. For this, an FEA model was developed and tested.

It has been made clear that the operation of the device depends on C_1 and C_2, but a third capacitance, C_3, necessarily exists between the two electrodes resting on the SiO_2 surface. In order to provide a complete prediction of the device parameters, it was advantageous to further analyze this C_3 value, although it was known that this capacitance would not influence the device behavior. As seen below in Figure 2.9, C_3 can be subdivided into a capacitance and resistance occurring in the SU-8 dielectric, represented by C_d and R_d, in parallel with a capacitance and resistance in the silicon dioxide passivation layer, labelled C_{ox} and R. As seen in Figure 2.9, these values were viewed in a "per unit sensing scale" manner that could be extrapolated to deduce the value for a complete device.

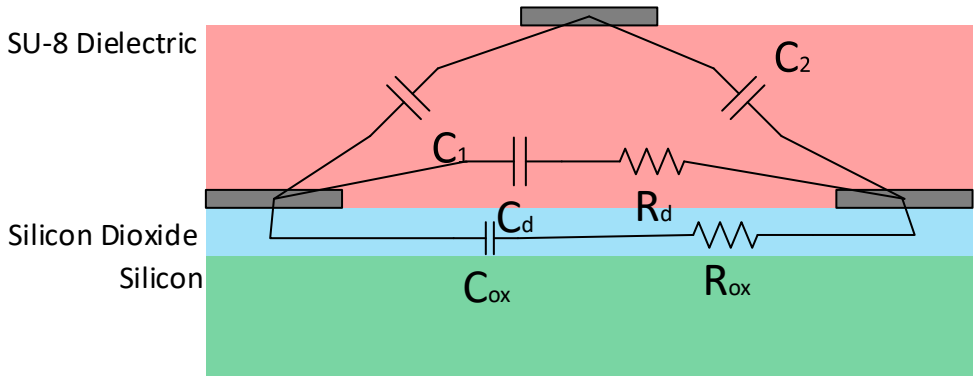


Figure 2.9. Hybrid schematic showing device structure with overlay of lumped elements, including parasitics.

In each unit sensing cell, the two bottom electrodes can be represented as coplanar strips, for which an analytical expression for capacitance exists:

$$C = \frac{\varepsilon_{eff} * l * K\left(\sqrt{1-k^2}\right)}{K(k)}, \tag{2-12}$$

where k is defined by:

$$k = \frac{d}{2w+d}. \tag{2-13}$$

Here, l is the length of the strips, $K()$ is the elliptical integral, d is the distance between the electrodes, and w is the width of the electrodes. The value ε_{eff} in the context of the shear stress sensor can be the SU-8 dielectric or the SiO_2, as the coplanar strips form a capacitor of this form in both materials. The relative permittivity found in the SU-8 during measurements shown in Chapter 4 is $\varepsilon_r = 3.8$, and the value for silicon dioxide is documented to also be roughly $\varepsilon_r = 3.8$. This means that C_{ox} and C_d will be equal, and their parallel connection will yield C_3, given by equation 2-12 above. In this simplified view, C_{ox} and C_d could be calculated from equation 2-12, with an additional factor of ½ to account for their occupancy of roughly half of the space forming the capacitance between the coplanar strips. Using equation 2-12 above, the predicted C_3 values could be calculated for each device variant. Here, C_3 represents the total capacitance formed by the two parallel capacitances formed through the two materials. These values are given below in Table 2.5. In addition to the capacitances that form C_3, there is a resistance that is present through the silicon dioxide passivation layer and a resistance in the SU-8. This resistance can be calculated using the equation $R = \rho * \frac{L}{A}$, where ρ is the resistivity of the material, L is the length of the resistor, and A is the cross sectional area of the resistor. Using a resistivity value of $\rho = 3 \times 10^{15}$ Ω•cm for SiO_2 and $\rho = 1.8 \times 10^{16}$ Ω • cm for SU-8, the value of R per unit sensing cell was calculated for each device. Because the unit sensing cells are in parallel, and each cell is presumed to have the same resistance,

the total resistance can be found by dividing this value by the number of sensing cells per device. This value is also presented in Table 2.5.

Device Type and Trace Width	Predicted total C_3 Capacitance [pF]	Resistance in SiO_2 [Ω]	Resistance in SU-8 [Ω]
Small Device 2µm	1.215	5.771e17	3.462e18
Small Device 4µm	0.979	1.086e18	6.335e18
Bidirectional Device 2µm	2.229	3.145e17	1.887e18
Bidirectional Device 4µm	1.759	6.044e17	3.626e18
Pressure Enabled Device 2µm	5.317	1.319e17	7.912e17
Pressure Enabled Device 4µm	4.204	2.529e17	1.475e18

Table 2.5 Parasitic Capacitances and resistances of Silicon Dioxide and SU-8.

As previously mentioned, because these elements are in parallel with those that define the device operating mechanism, C_1 and C_2, their presence does not impact how the device operates. The bias voltage signals are applied across the parallel components, and thus the presence of C_3 and the resistances does not impact the voltage divider formed by C_1 and C_2 and the differential capacitive scheme. It is was important to collect these value estimations, however, to have for points of investigation in the event that the device did not operate properly. With this task complete, the simulations could progress to the numerical phase.

2.2.2 Finite Element Analysis

The next step in predicting the behavior of the supposed devices was to numerically calculate the sensitivity, comparing the numerical prediction to the analytical prediction for validation. The finite element method is widely used to obtain numerical results for models of real world physical situations. FEA modelling involves breaking the entire domain of interest into smaller, simpler elements. These elements can be subjected to boundary conditions that give rise to solutions to the associated partial differential equations of interest, yielding a system of algebraic equations. These equations are then assembled for the entire domain. The solution to these equations are solved by minimizing error functions in the background of the computer program. In the UT Acoustics MEMS group, ANSYS Simulation Software and COMSOL Multiphysics Modeling Software are both frequently used for finite element method simulations.

Modifying the ANSYS model from the first generation piezoelectric manifestation of this device, a model was constructed with the code found in Appendix B. The model, seen below in Figure 2.10, represents one "slice" of a single unit sensing cell. In other words, this model only represents a fraction of a total device, and must be extrapolated to achieve predictions for a true device embodiment. The reason for approaching the model this way is primarily to allow for a model that can be executed by a normal computer system in a reasonable amount of time. The element size is 0.1μm, and so if the entire 1.8mm by 1.8mm device was modeled, the computation would become unwieldly. Thus, only a portion of the device is modeled and extrapolated to fit the device in its entirety. Additionally, since there are multiple embodiments of the shear stress sensor, it is beneficial to model a section that can be extrapolated to any of the device variations without changing the entire model.

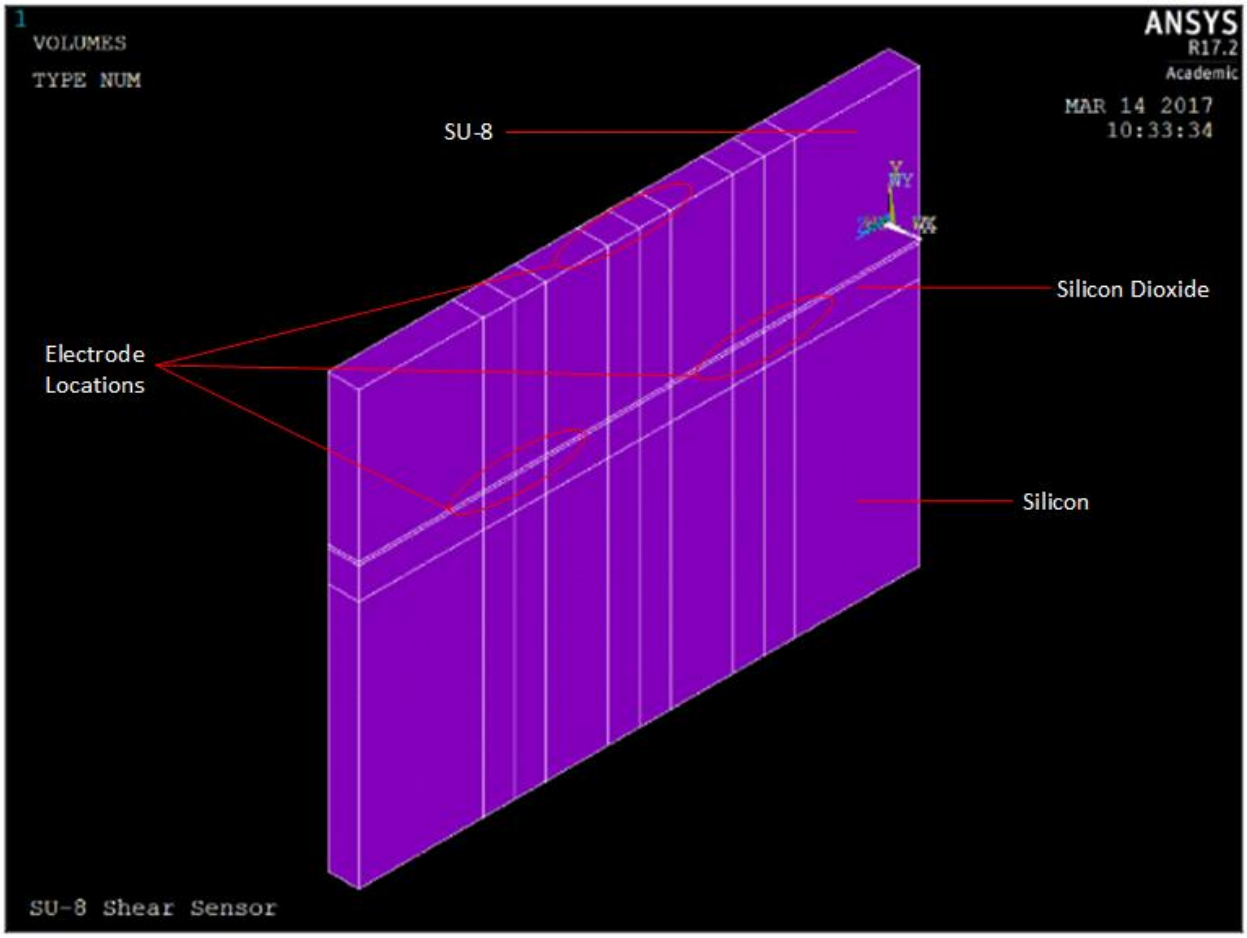


Figure 2.10. ANSYS Simulation of a small section of a unit cell used to predict device sensitivity.

The model was first used to calculate the resting capacitance per micron, which is then multiplied by the total length of all unit sensing cells in a particular device variant. The model was then used to calculate the displacement of the top surface of the SU-8 due to a 1 Pascal shear stress. To ensure the force was being applied in the correct direction, mechanical boundary conditions are imposed to restrict movement. Specifically, the SU-8 is held rigid where it meets the silicon dioxide substrate, and is additionally restricted to movement only in the direction perpendicular to the length dimension of the unit sensing cells. This is achieved by imposing a zero deflection boundary condition in the other two

orthogonal directions. The implicit assumptions of these boundary conditions are that the dielectric film will actually only deflect in the direction perpendicular to the sensing cell length dimensions, and that the deflection was a pure shear strain with no compression from normal pressure. These assumptions were accepted with the acknowledgement that they were idealizations, and that the physical devices would disobey these assumptions to some degree. The result of this simulation showed that a 1 Pascal shear stress resulted in 6.754×10^{-15}m of displacement, or 6.754 femtometers. New capacitance values from the model resulting from the shear displacement were obtained and thus the sensitivity M was obtained numerically. The capacitance, C, was determined by specifying the voltage, V, at each electrode, then using then simulating the resulting charge, Q, on each electrode. The capacitance was then simply calculated as $C = \frac{Q}{V}$. This calculation was repeated with the displaced top electrode to determine the change in capacitance. This method was used in both the COMSOL and ANSYS models. Table 2.6 below summarizes the different capacitances for each device embodiment found with the model, as well as the sensitivities for the two trace width variations.

Device Type and Trace Width	Total Device Capacitance (Resting) [pF]	Device Sensitivity [F/Pa]
Small Device 2µm	1.440	7.739e-22
Small Device 4µm	1.112	8.679e-22
Bidirectional Device 2µm	2.642	1.420e-21
Bidirectional Device 4µm	1.997	1.560e-21
Pressure Enabled Device 2µm	6.301	3.386e-21
Pressure Enabled Device 4µm	4.773	3.727e-21

Table 2.6 Capacitance and Sensitivity Values Based on ANSYS Numerical Model

Another software program, the previously mentioned COMSOL Multiphysics Modeling suite, was used to model the device in conjunction with the ANSYS model. The same exercises were executed to find the resting capacitance, the deflection due to 1 Pascal of shear stress, and the resulting change in capacitance due to the deflection. The model additionally applied increased stresses of 10, 100, and 1000 Pascals to confirm that the deflection increased linearly and thus the sensitivity was constant. Given the small deflections expected by the device, the both the COMSOL and ANSYS models were restricted to strictly linear geometric deformation. As expected, the sensitivity was nearly constant. An image of the COMSOL model is found below in Figure 2.11, as well as results for the simulation in Table 2.7.

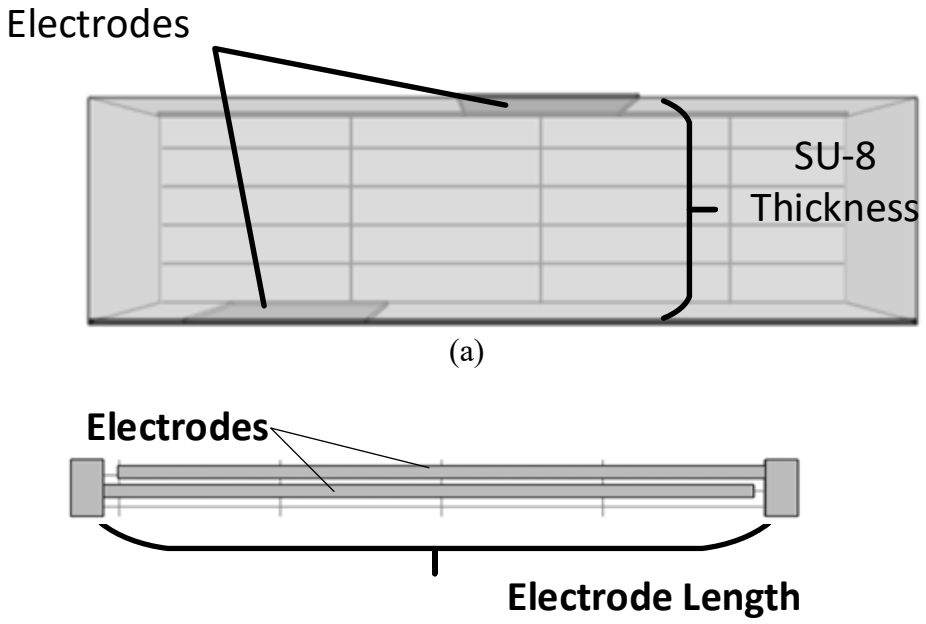


Figure 2.11. COMSOL model. (a) Cross sectional view showing two electrodes separated by dielectric and (b) top down view of same electrodes.

Device Type and Trace Width	Total Device Capacitance (Resting) [pF]	Device Sensitivity [F/Pa]
Small Device 2µm	0.920	5.010e-22
Small Device 4µm	0.754	5.211e-22
Bidirectional Device 2µm	1.688	9.190e-22
Bidirectional Device 4µm	1.355	9.364e-22
Pressure Enabled Device 2µm	4.026	2.192e-21
Pressure Enabled Device 4µm	3.239	2.238e-21

Table 2.7 Device Capacitances and Sensitivities Based on COMSOL Numerical Model

The COMSOL and ANSYS models predict results within the same order of magnitude, but have a non-negligible discrepancy in predicting the capacitances of the devices. However, upon inspecting the models, there are several contributors to the disparity between the two models. The ANSYS model incorporates the substrate beneath the SU-8 more completely, including the silicon dioxide layer, as well as a portion of the silicon wafer below. When the electrical conditions are imposed, the substrate is subjected to mechanical forces that can alter the capacitance between the electrodes. The COMSOL model only includes the SU-8 dielectric layer, and thus does not account for the effect of the substrate on the capacitance. Additionally, the ANSYS model includes a complete unit cell comprised of two bottom electrodes and one top electrode, while the COMSOL model only includes one bottom electrode and one top electrode. Moreover, the COMSOL model includes a small section of the electrode that would connect to the adjacent unit cell, adding another slight difference in the geometry of the capacitor. Due to the geometry of the unit cell, the complex electric field of one of the formed capacitors interacts with the electric field formed by the second capacitor. This interaction alters the capacitance value of each capacitor, and so by only incorporating one capacitor, the COMSOL model does not account for the effect of a second capacitor and thus changes the predicted capacitance value. The presence of these subtle differences accumulate and cause a slight variation in the predicted capacitance and resulting sensitivities of the models.

2.3 Model Comparisons

The analytical models provide an educated starting point for estimating the behavior of the device, despite the known assumptions that are taken that allow the use of ideal equations. It is known that the device does not truly represent an ideal parallel plate

capacitor or pair of wires, but the differences can be ignored for the sake of gaining an estimation of the order of magnitude of the relevant values of the device. The caveat is that the values must be taken with caution, as they do not accurately represent the true device. The device can be more accurately represented with a numerical model that utilizes finite element analysis. The analytical model can be used to benchmark the numerical model; if the values extracted from the models are of the same order of magnitude and closely agreeing, it is reasonable to confirm the numerical model is accurate can be used to predict the device behaviors. Table 2.8 below summarizes the results of the numerical and analytical models for comparison.

Device Type and Trace Width	Parallel Plate Sensitivity [F/Pa]	Projected Parallel Plate Sensitivity [F/Pa]	Wire Model Sensitivity [F/Pa]	ANSYS Model Sensitivity [F/Pa]	COMSOL Model Sensitivity [F/Pa]
Small Device 2µm	2.016e-22	3.675e-22	6.416e-22	7.739e-22	5.010e-22
Small Device 4µm	2.304e-22	5.447e-22	1.010e-21	8.679e-22	5.211e-22
Bidirectional Device 2µm	3.698e-22	6.741e-22	1.177e-21	1.420e-21	9.190e-22
Bidirectional Device 4µm	4.139e-22	9.788e-22	1.815e-21	1.560e-21	9.364e-22
Pressure Enabled Device 2µm	8.820e-22	1.608e-21	2.807e-21	3.386e-21	2.192e-21
Pressure Enabled Device 4µm	9.892e-22	2.339e-21	4.338e-21	3.727e-21	2.238e-21

Table 2.8. Sensitivities of Analytical and Numerical Models

Comparison of the models confirms the predictions of their validity. The analytical models, which include the most assumptions that are invalidated by the true device, show the most variance in their predictions: the wire model seems to overestimate the sensitivity as compared to the parallel plate sensitivity. The projected parallel plate model, which includes the most corrections to attempt to match it to the true device, compares quite well with the numerical models. As expected, the COMSOL and ANSYS numerical models are very similar in order of magnitude and quite close an absolute value as well. With this satisfactory agreement between all of the models both numerical and analytic, we were comfortable moving forward with the fabrication of the device, confident that we had accurately predicted its behavior. These estimates would also serve as the benchmarks for the device testing that is described in Chapter 4.

Chapter 3: Device Fabrication

The fabrication of the differential capacitive shear stress sensors can be broken into three major phases. In the first phase, an electrical passivation layer and the bottom electrode pattern is developed. In the second phase, the middle dielectric structure is constructed through photolithography techniques. In the third phase, the top electrode pattern is carefully developed as to achieve proper adhesion to the dielectric structures. In this chapter, a detailed look at the development of a successful fabrication process is examined, concluding with the packaging efforts that took place to prepare the device for testing. Appendix D, which illustrates the steps involved in this fabrication, will be particularly useful while reading this section.

3.1 Bottom Electrode

The initial step in the fabrication was the choice of substrate. The close proximity of the bottom electrodes introduces the possibility of significant signal leakage. For this reason, it was determined that an isolation layer on the substrate of the device would decrease the amount of leakage depending on the isolation layer material. The quoted nominal resistivity value for the undoped silicon wafers used for these devices is on the order of 1000-10,000 Ω•cm [15]. As these wafers become doped, the resistivity decreases, increasing the possibility of unwanted leakage. Since the wafers aren't perfectly pure, it was wise to electrically isolate the devices from the silicon substrate. A common material for such a passivation layer is silicon dioxide (SiO_2), given its high resistivity level. The nominal value of the resistivity of SiO_2 is roughly 3×10^{15} Ω•cm [14], which is much greater than silicon, leading to a lower leakage current between the bottom electrodes when placed upon SiO_2 rather than only silicon. Given this beneficial resistivity value and relative fabrication ease, SiO_2 was selected as our passivation layer.

3.1.1 Thermal oxidation

After a piranha clean to remove impurities present on the silicon wafer, a thin film of SiO_2 was thermally grown in an MRL Field Oxidation furnace. The following equation has been empirically developed for our specific furnace, and offers an estimation of the growth rate of the SiO_2:

$$T = 421.28 * t^{0.5472} \quad (3\text{-}1)$$

Where thickness T is in Angstroms and time t is in minutes. A thickness of 1μm was targeted, for which a growth time of 300 minutes or 5 hours is estimated. Several wafers were thermally oxidized, and the resulting SiO_2 film thickness was measured using a J.A. Woollam M-2000 DI ellipsometer and found to be around 0.97μm, just shy of the target of 1μm.

3.1.2 Bottom Electrode Lithography

After an electrical isolation layer is grown, the next step is to create the bottom electrode pattern. This is achieved with photolithography, metal deposition, and lift off. The wafer is first coated with an HMDS layer to promote the adhesion of the photoresist. This is achieved with a YES HMDS oven, which both dehydrates the wafer and applies the adhesion promoter coating. For this particular photolithography process, AZ 5214 positive photoresist was used [16]. The photoresist is applied by spin coating: roughly 5mL of the material is dispensed on the wafer and the wafer is spun at 3000 RPM for 30 seconds to yield a coating that is approximately 1.6μm thick. The photoresist coating is then soft-baked for 50 seconds at 110° Celsius. In the next step, the alignment and UV exposure of the photoresist coating is executed with a Karl Suss MA6 aligner. For this photoresist, it was previously determined that 13 seconds was an adequate exposure time [6]. When the exposure is complete, the photoresist pattern is developed in a solution that has a ratio of four parts DI water to one part AZ 400K. A properly developed pattern is

achieved after 22-25 seconds submerged in the developer solution. Given the feature size of the electrodes and spacing between electrodes, an over-developed photoresist layer can make the electrodes too wide, possibly causing unwanted electrode connections. If the photoresist coating is successfully developed, the wafer is ready for the first metal layer deposition.

3.1.3 Bottom Electrode Deposition

The selection of metal for the electrodes, both bottom and top, was motivated by cost and ease of fabrication. Since virtually any metal would satisfy the needs of the electrode, the material was selected based on what was available to fabricate rapidly and cost effectively. Two eligible candidates that met these criteria were Aluminum and Titanium. Titanium is available in the UT MRC clean room by DC Sputtering with a KJL sputterer, by DC sputtering with a Univex 450 sputterer, and possibly by other means such as CHA evaporation. Aluminum is also available for sputtering in the Univex sputterer. Initially, titanium was to be sputtered with the KJL sputterer, which can only process one wafer at a time. However, this process was much slower than using the Univex sputterer, which can process up to six wafers at once. The sputtering of aluminum in the Univex tool is done on a stage that is situated in close proximity to the sputtering target, which causes the substrate temperature to rise considerably during the sputtering, up to temperatures between 180° C and 200° C. This temperature is too high for the AZ 5214 photoresist layer, and the result is a corrupted and cracked photoresist layer that causes the metal to deposit directly on the SiO_2 in unwanted regions. The corrupted sputtered aluminum layer is shown below in Figure 3.1.

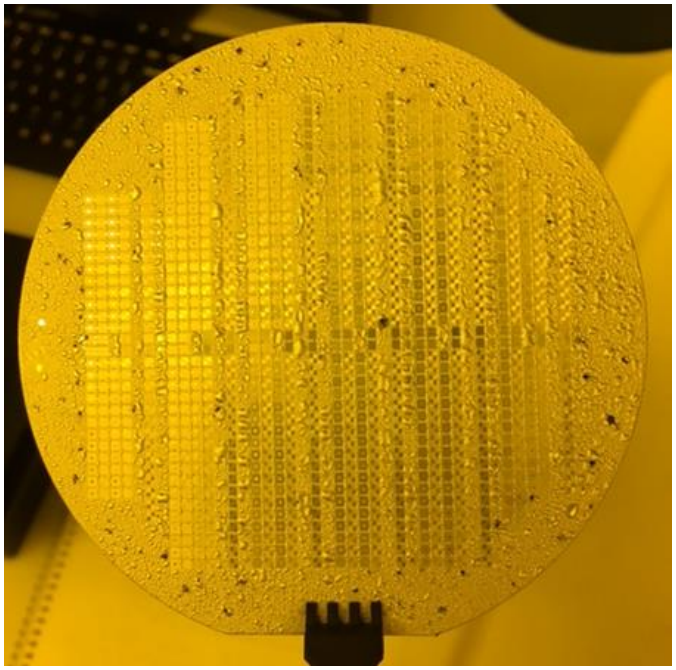


Figure 3.1. Attempted aluminum deposition via sputtering, corrupted by high temperature damage to photoresist.

Titanium was a suitable alternative for the unsuccessful aluminum sputtering. Additionally, it was observed by Dai et al. that titanium has been observed with the best adhesion strength to SU-8 when compared to other common metals such as chromium, copper, gold, and nickel [17]. This was beneficial to our fabrication both when promoting adhesion of the dielectric layer to the wafer, as the bottom electrode would already be in place, and when depositing the top electrodes later in the fabrication process.

While the stage for the aluminum deposition is roughly two inches from the sputtering target, the stage for titanium deposition has a larger distance between the target and the wafer, 6-7 inches. This results in less unwanted heating of the substrate due to the radiation of the sputtering, and thus the AZ 5214 photoresist can withstand the deposition conditions. Because the stage in the Univex sputterer rotates and handles up to six wafers, and we had no plan to change the stage rotation speed from 3 rotations per minute, it was

convenient to calculate the deposition thickness per rotation of the stage when estimating the deposition rate. In a standard recipe with 30sccm Argon gas flow and 325 W of power, the deposition rate was estimated to be 1.15nm per wafer per full rotation of the stage, specifically when the rotation speed was 3 RPM. This allowed us to avoid calculating the amount of time each wafer spent below the sputtering target per rotation.

Determination of the target thickness of the electrodes was based on successful previous devices. Devices within our research group had a typical electrode thickness around 100nm. The concern with the shear sensor device was that with topology on the wafer, subsequent layers that were applied via spin coating would be distorted due to features on the wafer. Electrodes with a thickness of 130nm were found to have a negligible effect on subsequent layers spun on top of them. For this reason, we targeted an electrode thickness of 100-130nm. With the known Univex 450 deposition rate, 32 minutes of deposition and a stage rotation of 3 RPM, a titanium layer thickness of close to 110nm was consistently achieved.

3.1.4 Bottom Titanium Lift Off

After the titanium sputtering is complete, the photoresist must be dissolved to remove the excess metal. This leaves behind the desired bottom electrode pattern on the wafer in what is known as "lift off". The traditional method for lift off is submerging the wafer in a solvent, usually acetone, for an extended period of time [18]. This allows the acetone to dissolve the photoresist, and release the metal that was on top of the photoresist. The acetone slowly creeps under the metal, and so the process may take several hours using the traditional method. The danger in this method is that small particles of metal may be lifted off and then re-deposited on the wafer. Our research group has an alternative method that allows for a faster lift off, leaving less time for metal

to possibly be re-deposited. In the alternative method, the wafer is placed in an empty beaker, which is then placed in an ultrasonication system. The system is turned on, which rattles the wafer for about 5 seconds, until acetone is poured in the beaker to submerge the wafer while the ultrasonication system continues to run for an additional 20-30 seconds. The rattling and ultrasonication fractures the surface of the unwanted metal, allowing acetone to penetrate faster to dissolve the photoresist. When there are no structures on the wafer that are sensitive to ultrasonication, this method is effective at quickly removing the unwanted metal and photoresist. However, it was found during later processes that some structures might be damaged by the ultrasonication, in which case the traditional lift off method must be used. Given the strong adhesion between SiO_2 and titanium, ultrasonication did not damage the bottom electrode patterns, and so the alternative method was used achieve clean electrode patterns, as shown below in Figure 3.2.

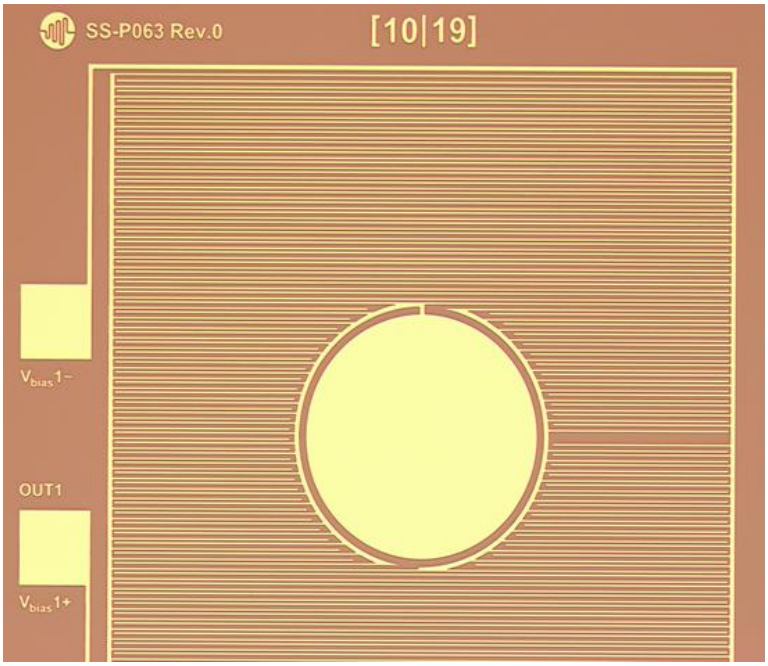


Figure 3.2. Successfully developed bottom electrode pattern achieved using lift off technique with ultrasonication.

Once a satisfactory bottom electrode pattern is achieved through lift off, various remnant particles of photoresist may remain on the surface of the wafer. It is wise to remove these particles away using oxygen plasma ashing at 300 W of power for about 60 seconds. Our tool of choice for this cleaning is the Nordson MARCH PX-250 Asher. This cleans the surface and removes unwanted particles, avoiding possible propagation of defects throughout the rest of the fabrication process, completing the creation of the bottom electrode pattern and preparing it for subsequent processing steps.

3.2 Dielectric Middle Layer

The next step in the fabrication process is the development of the middle dielectric layer. This layer must be stable enough to withstand a shear stress without being fractured, and compliant enough to displace a detectable amount from said shear

force. Photoresist polymers offer a viable option for this layer. Photoresists are compliant and can be shaped into desired structures via photolithography. SU-8 photoresist, specifically, has the beneficial capability of being cured with hard-baking to produce permanent device structures that are robust to chemical exposure and can withstand mechanical forces. Additionally, SU-8 is a negative photoresist with high aspect ratio capabilities. Specifically, MicroChem SU-8 3005 negative photoresist [6] was selected for use, as it could be spun to a thickness suitable for our devices - targeted at 4μm. As a negative photoresist, the regions of the coating exposed to the UV light are cross-linked and do not dissolve in developer, whereas a positive photoresist is dissolved by developer in the regions where the UV exposure occurs. This is key to the fabrication of this device, as in later steps when AZ 5214 lithography must be processed on top of the SU-8, the mask patterns are aligned such that areas of SU-8 that are exposed to UV radiation a second time are regions designed to be permanent. This means that the doubly exposed SU-8 simply receives an extra dosage of radiation without disrupting the structure in any way. If the middle layer were a positive photoresist, this process would not work correctly. Challenges with this layer were associated with adhesion of the SU-8 to the SiO_2 substrate and finding a viable way to process the SU-8 such that the top AZ 5214 lithography in subsequent processing steps was possible.

3.2.1 Exclusion of Hard Baking and Postponed Development

The initial fabrication plan did not include the hard baking step of the SU-8 processing that would ultimately be needed in the final design. The intention was to keep the dielectric layer as compliant as possible, and curing the SU-8 naturally increases the stiffness of the layer. A brittle middle dielectric layer will have a smaller displacement for a given force, and so hard baking was avoided. After an acetone, methanol, and

isopropyl alcohol (AMI) cleaning, the wafer was dehydrated for 2 minutes on a 100° C hot plate. After cooling the wafer, SU-8 3005 was then spun directly on the SiO_2 and titanium surface. The photoresist is spun at 4000 RPM for 40 seconds to yield a target thickness of 4μm. The wafer is then soft baked at 95° C for 3 minutes before exposure. The mask alignment and exposure is done with the same Karl Suss MA6 aligner. The initial exposure time was 8.5 seconds. This is a shorter exposure than the 13.5 seconds the SU-8 3005 datasheet suggests, as we did not want to over expose a thin layer and lose feature details. It would later be decided that since the feature sizes were large and the SU-8 edges did not have high precision features that over exposure was beneficial. After the exposure, the wafer undergoes a post-exposure bake (PEB) to fully crosslink the SU-8. This baking occurs at 95° C for 3 minutes. After the PEB, the pattern is visible on the SU-8 film.

As previously mentioned, spin coating a layer of photoresist on a surface with existing topology such as developed SU-8 structures causes non-uniform thickness coatings that may cause fabrication problems. In an attempt to preserve a planar surface on which the top coating of AZ 5214 could be applied, the development of the SU-8 layer was postponed. Instead, the SU-8 would be processed through the PEB step, at which point the SU-8 development would be skipped and the rest of the fabrication steps would be executed. It was anticipated that the AZ 400K developer could develop the AZ 5214 and the SU-8 simultaneously. This method would suffice, as the only areas exposed to the developer would be the UV exposed AZ 5214 photoresist. If the SU-8 was not developed with the 5214, it was anticipated that it would remain un-developed until the top electrode lift off, when the acetone would develop the SU-8; this was also a suitable outcome.

When this fabrication recipe reached the lift off step of the top electrode, the delamination of the SU-8 layer from the substrate was observed seconds after the wafer was submerged in the acetone. This was initially interpreted as an adhesion problem between the SU-8 and the SiO_2 substrate, and so it was addressed as such. However, another mechanism for the failure was the underexposure of the SU-8 layer. With a negative photoresist in which the UV exposed regions are cross-linked, the linking begins at the surface where the light initially makes contact with the film, and progresses towards the substrate. If the SU-8 coating is under exposed, the region making contact with the SiO_2 substrate is not cross linked, and thus it can be dissolved by SU-8 developer or acetone. This phenomenon has been noted across various sources on the internet [19]. This issue is illustrated below in Figure 3.3.

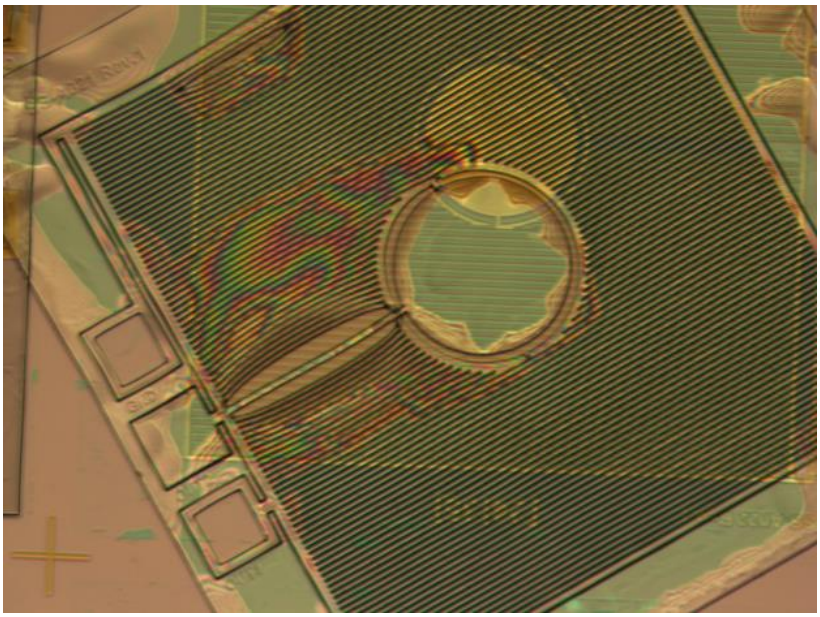


Figure 3.3. Delamination of SU-8 Structures due to under exposure and/or poor adhesion.

If the SU-8 is underexposed when the fabrication reaches the top lift off step, the acetone will dissolve the region of the SU-8 in contact with the SiO_2 and the devices will be delaminated. To fix this problem, the SU-8 was heavily over-exposed, noting that the devices could only benefit from being exposed longer than needed. An exposure time of 20 seconds was settled upon for later fabrication attempts.

The delamination problem was initially interpreted as an adhesion problem between the SiO_2 and the SU-8. Previous experience suggested that the introduction of MicroChem's adhesion promoter, OmniCoat, which is designed for use with SU-8 photoresists, can solve adhesion problems. This was the primary candidate for addressing the delamination issue, and the secondary potential solution was to use plasma activation to prepare the SiO_2 surface to promote better adhesion. Particularly, O_2 plasma activation temporarily converts the SiO_2 layer from hydrophobic to hydrophilic, as found by Zhao et al. in [22]. We anticipated that a hydrophilic surface would be more ideal for creating a better bond between the substrate and the SU-8 during spin coating and processing.

The first attempt at addressing the delamination issue was the introduction of OmniCoat, which is a solvent-based liquid that is spun and baked onto the wafer before the SU-8. Because the liquid has a very low viscosity, it only produces a film layer of about 5-10nm per spinning, when spinning at 3000 RPM for 30 seconds. A film thickness of at least 17nm is suggested in order to have an effective adhesion promotion layer. This means that three layers applied sequentially provides an adequate film thickness. Each individual layer must be baked for 60 seconds at 200° C after spin-coating. The SU-8 is then processed as normal on top of the OmniCoat. To isolate the effects of the OmniCoat addition, the SU-8 development was again postponed until the lift off step near the end of the fabrication. In this second attempt, there was improvement in the adhesion of the SU-8. However, using the traditional lift off method of extended acetone soaking, it was

observed that after more than an hour of soaking, the SU-8 structures again began to delaminate. Additionally, it any ultrasonication treatment was used during lift off, the devices immediately delaminated. A separate wafer was processed similarly, introducing the additional plasma treatment, however no significant improvement in adhesion was observed. It was at this point that it was determined that exclusion of the hard baking step was not a viable option, and the efforts shifted to processes including the SU-8 hard bake curing.

3.2.2 Inclusion of SU-8 Hard Bake and Immediate Development

With the introduction of the hard baking of SU-8, several other process steps were forced to change. Most importantly, the development of the SU-8 could no longer be postponed until the top AZ 5214 development or until post-lift off. Hard baking of the SU-8 is achieved at temperatures between 150-200° C for 15 minutes or longer. SU-8 begins to crosslink due to thermal exposure at 120°, and therefore if the SU-8 was not developed before hard baking, the entire coating would become permanent and no structures could be realized. Thus, the SU-8 must be processed traditionally, with the hard bake step following development. After processing the SU-8 through the PEB step as described above, including OmniCoat pre-coating, the SU-8 is developed by submerging the wafer in SU-8 Developer (1-Methoxy-2-propyl acetate) for 1-2 minutes. When removing the wafer from the developer, it must be spraying with isopropanol, and it is also beneficial to submerge the wafer in an isopropanol bath for 1-2 minutes to remove any small remnant particles. Early in the fabrication process, the wafers were mistakenly rinsed with DI water instead of IPA, creating a ‘droplet’ type defect, which can be seen below in Figure 3.4.

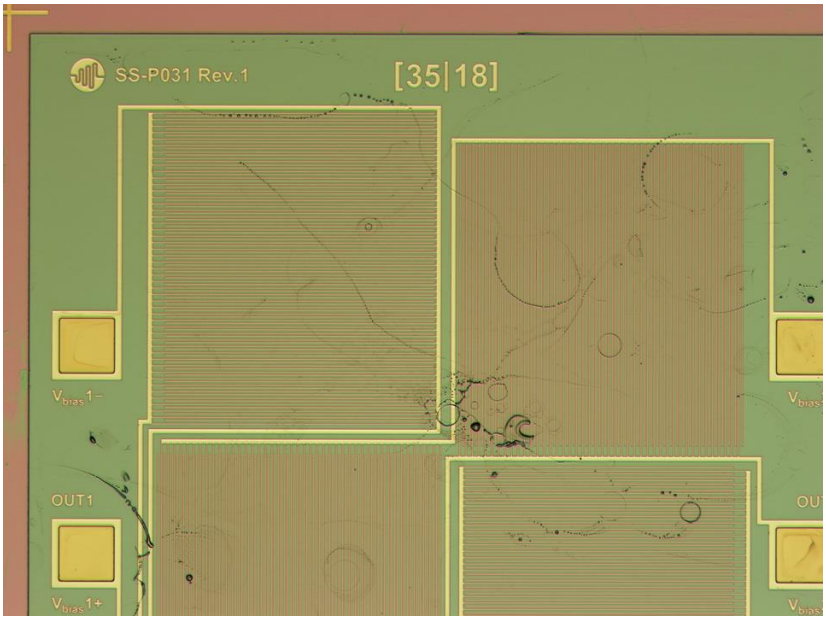


Figure 3.4. SU-8 Surface defects caused by improper DI water rinse instead of IPA rinse.

As long as the wafers are rinsed with IPA, this defect does not occur. After rinsing the wafer thoroughly with IPA, a DI water rinse and dry is appropriate. The wafer is then prepared for hard baking. For SU-8, a 4μm film is relatively thin, and so hard-baking does not need to be as long. Using [6] as a reference for temperature, it was found that hard baking for 15 minutes at 160° C was sufficient. placing the wafer on a hot plate around 70° C and ramping up to 160° in about 15 minutes, hard baking for 15 minutes, and then ramping back down to below 70° before removing the wafer from the hot plate was a suitable procedure. The procedure also left no signs of chipping or cracking of the SU-8, which had been observed in trials when no ramp up and ramp down were used.

As mentioned previously, the two main concerns with hard baked SU-8 were surface topology making subsequent spin coating difficult and the loss of compliance in the hard baking reducing the possible displacement due to shear force. In the processing

steps following the hard bake curing, the effect of the topology on the top layer spin coating would be revealed.

3.3 TOP ELECTRODE

The first challenge in developing the top electrode involved obtaining a viable photoresist layer by spin coating in the presence of surface topology from SU-8 structures. However, the more prominent challenge became effectively depositing metal on the dielectric with adhesion strong enough to remain in place. Learning about these issues came from both the original process without the hard baking step, as well as the method including the hard bake curing.

3.3.1 Metal Deposition Attempts Without Hard Bake

With no hard bake step executed, the process of developing top electrodes began with the photolithography of AZ 5214. Because the undeveloped SU-8 provided a flat surface to apply the 5214, the processing of the AZ 5214 photoresist was the same as for the bottom electrode. The photoresist is spun on at 3000 RPM for 30 seconds, followed by a soft bake for 50 seconds and 110° C. UV exposure with the MA6 lasts 13 seconds, and development occurs for 22-25 seconds in an AZ 400K and DI water mixture with a 1:4 ratio, respectively.

There was concern about how undeveloped SU-8 would be affected by AZ 400K developer. Although the composition of SU-8 developer (1-Methoxy-2-propyl acetate) and AZ 400K (Potassium borates) aren't related, it was unknown if the corrosive nature of the AZ 400K would unintentionally etch the SU-8. After development of the AZ 5214 photoresist, the top electrode pattern was very faintly visible, as seen below in Figure 3.5.

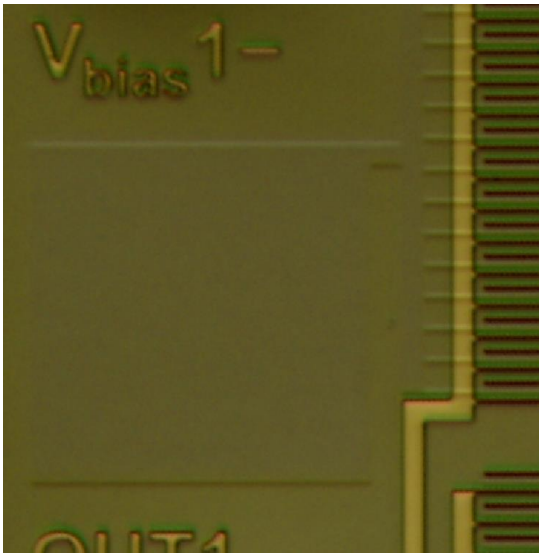


Figure 3.5. Developed AZ 5214 coating on top of SU-8. Pattern is present but can only be faintly seen.

It was not evident at this point if any corruption of the SU-8 from the AZ 400K had occurred, so we proceeded to the deposition of the top electrode metal. The same 32-minute Univex 450 titanium deposition was executed and the first attempt at top electrode lift off was the next processing step. The wafer was submerged in acetone, and it was obvious that the metal was not adhering to the SU-8 regions, as the titanium was peeling off of the wafer in large continuous sheets, leaving nothing on the wafer. This wafer was examined under the microscope, and it appeared that the pattern for the 5214 photoresist layer still remained. Because the acetone removed all of the AZ 5214 during lift off, the presence of the pattern after lift off suggested that the AZ400K developer had etched into the SU-8 during the top electrode lithography development. This side effect can be seen below in Figure 3.6.

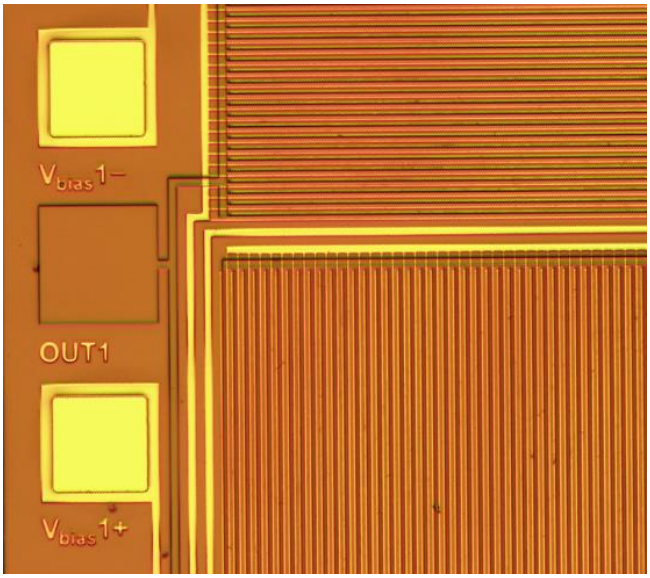


Figure 3.6. AZ 5214 top electrode pattern remaining after AZ 5214 removal, suggesting AZ400K developer was unintentionally etching SU-8 structures.

Further evidence of this etching was found on separate wafers in which the same process was followed with the addition of a short amount of ultrasonication during lift off. The metal was still completely removed, but it was also seen that areas of SU-8 that were meant to have no topography were being ripped into uniform slices by the ultrasonication, suggesting that the AZ400K had etched trenches into the SU-8, and the ultrasonication had fractured the trenches. This can be seen below in Figure 3.7.

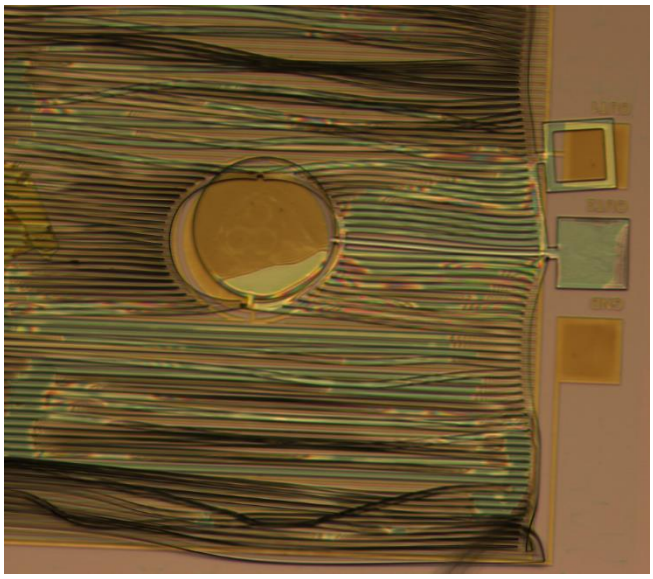


Figure 3.7. Long strands of separated SU-8 structures suggest AZ400K etching of SU-8, creating weak regions that are fractured during ultrasonication.

The more concerning result of the initial metal depositions was that no metal was sticking to the SU-8, whatsoever. This was one indication that hard baking the SU-8 may be necessary. First, however, a quick test of the effect of plasma treating the SU-8 surface was conducted. The O_2 plasma can increase the surface roughness of the SU-8, possibly enhancing the adhesion between the metal and the dielectric, as suggested by Kilchenmann et al. in [20]. Repeating the fabrication process with the addition of the plasma treatment of the SU-8 before the application of the AZ 5214 coating yielded no noticeable increase in adhesion: nearly all of the metal lifted off and left no top electrode pattern on the wafer.

Having no metal adhere to the wafer, as well as evidence that the AZ400K developer was corroding the dielectric layer, it was evident that hard baking the SU-8 would be necessary. It was surmised that curing the SU-8 would increase its tolerance to chemicals such as the AZ400K, and possible enhance the adhesion of deposited metals.

3.3.2 Metal Deposition Attempts With Hard Bake Curing

Initial attempts at metal deposition on hard baked SU-8 occurred with the presence of an OmniCoat adhesion layer below the SU-8. The SU-8 was hard baked according to the aforementioned ramp up recipe, starting around 70° C, ramping up to 160° C, curing for 15 minutes, and letting the wafer cool on the hotplate until a temperature less than 70° C was reached.

When spinning the top 5214 photoresist, the potential for distortion due to the SU-8 topology was possible. For this reason, the 5214 processing recipe was slightly modified to ensure thorough coverage of the features. The amount of photoresist poured on the wafer exceeded the standard amount, making sure that all features of the wafer were covered prior to spinning. Additionally, the spin speed was decreased from 3000 RPM to 2000 RPM, while the duration of the spin coat was still 30 seconds. While there were axial streaks observed where the AZ 5214 where the SU-8 features distorted the coating, the coating appeared to be sufficiently uniform. The parameters for exposure and development of the AZ 5214 layer were kept the same. Similar to the case for the SU-8 without hard baking, the top electrode pattern could only faintly be seen on top of the SU-8. Using the same titanium metal sputtering recipe with the Univex 450 DC sputtering tool, a 32-minute deposition was executed. In order to focus on the effect of the hard baking on the adhesion of the metal, the traditional lift off technique was used. After an acetone soaking period, it was evident that the electrode pattern was partially adhering to the SU-8. While there was not a viable electrode pattern, an improvement was observed, suggesting that cured SU-8 was a move in the correct direction. This result is shown below in Figure 3.8.

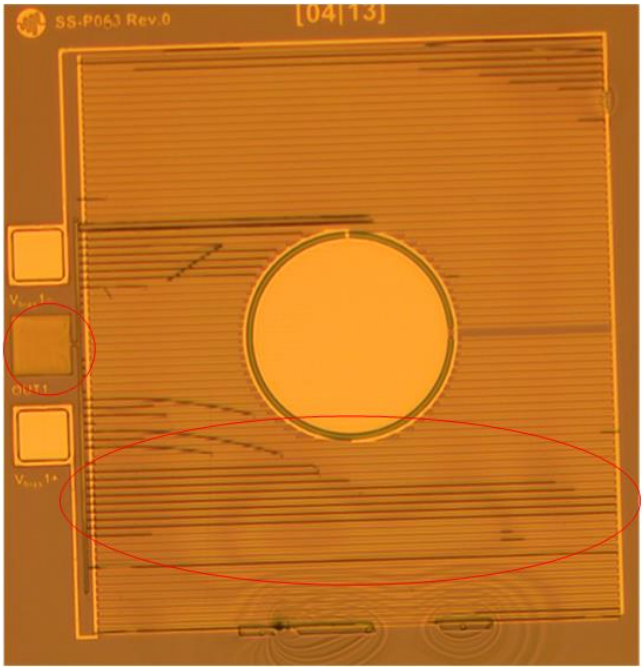


Figure 3.8. Partially successful top electrode deposition. Regions of adhering electrode indicated in red.

Since the top electrode pattern was not complete, this particular wafer was sacrificed to learn more about the lift off process and what effect ultrasonication had on the structures. The wafer was submerged in acetone for a total of roughly 150 minutes. After this amount of time, there was noticeable delamination of the SU-8 surfaces. The wafer was subjected to a short, 5-second ultrasonication treatment, after which the delamination effect was more severe, indicating the hard baked SU-8 structures were not satisfactorily adhered to the substrate.

3.3.3 Introduction of Top OmniCoat Adhesion Promotion Layer

The biggest challenge remaining in the fabrication was achieving adhesion of the top electrode to the SU-8. With hard bake curing of the SU-8, the adhesion was improved, but not enough to yield electrodes. Traditionally, OmniCoat is used as a adhesion promotion layer between the substrate on the SU-8, but we decided to attempt

to use an additional OmniCoat layer between the SU-8 and the top electrode titanium. After investigating prior usage of OmniCoat as an adhesion layer in a similar fashion, one similar usage was found by Nordstrom et al. in [21]. The existing fabrication process remained the same, with the addition of a triple coating of OmniCoat inserted between the hard bake step and the top AZ 5214 photoresist spin coating. Each of the three OmniCoat layers was spun at 3000 RPM for 30 seconds, followed by a 200° C bake for one minute. The top AZ 5214 lithography was processed on top of the new OmniCoat layer the same as in prior attempts. When observing the top electrode photoresist pattern after its development, the pattern was easily visible with the addition of the OmniCoat. This can be seen below in Figure 3.9.

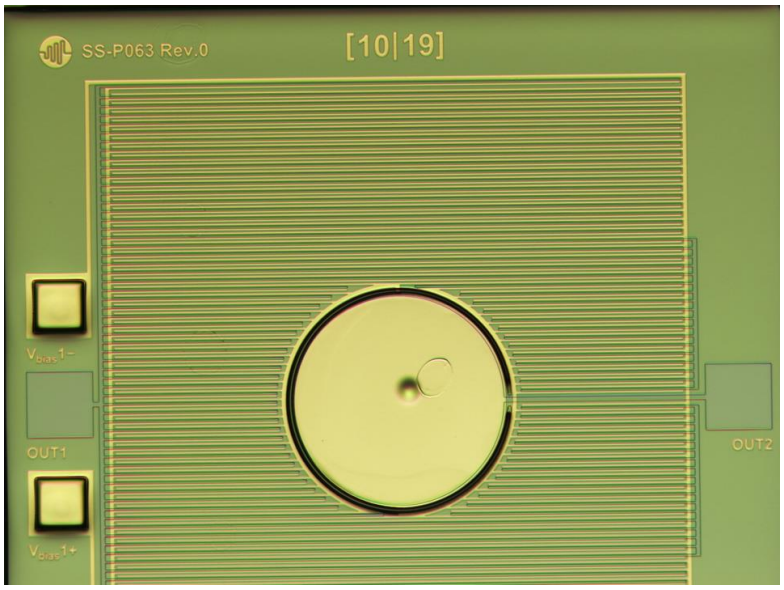


Figure 3.9. Improved visibility of top AZ 5214 photoresist pattern, as compared to poor visibility depicted in Figure 3.5.

Unfortunately, the addition of the top OmniCoat layer did not come without a cost. When the first of three top OmniCoat layer coatings is applied, a surface defect is

developed on a high percentage of the devices. This negative side effect would later be investigated and more information is provided in section 3.4. The defect can be seen below in Figure 3.10.

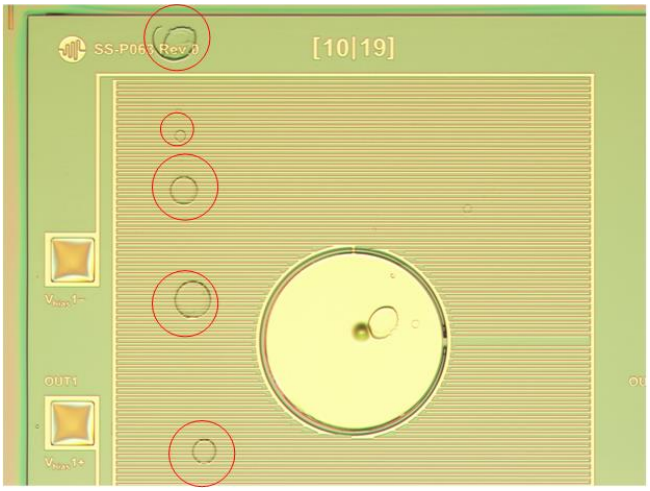


Figure 3.10. SU-8 Surface defect introduced by first application of top OmniCoat adhesion promotion layer.

The second and third OmniCoat layers did not seem to increase the density of the defects on the surface, and so it appears that the introduction of the defect is introduced by the initial interaction between the SU-8 and the OmniCoat.

Top electrode metal deposition was again attempted, this time with the focus on the effect of the newly introduced OmniCoat film between the SU-8 structures and the top metal pattern. The same sputtering recipe in the Univex was used, sputtering titanium for 32 minutes. The traditional, long-term soak method was used for lift off because previous experiments showed ultrasonication leads to delamination. The soaking lasted just over two hours with the aid of gentle acetone spraying to further remove excess metal. After one hour of the soaking, the wafer was observed, and the electrode pattern

was well adhered, but had dark regions along the electrodes, as can be seen below in Figure 3.11.

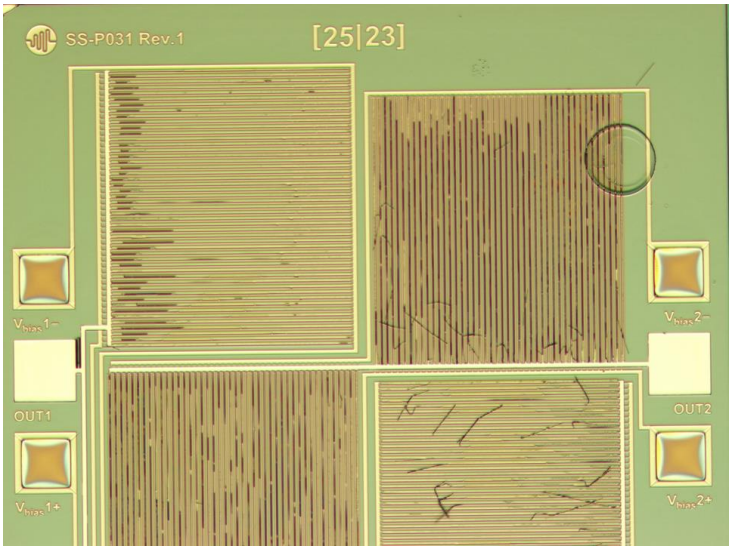


Figure 3.11. Top electrode pattern with successful adhesion, but presence of dark region defects and OmniCoat surface defect (top right).

Initially, these dark regions were interpreted as defects on the metal pattern. However, the result at the end of the two-hour lift off was a complete electrode pattern with fewer such defects. It was evident that these defects were a result of not enough time given to lift off. In any case, the top metal adhesion was improved enough to yield complete top electrode patterns on many devices. The defects located at the top OmniCoat layer seemed to potentially destroy areas of the electrode pattern where the electrode was unable to conform to the topography of the defect, and thus represented a problem that require further investigation. Examples of these types of defects can be seen below in Figure 3.12.

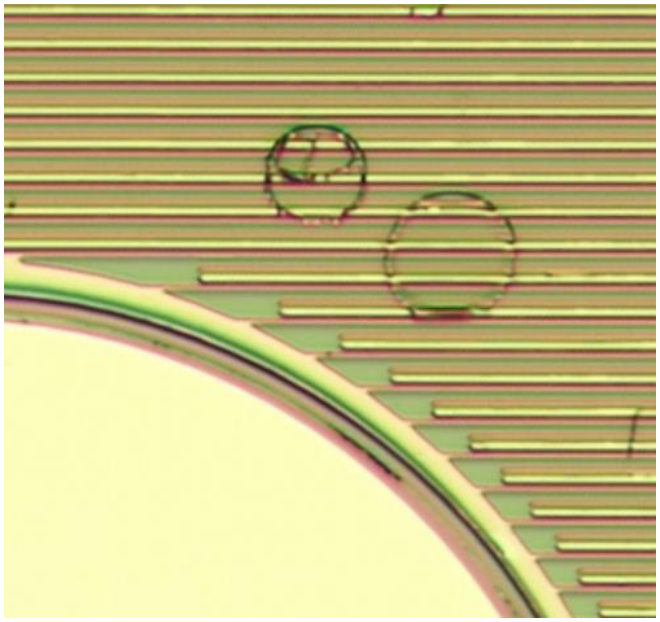


Figure 3.12. OmniCoat surface defects potentially causing fractures in top electrode pattern.

At the end of the lift off process and observation of the completed top electrodes, the wafer was subjected to a short ultrasonication of 10 seconds to test the robustness the SU-8 structures. Unfortunately, the structures showed levels of delamination varying from partial to complete detachment. This observation urged further investigation of the adhesion of the SU-8 to the SiO_2 substrate. One option that remained untested was using hard-baked SU-8 without the OmniCoat adhesion promotion layer between the SiO_2 and the SU-8. OmniCoat is advertised as an adhesion promotion layer as well as a layer that enables the removal of SU-8. The photoresist is notoriously difficult to remove from most substrates, and the addition of OmniCoat allows for its removal by soaking in MicroChem's RemoverPG solution. So while OmniCoat can strengthen adhesion, it also serves as a weak point under SU-8 structures intended to allow removal. These uses seem to be at odds with each other, and so it was unclear if the OmniCoat in our devices was helping more as an adhesion promoter, or possibly having a negative effect by creating a

weak spot in the device and causing delamination. For this reason, we pursued devices that excluded the bottom OmniCoat layer, but keeping the top OmniCoat layer between the SU-8 and the top electrodes in place. All other aspects of the fabrication process remained the same, while the triple spin coating of the OmniCoat onto the bottom electrodes before the spin coating of the SU-8 photoresist was left out. When the new wafers without bottom Omnicoat were ready for the top electrode lift off, the traditional, acetone-soak lift off method was used initially. The new devices without the bottom OmniCoat were soaked for 2 hours without ultrasonication, after which the majority of the unwanted titanium was released. Next, the wafer was subjected to 5 seconds of ultrasonication. This treatment removed the remaining unwanted titanium, and seemed to create no delamination issues. The wafer was further subjected to 10 and 15 second ultrasonication treatments, after which the results were the same: no delamination was observed. Finally the wafer was allowed to soak for 30 minutes longer in acetone to investigate if the ultrasonication created a sort of nucleation point for delamination that was slowly corrupted by the acetone. However, even after this soak, no delamination or indications of such were found. This test conclusively showed that the combination of hard baking and exclusion of the bottom OmniCoat was the solution to the SU-8 adhesion issues. While the OmniCoat previously helped the adhesion when the SU-8 was not hard bake cured, it hindered the adhesion of the hard baked SU-8 structures and created a weakness during acetone soaking. A new fabrication cycle excluding the bottom OmniCoat was executed, and the devices were not damaged by ultrasonication during lift off, meaning the conservative, traditional lift off method could be substituted with our research group's more aggressive method. With a successful fabrication recipe and lift off process defined, wafers with testable devices were yielded. The OmniCoat film defect was still present, but many devices did not exhibit the defect, and so many successfully

fabricated devices were present on the wafers. Below are images of each of the successfully fabricated device variants.

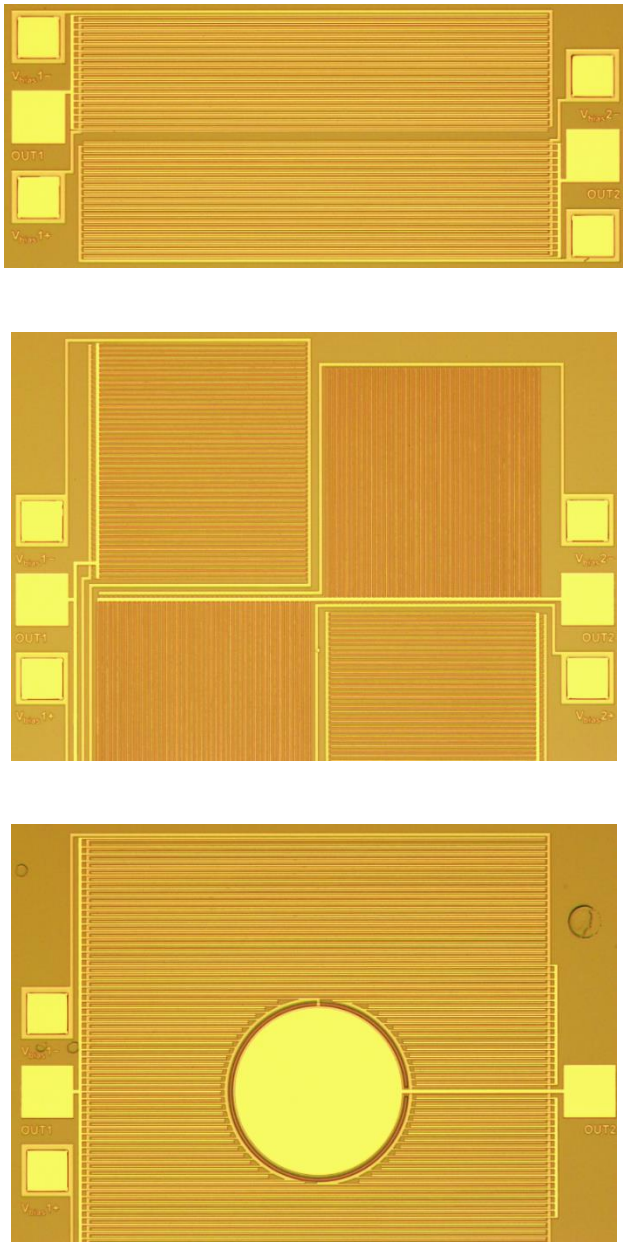


Figure 3.13. Successfully fabricated devices from each embodiment variant. Small Area device (top), Bidirectional Device (middle), and Pressure Enabled Device (bottom).

3.4 Investigation of Top OmniCoat Defect

With the major fabrication hurdles resolved, the remaining matter of contention to yield satisfactory devices is the defect introduced when the top OmniCoat layer is applied to the hard-baked SU-8. It was observed that the top metal electrodes inconsistently conform to the defect, sometimes yielding a continuous electrode, but often yielding a fractured electrode pattern. Examples of these two situations can be seen below in Figure 3.14.

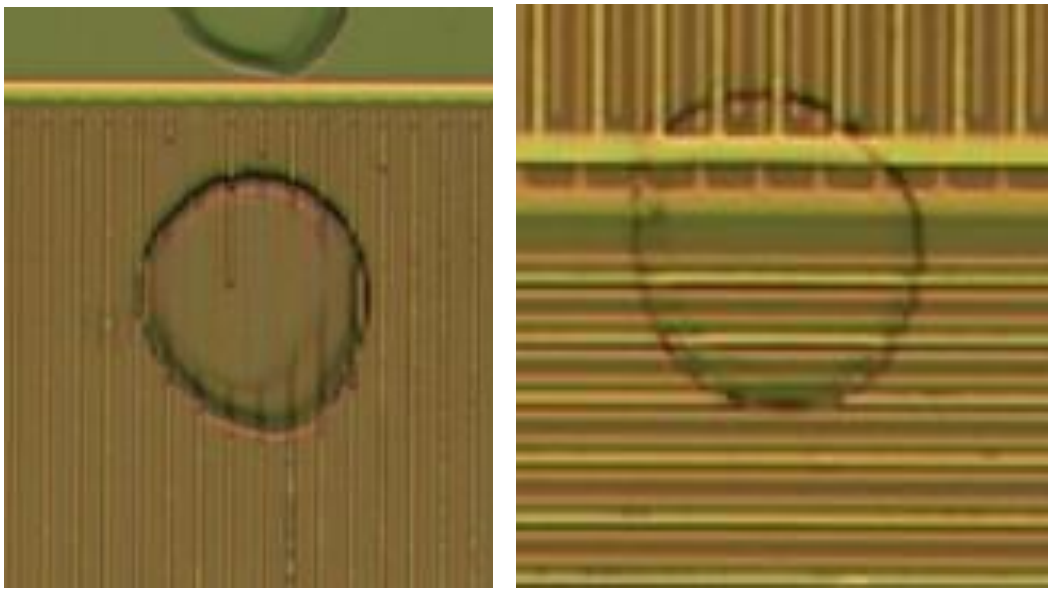


Figure 3.14. Two defects caused by top OmniCoat layer, one causing sever electrode damage (left), and one appearing to not completely destroy electrodes (right).

The effect of this defect is too inconsistent to ignore, and so much time was given to determining the origin of this defect and how to eliminate or at least reduce its presence. The first step was to determine if the defect was a protrusion from the SU-8 surface or a valley in the surface. The defects were examined under a scanning electron microscope (SEM), and the result was that the defects appear to be small rings on top of

the SU-8 and OmniCoat surface. The scale of the defect hovered around 0.25-0.75μm in height. One example profile of a defect is shown below in Figure 3.15.

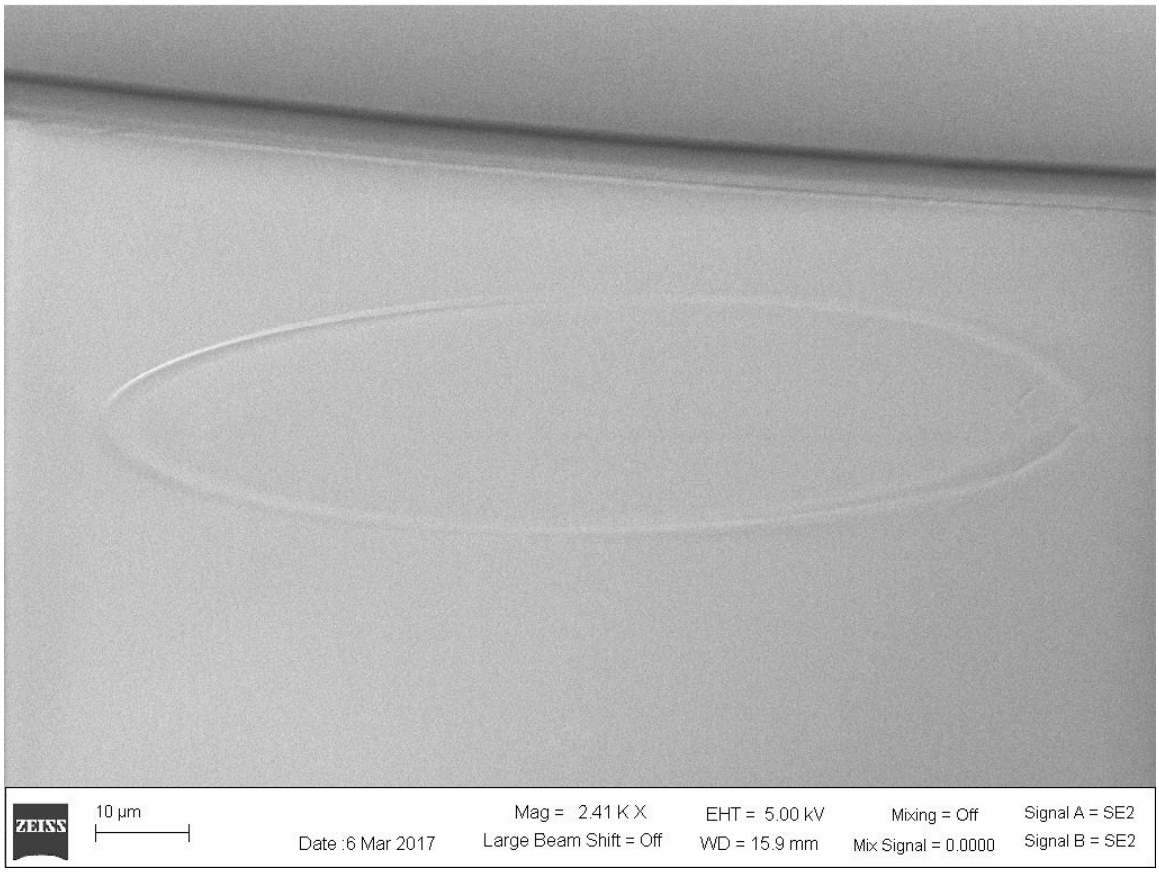


Figure 3.15. OmniCoat surface defect as observed in SEM.

When compared to the thickness of a single OmniCoat layer, which is usually tens of nanometers thick, the much larger defect does not appear to be made of OmniCoat. Rather, this suggests that perhaps the OmniCoat is removing particles of SU-8 and re-depositing them about the wafer surface. Several experiments were conducted that provided more information about this issue. The application of the OmniCoat layer was executed at different points during the SU-8 processing. The intended placement for the

OmniCoat application was after the SU-8 hard baking, and so the process was instead placed after the exposure before the post exposure bake, as well as after the post exposure bake before development.

In the first experiment, the OmniCoat application was done just after the UV exposure of the SU-8, in this case, the SU-8 coating and pattern was completely destroyed. There was no appearance of a pattern during the subsequent post exposure bake, and the SU-8 layer appeared to be almost completely dissolved. This peculiar result prompted the reexamination of the chemical content of the OmniCoat. The chemical name of the active ingredient in OmniCoat is propylene glycol monomethyl ether. Another chemical obviously known and intended to dissolve SU-8 is SU-8 Developer, whose active chemical ingredient is propylene glycol monomethyl ether acetate. These chemicals are very similar, and so it is not surprising that OmniCoat would have a similar effect on undeveloped SU-8. The conclusion from this first experiment was that OmniCoat acts as an unintended developer of SU-8.

In the second experiment, the OmniCoat application was done just after the post exposure bake of the SU-8, when the pattern was apparent, but the SU-8 had not yet been developed. Given the results of the first experiment, it was expected that the OmniCoat application would, in essence, replace the development step by dissolving the unexposed regions of SU-8. Expectations were confirmed, and the OmniCoat developed the SU-8 upon application.

Together, these two experiments gave some insight into the possible source of the OmniCoat defect. If the OmniCoat is capable of dissolving unexposed SU-8, it is possible that the defect may come from the OmniCoat dissolving small particles of SU-8 that were missed during the true development, redepositing these particles on the SU-8 surface

during the spin application of the OmniCoat. This hypothesis was the motivation for several further experiments to mitigate the defects.

3.4.1 Altering the development process

If remnant SU-8 regions are available for development by the OmniCoat application, this suggests that the SU-8 is not completely developed during the previous designated development step, and so the first experiment was to adjust the development process. The manufacturer's data sheet suggests a development time of 1-2 minutes in the designated SU-8 developer for SU-8 3005 at thicknesses of 4-10μm. An IPA spray to remove the developer and remnant particles follows the development. Assuming there were undeveloped particles remaining using this recipe, the development time was increased to as high as 5 minutes. Given the relatively large scale of the SU-8 structures and lack of small critical features, over-development did not threaten the devices. Additionally, the aforementioned submersion of the wafer in IPA after the development for 1-2 minutes with agitation was implemented. The hope was that this would do a more thorough job of removing all of the remnant particles of developed SU-8 than only an IPA spray would do. Unfortunately, the increased duration of the development and the addition of the IPA bath to the IPA spray did not seem to have a significant effect on the existence of the defect when the OmniCoat was applied. After hard baking and application of the first OmniCoat layer, the defects were still present, and the density did not seem to be significantly changed.

3.4.2 Tuning Spin Coat Process

After attempts to adjust the SU-8 development to mitigate the OmniCoat defect did not yield improvements, focus shifted to adjusting the OmniCoat spin coating process. Whether or not the origin of the defect was undeveloped SU-8, when the

OmniCoat is applied and the wafer is rotated, the defects are spread and distributed about the wafer. By adjusting the spinning speed, it is possible that the centrifugal force reduction on the particles may decrease the degree to which the particles are spread about the wafer surface. The spin speed was reduced to as low as 1500 RPM for 30 seconds, with 2000 and 2500 RPM also attempted. However, this adjustment also brought no observable change in the density or distribution of the defects on the surface of the wafer.

Another hypothesis was that the amount of time allowed between pouring the OmniCoat on the wafer and beginning the spinning could affect the density of the defects. If a time constant is involved in the interaction between the OmniCoat and SU-8 and the subsequent deposition, it was possible that a waiting for a longer time between pouring the OmniCoat on the wafer and initiating the rotation may prevent the rotation from causing defects. If the reaction has already occurred before the spinning occurs, and the SU-8 particles are affected by the OmniCoat, but the rotation is not present to cause translation of the particles, they may remain deposited in the original location. Assuming this to be true, the OmniCoat was applied to a wafer, and then given 1 minute to sit in place before the spinning occurred. Fortunately, this seemed to slightly decrease the density of the defects on the SU-8 structures, although not eliminating them completely. At this point, further investigation of the defect was suspended, having achieved viable devices with a decreased defect density.

3.5 Device Singulation and Packaging

With wafers containing completed devices achieved, the next step was to isolate all of the devices on the wafer into singular devices. This was achieved using an ACT Dicing saw, which has an automated system to dice wafers. Given the small size of our devices, the weak adhesion of the tape used to mount the wafer, and the saw blade's

water-cooling system that operates at a high pressure, there was fear that the devices would be washed away during the automatic dicing. To prevent this possible loss of devices, the wafer was diced leaving roughly 25μm of the 500μm silicon thickness remaining at the bottom of the wafer, keeping the wafer connected and not to be washed away, while still easy to fracture and singulate by hand. The dicing process also casts silicon particles about the surface of the wafer, and so a protective photoresist layer is spun on the wafer prior to dicing. AZ 5209 photoresist is used as a protective layer, it is spun at 3000 RPM for 30 seconds, followed by a 50 second soft bake at 110 °C. This photoresist is spun directly on top of the wafer. After dicing, each individual device must be washed in acetone to remove the protective photoresist layer. After the cleaning step, the device isolation is complete and devices are prepared for testing. Images of example singulated devices can be seen below in Figure 3.16.

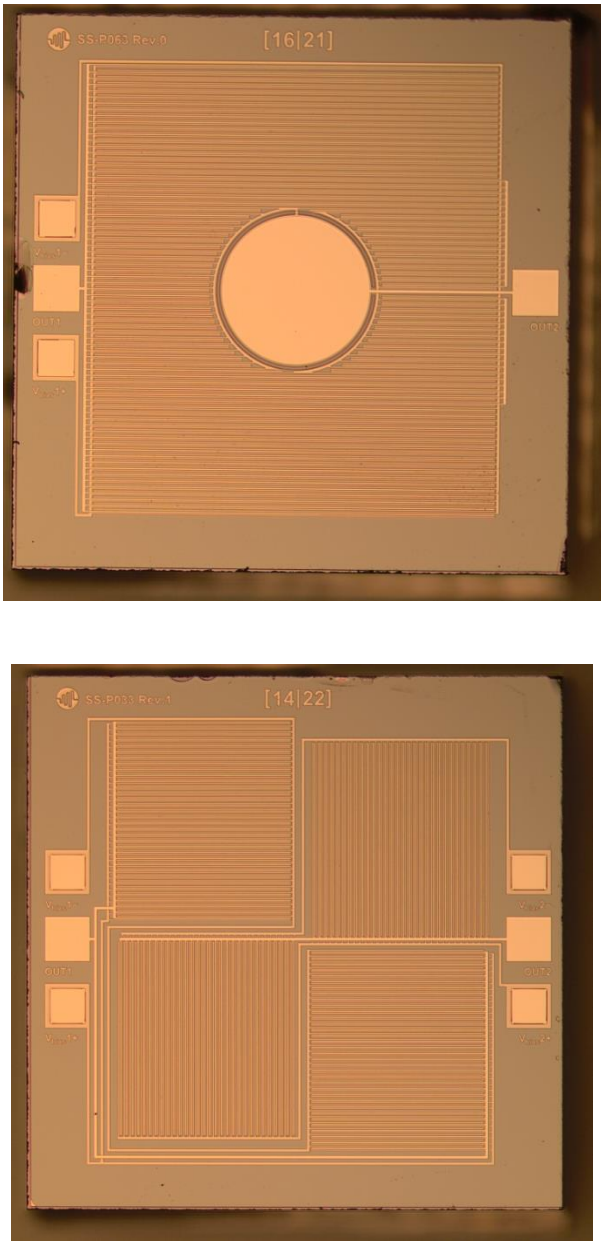


Figure 3.16. Devices isolated using ACT Dicing Saw. Pressure enabled sensor (top) and Bidirectional sensor (bottom)

After the dicing process is completed, the devices must electrically connected to a circuit board that can be used for testing. A single shear stress sensor is first secured to the printed circuit board using Dymax 920 UV-cured epoxy glue, which requires a 30

second UV exposure to cross link and harden the epoxy. Once secured to the circuit board, a West Bond Model 7476D wire bonder is used to couple wires to the bond pads of the device. The other end of the wire is connected to the terminals on the printed circuit board that fan out to larger wire ports. The West Bond 7476D wire bonder utilizes ultrasonic energy to heat the wires and then applies a pressure to the wire to contact the bond pad such that the wire is coupled to the bond pad. While this method worked effectively for the titanium bond pads that are deposited directly on the SiO_2 surface, it failed when applied to the bond pads located on top of the SU-8 film. As seen below in Figure 3.17, the attempted wire bond removed the electrode film from the SU-8 and damaged the SU-8 underneath.

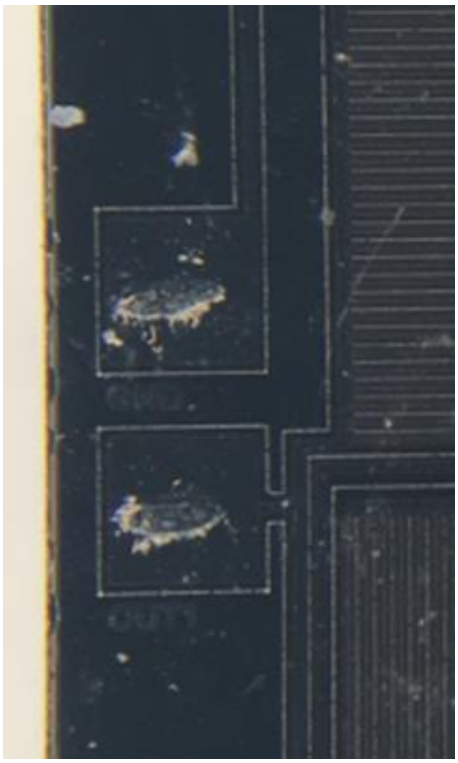


Figure 3.17. Two bond pads on top of SU-8 in which the wire bonding technique failed, damaging the SU-8 underneath and not facilitating a bond with the wire.

Metal delamination and SU-8 deformation during bonding is a documented issue from Sameoto et al. in [23], and can sometimes be improved by hard baking and plasma surface activation, however we were unable to improve the bond yield with these methods. After attempting to lower the duration and power of the ultrasonic pulse used to couple the bond pad and the wire without success, an alternative method was sought. Also available in our lab is a conductive epoxy, the H20E kit from Epoxy Technology, which can form a conductive pathway after being cured. The epoxy was carefully applied to only make contact with the bond pad on top of the SU-8, then traced down the side of the device to the circuit board, where it could make contact with a pre-placed wire. The conductive epoxy required a 5 minute curing time at 150° C. Although this process is much slower and less elegant than the use of the wire bonder, it proved effective when later testing the devices. To avoid contact between the different wires and epoxy traces, the electrical connections were coated with UV cured epoxy in the regions where potential contact lurked, namely right around the bond pads. A completed, packaged device is shown below in Figure 3.18.

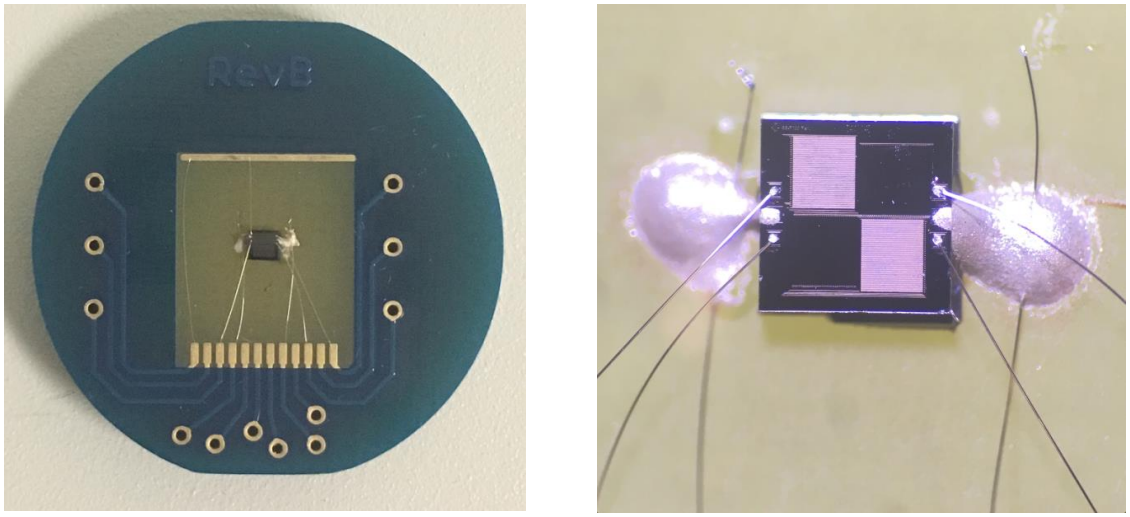


Figure 3.18. Completed device, secured and electrically connected to PCB using combination of wire bonding and conductive epoxy techniques. (left) Entire apparatus. (right) Zoom to show detail of wire bonds.

With the device secured to the printed circuit board and wired for electrical access, the production of the sensor apparatus was complete and device testing was set to begin.

Chapter 4: Testing and Analysis

After device fabrication, we sought to characterize the functional characteristics of the shear stress sensors. This testing was done in two main phases. First, the devices were tested for their intrinsic characteristics, with the goal of quantifying the dielectric constant, capacitance, and perhaps other properties that had not been foreseen. In the second phase of testing, the sensors' electrical properties were quantified. The devices were tested for shear stress sensing functionality by applying shear forces and quantifying the electrical response of the devices. Using the results of these two tests, the devices could be compared to the analytical and numerical models described in Chapter 2 to determine if they were functioning as expected. The rest of this chapter will detail these testing processes and list their results.

4.1 Intrinsic Device Characteristics With Admittance Spectroscopy

Before testing the sensors' functionality, it was necessary to determine their electrical properties as to properly analyze the device behavior. Mainly, the capacitance of the devices was needed, but it was also necessary to determine the relative dielectric constant, ε_r, so that potential departures from the manufacturer's quoted value could be brought to light. To determine the dielectric constant value for the SU-8 3005 in our fabricated devices, we used the parallel circular plate capacitors shown in Figure 2.5. These devices closely approximate an ideal parallel plate capacitor, and so with known dielectric thickness and plate area, the dielectric constant estimation can be made easily if the capacitance is known. For this task, as well as the subsequent tasks of measuring device capacitance, admittance spectroscopy was utilized. Admittance spectroscopy applies a broad-band voltage waveform V_{in} across the frequency band of interest to the device input, and the device is placed in series with a trans-impedance amplifier (TIA),

which provides a measurement of current through the device with a low noise level. An FFT is applied to the output waveform from the TIA, and the output of the amplifier is presented as a frequency response of the sensor admittance. This process is described in detail by Kim et al. in [24]. Figure 4.1 shows a schematic of the admittance spectroscopy test.

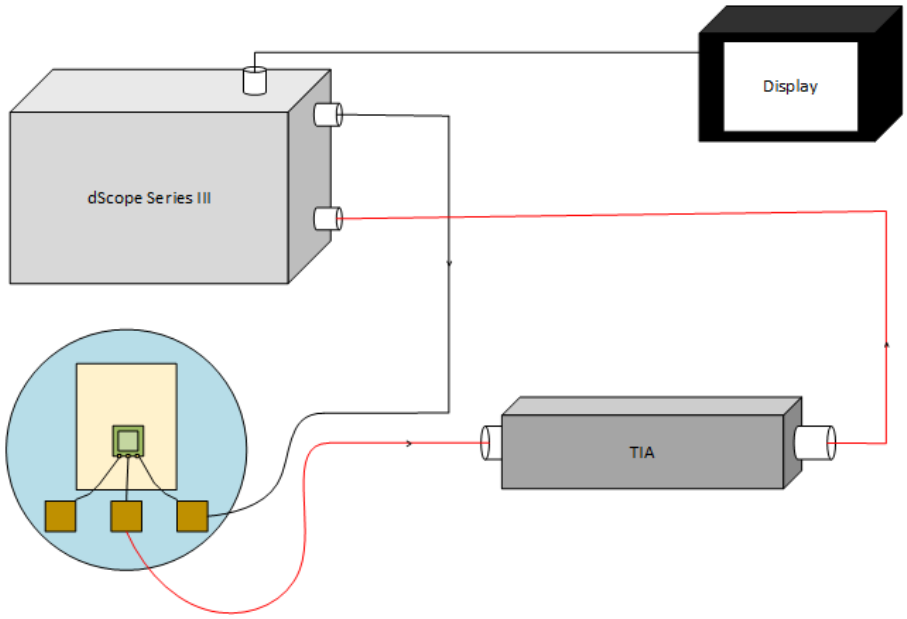


Figure 4.1. Schematic of admittance spectroscopy measurement. Audio analyzer (dScope) produces input broadband input waveform to device. Device is connected in series with TIA, which amplifies current through the device. Signal is returned to dScope, which executes FFT of the signal, providing a frequency response of the inverse of the impedance (admittance).

The admittance of a capacitor, Y, is known to be $Y = jwC$, which has a frequency response that is linear on a logarithmic scale, displaying a 20 dB/decade slope. This means that if the devices display this 20 dB/decade linear increase in their admittance spectroscopy output waveform within a reasonable frequency range, it indicates that the device's electrical behavior is that of a capacitor. Applying this technique to the circular parallel plate capacitor devices, C_{device} can be estimated for

individual devices. With this information, an estimation for the relative dielectric constant of the SU-8 3005 dielectric layer can be calculated using the equation:

$$\varepsilon_r = \frac{C_{device} * d}{A * \varepsilon_0}. \tag{4-1}$$

In our test set up, a Prism Sound dScope Series III was used to generate the broadband input waveform, as well as record the device output waveform and execute the FFT. The TIA used for the experiment featured a 100kΩ feedback resistor and an input capacitance of 18 pF. The analytical output of the TIA, as well as a circuit diagram representing this test, is given below:

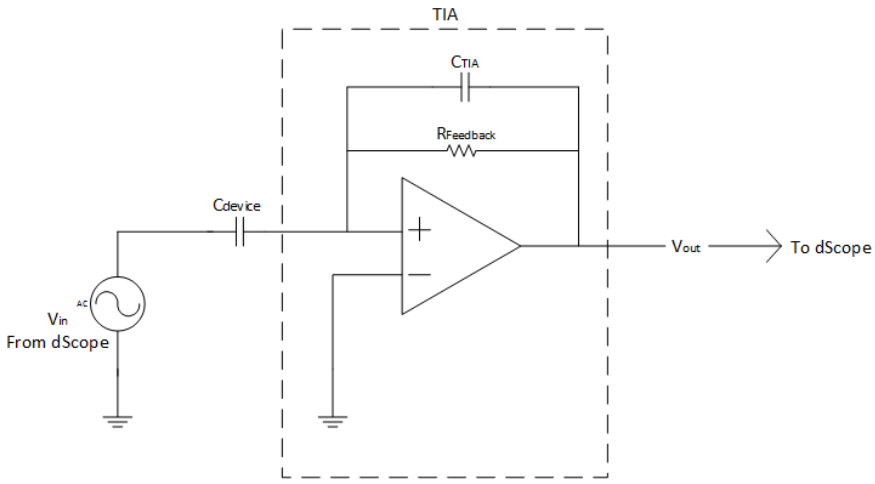


Figure 4.2: Circuit diagram used in admittance spectroscopy experiments.

$$C_{device} = \left| \frac{V_{out}}{2\pi f * V_{in}} * \frac{1}{Z_{feedback}} \right| \tag{4-2}$$

$$Z_{feedback} = R_{feedback} \,||\, C_{TIA} \tag{4-3}$$

Averaging the relative dielectric constant estimations from 13 individual circular parallel plate capacitors, the estimated value for ε_r was 3.86 with a standard deviation of 0.08. This value agrees with the various sources of estimations that can be found from a variety of sources: in [25] Thorpe et al. use 4, [6] gives 3.28, [13] gives 3.2, [26] Ayad et al. reports 2.85 at GHz frequencies, and [19] reports 3-4.5. Figure 4.3 below shows the admittance spectra of the circular parallel plate capacitors with the characteristic 20 dB/decade linearly increasing behavior. The region of interest is above 3000Hz, when the linear region is clearly visible. Below this region, the spectrum is dominated by 60Hz interference and the many harmonics of this interference.

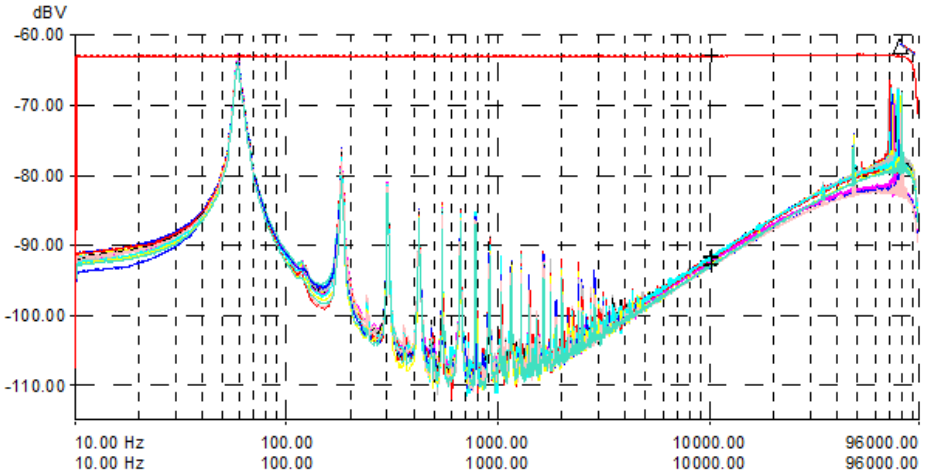


Figure 4.3. Admittance spectroscopy measurements for 13 circular parallel plate capacitor devices. The characteristic 20dB/decade slope is clearest in the region of 5kHz to 10kHz. Shown in red is the flat, broadband input signal.

Next, the individual capacitances of the shear stress sensor devices was to be determined for comparison with the analytical and numerical model predictions. Applying the aforementioned admittance spectroscopy technique to the ports of the device offers an estimation of the capacitances heretofore labeled as C_1 and C_2. Figure

1.5, which illustrates these capacitances, is repeated here for convenience, with C_3 also added.

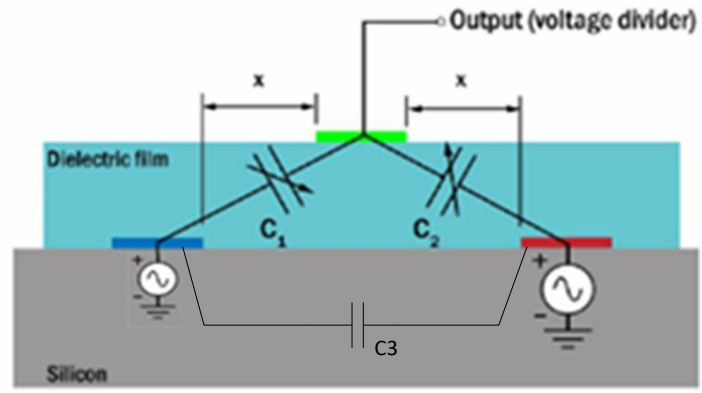


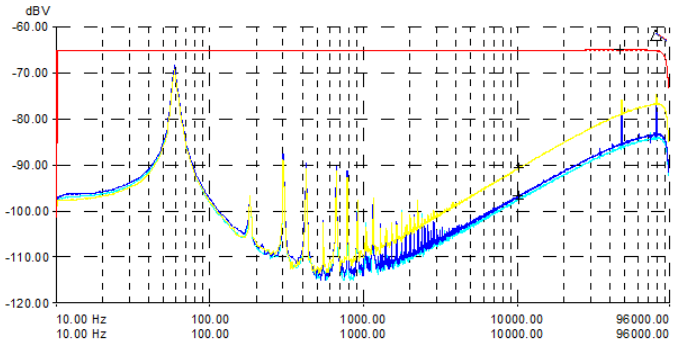
Figure 1.5 Repeated for convenience.

An additional capacitance, C_3, was measured between the two terminals located on the silicon dioxide substrate surface. This third capacitance was important because the capacitance measurement between any two ports on the device was actually a measurement of that capacitance in parallel with the series combination of the other two capacitances (refer to Figure 1.5). In light of this, a system of equations can be generated from the three capacitance measurements, as given below:

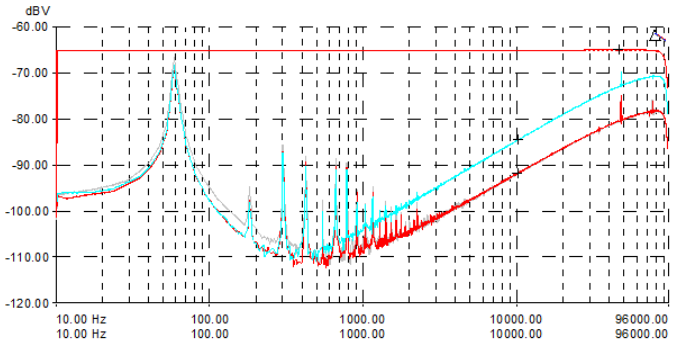
$$C_1 = \frac{C_2 * C_3}{C_2 + C_3} \quad C_2 = \frac{C_1 * C_3}{C_1 + C_3} \quad C_3 = \frac{C_1 * C_2}{C_1 + C_2} \tag{4-4}$$

Due to the non-linear terms present in the numerator, these equations cannot be solved outright. However, a MATLAB script was written during testing of previous device generations that iteratively estimates the true capacitances based on the initial measurements, minimizing error to a user specified convergence level. This script can be found in Appendix C. Admittance spectroscopy was used to obtain an initial measurement of C_1, C_2, and C_3, which were then adjusted using the MATLAB script

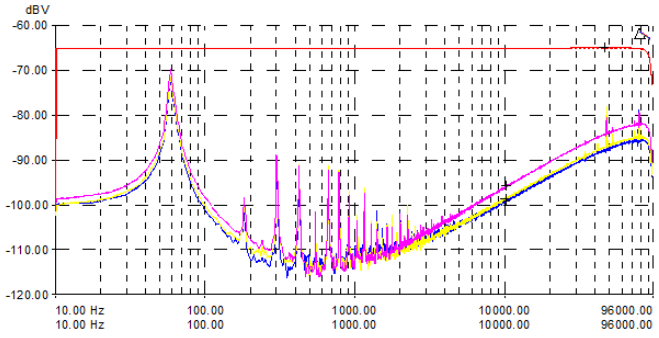
mentioned above. The admittance spectra for the different device variants can be seen below in Figure 4.4 a-c, followed by Table 4.1, which summarizes the measured capacitance values for the different devices.



(a)



(b)



(c)

Figure 4.4a-c. Sample admittance spectra for the three device variants. Bidirectional device in (a), pressure enabled device in (b), and small area device in (c).

Device Type	C1 Measurement (Adjusted) [pF]	C2 Measurement (Adjusted) [pF]	C3 Measurement (Adjusted) [pF]
Small Device 2µm	0.93	0.78	3.09
Small Device 4µm	0.80	0.85	3.06
Bidirectional Device 2µm	1.42	1.53	5.58
Bidirectional Device 4µm	1.41	1.35	5.35
Pressure Enabled Device 2µm	2.87	2.73	12.08
Pressure Enabled Device 4µm	2.53	2.78	11.83

Table 4.1. Sample Measured Capacitance Values for Device Variants

As can be seen by comparison to Tables 2.2, 2.3, 2.6, and 2.7, these measured capacitance values are in reasonable agreement with those predicted by the numerical models, especially those given by the numerical models. The main sources of error are likely the regions of the devices that were not included in capacitance estimations, such as the bond pads and traces connecting the bond pads to the sensing regions, and the capacitance associated with the fan-out wiring of the printed circuit board and the unshielded wires used to couple to the printed circuit board. Additionally, the measurements are subject to noise present in the equipment that cannot be avoided. The uniformity of the SU-8 thickness is also not perfect, and this creates variation in the true capacitance. Finally, the OmniCoat constitutes a very small portion of the dielectric thickness, but it is ignored in the capacitance estimations, assumed to have a negligible effect on the overall capacitance. Despite these likely sources of accumulated error, it

appears our measurements are quite consistent with the numerical model predictions, although generally slightly smaller than those predicted by the numerical models. The measured capacitances follow the same predicted trends as the models, particularly that the 2μm devices tend to have a slightly greater capacitance than the 4μm for a given device design. With satisfactory capacitance measurements obtained, the sensitivity could be quantified.

4.2 Testing Sensing Capabilities

The next step in characterizing the devices was to test their actual capabilities in sensing a shear stress via differential capacitive sensing. This meant a mechanism for applying a shear force to cause the deformation and shear strain of the top surface of the dielectric was needed. As mentioned in Chapter 2, a rather large shear stress can be generated with physical contact on the top surface of the device. In short, we needed to grab on to the top of the device and apply force in the direction tangent to the dielectric surface while holding the rest of the device rigid. With the surface area of the sensing region known, the shear stress applied could be found if the force applied to the surface was a known value. For example, if a test mass was hung from the device, only held by the sensing surface, the force on the sensing area could easily be calculated as $F = m * a$ where m is the test mass and a is the acceleration due to gravity, 9.8 m/s^2. From this force, the stress applied is simply the force divided by the sensing area. Revisiting the device circuit diagram with the parasitic capacitance left out, as it is below in Figure 4.5, it can be seen that ideally, with no force applied, the $+V_{ac}$ signal and the phase inverted $-V_{ac}$ signal should destructively interfere at the V_{out} node, producing a 0V output because the values of C_1 and C_2 are equal.

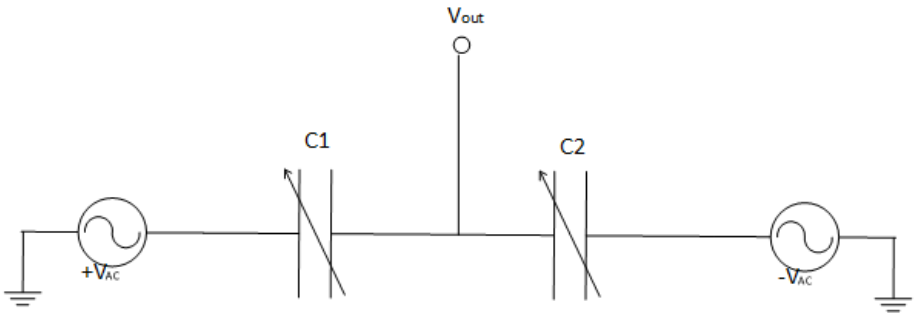


Figure 4.5. Simplified circuit model for shear stress sensors, ignoring parasitic capacitance, C_3.

When the force is applied, $C_1 = C_1 + \Delta C$ and $C_2 = C_2 - \Delta C$ and thus the output voltage is no longer zero. If $+V_{ac}$ and $-V_{ac}$ are sinusoids, then V_{out} will also be a sinusoid when the device is subjected to a stress that makes $C_1 \neq C_2$. Human error introduced in fabrication causes misalignment of the electrode located on top of the SU-8 film. This causes the resting values of C_1 and C_2 to slightly differ, and therefore means that the signal at V_{out} is not identically 0 when there is no load, but rather some small sinusoidal signal. This signal will be referred to here forward as the "resting sinusoid". The existence of this misalignment does not change the function of the senor, but it does require care when interpreting the sensor's electrical response. If the shear stress is applied in the direction that moves the top electrode towards the perfectly aligned position exactly between the two bottom electrodes, then the resting sinusoid is expected to reduce in amplitude, as C_1 and C_2 are approaching equality as the top electrode moves towards the aligned position. If the shear stress is applied in the direction that moves the top electrode further out of alignment, then the resting sinusoid is expected to increase in amplitude.

4.2.1 Mechanical Test Aspects

Several methods were attempted to apply a shear stress to the device under testing. First, Kapton tape was cut and folded to create an apparatus in which the adhesive was only exposed in the small region intended to make contact with the device. The tape was pressed to the surface of the device, then could be pulled from either direction perpendicular to the direction of the sensing unit cells. This apparatus can be seen below in Figure 4.6.

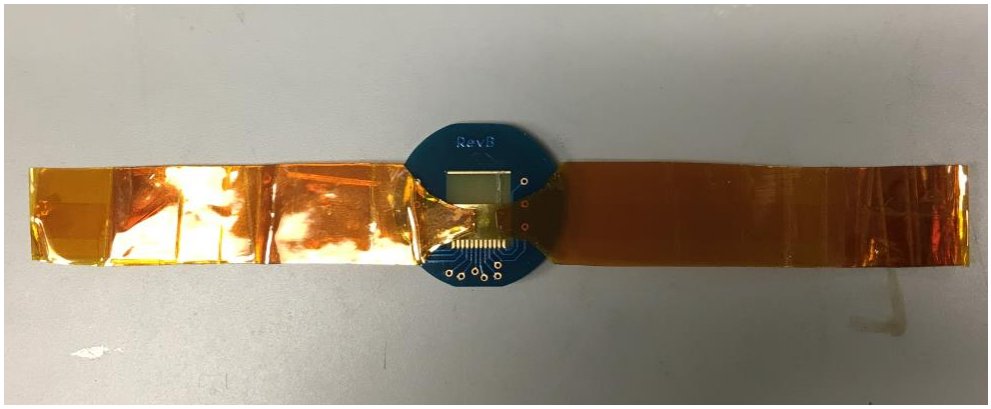


Figure 4.6. Kapton tape used to attempt to apply shear stress to sensor.

This method had very poor results. The first pitfall of this method was the delicate wire bonds accidentally touching the adhesion surface of the tape and promptly being ripped off. To combat this, a thin layer of UV-cured epoxy was applied to the top surface of the device as to firmly secure the wire bonds and prevent any unwanted disconnections. The tape was then reapplied to the device, although in this configuration the adhesion region of the tap was making contact with cured epoxy. Unfortunately, the interaction between the epoxy and the tape adhesion material was not strong enough to sustain a reasonable bond, and the tape simply pulled away under tension. At this point, the Kapton tape method was abandoned. Instead, a new technique was attempted in

which a 1 inch by 3 inch glass microscope slide was secured to the sensing surface of the device by applying a small amount of UV-cured epoxy to the sensing surface then balancing the glass slide on the device such that it only made contact with the sensing surface, as shown below in Figure 4.7.

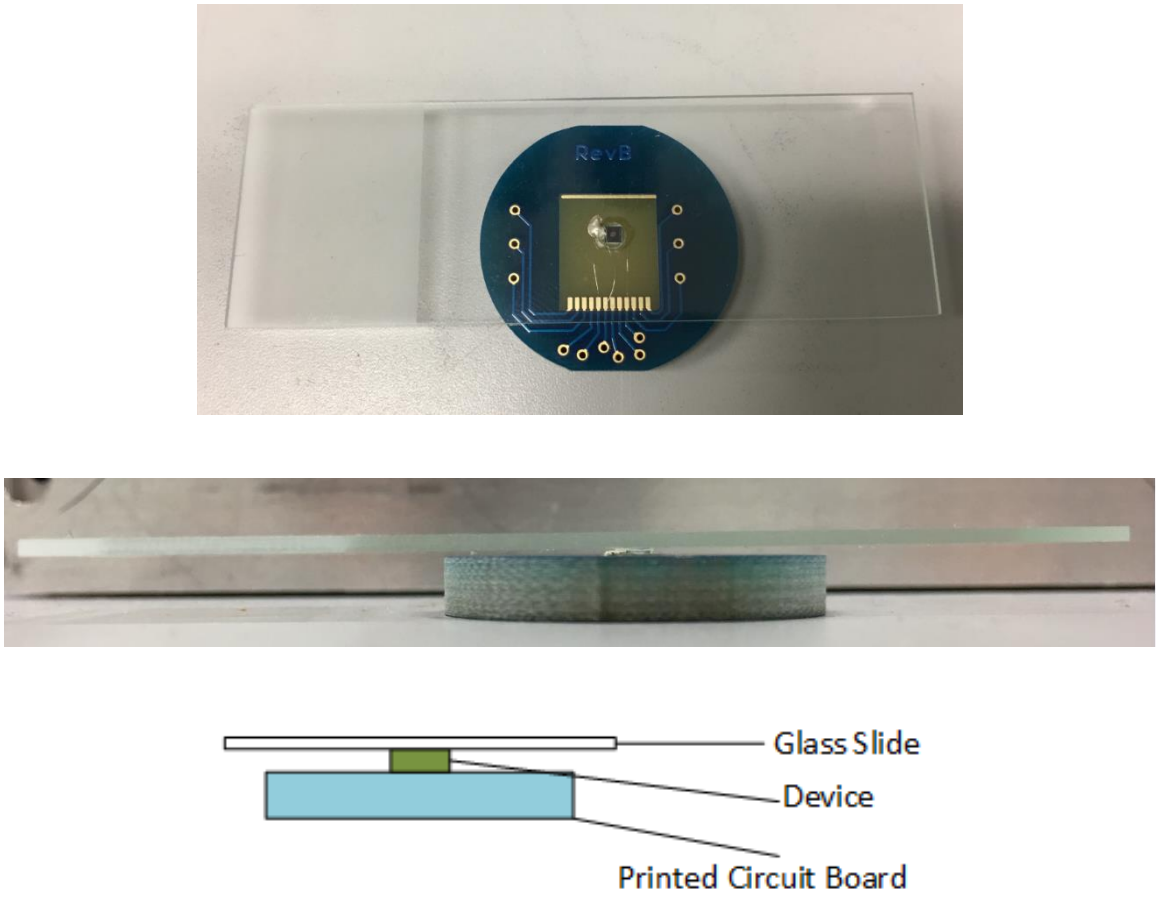


Figure 4.7. Mounted glass slide apparatus for applying shear stress. Top view (top), side view (middle), and diagram of mounting (bottom).

With the glass slide mounted to the device, there was a much larger surface area available for tape to make contact with. The tape could strongly adhere to the glass slide, and by tensioning the tape, the glass slide could apply the shear stress to the device in

either of the directions of interest. Moreover, the glass slide shielded the wires and wire bonds underneath from outside contact, preventing damage to the test apparatus when a load was applied. With a viable method for applying a load to the sensor, the electrical aspects of the test could be given attention.

4.2.2 Electrical Test Aspects

The signal generation and recording for the test was all performed using the dScope Series III analogue and digital audio analyzer from Prism Sound. The analyzer can produce two synchronized analogue output signals with one signal being phase-inverted. For the purposes of this experiment, the dScope generated two sinusoidal signals at a frequency of 1kHz and a peak-to-peak voltage of 2V, representing the aforementioned $+V_{ac}$ and $-V_{ac}$. These two signals are transmitted via BNC cable to the device ports. Initially, alligator clips were used to connect the BNC cables to the sensors, but a device enclosure with integrated connectors was later assembled, as described below. The two sinusoidal signals were applied to the two terminals of the device on the silicon dioxide substrate, and the V_{out} signal was transmitted from the top electrode via BNC cable to a junction gate field-effect transistor (JFET). A JFET amplifier was selected for use due to the high input impedance and exceptionally low noise. The particular JFET used for this experiment provides 23 dB of gain, roughly equivalent to a factor of 10, with a 4nv/√Hz noise floor. The amplified signal is transmitted back to the dScope via BNC cable. The audio analyzer then processes the signal in multiple ways. Using the continuous-time detector, a hardware-based low-pass filter is applied in a first attempt to remove unwanted interference. Further, the dScope has the ability to apply a high order digital filter with a very narrow bandwidth, which tracks the device input signal's frequency to use as the filter center frequency, 1kHz in this case. This further

isolates the signal of interest from interference. This waveform is that which was analyzed for the sensor behavior. Additionally, the dScope executes an FFT and displays this frequency data, which is also of interest for this experiment. A schematic summarizing this experiment setup is displayed below in Figure 4.8.

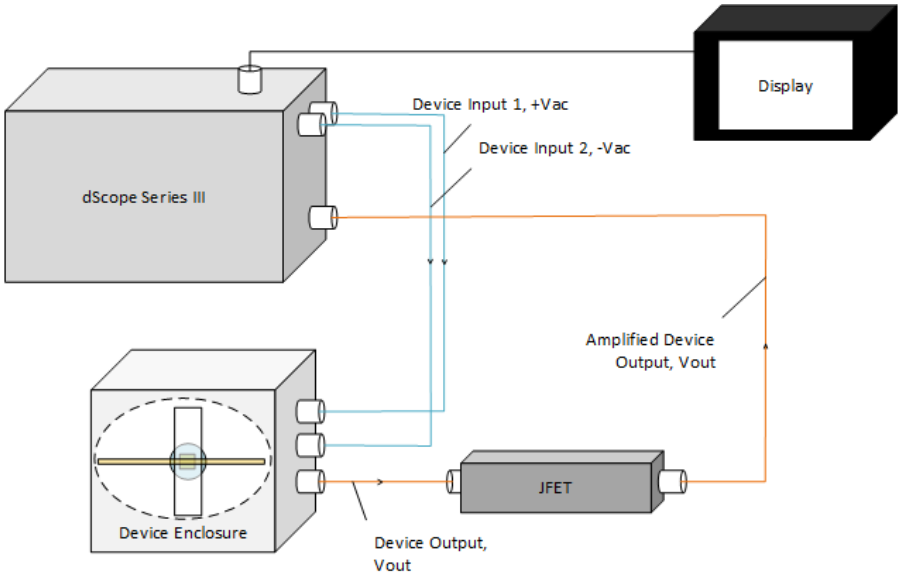


Figure 4.9. Schematic of shear stress sensor characterization experiment. The dScope analyzer generates the opposite phase sinusoidal signals which are delivered to the device inside the shielding enclosure. The output from the device is delivered to the JFET amplifier, which provides low noise gain, then returns the signal back to the dScope, which filters and displays the device output signal.

The inclusion of the enclosure above was not initially part of the test set up. The device was at first simply connected from the PCB to the signal generator and analyzer by small gauge wires connected to BNC cables with alligator clips. However, this badly exposed the device to outside electromagnetic interference, particularly at the 60Hz frequency. The output waveform of the device in the absence of an enclosure, in which

the signal of interest is modulated by the interference with much greater amplitude, was not usable. To counter this noise, a previously fabricated aluminum shielding enclosure was adapted for this test. This allowed the self-shielded BNC cables to connect directly to the enclosure, and the small gauge wires to connect to the BNC terminals within the protected confines of the shield, blocking out most electromagnetic interference corrupting the signal. An image of the actual test set up, including the aluminum shielding enclosure is shown below in Figure 4.10.

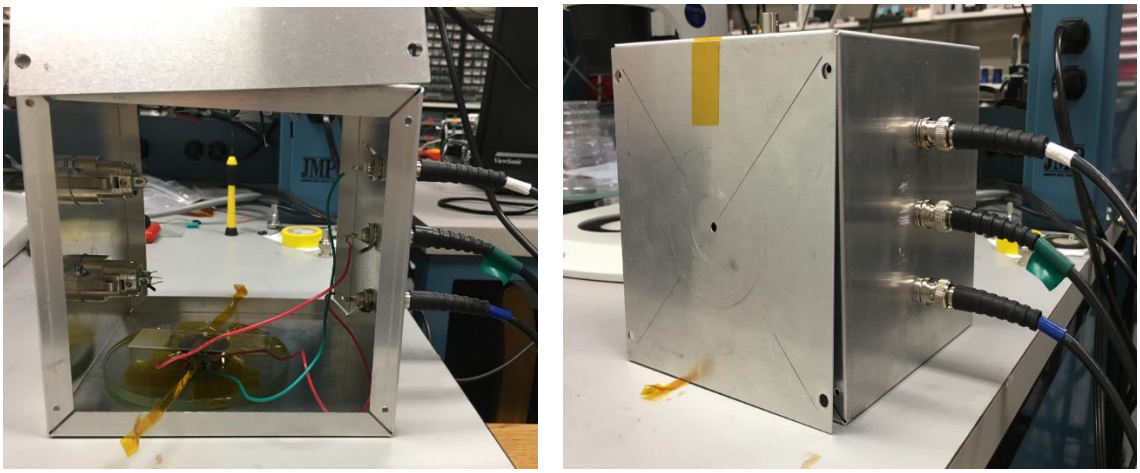


Figure 4.10. Shielding enclosure with shear stress sensor outfitted for testing inside. Red small gauge wires carry the input signals to the device while the green small gauge wire carries the output signal out of the device (left). Kapton tape tabs used to hang test masses from either side of the sensor also visible (left)

4.2.3 Test Execution and Results

The execution of the test consisted of hanging a test mass from the tape, which applied the load to the glass slide, which in turn transferred a shear stress to the sensor. Depending on the direction of the shear stress, the resting sinusoidal signal of the device was expected to increase or decrease in amplitude as previously described. First, while

the 2V peak-to-peak sinusoidal signals were applied to the device terminals, the resting sinusoidal output signal of the device was recorded on the dScope display software. Next, the test mass of 90.6g was fastened to the tape apparatus to apply the shear stress, and the new sinusoidal signal was recorded on the same screen as the resting sinusoid. Finally, the test mass was hung from the other side of the sensor, applying a shear stress in the opposite direction. Again, the response sinusoid was recorded on the same screen as the previous two measurements. In post-processing, the peak amplitude changes of the sinusoidal output signals were measured. The output waveforms for a bidirectional device with 4µm electrode traces is shown below in Figure 4.11.

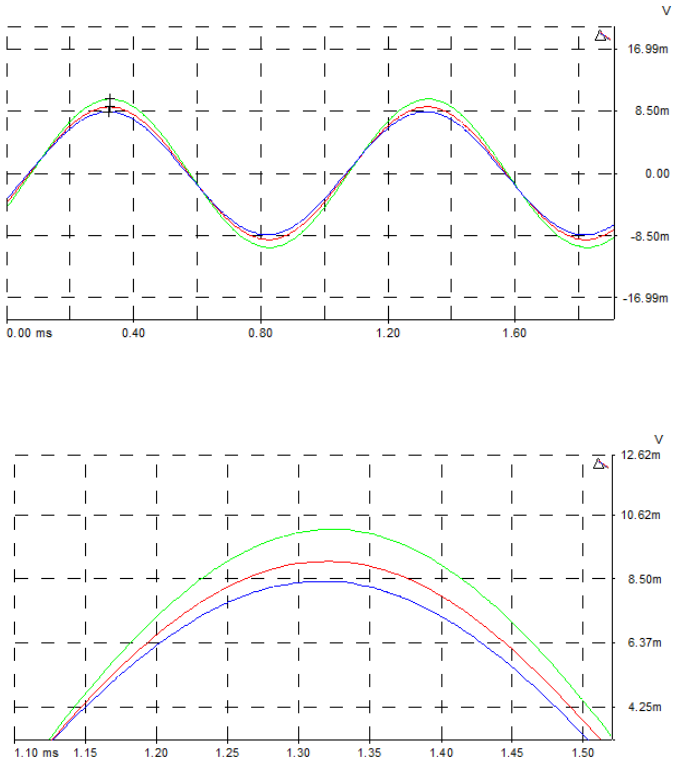


Figure 4.11. Waveforms of shear stress sensor output. Full waveform (top) and zoomed view of peaks (bottom). Red signal is the resting sinusoid (no load). Green is the sinusoid of test mass hung in direction 1, and the blue waveform is the sinusoid of test mass hung in direction 2.

As expected, it can be seen that the resting sinusoid increased and decreased in response to the two shear stresses applied in opposite directions. What this data does not show is that the sinusoids from the shear stresses did not quickly return to the resting sinusoid when the test mass was removed. Rather, the output waveform slowly crept back to the resting sinusoid shape, and on occasion, it would settle into a slightly different resting sinusoid, as is reflected in Table 4.2. After further investigation, this was determined to likely be a result of the viscoelastic effects of the SU-8 film. As demonstrated by Xu et al. in [27] and Park et al. in [28], the storage and loss modulus of SU-8 are considerably affected by the hard-baking step, and the presence of a non-negligible relaxation time is widely acknowledged. Satisfied with the behavior indicating roughly equal and opposite response to loads in opposite directions, we focused on a single direction to take measurements in order to calculate the sensitivity of the device. The measurements from the device loading experiment are listed below in Table 4.2. Note: these measurements do not correspond to the illustrative graphs shown in Figure 4.11

Trial Number	Resting Sinusoid Peak Voltage [mV]	Peak Voltage under Load [mV]	Peak-to-Peak Voltage Swing [mV]
1	0.197	0.231	0.068
2	0.218	0.240	0.044
3	0.227	0.236	0.018

Table 4.2 Peak Voltages for Shear Stress Sensor Readout Testing

With quantitative measurements on the sensor's response behaviors, it was possible to compare the true device behavior to the predicted behavior from the analytical

and numerical models. Analyzing the circuit diagram model of the transducer, the expression for the change in capacitance can be extracted, and it is determined to be:

$$\Delta C = \frac{\Delta V * C_{total}}{V_{pp}} \tag{4-5}$$

$$\Delta V = V_{pp,Load} - V_{pp,Rest} \tag{4-6}$$

$$C_{total} = C_{device} + C_{parasitic} \tag{4-7}$$

From which the sensitivity, *M*, can be determined as:

$$M = \frac{\Delta C}{\tau} = \frac{\Delta V * C_{total}}{\tau * V_{pp}} \tag{4-8}$$

Thus, with the values ΔV and V_{pp} known via measurements, C_{total} and shear stress τ are needed to determine the device sensitivity. To obtain C_{total}, an additional admittance spectroscopy measurement was taken in which the device under measurement was the combination of the aluminum shielding enclosure and the device with small gauge wire connections inside. This measurement gave the C_{total} value, outright, and with the capacitance of the device measured from previous spectroscopy measurements, the $C_{parasitic}$ calculation was simply the difference between the two, which was found to be approximately 7pF. The value τ in Pascals can be simply calculated from the known test mass of 90.6g. The shear force generated by this weight $F = m * a$ = 0.0906kg * 9.89 m/s^2 = 0.896034 N. This force corresponds to a shear stress $\tau = \frac{F}{A}$, where A = 1.8mm by 1.8mm = 3.24×10^{-6} m^2, giving a shear stress of τ = 274,000 Pa or 274 kPa. With these values, the values in Table 4.3 below that show sensitivity calculations for the different test trials from Table 4.2 above.

Trial Number	Calculated Sensitivity [F/Pa]
1	9.854e-22
2	6.376e-22
3	2.608e-22

Table 4.3. Measured Shear Stress Sensor Sensitivities for Bidirectional Device

With this sensitivity measurement, it was possible to compare the calculated behavior from the analytical and numerical models to the true device data. Particularly, this experiment was conducted on the bidirectional device variant with 4µm electrode traces, although the data can be extrapolated to the other devices. For the sake of testing, we focused on this device for no other reason than it was the first to be successfully packaged. The table below summarizes the analytical models' predicted sensitivities, the numerical model predicted sensitivities, and the average sensitivity based on the sensor testing measurements.

Source	Sensitivity Value [F/Pa]
Parallel Plate Analytical Model	4.139e-22
Projected Parallel Plate Analytical Model	9.788e-22
Parallel Wires Analytical Model	1.815e-21
COMSOL Numerical Model	9.364e-22
ANSYS Numerical Model	1.560e-21
Lab Measurement	6.279e-22

Table 4.4. Sensitivities from Analytical Models, Numerical Models, and Measurements for 4μm Bidirectional device.

Another valuable calculation for the device that could be drawn from the lab measurements was the minimum detectable signal (MDS) defined by the following expression:

$$MDS = \frac{N}{S}. \tag{4-9}$$

MDS is given in units of $\frac{Pa}{\sqrt{Hz}}$, where N is the noise floor measured in units of $\frac{V}{\sqrt{Hz}}$, and S is the sensitivity. Here, it is important to note that S is the sensitivity in units of $\frac{V}{Pa}$, instead of the previously defined M defined as $\frac{\Delta C}{\tau}$. Here, we assume the noise, N, to be $1\frac{nV}{\sqrt{Hz}}$, which is typical of available electronics. In regards to S, the voltage output per Pascal of shear stress must be determined. This is a fairly simple calculation, as it was know what the voltage output swing was for a given shear stress generated by a known test mass. Using the voltage swings in Table 4.2 and a known test mass of 0.0906 kg generating 274kPa of shear stress, the average sensitivity S of the three trials was found to be $S = 1.58 \times 10^{-10}$. The MDS can then be calculated with the assumed value of N, resulting in an estimated minimum detectable signal of roughly $6.32\frac{Pa}{\sqrt{Hz}}$. This value

considerable underperforms the previous generation shear sensor device presented in [11], which was estimated to be 0.0529 $\frac{Pa}{\sqrt{Hz}}$ at a frequency of 1.5 kHz. The difference in device capability is mainly due to the different sensing mechanism, in which it is clear that in this case, piezoelectric sensing is superior. It is also important to note that the sensitivity of the capacitive shear stress sensor is dependent on the bias voltage level. By increasing the V_{pp} level, the voltage swing for a given shear stress load increases. This means that the capacitive shear stress sensor can give improved readings with increased bias voltage, but to be as effective as the piezoelectric shear stress sensor, the bias voltage would need to be on the order of 10^3 V, which may damage the device.

Despite the instability from one measurement to the next, the few consistent measurements we were able to obtain showed sensitivities that fall squarely in the range predicted by the analytical and numerical models. With these agreeable results, we were confident that we had thoroughly modeled and predicted the device's behavior, and also confident that we had successfully characterized the device's behavior by testing its functionality in a laboratory controlled experiment.

Chapter 5: Conclusion

In this document I have presented the design, fabrication, and characterization of a shear stress sensor utilizing differential capacitive sensing. This device was designed to meet several specifications set out by the Air Force Office of Scientific Research (AFOSR). Particularly, this sensor was intended to fulfill the need for a shear stress sensor that could measure static flow, commonly referred to as DC flow. Previous generations of the device had utilized piezoelectric transduction as the mechanism for sensing dynamic or AC flow. These generations were limited to dynamic flows due to the ephemeral signals produced by piezoelectric transducers. The previous generation of this shear stress sensor provided a photolithography mask set that could yield a device of the same general shape and geometry, but with a new embodiment in which a dielectric film replaced the piezoelectric film. In this way, a differential capacitive sensor would be fabricated instead of a piezoelectric transducer. The capacitive shear stress sensor described in this paper is capable of sensing static flow conditions due to the sensing mechanism. In capacitive sensing, a capacitor is monitored for a departure from its resting state capacitive value. This departure from the resting value can be used in conjunction with the device geometry and intrinsic physical and electrical properties to calculate the shear stress on the device. From these shear stress measurements, the user can further deduce information about the flow environment.

To develop this sensor, we first created analytical and numerical models to represent the theoretical device. These models would provide a reference for comparison of the true sensor's behavior after fabrication, allowing us to ascertain the viability of the device, and characterize the sensing capabilities of the devices once fabricated.

Analytical models were constructed using the well-known equation for capacitance of a parallel plate capacitor, $C = \frac{\varepsilon_r * A}{d}$. Although our device did not exactly represent a parallel plate capacitor physically, the estimate would provide a baseline for device metrics and behavior. Additionally, the device was analytically modeled using the known equation for capacitance between two cylindrical wires. Again, although this is not a true physical representation of the device, it was a worthy starting point for device behavior prediction. With the known mechanical properties of the dielectric film material, SU-8 3005, the deflection of the top surface of the film due to 1 Pascal of shear stress was calculated. Under this stress, the capacitance slightly changes, and this change can be predicted using the analytical models, yielding a device sensitivity, $M = \frac{\Delta C}{\tau}$, which was used as the figure of merit for this project. The analytical models predicted a sensitivity in the range of 2×10^{-22} to 4×10^{-21} F/Pa, depending on which device embodiment was selected. For the purposes of comparison, the model for the bidirectional device with 4μm electrodes was useful. For this model, the analytical sensitivity predictions were roughly 4.1×10^{-22} F/Pa, 9.7×10^{-22} F/Pa, and 1.8×10^{-21} F/Pa.

The devices were next modeled numerically using COMSOL and ANSYS finite element analysis software. These models numerically predict the original device capacitance, the deflection of the top surface of the device due to 1 Pascal of shear stress, the new capacitance under the load, and finally the sensitivity of the device. The numerical models both predicted a sensitivity roughly equal to 1×10^{-21} F/Pa. Comparison of the numerical model to the analytical model shows reasonable agreement, and so we were comfortable moving forward with the device development.

The fabrication of the device was separated into three main phases: bottom electrode, middle dielectric layer, and top electrode. The devices were fabricated 500μm silicon wafers, with a thermally oxidized silicon dioxide electrical isolation layer with a

thickness of 1μm. In the bottom electrode phase, photolithography was used to create a pattern for the bottom electrodes. Titanium was deposited on the sample via DC Sputtering in a Univex 450 sputtering system. Acetone submersion followed, dissolving the remaining photoresist and lifting off the unwanted metal, leaving an intricate bottom electrode pattern in place. In the next phase, photolithography is again used to develop the middle dielectric layer of the devices. MicroChem's SU-8 3005 epoxy-based negative photoresist was selected because of its expected compliance and its capabilities as a permanent installment in MEMS devices after hard baking. The main challenge with properly constructing these SU-8 structures was optimizing the use of the associated adhesion promoter, MicroChem's OmniCoat, in combination with the hard baking step. Without hard baking, the thin OmniCoat layer improved adhesion between the SU-8 and the substrate. However, after hard baking, the OmniCoat became a weakness in the SU-8 structures and made them susceptible to delamination during later processing steps. Ultimately, it was found that hard-baked SU-8 adhesion was strongest in the absence of an OmniCoat layer between the silicon dioxide substrate and the SU-8 dielectric layer. In the final and most challenging phase of the fabrication, the top electrode was deposited on top of the dielectric layer using the same process as in the first phase's bottom electrode deposition. The challenge was to achieve proper adhesion between the SU-8 and the deposited metal. The solution discovered was to apply a layer of OmniCoat to the top of the hard-baked SU-8 before depositing the metal. This properly facilitated the adhesion between the titanium electrodes and the SU-8 dielectric surface, although it did introduce a surface defect that we were unable to completely eliminate. After completion of the fabrication, the wafers were diced to isolate each device, then mounted and wired to a printed circuit board for testing.

Following the fabrication, the shear stress sensors were evaluated for their functionality so as to be compared to the predicted behavior from the analytical and numerical models. Testing consisted of two primary experiments. In the first experiment, the devices' electrical properties, specifically device capacitance and the dielectric constant of the SU-8 3005 dielectric layer, were measured using admittance spectroscopy. The relative dielectric constant for the SU-8 3005 present in our sensors was determined to be 3.8. Admittance spectroscopy was used to obtain capacitance measurements for each device variant, and these measurements reasonably agreed with the capacitance estimations given by the numerical models. With the intrinsic properties of the devices measured, it was possible to evaluate the sensing capabilities. By applying a shear stress load in the directions perpendicular to the length of the sensing cells, while applying sinusoidal voltage signals of opposite polarity to the input ports of the device, the output voltage signal was also a sinusoidal signal that increased or decreased in amplitude under the load. The difference in the output amplitude, in addition to the total capacitance of the device and the wiring scheme, could be used in conjunction to estimate the sensitivity of the devices. While this experiment suffered due to the viscoelastic mechanical properties of the SU-8, the sensitivity was still successfully estimated to be roughly 6.3×10^{-22} F/Pa. While not in exact agreement with the numerical and analytical estimations of sensitivity, the measured sensitivity is reasonably close to these values, and we were pleased with the result.

The sources of disparity between the simulated sensitivity and the measured sensitivity are likely due in large part to the idealized assumptions that were used when creating the models and simulations. The analytical model initially treated the device unit cells as ideal parallel plate capacitors, which is an obvious departure from reality that greatly simplifies the complex nature of the electric field present in the true devices.

Furthermore, the models only focused on the device unit sensing cell arrays, while the device infrastructure to wire these arrays together, as well as the bond pad structures, were ignored in calculations. These elements contribute to the overall capacitance of the device even though they are not intended to contribute to the sensing functionality. Including these elements in the model causes it to become too large and complicated to manage, and so they were ignored, inevitably introducing more error into the models' predicted capacitance values. Fabrication introduces another source for error as the target device dimensions are not precisely realized, and are certainly not constant across an entire silicon wafer. The SU-8 film thickness, for example, was intended to be 4μm thick, but was measured to be in the range of 4.6-5.2μm, with considerable variation depending on the location on the wafer. These nuances that the physical devices are subject to create unavoidable disparities between the idealized device simulations and the real sensors produced.

There are many directions this work could be taken in the future. On a small scale, the device quality could be marginally improved by further investigation of the OmniCoat surface defect introduced in fabrication. No clear remedy was found during this project, and so the device yield percentage per wafer was negatively impacted. Through investigation of a way to prevent this defect, or perhaps an alternative adhesion promoter for the top electrode processing, this negative impact of these defects could be mitigated and possibly even eliminated. Many of the limitations and uncertainty in device behavior originated with the dielectric SU-8 film, and so it is a worthy candidate for further research. An investigation into ideal materials to replace the SU-8 could be executed to find a material better suited for this application. A replacement material would ideally have an increased dielectric constant, a higher compliance, deformation behavior that is as close to exclusively elastic as can be found, and potential robustness to

high temperatures. This would increase the capacitance and sensitivity, while making the device behavior more predictable as far as relaxation time after a load is applied then removed. The challenge would likely be finding a material compatible with the fabrication requirements that exhibits the robustness and permanent capabilities of SU-8. Equally important in future work is the implementation of this device in true flow measurement scenarios. As mentioned at the outset of this document, the target application for the device is at high speed, high temperature flow environments. While this particular device generation was not designed to withstand high temperatures, it is designed for high speed flows that can generate 5 Pascals or more of shear stress. Future work includes the implementation of this device for testing in true shear stress inducing environments, rather than in an experiment in which the load is tactilely applied to the sensor. It is likely that this experiment would occur in a high speed wind tunnel, particularly one that can generate high amounts of shear stress. Similarly, it would be of interest to integrate the sensor into a system that can demodulate the sinusoidal output of the sensor and provide a direct readout of the shear stress on the device. Finally, to make the device usable in a wider variety of environments, it would likely need to be integrated into a system that can provide input sinusoidal signals without the need for the entire dScope analyzer. The analyzer is too large to have present at every implementation of the sensor, and so a more compact alternative would boost the sensor's applicability to many scenarios.

Appendix A

Analytical Model MATLAB Script

```
clc; clear;
%% Compute Capacitance Using Wire formula
L = 1300e-6; %Length of electrode finger
separation = 2e-6;
trace_width = 4e-6;
height = 4.8e-6;
d = sqrt(height^2 + (separation+trace_width)^2);
a = sqrt((50e-9)^2 + (trace_width/2)^2);
Ep0 = 8.854e-12;
Epr = 3.8;
Ep = Epr*Ep0;
numberofFingers = 73; %68 for bidirectional
C_wire = (pi*Ep*L)/(acosh(d/(2*a))) %Capacitance per finger
C_totalWire = C_wire*numberofFingers;

%% Compute Capacitance Using Parallel Plate-like approach
C_parallel = Ep*L*trace_width/d
C_totalParallel = C_parallel*numberofFingers;

%% Adjusted Parallel plate using projection
theta = atan((4.8e-6)/(trace_width+separation));
trace_proj = trace_width*sin(theta);
d = (trace_width + separation)/(cos(theta));
d_proj = d - 2*(0.5*trace_width*cos(theta));
A = trace_proj*L;
C_ProjectedPlate = Ep*A/d_proj

%% Compute deflections
Pressure = 1;
A = (1.8e-3)^2;
F = A*Pressure;
tau = F/A;
E = 2.0e9; % 2.0 GPa, According to MicroChem
nu = 0.22;
G = E/(2*(1 + nu)); %Shear Modulus
gamma = tau/G
deflection = height*tan(gamma)

%% Calculate New capacitance with deflection
separation_new = separation + deflection;
d_new = sqrt(height^2 + (separation_new+trace_width)^2);
C_wire_new = (pi*Ep*L)/(acosh(d_new/(2*a))); %Capacitance per finger
C_totalWire_new = C_wire*70;
deltaCwire = C_wire_new - C_wire;
SensitivityWire = abs(numberofFingers*deltaCwire/Pressure)
```

```
C_parallel_new = Ep*L*trace_width/d_new;
deltaCparallel = C_parallel_new - C_parallel;
SensitivityParallel = abs(numberofFingers*deltaCparallel/Pressure)

theta = atan((4.8e-6)/(trace_width+separation_new));
trace_proj = trace_width*sin(theta);
d = (trace_width + separation_new)/(cos(theta));
d_proj = d - 2*(0.5*trace_width*cos(theta));
A = trace_proj*L;
C_ProjectedPlate_new = Ep*A/d_proj;
deltaCproj = C_ProjectedPlate - C_ProjectedPlate_new;
SensitivityProjectedParallel = abs(numberofFingers*deltaCproj/Pressure)
```

Appendix B

ANSYS Model Script

```
!=============================================================
! SU-8 shear sensor simulation
! Randy Williams and Colton Snell
! 2016-10-14
! The University of Texas at Austin
!=============================================================
/FILNAME, SU8shear_unit_cell_APDL_v1, 1
/TITLE, SU-8 Shear Sensor
do_capacitance = 1
Lat_Disp_Test = 0
/PREP7
EMUNIT, mks                                  ! All units in meters, kg, seconds
*AFUN,DEG  ! units for angular functions are in degrees

!=============================================================
! Definition of geometry
!=============================================================
w_elec = 2.0e-6            ! width of electrodes
w_gap1 = 4.0e-6            ! width before + electrode
w_gap2 = 2.0e-6 !(2.0e-6 + 1.85059e-9)  ! width between + and groudn electrodes  2.8 for asymmetric (as
built) case
w_gap3 = 2.0e-6!(2.0e-6 - 1.85059e-9)   ! width between ground and - electrode 1.2 for asymmetric (as built)
case
w_gap4 = 4.0e-6            ! width after - electrode
depth = 1e-6       ! depth of unit cell parallel to electrode direction
ELEMSIZE = 0.2e-6
t_PZT = 4.8e-6             ! SU-8 thickness
t_air = 0.2e-6                       ! [m] - Thickness of air layer above film
t_TiOx = 0.1e-6
t_SiO2 = 1.0e-6
t_Si = 8.0e-6
bottom_loc = -t_SiO2-t_Si
BTOL, 1E-6
SELTOL, 1e-8

!=============================================================
! Draw the model
!=============================================================
BLC4, 0, 0, depth, t_PZT, w_gap1
WPOFFS, 0, 0, w_gap1
BLC4, 0, 0, depth, t_PZT, w_elec/2
WPOFFS, 0, 0, w_elec/2
BLC4, 0, 0, depth, t_PZT, w_elec/2
WPOFFS, 0, 0, w_elec/2
BLC$, 0, 0, depth, t_PZT, w_gap2
```

```
WPOFFS, 0, 0, w_gap2
BLC4, 0, 0, depth, t_PZT, w_elec/2
WPOFFS, 0, 0, w_elec/2
BLC4, 0, 0, depth, t_PZT, w_elec/2
WPOFFS, 0, 0, w_elec/2
BLC4, 0, 0, depth, t_PZT, w_gap3
WPOFFS, 0, 0, w_gap3
BLC4, 0, 0, depth, t_PZT, w_elec/2
WPOFFS, 0, 0, w_elec/2
BLC4, 0, 0, depth, t_PZT, w_elec/2
WPOFFS, 0, 0, w_elec/2
BLC4, 0, 0, depth, t_PZT, w_gap4
WPOFFS, 0, 0, -(3*w_elec + w_gap1 + w_gap2 +w_gap3)
ALLSEL, ALL
!WPOFFS, 0, t_PZT, (w_gap1 + w_gap2 + w_elec)
!BLC4, 0, 0, depth, 0.1e-6, w_elec
!WPOFFS, 0, -t_PZT, -(w_gap1 + w_gap2 + w_elec)
!ASEL, S, LOC, Y, t_PZT,t_PZT
!VEXT, ALL, , , 0, 0.1e-6, 0
ASEL, S, LOC, Y, 0, 0
VEXT, ALL, , , 0, -t_TiOx, 0
ALLSEL, ALL
ASEL, S, LOC, Y, -t_TiOx, -t_TiOx
VEXT, ALL, , , 0, -t_SiO2, 0
ALLSEL, ALL
ASEL, S, LOC, Y, -t_TiOx-t_SiO2, -t_TiOx-t_SiO2
VEXT, ALL, , , 0, -t_Si, 0
VGLUE, ALL                              ! Glues air and PZT layer
ALLSEL, All
surf_area = (3*w_elec + w_gap1 + w_gap2 +w_gap3 + w_gap4)*depth
!/view, , -1,0,0
!VPLOT
!/REPLOT

!=============================================================
!  Element types
!=============================================================
ET, 1, SOLID186                         ! Hexahedral coupled element  (w/ Keyopt:11 - Structural-thermal
analysis option)
ET, 2, SOLID226, 1001           ! (keyopt = 1001: Electroelastic Analysis)
ALLSEL

!=============================================================
! Material properties taken from DK's energy harvester code
!=============================================================
! Silicon ------------------------------------------------------------
density_beam = 2329                     ! Beam density (kg/m^3)
young_beam = 160E9                      ! Beam Young's Modulus (Pa)
poisson_beam = 0.23                     ! Beam Poisson ratio
MP, DENS, 1, density_beam               ! Density of Beam
MP, EX, 1, young_beam                           ! Young's Modulus of Beam
MP, NUXY, 1, poisson_beam               ! Poisson Ratio of Beam
```

```
TB, PIEZ, 1, , , 0                  ! Set the piezoelectric property to zero
TBDATA, 3, 0
TBDATA, 6, 0
TBDATA, 9, 0
TBDATA, 14, 0
TBDATA, 16, 0
TB, DPER, 1, , , 0                  ! Set the dielectric relative permittivity of SiO2
TBDATA, 1, 11.7, 11.7, 11.7
! SU-8 ---------------------------------------------------------------------
!SU-8 (isotropic)
MP, DENS, 2, 1075
MP, EX, 2, 2.0E9
MP, NUXY, 2, 0.22
TB, PIEZ, 2, , , 0                  ! Set the piezoelectric property to zero
TBDATA, 3, 0
TBDATA, 6, 0
TBDATA, 9, 0
TBDATA, 14, 0
TBDATA, 16, 0
TB, DPER, 2, , , 0                          ! Relative Permittivities at constant stain
TBDATA, 1, 3.8, 3.8, 3.8            ! in matrix form
! SiO2 ----------------------------------------------------------------------
MP, EX, 3, 70E+9          ! Young's modulus of SiO2
MP, NUXY, 3, 0.17         ! Poisson's ratio of SiO2
MP, DENS, 3, 2200                   ! Density of SiO2
TB, PIEZ, 3, , , 0                  ! Set the piezoelectric property to zero
TBDATA, 3, 0
TBDATA, 6, 0
TBDATA, 9, 0
TBDATA, 14, 0
TBDATA, 16, 0
TB, DPER, 3, , , 0                  ! Set the dielectric relative permittivity of SiO2
TBDATA, 1, 3.9, 3.9, 3.9
! TiO2 ----------------------------------------------------------------------
MP, EX, 4, 282E+9                   ! Young's modulus of TiO2
MP, NUXY, 4, 0.28         ! Poisson's ratio of TiO2
MP, DENS, 4, 3970                   ! Density of TiO2
TB, PIEZ, 4, , , 0                  ! Set the piezoelectric property to zero
TBDATA, 3, 0
TBDATA, 6, 0
TBDATA, 9, 0
TBDATA, 14, 0
TBDATA, 16, 0
TB, DPER, 4, , , 0                  ! Set the dielectric relative permittivity of SiO2
TBDATA, 1, 6.25, 6.25, 6.25

!=================================================================
! Material Assignment & Meshing
!=================================================================
SELTOL, 1E-10                       ! Tolerance for selection
VSEL, S, LOC, Y, 0, t_PZT
VSEL, R, LOC, Z, 0, w_gap1+w_elec
```

```
VATT, 2, , 2, 0
ESIZE, ELEMSIZE
ALLSEL, ALL
VSEL, S, LOC, Y, 0, t_PZT
VSEL, R, LOC, Z, w_gap1+w_elec, w_gap1+w_elec+w_gap2+w_elec/2
VATT, 2, , 2, 0
ESIZE, ELEMSIZE
ALLSEL, ALL
VSEL, S, LOC, Y, 0, t_PZT
VSEL, R, LOC, Z, w_gap1+w_elec+w_gap2+w_elec/2, w_gap1+w_elec+w_gap2+w_elec+w_gap3
VATT, 2, , 2, 0
ESIZE, ELEMSIZE
ALLSEL, ALL
VSEL, S, LOC, Y, 0, t_PZT
VSEL, R, LOC, Z, w_gap1+w_elec+w_gap2+w_elec+w_gap3,
w_gap1+w_elec+w_gap2+w_elec+w_gap3+w_elec+w_gap4
VATT, 2, , 2, 0
ESIZE, ELEMSIZE
ALLSEL, ALL
VSEL, S, LOC, Y, 0, -t_TiOx
VATT, 4, , 2, 0
ESIZE, ELEMSIZE
ALLSEL, ALL
VSEL, S, LOC, Y, -t_TiOx, -t_TiOx-t_SiO2
VATT, 3, , 2, 0
ESIZE, ELEMSIZE
ALLSEL, ALL
VSEL, S, LOC, Y, -t_TiOx-t_SiO2, -t_TiOx-t_SiO2-t_Si
VATT, 1, , 2, 0
ESIZE, ELEMSIZE
ALLSEL, ALL
VMESH, ALL
ALLSEL, ALL

!=================================================================
! Selecting electrode nodes
!=================================================================
!!! Colton, 10/14/16 - separating bottom electrodes
ASEL, S, LOC, Y, 0
ASEL, R, LOC, Z, w_gap1, w_gap1+w_elec
NSLA, S, 1
CP, 6, VOLT, ALL                                                    ! Set the degree of
freedom as Voltage for top electrode
*GET, N_GND2, NODE, 0, NUM, MIN                    ! Get the minimum no. of nodes from the nodes on
the surface
ASEL, ALL
ASEL, S, LOC, Y, 0
ASEL, R, LOC, Z, w_gap1+w_elec+w_gap2+w_elec+w_gap3,
w_gap1+w_elec+w_gap2+w_elec+w_gap3+w_elec
NSLA, S, 1   ! changed from A
CP, 1, VOLT, ALL                                                    ! Set the degree of
freedom as Voltage for top electrode
```

```
*GET, N_GND1, NODE, 0, NUM, MIN                    ! Get the minimum no. of nodes from the nodes on
the surface
ALLSEL, ALL
ASEL, S, LOC, Y, t_PZT
ASEL, R, LOC, Z, w_gap1+w_elec+w_gap2,w_gap1+w_elec+w_gap2+w_elec
NSLA, S, 1
CP, 2, VOLT, ALL                                   ! Set the degree of freedom as Voltage for top
electrode
*GET, N_POS, NODE, 0, NUM, MIN                     ! Get the minimum no. of nodes from the nodes on
the surface
ALLSEL, ALL

!=================================================================
! mechanical boundary constraints
!=================================================================
NSEL, S, LOC, Y, bottom_loc, bottom_loc        ! Constrain the bottom of the SU-8 layer from moving
D, ALL, UX, 0                                  ! Boundary condition
D, ALL, UY, 0                                  ! Boundary condition
D, ALL, UZ, 0                                  ! Boundary condition
ALLSEL, ALL
! Constraint the walls where the "slice" was sectioned to move in the y-z plane only. TODO: replace these
with a better symmetry condition
NSEL, S, LOC, X, 0, 0
NSEL, U, LOC, Y, bottom_loc, bottom_loc
D, ALL, UX, 0                                  ! Boundary condition
ALLSELL, ALL
NSEL, S, LOC, X, depth, depth
NSEL, U, LOC, Y, bottom_loc, bottom_loc
D, ALL, UX, 0                                  ! Boundary condition
ALLSEL, ALL
NSEL, S, LOC, Y, t_PZT, t_PZT
CP, 3, UX, ALL
CP, 4, UY, ALL
CP, 5, UZ, ALL
ALLSEL, ALL
NSEL, S, LOC, Y, t_PZT
NSEL, R, LOC, X, 0
NSEL, R, LOC, Z, w_gap1+w_elec+w_gap2+w_elec/2
*GET, N_top_mid, NODE, 0, NUM, MIN
ALLSEL, ALL
FINISH
!=================================================================
! Resting Position Capacitance calculation
!=================================================================
*IF, do_capacitance, EQ, 1, THEN
   /PREP7
   D, N_GND1, VOLT, 1
         D, N_GND2, VOLT, -1
   D, N_POS, VOLT, 0
   ALLSEL, ALL
   NSEL, S, LOC, Y, t_PZT, t_PZT  ! select nodes to apply no-shear condition
   D, ALL, UZ, 0
```

```
        D, ALL, UX, 0
        D, ALL, UY, 0
    ALLSEL, ALL
    FINISH
    /SOLU
    ANTYPE, STATIC                          ! Static Analysis
    BCSOPTION,,INCORE
    CNVTOL, U, 1E-15                    ! Displacement convergence tolerance
    CNVTOL, CHRG, 1E-11                     ! Charge convergence tolerance
    SOLVE
    *get, C_P, NODE, N_POS, RF, CHRG                ! Capacitance Calculation
        *get, C_G, NODE, N_GND1, RF, CHRG       ! Capacitance Calculation
        *get, C_G2, NODE, N_GND2, RF, CHRG
        C = C_P/depth                               ! the 0.6e-3 is in order to give the capacitance for
the length of the real device electrode for bidirectional
        C1 = ((C_P-C_G)/2)
        C2 = ((C_P-C_G2)/2)
   /COM Total capacitance C = %C% F             ! Print the capacitance value
        /COM Charge P = %C_P%
        /COM Charge G1 = %C_G%
        /COM Charge G2 = %C_G2%
        /COM C1 = %C1%
        /COM C2 = %C2%   These should be multiplied by number of unit cells in device
    FINISH
    /post1
        !PLVECT,U, , , ,VECT,ELEM,ON,0
    !PLVECT,D, , , ,VECT,NODE,ON,0
    !/VSCALE,1,0.5,0
    /view, , -1,0,0
    /REPLOT
    *CFOPEN, SU8cap_results_2000_nm, txt
    *VWRITE, 'C', C
    (A, E)
    *CFCLOS
*ENDIF

!=================================================================
! Lateral Displacement Test
!=================================================================
*IF, Lat_Disp_Test, EQ, 1, THEN

    /PREP7
    D, N_GND1, VOLT, 1
        D, N_GND2, VOLT, -1
    D, N_POS, VOLT, 0
    ALLSEL, ALL

    ALLSEL, ALL
    NSEL, S, LOC, Y, t_PZT, t_PZT  ! select nodes to apply shear
    CM, surf_nodes, NODE
    *GET, surf_node_count, NODE, 0, COUNT
    shear_stress = 1
```

```
    total_force = shear_stress*surf_area
    node_force = total_force/surf_node_count
    F, ALL, FZ, node_force
    ALLSEL
    !FINISH

    /SOLU
    ANTYPE, STATIC                              ! Static Analysis
        PSTRES, 0
        CNVTOL, U, 1E-15
        CNVTOL, CHRG, 1E-15
    BCSOPTION,,INCORE
    SOLVE
        !FINISH

        *get, x_disp, NODE, N_top_mid, UZ  ! get displacement of top middle node for compliance calc
        /COM x_disp from 274kPa shear = %x_disp%

    /post1
    RSYS, 0
    !PLVECT,D, , , ,VECT,NODE,ON,0
    !/VSCALE,1,0.5,0
    !/view, , -1,0,0
    !/REPLOT
        SAVE
        FINISH

*ENDIF
```

Appendix C

MATLAB Capacitance Correction Script

```
% This script is used to take the capacitances measured across the
three
% terminals of the piezoelectric shear sensors, and solve for the
indiviual
% internal capcitances between the electrode pairs.
% Randy Williams
% 2015-05-06
% Capacitances measured at the three terminals
C_no = 1.55;   % between negative bias and ground
C_po = 1.63;   % between positive bias and ground
C_pn = 3.27;   % between positive and negative bias
% Use terminal values as initial guesses for individual internal
% capacitances
C1 = C_no;  % between negative bias and ground
C2 = C_po;  % between positive bias and ground
C3 = C_pn;  % between positive and negative bias
% Iteratively solve for the individual internal capacitances, based on
% measured terminal values and initial guesses:
error_1 = 1; error_2 = 1; error_3 = 1;  n=0;
while max(abs([error_1, error_2, error_3]))>=0.0001
C1_new = C_no - (C2*C3)/(C2+C3);
C2_new = C_po - (C1*C3)/(C1+C3);
C3_new = C_pn - (C2*C1)/(C1+C2);
error_1 = (C1_new - C1)/C1
error_2 = (C2_new - C2)/C2;
error_3 = (C3_new - C3)/C3;
C1 = C1_new;
C2 = C2_new;
C3 = C3_new;
n=n+1
end
% return the three individual elemental capacitances:
C1  % between negative bias and ground
C2  % between positive bias and ground
C3  % between positive and negative bias
```

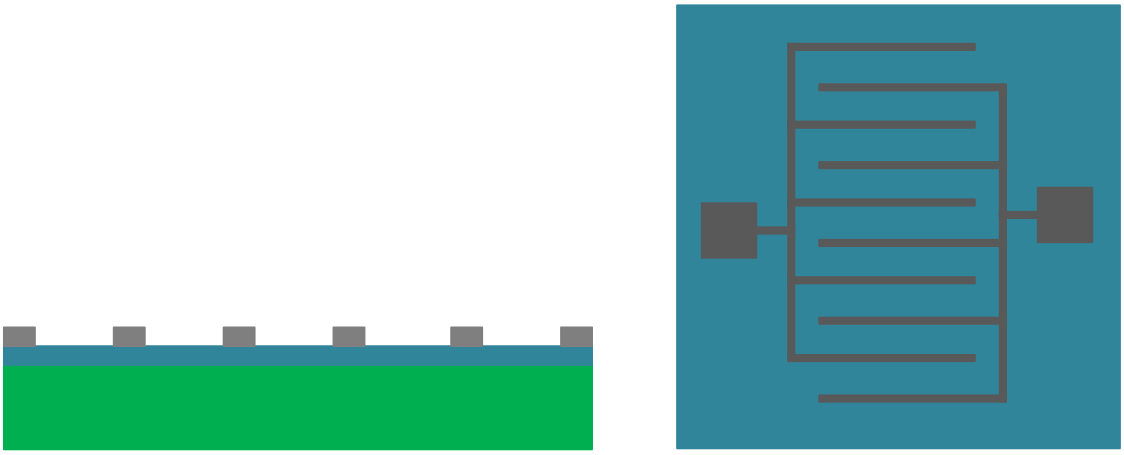
Appendix D

Fabrication Schematic

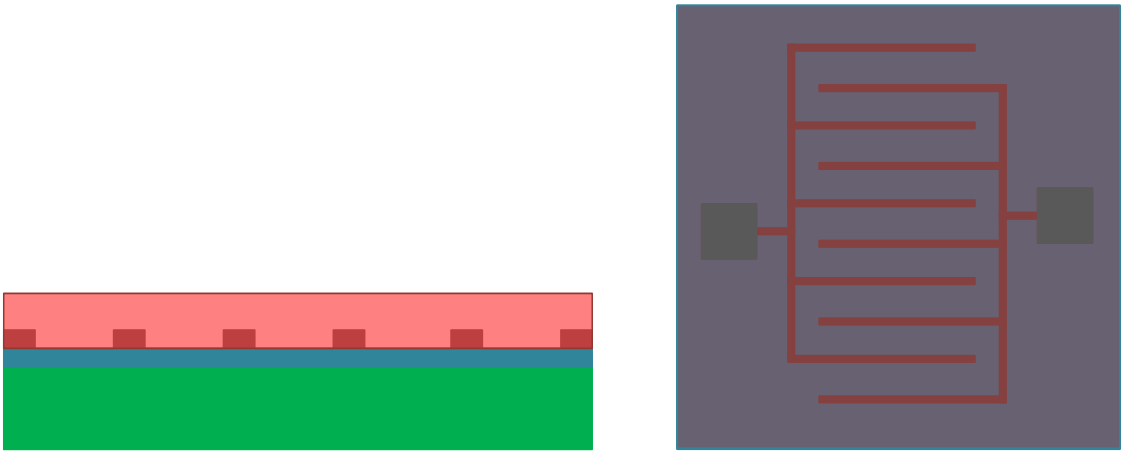
1. Silicon wafer is cleaned and a 1µm thick Silicon Dioxide passivation layer is thermally grown.

2. AZ 5214 Photoresist film coating is applied and patterned in shape of bottom electrode design.

3. Titanium is sputtered on the entire wafer. A thickness of 100-130nm is targeted for the electrode thickness.

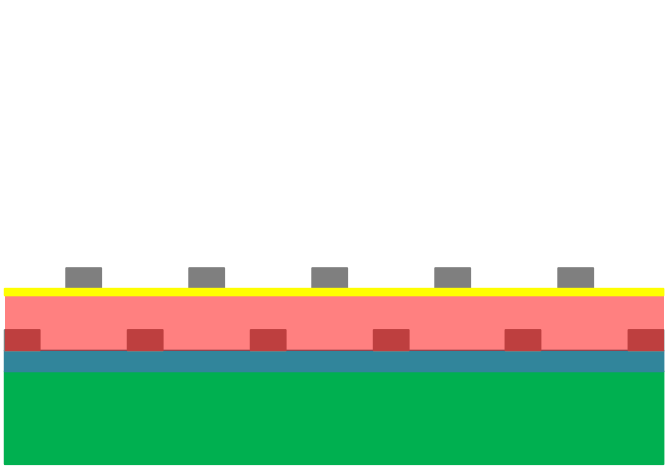


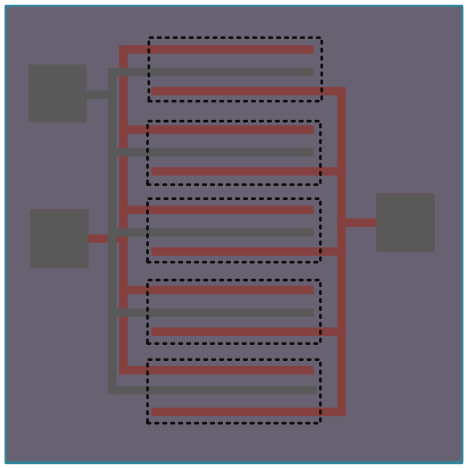
4. (Left) Wafer is submerged in acetone to initiate lift-off process, removing unwanted photoresist and titanium, leaving behind completed bottom electrode pattern. (Right) Top view of wafer showing simplified electrode pattern with bond pads included.



5. (Left) The dielectric layer, made of SU-8 negative photoresist, is coated on the wafer at a target thickness of 4µm (achieved 4.8µm). (Right) Top view of SU-8 coated wafer. The coating is patterned to isolate devices on the wafer and to uncover the bottom bond pads.

6. The SU-8 is hard baked to fully cure, then a thin coating of OmniCoat adhesion promoter is applied to the top of the SU-8 surface to prepare it for the top electrode deposition.





7. Repeating Steps 2-4, the top electrode metal is achieved with another round of photolithography, titanium sputtering, and lift-off. (Right) top view illustrates the top electrode pattern, completing the unit cell structures, which are indicated by the dotted boxes. This completes fabrication and the wafers is prepared for dicing and packaging.

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