Solid-State Fault Current Limiting for DC Distribution Protection

L. Qi, J. Pan
Corporate Research Center
ABB Inc.
Raleigh, NC, U.S.A.
{lisa.qi, jiuping.pan}us.abb.com

X. Huang
Corporate Research Center
ABB Ltd.
Beijing, China
Helen-xing.huang@cn.abb.com

X. Feng
Center for Electromechanics
University of Texas at Austin
Austin, TX, U.S.A
x.feng@cem.utexas.edu

***Abstract*—This paper discusses solid-state fault current limiting technologies. Both solid-state fault current limiters and converters can quickly limit DC fault currents and permit other protective devices to perform appropriate fault interruption and/or isolation. Different system protection strategies using solid-state fault current limiters and converters are presented and analyzed. The advantages and disadvantages of different methods are also discussed and compared.**

Keywords—solid-state, fault current limiting, fault current limiters, converters

I. INTRODUCTION

Fast DC current interruption or limiting is required by DC distribution due to fast increasing DC fault currents contributed by distributed capacitors and DC sources. In DC distribution systems, solid-state protective devices are preferred since they can rapidly limit the increasing DC fault currents with ultrafast speeds and reduce downstream fault capacities. In the literature, solid-state fault current interruption devices, such as solid-state circuit breakers, may also be counted as solid-state fault current limiting devices since peak fault currents are limited by interruption. However, fault current limiting devices are different from fault current interruption devices in that they limit fault currents and allow other protective devices to interrupt or isolate faults. Different requirements on solid-state interruption and limiting devices in utility systems are given in [1][2]. The solid-state fault current limiting devices to be discussed in this paper are solid-state fault current limiters and converters.

In this paper, the fault management using solid-state fault current limiting devices is studied for DC distribution systems, such as shipboard power systems. Solid-state fault current limiters and converters have different applications, impacts, benefits, and shortcomings. In general, a fault current limiting device reduces DC fault currents, and thus allows fault segregation by low cost protective devices at downstream. The reduced fault currents potentially leave more time for fault location, fault isolation, and system restoration.

The outline of this paper is given as follows. In Section II, solid-state fault current limiters and a system protection approach is discussed. In Section III, converter fault handling methodologies and the corresponding system protection strategy are presented. Finally, a summary of this paper and conclusions are given in Section IV.

II. SOLID-STATE FAULT CURRENT LIMITERS

In AC systems, different series, bridge, and resonant types of solid-state fault current limiters shown in Fig. 1 are reviewed and summarized in [3]. Currents at normal conditions flow through Solid-State Switches (SSSs) and the fault current limiting function is achieved by insertion of inductors. In bridge and resonant types of limiters, the inductors are compensated at normal conditions and have little or no impact on normal currents.

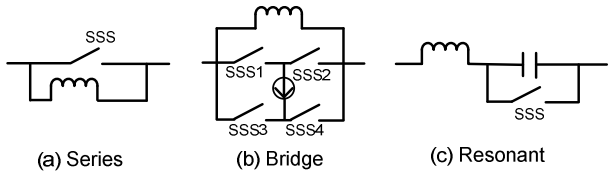

Fig. 1. Diagrams of solid-state fault current limiters for AC systems

In DC systems, series and bridge types of solid-state fault current limiters are still applicable. For the bridge type fault current limiters, normal currents flow through the inductor connected in the bridge circuit. In addition to the selection proper semiconductor devices, the selection of limiting inductors is one major design challenge. Saturation of the inductors at DC fault condition should be avoided in order to ensure the fault current limiting functionality. Superconductive inductors may be used in the bridge type of solid-state fault current limiters in order to have low conduction losses at normal conditions. In addition, the superconductive inductors can also be used as energy storages for backup during emergency [3].

As described earlier, the solid-state fault current limiters reduce fault currents but not necessarily interrupt fault currents. In order to provide a cost effective system protection solution in practical applications, solid-state fault current limiters can be

placed upstream, and low fault interruption protective devices, such as conventional mechanical circuit breakers, downstream [1][2]. This system protection solution is cheaper than a full solid-state DC protection solution but can still reduce fault currents and energy for protected equipment. This solution can satisfy selectivity by tripping and opening the protective devices closest to the identified fault locations.

The implementation of the previously described protection solution on an AC distribution system is shown in Fig. 2. A series type of solid-state fault current limiter, SSFCL, is used at upstream and two conventional mechanical circuit breakers, MCB1 and MCB2, are downstream. The current flowing through the limiter and the bus voltage are measured and shown in Fig. 3. A fault is applied downstream of MCB1. After the fault occurrence, SSFCL reacts immediately to limit the fault current. The fault current is reduced but maintained above the short-time tripping level of the downstream MCB1. MCB1 thus trips and opens after certain mechanical operation time delay. Depending on system voltage tolerance, fast mechanical circuit breakers can be selected to reduce the time of the system under low voltage. Once the fault is cleared, the SSS of SSFCL recloses and the source continues to supply power to the healthy loads downstream of MCB2. The implementation of the system protection solution to a DC distribution system would be similar to the AC distribution system. To ensure cost-effectiveness, either conventional AC circuit breakers or mechanical DC circuit breakers can be applied as downstream circuit breakers.

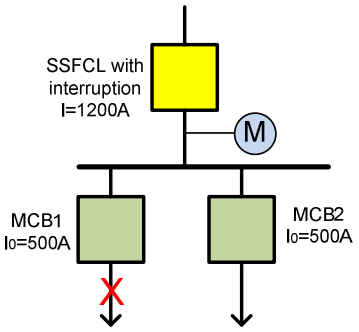

Fig. 2. Implementation of a solid-state fault current limiter in an AC distribution system

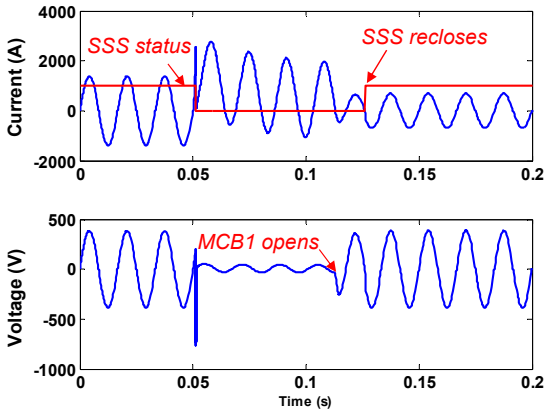

Fig. 3. The simulated SSFCL current and bus voltage

III. Converter Fault Current Handling

DC fault currents can be actively limited or bypassed by converters. Converter topology and control are critical in different converter fault current handling technologies. Some converter can not only limit fault currents but also further reduce DC fault currents to zero. Thus, low cost no-load DC switches can be applied with such converters to isolate faults and for maintenance. This system protection solution is feasible to some system applications and may be more cost-effective than other protection solutions.

A. Converter Fault Current Limiting

For economic and efficiency reasons, most commercially used converters in Low Voltage DC (≤1kV) and low end Medium Voltage DC (≤10kV) distribution systems are two- or three-level Voltage Source Converters (VSCs); while in high end MVDC (≥20kV) distribution systems, multi-level converters and Modular Multi-level Converters (MMCs) are advantageous.

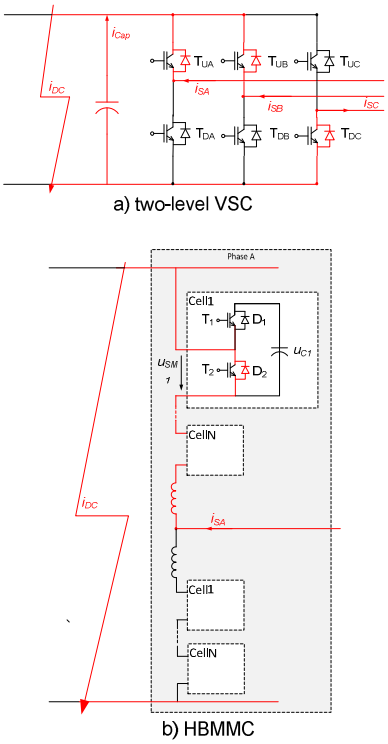

Fig. 4. DC short circuit paths of VSCs and HBMMCs

Usually, conventional two-level VSCs handle DC faults by turning-off all IGBTs in order to prevent device breakdowns. The fault current paths of a two-level VSC and a HBMMC (Half Bridge MMC) after the IGBT turning-offs are indicated in Fig. 4. DC fault currents from upstream sources are uncontrollable because of freewheeling diodes. In two-level VSCs, the capacitors discharge during DC faults. The capacitors in the HBMMC are prevented from discharging due to the turning-offs of IGBTs, but there are circulating fault currents due to the arm inductors. In summary, conventional two-level VSCs and HBMMCs cannot limit DC fault currents and DC circuit breakers are required to interrupt fault currents.

A comprehensive study of the fault behavior of different types of COTS (Commercial-Off-The-Shelf) low voltage converters can be found in [4]. Without any change in converter topologies or semiconductor devices, most of these converters do not have fault current limiting capability.

Advanced, more complex and expensive, converter topologies and control allow effective fault current limiting [5]-[11]. Examples of existing fault current limiting converters include thyristor rectifiers, DC-DC buck converters, Full Bridge Modular Multi-level Converters (FBMMCs), and Clamp double Modular Multi-level Converters (CDMMCs). The fault current and energy limited by a DC-DC buck converter are shown in Fig. 5. After a DC fault is detected, the buck converter reacts to limit the DC fault currents. A two stage fault limiting strategy can be employed. At the first stage, the fault currents are limited to low values, which can help accurately identify the DC fault location. High capacitor discharging still exist due to the delays of the converter control. At the second stage, the fault currents are further decreased to lower values to allow the opening of the low-current DC switches closest to the fault location. At the second stage, the fault currents are often reduced to zero to allow the fast opening of the no-load DC switches. The fault energies measured at different locations (level 3, 4, and 5) of the DC system are also reduced with the limited DC fault currents. In this way, the fault current withstands for downstream equipment are reduced consequently reducing equipment costs. It should be noted that the buck converter becomes a surge-less DC circuit breaker if the IGBT of its upper arm is always on at normal conditions and off at fault conditions.

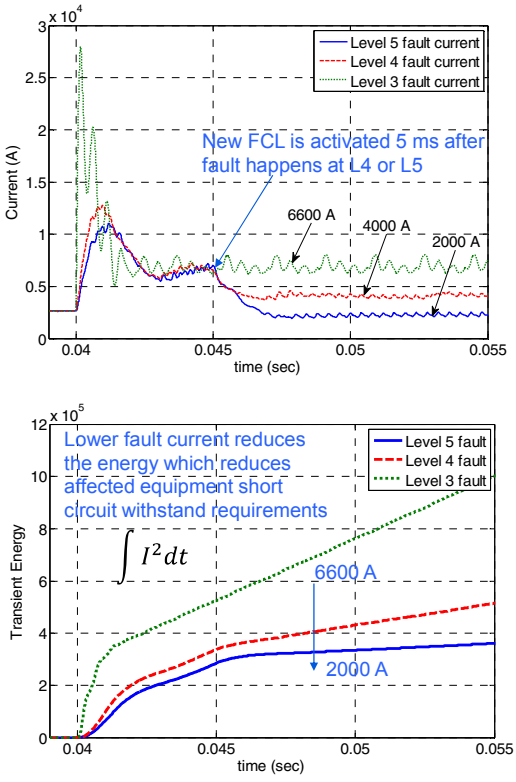

Fig. 5. Limited fault current and energy by a DC-DC buck converter

Active or controllable switches should be on DC fault paths to permit the converter fault current limiting. For example, the anti-parallel diodes of HBMMCs on fault paths can be replaced by thyristors to control fault currents [9]. Additionally, event switching puts different design requirements on the semiconductor switches compared to conventional converter switching. Higher design requirements, more controllable semiconductor switches, and more complex topologies lead to higher cost, lower efficiency, and lower reliability of converters. As a consequence, although protection function can be combined into a converter design, the converter fault current limiting may not to more cost-efficient than to a stand-alone solid state fault current limiting device.

B. Converter Fault Current Bypassing

Alternatively, converter fault current handling can be achieved by fault current bypassing. Artificial AC short circuits are created by manipulating active switches of converters [12]. A bypassing circuit of a two-level voltage source converter is shown in Fig. 6 [12]. An IGBT of one upper arm is closed and the AC source is short circuited. The fault currents from the AC source are unable to flow into the DC system. After the discharging currents of the converter capacitors go to zero, the DC fault current becomes zero. In HBMMCs, the fault bypassing scheme can also be implemented. For example, a double thyristor switch is added at each HBMMC submodule and can create a three-phase AC fault by short circuiting both upper and lower arms [13]. With natural damping, the DC fault current becomes zero once the circulating currents of the arm inductors are damped to zero [13]. Similar to the converter fault current limiting, some changes should be made to the conventional two-level voltage source converters and HBMMCs in order to apply the fault current bypassing. The changes should allow the converters to bypass DC fault currents and tolerate high AC fault currents.

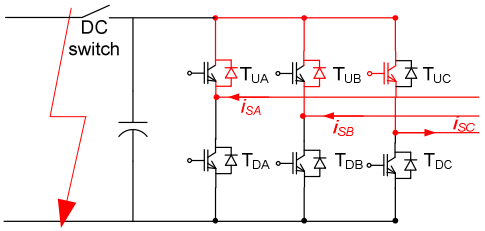

Fig. 6. DC fault current bypassing circuit of a two-level VSC [12]

In order to demonstrate the fault current bypassing of HBMMCs, two methods of bypassing DC fault currents [12], [13] are compared with the conventional method of turning-off all IGBT switches during dc faults. The equivalent HBMMC circuits of the three methods are presented in Fig. 7. In Fig. 7(a), both the AC sources and arm inductors contribute to DC fault currents if all IGBTs are turned off. By short circuiting all upper arms as described in [12], DC fault currents are only contributed from arm inductors as shown in Fig. 7(b). By connecting the inductors in upper arms and the capacitors in lower arms as described in [13], the DC fault current includes both contributions from the lower arm capacitors and the inductors as shown in Fig. 7(c).

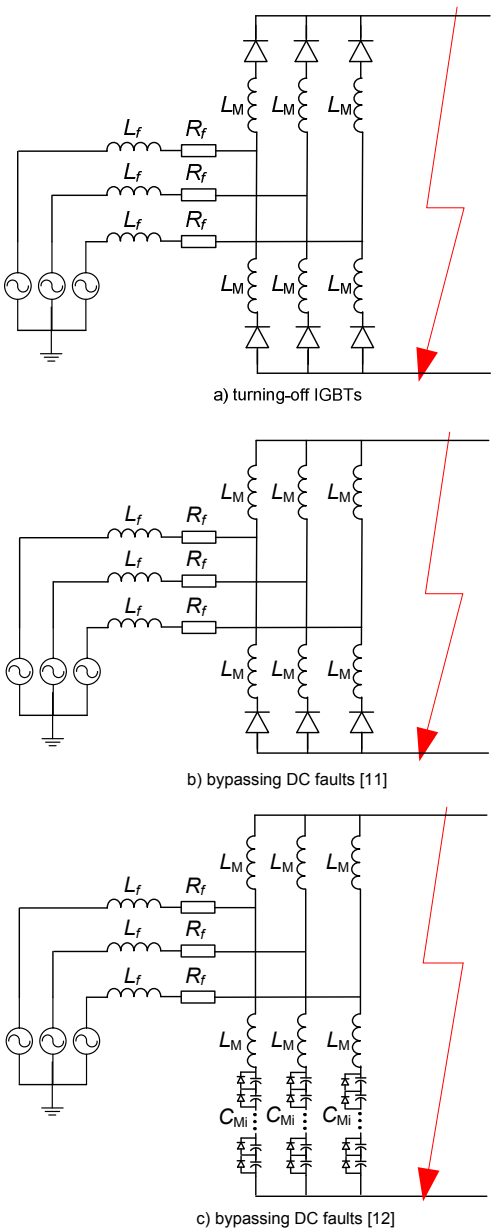

Fig. 7. Equivalent circuits of different DC fault current handling methods

The simulated DC fault currents of the three methods are shown in Fig. 8. All DC fault currents go to steady state values since no damping is modeled. The steady state DC fault currents are caused by arm inductors. In practical systems, the DC fault currents would gradually go to zero since natural damping exists on fault paths. In the conventional method of turning-off all IGBTs, the DC fault current is highest due to the sustained ccontribution from the upstream AC source. The semiconductor switches of all upper arms in the method given in [12] should have high ratings since they need to tolerant AC fault currents for a while. The DC capacitors discharge during the initial transients if the lower arms are connected in the way as described in [13]. Therefore, system restoration is longer in order to recharge these capacitors. This method is not recommended for practical applications since high capacitor discharging exist and may cause damages to system and equipment.

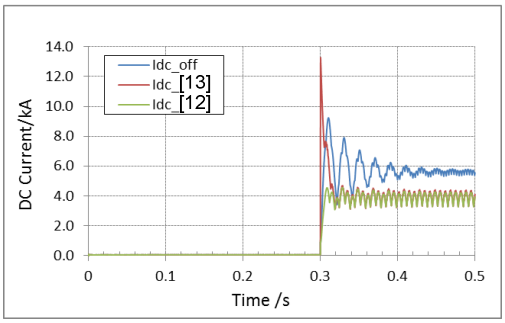

Fig. 8. Simulated DC fault currents of three DC fault handling methods

C. Fault Location and System Restoration

A complete process of converter fault current handling starts from fault occurrence and ends at system restoration. Communication based fault location methods work well in this case since the protection speed requirement is relaxed after DC fault currents are quickly limited or bypassed. After DC fault currents become zero, no-load DC switches closest to fault locations can isolate DC faults. Once the faults are isolated, the system can be restored. It should be noted that selectivity is lost in the converter fault handling methods since affected converters should be shut down or bypassed in order for no-load switches to open at zero current. In a ring configuration system, loss of power occurs at a DC fault downstream of the ring since all converters contribute to the fault currents of the DC switches next to the fault. This is a major disadvantage of using converters compared to using solid-state fault current limiters for the DC fault current limiting.

The longer time a converter takes to limit or bypass DC fault currents, the higher stresses on a system due to high DC fault currents. Thus, the maximum allowable time to limit DC fault currents is decided by the maximum fault withstands of the system at high DC fault currents. The maximum allowable time for fault location, isolation, and system restoration can be obtained from the maximum fault withstand of the system at low DC voltage or high AC fault currents. With the converter fault limiting technology, the maximum fault withstand is the maximum allowable time for the system to survive at low voltage. With the converter fault current bypassing technology, high fault currents continue to flow through the converter and its upstream system until the converter is restored to normal operation. The maximum fault withstands of the converter and its upstream system at AC faults determine the maximum allowable time for fault location, isolation, and system restoration.

Conventional differential and current direction protection methods can be used to detect and location DC faults. Since the DC fault currents are quickly limited after fault detection, high speed fault location and isolation are no longer required by the converter fault current limiting technology. It is possible the same hardware and software setup of AC differential and current direction protection may still be applicable to the

converter fault current limiting technology. The converter fault current bypassing technology requires faster fault location and isolation than the converter fault current limiting technology since high fault currents continue to flow through the converter and its upstream system even after the DC fault currents are bypassed. Fast fault location, isolation, and system restoration are thus required to reduce the electrical stresses on the converter and its upstream system.

IV. Summary and Conclusions

A fault protection solution can be a proper combination of a solid-state fault current limiting technology applied with a fault isolation technology. Because of rapid fault current limiting by solid-state switches, the speed requirement on DC protection derived from the fault withstands of protected systems can be relaxed. The choice of a proper fault protection solution is application dependent with considerations of required system protection features.

DC distribution protection can be achieved by solid-state fault current limiters at upstream to limit fault currents and conventional mechanical circuit breakers at downstream to trip and isolate faults. Selection of appropriate limiting inductors is the key to design solid-state fault current limiters.

DC distribution protection can also be accomplished by converters to reduce DC fault currents to zero and no-load switches to isolate faults. Converter topologies and control are critical both for fault current limiting and bypassing. Main shortcomings of the converter fault current handling include

- DC fault currents may not be fully limited due to the uncontrollable discharging from capacitors and inductors;
- Selectivity could be lost due to the shut-downs of multiple converters;
- Some changes in topologies and/or semiconductor switches are necessary to allow controllable switching on fault paths, which normally results in increased cost;
- Converters need to be restarted and restored to normal operation after faults are isolated;

Between the two converter fault current handling technologies, the converter fault current limiting has lower requirements on device ratings of converters and speed of fault location, isolation, and system restoration than the converter fault current bypassing.

References

[1] R. K. Smith, P. G. Slade, M. Sarkosi, E. J. Stacey, J. J. Bonk, H. Mehta, "Solid-state distribution current limiter and circuit breaker: application requirements and control strategies," *IEEE Trans. Power Delivery*, vol. 8, no. 3, pp. 1155-1164, July 1993.

[2] P. G. Slade, R. E. Voshall, J. Porter, L. Hong, "The utility requirements for a distribution fault current limiter", in IEEE Trans. On Power Delivery, Vol. 7, No. 2, April 1992, pp. 507-515.

[3] A. Abramovitz, K. M. Smedley, "Survey of solid-state fault current limiters," *IEEE Transs. Power Electronics*, vol. 27, no. 6, pp. 2770-2782, June 2012.

[4] ABB, "Faults in LVDC microgrids with front-end converters", 2015. [online]https://library.e.abb.com/public/a4760216a7d24bbabe5946f9d193ff40/1SDC007113G0201.pdf.

[5] P. Salonen, P. Nuutinen, P. Peltoniemi, J. Partanen, "LVDC distribution system protection – solutions, implementation and measurements," in *Proc. 2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1-7.

[6] P. Salonen, P. Nuutinen, J. Partanen, "Protection scheme for an LVDC distribution system," in *Proc. 20th International Conference on Electricity Distribution, 2009, pp. 1-4*.

[7] R. M. Cuzner, V. Singh, "Future shipboard MVdc system protection requirements and solid-state protective device topological tradeoffs," *IEEE Journal of Emerging and Selected Topics in Power Electronics, Special Issue on Emerging Electric Ship MVDC Power Technology*, vol. 5, no. 5, pp. 244-259, March 2017.

[8] R. Cuzner, D. MacFarlin, D. Clinger, M. Rmmey, G. Castles, "Circuit breaker protection considerations in power converter-fed DC systems," in *Proc. 2009 IEEE ESTS*, Washington D.C., 2009, pp. 360-367.

[9] B. Bertil, N. Staffan, and J. Tomas U., "Fault Current Limitation in DC Power Transmission Systems", Patent US8830708 B2, Sept. 11, 2009.

[10] D. Schmitt, Y. Wang, Th. Weyh, R. Marquardt, "DC-Side Fault Current Management in extended Multi terminal-HVDC-Grids," in *Proc. the 9th International Multi-Conference on Systems, Signals and Devices*, 2012, pp 1-5.

[11] R. Marquardt, "Modular Multilevel Converter Topologies with DC-Short Circuit Current Limitation," in *Proc. 2011 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2011, pp. 1425-1431.

[12] T. David, D. C. Clharnock, and O. Nuamdl, "Converter for HVDC Transmission and Reactive Power Compensation", Patent US9065299B2, June 18, 2010.

[13] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, L. Li, "Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems," *IEEE Trans. Power Delivery*, vol. 28, no. 1, pp. 483-490, Jan 2013.

[14] Z. XiaoPing, L. Zhou, "Power Converter", Patent application 2013079937A3, Nov. 30, 2011.