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Graphene and Hexagonal Boron Nitride Heterostructures For Beyond CMOS Applications

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Graphene and Hexagonal Boron Nitride Heterostructures For Beyond CMOS Applications

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Graphene and Hexagonal Boron Nitride Heterostructures For Beyond CMOS Applications

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Scaling limits of conventional complementary metal oxide semiconductor (CMOS) technology has motivated the research of numerous *beyond CMOS* device concepts. One such device is the interlayer tunnel FET (ITFET). This device is demonstrated using the two-dimensional (2D) materials bilayer graphene and hexagonal boron nitride (hBN). Stacking these materials together, we fabricate a double bilayer graphene and hBN heterostructure where the two graphene layers function as the top and bottom electrodes and the hBN as the tunnel barrier of the ITFET. Significant negative differential resistance (NDR) in the interlayer current-voltage characteristic is demonstrated at room temperature. Electrostatic analysis reveals that the multiple NDR peaks are due to energetic band alignment between the two sub-bands of the top and bottom bilayer graphene at the *K*-point of the Brillouin zone. Temperature dependent and parallel magnetic field measurements are conducted to further confirm that the conduction mechanism is momentum and energy conserving resonant tunneling. In addition, we demonstrate how the NDR can be used for implementing a one-transistor static random access memory element.

Improvements in the transfer method which allowed rotationally aligned top and bottom electrode layers, made possible extensive experimental studies of 2D heterostructure based ITFETs. Utilizing such technique, we conducted experiments

involving thicker multilayer graphene. We analyze how the graphene thickness and stacking order can influence the resonance condition and how this affects the overall device characteristic. The effects of interlayer hBN scaling such as increased tunneling current and peak position shifting is also briefly dealt with. Current-voltage simulations based on Bardeen transfer Hamiltonian approach were conducted for these devices, and it is shown that the peak positions predicted by theory match well with those obtained through measurements.

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CHAPTER 1: Introduction

1.1 MOTIVATION: SCALING LIMITS OF CMOS

The rapid scaling of Si-based metal oxide semiconductor field-effect transistors (MOSFETs) or complementary MOS (CMOS) allowed an exponential increase in the density and performance of integrated circuits (ICs) [1],[2]. Following the so called Moore's law [1],[2], each new process technology node brought about a 50 % increase in operating frequency and 100 % increase in density [3]. This allowed vast improvements in our everyday lives by making possible the development of many electronic gadgets. Handheld devices now possess vast computing power at an affordable cost that is available to almost everyone. However, this simple trend of exponential improvement came to a halt when the operating frequency of ICs would no longer scale with each process node due to the limitation of power density. It was predicted that if the same trends continued, the power density on a chip would reach the level of a nuclear reactor, rocket nozzle, and eventually the surface of the sun [Figure 1.1] [3]. As a result, since the early 2000s, while the transistor density would continue to increase, the loss in the performance gain due to the frequency remaining constant had to be made up for elsewhere [Figure 1.2]. This was mostly achieved through architectural improvements, especially multi-core scaling, where the number of processing cores would be increased for parallel processing. However, according to Amdahl [4], the gain in performance through multi-core scaling is limited by how much of a workload can actually be parallelized. For example, for a workload that has a portion of 50 % that can be processed in parallel, the speed up from the multi-core scaling would be limited to 2X regardless of how many processing cores are employed. Moreover,

as the number of cores increase, due to the overall power constraints, not all cores can be used simultaneously and a large portion of them – as much as 50 % – have to be powered down, limiting the performance gain [5]. Without vast improvements in the power consumption of the individual transistor device, multi-core scaling could also come to an end [6]. This demands the development of a new device that can fundamentally overcome such problems relating to power consumption that plagues Si-based CMOS technology. There are numerous device concepts that have been proposed and demonstrated for this purpose. These devices are commonly referred to as *beyond-CMOS* devices. While some of these devices are based on completely different physical properties such as electric dipole, magnetic spin, and orbital states for switching operations, some are still based on charge transport. In this work we focus on beyond-CMOS charge based tunneling FETs.

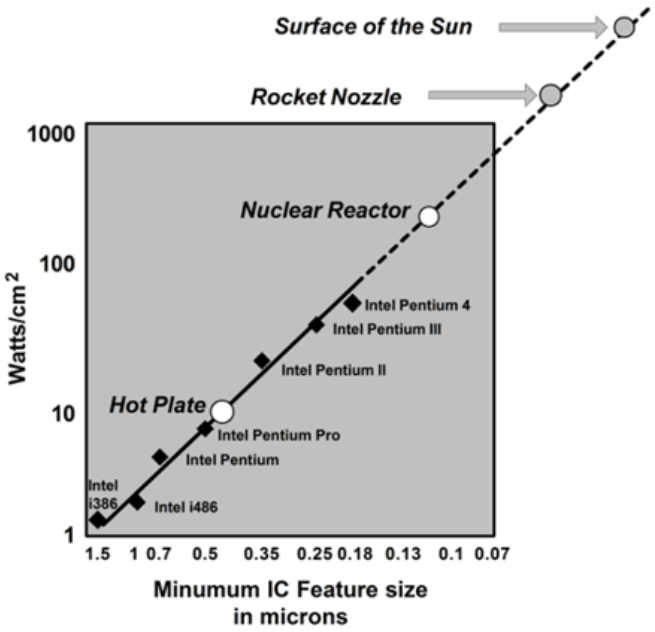

Figure 1.1 If frequency scaling continued at the same pace, power density on an IC would have reached that of the surface of the sun. Adapted from [3].

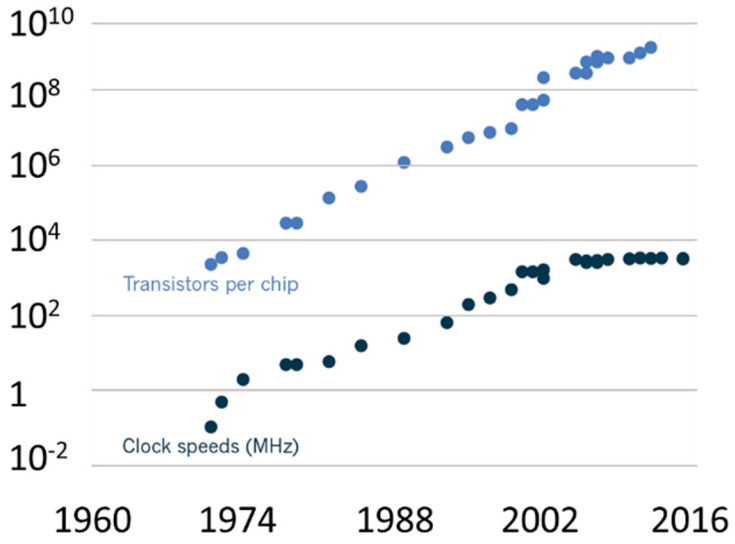

Figure 1.2 Scaling of transistor density and plateauing of frequency scaling during the early 2000s. Adapted from [6].

1.2 Emergence of 2D Materials

1.2.1 Graphene

While on the one hand the scaling limits of CMOS are becoming more and more apparent, at the same time vast opportunities are opening up, especially in the field of a new class of two dimensional (2D) materials. Graphene was first isolated and studied experimentally by Novoselov and Geim et al. [7],[8],[9]. This single atomic layer of graphene – a monolayer of carbon atoms packed into a dense honeycomb crystal structure – can also be viewed as an individual atomic plane extracted from graphite or as an unrolled single-wall carbon nanotube. It was believed that such planar graphene could not exist in

the free state due to its energetic instability [10]. However, using micromechanical cleavage, or exfoliation, of highly ordered pyrolytic graphite (HOPG) with adhesive tapes, graphene was successfully isolated onto an oxidized silicon wafer. A field effect transistor (FET) was demonstrated using this new material, and carrier mobility of up to 10,000 $cm^2/V{\cdot}s$ for monolayer and 15,000 $cm^2/V{\cdot}s$ for multilayer graphene was observed at room temperature. The mean free path was in the range of 0.4 μm in spite of the material being in close proximity to the underlying SiO_2 and unprotected from the ambient environment.

1.2.1.1 Properties of Graphene

Graphene can be viewed as a Bravais lattice with a two-atom basis. The two basis atoms are often distinguished as A and B atoms [Figure 1.3(a)]. Carbon atoms in the graphene form have three sp^2 hybridized orbitals which contribute to the three σ bonds to the neighboring in-plane (x-y plane) carbon atoms that are separated by 120 °, forming a hexagonal lattice. The remaining p_z orbital that is orthogonal to the graphene plane contributes to the π bond. While the σ bonds only contribute to fully occupied valence band, the π bond gives rise to bands relating to carrier conduction. The energy-momentum dispersion of monolayer graphene can be calculated using the nearest neighbor tight-binding approach since the π bonds of neighboring carbon atoms only weakly perturb each other.

$$\mathrm{E} = \pm\gamma_0 \sqrt{1 + 4\cos\left(\frac{\sqrt{3}a}{2}k_x\right)\cos\left(\frac{a}{2}k_y\right) + 4cos^2\left(\frac{a}{2}k_y\right)}$$

Here, γ_0 represents the nearest neighbor hopping potential, k_x and k_y are the x and y momentum components, and a is the lattice constant with a value of 2.46 Å. The conduction and valence bands meet at the *K* and *K`* points of the first Brillouin zone and the energy momentum dispersion around this point can be approximated by $E = \pm\hbar v|\mathbf{k}|$, where $\hbar$ is the reduced Plank constant, $v$ is the Fermi velocity, and $\mathbf{k}$ is the momentum with reference to the *K* or *K`* points [Figure 1.3(b)].

Subsequent studies revealed interesting physics that could be probed with this material system. It was experimentally revealed that electrons in graphene acted as a 2D Dirac fermion with zero rest mass and effective transport speed that equals the speed of light [8],[9]. In other words, relativistic quantum phenomena could be studied in a benchtop experiment using monolayer graphene. Its electronic properties were dealt with extensively by Castro Netro et al. [11]. Among other interesting properties [12],[13] is the ability of graphene to carry large currents [14] and transfer heat effectively [15], is impermeable to gases [16], and is one of the strongest materials known [17]. These properties could potentially be used for interconnect applications, heat sinks in ICs, sensors, and nanoelectromechanical systems (NEMS), respectively [13].

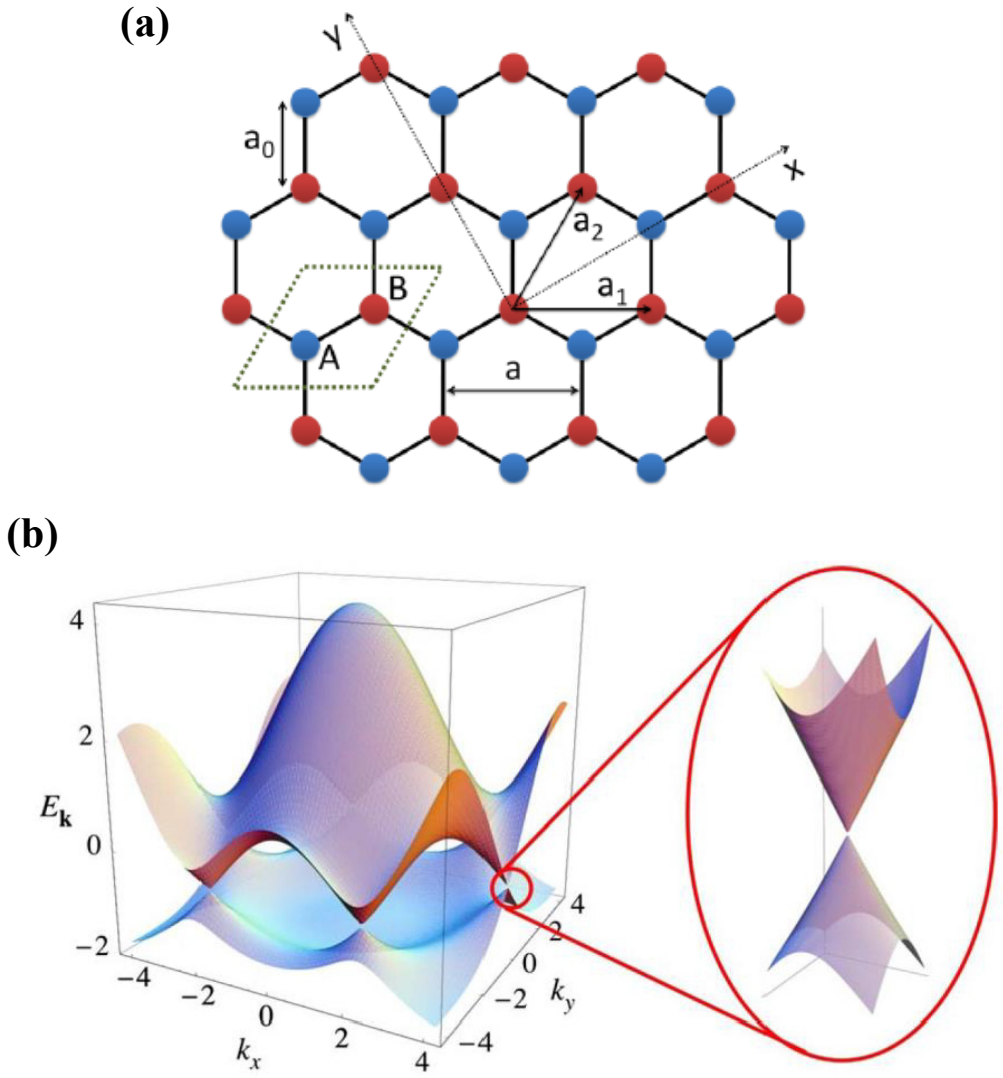

Figure 1.3 (a) Crystal structure of monolayer graphene. It can be viewed as a Bravais lattice with two basis atoms A and B. (b) Band structure of monolayer graphene. The conduction and valence bands meet at the K and K` points of the first Brillouin zone and the bands around those points can be approximated as having a linear dispersion relation. Adapted from [11].

However, the initial excitement with the material was its potential as a channel material for logic type MOSFET application due to its exceptionally high mobility. Nevertheless, a major drawback of the material for this purpose was that it had no band gap in the monolayer form. It can be considered a zero band gap semimetal or a metal with no band overlap. Many attempts have been made to open up a band gap in graphene, for instance, by defining narrow channels – graphene nanoribbons (GNR) [18],[19],[20] – or by applying electric-field to bilayer [21] and some multilayer graphene [22]. GNRs with a band gap of up to 0.5 eV and resulting ON/OFF current ratio of 10^7 have been demonstrated for widths that are sub-10 nm. However, this was at the cost of reduced ON current density [18] possibly due to the scattering at the edges [19]. For bilayer graphene, the magnitude of band gap has been proved to be insufficient, with 0.25 eV gap opening at a vertical electric-field of 3 V/nm [21]. Therefore, for practical logic applications, either the use of a different device mechanism (tunneling transistor) or of a different material which does exhibit a finite and sizable band gap (transition metal dichalcogenides: TMDs) is required. In this work, we focus on the former.

1.2.1.2 Transport Properties of Graphene FETs

When graphene is used as a channel material of an FET, and vertical electric-field is applied onto it through an external gate bias, the transfer characteristic (resistance versus applied voltage) curve shows a local maximum in the resistance – which is often referred to as the charge neutrality point (CNP) or the Dirac point [Figure 1.4]. This is because as the bias is increased from negative to positive, the carrier type switches continuously from holes to electrons with a small transition region where the density of states is low and

effectively only a small density of carriers populate the channel. This is unlike in conventional semiconductors where there is always a sizeable band gap which tends to show a cut off in conduction when the Fermi level lies deep within the band gap. In other words, either side of this maximum resistance (or minimum conductivity) point, the graphene channel is populated by electrons on the right and holes on the left. This kind of behavior is referred to as *ambipolar* current conduction. Typical graphene FETs exhibit this kind of behavior with relative symmetry between the electron branch (right) and the hole branch (left) – although this can be altered by external non-ideal effects which can make the transfer characteristic curve asymmetric.

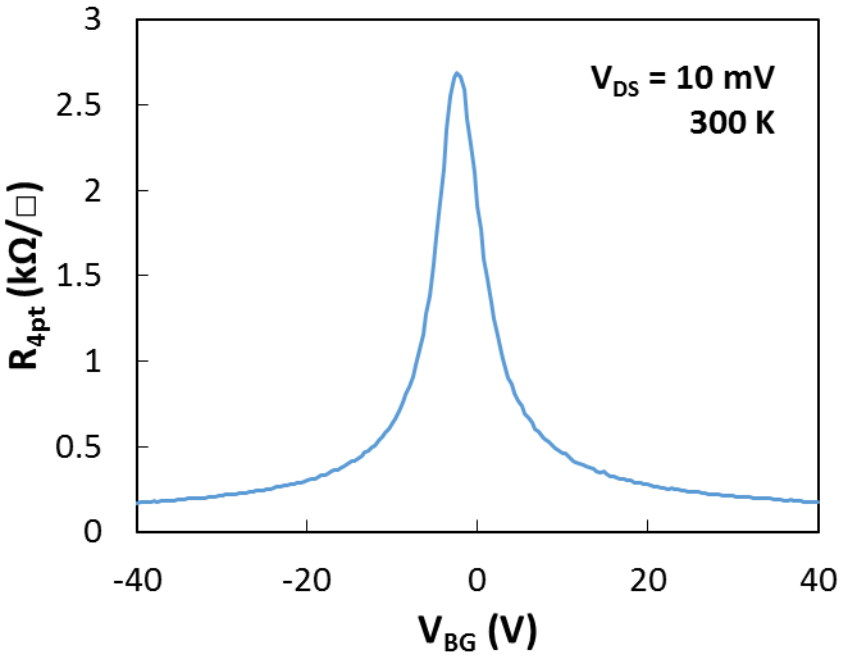

Figure 1.4 Transfer characteristic or resistance (R) versus back gate bias (V_{BG}) curve example of a monolayer graphene FET fabricated on top of 280 nm SiO_2 grown on a heavily As doped Si (100) wafer. The resistance has a maximum (Dirac point or CNP). On either side of the peak, electrons are induced on the right and holes on the left and the resistance decreases.

1.2.1.3 Thickness Determination

Depending on the thickness of graphene, the band structures can change drastically. For instance while monolayer graphene has a linear dispersion relation, bilayer graphene shows a parabolic dispersion. Trilayers can possess both linear and parabolic bands depending on the stacking order of the graphene planes. At around 10 monolayer of graphene the band structure approaches that of bulk graphite [23]. Hence, it is paramount to accurately determine the thickness of a graphene flake once they are exfoliated onto a substrate and before further experimentation. While optical contrast under a microscope can provide a good estimate for the thickness [24], more accurate measurements can be made with Raman spectroscopy [25].

When photons are projected onto a medium, while most photons are reflected or transmitted through elastic scattering, some are inelastically scattered by phonons. This inelastic scattering of photons due to phonons is called Raman scattering. This is measured by the energy difference (wavelength difference or Raman shift) between the scattered and incident photons. In the case of graphene, major signatures in the Raman spectrum are the G and 2D peaks which show up at wavelengths of 1580 cm^{-1} and 2680 cm^{-1}, respectively. Due to the varying vibrational (phonon) modes for different graphene layer thickness, Raman signatures can be used for determining the thickness, in addition to identifying any other changes that affect the electronic properties of the medium such as doping, strain, and defect. For example, monolayer and bilayer graphene share the same G peak signature due to their similarity in the phono dispersion near the Γ point. However, there exists a clear distinction for the 2D peak due to bilayer graphene having an additional sub-band at higher energy and therefore more possible scattering modes. As a result, the 2D peak width for bilayer graphene is wider at around 50 cm^{-1} compared to monolayer graphene at 25 cm^{-}

[1]. This difference in the 2D peak width and also the subtle differences in the shape of the 2D peak can be used to distinguish different graphene layer thickness as is shown in Figure 1.5.

1.2.1.4 Stacking Order

Multilayer graphene can theoretically have a varying degree of stacking order, depending on how one lattice plane is positioned on top of another existing hexagonal lattice graphene plane(s). For instance, bilayer graphene could have AA, AB or AC stacking order, and also other stacking orders where the top plane is positioned in various intermediate positions. However, in reality, this is not the case, because some of these combinations cannot exist due to them being energetically unstable [26]. As a result, only two types of stacking actually occur in natural graphite and consequently in exfoliated graphene, namely, Bernal(ABABAB…)-stacking and rhombohedral(ABCABC…)-stacking [Figure 1.6]. Such difference in the stacking order can result in a drastically different band structure. As a consequence, when analyzing devices with multilayer graphene above three monolayers, it is essential to distinguish between the two different stacking orders prior to device fabrication. It has been experimentally demonstrated that due to the difference in the band structure, one can distinguish between the different stacking order either by optical conductivity measurements [27] or Raman spectroscopy [28]. Especially with the Raman spectrum, there are known to be many features that can be used to distinguish between the two stacking orders, the 2D peak width and shape being one of them. Using this differentiating feature one can draw out a 2D map of which region

of a given flake is Bernal and which is rhombohedral, and use selective portions of the flake for further processing.

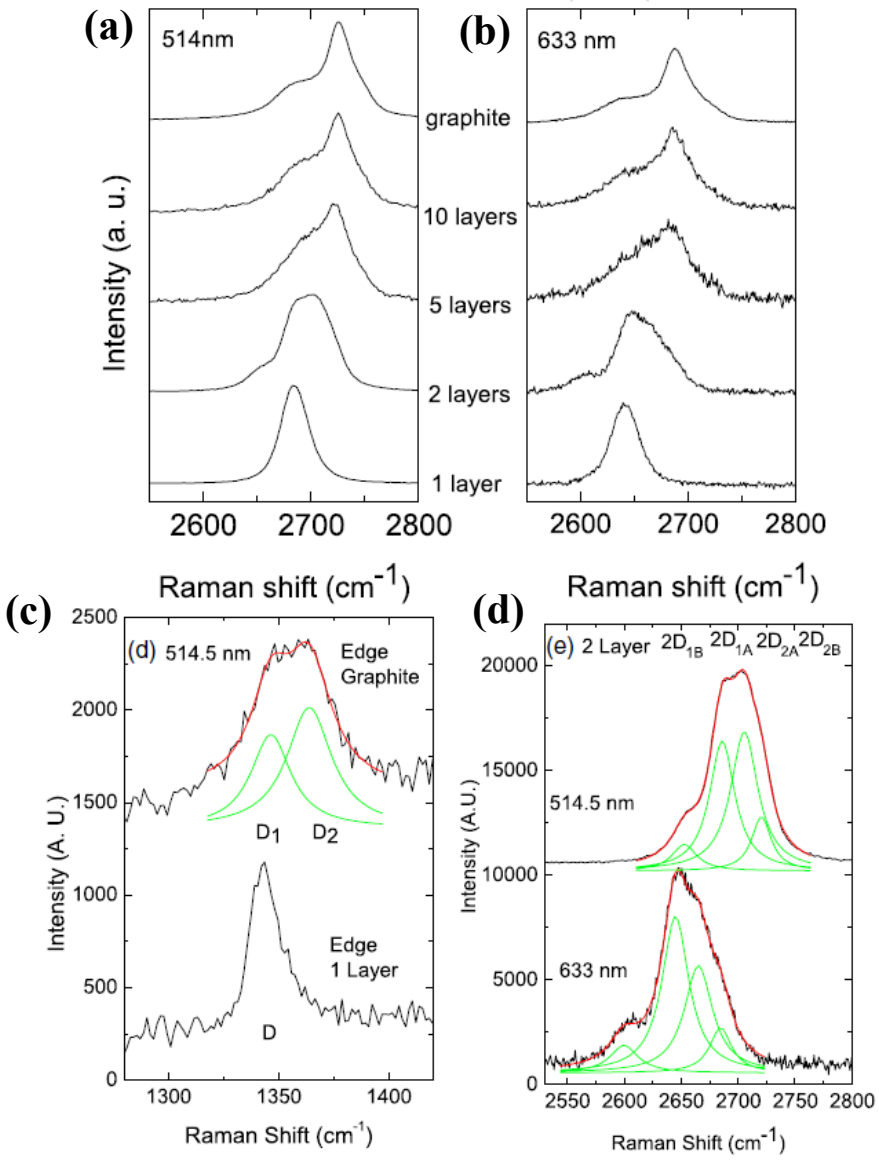

Figure 1.5 Raman spectra for different graphene thickness for (a) 514 nm and (b) 633 nm lasers. (c) D peak components for graphite and monolayer graphene and (d) 2D peak components for bilayer graphene at different laser wavelength. Adapted from [25].

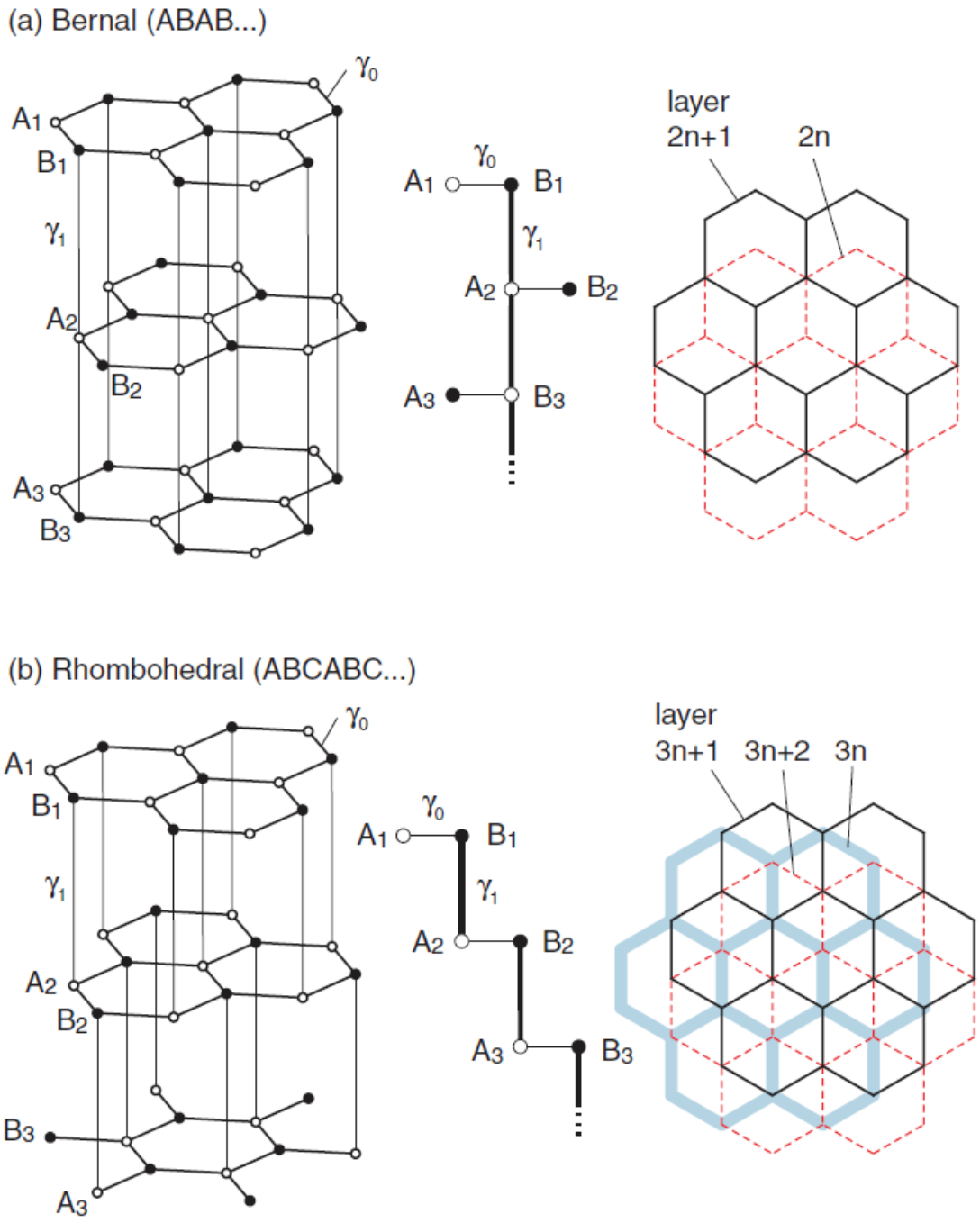

Figure 1.6 Schematic of the lattice structures of (a) ABA (Bernal) stacking and (b) ABC (rhombohedral) stacking. Right panel is the top view. Adapted from [29].

1.2.2 Hexagonal Boron Nitride (hBN)

Although the first demonstrations of graphene FETs on SiO_2 substrates were quite impressive, nevertheless, it was soon discovered that inhomogeneous substrate effects such as charged surface states and impurities [30],[31], substrate surface roughness [32], and surface optical phonons [31] were limiting the mobility and uniformity of the devices. Suspended graphene devices which were free from such effects showed mobilities of up to 200,000 $cm^2/V \cdot s$, more than one order of magnitude greater than on SiO_2 supported substrates [33],[34]. However, since suspended structure are mechanically unstable, there was still a motivation for studying other materials for its use as a stable defect free smooth substrate for graphene FETs. Also, for vertical tunnel FETs, there was a need for a material that could function as a defect free tunnel barrier which at the same time would not adversely affect the characteristics of the graphene layers. Such a material was found to be hexagonal boron nitride (hBN) [35],[36].

1.2.2.1 Properties of hBN

hBN can be viewed as having the same crystalline structure with graphite with boron and nitrogen atoms replacing the inequivalent A and B sublattices in the Bernal structure. It has a large band gap of 5.97 eV [37] and a small lattice mismatch (1.7%) with graphite [38]. Due to the strong in-plane ionic bonding of the planar hexagonal lattice structure, hBN is relatively inert and is free of dangling bonds or surface charge traps. Furthermore, the atomically smooth surface can effectively suppress rippling in graphene, which could further enhance graphene FET performance. In terms of its dielectric properties h-BN has a dielectric constant of 3~4 and reported breakdown voltage of 0.7

V/nm – though in our experiments, we have observed even higher breakdown fields exceeding 1.5 V/nm. These properties are comparable to those of SiO_2 allowing the use of hBN as an alternative gate dielectric [39]. Moreover, the surface optical phonon modes of hBN have energies two times larger than similar modes in SiO_2, suggesting the possibility of an improved high temperature and high electric-field performance of hBN substrate based graphene devices over those using typical SiO_2 substrates.

1.2.2.2 hBN as a Substrate

Due to the atomically smooth surface of hBN (3 times less rough than SiO_2) [35], placing graphene on top of this layer could possibly allow reduced corrugations in the graphene which tends to conform to the underlying substrate [40],[41]. Atomic force microscope (AFM) measurements taken after transferring graphene onto hBN, revealed that the surface roughness of the graphene followed exactly that of the hBN [35]. In terms of graphene FET performance, they were able to demonstrate monolayer graphene mobility of 60,000 $cm^2/V{\cdot}s$ and bilayer graphene mobility of 40,000 $cm^2/V{\cdot}s$ [35]. Moreover, graphene on hBN exhibited a far sharper resistance peak, which meant that the charge carrier inhomogeneity resulting from electron-hole puddles was much reduced compared to graphene on SiO_2 with an upper bound on the disorder induced carrier density fluctuation of 7×10^{10} cm^{-2}. When H_2/Ar annealing was conducted on the samples, the characteristics were further improved while the Dirac point remained essentially the same, possibly due to the graphene conforming more closely to the underlying hBN. For graphene on SiO_2, increased conformance through high temperature thermal annealing would have brought about increased corrugations in the graphene and also heavier doping, but for graphene on

hBN this was not the case. In addition, magneto transport measurements were conducted to show the high quality of graphene on hBN [35].

1.2.2.3 hBN as a Tunnel Barrier

Since hBN is an effective insulator with a large band gap, it has the potential to be used as a tunnel barrier dielectric. When the tunnel FET is integrated in such a way that the electrode layers that sandwich the tunnel barrier is graphene, there are additional advantages in using hBN. Since hBN has a lattice constant that is well matched with graphene, it induces minimal strain. Also, due to the inert and flat surface properties of hBN, its effect on the graphene transport properties can be minimized. In addition, due to its high breakdown voltage, sufficiently high electric fields can be applied across it.

The first demonstrations of hBN being used as a tunnel barrier was presented by Britnell et al. [36]. Graphene and hBN was stacked into a sandwiched structure where the graphene layers would function as the two electrode layers and the hBN as the tunnel barrier. Devices with hBN tunnel barrier thickness of 1 to 30 atomic layers was investigated. It was shown that through tuning of the Fermi level of the top and bottom graphene through the external gate bias – which was possible due to the low density of states (DOS) for monolayer graphene near the Dirac point – the effective barrier height through the hBN tunnel barrier could be modified and hence the level of tunneling current. Also, through investigation of different hBN tunnel barrier thickness, it was suggested that the optimal thickness in terms of the tunneling current characteristics would be around 4-7 atomic layers considering the field applied across the dielectric. For thicker hBN, it was

suggested that they were more prone to dielectric breakdown at the same electric-field possibly due to defects in the crystal.

Based on studies on tunneling through hBN between two metal electrode layers, some have suggested that the defects in the interlayer tunnel barrier hBN could play a role in determining the characteristics of such devices [42],[43]. Although, for thin hBN, the tunneling current is exponentially dependent on the hBN thickness, for thick hBN, they have observed Coulomb blockade like features such as suppressed tunneling around zero bias and step-like features in the current-voltage characteristics at larger biases. The interval of the steps were shown to correspond to nm-size defects in the hBN crystal. Nevertheless, such features were shown to disappear when the devices were annealed, suggesting that even if the hBN crystals are non-ideal and do have defects, such could be mitigated by using high temperature annealing.

1.3 TUNNELING DEVICES

The first device utilizing quantum tunneling as the main current conduction mechanism was introduced by Esaki [44]. A heavily-doped Germanium p-n junction was used where electrons in the conduction band of the n-side of the junction would travel into the valence band of the p-side through inter-band tunneling. A distinctive feature was observed in the current-voltage characteristic of this device, namely, negative differential resistance (NDR), where an increase in the applied voltage between two electrodes results in a decrease in the current between those two same electrodes. Such characteristics could be used for simpler implementations of bistable circuits, high frequency oscillators, frequency converters, and amplifiers.

Another class of tunneling device that exhibit this type of NDR feature is the resonant tunneling diode (RTD) which can be classified as a unipolar *intra-band* RTD whereas the device introduced by Esaki can be classified as a bipolar *inter-band* tunneling device. This was first demonstrated in compound semiconductor based two dimensional electron gas (2DEG) systems with double AlGaAs barriers sandwiching a thin GaAs layer grown through molecular beam epitaxy (MBE) [45]. Due to confinement between two tunnel barriers in the x-direction (current flow direction), the GaAs layer would have discrete energy levels – which is actually the bottom state of a 2DEG with zero transverse (yz-plane or plane perpendicular to current flow) momentum. When an external gate bias is applied to the GaAs layer, once the Fermi level of the emitter is aligned to the resonant level of the GaAs, current will start to flow through resonant tunneling of electrons. As the bias is increased further so that the resonant energy level drops below the conduction band of the emitter, tunneling is no longer permitted and only current flowing through scattering channels or thermionic emission remain, which constitutes the background current. This will also result in NDR characteristics in the current-voltage relationship [Figure 1.7].

Another implementation is the 2D-2D tunneling device where tunneling occurs between two overlapping 2DEGs. Using two GaAs 2DEG layers separated and confined by AlGaAs barriers, Eisenstein et al. were the first to demonstrate such a device [46]. In this configuration, the AlGaAs barriers on either side of the GaAs layers provide the quantum confinement in the x-direction (current flow direction), and the barrier layer in-between the two GaAs layers acts as the tunnel barrier. Carriers would tunnel directly from one 2DEG to another through resonant tunneling when the sub-band edges of the two 2DEG are in energetic alignment with each other.

A structural and behavioral combination of the inter-band tunnel diode and the intra-band RTD (or 2D-2D tunneling FET) is the resonant inter-band tunneling diode

(RITD) [47],[48]. Here, the electrons in the conduction sub-band of one 2DEG tunnels into the valence sub-band of the other 2DEG. Such devices have shown extremely high peak-to-valley current ratio (PVCR) – a measure of the device performance of NDR devices – of over 140 [49],[50]. In any case, in these tunneling devices, the electrons would travel through the structure in accordance with energy conservation and transverse momentum conservation – where transverse means perpendicular to the current flow and longitudinal refers to direction parallel to the current.

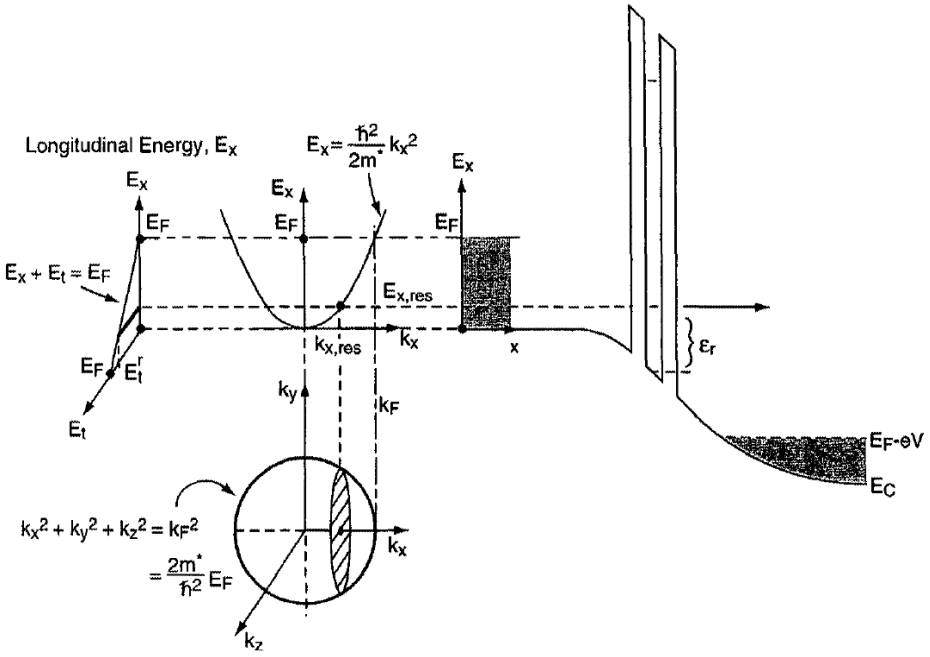

Figure 1.7 Schematic illustration of how an RTD operates in terms of the conduction band profile. Electrons tunnel from left to right. $E_{x,res}$ is the total energy of the resonant state with zero transverse momentum. The parabola to the left is the energy dispersion of the left emitter in the current flow direction. The sphere represents the 3D momentum states in the emitter, and the shaded circle depicts the states that contribute to resonant tunneling. Adapted from [51].

1.4 Heterostructures Based on 2D Materials

Although the individual 2D materials themselves showed interesting new physics and potential applications, stacking any number of these 2D materials in the vertical direction with varying combinations was suggested to further expand the possibilities, analogous to building with Lego blocks [52]. Such structures were made possible by various techniques that were developed for transferring 2D flakes one on top of each other. In these so called van der Waals heterostructures, the in-plane covalent bonds provides stability of the 2D crystal while the van der Waals force in the vertical direction between layers is relatively weak but still sufficient enough to keep the stack together. Van der Waals heterostructures have the potential to be used in a variety of applications. Of particular interest in terms of semiconductor devices is the tunneling based FET. Since 2D materials have atomically flat surfaces with very abrupt hetero-junction interfaces, they have the potential to be used in implementing tunneling FETs that were in the past implemented with conventional compound semiconductor materials grown with MBE. The first demonstrations of such 2D-2D tunneling devices using monolayer graphene and hBN were presented by Britnell et al. [36], and many studies using a variety of 2D materials have followed.

1.5 Overview

The outline for this dissertation is as follows. First, in Chapter 2, the results for a double bilayer graphene interlayer tunnel field-effect transistor (ITFET) (or 2D-2D tunneling transistor) with hBN tunnel barrier is presented. Details of the fabrication process, measurement conditions, and measurement results are followed by a detailed

electrostatic analysis which provides evidence that the mechanism behind the various features of the ITFET is indeed resonant tunneling. Low temperature measurement and in-plane magnetic field measurement results are also presented as evidence for resonant tunneling behavior. Then, demonstration of a 1-transistor memory element that utilizes the characteristic NDR of the ITFET is given. In Chapter 3, further experiments with double multilayer graphene ITFET is presented. The ITFET characteristic dependence on the graphene electrode layer thickness is analyzed and a list of requirements for obtaining improved performance is suggested. In Chapter 4, conclusions to this work and suggestions on future research projects are given. In the first appendix, the influence of electron beam lithography (EBL) process on graphene FET characteristics is discussed. It is shown that the exposure current used during EBL can have a major influence on the device mobility, residual carrier density and the Dirac point. In the second appendix, attempts made on double graphene heterostructures with air-gaps are presented.

CHAPTER 2: Double Bilayer Graphene Hexagonal Boron Nitride Heterostructure Operating as an Interlayer Tunnel FET (ITFET)

2.1 INTRODUCTION

Layered heterostructures of two dimensional (2D) materials have become a vast field of research with reports of interesting physical phenomena for a wide variety of potential applications [52]. One such application is the vertical interlayer tunneling device, such as has been demonstrated for a stacked monolayer graphene - hexagonal boron nitride (hBN) - monolayer graphene heterostructure [36]. Application of a gate voltage enables one to modulate the interplay among the density of states (DOS) and the electrostatic potentials in the two graphene layers, and thereby control the current flow between layers. However, the tunneling in [36] was believed to be non-resonant. If the band structures can be aligned, then resulting resonant interlayer tunneling could be the basis for interlayer tunneling FETs (ITFETs) with negative differential resistance (NDR) [53],[54],[55],[56]. Recently, it has been reported that NDR has been achieved through physical rotational alignment of two graphene layers that, in turn, aligns the Dirac cones at the corners (K-points) of the Brillouin zone [55]. Similarly, for bilayer graphene (BLG), rotational alignment of the parabolic band structures has been shown to produce substantial NDR [56]. Recent advances in fabrication of so-called van der Waals heterostructures of layered 2D materials have made it possible to fabricate devices with clean hetero-interfaces [57]. Utilizing such techniques, we have fabricated a stacked double BLG heterostructure with hBN used as the bottom dielectric, interlayer tunnel barrier dielectric, and the top capping layer. We report here the results for this structure operating as a vertical ITFET device. We show multiple NDR peaks, consistent with the more complex band structure of BLG as

compared to monolayer graphene. Through electrostatic analysis, temperature-dependent and in-plane magneto-transport measurement, it is confirmed that the NDR is a result of resonant tunneling due to band alignment between the two graphene layers. We also demonstrate that a one transistor static random access memory (SRAM) or latch can be realized using this NDR characteristic.

2.2 FABRICATION PROCESS

2.2.1 Graphene and hBN Flake Preparation

A detailed description of the fabrication process flow is as follows. Heavily As-doped Si wafers with (100) orientation were oxidized in a wet oxidation furnace in order to grow a 280-300 nm thick SiO_2 film on top of the Si substrate. This thickness is known to be optimal for distinguishing 2D materials that are exfoliated on top of it [24]. First, natural graphite (supplied by NGS Naturgraphit GmbH) and hBN crystals (supplied by Taniguchi and Watanabe [37]) are peeled onto regular scotch tape. Then the exfoliated crystals were again peeled onto an adhesive Gel-Film® placed on a slide glass. Only graphite crystals that had very shiny surfaces with large grain boundaries were used for graphene exfoliation since these were the ones that tended to yield larger high quality flakes [Figure 2.1]. If the crystals did not show such pristine condition and had a foggy or matte surface, then the crystals were peeled extensively with scotch tape until the highly reflective surface was revealed. Prior to exfoliation, the Si substrates were baked on a hot plate at 180 °C for 5~10 minutes in order to remove adsorbents and water molecules which inhibit graphene or hBN from adhering onto the substrate [58]. Then, the Si substrates were

placed face-down onto the adhesive Gel-Film® and pressure was applied to the substrates onto the Gel-Film® using tweezers. BLG flakes with straight edges were searched for under an optical microscope. We avoid the use of plasma treatment of the substrate or other techniques frequently used for obtaining large area exfoliated graphene flakes [59],[60]. This is because such techniques are often the result of enhanced graphene to substrate bonding, which we have found, tends to inhibit the pickup of graphene later on during the transfer process. The BLG was confirmed through a combination of optical contrast and Raman spectroscopy [25],[61]. The Raman spectrum of graphene shows two distinctive peaks at 1580 cm^{-1} (G peak) and 2680 cm^{-1} (2D peak), and BLG can be distinguished from monolayer and multilayer graphene by extracting the 2D peak width, which is roughly 53 cm^{-1} compared to 25 cm^{-1} for monolayer graphene and higher values for multilayer graphene. In terms of the hBN, for the top encapsulating layer and bottom substrate, large uniform and relatively thick flakes (10~20 nm) were searched for. For the interlayer tunnel barrier, thin hBN of 3 to 6 atomic layers was required for reliable measurement of NDR characteristics at room temperature [54]. The hBN layer thickness was first determined through a combination of optical contrast, Raman spectroscopy [62] and atomic force microscopy (AFM) [63]. The Raman spectrum of hBN shows a distinctive peak at around 1360 cm^{-1}. Since the tunneling current level through an hBN tunnel barrier is quite well established [36],[54],[56], the thickness was further confirmed through tunneling current level post device fabrication. All graphene and hBN flakes were annealed at 350 °C for 8 hours in a 10^{-7} Torr vacuum environment to ensure that the flakes were clean of hydrocarbon residues before transfer [64],[65]. Hydrocarbon residues are knows to inhibit pickup of the graphene flakes during transfer [66].

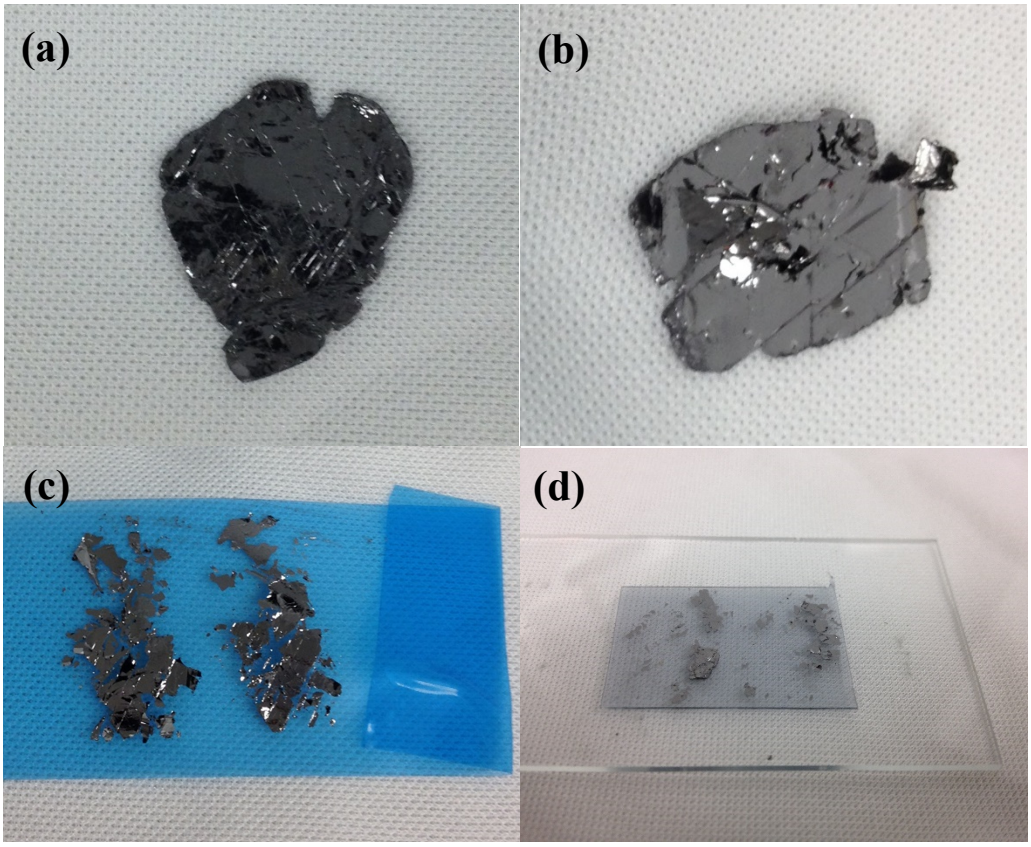

Figure 2.1 (a,b) Examples of the graphite crystal used for exfoliation. Crystals with large grains and shiny surfaces tend to yield larger high quality exfoliated graphene flakes. (c) The crystals are first peeled onto scotch tape with which the crystals are peeled onto the (d) Gel-Film® placed on a slide glass.

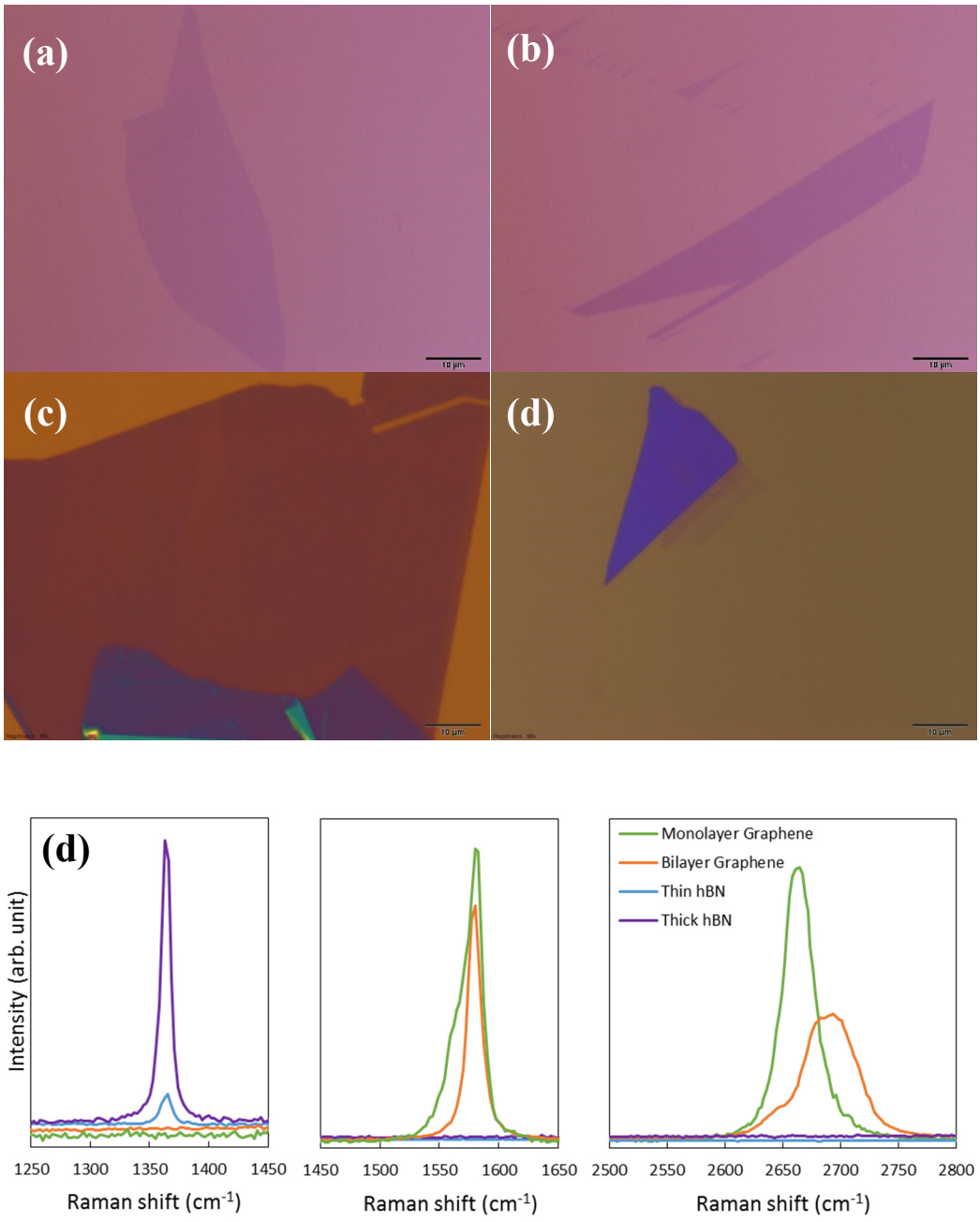

Figure 2.2 Examples of exfoliated (a) monolayer graphene (MLG), (b) bilayer graphene (BLG), (c) thick (~10 nm) hBN used for the top capturing layer and bottom substrate layer and (d) thin (~1 nm) hBN used for the interlayer tunnel barrier. (e) Raman spectrum for monolayer and bilayer graphene, and also thick and thin hBN.

2.2.2 Flake Transfer

Previously, 2D flake (especially graphene) transfer was achieved by a wet chemical (water) mediated wet-transfer process mostly developed for transferring chemical vapor deposition (CVD) grown graphene sheets on Ni surfaces [67] and Cu foils [68],[69] onto different substrates. The method involved spin coating the graphene with poly-methyl-methacrylate (PMMA), removing the substrate SiO_2 through wet etching in a NaOH solution to capture the flake onto the PMMA film, and then placing the film onto a new substrate and subsequently dissolving the PMMA layer in acetone [68]. With the use of a micro manipulator, improvements could be made to the accuracy of the transfer process. However, it was quickly noticed that graphene coming into contact with water was detrimental to the quality of the flake and ultimately the device performance. This is why the dry transfer process method became more widely used [70],[71],[72],[73]. However, if one was to make a stack with multiple 2D materials, both wet and dry transfer methods involved a layer-by-layer transfer where each individual layer had to be transferred onto an existing stack one layer at a time, and the risk of failure for each step was quite high.

Wang et al. [57] and others [74],[75] introduced a new method of transfer which utilized the van der Waals force between 2D materials. This method utilized the difference in the van der Waals force that occurs between distinct materials. For instance, the bonding force between hBN and SiO_2 is smaller than the force between hBN and the polymer stamp at a certain temperature. So when the stamp makes contact to the hBN and subsequently retrieved, the hBN flake gets *picked-up* by the stamp. With the use of a polymer stamp and by carefully controlling the temperature at which the contact to the material is made, one could sequentially *pick up* various 2D materials one at a time and stack them together to make heterostructures with relative ease. After the flakes are all captured, one can release

the stack onto a fresh substrate for further processing by simply increasing the substrate temperature. At higher temperatures, the polymer loses some of its adhesiveness and the bonding between the stack and substrate SiO_2 increases beyond that of the bond between the stack and polymer, and as a result the stack gets released onto the substrate. Alternatively, one could at this step, also intentionally delaminate the PPC film from the PDMS stamp by increasing the substrate temperature. Later on, the PPC film can be dissolved in chloroform or acetone.

One thing that had to be considered with this method was that due to the very weak bonding between the polymer and graphene, graphene flakes could not be picked up directly by the polymer stamp. Only when hBN is present can graphene be picked up. This requires a stable thick top hBN to start off with for making double graphene layer heterostructures. As a result, one ends up with a situation where the graphene layers are completely covered by the top hBN and it becomes impossible to make conventional 2D contacts to the graphene layers. Fortunately, it was shown that with optimized lithography, active plasma etching, and metal combination, one-dimensional (1D) contacts to the side edge of the graphene layer was not only sufficient but was shown to be better than that of the 2D contacts in terms of contact resistance [57].

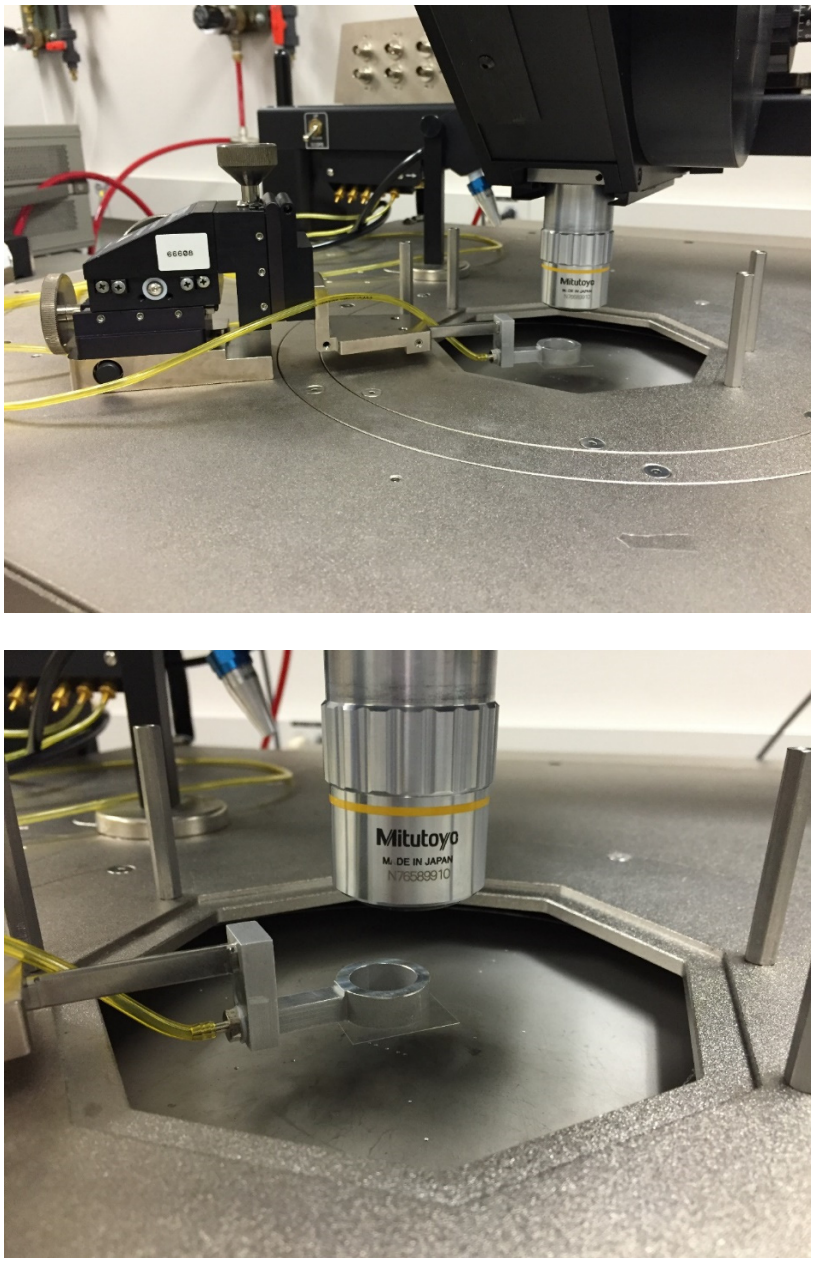

Figure 2.3 The stamp-and-stack transfer setup. A Cascade probe station equipped with a heated chuck is used. The probe arm was retrofitted so that the slide glass holding the PDMS/PPC stamp could be attached to it by pulling vacuum on the O-shaped ring. A 10X objective lens is used. The digital zoom capability of the microscope allows us to easily distinguish features down to a few μm and hence the flakes can be aligned to within these dimensions.

For the transfer, we made use of a Cascade probe station equipped with a chuck capable of heating the substrate up to 200 °C and also capable of pulling vacuum on the sample for stable positioning. The probe arm was modified so that we could make use of the micromanipulators and at the same time attach a slide glass holding the polymer stamp at the end of the probe arm by pulling a vacuum through an O-shaped ring. The setup is shown in Figure 2.3. We utilized the microscope embedded in the probe station which had a 10X objective. Through the digital zoom capability of the equipment, we were able to distinguish features down to a few μm and as a result obtain transfer alignment on that scale. During the transfer, the chuck was used for macro-manipulation (i.e., locating flakes on a sample) and the probe arms were used for fine adjustments to the alignment.

The hBN and graphene flakes in our experiment were picked up sequentially from the top to bottom using this polymer stamp transfer method with the transfer setup shown in Figure 2.3. First step of the process is to prepare the polymer stamp. A sliver of polydimethylsiloxane (PDMS) is placed onto a thin slide glass. The adhesive PDMS allows strong bonding between PDMS and glass so that there is no need for additional adhesive. Then, a 15 % solution of polypropylene carbonate (PPC) in anisole is spin coated onto the PDMS at 4000 rpm for 60 s. The stamp is then baked at 140 °C for 2 minutes on a hot plate in order to remove the remaining solvent. The extent of baking at this point, effectively controls how well the PPC sticks to the PDMS and is an important factor for determining the pickup and release temperature later on in the process flow. With a lower bake temperature and shorter bake duration, the bond between the PPC layer and PDMS is decreased. This can potentially lead to undesirable situations during the transfer process, where the PPC film gets unintentionally delaminated from the PDMS stamp and gets adhered to the substrate.

Using this stamp, a large and thick hBN flake is picked up onto the PPC coated stamp at 45 °C. A suitable temperature for the pickup must be found. In order to avoid the delamination of PPC from PDMS, the temperature must be low, but at the same time the temperature must be high enough so that the bond between the hBN layer and PPC is strong enough for it to be picked up. For our experiments, 45 °C was determined as the optimum temperature. The hBN flake must be thick enough to be stable during the whole transfer process (thin flakes tend to curl up), but not too thick so that the layers below the hBN become invisible. Then, with the hBN flake the top graphene layer is picked up, also at 45 °C. The sample holding the interlayer hBN is then placed onto the chuck and the flake is picked up using the hBN-graphene stack at the same temperature. It should be noted here that the hBN was not intentionally oriented to crystallographically align with the top or bottom graphene. Similarly, the bottom graphene is picked up. During this pickup process, the bottom graphene flake was rotationally aligned to the top graphene in such a way that the longest straight edges of the two graphene flakes formed roughly a 60 ° angle [56]. This was to achieve rotational alignment between the two K-points of the top and bottom graphene layers in momentum space. Vacuum annealing (350 °C for 8 hours at 10^{-7} Torr vacuum) the stack after transfer was also conducted. This was to again clean the top surface of the stack which was exposed to the polymer stamp, remove or relocate the air bubbles [Figure 2.4] [76] which can potentially modify the properties of the 2D materials [77],[78], and also help re-orient the graphene layers into alignment [79].

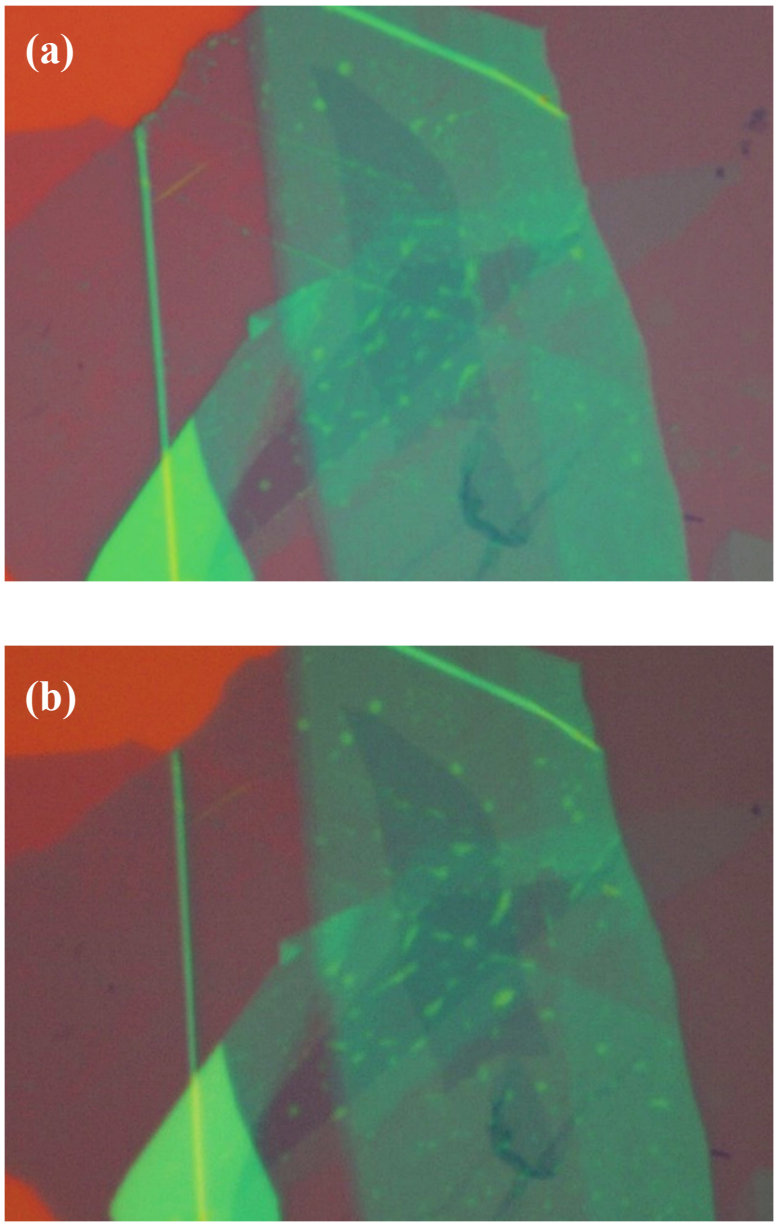

Figure 2.4 Optical microscope image of the BLG and hBN heterostructure (a) after transfer and (b) after vacuum annealing at 350 °C for 8 hours. Vacuum annealing after transfer helps reduce the air bubbles or at least move them to the edges of the hBN or graphene flakes so that the overlap region is relatively clear of them.

2.2.3 Device Fabrication

The heterostructure stack is then exposed to O_2 plasma in a reactive ion etching (RIE) chamber (Plasma-Therm 790 Series) for 5 seconds at a power of 75 W, gas flow rate of 15 sccm, at a chamber pressure of 200 mTorr. This was to ensure that the surface was hydrophilic [80] because sometimes due to hydrophobic residues left on the substrate during the transfer process the resist would not get spin-coated. A resist layer of PMMA (950K 4 % dissolved in anisole, supplied by MicroChem corp.) is spin-coated at a rate of 4000 rpm for 40 seconds to obtain a 470 nm film. The sample is subsequently baked at 140 °C for 2 minutes to remove any residual solvent. The recommended bake temperature for solvent removal is 180 °C, but a lower temperature was used in order to reduce the level of thermal expansion induced stress on the stack. Then a layer of hydrogen silsesquioxane (HSQ) is spin coated at 3000 rpm for 60 s on top of the PMMA and the sample is again baked at 140 °C for 2 minutes in order to remove the solvents. A negative resist (HSQ) is used in order to obtain an etch profile that has a positive slope which more effectively exposes the sides edges of the graphene flake after plasma etching [60]. Electron beam lithography (EBL) is performed using a Zeiss Neon 40 scanning electron microscope (SEM) equipped with a Raith Elphy Quantum Pattern Generator system with an exposure current of roughly 30 pA, and the energy, dose, and step size fixed at 20 keV, 100 $\mu C/cm^2$ and 4 nm, respectively. The resist is then developed in a AZ® 726 MIF (2.38 % Tetramethylammonium hydroxide (TMAH) in H_2O) for 5 minutes with slight agitation for 1 mintue at the start and end. Right away, the sample is rinsed in flowing deionized water (DIW) for 2 minutes. The sample is then exposed to O_2 plasma in an RIE chamber for 2 minutes for etching away the PMMA along the HSQ pattern down to the substrate SiO_2. Then, the sample is processed with CHF_3 + O_2 plasma for 90 seconds at a power of 100

W, gas flow rate of 15 sccm, at a chamber pressure of 50 mTorr to pattern the graphene and hBN stack into a Hall bar geometry for both the top and BLG. Additional O_2 plasma processing is conducted to remove any residue that might be hanging over the edge of th heterostructure stack. The sample is then submersed in acetone for 10 minutes in order to remove the PMMA layer and HSQ layer on top of it. An additional vacuum anneal process (350 °C for 8 hours at 10^{-7} Torr vacuum) was conducted in order to help remove dopants and air bubbles at the graphene and hBN interface that formed during the transfer process and ensuing active patterning steps. Subsequently, another layer of PMMA is spin coated using the same conditions given above, and EBL is performed to pattern the metal contacts. Metal contacts to the top and bottom BLGs were simultaneously patterned, using 8 nm of chromium and 28 nm of gold deposited by thermal evaporation [Figure 2.5]. Because a thick hBN layer was needed to pick up the graphene flake, only the edges of the graphene flake would be exposed after the active region is patterned through EBL and plasma etching. Hence, when metal is evaporated onto this structure, contact between the graphene and metal is only made at the edges. However, it has been shown that these types of 1D contacts are known to be stable even down to low temperatures when suitable combination of metal material is used, in which case they show contact resistance that is even lower than their 2D counterparts [57].

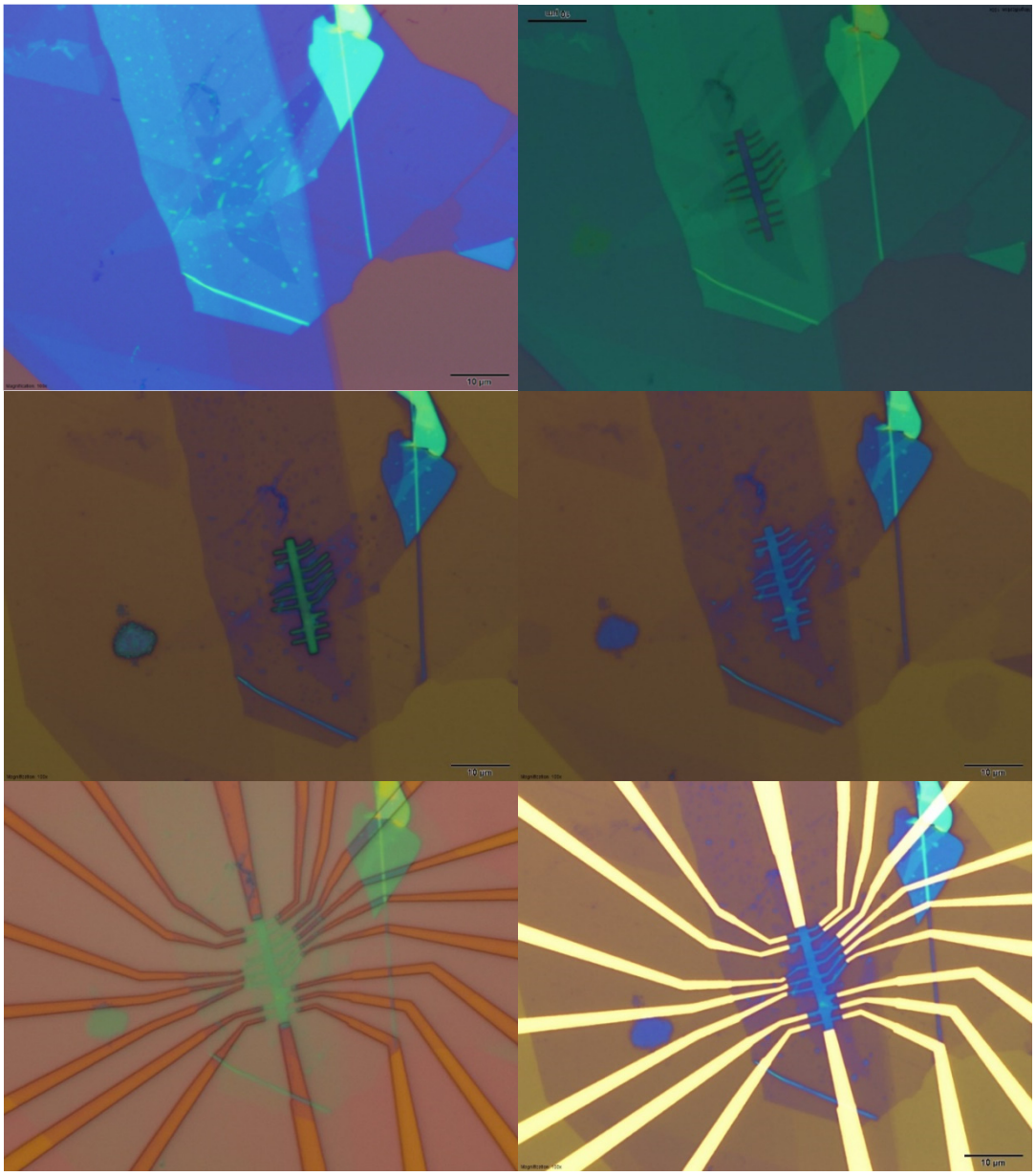

Figure 2.5 Optical microscope images of the device after key process steps. From top left to bottom right, the images show the device after vacuum annealing, EBL active patterning, CHF_3+O_2 plasm etch, PMMA & HSQ strip in acetone, metal contact EBL, and finally, metal deposition and lift-off.

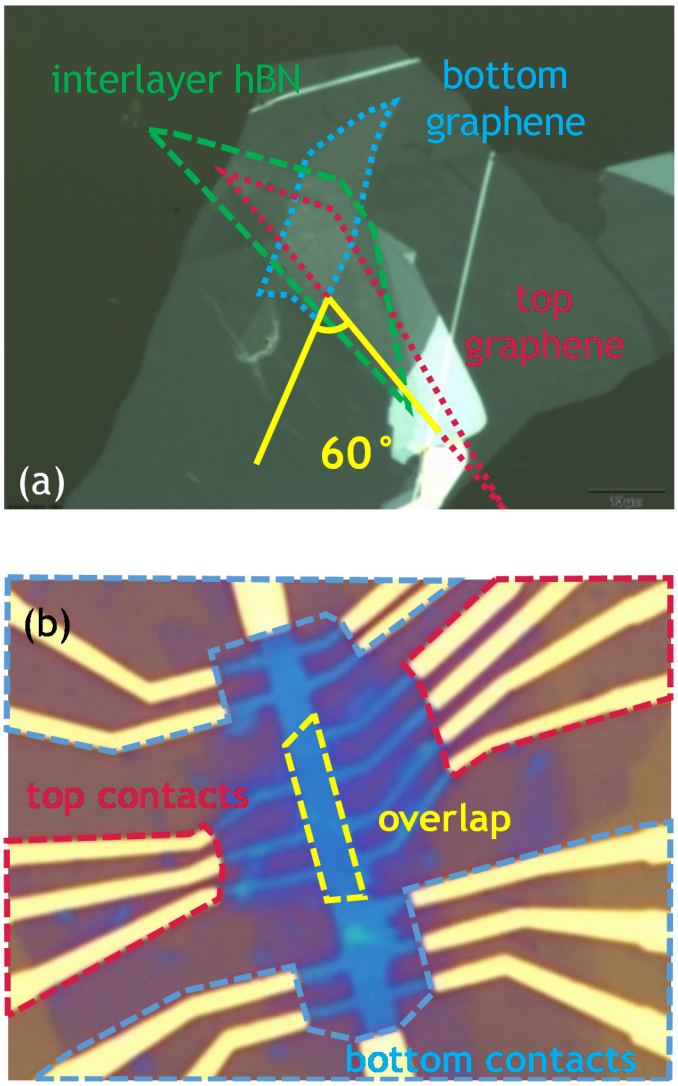

Figure 2.6 (a) Optical microscope image of the BLG and hBN heterostructure stack during transfer. The flakes are transferred in such a way that multiple independent contacts to the top and bottom graphene layers can be made, and that the straight edges of the two graphene layers make a 60 ° angle with each other. (b) Optical microscope image of the device after active patterning and metal contact process showing the actual overlap region where current conduction occurs.

2.2.4 Measurement

Previous studies conducted on the ITFET only involved I-V measurements across the tunnel barrier, and as a results a more detailed analysis of the characteristics was not possible [54],[55]. In our study, multiple contacts to both the top and bottom layers were made in order to independently probe the intralayer characteristics of the BLG [Figure 2.6]. Individual characterization of the top and bottom bilayer graphene allows us to conduct electrostatic analysis on the measurement results, and hence determine the electrostatic potential and carrier density at a given external bias point. A Lakeshore probe station operating under a vacuum environment in conjunction with a B1500A parameter analyzer was used for electrical measurements. Before measurements, the contact resistance was checked [Figure 2.7]. To characterize the device, the interlayer current (I_{IL}) was measured as a function of the interlayer bias (V_{TL}) applied to the top layer while the bottom layer was grounded. The n^+ Si substrate was used as the back gate. A schematic diagram of the device structure and biasing scheme is given in the inset of Figure 2.8. The individual layer resistances were also measured as a function of V_{TL} and back-gate bias (V_{BG}) [Figure 2.9].

2.3 DEVICE RESULTS

The main result of our study is shown in Figure 2.8. At $V_{BG} = 40$ V, two clear NDR peaks can be observed at $V_{TL} \approx 50$ mV and $V_{TL} \approx 600$ mV; another relatively less conspicuous hump at $V_{TL} \approx -500$ mV. These peaks are observed at higher V_{TL}, in addition to the ones found in a previous report [56]. It can be noted that the position and intensity of the peaks vary with the applied V_{BG}, although the overall underlying background curve remains unchanged. As V_{BG} is decreased, the current level for both peaks on the positive

V_{TL} side decreases and diminishes at certain biases. Further, when V_{BG} is turned negative and the bias is increased negatively, a peak appears at negative V_{TL} and the height of this peak starts to increase with V_{BG}. This trend is consistent with results shown in [54],[55],[56] and similar arguments in terms of the band alignments of graphene can be used here also to understand the origin of the NDR peaks.

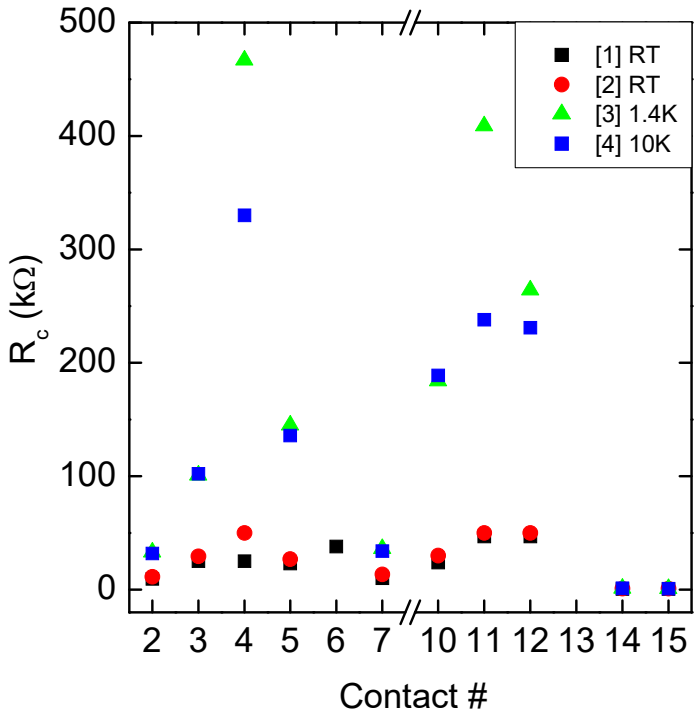

Figure 2.7 Contact resistance for the device at room temperature down to 1.4 K. Although some contacts showed a dramatic increase at low temperatures (10 K) there were sufficient number of functioning contacts that could be used for layer characterization and interlayer I-V measurements.

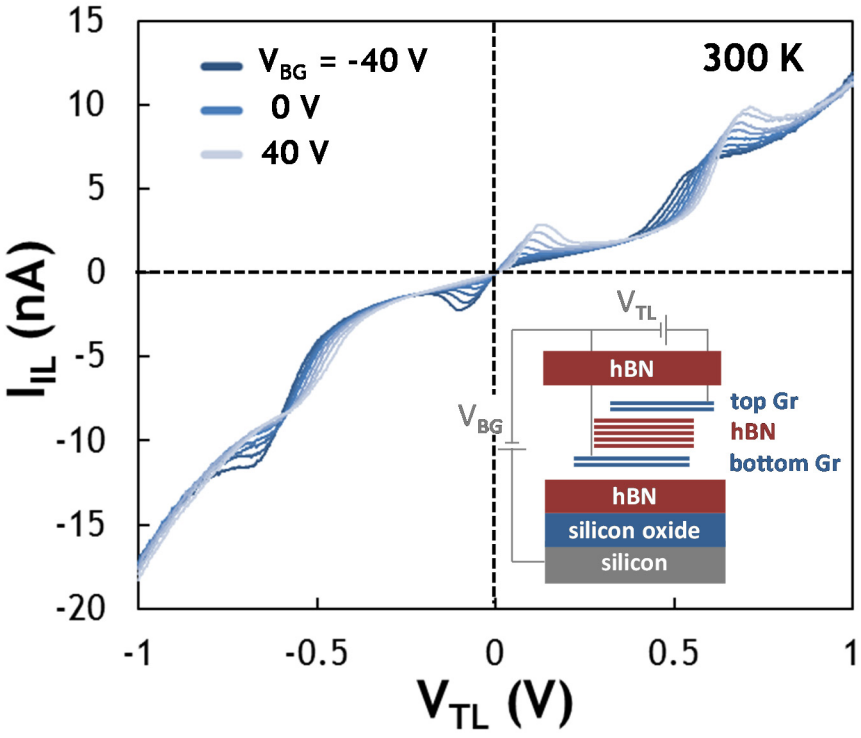

Figure 2.8 Interlayer current-voltage characteristics showing multiple NDR peaks. The bottom-right inset shows the schematic and biasing scheme of the device; the n^+ Si substrate is used as the back gate while the top layer is biased and the bottom layer is at ground.

2.3.1 Electrostatic Analysis

In order to show a clearer picture of the resonance conditions, it is instructive to examine the I_{IL}-V_{TL} characteristics as a function of the electrostatic potential difference between the two bilayers (V_{ES}). Because each layer has a finite chemical potential (Fermi energy), the applied interlayer bias can be written as $V_{TL} = V_{ES} + \mu_T - \mu_B$, where μ_T (μ_B) is the top (bottom) layer chemical potential measured with respect to the charge neutrality point. The layer densities and chemical potentials can be calculated as a function of V_{BG} and V_{TL} using the electrostatic model of [56].

Using the following set of equations, given that we have an accurate enough value for the back gate capacitance (C_{BG}) and interlayer capacitance (C_{INT}), a relationship between the external biases and the electrostatic potential of the individual layers and carrier concentration could be established.

$$e\left(V_{BG} - V_{BG,DNP}\right) = \frac{e^2(n_B + n_T)}{C_{BG}} + \mu_B \qquad (Equation\ 2.1)$$

$$e\left(V_{TL} - V_{TL,DNP}\right) = -\frac{e^2 n_T}{C_{INT}} + \mu_B - \mu_T \qquad (Equation\ 2.2)$$

Here, V_{BG} and V_{TL} are the back gate and top layer external biases, and $V_{BG,DNP}$ and $V_{TL,DNP}$ are V_{BG} and V_{TL} when both the top and bottom graphene layers are at the CNP, respectively. The double neutrality point (DNP) is defined as the bias point where the charge neutrality line (CNL) of the two BLGs coincide [Figure 2.9(a)]. n_B and n_T are the charge carrier density, and μ_B and μ_T are the electrostatic potential of the bottom and top layer, respectively.

In order to obtain a more accurate C_{BG} value, a vertical magnetic field of 13 T was applied to the sample. Due to the Landau level splitting of the bottom BLG, the resistivity

contour plot of the top BLG shows a staircase behavior [Figure 2.10(a)]. The carrier density of the bottom BLG will be $n_B = \nu eB / h$, where h is the Planck constant. Combining this with equations 2.1 and 2.2 yields,

$$C_{BG} = \frac{e^2 B}{h}\left(\frac{\Delta(V_{BG} - V_{TL})}{\Delta\nu}\right)^{-1} \qquad (Equation\ 2.3)$$

From this relation, one can extract the back gate capacitance by simply reading the slope from a plot of $\Delta(V_{BG} - V_{TL})$ - the change in $V_{BG} - V_{TL}$ corresponding to a bottom layer filling factor change $\Delta\nu$ along the top layer charge neutrality line (CNL) against change in filling factor $\Delta\nu$. An example of this extraction method is shown in Figure 2.10, where for this specific device $C_{BG} = 12.87$ nF/cm^2.

For the interlayer capacitance C_{INT}, one can consider that at the CNL of the bottom layer we can assume $n_B = \mu_B = 0$ and from equations 2.1 and 2.2 we obtain the following expression.

$$C_{INT} = -\frac{eC_{BG}(V_{BG} - V_{BG-DNP})}{e(V_{TL} - V_{TL-DNP}) + \mu_T\left(\frac{C_{BG}(V_{BG} - V_{BG-DNP})}{e}\right)} \qquad (Equation\ 2.4)$$

When the electrostatic potential drop across the hBN dielectric is zero we have

$$eV_{TL} + \mu_T(n_T) - \mu_B(n_B) = 0 \qquad (Equation\ 2.5)$$

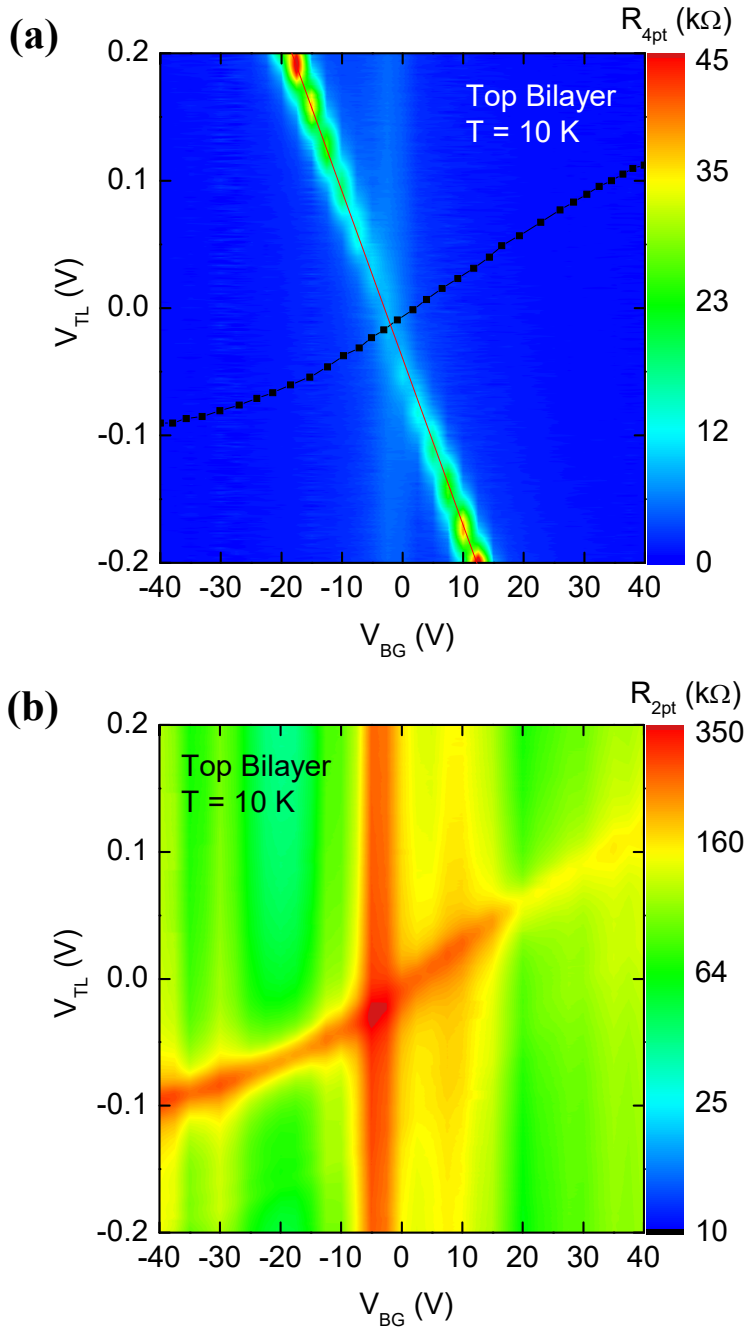

Figure 2.9 Contour plot measured at 10 K for (a) bottom BLG and (b) top BLG. The black dotted line shown in (a) is the charge neutrality line (CNL) of the top bilayer. The intersection between the CNL of the bottom bilayer and CNL of the top bilayer is the double neutrality point (DNP). For this particular device DNP occurs at V_{BG} = -2.185 V and V_{TL} = -0.013 V.

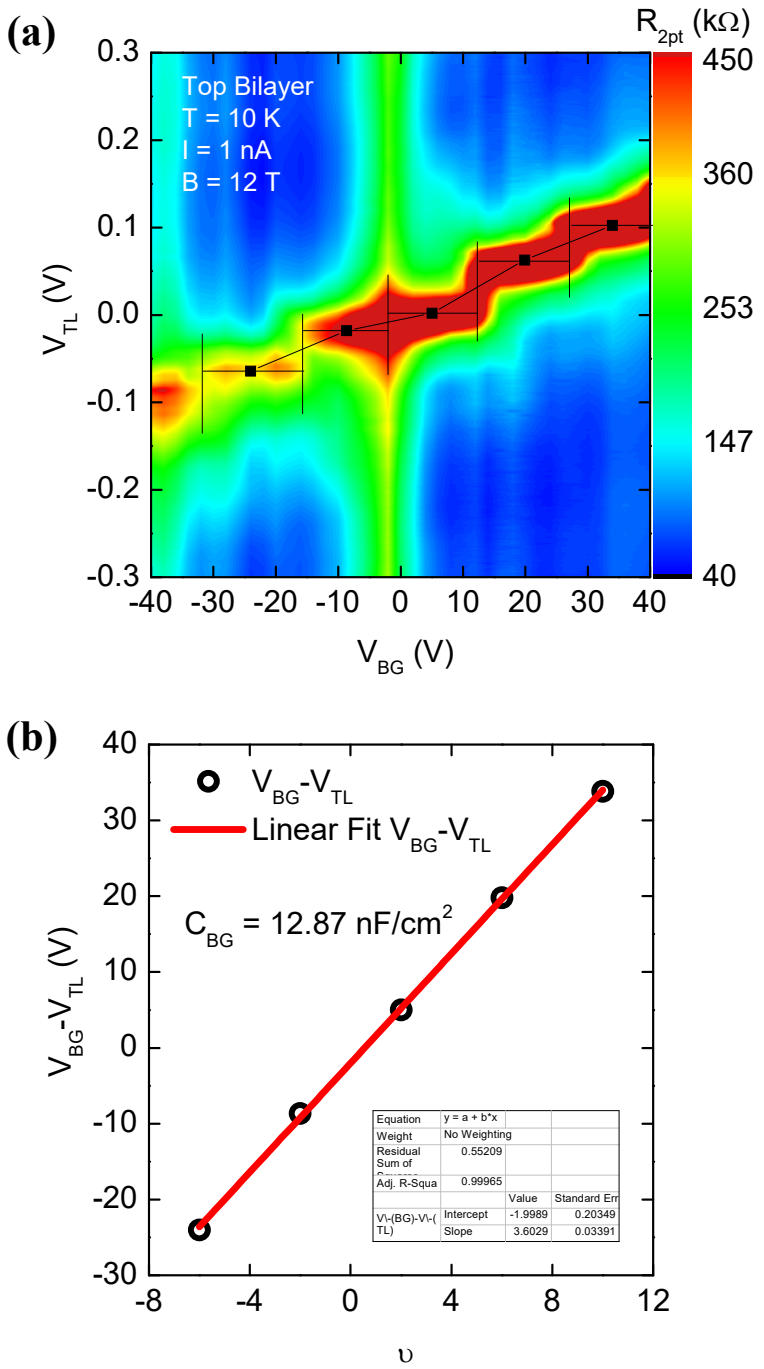

Figure 2.10 (a) Contour plot measured at 10 K for the top BLG under applied vertical magnetic field of 12 T. The black dotted line shows the various filling factors for the Landau levels. (b) The plot from equation 2.3 where the slope gives the value of the back gate capacitance (C_{BG}).

Figure 2.11(a) shows the differential conductance dI_{IL}/dV_{ES} as a function of V_{TL} (top axis) and V_{ES} (bottom axis) at varying temperatures between 1.5 K and 300 K. It can be noted from Figure 2.11(a) that the conductance peaks become somewhat sharper at lower temperature but overall, has a relatively weak temperature dependence, which is indicative of resonant tunneling. In Figure 2.11(b) dI_{IL}/dV_{ES} is plotted as a function of V_{ES} with varying V_{BG}. Figure 2.11(b) data reveals an interesting finding. While the interlayer tunneling resonances occur at V_{TL} values which depend on the applied V_{BG}, the position of the resonance as a function of V_{ES} is independent of back-gate bias. Indeed, the resonance at small V_{TL} occurs always at $V_{ES} = 0$ V, while the second resonance, in the range $|V_{TL}| \approx 0.5 – 0.7$ V, occurs at $V_{ES} = \pm 0.4$ V. This observation suggests the following origin for the two resonances [Figure 2.11(c)]. The first resonance occurs when the charge neutrality points of the two layers come into alignment, and the second resonance occurs when the lower conduction band of one layer aligns with the upper conduction band of the other layer. The separation between the resonance peaks is 0.4 V, which is in very good agreement with the reported energy difference between the first and second band of BLG at the K-point [80].

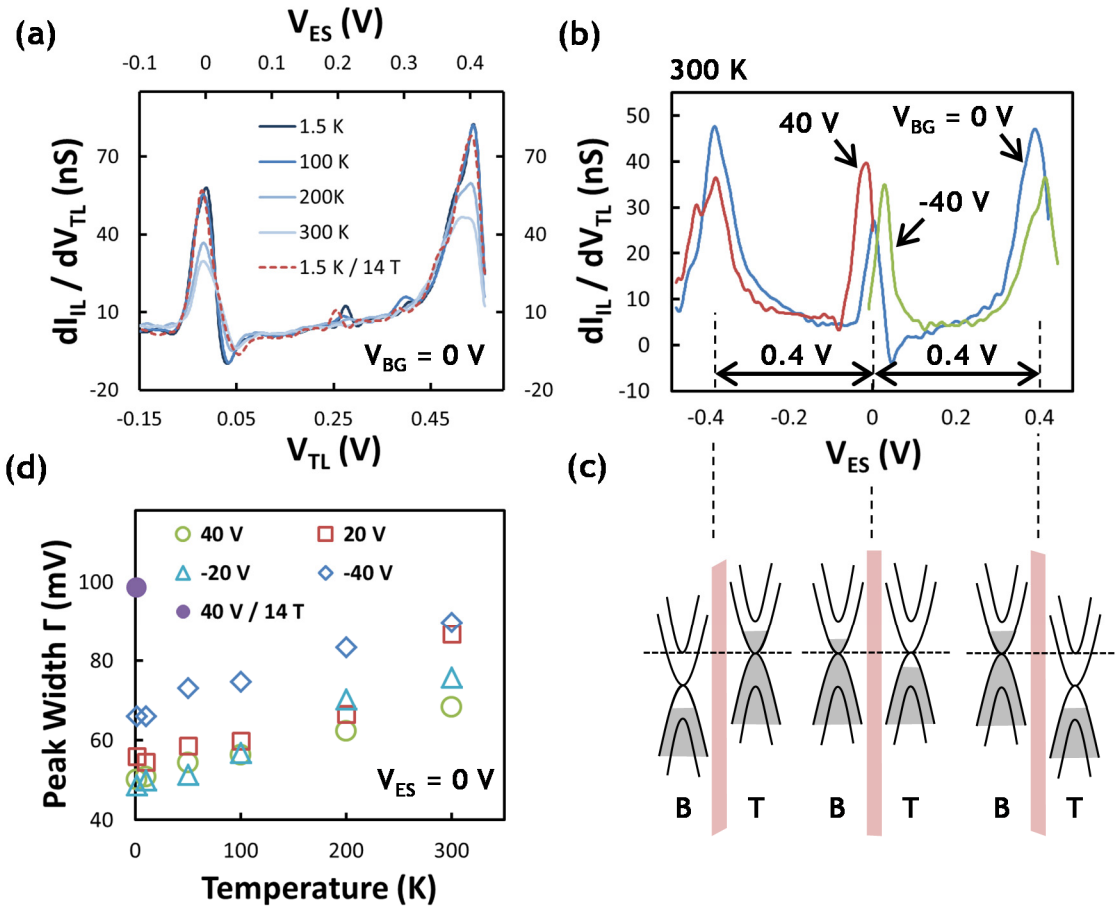

Figure 2.11 (a) Differential conductance (dI_{IL}/dV_{TL}) versus V_{TL} (bottom axis), and electrostatic potential difference V_{ES} (top axis). Temperature and magnetic field dependence is also shown. (b) dI_{IL}/dV_{TL} versus V_{ES} for varying V_{BG}. (c) Band diagram for corresponding bias conditions. The resonance peaks coincide with band alignment conditions. (d) Conductance peak width dependence on temperature.

2.3.2 Temperature Dependence

To further probe the NDR mechanism, the interlayer tunneling characteristics were probed as a function of temperature [Figure 2.12] Although the NDR peaks do sharpen as the temperature is lowered down to 1.5 K, it can be noted from the I-V chracteristics that the temperature dependence is fairly weak. The full width of the conductance (I_{IL}/V_{TL}) peaks at half maximum were calculated and plotted versus temperature at different V_{BG} [Figure 2.11(d)]. The data show the resonance widths depend weakly on temperature in the range 1.5 – 300 K, which is indicative of resonant tunneling [45] and implies that acoustic phonon scattering is a secondary source of broadening. With a very high degree of rotational alignment required to see any resonances, small degrees of rotational misalignment remain a likely culprit for broadening.

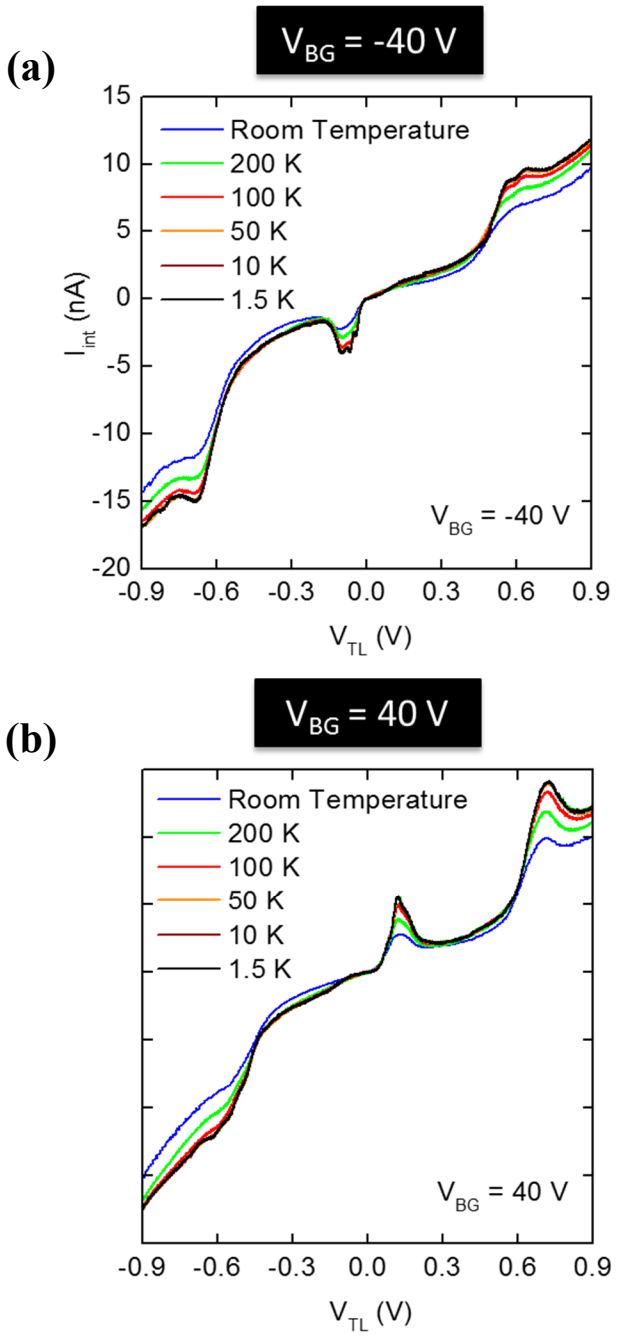

Figure 2.12 Temperature dependence from room temperature down to 1.5 K of the device for (a) V_{BG} = -40 V and (b) V_{BG} = 40 V.

2.3.3 Measurement under In-Plane Magnetic Field

The device characteristics were also examined in the presence of an in-plane magnetic field, applied parallel to the heterostructure plane and perpendicular to the carrier tunneling transport direction as shown in Figure 2.13. The experimental result in perpendicular magnetic fields are discussed extensively in [56],[81]. The in-plane magnetic field supplies momentum to the carrier traveling across the tunnel barrier and effectively induces a shift in momentum space of the two layers energy-momentum dispersions relative to each other, and alters the rotational alignment [55]. The effects of such can be seen in Figure 2.14, where an in-plane magnetic field of 12 and 14 T is applied. The resonant peak sharpens on one side and broadens on the other depending on the direction of the carrier transport. If, for instance, current is flowing in the +z direction and the parallel magnetic field is applied in the +y direction, then the momentum transferred onto the carrier would be in the –x direction. When the current direction is reversed (–z) with magnetic field direction maintained (+y), then the momentum transfer would be in the +x direction. So for a given magnetic field direction, the peak on one side of the I-V curve will sharpen while on the other side it will broaden. This explanation matches the result shown in Figure 2.14. However, it is unclear why for any current direction the secondary resonant peaks are both broadened.

A current carrying wire $\vec{l}$ under applied magnetic field $\vec{B}$ will experience a Lorentz force $\overrightarrow{F_B} = I\vec{l} \times \vec{B}$ where I is the current. Dropping time on either side of the equation gives the momentum $\Delta\overrightarrow{p_B} = ed\overrightarrow{l_z} \times \vec{B}$, where e is the elementary charge and d is the tunnel barrier thickness. With an applied magnetic field of 14 T, the shift in the momentum would be 3.2×10^{10} m^{-1} with the momentum at the K point $|\Gamma K| = 1.7 \times 10^{10}$ m^{-1}. Thus, the effective change in rotational alignment amounts to roughly 0.1 °. This

seemingly small change causes a dramatic change in the sharpness of the NDR peak as has been predicted by theory and as shown in Figure 2.14, and exhibits how critical rotational alignment is in determining the performance of ITFETs based on 2D materials that have carriers that are located at the edges of the Brillouin zone.

Figure 2.11(a,d) data show that the conductance peak slightly broadened when a 14 T magnetic field was applied parallel to the sample plane. However, elastic scattering and, at larger back gate biases, band distortion due to inter-bilayer electric fields and predominantly spontaneous optical phonon emission when the resonance occurs at interlayer chemical potential differences larger than the optical phonon energy, also could contribute to broadening.

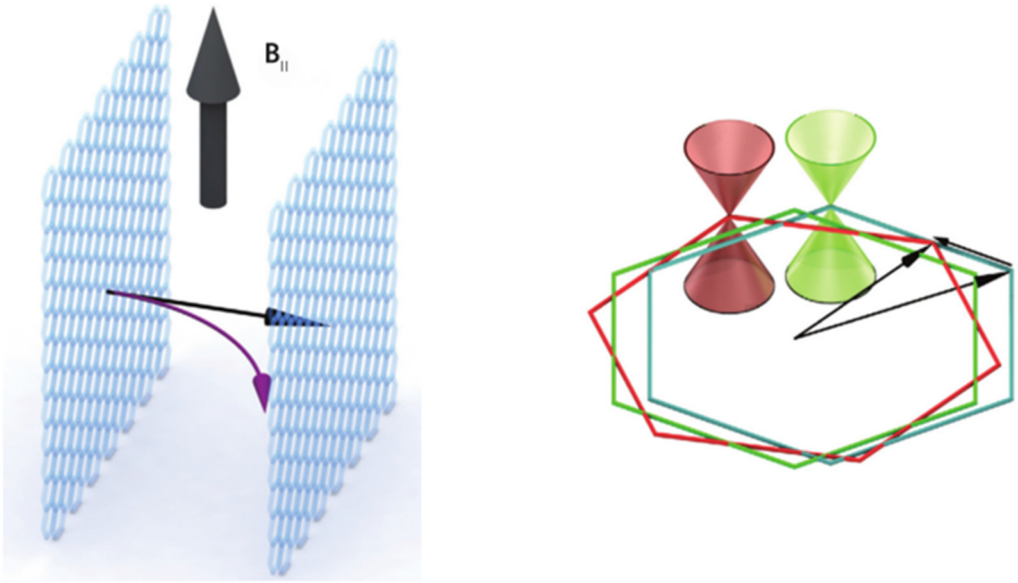

Figure 2.13 Illustration of how an applied magnetic field parallel to the graphene plane and perpendicular to the tunneling electron transport direction (z direction) can lead to a momentum transfer in the x-y plane and effectively shift the bands of one layer relative to the other in the x-y plane. Adapted from [55].

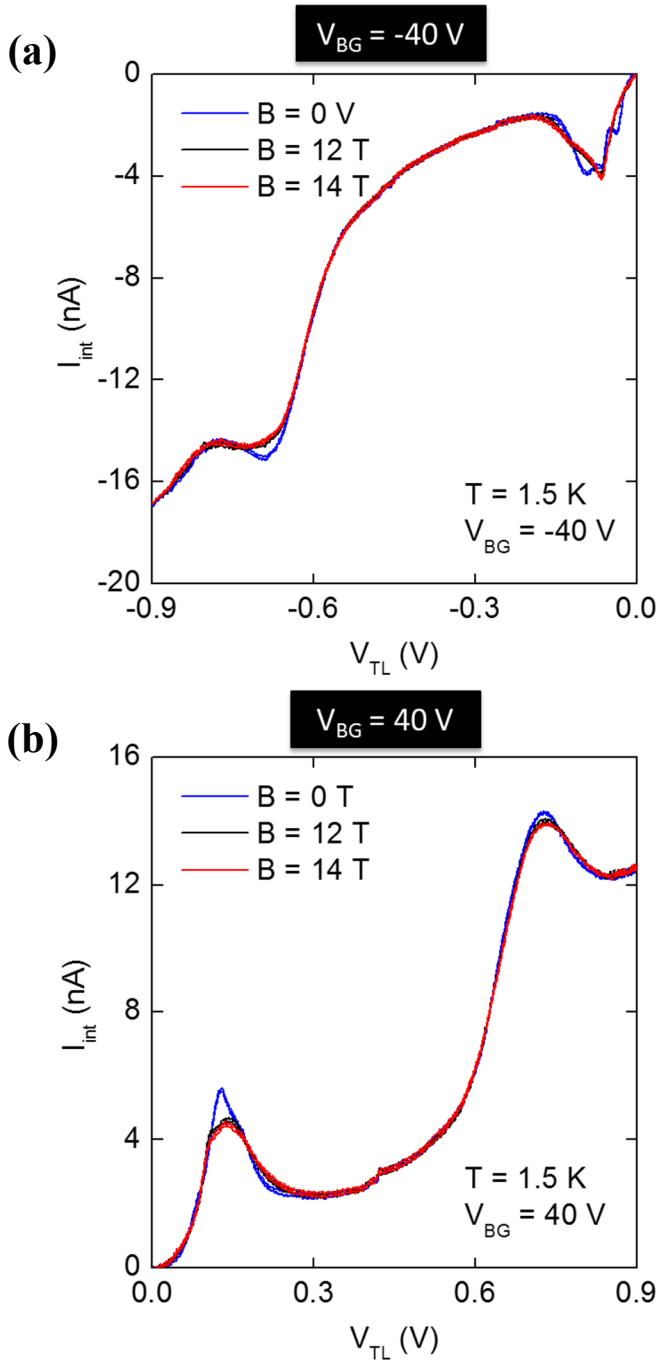

Figure 2.14 I-V characteristics for (a) V_{BG} = -40 V and (b) 40 V for varying parallel magnetic field magnitude (0, 12 14 T).

2.3.3 Band Gap Opening in Bilayer Graphene and Effects Thereof on ITFET Operation

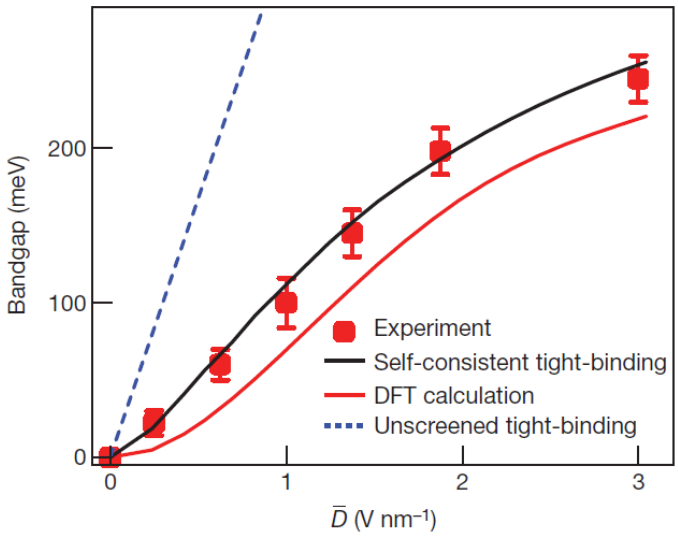

Figure 2.15 Band gap in bilayer graphene as a function of applied vertical electric-field. The experimental observation (red squares) matches well with the theoretical predictions based on self-consistent tight-binding model (black traces). Adapted from [21].

Since BLG is known to open up a finite band gap when a vertical electric field is applied [Figure 2.15] [21], we address the role of BLG bandstructure change as a function of V_{BG} and V_{TL} and its impact on interlayer tunneling characteristics. In addition to tuning the layer densities of the heterostructure, the applied V_{BG} and V_{TL} change the transverse electric fields across the two bilayers, and consequently their energy momentum-dispersions. For the device considered here the electric field across the top layer is independent of V_{BG} for the $V_{ES} = 0$ resonance, while the transverse field across the bottom layer varies from E = -0.28 V/nm at V_{BG} = -40 V to E = 0.30 V/nm at V_{BG} = 40 V [56]. This, in turn, leads to a band-gap opening in the bottom layer at large positive and negative

V_{BG} values, which can alter the electrostatic potential conditions at which the resonance occurs [83]. The corresponding band gap opening at these electric-field according to Figure 2.15 is 20~30 meV. The small magnitude of the band gap opening is the reason behind the effects of such not being clearly visible at room temperature. For example, in the case of a bottom (top) layer with finite (zero) band gap, two closely spaced resonant peaks are expected near V_{ES} = 0, associated with the bottom layer conduction or valence band alignment with the top layer neutrality point. Signatures of this phenomenon are observed in the interlayer current-voltage characteristics of our device at low temperatures as can be noted in Figure 2.16.

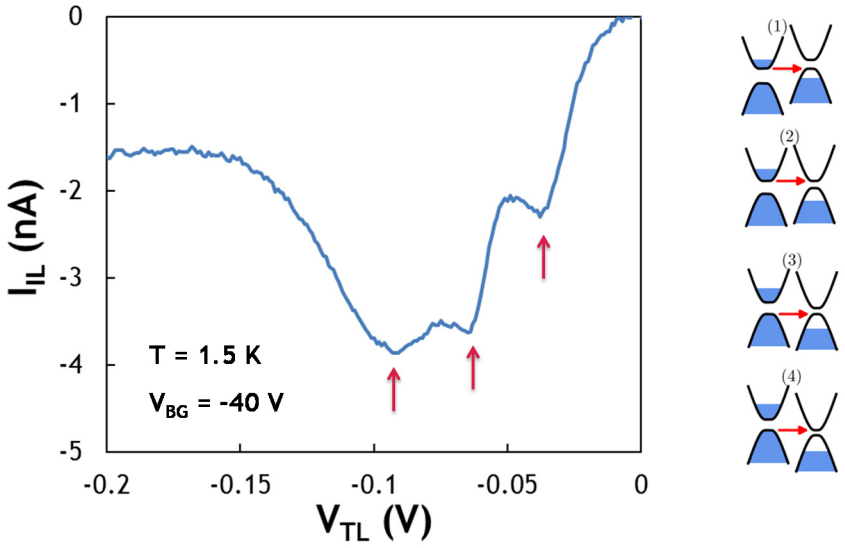

Figure 2.16 Interlayer I-V characteristics at 1.5 K with V_{BG} = 40 V bias. It can be noted that the broad overall NDR peak is split into multiple peaks. This is due to the band gap opening of BLG at high vertical electric field, and the associated increase in the number of resonance conditions that can be established.

2.4 SRAM APPLICATION

Connecting two NDR devices in series, the characteristic curve of the two devices form two stable points in equilibrium where the circuit can fall into. These stable points can serve as the logic LOW and HIGH states and can therefore be used as a memory element [84]. Utilizing the NDR characteristic of our device, we demonstrate a one transistor latch or SRAM operation at room temperature, as shown in Figure 2.17. When a load resistor is connected in series with the ITFET device, the characteristic curve of the two elements will make intersections at two stable points – for convenience we will call them left and right stable points. If one sweeps the V_{DD} in the circuit diagram of the inset in Figure 2.17(b) from LOW to HIGH, the output voltage (V_{OUT}) will initially be settled to a point where the load line and characteristic curve make an intersection at the low voltage region (left stable point). As V_{DD} is increased, the load line moves up along the curve, and once the V_{DD} is high enough that the intersection between the load line and the device characteristics reaches the peak point of the curve and can no longer be established in the low voltage region, V_{OUT} will make a sudden jump to the high voltage region (right stable point) where the load line and characteristic curve makes a second intersection. When V_{DD} is at HIGH, the intersection between the load line and device curve is initially established in the high voltage region (right stable point) and therefore V_{OUT} is at HIGH. When V_{DD} is decreased from HIGH to LOW, V_{OUT} will remain HIGH until the load line reaches a point where the right stable point forms at the valley of the device characteristic curve, at which point the intersection point will jump from right to left and V_{OUT} will fall from HIGH to LOW. By varying V_{BG}, the peak-to-valley current ratio (PVCR) of the NDR peaks can be varied, which determines the intersecting points of the load line and the device

characteristics, resulting in a variation in the SRAM operation window. At the extreme bias where there is no NDR, such operation does not occur as can be noted from Figure 2.17.

If one replaces the load resistor with a conventional MOSFET acting as the access transistor, this setup can be used as an SRAM. Conventional implementation of an SRAM cell consists of 6 MOSFETs; four for the cross coupled inverters for data storage and two for the access transistor for controlling the access to the data storage region during read and write operation. Our implementation will only require one MOSFET for the access control and one ITFET for the data storage. Considering the fact that SRAM cache in a modern processor makes up over 50 % of the die area and this percentage is increasing with scaling and is expected to exceed 80 % in the near future [http://electroiq.com/blog/2014/02/the-most-expensive-sram-in-the-world-2-0/] reducing the number of components for the same functionality will be a significant game changer. However, currently, the performance of this ITFET based SRAM lacks far behind that of the MOSFET only implementation and significant improvements must be made for practical use. We surmise that with a higher PVCR, which can be achieved through better rotational alignment and elimination of non-ideal effects [56], one would be able to increase the operation window. Furthermore, by increasing the number of tunnel barriers to make multi-barrier structures could allow for multiple NDR peaks to appear, with which one could potentially implement multi-valued SRAM [85].

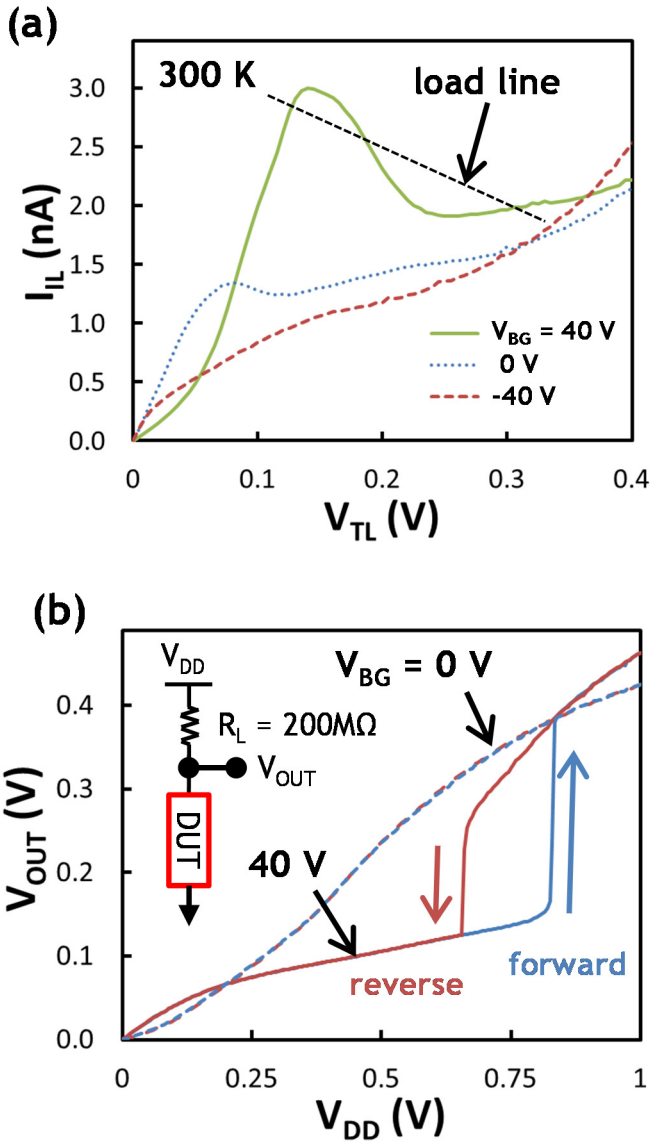

Figure 2.17 (a) Interlayer I-V characteristics at different V_{BG} biases, and the load line of the series connected resistor. The NDR at high V_{BG} allows two stable points with the load line for latch/SRAM operation. (b) Output characteristics of the SRAM. An operation window of 0.2 V can be obtained at V_{BG} = 40 V.

2.5 SUMMARY

In summary, we demonstrated a double BLG heterostructure operating as a vertical ITFET, which shows multiple NDR peaks up to room temperature, consistent with resonant tunneling due to the alignment of the two sub-bands of the two BLG layers. In addition, based on electrostatic calculations we have shown that the peaks occurring at higher voltages are due to the alignment of the lowest sub-band of one layer to the second sub-band of the other layer. The characteristic NDR peaks show a very weak temperature dependence, indicative of resonant tunneling. Parallel magnetic field applied to the device resulted in sharpening/broadening of the NDR peaks depending on the current direction. By connecting a load resistor to the device, we have also demonstrated that the device can be operated as a one transistor SRAM or latch.

CHAPTER 3: ITFETs with Varying Graphene Conduction Layer Thickness: Effects of Band Structure on Device Characteristics

3.1 INTRODUCTION

Advancements in the fabrication techniques for heterostructures based on two-dimensional materials has facilitated the study of such structures for various applications [52]. Such structures have also been studied as vertical tunnel field effect transistors (TFETs) in recent years [36],[86]. Especially, interlayer tunnel FETs (ITFETs), whose operation is based on band alignment and resultant resonant tunneling between two conduction layers through a tunnel barrier, offer the possibility of obtaining sharp negative differential resistance (NDR), and has attracted much attention [54]-[56],[87]. Such devices have been demonstrated for double monolayer graphene [54],[55] and double bilayer graphene [56],[87] functioning as the conduction layer, with hexagonal boron nitride (hBN) used as the interlayer tunnel dielectric. These devices exhibited NDR characteristics which are gate tunable. Also, there have been theoretical predictions of such phenomenon occurring even between distinct number of graphene layers [88], and also reports of possible phonon-mediated resonant tunneling [89]. Attempts have been made to model such behavior, which has helped in better understanding the physics behind such devices [53],[83],[82],[90],[91],[92],[93]. Various applications that utilize this NDR characteristic have also been demonstrated [55],[87],[94]. However, the NDR observed in these devices were only comparable to that which have been obtained in the past in terms of peak-to-valley current ratio (PVCR), for instance, in Ge pn-junction Esaki diodes [44], and inferior to that obtained for InGaAs/AlAs/InAs resonant tunneling diodes [49],[50], although the voltage at which the NDR peaks occur was somewhat scaled down.

Notwithstanding theoretical work on what kind of materials and device dimensions would be advantageous for obtaining higher PVCR in these two-dimensional (2D) heterostructures [95],[96], corresponding experimental efforts into identifying performance-limiting factors for ITFETs have been limited. Here, we present the results of an exploration of various combinations of different graphene layer thickness and hBN thickness, with the aim of providing a list of lessons learned which will act as a guide to what kind of materials or band structures should be used in order to achieve improved performance in ITFETs; i.e., enhanced PVCR. We explored double bilayer, trilayer, quadlayer, and both Bernal-stacked and rhombohedral-stacked pentalayer graphene as the electrode layer, with varying hBN tunnel barrier thicknesses. We find that the differing band structure for the multilayer graphene layers with varying graphene thickness causes significant changes in the interlayer current-voltage characteristics, and that certain band structures are more preferable than others in obtaining higher PVCR. Also, we find that with extremely thin interlayer hBN thicknesses of two atomic layers and even number of layer graphene, the resonance peaks can split into smaller sub-peaks at high biases due to the band gap opening effect, and cause the overall peaks to broaden.

3.2 Fabrication of Device

3.2.1 Improvements in Transfer Method

The introduction of polymer stamp based van der Waals transfer method has facilitated the fabrication of heterostructure devices [57], and made possible numerous studies on tunneling field effect transistors (TFETs) made with various 2D materials

[97],[98],[99],[100],[101]. However, for resonant tunneling ITFETs made with 2D materials that exhibit a conduction band minima at the K point, rotational alignment between the two electrode layers was still a problem that had to be addressed. Initially, the method for establishing rotational alignment between the graphene electrode layers was by identifying the straight edges of the exfoliated graphene flakes which made multiples of 30 ° angles at the corners, and aligning the two layers during transfer in the hopes that such an edge would be of the same major crystallographic orientation, namely zig-zag or armchair. It was later shown that through polarized Raman spectroscopy one could actually distinguish between the two types of edges after exfoliation, and by carefully aligning the flakes during the transfer process, one could establish rotational alignment within a range of 2 ° [55],[102]. In addition, it was shown how one could check the final rotational alignment between the top and bottom layers by assessing the level of broadening of the 2D peak of graphene on hBN through Raman spectroscopy [103]. Although this method provided a more definitive way for rotationally aligned electrode layers, it was still a time consuming arduous process. It involved obtaining graphene flakes that had an edge with a major crystallographic orientation, conducting Raman measurements for each flake and each edge, and going through a risky layer-by-layer transfer process. In addition, the level of alignment achievable was still limited by how accurately one could distinguish the straight edges of the graphene flake during transfer under an optical microscope.

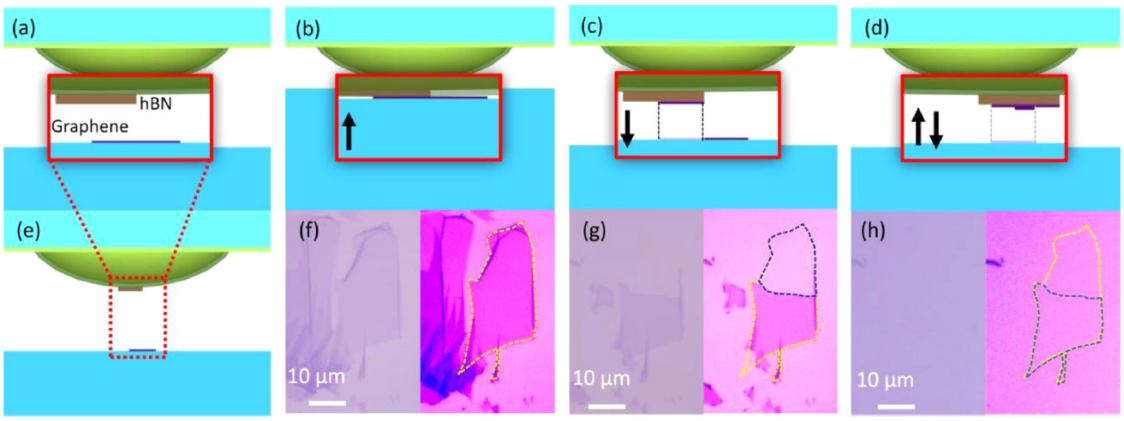

Figure 3.1 Illustration of how with the use of a hemispherical shaped polymer stamp, one can selectively pick up portions of a monolayer graphene flake. The stronger bonding between hBN and graphene relative to that of graphene and SiO_2 and also the intralayer bonding, allows the graphene to tear and get selectively picked up. Adapted from [104].

Further facilitation to the transfer process for 2D heterostructures – more specifically for ITFET fabrication – was made recently. Kim et al. introduced an improved rotationally aligned transfer method by making use of a hemispherical shaped polymer stamp instead of a flat one, which allowed a smaller selective contact area of the polymer stamp to the substrate [Figure 3.1] [104]. Using this hemispherical polymer stamp, one would first pick up an hBN flake with which, selective contact would be made to a single monolayer graphene flake. When the stamp is retrieved, only a portion of the monolayer graphene flake where it had made contact to the hBN would get picked up and the remaining uncontacted area would remain on the substrate. This is primarily due to the stronger bond between hBN and graphene over graphene and SiO_2, and also the very weak bond between the polymer stamp and graphene. Then, stacking it onto the remaining portion of the graphene flake, they were able to make an artificial bilayer graphene stack. The process steps are described in Figure 3.1.

3.2.2 Flake Transfer

The double multilayer graphene ITFETs used in this study are fabricated using a process similar to this recently developed dry transfer method that can ensure the rotational alignment of the two graphene conduction layers [104]. A large multilayer graphene flake – whose thickness and stacking order is determined by a combination of optical contrast and Raman spectroscopy [25],[61],[105],[106],[107],[108] – is first sectioned into separate parts with clearly identifiable straight edges by means of electron beam lithography (EBL) and O_2 plasma etching, as shown in Figure 3.2(b). Then, vacuum anneal is conducted in order to remove polymer residues on the graphene flakes, which tend to hinder the pickup of patterned flakes with the polymer stamp. It has been reported that the stacking order of graphene does not change with conventional processing for device fabrication with reports of stable rhombohedral-stacking up to processing temperatures of 800 °C [107]. Nevertheless, we confirmed through Raman mapping that no change in the stacking order for multilayer graphene occurred during the transfer or device fabrication process. Using a polymer-coated glass stamp, the top hBN is first picked up, with which the top graphene, interlayer hBN, bottom graphene, and bottom hBN flakes are picked up sequentially and selectively. The position and rotation of the samples on the stage or the stamp itself are unaltered throughout the transfer process. This process flow ensures that the two graphene layers are rotationally aligned in real space, and as a result, that the two *K*-points of the top and bottom layer graphene are rotationally aligned in k-space [104], which allows momentum conserving tunneling to occur. Even if the stamp or stage orientation is accidentally altered, one could still rely on the straight edges of the patterned graphene flakes in order to establish rotational alignment, although this would be a slightly less accurate method. The whole stack is then landed onto a fresh Si/SiO_2 substrate as shown

in Figure 3.2(f). Several samples were made using this method, with varying graphene and hBN layer thicknesses. Optical microscope images of some of them are shown in Figure 3.3 and a list of samples with their respective graphene and interlayer hBN tunnel barrier thickness is given in Table 3.1.

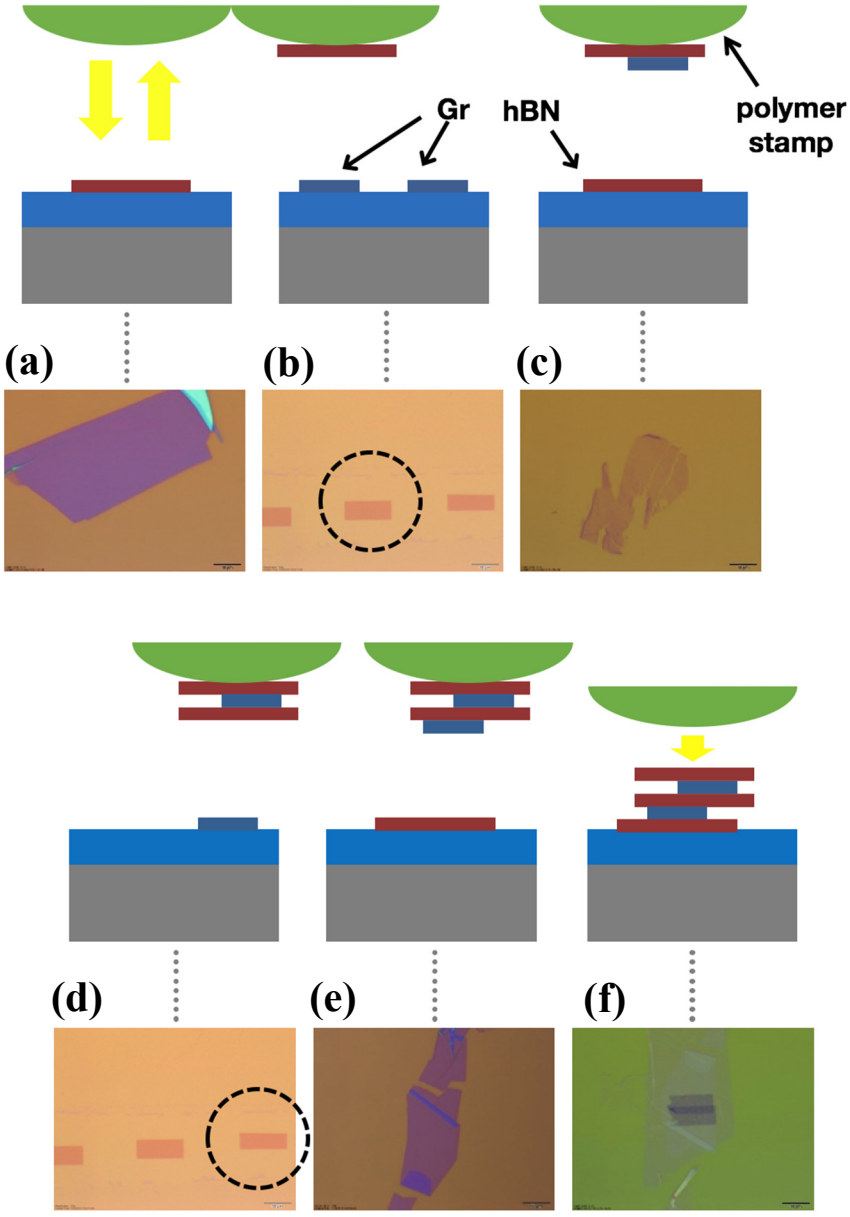

Figure 3.2 Illustration of how the transfer process is conducted. (a) Using a bulb-shaped polymer stamp, a relatively thick top hBN layer is picked up. Then, (b) a pre-patterned graphene flake for the top electrode layer is picked up without the stamp making contact to adjacent flakes. Without altering the rotation of the graphene sample, (c) the interlayer hBN and (d) bottom electrode graphene layer is captured sequentially. Finally, (e) the bottom hBN is added to the stack and (f) released onto a fresh Si/SiO_2 substrate for further processing.

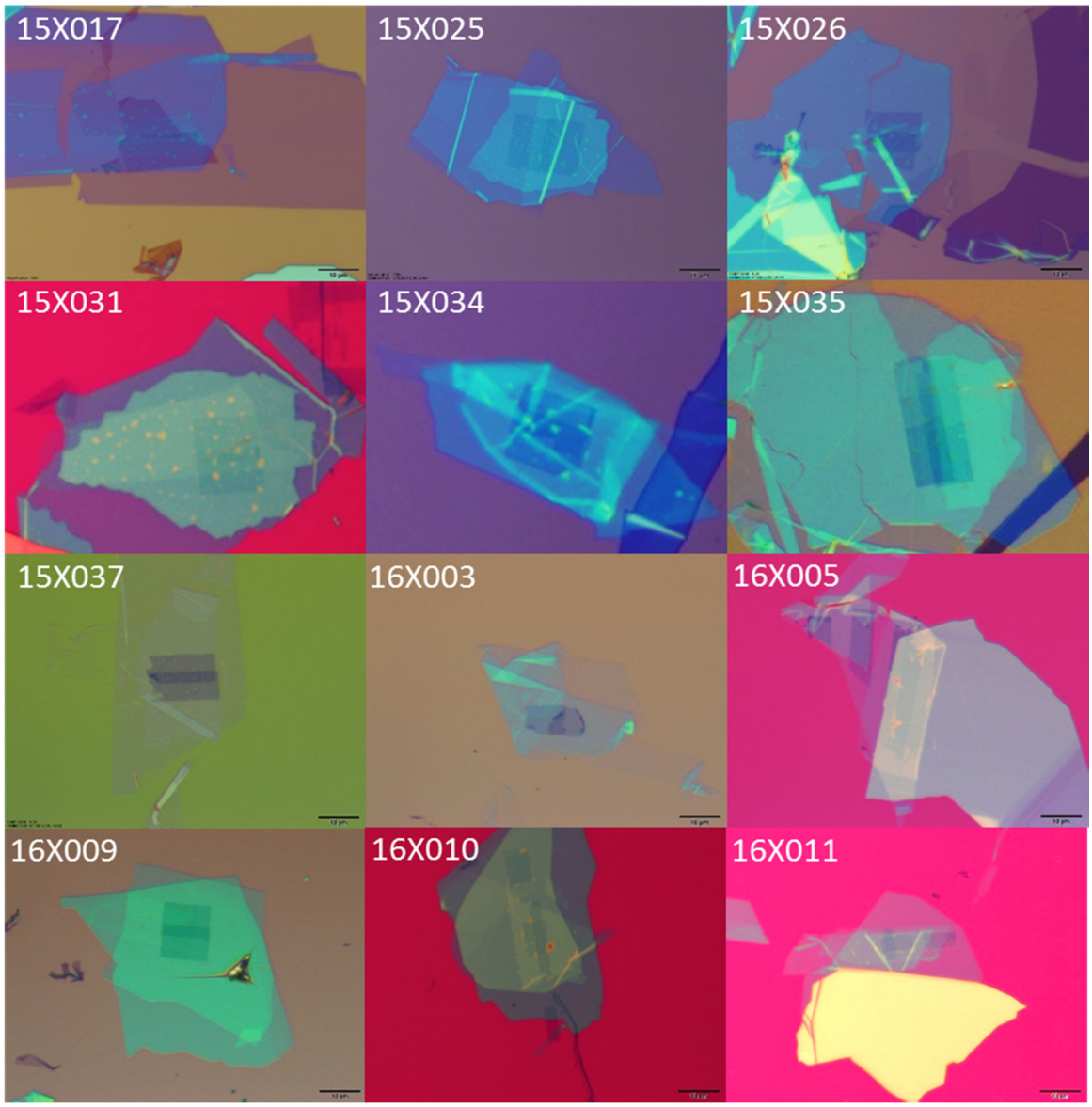

Figure 3.3 Optical microscope images of several devices that were fabricated using the rotationally aligned transfer method. Graphene and interlayer hBN thickness for each device is given in Table 3.1.

Graphene Layer Thickness	hBN Layer Thickness						
	1	2	3	4	5	6	7
M				15X032 15X036			
B		15X031		GB70	14X021 15X035	15X031	
bT					15X035	15X025 16X003	
rT		15X030		15X026		15X022	
bQ	15X034	15X037		16X009			
rQ							16X005
bP			15X017	16X009			
rP					15X035		

Table 3.1 List of fabricated devices. Graphene layer thickness and stacking order is shown on the rows. Thickness ranges from monolayer to pentalayer and for different stacking order (Bernal and rhombohedral) for tri-/quad-/penta-layer. The columns are for varying interlayer hBN tunnel barrier thickness ranging from 1 to 6 atomic layers. Sample numbers written in green are devices that showed clear NDR, yellow represents samples that only showed staircase features in the IV characteristics, red represents samples with no NDR feature or sample with high leakage, and finally grey denotes samples that were lost during processing. Samples that underwent a vacuum anneal step after active plasma etching is underlined.

3.2.3 Graphene Stacking Order

In theory, multilayer graphene can have a varying number of stacking order depending on the layer thickness. However, it is well known that for graphite there are mainly two stacking orders that occur naturally [109]. It was suggested in the same study that the relative portion of the stacking orders were around 14 % ABC-stacking, 6 % disordered, and the remaining 80 % ABA-stacking. This is because these are the only stacking orders that are energetically favorable [26]. Studies done on exfoliated graphene also show that graphene has a similar proportion for the stacking order [27],[107]. One can clearly differentiate between these two stacking orders by either Raman spectroscopy [107],[108],[110],[111],[112] or infra-red excitation measurements [27]. Since infra-red excitation measurements require special instrumentation especially for fine spatial resolution, we utilize the Raman method in our experiements. The difference in the Raman spectrum shows up most prominently in the 2D peak [107] which originates from the double-resonant electronic process, and as such is sensitive not only to the phonon modes but also to the electronic band structure [113]. Other modes such as the G* and M bands [108], and also CN1 [112] have also shown to be distinctive for different stacking order. In our study, we used the difference in 2D peak width and shape [Figure 3.4] in order to distinguish between ABA- and ABC-stacking. Band structures for ABA- and ABC-stacking has been expected to vary drastically [114],[115],[116],[117] and also proven so through experiments [118],[119],[120],[121]. For example, while ABA-stacked graphene has a Dirac cone band for odd number of layers [114], ABC-stacked graphene does not have such a band and exhibits extremely flat bands or low-energy van Hove singularities [120]. Also, while ABA-stacked trilayer remains semi-metallic [122] under applied electric field, ABC-stacked trilayer opens up a sizable band gap [29],[117],[123],[124],[125],[126].

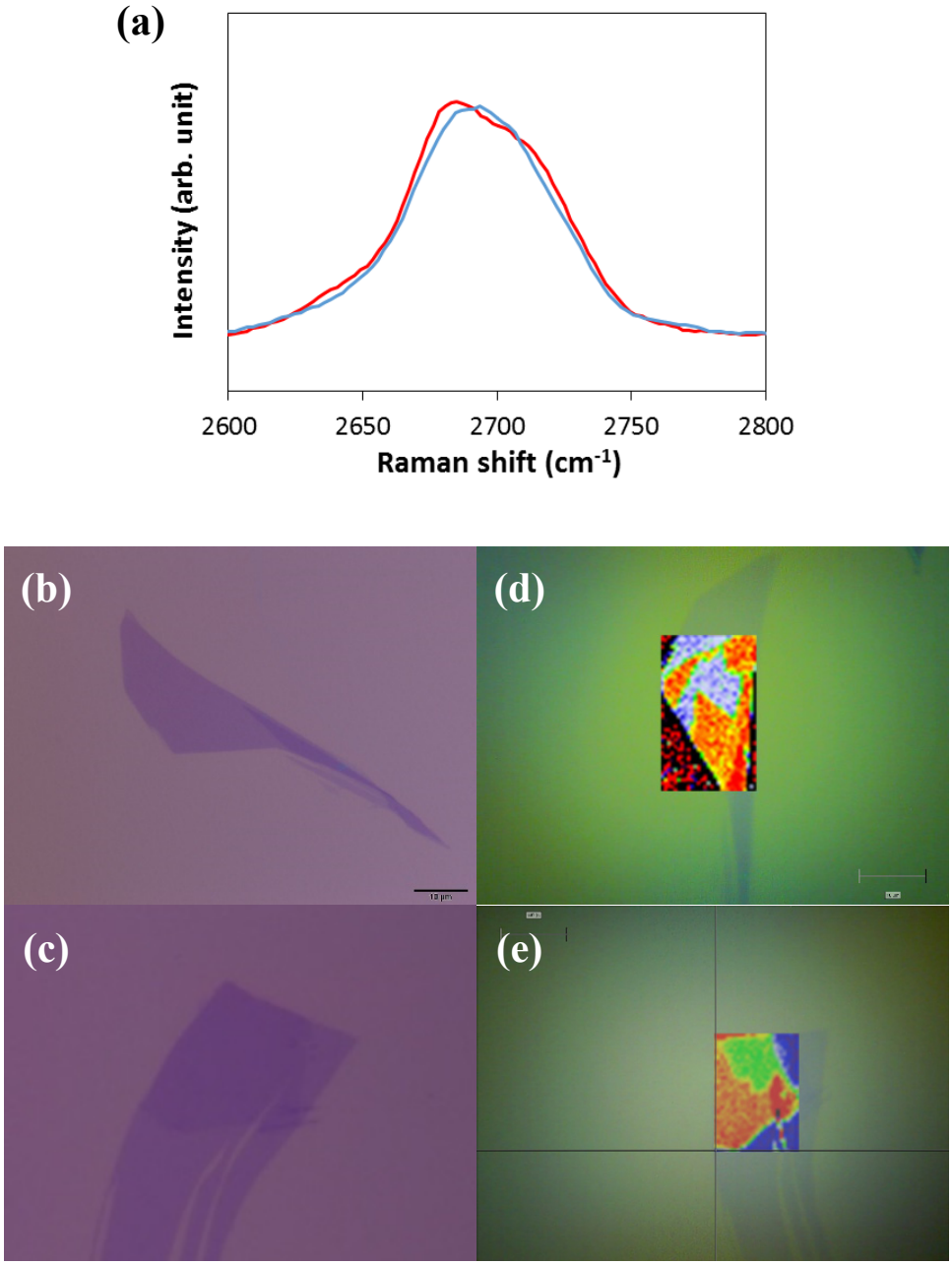

Figure 3.4 (a) Raman spectrum comparison between ABA(Bernal)-stacking (blue) and ABC(rhombohedral)-stacking (red). ABC-stacking shows a distinctive head and shoulder feature while ABA shows a smooth head only. Below images show how a seemingly uniform (b) trilayer and (c) quadlayer graphene flakes can reveal different stacking order under the (d,e) Raman spectroscope (red: ABC-stacking, green/blue: ABA-stacking)

3.2.4 hBN Thickness Determination through Raman Spectroscopy

Determining the hBN layer thickness prior to flake transfer and device fabrication is essential in order to obtain a reasonable current level for the ITFET operation and also for the NDR to appear. Previously, the hBN thickness could only be estimated through a combination of optical contrast and AFM measurements. However, due to constraints on the optical contrast for thin hBN [62] and errors in the AFM measurements [127] prevented one from accurately determining the hBN layer thickness. It was hinted by Gorbachev et al. [62] that the hBN Raman peak intensity seemed to have a correlation with the thickness but no hard evidence was provided.

For this purpose we developed a method for pre-determining the interlayer hBN thickness through Raman spectroscopy before any processing. We established a direct correlation between the Raman hBN peak intensity at 1364 cm^{-1} (or its ratio to the neighboring Si Raman peak at 965 cm^{-1}) with the hBN thickness determined by the interlayer current measured on a graphene-hBN-graphene heterostructure. The tunneling current level across an hBN tunnel barrier changes by over ~1.5 orders of magnitude for an additional single atomic layer of hBN [56],[86], so this can be a very accurate measure of the hBN layer thickness. The correlation that we established is shown in Figure 3.5. We first take the intensity of the Si and hBN peaks, which in this case is roughly 2250 and 1500 counts, respectively, and take the ratio of hBN intensity over Si intensity – 0.67. As an estimate, one can determine the hBN layer thickness by multiplying 16 to the hBN/Si peak intensity ratio and subtracting it by one. It can be noted that the correlation is fairly accurate with an R^2 of 0.94 down to a monolayer of hBN. In the example of Figure 3.5(a) it turns out the thickness of that hBN flake is 10 layers or 3 nm.

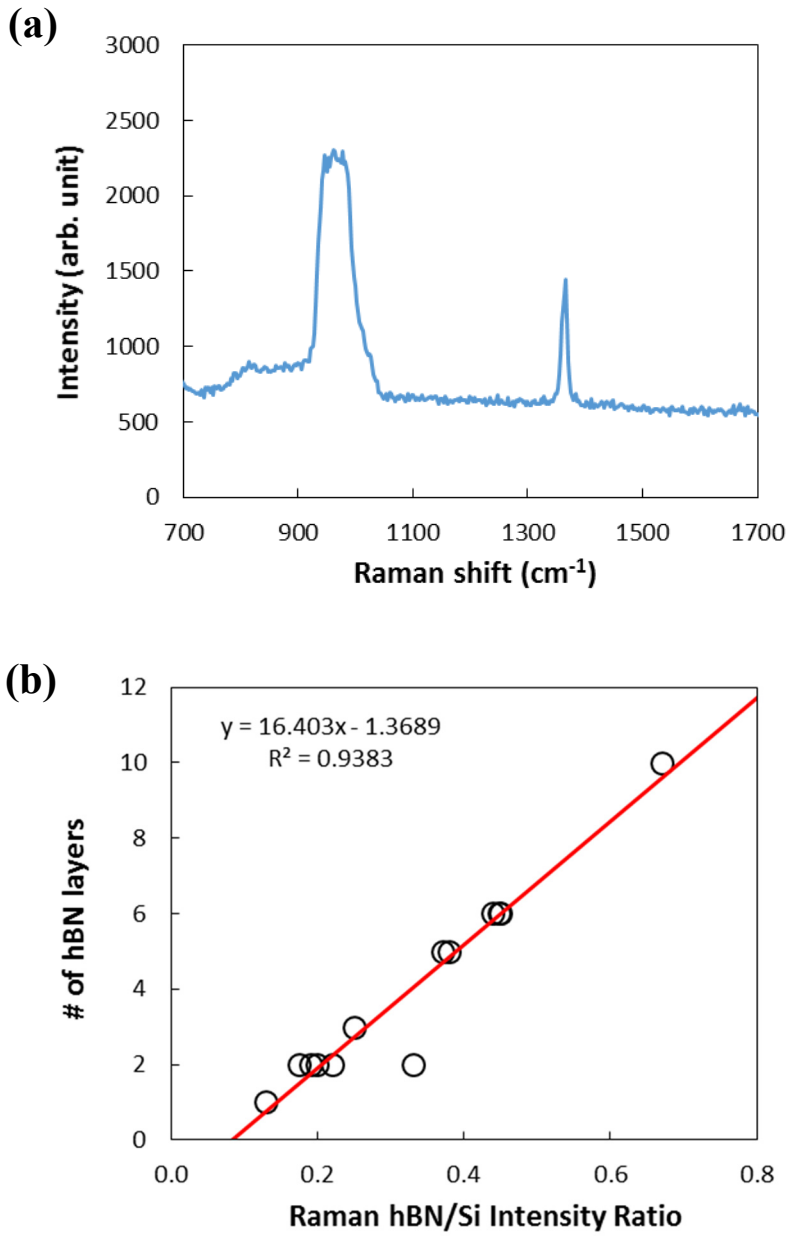

Figure 3.5 (a) Raman spectrum of a typical hBN flake. The peak at 1364 cm-1 is from the hBN and the peak at 965 cm-1 is from the Si. The ratio between the two is taken. (b) A correlation between this ratio and the hBN thickness determined by the tunneling current.

3.2.5 Device Fabrication

After the stack is made using the rotationally aligned transfer method, it is vacuum annealed at 350 °C for 8 hours for air bubble removal. Then, PMMA is spin coated at 3500 rpm for 40 seconds and baked on a hot plate at 140 °C for 2 minutes for removing the solvents. The active region is patterned using EBL with a beam current of 30 pA and dose of 280 $\mu C/cm^2$. While negative resist (HSQ) was used for the active patterning in our initial double bilayer graphene experiments, it was soon realized that this is not necessary and a positive resist (PMMA) is sufficient for obtaining good contacts. Subsequently, using the PMMA layer as an etch mask, the sample is exposed to a series of CHF_3+O_2/O_2/CHF_3+O_2/O_2 plasma etching for etching the alternating hBN and graphene layers. It was found that CHF_3+O_2 plasm was not suitable for effectively etching graphene and O_2 plasma did not etch hBN, so a series of plasma etching with a different gas was required. The PMMA layer is removed by dipping the sample in acetone for 10 minutes. A new PMMA layer is spin coated at 3500 rpm for 40 seconds and baked on a hot plate at 140 °C for 2 minutes for solvent removal. The metal contacts are also defined through EBL with subsequent thermal evaporation of 100 Å of Cr and 400 Å of Au and lift-off. This process flow results in independent one dimensional (1D) contacts to the edges of the top and bottom graphene [57]. For this particular device (15X035), we used a graphene flake that had regions of bilayer, Bernal-stacked trilayer and rhombohedral-stacked pentalayer graphene [Figure 3.6(b)]. The flake was sectioned in such a way, that when transferred on top of each other, the final device would have regions of double bilayer, bilayer-to-trilayer, double trilayer, trilayer-to-pentalayer, and double pentalayer, using the same top, interlayer and substrate hBN dielectric [Figure 3.6(c,d)]. In the discussions below, we only deal with the devices that have the same graphene thickness on either side. This experimental setup

was intended to minimize the microscopic device-to-device fluctuations between devices in terms of the rotational alignment, variations in the interlayer hBN, and surrounding environment. This ensured that these factors that can influence the tunneling characteristics were limited, and we were mostly observing the effects of multilayer graphene electrode layer thickness. In addition, we fabricated and characterized a double bilayer and double quadlayer graphene device with two atomic layers of interlayer hBN. The devices were characterized under high vacuum, and all measurements were conducted at room temperature. A simple schematic of the device and the bias condition is given in Figure 3.6(a), where the heavily doped back Si is used as back gate and the top layer is biased relative to the bottom layer. The device fabrication process steps are shown in Figure 3.6(b-e). Finally, the band structures for the graphene electrode layers used in this study are given in Figure 3.6(f) [23],[114].

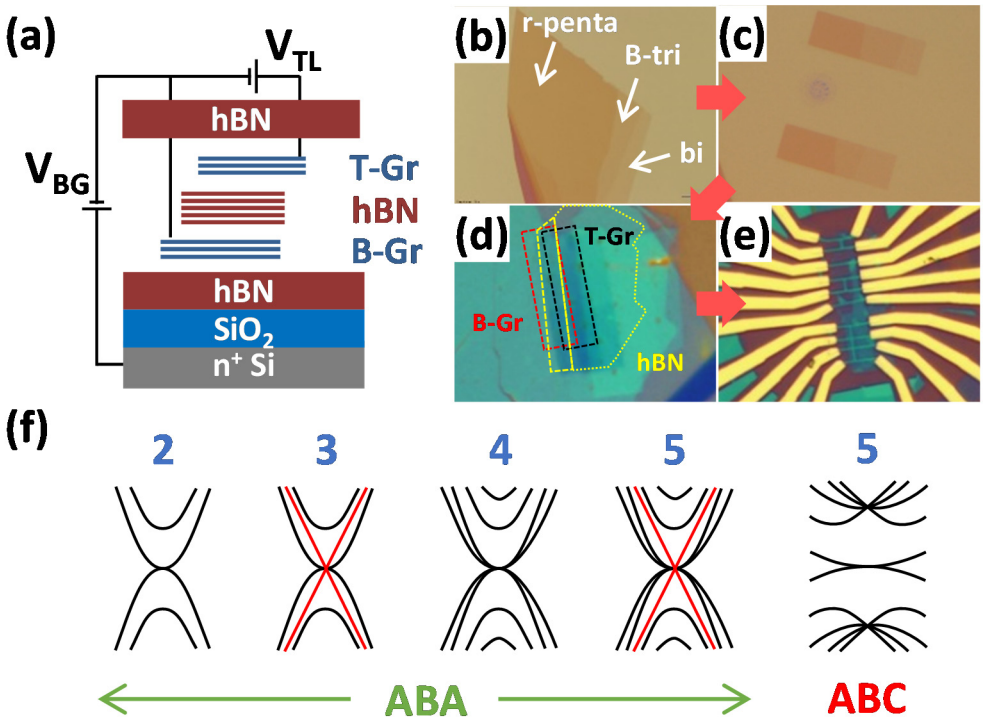

Figure 3.6 (a) Schematic of the device structure and biasing scheme. The thickness of the top and bottom graphene layers is varied from 2 to 5 atomic layers. (b) Initial graphene flake showing regions of bilayer, trilayer and pentalayer. (c) The graphene flake is divided into two parts by means of electron beam lithography and O_2 plasma etching. (d) The flakes are transferred to make an hBN-Gr-hBN-Gr-hBN heterostructure on top of a Si-SiO_2 substrate, while maintaining the relative rotational alignment of the two graphene layers. (e) The stack is partitioned into separate parts to make devices with various combinations of electrode layers. (f) Band structure for the electrode layer used in the devices for this study [114]. The top numbers indicate the number of graphene layers. Only odd number of layer graphene with Bernal (ABA) stacking exhibit a Dirac cone sub-band (red).

3.3 DEVICE RESULTS

3.3.1 Dependence on Graphene Thickness

Figure 3.7(a) shows the area normalized interlayer current (I_{INT}) versus top layer bias (V_{TL}) characteristics at room temperature of the three devices with differing graphene layer thickness fabricated at the same time. Only step-like features could be observed in the I_{INT}-V_{TL} characteristics for these samples, unlike previous results where multiple NDR peaks were observed for the case of double bilayer device [56],[87]. This could be attributed to a slight rotational misalignment between the two graphene layers as discussed below regarding the analysis of simulation results for pentalayer graphene ITFET. When we compare the same double bilayer graphene ITFET made in the previous batch (14X021) and this sample (15X035) as in Figure 3.8, we can note a clear difference in the characteristics, especially the NDR feature. Evidently, even with the same bilayer graphene used as the electrode layer and the same interlayer hBN thickness, the resonance peaks in 14X021 are much sharper than in 15X035. This we surmise to be due to a slight difference in the rotational alignment. It should be noted here that there is still the potential of misalignment when the sample or stamp is unintentionally shifted during the transfer process. In such cases, the straight edges of the graphene flakes are used to visually identify the rotational alignment. Under an optical microscope with a 10X objective, a misalignment of ~2 ° can be readily identified, which may be considered the maximum rotational misalignment.

Nevertheless, although the overall rotational alignment in 15X035 was less ideal than in previous devices, it is still safe to say that the rotational alignment between the bilayer, trilayer and pentalayer devices within the 15X035 batch would be the same since

they underwent the same transfer and device fabrication process. In Figure 3.7(b) for the differential conductance (dI_{INT}/dV_{TL}) versus V_{TL} plot, it can be noted that the step-like features of (a) show up as clear conductance peaks which correspond to conditions where the bands of the graphene layers would be aligned and resonant tunneling would occur. It is clear that an increase in the number of graphene layers results in a sharper peak (narrower width and higher intensity), as shown in the inset of Figure 3.7(b), where the width of the first resonance peak for each device extracted through a Lorentzian fit, is plotted against graphene layer thickness. The width Γ decreases from 295 mV for bilayer to 55 mV for pentalayer. This is an expected result from the increase in the density of states (DOS) for thicker graphene [11]. The increase in the DOS can be noted by the relative insensitivity of the characteristics with back gate bias (V_{BG}) for trilayer graphene compared to pentalayer graphene [Figure 3.9] and for bilayer graphene compared to quadlayer graphene [Figure 3.10]. When the V_{BG} is varied from -40 V to 40 V, the shift in the peak position for trilayer is 80 mV while the pentalayer characteristic is unchanged. This means that the DOS is large enough for pentalayer graphene that the series connection of the interlayer capacitance (C_{INT} in inset of Figure 3.7(a)) and quantum capacitance (C_Q) takes on a more dominant role in determining the characteristics of the device rather than the back gate capacitance (C_{BG}). Nevertheless, even with a sharper peak, with increase in the number of graphene layers, it is apparent that there is no NDR region in the characteristics for double trilayer and double pentalayer devices. It is highly probable that this is due to an increase in the number of sub-bands and decrease in the sub-band spacing for multilayer graphene which gives rise to an increase in closely spaced resonance conditions. It has recently been suggested that an increase in the number of sub-bands and decrease in sub-band spacing can result in a less prominent NDR peak [128].

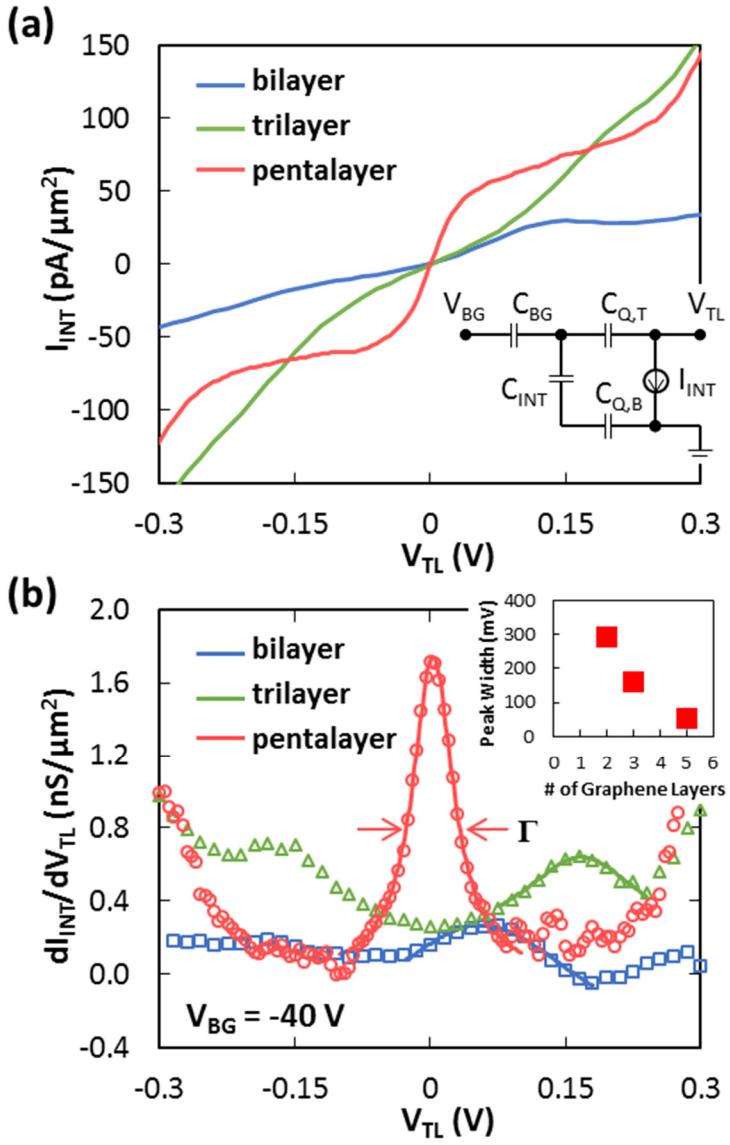

Figure 3.7 (a) Normalized current-voltage (I-V) characteristics at room temperature for double bilayer, trilayer, and pentalayer ITFETs sharing the same 5 atomic layer thick interlayer hBN. (b) The differential conductance (dI_{INT}/dV_{TL}) versus top layer bias (V_{TL}) of the same devices. The inset of (b) shows that with an increase in the number of graphene layers, the peak width decreases. Inset in (a) shows an equivalent circuit model of the device. Data is taken from sample 15X035.

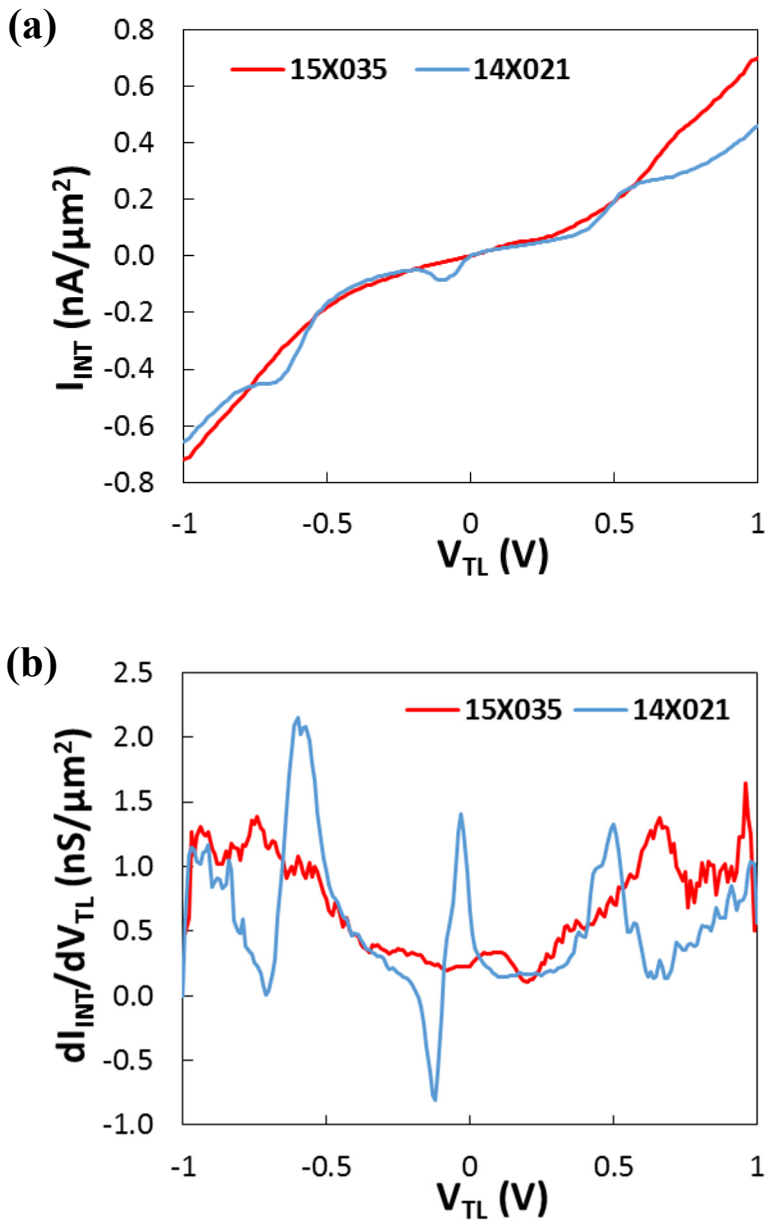

Figure 3.8 (a) Normalized I-V characteristics and (b) dI_{INT}/dV_{TL} characteristics at room temperature for two double bilayer ITFETs with presumably differing rotational alignment, 14X021 (blue) and 15X035 (red).

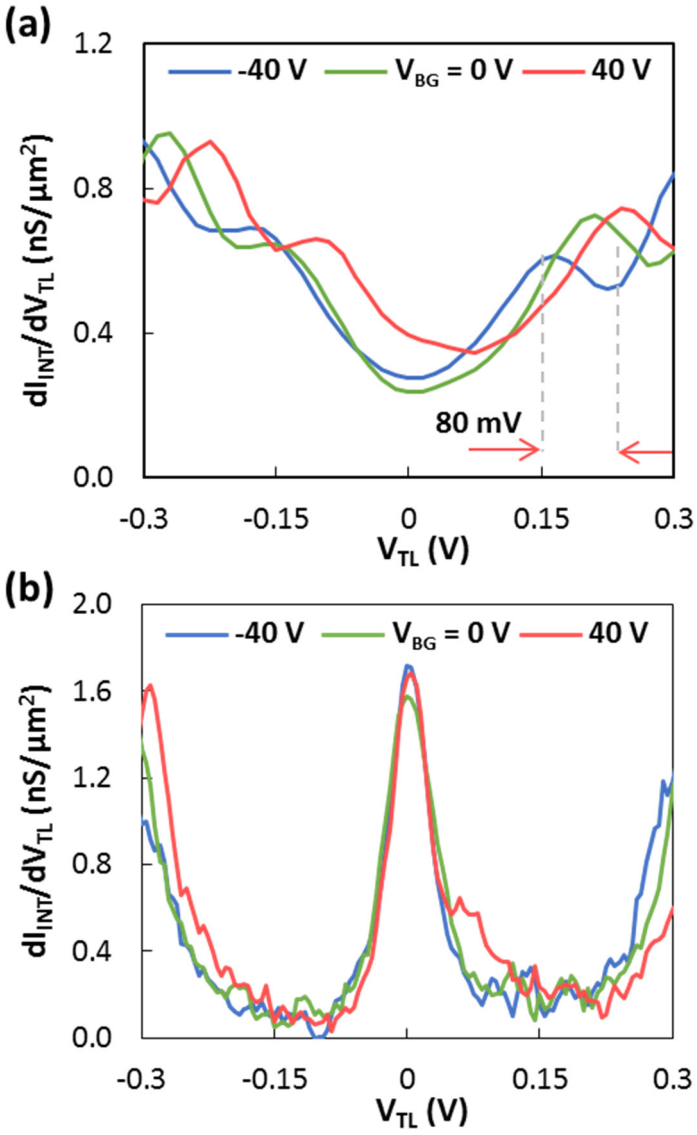

Figure 3.9 dI_{INT}/dV_{TL} as a function of V_{TL} for varying V_{BG} for (a) double trilayer and (b) double pentalayer. Data taken from sample 15X035.

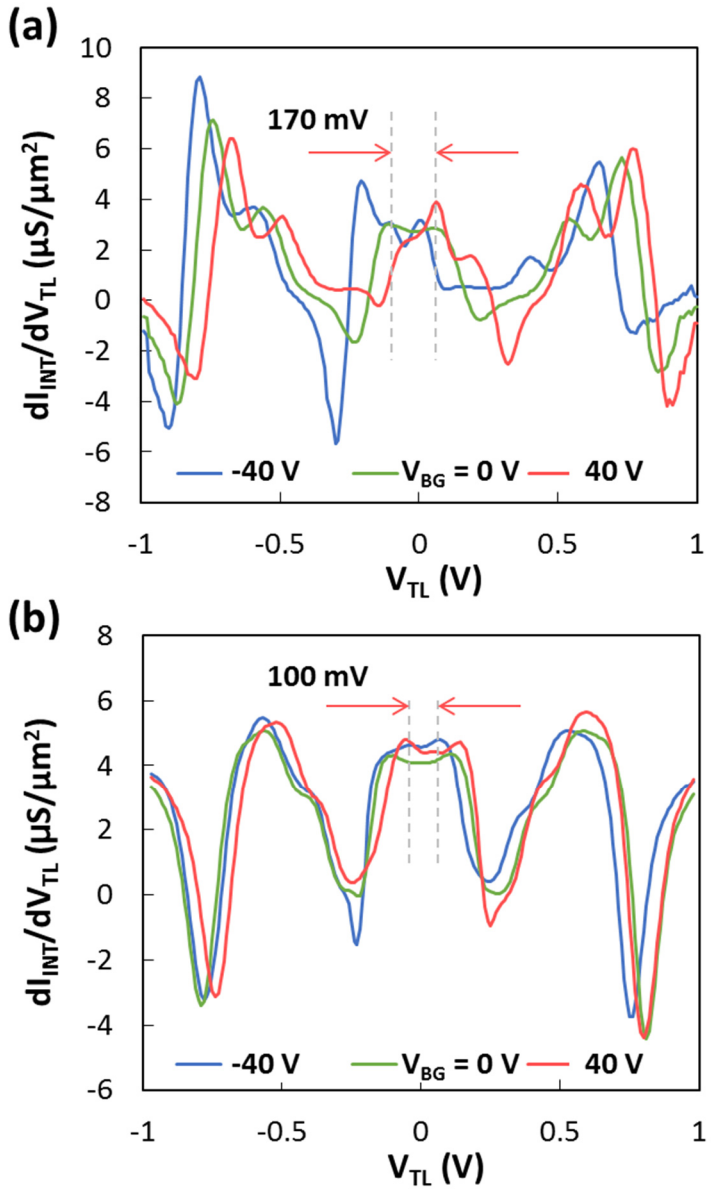

Figure 3.10 dI_{INT}/dV_{TL} as a function of V_{TL} for varying V_{BG} for (a) double bilayer and (b) double quadlayer ITFET. Data taken from samples 15X031 and 15X037, respectively.

3.3.2 Stacking Order Comparison

This phenomenon of decreasing sub-band spacing resulting in less prominent NDR, becomes more apparent when we compare the characteristics of double pentalayer graphene with differing stacking order, namely, Bernal-stacking versus rhombohedral-stacking, as is shown in Figure 3.11. Since Bernal-stacked pentalayer graphene has a Dirac cone band like monolayer graphene in addition to the four parabolic sub-bands, there are much more conditions when resonances can occur, as was shown for tunneling between monolayer graphene (Dirac cone) and bilayer graphene (two parabolic bands) separated by hBN [88]. It was shown that there will be more closely spaced resonance conditions than compared to devices with the same thickness for the two graphene electrode layers, due to the Dirac cone of the monolayer graphene and the two parabolic bands of the bilayer graphene making intersections at various biases. In other words, there will be many more resonance peaks for Bernal-stacked double pentalayer graphene due to additional resonance conditions established between the Dirac cone sub-band of one layer to the parabolic sub-bands of the other layer. Hence, the resonance peaks will be more closely spaced for Bernal-stacking, and therefore, interference effects for it will be more pronounced when compared to rhombohedral-stacking. This is evident in the dI_{INT}/dV_{TL} plot of Figure 3.11 where the valleys of the red curve (rhombohedral-stacking) are seen to be lower in intensity compared to the blue curve (Bernal-stacking), due to the slightly larger spacing between the first and second resonance peak. In our Bernal to rhombohedral-stacking comparison, we see that in the range of V_{TL} = -0.7 ~ 0.7 V, Bernal-stacking shows 10 distinguishable peaks while the rhombohedral case shows only 5 such peaks. It should be noted here that the two device did not have the same interlayer hBN thickness, with the Bernal-stacked device having three atomic layers while the rhombohedral-stacked device

had five. As shown in Figure 3.12, when two double bilayer graphene devices are fabricated in a single batch with different hBN thicknesses, we consistently observe that thinner hBN thickness results in resonance peaks that are more spaced apart with a lower valley in the differential conductance on either side of the first resonance peak. This is a result of the increase in the interlayer capacitance, as discussed by Kim et al. [104]. In other words, if the Bernal-stacked device had been fabricated with the same hBN thickness as that of the rhombohedral-stacked device, the resonance peaks would have been more closely spaced and the differential conductance valleys would have been even higher.

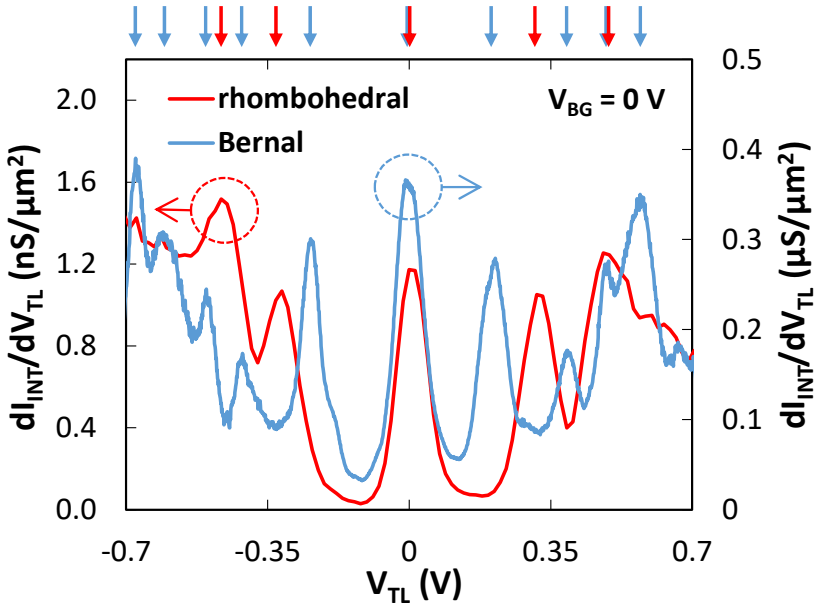

Figure 3.11 dI_{INT}/dV_{TL} comparison between Bernal-stacked (blue) and rhombohedral-stacked (red) pentalayer graphene ITFET. There are many more conductance peaks for the Bernal-stacked case. This is because odd-number of layer Bernal-stacked graphene has a Dirac cone sub-band which allow for more resonant tunneling conditions to be established with the parabolic bands of the other layer as described in [87] between monolayer and bilayer graphene. The first conductance valleys of the Bernal-stacked ITFET is higher due to the more closely spaced secondary resonance. Data taken from 15X017 and 15X035 for the Bernal- and rhombohedral-stack, respectively.

3.3.4 hBN Interlayer Tunnel Barrier Thickness

It is quite obvious that the hBN tunnel barrier thickness influences the tunneling current level. It has been known that the tunneling current level increases by about an order of magnitude to 1.5 order of magnitude with each decrease of one atomic layer of hBN. In Figure 3.13, we can see that there is a fairly consistent trend with hBN scaling [36],[56],[86],[104]. The same has been verified in our experiments with, for instance, a comparison between two atomic layers and six atomic layers of interlayer hBN. In Figure 3.12 we note that the difference in the current level is roughly five orders of magnitude for a difference of four atomic layers of hBN.

However, less obvious is the fact that depending on the interlayer hBN thickness, we observe a difference in the resonance peak width and also the peak position. More explicitly, the peak width increases and the peak positions tend to shift to higher interlayer voltages when the thickness is scaled down, as is evident in the plots of Figure 3.12. Here, a scaling of the hBN layer by 4 atomic layers results in a shift in the secondary resonance peaks by as much as 150 mV. This is due to the interplay between the finite quantum capacitance of bilayer graphene versus the increasing interlayer capacitance of the dielectric with scaling down of the thickness [104]. At the secondary resonance, the electrostatic potential difference between the two layers would be fixed at V_{ES} = 0.4 V. When the hBN is scaled down and the interlayer capacitance increases, this brings about an increase in the carrier density ($Q = C \cdot V$) which appears as an increase in the chemical potential of the bilayer graphene. Since the external bias V_{TL} is a sum of the potential difference and layer chemical potential, a higher V_{TL} is required for the secondary resonance to occur. The same argument can be given for the case of resonance peak broadening with hBN scaling.

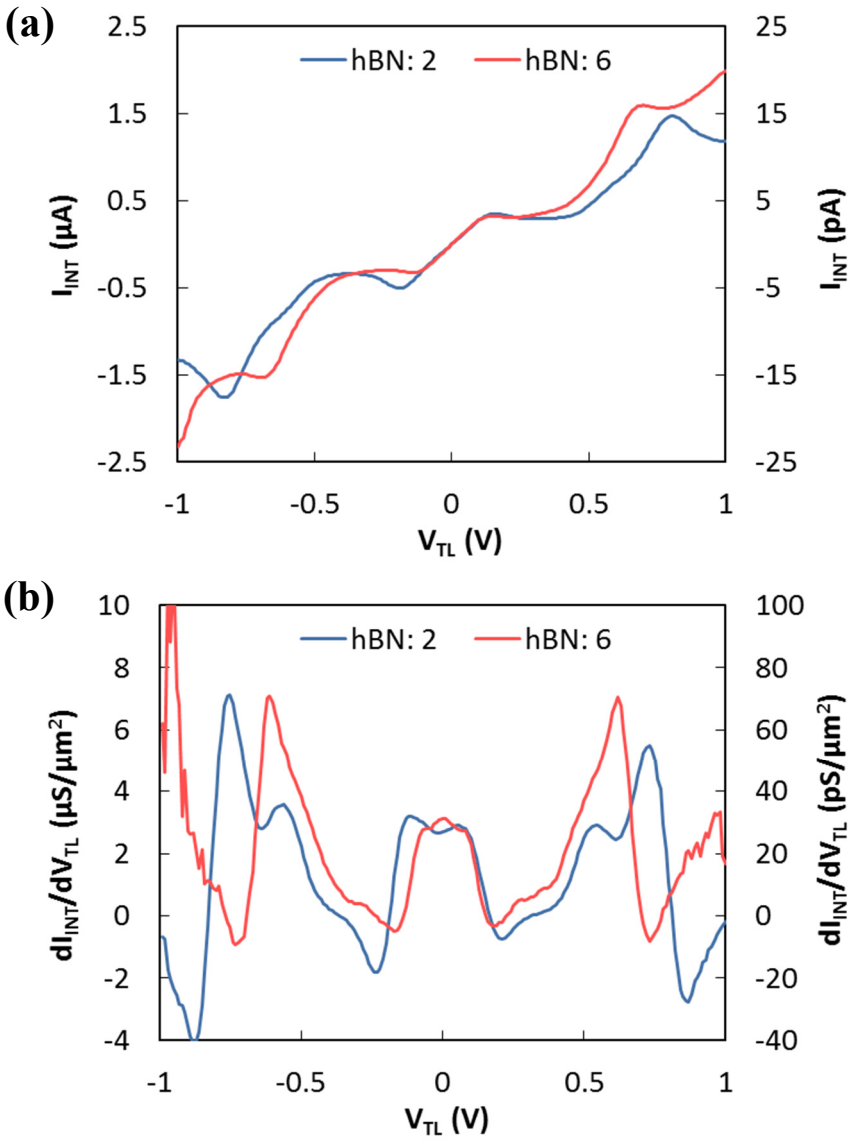

Figure 3.12 (a) I-V characteristics and (b) dI_{INT}/dV_{TL} characteristics at room temperature for a double bilayer graphene ITFET with two atomic layers of interlayer hBN (blue) and six atomic layers of interlayer hBN (red). Data taken from 15X031.

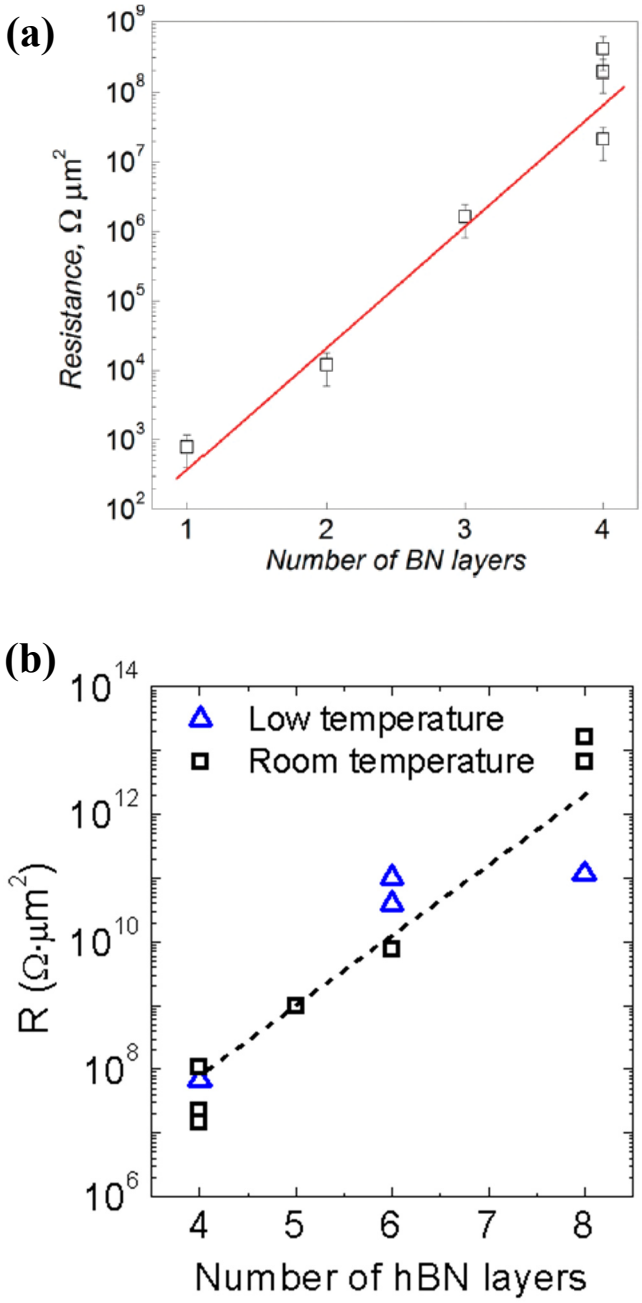

Figure 3.13 Tunneling resistance dependence on interlayer hBN thickness for (a) non-resonant tunneling (adapted from [86]) and (b) resonant tunneling (adapted from [56]).

At the extreme of monolayer interlayer hBN, we observe peculiar behavior which still remains to be explained. The resonance peak position seems to depend on the contact resistance. This was first revealed when the sample was wire-bonded and the peak position of the first resonance shifted from 0.25 V to 0.7 V. Furthermore, when the temperature was decreased from 250 K down to 2 K the peak position again shifted from 0.7 V to 1.0 V. When different contacts with different contact resistance to the top and bottom graphene were used for the interlayer current-voltage measurement, the peak position shifted by as much as 0.2 V. We surmise based on these results that for monolayer hBN the total interlayer current may not be limited by the interlayer tunnel barrier but rather the contacts or the top and bottom graphene access regions leading to the overlap region. In other words, this may be a result of a different phenomenon than what has been observed for other ITFETs.

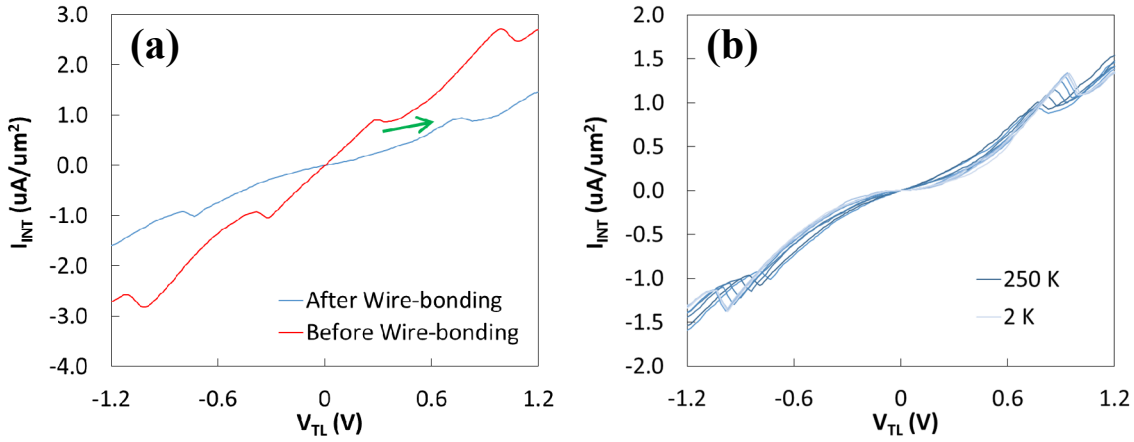

Figure 3.14 Interlayer current-voltage characteristic comparison (a) before and after wire-bonding and (b) as a function of temperature. Factors that lead to increase in contact resistance tends to result in an outward shift of the peaks. Data taken from 15X034.

3.3.3. Even-Number-of-Layer Graphene

In Figure 3.15, we compare the characteristics of a double bilayer graphene with that of a double quadlayer ITFET. Though the devices were fabricated separately, they had the same interlayer hBN tunnel barrier thickness of two atomic layers yielding currents on the order ot $\mu A/\mu m^2$. The band structure of even number of layer graphene does not exhibit a Dirac cone regardless of the stacking order [114],[129]. Therefore, additional resonance conditions that arise from the tunneling between the distinct linear and parabolic bands are absent. As a result, we expect fewer resonance conditions, less interference, and hence improved NDR characteristics. As can be noted from the figures, this is indeed the case where we can see clear NDR features in the I-V characteristics. Further, the double quadlayer device exhibits a significant NDR comparable to that of double bilayer device. As expected, the double quadlayer device has an enhanced resonance due to its higher DOS. This is evident from Figure. 3.15(b) where the normalized peak intensity of the first resonance is larger than that of the double bilayer device. However, due to the smaller spacing from the first sub-band to the second sub-band for quad-layer graphene ($0.6\ \gamma_1$) compared to bilayer graphene ($\gamma_1 = 0.4$ eV), the secondary resonance peaks occur closer to the first peak, which, in turn, acts to increase the intensity of the valleys adjacent to the first peak, and prohibits the device from having a larger PVCR. In other words, the second resonance interferes with the first resonance.

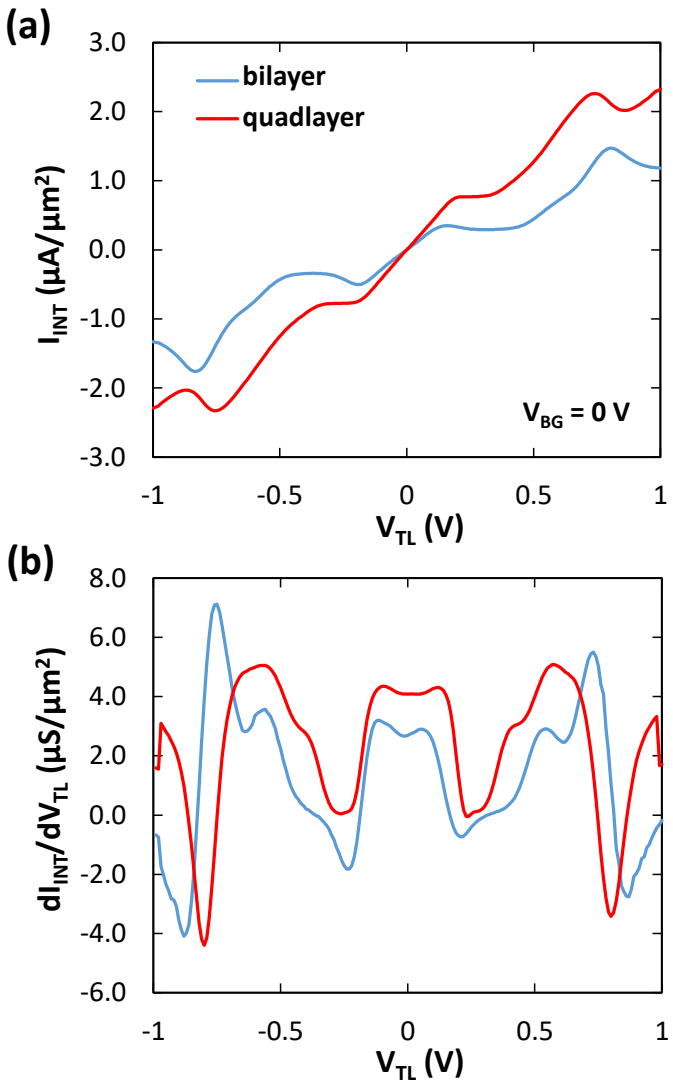

Figure 3.15 (a) I-V characteristics at room temperature of double bilayer (blue) and double quadlayer (red) ITFETs with the same hBN thickness of 2 atomic layers but made separately. Clear NDR peaks occurring at regular intervals can be noted. (b) The differential conductance for the same devices. The first resonance peak of the double quadlayer device shows slightly higher differential conductance but the first resonance valley is less pronounced compared to the double bilayer device. This is a result of the secondary peaks occurring at a slightly lower bias for double quadlayers compared to double bilayers due to the smaller separation of sub-bands. The smaller separation of peaks means that the resonance of one interferes with the other and makes them less prominent. Data taken from 15X031 and 15X037 for bilayer and quadlayer, respectively.

3.4 SIMULATIONS

To corroborate the measurements with theory, we compute the tunneling currents using a Bardeen transfer Hamiltonian approach, following [83] and [82]. The tunneling current is obtained by carrying a probability weighted sum of the transition rates ($M_{\alpha\beta}$) between all the states ($\alpha,\ \beta$) between the top-layer and the bottom-layer, i.e.,

$$I = \left(\frac{A}{L_{ch}^2}\right)\left(\frac{8\pi e}{\hbar}\right)\sum_{\alpha,\beta}\left|M_{\alpha\beta}\right|^2\left(f_{TL}(E_\alpha) - f_{BL}(E_\beta)\right)\delta(E_\alpha - E_\beta) \quad (Equation\ 3.1)$$

where f_{TL} and f_{BL} are Fermi distribution functions of the top and the bottom layers, respectively. L_{ch} is the coherence length of an electron, A is the total overlap area between the top and bottom layers. The transition rates are computed by estimating the overlap integral of the wavefunctions in the top and the bottom layers (ψ_α and ψ_β, respectively) i.e.,

$$M_{\alpha\beta} = \frac{\hbar^2}{2m}\int dS\left(\psi_\alpha^*\frac{d\psi_\beta}{dz} - \psi_\beta^*\frac{d\psi_\alpha}{dz}\right) \quad (Equation\ 3.2)$$

where the integral is carried out over an area of L_{ch}^2. A finite coherence length of the electron $L_{ch} < \sqrt{A}$ accounts for further resonance broadening observed in the measurements. $M_{\alpha\beta}$ is further simplified following the formalism in [82].

To compute the tunneling currents, band structure for Bernal-stacked bilayer and quadlayer are obtained using a tight-binding formalism, with a band-gap that opens up in the presence of transverse electric fields across the bi/quad layer [21],[130]. And, in the

case of mono/tri/penta layer graphenes, the band structure is approximated using a combination of linear and parabolic bands [114].

The charging of the top and bottom layers are taken into account while estimating the electrostatic potentials (ϕ_{TL} and ϕ_{BL}, respectively) in both layers needed to compute the tunneling currents. This is done by solving the following coupled non-linear equations,

$$C_{BG}(V_{BG} - \phi_{BL}) + C_{INT}(\phi_{TL} - \phi_{BL}) + Q_{BL}(\phi_{BL}, V_{BL}) = 0 \quad (Equation\ 3.3)$$

$$C_{INT}(\phi_{BL} - \phi_{TL}) + Q_{TL}(\phi_{TL}, V_{TL}) = 0. \quad (Equation\ 3.4)$$

Here, C_{BG} (C_{INT}) is the bottom gate (interlayer) capacitance, $Q_{TL}(\phi_{TL}, V_{TL})$ and $Q_{BL}(\phi_{BL}, V_{BL})$ are the charges accumulated on the top and the bottom layers of the ITFET, due to the finite DOS, determined by assuming a Fermi distribution of carriers.

Using this model, we have calculated the dI_{INT}/dV_{TL} characteristics of a device with double Bernal-stacked pentalayer graphene structure. In Figure 3.16(a), individual components from the tunneling between like-bands (middle curve) and between that of the unlike-bands (bottom curve) are plotted with the measurement result (top curve). It can be noted from the plot that the positions of the resonance peaks match very well with that obtained for the measurements. It is clear that the broad NDR regions occurring on either side of the first resonance peak at roughly $V_{TL} = \pm 0.12 \sim 0.4$ V which results from the like-band tunneling, is dampened out by the unlike-band tunneling which happens to occur in the same range of V_{TL}. This confirms our previous argument that odd number of layer Bernal-stacked graphene is not suited for obtaining high PVCR NDR characteristics. One discrepancy between measurement and simulation is the peak width resulting from the unlike-band tunneling. This could be explained by a discrepancy in the assumed rotational alignment. In our simulations, we assumed perfect rotational alignment between the top

and bottom graphene layers. The tunneling current between a Dirac cone and the parabolic bands in the twisted structure displays a much richer behavior analogous to the study done by [88]. Therefore, we surmise that an unintentional slight rotational mis-alignment during fabrication might have been the cause for the sharper, and many more peaks resulting from unlike-band tunneling relative to the simulations. This is also in line with the less prominent NDR for double bilayer device compared to previously reported results [56],[87], that was transferred and fabricated simultaneously with the pentalayer device.

Calculations were also carried out for the double bilayer and double quadlayer case which results are shown in Figure 3.17(b,c) overlaid onto the measurement results. It can be noted from the figures that the overall peak positions obtained through our model agree well with measurements. The broadening of the peaks observed for the secondary peaks at high V_{TL} is also evident in the simulations. From the model results, we note that the broadening of the peaks is actually a result of there being multiple sub-peaks. This splitting of the secondary peak is because of a band gap opening at the Dirac point due to the presence of transverse electric fields [21],[130]. However, the band gap opening around $V_{TL} = 0$ due to the applied fields is close to zero, and cannot account for the flatness in the resonance around $V_{TL} = 0$. We surmise that this may be a signature of a non-resonant tunneling mechanism [89] or because of a contact issue.

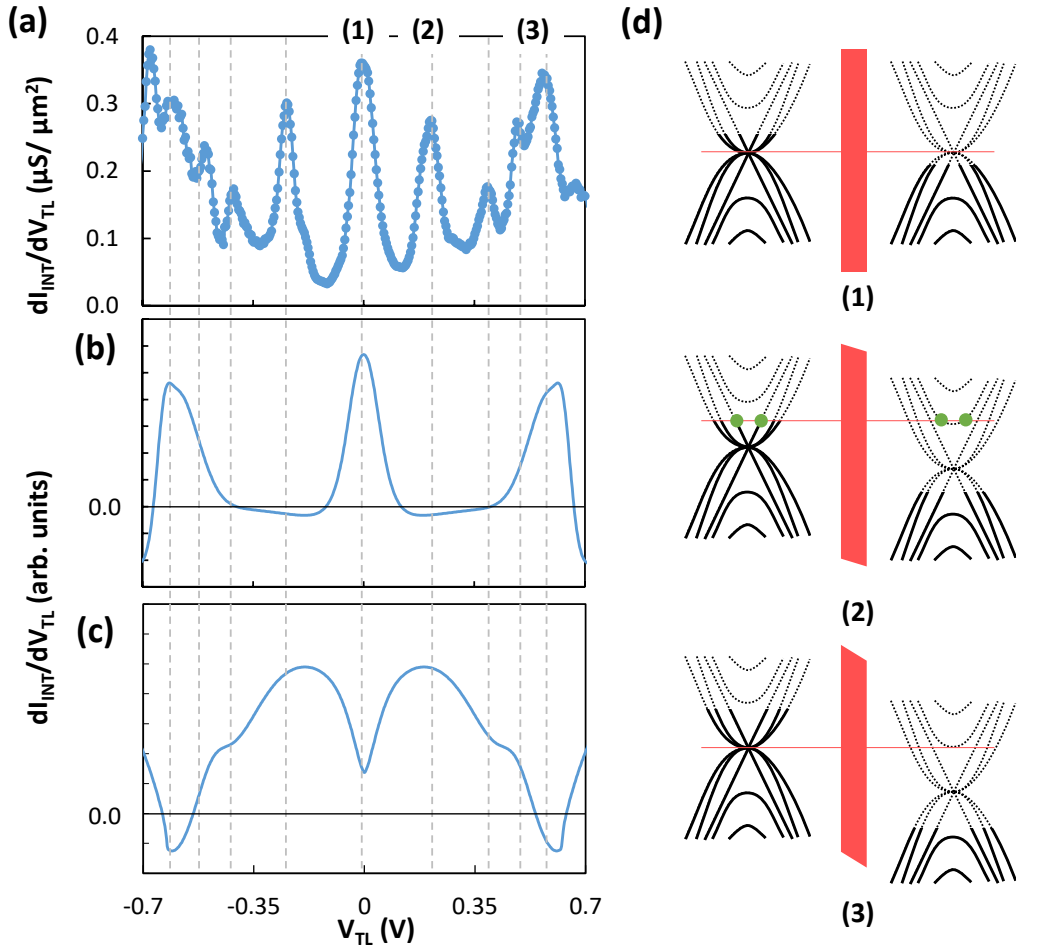

Figure 3.16 (a) Measurement result for a double Bernal-stacked pentalayer device. Data taken from 15X017. Simulation result for dI_{INT}/dV_{TL} of the same structure caused by (b) tunneling between like-bands and by (c) tunneling between the unlike-bands. Peak positions observed in the measurement result match well with the simulation results. (d) Band diagrams for cases (1-3) in (a), where solid lines represent filled bands and dotted lines empty ones.

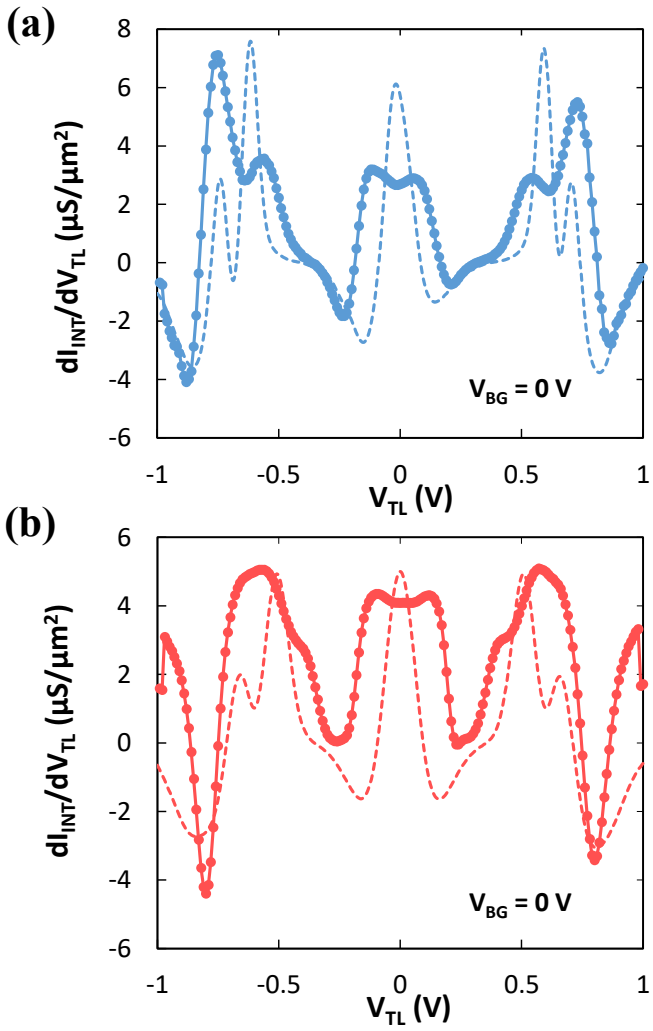

Figure 3.17 Comparison of measurement (symbols) and simulation (dotted line) for (a) double bilayer and (b) double quadlayer devices. The peak positions and peak broadening at high V_{TL} are well reproduced through simulation assuming a linear band gap opening with vertical electric field. Measurement data taken from 15X031 and 15X037 for bilayer and quadlayer, respectively.

3.5 BENCHMARKING

The performance of ITFETs in circuits is critical for beyond-CMOS logic applications. While the task of determining the numbers and the widths of the resonance peaks is complicated by the bandstructures of multilayer graphene, the strongest resonance peak, occurring with fully aligned bands of graphene multilayers and usually smaller gate/interlayer voltage combinations, is the main focus in low-power circuit applications. Our semi-quantitative compact model [131] shares the same components as indicated in the quantum simulations, with I_{INT} capturing only the main resonance peak by a linear leakage resistance in parallel with a Lorentzian-broadened resonance peak. The details of the SPICE circuit simulations are presented elsewhere [131]. These simulations show that, in the presence of the increasing leakage currents with increasing V_{TL}, a clock amplitude of 5~6 times the half-width of the resonance peaks is optimal for the performance of ITFETs in logic circuits. In terms of the g_{ON}/g_{OFF} ratio, namely the ratio between the slope of the resonance current peak and the slope of the background current, for which the PVCR is a good metric, it should be at least 5 for the simple gates such as inverters, and above 20 for complex gates such as NAND and NOR gates [Figure 3.18]. The 27.5 mV half-width of the resonance peak for graphene pentalayers, as illustrated in Figure 3.7(b), would allow energy consumption on the order of aJ per ITFET per clock-cycle, assuming nanoscale devices and GHz clock frequency. Consequently, with sharper resonance peaks, reducing the background leakage current should be the next step for improved g_{ON}/g_{OFF} ratio and, in turn, low-power operations.

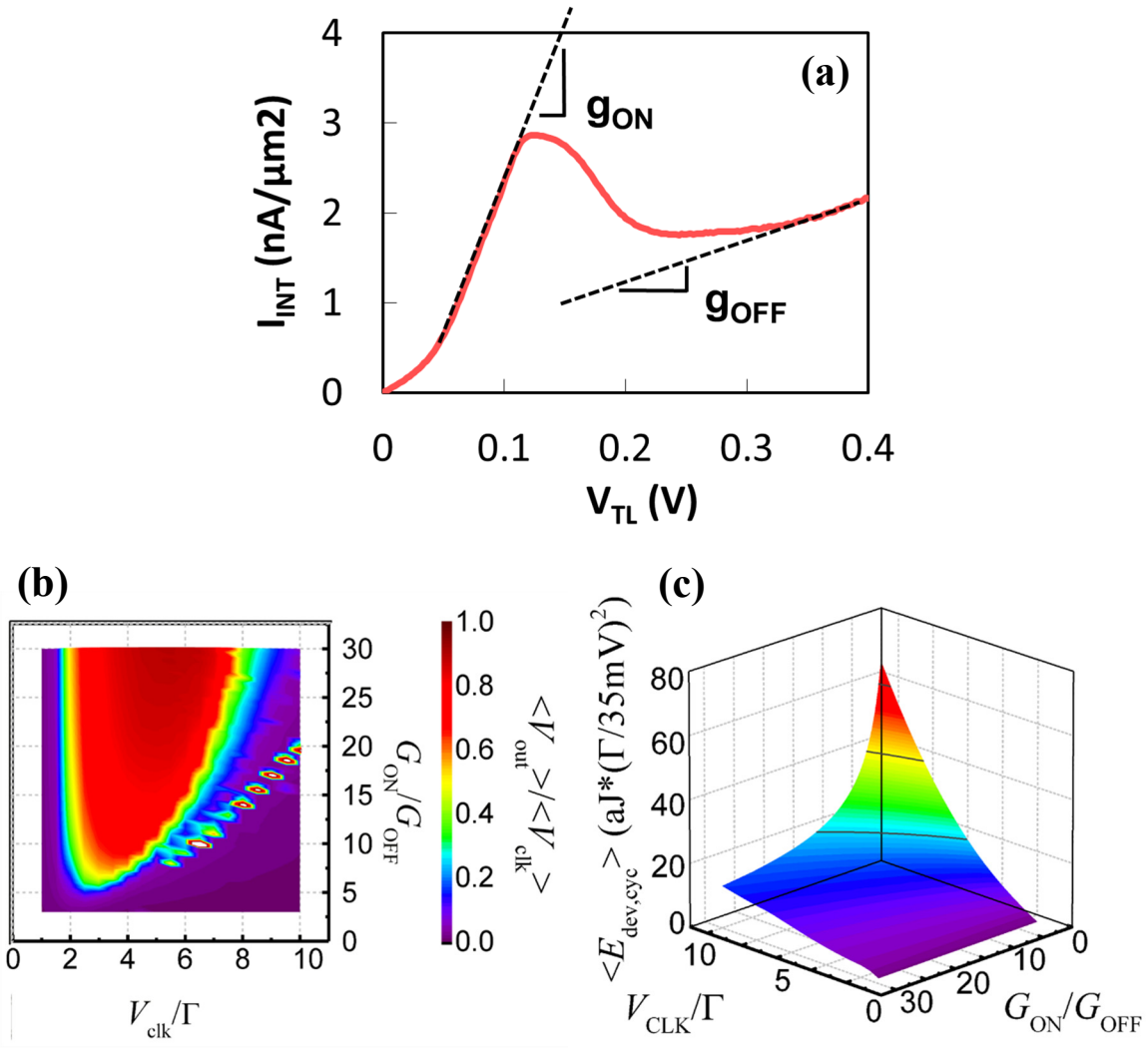

Figure 3.18 (a) Definition of g_{ON} and g_{OFF} in terms of the I_{INT}-V_{TL} characteristic of the ITFET. (b) g_{ON}/g_{OFF} ratio versus clock voltage plot showing where the device metric has to be in order for signal restoration. (c) Energy consumption per cycle as a function of g_{ON}/g_{OFF} and clock voltage. Higher g_{ON}/g_{OFF} is desirable for reduced energy. (b,c) are adapted from [131].

3.6 SUMMARY

In summary, we have explored various combinations of graphene and interlayer hBN thicknesses in order to experimentally study the effects of electrode layer band structure on the characteristics of ITFETs. Although an increase in the number of graphene layer does bring about an enhanced resonance stemming from increased DOS, due to an increase in the number of sub-bands and a decrease in the spacing between the sub-bands, the sharper resonance is dampened by closely spaced adjacent resonance peaks, inhibiting the device from attaining higher PVCR values. Especially, when using an odd number of layer graphene with Bernal-stacking, which has a Dirac cone band in addition to the parabolic bands, the number of resonance conditions radically increase causing further interference with the main resonance peaks. This is not the case for even number of layer graphene, which does not have a Dirac cone regardless of the stacking order, and therefore we are able to observe NDR. However, in this case also, the sharper resonance brought about by the increase in DOS is countered by the decrease in the sub-band spacing between parabolic sub-bands, limiting the PVCR. Also, for even number of layer graphene, band gap opening effects, which tend to split and broaden out the resonance peaks at high fields should also be taken into consideration. Moreover, we find that the increase in the DOS with the increase in the number of graphene layers, increases the influence of the interlayer capacitance on the device characteristics and decreases that of the external gate capacitances. In others words, the gate tunability is somewhat diminished. We suggest that the use of a material with an optimized DOS, minimal number of sub-bands or largely spaced sub-bands, and no change in the band structure as a function of applied bias would be advantageous in terms of implementing ITFETs with improved performance (higher PVCR) at low operating voltages. While the various TMD materials do have closely spaced

sub-bands, especially for multilayers [132], we do not think that they would influence ITFET performance due to the high DOS at the band edge, and as a result, the sub-bands not being able to be populated during normal operation [132],[133],[134]. We consider various TMDs to be favorable in terms of ITFET implementation. Remaining challenges are obtaining large enough TMD flakes to which the above fabrication method can be applied, obtaining high quality flakes which eliminates the band tail states [95], and finally, establishing low resistance, stable contacts to the TMD layers.

CHAPTER 4: Conclusion

4.1 SUMMARY

In this dissertation, an interlayer tunnel FET (ITFET) was demonstrated with a double bilayer graphene and hBN heterostructure [87]. Significant negative differential resistance (NDR) in the interlayer current-voltage characteristic was demonstrated at room temperature. Through electrostatic analysis, it was shown that the NDR was due to energetic band alignment between the top and bottom bilayer graphene. Additional NDR features at higher bias points were shown to be due to band alignment between the bottom sub-band of one layer to the top sub-band of the other layer. Temperature dependent and parallel magnetic field measurements were taken to further confirm that the conduction mechanism was momentum and energy conserving resonant tunneling. The NDR feature was used to demonstrate a one transistor static random access memory (SRAM) element operating a room temperature.

Improvements in the layer transfer method, which allowed rotationally aligned top and bottom electrode layers, made possible extensive experimental studies of 2D heterostructure based ITFETs. Utilizing such technique, we conducted experiments involving thicker multilayer graphene electrode layers [135]. It was shown that with an increase in graphene electrode layer thickness, the density of state (DOS) increase would bring about a significantly sharper resonance peak. However, at the same time, due to the same reason, the gate controllability of the NDR characteristic was shown to decline with increase in thickness. Moreover, due to the more complex band structure for multilayer graphene, there would be an increase in the number of bias points where band alignment

between the various sub-bands could occur and therefor, an increase in the number of peaks for a given bias range. This results in interference between the resonance peaks which tends to diminish the negative differential region. This was proven to be more so when multilayer graphene with odd number of layer and Bernal-stacking was used. This was due to the Dirac cone sub-bands within these graphene that caused an even more pronounced increase in the number of resonance conditions. Even number of layer graphene does not have the Dirac cone as a sub-band and as a result shows quite clear NDR features. Nevertheless, even number of layer graphene shows problems such as band gap opening and band distortion effects at high electric-field which tend to broaden the resonance peaks. The effects of interlayer hBN scaling was also briefly dealt with. It was noted that the current level increases by greater than one order of magnitude for each atomic layer decrease in the hBN tunnel barrier thickness. In addition, it was shown that the resonance peak width broadens and spacing between resonance peaks tend to widen when the hBN thickness is scaled down. It was argued that this was due to the interplay between the interlayer capacitance from the hBN layer and the quantum capacitance of the graphene layers. Simulations based on Bardeen transfer Hamiltonian approach were conducted for these devices, and it was shown that the peak positions predicted by theory matched well with those obtained through measurements.

4.2 Future Work

The bilayer pseudo-spin field-effect transistor (BiSFET) is based on the pairing of electrons in one layer to the holes in the other layer to form a Bose-Einstein condensate (BEC) in closely spaced double semiconductor system [136]. This still remains a highly

desirable device with possibilities of ultra-low power consumption [Figure 4.1]. In this regard, exploration of signatures of the BEC in a double multilayer graphene system seems to be a worthwhile effort with some groups recently claiming experimental demonstration of such in double bilayer graphene and hBN heterostructures [137],[138]. Another interesting device that might serve as an extension or improvement to the ITFET is the multi-barrier ITFET similar to what has been suggested for III-V semiconductor stacks (resonant injection enhanced field-effect transistor: RIEFET) [139]. Stacking multiple graphene and hBN layers to make multiple tunnel barriers, the device may show sharper resonance peaks than what we have demonstrated for the double barrier ITFET.

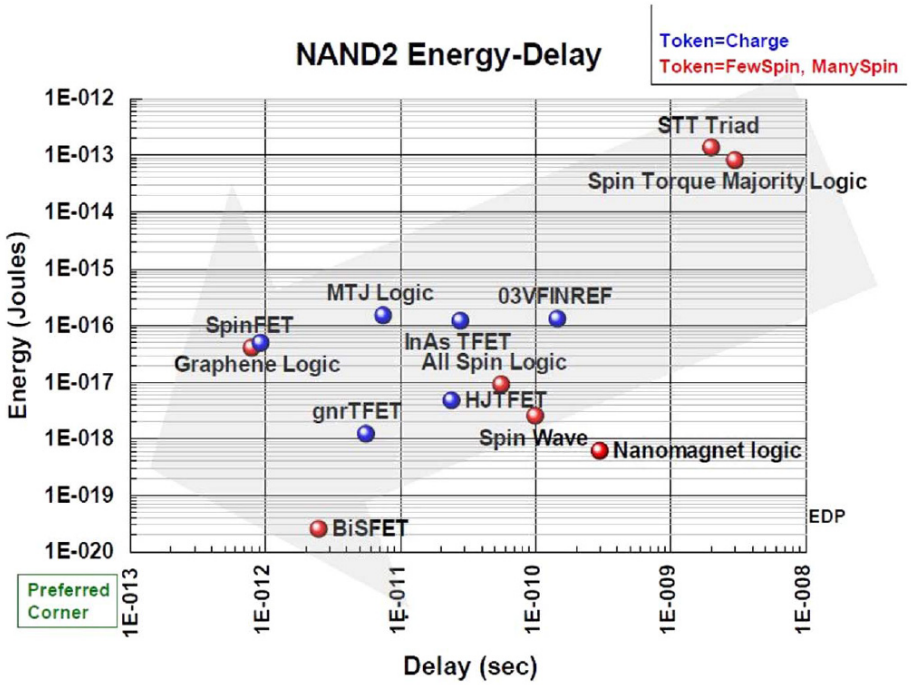

Figure 4.1 Energy-delay of a two-input NAND gate for implementations based on various beyond-CMOS device concepts. The BiSFET stands out for its promise of ultra-low power consumption, unmatched by other devices. Adapted from [140].

4.2.1 BiSFET with Double ABC-Stacked Multilayer Graphene

ABC(rhombohedral)-stacked graphene has a divergent DOS caused by van Hove singularity at the band bottom [Figure 4.2] [117] which is expected to be more conducive for observing the BEC in graphene and hBN heterostructures [141]. It was predicted that with ABC-stacked trilayer or quadlayer graphene, the enhanced electron-hole superfluidity would be observable at temperatures of up to 40 K at carrier densities as high as 10^{12} cm^{-2} [141]. Several experimental studies have been conducted to probe the properties of ABC-stacked multilayer graphene, and in particular, the high DOS of ABC-stacked multilayer graphene has been confirmed through experiments [Figure 4.2] [117],[120]. Although some reports show that the stacking order of graphene does not easily change with fabrication processing, little is known of what effects the various dry transfer methods employed for heterostructure formation has on the stacking order. It is still possible that the stacking order can abruptly change from ABC to ABA(Bernal)-stacking through strain induced during the transfer process and unexpected high temperature processing such as resist heating through electron beam lithography [107][142]. Also, considering the fact that forces from adhesion, friction, strain, and capillary action become important at the nanoscale, and that the energy barrier to changing stacking order is about 3 meV/atom [26], it is certainly possible for the stacking order to change. It has even been shown that the stacking order can be dynamically and intentionally adjusted using a vertical electrical field applied through an AFM tip [143]. Hence, we must ensure that the stacking order be preserved throughout the fabrication process. The method used for ITFET fabrication makes it very difficult to monitor the Raman signature of stacking order once the whole stack has been made through the stamp-and-stack transfer process. This is because the thick hBN beneath or above the graphene layers tends to modify the distinct Raman signatures

for different graphene stacking order [144]. Also, because graphene cannot be independently picked up with the polymer stamp and always requires an hBN layer on top [57], one can only make one dimensional contacts to the graphene. For mono-layer graphene it was shown that this results in improved contact resistance [57], but for multilayer graphene, several attempts have shown that the contacts are not good enough for low temperature lock-in measurements. Moreover, initial attempts for making these devices using the conventional stamp-and-stack transfer method used for ITFET fabrication has shown spurious Dirac points occurring at random voltages. We surmise this to be due to the random formation of air bubbles at the hetero-interfaces of graphene and hBN. For ITFETs, air bubbles do not significantly hinder the characterization of the device since it only has the effect of locally increased dielectric thickness, and if there is sufficient area of a bubble-free region, tunneling will occur and that current will dominate the overall characteristics. However, such air bubbles make analysis of the intralayer characterization and Coulomb drag results very difficult if not impossible [Figure 4.3]. Using a layer-by-layer transfer method it should be possible to make stable two-dimensional contacts to graphene, monitor the stacking order during processing, and also identify bubble free regions through AFM and make devices in these regions or conduct vacuum anneals in-between each transfer step to reduce the amount of residue that can get trapped and form such bubbles.

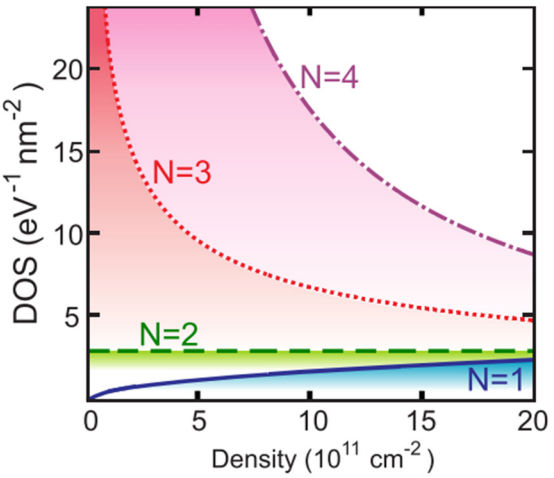

Figure 4.2 DOS for different number of layer graphene. Monolayer graphene has a vanishing DOS at low density while bilayer has a constant DOS. ABC-stacked tri and quad layer graphene has a divergent DOS at low density. This is expected to be more conducive for observing electron-hole pair superfluidity. Adapted from [141].

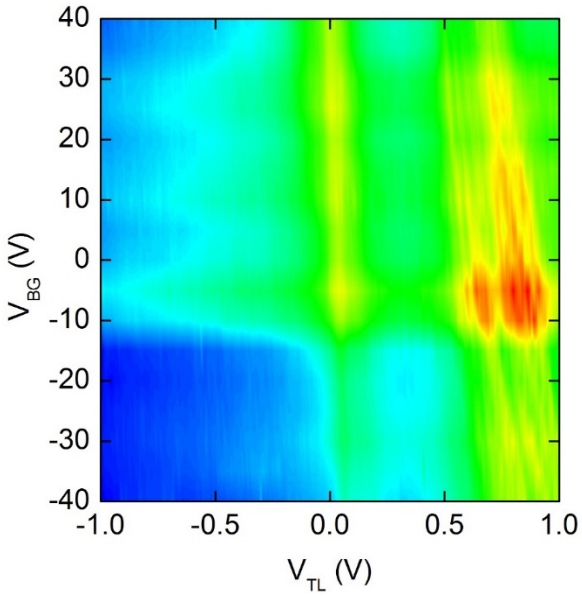

Figure 4.3 Contour plot of the top layer of a double ABC-stacked trilayer and hBN heterostructure fabricated using the stamp-and-stack transfer method.

4.2.2 Multi-Barrier ITFET

Resonant injection enhanced field-effect transistor (RIEFET) was first proposed as a device that could be implemented with a stack of MBE grown III-V compound semiconductor materials with multiple 2DEGs separated by multiple tunnel barriers [139]. When the device is in the ON state, the barriers would be transparent to electron flow through resonant tunneling acting as a kind of high-order band-pass filter. In the OFF state, the resonance path is eliminated and the current is cut-off. Various geometries were suggested for this device, which all seem implementable with the current state-of-the-art rotationally aligned 2D flake transfer technique.

4.2.3 Rotationally Aligned hBN Tunnel Barrier

It has been suggested that the rotational alignment of the interlayer hBN tunnel barrier to the respective graphene electrode layers may also influence the ITFET performance [145]. While the rotational alignment between the two graphene electrode layers has become quite straightforward with the introduction of a new transfer method [104], the alignment of the interlayer hBN tunnel barrier to the graphene layers is not as uncomplicated. However, as there are methods to determine the twist angle between monolayer or bilayer graphene with hBN in a graphene on hBN stack through Raman spectroscopy [103],[146], one may be able to implement such a device with a cleverly devised experimental setup.

Appendices

APPENDIX A: INFLUENCE OF ELECTRON BEAM LITHOGRAPHY ON THE TRANSPORT PROPERTIES OF GRAPHENE FIELD-EFFECT TRANSISTORS

A.1 Introduction

The potential for using high mobility graphene channel field-effect transistors (FETs) [7] for high-frequency applications has driven an immense amount of research in the field [12]. However, in reality, many factors limit the mobilities that can be practically obtained. Without addressing these issues, the potential advantages of employing graphene may be greatly reduced. Several of these factors that degrade the electrical transport characteristics, especially the carrier mobility, of graphene FETs have been identified. These include the type of substrate that is used, condition of the substrate in terms of physical corrugations and charged impurities, other extraneous impurities, and polymer residues introduced during the fabrication process. Techniques such as using ultra-smooth hexagonal boron-nitride (hBN) as a substrate material [35], removing the substrate to obtain suspended structures [147], pre-exfoliation surface treatment of the substrate [58], post-fabrication annealing [40],[148], and chemical treatment of the device [65] have all been shown to be effective in mitigating these effects. In addition to these factors, some have reported that the electron-beam lithography (EBL) process, which is commonly used to pattern the graphene active region and source/drain contacts, has a negative impact on the electrical characteristics of the device [149],[150],[151]. Several studies have been conducted to investigate the effect of electron beam irradiation on mobility

[152],[153],[154],[155]. Some have argued that irradiation of the device after fabrication causes defects in the graphene lattice, which shows up as an increase in the Raman D-peak intensity, and a consequent degradation of the mobility [152]. They also showed that this degradation becomes more severe with an increase in the cumulative exposure dose [152],[153]. However, more recently, it has been pointed out that crystalline defects cannot be the cause of degradation when the EBL acceleration voltage is too low to generate defects [155]. Instead, they argued that degradation could be due to hydrogen containing radicals that are generated by a depolymerization of the poly-methyl-methacrylate (PMMA) resist layer when the device is subjected to EBL processes. It was suggested that these radicals cause hydrogenation of graphene, resulting in device degradation. However, all of these prior reports considered direct bombardment of electrons onto the channel region and examined the effects thereof. This is not representative of EBL employed for device fabrication, since in the latter case, the channel region is not directly bombarded, but rather areas of the graphene where it is ultimately removed through plasma etching. Hence, we argue that the experimental setups used in these previous studies are insufficient for explaining the effects of EBL on device characteristics. In this report, we show that even for EBL exposure energies that are low enough (< 80 keV) to not directly displace carbon atoms from the graphene lattice [156], and for electron beams not directly targeted on the channel region, EBL can still cause degradation in the mobility. We give evidence that this degradation is indeed caused by resist depolymerization, and that the extent of depolymerization is dependent on the level of resist heating, which, in turn, is dependent on the EBL current level. This heating, which is greater for higher exposure currents, causes the PMMA to more readily generate radicals that get trapped between the graphene and resist interface. Electrical measurements and model fitting [157] reveal that a lower exposure current results in higher mobility, decreased variation in the charge neutrality

point (CNP), and lower residual carrier density (RCD). By controlling the exposure current level used during the EBL patterning, we were able to obtain very high mobility in excess of 18,000 $cm^2/V{\cdot}s$, approaching the reported record for graphene on a silicon dioxide (SiO_2) substrate [33].

A.2 Methods

The process flow and specific conditions used for the fabrication of the devices used in this study are as follows. A 280 nm SiO_2 layer is grown by means of dry thermal oxidation on a degenerately doped n-type Si (100) wafer. The highly doped silicon substrate functions as the back gate for the final graphene FET. Monolayer graphene flakes are then prepared by mechanical exfoliation from graphite crystals onto this substrate and verified using a combination of optical contrast, and Raman spectroscopy. A resist layer of poly-methyl-methacrylate (PMMA, 950K 6 % dissolved in anisole, supplied by MicroChem corp.) is spin-coated at a rate of 4000 rpm for 60 s to obtain a 470 nm film, and is subsequently baked at 140 °C for 120 s to remove any residual solvent. EBL is performed using a Zeiss Neon 40 scanning electron microscope (SEM) equipped with a Raith Elphy Quantum Pattern Generator system with the exposure current ranging from 10 pA to 125 pA, while keeping the energy, dose, and step size fixed at 20 keV, 320 $\mu C/cm^2$ and 4 nm, respectively. The resist is then developed in a 1:3 solution of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA) for 20 s and rinsed in IPA for 30 s. The sample is then exposed to O_2 plasma in a reactive ion etching (RIE) chamber (Plasma-Therm 790 Series) for 10 s at a power of 100 W, gas flow rate of 15 sccm, at a chamber pressure of 50 mTorr to pattern the graphene into a Hall bar geometry. Subsequently, another layer of

PMMA is spin coated using the same conditions given above, and EBL is performed to pattern the metal contacts. Finally, a combination of 5 nm chromium and 25 nm gold is deposited onto the sample in a thermal evaporator (Denton Vacuum Inc.) and then submersed in acetone for 24 hours to strip away the PMMA and lift-off the metal. Measurement of the device was performed in ambient immediately after retrieval from acetone on a Cascade probe station using an Agilent B1500A parameter analyzer. A 4-point probe configuration was used to eliminate effects of the contact resistance. The measured results were then fitted with a simple model to extract the mobility, CNP, and RCD [157]. An optical micrograph of a typical device used in this study is shown in Figure A.1(a), and its electrical characteristics, along with the model fit results, are shown in Figure A.1(b). It should also be mentioned that we maintained uniform channel dimensions of around 1.5-2 μm width, and 10-15 μm length for all of our devices in order to minimize the effects of device geometry [158]. Only devices showing a good fit ($R^2 > 0.99$) were used in the following discussion.

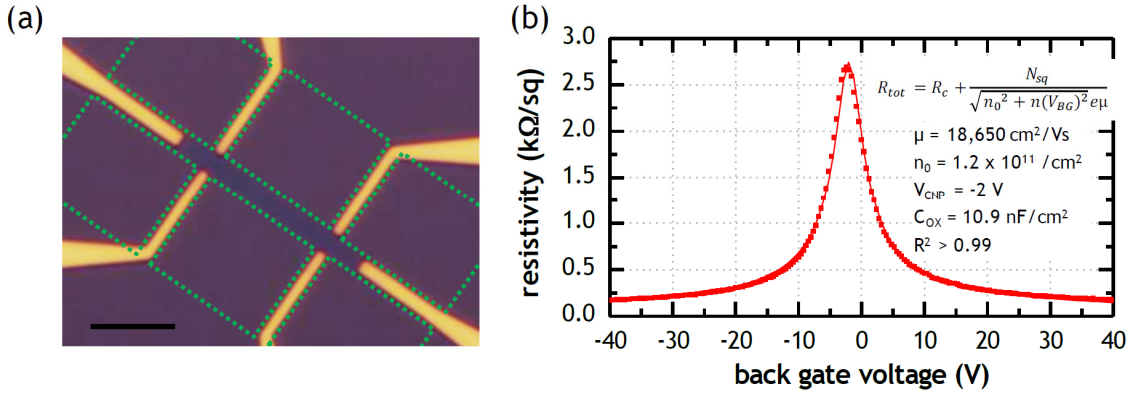

Figure A.1 (a) Optical microscope image of a typical device used in this study. Scale bar is 5 μm. The dotted green boxes indicate the regions where the electron beam is exposed during active patterning. (b) Transfer characteristic at room temperature (circles) and model fit result (solid line) of the device. A 4-point resistance measurement setup was employed using the outermost contacts for forcing current, and the inner two contacts for sensing the voltage.

A.3 Results and Discussion

Our main observation is summarized in Figure A.2. The mobility of the final devices shows a correlation with the exposure current level used during the active EBL step. In particular, the mobility is significantly lower at higher exposure currents. The CNP and RCD are also correlated with the exposure current level, albeit to a lesser extent. The CNP and RCD both increase with exposure current, as is evident in the device characteristics shown in Figure A.3(a). Furthermore, the device-to-device variation is also found to increase with exposure current. Raman spectroscopy results are shown in Figure A.3(b) for low, moderate, and high exposure current devices. As the exposure current is increased, there is a red shift in the G and 2D peaks and a decrease in the 2D-to-G peak intensity ratio, indicating that the graphene is more heavily doped [159]. It should also be noted that there is no significant D peak present in any of the devices, which points to there being no structural defects in the graphene nor any hydrogenation of graphene. Although there have been several reports on the degradation of mobility due to post-fabrication direct electron beam exposure of graphene FETs, suggesting a similar explanation for mobility degradation from EBL processes [153], the connection was unclear. This is because during the actual device fabrication process, when using a positive resist such as PMMA, the graphene channel area is not directly exposed to the electron beam whether there is a resist layer present on top or not. Although Woo and Teizer [155] added a PMMA resist layer on top of the graphene, here also the entire active region was exposed to the electron beam. Moreover, the exposure dose used in the experiments was well in excess of values that are used for EBL during typical FET fabrication, and unlike our results, there was a significant D-peak in the Raman signature after irradiation [155]. In our experiments, which itself is a standard procedure for fabricating graphene FETs, with commonly used dose for PMMA

resist, the electron beam is irradiated onto regions of the graphene where it is ultimately removed by plasma etching, and none of the active graphene channel region is directly exposed to the electron beam. Although the electron beam is directly exposed onto the resist on top of the graphene layer for the contact EBL step, it is limited to a relatively small portion of the contact regions, and the effects of which, if any, are eliminated when using a 4-point probe measurement setup. Even after the elimination of any contact effects, we observe a correlation between the mobility and electron beam exposure current. Moreover, previous reports only showed dependence on the electron energy and dose, and not the exposure current. Our results show that the extent of degradation is dependent on the rate at which electrons are irradiated onto the sample and suggests that resist heating – which is known to be highly dependent on the exposure current – could be playing a role. This is apparent when considering the results shown in Figure A.4. In Figure A.4(a), a graphene flake after PMMA coating and bake is shown, and the shaded region is where the electrons are exposed during EBL. Right after the EBL step and before development with MIBK, it can be seen in Figure A.4(b) that the graphene flake has curled up. This is similar to the case of Figure A.4(c,d) where the graphene flake is curled up after an excessive baking step of 220 °C for 2 minutes. In other words, it is likely that the graphene curling up during EBL is caused by excessive resist heating and the resulting stress caused by the mismatch in the thermal expansion coefficient of PMMA and graphene [160],[161]. It should also be noted that the discoloration of PMMA in the exposed region seems to be dependent on the type of substrate. There is more change in color where the graphene was present compared to bare SiO_2, as marked by solid and broken arrows in Figure A.4(b), respectively. This could be due to the spreading of the resist heating through the highly conductive graphene layer as discussed below.

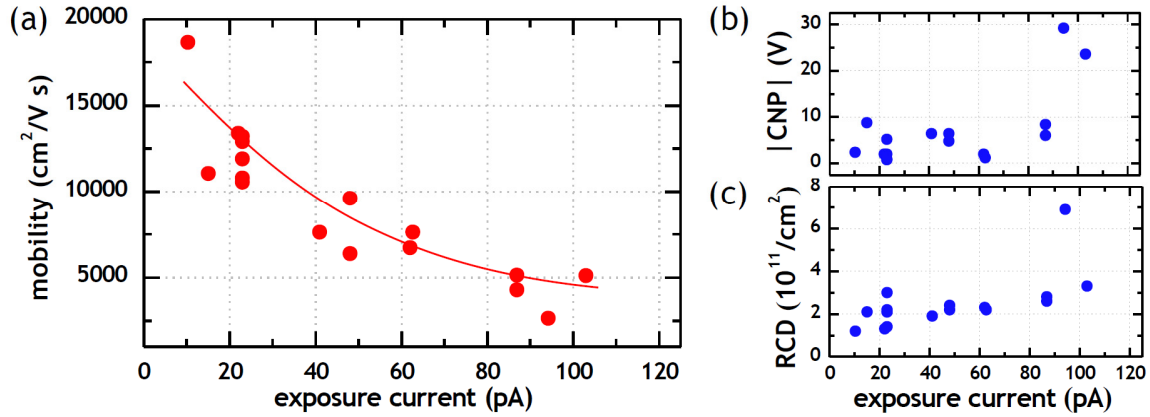

Figure A.2 Correlation between exposure current used for the electron beam lithography (EBL) and (a) extracted carrier mobility, (b) charge neutrality point (CNP) and (c) residual carrier density (RCD). As the exposure current is decreased, the mobility increases, the RCD decreases, while the CNP comes closer to 0 V with reduced device-to-device variations. The red curve in (a) is not a fit but only intended as a guide to the eye.

Here, we show that the difference in the level of resist heating originating from the difference in exposure currents used in our experiment is sufficient to explain the observed correlation. A general model based on a multilayer Green's function solution for the heat diffusion equation for resist heating effects for EBL, has been previously reported for the case of direct writing onto various substrates [162],[163],[164],[165],[166]. Its validity was experimentally verified using thermocouple measurements [161],[163]. It was shown that even for a relatively low beam current density of 100 A/cm^2 and a low dose of 100 μC/cm^2, the temperature on the surface of the resist can reach up to 750 °C at a depth of 0.4 μm – which is approximately the thickness of the PMMA resist layer in our experiments [165].

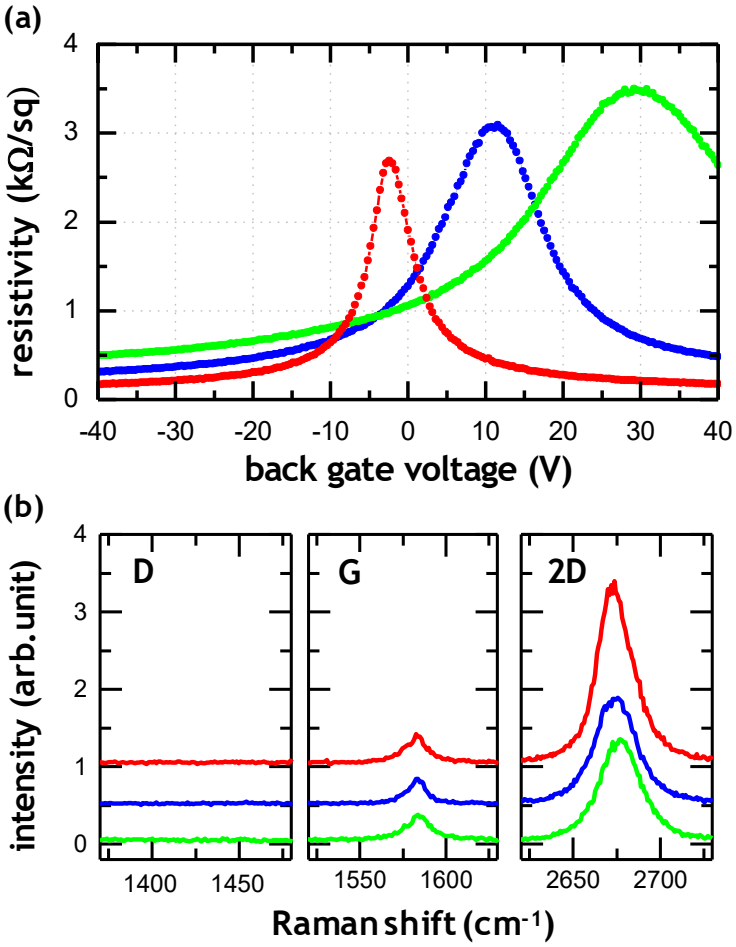

Figure A.3 (a) Electrical measurement and (b) corresponding Raman spectroscopy results for select devices fabricated with low (red), moderate (blue) and high (green) EBL exposure current level. Low exposure current results in better electrical characteristics. As the exposure current is increased, there is a red shift in both the G and 2D peaks, and simultaneously, a decrease in the 2D to G peak intensity ratio, which both indicate that the devices fabricated with a higher exposure current are more heavily doped. Also, it should be noted that there is no D peak present in any of the devices, meaning there are no crystalline defects or hydrogenation present in our devices.

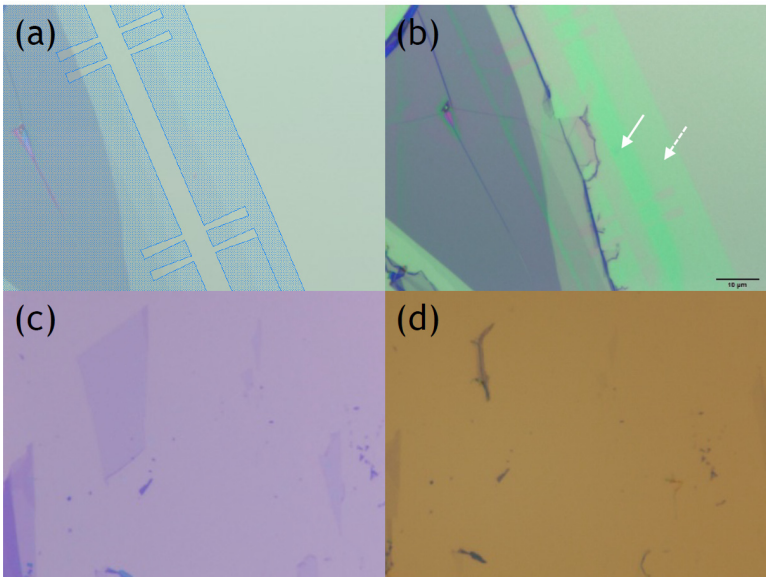

Figure A.4 (a) Graphene flake after PMMA coating and bake. Electron beam is exposed onto the shaded regions. (b) The flake shown in (a) after the EBL and before develop using a 300 pA/nm^2 current. It can be noted that the graphene has curled up, absent any processing other than EBL. This is similar to the case when (c) exfoliated graphene (d) baked at 220 °C curls up due to excessive heating and mismatch of the thermal expansion coefficients of graphene, SiO_2 and PMMA.

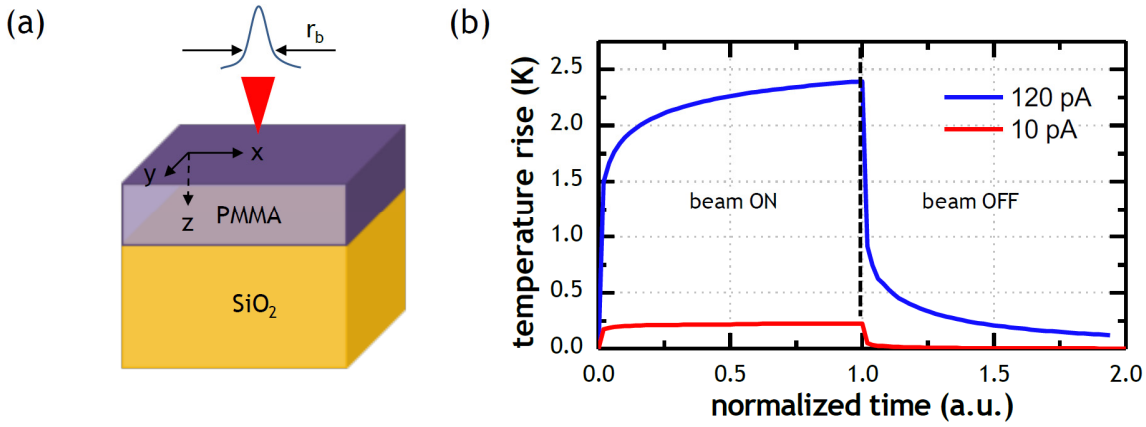

Figure A.5 (a) Schematic of the setup and axes used for simulation. (b) Calculated rise in temperature at the midpoint in depth of the PMMA resist as a function of normalized dwell time - where 0 indicates when the beam is turned on and 1 when it is turned off - for a single spot exposure of two different exposure current levels.

The general solution for the resist heating problem is given as a four dimensional integration of a Green's function over the heat source region,

$$\mathrm{T(x,y,z,t)} = \int dt` \int dx`dy`dz` \frac{1}{\rho\, C_p} G(x,y,z,t,x`,y`,z`,t`)g(x`,y`,z`,t`)$$

where, G is the Green's function, g represents the heat generation distribution due to the electron beam, ρ the mass density, and C_p the specific heat of the resist. The x, y, z, and t coordinates represent the temperature evaluation field, and the prime coordinates represent the heat source region. Assuming a Gaussian beam, the heat generation function g can be approximated by

$$\mathrm{g(r,t)} = \frac{\mathrm{V\,Q}\,\lambda\left(\frac{\mathrm{z}}{R_g}\right)}{R_g\,\theta} e^{-\frac{r^2}{2{r_b}^2}}$$

Here, V is the acceleration voltage, Q is the dose, λ is the Everhart-Hoff function representing the energy-loss distribution perpendicular to the surface, R_g is the Grün range, θ is the dwell time, and r_b is the beam radius [162].

Using this model, we calculated the temperature rise for two different exposure current levels with all other parameters held constant. Parameters such as the acceleration voltage, dose, and beam size used in the simulation were identical to those used in the experiments. Our simulation results, shown in Figure A.5, clearly illustrates the difference in resist heating that can result from the difference in EBL current level. Due to computational limits, we were not able to directly simulate real situations where a typical process would require roughly 10^8 such exposures in continuous sequence. However, it can be noted from Figure A.5 that an order of magnitude difference in the exposure current results in roughly an order of magnitude difference in the rise of temperature. Moreover, it

should be emphasized that since graphene has a very high thermal conductivity compared to the underlying SiO_2 layer [15], once this heat is transferred to the graphene layer, it can quickly spread across the whole flake. The transferred heat causes the resist on top of it near the interface to heat up and release alkyl, methyl and formyl group radicals [163],[167],[168]. This occurs not only at the directly exposed regions but also at the interface between the active channel region of the graphene and PMMA where the electron beam is not exposed. It has been suggested that in the case of ion bombardment, the depolymerization temperature of PMMA is significantly reduced from 360 °C to 115 °C [169],[170]. In other words, due to the combined effect of resist heating and the spreading of this heat through the graphene layer, a local depolymerization process can be initiated at the graphene and PMMA interface even where the electron beam is not directly exposed. This is in addition to the regular molecular weight reducing main-chain scissions and side group modifications that create radicals where the PMMA is directly exposed to electron beams [171],[172]. This depolymerization process can be further assisted by mobile radicals that are generated in the electron beam exposed regions. This means that even a relatively moderate temperature increase at the graphene active channel and PMMA interface can result in the release of radicals and accumulation of various polymer species generated by these radicals in this region. It should also be noted that exposing electron beams to PMMA has been found to result in a large yield of negatively charged radicals [172], and this may be a reason why we consistently observe a large positive shift in the CNP at higher exposure currents as shown in Figure A.3(a).

These radicals, generated through resist heating during EBL, could otherwise dissolve and be eliminated when subjected to solvents such as isopropyl alcohol (IPA) or acetone used during subsequent fabrication steps. However, as depicted in Figure A.6, the O_2 plasma etch step produces non-volatile carbonyl and carbonate residuals on the top

surface of the PMMA [173]. When the second PMMA layer is spin coated onto the substrate for metal contact EBL, these residuals are swept underneath the first PMMA layer. During the subsequent baking step, they are solidified and locked in place on top of the graphene, thereby, trapping the radicals that were generated during the EBL process earlier. The presence of this solidified residual layer is shown in the AFM image of Figure A.7(a). When compared to a control group shown in Figure A.7(b), where a cleaning process is introduced after the O_2 plasma etch and before the second PMMA layer coating in order to remove the residuals on top of the PMMA, it can be noted that these residuals form a roughly 5 nm thick layer on top of the graphene active region as well as other edges of the exposed region. PMMA, when spin coated onto a substrate, is hydrophobic and forms roughly a 70 º contact angle with de-ionized water [80]. Though this is somewhat reduced when subjected to oxygen plasma, for low power and short durations it is not significantly reduced [80]. Although in a strict sense, a contact angle of 70 º would not be considered hydrophobic, it has been shown that even for this level of hydrophobicity, the same effect on the device characteristics as for a 90 º contact angle substrate can be obtained [58]. Also, this is significantly larger than for the thermally oxidized SiO_2 substrate which water contact angle is close to 0 º for thicknesses beyond 30 Å [174]. Therefore, this polymer residual layer acts as a screening layer for moisture induced ambient effects during measurement from influencing the electrical characteristics, as has been demonstrated with other hydrophobic materials [58],[175],[176]. It has also been shown that coating graphene FETs with a hydrophobic layer can increase the mobility by a factor of 100 % [177]. In addition, this layer effectively traps any radicals that were generated by the EBL process and allows the device characteristics to be determined by the amount of these trapped radicals, free from ambient effects. We have also confirmed

that this layer is not removable by vacuum or forming gas anneal processes even at temperatures as high as 400 °C.

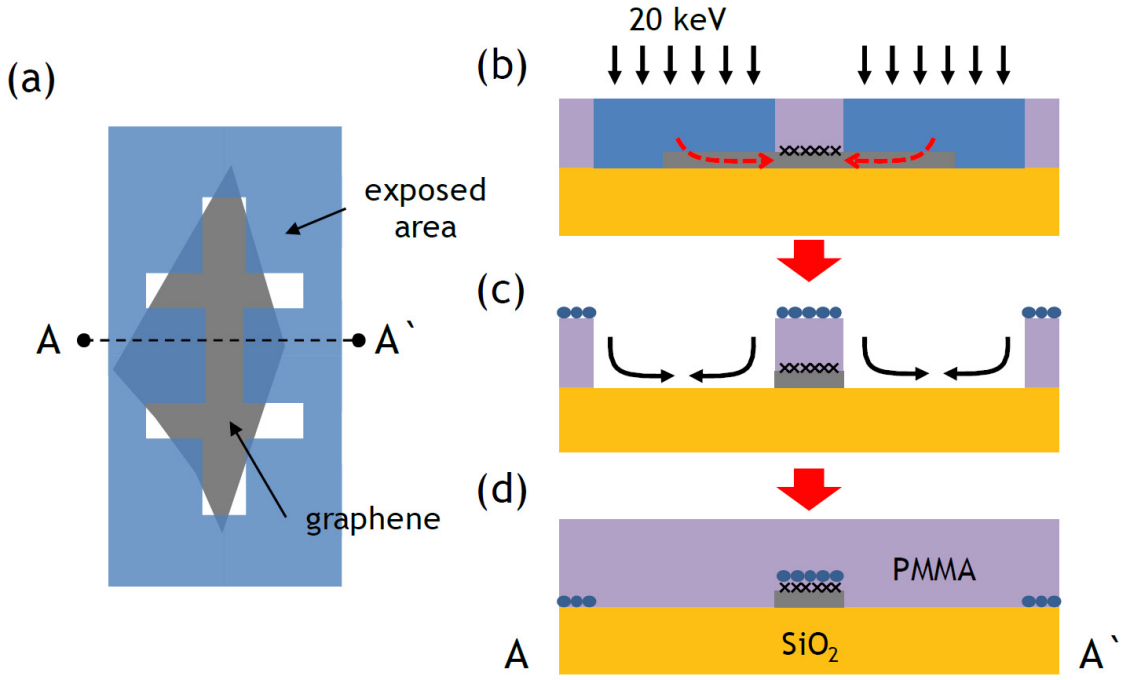

Figure A.6 Description for the formation of residuals and trapping of radicals on top of the graphene active region. (a) Top down view showing the initial as-exfoliated graphene flake and electron beam exposed region. (b) The electron beam heats up the resist which is transferred through the graphene to the unexposed graphene-PMMA interface causing it to depolymerize. (c) The exposed area is developed, and a subsequent plasma etch forms non-volatile hydrophobic residuals on top of the PMMA surface which is (d) swept underneath the existing PMMA layer when the second PMMA layer is spin-coated, and solidified in place during bake procedure.

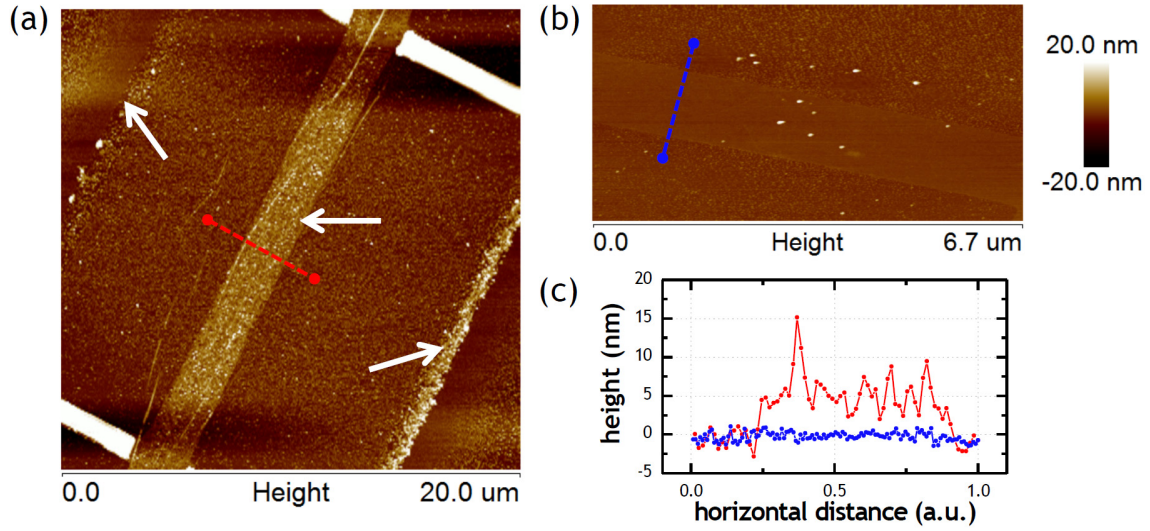

Figure A.7 AFM image of devices (a) without cleaning and (b) with IPA cleaning after the O_2 plasma etch step. The white arrows in (a) indicate the edges of the PMMA after development and corresponds to the sites where residual accumulation occurs. (c) Line profile across the graphene active region of each device (color matched), where it can be noted there is a 5 nm thick polymer residual layer on top of graphene for the device without cleaning.

In order to further confirm our hypothesis, we performed three control experiments. In the first experiment, O_2 plasma etch time was increased to 60 s with all other conditions being unaltered. For this group, the correlation between exposure current and mobility, CNP, and RCD all disappear and the mobility is relatively constant in a range of 2,000 - 3,000 $cm^2/V{\cdot}s$, regardless of the exposure current, as can be seen in Figure A.8. This is because when the etch time is increased, more radicals are generated by the plasma process on top of the PMMA and subsequently swept underneath the existing PMMA layer [173]. This effect overshadows the radicals introduced by the EBL process and dominates the electrical characteristics of the device. In a second control experiment, an electron beam evaporator (CHA Industries) with an acceleration voltage of 10 keV is used instead of thermal evaporation for the metal deposition process, with all other conditions held

constant. Here, the baseline correlation between EBL current and mobility disappears at low EBL exposure currents as is shown in Figure A.8, and the mobility is in the range of 4,000 – 5,000 $cm^2/V{\cdot}s$. E-beam evaporation is known to have effects such as secondary electron scattering and X-ray emission which can potentially degrade the PMMA layer and release radicals [178]. Thus, the radicals from the EBL process dominate when EBL exposure current is large, while at low EBL exposure current levels, the radicals generated by the electron beam evaporation process degrade the graphene mobilities. In the final control experiment, a cleaning process involving a 5 minute dip of the sample in IPA is introduced after the plasma etch and before the second PMMA layer coating, with other conditions being constant. In this case also, the devices show no correlation between their electrical characteristics and exposure current, and the mobility is relatively constant in a range of 6,000 – 8,000 $cm^2/V{\cdot}s$. Since the hydrophobic residual layer created by the plasma process is removed by the IPA rinse, there are no residuals on top of the graphene to either protect the device from ambient effects nor hold down the radicals that are generated during the EBL process. Thus, the characteristics are determined by the ambient and substrate condition and show a constant mobility value that is typically reported in the literature for graphene FETs on SiO_2.

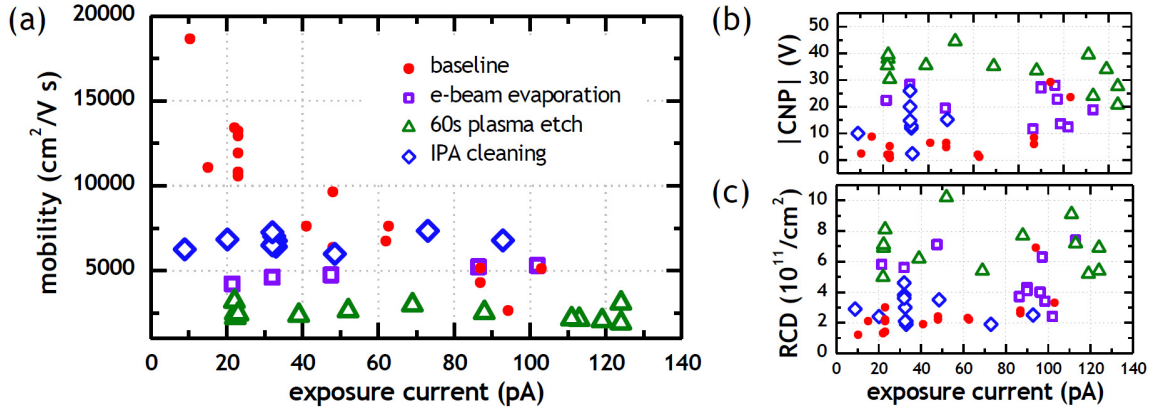

Figure A.8 Correlation between EBL exposure current and (a) extracted mobility, (b) charge neutrality point (CNP) and (c) residual carrier density (RCD) for three control experiments. The correlation breaks down when either more radicals are introduced through e-beam metal evaporation (purple squares) or longer O_2 plasma etch time (green triangles), or when the radicals are removed through the removal of the polymer residual (blue diamonds).

A.4 Conclusions

Although there have been numerous reports on the effects of electron beam exposure on the transport properties of graphene FETs, the experimental setups were not representative of actual device fabrication processes, and therefore had limited explanatory power. Most of the experiments involved direct exposure of electron beams onto graphene FET channel regions without any resist layer present. Even when a resist layer was introduced, the electron beam was exposed onto the channel regions, which is not the case in actual graphene FET fabrication process using a positive resist such as PMMA. In this report, we provide direct evidence of exposure current dependent resist heating induced depolymerization of PMMA during the EBL process commonly used for graphene

patterning. When a high exposure current is used, the resist heating is severe, leading to an enhanced release of radicals near the graphene and resist interface. Subsequently, when the sample is processed with O_2 plasma etch for active patterning, a hydrophobic residual layer forms on top of the PMMA. Upon spin coating of the second PMMA layer for metal contact patterning, this residual layer is swept underneath the existing PMMA and on top of the graphene active region. Radicals that are released from the previous EBL process get stuck at the interface between the graphene and residual layer, which ultimately determines the electrical characteristics. We performed resist heating calculations to show that an order of magnitude difference in the exposure current level roughly translates to an order of magnitude difference in the temperature rise. In other words, we found that the use of a higher exposure current leads to increased radical release, which get trapped at the residual layer and graphene interface, resulting in lower mobilities, positively shifted CNPs, and higher RCDs. Furthermore, we give evidence for this hypothesis through three control experiments where more radicals were intentionally introduced by an increase in O_2 plasma etch time, employing e-beam evaporation for the contact metal deposition, and also by removing the residual layer to obtain devices without any trapped radicals. By minimizing the exposure current for the EBL process, minimizing the plasma etch time, and using thermal evaporation for the metal deposition, trapped radicals can be minimized to obtain enhanced electrical characteristics. As a result of our findings, we were able to demonstrate mobility of up to 18,000 cm^2/Vs on SiO_2 substrates.

We believe that our findings can be generalized to other 2D material based devices and other nanoscale devices, other resist materials or polymers, and other heat inducing lithography processes in general, provided that the generated radicals can get trapped at various interfaces. In the case of electron beam induced resist heating, we think that whenever the resist material is not sensitive and requires a high enough dose to cause

sufficient resist heating for depolymerization to occur, as is the case for PMMA, our findings should be taken into consideration. In addition to these lithography processes, care must be taken in order to prevent excessive heating of PMMA resist, or any other polymer, above its depolymerization temperature, in order to avoid the effects of trapped radicals. In the case of PMMA, depolymerization occurs at roughly 360 °C without any assistance from electron or ion beams, and at 115 °C in the presence thereof [169],[170]. We also note that it is possible that variations in the reported mobility of many 2D FETs might be caused by differences in the EBL process condition and that further study of this effect in such devices will be worthwhile.

APPENDIX B: AIR-GAP DOUBLE GRAPHENE HETEROSTRUCTURE FOR BILAYER PSEUDO-SPIN FIELD-EFFECT TRANSISTOR

B.1 Introduction

In order to reduce screening from the surrounding dielectric environment that inhibits the formation of a Bos-Einstein condensate (BEC), it was suggested that a low-k dielectric surrounding the device would be desirable [179]. As a part of an effort to experimentally realize this condition, air-gapped double graphene heterostructures were studied. In this device, the two graphene sheets would be separated by an air-gap region. The objective was to conduct Coulomb drag measurements across this region to identify signatures of a BEC. Initial attempts relied on simple wet transfer of a graphene flake onto a graphene FET with pre-defined metal pillars that would hold the top graphene in place, and at the same time act as the metal contacts to the top graphene layer. It was soon realized that this method required the transfer film (PMMA) to remain in place through the measurements in order to prevent the collapse of the top graphene layer onto the bottom. However, the sample could not be cooled down to liquid nitrogen temperature (77 K) for further characterization because of the high thermal expansion (contraction) coefficient of the PMMA layer causing the top layer to curl up. Later, the air-gap was defined through selective physical vapor deposition (PVD) or selective atomic layer deposition (ALD) growth of dielectrics onto the bottom graphene FET. However, the quality of such films proved to be insufficient, although every effort was made to make a pristine bottom graphene FET surface. Additional attempts were made using pre-patterned hBN films as the pillar layer. However, it was surmised that as soon as measurements were made, the top layer seemed to collapse onto the bottom layer due to the strong electrostatic attraction,

and when close enough, due in part to the van der Waals force. Calculations show that if sufficiently thick top graphene layers are used or if the top graphene layer is supported by a thick hBN layer on top to increase the stiffness of the top stack, one might be able to overcome this issue of electrostatic force induced top layer collapse.

B.2 Approaches

B.2.1 Metal Pillars

In this approach, the bottom graphene FET was first fabricated. The contacts to the bottom graphene were simultaneously defined with the metal pillars that would hold up the top graphene layer and also act as bottom contacts to the top layer, through EBL and Cr + Au lift-off [Figure B.1]. While we were able to obtain intralayer resistance measurements of the top and bottom layer independently [Figure B.2], further characterization of the device was not possible, and a few problems with this approach were later identified. Firstly, the current in one layer was perpendicular to the other so Coulomb drag measurements were not possible. Secondly, the contacts to the top layer were not stable. Thirdly, in order to accommodate a large margin for the wet transfer of the top layer and at the same time try to minimize the air-gap width, the bottom graphene FET had to have a very narrow and long channel. This tended to cause the bottom graphene channel to curl up quite easily during the wet transfer process. Fourthly, the metal pad thickness had to be minimized in order to detect any kind of interaction between the two layers but at the same time had to be thick enough to not cause a significant increase in the contact resistance.

Lastly, the structure required the presence of the transfer PMMA film to be intact, which prohibited low temperature measurements

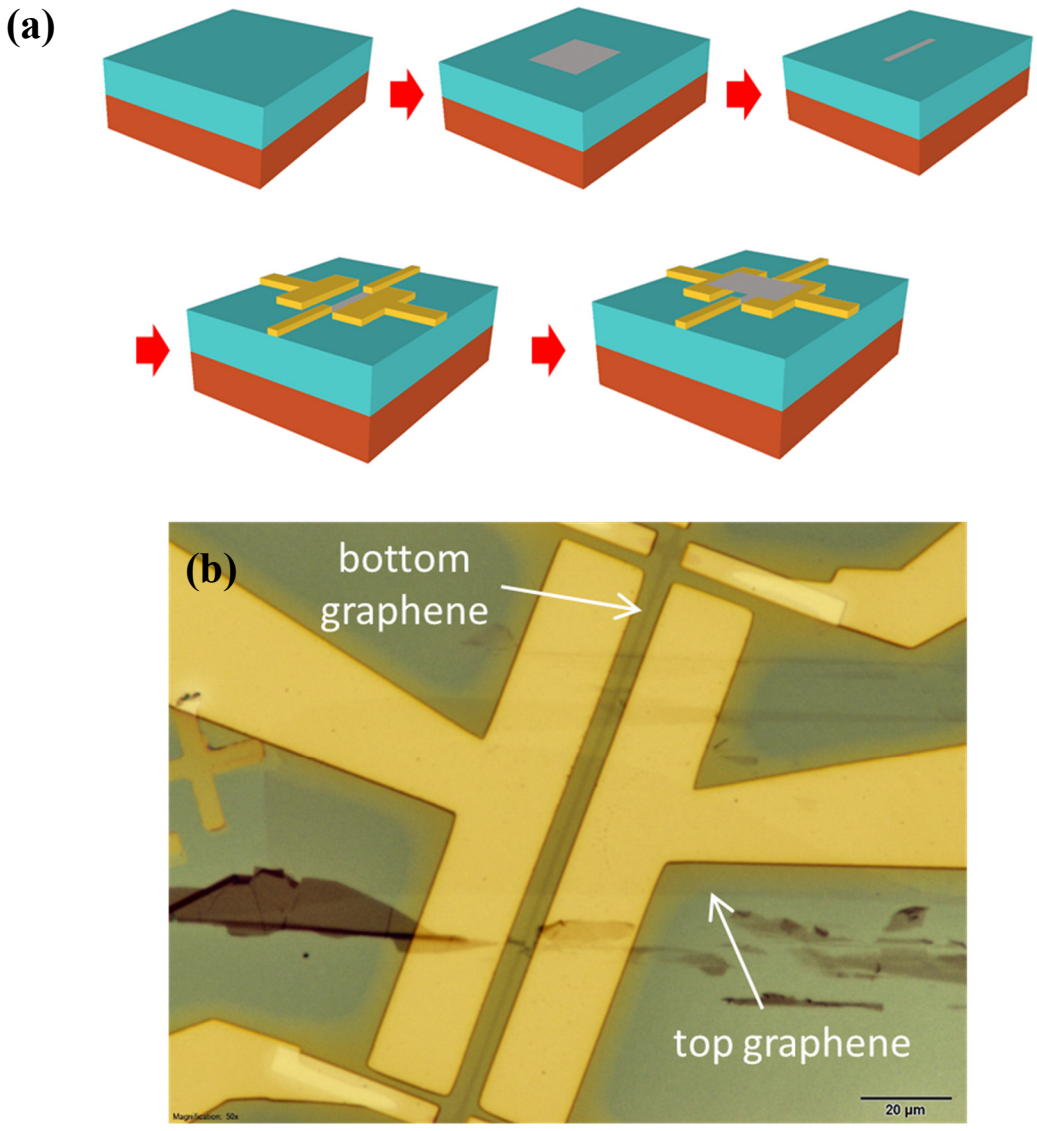

Figure B.1 (a) Process flow for air-gap device with metal pillars. Graphene exfoliation, bottom graphene patterning and contact formation, followed by top graphene transfer. (b) Optical microscope image of device after transfer. (Sample # 12S027).

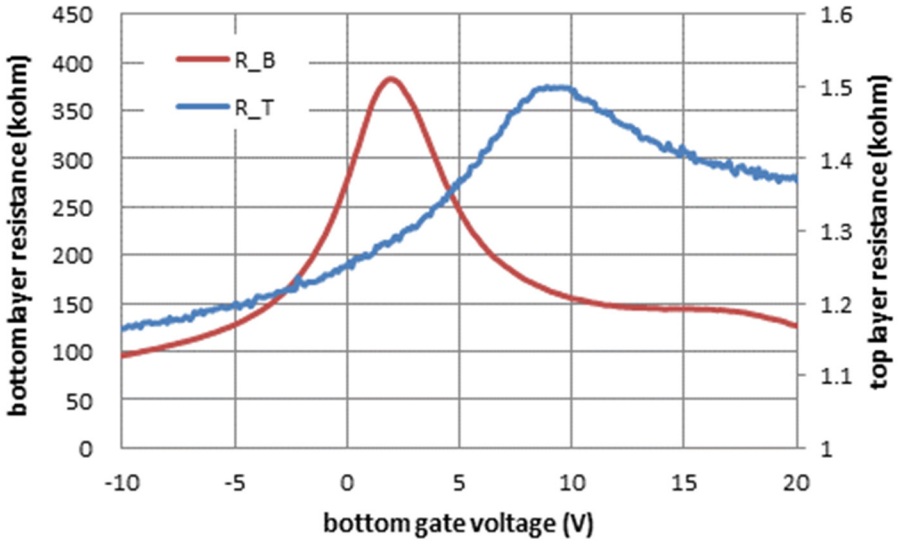

Figure B.2 Layer characterization result for the device shown in Figure B.1. The bottom layer (red/left) showed much higher resistance compared to top layer (blue/right) due to its elongated geometry.

Although some of these problems could be solved by defining additional top contact pads, using two step metallization, utilizing improved transfer methods, and removal of the PMMA film through dissolving in acetone and super-critical drying methods used for suspended structures, there was a limit to the geometry of the deivce we could study with this approach.

B.2.2 PVD Oxide and ALD Dielectric Pillars

An alternative route was explored. In this method, we would first pattern the pillar region independently through EBL on a pre-fabricated bottom graphene FET. Then, the patterned region was filled with PVD oxide and lift-off was conducted to leave a region where the air-gap between the two graphene layers would form [Figure B.3].

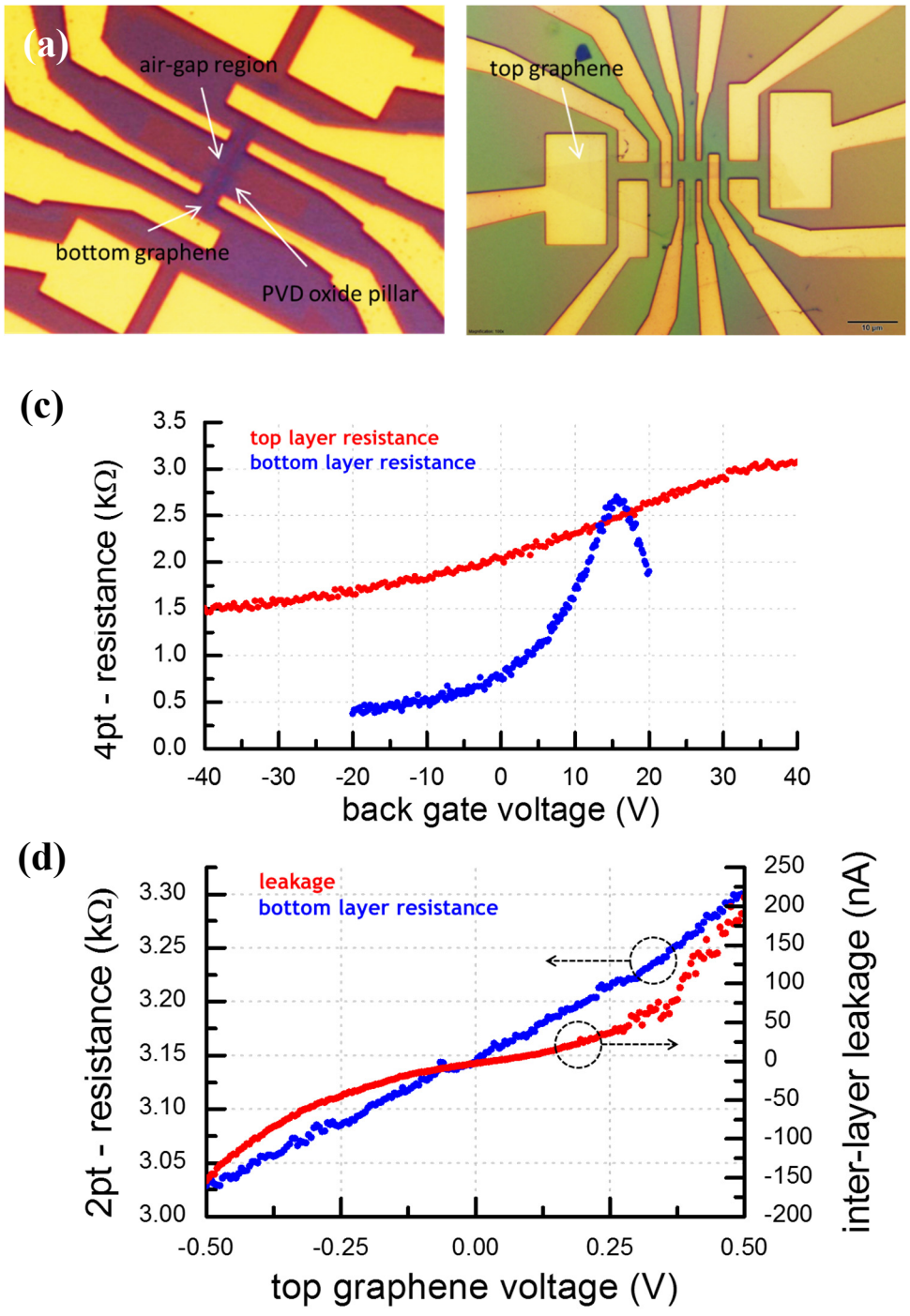

Figure B.3 Device made with PVD oxide pillar approach (a) after PVD oxide lift-off and (b) after top layer transfer. (c) Intralayer characterization results and (d) interlayer leakage (Sample # 12S152).

Although intralayer characterization results were obtained, the interlayer leakage of the device was too large [Figure B.3(c,d)] at 2.5 MΩ area-normalized interlayer resistance. Multiple devices showed similar results with the interlayer resistance in the range of 0.1 ~ 2 MΩ. This was surmised to be the result of the low quality PVD oxide being used as the pillars. In order to improve the leakage, PVD oxide was replaced with selective ALD Al_2O_3 growth through patterned deposition of an Al seed [Figure B.4] [157]. With ALD grown pillars, the leakage was drastically improved with interlayer resistance in the range of 0.1 ~ 0.5 GΩ. However, repeated measurements quickly resulted in degraded interlayer leakage characteristics even for selective ALD growth [Figure B.5(a)]. The problem with ALD grown dielectrics was that if the surface of the bottom graphene FET was not pristinely clean, there would be pin holes in the dielectric [Figure B.5(b,c), Figure B.6], and this problem would exacerbate when the thickness of the dielectric was scaled down. For very thin ALD dielectric, the randomly dispersed seed layer was not enough to laterally cover the graphene surface. However, when the thickness is increased in order to reduce the pin-hole defects, the air-gapped region would also close up and fill with the dielectric due to lateral growth [Figure B.7].

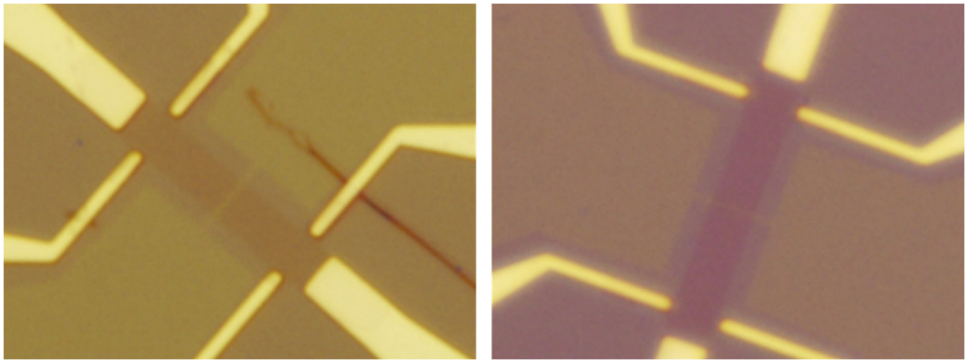

Figure B.4 Optical microscope images of devices made with selective ALD growth pillars.

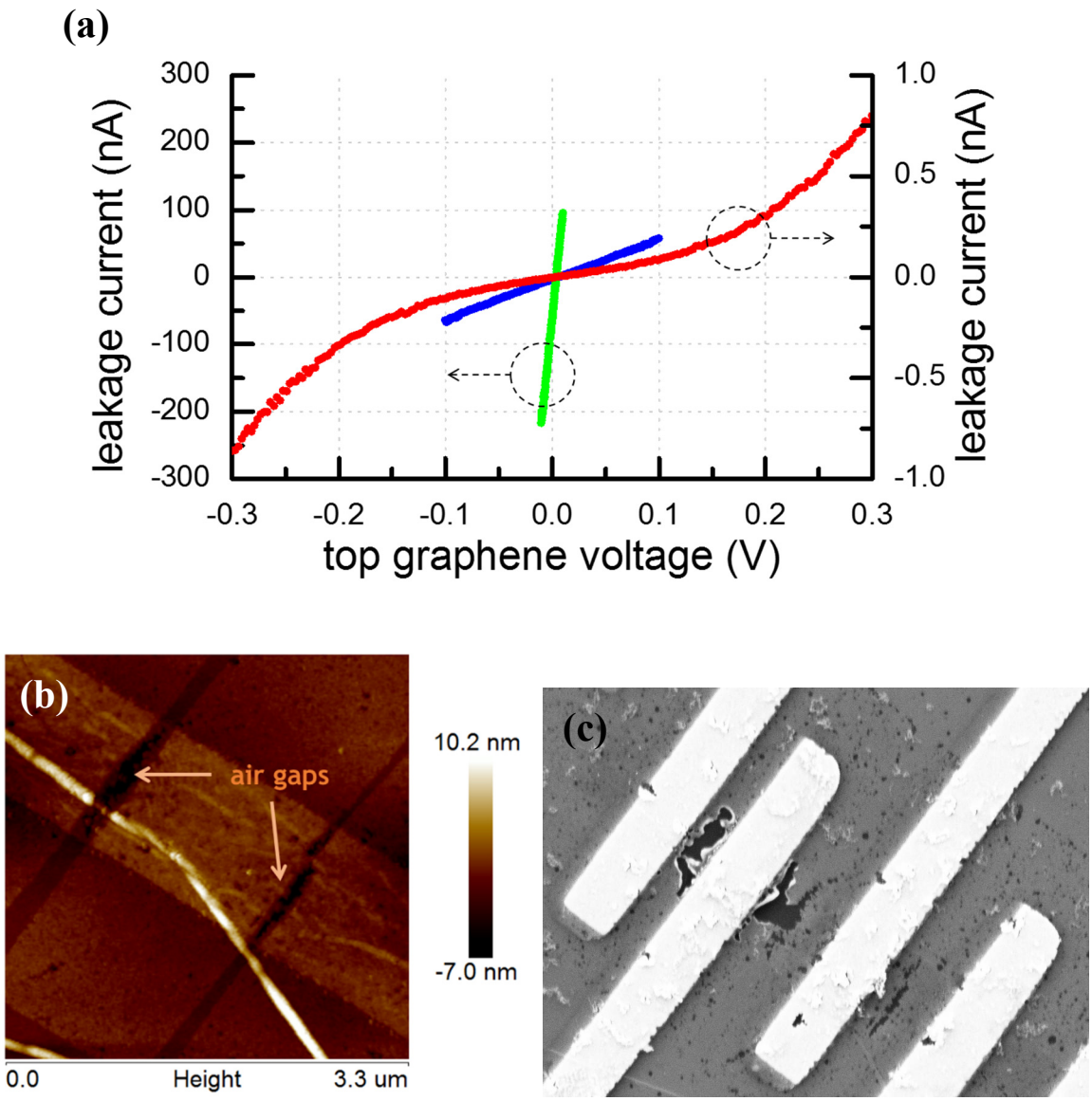

Figure B.5 (a) Initial interlayer leakage (red) was near the GΩ range but repeated measurements caused the leakage to increase dramatically (blue, green). (b) AFM image of the device showing the two air-gapped region and (c) scanning electron microscope (SEM) image of the same device after metallization.

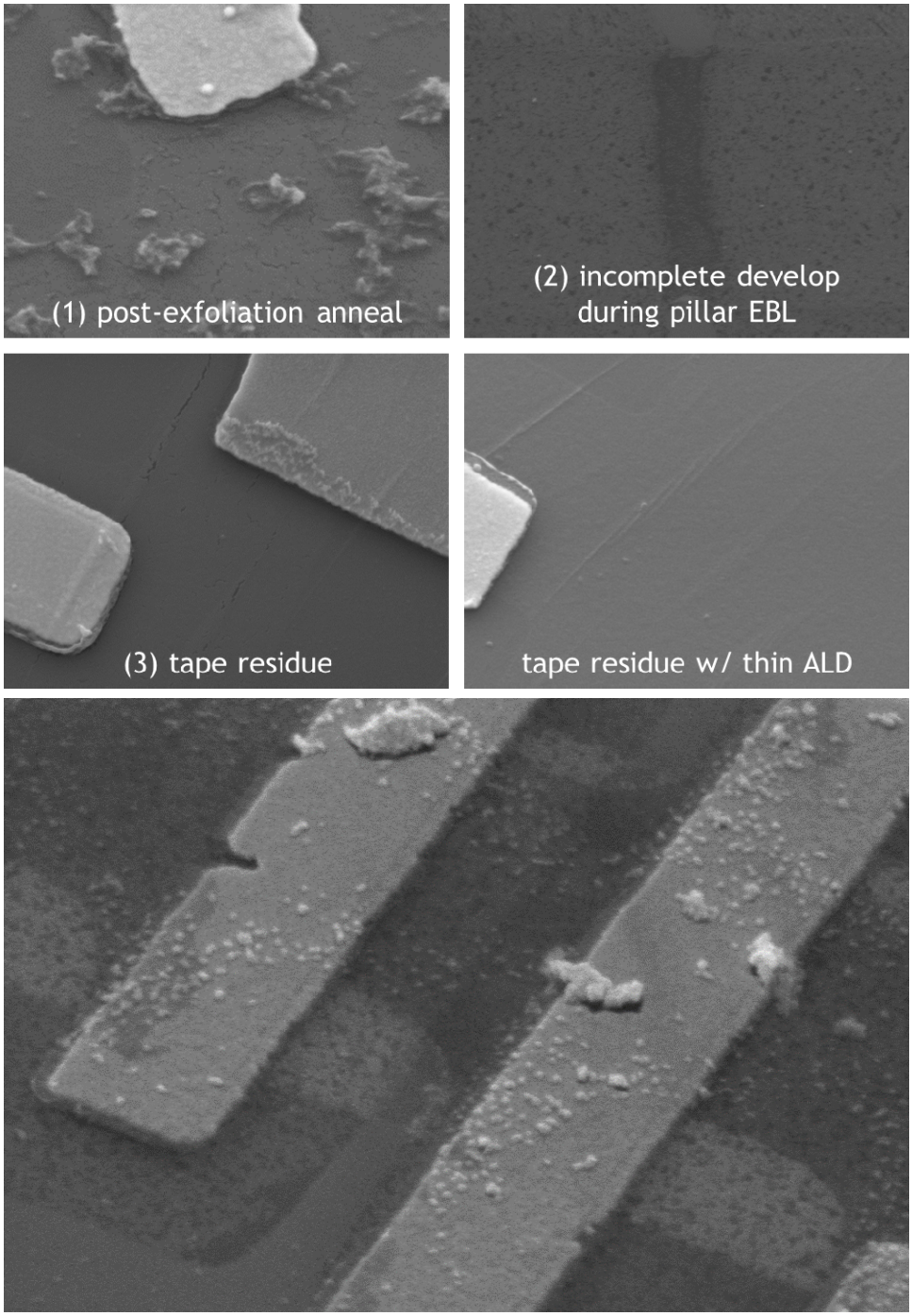

Figure B.6 (1-4) SEM images showing some of the issues identified using the ALD HfO_2 growth pillars. (Bottom) SEM image showing the air-gap region of the device. Note how the contacts to the top graphene layer covers the pin-holes in the pillar dielectric to create a short path to the bottom layer.

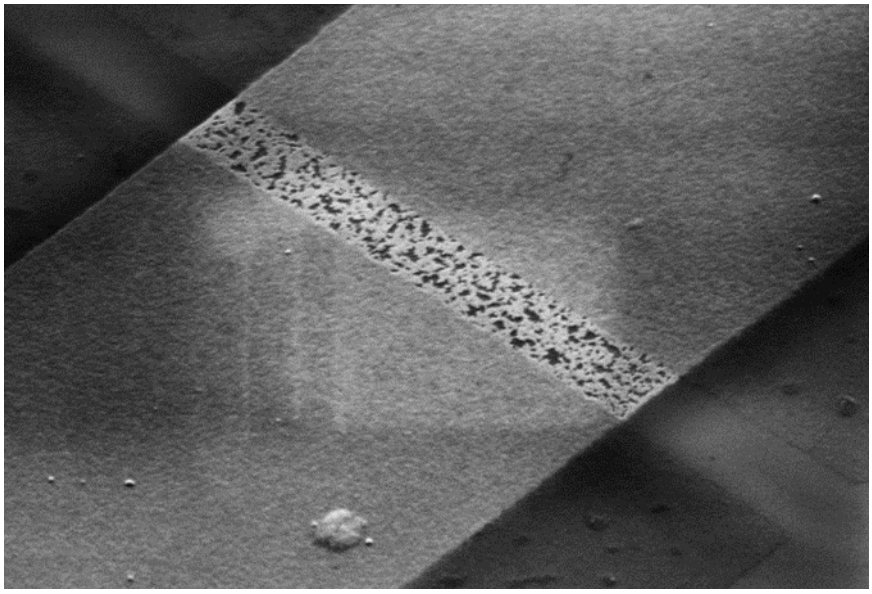

Figure B.7 SEM image that shows how when the Al_2O_3 dielectric is thick enough to have no pin-holes in the pillar region, the air-gapped region also fills up with the dielectric.

B.2.3 Patterned hBN Pillars

The next approach involved the use of a pre-patterned hBN flake as the pillar layer. A fine slit would be opened with EBL and CHF_3+O_2 plasma etching of an as-exfoliated hBN flake. Then this flake would be used to make an hBN and graphene heterostructure similar to what was made for the ITFETs of Chapter 2 and 3. The only difference would be that the interlayer hBN would have a slit which would ultimately result in an air-gapped region between the two graphene layers. One device was made with this approach, but the device suffered from high levels of interlayer leakage. We checked that this was not coming from the air-gapped region but was from a different spot of the device.

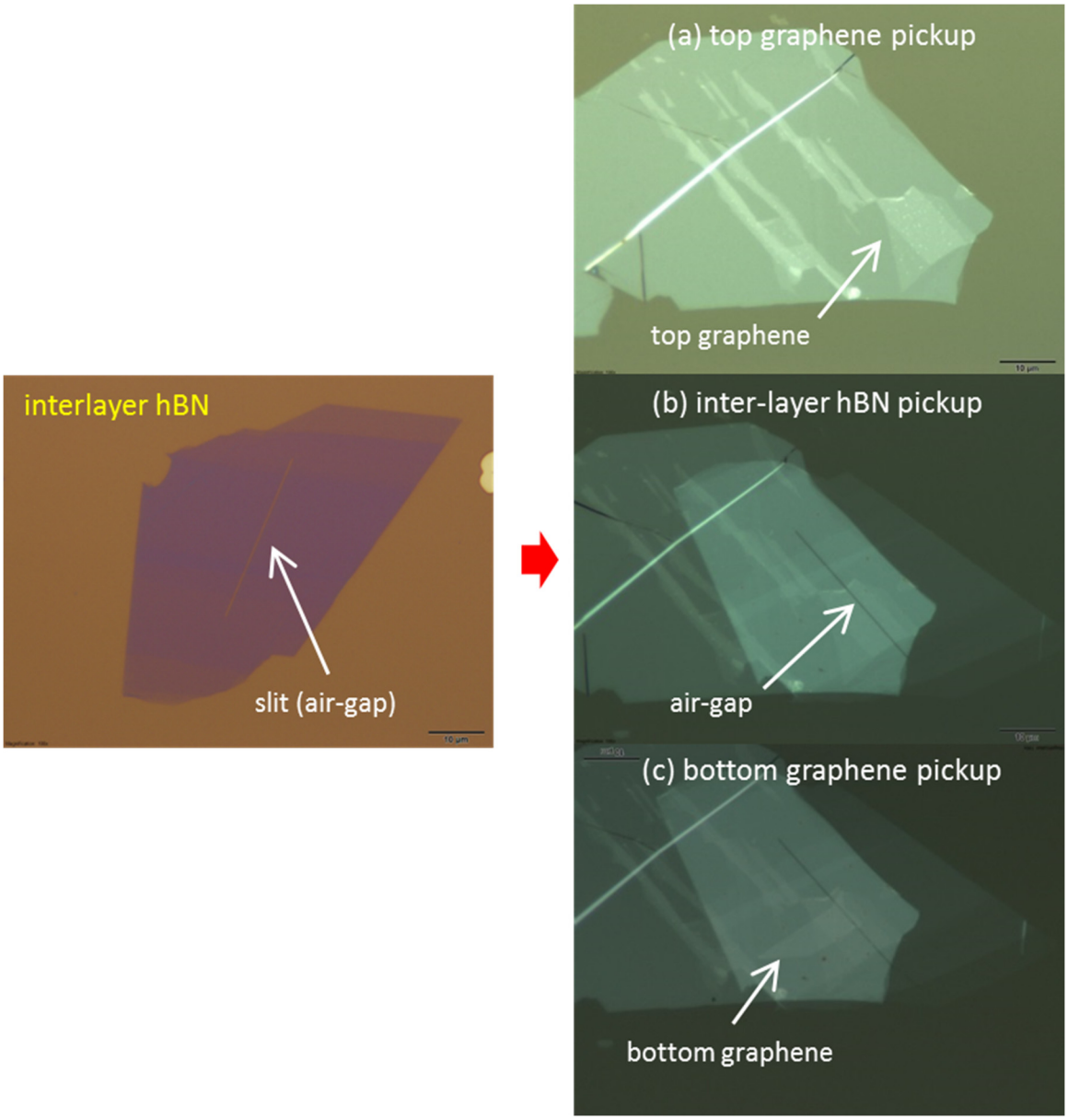

Figure B.8 Transfer process flow for device made with hBN pillars. An hBN flake is pre-patterned using EBL and plasma etching to make a slit. The top hBN and (a) top graphene is picked up, then (b) the interlayer pillar hBN, and finally (c) the bottom graphene.

B.3 Results and Discussion

Through these experimental efforts, it became evident that the most important issue with the air-gap device was the deformation and the possibility of an eventual collapse of the top graphene onto the bottom graphene layer. Several studies have dealt with this issue, and issues related to suspended graphene structures in general [16],[180],[181],[182]. Some have suggested that in such structures, the van der Waals force can cause the top graphene to adhere to the side surface of the pillar region to cause sagging of a few nm if the graphene sheet is permitted to either slip or stretch to a certain extent [16],[180]. Also, AFM measurements on such structures have been shown to cause additional deformation depending on the load [181]. A thorough study on how much sagging occurs for an electric field applied to suspended graphene was also presented and a model for the phenomenon was presented [182]. Graphene deformation h_0 can be modeled as a thin film that is double clamped at $x = -L/2$ and $x = L/2$ under a uniform pressure P in the out-of-plane direction by the equation [Figure B.9(a)],

$$PL^2 = 8T_0 t h_0 + \frac{64}{3}\frac{Et}{L^2(1-\nu^2)}h_0^3 \qquad (B.1)$$

where $t = 0.34\,nm$ is the thickness of the graphene layer, E the Young's modulus, and ν the Poisson ratio with a range of 0.1 to 0.3 for monolayer graphene. T_0 is the pre-existing stress on the membrane at $P = 0$. We can use for the pressure $P = (C^2V_g^2)/(2\varepsilon_0)$ where C is the capacitance per unit area between the graphene sheet and the back gate, V_g is the applied back gate voltage, and ε_0 is the permittivity of free space in the case of a simple parallel plate capacitance approximation. For the case of an air-gap region on top of a SiO_2 substrate we can write,

$$P = \frac{\varepsilon_0}{2}\left(\frac{\varepsilon_r}{\varepsilon_r d_1 + d_2}\right)^2 V_g^2 \qquad (B.2)$$

where d_1 = 280 nm is the SiO_2 thickness, d_2 = 100 nm is the air-gap thickness, and ε_r = 3.9 is the dielectric constant of SiO_2. In order to accommodate for the bending of the graphene sheet with applied bias we can use for the capacitance

$$C = \frac{\varepsilon_0}{\sqrt{h_0(d_1 - h_0)}} \tan^{-1}\left(\sqrt{\frac{h_0}{(d_1 - h_0)}}\right) \qquad (B.3)$$

which is to be self consistently solved together with equation B.1 and B.2. With this model we were able to predict how much sagging would occur for a given air-gap width and applied back gate bias [Figure B.9(b,c)].

Based on these results and equation B.1, if one is to increase the Young's modulus E of the membrane by using thicker multilayer graphene [Figure B.9(b)] or supporting it with a thick hBN on top, it may be possible to minimize the deformation h_0. This is why it might perhaps be worthwhile to explore the air-gap device once more.

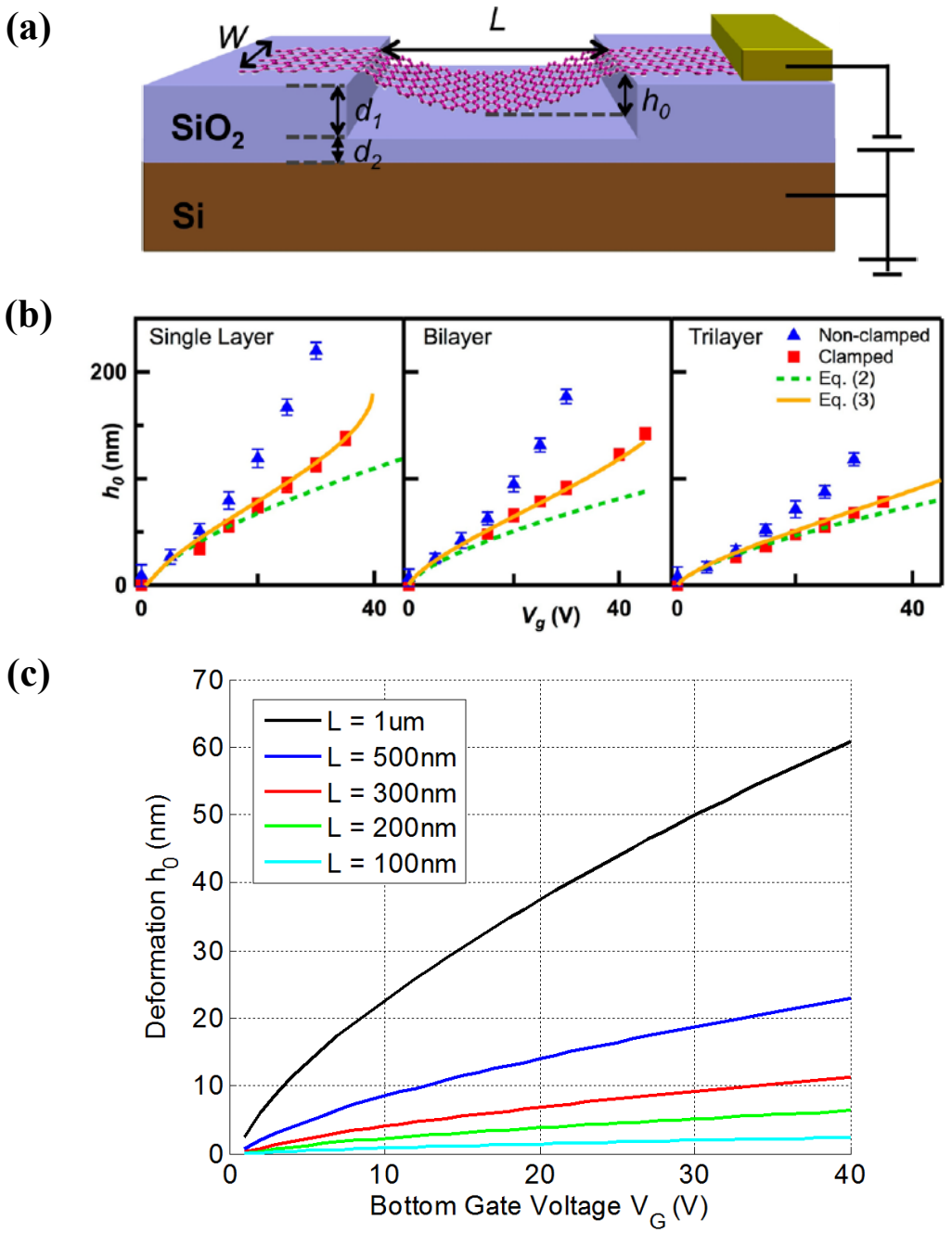

Figure B.9 (a) Description of the geometries involved in the modeling of suspended graphene deformation. (b) Measurement and simulation results for mono/bi/trilayer graphene. Adapted from [179]. (c) Simulation results for typical experimental conditions for the air-gap device.

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