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Towards reproducible graphene synthesis on optimized copper substrates

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Towards reproducible graphene synthesis on optimized copper substrates

by

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Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

May 2016

Dedication

For my mother

Acknowledgements

I would like to thank Dr. Andrew Morrill and Dr. Martin Moskovits from UC Santa Barbara and Dr. John Lee from San Jose State University, for showing me that research of innovative topics can be challenging and rewarding as well. They showed me that even though times may get rough, the rewards from good research can make it worthwhile and got me started on my path to an advanced degree.

Next, I would like to thank all of the wonderful people that have touched my life during my time at UT Austin. Huifeng Li and Bin Zhang for being there to answer some of the more trivial questions I had during my initial time in a research group. Matt Charlton, Charles Amos, and Carl Magnusson whom I worked closely with helped to keep my initial ideas in focus. I would like to thank all of all my colleagues in the Ruoff Research group: not only the posts-docs, but the numerous and talented visiting scholars from all around the word, my fellow grad student learn from. My lab mates Li Tao, Milo Holt, and Saungeun Park were there to engage in some meaningful discussions and to lend a hand for experiments. Richard Piner for keeping the shared characterization equipment (SEM, micro-Raman, etc.) up and running. The research administrators, Shannon Wilkerson, Dustin Wilson, and Amy Jablon were wonderful at navigating the bureaucracy of the university. Most importantly, I would like to thank Prof. Rodney Ruoff, for letting me join his fantastic group and Prof. Deji Akinwande for letting me continue in my studies after Prof. Ruoff left.

I am grateful to all members of my committee, Prof. Register, Prof. Banerjee, Prof. Tutuc and Prof. Cullinan for reading my thesis and giving me valuable feedback. I cannot thank enough my supervisor, Prof. Deji Akinwande for all his guidance and support. He took

me in after Prof. Ruoff left and welcomed me into his group. I enjoyed the freedom that he gave me for picking my research topic and trying different approaches to answer them.

Finally, I would like to thank my family. Melissa and Alice for whom I would never have been able to make it as far as I have. They make this all worth doing.

Towards reproducible graphene synthesis on optimized copper substrates

Alvin Lynghi Lee, Ph.D.

The University of Texas at Austin, May 2016

Supervisor: Deji Akinwande

As more knowledge is accumulated in the synthesis of 2D materials, such as graphene, graphene analogues, and transition metal dichalcogenides (TMDs), we are confronted with widely varying qualities of materials synthesized. In order to integrate into current VLSI technology and beyond to wearable technologies, the synthesis of the materials needs to be facile and provide reproducible quality.

In order for reproducible graphene to be made, we must have a better understanding of the mechanism that causes the differences in quality of graphene synthesized. Different groups report graphene mobilities with larges variance. Even within the same research group there can be differences in graphene quality from piece to piece. To further graphene research, the quality should be close to the level that we would expect less than a 10% difference from batch to batch or group to group. We examine graphene grown on copper of varying purities. Commercially available copper was chosen to be able to have this work be easily replicated. Additionally, we produced copper film using E-beam evaporation, which is a commonly used method. Graphene was synthesized using methods that have already been outlined in literature to examine the role of the substrate.

To enable a transition to flexible substrates for wearable devices, we investigate the use of polymer electrets to provide electrostatic doping to graphene. The benefit of using polymer electrets is that they are solution processable and have well understood properties. These properties hold promise for developing wearable graphene devices. The properties of electrets can be further extended to other 2D materials providing the same benefits that they afforded graphene.

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Chapter 1: Introduction

Graphene, a highly researched carbon allotrope, has been touted for its remarkable electronic, optical, and mechanical properties. [1-4] Utilizing the high mobility and thermal transport properties, flexible electronics, on par with current silicon- based devices could be realized. In order for graphene integrate into the semiconductor industry, methods to grow high quality graphene that are easily reproducible need to be developed.

There are many different ways to synthesize graphene such as reduction of graphene oxide,[5-8] epitaxial growth on SiC wafers[9, 10], chemical vapor deposition (CVD) on metal thin films,[11-13] CVD on metal foils,[14-18] and most recently on hydrogen-terminated single crystalline germanium surfaces.[19] These production methods produce graphene of varying quality and size. The method that is most commonly used is CVD on transition metals. Graphene growth on metals has the widest range of growth parameters providing an even larger number variation in quality.

In short, the CVD mechanism uses a carbon source, either gaseous or solid. The gaseous phase can be further split to include vapor phase liquid precursors. Numerous sources have cited low temperature growth, but they typically involve annealing at a high temperature, thus they are not true low temperature growth. The process for CVD growth involves allowing the carbon precursor to come into contact with the catalyst substrate. Once contact has been established, the carbon can remain on the surface or it can desorb. If desorption occurs then the carbon could potentially still come back into contact with the surface through collisions with other molecules above the surface. Finally, when the

carbon finds a nucleation site it will begin to form graphene. This is for substrates have low carbon solubility.

For substrates that have higher carbon solubility, a different growth mechanism occurs. The carbon will diffuse into the metal and upon cooling down the furnace the carbon will segregate out of the metal forming multiple layers of graphene. This is not desirable since the number of layers is not easily controllable. It is possible to grow monolayer graphene using metals that have carbon solubility by performing a quench cooldown. The quenching prevents diffusion of carbon form the metal bulk onto the surface during cooldown. This method allows for the formation of monolayer graphene even though the metal can produce multiple layers.

In order to adapt graphene for use in industry, methods to scale the growth area of graphene are needed. Different methods have been demonstrated for scaling the area of graphene grown.[20, 21] Hurdles exist in order for an easier transition into the semiconductor industry; one of these hurdles is consistent quality regardless of growth location, i.e. graphene grown in different parts of the world should yield the same quality and the other is scaling of the quality.

To address the issue of consistency, we examined the impurities of commonly used foils. Copper foils have large copper grains, but they suffer from impurities. The highest purity, readily, and commercially available copper source, Cu101 alloy, is 99.995% pure. Here we will show what possible effects the impurities can have on graphene synthesis. Different groups have recognized the presence of white dots after growth through scanning electron microscopy (SEM). These white dots have also been shown to act as

nucleation centers for graphene etching.[22] The reason for these white dots has not been definitively shown.

To address the concern of being able to scale consistent graphene growth, a method that shows promise for scaling is the use of copper films on insulating wafers.[11, 23, 24] The wafers provide a rigid support and are already widely used by industry, while the copper acts as the growth substrate. However, the average mobility of charge carriers using this method is no better than that of graphene grown using copper foils and then transferred. One possible reason for this is the small grain size of the copper film that develops.[25] Even though the surface is <111> textured there are still individual copper grains.[11] The grain boundaries do not impede graphene growth, but they could potentially be a source for reduced carrier mobility. This is because we are transferring a 3D terrain onto a 2D surface (similar to contour mapping).

1.1 OUTLINE

This dissertation is organized as follows. Chapter 2 discusses the roles of impurities found in bulk copper and how they interact during graphene synthesis. A discussion of the impact these impurities have on the quality of the graphene grown is also presented. Chapter 3 discusses the role of surface roughness on the graphene properties. In addition, the graphene is encapsulated to further reduce environmental effects. In chapter 4, graphene synthesis using copper thin film is investigated. The copper grain size of the copper thin film is enhanced to determine if transport properties can be improved with reduced copper. In chapter 5, the conclusions are summarized and future steps are discussed.

Chapter 2: Trace impurities in copper foils

2.1 Graphene CVD growth kinetics

Graphene growth under CVD conditions in its simplest form is illustrated in Figure 2.1. In short, the copper oxide is removed from the surface to allow the carbon precursor access to copper. The copper catalyzes the carbon precursor and carbon diffuses across the surface until finds a nucleation site. Once nucleation has begun, additional carbon atoms that are on the surface add to the initial carbon and form graphene domains. Eventually, the graphene domains will grow so large that they will start to stitch together at boundaries. When copper is no longer accessible the graphene growth will stop even if there is additional carbon.

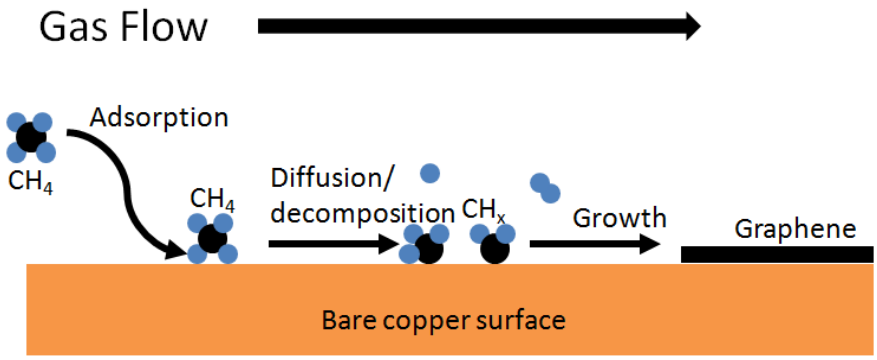

Figure 2.1 Cartoon of CVD graphene growth

There are many different types of CVD growth.[26] The most popular, low pressure CVD (LPCVD), grows graphene under reduced pressure conditions.[16, 27, 28] This type of growth evaporates copper at the same time as growth proceeds. A variant of LPCVD

growth is plasma enhanced growth.[22, 29, 30] Using this type of growth it is possible to achieve low temperature graphene synthesis. Plasma is stuck and the plasma can be used to reduce the copper surface allowing access to the copper metal. Once the copper metal is exposed, the plasma can then be used to break apart the carbon precursors to smaller molecules, which then proceed to graphene growth. This was demonstrated and is true low pressure growth as the temperature in the chamber does not rise above 500°C during the entire growth cycle, as seen in Figure 2.2.[22]

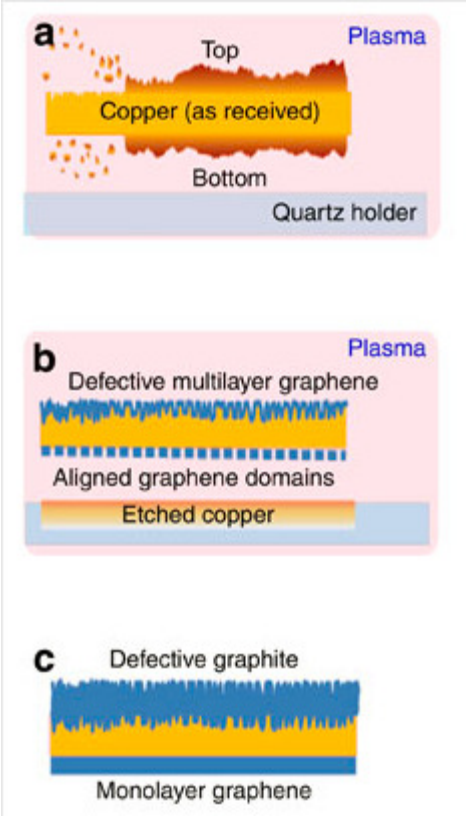

Figure 2.2 Plasma enhanced low temperature graphene growth. Temperature is maintained below 500°C during the entire growth.[22]

An alternative to low pressure growth is atmospheric pressure CVD (APCVD) growth.[16, 17, 31-33] The growth is carried out under atmospheric pressure. This type of growth eliminates the need for a vacuum and its support systems. Using atmospheric

growth there is minimal copper evaporation, so the copper can be reused many more times than the low pressure case. A variant of the atmospheric case is the use of induction heating to heat the copper.[34] This can increase the throughput of graphene growth, since the heating is considerably faster. It is possible to heat the copper foil from room temperature to growth temperature in less than two minutes.

Regardless of the CVD method, the growth steps are essentially the same as outlined in Figure 2.3.

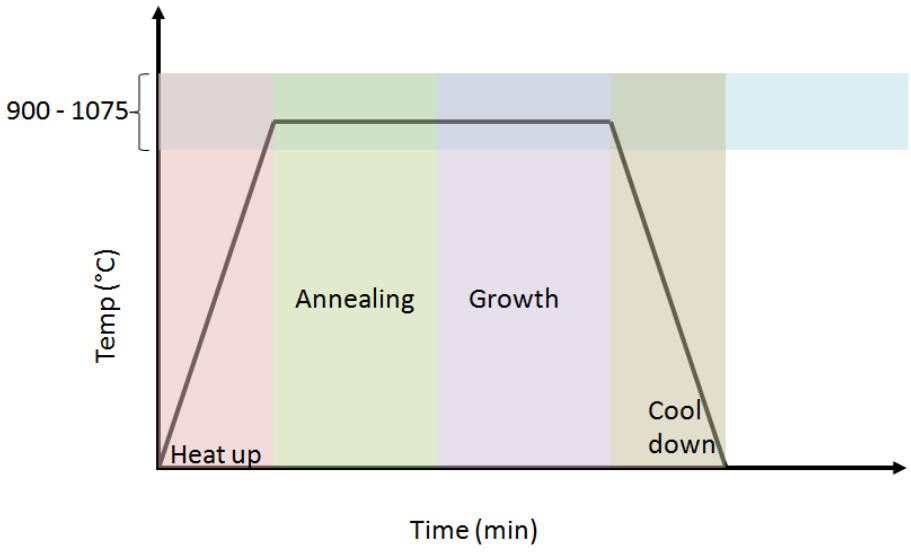

Figure 2.3 Outline of growth steps. Groups around the world have a wide range for growth parameters.

The copper surface is prepared for growth by removing the oxide surface. This is generally accomplished by using a reducing atmosphere while heating the copper. It is possible to reduce the oxide under vacuum and elevated temperature, but evaporation of the copper can occur simultaneously with the reduction. The conditions needed to reduce the copper oxide with just vacuum are shown in Figure 2.4.

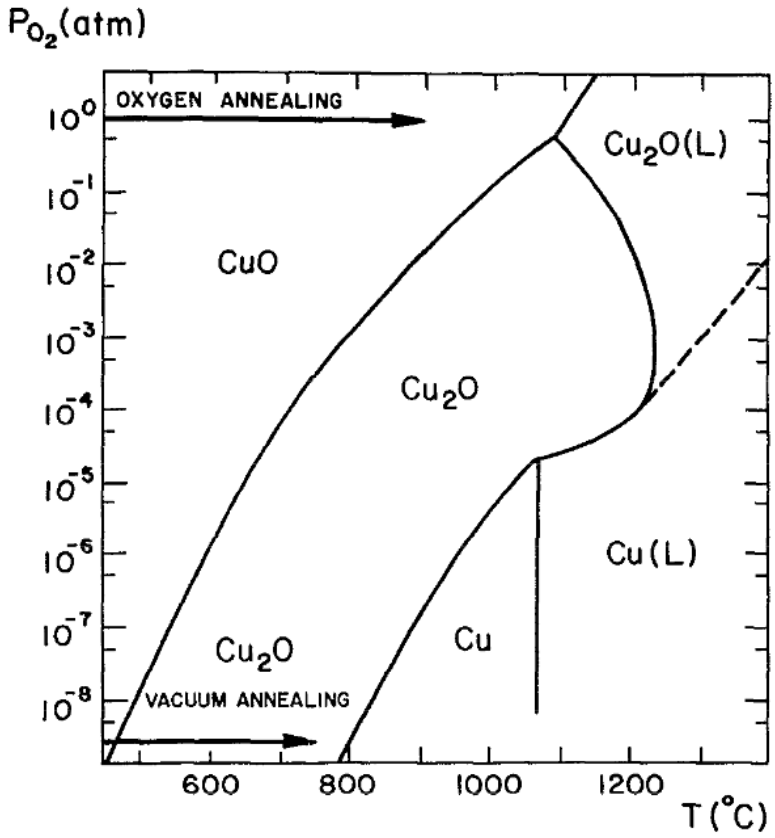

Figure 2.4 Pressure – temperature relationship in copper oxide system.

This process produces a thin layer of copper of the surface, but there is still copper oxide underneath the copper surface, as seen in Figure 2.5.[35] The reduction was carried out at This layering may be useful in the future since we are only concerned with the immediate surface and the underlying copper oxide could provide a more rigid substrate.

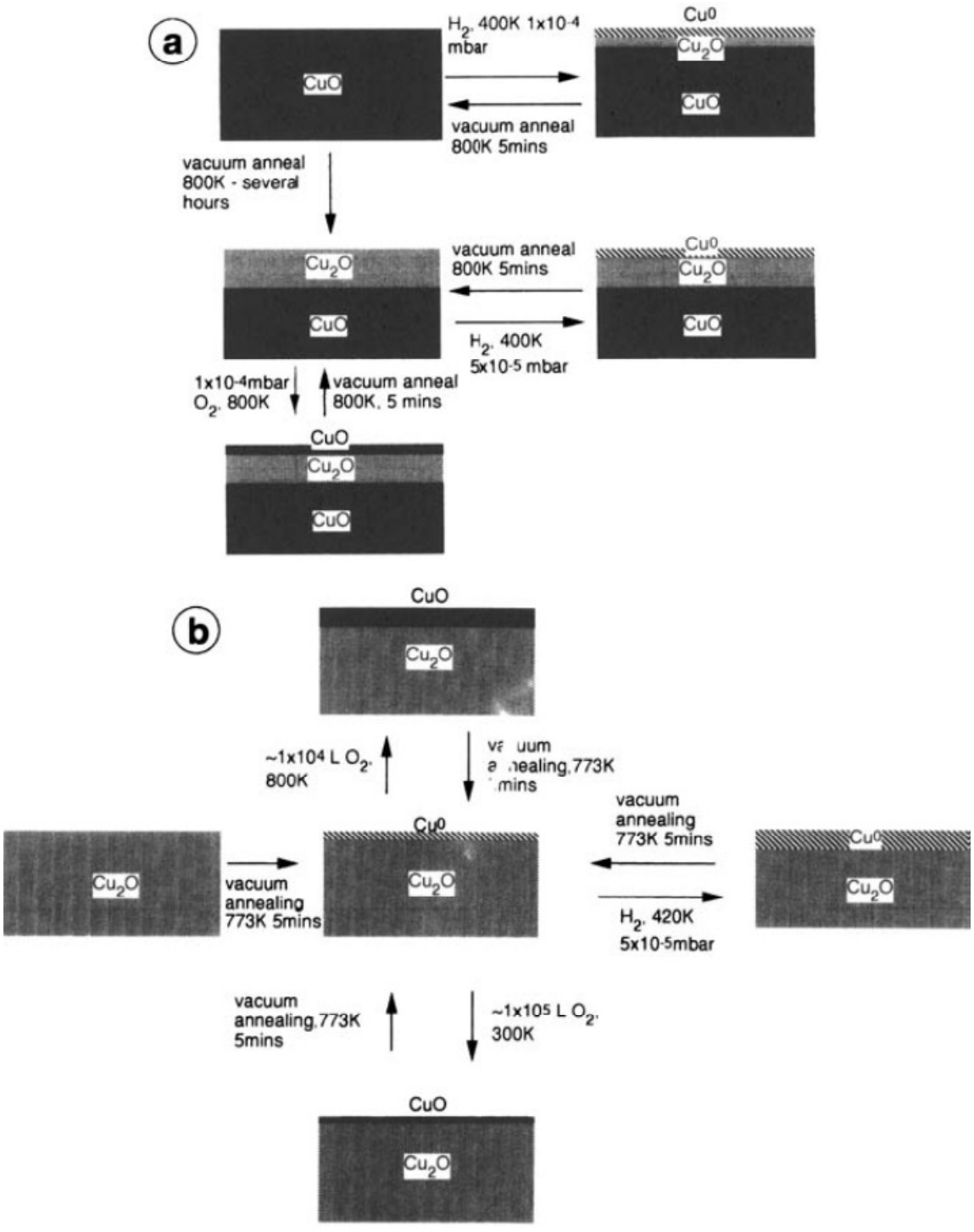

Figure 2.5 Changes to surface composition of CuO (a) and Cu_2O (b), with a variety of oxidation and reduction treatments.[35]

While it is possible to heat the copper oxide/copper to growth temperatures without using a reducing atmosphere, the copper oxide is eventually reduced during growth.[33, 36] Annealing of the copper can be performed but, this step is not necessary, as the annealing is useful for increasing the copper grain size. When the copper is at the growth temperature and copper is exposed to carbon then the graphene growth proceeds. Trace amounts of oxygen and water may be dragged into the growth chamber though leaks in the system can affect the growth kinetics of graphene.[37] After growth has been progressing for a period of time then the copper is cooled down with the growth gases maintained. The growth gases are maintained to prevent etching of the graphene.[38, 39] The etching occurs at defects and one of the largest sources of the defects is particulates on the copper surface.

2.2 IMPURITIES

The synthesis of monolayer graphene on copper is due in large part to the limited solubility of carbon in copper.[40-42] As a result, synthesis is a surface mediated process and one aspect of the resulting graphene quality is based on the condition of the surface. Of the different impurities that can be found in copper, the most troubling are the oxides can not be reduced in a graphene growth environment. Copper readily forms alloys with numerous elements, as is demonstrated by the various alloys (brass, bronze, bell brass, red bronze, to name a few) mankind has used over the years. The level of purity that we have needed copper to be at has never been as vital as it is to graphene growth, since just

the surface is used for synthesis. This issue has been given a cursory examination but we will examine it much further.[43]

Generally, copper is annealed prior to growth in a reducing environment. The main function of the annealing is to increase the grain size of the copper. The copper oxide that was present on the surface of the copper is reduced during the heat up, as well as during the initial stages of annealing. As shown in Figure 2., there could be trace impurities in the copper oxide, as well as the copper bulk. At elevated temperatures the surface of the copper becomes highly disordered. Theoretical calculations have demonstrated that the copper surface is essentially molten by surface melting.[44, 45] During annealing we are also allowing the growth of impurity particles on the surface.[46] The oxidized trace impurities, which are embedded in the copper oxide layer, can diffuse across the surface to form larger visible particles.

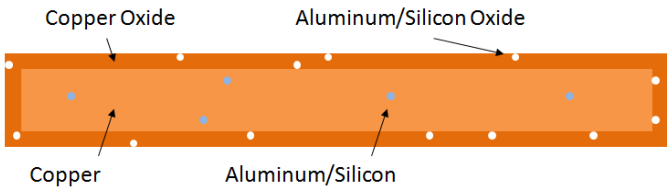

Figure 2.6 Impurities of concern within copper from vendors. Since these particles are small there is a low chance for them to drift away after the copper oxide is reduced.

To reduce the density of particles formed on the surface during annealing, we can remove the oxide prior to annealing/growth. Methods of copper oxide removal can be chemical or mechanical. However, the methods to remove the copper oxide do not necessarily remove all impurities. The use of chemical removal methods can leave some

impurities since some impurities are resistant to the chemical treatment. In addition, the methods used to remove the oxide can also impart their own impurities via residue. Chemical removal methods can entail the usage of an acid. Acetic acid is a selective acid that targets the copper oxide and leaves the copper alone.[47] The reaction that occurs to the copper oxide when using acetic acid is as follows:

$$CuO + 2CH_3COOH \rightarrow Cu(CH_3COO)_2 + H_2O \quad [2.1]$$

$$Cu_2O + 4CH_3COOH \rightarrow 2Cu(CH_3COO)_2 + H_2O + H_2 \quad [2.2]$$

Even though this is a selective acid, if the copper is left in the acetic acid for too long (~1 week) there will be the formation of copper acetate crystals on the copper foil itself. This could be caused the oxygen dissolution into the acetic acid, which oxidizes the copper. The newly formed oxide is then reduced and this cycle continues. After a period of time the concentration of copper acetate reaches saturation and crystals start to form using the copper surface as a nucleation site. The surface of the copper after overnight treatment in acetic acid is quite rough and we can still see evidence of impurities, Figure 2..

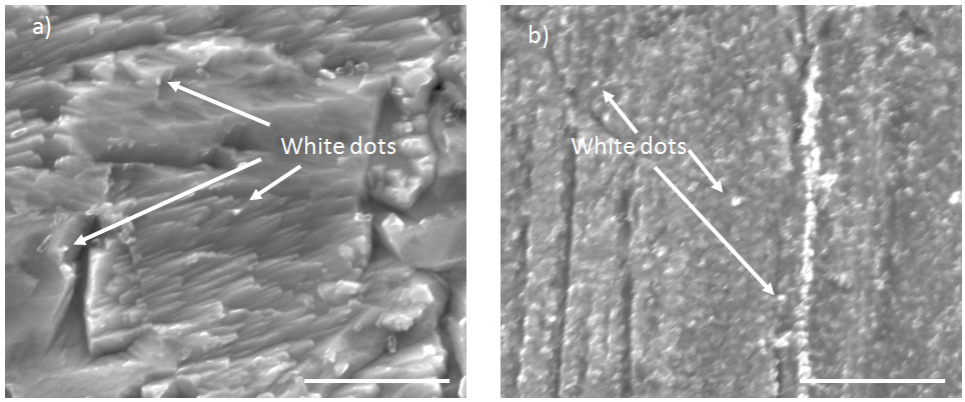

Figure 2.7 Appearance of white dots within copper oxide layer of (a) Alfa Aesar 99.8% copper and (b) Eagle Brass Cu102 copper. The arrows do not indicate all of the white dots as there are many present. Scale bar is 4 μm.

After the copper is removed from the acetic acid; there is the formation of a native oxide. This native oxide is thin compared with the oxide originally from the manufacturer as shown in Figure 2. using time-of-flight secondary-ion-mass-spectroscopy (TOF-SIMS).

a)

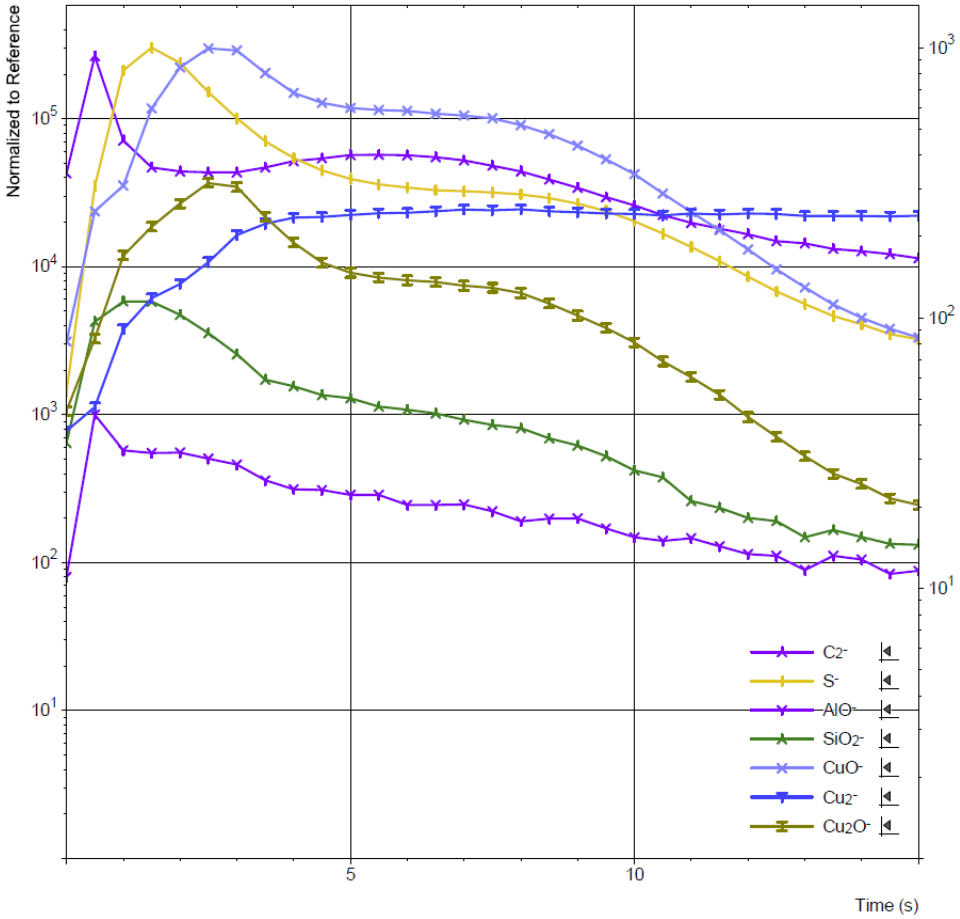

Figure 2.8 TOF-SIMS of (a) as-received Cu102 foil

b)

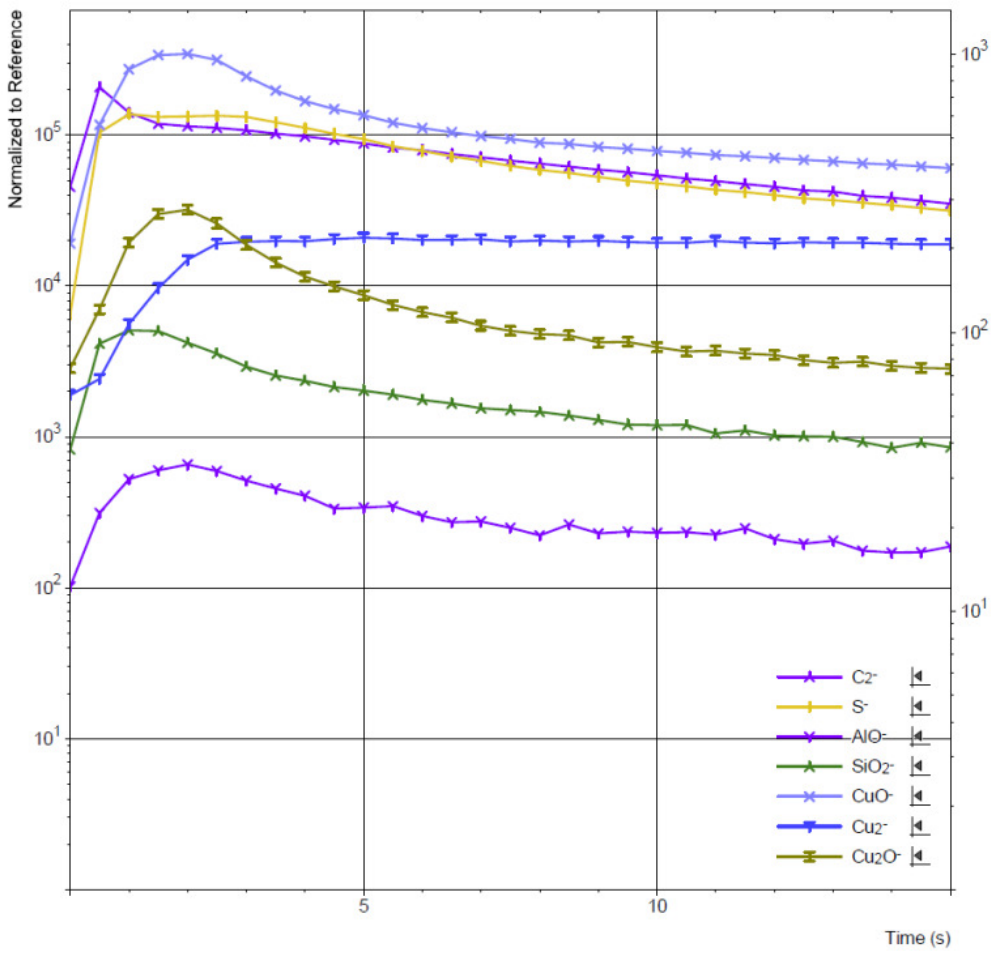

Figure 2.8 TOF-SIMS of (a) as-received Cu102 foil and (b) Cu102 foil after overnight etching in glacial acetic acid. The carbon and copper oxides have been removed as evidenced by the lack a shoulder on the respective lines. The presence of the same elements even after pre-treatment is due to the formation of a native oxide and interaction with atmosphere immediately after removal from the acid.

Additional etchants include dilute hydrochloric acid (HCl) and ammonium persulfate. HCl will not etch copper, but it will not etch copper oxide either. HCl undergoes a displacement reaction with the copper oxide, converting the copper oxide to copper chloride as follows:

$$CuO + 2HCl \rightarrow CuCl_2 + H_2O \quad [2.3]$$

$$Cu_2O + 2HCl \rightarrow 2CuCl + H_2O \quad [2.4]$$

Ammonium persulfate, typically used to etch the copper for transfer of graphene, is not selective of the material removed and if neglected the entire piece of copper could be etched away.

Mechanical means can leave particulates on the surface from the mechanical removal/polishing of the oxide layer. Progressively higher grits can be used to smoothen the surface of the copper and remove the oxide. Due to the ductile nature of copper, the particles used to remove the oxide from the surface of the copper can become embedded. After annealing, these impurities can act as a nucleation site for the growth of graphene. The impurity may or may not react with the carbon precursor depending on the type, either reducible or non-reducible. Reducible impurities would be elements, such as iron and nickel. Non-reducible impurities would be elements that form high temperature oxides, such as silicon and aluminum.

Reducible impurities may cause the formation of ad layers, since the elements previously mentioned have some slight carbon solubility. The impurities could increase the amount of carbon in an isolated area before diffusing back into the bulk. For non-reducible impurities, their presence increases the number of nucleation sites, as shown in Figure 2.. Increasing the number of nucleation sites, can lead to an increasing number of graphene domain boundaries. These boundaries can cause the overall electrical

performance of the graphene to degrade. Alternatively, as the graphene is growing, an oxide particle can interfere with the graphene domain growth front. This can cause the graphene to grow around the oxide reducing the performance of the graphene grown.

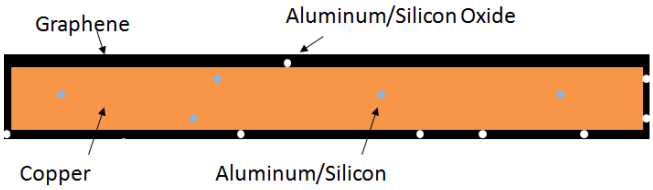

Figure 2.9 Oxide particle interaction during graphene growth. Oxide particles formed during annealing can act as nucleation sites. Oxide particles formed during growth can interfere with graphene domain growth.

2.2.1 Reducible trace impurities

The most commonly found trace impurity that can be reduced under normal graphene synthesis conditions is iron. Iron is present in trace amounts and is seen occasionally during EDX of copper. To determine the effects of large amounts of iron in copper, we introduce iron on the surface by the use of dilute iron chloride dissolved in ethanol. When we use this method the iron chloride will reduce to the metal iron under hydrogen flow and then diffuse into the copper. Since the iron is near the surface it will have the greatest chance for interaction with the graphene precursor gases. This amount of iron present near the surface is far greater than the amount present in the copper, but this will allow us to clearly demonstrate the effects of iron on graphene growth. Half of the copper was dip coated in the solution and allowed to air dry. The copper foil was then taken through the same growth as a normal piece of copper. Before growth there is a clear indicator of where the iron chloride is, however, after growth it becomes harder to identify where the iron was placed. Figure 2. shows the copper foil before and after

growth. The contrast difference in the images illustrates the difference between monolayer and multi-layer.

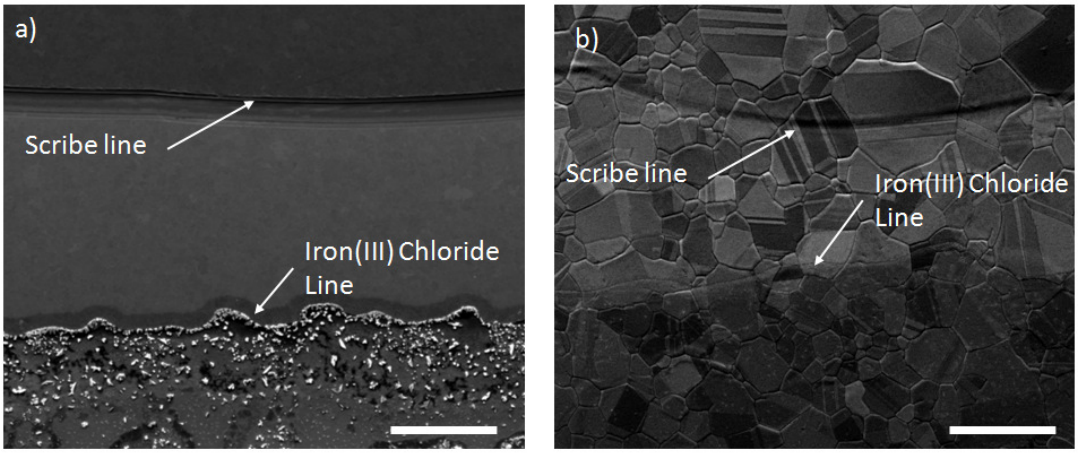

Figure 2.10 Copper foil with iron chloride coating (a) before graphene growth process. Iron (III) chloride crystals present on surface. (b) Appearance of multiple layers on surface of copper in presence of iron. Darker region below iron (III) chloride line is multi layer graphene. Scribe line to aid in optical microscopy. Scale bar is 100 μm.

The increase in the number of layers of graphene grown from copper alloys was demonstrated with nickel.[48] In this case, the alloy was a 70/30 Cu/Ni mixture. The alloy behaved similarly to using nickel, in that if the metal was quenched then the number of layers is one or has very few adlayers. Allowing the metal to slowly cool down increased the number of graphene layers. Since we only applied iron(III) chloride to one portion of our copper, we only grew multiple layers in the affected region. This was confirmed using Raman, Figure 2.. The spectra far away from the dipped region showed monolayer graphene, whereas near the iron(III) chloride we were getting area that were mixed monolayer and multilayer.

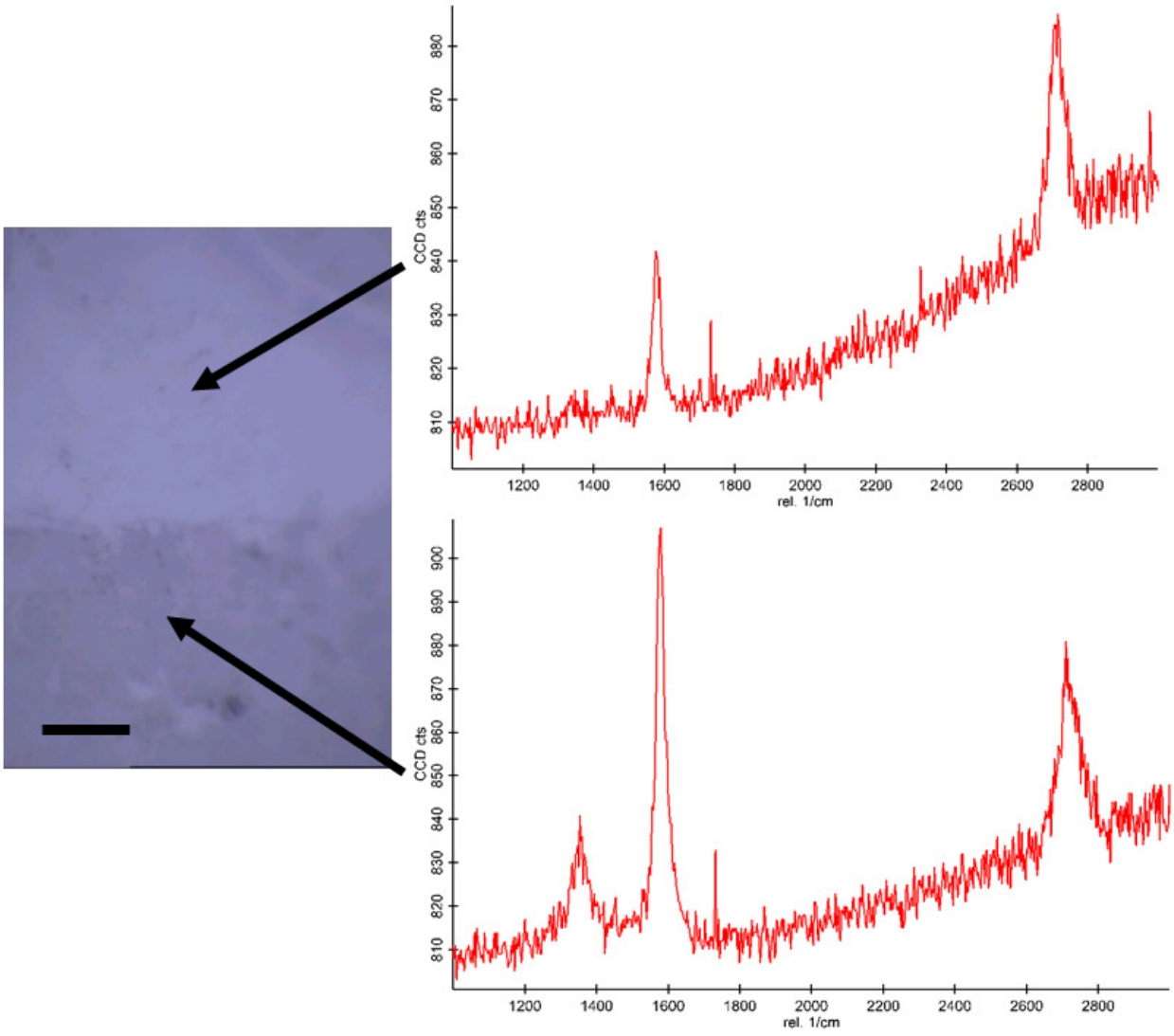

Figure 2.11 Raman comparison of iron(III) chloride treated region vs as received region. Light colored region is as received and darker region is iron (III) chloride treated region. Scale bar is 10 μm.

2.2.2 Non-reducible trace impurities

The roller used during the production of foils can impart different impurities. We have shown that if the impurities are reducible in the copper during normal graphene growth conditions, then they are of little concern. The impurities that need to be taken

into account are silicon and aluminum based. These impurities can come in the form of dust in the manufacturing environment or the materials used to maintain the equipment.

2.2.2.1 Possible Sources

There has been discussion as to the source of white dots on the copper surface after growth.[49] In order to demonstrate the most likely source of the particles different experiments were undertaken to highlight where origin of the particles could be. One thought is that the particles come from the quartz tube that is used for graphene growth, the quartz being the large source of silicon. Two different experiments were carried out to demonstrate that the source of the particles could not be from the quartz tube.

The simplest metric to illustrate that the particles are not coming from the quartz tube is that there is not an accumulation of particles near the edges of the copper where the copper comes into contact with the tube itself. There should be a gradient of particle density from high concentration (touching the tube) to the center to the copper foil every time there is graphene growth. An example of this is from copper film used in Chapter 4. The copper film was covered, but the edges were still exposed to the environment. There is a white dot gradient from the edge to the center, shown in Figure 2.. The particle source is the silicon from the SiO2/Si chip the copper film was evaporated onto. It was possible for some silicon to vaporize and enter through the gaps in the cover.

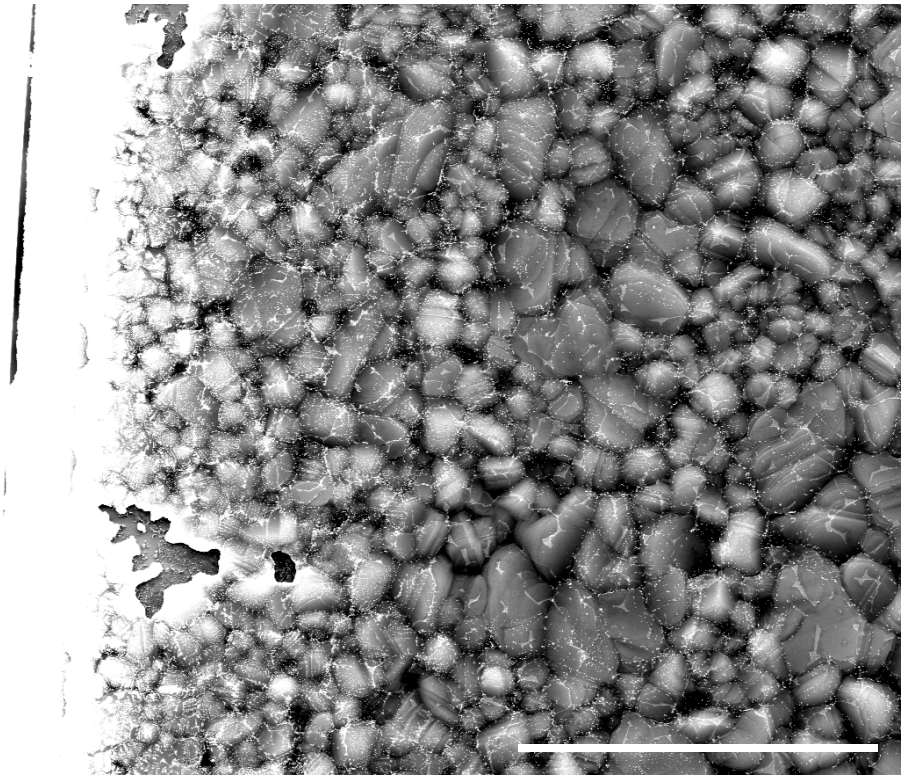

Figure 2.12 SiO_2 particle gradient on copper film. The edge of the copper film exposed to the environment is on the left; hence the concentration decreases moving from left to right. Scale bar is 40 μm.

Another method to demonstrate that the quartz tube is not the source of particulate was to use different copper foils annealed in an alumina (Al_2O_3) carrier tube placed inside of a quartz tube. A carrier tube was chosen since alumina is opaque and thus we would not be able to accurately place the copper within the heat zone of the furnace properly. The copper foils were annealed and examined under SEM. There was no difference between foils annealed in a plain quartz tube compared with those annealed in an alumina tube.

Copper of different purity levels were chosen to examine the levels of non-reducible impurities in copper. The copper sources used are shown in Table 2.1.

Table 2.1 Copper source and purity levels of copper.

Source	Purity listed
Alfa Aesar (25um)	99.8%
Mitsui Mining and Smelting Co. Electrodeposited and Polished (~35um)	99.4%
Eagle Brass Cu 102 Alloy (125um)	99.95%
Alfa Aesar Puratronic grade (250um)	99.99999%
McMaster Carr Cu101 Alloy (~600um)	99.995%
Evaporated copper film (0.8 – 1.5 um)	>99.9999%

All of the samples were individually annealed for 15 minutes in keeping with the graphene growth recipe for atmospheric pressure CVD (Appendix B). The evaporated copper film showed no signs of oxide particles on the surface, which is to be expected since during the evaporation process any oxides that form are left in the source crucible, the exception being near the edges as indicated in Figure 2.. The remainder of the copper sources had varying amounts of particles. Even though the Mitsui foil had the lowest listed purity levels, it had the least number of particles on the surface.

2.2.2.1 Impurities in the oxide layer

Each piece of copper was placed in acetic acid to strip off the oxide down to bare copper. In removing the copper oxide, we are also removing other copper compounds that could have formed on the surface of the copper as well.[50] Additionally, there could also be layers of other compounds that may have introduced during the processing to produce the foil. We examined the first four copper foils in Table 2.1 with TOF-SIMS to determine the layering of the materials on the surface of the copper. The Alfa Aesar 99.8% foil, Figure 2.a, has a thin layer of chromium, but that is expected. The Mitsui foil, Figure 2.b, has practically no aluminum oxide when compared to the other foils. The Cu102 alloy, Figure 2.c, had the thickest oxide layer of the four compared, as seen by the broad shoulder before crossing the copper line. The Alfa Aesar 99.99999% pure copper foil, Figure 2.d, had a very thin oxide layer. The oxide layer has been theorized to be related to the purity of the foil with higher purity copper oxidizing slower.[51]

a)

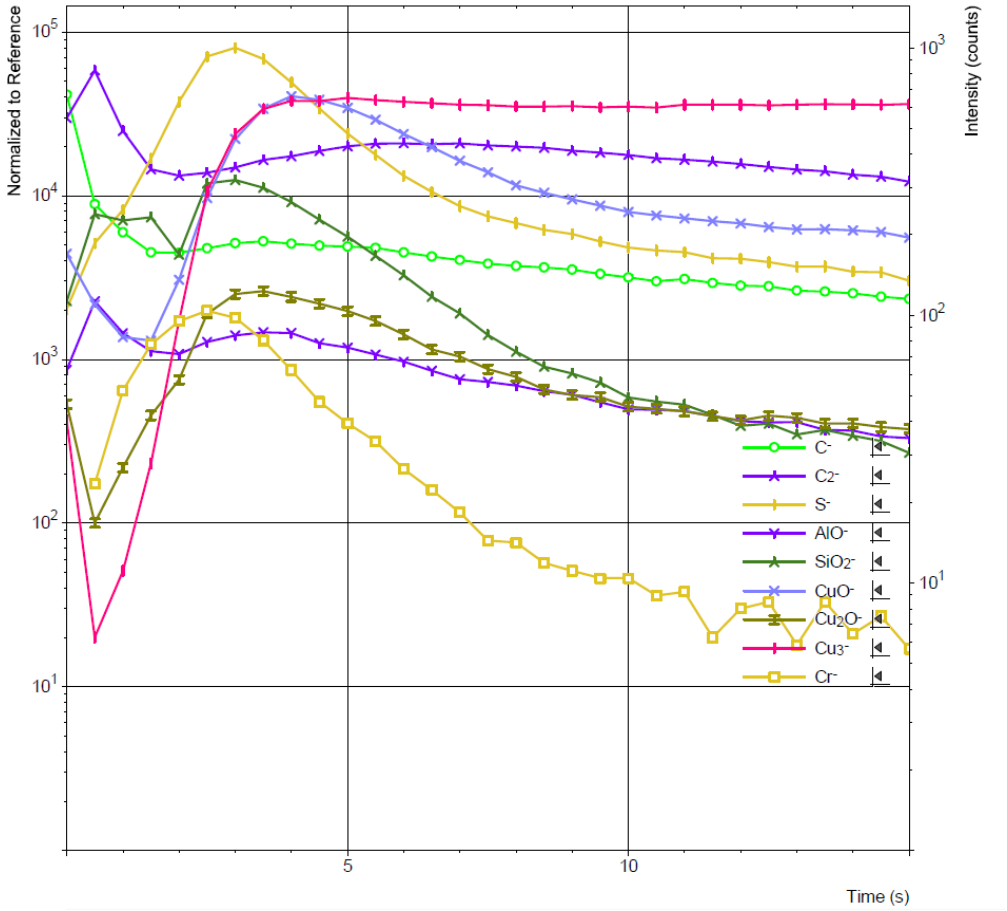

Figure 2.13 TOF-SIMS of (a) Alfa Aesar 99.85 purity

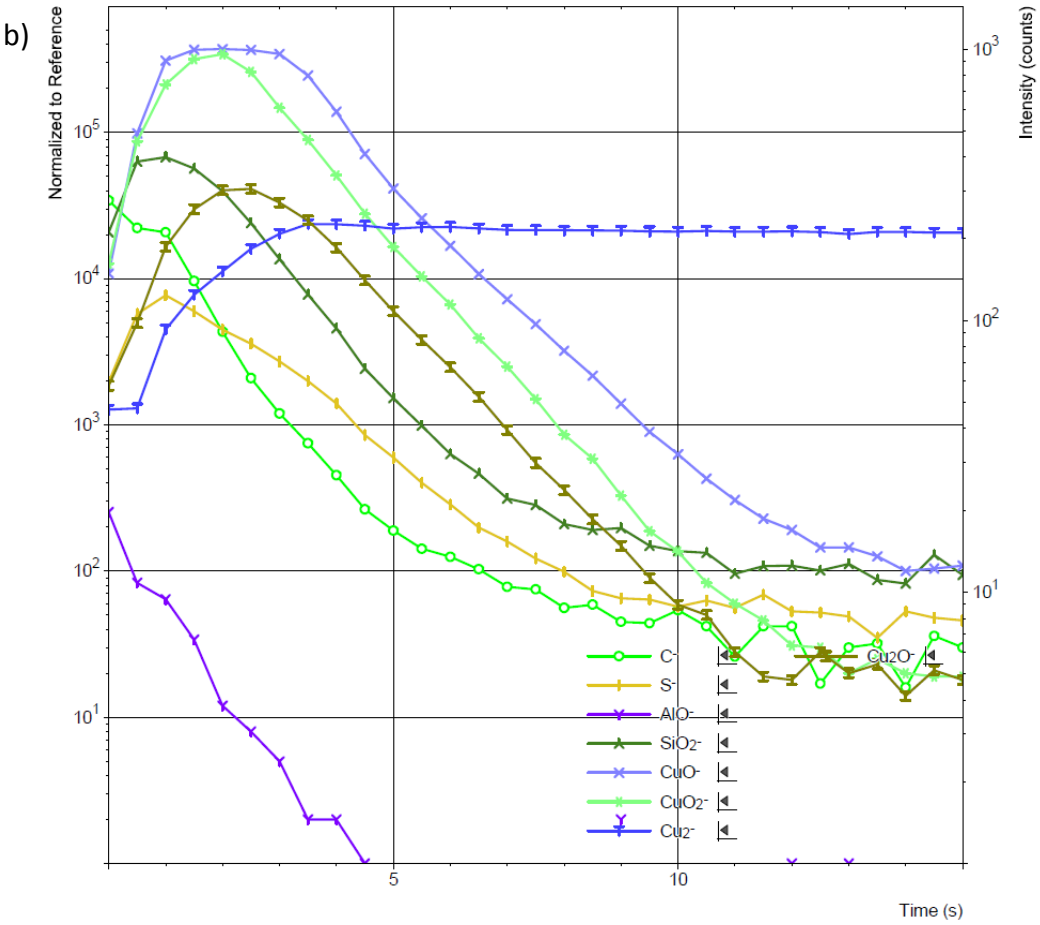

Figure 2.13 TOF-SIMS of (b) Oak Mitsui 99.4% purity.

c)

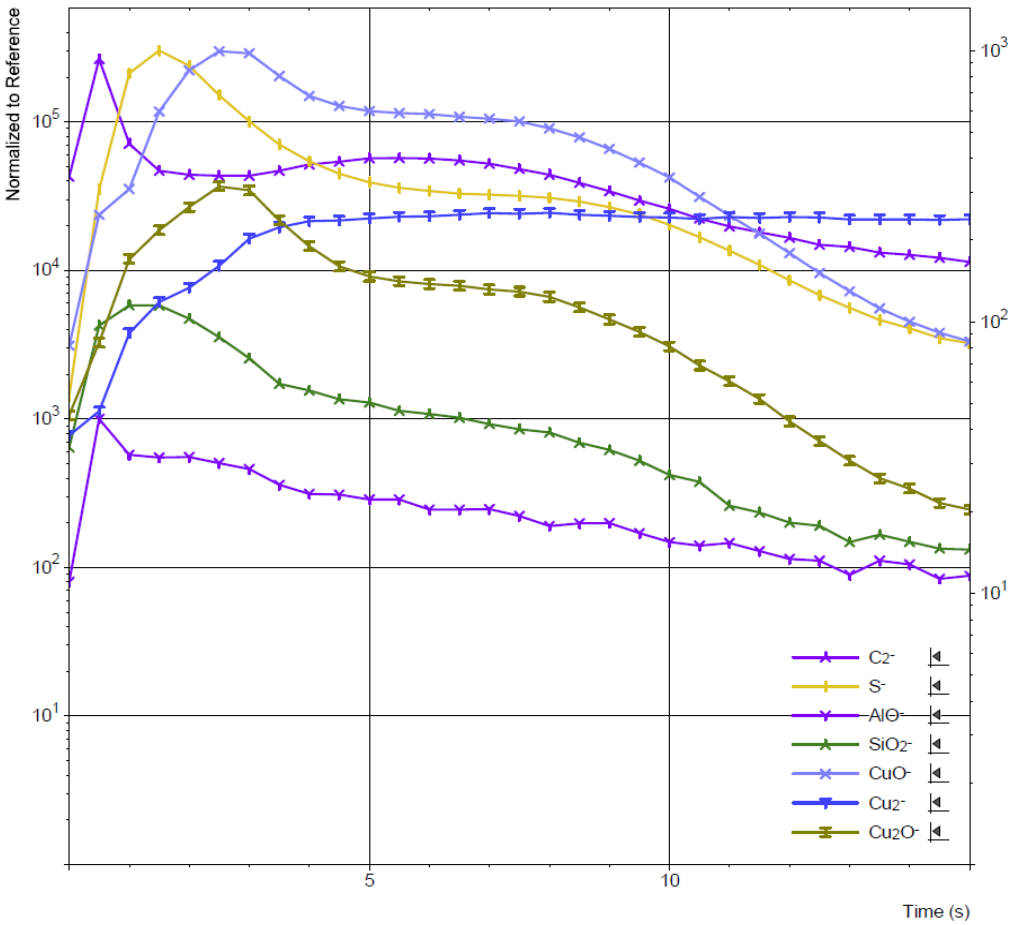

Figure 2.13 TOF-SIMS of (c) Eagle Brass Co 99.95% purity

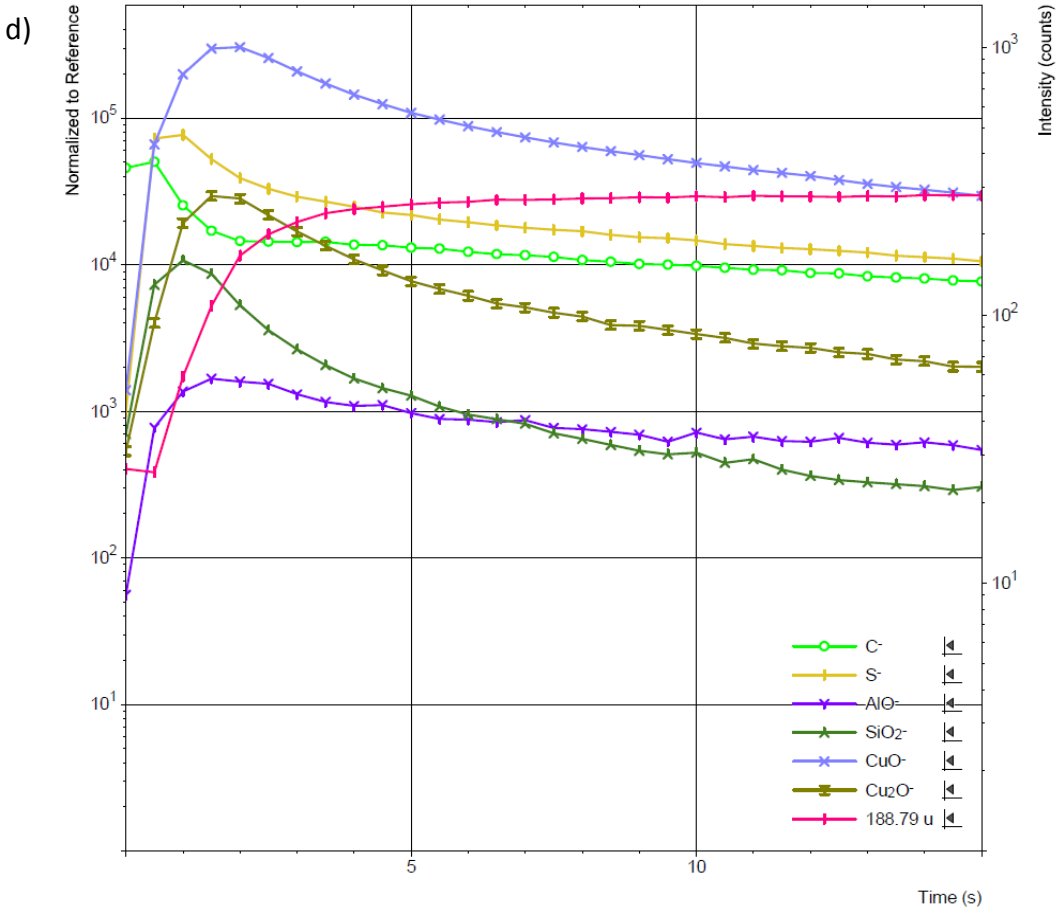

Figure 2.13 TOF-SIMS of copper foils of varying purity (a) Alfa Aesar 99.85 purity, shows chromium layer as told by vendor. (b) Oak Mitsui 99.4% purity, show an extremely low concentration of aluminum compared with other foils. (c) Eagle Brass Co 99.95% purity, shows a wide oxide layer. (d) Alfa Aesar 99.99999% purity.

A new native oxide layer forms once the copper is removed from the acid pre-treatment. This oxide layer again reacts with the various gases in the atmosphere to reform a patina; however, this patina is much thinner and as a result has less overall contamination as previously shown in Figure 2.b.

To better illustrate the presence of non-reducible impurities, 99.8% purity, Alfa Aesar copper foil was fully oxidized to ensure the impurities are oxidized as well. The copper oxide was then crushed and reduced under a hydrogen atmosphere in a quartz boat to minimize damage to the graphite crucible, as there will be water that evolves during the reduction process. This water can damage the crucible at the high temperatures that the reduction takes place. The newly reduced copper was then melted in a graphite crucible to allow insoluble oxides to the surface. A thin layer of oxides formed on the surface of the copper after cooling as shown in Figure 2..

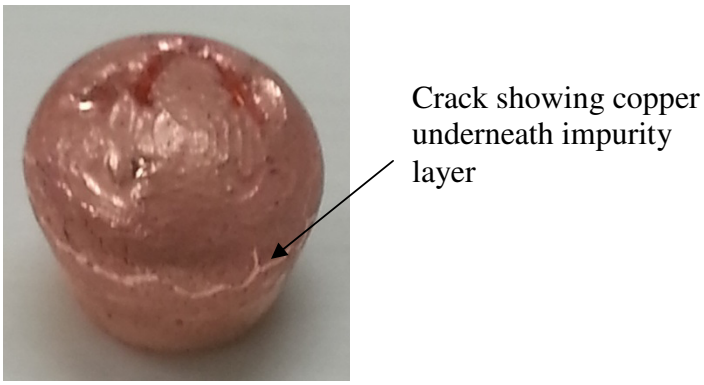

Figure 2.14 Copper ingot after oxidation processing. The crack is exposing copper underneath oxide layer. The purity of the starting copper is 99.8% from Alfa Aesar.

Afterwards, the oxide layer was removed and melted again. Following the melting there was additional oxide that came to the surface. The additional oxide that came to the surface is due to the impurities not being given enough time to segregate from the copper bulk. The oxide particles that were located within the bulk are not greatly affected by gravity and thus need more time to allow for migration to a free surface.

This method was repeated using the Cu101 alloy from McMaster Carr and a graphite mold to produce a usable copper piece with dimensions of 0.5 in x 2.5 in. The

copper piece experienced the same particle diffusion to the surface as the copper ingot as expected, but with a lower density since the starting material had a higher purity. Even though the impurity concentration was lower, impurities are still present in levels high enough to cause particles to come to the surface after repeated removal/melt cycles, similar to the copper ingot. Perhaps the usage of centrifugal melt casting would improve this process to the point where a copper piece can be relatively free of particles in a reasonable amount of time.

2.3 IMPURITY EFFECTS ON ELECTRICAL PERFORMANCE

To determine if the oxide particles that accumulate on the surface play a role in the quality of graphene, we chose to use the Mitsui foil. The relative lack of particles on the surface after growth allows us to introduce our own particles on the surface to see if there is an effect on electrical properties of graphene grown. In addition, the foils have been polished to achieve a low surface roughness (R_a ~ 20nm). Having a smooth surface will reduce the chances for particles to become immobilized during surface diffusion. We dip coated the foil in different concentrations (100 ppm, 10 ppm, and 1 ppm) of 3-5 nm SiO_2 particles suspended in ethanol. Ethanol was chosen to prevent the coffee ring effect from occurring as the solvent was evaporating.[52] SEM images taken after drying show a fairly even dispersion with clustering occurring at the higher concentrations. The dispersion of the nanoparticles is such that as we progress to higher concentrations in Figure 2.1, we see either larger cluster density or larger overall cluster size.

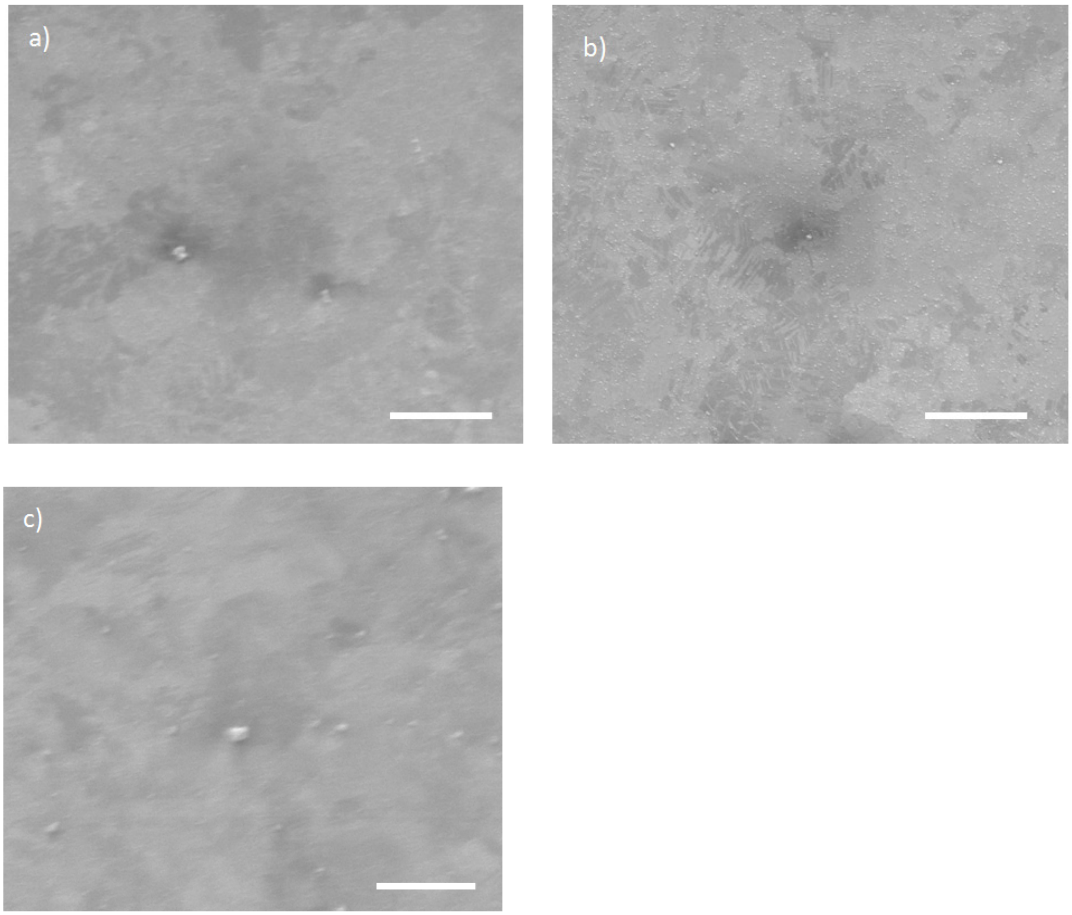

Figure 2.15 SEM images of SiO_2 nanoparticles after dispersion on Oak Mitsui foil. The nanoparticles were suspended in ethanol and dip coated onto the surface. Concentrations of suspended nanoparticles are (a) 1ppm, (b) 10 ppm, and (c) 100ppm. Scale bar is 10 μm.

As previously mentioned, at elevated temperatures, nanoparticles are free to diffuse across the surface and will agglomerate, this is shown in Figure 2.. There are some areas where the clusters have come together to forms a more coherent sphere. The situation in the image is not in this case; this is most likely due to the initial particle size of the nanoparticles used.

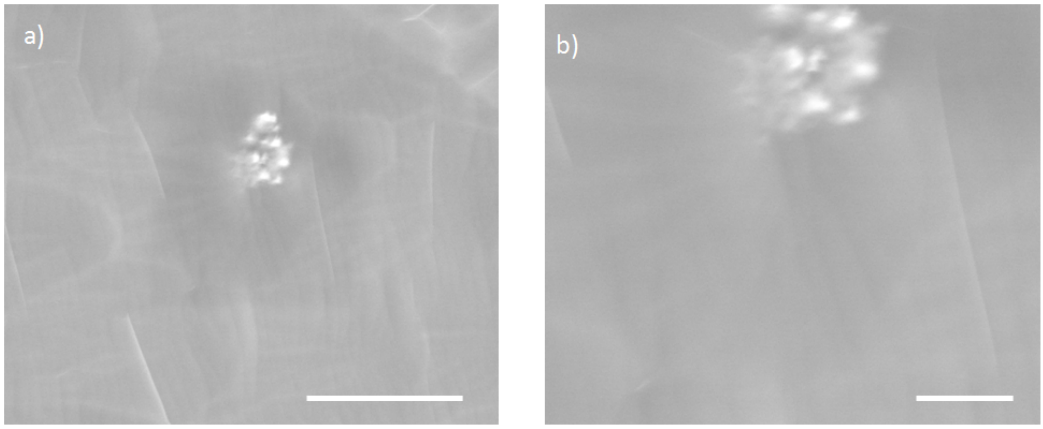

Figure 2.16 Example of nanoparticle agglomeration. (a) Cluster of SiO_2 nanoparticles. Scale bar is 4 μm. (b) Closer magnification of same cluster. Scale bar is 1 μm.

As expected, upon increasing the SiO2 nanoparticle concentration we have increased the density white dots on the surface of the copper. The number of clusters has also increased as seen in Figure 2..

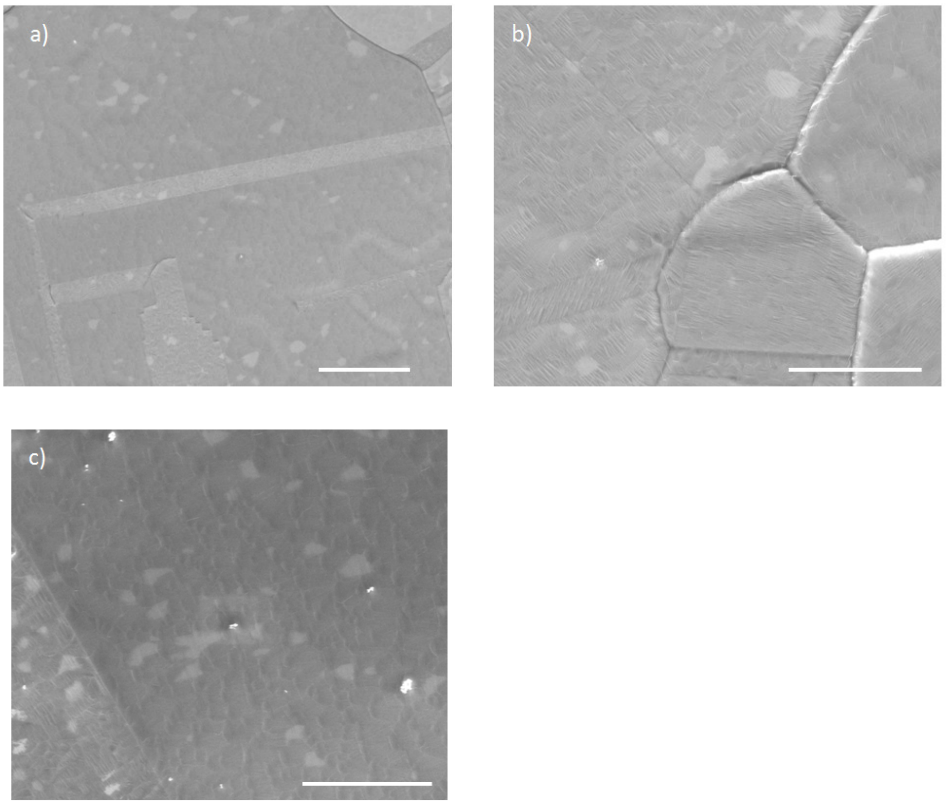

Figure 2.17 Controlled SiO_2 nanoparticle distribution after graphene growth. (a) 1 ppm nanoparticle concentration. Scale bar is 50μm. (b) 10 ppm nanoparticle concentration. White dots are located long copper grain boundaries. Scale bar is 30 μm. (c) 100 ppm nanoparticle concentration. Voids are likely etching of graphene during cooldown. Scale bar is 30 μm.

To determine the effects of impurities on electrical performance, we fabricated field-effect transistors to determine its electrical characteristics. A shadow mask was used to define our devices and electrical measurements were performed using typical setup with a widely used diffusive transport model for mobility extraction. We measured the electron and hole mobilities of the devices and analyzed the results to see if there was a statistical difference between the different concentrations, Figure 2.. Even though there

were differences in mobilities between the different concentrations, they were not significantly different enough to say that there was a marked drop in performance based on the difference in concentration. The cause is most likely the surface diffusion of the particles during the annealing phase of graphene growth.

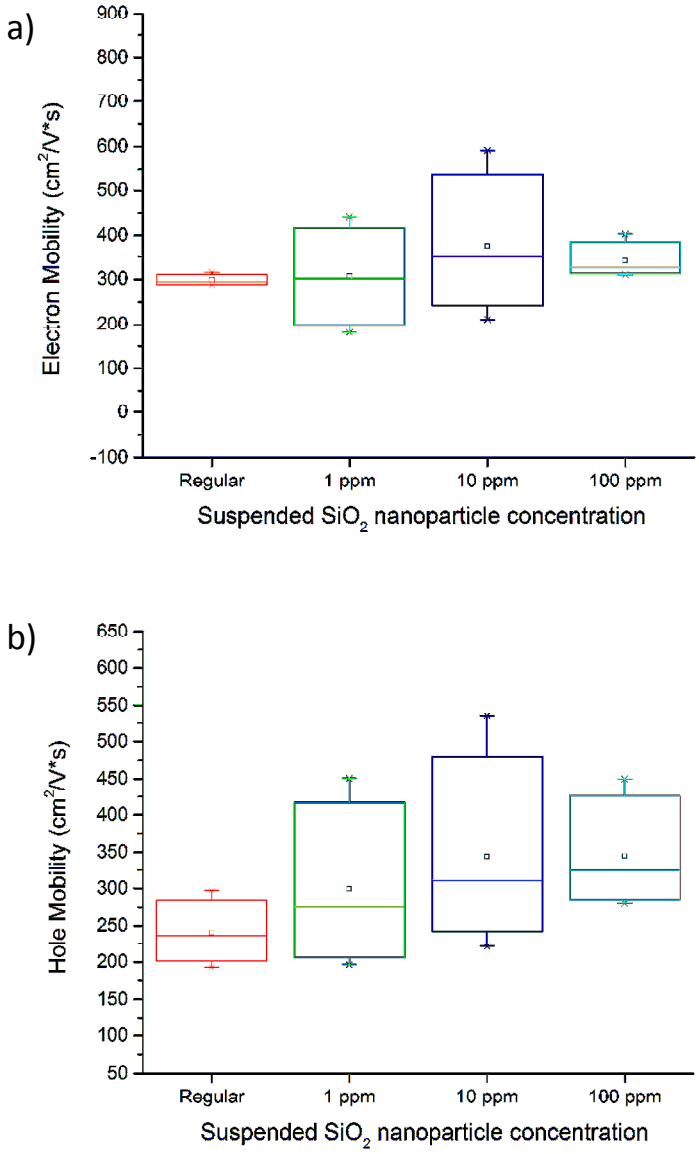

Figure 2.18 Statistical analysis of electron and hole mobility as a function of SiO_2 nanoparticle surface concentration. The average mobility between different surface impurity concentrations is not significantly different.

2.4 SUMMARY

Impurities within the copper impact the surface topology and ultimately graphene performance. The impact on device performance due to the impurities that diffuse to the surface is not as great as the large quantity of impurities that are located in the as received oxide layer. Reducible impurities can diffuse to the surface and aid in the formation of adlayers during graphene growth. These reducible impurities have a pathway to diffuse back into the bulk before interaction with the carbon precursor thus reducing their impact on the graphene.

Non reducible impurities on the surface during normal graphene growth conditions can interfere with graphene growth and its properties after growth. The easiest method to reduce these impurities is to remove the surface layer of the copper prior to growth. It is within this layer that we have pre-oxidized non reducible impurities. We could reduce this layer during the annealing step but we have seen that different vendors have different oxide layer thicknesses, thus different potential concentrations of non reducible impurities. Even if we remove this layer there is still the potential for impurities to diffuse to the surface and interact with the trace oxygen in the system. We have shown that removal of the oxide does not necessarily mean the removal of all the particles in the oxide.

We have demonstrated that even though there are impurities on the surface they can still diffuse across a smooth surface and agglomerate. They key being a smooth surface. If the surface is rough then the diffusion may not proceed as hoped and we would have a significantly performance difference. Since large areas of polished foils may be difficult to acquire, a different approach to reducing surface roughness is needed.

Chapter 3: Surface Roughness of Copper Foils[1]

3.1 ELECTROPOLISHING THE SURFACE

Electropolishing on copper foils has been investigated in order to reduce the surface roughness and to enable the growth of a more uniform monolayer.[16, 53, 54] A smoother surface is achieved through electropolishing by preferentially etching microscopic peaks in the metal surface to reduce the nucleation density by reducing the number of sites which atoms can start growth from.[55, 56] The use of electropolishing also removes particulate that may be embedded within the oxide covering the surface.[57] The use of electrochemistry to selectively etch the copper surface relies on using the appropriate potentials, as seen in Figure 3.1.[58] For copper the polishing regime is typically 3-6V. The higher the potential the faster then polishing occurs, but then the risk of pitting of the surface due to gas evolution becomes greater.

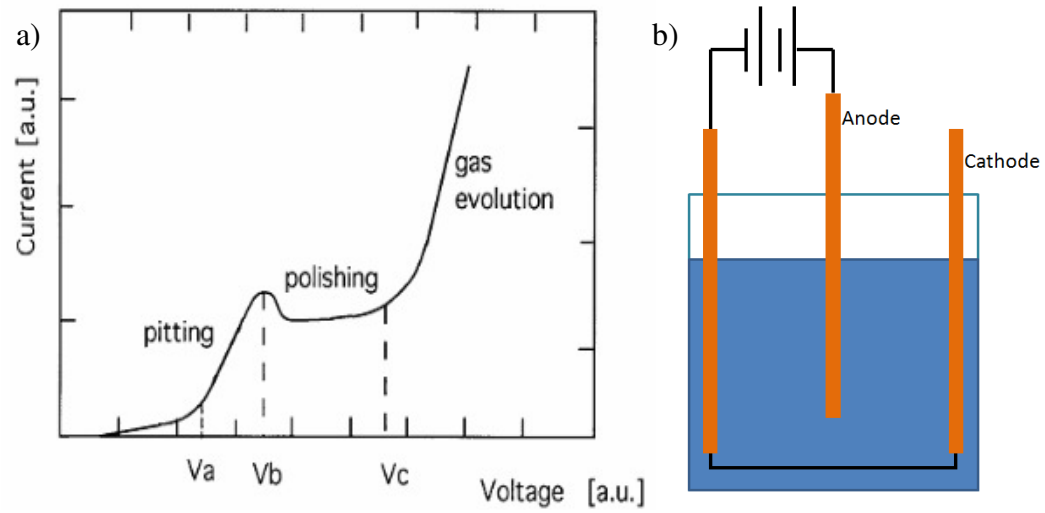

Figure 3.1 (a) Current density vs voltage of electropolishing copper.[58] (b) Physical arrangement of copper. The piece to be polished is the anode.

[1] This chapter is based on:
Ha, T.-J.; Lee, A. "Chemical vapor deposition grown monolayer graphene field-effect transistors with reduced impurity concentration." Electron. Mater. Lett. 2015, 11, 552-558. A.L. did the electropolishing and graphene growth. T.J.H performed electrical characterization and measurements

The surface of the copper becomes smooth in the polishing regime due to the peaks of the copper having a higher electric field than the remainder of the copper. As shown in Figure 3.2, this causes the dissolution of the copper to preferentially occur at that location, regardless of whether it is at a peak or in a valley.[58]

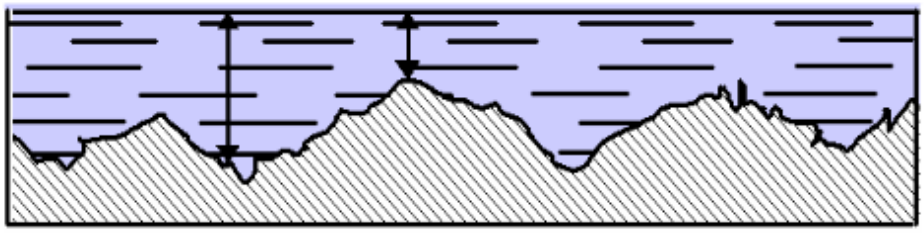

Figure 3.2 Removal of peaks at copper anode during polishing. Peaks have a higher electric field and are etched first.[58]

Such a technique can be used to obtain high-performance GFETs comprised of a more uniform graphene monolayer. Some studies on the effect that the electropolished copper foils have on the quality of graphene have been reported elsewhere. However, an overview of the device physics responsible for the restorative effect of the electronic characteristics in monolayer GFETs regarding impurity concentration has not been fully provided.

We observed improvements in the electrical properties of monolayer GFETs encapsulated with the appropriate amorphous fluoropolymer. We note that some reports have discussed improved electrical characteristics in GFETs due to the amelioration of disorder and/or defect characteristics in graphene films. However, very few of these studies have investigated the reliability of such a simple and general technique in minimizing device-to-device variation and long-term stability upon exposure to ambient air, including oxygen and water molecules. Furthermore, minimal attention has been given from an engineering point of view to the process optimization combined with pre-

and post-treatment to restore the electrical characteristics of GFETs for use in large-area electronics.

3.2 CHARACTERIZATION AFTER GROWTH AND TRANSFER

Electropolishing on the copper foils results in a decrease in the surface roughness (R_a) of the copper from ~200 to ~60 nm. The advantage of electropolishing when compared to conventional polishing is that fewer residues are left behind on the surface of the material. Since copper is a soft metal, there is a chance that some of the abrasive from conventional polishing might become embedded in the copper during the polishing process. Once embedded, it would interfere with the graphene growth by acting as a nucleation center for graphene growth. Since electropolishing is an electrochemical reaction where residual chemicals on the surface can be better removed, graphene films can be obtained with a better quality when an optimized process is used. GFETs fabricated with electropolished copper foils exhibit a shift in Dirac voltage in the negative direction, from 29.5 to 4 V toward 0 V and an increase in the resistance at Dirac point without any decrease in contact resistance. These results indicate that electropolishing improves the electron transport and increases the on-off current ratio. Chemical contamination and/or undesirable doping has been reported to result in a Dirac voltage shift, asymmetric electron and hole transport and increased carrier concentration through charge scattering.[59, 60] Hence, the restorative effect of electropolishing can be attributed to the suppression in the disturbance of the charge transport, which is affected by the chemical interaction with impurities induced by surface charge transfer and disordered morphology caused by microscopic peaks in the surface of the copper.

In order to extract the device key parameters of the GFETs, a diffusive transport model based on the total resistance from direct-current (DC) characteristics was applied by using the following expression[61]

$$R_{TOTAL} = R_{CONTACT} + \frac{L}{We\mu\sqrt{n_o^2 + n[V_G^*]^2}} \quad [3.1]$$

where μ is the field-effect mobility, n[V_G^*] is the density of the carrier concentration induced by the gate voltage away from the Dirac point, and n_o is the density of the carriers at the point of the minimum conductivity. Electropolishing on the copper foils increases the field-effect mobility from 1817 to 2868 cm^2/V-s, decreases the carrier density from 1.1×10^{12} to 6.0×10^{11} cm^{-2} and the width-normalized contact resistance is left almost unchanged, as shown in Figure 3.b. The electron and hole transport becomes significantly more balanced with a higher mobility of 2868 cm^2/V-s for the holes and 2628 cm^2/V-s for the electrons. Figure 3.c and d show statistical results of the field-effect mobility and the carrier density (n_o) in GFETs with and without electropolishing. 20 different GFETs fabricated in different batches at different times revealed that the field-effect mobilities had improved and the Dirac voltages had shifted towards 0 V. The device-to-device uniformity in the GFETs employing electropolishing significantly improved by a factor of two (the standard deviation decreased from 285 to 112 in the field-effect mobility and from 1.75 to 0.94 in the carrier density), which is critical for the practical use of GFETs in large-area nanoelectronics.

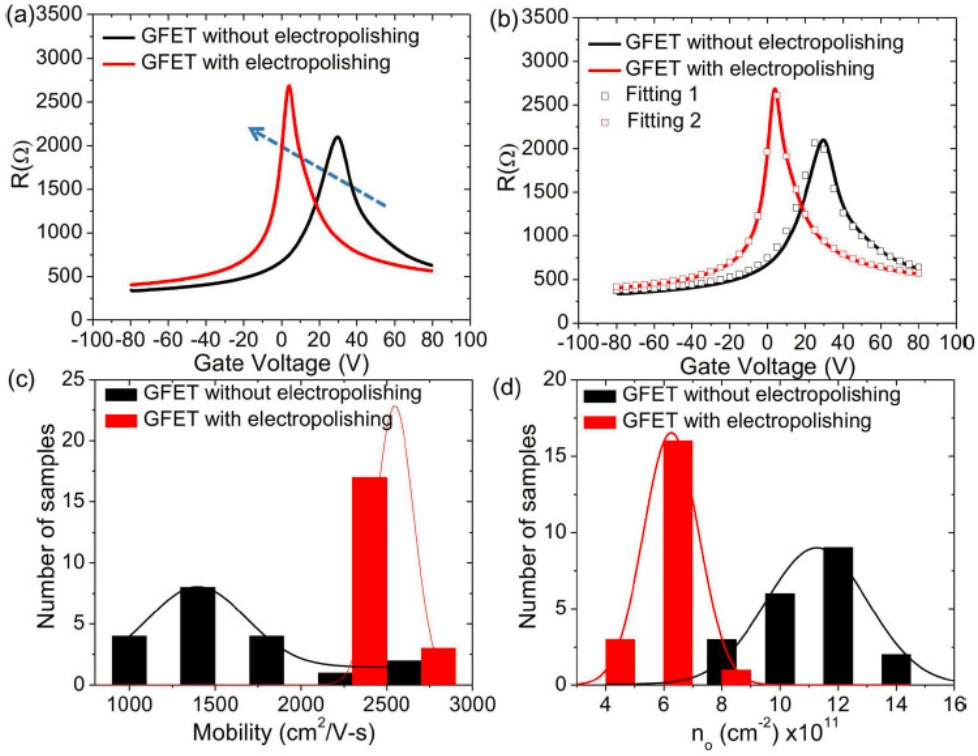

Figure 3.3 (a) Transfer characteristics of monolayer GFETs with and without electropolishing, (b) fitting using a diffusive transport model based on total resistance from DC characteristics and statistics results of (c) the field-effect mobility and (d) carrier density (n_o) in GFETs with and without electropoloishing.

Figure 3. shows the Raman spectra of GFETs fabricated with and without electropolishing. A decrease in the intensity of the D band at 1350 cm^{-1}, which is well-known as a disorder- or defect-induced peak, was observed in GFETs fabricated with electropolishing on the copper foils. As a result of the electropolishing pre-treatment, we see a direct response in the reduction in the D peak. The origin of some of the D peaks may be from nano-sized graphene domains or very small domains. We see these D peaks in other work where the size of each graphene domain is small and there is also morphological inhomogeneity.[59, 60, 62-64] By reducing the surface roughness, we have dramatically reduced the D peak found in the graphene, and a smoother surface allows us

to have a lower nucleation density. Therefore, we obtain larger domains and, subsequently, a lower D peak. This could be partially due to the reduction in the surface roughness but could also be a result of removing microscopic surface particles during electropolishing. We observed microscopic material embedded within the substrate, and after electropolishing, the material is removed from the same area.

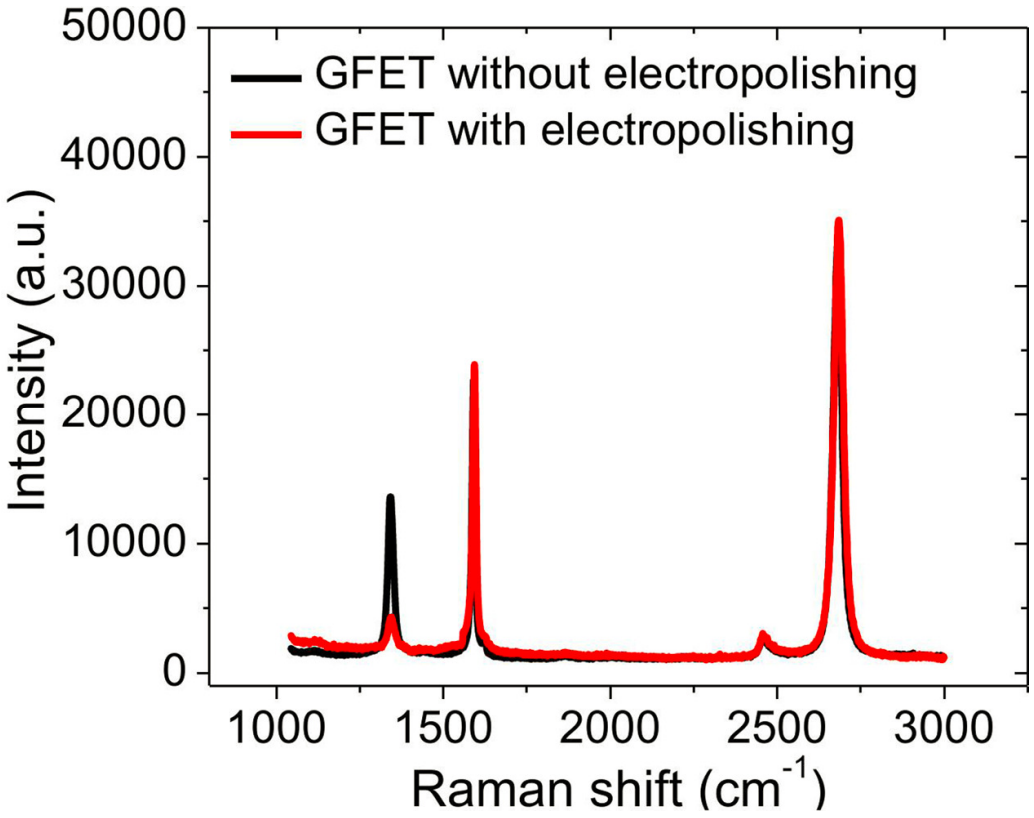

Figure 3.4 Raman spectra of GFETs fabricated with and without electropolishing, measured with a 442 nm blue laser.

Electropolishing is one of the easier methods of all methods known to reduce the nucleation density. By reducing the nucleation density, we are trying to gain larger graphene domains, which will ultimately result in a higher device performance since

there will be fewer defects in the many different graphene domains that are joined together, which is supported by the Raman spectra observations.

The charge transport properties of the GFETs can be strongly influenced by the interaction of functional molecules via dipole-dipole polarization, which can result in a modification of the electronic and material properties of GFETs.[65, 66] Figure 3.a shows the transfer characteristics of monolayer GFETs fabricated using a combination of electropolishing and fluoropolymer encapsulation in comparison to bare devices. Carbon-fluorine encapsulation improves the field-effect mobility from 2868 to 3918 cm^2/V-s, decreases the carrier density from 6.0×10^{11} to 2.1×10^{11} cm^{-2} and shifts the Dirac voltage from 4 V to 0 V. These results indicate that device performance of the GFETs can be restored through the dipole-dipole interactions of carbon-fluorine bonds in Teflon-AF to screen-out the effect of the interfacial interaction that determines the key device metrics. Graphene possesses a gapless electronic band structure and high residual impurities, and this can be an intrinsic challenge to achieve a logic circuit.[67-69] As shown in Figure 3.b, we have experimentally obtained an on-off current ratio with a substantial improvement up to 8 from 3 for the same density in the carrier concentration. We postulate that a smoother surface from electropolishing and a pool of strong carbon-fluorine dipole moments in the flouropolymer coating provide a charge buffer that relaxes the fluctuation in the electron-hole puddles.[62, 63, 70] The on-off current ratio can be further improved with further optimization in the deposition process to improve the charge transport and to reduce the effect of the impurities by inducing an oriented strong dipole-dipole interaction in the monolayer graphene.[71] Additional theoretical work includes a detailed analysis to demonstrate such a mechanism. Figure 3.c shows that GFETs encapsulated with fluoropolymer exhibit an excellent long-term stability in an ambient environment. A very small variation (<5%) was observed in the mobility of GFETs

employing carbon-fluorine encapsulation relative to the bare sample exhibiting a large drop in the mobility (up to 40%) after being kept in ambient air for 30 days. Such results were realized by reducing the chemical interaction between graphene and the -OH group from ambient air. Teflon-AF films possess highly hydrophobic surface characteristics with a water contact angle of 105° and a low permeability for the water molecules. The encapsulation in the GFETs with Teflon-AF can efficiently remove or repel water molecules from the grain boundary, which plays a role in inducing charge trapping/de-trapping. It must be noted that the improvement in mobility (that is, an increase up to 30%) was also observed after the GFET encapsulated with Teflon-AF films was kept in air for 30 days, and this result was not obtained via thermal annealing in a vacuum. Such results are supportive of our claim that the hydrophobic fluoropolymer is very effective in repelling water molecules that attach to the surface of graphene.

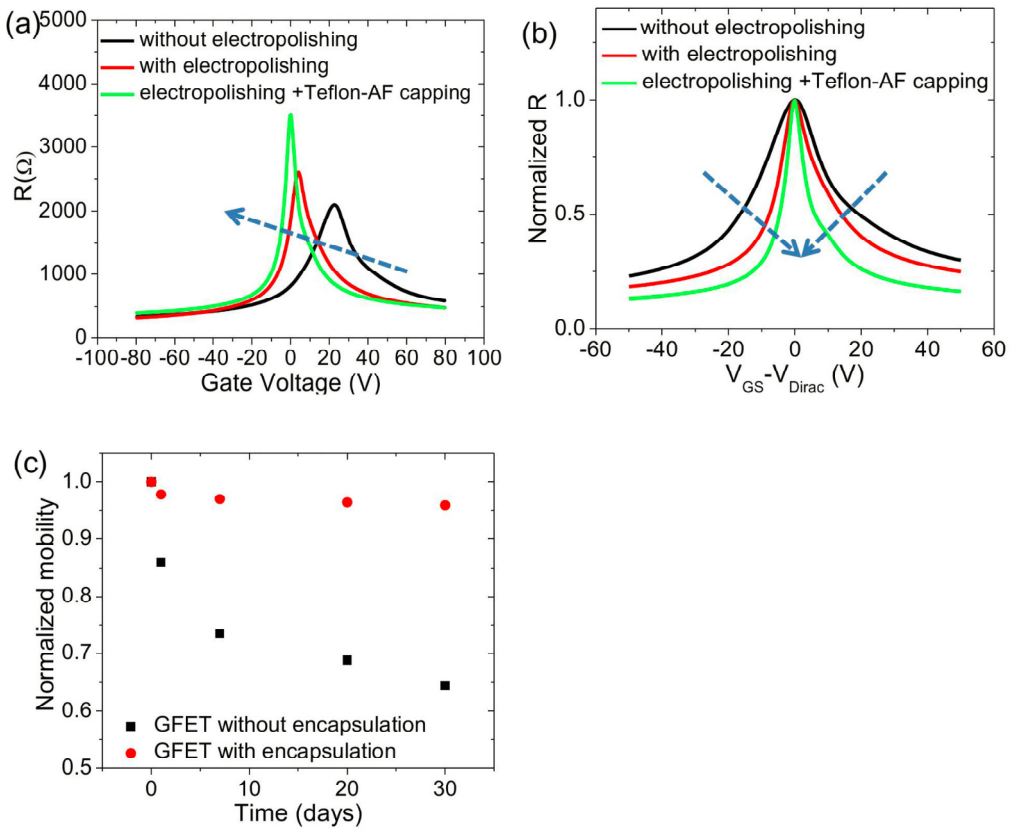

Figure 3.5 (a) Transfer characteristics and (b) normalized resistances as a function of V_{GS}-V_{Dirac} in monolayer GFET by using a combination of electropolishing and polymer encapsulation. (c) Variation in field-effect mobility as a function of exposure time in GFETs with and without Teflon-AF encapsulation after storage under ambient conditions for 30 days.

3.3 SUMMARY

Electropolishing can reduce surface roughness and remove most impurities from the surface of the copper prior to graphene growth. Particles that are embedded within the copper cannot be removed using this method. However, embedded particles may be

visible to the naked eye and thus those portions of the copper can be avoided when preparing the copper for growth.

The benefits of a smoother surface and less particulate manifest themselves in reduced graphene nucleation density and thus higher device performance. The impurities located within the copper bulk can still play a role by diffusing to the surface and interacting with the process gases. A smoother surface also allows for the impurities that do appear to have fewer impediments as they diffuse across the surface. This increases the size of large agglomerations of nanoparticles but reduces the overall number of particles on the surface during graphene growth. A simpler method to reduce the impurities would be to start with a much purer substrate.

Chapter 4. Copper film grain enlargement[2]

4.1 COPPER FILM

Copper film on a rigid substrate lends itself to be scaled up much easier, since the rigid substrate makes it simpler to handle the graphene on copper after growth. The copper film is also very pure copper since the impurities that may be present in the copper source are removed upon evaporation to deposit the copper onto the rigid substrate. However, once the copper film is annealed and copper grains start to grow the smoothness is reduced and the valleys formed between copper grains can cause reductions in electrical performance. To reduce the impact of the small copper grains, a method was developed to increase the copper grain size without evaporating the copper film during LPCVD conditions.

4.2 COPPER FILM GRAIN ENLARGEMENT

The conditions that are present during LPCVD are similar to that of physical vapor deposition (PVD) for evaporating metals; we have an evacuated chamber (furnace tube), an evaporation source (copper film), and an elevated temperature (annealing/growth temperature). The cover then acts as a "target" for the metal evaporating from our substrate, "source." Since the same conditions required for PVD

[2] This work is based on:

Lee, A. L.; Tao, L.; Akinwande, D. "Suppression of Copper Thin Film Loss during Graphene Synthesis." ACS Appl. Mater. Interfaces 2015, 7, 1527-1532.A.L. did the graphene growth and measurements. T.L. performed electrical characterization. D.A. supervised the work.

have been established, we used the equations that govern evaporation rates for a given pressure to arrive at Equation 4.1, which is derived from Langmuir-Knudsen theory

$$R_{evap} = 5.83 \times 10^{-2} A_s \left(\frac{m}{T}\right)^{1/2} P_e \qquad [4.1]$$

where 5.83×10^{-2} is an amalgam of all of the physical constants, A_s is the source area, m is the gram molecular mass, T is the temperature, and P_e is the vapor pressure.[72] Given our growth conditions, an evaporation rate of 8.0×10^{-7} g/s can be estimated from this equation. Since the films we used are 1.5μm thick, we had at most twenty-eight minutes before the entire film evaporated for uncovered growth. For capped growth, the cover piece is at the same temperature as the substrate. This would mean that any copper that evaporated from the substrate would most likely re-evaporate from the cover leading to a net zero transfer of copper atoms. As graphene grows and slowly covers the copper, a reduction in the evaporation of copper occurs. Copper that might be on the cover piece re-evaporating would end up on the surface of the graphene. This copper would then participate in the back and forth evaporation between the cover piece and graphene surface. The amount of copper that is trapped this way is less than our current detection capabilities. The mean free path for copper atoms during our annealing conditions is 9.6×10^{4} μm, which is much greater than the separation between the film and the cover as shown in Figure 4.1.

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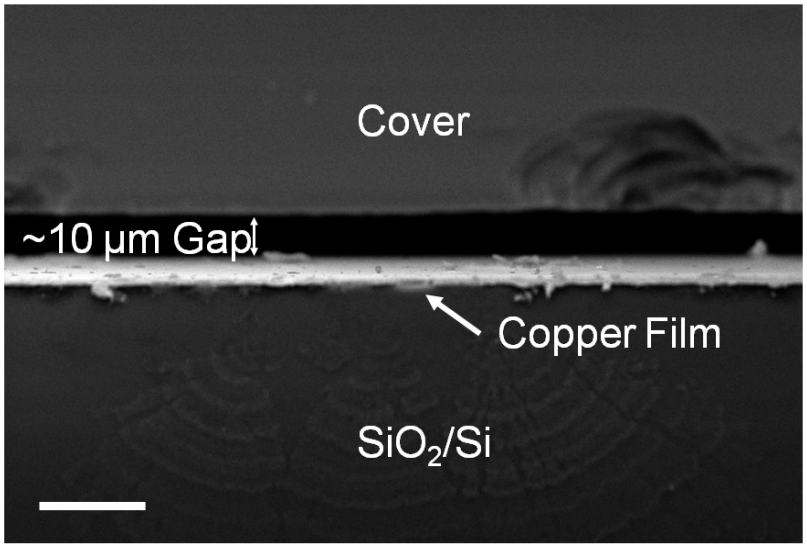

Figure 4.1 Separation distance between the cover and copper film. Scale bar is 20µm.

Near the edges of the cover, the copper has a path other than directly onto the cover. This results in copper loss near the edges due to diffusion of copper into the quartz tube. As copper is being lost from the edges, it becomes harder to lose more copper due to the increased distance of the exposed copper edges from the open space of the quartz tube. Figure 4.2 illustrates the minimization of mass loss due to evaporation by the use of a cover as compared with an uncovered sample. The mass loss percentage of the covered copper film approaches that of the uncovered copper film after nearly 120 minutes versus 5 minutes for the uncovered film. This indicates that the life-time of covered copper film is 16 times higher than the uncovered one, under the same process conditions. Leaving the uncovered copper film in the furnace for one hour would lead to complete loss of the copper film, whereas with the cover, the copper film has negligible loss. We can see the mass loss tracks with the estimated evaporation rate in Equation 4.1

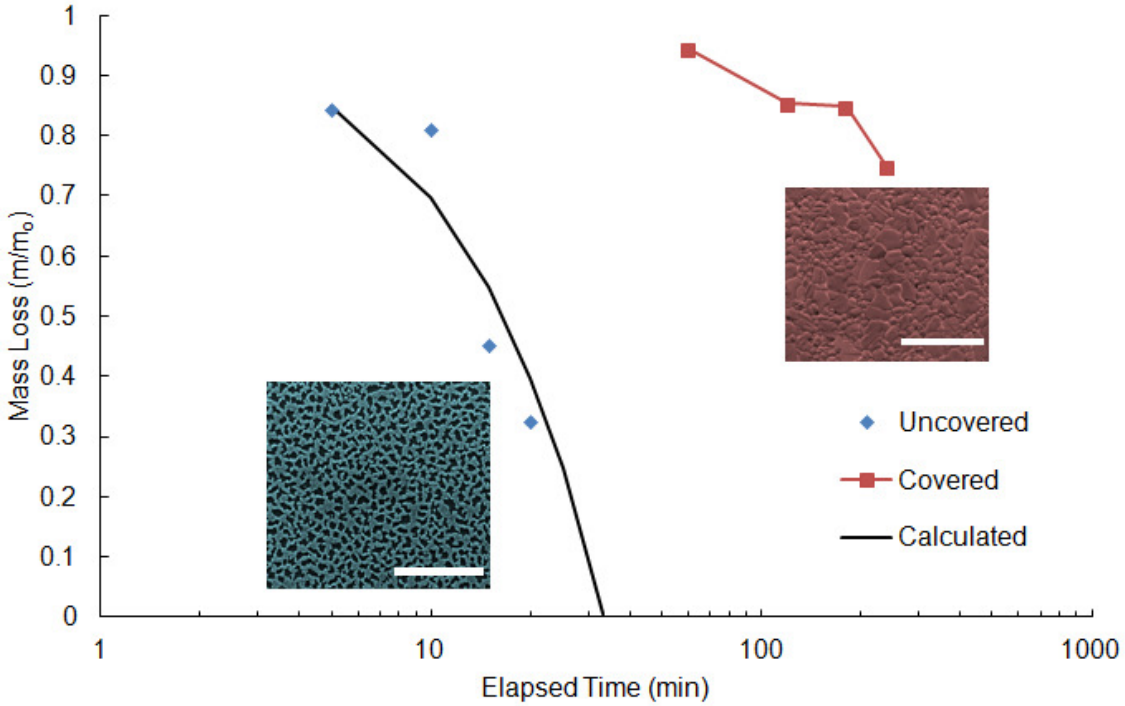

Figure 4.2 Copper mass loss comparison between uncovered and covered growth substrates. Calculated values based on sample dimensions of 7 mm x 8 mm. Copper mass lost in covered samples does not approach that of uncovered samples until approximately 120 minutes. At that point most of the grain growth has completed as seen in Figure 3. Inset images correspond to film coverage at maximum anneal times of 20 minutes and 240 minutes for uncovered and covered samples, respectively. Scale bars are 100 µm.

Once the annealing and growth have been completed, the cover itself comes off easily and there is no residual copper on the surface of the cover. Through the use of a cover our average copper grain size increases and pinholes are eliminated, as show in Figure 4.3.

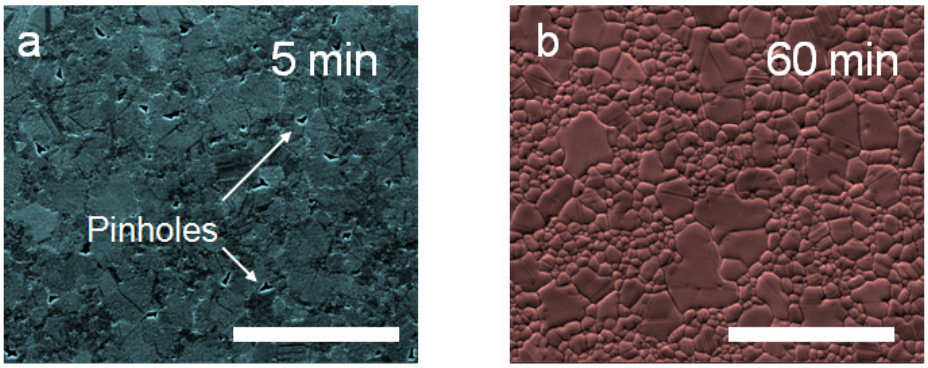

Figure 4.3 False color SEM images of both covered and uncovered growth. (a) Pinholes form from as little as 5 minutes of annealing. (b) With the use of a cover, even at 60 minutes there are no pinholes the appearance of larger copper grains is evident. Scale bar is 100µm.

The average size of the copper grains after a long annealing time remained fairly constant. On the uncovered sample we took the longest possible time while trying to maintain the least number of pinholes. In the covered samples, there were some extremely large copper grains, but after analysis of the size distribution we did not observe a shift to larger average copper grain size, Figure 4.4.

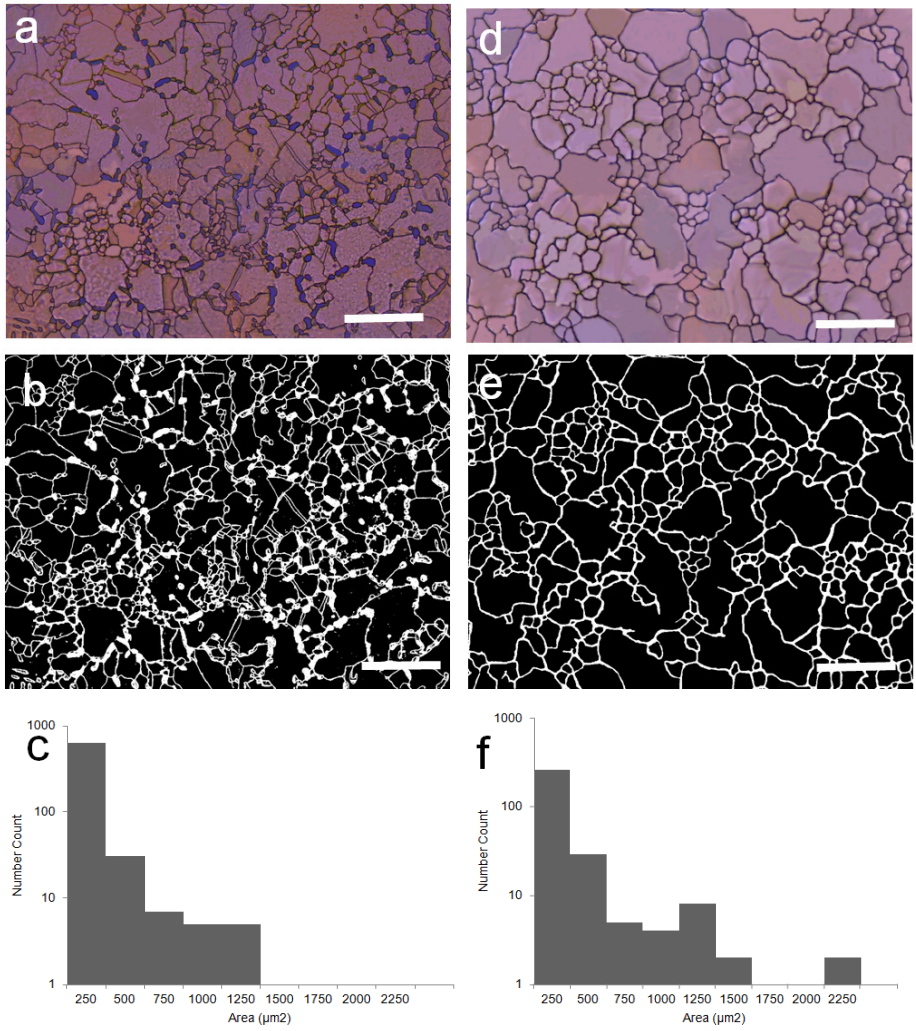

Figure 4.4 Dimensions of image are 280 µm x 211 µm. Taken with optical microscope. Area analyzed with ImageJ software. Copper grain interface enhanced for edge detection in ImageJ using Corel Photo-Paint X3. Area calculated with ImageJ is based on pixel count within each grain. (a-c) are from a five minute uncovered anneal. (d-f) are taken from a four hour covered anneal. (a) and (d) are the optical microscope images with their grain interfaces enhanced. (b) and (e) are the ImageJ image threshold adjusted images prior to are distribution count. (c) and (f) are histograms of the area distribution from different annealing conditions. The average grain areas are 206 μm^2 and 159 μm^2 for the uncovered and covered films, respectively. This corresponds to a diameter of ~16µm and ~14µm for the uncovered and covered films, respectively. All scale bars are 50 µm.

4.2 GRAPHENE GROWTH KINETICS

To determine how the cover affected the growth kinetics of graphene on a copper film, growth with isotopic precursors was used. The methane to hydrogen ratio was adjusted to determine the nucleation density as well as the growth rate of the individual graphene domains. With a cover there is a reduction of precursor flow onto the copper surface. This should lead to a reduced nucleation density and growth rate, which with further refinement; would lead to an increase in graphene domain size. As shown in Figure 4.5a and b, the statistical average of graphene domain size over numerous samples is approximately 5 μm for the uncovered copper film and 10μm for the covered copper film. We notice that the growth front shifts from a regular hexagon to an irregular polygon growth front. The growth does not seem to be dendritic because we have not observed the growth front to be anything other than straight. There is a reduction in the graphene nucleation density, but it does not approach the reduction found in other works, even when there is large hydrogen to methane ratio.[73, 74] There is also a corresponding reduction in the growth rate as there is a 12x increase in the cycle growth time for the covered copper film for the same apparent growth in the uncovered copper film. The quality of the graphene does not appear to change from the Raman spectroscopy. One metric of determining graphene quality is the presence or lack of a D peak located at ~1350 cm^{-1}. As shown in Figure 4.5c, there is no indication of a D peak. The FWHM of the uncovered sample may appear larger than the covered sample. The FWHM of the covered sample may be larger than the uncovered at a different point on the copper film.

Either way, the FWHM of the peaks is ~30 cm^{-1} which is indicative of monolayer graphene. By examining the I_{2D}/I_G ratio in Figure 4.5d, we can observe that the film is uniform and monolayer over the scan area.

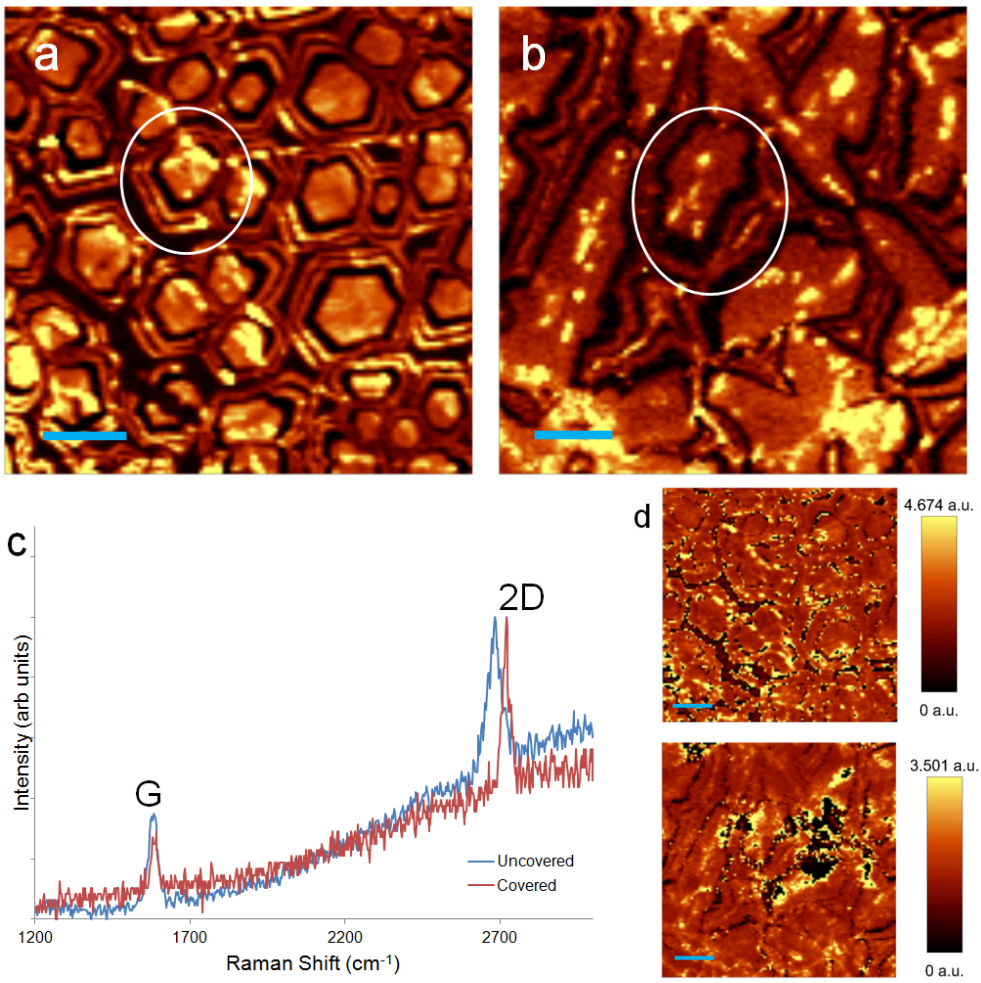

Figure 4.5 Raman map comparison of uncovered and covered graphene growth. (a) Raman mapping of the G peak of uncovered isotope labeled growth. Normal methane and ^{13}C enriched methane cycled in 1 minute increments, starting with normal methane. (b) Covered isotope labeled growth with the G peak mapped. Normal methane and ^{13}C enriched methane cycled in 12 minute increments, starting with normal methane. In (a) and (b) bright regions are normal methane and dark areas are ^{13}C enriched methane. Typical graphene domain has been circled (c) Comparison of typical Raman spectra from uncovered and covered copper films. The FWHM of the 2D peaks are 30 cm^{-1} and 32 cm^{-1} for the covered and uncovered films, respectively. (d) I_{2D}/I_G ratio for uncovered (five minute growth) and covered (60 minute growth) copper films, top and bottom, respectively. The dark regions are the copper grain boundaries. All scale bars are 5 µm.

4.3 ELECTRICAL PERFORMANCE

To verify the electrical performance, we fabricated field-effect transistors to determine its electrical characteristics. Electrical measurements were performed using typical setup with a widely used diffusive transport model for mobility extraction.[11, 23, 75] As shown in Figure 4.6a, a representative resistance versus back gate bias curve revealed ambipolar behavior with extracted field-effect mobility for hole and electron in a range of 2-3 k cm^2/V-s with carrier density around 3.3-3.8×10^{11} cm^{-2} on SiO_2/Si at ambient condition. The electrical property of covered synthesis is comparable to the same devices made from uncovered graphene (Figure 4.6b). This is most likely due to the grain size being comparable to the uncovered case.

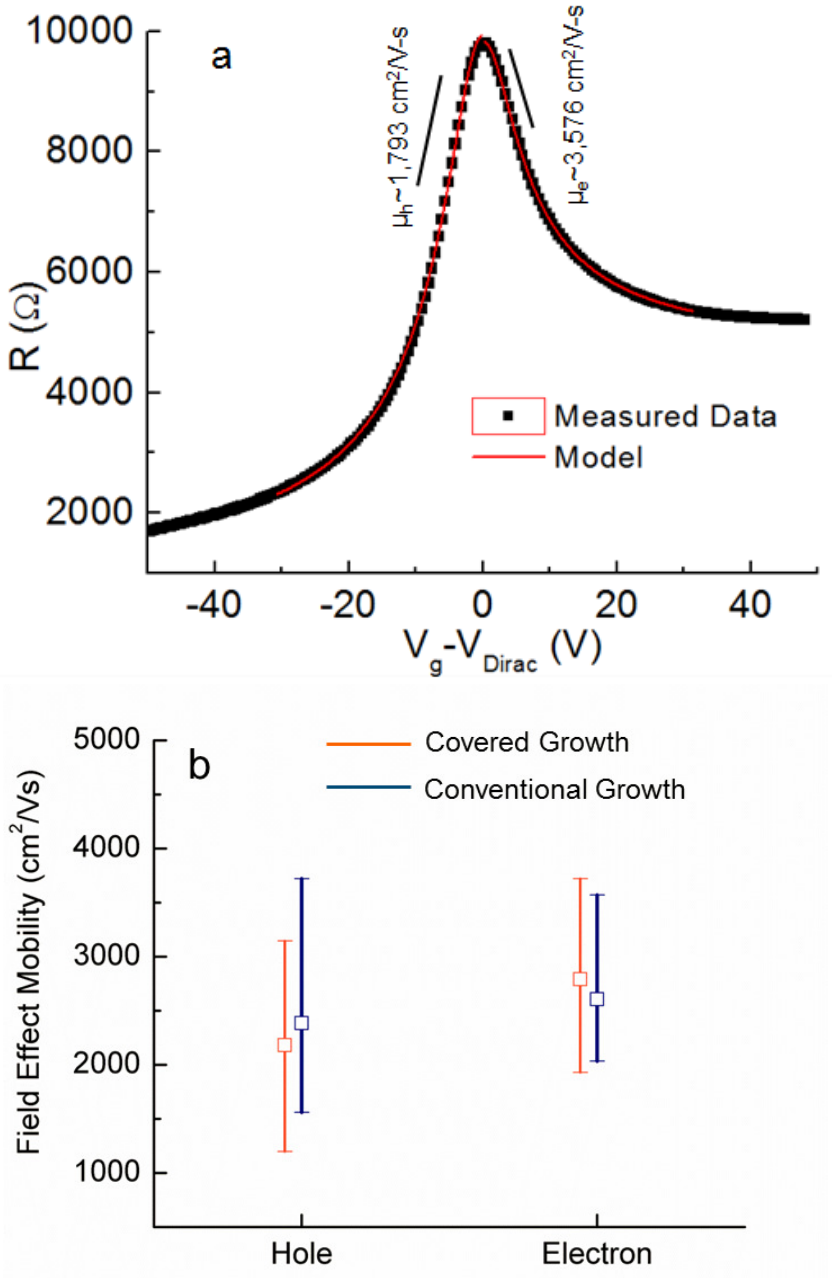

Figure 4.6 Electrical characterization of the graphene devices made from the two growth methods. (a) Resistance versus gate voltage characteristic with a model fit for a FET device, showing hole and electron mobility of 1,793 and 3,576 cm^2/V-s at ambient conditions. (b) Statistical values of field-effect mobility from several devices based on uncovered and covered growth of graphene.

4.4 SUMMARY

Copper thin film has no impurities that can interfere with graphene growth. The copper is very pure and the substrate is rigid, such that handling of the copper does not cause potential wrinkles in the copper possibly damaging the graphene. The copper thin film surface becomes much rougher after growth and this is due to the copper grains enlarging. We attempted to increase the copper grain size with additional annealing but this resulted in a few very large grains and the remainder of the grains remaining the same size.

Chapter 5: Conclusion

As various 2D materials are being discovered and characterized, we will always have the issue of the growth mechanism. The surface upon which the material grows is just as important as the material itself. Specific substrates are needed to grow different 2D materials, such as copper for graphene or silver for silicence. Particles can interfere with the growth fronts of the different materials. These particles can prevent the stitching together of the material to form a complete layer.

Just as the purity of silicon increased to match the required performance needs, so too must the purity of the growth substrates for 2D materials increase to the point where the purity of the growth substrates is at near the same level as silicon wafers. This purity will aid to achieve reliable growth of graphene and other 2D materials throughout the world regardless of local environmental conditions. The recipes will still need to be modified to match the conditions of the growth chambers i.e. to adjust for leaks but the factor of white dots and some adlayers can be removed from the equation as to why some people get 10x the performance of others.

Ideally, large area high purity single crystal copper foils should be developed to enable roll-to-roll production of reproducible high quality graphene. Graphene devices can reach the same reproducibility that silicon based devices currently enjoy. This idea can be further extended to other 2D materials that can benefit from large scale production.

Appendices

A: Low Pressure CVD (LPCVD) graphene growth

Step	Details
1. Copper foil preparation	Cut copper foil to desired size. Place foil in glacial acetic acid overnight.
2. Prepare system[1]	1. Fill vapor trap with liquid N2 (LN2), at least 10 minutes prior to growth. 2. Attach quartz tube to system. 3. Open the gas isolation valve. 4. Ensure mass flow controller isolation valves are open.
3. Load into quartz tube[2]	Insert the copper foil into the quartz tube using a push rod.
4. Annealing/ Graphene growth[3]	1. Open the vacuum isolation valve. 2. Pump down quartz tube until pressure <10mTorr ($0e^{-4}$ mBar). 3. Flow H_2 at 2 sccm. 4. Turn on furnace. Ensure T = 1030°C. 5. Anneal copper for desired time. 15 minutes (nominal). 6. Flow CH_4 at 5 sccm. 7. Grow graphene for 10 minutes. 8. Turn off furnace.

	9. Maintain gas flow during cooldown. 10. Wait for T <60°C. 11. Turn off gas flow. 12. Close vacuum isolation valve. 13. Break vacuum. 14. Remove copper
5. Restore system	1. Remove quartz tube. 2. Close gas isolation valve.
Notes: 1. Maintain the same materials usage for each tube to prevent possible cross contamination, i.e. copper quartz tube for copper and nickel quartz tube for nickel. 2. A smaller carrier tube can be used for easier insertion and removal of copper. Copper foil with the inside circumference of the carrier tube can be loaded. This allows large pieces of copper foil to be used without possible damage to the foil upon removal. 3. Accelerated cooldown can be used. To speed up cooldown at T <= 600C, crack open the furnace lid and use small metal piece to maintain crack. At T <=400C, furnace lid can be fully opened.	

Table A.1 Details for low pressure CVD growth of graphene

B: ATMOSPHERIC PRESSURE CVD (APCVD) GRAPHENE GROWTH

Step	Details
1. Copper foil preparation	Cut copper foil to desired size. Place foil in glacial acetic acid overnight.
2. Prepare system[1]	1. Attach quartz tube to system. 2. Open the gas isolation valve. 3. Open appropriate mass flow controller isolation valves are open. 4. Ensure atmosphere isolation and vacuum isolation valves are closed.
3. Load into quartz tube[2]	Insert the copper foil into the quartz tube using a push rod.
4. Annealing/ Graphene growth[3]	1. Open the vacuum isolation valve. 2. Pump down quartz tube until pressure $< 9e^{-3}$Torr. 3. Flow Ar at 500 sccm and H_2 at 10 sccm. 4. Close vacuum isolation valve. 5. Monitor analog pressure gauge near atmosphere isolation valve. 6. When pressure is slightly above atmospheric, open atmosphere isolation valve. 7. Turn on furnace. Ensure T = 1030°C. 8. Anneal copper for desired time. 15 minutes nominal.

	9. Flow H_2 at 75 sccm and CH_4 at 5 sccm. 10. Grow graphene for 10 minutes. 11. Turn off furnace. 12. Maintain gas flow during cooldown. 13. Wait for T <60°C. 14. Turn off gas flow. 15. Remove copper
5. Restore system	1. Remove quartz tube. 2. Close gas isolation valve. 3. Close flow controller isolation valves. 4. Close atmosphere isolation valve.
Notes: 1. Maintain the same materials usage for each tube to prevent possible cross contamination, i.e. copper quartz tube for copper and nickel quartz tube for nickel. 2. A smaller carrier tube can be used for easier insertion and removal of copper. Copper foil with the inside circumference of the carrier tube can be loaded. This allows large pieces of copper foil to be used without possible damage to the foil upon removal. 3. - Vacuum is not required. If vacuum is inoperable, APCVD operations can still continue. Set the same flow rates and allow gas flow for minimum of 10 minutes to purge/displace the quartz tube of atmospheric gases. - Accelerated cooldown can be used. To speed up cooldown at T <= 600C, crack open the furnace lid and use small metal piece to maintain crack. At T <=400C, furnace lid can be fully opened.	

Table B.1 Details for atmospheric pressure CVD (APCVD) growth of graphene

C: RADIO FREQUENCY CVD (RFCVD) GRAPHENE GROWTH

Step	Details
1. Copper foil preparation	Cut copper foil to desired size. Place foil in glacial acetic acid overnight.
2. Prepare system	1. Turn on RF chill water. 2. Turn on RF power supply. 3. Start InfraWin software. 4. Ensure emissivity E-Ratio is set for the metal to be used. 5. Close turbo pump isolation valve. 6. Ensure roughing pump isolation valve is closed. 7. Ensure the gas isolation valve is closed. 8. Ensure individual gas isolation valves are closed.
3. Load into quartz tube	1. Insert the copper foil into the quartz carrier tube. 2. Insert carrier tube using a push rod. 3. Align the copper foil with the RF copper coils.
4. Annealing/ Graphene growth	5. Open the roughing pump isolation valve. 6. Pump down quartz tube until pressure < 0.030 Torr. 7. Close the roughing pump isolation valve. 8. Open turbo vacuum isolation valve. 9. Monitor ion gauge pressure gauge. 10. Pump down quartz tube until pressure $<9e^{-6}$ Torr. 11. Shut turbo pump isolation valve. 12. Open gas isolation valve.

	13. Open 95/5 Ar/H_2 isolation valve to 350 Torr. 14. Close 95/5 Ar/H_2 isolation valve. 15. Close gas isolation valve. 16. Press “Start” button on RF power supply. Observe white light on RF controller turns on. 17. Using arrow keys on RF controller increase power. 18. Monitor temperature using InfraWin software. Set power so T ~ 1030°C. 19. Anneal copper for desired time. 15 minutes nominal. 20. Set power to 0%. 21. Allow copper to cool for 15 minutes. 22. Repeat steps 5 – 12. 23. Open Ar isolation valve to 700 Torr. 24. Close Ar isolation valve. 25. Close gas isolation valve. 26. Repeat steps 17-21. 27. Repeat steps 5-12. 28. Open Ar isolation valve to 100 Torr. 29. Repeat steps 17 and 18. 30. Open 95/5 Ar/CH_4 isolation valve closer to gas cylinder. 31. Use needle valve to slowly allow 50 Torr 95/5 Ar/CH_4 32. Close 95/5 Ar/CH_4 needle valve to slowly allow 50 Torr

	33. Close 95/5 Ar/CH_4 isolation valve closer to gas cylinder. 34. Grow graphene for 15 minutes. 35. Set power to 0%. 36. Cooldown for 15 minutes. 37. Remove carrier tube.
5. Restore system	1. Open the roughing pump isolation valve. 2. Pump down quartz tube until pressure < 0.030 Torr. 3. Close the roughing pump isolation valve. 4. Open turbo vacuum isolation valve.

Notes:

1. Maintain the same materials usage for each tube to prevent possible cross contamination, i.e. copper quartz tube for copper and nickel quartz tube for nickel.
2. A smaller carrier tube can be used for easier insertion and removal of copper. Copper foil with the inside circumference of the carrier tube can be loaded. This allows large pieces of copper foil to be used without possible damage to the foil upon removal.
3. - Vacuum is not required. If vacuum is inoperable, APCVD operations can still continue. Set the same flow rates and allow gas flow for minimum of 10 minutes to purge/displace the quartz tube of atmospheric gases.
   - Accelerated cooldown can be used. To speed up cooldown at T <= 600C, crack open the furnace lid and use small metal piece to maintain crack. At T <=400C, furnace lid can be fully opened.

Table C.1 Details for radio frequency CVD (RFCVD) growth of graphene

D: ELECTROCHEMICAL DELAMINATION (BUBBLE) TRANSFER OF GRAPHENE

Step	Details
1. Copper foil preparation	Spin coat support polymer
2. Prepare system	1. Pour 0.5M sodium sulfate (Na_2SO_4) in appropriate sized container. 2. Pour DI water into reception container. 3. Set DC power supply to 5 V and 1.5A. 4. Attach platinum mesh to anode (+) and insert into electrolyte.
3. Connecting work piece	Attach work piece to cathode (-)
4. Delamination[1,2]	1. Turn output of power supply on. 2. Slowly insert end of work piece into electrolyte. 3. Leave work piece end in electrolyte until PMMA/graphene begin to peel away from copper. 4. Continue to slowly insert work piece into electrolyte, allowing time for PMMA/graphene to lift off. 5. Turn output of power supply off when PMMA/graphene has completely lifted off copper. 6. Scoop PMMA/graphene from electrolyte and place in DI water.

	7. Detach the copper from the cathode (-) 8. Repeat step 4 if there are more work pieces.
5. Clean up	1. Detach the platinum mesh from the anode (+) 2. Rinse thoroughly with DI to prevent buildup of sodium on mesh. 3. Store platinum mesh in ethanol.
Notes: 1. Tweezers can be used to help move PMMA/graphene if it becomes stuck in one region during bubbling. Exercise care as the PMMA is fragile. 2. The PMMA/graphene may not completely float away from the copper, so if lifting the PMMA adheres to the copper when removing the copper then you can use the copper to transfer the PMMA/graphene to the DI.	

Table D.1 Details for bubble transfer of graphene

E: ELECTROPOLISHING COPPER

Step	Details
1. Copper foil preparation	Cut copper to size appropriate for container and DC power supply
2. Prepare system[1]	1. Pour pre-mixed electropolishing solution into appropriate sized container. (see recipe in notes) 2. Pour DI water into reception container. 3. Set DC power supply to 5 V and 3A. 4. Attach large copper foil piece to cathode (-).
3. Connecting work piece	Attach work piece to anode (+)
4. Electropolishing[2]	1. Insert entire work piece into solution 2. Turn output of power supply on. 3. Observe bubble formation on work piece 4. Maintain power until bubbles reach the top of the work piece. 5. Turn output of power supply off when bubbles have reached the top of the work piece. 6. Rinse work piece with DI water. 7. Place work piece in ethanol. 8. Repeat if there are more work pieces.
5. Clean up	1. Detach the large copper foil from the cathode (-)

	2. Rinse thoroughly with DI, if future use is desired.

Notes:

Electropolishing solution (can be scaled)

- 100 mL DI water
- 50 mL Phosphoric acid (Ortho-phosphoric is another name)
- 50 mL Ethanol
- 10 mL Iso-propyl alcohol
- 1 g Urea

The phosphoric acid is doing the main work. The other ingredients are there to improve viscosity and appearance of the copper when done.

The larger the current of the DC power supply the larger the work piece that can be polished. Electropolishing size is current limited.

1. Copper foil cathode should be at least twice the surface area of the work piece.
2. The work piece can be left in longer if desired. Longer times can further reduce surface roughness. However, pitting can start to occur for longer times as the copper is etched. This is due to increased current through the work piece, eventually pushing the work piece into the oxygen generation regime.

Table E.1 Details electropolishing copper

F: ELECTROPLATING COPPER

Step	Details
1. Substrate preparation	Size substrate appropriate for electroplating
2. Prepare system[1]	1. Pour pre-mixed electroplating solution into appropriate sized container. 2. Pour DI water into reception container. 3. Set DC power supply to 5 V and appropriate current. 4. Attach large copper foil piece to anode (+).
3. Connecting work piece	Attach work piece to cathode (-)
4. Electropolishing[2]	1. Insert entire work piece into solution 2. Turn output of power supply on. 3. Observe current on DC power supply. 4. Maintain power until desired thickness (~12.5 μm/hr) 5. Turn output of power supply off when desired thickness reached. 6. Rinse work piece with DI water. 7. Repeat if there are more work pieces.
5. Clean up	1. Detach the large copper foil from the anode (+) 2. Rinse thoroughly with DI, if future use is desired.

Notes:

Electroplating solution is commercially bought from Transene.

1. Per Transene, the current should be set 20 – 50 A/ft^2 -> ~0.022 – 0.054 A/cm^2. Higher current results in faster plating, but it becomes less even.
2. The thicker the plating the rougher the surface becomes. This is caused by uneven plating.

Table F.1 Details for electroplating copper

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