Fault inductance based protection for DC distribution systems

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Keywords: DC distribution system, DC protection, fault location, inductance, hardware-in-the-loop.

Abstract

The fault protection is a critical element to ensure the reliable and secure operation of DC distribution systems. Most DC distribution systems are tightly coupled systems with low line impedances which may result in fast current increase during a fault. Thus, it is challenging to develop a fast and reliable DC fault protection method. This paper proposes and develops a novel fault inductance based DC protection method without communication between protection units at different locations. The performance of the developed protection algorithm was validated in a Real-Time Hardware-In-the-Loop (RTHIL) test platform. The testing results indicate that the developed inductance based fault location algorithm detects and locates faults with fast speed and high accuracy. Preliminary sensitivity analysis on measurement errors are also conducted to study impacts on accuracy of estimated fault inductance.

1 Introduction

Recent improvements of power electronic technology facilitate developments of DC power systems. Low voltage DC (LVDC) has been applied to commercial buildings [1], marine vessels [2] and datacenters [3]. Protection is one important aspect of the system design and should be considered from the beginning of system design in order for high system reliability and cost effective operation. In certain DC distribution systems, fault currents develop promptly due to small system inductance and fast protection is required to improve DC system reliability [4,5]. Due to the fast rising speed of fault currents, it is a challenge to develop a fast fault detection, location, and coordination method.

In DC systems with large line inductances, such as HVDC systems and DC traction systems, overcurrent and rate of rise of current (*di/dt*) protections are applicable. Protection selectivity is achieved by differentiating different fault current signatures at different locations [6]. However, in a tightly coupled DC distribution system, the overcurrent and *di/dt* protections are difficult to implement due to the low line impedance. Distance protection has been used in AC power systems for many years. This method locates faults using the equivalent impedance estimated by the steady-state fault voltage and current [7]. If the estimated impedance is less than the total impedance of the protection zone, the fault is identified as an internal fault. However, in a DC distribution system, fast fault detection, location, and isolation is required before reaching steady-state because of fast increasing DC fault currents.

An online inductance based fault location method for DC distribution system protection was proposed in [8]. The line inductance from a large capacitor to a fault is estimated by the capacitor voltage and the line current at the initial stage of the capacitor discharging. In this paper, a DC distribution protection based on a novel fault location method is proposed. The proposed fault location method utilizes local voltage, current, and *di*/*dt* measurements to estimate the equivalent fault inductance on the fault path. The proposed DC protection method does not require communication between protection units at different locations, so the DC protection can be fast and reliable.

The outline of this paper is given as follows. In section 2, DC protection using a novel inductance based DC fault location algorithm is discussed. Numerical simulations verify the performance of the DC fault location algorithm. Section 3 presents the Real –Time Hardware-In-the-Loop (RTHIL) test results of the DC protection using the proposed inductance based fault location algorithm. A sensitivity analysis for measurement errors is conducted in section 4. At last, some conclusions are given in section 5.

2 DC protection based on fault inductance

In this section, the proposed DC protection is described. Theoretical deduction is given to derive the estimated fault inductance using local measurements. Simulations verify the effectiveness of the inductance based fault location algorithm and thus the DC protection method.

2.1 An example DC distribution system

The single-line-diagram of an example Low Voltage DC (LVDC) distribution system is shown in Figure 1. The system includes an AC/DC UPS with 100 kW power rating, multiple feeders, and various DC loads. The voltage rating is 380 V DC. The total capacity of the system is 96 kW. The DC/DC converter in the UPS includes a fault current limiter. Once a fault happens, the averaged current flow through the converter would be limited to 150% of the nominal current. Due to the communication delay and the control time constants, fault currents normally are uncontrolled for a few milliseconds before limited to a fixed value. DC fault currents

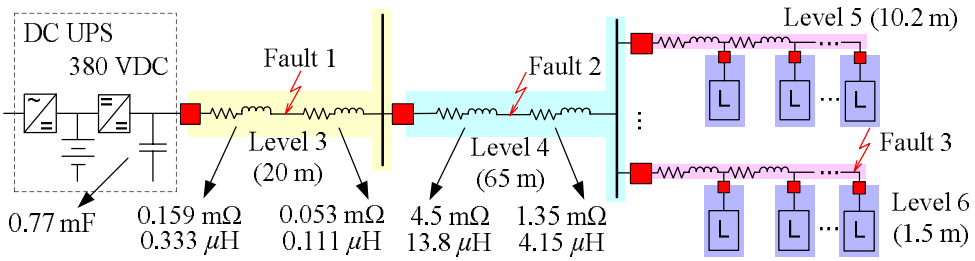


Figure 1: Single-line-diagram of a low voltage DC distribution system.

are mainly contributed by the uncontrollable capacitor discharge at the converter output filter. The converter capacitor discharge can be large enough to damage downstream equipment and devices.

The system includes one level 3 feeder, one level 4 feeder and four level 5 feeders. Protective devices, such as DCCBs (DC Circuit Breakers) are installed at each feeder. Level 4 feeder supplies power to four level 5 feeders and each level 5 feeder supplies power to eight constant loads. The loads are modeled as constant resistive loads and each load has 3 kW power rating. The line is modeled with a resistor and an inductor. The impedances of different feeders are shown in Figure 1. The total line inductance of level 5 feeder is 4.8 μH. The line inductance from level 6 breaker to load is 0.432 μH. Various faults can be placed in the system to test the performance of the developed DC protection method.

2.2 Fault inductance estimation

In this section, a novel based fault detection and location method for DC distribution systems is developed. The discharge of the capacitor in the UPS output filter through system inductance causes significant oscillations right after a fault. The fault can be detected by either under voltage or over current or both. The voltage, current, and *di/dt* are measured at each protective device. These signals are used by a microprocessor to estimate the equivalent fault inductance between the local protective device and the fault.

Since the fault resistance is varied for different faults, it is hard to use the estimated equivalent fault resistance to locate a fault. This work proposes to use the equivalent fault inductance to locate fault. The inductance in levels 3-5 of the system is illustrated in Figure 2. L_3, L_4, and L_5 represent the equivalent inductances of levels 3-5. These values are determined by the actual line inductances. If the estimated inductance at a certain local protective device is less than the predefined line inductance, the fault is considered as an internal fault. The device will isolate faulted segments and the healthy part will go back to normal operation.

Accurate inductance estimation becomes a key factor for this DC protection method. To accurately estimate the equivalent inductance between a protective device and a fault, an equivalent electric circuit is used as Figure 3. Circuit parameters L and R represent the equivalent inductance and resistance between the measuring point and the fault. R_F is the fault resistance. The state space equation of the circuit is expressed in Equation (1).

$$v = L\frac{di}{dt} + (R + R_F)\cdot i \qquad (1)$$

The voltage, current and d*i*/d*t* are sampled at each time step. (R+R_F) and L then are estimated from data sampled at multiple time steps using the least square method. The relationship of the multiple sampled data is shown in Equation (2).

$$B = A\cdot\begin{bmatrix} L \\ R+R_F \end{bmatrix},\ A = \begin{bmatrix} \frac{di}{dt}(0) & i(0) \\ \frac{di}{dt}(1) & i(1) \\ \vdots & \vdots \\ \frac{di}{dt}(N) & i(N) \end{bmatrix},\ B = \begin{bmatrix} v(0) \\ v(1) \\ \vdots \\ v(N) \end{bmatrix} \qquad (2)$$

The sampling rate can be chosen as 20-100 μs depending on the time constant of the DC distribution system. The unknown parameters in Equation (2) are estimated by Equation (3).

$$\begin{bmatrix} L \\ R+R_F \end{bmatrix} = (A^T A)^{-1} A^T B \qquad (3)$$

An online moving-window least square method [9] is used to identify the fault inductance L. The fault resistance R is unobservable since R_F is normally unknown. The inductance estimation flowchart is shown in Figure 4. Once a fault is detected, the fault location routine is activated. If the number of data samples is less than M (M is the size of the moving window in the least square method), all the data are used in the inductance estimation. Otherwise, only the most recent M samples are used. If T_{max} is reached, the fault location routine is exited.

2.3 Simulation verification

In this section, numerical simulations are used to validate the proposed DC protection method. The LVDC system as shown in Figure 1 is simulated in MATLAB/SimPowerSystem with a step size of 5 μs. Once a fault happens, the converter limits the fault current to 1.5 times of the nominal current in 600 μs. The inductance based fault location algorithm described in section 2.2 is implemented associated with each protective device using the basic MATLAB/SIMULINK building blocks. The sampling rate is chosen as 20 kHz. The most recent 10 data samples are used to locate a DC fault. Three

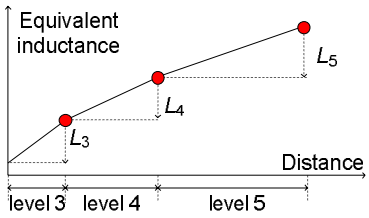


Figure 2: Equivalent inductances in levels 3-5.

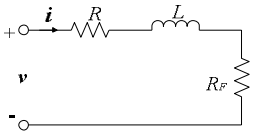


Figure 3: Equivalent circuit used in inductance estimation.

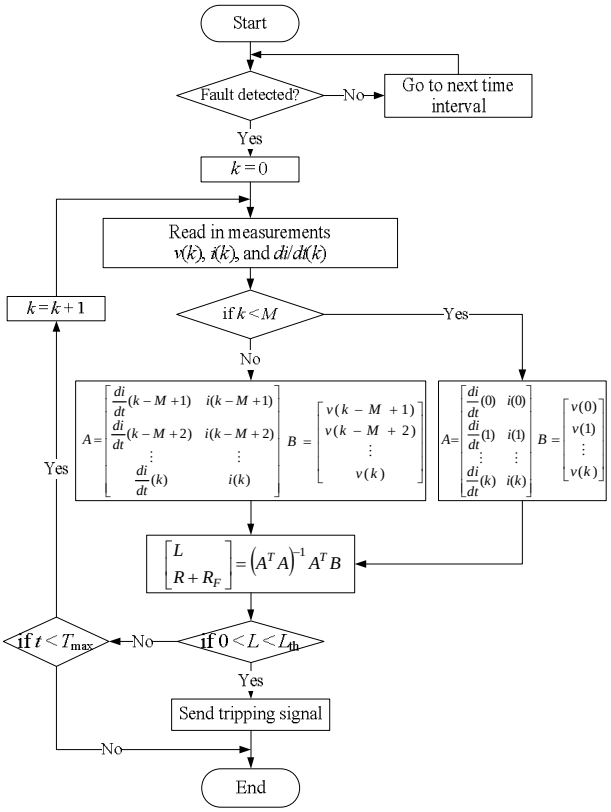
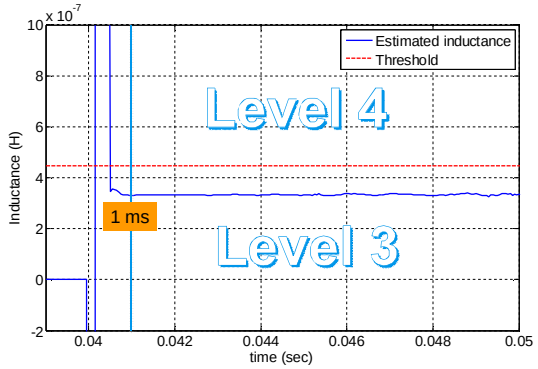


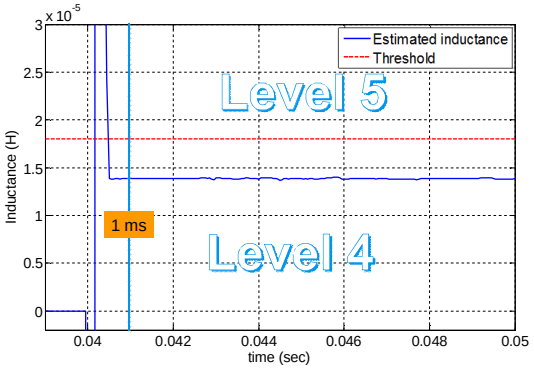
Figure 4: Flowchart of the proposed fault location algorithm.

different faults are studied and the fault resistance R_F is assumed to be 2 mΩ.

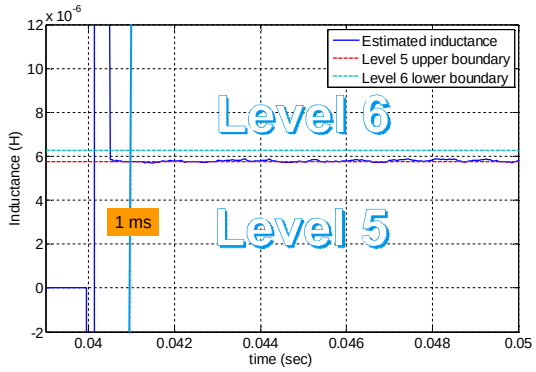
Fault 1 is at 15 m from the level 3 breaker. The estimated inductance of the level 3 breaker from the proposed fault location algorithm is shown in Figure 5(a). The estimated inductance is below the line inductance of level 3, so the level 3 breaker trips and isolates the fault. Fault 2 is at 50 m from the level 4 breaker. The estimated inductance of the level 4 breaker from the proposed fault location algorithm is shown in Figure 5(b). The estimated inductance is below the line



(a) Estimated inductance at level 3 breaker for fault 1



(b) Estimated inductance at level 4 breaker for fault 2



(c) Estimated inductance at level 5 breaker for fault 3

Figure 5: Estimated inductances for various faults.

inductance of level 4, so the level 4 breaker trips and isolates the fault. The fault is also observed at the level 3 breaker, but the estimated inductance at the level 3 breaker is higher than the level 3 threshold. Thus, the level 3 breaker keeps closed. Fault 3 is at the end of the level 5 feeder. The estimated inductance at the level 5 breaker is shown in Figure 5(c). The estimated inductance is below the line inductance of level 5, so the level 5 breaker is selected to isolate the fault. The fault is also observed at level 3 and level 4 breakers, but the estimated inductances are higher than their line inductances. Thus, level 3 and level 4 breakers keep closed. The impact of the fault is

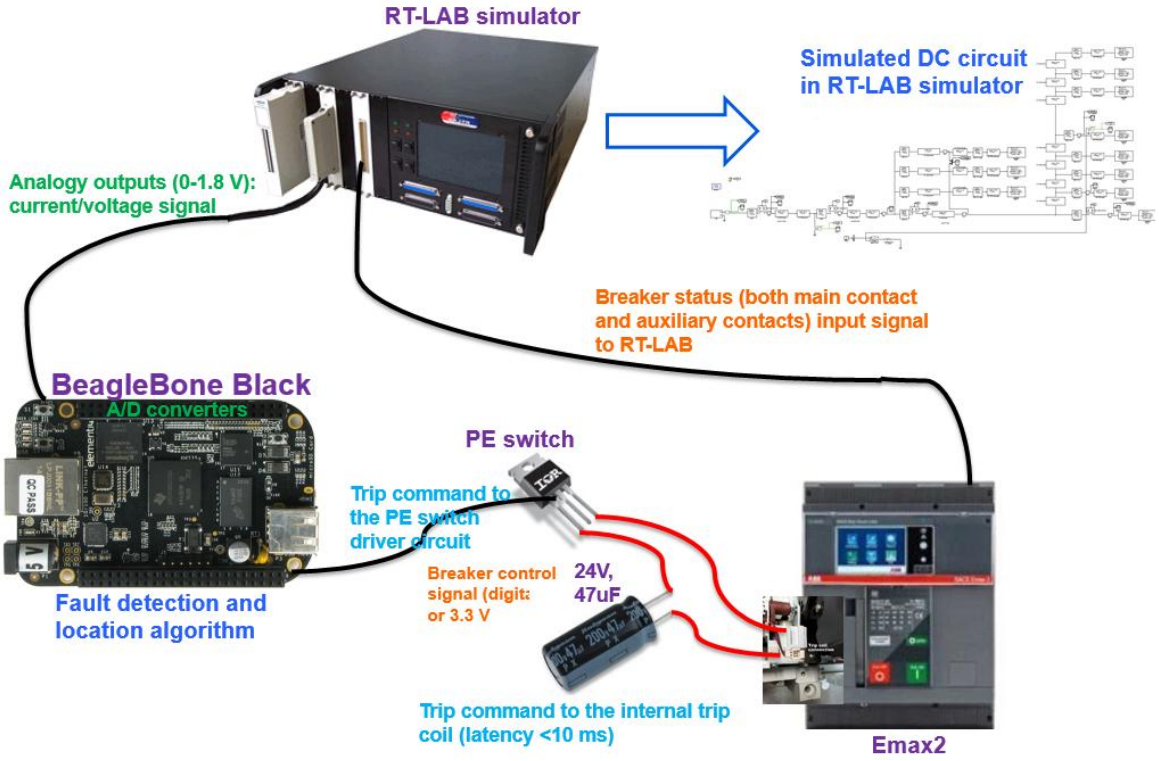


Figure 6: Diagram of the real-time hardware-in-loop simulation test system.

minimized by only opening the circuit breakers closest to the fault locations.

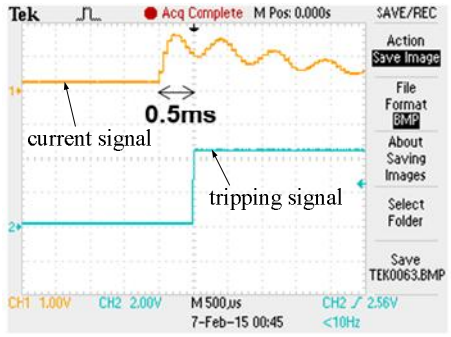
The numerical simulation verifies that the fault location algorithm accurately estimates the fault inductance from a protective device to a DC fault. The fault can be detected and located in one millisecond.

3 Hardware-in-the-loop test results

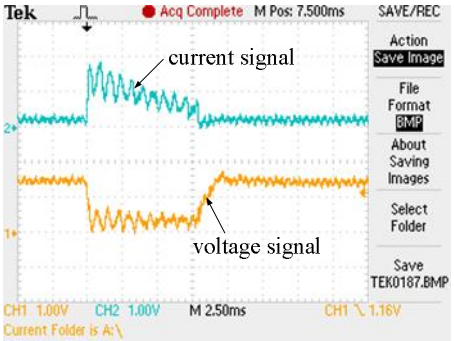
This section discusses the implementation and test results of the proposed protection method in a RTHIL simulation platform. The 380 V DC distribution system in Figure 1 is simulated in the Opal-RT simulator. The inductance based fault location scheme is deployed in a Texas Instrument (TI) BeagleBone board. ABB Emax 2 DC breaker [10] is used to emulate the protective device. Figure 6 shows the diagram of the RTHIL platform.

The TI Beaglebone board is a microcontroller and has an AM3358 1GHz ARM® Cortex-A8 and 512MB DDR3 RAM. Two built-in 32-bit 200-MHz programmable real-time units (PRUs) on the board read in data from onboard A/D converters. The board includes seven analog I/Os and 65 digital I/Os. To implement the proposed protection scheme, three analog input channels are used to input the measured voltage, current and *di*/*dt* signals; one digital output channel is used to send open/close command to the Emax breaker.

Current, voltage, and *di*/*dt* signals at a local protective device



(a) current and tripping signals



(b) current and voltage signals

Figure 7: Representative waveforms of a RTHIL test case.

are measured from the Opal-RT model and converted to analog signals in the range of 0-1.8 V through the I/O module on the Opal-RT simulator. The analog output channels are wired to input channels of the BeagleBone board. The protection scheme on the BeagleBone board is periodically executed to detect a fault (cycle: ~25 μs). Once the fault is detected, the fault location routine is activated to estimate the location of the fault. If the estimated inductance between the protective device and the fault is less than a predefined threshold, a tripping signal (binary) is generated. The tripping signal is wired to a power electronic switch, which controls the discharge of a pre-charged capacitor (24V, 47μF). When the tripping signal is arrived, the switch is closed and the discharging current of the capacitor trips the Emax breaker. The higher the discharging current, the faster it trips. The actual status of the Emax breaker is wired back to the Opal-RT simulator to close the simulation loop. The transients after the Emax breaker open then can be observed.

A fault is placed at the downstream of the level 4 breaker. The voltage, current, and *di*/*dt* at the level 4 breaker (Emax) are measured and sent out through the analog output channels of the Opal-RT simulator to the BeagleBone board. The simulation solver is ode3 (Bogacki-Shampine). The sampling rate of the BeagleBone board is chosen as 7 μs. Each data point including voltage, current, and *di*/*dt* is obtained by the BeagleBone board. The voltage, current, and *di/dt* are read in sequentially.

Figure 7 shows representative current, voltage and tripping signals captured by an oscilloscope. When a fault happens, the fault current increases fast and the DC protection based on the fault inductance detects and locates the fault and then sends out a tripping signal to the Emax breaker in ~0.5 ms. The Emax breaker takes ~7 ms to isolate the fault. The voltage returns to the nominal value after the fault is cleared as shown in Figure 7(b).

To validate the performance of the developed DC protection method, various RTHIL simulation tests were conducted. Table 1 shows the accuracy and the speed from 30 test cases. Three different line lengths and fault resistances are used in these tests. The test results indicate that the inductance estimation error is always less than 8.4% and the total fault detection and location time is less than or equal to 0.7 ms.

ID	Actual L (μH) / fault R (mΩ)	Estimated L (μH)	Error (%)	Fault location time (ms)
1	30 / 20	29.461	-1.80	~0.3
2	30 / 20	28.524	-4.92	~0.35
3	30 / 20	27.695	-7.68	~0.55
4	30 / 20	27.963	-6.79	~0.5
5	30 / 20	27.722	-7.59	~0.6
6	30 / 20	27.903	-6.99	~0.65
7	30 / 20	28.859	-3.08	~0.65
8	30 / 20	27.760	-7.47	~0.5
9	30 / 20	28.967	-3.44	~0.65
10	30 / 20	29.195	-2.68	~0.7
11	18 / 20	18.152	+0.84	~0.5
12	18 / 20	16.831	-6.49	~0.35
13	18 / 20	16.680	-7.33	~0.25
14	18 / 20	16.659	-7.45	~0.5
15	18 / 20	16.548	-8.06	~0.5
16	18 / 20	16.490	-8.39	~0.5
17	18 / 20	17.121	-4.88	~0.65
18	18 / 20	17.184	-4.53	~0.7
19	18 / 20	17.259	-4.12	~0.65
20	18 / 20	16.582	-7.88	~0.7
21	30 / 2	29.461	-1.80	~0.3
22	30 / 2	28.524	-4.92	~0.35
23	30 / 2	27.695	-7.68	~0.55
24	30 / 2	27.963	-6.79	~0.5
25	30 / 2	27.722	-7.59	~0.6
26	30 / 2	27.903	-6.99	~0.65
27	30 / 2	28.859	-3.08	~0.65
28	30 / 2	27.760	-7.47	~0.5
29	30 / 2	28.967	-3.44	~0.65
30	30 / 2	29.195	-2.68	~0.7

Table 1: Summary of 30 RTHIL test results.

4 Preliminary sensitivity analysis

In previous RTHIL tests, it is assumed that the voltage, current, and *di/dt* signals are measured accurately from the Opal-RT simulator. The error is only introduced by the D/A conversion of the Opal-RT simulator and the A/D conversion of the BeagleBone board. The A/D or D/A conversion accuracy is well controlled under 0.5%. In practical applications, there always are more errors in measurements. In this section, a preliminary sensitivity analysis on the measurement errors is conducted. The fault in the previous RTHIL test is used for this sensitivity analysis. The distance between the fault and the level 4 breaker is 50 m. The fault resistance is 2 mΩ.

In the voltage sensitivity analysis, the measurement errors of current and *di/dt* are assumed to be zero. The measurement error of the voltage signal is varied from 0.025% to 1.25% of the rated voltage (380 V). The inductance estimation results are shown in Figure 8. If the voltage measurement error is less than 0.5% of the rated voltage, the estimated inductance would be very close to the actual value. Similarly, the current sensitivity analysis is conducted through varying the current measurement error from 0.005% to 1.5% of the maximum current (2000 A) with the measurement errors of voltage and *di/dt* as zero. The inductance estimation results are shown in Figure 9. The estimation accuracy is good enough if the current measurement error is less than 0.5%. For low current sensors, most of closed loop hall effect DC current sensors can achieve this accuracy requirements.

In case of higher measurement errors in voltage or current, a digital low-pass filter with a small time constant (less than 1

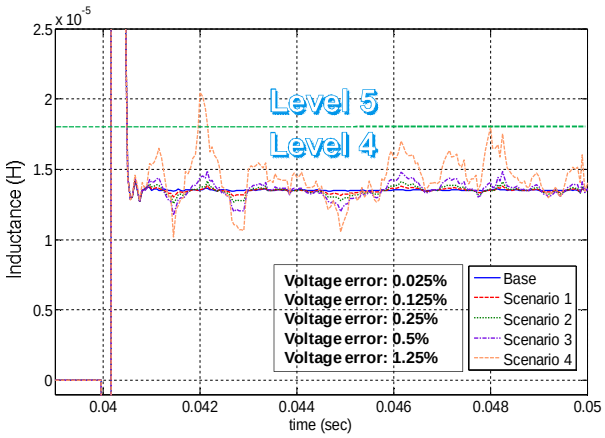


Figure 8: Sensitivity analysis for voltage measurements.

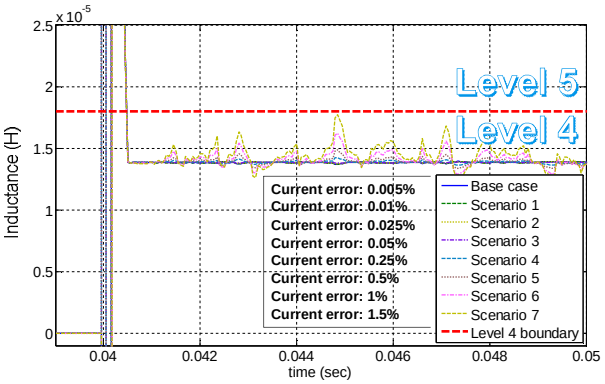


Figure 9: Sensitivity analysis for current measurements.

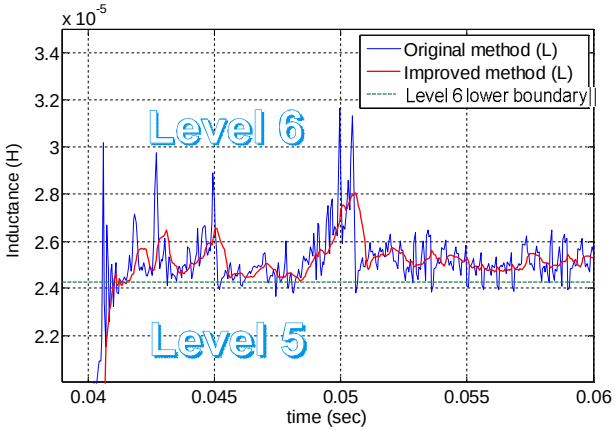


Figure 10: Improved inductance estimation result.

ms) is applied on the estimated inductance to filter out spikes. The comparison of the original and the improved inductance is shown in Figure 10. The low-pass filter smooths out the estimated inductance and thus helps DC fault location. The disadvantage is the time delays introduced by the filter. The sensitivity study in this section is just a preliminary analysis. More detailed analysis will be given in a future paper.

5 Conclusions

This paper presents a fault inductance based DC fault protection method for DC distribution systems. The developed method only needs local voltage, current, and di/dt measurements without any communication, so the protection speed is fast and the reliability is high. The protection scheme was implemented on a TI microcontroller. The implemented protection algorithm was tested on a RTHIL simulation platform. The RTHIL test results indicate that the fault detection and location speed is within 1 ms and the estimation error is less than 8.4%. The developed method can accurately locate faults if measurement errors are below certain levels. If measurement errors are high, measures, such as filters, should be adopted to improve the accuracy of the estimated inductance.

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