Applications of an Auxiliary Resonant Commutated Pole Converter

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***Abstract*- The Auxiliary Resonant Commutated Pole Converter (ARCP) utilizes an auxiliary resonance circuit to enable zero voltage turn on in the main circuit and maintain zero current turn off in the auxiliary circuit. The ARCP converter can therefore be designed with snubbers that are undersized for the power rating of the switches. Another advantage of the ARCP converter is that it can be driven by a PWM control source. This paper discusses some concepts that need consideration in order to operate an ARCP converter with undersized snubber circuits and standard PWM sources. It also discusses the need to coordinate the voltage supply and the load current for successful commutation. Test data is presented related to these issues.**

INTRODUCTION°

The Auxiliary Resonant Commutated Pole Converter (ARCP) has been, since it was first introduced [1], one of the best topologies for achieving soft-switching in high power converters. Figure 1 shows a single-phase equivalent circuit of the ARCP inverter, which is essentially the circuit proposed in [1], where a detailed explanation of its basic functioning is also given. The zero voltage turn on of the main power switches, S1 or S2, is achieved by using, in addition to the standard inverter pole, an auxiliary circuit that drives the voltage across the main switch to zero by inducing a resonance between an inductor L_r and the snubber capacitor C_r across the switch.

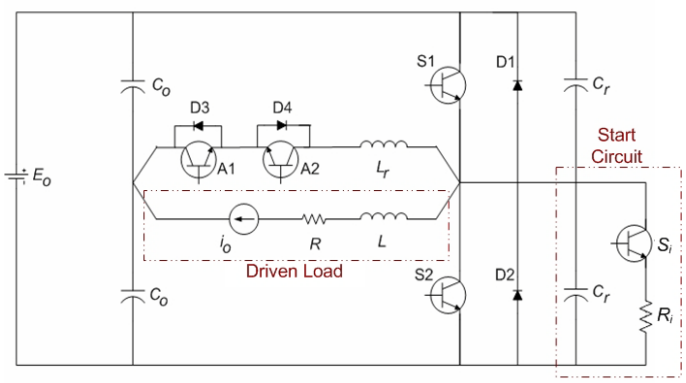

Figure 1: Single phase ARCP circuit topology with initializing circuit (S_i, R_i).

At the Center for Electromechanics of the University of Texas, (CEM-UT) a 2-MW ARCP converter has been built and is being testing an as part of a larger project as described in [2] and [3]. The converter's main specifications are listed in Table 1 and a photograph of the converter is shown in Figure 2. There are 4 compartments in the converter with the controls and brake section behind the left-most 2 doors and the phase A and phase B compartments (doors off) to the right (Phase C is not shown).

TABLE I
ARCP INVERTER DESIGN PARAMETERS

			units
Bus Voltage	Minimum Nominal Maximum	1,000 1,960 2,400	Vdc
Output	Voltage, L-L Current , L	1,100 1,200	Vrms Arms
Frequency	Output fund. Switching Commutation	0 ~ 250 4 40	Hz kHz kHz

It must be noted that, whereas the equivalent circuit shown in Figure 1 is very useful in the detailed theoretical description of the commutation process, the actual connection of the converter to a 3-phase load may or may not have a hard wired current return path to the DC bus center, as shown. In fact, the CEM-UT converter drives a delta-connected load so that the load current initiated in one phase is returned to the DC bus via the next phase in the firing sequence. Figure 3 shows this arrangement schematically: there each converter phase comprises a circuit identical to that shown in Figure 1 except for the driven load, which is now shown separately in the delta motor configuration.

° *This material is based upon work supported by Federal Railroad Administration cooperative agreement, DTFR53-99-H-00006 Modification 7, dated May 2006. Any opinions, findings, and conclusions or recommendations expressed in this publication are those of the authors and do not necessarily reflect the view of the Federal Railroad Administration and/or U.S. DOT.*

Figure 2: Operational ARCP converter showing control bay (left), brake bay, and the A & B phase bays (right, doors off).

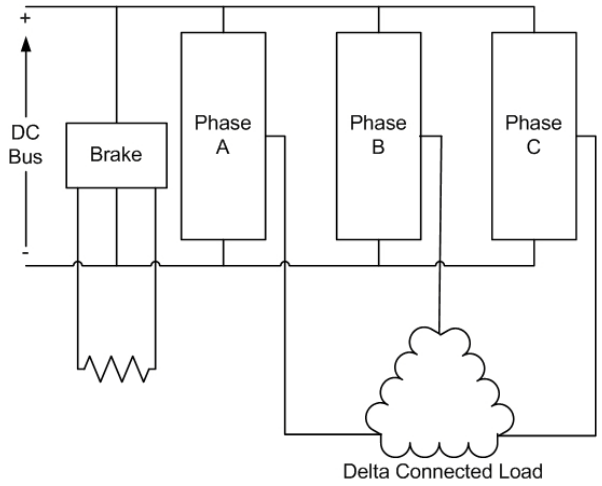

Figure 3: Block diagram of the CEM-UT 3-phase ARCP drive and delta-connected load.

I. INITIALIZATION OF THE SYSTEM

The soft-switching operation of the ARCP results in many advantages, among which is the very practical one of being able to operate it with much smaller snubbers than those used in its hard-switched counterpart.. However, the system needs to be in the full switching sequence in order to generate the currents that force the soft commutation. This creates a difficulty upon start-up since the switches cannot be properly activated unless the system is already running. The solution to this involves adding a hard switched device in parallel with either the upper or lower switches to discharge the switch capacitors before the initial gate signal is allowed through. Furthermore, the control circuitry, implemented in a Field Programmable Gate Arrays (FPGA), must insure that the first gate signal of the sequence is applied to the switch whose snubber capacitor has just been discharged, either the upper or the lower. In the CEM-UT converter the lower switches have been chosen for the discharge circuitry as shown in Figure 1. This start circuit, activated only upon start-up, will reduce the voltage across the negative bus switches to zero so that normal operation can begin.

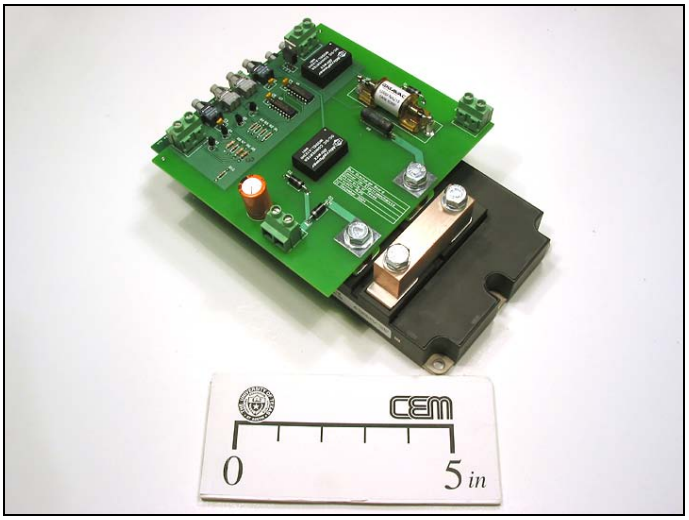

Figure 4: Phase start circuit with discharge switch and resistor and control interface.

The time required to discharge the capacitor in the start circuit, $\tau = R_i C_f$, can be arbitrarily long or short, so R_i can be chosen to make the discharge switch (S_i) and resistor a convenient size. Figure 4 shows the start circuit built for the CEM-UT inverter. The IGBT discharge switch is the same component used for all of the main and auxiliary switches to maintain commonality of parts. The board also contains a 5-W discharge resistor, R_i, and a high voltage isolation switch, which serves to reduce the liability for voltage breakover faults after the start function is completed. A fiber-optic control completes the board assembly. The discharge time is long compared to the normal commutation time and, while the capacitor is being discharged, all gate pulses to the main converter switches are blocked. Upon achieving full discharge, the zero voltage condition across the S2 switches is reported by a sensing circuit to the FPGAs that initiate the firing sequence with the gate signals to the S2s as shown in Figure 5.

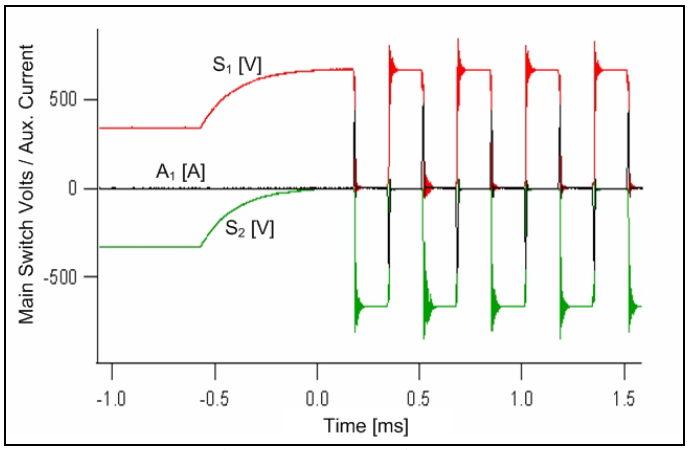

Figure 5: Voltage waveforms at the startup of the ARCP converter driven to zero by the discharge circuitry.

II. SHORT PWM PULSES

The resonant process whereby the voltage across the main switches is driven to zero is not an instantaneous one but takes a finite amount of time. The next transition cannot begin until the previous cycle has finished. When using a standard PWM controller the pulse width becomes arbitrarily small for a m_a near 0 or 1. The zero crossings (m_a = 0) guarantee that there will be pulses generated that transition faster than an ARCP converter can respond. In the particular case of the CEM-UT converter, the time needed to completely commutate is approximately 15-18 us as shown in Figure 6. Thus, no PWM pulses shorter than this time interval can be tolerated and, in this case, the control circuit will detect a conflict and the drive will go into a benign shutdown.

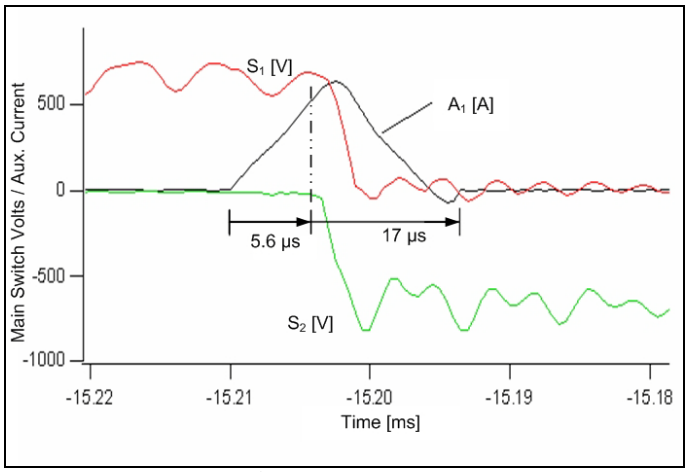

Figure 6: Measurement of the time required to complete one transition.

There are two solutions to this problem: one is to generate a custom PWM signal to feed the ARCP converter with only valid pulse widths ($t_{w(min)}<m_a<t_{w(max)}$, where $t_{w(min)}>0$, and $t_{w(max)}<1$), the other is to filter a standard PWM signal to eliminate all pulses shorter than the maximum expected transition time. The latter approach was selected for the ARCP converter at CEM-UT. A digital filter was implemented with FPGAs to ignore all pulses shorter than a pre-selectable time. Figure 7 shows an example of the effective blanking out of unwanted short pulses from the PWM signal used to drive our converter. Figure 8 is a wider view of the filtered gate signals for S1 and S2 of a single phase. It can be seen to effectively remove gate transistions whenever the modulation index is too close to 0 or 1. It must be noted that the elimination of short pulses from the PWM sequence has the inevitable result of distorting the waveforms since the full PWM sine coding has been altered. This necessary compromise must be taken into account in the design process. The distortion, although minor, has not been quantified in the current set-up as of this writing.

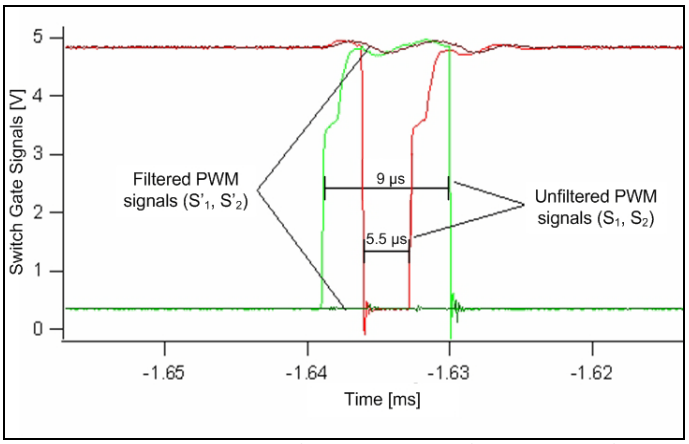

Figure 7: Original PWM waveforms and outputs of the short pulse filter.

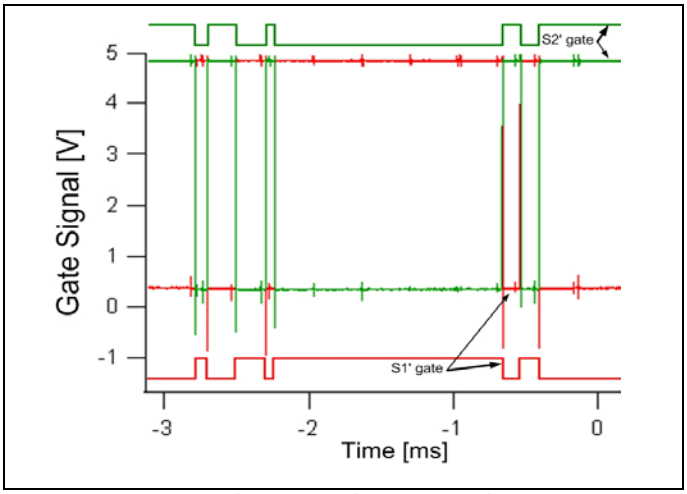

Figure 8: Filtered output of gate signals for S1 and S2 of one phase (upper and lower traces added for clarity).

III. VOLTAGE AND CURRENT REQUIREMENTS

At the writing of this paper, the high voltage DC supply needed to power the DC bus was just getting ready for use. Therefore, the converter has been preliminarily tested using rectified laboratory 460 Vac power, capable of supplying only a 680 volt DC bus. This, of course, limits the capability to generate the required current for commutation. This limitation becomes more severe the higher the current load required to be commutated by the ARCP converter. The current in the

auxiliary circuit that allows the soft-switching of the main switches is controlled by three variables: the auxiliary inductance, the DC bus voltage, and the boost time. The boost time is defined as the amount of time that the auxiliary current is allowed to flow before the main switch currently ON is turned OFF, starting the commutation process [1]. In Figure 6, the boost time is marked at 5.6 µs. The auxiliary inductance value is dictated by the desired resonance period as compared to the period of the switching frequency. Once chosen, its value is fixed. The DC bus voltage is set by the available supply. If this is lower than the rated voltage, as in our preliminary tests, one is left only with the boost time as a means to make up for any deficit: an increase in boost time means an increase in the auxiliary current with it. At this point in the test process, the CEM-UT converter has been limited to the 680 volt DC bus while the eventual DC bus voltage will be 1960 Volts.

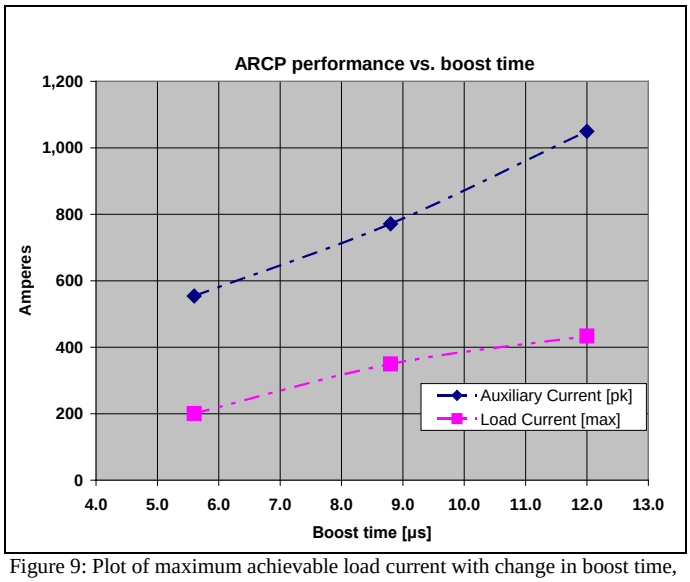

Figure 9: Plot of maximum achievable load current with change in boost time, with the 680 Vdc bus.

A sequence of several tests were conducted with the boost time increased progressively from 5.6 µs, to 8.8 µs, and to 12 µs to see how this would compensate for the limits set by the low DC bus. The results of these tests have been summarized in Figure 9. Figure 10 and Figure 11 provide a comparison as the peak auxiliary current is increased from about 630 A, t_{Boost} = *5.6 µs*, to 1030 A, t_{Boost} = 12 µs. When the maximum achievable load current (Figure 9) was exceeded, the inverter would simply fail to complete the commutation and all switching would stop in a benign shutdown.

However, in addition to the increased capability to commutate the load current, the larger auxiliary current pulse also creates more noise on the DC bus upon turn-off of the main switches, as can be seen from Figure 11. In fact this ringing noise can become so large as to be comparable to the DC bus voltage itself, leading to more instability in the ARCP operation. This problem is particularly bothersome at low DC bus voltages, as were used in the preliminary tests. It is expected that, with the DC bus voltage in the proper range shown in Table 1, this ringing will be a smaller percentage of the bus voltage and will not compromise the operation of the ARCP converter.

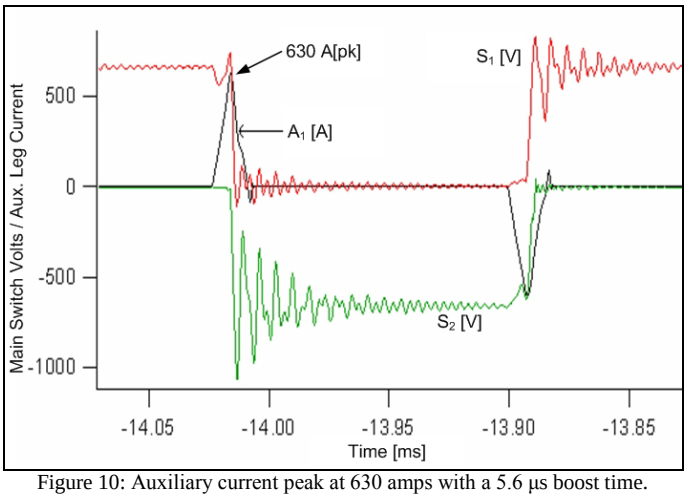

Figure 10: Auxiliary current peak at 630 amps with a 5.6 µs boost time.

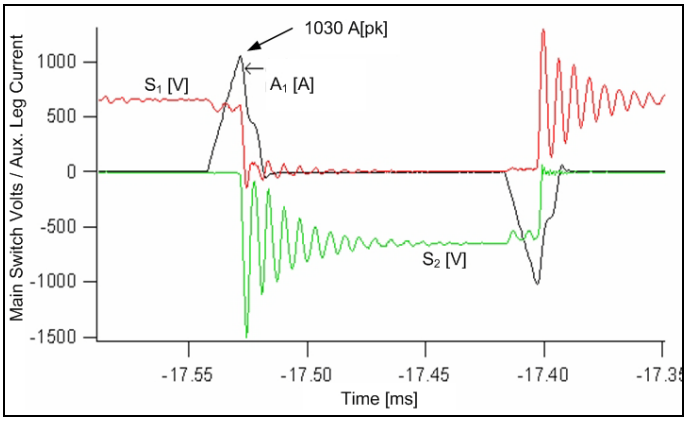

Figure 11: Auxiliary Current peak at 1030 Amps and the oscillations on the switch voltage with a 12 µs boost time.

This approach of increasing the boost time produces the concomitant issue that the extended boost time directly affects the time required to commutate (Figure 12). It also requires a modification to the PWM filter design or of the PWM source specifications as discussed previously. Undoubtedly, using a variable boost time controller would be desirable. The boost time could be updated automatically by the control circuit depending on the level of the load current and the bus voltage. This may also mitigate some of the increased harmonics resulting from filtering short PWM pulses. The added complexity of this approach has, for the time being, discouraged its adoption by CEM-UT. A fixed boost time, sufficient to cover the anticipated needs, is currently being used, leaving the tunable boost time for a next generation design.

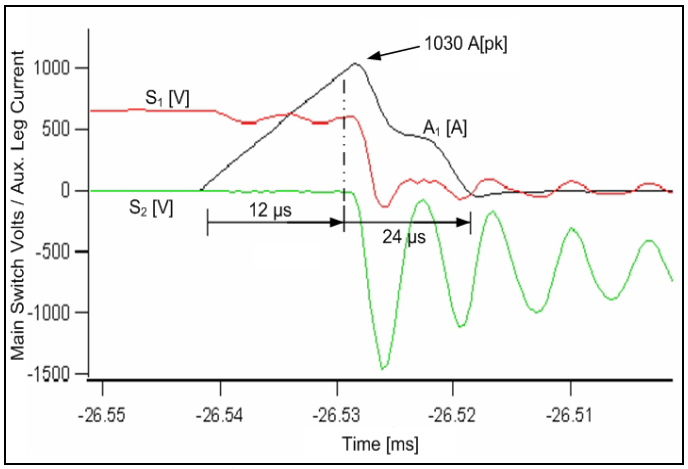

Figure 12: Time required for complete commutation with extended boost time.

CONCLUSIONS

The ARCP converter offers potential gains in size and efficiency of power conversion and with proper consideration of its characteristics can be used to run high speed and high power loads. Some precautions, however, are in order, as discussed in this paper:

a. A start up circuit should be used to properly initialize the switching sequence,

b. A custom PWM source with 9-switch output may be advantageous over implementing the translation of commercial off-the-shelf PWM controller (6 switch) outputs, and

c. Careful consideration should be made of the load current requirements and the auxiliary current needed to commutate the switches under load. This last point becomes a further consideration, particularly, if the DC bus is subject to variation as it often is in mobile applications.

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