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Graphene and MoS_2 Devices for Wafer-Scale Integrated Silicon Nanotechnology

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Graphene and MoS_2 Devices for Wafer-Scale Integrated Silicon Nanotechnology

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Dedicated to

My Mother and My Father

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Graphene and MoS_2 Devices for Wafer-Scale Integrated Silicon Nanotechnology

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The largest applications of layered two-dimensional (2D) materials such as graphene and transition metal dichalcogenides (TMDs) will likely be realized when combined with ubiquitous Si very large scale integrated (VLSI) technology. The two grand challenges to realize this goal are wafer-scalable device development which preserves the high performance of mechanically-exfoliated 2D films, and integration of 2D materials onto Si CMOS via scalable bonding transfer.

To address the first challenge, we investigate the scalable growth of polycrystalline graphene and MoS_2 through chemical vapor deposition (CVD) and their integration with Si VLSI technology. Material characterization techniques (STM, XTEM and XRD) are used to investigate the quality of the grown graphene film. The uniformity of the grown film is probed through large-area Raman mapping on 150 and 300 *mm* Si substrates and reveals > 95% monolayer uniformity with negligible defects. The electrical properties of the grown film on 100 *mm* substrate are investigated by transferring it to a target Si substrate. About 26,000 graphene field-effect transistors (GFETs) were realized by conventional Si-CMOS compatible fabrication method. The field-effect mobility, sheet

and contact resistance are investigated on a statistically large number of devices chosen randomly. Intrinsic graphene features such as soft current saturation, three-region output characteristics at high electric field and frequency doubler and amplifiers are observed on the wafer-scale. Our growth and transport results on scalable CVD graphene have enabled 300 *mm* synthesis instrumentation that is now commercially available.

Using similar growth and development mechanisms, we investigated the large-area growth of monolayer MoS_2 on Si platform and probed the electrical properties of the film by using a platform of back-gated field-effect transistors (FET).

To address the second grand challenge, we developed a novel method for mechanical delamination of graphene onto an arbitrary target substrate that potentially can be scaled up to wafer-scale. Large area and high quality graphene synthesized on Cu film, using the above-mentioned process, is transferred to a Si substrate using a novel direct mechanical delamination process based on fracture mechanics. The electrical characterization of the transferred film indicates the good quality of the mechanically delaminated graphene and holds great promise for the future integration of 2D materials with Si-CMOS.

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Chapter 1 : Introduction

1.1. MOTIVATION

Two-dimensional (2D) materials have attracted widespread attentions in different science and engineering fields over the last decade due to their novel electronic, optical and mechanical properties. These materials are atomically thin layered crystalline solids which represent the thinnest unsupported crystalline materials that can be realized. Their layered structures are defined by covalent bonding within each layer and van der Waals bonding between the layers. The mostly well-studied 2D materials are graphene and transition metal dichalcogenides (TMDs).

Graphene, the two-dimensional sheet of carbon atoms, has attracted a lot of attention on a wide variety of high-performance device applications after its first experimental discovery about a decade ago.[1] The main reason behind the fast development of graphene research is due to its unique properties that have already surpassed those observed in other types of materials such as enhanced electrical and thermal conductivity, high mechanical strength, high impermeability to gases and optical transparency. However a lack of a bandgap in graphene has been a drawback to its application in low-power switching or digital transistors. The limitation of graphene applications in digital devices, has motivated the search for other 2D materials with substantial bandgap such as TMDs.

Molybdenum disulfide is a prototypical TMD that has been attracting interest due to it large semiconducting band structure ($E_g \sim 1.8\ eV$ for monolayer and 1.3 eV for bulk films) which is ideal for bulk electronics. However its reported relatively low carrier

mobility (< 200 $cm^2/V.s$ at room temperature) limits its application for high-speed digital electronics.

Nevertheless, the largest application of 2D materials will likely be realized when combined with ubiquitous Si complementary metal-oxide-semiconductor (Si-CMOS) technology (Figure 1.1). However, this integration has proven to be a grand challenge due to (i) the lack of a reliable large-scale preparation scheme for graphene and other 2D materials which preserves the high performance of the mechanically-exfoliated films and (ii) a reliable transfer/bonding method for bonding 2D materials to the target Si substrates.

Over the past decade, researchers have developed methods to address the above-mentioned challenges. Several different methods have been proposed for growing wafer-scale graphene, including epitaxial growth on SiC wafers,[2,3] reduction of graphene oxide,[4,5] chemical vapor deposition (CVD) on metal thin films,[6-8] and recently on hydrogen-terminated single-crystalline germanium surfaces.[9]

The epitaxial growth of graphene has been performed on both the so-called Si-face or C-face of SiC wafers at ultra-high vacuum (UHV) condition and at typical temperatures above 1200 ^oC has often resulted in mainly multilayer graphene.[2,10] The epitaxial growth on h-BN substrates reported at relatively lower temperature of ~500 ^oC is restricted mainly by the size and the high cost of the growth substrates.[11] Even though, this development method can potentially be used for developing graphene on commercial SiC substrates, it is restricted by the high cost of the growth substrates and high temperature processing and therefore not compatible with Si-CMOS processing.

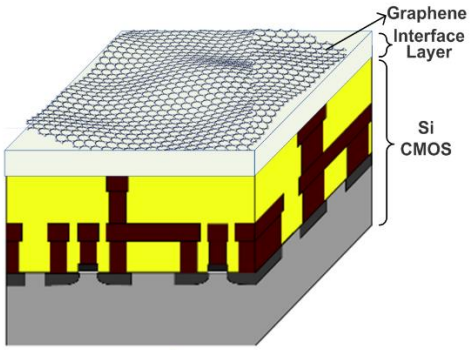

Figure 1.1: Schematic showing the integration of graphene with Si-CMOS circuit.

The reduction of the graphene oxide sheets performed at lower temperatures of ~ 300 *°C* often results in multilayer graphene which has applications mainly as composites, coatings, transparent and conductive layers and energy storage,[12] and is not suitable for VLSI applications.

The CVD mechanism based on gaseous and solid carbon sources, among the abovementioned methods, is the most well-studied and reproducible mechanism and is more likely to be compatible with VLSI technology. The CVD mechanism based on gaseous and solid carbon sources can be achieved on catalytic metal substrates at temperature as low as 650 *°C* and 300 *°C*.[13, 14] The CVD process can be described in three different stages; in the first stage, the precursor molecules collide with the surface and they can adsorb on it, scatter back to the gas phase or directly proceed to the next step. In the second stage, the carbon source molecules, dehydrogenates or partially dehydrogenates to form active species on the catalyst surface and finally in the last stage, these active species coalesce, nucleates and form graphene. Liquid sources of carbon have higher adsorption energy on Cu (111) surface and lower activation energy of dehydrogenation and smaller

nucleation barrier energy compared to the gaseous precursor.[15] It results in lower temperature of graphene growth for liquid and solid precursors.

The CVD growth of graphene based on CH_4 precursor on Cu foils have been investigated, where the former (Cu foils) has been the most widely adopted method. However, the CVD growth of graphene on inexpensive and widely-available Cu foils while having great potential for roll-to-roll or flexible technology,[6,16,17] is not compatible with Si CMOS integration process due to the lack of mechanical rigidity of Cu foils. On the other hand, deposited Cu films on standard oxidized silicon wafers that afford integration compatibility with Si VLSI, previously suffered from uncontrolled polycrystalline structure that leads to defective graphene formation with inferior performance like lower carrier mobility.[18] Recent progress revealed the growth of monolayer graphene with minimal defects by controlling parameters such as hydrogen or oxygen on the Cu surface to promote Cu(111) crystallization or to suppress graphene nucleation, resulting in the growth of large graphene domains across several Cu grains respectively.[19-21] These studies suggest that the high-quality of graphene synthesized on polycrystalline films is sufficient for device applications. Most remarkably, transport studies on polycrystalline graphene reported here offer higher peak mobility and improved sheet resistance than previous reports on single-crystalline synthesized graphene.[9,22] This counter-intuitive observation can be understood from theoretical and experimental analyses that suggest grain boundary scattering is likely not the dominant mechanism limiting charge transport in wafer-scale graphene devices.[23-25]

Nevertheless, due to the maturity of VLSI technology, the suitable growth and bonding methods for integrating 2D materials, must be compatible with the ubiquitous Si processing and make the most use of commercially available instrumentation.

Currently there are no general methods compatible with Si processing for integrating graphene grown by the current two major methods (CVD on metal films and epitaxial growth on SiC) with conventional Si integrated circuit platform. The most common approach for transferring CVD graphene grown on metal substrates is to use the PMMA-assisted stamp method which is obtained by etching the growth substrate and releasing and transferring the graphene, supported by PMMA stamp, onto the Si target substrate. This method can takes up to several hours and often results in wrinkled graphene and is not compatible with wafer-scale Si processing. Several transfer methods such as wet lift-off transfer, and electrochemical delamination that are convenient for small samples, are not scalable to full wafer sizes, which are required for practical large scale integration with silicon. To address the integration challenge, a reliable method for bonding/transferring graphene onto Si substrate must be developed. While the wafer-scale growth of graphene has been investigated extensively in the past few years, only a few efficient transfer mechanisms are suggested for integration of graphene with Si substrate that are semi-compatible with Si processing. Some of them are reviewed in the following paragraphs.

To address the bonding and transfer question from SiC wafers and inspired by silicon-on-insulator technology, Dong et. al.[26] reported bonding a silicon substrate to the graphene grown on SiC wafers. Using the mature SOI technology, hydrogen ions were implanted into Si substrate. In the next step both substrates were coated with thin Al_2O_3 films as the bonding interface. Upon heating the bonded interface to 400 ^oC, the silicon

wafer split at the ion implantation depth (smart cut). The results shown on 3 *mm* substrates suffer from low yield and restricted by the high cost and limited size of SiC wafers.

In a different approach, Kim et. al.[22] reported a layer-resolved graphene transfer from SiC wafers via engineered strain layers. In their method, they deposited a thin layer of Ni film followed by a thermal release tape on graphene grown on the SiC wafer. The binding energy between Ni-graphene ($\gamma_{Ni\text{-}G}$ = 140 *meV*) is higher than the binding energy between graphene-SiC wafer ($\gamma_{G\text{-}SiC}$ = 106 *meV*). The exfoliation of graphene from SiC wafer was induced by the accumulated internal strain of Ni film that was strongly bound to graphene. The exfoliated graphene was then transferred to a Si/SiO_2 wafer for device fabrication. This method showed on 100 *mm* wafers, allows the fast transfer of graphene and multiple use of SiC wafer for the subsequent graphene growth. However due to the multilayer nature of graphene grown on SiC wafer, multiple rounds of exfoliating were required for obtaining a single layer graphene.

Different approaches have been used to address the transfer and bonding issues of the graphene obtained by CVD method to Si platform. Wang et. al.[17] and Gao et. al.[27] reported direct electrochemical delamination of CVD graphene grown on Cu and Pt foils onto the flexible polyimide and Si substrates. In their method, the transfer substrate (polyimide) or PMMA is spin coated on the graphene grown on metal foil substrate. The delamination process takes place in aqueous Na_2SO_4 solution, Cu (Pt)/graphene/polyimide (PMMA) is used as the cathode and a Pt mesh as the anode electrode. By applying a direct bias across the cell electrodes, the water in the electrolyte solution undergoes electrolysis process to form hydrogen bubbles. The hydrogen helps to separate graphene from the foil substrate. This fast-paced transfer method preserves the surface topology of graphene and does not result in wrinkles and ripples that are inevitable in PMMA-assisted stamp method,

however is not compatible with Si processing due to the flexible nature of the growth substrate.

In a somewhat different approach based on fracture mechanics, Yoon et. al.[28] used a dry transfer process based on direct mechanical delamination to transfer CVD graphene grown on Cu coated Si substrate to a flexible substrate. In their etch-free approach, the growth substrate of graphene is bonded to a second silicon substrate through a thin epoxy layer. Using double cantilever beams, an adhesion energy of 0.72 Jm^{-2} was reported for graphene and Cu film. Using a similar approach and by controlling the separation rate of the double cantilever beam, Na et. al.[29] transferred graphene grown on the copper foil onto a Si substrate. The adhesion energy reported between graphene and Cu foil is 6 Jm^{-2} and graphene and epoxy is 3.4 Jm^{-2}. This technique offers several advantages including a contamination-free graphene surface and a low-temperature processing that is compatible with silicon technology. We used this technique to transfer CVD graphene from Cu thin films to Si substrate.

1.2. OUTLINE

The dissertation is organized as follows. Chapter 2 is focused on CVD growth of graphene on 100-300 *mm* substrate and the large-scale material characterization. The transfer process of the graphene to a 100 *mm* Si substrate for device fabrication is explained in Chapter 2. In chapter 3, the steps taken for the fabrication and characterization of back-gated graphene field-effect transistors (GFET) are explained. The device yield and electrical transport properties of the FETs at room and low temperature from a statistical point of view is discussed as well. In Chapter 4, a new bonding technique based on mechanical delamination of graphene onto the target substrate will be introduced and the

film properties is compared to graphene transferred using PMMA-assisted method. In Chapter 5, CVD growth process of MoS_2 on SiO_2 and Si_3N_4 substrates and the statistical electronic properties of monolayer MoS_2 using a FET platform will be discussed. A new passivation technique for improving the electrical performance of FETs on monolayer MoS_2 will be discussed. Finally in chapter 6, the conclusion is summarized and future steps will be discussed.

Chapter 2

Wafer-scale Polycrystalline CVD Graphene[1]

2.1. Role of kinetic factors in growth of CVD graphene

The kinetic of the CVD growth process of graphene on Cu catalyst surface is depicted in Figure 2.1. The precursor molecules first reach the surface of the catalyst film and get absorbed on the surface. In the next step, they decompose to form active carbon species and diffuse on the surface of the catalyst or into the catalyst, close to the surface. Finally the hydrogen atoms form H_2 gas and leave the surface while the diffused carbon atoms form the graphene on the surface of the catalyst film.[30]

The CVD growth of graphene starts by preparing the substrate. The growth substrates consist of ~ 500-900 *nm* copper film, deposited using electron-beam (e-beam) evaporation method at a vacuum level of 4E-6 *Torr*, on commercially-available 300 *nm* thermally-grown SiO_2 on Si wafer. The CVD graphene synthesis procedure was carried out in an AIXTRON BM300T® CVD system with cold-walls chamber and a substrate and a shower-head heater setup for a uniform heat-distribution on the 100 *mm* growth substrate. Here we use a low-pressure CVD (LPCVD) process (0.1-1 *Torr*) to grow graphene.

The graphene growth on a metal catalyst is controlled by factors including the carbon solubility limit in the metal catalyst, its crystal structure, lattice parameter and thermodynamic parameter such as the temperature and pressure of the system. The chamber is pumped down to 0.01 *mBar* (~0.8 *mTorr*). The hydrogen gas is then introduced

[1] This chapter is based on reference 32. S.R. did the graphene growth and measurements, L.T helped with the graphene growth, F.C. and S.P helped with low-T measurements, A.J., S. B, N. R., and K. T. provided the Raman data on 300 mm substrates and D. A supervised the work.

into the system (total pressure: 25 *mBar*) and the system is heated up to the final annealing/growth temperature ($T \sim 900\ ^{o}C$). At 900 ^{o}C, the Cu films are annealed first in hydrogen-saturated ambient (flow rate: 1000 *sccm*), for 5 minutes to initiate the Cu grain growth and remove the residual copper oxide.[20] Subsequently Pure methane gas is introduced into the chamber (flow rate: 15 *sccm*) for 6 minutes to initiate the graphene growth process. After that, the system is the cooled down to room temperature in hydrogen ambient.

The hydrogen-saturated annealing step is performed on the uniformly heated substrate, to promote the growth of hexagonal-phase Cu(111) structures (~> 10 μm) and is followed by the growth step with pure CH_4 and without H_2, which subsequently leads to the formation of scalable monolayer graphene with negligible defect density.

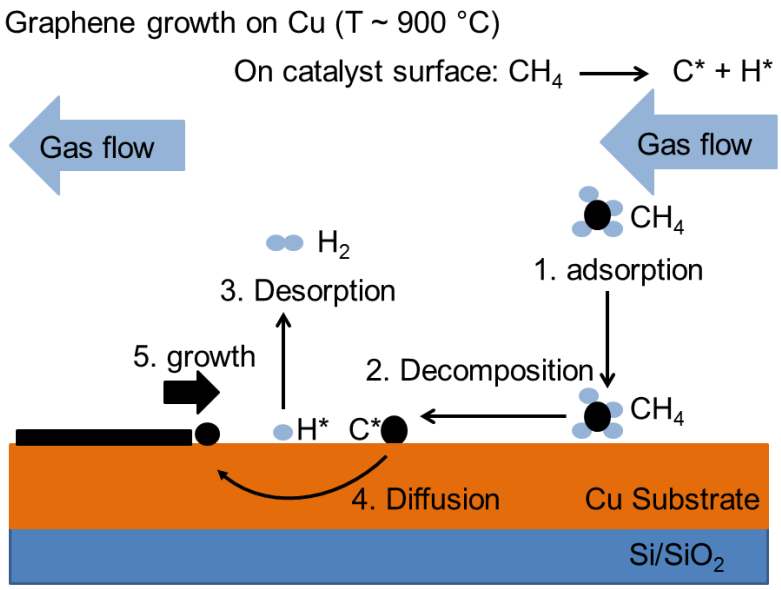

Figure 2.1: Illustration of CVD mechanism showing the steps that must be taken for growing graphene.

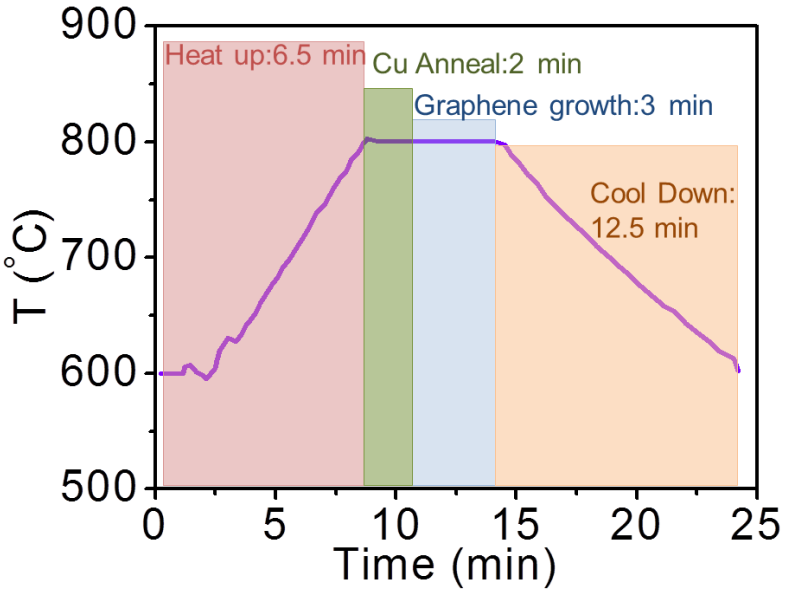

Figure 2.2: Process steps for growing graphene and their corresponding time scales. At ~ 600 *°C*, the infrared thermometer turn on and starts recording the chamber temperature at the center of the loading platform. From that point the complete growth process takes only 24 minutes. The lower growth temperature shown here is achieved in a 300 *mm* CVD chamber with multiple heaters for keeping a uniform heat distribution across the chamber.

2.2. CHARACTERIZATION AFTER GROWTH

2.2.1 Copper surface morphology

The atomic force microscopy (AFM) images shown in Figure 2.3 reveals that the e-beam evaporated copper film has polycrystalline texture with Cu grain size ~ 50 *nm* and a typical root mean square (rms) roughness < 5 *nm*. However, the annealing step in hydrogen-saturated ambient at 900 *°C* increases both the grain size to > 10 μm and the

roughness of the Cu film to ~ 30 *nm*. The polycrystalline structure of Cu film is copied by graphene and results in the growth of polycrystalline graphene.

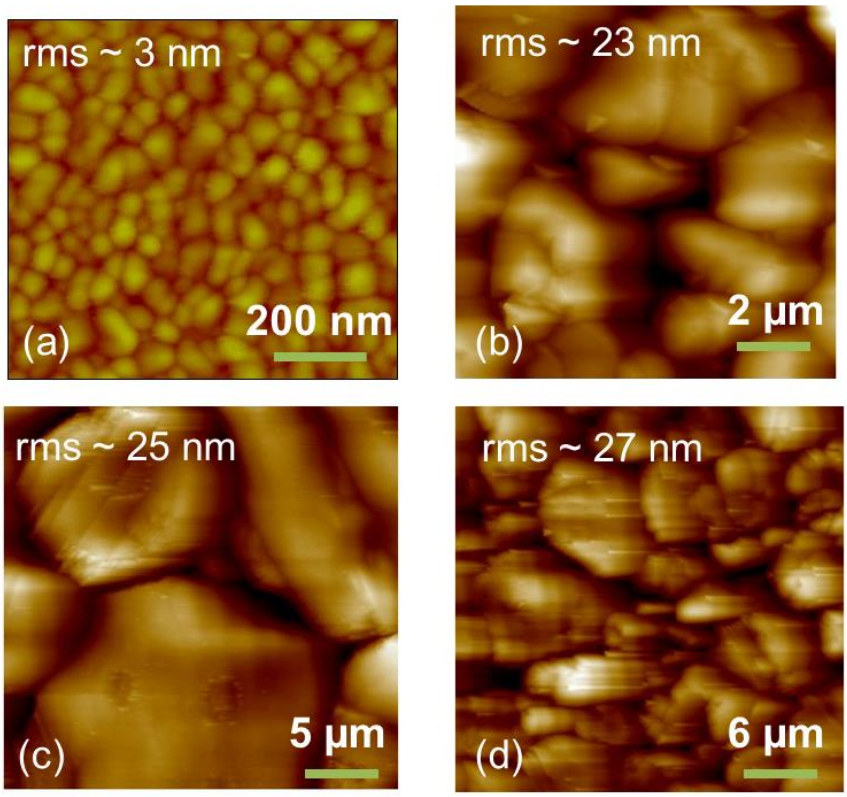

Figure 2.3: AFM images of the surface of the Cu film after deposition (a) and after annealing (b-d) reveals the grain size and roughness of the film increases after annealing. The scan area is 10, 20 and 30 μm for b, c and d respectively.

2.2.2. Copper crystalline structure

The X-ray diffraction (XRD) data reveals that the e-beam evaporated copper film has a polycrystalline nature with no dominant crystal orientation (Figure 2.4). After the

annealing step in hydrogen-saturated ambient, the Cu grains grow to a typical size > 10 μm and form a polycrystalline film with a dominant Cu (111) orientation. The hexagonal phase of Cu (111) structures with a lattice constant of 2.56 ^{o}A close to that of graphene (2.64 ^{o}A) has shown to promote the growth of monolayer graphene.[31]

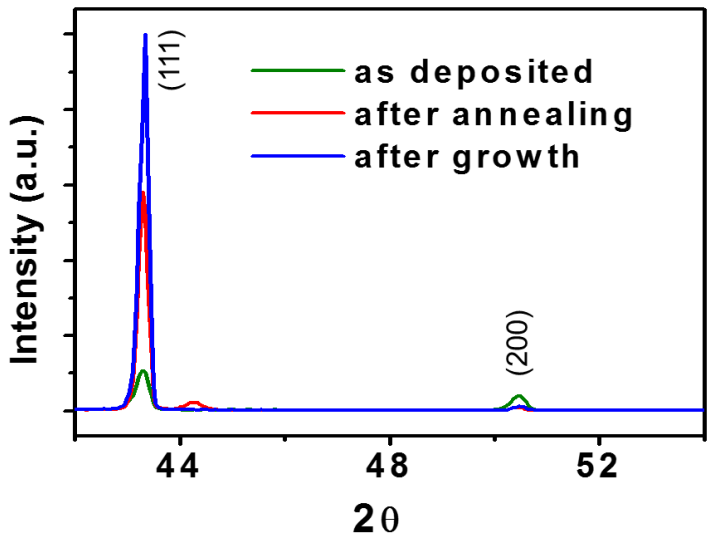

Figure 2.4: XRD data shows the growth of Cu (111) orientation is promoted after annealing and graphene growth steps compared to as-deposited films.

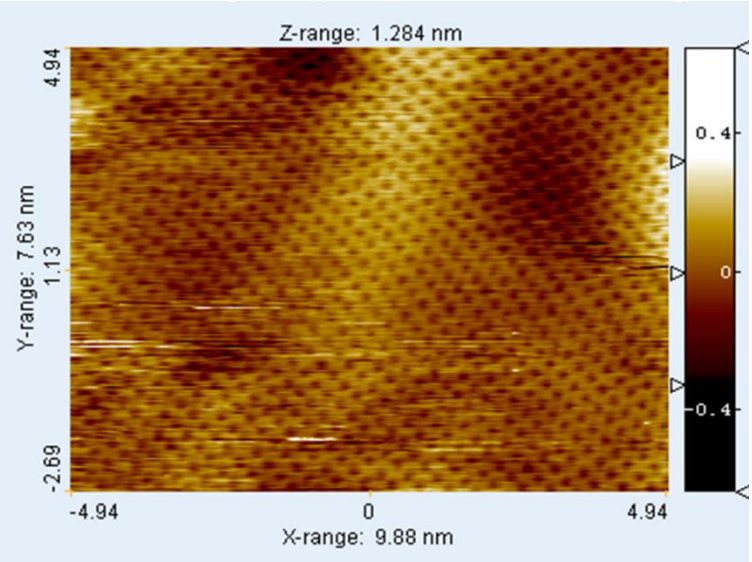

Figure 2.5: STM image shows the characteristic hexagonal networks of carbon atoms grown on Cu film substrate.

2.2.3. Graphene microscopy

To investigate the structural property of the grown film, we used scanning tunneling microscopy (STM) imaging. The STM image shown in Figure 2.5, reveals the characteristic hexagonal and honeycomb network of carbon atoms with a lattice constant of 2.64 ^{o}A. It confirms that monolayer graphene is grown using the CVD process that was developed for this study. The absence of no moiré pattern, an interference pattern that appears when two or more grids are overlaid slightly askew, is another indication of growing a single monolayer of graphene on the copper.

2.3. SCALABLE GROWTH OF GRAPHENE ON 100-300 *MM* WAFERS

The CVD graphene growth, demonstrated on 100 *mm* at 900 °*C* in BM300T® CVD system, has been adopted by our collaborators in AIXTRON on 150 *mm* and 300 *mm* substrates at lower temperature range of 750-800 °*C* (Figure 2.2). The images of the substrates used for this study are shown in Figure 2.6. The reduction in the growth temperature has been achieved by employing multiple heaters on the substrate platform and as a result a more uniform heating of the gas flux in the vertical and lateral directions. The homogeneous heat distribution in the growth chamber is critical in order to produce graphene with low defect density and uniform quality across the 300 *mm* wafer. The homogeneous heat distribution in the chamber is monitored by three thermocouples located at radius 49 *mm* (A), 125 *mm* (B) and 135 *mm* (C) from the center of the substrate. These locations correspond to the distinct substrate heating zones. The readings of these sensors at the end of annealing and growth steps are listed in Table 2.1. The difference between the temperature of the annealing and growth is due to the difference in the thermal capacity of gasses used during these steps.

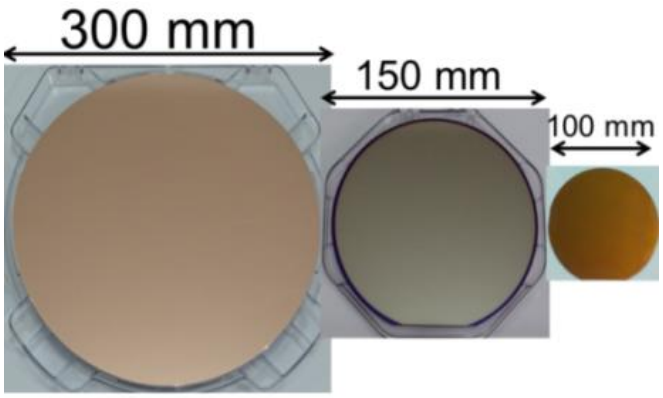

Figure 2.6: Images of the 100 to 300 *mm* substrates used for growing graphene for this study.

Table 2.1 Temperature readings of sensors located at three different regions of the substrate, the radius is measured from the center of the Si substrate.

Radius (*mm*)	Annealing Temperature (°*C*)	Growth Temperature (°*C*)
A: 49	771.5	763.5
B: 125	763.2	754.8
C: 135	765.3	755.3

2.4. RAMAN METROLOGY

To study the uniformity of the grown film on 150 and 300 *mm* substrates, Raman spectroscopy mapping was employed. Figure 2.7 shows the Raman spectroscopy mapping data of graphene grown on 150 *mm* Cu substrates (map area: 500 μm × 500 μm), collected using a 442 *nm* laser (Renishaw inVia) with a focal point size of 2 μm and a step size of 5 μm and an objective lens of 100X.

The mapping results, collected from five different locations of the 150 *mm* substrate (500 μm × 500 μm mapping area), shows an average value of ~ 2.62 for 2D:G intensity ratio (I_{2D}/I_G) with standard deviation of 0.19. Mapping of D:G intensity ratio (I_D/I_G) on the same locations, shows an average value of 0.06 with deviation of 0.008, indicating the good structural quality of the synthesized graphene on 150 *mm* substrates. Based on the statistical analysis of the Raman mapping data, monolayer graphene was achieved on 150 *mm* substrates with negligible defects.

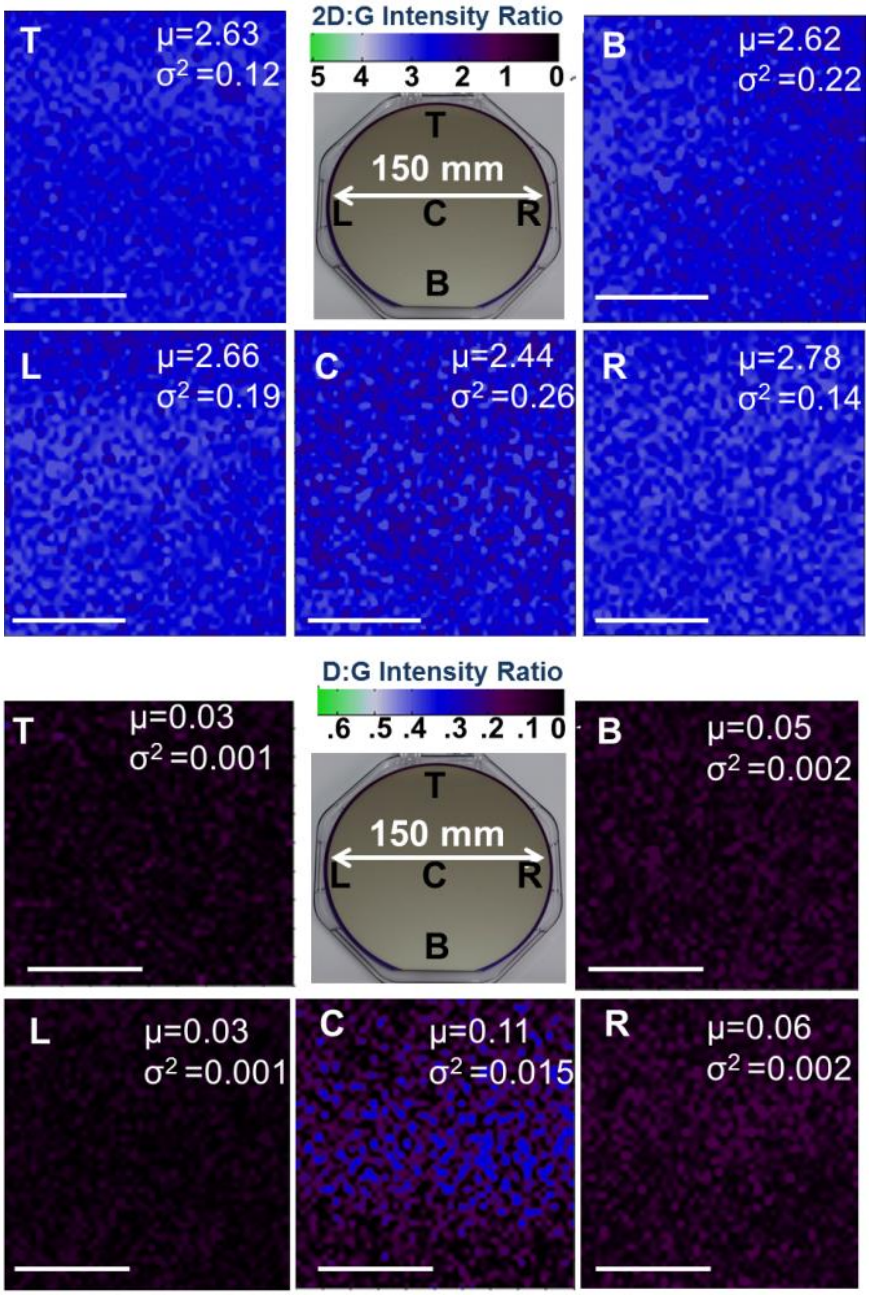

Figure 2.7: Large-area Raman mapping of graphene on 150 *mm* Cu substrates reveals > 95% monolayer continuity and average value of ~ 2.62 for I_{2D}/I_G and average value of ~ 0.06 for I_D/I_G. The average value and the standard deviation of I_{2D}/I_G and I_D/I_G for each Raman map are presented. The view of the 150 *mm* wafer, used for this study, is shown at the top center of the image. The scale bar represents 200 μm.

Similarly, Raman mapping was performed on a 300 *mm* substrate after growth using a 457 *nm* laser with focal point size of 0.9 μm, under ambient condition. The map data confirmed uniform monolayer graphene with a negligible defect peak, and average values of 0.2 and 3.4 for I_D/I_G and I_{2D}/I_G on an area of 150 μm ×150 μm at the center of a 300 *mm* substrate (Figure 2.8(a) and (b)). The view of the 300 *mm* substrate used for this study and the results of the Raman spot scans as a function of distance from the center of the wafer, are shown in Figure 2.8(c) and (d). An average value of 2.6 is achieved for I_{2D}/I_G spot scans along the radial direction comparable to the average I_{2D}/I_G on 150 *mm* substrate, confirming the scalability of the growth process.

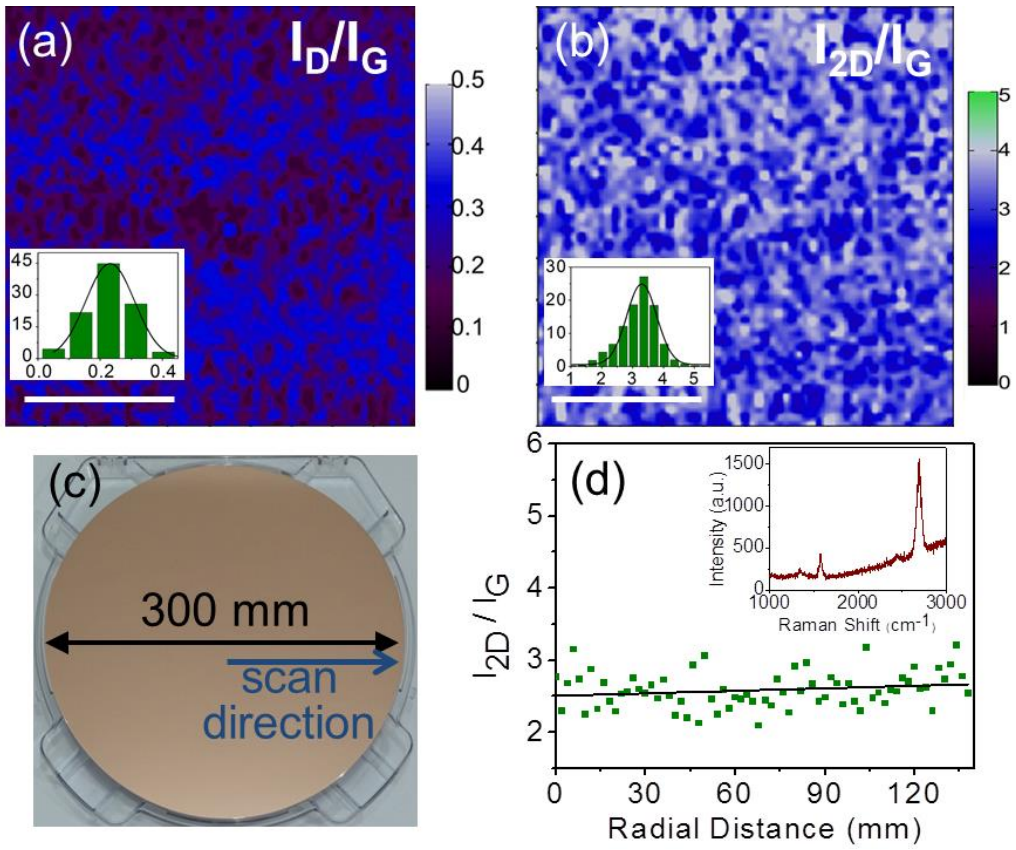

Figure 2.8: (a) I_D/I_G and (b) I_{2D}/I_G Raman mapping at the center of a 300 *mm* growth substrate shows high quality of graphene with a negligible defect peak, the insets are the histogram distributions of I_D/I_G and I_{2D}/I_G, with average values of 0.2 and 3.4 respectively. Scale bars displays are 50 μm. (c) View of the 300 *mm* substrate used for this study, arrow shows the direction of the Raman spot scans. (d) I_{2D}/I_G of Raman spot scans performed along the radial direction of the 300 *mm* substrate, the inset shows a representative Raman spectrum.

Table 2.2 Comparison of I_{2D}/I_G and I_D/I_G between different reported wafer-scale graphene synthesis methods.

Substrate size (*mm*)	I_{2D}/I_G	I_D/I_G	Reference
Cu film/ 100-300	**2.6-3.3**	**0.03-0.22**	**Rahimi, 2014 [32]**
Ge(110)†/ 100	3.5	0.03	Lee, 2014 [9]
SiC†/ 100	1.6-1.9	0‡	Kim, 2013 [22]
Cu film/ 100	3	0.2	Tao, 2012 [31]
Cu film/ 150	4.5	0.3	Heo, 2011 [13]
Ni/Cu films/ 75	3.5	0.25	Lee, 2010 [8]

† Single-crystalline substrates.

‡ Graphene structures always contain a finite defect peak.[33] No defect peak was reported, as such this reported value is likely to be incorrect.

2.5. DIMENSION OF THE GRAPHENE GRAINS

Table 2.2 summarizes the results of Raman spectroscopy scanning obtained here and compares it to other extracted and reported values of I_{2D}/I_G and I_D/I_G from wafer-scale CVD and epitaxially-grown mono- and polycrystalline graphene. Using equation 2.1, where L_a is the graphene grain size, and λ_l is the wavelength of the laser used for Raman spectroscopy, we also compare the graphene domain size obtained for different wafer-scale reports and compare them to the grain size obtained here,[34]

$$L_a(nm) = 2.4 \times 10^{-10}(\lambda_l^4)(\frac{I_G}{I_D}) \quad (2.1)$$

Table 2.3 Comparison of graphene domain size between different reported wafer-scale graphene synthesis methods.

Substrate size (*mm*)	L_a (*nm*)	Reference
Cu film/ 100-300	**40-350**	**Rahimi, 2014 [32]**
Ge(110)†/ 100	550-640	Lee, 2014 [9]
SiC†/ 100	---	Kim, 2013 [22]
Cu film/ 100	45	Tao, 2012 [31]
Cu film/ 150	~65	Heo, 2011 [13]
Ni/Cu films/ 75	~80	Lee, 2010 [8]

† Single-crystalline substrates.

The comparison shows the saturated hydrogen annealing and methane-only precursor for the growth step in this study leads to the largest graphene grain size and the largest value of I_{2D}/I_G while I_D/I_G does not exhibit a significant increase with scale-up in the growth wafer substrate.

2.6. GRAPHENE TRANSFER TO DEVICE SUBSTRATES

For the wafer-scale device fabrication, the graphene grown on 100 *mm* Cu film substrate was transferred to a 90 *nm* SiO_2 substrate by selective etching of the growth substrate.

The wet transfer process starts by coating the graphene on Cu film with a 200 *nm* thick PMMA film (M_w = 495,000 from Sigma-Aldrich) as the support layer. The PMMA was spin coated on the growth substrate with a spin rate of 2000 rpm and a ramp rate of 1000 rpm for 60 seconds. The edges of the substrate was then wiped off thoroughly with

acetone to clear off any PMMA trace that might have been left from the spin coating process. The PMMA coated substrate is then left inside a vacuum desiccator (~30 *mbar*) at room temperature for at least 8 hours. This long wait time helps the PMMA solvent to evaporate and leave a solid support film left on the graphene. In the next step, the PMMA-coated graphene is released by selective etching of the Cu substrate film using an ammonium persulfate ($(NH_4)_2S_2O_8$) (40 *ml*) mixed by Buffer Oxide Etch (BOE) 1:6 (1 *ml*) aqueous solution at room temperature. After the etching process is complete (~ 4 hours) the released PMMA-coated graphene is scooped out of the etching solution using the original growth substrate and is transferred to a beaker with clean DI water and left there for 30 minutes. After that, the graphene and PMMA support layer are then transferred to a 90 *nm* SiO_2 substrate and left in the vacuum desiccator for ~8 hours. This results in the interlayer water between graphene and substrate to evaporate and brings the graphene in contact with the SiO_2 substrate. In the last step, PMMA is baked at 180 *°C* for 3-5 minutes and the substrate is immersed in DI water for ~8 hours to remove the PMMA. The graphene is then rinsed with IPA and left in the vacuum desiccator to dry up for the fabrication process. The main steps of the graphene transfer process are shown in Figure 2.9.

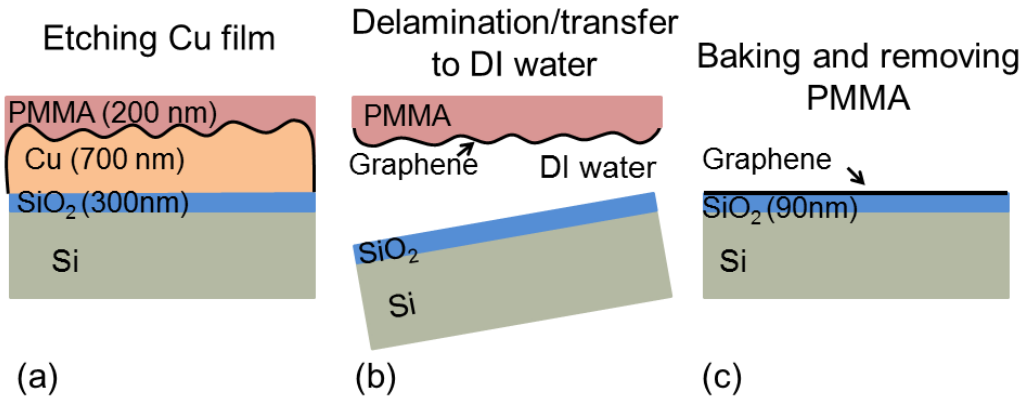

Figure 2.9: Illustration of the PMMA-assisted wet transfer of graphene, (a) Cu substrate etching, (b) graphene/PMMA stack being transferred to DI water, (c) Graphene is moved to its final substrate (90 *nm* SiO_2), PMMA is baked and subsequently removed in acetone.

2.7. GRAPHENE POST-TRANSFER CHARACTERIZATIONS

Several different characterization techniques were utilized for probing the material properties of graphene after the transfer process.

2.7.1 Number of grown layers

The cross-sectional images of the film after the transfer (Figure 2.10), taken by transmission electron microscope (TEM) reveals that, the transferred graphene is monolayer and has good structural quality.

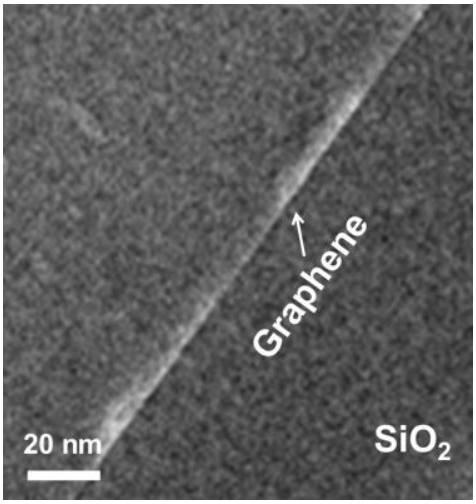

Figure 2.10: X-TEM image of the graphene after transfer to 90 *nm* SiO_2 shows the monolayer film has a good structural quality.

2.7.2 Surface roughness

After transferring the graphene to SiO_2 substrate, AFM imaging is used to quantify the surface roughness. CVD Graphene transferred by PMMA-assisted method is known to be rougher compared to the exfoliated graphene samples. The roughness mainly caused by the PMMA residue left on the graphene. The results of surface roughness measurements of graphene after removing the PMMA support layer is shown in Figure 2.11. The average rms roughness, normally more than 1 *nm*, could reach 4-6 *nm* for an area of 10 × 10 μm. The PMMA assisted transfer method is used in chapter 3 for transferring graphene from a 100 *mm* Cu film substrate to the same-size 90 *nm* SiO_2 substrate. This transfer method is not compatible with batch Si-CMOS processing. Therefore, in chapter 4, a new transfer method, compatible with batch Si processing, for graphene will be described, in which graphene is directly transferred to a secondary substrate without using a PMMA support layer.

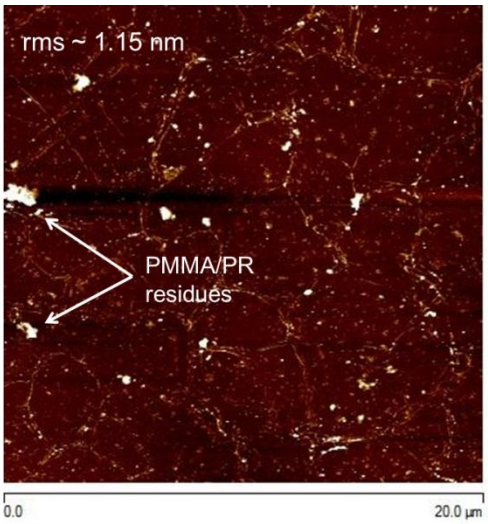

Figure 2.11: AFM image of the graphene after transfer to 90 *nm* SiO_2.

2.7.3. Post-transfer Raman statistics on 100 mm wafer

The wafer-scale graphene preserves its high quality after transfer from 100 *mm* growth substrate to the same wafer size. The Raman spot scans were collected from Graphene after the transfer to Si/SiO_2 substrate due to larger Raman scattering intensity on Cu substrate and lower spectral background on Si/SiO_2. Figure 2.12(a) shows the Raman spot scans, taken from five different locations on the 100 *mm* Si/SiO_2 substrate after the transfer with negligible defect peak and good quality across the 100 *mm* wafer. For instance, average value of I_{2D}/I_G after the transfer, presented in Figure 2.12(b), shows a narrow distribution within 2.5-3 with negligible defect ratio, comparable to the values extracted from graphene on the Cu film substrate and before the transfer.

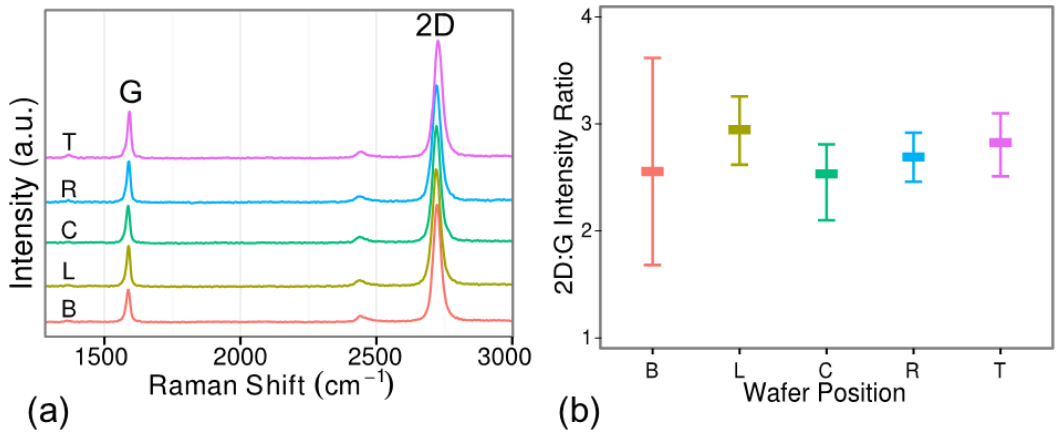

Figure 2.12: (a) Representative of Raman spot scans from five different locations of graphene transferred onto a 100 *mm* wafer, (b) Statistical distribution of I_{2D}/I_G on these locations gives an average value of 2.8.

2.8. SUMMARY

In summary, we have demonstrated the state-of-the-art on scalable CVD polycrystalline graphene synthesis. Different materials characterization techniques that used for probing the graphene properties, synthesized on 100 to 300 *mm* Si substrates, shows the grown film has superior properties compared to the previously reported polycrystalline graphene. The large-area Raman mapping method confirms the uniform quality of the CVD graphene grown on up to 300 *mm* substrates.

Chapter 3 : Graphene Field-Effect Transistors [2]

3.1. INTRODUCTION

In the previous chapter, the material properties of the CVD graphene grown on Cu film was studied through a variety of methods, such as AFM, SEM, TEM and mapping through Raman spectroscopy. In this chapter, the electrical properties of the CVD graphene is studied using the field-effect transistor (FET) platforms fabricated on the transferred graphene.

3.2. BACK-GATED GFETS

Two transistor structures have been mainly used and reported in the literature for studying the electrical properties of graphene; top-gated and back-gated structures. In the back-gated structure, the heavily p-doped Si wafers (Orientation: 100, Resistivity: 0.001-0.01 *Ohm.cm*, thickness: 525 μm) capped with 90 *nm* thermally-grown SiO_2, used as the target substrate for transferring graphene, are used as the gate stack. In contrast, in the top-gated structure, the gate dielectric and contact metal are deposited using a physical evaporation methods on graphene. For this study, a standard UV photolithography method was employed for fabricating about 26,000 back-gated GFETs.

To fabricate the back-gated GFETs, three layers of lithography are required. These three layers include patterning the alignment marks, the active device channel and source/drain contacts. In the case of chip-scale GFET characterization, all three lithography steps have been performed using PMMA as the resist material and e-beam lithography,

[2] This chapter is based on references 65. S.R. did the graphene growth and measurements. S. R. N. did the delamination tests. L. T. helped with the graphene growth. K. M. L. and D. A. supervised the work.

which has a low throughput, but results in smaller contamination of the graphene and therefore smaller contact resistance, larger mobility and a better device performance. It has been reported that employing photolithography using ultraviolet light sensitive polymer films (photoresist) results in more contamination of the graphene and therefore a lower device performance.[35] Nevertheless, the photolithography method is the process that is being used for Si processing technology and therefor it has to be used as the lithography method for the final purpose of integrating graphene with Si CMOS. For that reason, the back-gated GFETs for this study are fabricated using the photolithography process here.

3.2.1 Fabrication Process

The 100 *mm* Si substrate are thoroughly cleaned by Piranha solution for 10 minutes and rinsed with DI water afterwards. Using a dry oxidation process at 1000 ^{o}C, 90 *nm* SiO_2 is thermally grown on the Si substrate.

In the first step of the device fabrication process, the alignment marks (AM) are patterned on the substrate. To pattern the AM, lift-off resist (LOR) is used to facilitate the lift-off process. LOR 3B is spin-coated on the substrate (3000 rpm for 45 seconds) and is baked on the hot plate at 170 ^{o}C for 5 minutes. The thickness of the LOR that depends on the spin speed and the baking temperature is measured to be ~ 450 *nm* after baking. Then positive photoresist (PR) S1805 is spin-coated on the substrate (4000 rpm for 60 seconds) and is baked on the hot plate at 120 ^{o}C for 2 minutes. The final thickness of the stack after baking is ~ 1 μm. Using the EVG aligner (λ = 405 *nm*, P = 36.5 mW/cm^2 and λ = 365 *nm*, P = 19.5 mW/cm^2, exposure time = 0.6 seconds) and the first layer quartz mask, AM are patterned on the substrate. The PR is then developed in MIF 300 developer solution for 2-2.5 minutes and rinsed with DI water thoroughly to remove any developer trace. The

development time depends on the pattern and must be optimized accordingly. The substrate is then loaded into e-beam deposition tool (CHA1) for metal deposition Ti/Pd (1.8 *nm*/48 *nm*) at a base pressure of 4E-6 *Torr*. The lift-off process is then performed in Remover PG solution (40 *°C*) for 5 minutes, followed by Acetone/IPA rinse, each for 2 minutes.

Once the substrate is patterned with AM, CVD graphene is transferred onto it using the PMMA-assisted method, described in chapter 2. Microscope images of the graphene after transferring to the fabrication substrate is shown in Figure 3.1. After removing the PMMA support layer from graphene, the substrate is coated with S1805 resist and baked using the above-mentioned process. Using the EVG aligner and the second layer quartz masks (active area), the photoresist is exposed for 0.8 seconds. The resist development is performed in MF-319 or MIF-726 for 75-90 seconds, followed by a DI water rinse and N_2 blow dry. Using Plasmatherm II graphene is etched from the exposed area (50 *W* for 55 seconds).

In the third layer, source and drain (S/D) contacts are patterned and deposited. Without removing the resist from the second layer, LOR 3B and S1805 resist are spin coated and baked using the steps given for AM patterning. Using the EVG aligner and the third layer mask, S/D are patterned (exposure time: 0.6 seconds, development time: 2-2.5 minutes in MIF-300) and the metal contacts, Ti/Pd (1.8 *nm*/48 *nm*) are deposited in CHA1. A lower base chamber pressure at this stage would results in better quality of the contacts. After metal deposition, the substrate is immersed into Remover PG solution (40 *°C*) for 5 minutes. Agitating the Pyrex container slowly helps the lift-off process be done faster. The substrate is then rinsed with Acetone/IPA thoroughly.

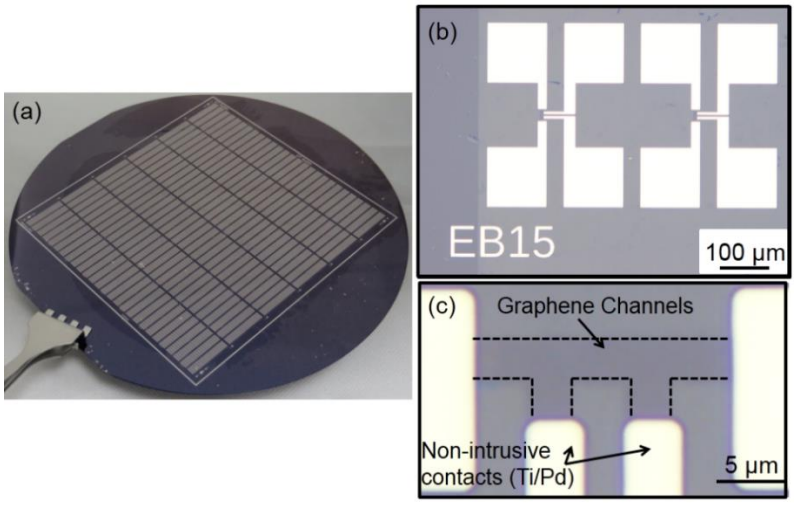

Figure 3.1: (a) 100 *mm* substrate after device fabrication, (b, c) Optical microscope images of four-probe devices under 10X and 100X magnification.

A variety of two and four-probe back-gated GFETs with varying length and width (3, 6 and 9 μm) were fabricated to investigate the electrical characteristics of the graphene channels. An image of the substrate after completing the fabrication process and optical images of a fabricated four-probe device (W=3 μm, L=9 μm) with non-intrusive contact pads is shown in Figure 3.1.

3.3 ELECTRICAL PERFORMANCE

The two- and four-contact GFETs were characterized through DC electrical measurements using a Cascade prober and semiconductor parameter analyzer B1500 at room ambient. In order to statistically characterize the graphene grown on 100 *mm* substrate, 550 GFETs were randomly chosen from five different sections of the substrate and measured through DC characterization method.

3.3.1. Low and high-field DC performance

The low-field DC electrical measurements are done by sweeping the back gate bias in [-30, 30] V range while a constant voltage being applied between the source and drain (100 mV) and the drain current is recorded. Figure 3.3(a) and (b) present the channel resistance and drain current (I_d) of three representative GFETs, with varying width (3, 6 and 9 μm) and uniform length (3 μm), as a function of applied gate voltage at room ambient. The asymmetry between the hole and electron transport, observed mainly for two-probe GFETs at 78-300 K range, most likely originates from pinning of the charge density below the metal contacts,[36] and the higher scattering rates of electrons in the channel by the impurities.[37,38]

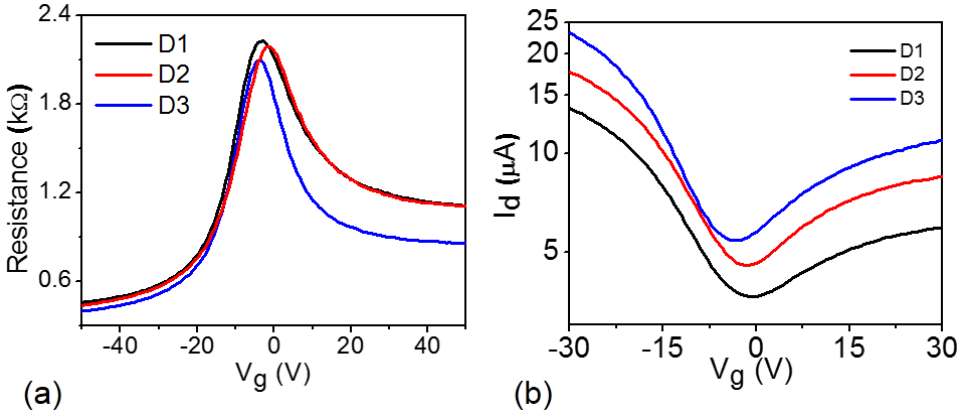

Figure 3.2: (a) Channel resistance vs. gate voltage for three representative two-probe devices, (D1: (W = 3 μm, L = 3 μm), D2: (W = 6 μm, L = 3 μm) and D3: (W = 9 μm, L = 3 μm)) at room ambient and V_d = 100 mV, mobilities are in the 2000-2500 cm^2/Vs range. (b) Drain current of the same devices vs. back gate voltage on a semi-log scale.

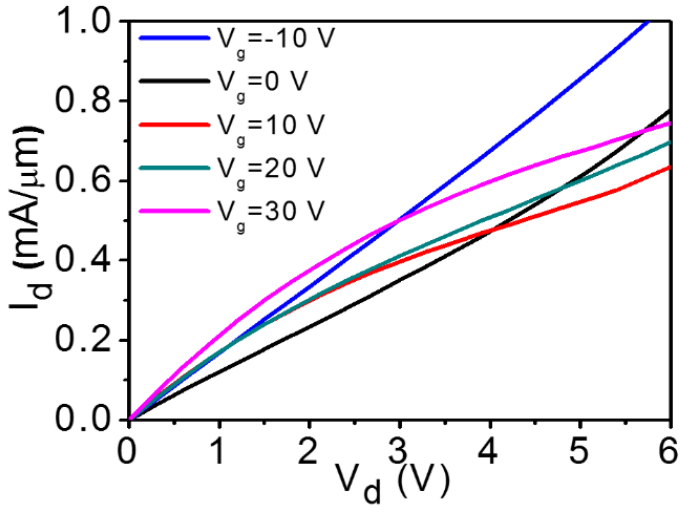

Figure 3.3: I_d-V_d characteristics of a high-mobility device, (W = 6 μm, L = 3 μm), μ = 10600 cm^2/Vs and V_{Dirac} = 0 V, at different back gate voltage showing the intrinsic soft saturation of graphene.

Figure 3.3 presents I_d versus drain voltage (V_d) characteristics of a two-probe GFET (W = 6 μm, L = 3 μm) at different V_g. The soft saturation region, which reflects the ambipolar nature of graphene, was previously reported for exfoliated flakes mainly with top-gated structures.[39-41]

This effect has been observed and reported on the high-mobility inductively heated synthesized CVD graphene on 300 *nm* SiO_2 back-gate dielectric.[42] The current saturation effect is shown to be pronounced in high-mobility GFETs with low contact resistance.[43] The observation of this effect along with the kink effect in our wafer-scale GFETs indicates the high intrinsic quality of the grown graphene.

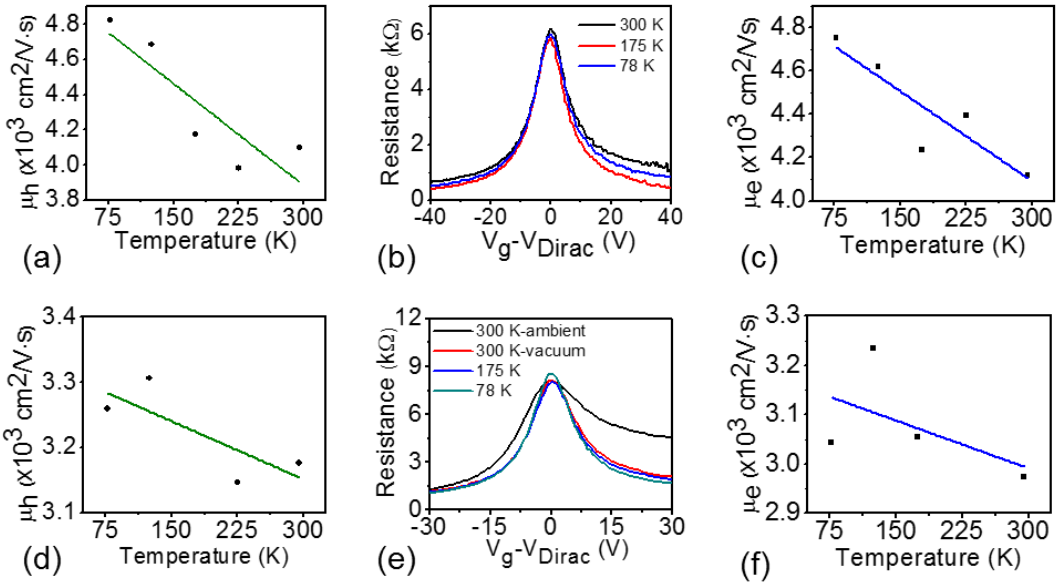

Figure 3.4: Temperature-dependence of (a), (d) hole mobility (μ_h) and (c),(f) electron mobility (μ_e) of two representative four-probe GFETs ($W = 3\ \mu m$, $L = 6\ \mu m$) from 78-300 *K*, (b), (e) Transport curves of these two GFETs from 78-300 *K*.

3.3.2. Temperature-dependent transport

The temperature-dependent mobility of electrons and holes of a representative GFET ($W = 3\ \mu m$, $L = 9\ \mu m$) at 78-300 *K*, is presented in Figures 3.4(a)-(c). The observed mobility increases by ~ 20% when temperature is reduced to 78 *K* suggesting that electron-phonon scattering is a significant scattering mechanism. A second device with lower room-temperature mobility and higher residual carrier density showed weaker dependence (~ 5%) on temperature for the same range (Figure 3.4(d)-(f)). This suppressed temperature-dependence behavior suggests that the dominant scattering mechanism is likely to be charged impurities.[44,45] We observed a more symmetric V-shape transport characteristics from the four-probe GFETs after high vacuum (10^{-6} *Torr*) pumping for several hours (Figure 3.4(e)) resulting in the desorption of moisture and volatile adsorbates.[46]

3.3.3. Analogue electrical response

Given the high average carrier mobility and demonstrated current saturation at room ambient, the wafer-scale high-performance GFETs are suitable for analog applications such as amplifiers and non-linear high-frequency devices.[47-49] A triple-mode single-transistor amplifier is demonstrated based on the wafer-scale back-gated GFETs. Examples of a frequency doubler and non-inverting and inverting common-source amplifiers are presented in Figures 3.5 along with a schematic of the circuit in Figure 3.6. The supply voltage, V_{DD} was set to 500 mV for low-power operation with load impedance of 1 $M\Omega$. V_g is the combination of a fixed DC voltage and a small sinusoidal AC signal provided by a function generator. The input frequency which is limited by the measurement setup was 12 kHz. The gate bias of the GFET was adjusted to be in the hole or electron branch or ambipolar point for non-inverting or inverting common-source amplifiers or frequency amplification respectively (Figure 3.5(a)). Here a 6.5X voltage gain for hole branch (Figure 3.5(b)), with the expected non-inverting amplifier response, and a 3X gain for electron branch (Figure 3.5(d)), between the output (at the drain) and input (at the gate), is demonstrated. The mismatch in the gain of electron and hole branch is possibly due to the asymmetry of the transport characteristics of the device at room ambient. Once the device was biased at the minimum conduction point, the input signal sees a positive gain in its positive phase and a negative gain in its negative phase, resulting in frequency doubling. Figure 3.5(c) demonstrates the frequency doubling with an input signal of 12 kHz and output signal of 24 kHz.

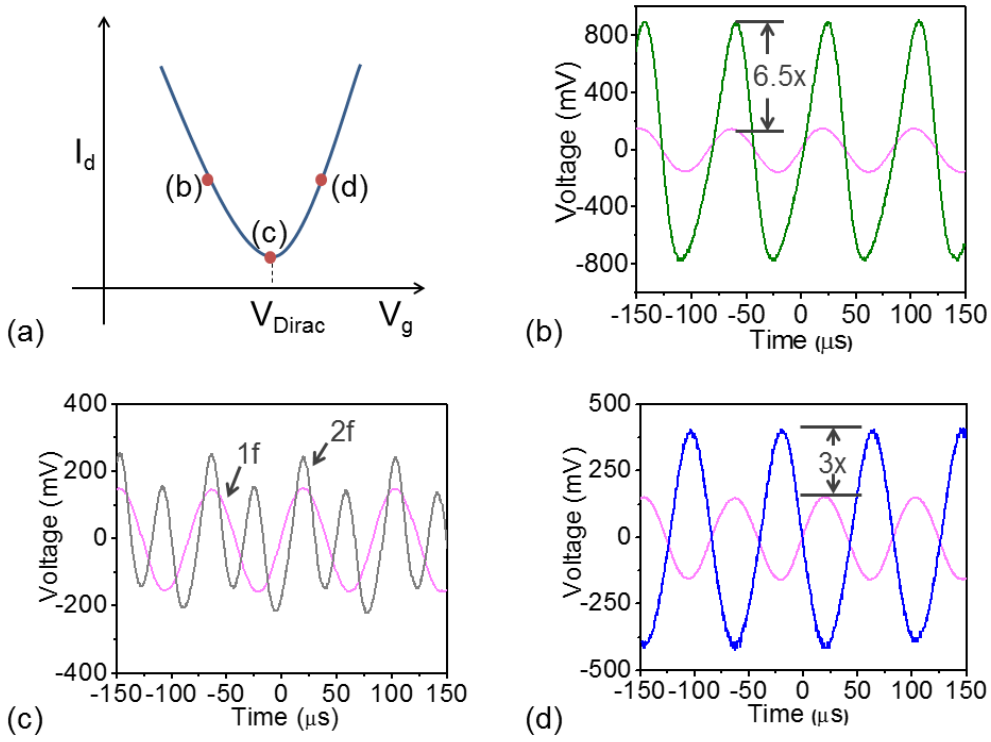

Figure 3.5: (a) Schematic of I_d-V_g curve showing the corresponding applied gate bias for (b) non-inverting amplification, (c) frequency doubler and (d) inverting amplification. The pink curve represents the input signal.

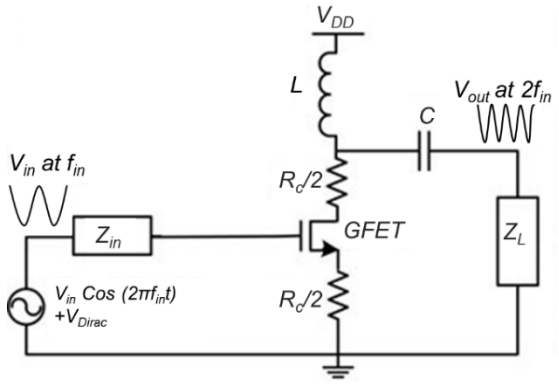

Figure 3.6: Schematic of the circuit used for analogue measurements of GFETs.

3.4. ELECTRICAL PERFORMANCE STATISTICS

3.4.1. Device yield

The DC Electrical performance was measured at room temperature. Due to the long time required for performing the field-effect modulation by sweeping the back gate bias in [-30, 30] *V* range on every fabricated GFET, a statistical study was carried out on 550 randomly chosen GFET across the wafer. A device yield of 74% is achieved comparable to the 70-80% yield of early (1960s) silicon wafer-scale device development.[50]

The margin of error on the device yield, which is an important factor when the number of measured samples is smaller than the total population of interest, and is known as the confidence interval (c), can be calculated using equation 3.1: [51]

$$c^2 = \frac{Z^2 p(1-p)}{ss} \tag{3.1}$$

where *ss* is the measured sample size, *p* is the percentage of picking a choice and *Z* is 1.96 for 95% confidence level. When the sample size is smaller than the total population, *ss* is adjusted by equation 3.2:

$$ss' = \frac{ss}{1+\frac{ss-1}{pop}} \tag{3.2}$$

where *ss'* and pop are the new sample size to be used in equation 3.1 and the total population of interest respectively. In our calculations, *p*, *ss'* and pop are 0.74, 538 and 26000 respectively. Using equation 3.2, *'c'* can be calculated to be 0.037 or 3.7%. The low value of confidence interval indicates that if all devices had been tested, the device yield would be in the range of (74 ± 3.7)% with 95% probability. The device yield is 20% higher yield than reported prior work.[13]

3.4.2. Device Performance Metrics

The distribution of the field-effect mobility, Dirac voltage (V_{Dirac}), contact resistance ($R_{contact}$) and sheet resistance (R_{sheet}) under ambient condition, in the form of cumulative probability plots, are presented in Figure 3.7(a)-(d). The average value of the field-effect mobility, which is extracted using a widely-accepted diffusive transport model,[52] is observed to be 2113 cm^2/Vs and most notably the mobility of 5% of GFETs is above 10,000 cm^2/Vs, 5X higher than prior result over the same range.[13] These values of mobility are comparable to the mobility values extracted from high-quality small-scale polycrystalline CVD graphene samples,[53,54] and epitaxially-grown graphene on wafer-scale single crystalline substrate.[9,22] The high values of mobility at room temperature here is comparable to the best Si-MOSFETs mobility reported at low-temperature. In addition, as we discussed before the graphene mobility is relatively temperature-independent, making room temperature 2D graphene mobility to be among the highest in field-effect transistor devices. The high percentage of devices with μ > 10,000 cm^2/Vs achieved here is a further evidence of the previous reports that high carrier mobility mainly correlates with graphene domain structures generated during the synthesis process and impurity concentration rather than graphene domain size.[55-58]

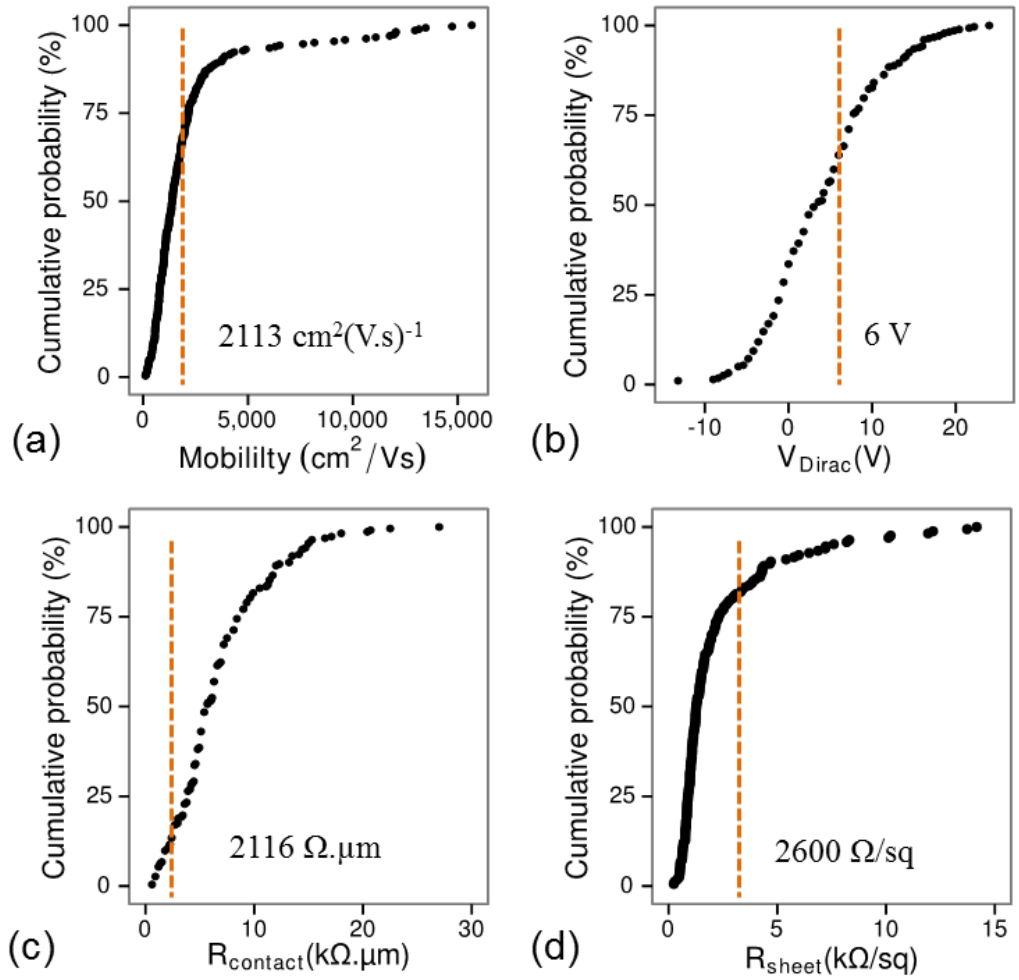

Figure 3.7: Cumulative plots of (a) field-effect mobility (mean: 2113 cm^2/Vs), (b) V_{Dirac} (mean: 6.2 V), (c) $R_{contact}$ (mean: 2116 $\Omega.\mu m$) and (d) R_{sheet} (mean: 2600 Ω/sq). The device arrays have dimensions in the micrometer range and all measurements are performed under ambient conditions.

The statistical 5-95% mobility and $R_{contact}$ distribution at five different locations of 100 *mm* wafer is presented in Figure 3.8(a) and (b). The comparison between Figure 3.8(a) and (b) suggests that regions with lower average $R_{contact}$ show higher average mobility values. Considering the Raman spot scans, after the transfer (Figure 2.11), the variation of mobility and $R_{contact}$ distribution at different locations on the wafer after fabrication process, is believed to be mainly due to the resist residue rather than initial differences in the quality of grapheme.[59] The high value of average mobility, achieved here, is a promising indicator that the likely success of ongoing integration research in addressing the sources of electrical variability, coming from the residue of the transfer and fabrication process, will result in uniformly high-performance graphene devices at wafer-scale. It is also worth noting here that the dimensions of the largest channels ($3\ \mu m \times 9\ \mu m$) are smaller than the average domain size of the synthesized film ($\geq 10\ \mu m$) obtained by our growth process. We expect that, with similar likelihood, the transistor channels traverse graphene domain boundaries or are contained within a single graphene domain.

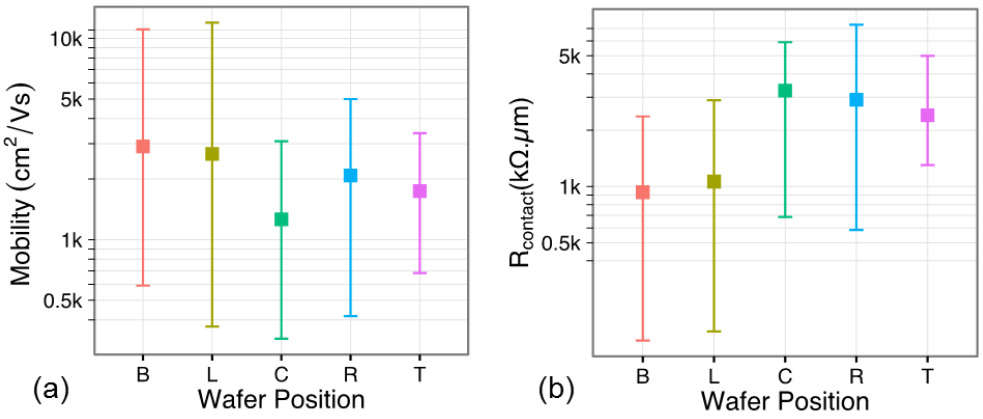

Figure 3.8: 5–95% distributions of (a) mobility and (b) $R_{contact}$ at five locations on 100 *mm* wafer. The variation is mostly due to non-uniform transfer process and resist residue.

The Dirac voltage, presented in Figure 3.7(b), is narrowly distributed around 0 ± 10 *V* and shows an average value of 6.2 *V*. The positive and negative shifts of V_{Dirac} around 0 *V* is indicative of the slight p and n-doped channels which is believed to be caused by the net effect of moisture adsorption and photoresist impurities from the fabrication process, [35,37,38] and the doping from SiO_2 substrate.[60] The contact resistance, obtained by fitting the channel resistance versus the gate voltage, has an average value of 2116 $\Omega.\mu m$, comparable to the reported Pd-based graphene-metal contacts fabricated by electron-beam (e-beam) lithography,[61-63] suggesting that the performance of the graphene/metal contact does not change drastically when the low-throughput e-beam lithography method is replaced by the CMOS-compatible UV photolithography at wafer-scale. The sheet resistance, measured at floating back-gate potential, has an average value of 2600 Ω/sq comparable to 1-2 $k\Omega/sq$

reported for the chip-scale CVD graphene devices,[64] and ~ 3000 *Ω/sq* reported for the wafer-scale single crystalline graphene.[9]

3.5. PERFORMANCE BENCHMARKING

In Table 3.1 we compare the peak mobility (μ_{max}) at T=300 K and the impurity density (n) obtained here with other wafer scale poly- and single crystalline CVD and epitaxially-grown graphene reported previously. The impurity density could reside either inside the substrate or be created near the graphene-substrate interface during the fabrication process. The impurity density listed in Table 3.1 for Kim et al.,[22] Lee et al.,[9] and Heo et al.[13] are exact reported values and the listed values for Lee et al.,[8] and Tao et al.[31] and are extracted through equation 3.3:

$$n \cong C_{ox}\left|V_g - V_{Dirac}\right|/e, \tag{3.3}$$

for nonzero V_{Dirac}, where V_g and e are the gate bias and the electron charge, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ is the gate capacitance per area and ε_{ox} and t_{ox} are the gate dielectric and thickness respectively.[39] The impurity density of measured devices here that falls in the range of (3.4-29) × 10^{11} cm^{-2}, is extracted through a diffusive transport model and indicates the relatively low concentration of impurities in the synthesized graphene. Using the extracted value for impurity density and a simple analytical equation (3.4) the maximum value for linear tail mobility of graphene for each report can be derived:

$$\frac{\mu}{\mu_0} \approx 50\ \frac{n_0}{n_{imp}}, \tag{3.4}$$

Where $\mu_0 = 1\ m^2/Vs$ and $n_0 = 10^{10}\ cm^{-2}$.[58] Note that based on equation (3.4), for a specific gate dielectric, the low-field mobility depends on charge impurity scattering concentration, lower impurity values results in higher carrier mobility, and to improve carrier mobility is to improve graphene quality. The value of μ_{max} here is one of the highest reported values for polycrystalline graphene so far and is ~ 40% higher than the best value reported for single crystalline graphene. Note that except the data reported in this work, Lee et al.[9], Heo et al.[13] and Lee et al.[8] , the rest of the reported values in Table 3.1 are based on a limited number of measurements performed on devices fabricated using e-beam lithography.

Table 3.1 Comparison of carrier mobility, ion contamination impurity between the current study and previously reported wafer-scale graphene.

Substrate size (*mm*)	μ_{max} (cm^2/Vs)	n ($\times 10^{11}\ cm^{-2}$)	Reference
Cu film/ 100-300	**15660**	**3.4 - 29**	**Rahimi, 2014** [32, 65]
Ge(110)†/ 100	10600	3**	Lee, 2014 [9]
SiC†/ 100	2700	10 - 100	Kim, 2013 [22]
Cu film/ 100	4900	10**	Tao, 2012 [31]
Cu film/ 150	23000*	10 - 40	Heo, 2011 [13]
Ni/Cu films/ 75	3000	28**	Lee, 2010 [8]

† Single-crystalline substrates.

* Only 3% of measured devices showed $\mu > 3{,}000\ cm^2/Vs$.

** Data is based on single device report.

3.6. SUMMARY

In summary, we have demonstrated the statistical electrical performance of CVD polycrystalline graphene on 100 *mm* substrates. The device performance is benchmarked against that of previous wafer-scale polycrystalline graphene and reports on CVD single-crystalline graphene on Hydrogen-terminated germanium substrates and epitaxial-grown graphene on SiC substrates. The successful integration of CVD graphene on wafer scale is achieved by not only enhancing the performance of individual graphene devices but also uniform performance across many devices. Our CMOS-compatible device fabrication process achieved the yield of 74% with charge mobility, contact resistance and sheet resistance superior to existing reports on the wafer-scale GFETs. The observation of soft saturation effect and demonstration of frequency doubler and analog amplifiers based on wafer-scale graphene make GFETs suitable for analog and high frequency circuit applications.

In order to preserve the outstanding device performance, passivation methods such as the one reported before,[66,67] must be developed to reduce the device exposure to the ambient and moisture which could potentially degrade the device performance.

Chapter 4 : Dry Mechanical Delamination for Bonding Graphene onto Si Substrate

4.1. INTRODUCTION

The combination of graphene with Si technology is widely considered among the greatest prospects for adopting graphene discoveries in research laboratories into practical electronic applications. However, the high temperature growth of graphene monolayers is not compatible with Si processing. For this reason, the controlled transfer of graphene from the growth surface onto the target substrate is crucial for developing graphene nanotechnology. The transfer of graphene remains a substantial hurdle and no facile process has emerged that can enable automated transfer integration with rigid Si substrates.

Despite the intensive research that has been conducted in the past few years on wafer-scale growth of graphene, there is no general and robust approach for transferring large-area graphene onto Si surface. The existing transfer methods, often developed for specific applications and not suited for integration with rigid wafer-scale Si, suffer from drawbacks such as the long process time and the use of reactive chemicals for etching the growth substrate and therefore unwanted contamination and film wrinkling.

In this chapter, we demonstrate an etch-free, low-temperature and scalable direct delamination of graphene from copper films onto Si substrate with significantly minimal metal contamination on the transferred films. This process is developed based on fracture mechanics concepts and the direct measurements of the interface adhesion energy between the CVD graphene, its growth surface and the Si substrate. The copper ion contamination on graphene obtained by the direct delamination method is measured by secondary ion mass spectroscopy (SIMS) and is compared to two other major transfer techniques.

4.2. MECHANICAL DELAMINATION

As in exfoliation, an intermediate carrier film is required for the future bonding technique developed for graphene (epoxy in Figure 4.1). The adhesive interaction between the carrier film and CVD graphene depends on the contact and environmental factors and can be assumed to be van der Waals in nature. This is supposedly weaker than the interaction between the graphene and the seed metal catalyst used for growing graphene.[68] Given that, there are two interfaces that are of great interest for transferring CVD graphene to the fabrication substrate; i. copper and SiO_2 interface and ii. Graphene and copper substrate. In the former option graphene/copper stack are separated from the growth substrate and in the latter option graphene is separated from the copper seed layer. In this chapter, the results of both cases will be presented and discussed.

4.3. KEY SETUP PARAMETERS

The mechanical delamination process starts by covering the CVD graphene grown on copper film with a 3-30 μm thick carefully chosen epoxy (EP30, MASTERBOND), Figure 4.1(a) and (b). Experiments with other bonding agents such as polyimide (PI-2574, HD Microsystems) and SU-8 resulted in poor adhesion between graphene and the bonding agent. Another reason for choosing the EP30 as the bonding agent is its transparency to Raman spectroscopy which as will be discussed later, is important for evaluating delaminated graphene on the epoxy through Raman spectroscopy.

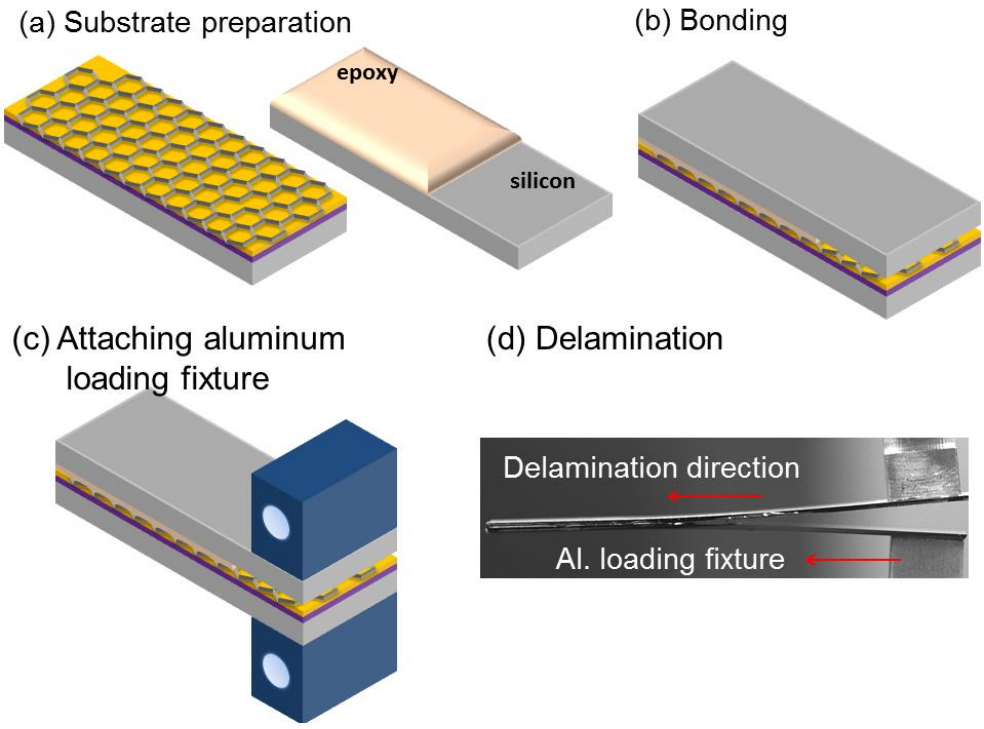

Figure 4.1: Schematic of dry delamination of CVD graphene from Cu seed film, (a) target substrate is coated with epoxy and (b) bonded to the graphene growth substrate, (c) aluminum loading fixtures are attached to the top and bottom substrates and (d) image of the delamination process.

The epoxy resin and hardener were mixed in a four to one ratio by weight. The air bubbles created during the mixing process are removed by placing the mixture in a vacuum desiccator for 10 minutes. The epoxy is then applied to surface of a bare Si (100) strip (1×4 cm^2). The graphene substrate and Si strip are then placed in contact with the epoxy-coated graphene. The stack is then cured at 100 ^oC for 2 hours. Finally two aluminum loading tabs are bonded to the top and bottom Si strips (Figure 4.1(c)). By fixing one of the tabs and applying a normal force with specified loading rate to the other tab, delamination can occur along any of the interfaces present in the stack. The interfaces of interest here are

copper/SiO_2 (Figure 4.2(i)) and graphene/copper (Figure 4.2(ii)). The separation of graphene from copper interface is more challenging than copper/graphene stack from the SiO_2 due to the mechanical mode mixity caused by the surface roughness of copper seed layer. It was discussed in chapter 2 that the rms roughness of as deposited copper seed layer is < 5 *nm*. During the high temperature annealing process, the roughness of the seed copper layer increases to >50 *nm*. The CVD graphene follows the copper surface morphology during the growth step and the low-viscosity epoxy follows the surface roughness of copper/graphene stack. The separation interface is controlled by tuning the loading rate of the top beam and the thickness of the epoxy film. In contrast to the delamination along graphene/copper interface, which results in graphene-only transfer to the epoxy, an extra step of etching copper after delamination along copper/SiO_2 interface is required for getting access to the transferred graphene. This step can be done in ammonium persulfate (APS-100) solution followed by DI water rinse.

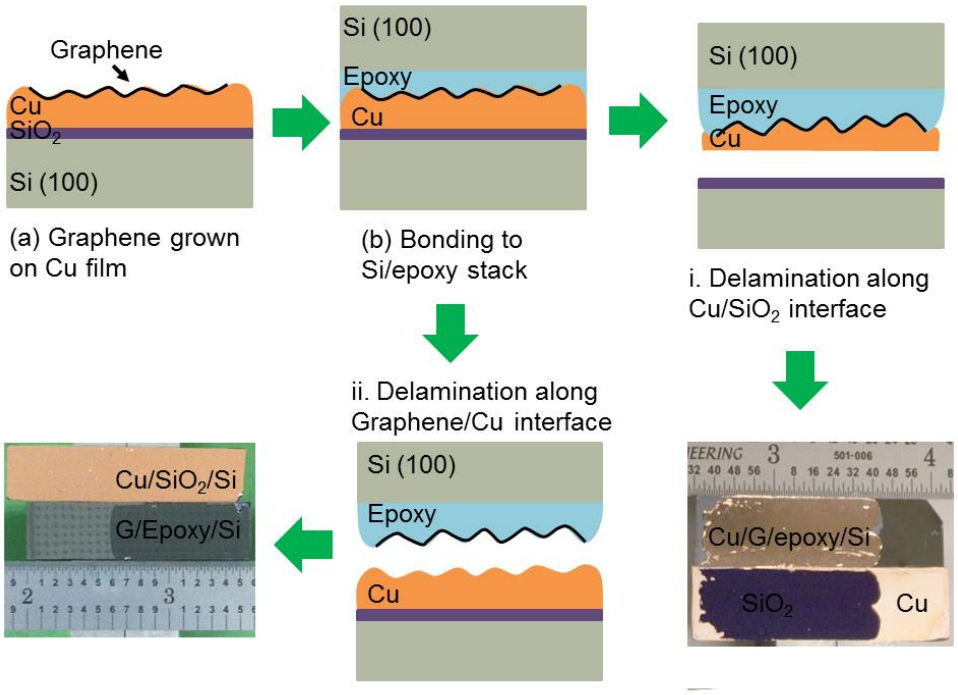

Figure 4.2. Schematic of the mechanical delamination scenarios: the interfaces of interests are (i) copper/SiO_2 and (ii) graphene/copper.

4.4. SURFACE CHARACTERIZATION OF MECHANICALLY-DELAMINATED GRAPHENE

4.4.1 Arbitrary transfer of graphene

The surface of the delaminated graphene samples were characterized using different methods. Figure 4.3(a) and (b) show the SEM imaging of the copper film and epoxy substrates after delamination. The border of graphene delaminated area on the copper film is clearly shown in Figure 4.3(a). This suggests that, using mechanical exfoliation, arbitrary areas of graphene can be transferred to a secondary substrate. Figure 4.3(b) shows a quite uniform transfer of the graphene on the epoxy with minimal defects.

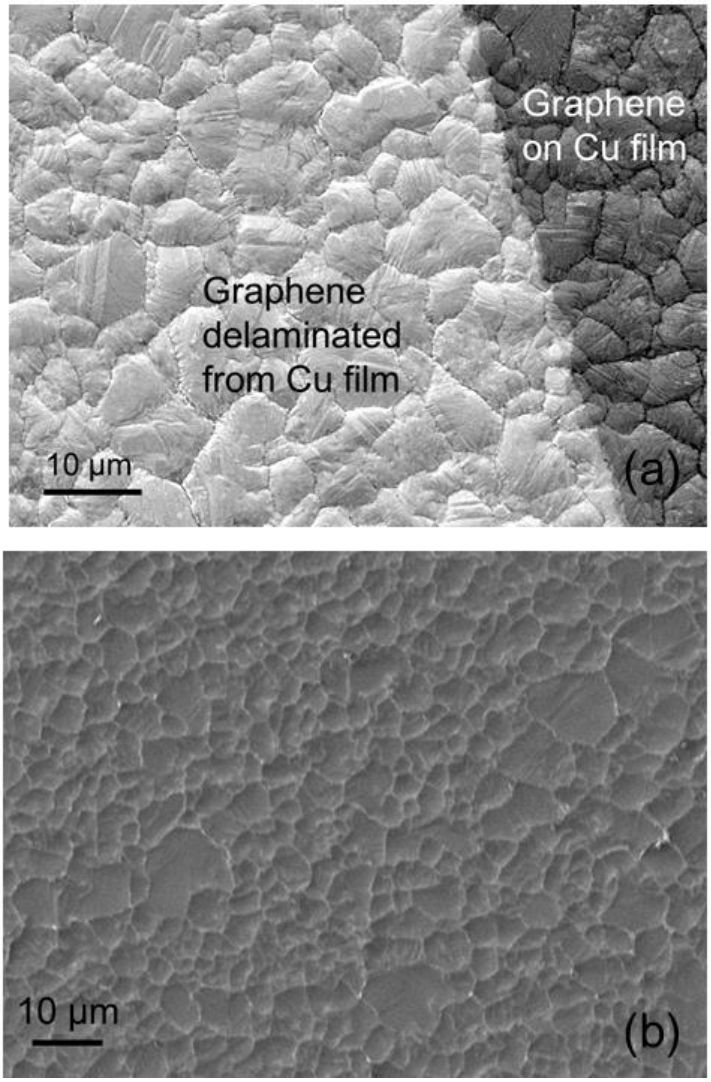

Figure 4.3. (a) SEM image of the copper seed layer after delamination shows the regions with and without graphene, (b) SEM image of the epoxy surface after the delamination shows graphene fully transferred to epoxy.

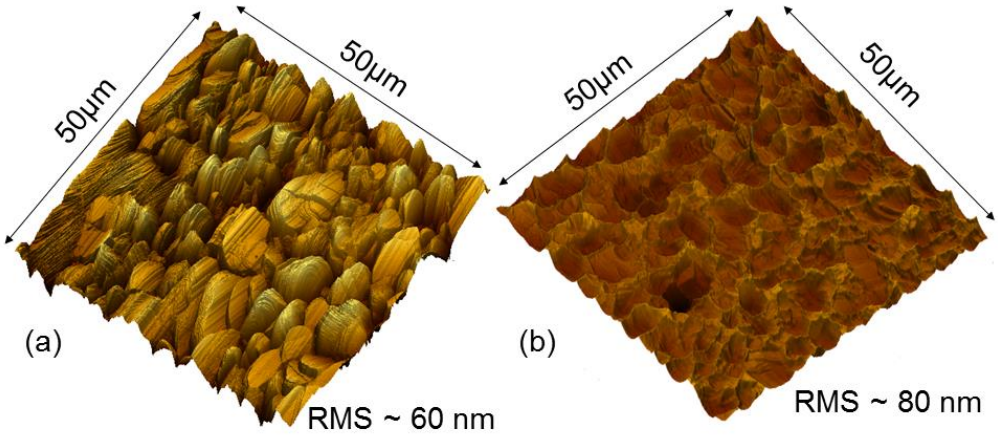

Figure 4.4. (a) AFM imaging on the copper/graphene surface reveals an rms roughness of ~ 60 *nm*, (b) AFM imaging on the epoxy/graphene surface after the graphene exfoliation shows an rms roughness of ~80 *nm*. Both images are taken on an area of 50 μm × 50 μm.

4.4.2. AFM imaging of the epoxy surface

Since the epoxy copies the copper film surface, the rms roughness of the epoxy after the graphene transfer is expected to be the same as the rms roughness of the copper film after the graphene growth (Figure 4.4). The high film roughness after transfer can potentially cause challenges for device fabrication which will be discussed later. To address this challenge, new methods should be developed for restricting the roughness of copper after CVD growth of graphene.

4.4.3. Raman Metrology

To provide further details of the graphene transfer to the epoxy surface after the delamination process, the epoxy surface was scanned using Raman spectroscopy method.

Using a 488 *nm* wavelength laser, Raman spot scans were taken from Si/spoxy (Figure 4.5(a)) and Si/epoxy/graphene (Figure 4.5(b)) surfaces. The epoxy shows a strong background and multiple peaks around and close to the graphene Raman peaks at 1605 cm^{-1} and 2870 cm^{-1}.

Despite this close proximity, the Raman spectroscopy on Si/epoxy/graphene transfer clearly shows the 2D and G peaks of graphene. In order to calculate the $I_{2D}:I_G$ of graphene transferred to the epoxy, the Raman spectrum of graphene on epoxy is deconvoluted (Figure 4.5 (c)). For this purpose, the Raman spectrum of the bare epoxy is fitted to Gaussian functions. In the next step, these Gaussian functions are subtracted from the Raman spectrum of graphene on epoxy. This process leads to the relative intensity ratio of 2D and G peaks of 2.7. This value is closed to $I_{2D}:I_G$ before transferring the graphene. To avoid this strong Raman background, the epoxy can be replaced by another bonding agent for the future research. Nevertheless, Raman spectroscopy still can be used as a powerful method for detecting the graphene on the epoxy substrate.

Figure 4.6 shows the results of Raman mapping of G and 2D peaks of graphene on the surface of the Si/epoxy/graphene. The laser wavelength used for the mapping is 488 *nm* with a focal point size of 1 μm and step size of 2 μm. The intensity of the graphene's G and 2D peaks on the epoxy are provided in arbitrary units in agreement with the Raman spot scans. The $I_{2D}:I_G$ is also provided and is in agreement with the data of the Raman spot scans. The Raman maps data conforms that large-area graphene is uniformly transferred to the epoxy substrate through the mechanical delamination technique.

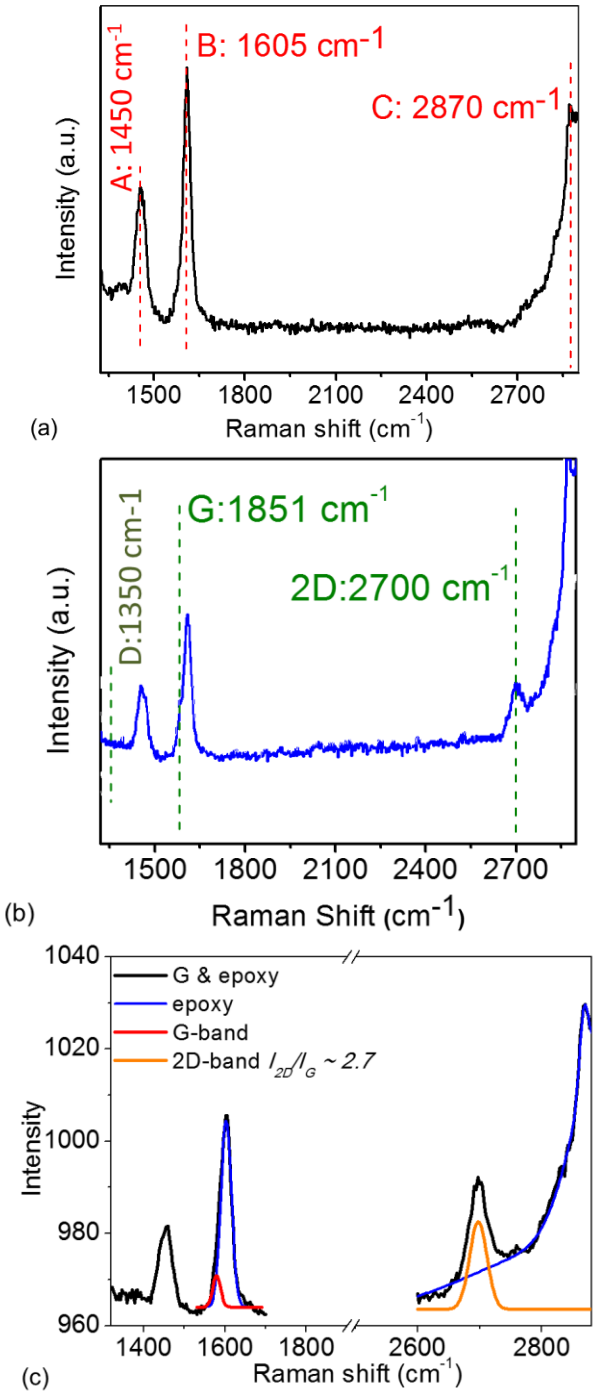

Figure 4.5. (a) Raman spectra of the bare epoxy and (b) graphene on epoxy. (c) De-convoluted Raman spectrum of graphene on epoxy exhibit an $I_{2D}/I_G \sim 2.7$.

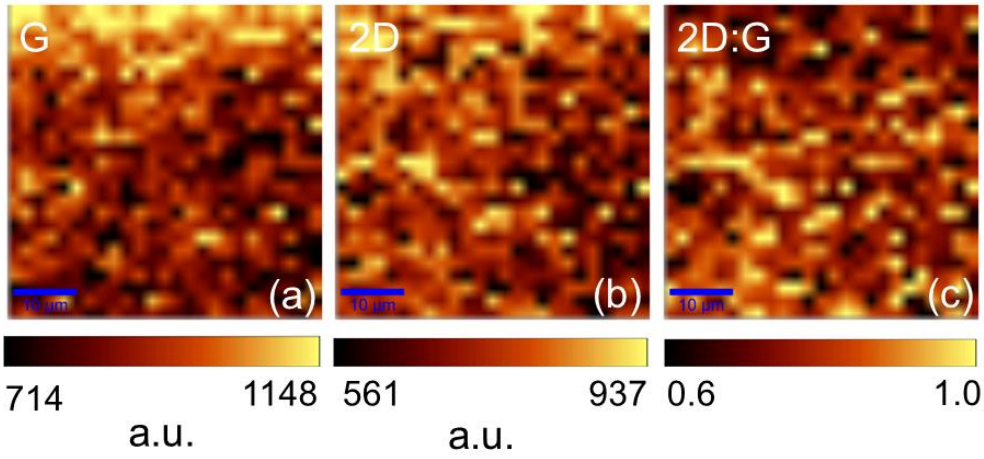

Figure 4.6: Raman mapping data on epoxy/graphene surface shows G and 2D peaks of graphene.

4.5. DEVICE FABRICATION STEPS

Measurements of the electrical sheet resistance is one of the way of characterizing the electrical properties of the graphene, mechanically exfoliated on the epoxy. The two different types of samples were processed with mechanical delamination in i. graphene/copper interface and ii. copper/SiO_2 interface. In the latter case, graphene was exposed by etching the copper by APS-100. The samples were rinsed with DI water for at least five times and dried with a N_2 gas gun afterwards.

In order to measure the sheet resistance, four-probe devices were fabricated on the Si/epoxy/graphene substrates using e-beam lithography. For the patterning purposes, 495 PMMA A4 was utilized (spin rate 2000 rpm for 60 seconds). Due to the low-thermal budget of the epoxy, instead of baking the PMMA after spin coating, it was left inside a vacuum desiccator overnight for the solvent to evaporate and leave a solid PMMA film (200 *nm* thick). In the next step, E-beam lithography (Jeol-JX60) was used for patterning the

alignment marks and source/drain contacts (dose: -5% of 500 C/cm^2). The e-beam evaporation method was used for deposing Ti/Au (5 *nm*/50 *nm*). A thick Ti layer was used to improve the adhesion between metal and graphene. The lift-off process was done in an acetone solution at 50 *°C*. In the second step, 495 PMMA A4 was spin coated on the sample and left to dry overnight. Using the same exposure conditions, the channels of four-probe structures (3 μm × 9 μm and *5* μm × 15 μm) were isolated.

To fabricate top-gate two-probe structures, the same steps were used for patterning the source/drain contacts and isolating the channels. The top gate was formed by spin coating the samples with 495 PMMA A4 and letting it to dry up overnight, followed by e-beam pattering of the top gate. Using e-beam deposition method, the top gate stack (30 *nm* Al_2O_3 or 40 *nm* SiO_2 / 5 *nm* Ti/ 45 *nm* Au) was then deposited at a base pressure of 2E-6 *torr*. The lift-off was then done in Acetone (45 *°C*). Using this method, two probe devices with varying channel width and length of 2, 3 and 5 μm were fabricated on the graphene transferred to the epoxy. Figure 4.7 shows the schematic of the fabrication steps for making four-probe and top gate devices.

Due to the high surface roughness of the graphene, the top-gated devices exhibited a huge leakage current through the gate dielectric. To resolve this issue, new methods need to be developed for reducing the growth temperature and as a result the surface roughness of copper during graphene growth.

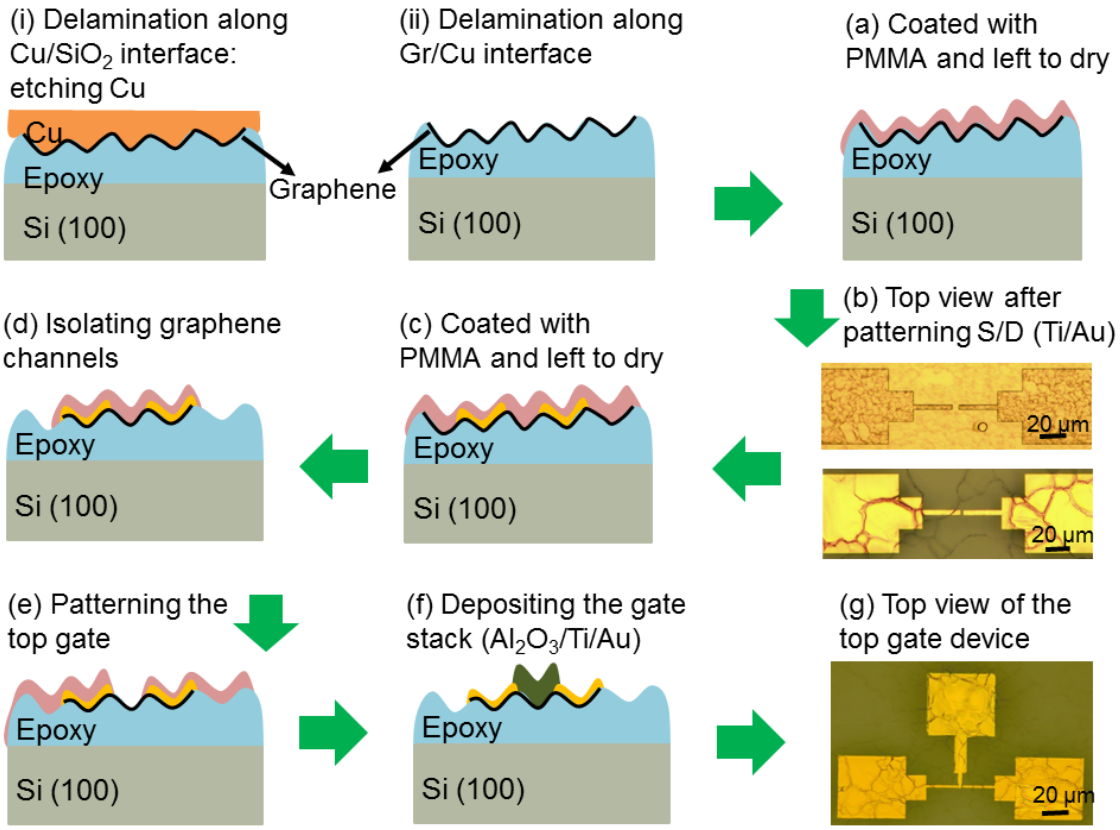

Figure 4.7: Schematic showing the device fabrication flow on Si/epoxy/graphene substrate (i), (ii) shows the delamination along Cu/SiO_2 and graphene/Cu interfaces, after etching the Cu film on case (i), both type of samples follow the same device fabrication steps. Four-probe devices used for sheet resistance measurements are fabricated using the same steps and by skipping the last step of patterning and depositing the top gate stack.

One challenge with fabricating devices on the epoxy/graphene surface is the large rms roughness of the graphene on epoxy. This surface roughness reduces the adhesion between metal and graphene and the fabrication yield especially during the lift-off process. The low adhesion between the delaminated graphene and the metal contacts results in peeling off the contact pads during lift-off process in the warm acetone. In order to improve

the device fabrication yield, future steps must be taken in growing graphene in order to increase the copper grain size and reduce its surface roughness.

4.6. SHEET RESISTANCE OF DELAMINATED GRAPHENE

Using the four probe devices, fabricated on epoxy/graphene stack, the sheet resistance of graphene was measured. The results were compared to the sheet resistance obtained from the 100 *mm* wafer transferred through PMMA-assisted technique and electrochemical delamination of graphene onto flexible substrates reported elsewhere,[17] is shown in Figure 4.8.

The average value of the sheet resistance of the graphene transferred by a wet transfer method is ~30% lower than the mechanically delaminated samples. The larger variation along the average R_{sheet} value reveals the low uniformity of the wet transferred film.

On the other hand, the two mechanically delaminated samples show a much smaller variation around the average values which suggest more uniform characteristics of the transferred films. The reason for higher average sheet resistance values of the mechanical transfer is likely the large roughness of the transferred film compared to the PMMA wet transfer method. The roughness coming mainly from the polycrystalline structure of the Cu film, can be avoided by growing graphene on single crystalline substrates.[9]

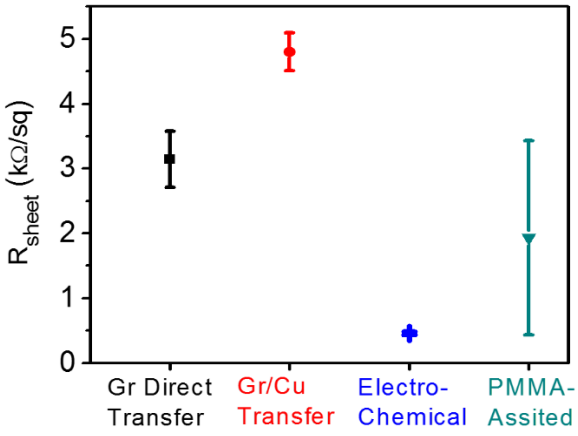

Figure 4.8. Sheet resistance distribution of the wafer-scale PMMA-assisted transferred graphene and electrochemical delamination on flexible substarte,[17] compared with transfer through the delamination techniques along graphene/Cu and Cu/SiO_2 interfaces.

4.7. METAL CONTAMINATION CAUSED BY THE GRAPHENE TRANSFER PROCESS

The adhesive interaction between the CVD graphene and PMMA or copper film is likely to be van der Waals in nature. The strongest of these interaction is supposedly between graphene and the growth catalyst seed layer. This strong adhesion could result in unwanted contamination and doping of the graphene by the metal catalyst after the transfer to the target substrate.[69] So far, a large amount of research has been reported on polymer residue on graphene after transfer and how it might impact the electrical device performance.[70] One of the challenges of integrating graphene with Si platform is to make sure CVD graphene complies with stringent purity standards of Si industry. However, CVD graphene is prone to the metallic contamination during the growth process on metallic substrates and the substrate etching in aqueous metal etchants for the transfer to the target substrate. Measurements of the metal contamination can shed light on the reasons of the

variation of electronic transport properties and device performance.[71] It is a well-known fact in the case of Si that metallic impurities even at low concentration (10^{10}-10^{11} cm^{-2}) can deteriorate the performance of electronic devices severely.[72,73]

Copper contamination on the transferred graphene was evaluated with time-of-flight secondary ion mass spectroscopy (TOF-SIMS). The TOF-SIMS enables very high depth resolution ideal for thin films (and thus 2D materials) and also parts-per-billion (ppb) sensitivity. The samples were analyzed with a commercial ION-TOF TOF.SIMS 5 instrument configured with a 30 keV Bi^+ analysis ion beam and 1 keV O_2^+ sputtering ion beam. The analysis beam was operated in the high current (HC) bunched mode (100 ns pulse duration) for high sensitivity. The sputter beam was rastered over 350 μm × 350 μm and the analysis beam over 200 μm × 200 μm to eliminate crater-edge effects in the collected ions. Positive secondary ions were collected in the analyzer column giving mass resolution better than 5000 ($m/\delta m$) for all masses. An electron gun was used to compensate for any charge accumulation in the sample. The instrument main chamber was pumped down to below 10^{-8} $Torr$ during analysis.

The Cu+ secondary ions collected represent the Cu impurities on the graphene films. By collecting a profile from a reference Cu thin film (e-beam deposited, the same film used as the substrate for CVD graphene growth), we obtain a reference intensity of Cu+ counts with a known concentration which can then be compared with the transferred graphene films which have trace Cu contamination by the external reference standard method.[74] This method gives the concentration of the analyzed sample (c_A) with respect to the reference sample (c_R) by the simple relation:

$$\frac{I_A}{I_R} = \frac{C_A}{C_R} \tag{4.1}$$

where I_A is the intensity of secondary ion signal of the analyzed sample and I_R is the secondary ion signal of the reference sample, and that the signal is from the same ion species (Cu+ in this case). Here, we make the assumption that the Cu reference surface is the (111) surface, as it is energetically favorable and the closest packed configuration for Cu (thus calculations give a maximum Cu contaminant concentration).[75] Given the Cu+ depth profiles, the Cu+ secondary ion signal intensity corresponding to the graphene layer can be fit at the precise depth because that depth corresponds to the maximum C+ secondary ion signal intensity.[76,77] The Cu (111) surface gives c_R of 2.21×10^{15} *at/cm*^{2} and I_R of 3.4×10^4 counts.

The mapping results are shown in Figure 4.9(a)-(d). The surface copper concentration on graphene transferred with PMMA stamp method (Figure 4.9(b)) is ~two orders of magnitude larger than the copper concentration on the reference bare SiO_2 substrate (Figure 4.9(a)). On the other hand, the copper contamination on the graphene directly delaminated from copper substrate (Figure 4.9(c)) is ~three orders of magnitude smaller than reference and copper concentration remained on graphene after etching copper from copper/SiO_2 delamination is an order of magnitude smaller than the reference SiO_2. The reason is likely due to the fact that with the PMMA transfer method, copper has to be etched from the bottom surface of the graphene which eventually will be in contact with the final substrate that is used for scooping it out of the solution. As a result, one cannot avoid trapping copper ions between the graphene and substrate.

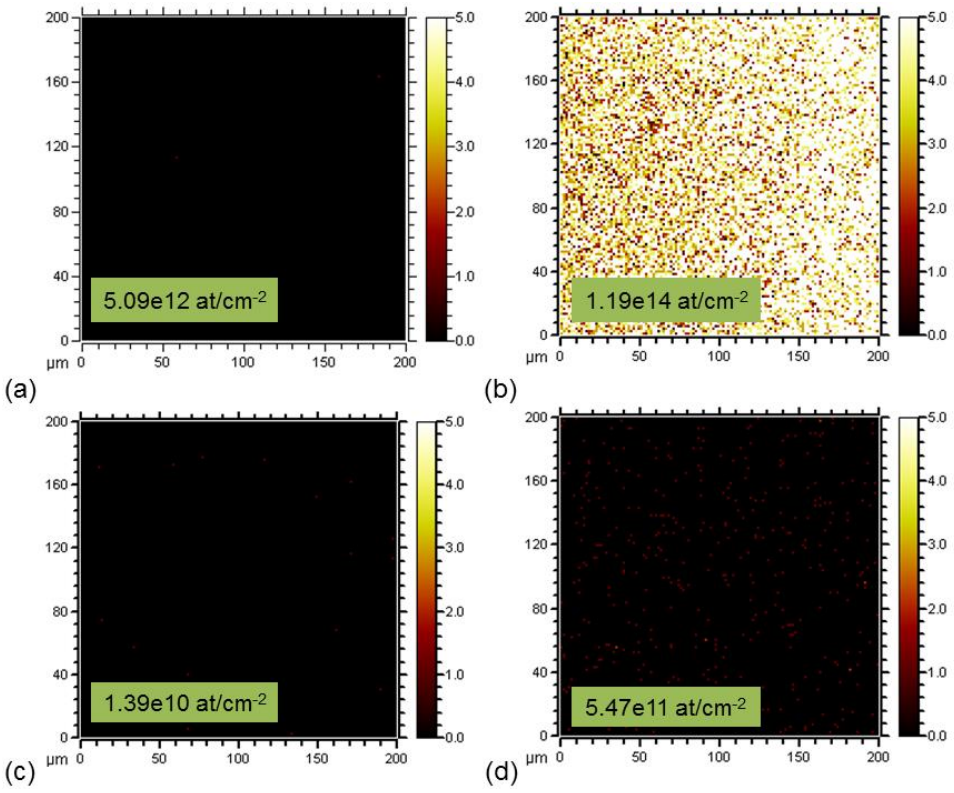

Figure 4.9: TOF SIMS maps show the copper contamination levels of (a) SiO_2 reference sample, (b) graphene transferred by PMMA stamp method, (c) mechanical delamination of graphene from copper seed layer and (d) mechanical delamination of copper from SiO_2 substrate.

However in direct delamination of copper from SiO_2 substrate, the copper is etched from the top face of graphene which will be rinsed with DI water several times later on. This will reduce the copper concentration on the surface.

4.8. SUMMARY

Large-scale device application of graphene is not possible without addressing the question of integrating graphene to Si substrate. We addressed this question by developing

a permanent bonding technique between graphene and the final device substrate. The bonding is based on mechanical delamination of different interfaces of thin films and is proved to be very efficient in delaminating large area of graphene with high continuity. This technique which is tested on substrates up to $1\times4\ cm^2$ can potentially scaled up to wafer-scale. Our findings indicate that the copper contamination level obtained from our delamination technique is a few orders of magnitude smaller than what that has already achieved with widely-used PMMA-assisted method. This holds great promise for the future of large-scale electronic applications of graphene.

Chapter 5 : CVD Monolayer MoS_2 Field Effect Transistors

5.1. INTRODUCTION

The remarkable electrical, mechanical, and optical properties of graphene has initiated research on other two-dimensional (2D) materials such as transition-metal dichalcogenides (TMDs). Of the TMDs, molybdenum disulfide (MoS_2) has particularly attracted a lot of attention to its tunable energy bandgap as a function of number of monolayers, e.g. bulk MoS_2 has an indirect bandgap of 1.3 eV, while monolayer MoS_2 has a direct bandgap of 1.8 eV.[78-80] This tunable bandgap allows for high I_{on}/I_{off} FETs and the confinement of channel charge carriers to nearly atomic thicknesses (0.65 nm) which improves gate control and reduces short-channel effects. However, the device-to-device variability of the electrical performance of FETs fabricated on 2D materials, including gate hysteresis and imprecise threshold voltage (V_{th}) control is usually considered a challenge to their commercialization. One of the main reasons of this variation is known to be environmental moisture adsorbed on the hydroxylated gate dielectric surface and the hydrophilic surface of MoS_2.[81-84] In this chapter, a general method for improving the DC electrical performance of MoS_2 FETs using a polymer cap is demonstrated. The polymer used for this study is the DuPont Teflon-AF. It has an amorphous structure and a polar bonds of C-F with dipole moments of 1.13 D.[85] MoS_2 FETs were encapsulated inside Teflon AF by a spin coating process (4000 rpm, 1 minute) and cured at 250 ^oC for 30 minutes in N_2 glovebox. The electrical performance of ~ 60 MoS_2 FET at low and high electric field were monitored before and after applying the cap. The polymer causes no structural change to the MoS_2 and leads to improvement in key electrical device metrics.

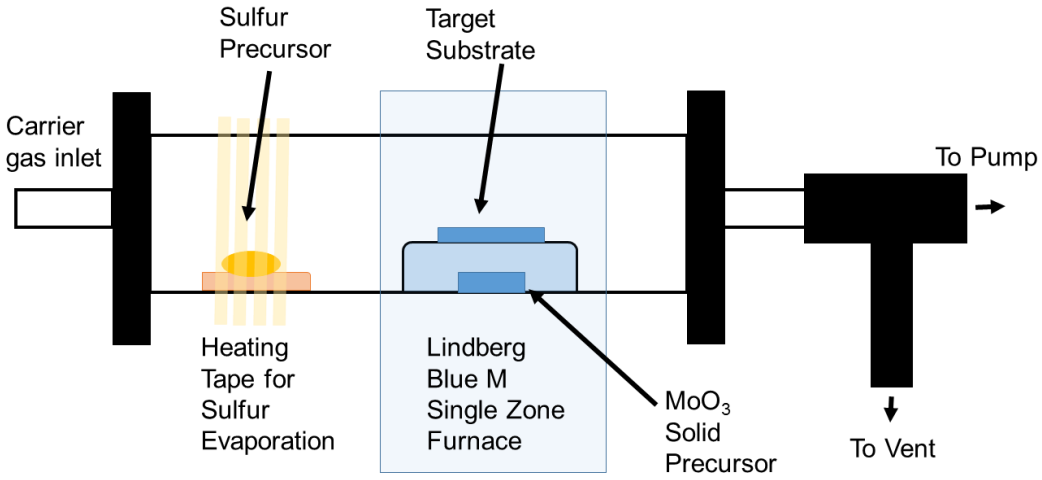

Figure 5.1: Schematic of the CVD growth furnace.

5.2. CVD GROWTH OF MoS_2

The MoS_2 atomic layer films were grown on heavily doped Si wafers capped by 300 *nm* SiO_2 and by standard vapor transfer growth process. A schematic of the CVD tube system used for growing MoS_2 is shown in Figure 5.1.

Large area MoS_2 monolayer films were grown directly on surface cleaned SiO_2 (285 nm)/ Si substrates using vapor transport process starting from solid precursors. The starting materials were MoO_3 (15 mg) and sulfur (1 g) powder that were loaded in separate alumina crucibles and placed inside the tube (inner diameter = 22 mm), with the sulfur crucible outside the actual furnace and heated independently using a heating tape.

After loading the starting material and the substrates, the tube was pumped down to base pressure (< 10 mTorr), and then the gas lines were purged by flowing in UHP N_2 gas at 200 sccm. After 4 purging cycles, the tube was brought to atmospheric pressure with N_2 flow at 10 sccm. Then temperature of the furnace was raised to 850 °C at a rate of 50 °C/min. When the temperature of the tube furnace was at 650 °C, the sulfur was heated to

150 °C (+/- 5 °C) and kept at that temperature. The growth continued for 5 min at 850 °C. After the 5 minutes at 850 °C the heater to the furnace was turned off for cooling without any feedback. Heating of the sulfur was cut off once the furnace cooled down to 650 °C. By controlling the growth parameters we were able to obtain pseudo-continuous areas in the *mm* by *mm* scale. An image of the Si/SiO_2 chip and a microscope image of the monolayer MoS_2 under microscope is shown in Figure 5.2.

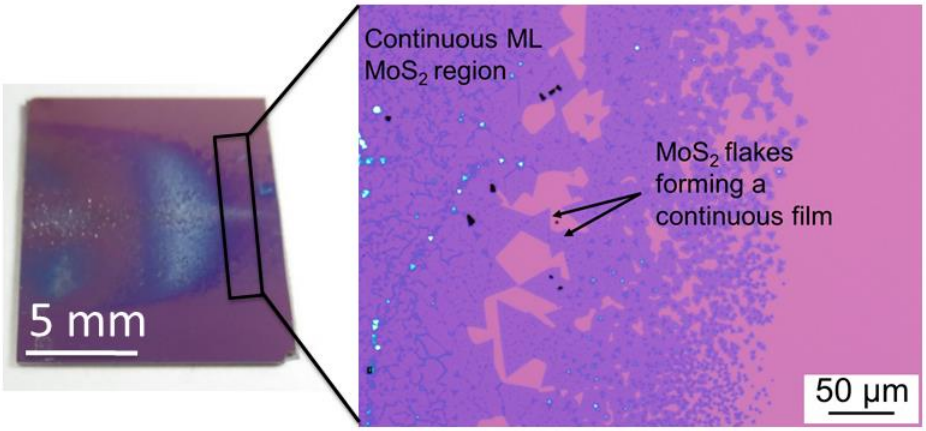

Figure 5.2: Image of the Si/SiO_2 substrate after the growth and a microscope image of the monolayer MoS_2.

5.3. Raman and Photoluminescence Metrology

Because of its sensitivity to interlayer coupling, Raman spectroscopy is a standard technique to determine the number of CVD-grown monolayers. Also, the direct bandgap of monolayer MoS_2, leads to a pronounced photoluminescence (PL) peak when excited by the same laser in the Raman setup. Figure 5.3 (a) and (b) show the corresponding Raman and PL spectra of CVD-grown monolayer MoS_2 before and after applying the polymer cap.

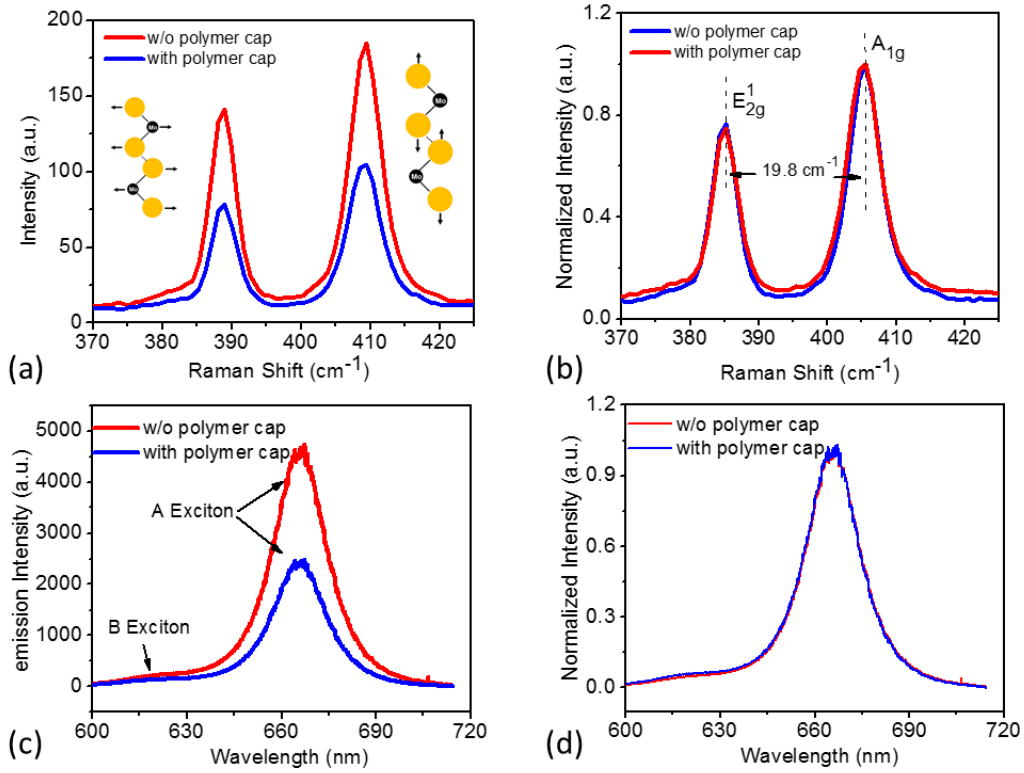

Figure 5.3: Raman and PL spectra of ML MoS_2 before and after applying the polymer cap. Comparison of (a) absolute values, and (b) normalized values of Raman peaks. Comparison of (c) absolute values and (b) normalized values of PL peaks.

The Raman peak positions of an out-of-plane A_{1g} and in-plane E^1_{2g} peaks for monolayer MoS_2 is 409 and 389 cm^{-1} corresponding to a peak separation of 19.8 cm^{-1}, characteristics of monolayer MoS_2.[86] The PL peak position of the A exciton is at 1.86 eV, consistent with reported values for monolayer MoS_2.[87] No changes is observed in Raman and PL spectra suggesting that the polymer encapsulation does not lead to any structural change on MoS_2.

5.4. DEVICE FABRICATION PROCESS

Back-gated filed-effect transistors were used as the chosen platform to study the electrical properties of the CVD monolayer MoS_2 films. In order to statistically study the film, a device fabrication method based on photolithography and similar to the fabrication process of GFETs were used. The details of the fabrication process is explained in Appendix D.

The device fabrication process started by growing 300 *nm* thermally-grown SiO_2 on heavily p-doped (ρ = 0.001-0.01 $\Omega.cm$). Using photo-lithography and a bilayer resist process, the alignment marks, Cr/Pt (4 *nm*/15 *nm*), were patterned and deposited. A 20-second rinse in the Piranha solution was used for the lift-off process. This helped to ensure no photoresist contamination is left on the growth surface.

In the next step, the monolayer MoS_2 was grown on the substrates using the CVD process described in section 5.2.

The next step after the growth is to isolate FET channels. For this step, photoresist S1805 is spin coated on the sample and baked at 120 ^oC. Using a photolithography process, the resist is exposed for 4 seconds and developed in MF-26A developed solution for 1 minute. Using Cl_2 plasma (40 *mTorr*, Power: 75 *W* for 1 minute) the device channels were isolated. Without removing the resist from the MoS_2 channels, LOR 3B and S1805 are spin coated on the substrate and baked. In the last step the source and drain contacts are patterned and filled with Ag/Pd (20 *nm*/ 20 *nm*) metal pads.

The lift-off process is done in Remover PG at 50 ^oC, followed by Acetone and IPA rinse.

Using this technique, devices with constant channel length of 3 μm and variable channel width of 3, 6 and 9 μm were fabricated.

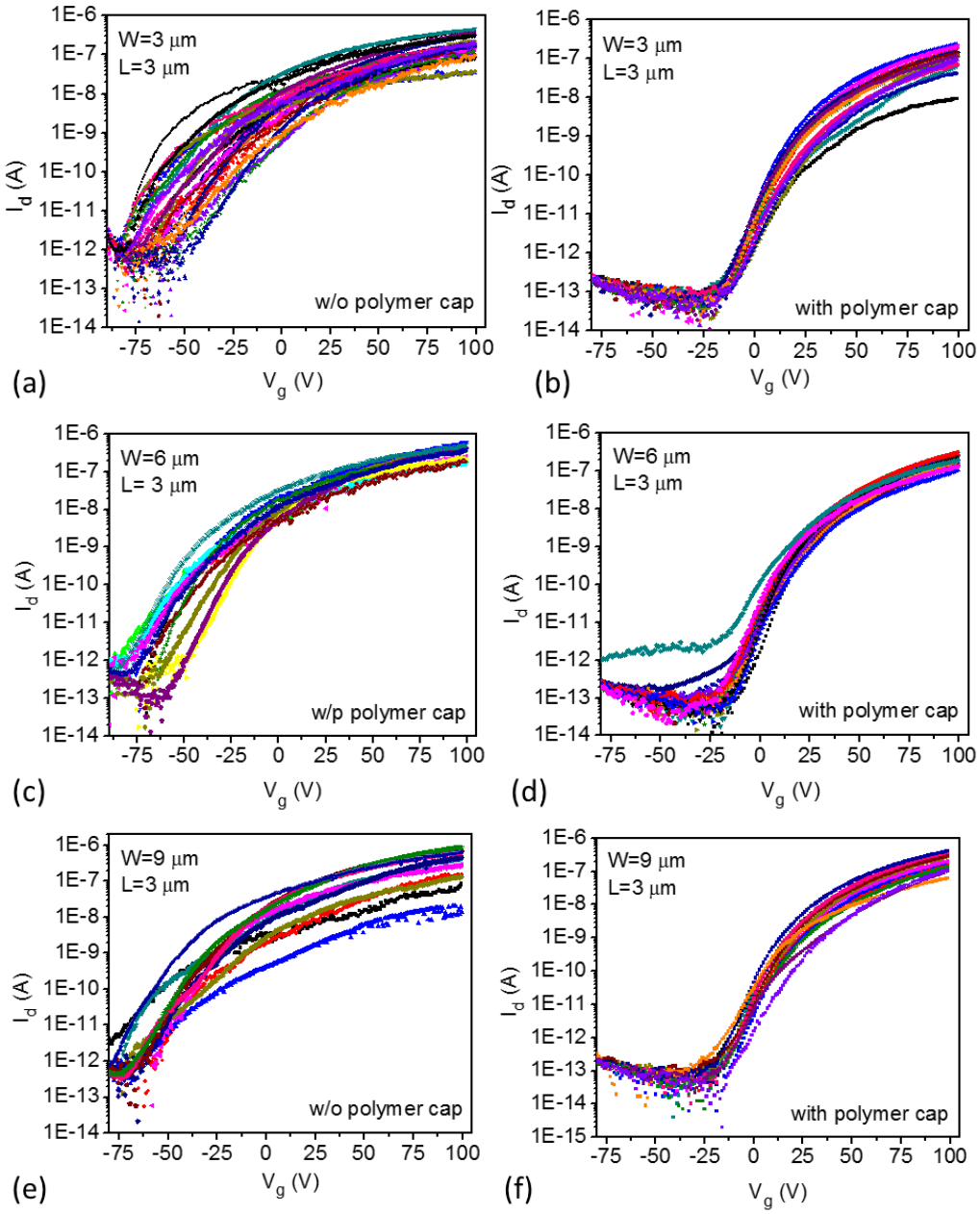

Figure 5.4: Electrical transport characteristics of ML MoS_2 FETs of devices with fixed channel length (L = 3 μm) and variable channel width (W = 3, 6 and 9 μm) before (a,c and e) and after (b, d and f) coating with polymer cap.

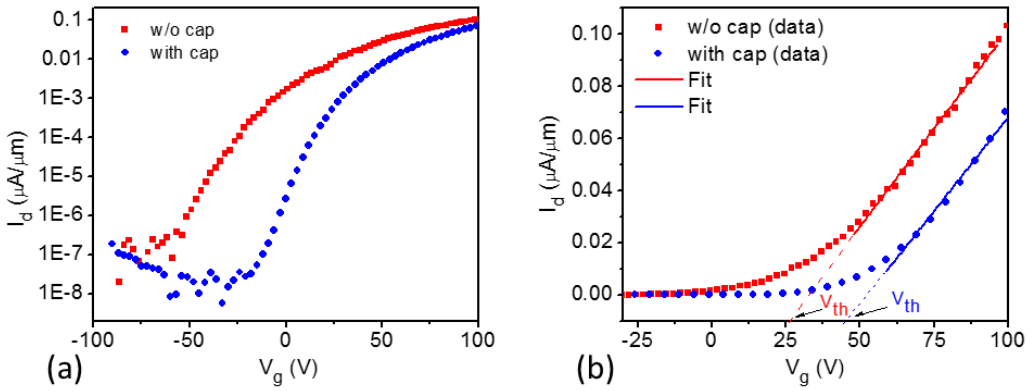

Figure 5.5: Electrical transfer curves of representative MoS_2 FETs before and after applying the polymer cap in (a) log scale and (b) linear scale.

5.5. DC ELECTRICAL CHARACTERIZATIONS

The DC electrical performance of 60 randomly-chosen back-gated MoS_2 FETs were tested before and after applying the Teflon-AF cap. The statistics of the electrical performance of the FETs were then studied and were compared to show the performance improvement by applying a capping layer.

Figure 5.4(a)-(f) show the transport electrical characteristics of MoS_2 FETs with fixed channel length of 3 μm and variable channel width of 3, 6 and 9 μm.

The use of polymer cap enables significant improvement in key performance metrics of all the tested devices, reduces the electrical performance variations and improves the devices to device consistency.

Figure 5.5(a) compare the transfer curves of representative MoS_2 FETs, before and after applying the polymer cap. The threshold voltage that can be extracted by interpolating the linear regime of the transfer curve, shifts towards more positive values (Figure 5.5(b)). The off-current is reduced by an order of magnitude, resulting in a similar improvement in

the transistor I_{on}/I_{off} ratio. The subthreshold swing behavior is improved in all devices after applying the polymer cap. The reduction in subthreshold swing and I_{on}/I_{off} could be a direct result of the polar nature of the Teflon-AF cap which neutralizes the charge impurities and defects and results in a reduced off-state current.[88]

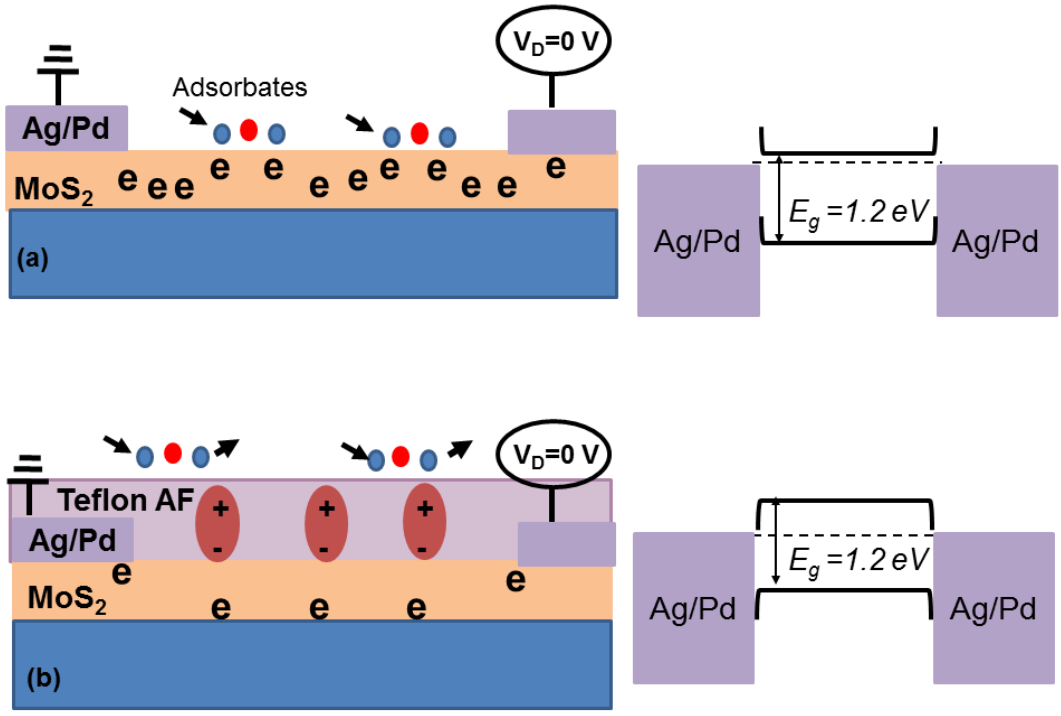

Figure 5.6: (a) Schematic cross section and energy band diagram of MoS_2 FET before polymer encapsulation shows the impact of local electric fields of adsorbates in room ambient on the channel charge conduction. (b) Schematic cross section and the band diagram of the MoS_2 FET after applying the polymer cap shows a reduction of the carrier density duo to the internal dipole electric field of the C-F bonds in the polymer. Diagrams are sketched for $V_g = V_d = 0$ V.

Figure 5.6 shows a schematic of the device cross section and the energy band diagram before and after applying the polymer cap. The hydrophobic nature of the cap repels the moisture molecules of the ambient. This reduces the charge sharing between the ambient moisture molecules and the channel and reduces the off current state. The dipole moments of the cap can get easily aligned to the external electric field of the back gate and reduces the charge density within the channel. This reduction in the charge density shows up in the form of a slight reduction in the drain current.

5.6. DEVICE PERFORMANCE STATISTICS

The histogram distributions of the threshold voltage (V_{th}) and hysteresis of 60 devices measured in ambient condition before and after applying the cap are presented in Figure 5.7.

Before applying the cap, the V_{th} of ML MoS_2 FETs ranges -25 to 25 V and with the off-state current value reaching 10 $nA/\mu m$. This prevents the FETs from turning off completely at V_g=0 V. The V_{th} data shows a positive shift and a narrower distribution after applying the polymer cap. The average value of V_{th} shifts from ~20 V to ~53 V after applying the polymer cap, reducing the drain current by ~ 2-3 orders of magnitude at V_g = 0 V. This positive shift could be due to lower density of the carriers in the channel after applying the cap. This along with the improvement of the subthreshold swing lead to the lower drain current at 0 V.

The gate hysteresis depends on several factors such as the gate sweep range, the sweep steps and the impact of environment on the channel and gate oxide. The first two factors are the same for pre and post polymer application. The gate bias ranges -100 $V < V_g$ < 100 V and ΔV_g = 1 V for both cases. The main difference, coming from the third factor,

causes a smaller average ΔV_g and an improved consistency from device to device after applying the polymer cap.

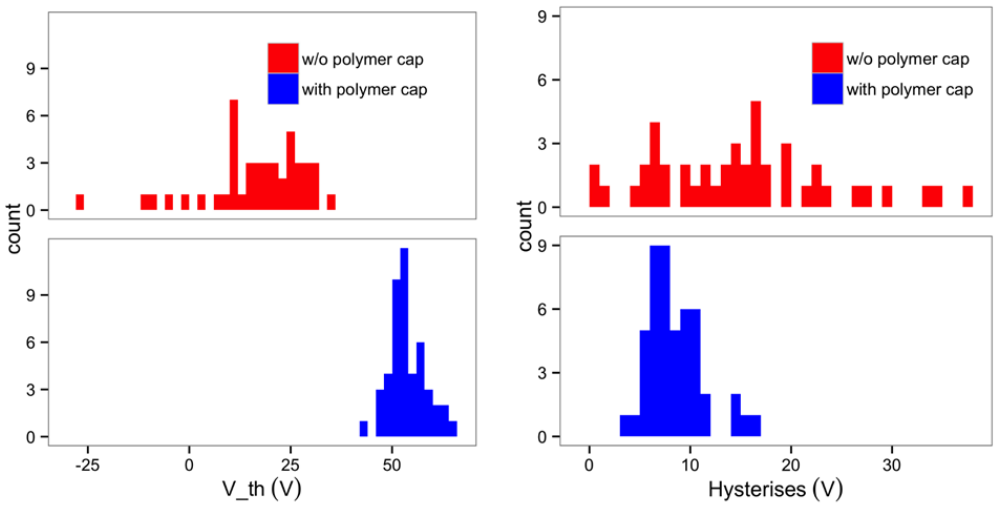

Figure 5.7: Histogram distribution of the threshold voltage (V_{th}) and the hysteresis before and after applying the polymer cap.

The histogram distributions of the subthreshold swing (*SS*) and mobility before and after applying the cap are presented in Figure 5.8.

The subthreshold swing (SS) is calculated using equation 5.2:

$$SS = \ln(10)\frac{d(V_g)}{d(ln(I_d))} \tag{5.2}$$

Because of using 300 *nm* thick SiO_2 gate dielectric, the SS values are in the range of several *V/Dec*. The average subthreshold swing value shows 31% improvement after

applying the polymer cap and reduces from 16 *V/Dec* to 11 *V/Dec*. This could be understood by less charge sharing between the channel and the adsorbates in ambient.

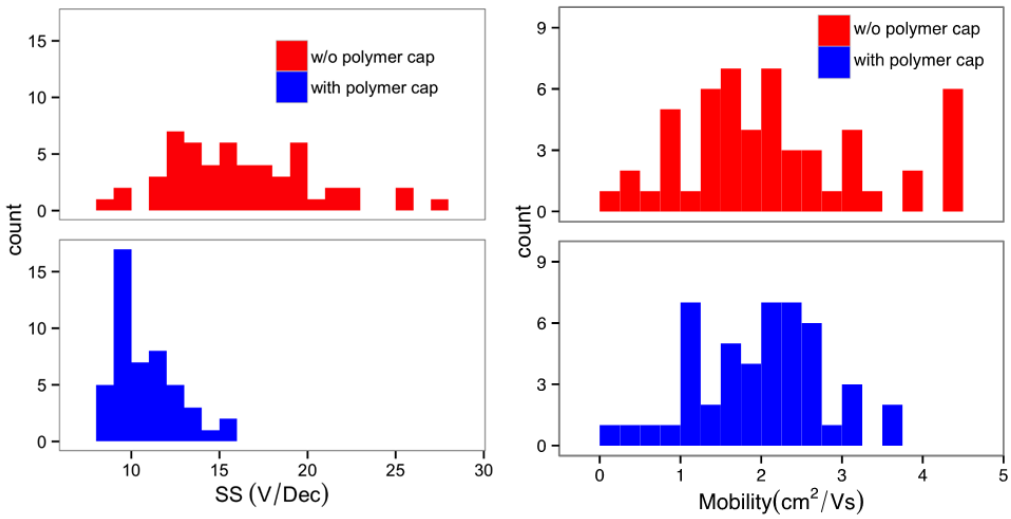

Figure 5.8: Histogram distribution of subthreshold swing (*SS*) and field effect mobility before and after applying the polymer cap.

The field-effect mobility (μ) can be extracted based on the slope of dI_d/dV_g fitted to the linear regime of the transfer curves using the following equation:

$$\mu = \frac{L}{WC_{ox}V_d}\frac{dI_d}{dV_g} \tag{5.1}$$

where *W* and *L* are the width and length of channel, C_{ox}= 115E-10 F/cm^2 is the capacitance per unit area of the 300 *nm* gate oxide dielectric, V_d=0.2 *V* is the drain voltage, V_g and I_d are the gate voltage and drain current respectively. The extracted filed-effect mobility

ranges 1-5 cm^2/Vs. The average mobility does not show a significant change after applying the polymer cap. This indicates that the adsorbates in the ambient does not play a significant role in scattering carriers. It has been reported previously that the dominant scattering mechanism of carriers above 100 K are the substrate phonons.[83]

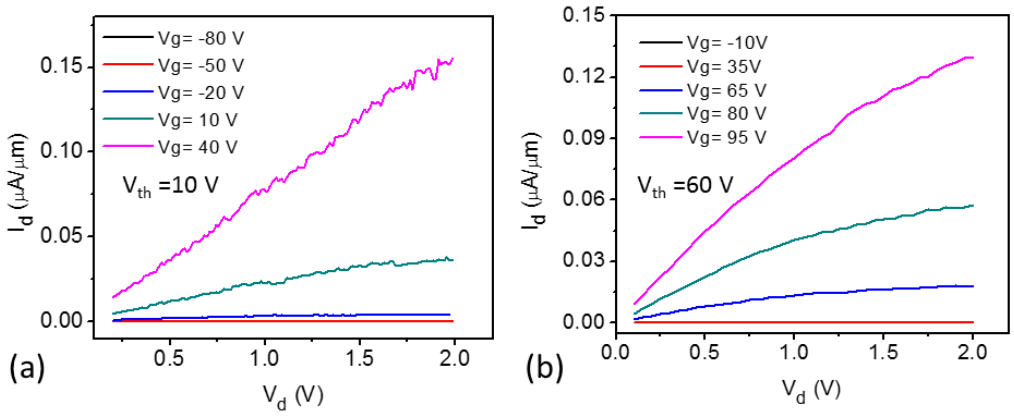

Figure 5.9: High field behavior of a representative MoS_2 FET (a) before and (b) after applying the polymer cap.

5.7. HIGH-FIELD BEHAVIOR

The high electric field behavior of a representative MoS_2 FET before and after applying the polymer is shown in Figure 5.9 (a) and (b). As in low electric field regime, the drain current shows a slight reduction after applying the polymer, which can be understood by a reduction in the carrier density of the channel. The MoS_2 FET shows a semi-saturation behavior after applying the polymer cap. The origin of this current saturation is not well understood but could be due to the minimized charge sharing and smaller density of carriers after applying the cap.

5.8. SUMMARY

The CVD growth of large area monolayer MoS_2 and the uniformity of the material and electrical properties of the grown film was demonstrated. We used a platform of back-gated field-effect transistors to evaluate the device performance. The electrical performance of the MOS_2 FETs was evaluated before and after applying a polar polymer coating (Teflon-AF). The data shows improvement in key device metrics, suggesting that the polar nature of the polymer cap reduces the impact of charge defects and interfacial electronic traps on device performance. The cap, which is only 100 *nm* thin, can be used as a passivation material for improving the performance of other 2D solids.

Chapter 6: Conclusion

The combination of the 2D solids with Si technology is widely considered among the greatest prospects of adopting the discoveries of this new category of materials in research laboratories into practical electronic applications. Integrated 2D solids with Si can benefit from both the maturity of Si technology and the outstanding electronic, optical, thermal and mechanical properties of these materials.

However, this integration has proven to be a grand challenge due to (i) the lack of a reliable large-scale preparation scheme for 2D materials which is compatible with the standard Si technology and preserves the high performance of the mechanically-exfoliated films and (ii) a reliable transfer/bonding method for bonding 2D materials to the target Si substrates.

In this thesis, we tried to address the first challenge by adopting the chemical vapor deposition mechanism for large-scale growth of graphene and molybdenum disulfide. The uniformity of the CVD-grown films and the device performance consistency was discussed in details.

The challenge of bonding to Si platform was addressed by a novel approach, mechanical delamination technique. The graphene obtained by direct delamination method, showed promising electrical properties. To reduce the film roughness after the transfer process, further research is required, such as new growth techniques for synthesizing graphene on single-crystalline substrates.

Appendices

A: Wafer-scale growth of graphene on copper thin films

Step	Details
1. SiO_2 growth	Grow 300 *nm* SiO_2 using "Gate oxide" furnace and running recipe "Gate 1050" for 7 hours 30 minutes.
2. Cu film deposition	Deposit ≤ 1 μm of Cu (purity 99.999% in graphite crucible) by CHA1, deposition rate ≤ 1 *nm/sec*, the temperature of the chamber can go up to 100 *ºC*.
3. Graphene growth using BM LPCVD process	1. Load the Cu coated Si substrate into the BM chamber. 2. Wait for the pressure < 0.03 *mBar*. 3. Purge with H_2 (1000 *sccm*) for 40 seconds. 4. Pump to pressure < 0.02 *mBar*. 5. Flow H_2 with 1000 *sccm* and 10 *mBar* . 6. Start bottom and top heaters with 150 *ºC/min*. 7. Start IR sensor at TC (thermos-couple reading) = 550 *ºC*. 8. Tune IR to 910 *ºC* (50 *ºC/min*). 9. At IR = 910 *ºC*, wait for 300 seconds (annealing step in H_2 ambient). 10. Turn off H_2 flow. 11. Wait for the pressure < 0.5 *mBar*. 12. Turn on CH_4 (flow rate: 15 *sccm*) and wait for 40 seconds. 13. Grow graphene for 360 seconds. 14. Start cooling down by setting top and bottom heater to 400 *ºC*. 15. Turn off IR sensor and CH_4 flow at 550 *ºC*. 16. Turn on N_2 flow (500 *sccm*) and wait for the temperature to go down to 120 *ºC*. 17. Unload the wafer.

Table A1: The details of wafer-scale growth of graphene on copper thin films.

B: Graphene transfer to 100 *mm* Si Substrate

Step	Details
1	Spin coat 495 PMMA A4 on 100 *mm* growth substrate of graphene (2000 *rpm* for 60 seconds).
2	Clean up the edges of the wafer using Acetone and a clean wipe.
3	Leave the wafer into a vacuum desiccator for 24 hours to dry up.
4	Mix 1 *ml* of BOE (1:6) with 40 *ml* of APS-100 copper etchant in a clean Pyrex dish.
5	Immerse the PMMA-coated wafer into the etching solution for ~ 4 hours. Check for the copper to be etched completely and graphene to be floating on the etching solution.
6	Remove the graphene/PMMA stack from the etching solution using a clean 100 *mm* Si wafer and place it into DI water for half an hour. This step can be repeated to reduce the copper contamination caused by the previous etching step.
7	Remove the graphene from DI water, using the target substrate.
8	Leave the substrate in a vacuum desiccator for 24 hours to dry up.
9	Bake the PMMA on the hot plate at 180 *°C* for 3-5 minutes.
10	Remove the PMMA by immersing the substrate in Acetone for ~8 hours. Acetone can be refreshed every hour to reduce the PMMA residue.
11	Rinse with IPA and gently blow dry with N_2 gun.

Table B1: Steps for transferring graphene from 100 *mm* Si substrate to the same size target substrate.

C: Fabrication steps of GFETs

Step	Details
1. SiO_2 Growth	Grow 90 *nm* SiO_2 using "Gate oxide" furnace and running recipe "Gate 1050" for 60 minutes.
2. Graphene Transfer	Transfer graphene using the process detailed in Appendix A.
3. Alignment mark patterning	1. Coat with LOR 3B (3000 rpm for 45 seconds), bake on the hot plate at 170 *°C* for 5 minutes. 2. Coat with S1805 (4000 rpm for 60 seconds), bake on the hot plate at 120 *°C* for 2 min. 3. Expose for 0.6 seconds by EVG aligner (36.5 mW/cm^2 for 405 *nm* wavelength and 19.5 mW/cm^2 for 365 *nm* wavelength). 4. Develop at MIF-300 for 2-2.5 minutes. 5. Rinse with DI water and blow dry with N_2 gun. 6. Deposit Ti/Pd (1.8 *nm*/48 *nm*) with CHA1. 7. Immerse in Remover PG for ~1 hour (T=300 *K*), slowly agitate to see the photoresist coming off. 8. Immerse in Acetone and IPA for 2 minutes each and blow dry with N_2 gun.
4. Isolation of Device Channels	1. Coat with S1805 (4000 rpm for 60 sec). 2. Bake on the hot plate at 120 *°C* for 2 minutes. 3. Expose for 0.6-0.7 seconds by EVG aligner. 4. Develop in MIF-319 for 75 seconds. 5. Rinse with DI water and blow dry with N_2 gun. 6. Etch graphene using Plasmatherm II and O_2 plasma (O_2 pressure: 200 *mTorr*, Power: 50 *W* for 55 seconds). 7. Check under microscope to make sure graphene is etched from the unprotected area.

4. Patterning of Source/Drain Contacts	1. Coat with LOR 3B (3000 rpm for 45 seconds), bake on the hot plate at 170 *°C* for 5 minutes. 2. Coat with S1805 (4000 rpm for 60 seconds), bake on the hot plate at 120 *°C* for 2 min. 3. Expose for 0.6 seconds by EVG aligner. 4. Develop at MIF-300 for 2-2.5 minutes. 5. Rinse with DI water and blow dry with N_2 gun. 6. Deposit Ti/Pd (1.8 *nm*/48 *nm*) with CHA1. 7. Immerse in Remover PG (40 *°C*) for ~5 minutes, slowly agitate to see the photoresist coming off. 8. Immerse in Acetone and IPA for 2 minutes each and gently blow dry with N_2 gun.

Table C1: The details of fabrication of GFETs on 100 *mm* Si substrate.

D: Fabrication steps of FETs on MoS_2

Step	Details
1. Alignment mark patterning	1. Coat with LOR 3B (3000 rpm for 45 seconds), bake on the hot plate at 170 *ºC* for 5 minutes. 2. Coat with S1805 (4000 rpm for 60 seconds), bake on the hot plate at 120 *ºC* for 2 min. 3. Expose for 4 seconds by MA6 aligner. 4. Develop the resist using MF-26A for 1 minute. 5. Rinse with DI water and blow dry with N_2 gun. 6. Deposit Cr/Pt (4 *nm*/16 *nm*) with CHA1. 7. Immerse in Remover PG for ~5 minutes (T=40 *ºC*) to lift off the resist. 8. Immerse in Acetone and IPA for 2 minutes each and blow dry with N_2 gun. 9. Clean in Piranha solution for 10 seconds to remove resist residue before MoS_2 growth.
2. MoS_2 growth	Grow monolayer MoS_2 at 850 *ºC* using solid precursors.
3. Isolation of Device Channels	1. Coat with S1805 (4000 rpm for 60 sec). 2. Bake on the hot plate at 120 *ºC* for 2 min. 3. Expose for 4 seconds by MA6 aligner. 4. Develop the resist using MF-26A for 1 minute. 5. Rinse with DI water and blow dry with N_2 gun. 6. Etch graphene using Plasmatherm II and Cl_2 plasma (Cl_2 pressure: 40 *mTorr*, Power: 75 *W* for 1 minute). 7. Check under microscope to make sure MoS_2 is etched from the unprotected area.
4. Patterning of Source/Drain Contacts	1. Coat with LOR 3B (3000 rpm for 45 seconds), bake on the hot plate at 170 *ºC* for 5 minutes. 2. Coat with S1805 (4000 rpm for 60 seconds), bake on the hot plate at 120 *ºC* for 2 min. 3. Expose for 4 seconds by MA6 aligner. 4. Develop the resist using MF-26A for 1 minute.

	5. Rinse with DI water and blow dry with N_2 gun. 6. Deposit Ag/Pd (20 *nm*/20 *nm*) with CHA1. 7. Immerse in Remover PG (40 *°C*) for ~5 minutes, slowly agitate to see the photoresist coming off. 8. Immerse in Acetone and IPA for 2 minutes each and gently blow dry with N_2 gun.
5. Polymer Encapsulation	1. Spin coat Teflon AF at 4000 rpm for 1 minute. 2. Cure at 250 *°C* for 30 minutes in N_2 glovebox.

Table D1: The details of fabrication and encapsulation of FETs on monolayer MoS_2 grown on SiO_2 and Si_3N_4 substrate.

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