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Metal-Oxide-Semiconductor Devices Based on Epitaxial Germanium-Carbon Layers Grown Directly on Silicon Substrates by Ultra-High-Vacuum Chemical Vapor Deposition

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by

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Dedication

To my wife, Julia, whose loving support and encouragement has made all the difference.

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Metal-Oxide-Semiconductor Devices Based on Epitaxial Germanium-Carbon Layers Grown Directly on Silicon Substrates by Ultra-High-Vacuum Chemical Vapor Deposition

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After the integrated circuit was invented in 1959, complementary metal-oxide-semiconductor (CMOS) technology soon became the mainstay of the semiconductor industry. Silicon-based CMOS has dominated logic technologies for decades. During this time, chip performance has grown at an exponential rate at the cost of higher power consumption and increased process complexity. The performance gains have been made possible through scaling down circuit dimensions by improvements in lithography capabilities.

Since scaling cannot continue forever, researchers have vigorously pursued new ways of improving the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs) without having to shrink gate lengths and reduce the gate insulator thickness. Strained silicon, with its ability to boost transistor current by improving the channel mobility, is one of the methods that has already found its way into production.

Although not yet in production, high-κ dielectrics have also drawn wide interest in industry since they allow for the reduction of the electrical oxide thickness of the gate stack without having to reduce the physical thickness of the dielectric. Further out on the horizon is the incorporation of high-mobility materials such as germanium (Ge), silicon-germanium ($Si_{1-x}Ge_x$), and the III-V semiconductors.

Among the high-mobility materials, Ge has drawn the most attention because it has been shown to be compatible with high-κ dielectrics and to produce high drive currents compared to Si. Among the most difficult challenges for integrating Ge on Si is finding a suitable method for reducing the number of crystal defects. The use of strain-relaxed $Si_{1-x}Ge_x$ buffers has proven successful for reducing the threading dislocation density in Ge epitaxial layers, but questions remain as to the viability of this method in terms of cost and process complexity.

This dissertation presents research on thin germanium-carbon ($Ge_{1-y}C_y$) layers on Si for the fabrication of MOS transistors with improved drive currents. By incorporating a small amount of C in Ge, the crystal quality of Ge epitaxial layers grown directly on Si can be dramatically improved. The $Ge_{1-y}C_y$ layers have been used to fabricate high-drive-current *p*-MOSFETs with high-κ dielectrics and metal gates. In addition to the electrical results, materials-related experimental data was acquired and analyzed to provide insights on the surface morphology, crystal quality, strain, C incorporation, and growth kinetics of the $Ge_{1-y}C_y$ layers. This work describes an exciting new possibility for the ultimate goal of incorporating high-mobility semiconductor materials in CMOS technology.

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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Steady, exponential increase in the performance of silicon-based complementary metal-oxide-semiconductor (CMOS) integrated circuits has been a reliable feature of semiconductor technology since the integrated circuit was invented in 1959. During the 1970s the semiconductor industry settled into a pattern of producing a new generation of integrated circuits every three years, with each new generation containing four times the number of transistors, four times the memory, and operating at more than twice the speed of the previous generation. The manufacturing cost per transistor has also been drastically reduced, since successive technology nodes have had increasing numbers of transistors per chip. The trend of shrinking circuit features and faster performance was famously predicted by Gordon Moore in 1965. Widely known as "Moore's Law," it continues to be a guiding principle for electronics innovation in the 21st century.

Advances in lithography have long been the driving force behind Moore's Law. Since each new technology node has required smaller circuit dimensions to achieve the sought-after performance gains, researchers and developers have been constrained to find ways of improving lithography to enable the patterning of smaller features. For metal-oxide-semiconductor field-effect transistors (MOSFETs) used in high-performance CMOS, scaling has required that the gate length be reduced to the sub-100 nm regime. According to the 2005 International Technology Roadmap for Semiconductors (ITRS),

by the year 2010, the MOSFET gate length for high-performance logic will need to be below 18 nm [1]. By 2020, the 2005 ITRS predicts a gate length of 5 nm. The technological challenge is daunting, and it appears that physical (and practical) limits to scaling are on the horizon. Significant scaling challenges must be overcome to satisfy the ever-increasing demands on transistor performance—both in the short term and in the long term [2].

Huge resources have been invested in the search for new materials that can improve integrated circuit performance without the need for scaling. One of the main concerns for MOSFETs is the thickness of the gate insulator. With the reduction of gate lengths and increased channel doping, the gate oxide thickness has been reduced dramatically in order to maintain gate control over the channel. For high-performance logic technology, the 2005 ITRS predicts that a gate stack with an effective oxide thickness of 6.5 Å and a maximum gate leakage current density of 1560 A/cm^2 will be required by 2010 [1]. It is unlikely that conventional, thermally-grown silicon dioxide (SiO_2) dielectrics will be able to satisfy this requirement, since quantum-mechanical tunneling current through the oxide increases exponentially with decreasing physical thickness [3]. Indeed, a physical thickness of 10-15 Å corresponds to only 3-4 atomic monolayers of SiO_2. High-κ dielectrics have been proposed to mitigate the oxide scaling problem [4, 5]. Since high-κ oxides have a larger dielectric constant than SiO_2, they can have a greater physical thickness without sacrificing gate control. The increased thickness of the layer diminishes quantum tunneling current.

A conventional metric for measuring CMOS performance is the MOSFET intrinsic delay, denoted by τ, which is equal to the total capacitance times the supply voltage divided by the total current, or CV/I. While oxide scaling and/or the use of high-κ dielectrics decrease the gate capacitance, and hence reduce τ, the MOSFET delay

can also be improved by boosting the transistor drive current via reducing the device resistance. Much effort has been exerted in modern CMOS technology to mitigate parasitic resistances, including the engineering of abrupt junctions, the reduction of the contact metal Schottky barrier height, and the development of novel implantation and annealing schemes to reduce dopant diffusion and increase dopant activation. In the most recent technology nodes, intense efforts have been also applied toward reducing the device resistance by improving the channel mobility, particularly with the use of strain.

Indeed, channel and/or strain engineering may be the only means of dramatically improving Si-based CMOS circuits in the near future. Compressively-strained silicon-germanium alloys ($Si_{1-x}Ge_x$) on Si [6-10] and biaxial tensile-strained Si on relaxed $Si_{1-x}Ge_x$ buffer layers [6-8, 11] were two of the first approaches that drew interest from research scientists. These wafer-level strain methods have never made their way into large-scale manufacturing. On the other hand, uniaxial process-induced strain has been introduced into manufacturing [12-15] and is now being adopted in all 90-, 65-, and 45-nm high-performance logic technologies [16].

In theory, the highest performance gains that can result from channel engineering arise from a combination of strain engineering and the introduction of non-silicon materials with higher intrinsic mobility. One of the most attractive materials that has emerged in the research literature in recent years is Ge, which has a higher bulk mobility for both electrons (2×) and holes (4×) relative to Si. Germanium-channel MOSFETs have drawn attention due to the advances that have been made in high-κ gate dielectric technology [17-25]. Higher bulk mobility and a demonstrated compatibility with high-κ dielectrics (and reduced interfacial layer thicknesses compared to Si) make Ge a potential candidate for improving MOSFET drive current while allowing for continued aggressive scaling of the gate oxide.

The findings that will be presented in this treatise fall under the umbrella of research that investigates ways of integrating Ge epitaxial layers on Si wafers for improving channel mobility in MOSFETs. The specific focus of this research was to initiate the development of MOS devices that incorporate Ge layers doped with small amounts of C ($Ge_{1-y}C_y$) on Si (100) substrates. The addition of C to Ge facilitates high-quality, two-dimensional growth directly on Si. All of the device data in this study involved high-κ dielectrics (and metal gates), but the properties of specific high-κ materials was not a primary interest. The remaining sections of this introductory chapter will provide a brief overview of high-κ dielectrics, integration challenges of high-κ materials in Si-based CMOS, recent progress in high-κ/metal gate MOSFETs fabricated on bulk Ge wafers, and approaches for incorporating Ge layers on Si.

1.2 HIGH-κ GATE DIELECTRICS

As mentioned above, high-κ oxides have a higher dielectric constant than SiO_2, which means that the physical thickness of the oxide can be increased without sacrificing the control of the gate over the channel (i.e. decreasing the oxide capacitance). Thicker oxides reduce the quantum tunneling current through the gate. The oxide capacitance (C_{ox}) can be expressed as

$$C_{ox} = \frac{\kappa \varepsilon_0}{t_{phys}}, \tag{1.1}$$

where C_{ox} is the capacitance per unit area, κ (= 3.9 for SiO_2) is the dielectric constant, ε_o is the vacuum permittivity, and t_{phys} is the physical dielectric thickness. From Equation 1.1 we see immediately that for a constant C_{ox}, the use of a high-κ (>3.9) material with a

larger dielectric constant compared to SiO_2 allows for a larger physical thickness. The equivalent SiO_2 thickness (t_{eq}) of a high-κ dielectric is given by

$$t_{eq} = \frac{3.9}{\kappa} t_{phys} . \tag{1.2}$$

Figure 1.1 shows a plot that was generated by Locquet *et al*. that compares the calculated tunneling leakage current density of SiO_2 to that of three other theoretical oxide systems as a function of t_{eq} [26]. The four sets of data points show the effect of varying the relative dielectric constant, the tunneling barrier height, and the tunneling effective mass (denoted in the figure as ε, Φ, and m_h, respectively). The substrate for these calculations was *p*-type Si with a doping density $N_a = 4.7\times10^{17}$ cm^{-3}. The barrier height is defined as the difference between the Fermi level and the valence band. The solid squares in the figure correspond to SiO_2. As shown in Fig. 1.1, materials with a higher relative dielectric constant show several orders of magnitude lower tunneling current than SiO_2 at the same t_{eq} due to increased t_{phys}. If the tunneling barrier height and the tunneling effective mass were to remain constant for all high-κ materials, then the benefits of a higher dielectric constant would be enormous, giving nearly ten orders of magnitude improvement in the tunneling current (as seen by comparing the solid circles to the solid squares in Fig. 1.1). Unfortunately, materials with a higher dielectric constant typically have a lower tunneling barrier and smaller tunneling effective mass.

The possible high-κ dielectric candidates to replace SiO_2 include metal oxides such as Ta_2O_5 [27, 28], TiO_2 [29, 30], ZrO_2 [31], HfO_2 [32], Y_2O_3 [33], Al_2O_3 [34, 35] and La_2O_3 [36] as well as their silicates and aluminates. Table 1.1 lists several high-κ dielectrics with their corresponding dielectric constants, band gap energies, and band offsets, as tabulated by Robertson in [37]. Also included in Table 1.1 are thermal

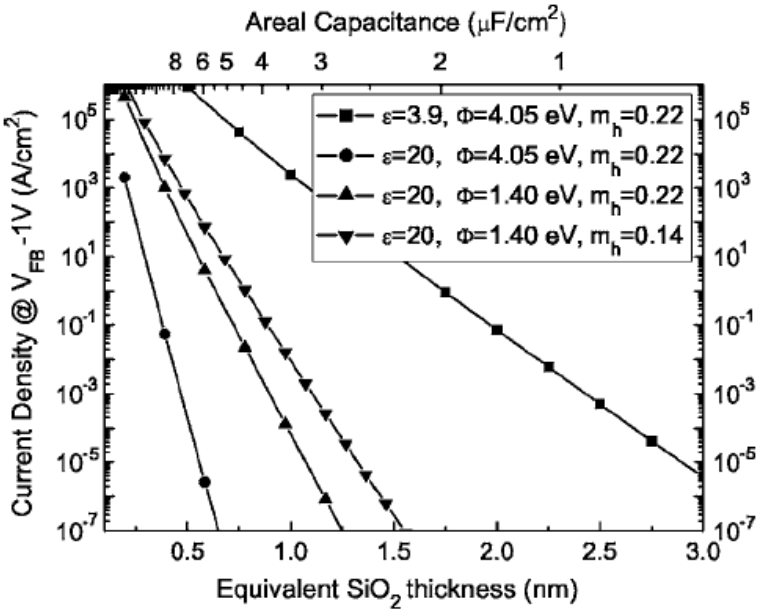


Figure 1.1. Absolute values of the calculated oxide tunneling current at $V_{FB}-1$ V vs. t_{eq} for SiO_2 (solid squares) and three other hypothetical oxide/Si systems. The top axis is the normalized capacitance corresponding to t_{eq} [26].

stability data with respect to Si, compiled by Wong [38]. While the most obvious requirement for extending oxide scalability is that the new material have a high dielectric constant, additional criteria must be met to make the high-κ dielectric a viable replacement for SiO_2. The material must have sufficiently large conduction and valence band offsets to form a barrier between the Si substrate and the gate electrode, since the oxide tunneling current is exponentially dependent on the square root of the barrier height [39]. The material must be thermodynamically stable on Si as well, able to withstand the high temperatures commensurate with the CMOS process.

There are also a number of integration challenges [40, 41] that must be overcome before high-κ dielectrics can be incorporated into a future technology node. For example, it has been reported that Fermi-level pinning due to trapped charges in

Dielectric	Relative Dielectric Constant ($\varepsilon/\varepsilon_0$)	Band Gap (eV)	Conduction Band Offset (eV)	Valence Band Offset (eV)	Thermal Stability w.r.t. Silicon
SiO_2	3.9	9.0	3.2	4.7	>1050 °C
Si_3N_4	7	5.3	2.4	1.8	>1050 °C
Al_2O_3	9	8.8	2.8	4.9	~1000°C RTA
La_2O_3	30	6.0	2.3	2.6	-
Y_2O_3	15	6.0	2.3	2.6	Silicate formation
ZrO_2	25	5.8	1.5	3.2	~900 °C
Ta_2O_5	22	4.4	0.35	2.95	Not stable
HfO_2	25	5.8	1.4	3.3	~950 °C
$HfSiO_4$	11	6.5	1.8	3.6	-
TiO_2	80	3.5	0	2.4	-
a-$LaAlO_3$	30	5.6	1.8	2.7	-
$SrTiO_3$	2000	3.2	0	2.1	-

Table 1.1. Properties of high-κ dielectrics, compiled from review articles written by Robertson [37] and H.-S. P. Wong [38].

high-κ/polysilicon transistors is responsible for high threshold voltages, which degrades the drive current [42]. Charge trapping experiments by Gusev *et al*. showed that the trap density in Al_2O_3 and HfO_2 is much higher than in SiO_2 [43]. The higher trap density leads to threshold voltage instabilities [44, 45]. Perhaps the greatest integration challenge for high-κ dielectrics is the observed degradation in the MOSFET carrier mobility. Figure 1.2 shows several *n*-MOSFET effective mobility (μ_{eff}) vs. vertical effective field (E_{eff}) plots by Gusev *et al*. showing the degradation of the electron mobility for HfO_2 and Al_2O_3 gate stacks compared to an oxynitride control and the universal curve for Si [43]. The reason for this mobility degradation has not been fully elucidated at this time. Proposed mechanisms include Coulomb scattering due to trapped charges [46-48] and the coupling of low-energy surface optical phonon modes

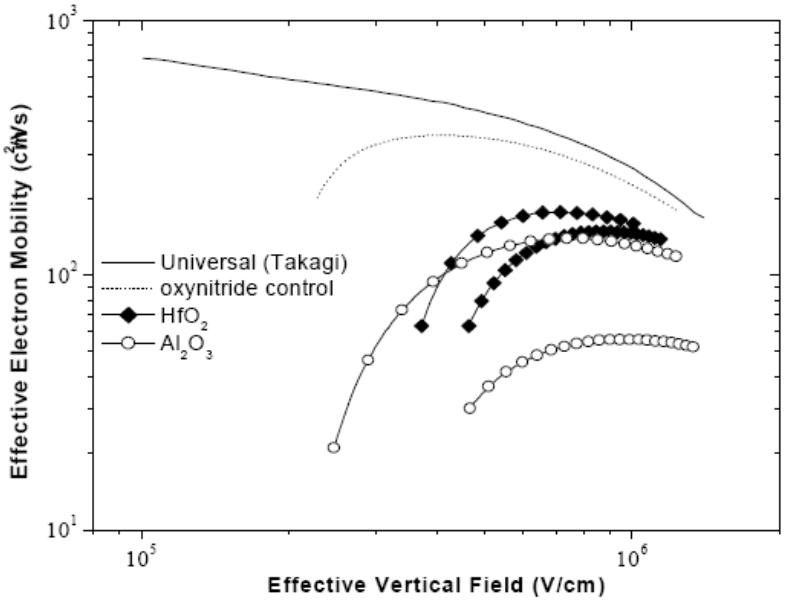


Figure 1.2. Effective mobility vs. vertical effective field data for *n*-MOSFETs showing degraded mobility using HfO_2 (solid diamonds) and Al_2O_3 (open circles) gate stacks compared to an oxynitride control (dashed line) and the universal curve for Si (solid line). The two curves for HfO_2 and Al_2O_3 resulted from differences in process conditions [43].

arising from the polarization of the high-κ dielectric to the inversion channel charge carriers [49, 50]. While historically mobility degradation has been a common feature of high-κ dielectrics, process improvements [51-53] and the use of fully-silicided polysilicon [54, 55] or dual work function metal gates [40, 56] have mitigated these concerns significantly. Fully-silicided and dual work function metal gates have the additional (and equally important) advantage of improving oxide scalability through the reduction of the polysilicon depletion effect [57].

In addition to extending oxide scalability on Si, high-κ dielectrics have opened up many new possibilities for high-channel-mobility MOSFETs. The native oxides on high-mobility Ge and III-V semiconductors are not suitable for CMOS, but the advent of

high-κ materials has generated a tremendous flurry of research on these alternative channel materials. The next section will discuss recent research on MOS devices fabricated on bulk Ge substrates using high-κ dielectrics and metal gates.

1.3 HIGH-K/METAL GATE STACKS ON BULK GERMANIUM WAFERS

Due to their poor mechanical strength and high cost, bulk Ge wafers are not compatible with CMOS. Thus, Ge-channel devices for high-volume manufacturing must be fabricated using epitaxial Ge layers on Si. Due to the challenges of depositing high-quality Ge crystal on Si, however, bulk Ge wafers are better suited for studying the properties of the gate stack [17-22, 25]. In this way, the deleterious effects of crystal defects on the electrical properties of the Ge-based gate stack are eliminated.

Bulk Ge crystal is not unfamiliar to the semiconductor industry, at least historically. The first transistors were made using Ge crystals. Silicon totally eclipsed Ge, however, due to the advantageous properties of its native dielectric SiO_2. Unlike Si, Ge does not possess a stable natural oxide that can passivate the surface, act as etch protection, or be used as a high-quality gate insulator [58, 59]. The thermodynamic instability of germanium dioxide (GeO_2) was shown by Prabhakaran *et al*. [60], who reported that low-temperature annealing of GeO_2 resulted in the transformation of GeO_2 to GeO on the surface, which thermally desorbed at around 420 °C. Thermal desorption at such low temperatures makes GeO_2 impractical as a gate dielectric for CMOS processes that require high-temperature steps. Another major drawback of GeO_2 is that it is soluble in water [58-60], which rules out almost all wet chemical processes that would attempt to use the Ge native oxide as an etch barrier.

The native dielectrics of Ge, including GeO_2, germanium nitride (Ge_3N_4) [61-63], and germanium oxynitride (GeO_xN_y) [61, 64], have all been explored as potential gate insulators for CMOS. In the 1990s, creative methods were employed for growing better-quality GeO_2 on Ge for MOS applications [65, 66]. But since GeO_2 is volatile at relatively low temperatures and is water soluble, alternative fabrication schemes that cover one of the native dielectrics (or the bare Ge surface) with a non-native insulator have proven more promising. One of the earliest examples of the non-native dielectric approach was reported in 1971 by Iwauchi and Tanaka, who demonstrated Ge MOSFETs with Al_2O_3 dielectrics using reactive DC sputtering of Al [67]. In 1986, Chang *et al*. obtained good interface properties through the use of thick films of an aluminum-phosphorus oxide mixture deposited over native GeO_2 [68]. Even SiO_2 has been explored as a possible non-native insulator on Ge [69, 70], but while SiO_2 has proven extremely successful on Si, its use on Ge has been proven to be much less effective. The main reason for this is the poor quality of the SiO_2/Ge interface. A solution to the SiO_2/Ge interface problem was proposed by Vitkavage *et al*., who examined the possibility of depositing a thin layer of Si onto the Ge substrate as a buffer layer prior to SiO_2 deposition [69]. The Si interlayer seemed to improve the interface with the Ge substrates, which was evidenced by a drastic reduction in the density of interface states [69].

The initial studies investigating non-native insulators on Ge concentrated on achieving good interface and bulk characteristics, and not necessarily on reducing the equivalent oxide thickness (EOT). As a result, most of the films were relatively thick, and would be unlikely to offer an EOT of less than 10Å to advance beyond the sub-20 nm regime. For example, the 2005 ITRS roadmap predicts the EOT for high-performance logic to be 9Å by the year 2008 and 5Å by 2012 [1]. Fortunately, the

natural progression of these lines of research has led to the use of high-κ dielectrics, which do offer the potential of scaling below 10Å (as described earlier).

Much of the groundwork for high-κ/metal gate Ge-based MOSFETs has already been established. In 2002, Shang *et al*. reported a Ge *p*-MOSFET with a thin GeO_xN_y and low-temperature oxide (LTO) gate stack on a bulk Ge substrate, demonstrating 40% hole mobility enhancement over Si and an EOT of 80 Å [21]. In the same year, Chui *et al*. reported mobility-enhanced Ge *p*-MOSFETs with ultra-thin (6-10Å) ZrO_2 dielectrics fabricated by UV ozone oxidation of sputtered Zr [19]. In the following year (2003), Bai *et al*. reported low-leakage MOS capacitors on Ge substrates with an EOT of 13 Å formed by rapid thermal treatment of the Ge surface in NH_3 followed by *in situ* rapid thermal CVD of HfO_2 [25].

An important finding in the recent literature on Ge MOSFETs is the effectiveness of using thin GeO_xN_y as a surface passivation layer for subsequent high-κ deposition [25, 69-73]. For example, the study by Bai *et al*. showed that the formation of a GeO_xN_y passivation layer by rapid thermal annealing in NH_3 prior to HfO_2 deposition reduced the leakage current in MOS capacitors from 150 mA/cm^2 to 6 mA/cm^2 and lowered the EOT by a factor of two [25]. Van Elshocht *et al*. attributed the improved electrical performance and lower EOTs of nitrided devices to reduced updiffusion of Ge or GeO into the HfO_2 layer, prevention of HfO_2 epitaxy, and significantly reduced interfacial layer thickness [71]. The main drawback of the use of GeO_xN_y as a passivating layer is that large interface trap densities and large flat band voltage shifts have been observed in the capacitance-voltage characteristics [72]. This disadvantage has led researchers to explore other passivation layers for improving the Ge/high-κ interface, including epitaxial Si [73], plasma-PH_3/AlN [74], and sulfur [75].

As will be seen in the next section, much progress has been made toward integrating Ge epitaxial layers on Si, which is a necessary hurdle for incorporating Ge in CMOS processing. The integration challenges that still remain for Ge are demonstrating superior short-channel characteristics and reducing external device resistance. Short-channel characteristics are just beginning to emerge in the research literature [73, 76]. High external resistance, presumably due to poor dopant activation, has been blamed for the inferior performance of Ge *n*-MOSFETs [77].

1.4 APPROACHES FOR INTEGRATING GERMANIUM ON SILICON

1.4.1 Heteroepitaxial Growth of Germanium on Silicon

In an effort to make Ge transistor channels compatible with Si-based technologies, novel methods have been developed that attempt to integrate Ge epitaxial layers on Si wafers. Germanium has a 4% larger lattice parameter than Si, which makes high-quality Ge layers on Si difficult to prepare due to large lattice mismatch (a_{Ge} = 5.658 Å; a_{Si}=5.431 Å). The lattice mismatch causes biaxial compression in the plane of growth, resulting in a tetragonally-distorted lattice, as shown in Fig. 1.3(a). For a fully-compressively-strained epitaxial layer that has not undergone relaxation, the in-plane lattice parameter ($a_{\|}$) conforms to the substrate, and the out-of-plane lattice parameter ($a_{\perp}$) is stretched out in the growth direction. Thus, for a compressively-strained film, $a_{\|}$ is smaller than the relaxed lattice parameter (a_r), and $a_{\perp}$ is larger. In the case of tensile stress, the epitaxial layer has a smaller relaxed lattice parameter than the substrate, so the film undergoes biaxial tension, i.e. $a_{\|}$ is larger than a_r and $a_{\perp}$ is smaller. The relationship between the relaxed lattice parameter a_r, the out-of-plane lattice parameter $a_{\perp}$, and the in-plane lattice parameter $a_{\|}$ is given by

$$a_{\perp} - a_r = -2\nu\left(a_{\parallel} - a_r\right), \tag{1.3}$$

where ν is the Poisson's ratio for the material. The schematic diagram in Fig. 1.3(a) shows the tetragonal distortion in a compressively-strained epitaxial film deposited on Si. As a strained epitaxial film grows thicker, the strain energy builds, and eventually the strain energy is relieved through the formation of dislocations or changes in the surface morphology. The thickness below which the epitaxial layer remains fully strained is

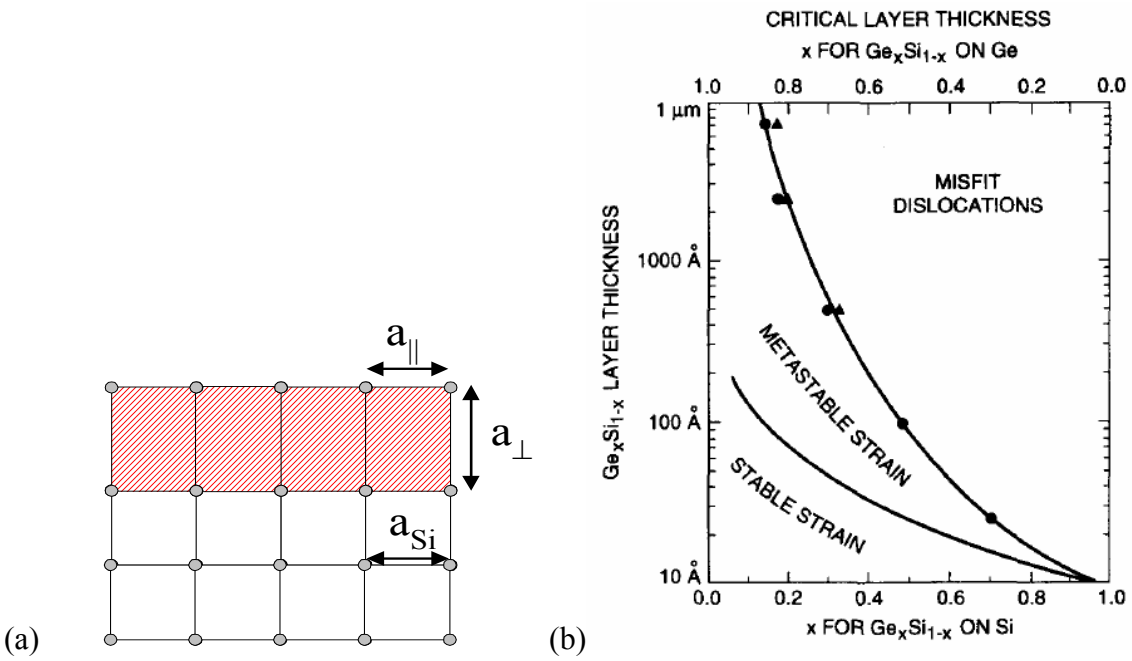


Figure 1.3. (a) Diagram showing the tetragonal distortion of a compressively-strained epitaxial layer grown on Si, where $a_{\parallel}$ and $a_{\perp}$ correspond to the in-plane and out-of-plane lattice parameters, respectively. (b) Plot of the critical layer thickness (t_{crit}) for $Si_{1-x}Ge_x$ deposited on Si, as a function of the Ge mole fraction, as given by Bean [78].

called the critical thickness, or t_{crit}. Figure 1.3(b) shows the dependence of t_{crit} on the Ge mole fraction for $Si_{1-x}Ge_x$ deposited on Si, as given by Bean [78]. The "stable strain" region shown in Fig. 1.3(b) corresponds to strained layer configurations that are in their lowest energy state, for which dislocations will not form. The "metastable strain" region corresponds to strained layers that are grown at low temperatures, for which dislocations may not have formed during growth, but for which dislocations may form after subsequent thermal processing. For film thicknesses greater than those in the "metastable strain" region, dislocations will form to reduce the strain energy. As seen in Fig. 1.3(b), t_{crit} decreases rapidly as the Ge mole fraction increases, due to increasing lattice mismatch. For pure Ge grown directly on Si, t_{crit} is between 10-15 Å, corresponding to only a few monolayers of epitaxial growth [79].

Heteroepitaxial growth typically proceeds in one of three growth modes: Frank-van der Merwe (F-vdM), Volmer-Weber (V-W), and Stranski-Krastanow (S-K). Figure 1.4 is a schematic drawing showing these three types of growth. F-vdM growth is layer-by-layer, V-W is island growth, and S-K is layer-by-layer growth followed by the formation of islands. The model for Ge (and $Si_{1-x}Ge_x$) on Si is S-K [79], where the Ge grows in a monolayer fashion to a thickness of 10 to 15 Å above which dome-shaped islands start to form due to local elastic deformations that relax to reduce the lattice strain. The islanding effect can be suppressed by low growth temperature [80-82] or by the use of surfactants, such as As and Sb [83, 84].

1.4.2 Silicon-Germanium Graded Buffer Layer Method for Depositing Ge on Si

One of the most successful methodologies that has been demonstrated for integrating pure Ge or high-Ge-content $Si_{1-x}Ge_x$ layers on Si substrates is the graded buffer layer approach, pioneered by researchers at Bell Laboratories [85] and the

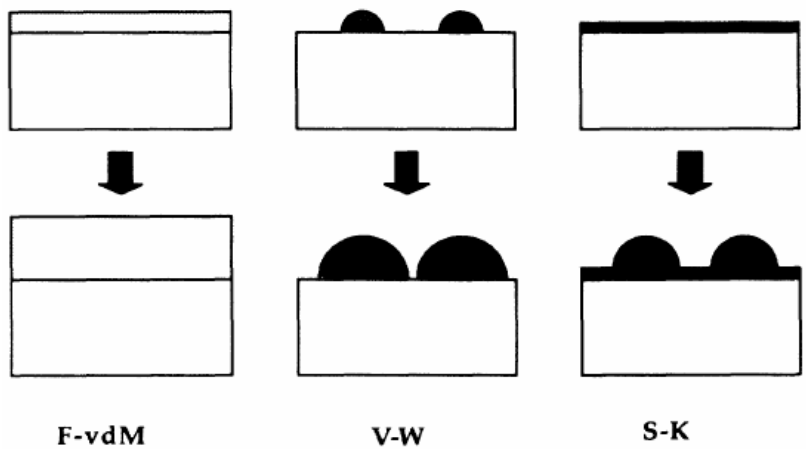


Figure 1.4. Schematic showing the three major heteroepitaxial growth modes: Frank-van der Merwe (F-vdM), Volmer-Weber (V-W), and Stranski-Krastanow (S-K) [79].

Massachusetts Institute of Technology [86]. In essence, the approach consists of accommodating the 4% lattice mismatch between Si and Ge in stages by depositing $Si_{1-x}Ge_x$ with gradually increasing Ge mole fraction. Figure 1.5(a) shows a schematic of the structure and growth conditions of a $Si_{1-x}Ge_x$ graded buffer heterostructure, as depicted by Currie *et al*. [86]. Strain relief is facilitated by threading dislocation glide. As film growth progresses, a characteristic cross-hatch surface roughness begins to appear which inhibits dislocation glide, and dislocation pileup occurs. To remove this impediment, a chemical mechanical polishing (CMP) step is performed to remove the cross-hatch roughness, and film growth is continued. When the process is finished, a relaxed high-Ge-content $Si_{1-x}Ge_x$ or pure Ge layer lies on the surface. For additional effective mobility enhancement in transistors, the top layer can be engineered to retain biaxial strain rather than being fully relaxed. The layer can be compressively-strained

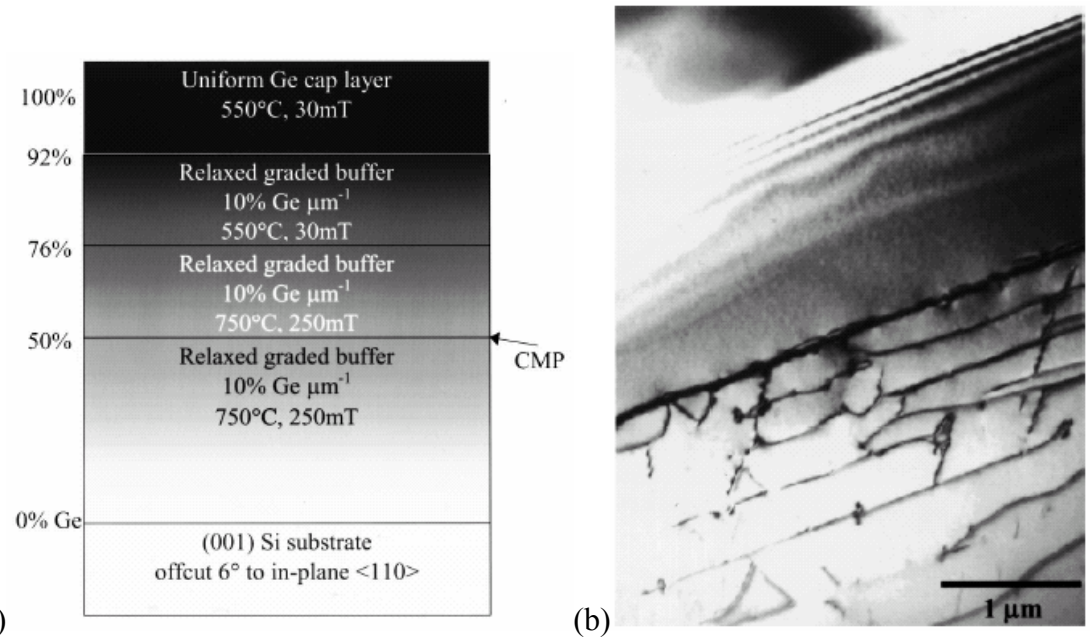


Figure 1.5. (a) Schematic of the structure and growth conditions for a $Si_{1-x}Ge_x$ graded buffer, including chemical mechanical polishing. (b) Cross-sectional transmission electron microscopy image of the upper portion of a $Si_{1-x}Ge_x$ graded buffer heterostructure, including the Ge cap layer [86].

Ge for hole mobility enhancement [23] or tensile-strained Si for electron mobility enhancement [88].

Since for device purposes the relaxed layers are nearly indistinguishable from a bulk wafer of the same material, the relaxed heterostructure is often referred to as a "virtual substrate." Figure 1.5(b) shows a cross-sectional transmission electron microscopy (TEM) image of the upper portion of a $Si_{1-x}Ge_x$ virtual substrate, including the pure Ge top layer. The threading dislocations are easily visible in this image, but we see that they do not thread to the surface, at least within the resolution of the TEM image. In reality, some threading dislocations do thread to the surface. Typical areal threading dislocation densities of these virtual substrates are on the order of 3×10^6 cm^{-2} [86].

The obvious disadvantage of the graded buffer layer approach is the intolerable process complexity, especially considering the call for a CMP step to remove surface roughness on the virtual substrate. To be incorporated into CMOS manufacturing, the virtual substrates would almost certainly have to be prepared by a separate entity outside of the wafer fab, and would need to be provided at a low enough cost to make them attractive to semiconductor manufacturing companies. Another disadvantage of graded buffer layers stems from the lower thermal conductivity of $Si_{1-x}Ge_x$. Figure 1.6 shows the thermal conductivity of $Si_{1-x}Ge_x$ alloy as a function of the Ge mole fraction at 300 K [88]. We see from Fig. 1.6 that the thermal conductivity of $Si_{1-x}Ge_x$ at 300 K is relatively constant for Ge content x between 0.3 and 0.8, but varies greatly for values typical of a $Si_{1-x}Ge_x$ virtual substrate ($0.15 \leq x \leq 0.5$) [88, 89]. As the Ge mole fraction is varied from bulk Si (x=0) to x=0.3, the thermal conductivity of $Si_{1-x}Ge_x$ decreases

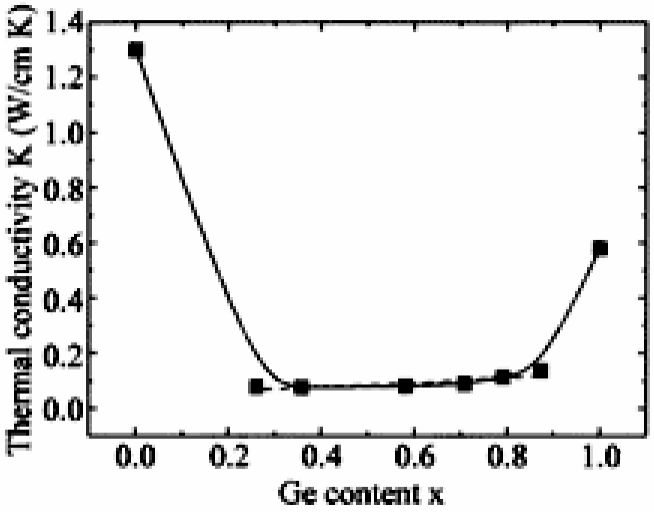


Figure 1.6. Thermal conductivity of $Si_{1-x}Ge_x$ as a function of the Ge mole fraction, as reported by Stohr and Klemm [88].

dramatically. Since the low thermal conductivity of the virtual substrate prevents heat conduction out of the transistor channel during operation, the device suffers from the "self-heating effect," which degrades the drive current [90, 91]. While it is true that the drive current degradation is only manifested during DC operation, the self-heating effect can also lead to a higher number of impact ionization events, which negatively affects the transistor reliability [92].

1.4.3 Additional Methods for Incorporating Ge on Si

Despite the success of the graded buffer layer approach for depositing low-defect-density Ge layers on Si substrates, many researchers have searched for alternative methods that reduce the epitaxial process complexity. Luan *et al*. showed that by depositing a thick Ge layer directly on Si with an initial low temperature phase and subjecting the wafer to a series of thermal annealing cycles, the threading dislocation density in the Ge films could be reduced to 2.3×10^{7} cm^{-2} [93]. A similar approach was investigated by Nayfeh *et al*. that used annealing in hydrogen to improve the crystal quality and surface roughness of the Ge layer [94]. Other methods employ abrupt changes in the Ge mole fraction during crystal growth to block defect propagation at heterojunction interfaces [95, 96].

One promising method shown by Hofmann's group at the University of Hannover involves the use of surfactants, such as As or Sb [83, 84]. The surfactant species is deposited on the surface of the wafer and drastically alters the strain relief mechanism of the Ge such that the dome-shaped islands consistent with the S-K growth mode do not appear. Strain relief is abrupt and confined near the interface with the Si substrate. Fig. 1.7 shows a bright-field TEM image of a 1-μm-thick Ge layer that was deposited

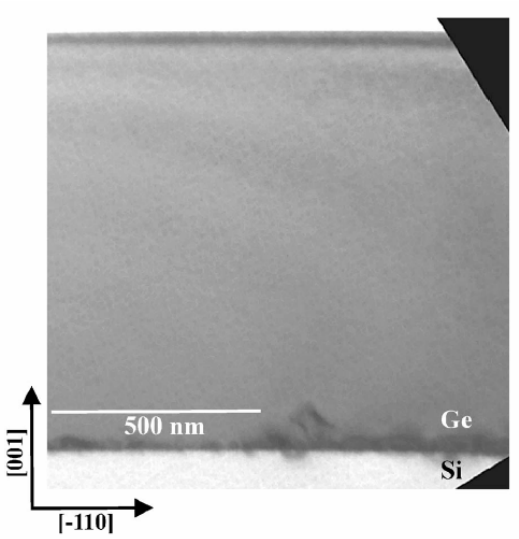


Figure 1.7. Bright-field TEM image of a 1-μm-thick Ge film deposited on Si using the surfactant-mediated epitaxy technique [84].

using Sb as a surfactant, as was shown by Wietler *et al*. [84]. In this figure, we see a highly-dense network of crystal defects that are confined near the Ge/Si interface, which is consistent with abrupt strain relief. While the surfactant-mediated technique has potential, it has only been demonstrated with molecular beam epitaxy (MBE) systems, which are not appropriate for high-volume manufacturing. Another disadvantage is of the technique is surfactant doping, which degrades the purity of the Ge layer.

Germanium-on-insulator (GOI) is another approach that combines the benefits of silicon-on-insulator (SOI) wafers and high-mobility strained Ge [97, 98]. GOI wafers are typically fabricated using the Ge condensation technique, depicted in Fig. 1.8 [97]. The process begins with a $Si_{1-x}Ge_x$-on-insulator (SGOI) substrate obtained using wafer bonding of an SOI wafer with a low-defect, relaxed $Si_{1-x}Ge_x$ layer obtained using the graded buffer technique (Fig. 1.8(a)). The SGOI wafer undergoes thermal oxidation

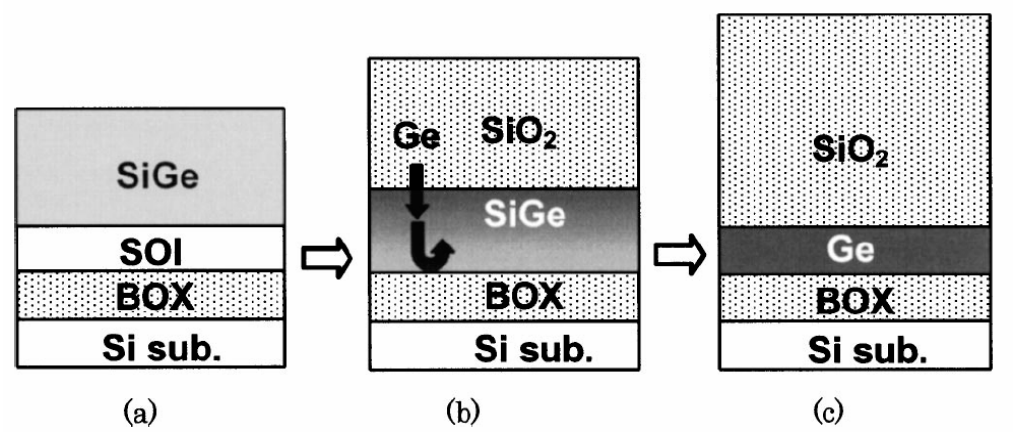


Figure 1.8. Schematic of the Ge condensation technique, which is used to fabricate Ge-on-insulator substrates [97].

(Fig. 1.8(b)), which enriches the Ge content in the $Si_{1-x}Ge_x$ layer as Ge atoms are rejected from the SiO_2. After the thermal oxidation is complete, the remaining substrate consists of a strained Ge layer lying directly on a buried oxide (Fig. 1.8(c)). Promising transistor performance has been demonstrated on GOI substrates [24, 99].

Besides Ge-channel CMOS applications, epitaxial Ge has promise in Si-compatible optoelectronics for infrared detection [100-102]. Moreover, since the lattice constants of Ge and GaAs are nearly equivalent, there is a lot of interest in integrating III-V materials on Si wafers using Ge virtual substrates [103, 104]. The prospects for optical integration becoming part of Si-based manufacturing seems very much coupled to the success of developing reliable methods for obtaining pristine-quality Ge-based layers on Si wafers.

1.5 CHAPTER ORGANIZATION

This chapter has presented a brief introduction to issues related to Ge MOSFET fabrication and integration. Since this dissertation focuses on MOS devices fabricated on germanium-carbon ($Ge_{1-y}C_y$) layers, the next chapter will be devoted to providing an overview of research related to $Ge_{1-y}C_y$. Chapter 3 will present findings on crystal growth and material properties of thin (> 35 nm) $Ge_{1-y}C_y$ layers prepared by ultra-high-vacuum chemical vapor deposition (UHV-CVD). In chapter 4, the transistor fabrication process for $Ge_{1-y}C_y$ MOSFETs will be given, and processing issues for $Ge_{1-y}C_y$ transistors will be discussed. Chapter 5 will present and discuss electrical data acquired from $Ge_{1-y}C_y$ *p*-MOSFETs fabricated on Si substrates, with and without a Si cap layer (i.e. buried-channel and surface-channel devices). Also included in chapter 5 will be a discussion of the effect of the Si cap layer thickness on the electrical properties of the buried-channel transistors. Chapter 6 will summarize the findings of this research and provide some concluding remarks.

CHAPTER 2

OVERVIEW OF GERMANIUM-CARBON LAYERS DEPOSITED ON SILICON SUBSTRATES

2.1 SILICON-CARBON AND SILICON-GERMANIUM-CARBON ALLOYS

2.1.1 Silicon-Carbon and Silicon-Germanium-Carbon Film Properties

Before addressing $Ge_{1-y}C_y$, it seems appropriate to first consider the work that has been done on binary silicon-carbon ($Si_{1-y}C_y$) and ternary silicon-germanium-carbon ($Si_{1-x-y}Ge_xC_y$) films, since historically they were the first to draw wide interest in the research literature. It has been well established that C atoms can be incorporated into $Si_{1-x}Ge_x$ to create metastable, ternary $Si_{1-x-y}Ge_xC_y$ films that show unique properties [105-118]. In chemical vapor deposition, for example, C can be incorporated into the $Si_{1-x}Ge_x$ epitaxial film by introducing a C-containing gaseous precursor such as methylsilane (CH_3SiH_3). Adding C to the film provides the following advantage: In strained $Si_{1-x}Ge_x$ films, the band gap is directly affected by the amount of strain, but in the ternary $Si_{1-x-y}Ge_xC_y$ system, strain and band gap can be controlled separately. In other words, C allows for independent engineering of band gap and strain [105, 112-117]. Estimates of the Ge-to-C ratio needed for perfect strain compensation in $Si_{1-x-y}Ge_xC_y$ range from 8:1 to 10:1 [105]. However, it is not clear that the C atoms need be in substitutional sites to provide strain compensation. It is thought that interstitial C reduces the strain energy of the film and increases its critical layer thickness [109-112]. In addition, recent work by Nitta *et al*. using Raman spectroscopy suggests that the

introduction of C into $Si_{1-x}Ge_x$ does not affect the local strain of Si–Si, Si–Ge, or Ge–Ge bonds, but rather reduces the overall average lattice constant of the film [118].

The developments with ternary $Si_{1-x-y}Ge_xC_y$ arose from studies that were done on the $Si_{1-y}C_y$ system [119], where tensile strain causes a lowering in the Δ_2 valleys and a raising of the HH and LH sub-bands, similar to the effect seen in strained Si on relaxed $Si_{1-x}Ge_x$ buffers [7]. The epitaxial growth challenges for $Si_{1-y}C_y$ prove difficult, however, due to the huge difference in the lattice parameter between C and Si. Whereas the lattice mismatch between Si and Ge is 4%, the lattice mismatch between Si and C is approximately 34%. The lattice parameter of diamond is about 3.56 Å, compared to 5.431 Å for Si [107]. Thus, large amounts of strain are incorporated in the crystal with small amounts of C. Another difficulty for $Si_{1-y}C_y$ is the small solid solubility of C in Si, which at the melting point of Si is only 3.5×10^{17} cm^{-3} [113, 120]. This is in contrast to the $Si_{1-x}Ge_x$ system in which Ge is completely miscible in Si. According to the binary phase diagram for Si and C, the only stable compound is stoichiometric silicon carbide (SiC). This means that $Si_{1-y}C_y$ alloys are inherently metastable, and that C will tend to precipitate out of solution with sufficient thermal energy [120]. Similar precipitation occurs in $Si_{1-x-y}Ge_xC_y$ alloys [115].

Fig. 2.1 shows a growth mode diagram for compounds containing Si and C, as given by Powell *et al*. [114]. The films for their study were grown by MBE, and the diagram is centered around a growth temperature of 500 °C. According to their methodology, at temperatures below 400 °C and for high C concentrations, twinning in the film leads to amorphous layers. At high temperatures and high C concentrations, the carbide phase dominates. Thus only a small window exists for the $Si_{1-y}C_y$ alloy phase, with the best results found between growth temperatures of 450 °C and 500 °C and small C concentrations. The precise boundaries for the diagram in Fig. 2.1 depend on the

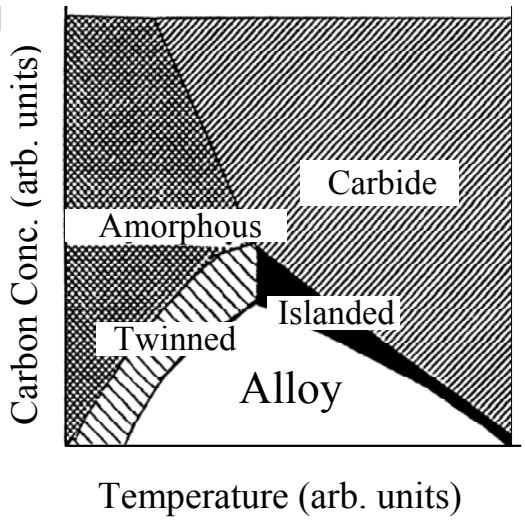


Figure 2.1. Diagram of the growth modes for $Si_{1-y}C_y$ films deposited by MBE and centered around a growth temperature of 500 °C [114].

growth method, but nearly all reports concur with the general pattern of low growth temperatures and small amounts of C [105-120].

2.1.2 Silicon-Carbon and Silicon-Germanium-Carbon MOSFET Applications

$Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ alloys have been shown to be useful in MOSFET applications, especially for engineering strain in the transistor channel. Given the recent trend in CMOS manufacturing of depositing $Si_{1-x}Ge_x$ layers in source and drain recesses to apply uniaxial compressive strain in the channel for *p*-MOSFET performance enhancement [14-15], it was only a matter of time before $Si_{1-y}C_y$ would be used for uniaxial tensile strain in *n*-MOSFETs [121-123]. Prior to these recent developments, however, biaxial-strained $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ layers were examined for direct use in the channel region rather than in the source and drain regions. Professor Banerjee's

group at the University of Texas was among the first to fabricate *p*-MOSFETs on $Si_{1-x-y}Ge_xC_y$ layers with enhanced performance [124, 125]. Quiñones *et al*. showed that biaxial-tensile-strained $Si_{1-y}C_y$ deposited directly on Si with a thin Si cap layer could be used for buried-channel *p*-MOSFETs with enhanced mobility [126]. Weber *et al*. demonstrated high-performance short-channel $Si_{1-x-y}Ge_xC_y$ *p*-MOSFETs with HfO_2 dielectrics and TiN metal gates [127]. Besides mobility enhancement, additional benefits of using C in the channel are reduced boron diffusion (which is important for achieving steep doping profiles in aggressively-scaled devices) [128], improved thermal stability [127, 129], and engineering of conduction and valence band offsets for carrier confinement using $Si/Si_{1-x-y}Ge_xC_y$ and $Si/Si_{1-y}C_y$ heterojunctions [130].

2.2 GERMANIUM-CARBON ALLOYS

2.2.1 Germanium-Carbon on Silicon Deposited by Molecular Beam Epitaxy

$Ge_{1-y}C_y$ initially drew interest in the research community for its potential as a lattice-matched system with Si capable of band gap engineering. Since C has an extremely low solid solubility in Ge ($<1\times10^{10}$ cm^{-3}) [131], the growth of $Ge_{1-y}C_y$ must be performed synthetically, under metastable conditions. The first $Ge_{1-y}C_y$ epitaxial layers were grown by MBE [132-139], and studies focused on growth kinetics, composition, structure, lattice constants, strain relaxation, C incorporation/precipitation, optical absorption, and band offsets. Most of these reports showed evidence for reduced lattice constant with higher C content, increased band gap compared to bulk Ge, and the ability to incorporate supersaturated levels of C despite the low solid solubility. A study by Osten *et al*. using *in situ* monitoring with reflection high-energy electron diffraction (RHEED) showed that the t_{crit} of MBE-grown $Ge_{1-y}C_y$ layers is between 10 and 20

monolayers, depending on the substrate temperature [137]. This is higher than the t_{crit} for pure Ge on Si [79, 137].

Relatively few studies have appeared in the research literature that examine the electrical and optoelectronic properties of $Ge_{1-y}C_y$ layers deposited using MBE. Shao *et al*. reported 1.3-μm photoresponsivity in *p*-$Ge_{1-y}C_y$/*n*-Si photodiodes with a reverse saturation current of about 10 pA/μm^2 at –1 V and high reverse breakdown voltage of up to –80 V [136]. The incorporation of C atoms gave a significant reduction in diode reverse leakage current, but the effects saturated with more C. The observation of higher forward turn-on voltages in addition to reduced reverse leakage currents was thought to be a result of an increased Ge band gap [140]. Band structure calculations and x-ray photoelectron spectroscopy (XPS) studies on $Si_{1-x-y}Ge_xC_y$ and $Ge_{1-y}C_y$ and seem to support this hypothesis [141-143].

2.2.2 Chemical Routes for Germanium-Carbon Layers on Silicon

While the MBE-grown $Ge_{1-y}C_y$ layers showed promising crystallinity and substantial C concentrations of up to 3 at. %, higher C concentrations were sought to reduce lattice mismatch and further increase the band gap. Assuming Vegard's law applies to the $Ge_{1-y}C_y$ system, a Ge to C ratio of 8.2:1 is necessary to produce lattice matching to Si. This corresponds to a C atomic concentration of 10.9 at. %, which has never been achieved with MBE. Given the difficulties of incorporating high concentrations of C in $Si_{1-y}C_y$ due to carbide precipitation (see Fig. 2.1) and the extremely low solid solubility of C in Ge, it may seem unlikely that $Ge_{1-y}C_y$ with concentrations above 5 at. % could be synthesized at all. Nevertheless, chemical routes have still been sought to increase the C concentration in the films to exceedingly high levels. The

tendency to form a carbide phase is not a problem in $Ge_{1-y}C_y$, since no hexagonal "GeC" crystal analogous to SiC has ever been synthesized or observed.

Prior to the work described in this dissertation, the only group that ever attempted to deposit $Ge_{1-y}C_y$ using chemical vapor deposition was Professor John Kouvetakis's group at Arizona State University [144-148]. Their approach was to develop novel precursors containing both Ge and C atoms that could be reacted with a Ge-only precursor (such as germane) to deposit $Ge_{1-y}C_y$ films at low temperature using ultra-high-vacuum chemical vapor deposition (UHV-CVD). The first major publication on their work appeared in *Applied Physics Letters* in 1996 by Todd *et al*. [144]. Motivated by the past successes of heteroepitaxial growth of $Si_{1-x-y}Ge_xC_y$ materials using silylmethanes such as methylsilane (CH_3SiH_3) and tetrasilylmethane ($C(SiH_3)_4$), they sought to utilize the analogous germylmethanes for depositing $Ge_{1-y}C_y$ layers. Their paper described the results of reacting methylgermane (CH_3GeH_3) and trigermylmethane ($HC(GeH_3)_3$) with germane (GeH_4) in a custom-built, hot-wall UHV-CVD reactor to form high-crystal-quality $Ge_{1-y}C_y$ with C concentrations ranging from 1.5 to 5 at. %.

The advantage of these precursors was said to be the existence of "pre-formed" Ge–C bonds that would make substitutional C incorporation into Ge more thermodynamically favorable. However, given the weak Ge–C bond strength compared to the C–H bond [149-151], one might suspect that the reaction pathway would favor the dissociation of the Ge–C bonds in the gas phase before C gets incorporated into the $Ge_{1-y}C_y$ epitaxial layer. Curiously, it was reported by Todd *et al*. that the CH_3GeH_3 precursor did not dissociate up to a temperature of 800 °C, but that reaction with GeH_4 occurred instantly at only 470 °C [144]. An argument in favor of substitutional C in Ge is that the dissociation energy of the Ge–C bond (4.7 eV) is higher than that of the Si–C bond (2.8 eV), so if C can be incorporated into substitutional sites in Si than it should

also be incorporated into Ge [149]. Complicating the matter further, though, is the fact that the Ge–C bond length in molecular compounds is only 1.9 Å, which is much shorter than the Ge–Ge bond length of 2.41 Å [149]. This means that very high strain fields would exist around individual C atoms, making substitutional C in Ge less energetically favorable [149].

Despite these uncertainties, the group at Arizona State University found experimentally that the reaction of germylmethanes with GeH_4 yielded acceptable- to good-quality $Ge_{1-y}C_y$ crystals with high C concentrations. Higher C concentrations were obtained using the higher order precursors containing more Ge–C bonds. Figure 2.2 shows two cross-sectional TEM images of $Ge_{1-y}C_y$ layers deposited directly on Si wafers using CH_3GeH_3 and $HC(GeH_3)_3$ precursors [144]. The image in Fig. 2.2(a) shows the $Ge_{1-y}C_y$/Si interface of a $Ge_{1-y}C_y$ layer with a C concentration of 1.5 at. % deposited with

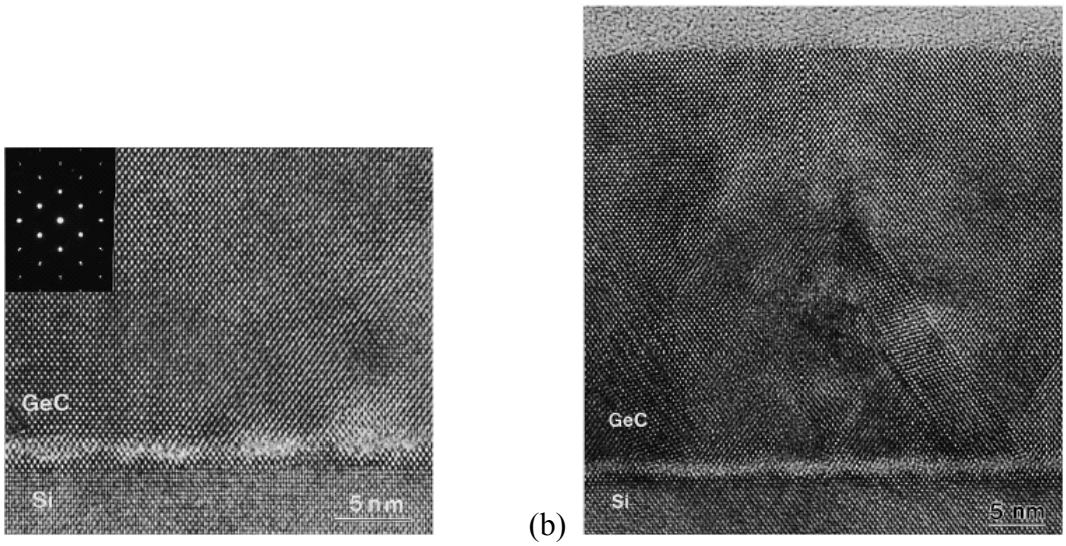


Figure 2.2. (a) Cross-sectional TEM image of $Ge_{1-y}C_y$ containing 1.5 at. % C deposited using the reaction of CH_3GeH_3 with GeH_4 at 470 °C. The inset shows the selected-area electron diffraction pattern [144]. (b) Cross-sectional TEM image of $Ge_{1-y}C_y$ containing 4.5 at. % C deposited with $HC(GeH_3)_3$ [144].

CH_3GeH_3. Stacking faults and twin defects were detected near the interface which did not persist to the surface. Fig. 2.2(b) shows a higher-C-concentration layer (4.5 at. %) deposited with $HC(GeH_3)_3$. The main difference that is immediately apparent is that the higher-concentration layer has a higher number of defects near the interface, which appear to be {111} stacking faults. Rutherford backscattering (RBS) channeling experiments confirmed the trend of higher defect densities for higher C concentrations [148]. Although the reason for this trend was never stated, one hypothesis is that the higher C concentration and the associated high strain fields surrounding individual C atoms has weakened the lattice sufficiently to make the appearance of stacking faults more favorable.

No electrical device results were ever reported on the $Ge_{1-y}C_y$ layers prepared by chemical vapor deposition. The primary focus of the research at Arizona State University was the search for novel ways of increasing the C concentration so as to match the lattice parameter of bulk Si. While this seems like a worthy goal, based on the published results it is unclear whether such high concentrations (10.9 at. % for lattice matching with Si) can ever be realized with low defect densities. The research has implications for Ge-channel MOSFETs, however, as will be seen in the subsequent chapters of this dissertation. Thin (< 35 nm) $Ge_{1-y}C_y$ layers with low C concentrations (from 0.5 to 1 at. %) can be used to fabricate high-channel-mobility transistors directly on Si without the need for buffer layers or thermal annealing.

2.3 SUMMARY

This chapter has provided an overview of crystal growth, materials properties, and device applications of $Si_{1-y}C_y$, $Si_{1-x-y}Ge_xC_y$, and $Ge_{1-y}C_y$ alloys to establish the proper

backdrop for the experimental results that follow in the remaining chapters of this dissertation. Carbon affects both the strain and band structure of heteroepitaxial films deposited on Si substrates, making it an attractive implement in MOSFET applications for engineering the channel. $Ge_{1-y}C_y$ films have been deposited using both MBE and CVD techniques, but very few electrical results have been reported. The next chapter will describe the growth conditions that were used for the thin $Ge_{1-y}C_y$ layers used in this work as well as provide further insights into the growth kinetics and film properties.

CHAPTER 3

EXPERIMENTAL RESULTS OF THE MATERIAL PROPERTIES OF THIN GERMANIUM-CARBON LAYERS ON SILICON

3.1 GERMANIUM-CARBON GROWTH METHOD

The $Ge_{1-y}C_y$ layers in this research [152-154] were deposited using a custom-built cold-wall UHV-CVD system installed at the Microelectronics Research Center at the University of Texas at Austin. As it is a cold-wall system, it is different from the conventional hot-wall UHV-CVD systems that were pioneered by Meyerson [155]. It consists of a load lock and a process chamber that are constructed of low-C-containing stainless steel with copper metal flanges for achieving an ultra-high-vacuum seal from the external environment. The load lock chamber exists as a buffer to the process chamber to prevent its exposure to atmosphere during wafer transfer. During wafer loading, a nitrogen-purged glove box is placed over the loading door and the load lock itself is continuously purged with high-purity nitrogen. After loading the wafers, the nitrogen purge is turned off and the load lock is roughed down to 200 mTorr using a liquid-nitrogen-based sorption pump. The load lock is then pumped for an hour or more with a turbomolecular pump to reduce the load lock pressure to the 10^{-7} Torr range before transferring wafers from the load lock chamber to the process chamber. The walls of the process chamber are streamed with cooling water to maintain a wall temperature of 40 °C to reduce the out-gassing of contaminants during growth. A high-volume turbomolecular pump is attached to the process chamber that maintains a base pressure between 5×10^{-10} and 1×10^{-9} Torr between depositions. All of these measures are critical for reducing the

partial pressures of water vapor and oxygen in process chamber. Reduced levels of water vapor and oxygen are essential to the UHV-CVD epitaxial deposition process, since low growth temperatures are used. At low growth temperatures, H_2O and O_2 contaminants are easily incorporated into the films, which is disastrous for the crystal quality [156].

Methylgermane (CH_3GeH_3) and germane (GeH_4) precursors were used for the $Ge_{1-y}C_y$ film deposition. The CH_3GeH_3 precursor was a 10% mixture diluted in He, and the GeH_4 was a 40% mixture in He. The flow rates and gas ratios were regulated using calibrated mass flow controllers. The typical starting substrates were 100 mm *n*-type Si (100) wafers with a resistivity of 1-10 Ω·cm. Before inserting the substrates into the UHV-CVD system, the wafers were cleaned in a 2:1 H_2SO_4:H_2O_2 piranha solution followed by a 40:1 deionized H_2O:HF dip for 30 seconds to remove the chemical oxide and leave the surfaces hydrophobic. The wafers were then immediately inserted into the load lock chamber, which was pumped down to below 10^{-6} Torr before loading into the process chamber. The base pressure of the process chamber before deposition was typically below 7.0×10^{-10} Torr. Before depositing the $Ge_{1-y}C_y$ layer, a Si buffer layer was grown. To begin the growth sequence, disilane (Si_2H_6) gas was introduced at a low flow rate until the Si buffer layer temperature of 650 °C was reached. Immediately following the Si buffer layer, while continuing to flow Si_2H_6, the temperature was lowered to between 400 and 450 °C. The Si_2H_6 was then turned off and the CH_3GeH_3 and GeH_4 precursors were introduced. The GeH_4 was introduced into the reactor at a flow rate of 10 sccm, and the CH_3GeH_3 was flown at rates between 0.7 and 1.2 sccm. The deposition pressure for the $Ge_{1-y}C_y$ layer was controlled at 5 mTorr. It was noticed that at 450 °C the $Ge_{1-y}C_y$ growth rate depended strongly on the amount of C incorporated into the film. As the C content increased from pure Ge (no CH_3GeH_3 flow) to about 1% C (1.2 sccm CH_3GeH_3 flow), the growth rate decreased from 10 Å/min to 1.7 Å/min. This lowering

of the growth rate is likely due to the presence of strong C–H bonds lying on the wafer surface that lead to a small increase in surface hydrogen coverage and reduce the sticking probability of GeH_4 [157]. For the experiments that utilized a thin Si cap layer on top of the $Ge_{1-y}C_y$ (see chapter 5) the temperature was raised to 550°C and a cap layer was deposited using Si_2H_6.

3.2 SURFACE ROUGHNESS, CRYSTALLINITY, DEFECT DENSITY, AND STRAIN

This section will discuss the quality of the thin $Ge_{1-y}C_y$ films grown using the UHV-CVD method described above. Atomic force microscopy (AFM) was used to measure the influence of C on the root-mean-square (RMS) surface roughness of the as-grown layers. A modified etch pit density (EPD) method was used to acquire a rough estimate of the threading dislocation density. Qualitative crystallinity and layer smoothness was evaluated by transmission electron microscopy (TEM), scanning electron microscopy (SEM), and ellipsometry. Reciprocal space mapping using x-ray diffraction (XRD) was used to determine strain. With the exception of the AFM samples described in the first subsection below, all of the $Ge_{1-y}C_y$ layers reported in this section were grown with the same CH_3GeH_3:GeH_4 flow ratio. However, the C concentration was not measured. (A discussion of the C concentration profile in $Ge_{1-y}C_y$ will be given later.)

3.2.1 Influence of Carbon on the Surface Roughness

3.2.1.1 Atomic Force Microscopy

Figure 3.1(a) shows a plot of RMS surface roughness measurements acquired on $Ge_{1-y}C_y$ films as a function of the CH_3GeH_3:GeH_4 flow ratio for two growth temperatures, 550 °C and 430 °C. From Fig. 3.1(a) we see that higher amounts of C (based on the

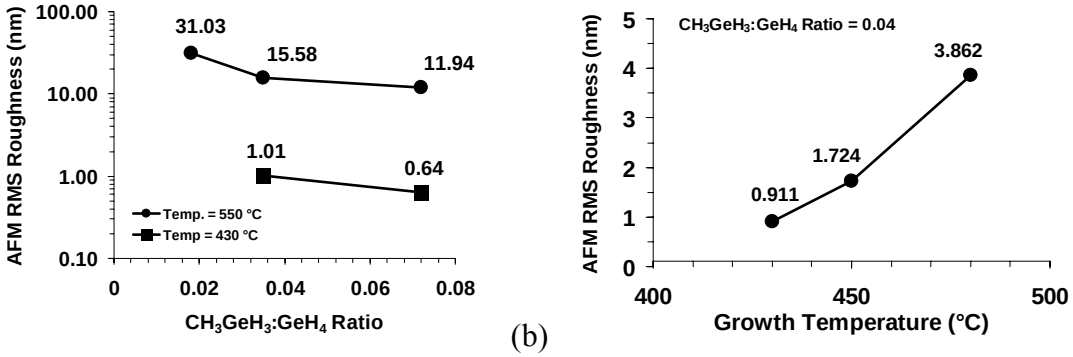


Figure 3.1. (a) RMS surface roughness measured by AFM of $Ge_{1-y}C_y$ films on Si with increasing GeH_4:CH_3GeH_3 ratios at growth temperatures of 500 °C (solid circles) and 430 °C (solid squares). (b) Surface roughness with increasing growth temperature for a fixed GeH_4:CH_3GeH_3 flow ratio.

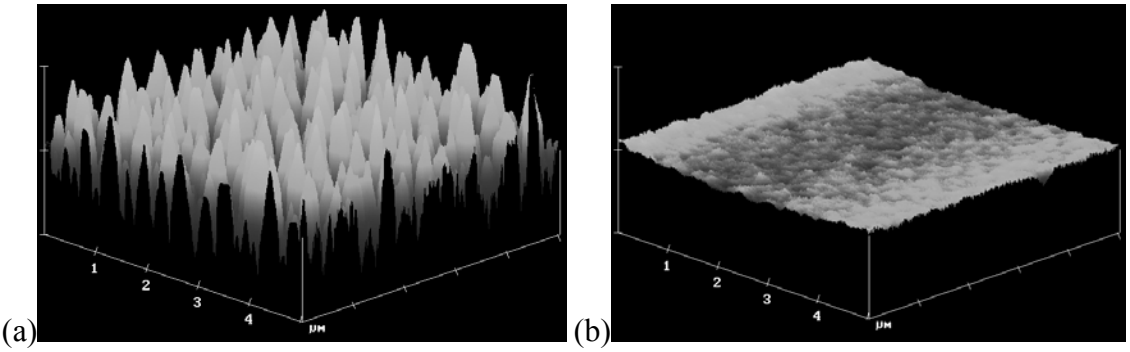


Figure 3.2. AFM surface plots of $Ge_{1-y}C_y$ films grown at two different temperatures with the same CH_3GeH_3:GeH_4 gas flow ratio. (a) $Ge_{1-y}C_y$ on Si grown at 550 °C, showing a high RMS roughness of 30 nm. (b) Film grown at 430 °C, showing an RMS roughness of only 0.32 nm.

CH_3GeH_3:GeH_4 gas flow ratio) lead to smoother films. We also see that the growth temperature drastically affects the roughness. The films grown at 550 °C (solid circles) were extremely rough compared to the films grown at 430 °C (solid squares). The effect of the growth temperature is seen even more clearly in Fig. 3.1(b), which is a plot of the surface roughness of $Ge_{1-y}C_y$ layers with a fixed CH_3GeH_3:GeH_4 flow ratio and the

growth temperature on the *x* axis. An increase in the growth temperature from 430 °C to 480 °C resulted in the surface roughness increasing from 0.9 nm to 3.9 nm. Figure 3.2 shows AFM surface plots acquired from a 5 μm × 5 μm measurement window for layers grown at 550 °C (Fig. 3.2(a)) and 430 °C (Fig. 3.2(b)). The film grown at 550 °C shows a high roughness of 30 nm, while the film grown at 430 °C shows a roughness of only 0.32 nm. From these AFM results we conclude that the smoothness of the $Ge_{1-y}C_y$ has a much stronger dependence on the growth temperature than on the C concentration, but that the C concentration is not a negligible variable. It was also observed that for a given growth temperature and CH_3GeH_3:GeH_4 flow ratio, the layer thickness did not appear to affect the surface roughness (up to a thickness of 100 nm). This means that thickness variations in these AFM samples should not have affected the results.

3.2.1.2 Scanning Electron Microscopy

Several characterization methods were used to compare the $Ge_{1-y}C_y$ film quality to that of pure Ge (no CH_3GeH_3 flow) to see the effect of C on the surface morphology and crystallinity. The pure Ge layers were grown using a similar method as described in section 3.1 except that no CH_3GeH_3 was flown, the deposition pressure was increased to 12 mTorr rather than 5 mTorr, and the growth temperature was lowered to about 380 °C. The lower temperature and slightly higher pressure for pure Ge epitaxy was required for a best-case comparison. The $Ge_{1-y}C_y$ could have been grown at 380 °C as well, but the growth rates were intolerably low at that temperature.

Figure 3.3 presents a qualitative comparison of the surface morphology for pure Ge and $Ge_{1-y}C_y$ growth on Si. Figure 3.3(a) shows a tilt-view SEM and a cross-sectional view (inset) of a 20-nm, selectively-deposited pure Ge layer grown directly on Si inside

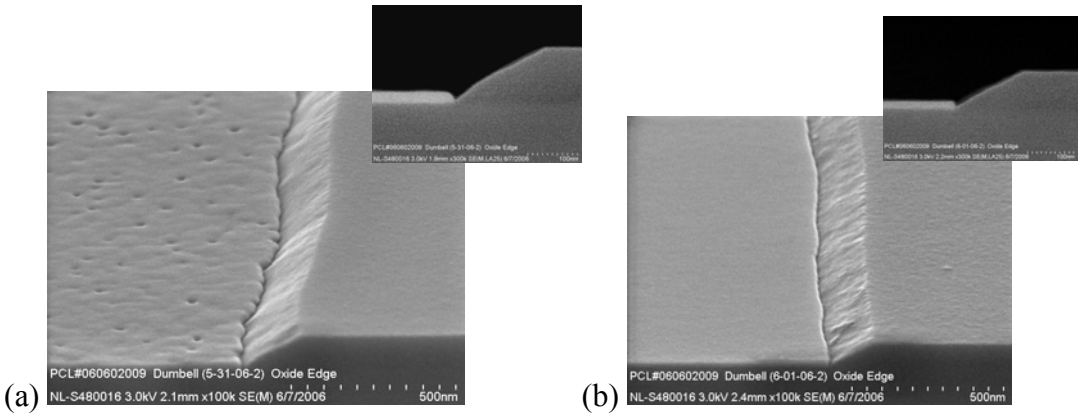


Figure 3.3. (a) Tilt-view and cross-sectional (inset) SEM images of a 20-nm pure Ge layer grown selectively in an SiO_2 window on Si. (b) Corresponding images for a $Ge_{1-y}C_y$ layer with comparable film thickness.

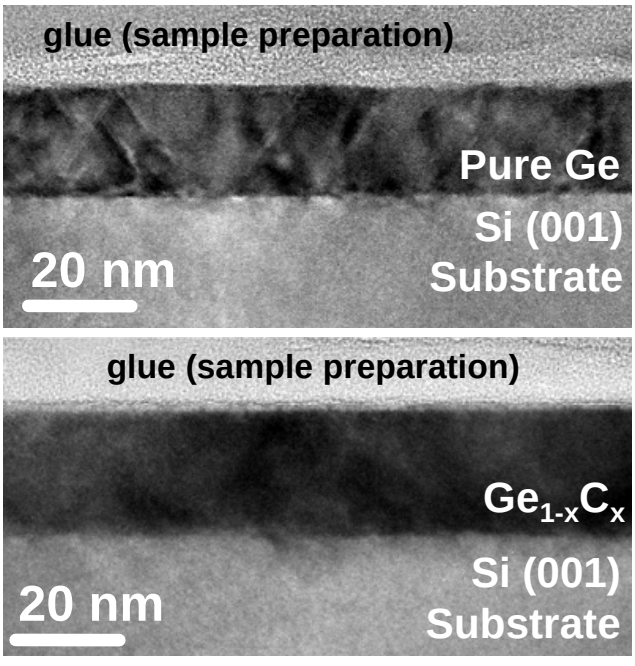
wet-etched SiO_2 windows. The figure shows the interface of the epitaxial Ge and the oxide edge. Figure 3.3(b) shows the corresponding images for a $Ge_{1-y}C_y$ layer of comparable film thickness. We see that the surface morphology for the pure Ge layer is markedly different, with greater roughness, pitting, and severe faceting at the oxide edge. This is a result of dome-shaped islands (consistent with the S-K growth mode) that have coalesced to form these features. In contrast, the $Ge_{1-y}C_y$ layer appears to be perfectly smooth with very little faceting. These SEM images are clear evidence of the dramatic influence that C incorporation has on the Ge film quality.

3.2.2 Defect Density

3.2.2.1 Transmission Electron Microscopy

Figure 3.4 shows a comparison of cross-sectional transmission electron microscopy images taken from $Ge_{1-y}C_y$ and pure Ge layers on Si with comparable film thicknesses. From Fig. 3.4(a) we see that the pure Ge layer shows a large number of

stacking faults and threading dislocations, whereas the $Ge_{1-y}C_y$ in Fig. 3.4(b) shows no threading dislocations (within the resolution limits). It is apparent in Fig. 3.4(b), however, that misfit dislocations are forming at the interface with the Si substrate, none of which thread toward the surface. It is thought that the high strain fields around individual C atoms cause significant retardation of dislocation glide, which confines defects at the interface with the Si substrate [111]. It is also possible, yet not confirmed at present, that SiC precipitates are forming near the $Ge_{1-y}C_y$/Si substrate interface. Osten *et al*. reported that the precipitation of SiC nanocrystals or other C-containing interstitial complexes is a mechanism for strain relaxation in tensile-strained $Si_{1-y}C_y$ and in $Si_{1-x-y}Ge_{1-y}C_y$ [158]. Further discussion on strain relaxation will be given in subsequent sections of this chapter.



(a)

(b)

Figure 3.4. Cross-sectional transmission electron microscopy images for (a) pure Ge and (b) $Ge_{1-y}C_y$ layers on Si with comparable film thickness.

3.2.2.2 Etch Pit Density

Conventional etch pit density (EPD) measurements for calculating threading dislocation densities cannot be used for very thin films (<50 nm). The EPD etching solutions found in the literature [93, 159, 160] preferentially etch defects, but they also exhibit a substantial etch rate for the film itself. If such an etch solution is used on a very thin film, the entire film is etched away before the etch pits can be resolved under a microscope. Nevertheless, EPD is one of the few techniques capable of calculating the area density of threading dislocations. In order to use EPD with very thin $Ge_{1-y}C_y$ films, a modified etch pit solution was used in conjunction with AFM. The solution contained 1000 mL CH_3COOH, 70 mL HNO_3, and 4.5 mL HF. This solution preferentially etched threading dislocations, and the remainder of the film etched at a rate of 10-20 Å/sec. The etch pits were small, but could easily be located using AFM in a 30 μm × 30 μm measurement window. Figure 3.5(a) shows an AFM scan of a 30-nm-thick, defect-etched $Ge_{1-y}C_y$ layer on Si. A zoomed view of one of the etch pits is shown in Fig. 3.5(b). The etch pit shown in Fig. 3.5(b) appeared to be roughly square shaped with a side length of about 200 nm. Three etch pits were located within the 30 μm × 30 μm window of Fig. 3.5(a), which would correspond to an EPD of 3.0×10^5 cm^{-2}. While this EPD technique has a statistical weakness based on the relatively small area of the measurement window, this was the highest number of etch pits that were discovered in any of the AFM scans that were performed. Thus 3.0×10^5 cm^{-2} was considered an "upper limit" for the EPD. (For larger area scans, the etch pits were too small to detect.) Pure Ge layers measured by the same method had an EPD of 2.1×10^8 cm^{-2}, which seems consistent with published reports [93]. A control measurement on a bulk Ge wafer

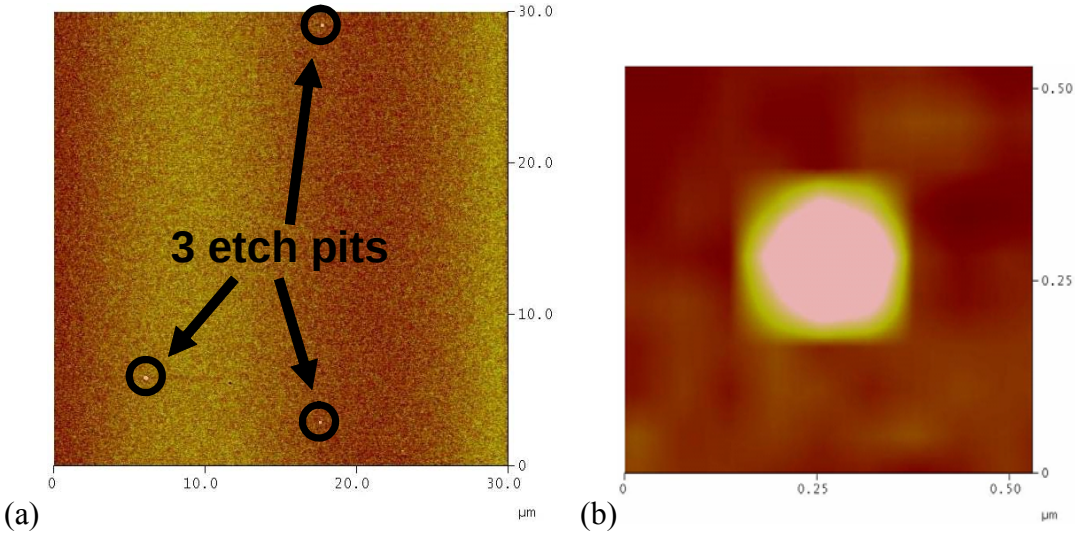


Figure 3.5. (a) AFM image of a 30-nm-thick, defect-etched $Ge_{1-y}C_y$ layer on Si acquired in a 30 μm × 30 μm measurement window. The etch pits are indicated by the arrows. (b) Zoomed view of one of the etch pits in (a). The etch pit appears to be roughly square shaped with a side length of about 200 nm.

revealed no etch pits. Within the statistical limitations of this EPD technique, it was concluded that the $Ge_{1-y}C_y$ layers had nearly three orders of magnitude improvement in the threading dislocation density over pure Ge films with comparable film thickness.

3.2.3 Strain Relaxation Measured by X-ray Diffraction

Triple-axis x-ray diffraction (XRD) was used to characterize strain relaxation in the $Ge_{1-y}C_y$ layers. Reciprocal space maps were measured over the (004) and (224) reflections with rotation around the sample normal to eliminate error due to epitaxial tilt. One of the maps measured around the (224) reflection is shown in Fig. 3.6 for a 30-nm-thick $Ge_{1-y}C_y$ layer on Si. It is clear that the $Ge_{1-y}C_y$ layer is mostly relaxed, based on the position of the peak relative to the dashed line in the figure, which corresponds to

the (224) planes in reciprocal space. By measuring the position of the $Ge_{1-y}C_y$ peak in reciprocal space, the in-plane ($a_{\|}$) and out-of-plane ($a_{\perp}$) lattice constants were determined. The value for $a_{\perp}$ was 5.679 Å, compared to a uniform lattice constant of 5.658 Å for fully-relaxed Ge. The value of $a_{\|}$ was 5.598 Å. The Poisson's ratio for Ge was used to calculate the relaxed lattice constant (a_r) of the $Ge_{1-y}C_y$ (with the assumption that the Poisson's ratio deviates little from the value for pure Ge for very low levels of C). The value of a_r for the $Ge_{1-y}C_y$ was 5.643 Å, which, when compared with the measured $a_{\|}$ and $a_{\perp}$, shows that the film is 78% relaxed. Since very few threading dislocations were found in these films, it is believed that abrupt strain relaxation occurs near the $Ge_{1-y}C_y$/Si interface. The residual compressive strain that is still present in the layer is beneficial for *p*-MOSFET mobility enhancement.

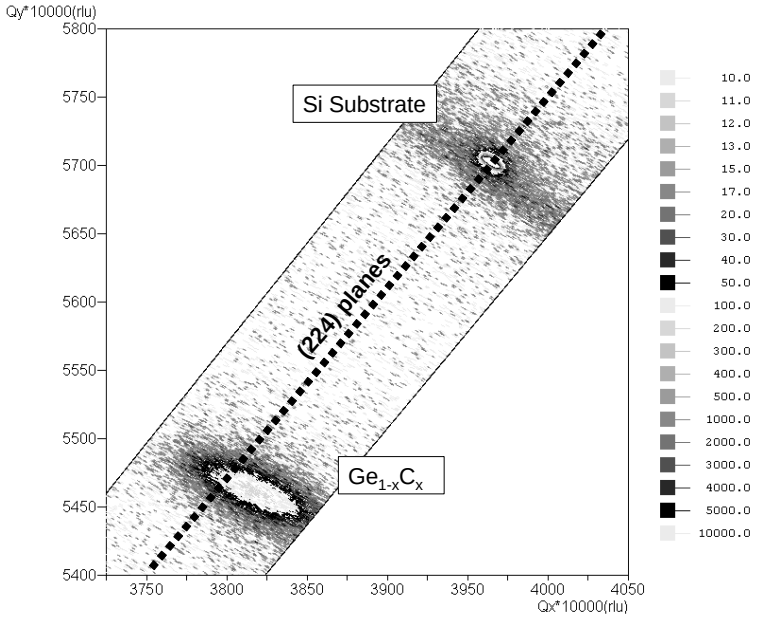


Figure 3.6. X-ray diffraction reciprocal space map of the (224) reflection for a 30-nm-thick $Ge_{1-y}C_y$ layer on Si. The dashed line corresponds to the (224) planes in reciprocal space.

3.3 GERMANIUM-CARBON GROWTH KINETICS

The kinetics of $Ge_{1-y}C_y$ growth by UHV-CVD differ significantly from that of pure Ge. As mentioned earlier, pure Ge on Si exhibits a Stranski-Krastanow (S-K) growth mode [79], which means that it grows in a layer-by-layer fashion, followed by three-dimensional island formation to relieve strain (see also Fig. 1.4). The defect-free Ge islands are roughly spherical or dome-like because the reduction in the strain energy exceeds the increase in the surface energy (surface area). When these spherical or dome-like islands coalesce, a continuous layer with a non-uniform film thickness is formed. The undulated surface results in a relatively rough surface morphology, as in Fig. 3.3(a). In contrast, our observations suggest that the $Ge_{1-y}C_y$ islands are truncated

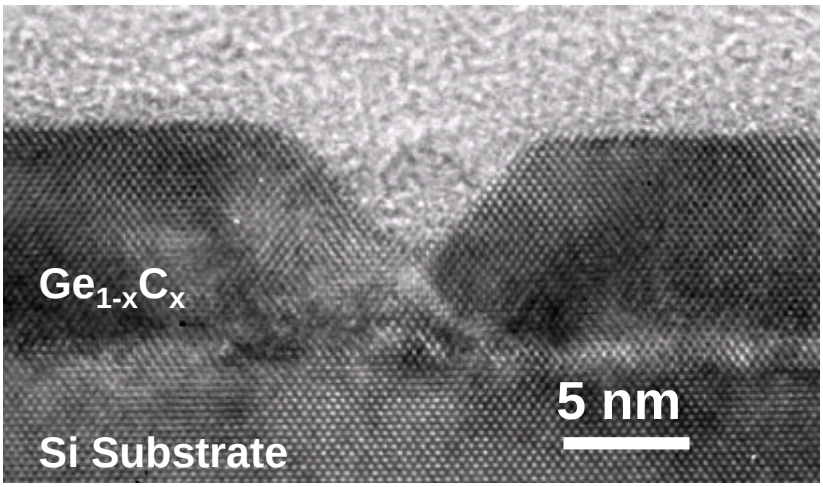
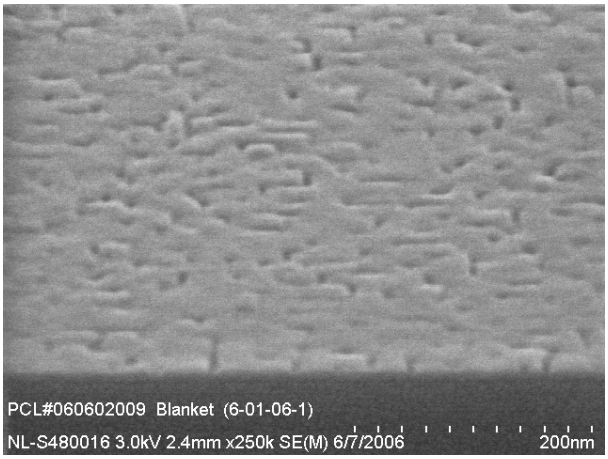


Figure 3.7. High-resolution cross-sectional TEM image of a $Ge_{1-y}C_y$ layer in the early stages of growth, before complete S-K island coalescence. In this image, we see what appears to be a triangular well in a 10-nm-thick $Ge_{1-y}C_y$ layer, which is postulated to be a result of two truncated-pyramid-shaped S-K islands that have coalesced to form this feature.

pyramids with a (001) top facet. Figure 3.7 shows a high-resolution cross-sectional TEM image of a $Ge_{1-y}C_y$ layer in the early stages of growth, before complete S-K island coalescence. In this image, we see what appears to be a triangular well in a 10-nm-thick $Ge_{1-y}C_y$ layer. We believe that this is the result of two truncated-pyramid-shaped S-K islands that have coalesced to form this feature. (Further analysis of films grown for shorter times would be required to verify this hypothesis.) A tilt-view SEM image of the same sample shown in Fig. 3.7 is shown in Fig. 3.8(a). Here we see that the triangular "wells" resulting from $Ge_{1-y}C_y$ island coalescence are crystallographic in nature, and are oriented along orthogonal directions. This is different from the more random pitting that is observed when dome-like pure Ge islands coalesce, as shown in Fig. 3.8(b). The films shown in the SEM images of Fig. 3.8 have comparable thicknesses and were grown under similar conditions, with the exception of the C incorporation and slightly different growth temperature and pressure (see section 3.2.1.2).

It has been shown that S-K growth in the $Si_{1-x}Ge_x$/Si system can result in either dome-shaped or truncated pyramids depending on the growth conditions [161, 162]. Since truncated pyramids are favored when misfit dislocations are the main catalyst for strain energy reduction [161], we speculate that a high density of misfit dislocations is making the formation of multi-faceted (dome-shaped) islands unfavorable. In other words, the C atoms are disrupting the lattice such that misfits are favored over island formation, leading to highly-abrupt strain relief near the $Ge_{1-y}C_y$/Si interface. A similar phenomenon is observed in surfactant-mediated epitaxy [83, 84]. The presence of the (001) top facet of the $Ge_{1-y}C_y$ islands explains why these films are remarkably flat compared to pure Ge on Si [152].

(a)



(b)

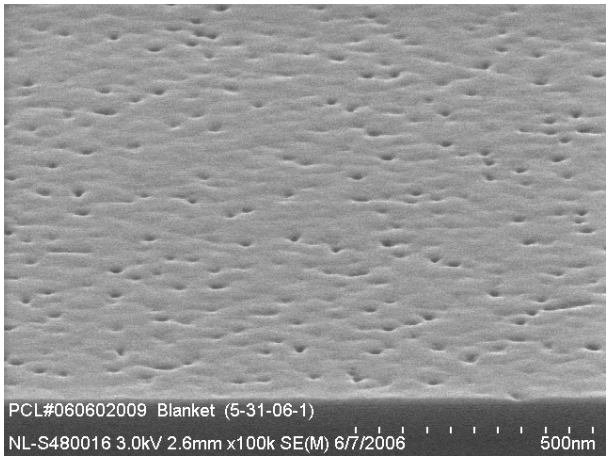


Figure 3.8. Tilt-view SEM images of (a) $Ge_{1-y}C_y$ and (b) pure Ge layers deposited on Si. The triangular "wells" (Fig. 3.7) resulting from $Ge_{1-y}C_y$ island coalescence are crystallographic in nature, and are oriented along orthogonal directions. The pure Ge layer shows random pitting, which occurs when dome-like islands coalesce.

3.4 CARBON CONCENTRATION AND LATTICE INCORPORATION

To better understand the C concentration profile and the possible mechanisms for strain relaxation, a $Ge_{1-y}C_y$ film was examined with energy-filtering transmission electron microscopy (EFTEM), electron energy loss spectroscopy (EELS), and secondary ion

mass spectrometry (SIMS). The $Ge_{1-y}C_y$ layer that was analyzed was about 35 nm thick, and the growth was performed with the same GeH_4:CH_3GeH_3 flow ratio as the layers that were characterized in the previous section. It has been discovered that the C atoms do not get incorporated throughout the entire layer, but are mostly confined to an interfacial region near the Si substrate. The results in this section provide the basis for this claim.

3.4.1 Secondary Ion Mass Spectrometry

The small size of C atoms makes them difficult to detect, and most materials characterization methods are not sensitive enough to quantify C concentrations. SIMS is one of the few techniques capable of measuring C concentrations, but care must be taken to assure that the measurements are as accurate as possible. The analyses for this work were performed with the help of Shifeng Lu, a SIMS expert that is currently with Micron, Inc. in Boise, Idaho. For these analyses, a primary beam of Cs^+ ions and net impact energy of 1 keV was used. A neutralization process was also performed for the purpose of charge compensation. A profilometer was used to determine the depth of the sputtered crater and calibrate the depth scale. The C and Si concentrations were determined by the relative sensitivity factors (RSFs) obtained from standard reference samples prepared by ion implantation of C^{12+} (5×10^{15} cm^{-2}, 60 keV) and Si^{28+} (1×10^{16} cm^{-2}, 100 keV) into bulk Ge (001) wafers. The SIMS profiles in Fig. 3.9 show the atomic concentrations of Si (solid line) and C (dotted line) in the $Ge_{1-y}C_y$ film. The data shows very low C concentration in the main portion of the film and higher C concentration at the $Ge_{1-y}C_y$/Si substrate interface. The units for the concentration of the Ge reference profile (dot-dashed line) are arbitrary, since SIMS cannot provide quantification of the matrix species. The concentration of C atoms near the $Ge_{1-y}C_y$/Si interface is about 1 at. %. The C atoms at the surface are due to contamination from the

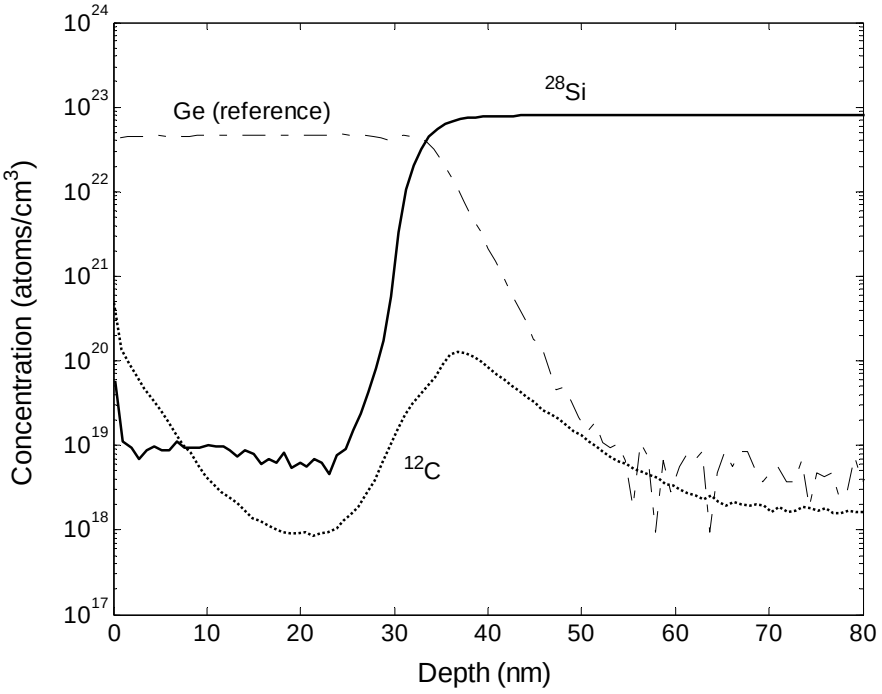


Figure 3.9. SIMS profile showing the atomic concentrations of Si (solid line) and C (dotted line) in the $Ge_{1-y}C_y$ film. The data shows very low C concentration in the main portion of the film and higher C concentration at the $Ge_{1-y}C_y$/Si substrate interface. The units for the concentration of the Ge reference profile (dot-dashed line) are arbitrary, since SIMS cannot provide quantification of the matrix species.

environment. The C atoms at the $Ge_{1-y}C_y$/Si interface come from the CH_3GeH_3 precursor, not from surface contamination from the environment prior to growth, since a pure Si epitaxial buffer layer was grown before $Ge_{1-y}C_y$ deposition.

3.4.2 Carbon Incorporation Near Germanium-Carbon/Silicon Interface

EFTEM and EELS results also support our claim that C is only incorporated near the interface with the Si substrate. The EELS studies were performed on a JEOL 2010F transmission electron microscope featuring a Schottky-type field emission gun (FEG).

Included in the system are scanning image devices operated as a scanning transmission electron microscope (STEM). The EELS spectra were recorded in STEM mode with a 0.2 nm probe size and 0.1 eV/channel dispersion. The convergence and collection semiangles were 3 mrad and 11 mrad, respectively. The typical full width at half maximum (FWHM) of the zero loss peak was 1.0 eV. The EFTEM analysis was performed on a FEI Tecnai G2 F20 X-TWIN microscope featuring a 200-kV energy filter incorporating GIF2001:YAG/B/1k.

EFTEM images were obtained using the C 1*s* core loss peak in order to obtain a qualitative map of the location of C atoms in the $Ge_{1-y}C_y$ layer. An EFTEM image can also be thought of as a two-dimensional map of the EELS spectra. Figure 3.10 shows the resulting image. We see a bright region near the interface that is fairly abrupt, with a thickness of about 12 nm. The total film thickness was 36 nm. From Fig. 3.10 we might conclude that the higher concentration of C atoms near the $Ge_{1-y}C_y$/Si interface occurred during epitaxial growth, but since C contamination from the external environment can accumulate at interfaces during TEM sample preparation, additional characterization is needed to determine the nature of these C atoms.

To address this, the type of hybridization present in the C (*sp*, sp^2 or sp^3) was systematically studied. Based on the analysis of the EELS spectrum, the type of hybridization present can be determined [163]. The energy of the characteristic C plasmon peak can give a very clear idea of the type of hybridization present in the C, where higher plasmon peak energies correlates to a higher concentration of sp^3 bonding [163]. Also, from the C 1*s* core loss peak, the ratio between the intensities for the 1*s*-2*p*(π^*) ($\boldsymbol{I_\pi}$) transition (characteristic of sp^2 hybridization located at 285 eV) and the 1*s*-2*p* ($\boldsymbol{I_\sigma}$) transition (characteristic of sp^3 hybridization at 293 eV) can give a quantitative idea of the ratio of the sp^2 and sp^3 hybridizations. A lower value of this ratio

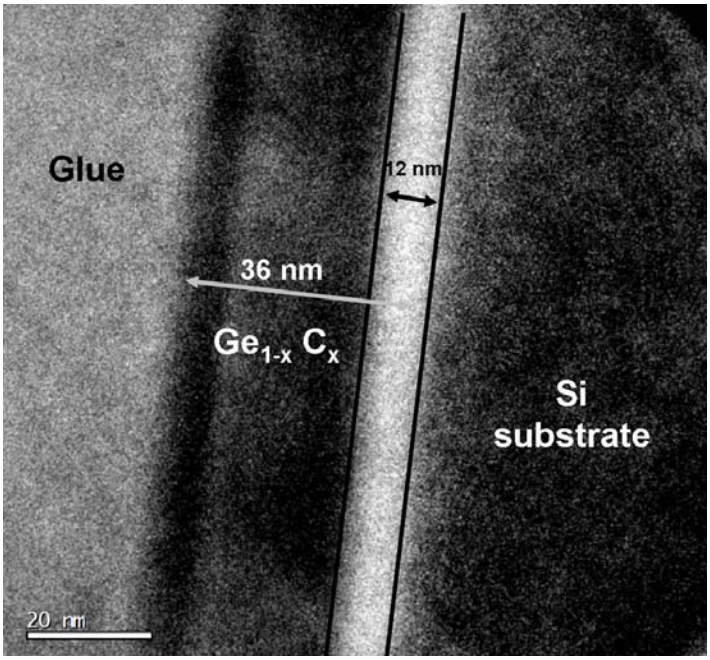


Figure 3.10. EFTEM image showing a bright region at the $Ge_{1-y}C_y$/Si substrate interface. This region indicates the presence of C atoms, and is approximately 12 nm thick.

corresponds to a higher presence of sp^3 hybridization.

It is claimed in other studies of $Ge_{1-y}C_y$ [144, 145] that C atoms occupy substitutional positions in the Ge diamond structure. If indeed the C is substitutional, the C atoms should present a sp^3 type of hybridization due to the tetrahedral bonding of C atoms with other atoms in the diamond structure [163]. Another possible explanation for C atoms exhibiting sp^3 character is that C-containing tetrahedral interstitial complexes or SiC crystallites are forming at the interface with the substrate [111, 158]. It is proposed that in the regions of the $Ge_{1-y}C_y$ layer where the C atoms form interstitial complexes or SiC crystallites or are incorporated into the Ge diamond structure, the sp^3 character of the C atoms should be more prominent than the sp^2 character. If the C atoms are external contaminants or interstitial C, the sp^2 character should be higher. We must emphasize

here that we do not expect Si-containing crystallites (such as SiC) to form in regions that are away from the $Ge_{1-y}C_y$/Si interface. The key advantage that we have in this regard is our use of CVD precursors that do not contain any Si atoms (CH_3GeH_3 and GeH_4). The only source of Si is from the substrate.

Figure 3.11 is a depth profile of the C plasmon peak energy measured in the C 1*s* core loss region of the EELS spectrum. The peak energy was measured at 4 nm intervals along the $Ge_{1-y}C_y$ profile. We observe in Fig. 3.11 how the energy of the C plasmon peak energy increases as we get closer to the $Ge_{1-y}C_y$/Si substrate interface. This is evidence for the higher sp^3 character of the C atoms located near this interface [163]. Amorphous C layers have a 23 eV plasmon peak for a 0% fraction of sp^3 hybridized C atoms, while the plasmon peak energy of 100% C atoms in sp^3 hybridization state (diamond) is close to 33 eV. As the fraction of C atoms in sp^3 hybridization state increases, the C plasmon peak energy increases.

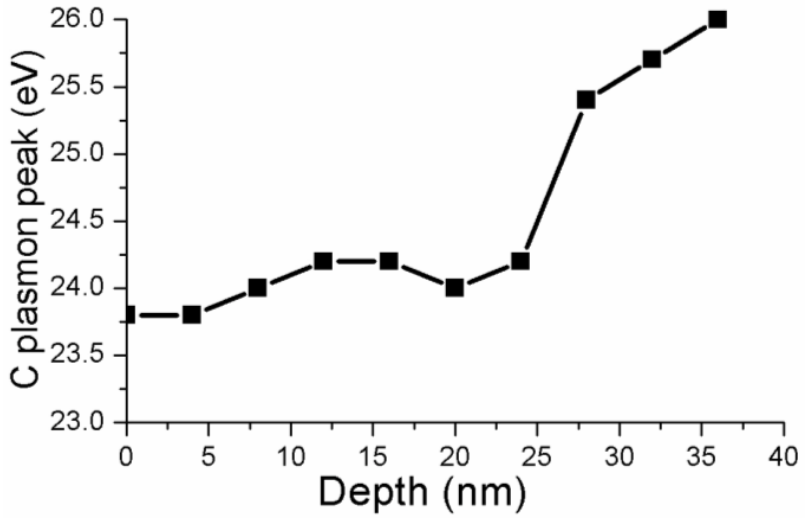


Figure 3.11. Depth profile of C plasmon peak energies obtained from the C 1*s* core-loss EELS spectra for a 36-nm-thick $Ge_{1-y}C_y$ layer.

As stated above, from the C 1*s* core loss peak, the ratio between the intensities for the 1*s*-2*p*(π*) (I_π) transition (characteristic of sp^2 hybridization located at 285 eV) and the 1*s*-2*p* (I_σ) transition (characteristic of sp^3 hybridization at 293 eV) is an indication of the ratio between the sp^2 and sp^3 hybridizations. The measured I_π/I_σ ratios are summarized in Table 3.1. We see in Table 3.1 that the ratio decreases as we get closer to the $Ge_{1-y}C_y$/Si substrate interface. This is additional evidence of the more pronounced sp^3 character in the C atoms encountered near the $Ge_{1-y}C_y$/Si interface.

Depth (nm)	**I_π (counts) (285 eV)**	**I_σ (counts) (293 eV)**	**I_π / I_σ**
0	20300	33825	0.6
4	19850	33072	0.6
8	16300	27092	0.6
12	23200	38600	0.6
16	10590	16809	0.63
20	4700	7500	0.62
24	13600	22974	0.59
28	22340	38380	0.58
32	17850	31019	0.57
36	17837	31900	0.55

Table 3.1. Ratios of the 1*s*-2*p*(π*) and 1*s*-2*p* transitions (I_π/I_σ) in the C 1*s* core loss region of the EELS spectrum in a 36-nm-thick $Ge_{1-y}C_y$ film.

In concordance with Fig. 3.11 and Table 3.1, it is concluded that C atoms in a tetrahedral configuration are preferentially encountered in a region (~12 nm) close to the $Ge_{1-y}C_y$/Si substrate interface. This could indicate the presence C-containing interstitial complexes or it could be substitutional C in Ge near the interface (or both). Both of these are mechanisms for strain relaxation [158], which helps to explain the low density of threading dislocations in the films.

3.4.3 Further Discussion of Strain Relaxation Mechanism

A theoretical study performed by P.C. Kelires [151] reported on the bulk and surface properties and structure of $Ge_{1-y}C_y$ alloys using Monte Carlo simulations. Those results suggested a preferential arrangement of C atoms as third nearest neighbors when C atoms occupy substitutional sites. The conclusion was that this configuration minimizes the elastic (strain) energy of the crystal lattice. For the surface properties, on the other hand, it was suggested that the lattice elastic energy could be relieved through the segregation of the C atoms to the top and bottom surfaces of the $Ge_{1-y}C_y$ film. This is due to the atomic size mismatch, which is appreciable even for the proposed third nearest neighbor configuration in the bulk. For the simulated case of a $Ge_{1-y}C_y$ (y = 0.03) film grown epitaxially on a Si substrate, the preferential segregation of C atoms to the surface and $Ge_{1-y}C_y$/Si interface was shown, but the inner layers still possessed an appreciable amount of C. This behavior was explained by considering that the Ge layers on a Si substrate are under compressive stress, and C serves to compensate this stress. It was concluded that the degree of segregation is determined by the competition between the need of Ge–C geometries in the bulk to compensate the epitaxial strain and the attraction of C atoms to energetically-favorable sites in the subsurface layers.

It has been shown that the $Ge_{1-y}C_y$ films in this work show significant strain relaxation despite a remarkably low number of threading dislocations. Based on these results, it is believed that strain relaxation is occurring through either structural means (substitutional C in Ge) or chemical means (C-containing tetrahedral interstitial complexes at the substrate interface) or possibly a combination of both. The EELS results in particular provide corroborating evidence for these claims.

3.5 SPECTROSCOPIC ELLIPSOMETRY RESULTS

To further characterize the epitaxial quality of $Ge_{1-y}C_y$ and compare its properties to bulk Ge, the dielectric function was measured on a thin $Ge_{1-y}C_y$ layer on Si (100) using spectroscopic ellipsometry. Spectroscopic ellipsometry is an experimental technique in which a beam of light with a well-characterized state of polarization and nearly parallel wave fronts is specularly reflected at an oblique angle of incidence ϕ by the surface of a flat and smooth sample (either bulk or thin film on substrate with interfaces parallel to the surface). The polarization state of the reflected beam is determined using a photodetector and a rotating polarizing element. The change in polarization is described by the ellipsometric angles ψ and Δ defined by the relationship

$$\tan(\psi)e^{i\Delta} = r_p / r_s = \rho\,, \tag{3.1}$$

where r_p and r_s are the complex Fresnel reflection coefficients for *p* and *s*-polarized light, respectively [164], and ρ is the complex Fresnel reflectance ratio. By collecting data at various wavelengths and angles of incidence, information about the sample, such as layer thicknesses and optical constants can be obtained by comparing the experimental data with results of model calculations based on the known characteristics of the sample (such as layer information from TEM, growth procedure, etc). For bulk or bulk-like samples (e.g., epitaxial semiconducting films with a native oxide on a substrate), it is sometimes useful to display the data as a pseudodielectric function instead of ellipsometric angles. The pseudodielectric function $\langle\varepsilon\rangle$ is calculated using the equation

$$\langle\varepsilon\rangle = \left(\frac{1-\rho}{1+\rho}\right)^2 \tan^2(\phi)\sin^2(\phi) + \sin^2(\phi)\,. \tag{3.2}$$

In the limit of a bulk sample with zero native oxide or roughness thickness (impossible to realize with a real sample), $\langle\varepsilon\rangle$ approaches the dielectric function, ε, of the bulk material.

For the $Ge_{1-y}C_y$ sample, the ellipsometric angles ψ and Δ as a function of photon energy from 0.74 to 9.5 eV with 0.01 eV steps were acquired on a J. A. Woollam VUV-VASE rotating-analyzer ellipsometer with a computer-controlled Berek wave plate compensator at four angles of incidence (60°, 65°, 70°, and 75°) [165], courtesy of Ron Synewicki at the J. A. Woollam Company. Equivalent data (700 wavelengths between 0.74 to 6.5 eV, at six angles of incidence between 55° and 80°) were obtained using a rotating-compensator ellipsometer with a multi-wavelength CCD detector. The depolarization of the reflected light beam was below 1% in the 0.74 to 9 eV spectral range, indicating high sample and data quality (especially uniform layer thicknesses) suitable for precision analysis of the spectra. No surface cleaning was needed or performed before ellipsometry measurement.

Analysis of the data was done with the help of ellipsometry expert Dr. Stefan Zollner at Freescale, Inc. To first order, an attempt was made to describe the optical response of the $Ge_{1-y}C_y$ sample using a model consisting of a Si substrate, a Ge epitaxial layer, and a GeO_2 native oxide. The optical constants of Si [165] and GeO_2 [166] were taken from the literature. Those of bulk Ge were determined with an undoped, high-resistivity Ge crystal [167] using the Jellison-Sales method for transparent glasses similar to published work for GaAs [168]. This model works surprisingly well (see Fig. 3.12) and yields both the thickness of the $Ge_{1-y}C_y$ layer and the thickness of the GeO_2 layer. It is concluded that the optical constants of $Ge_{1-y}C_y$ are very similar to those of bulk Ge, i.e., doping with carbon has only a minor influence on the optical constants of the $Ge_{1-y}C_y$. This has also been seen for C doping of Si [169]. The spectra, displayed as a

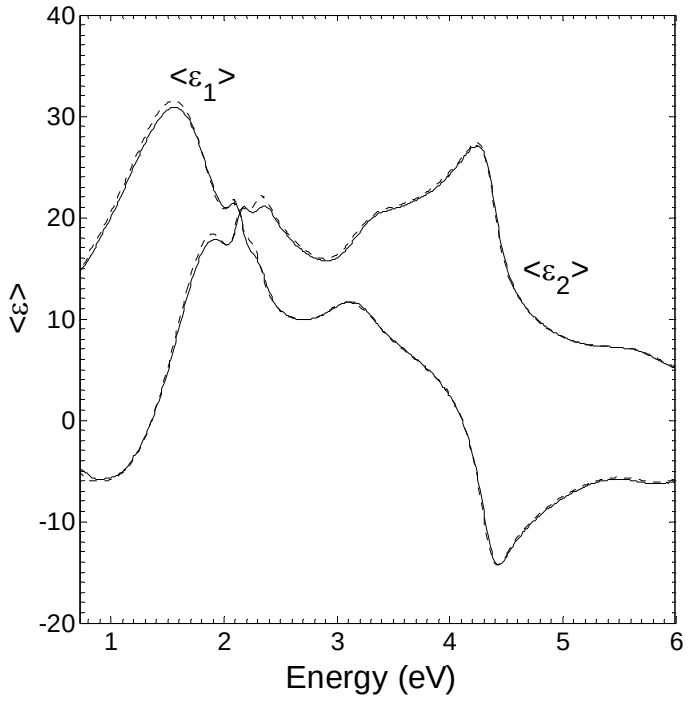


Figure 3.12. Real and imaginary parts of the pseudodielectric function $\langle\varepsilon\rangle$ as a function of photon energy (solid lines) for $Ge_{1-y}C_y$ acquired at four angles of incidence (60°, 65°, 70°, and 75°), all leading to the same result. The dotted lines show the best fit using a model, calculated using the optical constants of bulk Si, bulk Ge, and GeO_2. The only parameters in this fit are the thicknesses of the Ge and GeO_2 layer, 41.9 nm and 0.9 nm, respectively.

pseudodielectric function $\langle\varepsilon\rangle$ in Fig. 3.12, show the E_1, $E_1+\Delta_1$, E_0', and E_2 critical points near 2.2, 2.4, 3.4, and 4.2 eV, respectively. No attempt was made to find the precise location of these critical points [80]. Below 2 eV, interference oscillations due to multiple reflections of the infrared light within the $Ge_{1-y}C_y$ layer are visible. The high amplitude (35.5) of $\langle\varepsilon_2\rangle$ at the E_2 critical point indicates a smooth surface with minimal native oxide layer. We should note that the $Ge_{1-y}C_y$ layer thickness is determined mostly in the infrared region of the spectra, while the native oxide thickness is derived primarily

in the UV portion of the spectrum. Thus, both thicknesses can be determined independently. Surface roughness also enters the ellipsometry data analysis in the same manner as a native oxide, so the oxide thickness reported here may have two contributions, i.e., roughness and actual native oxide.

A closer comparison of the data and model in Fig. 3.13 shows slight differences in the infrared spectral region, where the interference effects dominate. This could indicate layer thickness variations or nonuniformities (either lateral or vertical) in the optical properties of the $Ge_{1-y}C_y$ layer. In comparison with ellipsometry spectra of similar epitaxial layers on a substrate, however, the agreement is excellent [169]. A small difference between data and model also exists near the $E_1+\Delta_1$ critical point (near 2.3 eV). This region is particularly sensitive to sample quality, strain, and composition effects. This was the same sample that was measured by x-ray diffraction reciprocal space mapping (see section 3.2.3 above), where the $Ge_{1-y}C_y$ sample showed some retention of compressive stress, with a relaxation of 78% based on measurements of the in-plane and out-of-plane lattice parameters. The near-perfect fit of the measured data to the bulk Ge model shows that the $Ge_{1-y}C_y$ sample is uniform and has high epitaxial quality. Thus, it is possible that the difference near the $E_1+\Delta_1$ critical point is due to both strain and C doping of the Ge layer.

In order to improve the agreement between data and model, the optical constants of the epitaxial layer were slightly adjusted (using those of bulk Ge as a starting point) while fixing the layer thicknesses derived in the first step. The complex dielectric function ε of the $Ge_{1-y}C_y$ layer was obtained, shown by the solid line in Fig. 3.13, and it was compared with that of bulk Ge [167], indicated by the dotted line. The main difference between the epitaxial layer and Ge is at the $E_1+\Delta_1$ critical point (near 2.3 eV)

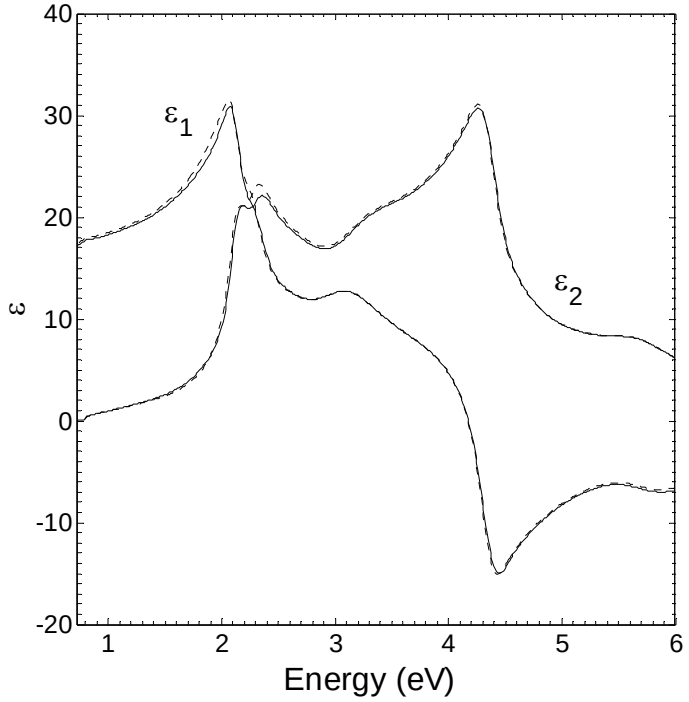


Figure 3.13. From the experimental data shown in Fig. 3.12, the real and imaginary parts of the dielectric function of the $Ge_{1-y}C_y$ alloy (solid lines) were determined by fixing the thicknesses as obtained in Fig. 3.12 and varying the optical constants of the alloy slightly (from those of bulk Ge, dotted lines) to achieve best agreement with the experiment.

for the reasons explained above.

The ellipsometry results reported in this section indicate that the $Ge_{1-y}C_y$ layer has high epitaxial quality and optical properties that are nearly identical to bulk Ge. It was shown earlier that the layers have a low concentration of C atoms in the main portion of the $Ge_{1-y}C_y$ film and the preferential localization of C at the interface with the Si substrate. The preferential localization of C atoms at the $Ge_{1-y}C_y$/Si interface is to be expected given the negligibly low solubility of C in Ge, and although this is disadvantageous for studying the effect of substitutional C on the optical and bandgap

properties of Ge, it is an advantage for MOS applications. In $Ge_{1-y}C_y$ MOSFETs, C atoms would act as alloy scattering centers that reduce the channel mobility. As will be seen in chapter 5, enhanced hole mobilities have been observed in our work on buried- and surface-channel high-κ/metal gate $Ge_{1-y}C_y$ *p*-MOSFETs. Carbon accumulation at the Si interface also helps explain why our films show low threading dislocation densities despite significant strain relaxation.

3.6 SUMMARY

This chapter described the $Ge_{1-y}C_y$ growth technique and provided insights into the growth kinetics, epitaxial quality, defect density, strain, and carbon incorporation of the films. The $Ge_{1-y}C_y$ layers appear to grow in an S-K growth mode, but the islands are not dome-like in shape as is the case with pure Ge. Despite significant strain relaxation, the films show a remarkably low number of threading dislocations. The C atoms appear to be preferentially located near the interface with the Si substrate, and EELS data suggests that the C exhibits tetrahedral bonding characteristics. Ellipsometry data shows that the $Ge_{1-y}C_y$ layers exhibit high epitaxial quality and have optical properties that are nearly indistinguishable from pure Ge.

Now that the material properties of the films have been described, the electrical characteristics of MOS devices fabricated on $Ge_{1-y}C_y$ layers will now be reported. It will be seen in chapter 5 that the $Ge_{1-y}C_y$ layers yield MOSFET devices with enhanced performance over their Si counterparts. Before reporting the electrical results, the next chapter will provide an overview of the device fabrication process with a discussion of the process-related challenges for $Ge_{1-y}C_y$ devices.

CHAPTER 4

GERMANIUM-CARBON MOS DEVICE FABRICATION PROCESS AND PROCESS-RELATED CHALLENGES

4.1 MOS DEVICE FABRICATION PROCESS

The MOS fabrication steps for all of the $Ge_{1-y}C_y$ devices reported in this dissertation were performed in the class-100 cleanroom of the Microelectronics Research Center at the J. J. Pickle Research Campus of University of Texas at Austin. In section 3.1, the growth process for the $Ge_{1-y}C_y$ layers using a custom-built, cold-wall UHV-CVD reactor was described. This section will provide the details of the remaining steps of the fabrication process for MOS capacitors and transistors on $Ge_{1-y}C_y$. The salient features of each fabrication step will be given, including any associated challenges. At the end of this chapter the fabrication steps will be summarized again for convenience.

4.1.1 Surface Pretreatment Before High-κ Deposition

After the wafers were removed from the UHV-CVD reactor following epitaxial growth, they underwent surface pretreatment before high-κ dielectric deposition, depending on whether a Si cap layer was deposited on top of the $Ge_{1-y}C_y$. For devices with a Si cap layer, the wafers were pretreated with a 40:1 deionized H_2O:HF dip for 30 seconds to remove the native SiO_2 on the Si cap layer. The removal of the native oxide improves the interface with the high-κ dielectric, and lowers the electrical thickness of

the dielectric stack. No pretreatments were performed on the $Ge_{1-y}C_y$ devices without a Si cap layer, even though this risked the formation of native GeO_2 or GeO on the surface.

It is noted that when GeO_2 or GeO is left on the surface of a Ge wafer, it can degrade the quality of the gate stack. Chapter 1 discussed ways that researchers have found to passivate the Ge surface before high-κ deposition, such as forming a GeO_xN_y interfacial layer by annealing in NH_3 [25, 69-73]. In addition, Chui has shown the impact of leaving or removing the Ge native oxide on high-κ capacitors with metal gates [170]. In that work, he compared the electrical characteristics of ZrO_2/Pt capacitors in which the Ge native oxide was kept, removed with DI water, or removed with HF vapor treatment. The wafers that were treated with HF vapor showed the least amount of gate leakage current and hysteresis in the capacitance-voltage curves [170].

The main reason that NH_3 anneals were not used in this work was to reduce the thermal budget and to avoid etching away the already-thin $Ge_{1-y}C_y$ film. If even small amounts of oxygen are present in the NH_3 annealing environment, the Ge atoms react with the oxygen to form GeO or GeO_2, which thermally desorbs from the surface above 420 °C [60]. One can easily see why the NH_3 anneal is acceptable for bulk wafers in which Ge etching is not a concern. The annealing facilities available at the Microelectronics Research Center at the University of Texas do not have low enough oxygen levels to make NH_3 anneals feasible for very thin Ge-based films. HF vapor treatments are not available either. For this research, the most feasible $Ge_{1-y}C_y$ surface passivation scheme, given the available resources, was the deposition of a Si cap layer. (The importance of the Si cap layer for the electrical performance of the MOS stack will be shown in the next chapter.)

4.1.2 High-κ Deposition

Minimizing the time between $Ge_{1-y}C_y$ epitaxy and high-κ deposition is critical for maintaining the integrity of the gate stack. Contaminants from the environment and native oxide formation are vital concerns, and as such it is important to deposit the high-κ dielectric on the $Ge_{1-y}C_y$ layer or Si cap as soon as possible after growth. Immediately following growth (or following surface pretreatment for samples with a Si cap layer) the wafers were placed under vacuum inside the load lock of a Kurt J. Lesker DC magnetron physical vapor deposition (PVD) sputtering system.

The PVD system at the University of Texas has two separate deposition chambers for depositing a variety of dielectrics and metals. For the $Ge_{1-y}C_y$ devices, HfO_2 was used as the gate dielectric because the deposition process is relatively simple and the properties and processing issues of HfO_2 are well established in the research literature. The HfO_2 was deposited using reactive sputtering of a high-purity Hf target in a 20-sccm Ar plasma with 6.5 sccm modulated O_2 flow, following a technique developed by Professor Jack Lee's research group at the University of Texas [171]. Figure 4.1 shows a schematic diagram of the O_2-modulated deposition process. The process begins by flowing sputtering Hf with Ar plasma for a certain time t_1. The O_2 flow is then turned on, and the plasma stabilizes during time t_s. After stabilization, both Ar and O_2 are flown for a time t_2 while the Hf reactively sputters to form HfO_2. The cycle is then repeated as many times as desired depending on the thickness required. For this work, only two such cycles were used for a final thickness between 4 and 6 nm. Following the PVD process, the wafers were removed from the sputtering system and an atmospheric-pressure furnace anneal was performed for 5 min. at 500 °C with 6 slm N_2 flow. The furnace anneal further oxidizes the HfO_2 layer, improving its electrical quality and homogeneity.

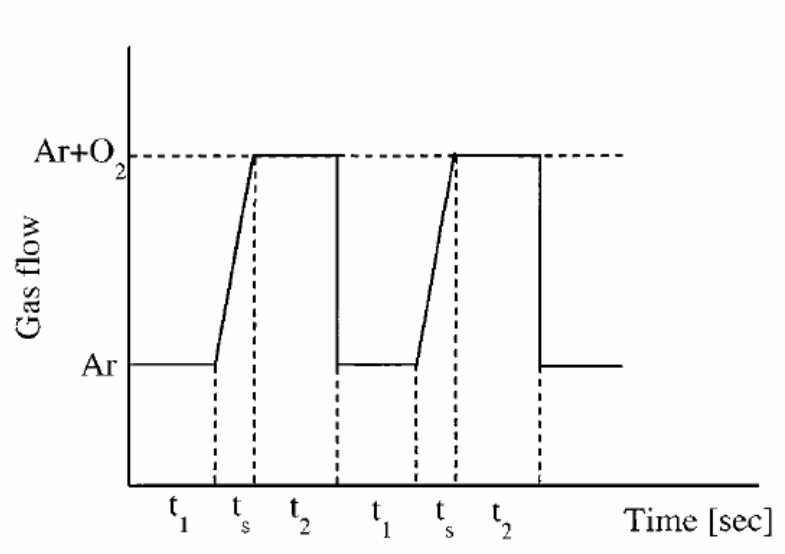


Figure 4.1. Schematic diagram of the O_2-modulated DC magnetron PVD process used to deposit the HfO_2. During t_1, only Ar gas is flown. The stabilization time after the O_2 begins flowing is represented by t_s. Both Ar and O_2 are flown for the time t_2 [171].

4.1.3 Metal Gate Deposition and Gate Stack Etching

Tantalum nitride (TaN) metal was used for the gate metal for all of the $Ge_{1-y}C_y$ devices. The TaN was deposited using reactive sputtering in a second chamber of the Kurt J. Lesker DC magnetron sputtering system with 20 sccm Ar flow and 10 sccm N_2 flow. The metal had a thickness of approximately 200 nm.

After TaN deposition, ring-type gates with varying inner and outer radii were patterned using conventional lithography. Also included on the gate mask were capacitor dots for measuring capacitance-voltage and leakage curves of MOS capacitors. The ring-type gates reduce the number of process steps required to complete a transistor, since the ring provides source and drain isolation without the need for active-region patterning.

Following photoresist patterning, the TaN metal was etched using reactive ion etching (RIE) with CF_4.

The HfO_2 did not undergo a high-temperature densification anneal since the $Ge_{1-y}C_y$ heterostructures cannot tolerate heavy thermal processing. This means that the HfO_2 was not impervious to the CF_4 gate etch, so the etch had to be qualified with send-ahead wafers to calibrate the etch time. There was no feedback mechanism to determine the proper etch time, so the gate etch posed a significant challenge. Multiple wafers with the same epitaxy and gate stack conditions needed to be prepared to improve the yield of working transistors. Figure 4.2 shows a cross-sectional TEM image of the edge of the

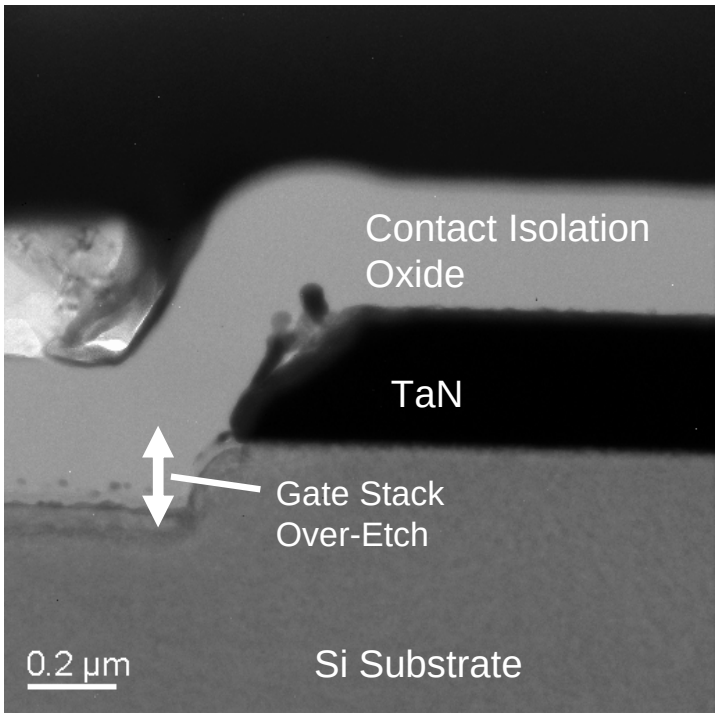


Figure 4.2. Cross-sectional TEM image of the edge of a HfO_2/TaN transistor gate stack, showing the over-etch of the TaN.

gate stack of a HfO_2/TaN transistor structure that has been over-etched. The figure shows the Si substrate, the TaN metal, and a contact isolation oxide deposited over the TaN. The HfO_2 dielectric is present between the Si and the TaN, but it could not be distinguished from the TaN in this image. There were no epitaxial layers in this device. From Fig. 4.2 we clearly see the over-etching of the gate stack, which is catastrophic to transistor performance since the channel is not aligned with the implanted source and drain regions.

4.1.4 Remaining Process

After gate etching with RIE, the photoresist was removed and the MOS capacitor structures were probed to check the integrity of the gate stack. If the capacitor characteristics looked acceptable, the wafers were sent to an external vendor for ion implantation. The *p*-MOSFET devices underwent BF_2 implantation with a dose of 5×10^{15} cm^{-2} and an implant energy of 25 keV, including rotation and 7° sample tilt. The dopant atoms were activated during a 2-hour, 530 °C low-temperature oxide (LTO) deposition step for contact isolation. It has been shown that *p*-type dopants in Ge can be activated at low temperatures [172], so the LTO step was found to be sufficient for dopant activation. No additional annealing was done to protect the integrity of the $Ge_{1-y}C_y$ crystal and prevent $Ge_{1-y}C_y$/Si interdiffusion. (Further information about the thermal stability of $Ge_{1-y}C_y$/Si will be provided in the next section.) While a detailed study of dopant activation was not performed, it was assumed that the dopants were not fully activated in the Si substrate below the $Ge_{1-y}C_y$.

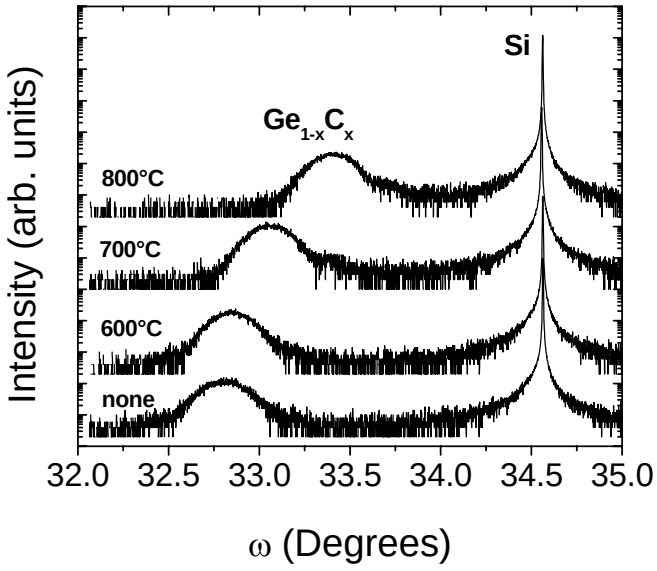
Following the LTO deposition, contacts were patterned and etched with a buffered oxide etch (BOE) solution. The BOE was able to etch through the HfO_2 layer as

well, since the HfO_2 had not undergone a densification anneal. The transistor fabrication process was finished with Al metallization, back-side metal, and a forming gas anneal at 450 °C for 30 min. The forming gas anneal improved the resistivity of the metal contacts.

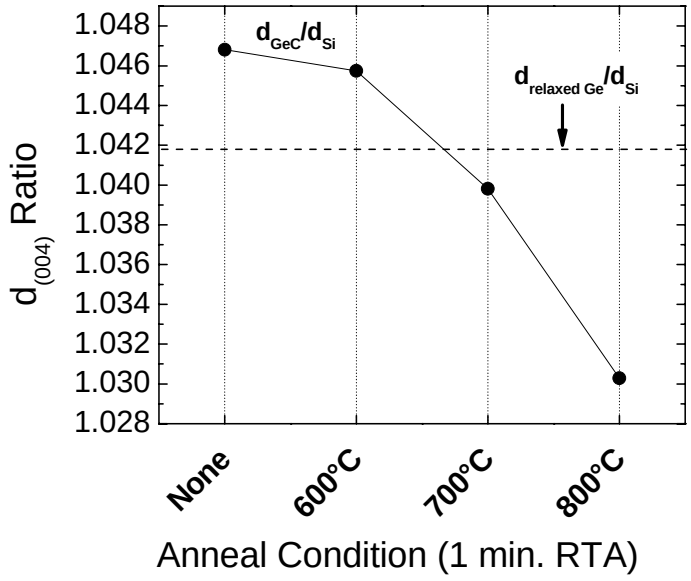
4.2 THERMAL STABILITY OF GERMANIUM-CARBON LAYERS

The highest temperature step that was used in the fabrication process was the 2-hour, 530 °C LTO deposition step for contact isolation. A casual survey of the research literature on Ge MOSFETs reveals that almost all of the fabrication processes use reduced thermal budgets compared to a conventional Si process. The reason for low thermal budgets is to maintain the integrity of the gate stack, and for Ge-on-Si devices, to prevent crystal defect formation and Si/Ge interdiffusion.

Indeed, thermal budget constraints are a concern for any strained-layer heteroepitaxial structure. For films that are thicker than the stable critical thickness (see Fig. 1.3(b)), thermal processing following growth can produce defects that are not present in the as-grown layer. In the case of thin $Ge_{1-y}C_y$ on Si with a Si cap layer, $Ge_{1-y}C_y$/Si interdiffusion and strain relaxation are mitigated by reducing the maximum temperature used during the fabrication process. To investigate the thermal stability of the $Ge_{1-y}C_y$ films with a Si cap layer, XRD was used in conjunction with rapid thermal annealing (RTA). Figure 4.3(a) shows a compilation of XRD rocking curves measured with a Philips X'Pert system on the ω–2θ scan axis for different anneal temperatures. The four curves in Fig. 4.3(a) correspond to samples with no anneal and samples with 1-min. RTA anneals at 600°C, 700°C, and 800°C. We see that the $Ge_{1-y}C_y$ layer peak shifts more significantly toward the Si substrate peak with higher anneal temperatures.



(a)



(b)

Figure 4.3. (a) Comparison of XRD rocking curves measured on the ω-2θ scan axis (and plotted as a function of ω) for $Ge_{1-y}C_y$/Si cap heterostructures after 600 °C, 700 °C, and 800 °C anneals compared to a sample with no anneal. (b) Plot of the change in the XRD-measured *d*-spacing of the (004) planes of the $Ge_{1-y}C_y$ layer (d_{004}). The anneal conditions are shown on the *x* axis, and the ratio of the *d*-spacing of the $Ge_{1-y}C_y$ layer to bulk Si is shown on the *y* axis. The dotted line corresponds to the ratio of the *d*-spacing of fully-relaxed Ge to bulk Si.

Part of this shift is due to strain relaxation, but since the $Ge_{1-y}C_y$ layers are already partially relaxed (see section 3.2.3), the shift is primarily due to Si atoms diffusing into the $Ge_{1-y}C_y$, which lowers the lattice parameter. The change in the lattice parameter due to thermal annealing is seen more clearly in Fig. 4.3(b), which shows the change in the measured *d*-spacing of the (004) planes of the $Ge_{1-y}C_y$ layer (d_{004}). The anneal conditions are shown on the *x* axis, and the ratio of the *d*-spacing of the $Ge_{1-y}C_y$ layer to bulk Si is shown on the *y* axis. The dotted line corresponds to the ratio of the *d*-spacing of fully-relaxed Ge to bulk Si. From Fig. 4.3(b) we see that the films are only partially relaxed before annealing and that both Si diffusion and strain relaxation contribute to the change in the *d*-spacing as the films undergo RTA anneals.

4.3 SUMMARY

Table 4.1 shows a summary of the fabrication process that was used for the $Ge_{1-y}C_y$ MOS devices in this research. The process is a short transistor flow that consists of growing blanket $Ge_{1-y}C_y$ heterostructures on Si, ring-type gate patterning and RIE etching, ion implantation and annealing, contact isolation, and Al metallization. Although the ring-type gates cannot be used to examine short-channel effects, they are ideal for comparing new semiconductor materials and/or gate stacks and for measuring carrier mobilities. The next chapter will discuss electrical results for the $Ge_{1-y}C_y$ MOS devices.

Step	Process	Notes
1	Si Substrate Cleaning	2:1 H_2SO_4:H_2O_2 piranha clean; 40:1 DI:HF
2	$Ge_{1-y}Cy$ Heterostructure Growth	See Section 3.1
3	Surface Pretreatment	$Ge_{1-y}Cy$ with Si cap - 40:1 DI:HF $Ge_{1-y}Cy$ without Si cap - None
4	PVD HfO_2	20 sccm Ar plasma reactive sputtering of Hf target with 6.5 sccm modulated O_2 flow (see Reference 171) Post-deposition furnace anneal at atmospheric pressure for 5 min. at 500 °C with 6 slm N_2 flow
5	PVD TaN	20 sccm Ar plasma reactive sputtering of Ta target with 10 sccm N_2 flow
6	Gate Pattern and Etch	Conventional lithography and timed RIE etch using CF_4 chemistry
7	Ion Implantation	BF_2, 5×10^{15} cm^{-2}, 25 keV, 7 degree tilt
8	Contact Isolation	Low-temperature oxide, 530 °C, 2 hrs.
9	Contact Pattern and Etch	Conventional Lithography and buffered oxide etch of contact holes
10	Metallization	Al sputtering on front side of wafer, metal patterning, Al sputtering on back side of wafer
11	Forming Gas Anneal	6 slm, 450°C, 30 min.

Table 4.1. Summary of $Ge_{1-y}C_y$ MOS device fabrication process.

CHAPTER 5

ELECTRICAL RESULTS FOR GERMANIUM-CARBON MOS DEVICES FABRICATED ON SILICON SUBSTRATES

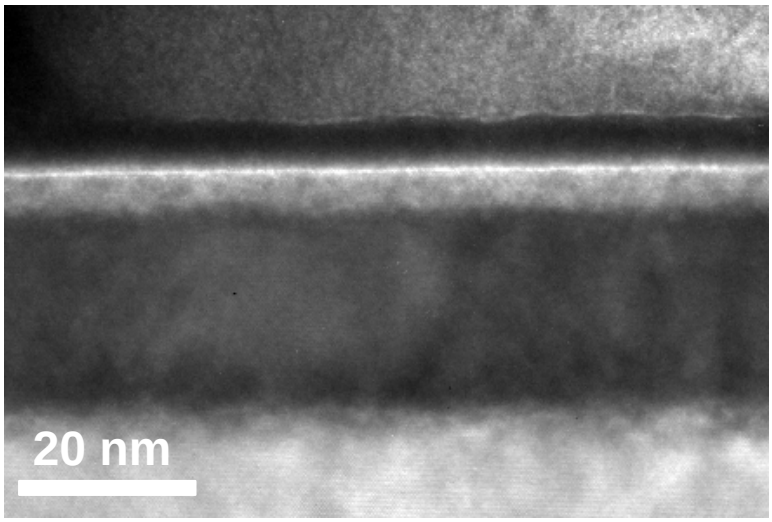
5.1 BURIED-CHANNEL GERMANIUM-CARBON *P*-MOSFETS

Using the process described in chapter 4, both buried- and surface-channel high-κ/metal gate $Ge_{1-y}C_y$ *p*-MOSFETs were fabricated on Si substrates. The buried-channel devices consisted of 20-nm-thick $Ge_{1-y}C_y$ layers similar to the layer shown in Fig. 3.4(b) but including a Si cap layer with a thickness of 3 to 5 nm. As will be seen below, the buried-channel devices performed much better than the surface-channel devices, since the surface-channel devices did not undergo pretreatment to prevent the formation of GeO or GeO_2 on the surface. This section will present the capacitor and transistor results for the buried-channel devices.

5.1.1 Gate Stack Imaging with Transmission Electron Microscopy

Figure 5.1 shows cross-sectional TEM images of a typical gate stack of the buried-channel $Ge_{1-y}C_y$ *p*-MOSFETs. In Fig. 5.1(a) we see a 20-nm-thick $Ge_{1-y}C_y$ layer, a 5-nm-thick Si cap, a 5-nm-thick HfO_2 layer, and the lower portion of the TaN metal. We also see the presence of a thin SiO_2 interfacial layer between the Si cap and the HfO_2. Figure 5.1(b) shows a higher-magnification view of the $Ge_{1-y}C_y$/Si-cap/SiO_2/HfO_2 interfaces. The SiO_2 interfacial layer was 1 nm thick for all of the buried-channel *p*-MOSFET samples.

(a)



(b)

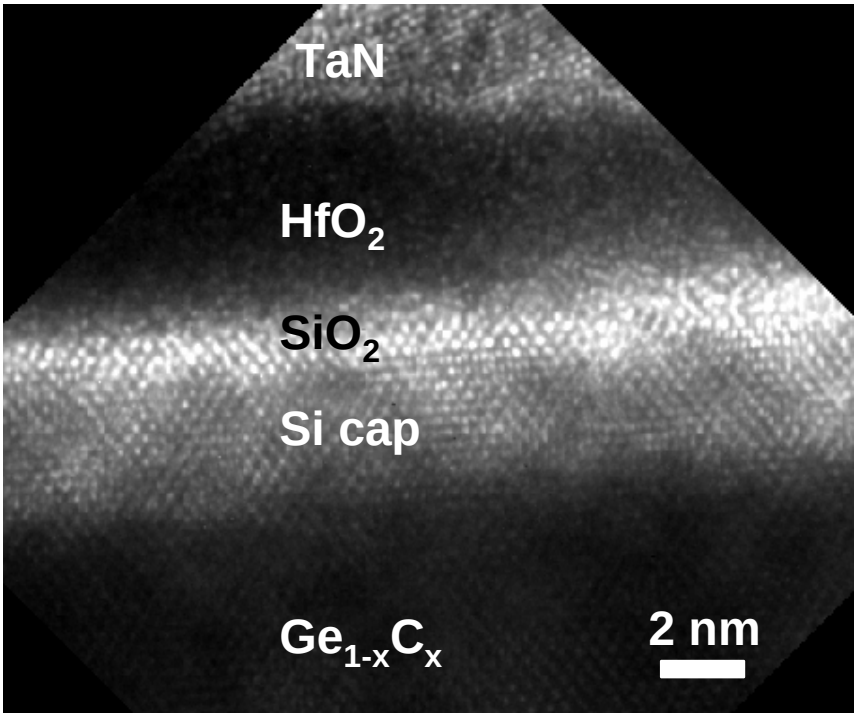


Figure 5.1. (a) Cross-sectional TEM image of the gate stack of buried-channel $Ge_{1-y}C_y$ *p*-MOSFET fabricated on Si. In this example, the $Ge_{1-y}C_y$ was approximately 20 nm thick, the Si cap layer was 5 nm thick, and the HfO_2 was also 5 nm thick. The thin, bright line between the Si cap and the HfO_2 is an interfacial SiO_2 layer. (b) Higher magnification image of the $Ge_{1-y}C_y$/Si cap/SiO_2/HfO_2 interface. The thickness of the SiO_2 interfacial layer was 1 nm.

5.1.2 Capacitors with No Silicon Cap Layer

MOS capacitor capacitance-voltage (C-V) and leakage data were taken on a $Ge_{1-y}C_y$ sample without a Si cap layer to show the electrical quality of the $Ge_{1-y}C_y$ layer before transistor processing. The measurements were taken on a $Ge_{1-y}C_y/HfO_2/TaN$ gate stack after gate RIE etch. Figure 5.2 shows the high-frequency (1 MHz) curve and the calculated low-frequency curve extracted using the NCSU CVC program developed by Hauser [173, 174]. The calculated interface trap density (D_{it}) was 4.82×10^{11} $eV^{-1}cm^{-2}$ and the electrical oxide thickness (EOT) was 2.3 nm. The high flat band voltage (V_{FB}) evident in Fig. 5.2 indicates high levels of negative fixed charge for uncapped devices, the origin of which is not well understood at present. Further discussion of the V_{FB} shift

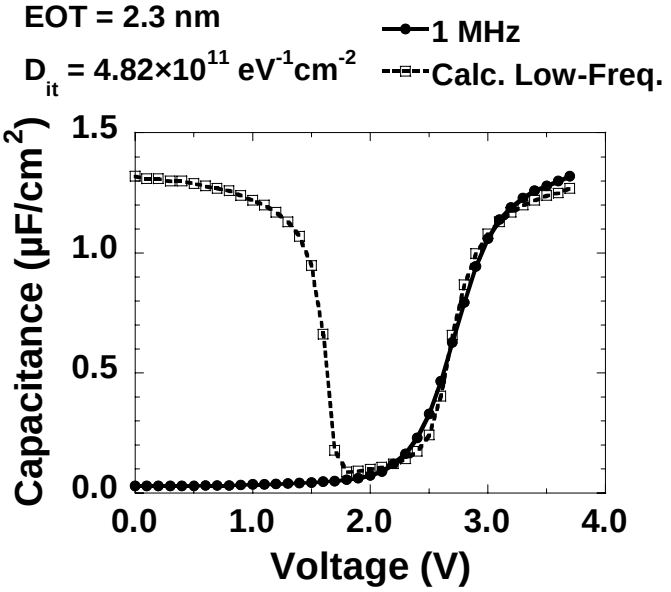


Figure 5.2. $Ge_{1-y}C_y$ (no Si cap) MOS capacitor C-V characteristics showing both the measured high-frequency (1 MHz) and calculated low-frequency curves. The EOT was 2.3 nm and the capacitor area was 1.54×10^{-4} cm^2.

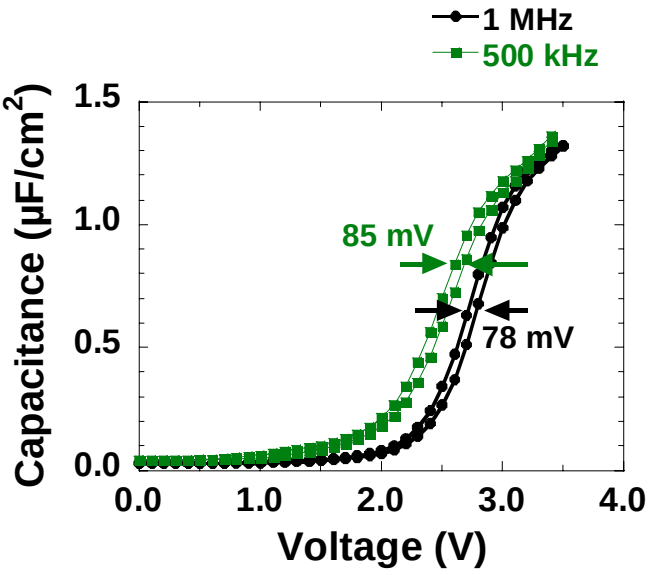


Figure 5.3. $Ge_{1-y}C_y$ (no Si cap) C-V hysteresis characteristics measured using forward and reverse sweeps at 1 MHz and 500 kHz. The hysteresis was 78 mV at 1 MHz and 85 mV at 500 kHz.

will be given in section 5.3, where a discussion of the influence of the TaN work function will be presented. The C-V hysteresis (see Fig. 5.3) measured using bidirectional voltage sweeps was 78 mV at a measurement frequency of 1 MHz and 85 mV at 500 kHz, with about 250 mV separating the 1-MHz curves and the 500-kHz curves. The hysteresis was smaller than or comparable to several of the published results on Ge high-κ/metal gate capacitors [72, 170, 175-177]. Figure 5.4 shows the capacitor leakage characteristics. The measured gate leakage in accumulation at a bias of +1 V was 3.3×10^{-5} A/cm^2, which is excellent for devices with comparable EOTs [72].

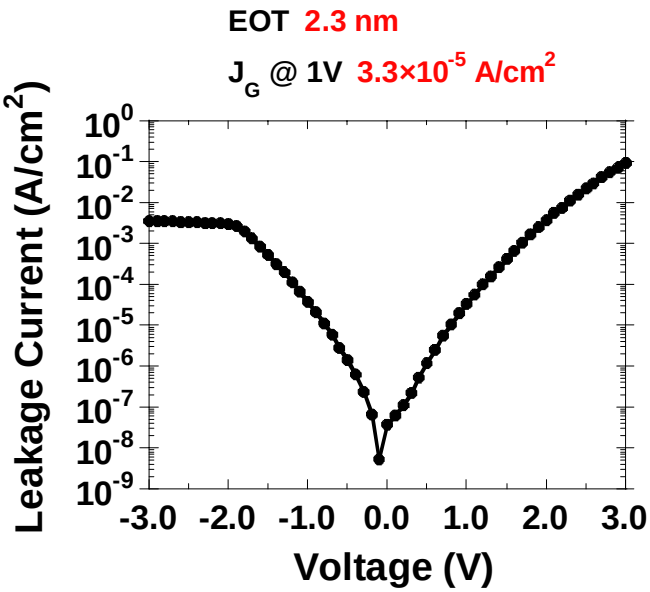


Figure 5.4. $Ge_{1-y}C_y$ (no Si cap) capacitor leakage characteristics before MOSFET processing. The measured leakage current density in accumulation (+1V) was 3.3×10^{-5} A/cm^2.

5.1.3 Gate Capacitance and Leakage of Buried-Channel *p*-MOSFET

Figure 5.5 shows gate capacitance-voltage (C_G-V_G) data after transistor processing for a buried-channel $Ge_{1-y}C_y$ *p*-MOSFET with an EOT of 1.9 nm. The Si cap layer for this device was 3 nm thick. The inset in Fig. 5.5 shows the gate leakage current density characteristic (J_G-V_G) in which the current was 1.4×10^{-5} A/cm^2 measured at a gate bias of +1 V in accumulation. The "kink" that is observed in the negative bias region (inversion) of the C_G-V_G curve results from the confinement of holes in the $Ge_{1-y}C_y$ layer due to the Si/$Ge_{1-y}C_y$ valence band offset. Figure 5.6 shows an energy band diagram for a Si/Ge/Si heterostructure *p*-MOSFET [178], showing the quantum well that is formed in the Ge layer due to the valence band offset with the Si substrate and the top Si cap layer.

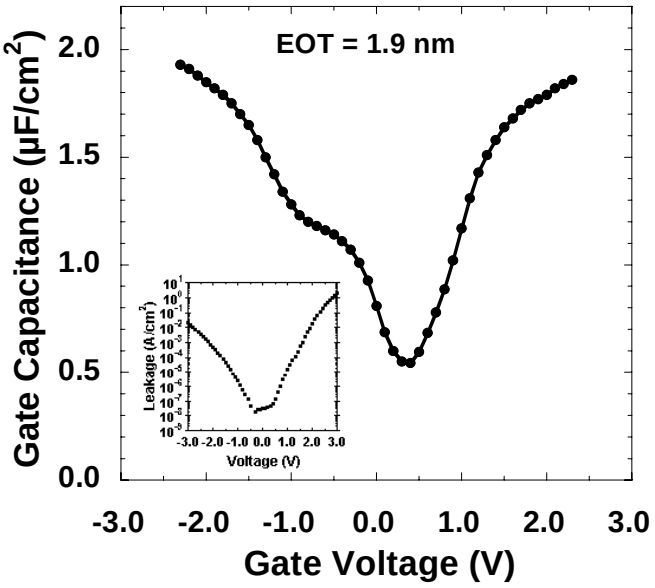


Figure 5.5. C_G-V_G and gate leakage (inset) characteristics for a buried-channel $Ge_{1-y}C_y$ *p*-MOSFET with a 3-nm-thick Si cap layer and an EOT of 1.9 nm.

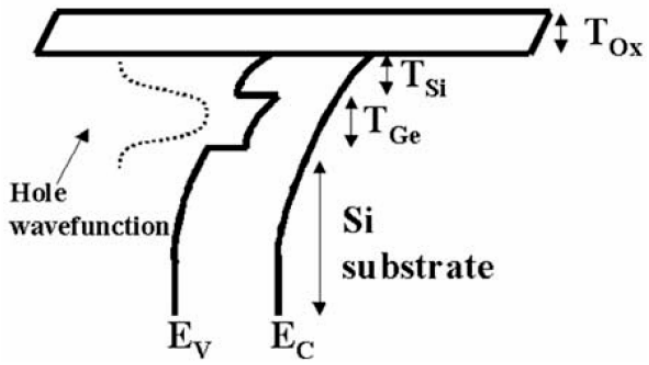


Figure 5.6. Band diagram of a Si/Ge/Si heterostructure *p*-MOSFET under inversion bias conditions [178].

The band gap for $Ge_{1-y}C_y$ should be nearly equivalent to that of a pure Ge layer since there is only a small amount of C in the film and the optical properties are similar to bulk Ge (see section 3.5). Since this is the case, we expect the band diagram to be very similar

to the depiction in Fig. 5.6, except perhaps for some differences due to the partially-relaxed nature of the $Ge_{1-y}C_y$.

The J_G-V_G curves for buried-channel, surface-channel, and Si control devices after transistor processing are compared in Fig. 5.7. The J_G-V_G curve for the buried-channel device is the same as the inset in Fig. 5.5. We immediately notice that the surface-channel devices (triangles) have a nearly two orders of magnitude increase in the gate leakage current density over the buried-channel (squares) and Si control (open circles) devices. This is due to the lack of proper surface passivation and the resulting updiffusion of GeO or Ge into the HfO_2 during processing [71, 179]. The impact on the transistor drive current characteristics will be seen later.

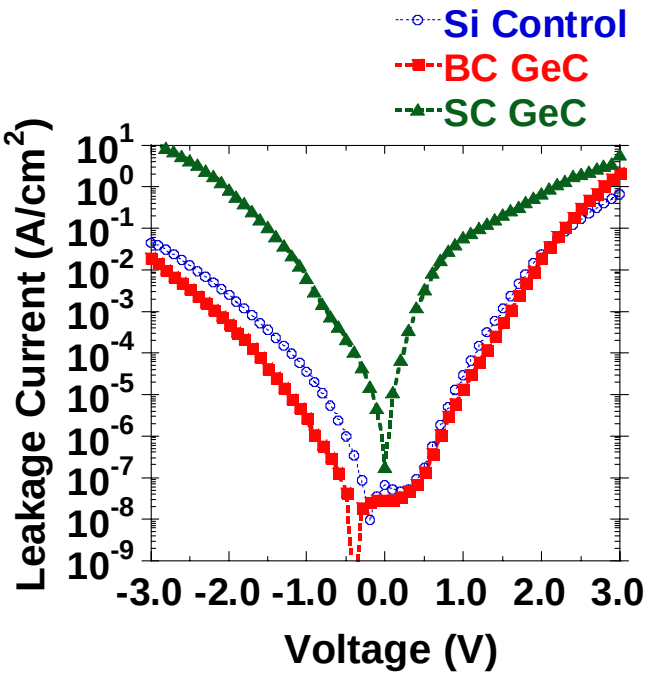


Figure 5.7. $Ge_{1-y}C_y$ J_G-V_G curves after *p*-MOSFET fabrication process. The surface-channel devices (triangles) exhibit increased gate leakage compared to the buried-channel (squares) and Si control (open circles) devices, which is presumably due to improper surface passivation and the resulting updiffusion of Ge or GeO into the HfO_2 during processing.

5.1.4 Transistor and Mobility Characteristics of Buried-Channel *p*-MOSFETs

Figures 5.8 and 5.9 show the drain current vs. drain bias (I_D-V_{DS}) and drain current vs. gate bias (I_D-V_{GS}) characteristics for a buried-channel $Ge_{1-y}C_y$ *p*-MOSFET compared to a Si control device (both with EOT=1.9 nm). The gate length, defined by the difference between the inner and outer radii of the ring-shaped gate, is 10 μm. The output characteristics for the buried-channel device (Fig. 5.8) show a 2× enhancement in the saturation drain current (I_{Dsat}) over the Si control. At a gate overdrive (V_{GS}-V_T) of 1 V, the I_{Dsat} for the buried-channel devices was 10.8 μA/μm, which is about twice as high as was reported by Ritenour *et al*. for surface-channel strained Ge devices on relaxed $Si_{1-x}Ge_x$/Si with the same gate length, gate overdrive, and a lower EOT [23]. The $Ge_{1-y}C_y$ buried-channel devices also showed a 1.8× enhancement in the linear drain current (I_{Dlin}) over the Si control at a V_{DS} of 50 mV (Fig. 5.9). Figure 5.10 shows that

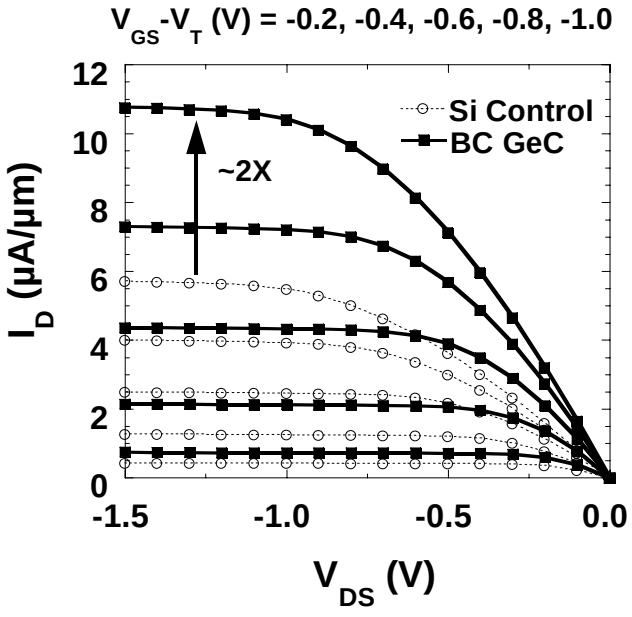


Figure 5.8. I_D-V_{DS} comparison of a buried-channel $Ge_{1-y}C_y$ *p*-MOSFET compared to a Si control device with the same EOT (1.9nm) and gate voltage overdrive.

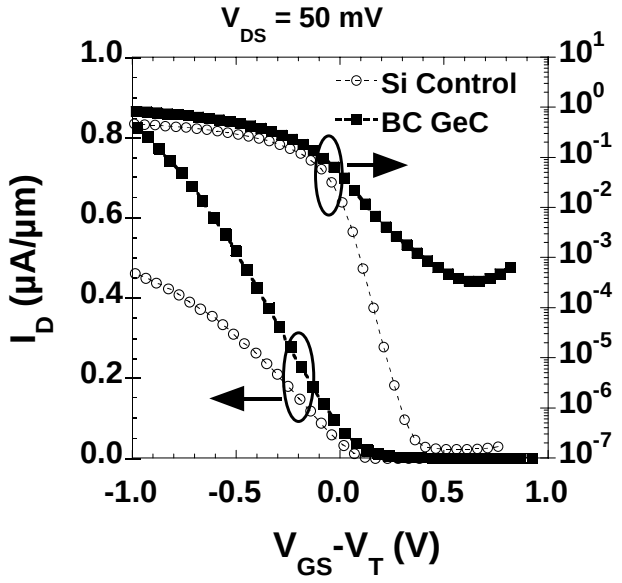


Figure 5.9. I_D-V_{GS} characteristics of a buried-channel $Ge_{1-y}C_y$ *p*-MOSFET compared to a Si control device plotted on both linear and log scale. The I_{on}/I_{off} ratio was greater than 5×10^4.

the devices had a 1.6× enhancement in the transconductance (G_m). The I_{on}/I_{off} ratio was greater than 5×10^4, but showed high subthreshold leakage compared to Si, which is partially due to band-to-band tunneling as a result of the lower bandgap of $Ge_{1-y}C_y$ [178].

Figure 5.11 shows the effective mobility (μ_{eff}) vs. vertical effective field (E_{eff}) curves for the buried-channel $Ge_{1-y}C_y$ *p*-MOSFET compared to the Si control device and the universal curve for Si [180]. Previously published μ_{eff} data for strained Ge on relaxed $Si_{1-x}Ge_x$/Si by Ritenour *et al*. [23] is also included in Fig. 5.10 for comparison. The mobility was extracted using the I_{Dsat} equation for MOSFETs with ring-type geometry [19]:

$$\mu_{eff} = \frac{I_{Dsat}}{C_{ox}} \frac{\ln(R_2/R_1)}{\pi(V_{GS}-V_T)^2}, \tag{5.1}$$

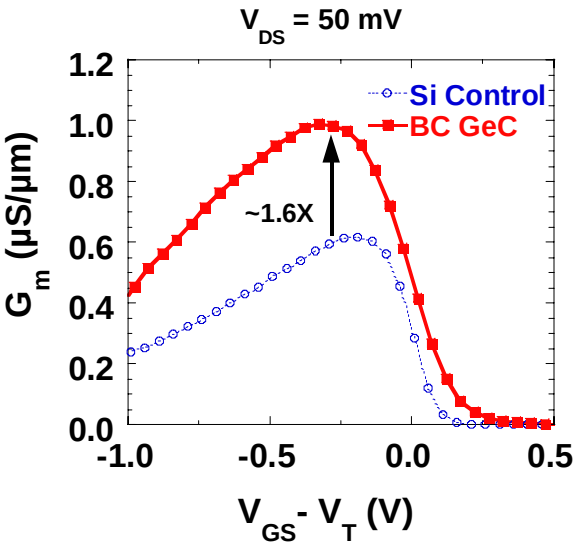


Figure 5.10. Transconductance (G_m) comparison of a buried-channel $Ge_{1-y}C_y$ *p*-MOSFET to a Si control device with the same EOT (1.9nm).

where R_1 and R_2 represent the inner and outer radii of the gate. E_{eff} was estimated according to

$$E_{eff} = \frac{1}{\varepsilon_{Ge}}\left(Q_d + \frac{Q_i}{3}\right) \tag{5.2}$$

where Q_d was calculated using the substrate doping, Q_i was estimated as $C_{ox}(V_{GS}-V_T)$, and ε_{Ge} was taken as $16\varepsilon_0$ (assuming $\varepsilon_{Ge} \approx \varepsilon_{GeC}$). As seen in Fig. 5.10, the buried-channel $Ge_{1-y}C_y$ *p*-MOSFET show 1.5× enhanced μ_{eff} over the universal curve for Si, an observation that is consistent with the drain current data. In addition, the hole mobility is slightly higher than was reported by Kar *et al.* for buried-channel, strained $Si_{1-x}Ge_x$ devices on Si using $Si_{1-x}Ge_x$ layers grown with the same UHV-CVD system that was used in this research [181].

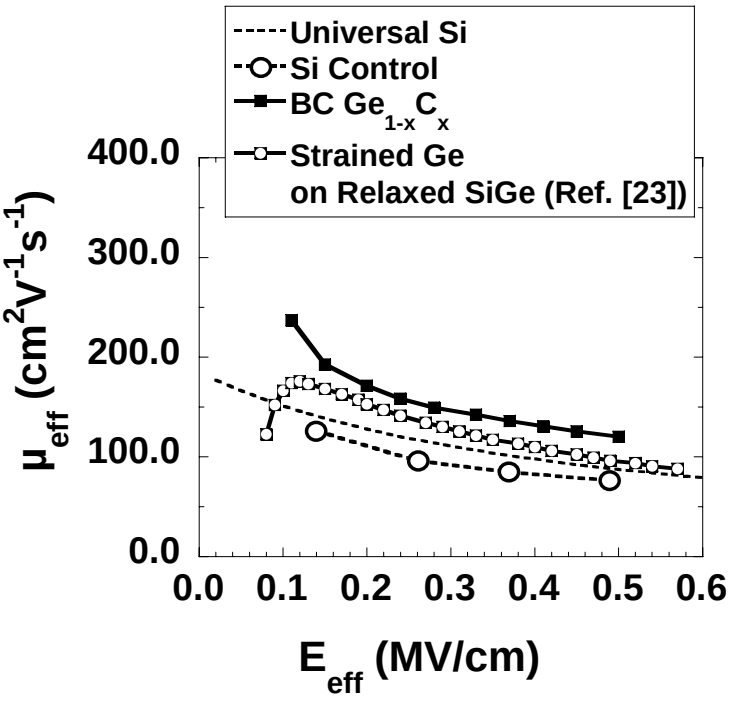


Figure 5.11. Effective hole mobility (μ_{eff}) of buried-channel $Ge_{1-y}C_y$ *p*-MOSFETs as a function of the vertical effective field (E_{eff}). Mobility data for surface-channel strained Ge on relaxed $Si_{1-x}Ge_x$/Si from Ritenour *et al*. [23] is included for comparison.

The transistor results presented above for buried-channel $Ge_{1-y}C_y$ *p*-MOSFETs demonstrate the feasibility of C incorporation into Ge grown on Si (100) wafers for achieving enhanced drive current. The enhanced mobility was realized in a Ge-on-Si architecture with a relatively simple CVD process, without the need for relaxed $Si_{1-x}Ge_x$ buffer layers [85-86], thermal annealing [93-94], defect-blocking at heterojunction interfaces [95-96], or surfactant-mediated epitaxy [83-84]. As mentioned earlier, surface-channel devices suffered degraded performance due to the lack of proper surface passivation to prevent Ge or GeO updiffusion into the high-κ dielectric. The next section

will give some electrical results for surface-channel $Ge_{1-y}C_y$ *p*-MOSFET devices and provide further explanation of the possible mechanisms for the degradation.

5.2 SURFACE-CHANNEL GERMANIUM-CARBON *P*-MOSFETS

5.2.1 Transistor and Characteristics of Surface-Channel *p*-MOSFETs

Figure 5.12 shows the output characteristics for a surface-channel $Ge_{1-y}C_y$ *p*-MOSFET compared to a Si control device with the same EOT (1.9 nm). The gate length is 10 μm. We see that the surface-channel $Ge_{1-y}C_y$ device exhibits nearly 3× higher I_{Dsat} than the Si control, but we also notice that the $Ge_{1-y}C_y$ device shows non-ideal behavior in the saturation region. The drain current continues to increase for increasing

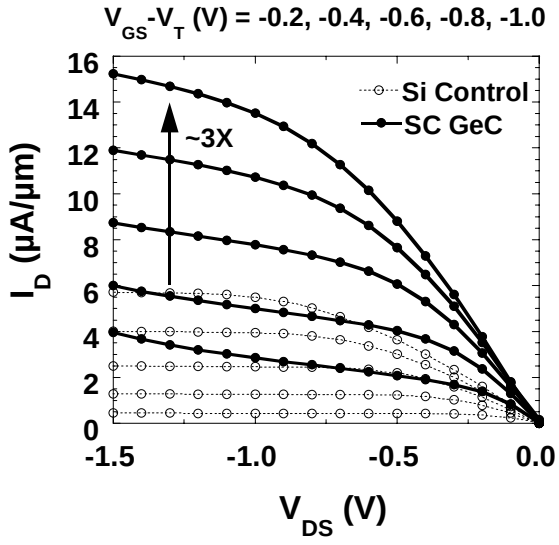


Figure 5.12. I_D-V_{DS} comparison of a surface-channel $Ge_{1-y}C_y$ *p*-MOSFET compared to a Si control device with the same EOT (1.9nm) and gate voltage overdrive. The devices show non-ideal behavior in the saturation region.

V_{DS}, and the slope is the same for all gate biases. This suggests that the surface-channel device has some resistor-like characteristics, probably indicative of a poor $Ge_{1-y}C_y/HfO_2$ interface. The early work by Chui *et al*. on surface-channel Ge *p*-MOSFETs showed I_D-V_{DS} characteristics that looked similar to the data shown in Fig. 5.12, even though the thermal budget was kept below 400 °C during the entire process [19]. Given this non-ideal behavior, reliable mobility numbers for the surface-channel devices cannot be obtained.

Figure 5.13 shows the linear I_D-V_{GS} curves for the surface-channel $Ge_{1-y}C_y$ device compared to the Si control, showing both the subthreshold characteristics and the linear I_D, as in Fig. 5.9. We see that the subthreshold leakage current for the surface-channel devices is extremely high with an I_{on}/I_{off} ratio of only 10^2. This can again be attributed

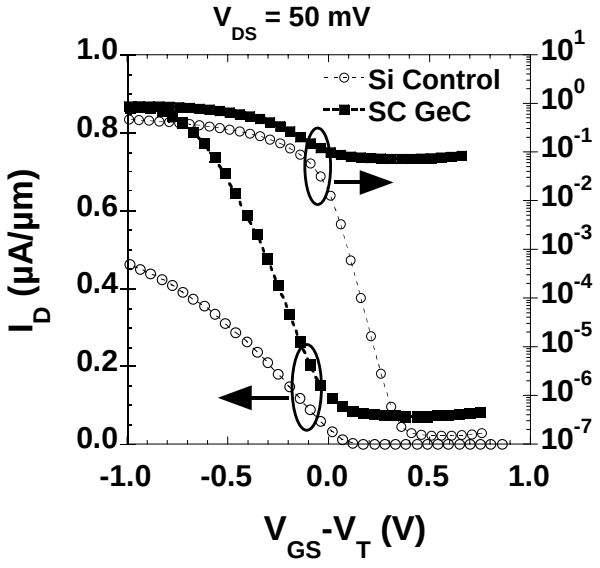
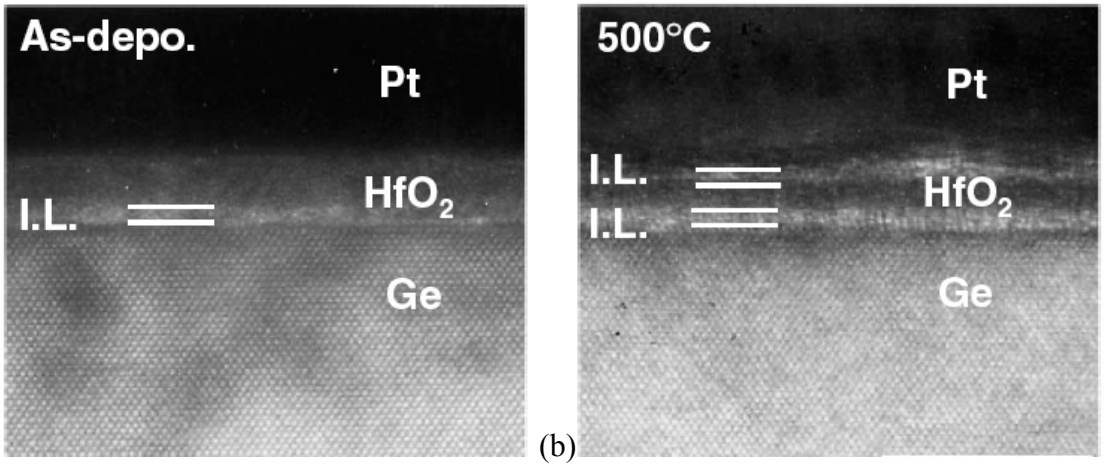


Figure 5.13. I_D-V_{GS} comparison of a surface-channel $Ge_{1-y}C_y$ *p*-MOSFET compared to a Si control device plotted on both a linear and a log scale. The surface-channel $Ge_{1-y}C_y$ devices show very high subthreshold leakage current.

to a poor $Ge_{1-y}C_y/HfO_2$ interface. To provide further insights into the mechanisms behind this degradation, the next subsection will highlight past research on the role of surface passivation of Ge substrates with HfO_2 dielectrics.

5.2.2 Mechanisms for Degradation in Surface-Channel *p*-MOSFETs

Researchers at the Toshiba Corporation have made significant progress in the effort to understand the role of GeO desorption on gate leakage increases in surface-channel Ge MOSFETs with HfO_2 dielectrics [182]. Figure 5.14 shows cross-sectional TEM images of a bulk HfO_2/Pt gate stack on bulk Ge before and after a 500 °C, 30 min. anneal in N_2, as shown by Kamata *et al*. [182]. In Fig. 5.14(a) we see that the as-deposited sample shows an interfacial GeO layer. When the sample is annealed, GeO diffuses into the HfO_2 and an additional interfacial layer forms at the interface with the



(a) (b)

Figure 5.14. Cross-sectional TEM images of a HfO_2/Pt gate stack on a bulk Ge wafer, both (a) before and (b) after a 500 °C, 30 min. anneal in N_2, as shown by Kamata *et al*. [182]. The annealed sample shows significant degradation of the HfO_2 layer and the formation of an additional interfacial layer with at the interface with the gate metal.

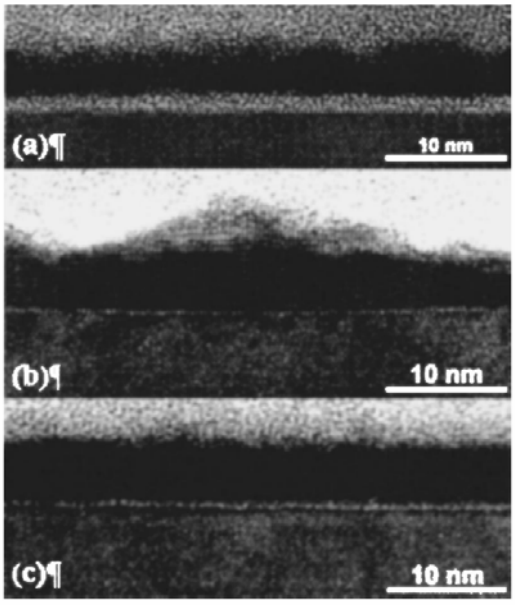


Figure 5.15. Cross-sectional TEM images of HfO_2 deposited on (a) Si, (b) Ge, and (c) Ge with NH_3 annealing for surface nitridation [71]. The surface-nitrided sample shows a higher quality dielectric.

gate metal. The structure of the HfO_2 is severely degraded (Fig. 5.14(b)). Interestingly, Kamata *et al*. noted that ZrO_2 dielectrics showed improved annealing behavior compared to HfO_2 [182]. Nevertheless, this result from the Toshiba group helps explain why the surface-channel $Ge_{1-y}C_y$ *p*-MOSFETs with HfO_2 dielectrics showed higher gate leakage (Fig. 5.7) and degraded transistor behavior (Figs. 5.12 and 5.13).

Similar TEM results were reported by Van Elshocht *et al*. who examined the effect of surface nitridation on bulk Ge wafers before HfO_2 deposition [71]. No additional annealing was done after HfO_2 deposition, but the deposition temperature of the HfO_2 was 485 ºC. Figure 5.15 shows images for HfO_2 deposited on Si, Ge, and NH_3-annealed Ge. From the TEM images we see that the HfO_2 films that were grown directly on Ge without surface nitridation showed much higher interface roughness

compared to the surface-nitrided devices (compare Figs. 5.15(b) and 5.15(c)). In addition, comparisons of TEM images with HfO_2 grown on Si wafers (Fig. 5.15(a)) revealed that the interfacial layer is much thinner on Ge. The authors conclude that both Ge diffusion and crystallization increase the interface (and/or surface) roughness, and that these can be mitigated using surface nitridation [71].

Finally, Lu *et al*. studied Ge diffusion and its impact on the electrical properties of HfO_2/Ge capacitors with TaN gates [179]. Figure 5.16 shows SIMS profiles for three Ge samples that underwent different surface preparation techniques, as given by Lu *et al*. [179]. The ion intensity ratio of Ge to Hf is plotted as a function of sputtering depth for samples with Ge native oxide (no surface preparation), HF last cleaning, and surface-nitridation. (The samples also underwent a post-metallization anneal at 600 °C in N_2 to evaluate the thermal stability.) It is immediately apparent in Fig. 5.16 that the surface-

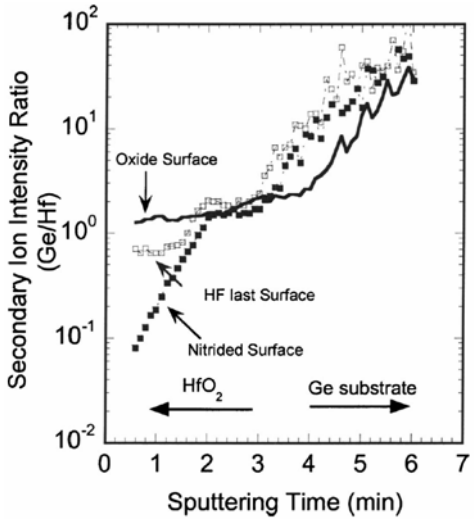


Figure 5.16. SIMS profiles showing the ratio of Ge and Hf ion intensities in Ge samples with native GeO_2 (no surface preparation), HF last surface preparation, and surface nitridation, as given by Lu *et al*. [179]. The surface-nitrided sample shows significantly reduced diffusion of Ge atoms into the HfO_2.

nitrided sample shows reduced Ge (or GeO) diffusion into the HfO_2 layer. In this case the authors proposed two mechanisms that could lead to Ge diffusion into the high-κ dielectric, both of which are related to the existence and the amount of GeO_2 on the surface. The first proposed mechanism was the following reaction taking place at the interface: $Ge+GeO_2 \rightarrow 2GeO$. The resulting volatile GeO (see also Kamata *et al*. [182]) was thought to diffuse through the oxide and into the high-κ dielectric during growth and post-deposition annealing, with the rate of diffusion enhanced by impurities in the HfO_2. The other proposed mechanism was the desorption of Ge-enriched volatile Hf-Ge-O complexes formed at the HfO_2/GeO_2 interface. One Hf atom would replace a Ge atom from the oxide since Hf is more electropositive [183]. Since surface nitridation consumes all of the GeO_2, both of the proposed mechanisms for Ge diffusion are suppressed.

It has been established, then, that Ge surfaces that are not properly treated lead to poor gate dielectric integrity, especially for HfO_2 dielectrics. This explains the degraded transistor behavior and higher gate leakage of the surface-channel $Ge_{1-y}C_y$ *p*-MOSFETs. Surface-nitridation techniques pose significant risks for thin (~20 nm) $Ge_{1-y}C_y$ layers because of strain relaxation, Si interdiffusion, and Ge etching by GeO formation and desorption. Accordingly, it is felt that epitaxial Si is the best solution for passivating thin $Ge_{1-y}C_y$ layers. In fact, merely depositing a few monolayers of Si is sufficient to passivate the surface [73]. Such thin epitaxial Si layers are usually oxidized during subsequent thermal processing, leading to surface-channel behavior [76].

In this research, however, Si cap layers with thicknesses between 3 and 5 nm were deposited, leading to buried-channel behavior. In buried-channel structures, the amount of coupling of the gate to the channel depends on the thickness of the Si layer. In the next section of this chapter, the effect of the Si cap layer on the electrical characteristics of the buried-channel $Ge_{1-y}C_y$ *p*-MOSFETs will be described.

5.3 IMPACT OF SILICON CAP LAYER ON GERMANIUM-CARBON *P*-MOSFETS

The impact of the Si cap layer thickness and the HfO_2 thickness on the $Ge_{1-y}C_y$ *p*-MOSFET drive current performance was evaluated by correlating electrical measurements with results from cross-sectional TEM. It was found that decreasing the Si cap layer thickness from 5 nm to 3 nm resulted in a 2× improvement in I_{Dsat}. The C_G-V_G characteristics show that the thickness of the Si cap has a greater impact on the measured capacitance in the buried-channel and strong inversion regions than in the accumulation region. The results presented below will provide additional insights into the buried-channel devices and underscore the importance of maintaining strict engineering controls on layer thicknesses to maintain high mobility enhancement.

5.3.1 Device Splits

Gate capacitance (C_G-V_G), gate leakage current (J_G-V_G), and transistor drain current data were measured on buried-channel $Ge_{1-y}C_y$ *p*-MOSFETs with different HfO_2 and Si cap layer thicknesses. Three $Ge_{1-y}C_y$ devices (denoted by A, B, and C) were characterized and compared. Devices A, B, and C had Si cap layer thicknesses of 5 nm, 3 nm, and 3 nm, respectively, and HfO_2 physical thicknesses of 5 nm, 5 nm, and 4 nm, respectively. The thicknesses of the layers were verified by cross-sectional TEM samples prepared from the same transistor gate stacks that were electrically characterized. The cross-sectional TEM image that was shown earlier (Fig. 5.1) came from device A. From that image we saw the presence of a thin SiO_2 interfacial layer between the Si cap and the HfO_2. The thickness of the SiO_2 interfacial layer (1 nm) was the same for all samples (A, B, and C). The device splits are summarized for convenience in Table 5.1.

Device	Si Cap Layer Thickness	HfO_2 Physical Thickness	SiO_2 Interfacial Layer Thickness	CET Measured at 100 kHz in Accumulation
A	5 nm	5 nm	1 nm	22 Å
B	3 nm	5 nm	1 nm	20 Å
C	3 nm	4 nm	1 nm	19 Å

Table 5.1. Summary of $Ge_{1-y}C_y$ device splits, showing the thickness of the Si cap layer, the HfO_2, the SiO_2 interfacial layer, and the capacitance equivalent thickness (CET) of the gate stack.

5.3.2 Analysis of Gate Capacitance-Voltage Curves

The C_G-V_G curves measured at 100 kHz for all three devices are shown in Fig. 5.17. The flat band voltage (V_{FB}) was shifted toward positive voltages for all devices, suggesting that a certain amount of fixed charge is still present in the oxide after forming gas anneal. We recall from section 5.1.2 that the MOS capacitors without a Si cap layer also exhibited a positive shift in V_{FB}.

Since the PVD TaN metal in this experiment did not undergo a high-temperature (≥ 950°C) post-metallization anneal, it believed that the metal work function on these devices is significantly lower than the expected mid-gap value of 4.6 to 4.7 eV, as reported in [184]. In fact, Kang *et al*. reported an as-deposited work function of only 3.6 eV for TaN that was deposited with identical process conditions as were used in this experiment [184]. It is assumed, therefore, that the ideal V_{FB} is negative on the lightly-doped *n*-type substrates used in this experiment, which means that the observed positive shift in the V_{FB} is probably due to oxide charge.

The capacitance equivalent thickness (CET) of the gate stack estimated from the accumulation region of the C_G-V_G curve was 22 Å, 20 Å, and 19 Å for devices A, B, and

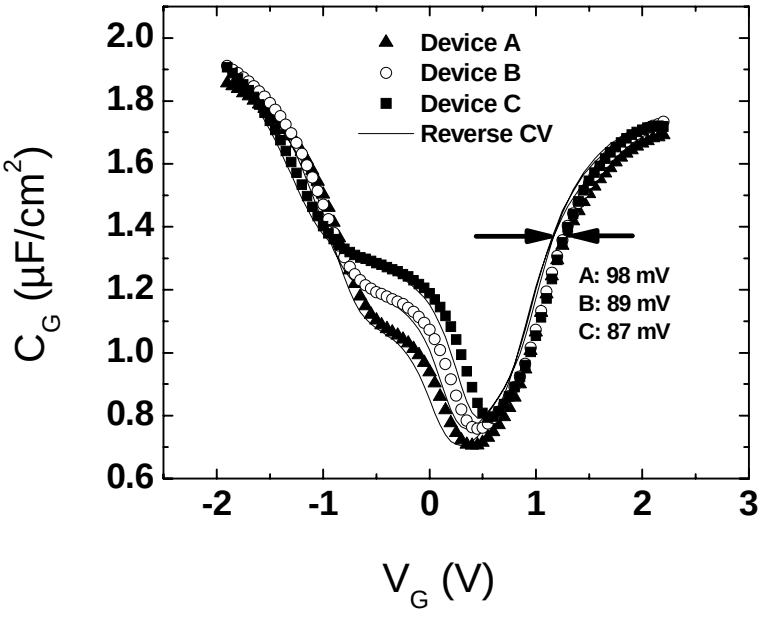


Figure 5.17. C_G-V_G curves of buried-channel $Ge_{1-y}C_y$ *p*-MOSFETs measured using forward and reverse sweeps at 100 kHz for devices A, B, and C. The hysteresis values measured in accumulation were 98 mV, 89 mV, and 87 mV, respectively.

C, respectively. Perhaps the most striking feature of the 100-kHz C_G-V_G data in Fig. 5.17 is the large differences among the three devices in the measured capacitance in the buried-channel region (V_G between -1V and 0V). This can be explained by the fact that device C had the thinnest Si cap layer (3 nm) and the thinnest HfO_2 layer (4 nm), so it is expected to exhibit the highest inversion capacitance in the buried-channel region. We note that the differences in the gate capacitance are more pronounced in the buried-channel region compared to the strong-inversion and accumulation regions. This confirms the expected impact of the Si cap layer thickness on the inversion charge density. In addition, since the relative dielectric constant of Si ($\varepsilon/\varepsilon_0$~11.7) is less than that of HfO_2 ($\varepsilon/\varepsilon_0$~25), we expect changes in the Si cap layer thickness to have a greater

impact on the gate capacitance in the buried-channel region than changes in the HfO_2 layer thickness (i.e., $\frac{\partial C_G}{\partial t_{Si}} > \frac{\partial C_G}{\partial t_{HfO_2}}$).

The hysteresis values measured in the accumulation region at 100 kHz for devices A, B, and C were 98 mV, 89 mV, and 87 mV, respectively (see Fig. 5.17). The J_G-V_G currents at V_{FB}-1V were 1.2×10^{-6}, 3.1×10^{-6}, and 2.5×10^{-6} A/cm^2, respectively (see Fig. 5.18). Figure 5.19 shows the C_G-V_G frequency dispersion characteristics for device A, for measurement frequencies of 100 kHz, 500 kHz, and 1 MHz. Three points on the C_G-V_G curve shown in Fig. 5.19 are labeled, corresponding to the capacitance values under strong inversion ("INV"), buried channel operation ("BC"), and accumulation ("ACC"). All three of the measured devices exhibited similarly-behaved characteristics,

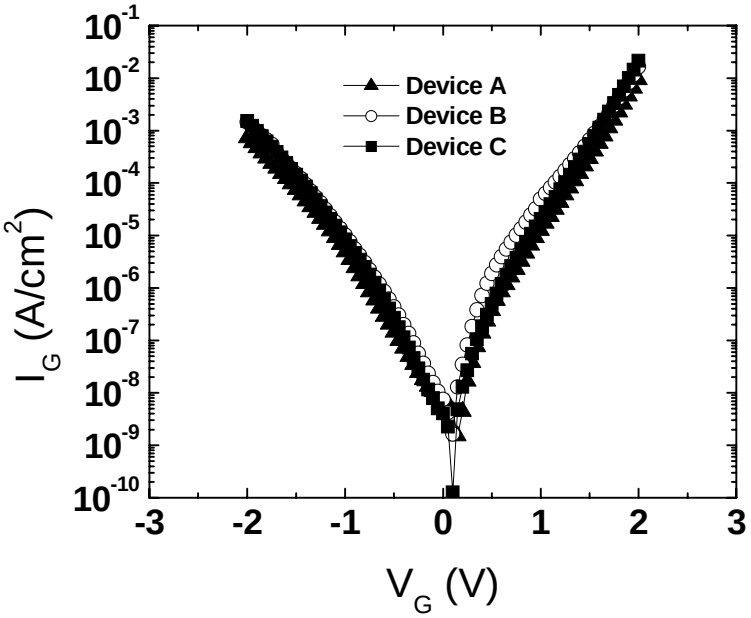


Figure 5.18. J_G-V_G leakage characteristics of buried-channel $Ge_{1-y}C_y$ *p*-MOSFETs. The measured leakage current density for devices A, B, and C were 1.25×10^{-5}, 4.91×10^{-5}, and 2.06×10^{-5} A/cm^2, respectively.

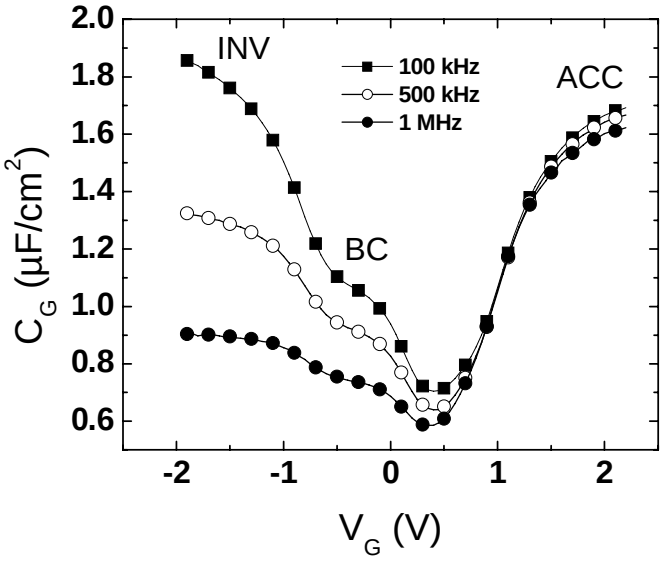


Figure 5.19. C_G-V_G frequency dispersion characteristics for device A, for measurement frequencies of 100 kHz, 500 kHz, and 1 MHz. Three points on the C_G-V_G curve are labeled, corresponding to the capacitance values under strong inversion ("INV"), buried channel operation ("BC"), and accumulation ("ACC").

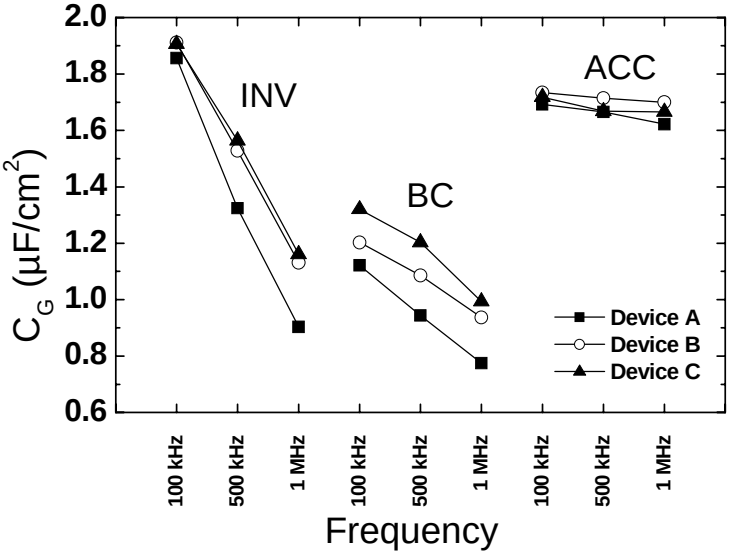


Figure 5.20. Gate capacitance values of all three devices (A, B, and C) at the three points of interest on the C_G-V_G curve ("INV," "BC," and "ACC") for each measurement frequency (100 kHz, 500 kHz, and 1 MHz).

with large frequency dispersion in inversion and minor frequency dispersion in accumulation. Figure 5.20 compares the gate capacitance values of all three devices (A, B, and C) at the three points of interest on the C_G-V_G curve ("INV," "BC," and "ACC") for each measurement frequency (100 kHz, 500 kHz, and 1 MHz). We see that the greatest frequency dispersion occurs under strong inversion ("INV"), since minority carriers are more susceptible to interface traps in surface-channel operation than in buried-channel operation. We also see that the effect of the Si cap layer thickness on the capacitance is more pronounced in the buried-channel region of the C_G-V_G curve ("BC"), which is again related to the effect of the Si cap on the inversion charge density.

5.3.3 Analysis of Transistor Characteristics and Mobility

The effect of the Si cap layer thickness on the *p*-MOSFET threshold voltage (V_T) during buried-channel operation is seen clearly in the I_D-V_{GS} plots shown in Figs. 5.21

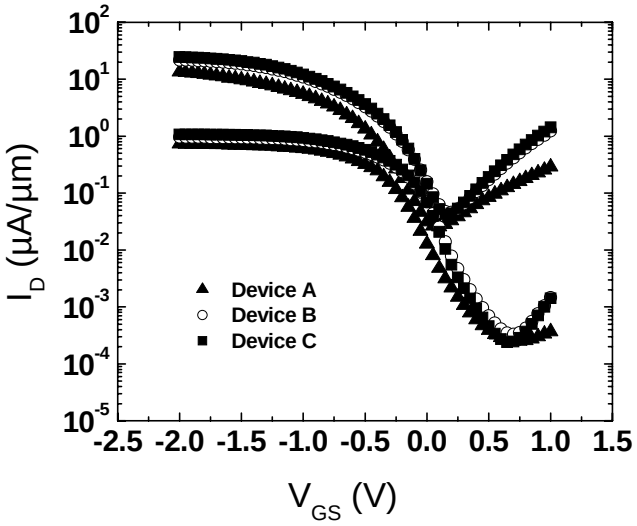


Figure 5.21. Linear (V_{DS} = 50mV) and saturation (V_{DS} = 1.2V) subthreshold characteristics for all three devices (A, B, and C).

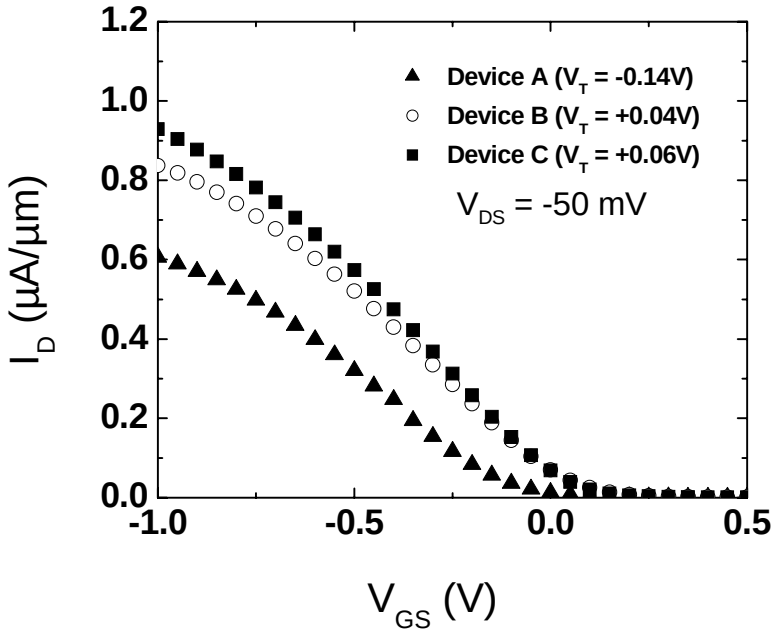


Figure 5.22. Linear I_D-V_{GS} characteristics for devices A, B, and C measured at V_{DS} = 50mV.

and 5.22. In Fig. 5.21, both the linear (V_{DS} = -50mV) and saturation (V_{DS} = -1.2V) subthreshold characteristics are plotted for all three devices (A, B, and C). The differences in V_T are seen even more clearly in Figure 5.22, which shows the linear I_D-V_{GS} characteristics. Device A has a higher V_T than devices B and C, since device A has a thicker Si cap layer. The calculated V_T using the extrapolation technique for device A was -0.14 V, while devices B and C had slightly positive V_T of +0.04 V and +0.06 V, respectively. The saturation drain current (I_{Dsat}) as a function of the gate overdrive (V_{GS}-V_T) is plotted in Fig. 5.23. We see that sample C, with the thinnest Si cap (3 nm), has nearly twice the drive current of sample A (5-nm Si cap). We note that the small change in the inversion capacitance as shown in Fig. 5.20 does not account for this difference alone, which means that sample C must have a higher-mobility channel.

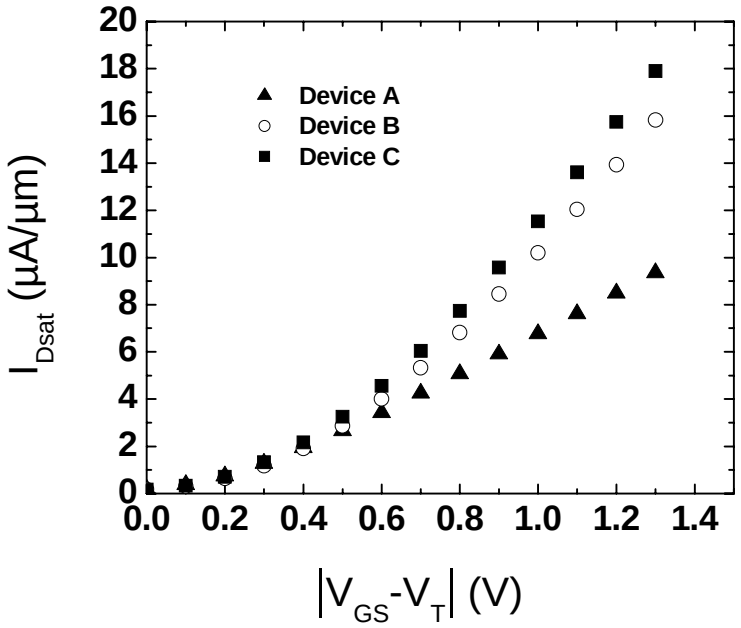


Figure 5.23. Saturation drain current (I_{Dsat}) for devices A, B, and C plotted as a function of the gate overdrive (V_{GS}-V_T). Device C has nearly twice the I_{Dsat} as device A for the same V_{GS}-V_T.

Figure 5.24 shows the effective mobility vs. vertical effective field (μ_{eff} vs. E_{eff}) curves for samples A, B, and C compared to the universal curve for Si. The effective mobility was calculated according to

$$\mu_{eff} = \frac{I_{Dlin} \ln(R_2/R_1)}{2\pi Q_i V_{DS}}, \tag{5.3}$$

where R_1 and R_2 represent the inner and outer radii of the gate, respectively; Q_i is the inversion charge; V_{DS} is the drain bias; and I_{Dlin} is the linear drain current (V_{DS} = 50 mV). Equation 5.3 was found by taking into account the device geometry, where the geometry

factor (L/W) is replaced by the equivalent ring-type geometry factor, $\frac{\ln(R_2/R_1)}{2\pi}$ [19]. E_{eff} was estimated according to

$$E_{eff} = \frac{1}{\varepsilon_{Ge}}\left(Q_d + \frac{Q_i}{3}\right) \tag{5.4}$$

where the depletion charge, Q_d, and the inversion charge, Q_i, were both extracted using the split *C-V* technique, and ε_{Ge} was estimated as $16\varepsilon_0$ (assuming $\varepsilon_{Ge} \approx \varepsilon_{GeC}$). As seen in Fig. 5.24, all three of the $Ge_{1-y}C_y$ *p*-MOSFETs show enhanced μ_{eff} over the universal curve for Si at low E_{eff}. As E_{eff} increases above 0.4 MV/cm, the mobility for device A drops below the universal curve, while devices B and C maintain some enhancement up to $E_{eff} \approx 0.6$ MV/cm. Since the Si cap layer is thicker for device A, we expect the Si cap to contain a larger proportion of the inversion charge at the same E_{eff} compared to devices B and C. If the mobility in the Si cap layer is much lower than the underlying $Ge_{1-y}C_y$, which we expect, then the Si cap layer acts as a parasitic channel that lowers the overall μ_{eff}. A competing phenomenon is surface roughness scattering, which is prevalent at high fields. (The competition between conduction in the Si cap vs. surface roughness scattering was thoroughly discussed by Lee *et al*. in their review of $Si_{1-x}Ge_x$ and Ge heterostructures [185].) We would expect devices B and C to suffer the greater loss in mobility at higher fields, since they have the thinner Si cap layer. However, since the Si cap layers for B and C are 3 nm thick, it is possible that surface roughness scattering is not significant enough to merge the mobility curves with that of device A at $E_{eff} \approx 0.6$ MV/cm. Krishnamohan *et al*. also observed improved μ_{eff} at the same E_{eff} in Ge-on-Si *p*-MOSFETs for thinner Si cap layers, but the improvements were lost in the surface-channel device [178]. We finally note that in the mobility analysis given above, we have

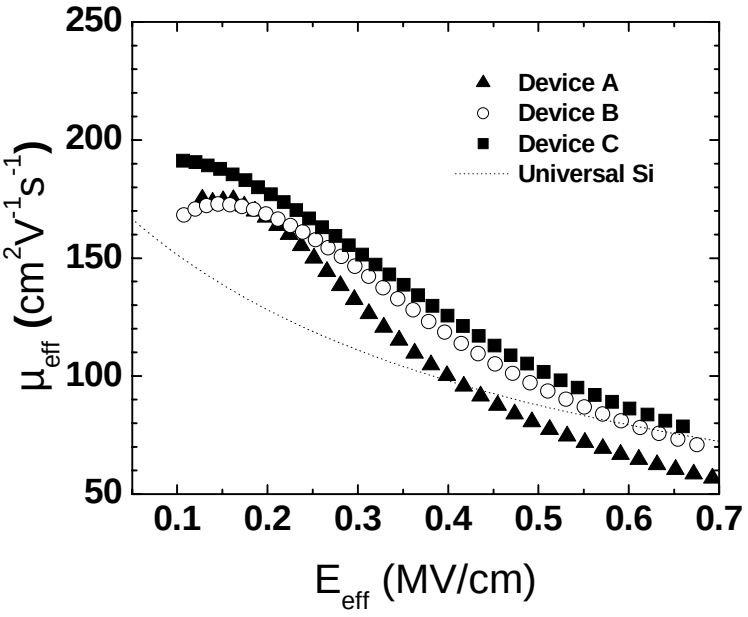


Figure 5.24. Effective mobility vs. vertical effective field (μ_{eff} vs. E_{eff}) curves for $Ge_{1-y}C_y$ devices A, B, and C compared to the universal curve for Si.

not considered the effect of charge scattering from the HfO_2 layer. For sputtered HfO_2 layers similar to those used in this work, the peak mobilities for *p*-MOSFETs were observed to be well below the universal curve for Si, even after forming gas annealing [186]. With an optimized gate stack using an improved high-κ deposition process, we expect an even greater hole mobility enhancement for $Ge_{1-y}C_y$ over Si.

5.4 SUMMARY

This chapter presented the electrical characteristics of MOS devices fabricated on $Ge_{1-y}C_y$ layers grown directly on Si substrates. Buried-channel devices ($Ge_{1-y}C_y$ with epitaxial Si cap layer) showed better performance than surface-channel devices since the

surface-channel devices did not receive surface treatment to prevent the formation and subsequent diffusion of GeO or GeO_2 into the HfO_2. The influence of the Si cap layer on the buried-channel devices was also examined, and it was found that the thickness of the Si cap has a significant impact on the drive current.

CHAPTER 6

CONCLUSION

6.1 SUMMARY AND CONCLUSION

When the era of scaling reaches its end, new innovations will become necessary to continue to deliver performance gains in CMOS integrated circuits. Process-induced strained Si has already become a mainstay of semiconductor technology, and high-κ dielectrics will almost certainly make their entrance as well (as gate leakage currents become too high to manage with traditional oxynitrides). Some debate still exists as to whether a high-mobility-channel such as $Si_{1-x}Ge_x$/Ge and III-V will ever be implemented, but it is certain that the option will become an increasingly serious consideration with each new technology node.

Germanium has drawn serious interest in the semiconductor research community for its compatibility with high-κ dielectrics and its high bulk mobilities compared to Si. Numerous processing challenges still need to be solved before Ge can be a serious competitor (or complement) for strained Si. Among those challenges lies the daunting task of integrating Ge layers on Si, which requires innovative deposition techniques. While strain-relaxed buffers have been the most successful method for reducing the crystal defect density, it has the disadvantage of high cost and intolerable process complexity. Other methods for integrating Ge on Si such as surfactant-mediated epitaxy and Ge-on-insulator have their own challenges.

This dissertation has described a method for incorporating Ge on Si by alloying the Ge layer with small amounts of C. As we have seen, the C drastically improves the crystal quality and allows for the direct deposition of Ge on Si. The C seems to preferentially locate near the interface with the Si substrate, which is advantageous since C atoms in the channel region would reduce the carrier mobility. We have seen that high-κ/metal gate $Ge_{1-y}C_y$ *p*-MOSFETs with enhanced hole mobility can be fabricated directly on Si substrates, which opens exciting new possibilities for Ge-based transistors.

6.2 RECOMMENDATIONS FOR FUTURE WORK

Figure 6.1 shows a C_G-V_G curve and output characteristics for a HfO_2/TaN $Ge_{1-y}C_y$ *n*-MOSFET. As seen in Fig. 6.1(a), the capacitor C-V curve behaves normally, with acceptable leakage (1.4×10^{-2} A/cm^2 at -1V) and reasonable interface trap density (5×10^{11} eV^{-1}cm^{-2}). We see in Fig. 6.1(b), however, that the transistor drive current is quite low (I_{Dsat} at V_{GS}-V_T=1V was 0.7 μA/μm for a gate length of 10 μm). As discussed earlier, Ge *n*-MOSFETs still suffer from low mobility, the reasons for which are not fully known at present. It is felt, therefore, that $Ge_{1-y}C_y$ *n*-MOSFETs can be explored after the causes for *n*-MOSFET mobility degradation in Ge are better understood.

In addition to exploring *n*-MOSFETs, short-channel behavior in $Ge_{1-y}C_y$ devices should also be investigated. However, very little has been published in the research literature on short-channel effects in Ge-based transistors. The main reason for this is that until very recently, Ge has only been investigated by university researchers who lack the advanced lithography tools and other process capabilities needed to fabricate short-channel transistors.

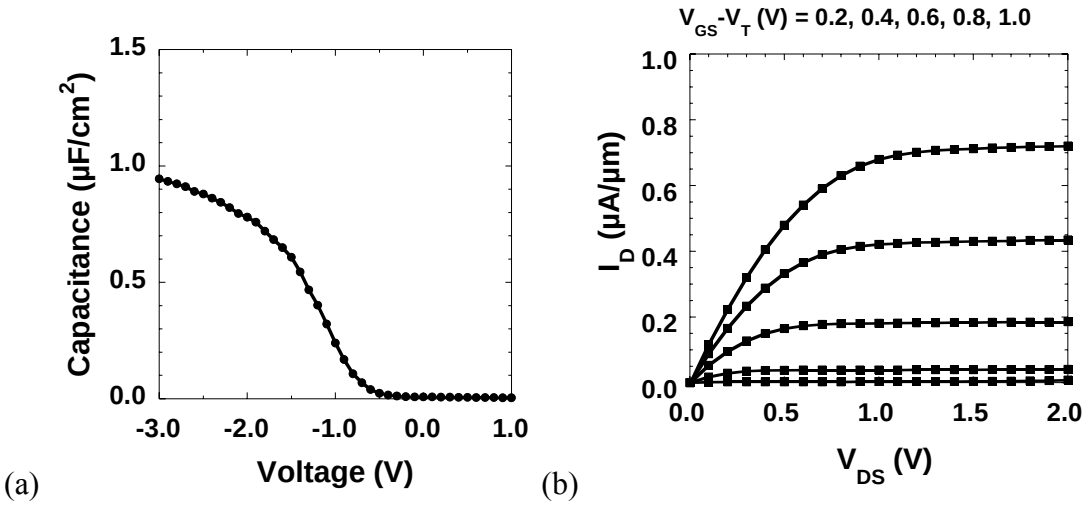


Figure 6.1. (a) C-V curve and (b) transistor output characteristics for a HfO_2/TaN $Ge_{1-y}C_y$ *n*-MOSFET.

Numerous other processing and materials-related issues with $Ge_{1-y}C_y$ layers are still not well understood. Dopant diffusion and activation, carbon-related defects, thermal stability/interdiffusion, and strain relaxation are areas that need further exploration. It is hoped that this research and the related publications will spawn increased awareness of the important role that C can play in high-mobility heterostructures fabricated on Si.

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