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A SEIR-Based ADC Built-In-Self-Test and Its Application in ADC Self-Calibration

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A SEIR-Based ADC Built-In-Self-Test and Its Application in ADC Self-Calibration

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REPORT

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Dedicated to my family.

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A SEIR-Based ADC Built-In-Self-Test and Its Application in ADC Self-Calibration

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The static linearity test is one of the fundamental production tests used to measure DC performance of analog to digital converters (ADCs). It comes with high test equipment cost. An ADC built-in-self-test (BIST) is an attractive solution. However the stringent linearity requirement for an on-chip signal generator has made it prohibitive. The stimulus error identification and removal (SEIR) method has greatly reduced the linearity requirement. However, it requires a highly stable voltage offset, which remains a daunting task. This work exploits the inherit capacitive sample-and-hold circuit used in various ADC architectures to inject offset with very good constancy. A 16-bit successive approximate register (SAR) ADC with the proposed BIST scheme is modeled and simulated in Matlab to prove its validity. The results show that the estimation error on the maximum INL is less than 0.07 LSB. This BIST solution is then naturally extended to the calibration of an ADC. It is shown missing codes of such ADC can be effectively estimated and calibrated out.

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Chapter 1

Introduction

CMOS scaling has continuously cut down chip manufacturing costs. It has also made possible the integration of a complicated system-on-chip (SOC). Nowadays, with the exponential increase in the number of transistors on a single chip, testing has become a major cost driver that is often comparable to the manufacturing cost. Structural-based test methods like scan automatic-test-program-generation (ATPG) and logic built-in-self-test (BIST) have greatly reduced the test cost of digital circuit. By contrast, the test cost of analog and mixed-signal (AMS) circuits has not decreased as much. They still rely heavily on specification-based test methods that need expensive mixed-signal testers. This is partly due to the lack of a widely acceptable AMS fault model. More importantly, it is because of their inherently different test requirements. While digital circuits only need to be checked against connection and speed, AMS circuit performance can only be evaluated through specification-based tests.

The analog-to-digital converter (ADC) is one of the most widely used AMS IP blocks in an SOC. It has complex performance metrics including static (DC) and dynamic (AC) specifications. Among those many static speci-

fications, the differential nonlinearity error (DNL) and integrated nonlinearity error (INL) are often the most difficult to measure. Production test of the above specifications is primarily based on two test techniques: the servo loop method and the histogram method [1]. The servo loop method suffers from the need of an accurate digital-to-analog converter (DAC) and a long testing time. By contrast, the histogram method is simpler and faster. Hence, it is the current dominant test method. Nevertheless, it requires an expensive mixed-signal tester with high test development-and-debug costs. This drawback motivates researchers to develop a low-cost histogram-based ADC BIST solution that obviates the need for the mixed-signal tester. Identifying a feasible ADC BIST solution and improving its performance are the focuses of this work.

The first section of this chapter reviews the definition of ADC static linearity. The following section reviews the mainstream test techniques. The last section presents the approaches of this work on addressing current challenges.

1.1 ADC Static Linearity Specification

There are several common static linearity specifications on almost every ADC data sheet. Before giving definitions of each parameter, some common ADC terminology is reviewed below to facilitate the definitions.

1.1.1 ADC Common Terminologies

An n-bit ADC converts a continuous time signal into a discrete time and discrete amplitude signal with $2^n(0, 1, \ldots, 2^n - 1)$ code bins [2]. The ideal code bin width (Q), which is same as least significant bit (LSB) is defined as:

$$Q = LSB = \frac{FSR}{2^n} \tag{1.1}$$

Where FSR is the full scale range of the ADC, sometimes it is called V_{FS}. When a single-ended ADC is in discussion, which is the case in this research, we often use the term V_{ref} to indicate the reference voltage of the ADC and it is the same as FSR or V_{FS}.

The code transition level $T[k]$ for code bin $k, k \in [1, 2^n - 1]$ is defined as the value of the ADC input where the transition happens between two adjacent code bins $k-1$ and k. Code bin width $W[k], k \in [1, 2^n - 2]$ is defined as the difference between code transition levels:

$$W[k] = T[k+1] - T[k] \tag{1.2}$$

Ideal code transition level $I[k]$ for code bin $k, k \in [1, 2^n - 1]$ is where the code transition happens from bin $k-1$ to k for an ideal ADC. The alternate definition of ideal code width Q can be found as below for all code bins:

$$Q = I[k+1] - I[k] \tag{1.3}$$

The above basic ADC terminology allows us to define ADC static parameters. Figure 1.1 illustrates the above terms with the assumption of terminal

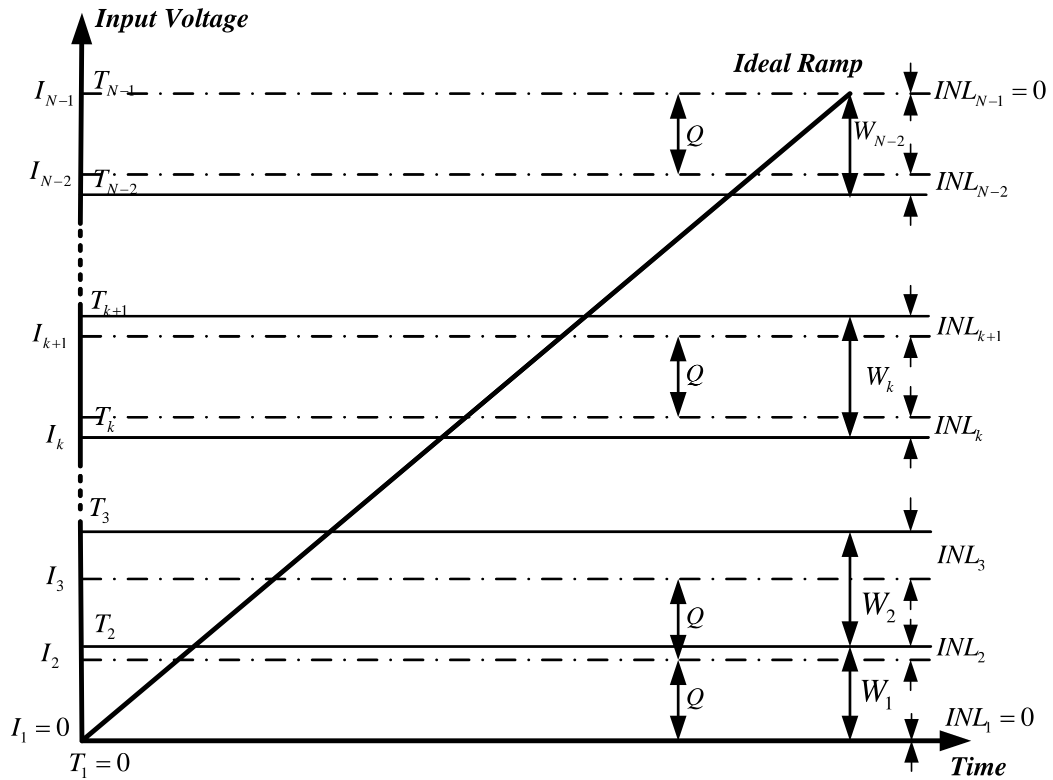


Figure 1.1: ADC Common Terminologies

based INL definition. This will be explained in detail in Section 1.1.2. N is equal to 2^n in the figure.

1.1.2 Offset and Gain Error

There are independently based (also known as best fit) and terminal based definitions for offset error and gain error. Independently based offset and gain error are defined as the values applied to the input as offset and gain to minimize the mean squared deviations between output values. The terminal

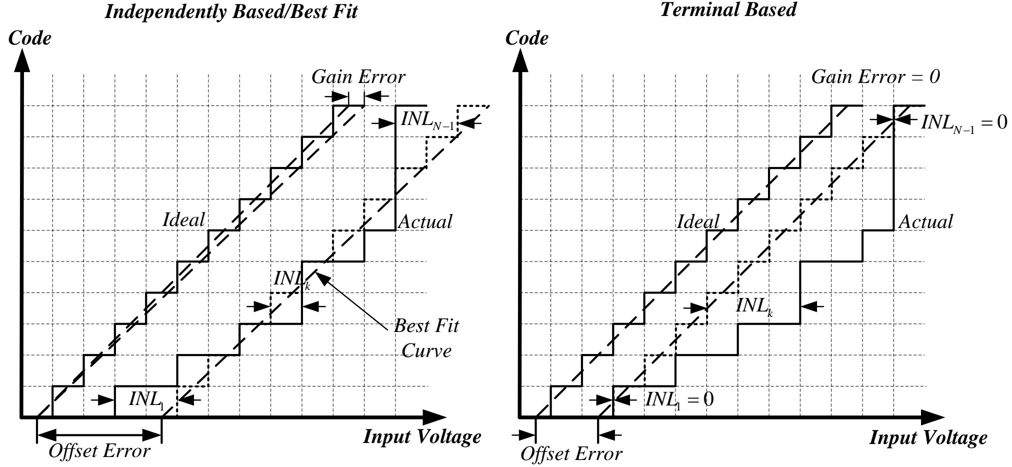


Figure 1.2: Independently Based vs. Terminal Based

based offset error and gain error are defined as the values applied to the input as offset and gain to achieve a zero deviation at the start and end terminals. In the terminal based definition, offset error is often called zero scale error and gain error is equal to full scale error minus zero scale error.

1.1.3 Differential Nonlinearity Error

Differential nonlinearity error (DNL) is defined as the difference between specified code bin width and ideal or average code bin width divided by ideal or average code bin width for $k \in [1, 2^n - 2]$.

$$DNL[k] = \frac{W[k] - Q}{Q} \tag{1.4}$$

Missing codes is an important ADC property, which can be derived from DNL. It happens when $W[k] = 0$, which is equal to $DNL[k] = -1$. The number of missing codes is often calculated by counting the number of bins that meet

the definition.

1.1.4 Integral Nonlinearity Error

Integral nonlinearity error (INL) is defined as the difference between the ideal code transition levels and measured code transition levels after the offset and gain errors have been corrected where $k \in [1, 2^n - 1]$.

$$INL[k] = \frac{T[k] - I[k]}{Q} \tag{1.5}$$

Thus INL can be different depending on which definition is used i.e. independently based or terminal based. This is illustrated in Figure 1.2. An independently based definition usually results in a better number (smaller INL error) and it makes more sense when the ADC under test has severe nonlinearity error. If it is not the case, INL error is expected to be close to both definitions. Since terminal based INL error is typically easier to measure than independently based case INL error, it is a more popular choice. In this work, we use terminal based definitions.

In practice, INL is often calculated as the integral of the DNL on prior bins with $k \in [2, 2^n - 1], INL[1] = 0$:

$$INL[k] = \sum_{i=1}^{k-1} DNL[i] \tag{1.6}$$

1.2 ADC Static Linearity Test Overview

As shown in the last section, all of the static errors can be calculated based on known code transition levels. Thus, the following test methods have

been developed to locate each code transition level.

1.2.1 Servo Loop Test Method

The servo loop test method is a classic ADC test method. It is also sometimes called a feedback loop test [2]. There are various kinds of implementations but the concept remains the same. An accurate digital to analog converter (DAC) generates analog input to be sent to the ADC for conversion. The conversion data is therefore compared to the input of the DAC. Incrementally changing the input value minimizes the difference. Eventually a transition point will be found out of a specific code. Repeating the process for each code, all transition points will be discovered.

There are a few drawbacks to this method [1]. The test accuracy highly depends on the resolution and accuracy of the DAC. Random noise will have a big impact on its accuracy as well. Plus, long test time is expected because of the settling time requirement of the DAC being used. Because of the above drawbacks, the servo loop ADC test method is rarely used in production nowadays. Instead, the histogram tests are dominant.

1.2.2 Histogram Test

The histogram test is based on the histogram of code occurrences from ADC conversions of a linear input. The principle of this test method is that an ideal ADC will yield known code density (hits per code). The deviation between the actual code density and ideal code density can be directly translated

into DNL and INL performance.

Let $H[i]$ represent the occurrence of code $i \in [1, 2^n - 2]$ and let H_{total} equal the sum of code occurrences of all code bins, then we have below equations where $T[1] = I[1] = 0, k \in [2, 2^n - 1]$:

$$H_{total} = \sum_{i=1}^{2^n-2} H[i] \tag{1.7}$$

$$T[k] = \frac{\sum_{i=1}^{k-1} H[i]}{H_{total}} \times FSR \tag{1.8}$$

Applying the above equations along with equations (1.2),(1.4),(1.5), we will be able to calculate DNL and INL accordingly.

Gain error (G) can be calculated as the ratio between average hits per code (H_{avg}) and ideal hits per code (H_{ideal}), see equations below:

$$H_{avg} = \frac{H_{total}}{2^n - 2} \tag{1.9}$$

$$G = \frac{H_{ideal}}{H_{avg}} \tag{1.10}$$

Offset error (Z) can be found as average distance between gain error compensated $T[k]$ and $I[k]$ as:

$$Z = \frac{\sum_{i=1}^{2^n-1} (T[k] \times G - I[k])}{2^n - 1} \tag{1.11}$$

In most product testing environments, a ramp input is typically the input that is chosen. There are several advantages to the ramp histogram test

method. First, each code bin will have multiple hits. With more hits per code, noise can be greatly suppressed. Secondly the performance parameters are defined based on an ideal ramp thus obtaining them is fairly straightforward as explained above. Thus the ramp histogram test method is the dominant test method used to extract static linearity parameters in a production test environment.

However, there are some disadvantages associated with this method as well. The measurement resolution, accuracy and confidence level are greatly dependent on the number of hits per code. In the case where noise presence is significant, a great number of hits per code may be needed to achieve accurate and consistent measurements. This will be directly translated into long tester time and here fore high cost. Another issue this method faces is the linearity requirement of the input ramp. To guarantee a good measurement of the performance of an n-bit ADC, we need to ensure a highly linear input ramp from the DAC with at least $(n+2)$-bit linearity. With a high resolution ADC, this requirement is often difficult to meet.

Some alternate approaches have been proposed to meet the stringent linearity requirement. The delta sigma DAC which has superior linearity is exploited to generate a sine wave as the test stimuli [1]. It is included as part of the IEEE ADC test standard [2]. However a much larger number of hits per code is needed to achieve a good code density analysis since a sine wave does not have an even distribution like a ramp does. The need for a larger number of hits per code makes this method less appealing as a production test solution

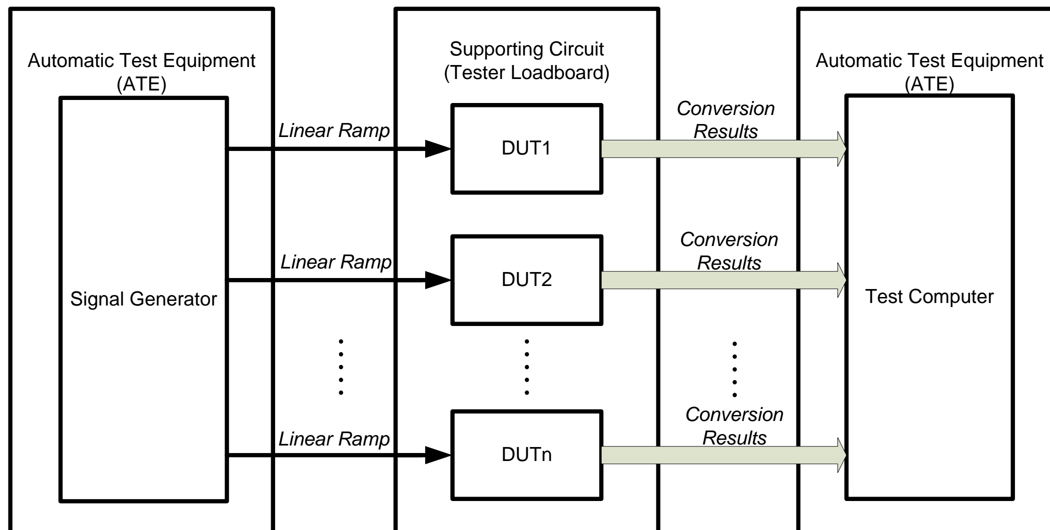


Figure 1.3: ADC Test System Block Diagram

than the ramp histogram method.

1.2.3 A Look at Real ADC Production Test

Figure 1.3 illustrates a typical ADC test subsystem during product testing. The linear ramp is generated from a programmable mixed signal generator which is part of the automatic test equipment (ATE). The signal generator module is often times one of the most expensive modules of the mixed signal ATE system.

A supporting ATE circuit board needs to be designed to hook up the test signal generator to the device under test (DUT) as well as voltage supplies, clock signals and digital capture buses. Decoupling capacitors are major components added on the circuit board. Sometimes a low pass RC filter is

also put in place to suppress noise on signal input and voltage supplies. After conversion, the data is collected and stored in the memory of the tester for the computer to analyze to calculate performance metrics as described earlier. The large amount of data transmitted between the device under test (DUT) and tester often consumes significant time (often longer than the actual ramp time) thus contributing significantly to cost.

There are some practical challenges associated with current production test implementations. First, the mixed signal ATE system is very expensive and is a significant investment for any semiconductor company. Much thoughts has been put into fully utilizing the system. However, due to various types of ADC designs with different resolutions, speed and accuracy requirements, it is often difficult to choose one system to fit all products, which inevitably drives the cost up. Furthermore, the number of signal generators is limited due to the cost, this often times prevents us from achieving high test parallelism. Lastly, the test development and debug cost of ADC on such a complex system is high compared to digital testing.

The above challenges have led researchers to look into possible alternatives. An on chip ADC BIST solution that can test ADC performance on chip without the need for expensive ATEs is no doubt the ultimate goal to solve all of the above issues.

1.3 ADC BIST Overview

As it becomes apparent that cost and complexity of testing ADCs is increasing rapidly with high resolution ADCs, an ADC BIST solution is looking much more attractive than ever. Before diving into reviewing available ADC BIST proposals, in the first section of this chapter we will review the fundamentals of analog BIST first. Therefore we can use these principles to measure the quality of existing solutions. The next section will then focus on the SEIR based ADC BIST solution to review its fundamentals. The last section will present a characterization of estimation error with different noise input levels, number of coefficients, resolution, etc.

1.3.1 Review of Analog BIST Principles [9]

The basic idea of analog BIST is to bring the signal generation, data analysis, and pass/fail determination functions on-chip. The greatest challenge of designing analog BIST circuits is the accuracy of the BIST circuit itself. The ATE usually needs to be an order of magnitude more accurate than the circuit under test.

The first key principle of an analog BIST circuit is that it should be easily testable itself. It is fairly easy to understand that all circuit components within the chip need to be thoroughly tested including the test circuit itself. Furthermore, only after the functionality or performance of the test circuit has been checked can the circuit be used to test other components. However, testing it should not require an advanced mixed-signal tester. Otherwise, the

benefit of inserting a BIST circuit has been significantly reduced. This means that it is desirable to use as much digital circuitry as possible to create an analog BIST circuit.

Another key principle is that a BIST circuit needs to have better yield than the circuit under test while achieving the required accuracy. It was pointed out that a previous case study found that only 70 percent of small analog-BIST circuits on a test chip achieved the required measurement accuracy [9]. This will inevitably impact the usefulness of a BIST circuit. This leads to the trend to design the BIST circuit as simple and small as possible so that yield is easy to guarantee.

The third key principle is that the BIST circuit cannot compensate for the imperfections of the circuit under test itself [10]. Loop back tests have been proposed and implemented in ADC and DAC test, transmitter and receiver test. if those design blocks appear on the same chip. A significant problem of loop back testing is it is difficult to distinguish between errors in the block under test and block used as stimuli. Worst of all is if a defect or performance issue in the block under test is compensated for by the block used as stimuli the result is test coverage loss.

The last principle of analog BIST is that it must allow direct correlation between the BIST output and the traditional test it replaces. This reflects the reality that a customer needs to be assured that the BIST circuit is able to provide same test coverage and accuracy as traditional specification based test does. A structural-based BIST solution may make this task harder than

the specification based BIST solution which will be reviewed next. As its name suggests, specification-based BIST tries to design in the test stimuli and response analysis on chip, therefore the solution is essentially the same as the ATE specification test.

1.3.2 Structural-Based ADC BIST

Structural-based BIST methods focus on testing the individual components of the circuit. The fundamental thought behind this is that if all components are non-defective or meeting spec, then the whole system that is created by those sub-circuits is proven out. Structural-based BIST of analog and mixed-signal designs have not gained in popularity like their digital counterparts. As mentioned earlier, part of the reason is that there is no widely accepted analog fault model.

In the case of ADC BIST, the capacitive DAC that has been widely used in SAR ADCs is studied the most. Various self tests or self calibration mechanisms are proposed. In [14], a self calibrating scheme is proposed by measuring error voltage due to capacitor mismatches. The mismatches can be used as coefficients to calibrate the digital output later, or it can be used to compare against thresholds to determine if the mismatch is large enough or is changed significantly enough to be considered a defect.

There are several drawbacks to this structural-based ADC BIST method. It has a dependency on specific ADC architectures. The above capacitor mismatch calibration mechanisms cannot be used for other types of ADCs which

do not have capacitive DACs. It is true that capacitor mismatch is the dominant contributor to linearity error of SAR ADCs. However, the comparator and the signal path are also important parts of the system that contribute to linearity error which are often not tested by structural BIST. The last drawback is that the performance is not directly derived from this test. A significant amount of correlation is needed to find the link between the specification and test results. Since they are not directly related, if the structural-based test is used to screen the parts, it poses the risk of either over rejecting or incorrectly passing. Therefore it can be used as a good safety measure that checks if the system is still relatively OK after it has been used for a while, but it cannot be a reliable production test method. In the self calibration case, the same production test based on specifications still need to be developed to ensure the performance after calibration.

1.3.3 Specification-Based ADC BIST

By contrast, a specification-based BIST solution tries to measure the analog and mixed-signal circuit performance on chip. In the case of ADC BIST, it is apparent that a linear signal generator needs to be implemented to provide the test stimuli. A performance analyzer also needs to be provided to evaluate the ADC output data on chip [12]. A ideal specification-based ADC BIST solution is illustrated in Figure 1.4.

This specification-based ADC BIST will have several advantages compared to its structural-based counterparts in many ways. First it does not

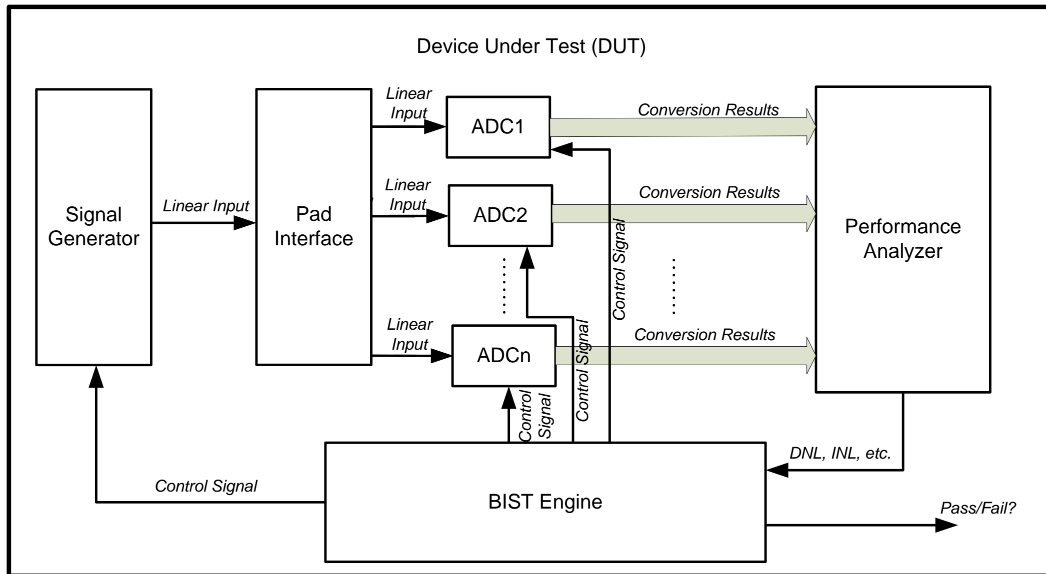


Figure 1.4: An Ideal ADC BIST System Block Diagram

depend on the specific ADC architecture. Any ADC that need to be tested against static linearity performance specifications can be tested in this way. The second advantage is that it is able to test the ADC as a whole instead of sub-blocks of the ADC. Moreover, it is able to include the ADC input pads in the BIST system, and thus mimics exactly what user will be seeing. The next advantage it has is that it allows direct correlation between the BIST reported performance and tester reported performance, thus it makes it a lot easier to evaluate the effectiveness of the BIST solution. Once correlation is found, the correlation result can be used to implement a true product screening solution.

With the above advantages, the specification-based ADC BIST is the focus of this work.

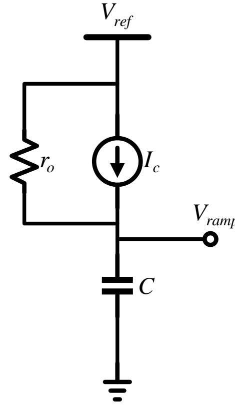


Figure 1.5: Conceptual Diagram of On Chip Ramp Generator

1.3.4 On Chip Signal Generator

As shown in the last section, an on chip test signal generator is essential for a specification-based BIST solution. Among various signals that can be used for histogram testing, a ramp signal or triangle wave is superior to other signal types e.g. sine wave. The great property of an ideal ramp signal is that it will yield an even occurrence of each code assuming the ADC under test is ideal. Thus, it makes it easy to calculate the performance metrics. It also requires fewer samples to be taken by the ADC to derive performance than that of a sine wave. This results in significantly less tester time which is critical to ADC test cost.

The most common on chip ramp generator is realized by charging a capacitor with a small current source. The architecture has been presented in several papers [3, 13]. Figure 1.5 above shows a typical block diagram:

Therefore,

$$V_{ramp}(t) = \frac{I_C}{C} \times t \tag{1.12}$$

However the linearity of the ramp is a major design challenge that we need to deal with. The linearity of the ramp depends on the output impedance of the current source and intrinsic linearity of the current source and the capacitor. The intrinsic linearity of the capacitor is usually very good, it was stated in [3] that 15 to 16 bits of linearity can be obtained from on-chip poly-poly capacitors.

Therefore, the focus has been on how to increase the output impedance or reduce the impact of the output impedance of the current source. Some techniques have been introduced including inserting a high gain operational amplifier in the feedback loop. The fact is that after much design effort the linearity achieved in [3] is only 11-bits which is not sufficient for high resolution ADC BIST. Alternatives have to be found to achieve the stringent linearity required.

1.4 Approach of This Work

As discussed in previous sections, the specification-based ADC BIST using the histogram test method is the most promising BIST solution to address the ADC static test challenge. The key requirement for the histogram method is a sufficiently linear ramp input. For an n-bit ADC, the linearity requirement for the ramp is $(n + 2)$-bit. For an ADC with more than 10-bit resolution,

such a high-linearity (> 12-bit) signal generator is very difficult to implement on-chip even with large area and power penalties. A significant amount of effort has been spent designing such an on-chip ramp generator. However, the highest achieved linearity is only 11-bit [3]. Hence, many researchers have been working to relax the linearity requirement of the input. Recently, a stimulus error and identification removal (SEIR) method has been developed that allows the use of a nonlinear ramp input (e.g., 7-bit) to test a high-resolution (e.g., 16-bit) ADC [4]. It uses two input ramp signals: the first one is directly from the on-chip ramp generator; the second one is equal to the first one plus a constant offset. Because they are highly correlated, the least-square (LS) estimation method can extract the nonlinearity information from the ADC outputs. Once the input nonlinearity is identified, it can be removed from measured histograms. As a result, the corrected histograms contain only the ADC nonlinearity, which can be measured with very high accuracy.

The key to this SEIR method is the addition of the constant voltage offset. The error in this analog computation has to be much smaller than 1 LSB over the entire input range, which remains a difficult task. So far, two techniques have been proposed [5, 6]. One approach is to use a standard analog voltage adder built with a high-gain (88 dB) operational amplifier. This scheme increases the design complexity and consumes power and area, which contradicts the BIST principle that the BIST circuit should be small and simple with its own performance being easy to guarantee. The other approach is to exploit the inherent offset of an amplifier by intentionally widening the

device mismatch. However, this method cannot guarantee a high constancy, as the input referred offset of an amplifier is signal dependent.

To solve this critical issue in the SEIR-based BIST scheme, this work presents a simple, low-power, and low-area method to inject the required constant offset. It exploits the inherit capacitive sample-and-hold circuit used in various ADC architectures (e.g., SAR, pipelined, cyclic, two-stage, delta-sigma, etc), and adds only a small redundant capacitor and a switch. It ensures that the injected offset will have very high constancy, which results in an accurate Integrated Nonlinearity (INL) estimation.

Once accurate estimation of INL becomes possible, it is straightforward to apply this method to calibrate the ADC to achieve better performance. To make sure the ADC is calibrate-able, wide codes need to be eliminated. A redundant SAR ADC with radix less than 2 and with process/voltage/temperature (PVT) variations carefully considered, it is possible to eliminate all wide codes. However large spreads of missing codes are inevitable. The ADC will rely on a calibration method and this work successfully proves itself to be an ideal candidate. Thus designing a low power, low area redundant ADC is possible using this method.

The rest of this report is organized as follows. Chapter 2 reviews ADC BIST basics, then presents SEIR based ADC BIST and its characterization results. Chapter 3 presents the method to inject constant offset for SEIR based ADC BIST and simulation results. Chapter 4 discusses the application of this method to implement digital calibration. The conclusion is in chapter 5.

Chapter 2

SEIR-Based ADC BIST

2.1 SEIR Concept Overview

The SEIR method [4] is proposed to address the stringent linearity requirement for the input ramp. Two functional related signals are generated and converted by the ADC under test, which results in a set of equations that contains nonlinearities of both the input source and the ADC. By canceling out ADC nonlinearity from the equations, the nonlinearity of input source can be estimated by algorithms like the standard least square method. With source nonlinearity extracted and removed, the ADC nonlinearity can be measured accurately. The fundamentals of the SEIR method are reviewed below.

2.1.1 Modeling of source nonlinearity

The input ramp signal $x(t)$ can be modeled below with its nonlinearity portion represented by $F(t)$:

$$x(t) = T_0 + (T_{N-2} - T_0)t + F(t) \tag{2.1}$$

where T_0 and T_{N-2} are the transition levels at the start and end terminals. The time t is normalized here with $t \in [0, 1]$. To estimate the source nonlinearity,

we need to model $F(t)$. It can be expanded in a set of trigonometric functions:

$$F(t) = \sum_{j=1}^{M} a_j F_j(t) + e(t) = \sum_{j=1}^{M} a_j \sin(j\pi t) + e(t) \tag{2.2}$$

Here only M harmonics are considered. It has been proved in [4] that the residue error $e(t)$ can be made negligible with the appropriate M been selected (e.g., $M = 20$).

2.1.2 INL calculation

Integral nonlinearity (INL) is defined as the difference between ideal transition edges $\{I_k\}$ and true transition edges $\{T_k\}$ for each code $k \in [1, N-1]$, where $N = 2^n$ for an n-bit ADC. Assuming the ADC is monotonic, the code transition time instances can be estimated by:

$$\hat{t}_k = \frac{\sum_{i=1}^{k} W_i}{\sum_{i=1}^{N-2} W_i} \tag{2.3}$$

where W_i is the number of occurrence of the i-th code retrieved from the histogram method. $\{T_k\}$ and $\{I_k\}$ can be calculated as:

$$T_k = x(\hat{t}_k) \tag{2.4}$$

$$I_k = T_0 + \frac{T_{N-2} - T_0}{N-2} k \tag{2.5}$$

Thus, INL can be derived as:

$$INL_k = \frac{T_k - I_k}{LSB} = (N-2)\hat{t}_k + \sum_{j=1}^{M} a_j F_j(\hat{t}_k) - k \tag{2.6}$$

where $LSB = (T_{N-2} - T_0)/(N-2)$.

2.1.3 Source nonlinearity estimation

If we know the source nonlinearity, we can remove it (2.6) and obtain an accurate representation of INL. To this end, SEIR uses two correlated inputs with a constant offset α in between:

$$V_1(t) = T_0 + (T_{N-2} - T_0)t + F(t) \quad (2.7)$$

$$V_2(t) = T_0 + (T_{N-2} - T_0)t + F(t) - \alpha \quad (2.8)$$

Applying (2.6), we have:

$$INL_k^{(1)} = (N-2)\hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(1)}) - k \quad (2.9)$$

$$INL_k^{(2)} = (N-2)\hat{t}_k^{(2)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(2)}) - k - \alpha \quad (2.10)$$

where $k \in [1, N-3]$. Since $INL_k^{(1)} = INL_k^{(2)}$, we can use the least-square method to estimate the source nonlinearity $\{a_j\}$ $(j \in [1, M])$ [4].

2.2 SEIR Characterization Results

Characterization has been done to verify the SEIR estimation accuracy under different circumstances including the number of hits per code (HPC), offset between the two ramps, number of coefficients of least square basis functions (M_b), different input noise levels on the ramp measured in signal-to-noise ratio (SNR) and different ADC resolutions. The purpose is to find and understand their impact on the accuracy of the least square estimation.

For each characterization, the simulation is repeated 10 times to evaluate the consistency. Two types of estimation error are analyzed. The first one is the estimation error between the absolute maximum INL error derived from an ideal ramp histogram test (INL_{true}) and the absolute maximum INL error derived from nonlinear ramp with SEIR estimation (INL_{ls}). Since the absolute maximum INL error is the one being reported as the test result compared against the specification, we name this estimation error $Error_{spec}$. Another estimation error of interest is the absolute maximum difference between INL_{true} and INL_{ls} across all code bins. This is reported with digital calibration in mind, since it determines how accurately we can calibrate the error out. Thus, we name this estimation error as $Error_{cal}$.

The basic circuit that was used for characterization is a very simple ADC modeled in Matlab and Simulink with no specific ADC architecture assumed. Nonlinearity is modeled with polynomials while sine function is chosen as the basis function as indicated in Equation 2.2.

2.2.1 Characterization of Hits Per Code

A large number of hits per code in histogram test method in general helps suppress the noise present at the input. This in turn improves the accuracy of equation 2.3, and thus thus improving the overall estimation accuracy. This trend is clearly shown in Figure 2.1 and Figure 2.2.

It is noted that there are some variations among the 10 simulations due to the random noise injected in the signal. The variance is reduced when

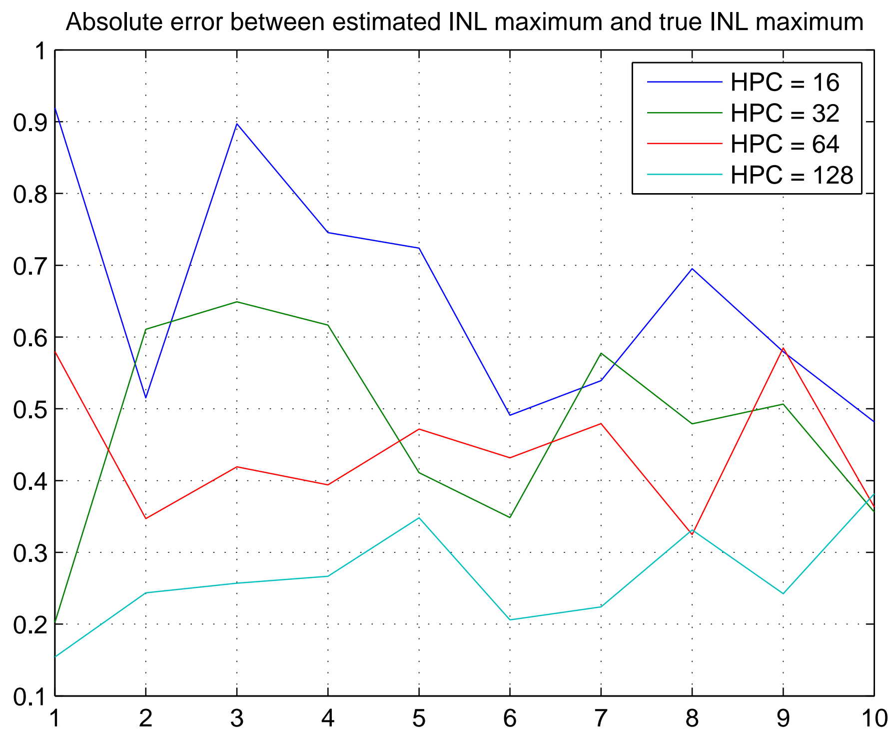


Figure 2.1: $Error_{spec}$ on Hits Per Code

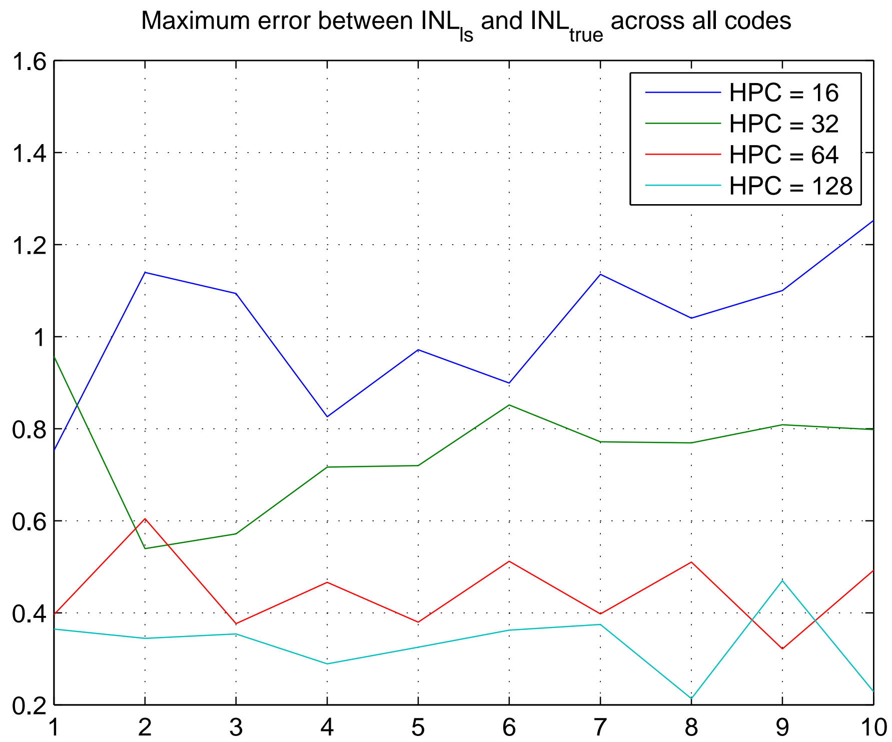


Figure 2.2: $Error_{cal}$ on Hits Per Code

larger hits per code is chosen because of the noise suppression. Another factor that can help reduce variance is the number of basis functions which will be reviewed in later section.

It is also noted that most of the time $Error_{spec}$ is less than $Error_{cal}$, this is well reflected in the Table 2.1 which lists the average of each type of error. The reason is that $Error_{cal}$ is defined as absolute maximum error across all code bins, most of the time it should be the largest error. However in some cases the $Error_{spec}$ is actually larger than $Error_{cal}$, this happens when the estimated INL has the maximum INL error shifted to a different code bin than the original one. In that case, it is possible to have $Error_{spec}$ larger than $Error_{cal}$.

Table 2.1: Characterization of Hits Per Code

2% input nonlinearity, 14-bit ADC		
$M_b = 20$, SNR = 65dB, Offset = 128LSB		
Hits Per Code	$Error_{spec}$ (LSB)	$Error_{cal}$ (LSB)
16	0.6587	1.0209
32	0.4757	0.7502
64	0.4395	0.4455
128	0.2655	0.3326

2.2.2 Characterization of Injected Offset

The amount of offset to be injected between the two ramps is also of interest in this research. An offset of up to 512 LSB has been characterized as

shown in Figure 2.3 and Figure 2.4.

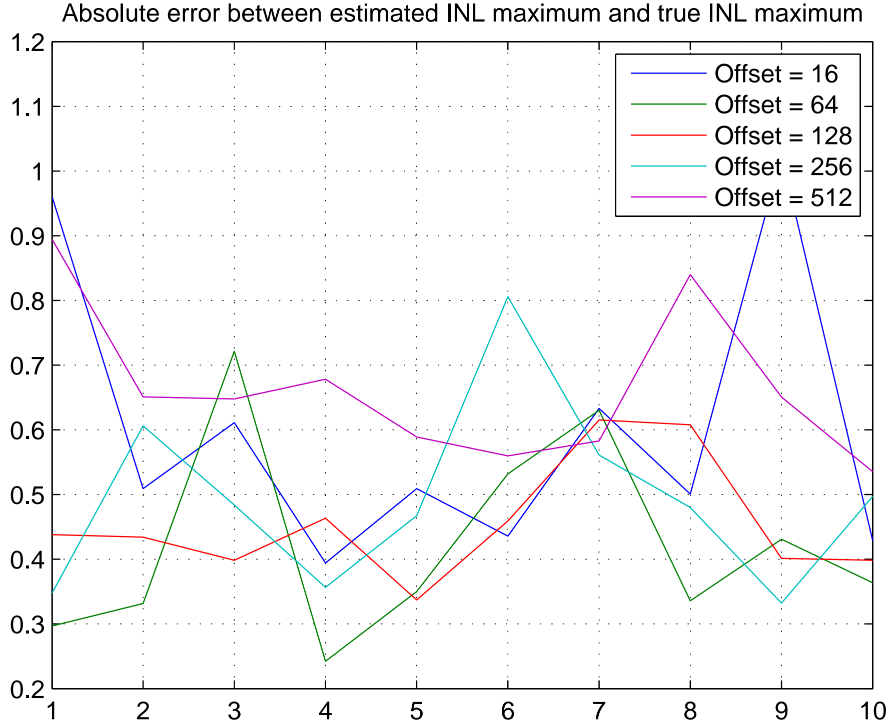


Figure 2.3: $Error_{spec}$ on Injected Offset

Table 2.2 lists the average of $Error_{spec}$ and $Error_{cal}$, the values are relatively close (between 64 LSB to 256 LSB). This property will help us later in choosing the amount of offset since it gives us more design flexibility in choosing offset. It is noted that too much and too little of offset are both undesirable. A small offset may not be able to generate sufficient differences at the same code level significantly increasing the impact that noise has on estimation accuracy [4]. If the offset is too large, a significant part of the

Figure 2.4: $Error_{cal}$ on Injected Offset

ramp will be thrown away per Equation 2.9 and 2.10 that affects the SEIR's capability to estimate nonlinearity across the entire range of the input ramp.

Table 2.2: Characterization of Injected Offset

2% input nonlinearity, 14-bit ADC		
M_b = 20, SNR = 65dB, Hits Per Code = 32		
Injected Offset (LSB)	$Error_{spec}$ (LSB)	$Error_{cal}$ (LSB)
16	0.6007	0.6675
64	0.4235	0.7439
128	0.4554	0.7654
256	0.4937	0.7262
512	0.6629	0.6168

2.2.3 Characterization of Number of Basis Functions

The choice of the number of basis functions is highly dependent on the nonlinearity of input ramp. With this characterization exercise, a 2% nonlinearity ramp is assumed with nonlinearity being modeled using polynomials with coefficients of up to t^4.

As shown in Figure 2.5 and Figure 2.6, starting from $M_b = 5$, the INL error can be estimated with relatively poor performance. With increased M_b, however, there is no significant accuracy enhancement between $M_b = 10$ and $M_b = 40$. With larger M_b, the consistency of estimation error is better. This is partly due to better estimation of higher order INL errors being introduced by the injected noise.

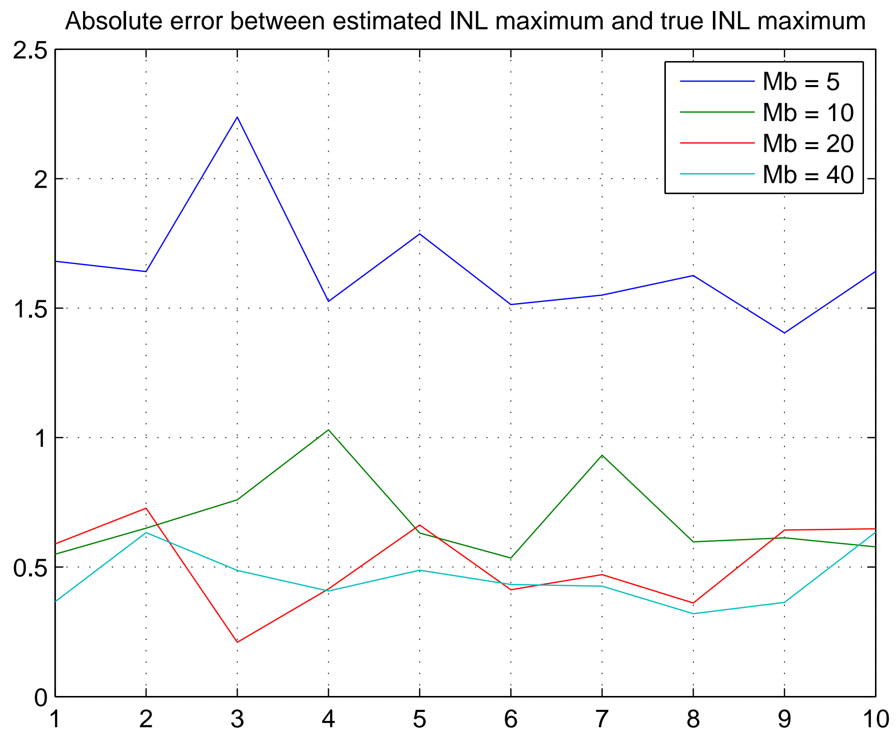


Figure 2.5: $Error_{spec}$ on M_b

Figure 2.6: $Error_{cal}$ on M_b

Table 2.3: Characterization of M_b

2% input nonlinearity, 14-bit ADC		
Injected Offset = 128LSB, SNR = 65dB, Hits Per Code = 32		
M_b	$Error_{spec}$ (LSB)	$Error_{cal}$ (LSB)
5	1.6608	1.6537
10	0.6878	0.7036
20	0.5141	0.6793
40	0.4562	0.6959

2.2.4 Characterization of Input Noise

As has been discussed in previous sections, input noise has a significant impact on the estimation accuracy. A large number of hits per code will help suppress the noise. Figure 2.7 and Figure 2.8 has shown the impact due to different input noise levels.

Table 2.4: Characterization of Input Noise

2% input nonlinearity, 14-bit ADC		
M_b = 20, Offset = 128LSB, Hits Per Code = 32		
Input Noise in SNR (dB)	$Error_{spec}$ (LSB)	$Error_{cal}$ (LSB)
40	1.9902	2.7026
55	0.9329	1.2112
65	0.4915	0.6302
80	0.2979	0.2882

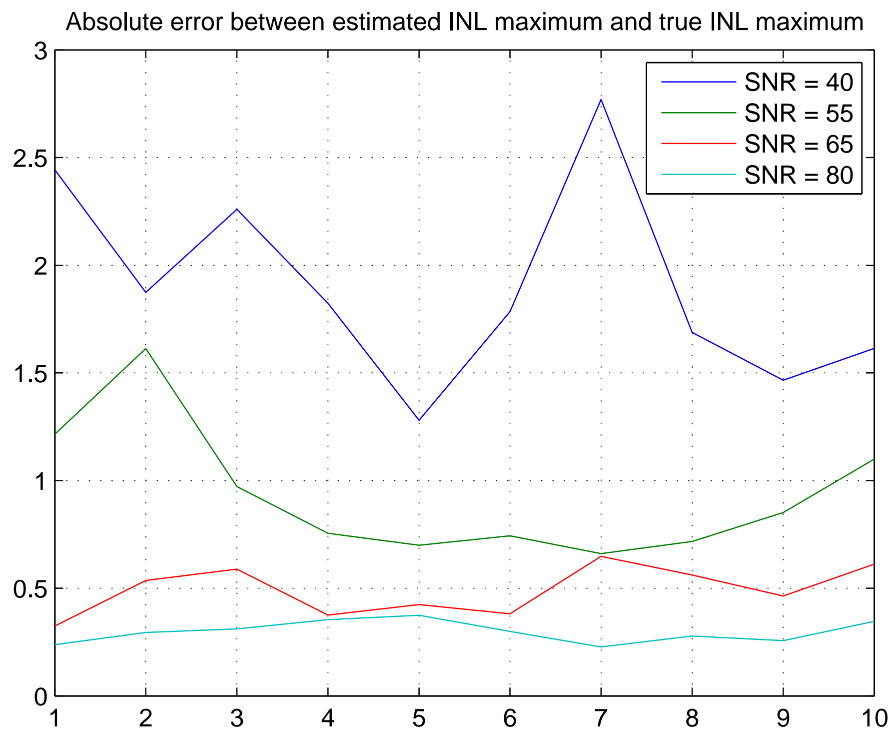


Figure 2.7: $Error_{spec}$ on Input Noise

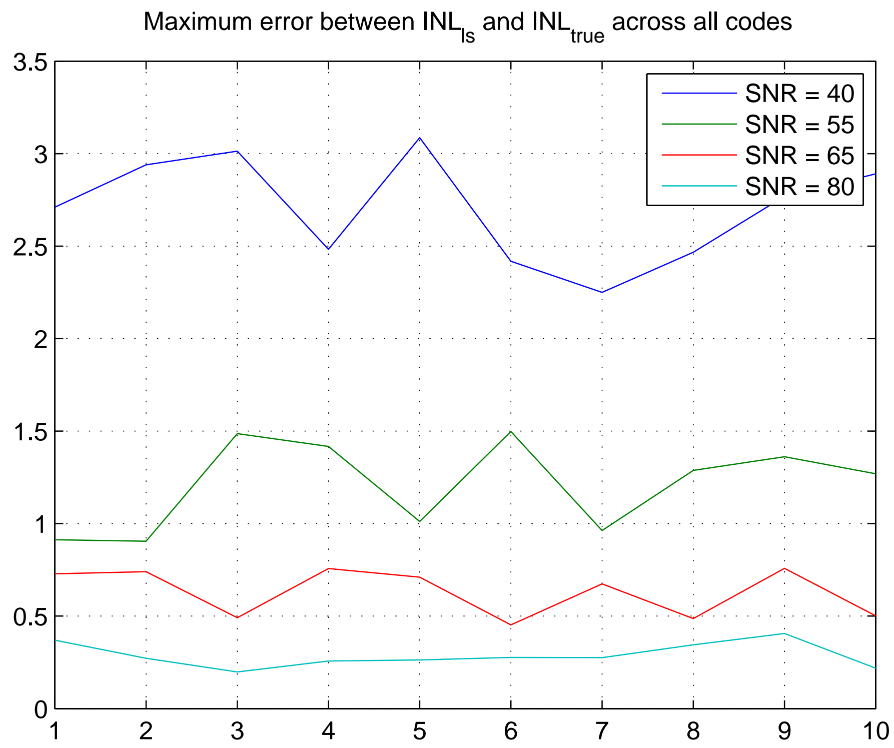


Figure 2.8: $Error_{cal}$ on Input Noise

2.2.5 Characterization of ADC Resolution

The above characterizations have assumed a 14-bit ADC. This section shows the characterization results on ADCs with different resolutions. It is clear that with a lower ADC resolution, we get better estimation error performance. For a 16-bit ADC, an estimation error of 1 LSB is achieved. It needs to be noted that an SNR of 65dB is assumed for all cases which might be too pessimistic for a 16-bit ADC. Nevertheless, it has shown that the SEIR method is still a reliable method to apply to high resolution ADCs.

Table 2.5: Characterization of ADC Resolution

2% input nonlinearity, SNR = 65dB		
M_b = 20, Offset = 128LSB, Hits Per Code = 32		
ADC Resolution	$Error_{spec}$ (LSB)	$Error_{cal}$ (LSB)
10	0.116	0.1926
12	0.2353	0.3052
14	0.4933	0.7338
16	0.9402	1.662

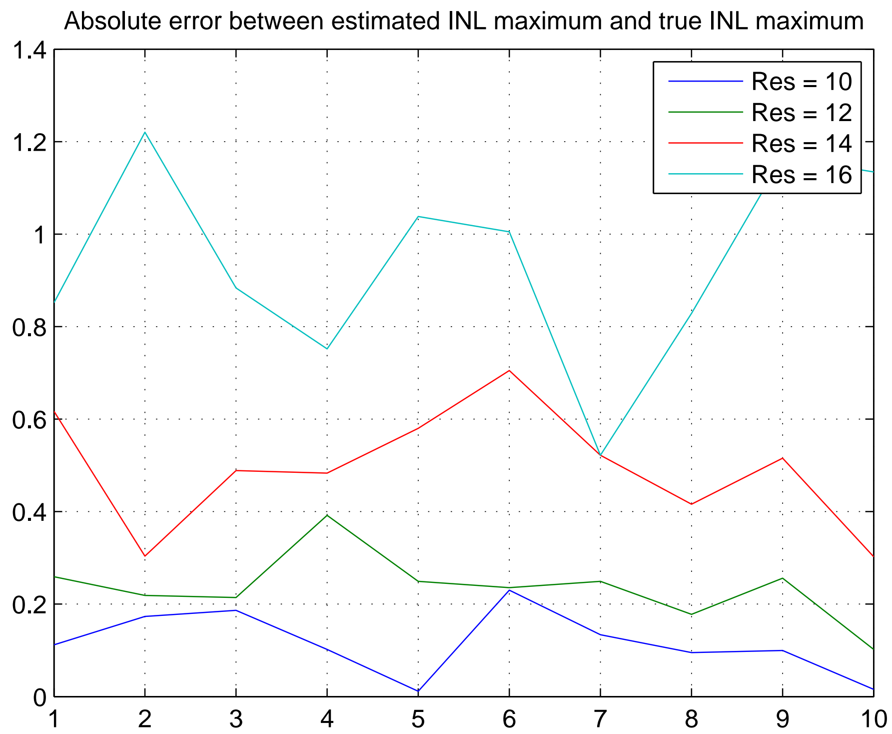


Figure 2.9: $Error_{spec}$ on ADC Resolution

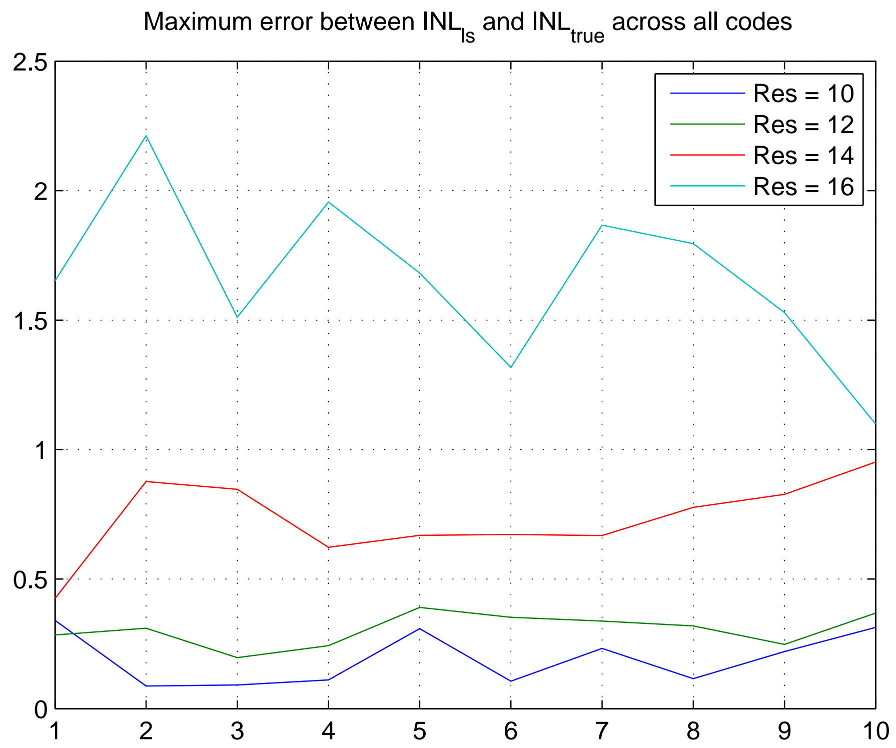


Figure 2.10: $Error_{cal}$ on ADC Resolution

Chapter 3

Offset Injection

3.1 Offset Injection Circuit

As mentioned earlier, the key to SEIR is the addition of a constant voltage offset to the original ramp input. This is nontrivial, as the *constancy* of this voltage offset has to be very high – its variation over the entire signal range has to be much less than 1 LSB. As explained in Sec. I, the existing approaches are complicated and area/power hungry, which is not well suited for BIST which demands simple and low-cost solutions.

Instead of designing a stand-alone offset injection circuit, this paper proposes a new scheme that embeds it inside the inherit capacitive sample-and-hold circuit of an ADC. Note that the proposed technique can be applied to various ADC architectures. However, for brevity, here we focus our discussion on its application to a SAR ADC, which is shown in Fig. 3.1. An extra capacitor C_p and a switch is added to the original capacitor array. During the normal operation or during the first run of BIST without injected offset, C_p is tied to V_{ss} during both sampling and evaluation phases. The ADC conversion results stay the same as that without C_p. When the offset injection is needed during the second run of the BIST, C_p is tied to V_{ss} during the sampling phase

and then switched to V_{ref} during the evaluation phase. A detailed derivation is shown below.

3.1.1 Normal operation

Let us assume that V_1 is the nonlinear input from an on-chip signal generator. During the sampling phase, the total charge Q at the comparator input V_x is:

$$Q = -V_1 \cdot C_{sum} \tag{3.1}$$

where $C_{sum} = \sum_{i=0}^{n-1} C_i + C_0$. The MSB is evaluated first with C_{n-1} switched to V_{ref} while all other capacitors are switched to V_{ss}. Now Q becomes:

$$Q = (V_x - V_{ref})C_{n-1} + V_x(\sum_{i=0}^{n-2} C_i + C_0 + C_p) \tag{3.2}$$

From (3.1) and (3.2), we can derive V_x:

$$V_x = -\frac{C_{sum}}{C_{sum} + C_p} V_1 + \frac{C_{n-1}}{C_{sum} + C_p} V_{ref} \tag{3.3}$$

By repeating the process to evaluate all bits, eventually we get:

$$V_x = -\frac{C_{sum}}{C_{sum} + C_p} V_1 + \frac{\sum_{i=0}^{n-1} D_1(i) C_i}{C_{sum} + C_p} V_{ref} \tag{3.4}$$

where $D_1(i)$ ($i \in [0, n-1]$) is the i-th binary conversion result. Thus, we can represent V_1 as:

$$V_1 = \frac{\sum_{i=0}^{n-1} D_1(i) C_i}{C_{sum}} V_{ref} + q_{n1} \tag{3.5}$$

where the quantization noise $q_{n1} = (C_{sum} + C_p)V_x / C_{sum}$. Note that it is still bounded by ± 0.5 LSB, as V_x decreases every conversion cycle.

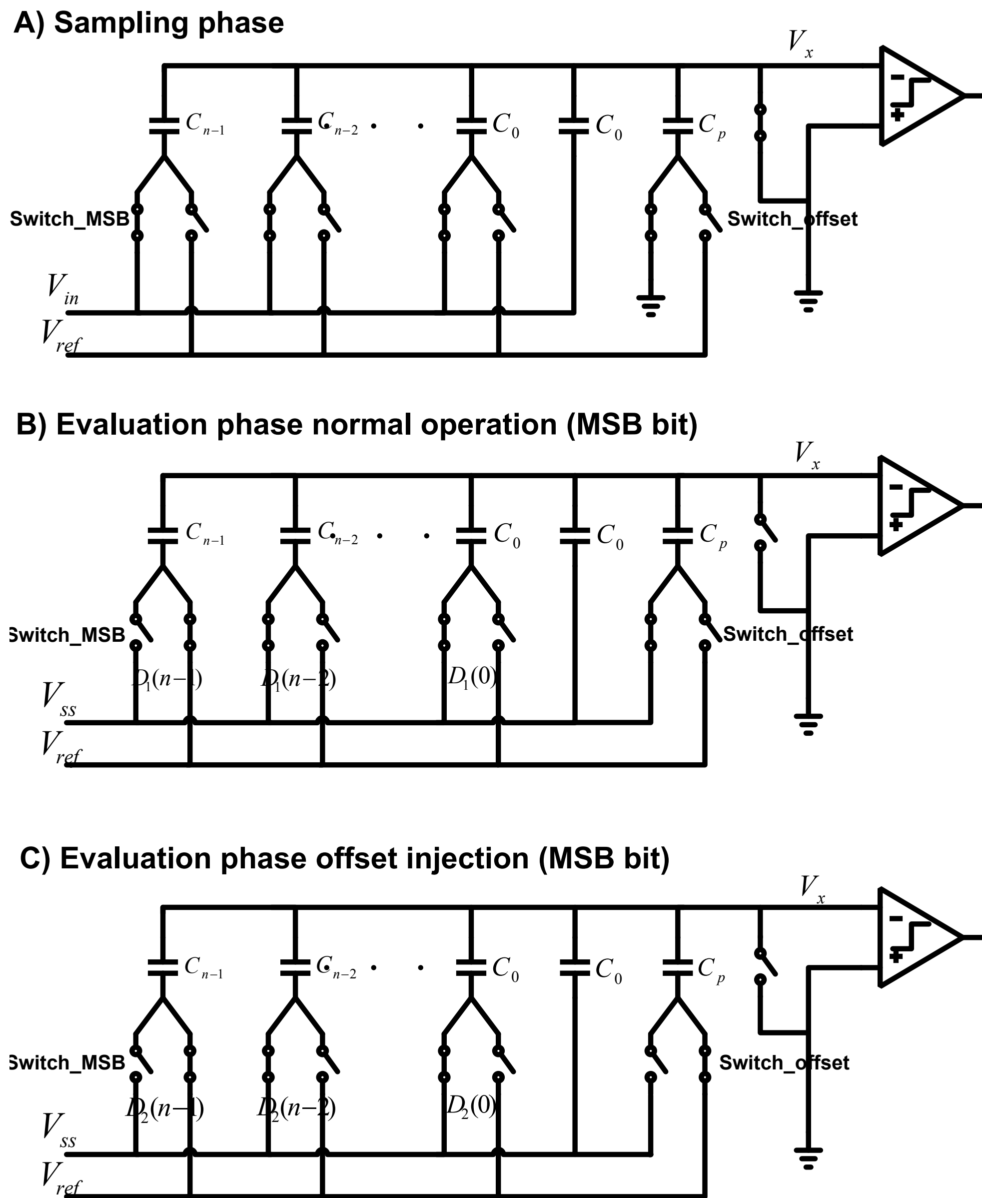


Figure 3.1: Offset Injection in Charge Sharing SAR ADC

3.1.2 Offset injection

To inject a voltage offset, the sampling phase is kept the same as before, but C_p is switched to V_{ref} during the evaluation phase. During the MSB evaluation:

$$Q = (V_x - V_{ref})(C_{n-1} + C_p) + V_x(\sum_{i=0}^{n-2} C_i + C_0) \tag{3.6}$$

From (3.1) and (3.6), we can derive V_x:

$$V_x = -\frac{C_{sum}}{C_{sum} + C_p} V_1 + \frac{C_{n-1} + C_p}{C_{sum} + C_p} V_{ref} \tag{3.7}$$

Repeating the evaluation process for all bits, we get:

$$V_x = -\frac{C_{sum}}{C_{sum} + C_p} V_1 + \frac{\sum_{i=0}^{n-1} D_2(i) C_i + C_p}{C_{sum} + C_p} V_{ref} \tag{3.8}$$

where $\{D_2(i)\}$ represent the new ADC conversion results. Now V_1 is:

$$V_1 = \frac{\sum_{i=0}^{n-1} D_2(i) C_i}{C_{sum}} V_{ref} + \frac{C_p V_{ref}}{C_{sum}} + q_{n2} \tag{3.9}$$

Let us define the equivalent input V_2 as:

$$V_2 \equiv \frac{\sum_{i=0}^{n-1} D_2(i) C_i}{C_{sum}} V_{ref} + q_{n2} \tag{3.10}$$

Thus V_2 is related to V_1 by:

$$V_2 = V_1 - \frac{C_p V_{ref}}{C_{sum}} = V_1 - \alpha \tag{3.11}$$

This shows that a second input V_2 with a constant offset α from V_1 is generated.

3.1.3 Constancy analysis

It is shown that a new input V_2 with a constant offset from the original input V_1 is generated simply by inserting a small capacitor C_p. The analog addition in the proposed scheme is essentially done in the charge domain by the inherent sample-and-hold circuit. This removes the need for a stand-alone offset injection circuit. Moreover, the charge addition is governed by the law of charge conservation, which guarantees its accuracy and linearity.

The constancy of injected offset depends on V_{ref} and the capacitor ratio between C_p and C_{sum}. As is well established, the capacitor ratio is very stable in CMOS technology, and its variation is below single digit PPM [7]. Therefore the constancy of V_{ref} is the dominant contributor to variation. Noise on V_{ref} can be greatly suppressed by decoupling capacitors. Since the entire test procedure is typically completed within seconds or minutes as worst case, the long-term drift performance, often specified in thousands of hours of V_{ref}, is typically not of concern. A voltage reference device with even long term drift performance in single digit PPM can be readily found in the commercial market [8]. As a result, the constancy of the injected offset can be easily made to be around 1 ppm, which is sufficient to test ADCs with even 18-bit resolution.

3.2 ADC Modeling and Simulation

The ADC is modeled using Matlab. Non-idealities of circuits and signal sources are taken into consideration, including V_{in} noise, V_{ref} noise and

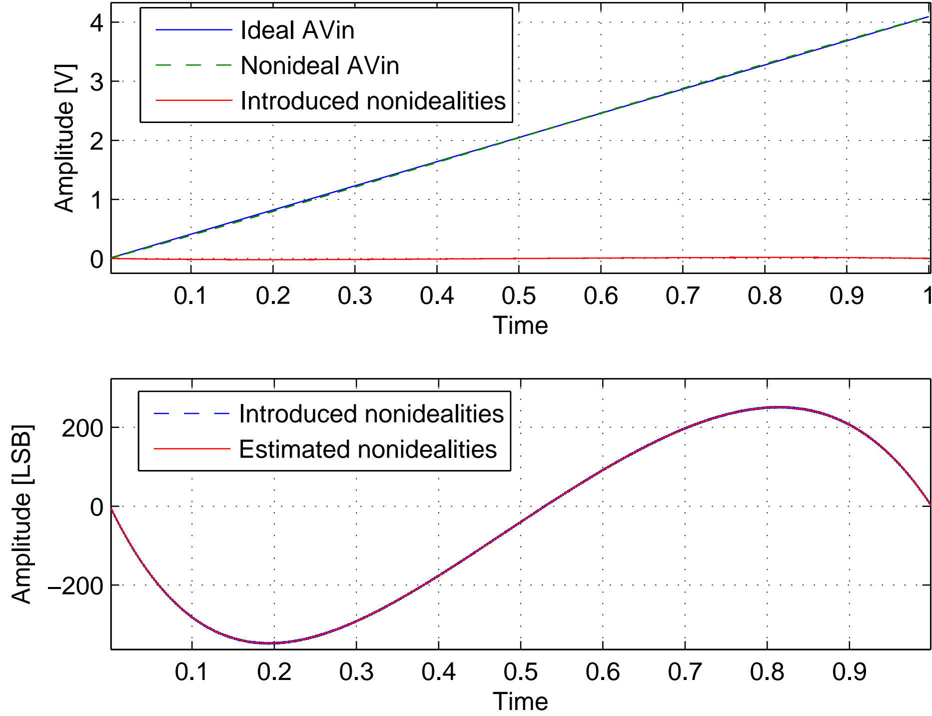


Figure 3.2: Nonlinear input

capacitor mismatches.

3.2.1 Modeling of a 16-bit SAR ADC

The binary weighted capacitor array is modeled with mismatches on several MSB capacitors to introduce INL errors. As illustrated in Fig. 3.1, a small capacitor C_p is added to the capacitor array for offset injection. The value of C_p is equal to C_7 to produce a voltage offset at around 128 LSB. V_{ref} is modeled with 1 LSB rms noise.

3.2.2 Modeling of the nonlinear input

A nonlinear input with roughly 8-bit linearity is created as described by the following equation:

$$\begin{aligned} V_{in} &= V_{ref} \cdot t + V_n \\ &+ b_1 t(t-1) \\ &+ b_2 t(t-1)(t-0.5) \\ &+ b_3 t(t-1)(t-0.5)(t-0.25) \\ &+ b_4 t(t-1)(t-0.5)(t-0.25)(t-0.75) \end{aligned} \tag{3.12}$$

where $b_1 = 0.01, b_2 = -0.4, b_3 = 0.1, b_4 = -0.5$, V_{ref} is set to 4.095 V, t is normalized to unit. V_n is the input noise with the rms value of 1 LSB.

Table 3.1: Characterization of the number of coefficients M_b

	$M_b = 15$	$M_b = 20$	$M_b = 30$	$M_b = 50$
Max INL Est. Error(LSB)	0.82	0.37	0.076	0.067
Max Est. Error across codes(LSB)	4.07	2.21	1.11	0.72

3.2.3 Simulation results

The number of coefficients M_b used to estimate the input nonlinearity is set to be 50 [see (2.2)]. The comparison between the estimated non-idealities and introduced non-idealities is shown in Fig. 3.2. The comparison between the estimated INL and the true INL as well as estimation error across all codes

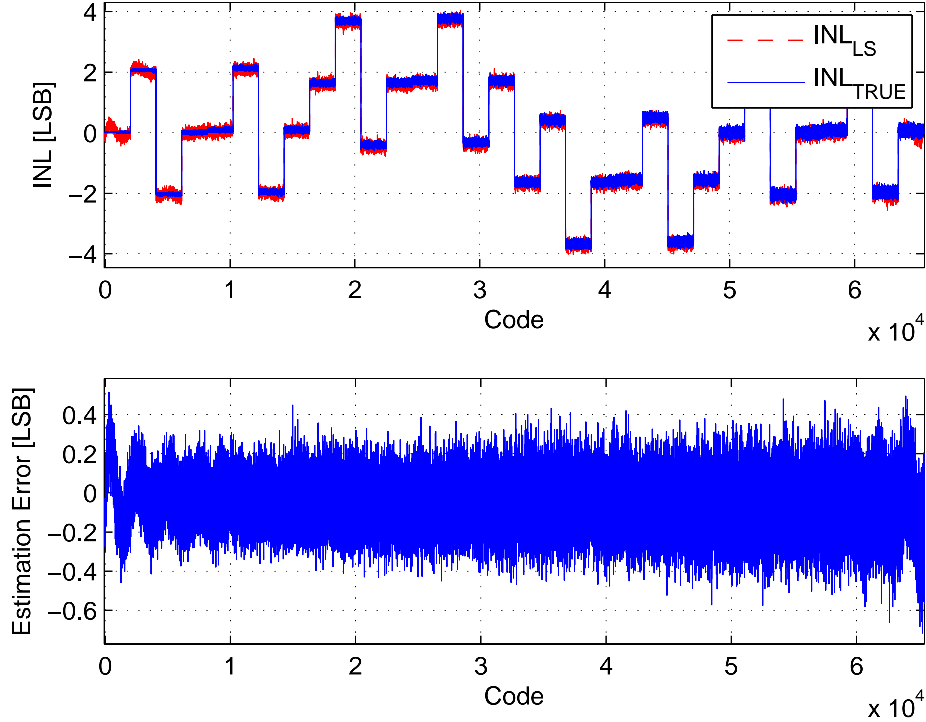


Figure 3.3: INL estimation

is shown in Fig. 3.3. Maximum INL is what appears on the data sheet of an ADC, and thus, is the most important parameter. Its estimation error is less than 0.07 LSB. Across all codes, the estimation error of all codes are within $+0.51/-0.72$ LSB.

It is noticed that biggest estimation error appears close to the beginning and the end of the codes where the sharpest slope resides which indicates the highest level of nonlinearity. When a small value of M_b is used, an oscillation on the estimation error is clearly seen. Table I shows the impact of M_b on the

INL estimation accuracy. The estimation error on the maximum INL decreases as M_b increases, and is less than 0.1 LSB for $M_b \geq 30$, which is sufficient for most ADC testing requirements.

Chapter 4

Application of ADC Self Calibration

The ADC self calibration techniques that were proposed in the 80's [14, 15] are widely used in pipeline and SAR ADC designs. The basic idea of ADC self calibration is to explore a method to find the imperfections of the ADC like capacitor mismatches thus one can calibrate them out to improve the ADC performance.

Redundancy is another technology to digitally enhance ADC performance by simply rejecting the analog imperfections from the converted results. Often times the redundancy comes with self calibration to ensure the ADC design is calibrate-able i.e. no wide code is present.

By reviewing the SEIR-based ADC BIST solution, it is apparent that the imperfections of the ADC i.e. static linearity error are readily available after the BIST. Thus, we can apply the estimated INL numbers to adjust ADC conversion result to achieve superior performance. Since a SAR ADC is chosen to illustrate our novel approach to inject offset, we will continue to use same SAR ADC design in this chapter as an example, except the radix is changed from 2 to 1.86 to make it a redundant SAR ADC.

4.1 Digitally Assisted ADC Design Overview

With process technology advancing to deep sub micro, the cost of manufacturing digital circuits is going down dramatically. Therefore the trend is to explore digital processing capabilities to reduce the analog design within ADC subsystems. Digital calibration and redundancy are two of the main techniques to fulfill that goal.

4.1.1 Digital Calibration

There are a lot of variations on how the digital calibration is performed. The two major groups of techniques are digital foreground calibration and digital background calibration.

A digital foreground calibration is like what is proposed in [14, 17]. In [14] a calibration DAC with 2 more bits resolution than the main DAC under calibration is designed into the system to perform measurements. The measured error is stored in memory and then is converted back into an analog voltage to be subtracted from the main DAC during normal conversion.

The property of digital foreground calibration is it measures the nonlinearity of the ADC upfront when the ADC is not in use. The calibration data can be stored in memory and can be used throughout the lifetime of the ADC. The drawback of this method is this is an interruption to customer usage. Thus, it is best used when the ADC does not need to perform continuous conversions. Applications like automotive would allow this. For example, when the car is

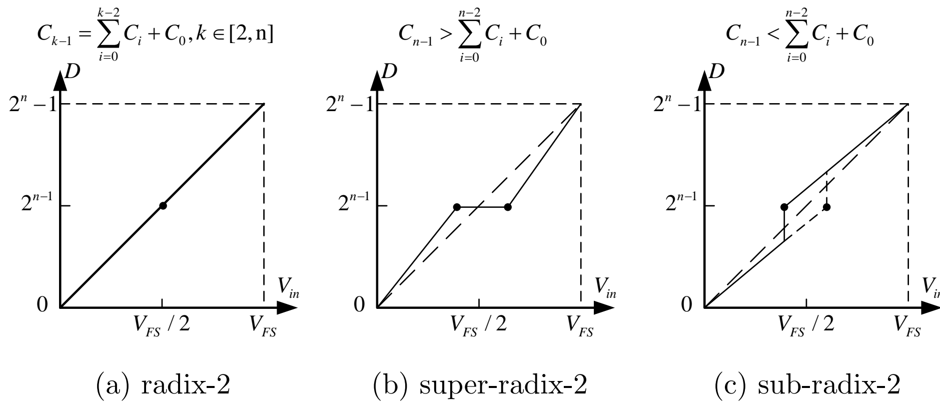
just started, a calibration routine can be kicked off. Another drawback is the calibration needs to be carried out periodically to compensate for voltage and temperature changes. Again, if intermittent self calibration is possible in the application, this is not a real concern. The SEIR-based BIST solution needs to bring the ADC offline and convert the signal from the ramp generator twice thus it is a digital foreground calibration technique.

By contrast, the digital background calibration does not require the ADC to be offline. Instead, the algorithms that perform the calibration run continuously during ADC conversion [16]. Typically, a learning curve is needed to extract the nonlinearity of the ADC. Since it is performed in the background, thus it can better adapt to the circuit changes to the PVT corners.

4.1.2 Redundancy

Redundancy is a technique that is widely used in pipeline ADC and SAR ADC architectures. The redundancy is introduced mainly to relax the DAC settling time, capacitor mismatch error and so on thus a low area, low power and fast ADC is possible. In a charge sharing SAR ADC, it comes in with a sub-radix-2 form such that each capacitor in the array is less than the total of its prior capacitors. Instead, the radix is chosen to be less than 2 to make sure there is redundancy on each input voltage. Therefore, a mistake during bit evaluation can be corrected later due to the redundancy.

As shown in Figure 4.1b, if a super-radix-2 format is used, a wide code will appear on code 2^{n-1} thus the error cannot be calibrated since the analog



(a) radix-2 (b) super-radix-2 (c) sub-radix-2

Figure 4.1: Transfer Curves for SAR ADCs[16]

input information around $V_{FS}/2$ is lost and thus cannot be recovered. By contrast, in the sub-radix-2 case as shown in Figure 4.1c, discontinuity has caused missing codes. Missing codes however can be easily calibrated out by simply removing them from the code space. This will inevitably reduce the resolution of the ADC. Thus in a sub-radix-2 SAR ADC, additional binary searching steps are needed to achieve the desired resolution. In this chapter, a 14-bit redundant SAR ADC is achieved using the 16-bit SAR ADC design from last chapter with the radix changed from 2 to 1.86.

4.2 Evaluation of Missing Code Impact

As redundancy has been introduced to alleviate the stringent capacitor matching requirement and reduce DAC settling time while allowing digital calibration at the same time, missing codes have been introduced. It has been stated in [4] that monotonicity and no missing code are assumed of the ADC

under test before starting to derive the SEIR method. Thus, a careful review of the missing codes impact on the SEIR based ADC BIST is needed to prove that the method is still valid with the existence of missing codes. The approach taken in this work is to review the fundamentals of SEIR method.

In Section 2.1.1 of modeling source nonlinearity, apparently the ADC missing codes will not have an impact. Now let's take a look at Section 2.1.2 of INL calculation to see if it is impacted. This foundation is the same foundation that enables the histogram ADC test method. Missing codes does not pose an issue to the histogram test method. In Section 2.1.3 of source nonlinearity estimation, the foundation is still valid even though certain code bins are missing. The only impact it brings to the source nonlinearity estimation is that we will have a fewer number of equations to perform the least square estimation. In the case that the number of missing codes is too large, the accuracy of the estimation may be impacted. However this could be an extreme case and can be taken care of at the initial design phase by choosing the appropriate radix.

With the above analysis, it is clear that the missing codes that are intentionally designed into the redundant SAR ADC would not pose a challenge to the SEIR-based ADC BIST method. Thus, it allows us to use the method to estimate INL performance for digital calibration. The same offset injection circuit as proposed in the previous chapter is still valid since the radix change does not change the fundamentals. The simulation results presented in Figure 4.2 prove out the theory. Estimation error is still very good considering the

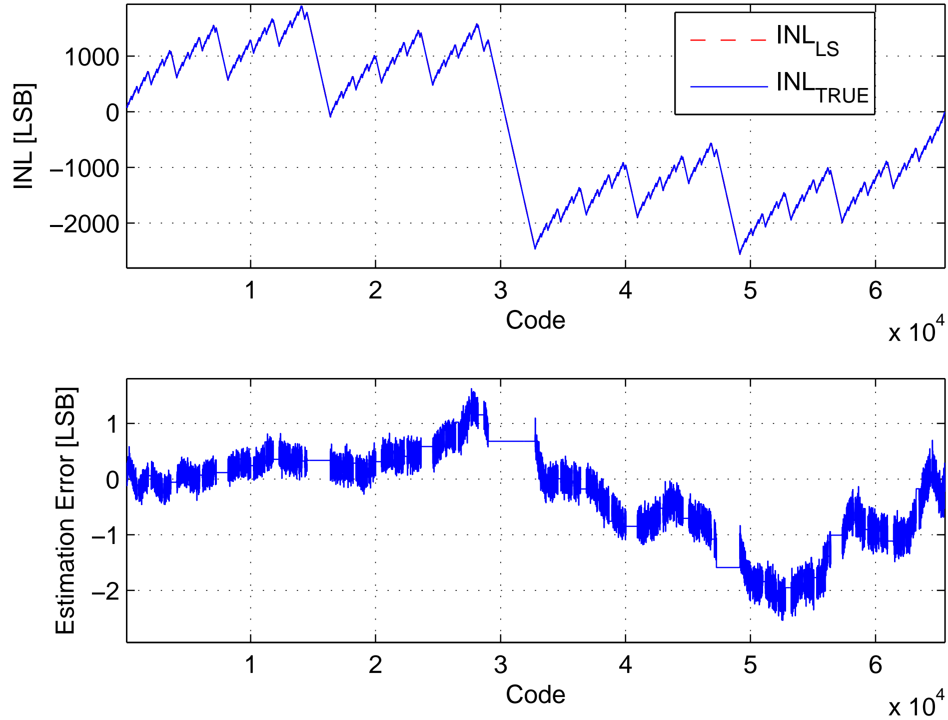


Figure 4.2: INL Estimation of Redundant SAR ADC

large INL errors.

4.3 Calibration Results

The same 16-bit SAR ADC design has been used from the previous chapter except the radix is changed from 2 to 1.86. The same input nonlinearity is assumed with the same imperfections of the ADC itself including noises and capacitor mismatches.

From Figure 4.3 we know there are 35532 missing codes ($DNL(i) =$

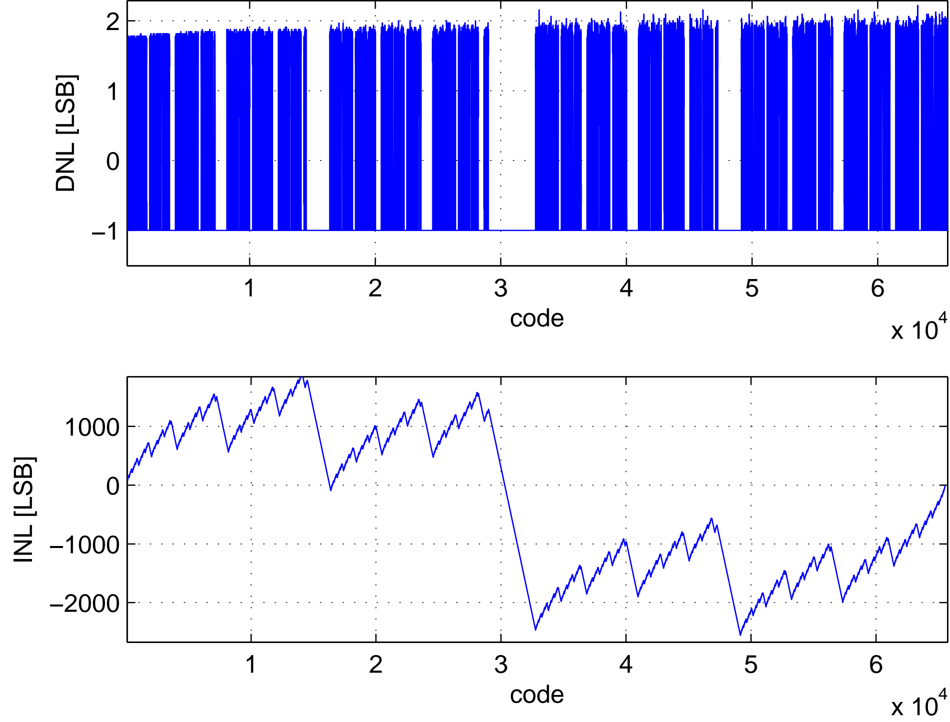


Figure 4.3: DNL and INL Error before Calibration

$-1LSB, i \in [1, 2^n - 1]$) introduced by this change, this redundant SAR ADC is not able to keep its 16 bit resolution. Instead its new resolution n_1 based on radix-2 is calculated as $2^{n_1} \leq 2^{16} - 35532 = 30004$ which leads to a new resolution with $n_1 = 14$.

The digital calibration can be done in multiple ways and is not the focus of this work. Assuming the estimated INL for all code bins is stored in memory, the proposed calibration algorithm is as simple as:

$$D_{cal}(i) = (D(i) + INL_{est}(D(i))) >> 2 \tag{4.1}$$

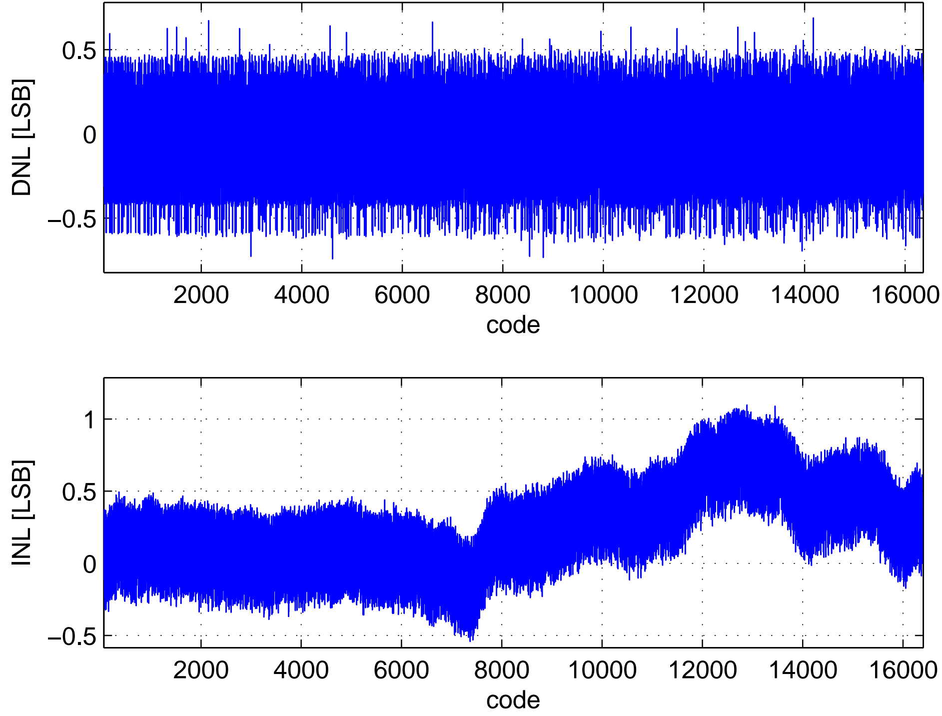


Figure 4.4: DNL and INL Error after Calibration

$D_{cal}(i)$ is the calibrated output at code i, $INL_{est}(D(i))$ is the estimated INL error that is used for compensation. Since a 14-bit ADC is what we target from original 16-bit resolution, the right shift by 2 can be done by simply throwing away the last 2 LSBs. Applying the same histogram test method to calibrated output D_{cal}, the DNL and INL plots have been shown in Figure 4.4. DNL error after calibration is mostly within +0.5LSB/-0.5LSB and INL error after calibration is within +1.1LSB/-0.5LSB.

Chapter 5

Conclusion

This chapter reviews and summarizes what has been accomplished in this work and also addresses the work needed in the future.

5.1 Summary of This Work

This work starts by reviewing the current ADC production test methodology and the ADC specifications that need to be guaranteed. As the cost of testing ADCs on ATEs is high and the number of ADCs being integrated on SOC is also going up, it is important to find alternatives to reduce test cost. ADC BIST is an attractive option which is studied in this work.

Different types of ADC BIST proposals have been reviewed. It has been found that the specification-based ADC BIST using the same ramp histogram test method as the production test methodology has many advantages to other structural-based ADC BIST methods. Therefore the focus in the paper is on how to implement the above ADC BIST on chip.

There are many challenges that must be overcome to reach this goal, stringent linearity requirements of the test signals is among the most challenging

ones. A SEIR method [4] that is proposed to reduce the linearity requirement has been reviewed and analyzed. This work continues and characterizes the SEIR method varying different impact factors and gives a good overview of the estimation accuracy under different configurations. This helps a designer make choices e.g. what is the number of hits per codes that should be used.

One of the challenges in implementing the SEIR method itself is to generate a constant offset between two input stimuli. Instead of looking into designing an offset injection circuit outside of the ADC, this work looks into minor changes to the capacitive sample and hold architecture that can be found on many types of ADCs to inject the needed offset. It is proven that the offset voltage being injected from this work is only dependent on the capacitor ratio between the inserted capacitor and the total value of whole capacitor array and also the consistency of V_{ref}. A very good consistency is achieved and is proven by simulation.

A natural extension of this work is explored. The estimated INL error can be used to calibrate the original ADC under test. If the circuit is available as part of the ADC design, we can design the ADC with less stringent requirements on capacitor matching etc. thus a low power, low area and high speed ADC becomes possible. This work reviews the possibility to apply the SEIR method on a redundant SARADC architecture with lots of missing codes and proves that it can be used. Simulation is carried out to further validate this idea.

5.2 Future Work Needed

There is still a lot of work that remains to be done to realize the ADC BIST system on chip.

The architecture of the ramp generator based on a current source charging a capacitor is most likely the architecture that will be chosen. However, to be able to test high resolution and low speed ADCs with sufficient hits per code, the slew rate of the ramp needs to be very small. This poses challenges for the ramp generator design. A very small current source is needed or a very large on chip capacitor is needed. Both are not desirable for on chip circuit realization. [5, 13] have proposed to generate a triangle waveform and to repeat it multiple times to solve the issue. Coherent sampling is required for this method to ensure that unique voltage levels are sampled throughout the test thus holding to the histogram method.

A traditional ADC test will try to test the whole range of ADC thus the input ramp will typically start at less than ground and ends above V_{ref}. With an on chip signal generator, it is often times not practical to do so. If full range coverage is critical to the application, some additional circuits may have to be introduced to fulfill this requirement.

As reviewed in the first chapter, the typical static performance metrics include DNL, INL, Offset, Gain etc. SEIR based BIST focuses on estimating INL performance which is one of the key parameters for static linearity. However to make it a full BIST solution that replaces traditional ATE test,

research has to be done to determine how to report the other performance metrics as well. In theory we should be able to derive DNL performance from INL, thus missing code performance can also be evaluated. However the accuracy of DNL and missing code estimation needs to be carefully studied. This work is not able to cover offset error and gain error of the ADC. The thought is to continue to use the ATE to measure the offset error and gain error since they are easy to measure on ATE. Very good DC references are typically required for those measurements but they are difficult to get on chip. [18] proposes a method based on SEIR to estimate offset and gain error on chip which is also a good alternative to look into.

This work is only targeting static linearity performance, not dynamic performance like SNR, THD etc. In order to derive dynamic performance, typically a good sine wave generator is needed. To implement a sine wave generator on chip with performance superior to the ADC under test remains a daunting task, which is not the focus of this paper. However, it will be another fundamental building block that is needed to reduce the dependency on mixed signal ATE to the minimum possible.

The SEIR method requires the standard least square method or other types of curve fitting algorithms to perform the nonlinearity estimation. It is anticipated that implementing the histogram method as well as SEIR on chip will occupy a large chip area even though they will be implemented as digital logic. Thus, it will need to be determined if it is cost effective to implement everything on chip to reduce ADC test cost while increasing chip manufacturing

cost significantly. One of the proposals is to exploit the processing power of the CPU that appears on most SOCs thus the algorithms would be implemented as software. Without dedicated hardware to perform the SEIR method, the estimation time needs to be carefully evaluated to see how large the impact is. The processing time will also be a critical component for field testing or calibration.

One of the challenges that is associated with implementing the histogram and SEIR method either in hardware or in software is memory allocation. A large amount of memory needs to be allocated to facilitate the task of calculating code bin width and performing curve fitting. Thus, the memory requirement need to be determined if the SOC is able to provide that memory. From a test perspective, we assume most of the memory is available for use during testing. From the digital calibration point of view, the calibration requires memory and adder/shift logic. The size impact can be significant if everything is implemented on chip. This is also an area of interest to explore further.

Overall, there are still challenges ahead to fully implement this BIST solution on chip. However it looks very promising and achievable since there are not major technical challenges here that prevent us from a real chip implementation.

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