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Nanoscale organic and polymeric field-effect transistors and their applications as chemical sensors

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Nanoscale organic and polymeric field-effect transistors and their applications as chemical sensors

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Dedication

To my parents

王秀岳 戚志红

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I owe my acknowledgement to my advisor Dr. Ananth Dodabalapur for guiding me to grow mature in scientific research. Acknowledgment is made also for the financial support through the research projects granted by NSF NIRT, DARPA, and AFOSR. Last but not the least, this dissertation could have been incomplete without the cooperation and help from my colleagues and friends Daniel Fine, Taeho Jung, Debarshi Basu, Suvid Nadkarni, Lawrence Dunn, Yeon Taek and Deepak Sharma.

Nanoscale organic and polymeric field-effect transistors and their applications as chemical sensors

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Supervisor: Ananth Dodabalapur

This work mainly focused on fabricating of nanoscale polycrystalline organic and conjugated polymeric thin-film field-effect transistors and investigating their scaling behaviors of electrical transport and chemical sensing properties. Devices with channel lengths systematically ranging from a few hundred microns down to sub 10 nm were successfully fabricated with the techniques such as stencil mask, photolithography, electron beam lithography, and break junction. The use of a novel four-terminal geometry ensures that the active area for charge transport and vapor sensing is truly nanoscale, and eliminates undesirable spreading currents traveling over the large area outside the defined channel to reduce the background signal level. It was discovered that upon scaling channel lengths from micron scale down to nanoscale, the dominating factors for charge transport and vapor sensing in organic thin-film transistors become different. At small dimensions, injection limited transport and field-dependent mobility are the dominant mechanisms for transport through the gate-modulated channel at low

and high longitudinal fields respectively. Furthermore for sub 10 nm channels, tunneling effect plays an important role. In micron scale devices, the drain current usually decreases as a sensing response upon exposure of the polycrystalline organic/polymeric semiconductor layer to the analyte, mainly because of the transistor threshold shift caused by the immobile charges at grain boundaries trapped by the dipolar analyte molecules. The vapor sensing behavior of nanoscale organic transistors is markedly different (in an opposite direction of response) from that of large-scale devices for the same analyte-semiconductor combination, due to the fact that the electrical transport in a nanoscale OTFT depends on its morphological structure and interface properties (such as the injection barrier at the metal-organic semiconductor contacts) which could be modulated by the delivery of analyte.

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Chapter 1

General introduction

1.1 History Perspective

Since the landmark discovery of conducting polymers in 1977 [1], much work has been done with small organic molecules and conjugated polymers to manufacture devices which take advantage of the unique properties of their conjugated π-electron systems, such as organic light emitting diodes (OLEDs), solar cells, smart cards, resistive chemical sensors and field-effect transistors [2-5]. Among these applications, the structure of field-effect transistors with an organic or polymer semiconductor as the electrically active layer, allows for the study of the two dimensional transport properties of the semiconductor material modulated by the charge carrier density due to increased gate bias [6-8].

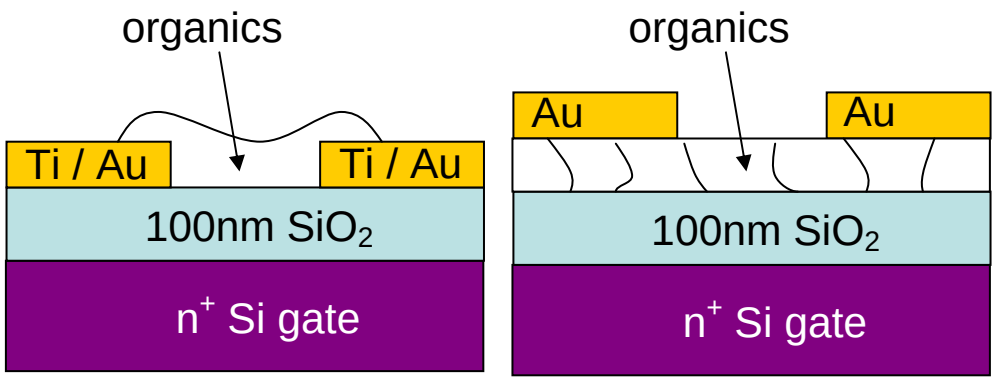


Fig. 1.1 Two typical architectures (top contact and bottom contact) in up-side down structure for organic transistors.

An upside-down transistor structure as shown in Fig. 1.1 for top and bottom contact architectures has been commonly used in organic FETs comprised of a rigid or flexible substrate, usually a highly doped silicon wafer or conductor covered plastic sheet, followed by a dielectric layer atop the substrate, such as silicon dioxide or an insulating polymer. The organic or polymer semiconductor and metallic source and drain contacts are then deposited on top of the gate dielectric [9-11]. This kind of structure reduces fabrication complexity and enables direct access to the active semiconducting layer to investigate its structure and morphology and how they relate to the electrical properties of the device.

Organic electronics will not replace classic Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) due to the low mobility values in organic materials

compared to that in single crystalline silicon. However, organic devices are still of considerable interest to the industry because of the low cost and mechanical flexibility of organic materials. In order to preserve this advantage, inexpensive methods have to be developed to fabricate organic devices. Field-effect transistors have been made with high mobilities (achieving 1 cm^2/Vs) from small organic molecules, such as pentacene, deposited by vacuum based sublimation [12, 13] and soluble conjugated polymers, such as regio-regular polythiophene, deposited by spin-coating, solution-casting or ink-jet printing processes [14-16]. Due to the relatively high cost in vacuum systems for subliming small molecules, conjugated polymers are preferred for industrial applications. To obtain high performance in polymer electronic devices, improvements in synthesis techniques are essential for high quality polymers with high purity, low residual doping and air stability. On the other hand, a solution based precursor technique for small molecules such as pentacene has been developed to be used in low cost processes such as ink-jet or spin-coat [17-19], which shed light on small molecules for their potentials in industrial applications.

1.2 Organic and polymeric materials

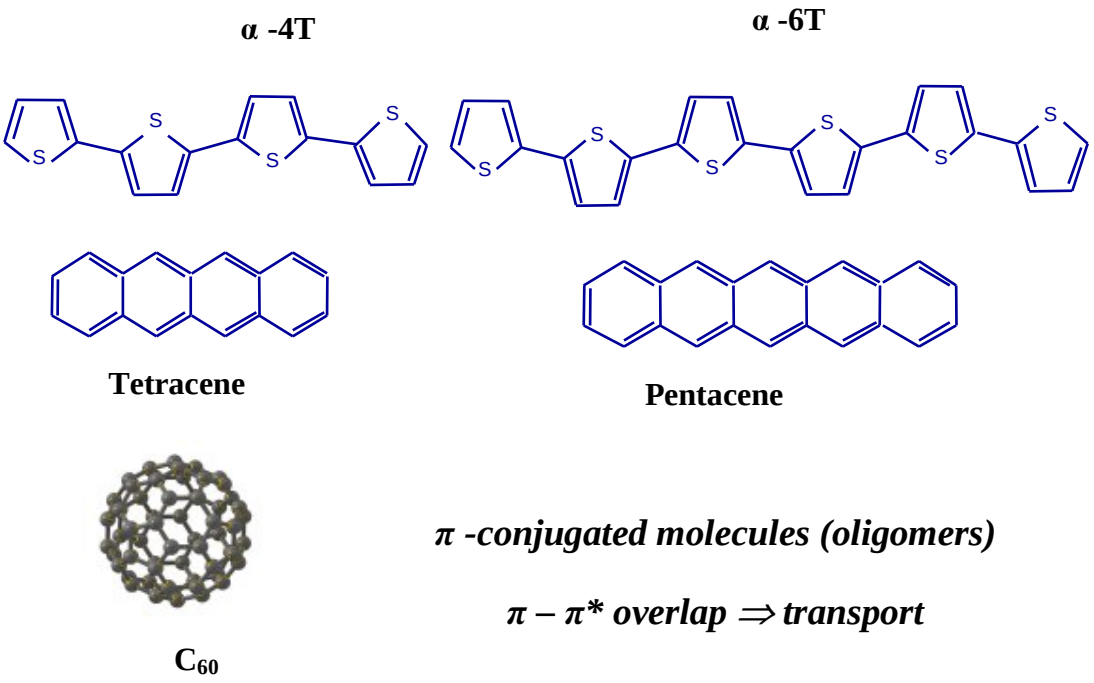


Fig. 1.2 Commonly used organic molecules. α-4T and α-6T are a chain of thiophene rings, and tetracene and pentacene are fused benzene rings. C_{60} demonstrates fullerene ball structure. CuPc and F-CuPc have a coordinate structure.

Fig. 1.2 lists the oligomer organic materials which have been commonly used in organic field-effect transistors. α-4T and α-6T are a chain of thiophene rings, and tetracene and pentacene are fused benzene rings, while CuPc (copper phthalocyanine) has a coordinate structure. All the aforementioned are p-type semiconductor with holes as the primary charge-carrier. In these materials, the mobility of holes is much higher than that of electrons, due to the process of electron traps. N-type organic semiconducting materials have also been drawing a lot of interest for applications such as Organic Light-Emitting Diode (OLED) and Complementary Metal Oxide Semiconductor (CMOS) circuits requiring bipolar carriers. C_{60} and copper hexadecafluorophthalocyanine (F_{16}CuPc) are commonly used n-type organic semiconductor materials.

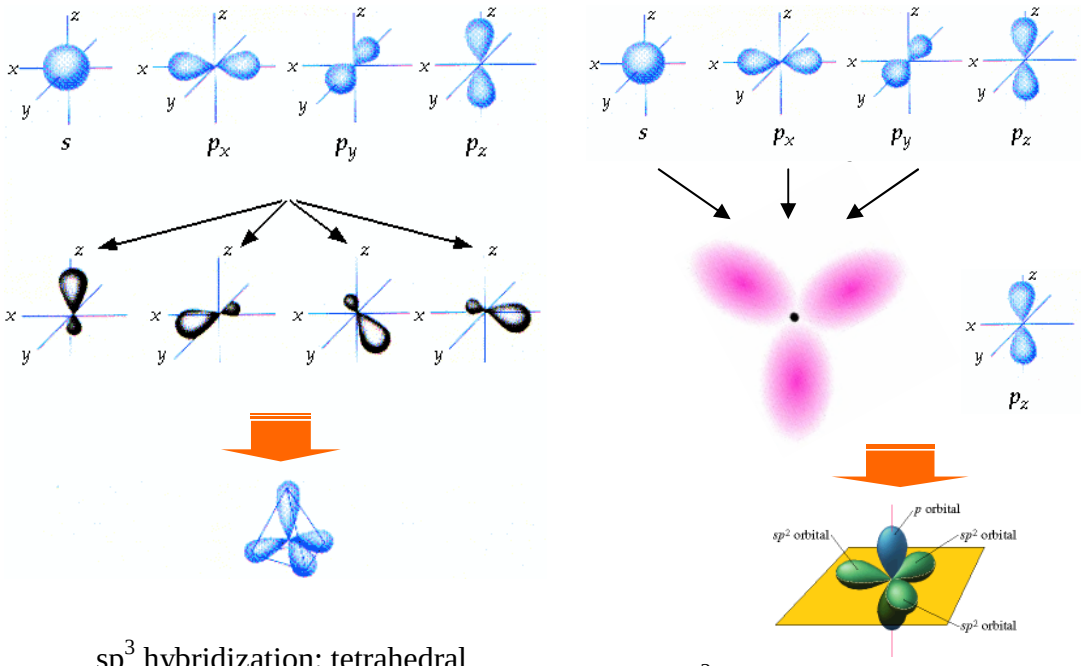
1.3 Theoretical aspect for the transport behavior in organic and polymeric materials

The semiconducting property of these organic materials originates from the delocalized π-electron (configured from sp^2 hybridization) in conjugated bonds (alternating single/double bond) between carbon atoms within one oligomer molecule or one polymer chain. In the following text, we will subsequently introduce these three key factors responsible for the occurrence of electrical transport, namely, sp^2 hybridization, conjugated bonds, and delocalized π-electron.

One carbon atom forms bonds to the surrounding atoms in two types of structures: tetrahedral-symmetric covalent bonds as in the diamond structure or hexagonal-

symmetric covalent bonds as in graphite. These are the basic structures to form compounds such as carbon-based oligomers or polymers. Of the former structure, insulating polymer such as polyethylene can be formed. These polymers are usually transparent. Of the latter structure, semiconducting conjugated polymer such as polyacetylene can be formed and these (usually chemically-doped) polymers possess a metal-like colorful glint.

There are four electrons in the outer-shell orbitals of a carbon atom denoted as $2s^2 2p^2$. When the carbon atom forms bonds with surrounding atoms, these four electrons rearrange themselves into four unpaired electrons (one electron jumps from s orbital to p orbital, noted as $s^1 p^3$). This process increases the system energy which is then reduced through the ensuing hybridization process. In the tetrahedral structure, all the four unpaired electrons on one carbon atom equally mix into each other through linear-combination to form four new energy-degenerated orbitals, known as sp^3 hybridization. Each of these four orbitals is able to form a σ bond (head-to-head) with one neighboring atom (such as carbon or hydrogen) and the four σ bonds are equally distributed in three-dimensional space which leads to a uniform bond angle of 109.5˚ [20]. In this tetrahedral structure, the electron configuration is saturated and no free electron is available for electrical conductance. The sp^3 hybridization of atomic orbital for bonding between carbon atoms is demonstrated in Fig. 1.3.



sp^3 hybridization: tetrahedral

sp^2 hybridization: triagonal

Fig. 1.3 The different hybridizations of atomic orbitals of a carbon atom.

1.3.1 sp^2 hybridization and alternating single/double bonds

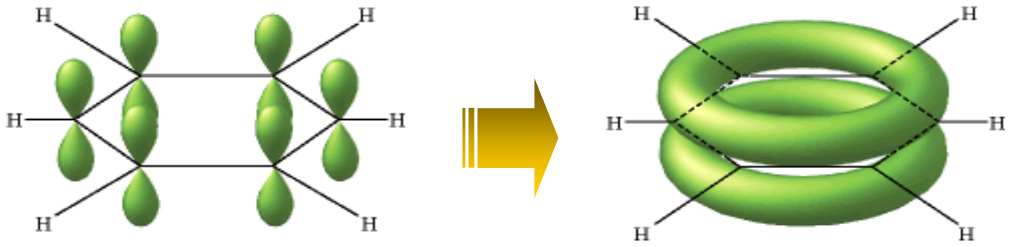
In the hexagonal structure, one electron from the s orbital and two from the p orbital hybridize into three new degenerated orbitals which equally lie on a two-dimensional plane forming a bond angle of 120˚ [20]. This is known as sp^2 hybridization, as shown in Fig. 1.3. These three hybridized orbitals pair with electrons from surrounding atoms by forming σ bonds. The remaining p_z electron (called π electron) forms π bond (shoulder-to-shoulder) with a π electron from the neighboring carbon atom. Therefore in

semiconducting organic molecules and polymers, there exist two type of coupling between neighboring carbon atoms: single bond (σ bond only) or double bond (σ bond plus π bond). The semiconducting property in an organic molecule and polymer chain arises from the alternating configuration of single/double bond.

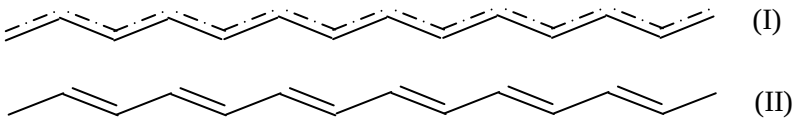
1.3.2 Organic molecular crystal

In organic crystals composed of small molecules, all the π electrons within one molecule form a delocalized π bond which makes electrons quite mobile inside a molecule, as shown in Fig. 1.4(a). The interaction between molecules is a weak Van der Waals force of attraction. Therefore the overlap of electron wave-function is much smaller than that in covalent bond. Consequently the mobility in organic molecular crystals is over two orders of magnitude lower than that in crystalline silicon where covalent bonds bind atoms into a lattice. The transport mechanism between molecules in organic semiconductors could be band-like transport [21,22], thermal activated independent hopping [23], correlated hopping [24,25] or tunneling [26].

Fig. 1.4 Alternating configuration of single/double bounds



(a) Two-dimensional delocalized π bond forms in small organic molecules.



(b) Due to the resulting instability in one-dimensional system, delocalized π bond depicted as (I) does not exist in a polymer chain; instead, an alternating configuration of single/double bond forms as (II) shows.

1.3.3 Conjugated polymer

There exists a two-dimensional delocalized π bond in small organic molecules. However in case of polymers which are one-dimensional chains, delocalized π bonds throughout the chain can not be formed due to its higher energy and the consequent instability of the system. Instead, the system chooses a conjugated state with a lower energy, where a π bond forms between every other pair of nearest carbon atoms so that single bonds (σ bond) and double bonds (σ and π bonds) alternate along the entire chain. This is the ground state of a polymer chain. In an exited state, with thermal activation or electron/hole dopants, a polymer chain will form either a soliton or a polaron. A polymer

chain usually forms two phases of ground state (two configurations of alternating single/double bonds), and the excited state of the polymer is the coexistence of these two phases of ground state. If the two ground-state phases (A and A') are symmetric and degenerated in energy, then the polymer will form a soliton in the excited state (the polymer configuration is then A+A' with A and A' interfacing over an interval of several carbon atoms), such as the case of trans-polyacetylene. If the two phases of ground state have different energies (phase A and B with energy B>A), then the polymer in the excited state will form a configuration as A+B+A with two lengthy phase A and one short phase B (only over a few carbon atoms). This configuration is called a polaron, such as the excited states in cis-polyacetylene and many other polymers. Since phase A and B are not symmetric and a single bond has a bond length different from a double bond, a polaron is a charge accompanied by a deformation of the lattice.

1.3.4 Charge transport in organic semiconductors

In most cases, the charge carrier contributing to electrical transport within conducting polymer materials is polaron. The intrachain transport mechanism is band-like polaron transport along the chain which is scattered by long wave-length acoustic phonon [27]. The interchain transport mechanism is phonon-assisted polaron hopping (perpendicular to the chain direction) and the major assists are from the optical phonon modes and the high-frequency acoustic phonon modes [28-29]. For transport between oligomer molecules, the charge carrier in most cases is hole (p-type material) and the

mechanism could be band-like transport, hopping or tunneling. In semiconducting organic materials such as molecular crystals and conjugated polymers, the band width is small so that we apply the terminology HOMO (highest occupied molecular orbital) and LUMO (lowest unoccupied molecular orbital) instead of those used for crystalline silicon (top of conduction band and bottom of valence band). This is the basic picture for transport within a single grain (a domain of well ordered oligomer molecules or well aligned polymer chains). The situation for transport between grains is complicated. Generally the presence of grain boundaries (the region between grains) limits the mobility of the polycrystalline organic semiconductors, because the disorder at grain boundaries leads to some localized states within the energy gap which trap the mobile charge carriers.

In addition to the above-mentioned transport mechanisms within the active organic semiconductor layer, the performance of an organic transistor also depends on many extrinsic factors, especially at the interfaces. The dielectric/semiconductor interface property affects the molecular ordering within one/two monolayers (equal to the channel depth) of the organic semiconductor, as well as determines the interface traps which also play a role on device mobility. The electrode/semiconductor interface property determines the injection barrier. In nanoscale transistors, the injection at contacts limits the transport of charge carriers at low gate bias and low source-drain bias, as well as leads to a sensing mechanism which is quite different from that in large scale devices.

1.4 The overall picture for scaling behaviors of organic transistors based on this work

This work mainly focused on fabricating nanoscale polycrystalline organic thin-film transistors (OTFTs) and investigating the scaling behavior of their electrical transport and chemical sensing properties. It was discovered that upon scaling the channel lengths of OTFTs from micron scale down to nanoscale, the dominating factors for charge transport and vapor sensing become different and the calculated mobility is not a constant any more. At small dimensions, injection limited transport and field-dependent mobility become the dominant transport mechanisms through gate-modulated channel at low and high longitudinal fields respectively. Fig. 1.5 demonstrates this scaling behavior in a big picture for channel lengths totally from 5 μm down to 10 nm.

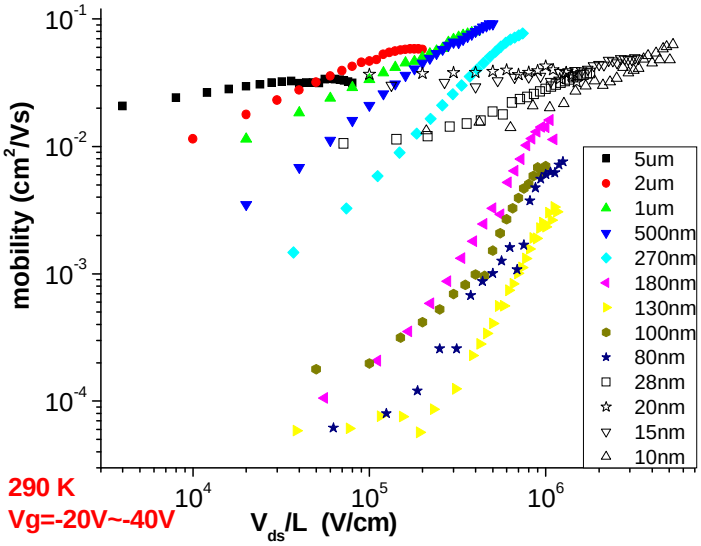


Fig. 1.5 The scaling behavior of charge transport in OTFTs. The channel lengths are ranging from 5 μm all the way down to 10 nm. Mobility was calculated through the transconductance at high gate biases for each longitudinal field, from the Id-Vds data taken at room temperature. Mobility-field curves were ploted on a full logarithmic scale.

The field-dependence of mobility is stronger at lower temperatures. Detailed explanation could be found in chapter 5. Additionally, for channels of ~20 nm or smaller, the mobility weakly depends on the longitudinal field. This is probably due to the non-uniform field distribution for these sub 10 nm channels with small W/L ratio (the field is uniform throughout the channel for those submicron devices with large W/L ratio) and due to the fact that at these small source-drain distances, the tunneling effect through the channel plays an important role which has a current-field relation quite different from that of hopping transport for field-dependent mobility in submicron devices. The detailed discussion about tunneling transport should be addressed to chapter 3.

Chemical sensing experiments examine the change of transport behaviors in OTFTs due to the delivery of analyte molecules. Correspondingly the sensing behavior would be different upon scaling, since the dominating transport mechanism becomes different at small dimensions. Fig. 1.6 is an overall look of the evolution of sensing behavior in OTFTs when channel length scales from 36 μm down to 33 nm. The use of a novel four-terminal geometry ensures that the sensor active area is truly nanoscale, and eliminates undesirable spreading currents which travel over the large area around the defined nanoscale channel. The sensor response was markedly different in nanoscale sensors compared to large-area sensors for the same analyte-semiconductor combination.

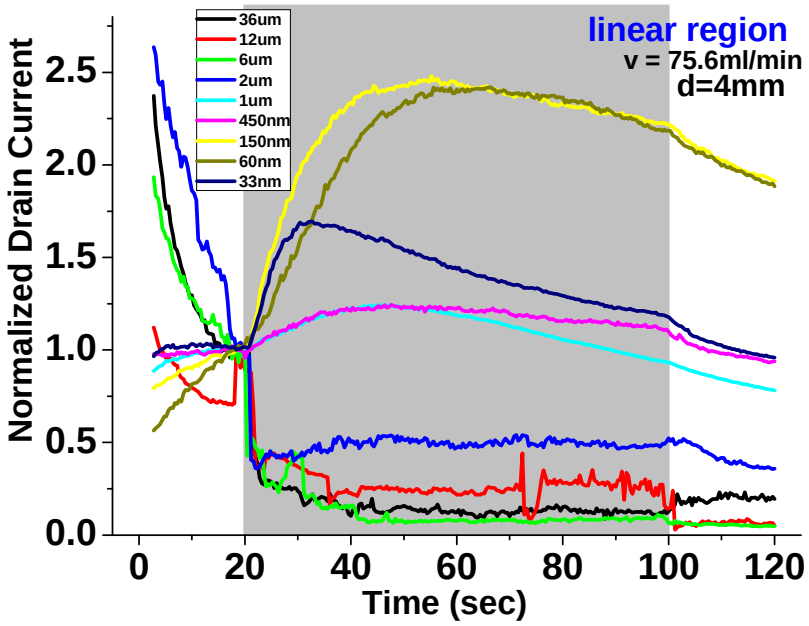


Fig. 1.6 The scaling behavior of chemical sensing by OTFTs. Here it is the pentacene TFTs sensing 1-pentanol vapor. Channel lengths range from 36 μm down to 33 nm. Sensing signal was detected from the drain current and it has been normalized to the current measured just before the analyte delivery. The shaded area indicates the interval when the organic semiconductor layer in an OTFT is exposed to the analyte.

In large scale devices, the drain current usually decreases as a sensing response upon exposure to the analyte, mainly because of the threshold shift caused by the immobile charges at grain boundaries trapped by the dipolar analyte molecules. The vapor sensing behavior of nanoscale organic transistors is different (here, in an opposite direction of sensing response) from large-scale devices for the same analyte-semiconductor combination, due to the fact that the electrical transport in a nanoscale OTFT depends on its morphological structure and interface properties (such as the injection barrier at metal-organic semiconductor contacts) which could be modulated by the delivery of analyte.

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Chapter 2

The fabrication of nanoscale organic thin-film field-effect transistors

Bottom-contact structures are preferred in the fabrication of nanoscale organic/polymeric thin-film field-effect transistors. To fabricate submicron devices, e-beam lithography is a commonly used tool in defining the electrode pattern. For top-contact structures, however, the lithography step has to be performed on top of the pre-deposited active organic layer, which degrades the organic material upon immersion in a solution, during developing and lift-off steps, or damages the organic material while evaporating metal atoms onto it. Hence, the bottom contact configuration is chosen over the top contact one. A heavily doped n-type silicon wafer serves as mechanical substrate and the gate. A SiO_2 layer that serves as the gate dielectric was then thermally grown on the substrate. The electrode patterns were made by e-beam lithography on a JEOL JBX-5DII. Metal electrodes with an adhesive layer (Ti or Cr) that improves sticking to SiO_2 were then deposited by e-beam evaporation in high vacuum, followed by a lift-off process. Gold was chosen as the electrode material, due to its high work function aiding the injection of holes into organic material, its air stability and its ability to form an ohmic contact with organic materials under certain optimal conditions.

2.1 The growth and characterization of gate dielectric layer

Prime grade heavily doped n-type silicon 4" wafers with (100) orientation were purchased to serve as the substrate and gate. The gate dielectric for the organic field-effect transistors was thermally grown oxide from the n^+ Si substrate which serves as the gate, due to the well-known high quality and mature fabrication techniques for thermally grown silicon dioxide. The single crystal silicon substrate was heavily doped by n-type dopants (Phosphorous or Arsenic) so that the depletion in the silicon as a gate was minimized. However, we found that the dopants in silicon diffuse under high temperature into the oxide if the oxide growth time is too long and cause significant gate leakage problems in the fabricated transistors. Therefore we chose the wet oxidation method (H_2 and O_2 ambient) instead of the dry method (dry O_2 ambient) in spite of the better quality and surface smoothness provided by dry method, simply because the dry method is a slower process and requires much longer time at the same temperature to grow the same thickness of oxide. In a typical example for growing oxide by the wet method, it takes 21 min at 950°C to grow 900 Å silicon dioxide out of n^+ silicon. After the oxide growth, the wafer was patterned with 70 μm X 200 μm pads of 30 Å Ti/500 Å Au, in order to characterize the capacitance-voltage with an HP 4284A LCR analyzer. Fig. 2.1(a) is a typical characteristic curve of areal capacitance versus DC bias for 850 Å SiO_2 grown on n^+ Si. The duration for each applied DC voltage is 1.5 sec which is long enough to exclude the deep depletion condition. The AC signal used to detect the capacitance values was set at 1MHz for standard high-frequency mode and 5 mV, an amplitude that is

negligible compared to the DC bias. As shown in Fig. 2.1(a), during the capacitance measurement, the silicon substrate was kept at ground, and Vg is the DC bias applied on gold pads. As seen in Fig. 2.1(b), the capacitance is slightly higher at the positive Vg end when n^+ Si is in the accumulation mode. The quality factor (Q) measured simultaneously for each datum point was always beyond 50 (most of them were beyond 100), which supports the integrity of the data. The measured areal capacitance (40 nF/cm^2) at the accumulation mode fits the calculated value for 850 Å SiO_2 (40.6 nF/cm^2) quite well.

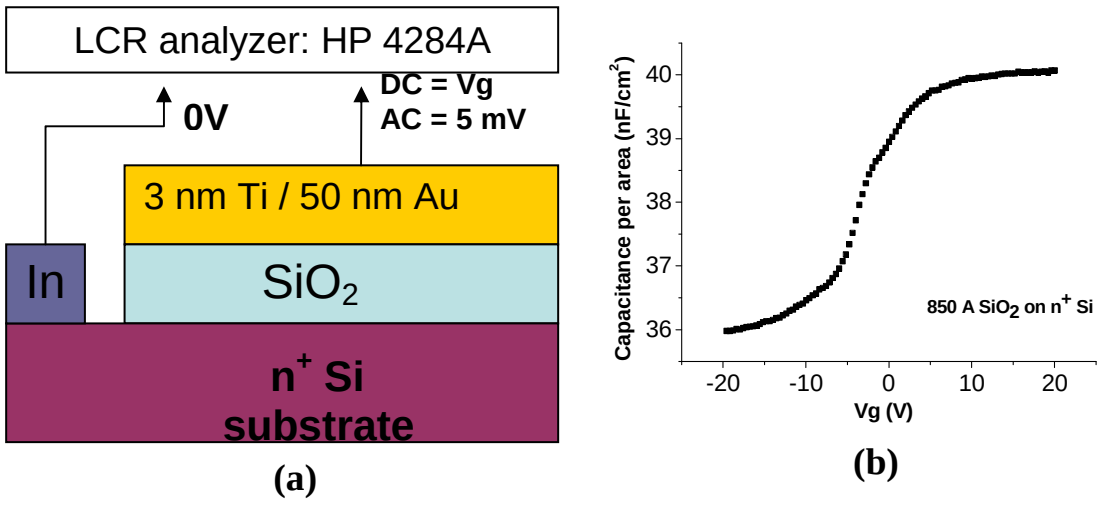

Fig. 2.1 The capacitance-voltage characteristic. (a) The experimental set-up for measuring the capacitance-voltage curve. (b) The capacitance-voltage characteristic curve measured at 1MHz for the oxide layer wet thermally grown on heavily doped n-type silicon.

2.2 The realization of nanoscale metal electrode patterns

In academia the best way to define nanoscale patterns is electron beam lithography. Due to its time cost, vacuum requirement and expensive maintenance, it is not a technique preferred by the industry except for mask fabrication. New techniques such as step-flash nanoimprint lithography have demonstrated the ability to fabricate nanoscale patterns down to sub 50 nm feature sizes with low cost, in a short time. Here we utilize e-beam lithography to define patterns, since our emphasis is not to improve the pattern technique.

E-beam lithography can be split into four steps, namely e-beam exposure, development, metal evaporation, and lift-off. To prevent particles from landing onto the wafer during fabrication, all these steps were implemented in a class 100 cleanroom without interruption.

After Pirhana clean (hydrogen peroxide : sulfuric acid = 1:2 in volume) and dehydration on 180°C hot plate, a SiO_2/Si wafer was spin-coated with ZEP520A e-beam resist, which is more sensitive than the commonly used resist PMMA. Spin rate of 3400 rpm for 1min generates a uniform layer of 400 nm thickness. Although higher spin rate and thereby thinner e-beam resist layer helps for better precision, it is not preferred here due to difficulties in lift-off. Based on our experience, 400 nm thick ZEP520A is already thin enough for 20 nm feature size and sometimes yields sub 10 nm devices. After spin-

coating, the wafer was prebaked on 180°C hot plate for 2min and then transferred into the e-beam chamber and kept for at least 3 hours to equalize its temperature with the environment (it is important for feature sizes < 30nm) before exposure to e-beam.

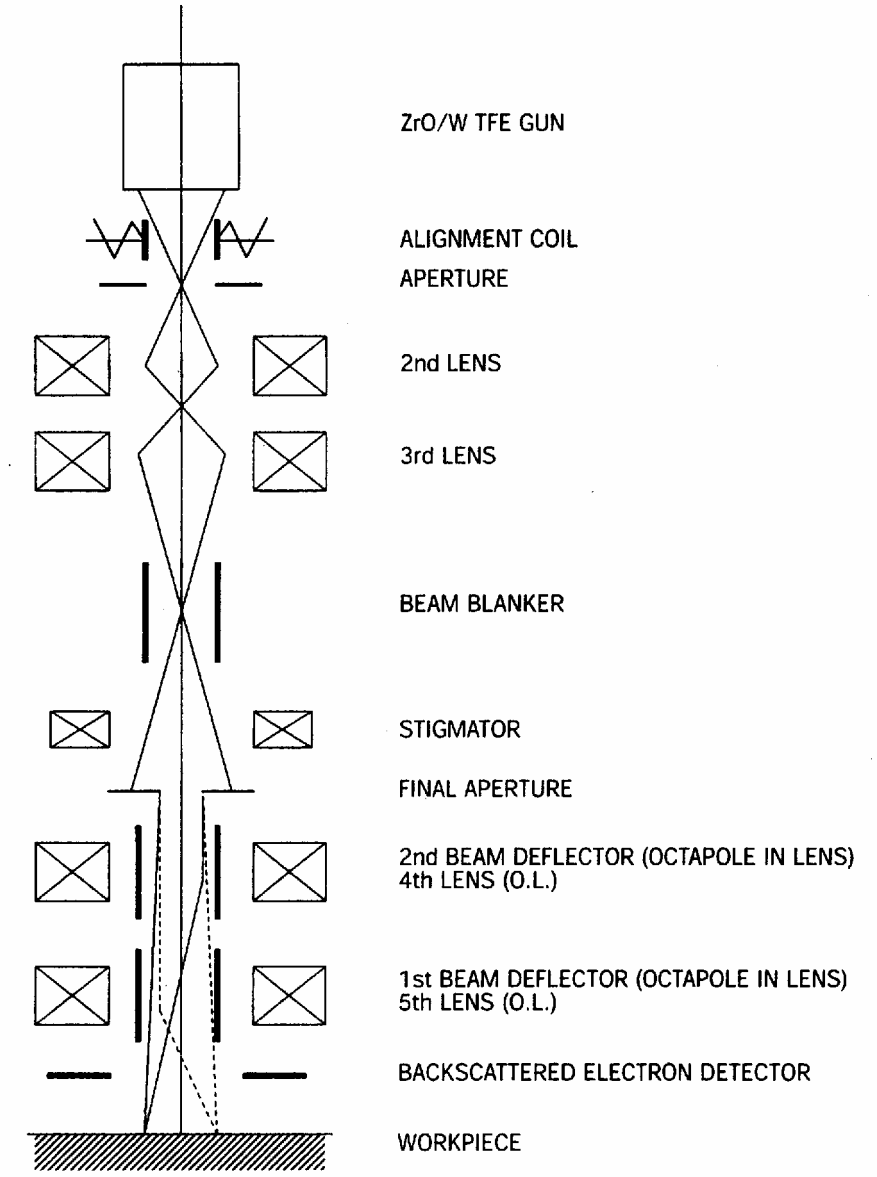

Fig. 2.2 The diagram for the principles of e-beam exposure.
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Fig. 2.2 is a diagram that shows the principal operation of e-beam exposure. To ensure the quality of defining patterns in nanoscale, the e-beam has to be adjusted before exposure to wafers. First of all, an alignment procedure was used to collimate the e-beam so that it was parallel to and met with the axis of e-beam lens. This involved the adjustment of the alignment coil and aperture in Fig. 2.2. The operation of this important step is shown in Fig. 2.3. A conducting (gold) particle of 100-200 nm in diameter could be used to observe when performing this step. When wobbling the e-beam in and out of focus continuously, if the SEM image of this particle is moving periodically, then the alignment is still not perfect.

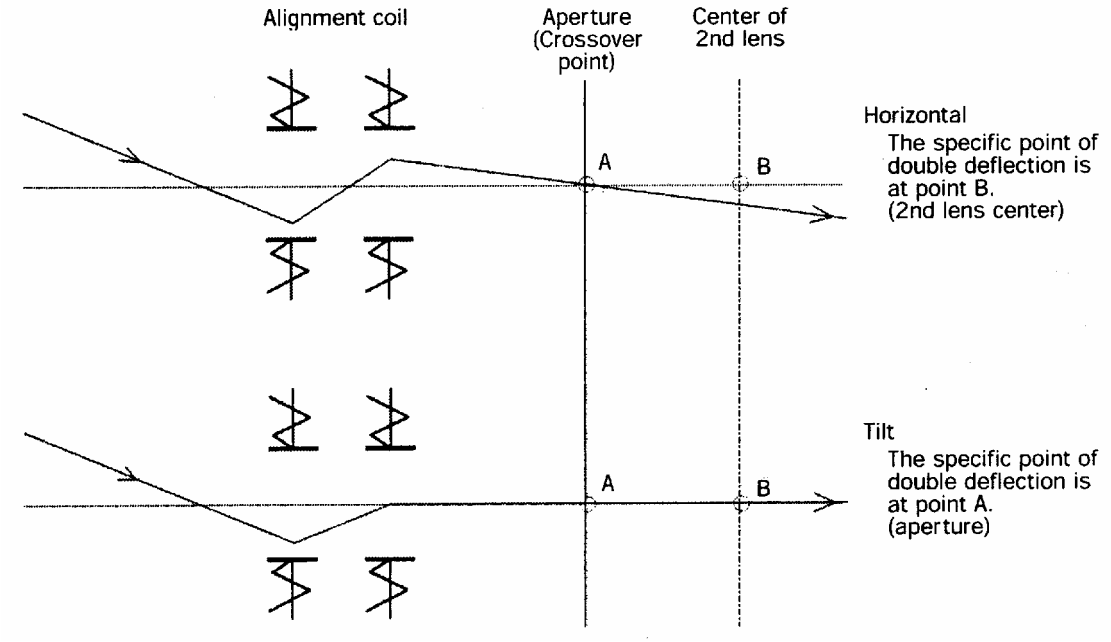


Fig. 2.3 The diagram for the operation of collimating e-beam in lens system. Reprinted with permission from JBX-6000FS/E General Statement, Copyright © 2002, JEOL Ltd.

After alignment, the e-beam is subject to an adjustment to correct the astigmatism. With the problem of astigmatism, the cross-section of the e-beam does not have a completely circular shape. Instead, it is an ellipse, which makes all the displayed SEM images stretch along one direction coherently when bringing the e-beam out of focus. The best pattern to observe for astigmatism correction is an array of complete round dots (<100 nm in diameter) made of metal. The object for long-time SEM display has to be conducting, because insulating material cannot dissipate charges quickly and thus deflect the e-beam. The last step before e-beam exposure is to focus the e-beam onto the wafer surface. This is realized by making a spot with the standing mode (not scanning) of electron beam in the ZEP520A layer on the wafer and then quickly observing its SEM image. The better focus status is, the smaller a spot can be made. After adjusting the focus to display the image of one spot, we move the stage which holds the wafer to make another spot at a different location and adjust the focus under a higher magnification. Usually a well-focused spot image should be observed under the magnification of $2 \text{ X } 10^5$ upon finish of this step, in order to pattern a line down to 20 nm wide.

The dosage of e-beam exposure is an important factor that affects the performance of e-beam lithography. The exposure is realized by discretely writing with spot-to-spot distance as step size. The actual dosage D is equal to $I \cdot t/d^2$, where I is the beam current, t is the duration of the exposure by electron beam on each spot, and d is the step size which is a multiple of 1.25 nm. The standard dosage D_0 is 180 $\mu C/cm^2$ for area exposure and 0.12 nC/cm^2 for line exposure, and the actual $D = D_0 \cdot r$, where r is the dosage ratio. The

parameters I, t, d have different influences on the pattern definition. Beam current and the actual dosage determine the time cost per area. It is difficult to maintain a very small beam current. The adjustment of dosage is reflected as the change of single spot duration time t, and the minimal t value is limited by 1/12MHz = 83.3 nsec. A smaller step size d is helpful for patterns definition with better precision. However, small values of d require very small t values which is subject to the limit of 83.3 nsec as minimum. Thus there exists a minimal d value for a certain actual dosage. The sizes of patterns designed in a gds file are not necessarily equal to those of actual devices after e-beam lithography, due to the choice of actual dosage D. Usually an over dose (actual pattern size larger than the design) is preferred as an optimal dosage, because a small-enough step size is necessary to generate sharp edges and uniform internal region. This effect is stronger in writing objects of smaller sizes. For example, Fig. 2.4 shows the relation between designed and actual geometries ("gap" means channel length), where the optimal dosage for larger objects (>150 nm wide electrodes) is ~50% of D_0, whereas the optimal dosage for smaller objects (40 nm wide wire) is ~15% of D_0. Around these optimal dosages, the relation between the designed and actual geometries was experimentally found to be expressed as the empirically linear equation shown in Fig. 2.4.

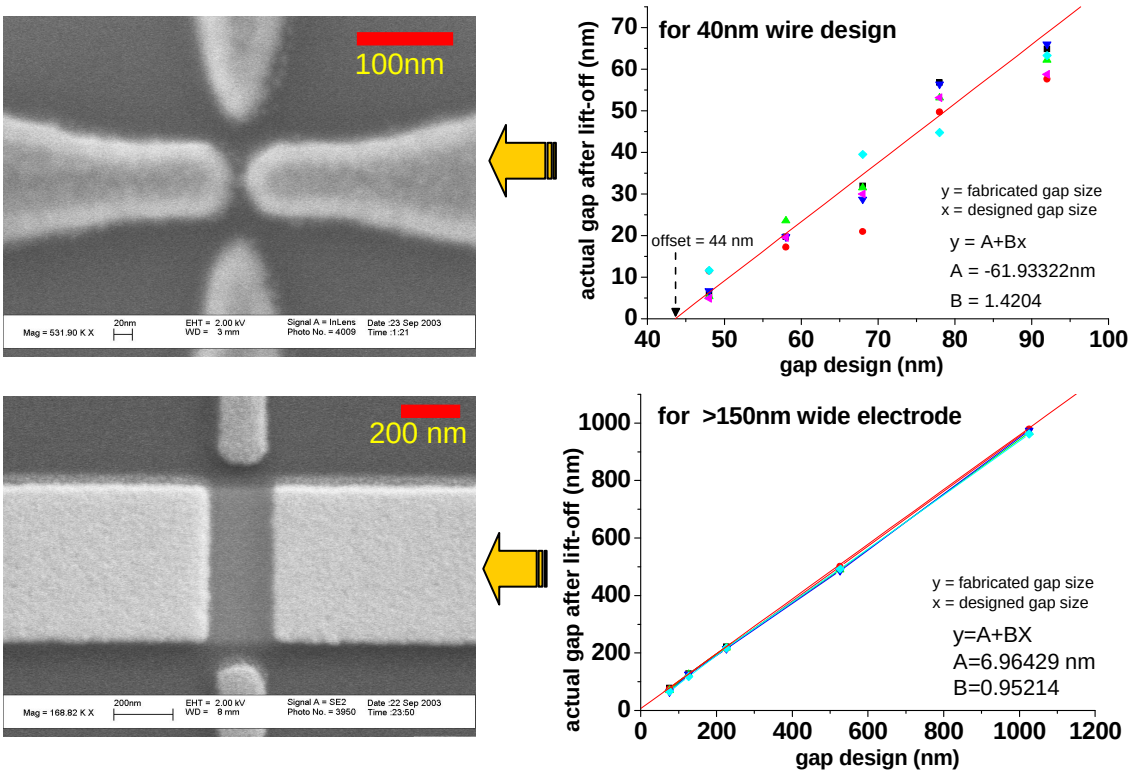


Fig. 2.4 The empirical equation about the obtained channel length versus the designed channel length in an optimal range of e-beam dosage.

After e-beam exposure, the wafer was developed in ZED-N50 developer for 90-120 sec and rinsed by soaking the wafer in a solution of IPA for > 1min and then washing with flowing IPA. It is important to note that after developing the e-beam resist, the wafer should not be post-baked because it deforms the sidewall and changes the lateral profile of the e-beam resist on a ~ 1 μm scale, and it makes lift-off difficult. Also the wafer should not stay too long (preferably < 24 hours) before metallization. Although e-beam resist is not sensitive to light like photoresist, long delays between development and metallization still affect the quality of fabrication due to the accumulation of airborne

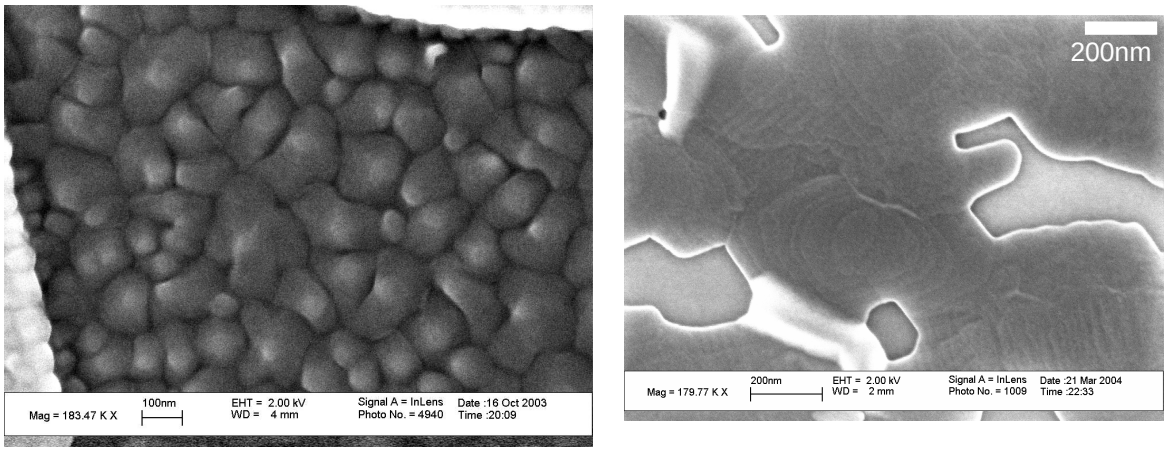
particles onto the unfinished wafer surface. Metallization was conducted in an e-beam evaporator which utilizes the high energy (10keV) of an electron beam to evaporate the target atoms. The vacuum of the chamber should be as high as 2-3 μTorr in order to obtain high quality metal layer. It is important to monitor the substrate temperature during this step, so that it is not high (>55 °C) enough to postbake the resist and thereby make lift-off difficult. Lift-off was done with the e-beam resist stripper 1-Methyl-2-pyrrolidone (NMP). The operation was conducted with a gas-filter mask in a fume hood. Usually ultrasonic agitation was applied to facilitate the lift-off of resist. For nanoscale devices, it is important to minimize the agitation intensity and time, to preserve the small features. Therefore it is a good idea to pre-soak the wafer in NMP for 5-8 hours to completely lift-off in aid of agitation for only about 1 min. No chemical reaction between NMP and the metal layer was found for this duration in NMP. NMP is a kind of reagent with potential hazards to human beings. A non-toxic substitute (photoresist stripper RS-111 from Cyantek) was tried by the author and it showed the same lift-off result as NMP.

2.3 The deposition of organic semiconductor (pentacene) layer

2.3.1 The influence of growth rate and substrate temperature

Bottom-contact devices were completed by thermally evaporating 300 Å-600 Å of pentacene (purchased from Aldrich) with a base vacuum of about 3×10^{-7} Torr at different growth rates and different substrate temperatures for different grain sizes.

High growth rates (4.4-7.1 Å/sec) at room temperature during thermal evaporation gave a pentacene layer of small grains with an average size of 80-140nm. Nanoscale channels comprised of larger pentacene grains, with an average size of 250 nm, were achieved by depositing pentacene with a slow growth rate (0.5 Å/sec) at room temperature. For channel lengths greater than a micron, an elevated substrate temperature (80 ºC) and a moderate growth rate (1.9 Å/sec) during deposition resulted in large grains with an average size of 1 μm. Attempts to deposit large pentacene grains onto nanoscale channels at elevated substrate temperatures did not yield favorable results. This could be attributed to the repulsion of the Au electrodes to the pentacene molecules at elevated substrate temperatures.



(a) **(b)**

Fig. 2.5 The Scanning Electron Microscopy (SEM) image of pentacene grains thermally deposited on SiO_2. (a) under high evaporation rate with substrate at room temperature; (b) under medium evaporation rate with substrate at elevated (80°C) temperature.

As shown in Fig. 2.5(a), under the normal condition (high evaporation rate with the substrate at room temperature), the size of the grown pentacene grains ranges in the order of 100 nm, with more disordered regions around the metal-organic semiconductor contact. The mobilities of the transistors based on this kind of pentacene layer were of the order of 10^{-2} cm^2/Vs, with a highest value of 0.12 cm^2/Vs observed in air for the transistors with a channel length of 1 um and W/L = 10. Fig. 2.5(b) shows the Scanning Electron Microscopy (SEM) image of the pentacene layer grown at a moderate evaporation rate and elevated substrate temperature. Under this condition, larger grains (~1 μm) were obtained as shown in Fig. 2.5(b). However the grain boundary spacing becomes larger under elevated substrate temperatures during growth, which might reduce the overall mobility and influence the chemical sensing properties.

2.3.2 Substrate surface cleaning

Generally a slower evaporation rate and higher substrate temperature gave larger grains and planar morphology. The substrate temperature has a stronger influence than the evaporation rate. Another factor which might affect the morphology of the organic semiconductor layer is how clean the substrate surface is. Organic semiconductor molecules like to stay and grow on hydrophobic surface. Table 2.1 summarizes the results for growing pentacene layer under different conditions.

Table 2.1 The average grain sizes of pentacene layer grown under different conditions

Average grain size	Pre-clean condition	Substrate temperature	Growth rate	Nominal thickness
77 nm	hot NMP	Room Temperature	10 Å/sec	750 Å
86 nm	O_2 plasma	Room Temperature	9.5 Å/sec	500 Å
125 nm	acetone	Room Temperature	11 Å/sec	750 Å
133 nm	acetone	Room Temperature	1 Å/sec for 1st 100 Å, then 10 Å /s	800 Å
140 nm	O_2 plasma	Room Temperature	5.9 Å/sec	500 Å
248 nm	boiled acetone	Room Temperature	8.5 Å/sec	665 Å
253 nm	hot NMP	30 ºC	0.7 Å/sec	800 Å
438 nm	N_2 plasma	63 ºC	0.8 Å/sec	500 Å
> 1um	O_2 plasma	83 ºC	2.5 Å/sec	370 Å
NMP = 1-Methyl-2-pyrrolidone				

Before depositing organic semiconductor molecules, the substrate has to be cleaned due to the organic residue left by photolithography/lift-off steps. For the commonly used substrate SiO_2, there are basically two ways to clean the surface: solution based and plasma based. The usual acetone/methanol/Deionized water clean cannot

remove the organic residue layer. The hot NMP (1-Methyl-2-pyrrolidone), heated under fume hood up to 90°C—its boiling point is able to remove the organic residue layer, but the substrate surface after cleaning is still not as hydrophilic as plasma cleaning. Both of oxygen and nitrogen plasma can remove the organic residues inherent from photolithography steps, while oxygen plasma at the same RF power intensity will cause more damage on SiO_2 surface, as shown in Fig. 2.6. The damage in Fig. 2.6 was caused by the oxygen plasma with a RF power intensity of 50 W over an area of 16 square inches, continuing for 3 min. However we found that under a RF power intensity of 25 W per 16 sq. in. for < 1min, oxygen plasma does not cause observable damage. We define this condition as “gentle oxygen plasma cleaning”. The effectiveness of nitrogen plasma in completely removing all the organic residues from every source of fabrication steps, is doubtful. As a result, gentle oxygen plasma cleaning is preferred rather than nitrogen plasma cleaning, to clean the wafer before organic semiconductor deposition.

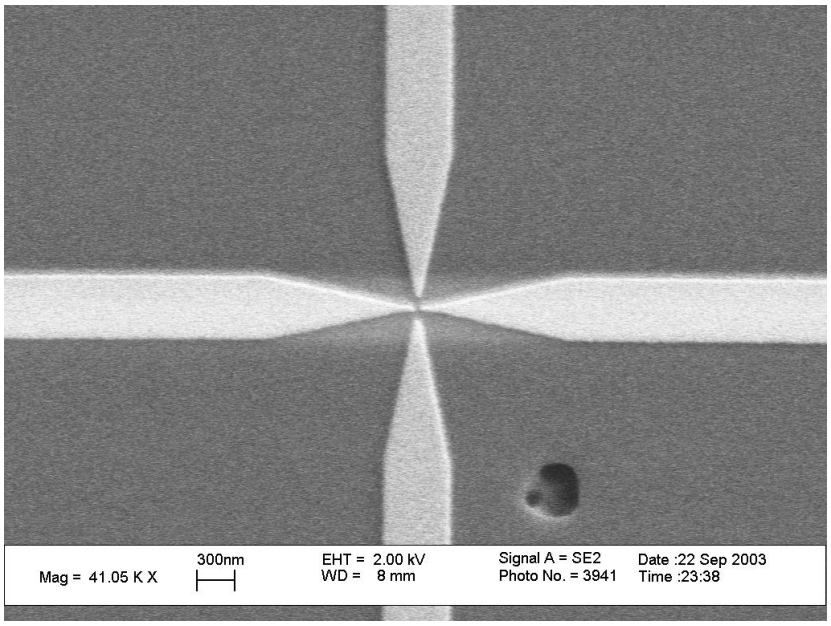


Fig. 2.6 The damage caused by strong and long-time oxygen plasma on the SiO_2 surface around a nanoscale device.

There is an alternative way for oxygen plasma clean, so called UV-Ozone, which utilize the strong oxidizing property of ozone enhanced in presence of ultraviolet radiation. Fig. 2.7 is an example for the influence of cleaning conditions on the organic semiconductor growth. It shows the Atomic Force Microscopy (AFM) images of pentacene layer grown with different pre-cleaning conditions. As mentioned before, organic semiconductor molecules tend to grow on hydrophobic surfaces. Therefore the average grain size of the pentacene layer obtained on hydrophilic substrate surface (cleaned by gentle oxygen plasma) is smaller than that on hydrophobic surface (cleaned by acetone).

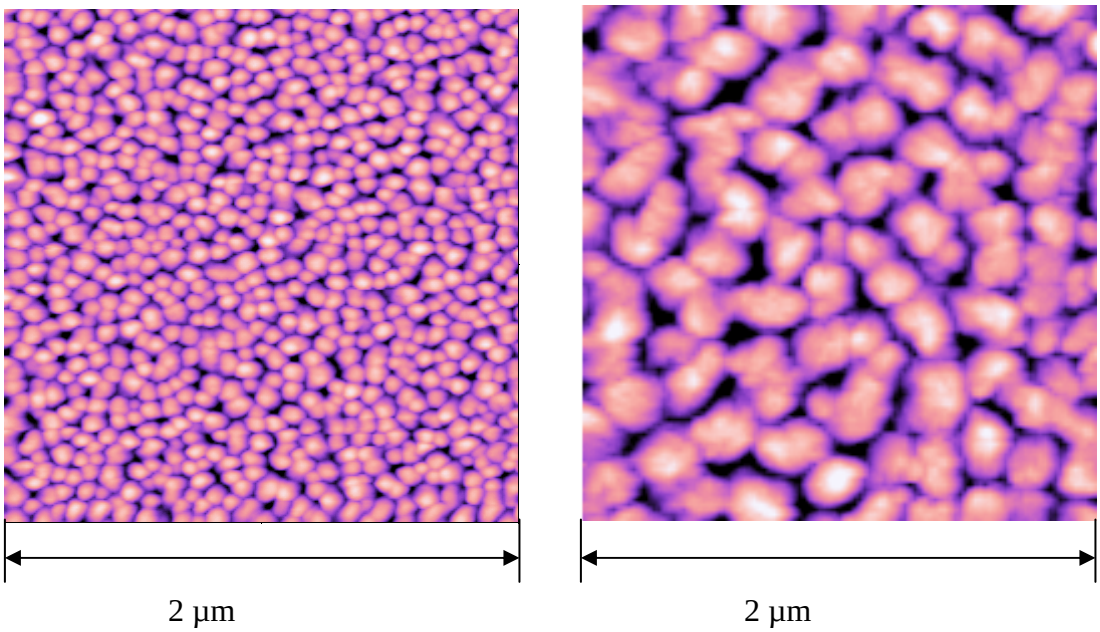


Fig. 2.7 The Atomic Force Microscopy (AFM) images of pentacene layer grown with different cleaning conditions (left: oxygen plasma clean; right: acetone clean), which lead to different grain sizes and various morphology.

2.3.3 Substrate surface treatment by self-assembled monolayers

To form an organic semiconductor layer with high mobility in field-effect transistors, the requirements for the quality and the morphology of the organic thin film are stiff. The source material to be evaporated has to be in high purity, usually post-purchase purified with cycling many times under a temperature gradient in vacuum. The grown film has to be uniform, flat, and have an ordered molecular stacking. For this purpose, after UV-ozone or gentle oxygen plasma cleaning, a surface treatment is desired to form a well-ordered self-assembled monolayer of alkyl groups, before depositing organic semiconductor layer.

Two commonly used materials for a self-assembled monolayer on top of SiO_2 are HMDS (Hexamethyldisilazane) and OTS [Trichloro(octadecyl)silane]. These molecules have two functional groups: silane group on one end and alkyl group on the other end. Under certain conditions (temperature and pressure), when these molecules come to the surface of SiO_2, they react with the surface dangling OH group which binds to the underlying Si atom by covalent bond. By excluding the byproduct such as HCl or NH_3 at a certain temperature (>110 °C usually), these molecules can then successfully bind to SiO_2 through Si-O covalent bond contributed by their silane group. Theses molecules can form a well-ordered large area by Van der Waals interaction along the lateral orientation, so that all the alkyl groups will head up and align to each other. Organic semiconducting molecules such as pentacene can then bind to these alkyl head groups by hydrophobic interaction, so that pentacene molecules can form an ordered layer. This results from the underlying well ordered self-assembled monolayer, over a large area. There is an optimal length of alkyl group in the case of self-assembled monolayer described here. Too short an alkyl group will not maximize the Van der Waals interaction for large area order as well as the hydrophobic interaction for accepting organic semiconductor molecules. Too long an alkyl group tends to bend and entangle for maximal entropy, which reduces the large area order of the monolayer. OTS has the optimal length of alkyl group. However HMDS is still employed due to its higher stability in air compared to OTS.

There are generally three methods to form the self-assembled monolayers: vacuum based evaporation, solution casting (soaking), and spin-coating. No matter which method is used, it is important to leave the dangling OH group at the top of SiO_2 layer to form the necessary Si-O covalent bond. This could be fulfilled by simply soaking the wafer in deionized water first then drying with nitrogen flow but no further drying in an oven or on a hot-plate. Meanwhile it is also very important to keep the ambient free of humidity, otherwise the HMDS or OTS molecules will react with the water molecules before they arrive at the wafer surface. This requirement could be fulfilled in vacuum or nitrogen environment.

Vacuum based evaporation is the best method in terms of the quality of the self-assembled monolayer. After purging the chamber with nitrogen, a vacuum below 100 mTorr is formed, followed by the introduction of the molecules of source material into the chamber for self-assembly. The chamber is always kept above 110 °C (150 °C for HMDS) for degassing the byproduct. However, this method requires relatively expensive and sophisticated equipments. An alternative method is to let the wafer stay in the upper space beyond the HMDS or OTS liquid surface at room temperature for a long time (> 8 hours). In the solution casting method, the wafer is soaked for 1-2 hour in a solution of the designated molecules dissolved in chloroform or ethanol with a concentration of 1-10 mM. The spin-coat method is the fastest (~ 5 sec) but not optimal for the formation of self-assembled monolayers due to the short time duration of designated molecules remaining on the wafer surface.

2.4 The identification of deposited pentacene layer

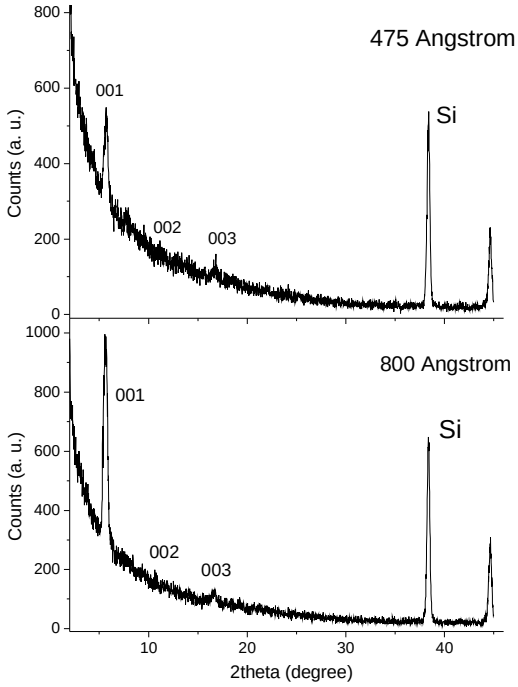


Fig. 2.8 The Small Angle X-ray Scattering spectrum of pentacene layers of different thicknesses.

For thin films of organic semiconductors such as pentacene deposited on Si/SiO_2 substrates, we have to use Small Angle X-ray Scattering (SAXS) for identification of the material's structure. Normal X-ray scattering method scans the incident angle (the angle between incident X-ray and the sample substrate plane) in a certain range, while keeping the incident X-ray beam and the detector (for the scattered X-ray) always symmetric to the sample substrate plane. However for thin films (< 100nm) deposited on a silicon or glass substrate, the detector in this manner cannot collect enough scattered X-rays at most of the incident angles. For incident angles larger than 5 degrees the scattering volume

involved in a thin-film is too small to be detectable. Therefore we use an alternative method Small Angle X-ray Scattering (SAXS) for the identification of the thin film material. In this method, the incident angle is kept at a small constant value (usually 3 degrees), and the detector is scanned to detect the scattered X-rays at different angles (as in Fig. 2.8, 2θ = angle between incident beam and scattered X-ray). Meanwhile, in SAXS method, a slice-source parallel to the sample plane instead of point source in the normal method, is used for the incident X-ray. By these two techniques, at every 2θ there is enough scattering volume involved to provide observable data for identification. Fig. 2.8 shows the SAXS data for pentacene layers of two different thicknesses. We swept the 2θ until the peak of the single crystal silicon substrate appears as an internal reference. With comparison to the literature [1, 2], we identified that the peaks in Fig. 2.8 represented the 001, 002 and 003 planes of pentacene. The 001 peak of pentacene was clear, while the 002 and 003 peaks did not possess enough intensity. It is also important to note that the peak positions for different thicknesses of the same material are the same, while the thicker film (800Å pentacene) features higher intensity, which indicates that these peaks are for the film instead of the underlying substrate.

2.5 Tips for fabricating organic thin-film field-effect transistors

To obtain high performance in organic devices and to study the transport behavior through the metal-organic interface and the gate-induced channel of polycrystalline organic layer (p-type), several experimental guidelines are recommended:

- employ bottom contact structure to avoid damage to organic layer in top-contact structure;
- utilize high work function and air stable metal as electrodes;
- employ an adhesive metal layer of 3nm or thinner;
- for good contact-sidewall profile, apply image-reversal photolithography technique before lift-off of metal electrodes or wet-etch metal electrodes to obtain ramping profile by under-cut;
- before depositing organic layer: apply UV ozone to clean the substrate and then treat the gate-dielectric and electrodes sequentially with two orthogonal self-assembled monolayers;
- purchase trap-free organic semiconductors and purify in temperature-gradient with multiple cycles under vacuum.

References:

[1] C. D. Dimitrakopoulos, A. R. Brown, and A. Pomp, J. Appl. Phys. 80 (4), 2501(1996)

[2] I.P.M. Bouchoms, W.A. Schoonveld, J. Vrijmoeth, T.M. Klapwijk, Synthetic Metals, 104, 175–178 (1999)

Chapter 3

The transport behavior of sub 10 nm OTFTs at room temperature

3.1 Introduction

Large scale organic thin-film transistors have received great interest from the scientific community due to their use in potentially low cost, large-area circuits, and their relatively high mobility [1,2]. It has significance in fundamental science and industrial applications to study the transport behavior at nanoscale dimensions. Characteristics of top contact organic thin-film transistors have been reported for channel lengths down to 30 nm fabricated with e-beam lithography [3]. Recently several groups reported their work on the performance of bottom contact organic thin-film transistors down to 50 nm [4] and 30 nm [5] channel lengths, also defined by e-beam lithography. Compared to expensive and time-costly e-beam lithography process, emerging techniques such as nanoimprint lithography combined with dry etching process have captured the attention of industry due to their potential as fast and inexpensive candidates to fabricate nanoscale devices. There have been several reports for utilizing these techniques to fabricate organic/polymeric transistors with channel lengths of 500nm [6] and 70nm [7]. However, the electrical transport properties of pentacene have not been studied in transistors with channel length near 10 nm. The transport mechanisms would be different when the channel length of a transistor shrinks to sub 10 nm, since tunneling effects

become important at these dimensions and it is also likely that charge transport between source and drain takes place through a single grain. Charge injection from the contact would play a very important role in such small geometry device as well. Indeed, we could have a situation in which the local morphology of organic semiconductor in the vicinity of the channel dominates the device behavior, leading to huge variations in individual transistor responses.

3.2 The design of guarding electrodes for true detection of nanoscale transport

Nanoscale organic field-effect transistors are meaningful in terms of scientific importance and industrial potential. However, it is technically difficult to pattern the active semiconductor area of devices with such small channel lengths. For transistors with a channel length near and below 10 nm, a large W/L ratio is not favorable due to a higher chance of shorted electrodes [5] and electrode edge roughness of the order of the channel length. Consequently, the spreading currents which travel outside the defined channel cannot be ignored for devices with small W/L ratios, and it becomes a concern if W/L is less than 10 [8]. We have fabricated a large number of devices in which the channel length is below 50 nm, with a small W/L ratio, and in which the active semiconductor layer and gate are not patterned. In such devices the spreading current which travels outside the defined channel will contribute to a large percentage of the total current. To collect the spreading current, we employed a separated pair of guarding electrodes near the two sides of the channel, unconnected to and kept at the same

potential as the drain. By this design, these guarding electrodes collect the spreading currents so that the drain current measured, is the direct current from source to drain, excluding contributions from macroscale spreading currents, as shown in Fig. 3.1. Devices were fabricated with below 50 nm channel lengths, small W/L ratios, and non-patterned active semiconductor layer and gate. The distance between a channel and its side guards in the produced devices ranges from 20 nm to 50 nm, almost comparable to the channel lengths. Measurements of the drain current were taken on the same device without biasing the side guards (I_{open}) and also with the side guards biased (I_{ds}). For nanoscale devices, I_{ds} and I_{open} manifested different behaviors. I_{open} behaved more like a long channel FET, which indicates a substantial component of spreading current. For each of the measured devices, the maximum value of I_{ds} was significantly lower than that of I_{open} under the same voltage configuration, and the ratio (I_{ds}/I_{open}) was below 70%. This ratio was found to positively correlate to the W/L ratio. The distance between a channel and its side guards and the geometry of the electrodes may affect I_{ds}/I_{open} ratio.

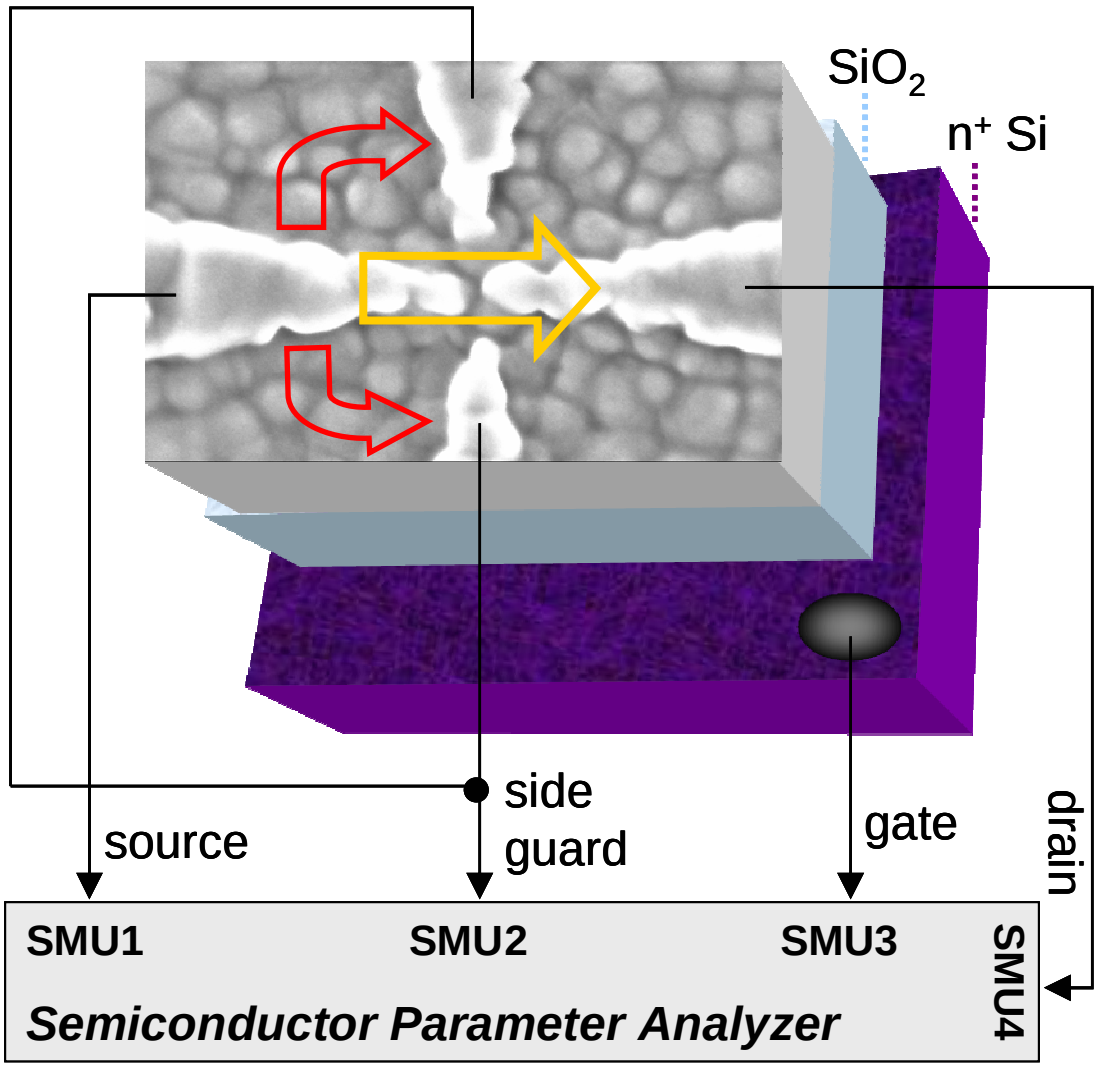


Fig. 3.1 3D device structure and circuit diagram for the function of side guards in a nanoscale transistor used as chemical sensor. To collect spreading currents traveling through the area outside the defined channel, two side guards were designed on the two sides of the channel, unconnected to and kept at the same potential as the drain. The three layers from top are bottom-contact pentacene and Au/Ti electrodes (surface shown by a SEM image of real device), SiO_2 as dielectric, n^+ Si as gate. Each SMU (Source-Measurement-Unit) of the Semiconductor Parameter Analyzer (Agilent 4155C) supplies voltage and measures current independently. SMU1, 2, 3, 4 serves as the source, side-guard, gate and drain, respectively. SMU1 = ground; SMU3 = V_g; SMU2 and SMU4 were set at the same value V_{ds}. Reprinted from Liang Wang, Daniel Fine, Deepak Sharma, Luisa Torsi and Ananth Dodabalapur, Analytical and Bioanalytical Chemistry, Vol. 383, No. 7, Dec. 2005, with kind permission of Springer Science and Business Media.

3.3 Experimental

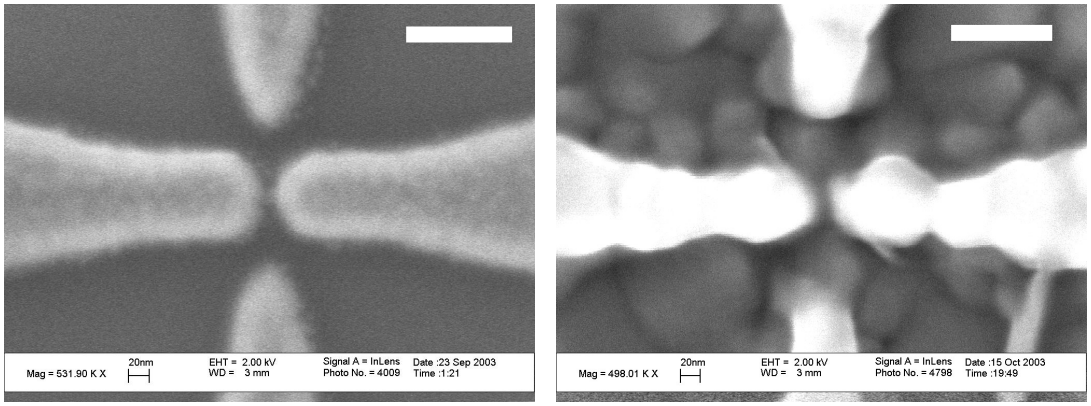


Fig. 3.2 SEM images of electrodes and semiconductor layer. (a) SEM image of a 5 nm channel just before pentacene evaporation. (b) SEM image of a 9 nm channel after I-V measurement. The white scale bars are 100 nm. Reprinted with permission from Liang Wang, Daniel Fine, Taeho Jung, Debarshi Basu, Heinz von Seggern, Ananth Dodabalapur, Appl. Phys. Lett., 85 (10), 1772 (2004). Copyright 2004, American Institute of Physics.

The 3D structure of a transistor device is shown in Fig. 3.1. A heavily doped n-type silicon substrate serves as the gate and a 100 nm thermally grown SiO_2 layer is used as the gate dielectric. The electrode patterns were defined by e-beam lithography on a JEOL JBX-5DII. 3 nm Ti / 45 nm Au was then deposited by e-beam evaporation, followed by a lift-off process. Electrode patterns of channel lengths ranging from 40 nm down to sub 10 nm were obtained. A pattern of a 5 nm channel with side guards as close as 20 nm away is shown in Fig. 3.2(a). Bottom-contact devices were completed by thermally evaporating 600 Å of pentacene (purchased from Aldrich) at a growth rate of 9 Å /sec with a base vacuum of 8×10^{-7} Torr. This gave an average grain size of about 100 nm. A HP 4145B Semiconductor Parameter Analyzer was used to measure the DC

electrical characteristics of the transistors in air at room temperature. The leakage currents through the gate dielectric were negligibly small compared to the source-drain currents. After the measurements, all the devices were examined by a field-emission SEM (LEO1530). About 20% of the patterned devices exhibited significant electromigration effects and were eliminated from the following characterization study.

3.4 Results and discussion

3.4.1 Good contact situation

Fig. 3.2(b) shows the post-measurement SEM image of a bottom-contact pentacene transistor of 9 nm channel length. By applying the same potential as the drain on the two side guards, the true source-to-drain current ($-I_{ds}$) was observed as shown in Fig. 3.3(a). The behavior of I_{ds} exhibited reasonable gate modulation. Due to the thickness of the gate dielectric layer (100 nm SiO_2), the operating gate voltage (V_g, up to -30V) in most cases is much higher than the operating drain voltage (V_{ds}, up to -5V), which causes the FET to operate in the linear region. Fig. 3.4 shows the calculation of field-effect mobility derived from the transconductance of I_{ds} in the linear region (at V_{ds} = -3V). The calculated mobility and on/off ratio (at V_{ds} = -5V) for this device are 0.046 cm^2/Vs and 97 respectively, assuming classical linear region operation.

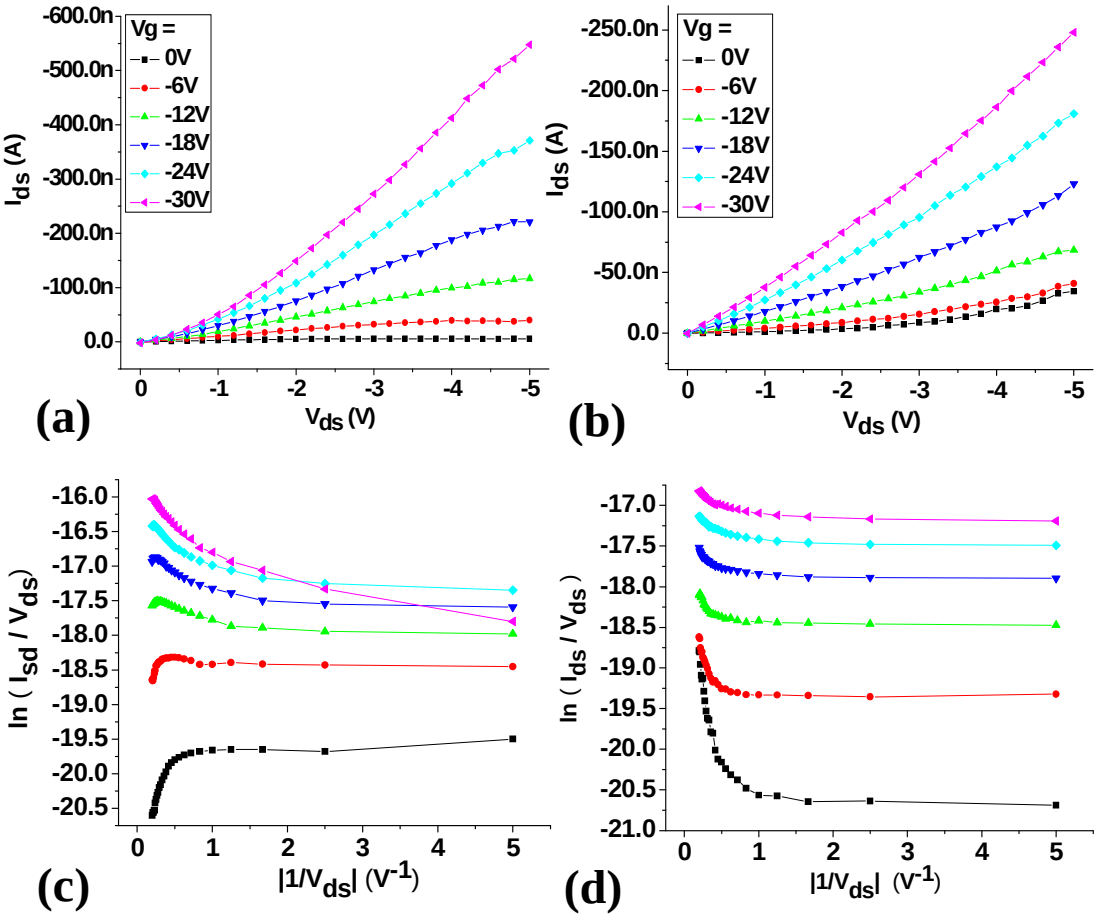


Fig. 3.3 DC characteristics of sub 10nm pentacene FETs. (a) DC I-V measurement of the device in Fig. 2(b), with the side guards biased at the same potential as the drain; (b) DC I-V measurement of a 19 nm channel device with the side guards biased; (c) ln(Ids/Vds) vs. 1/|Vds| plot of the data in Fig. 3(a); (d) ln(Ids/Vds) vs. 1/|Vds| plot of the data in Fig. 3(b). Reprinted with permission from Liang Wang, Daniel Fine, Taeho Jung, Debarshi Basu, Heinz von Seggern, Ananth Dodabalapur, Appl. Phys. Lett., 85 (10), 1772 (2004). Copyright 2004, American Institute of Physics.

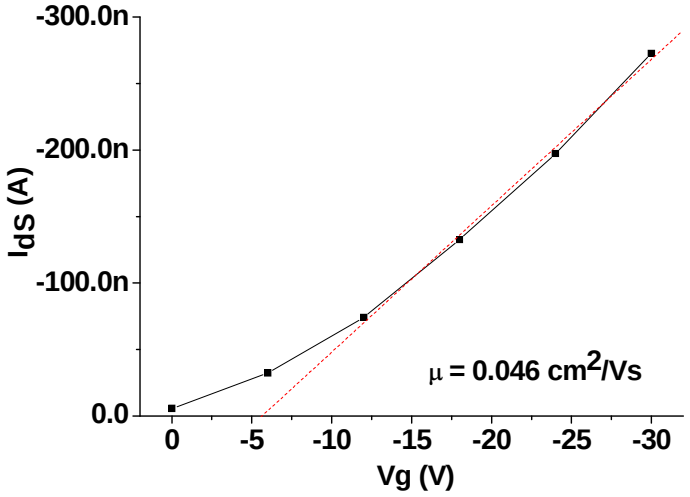


Fig. 3.4 Calculation of mobility of sub 10 nm pentacene FETs. From Fig. 3(a), using the transconductance in the linear region (Vds=-3V), W/L = 2.3 as measured from Fig. 2(b). Reprinted with permission from Liang Wang, Daniel Fine, Taeho Jung, Debarshi Basu, Heinz von Seggern, Ananth Dodabalapur, Appl. Phys. Lett., 85 (10), 1772 (2004). Copyright 2004, American Institute of Physics.

Short channel effects are expected when the channel length is smaller than the gate dielectric thickness [9]. In spite of the 100 nm thickness of the gate dielectric layer, the devices evaluated in this work did not manifest severe short-channel effects. The off-current in Fig. 3.3(a) is saturated beyond V_{ds} = -2.4V, corresponding to a longitudinal field of the order of 10^6 V/cm. Before saturation the conductivity is a constant. Both of these linear and saturation behavior indicate that space-charge-limited-current (SCLC) is not responsible for the transport at zero gate bias. The threshold voltage of this device is -5.6V, derived from the extrapolation in Fig. 3.4. For V_g = -6V where the device is already turned on, the I-V curve is still linear and the saturation sets in at V_{ds} = -4V. The saturation in drain current here at low gate biases could be attributed to velocity

saturation under high longitudinal field (>2MV/cm) in association with few gate-induced charges available in channel at low gate bias. At higher gate biases, the drain current still relates to V_{ds} linearly, and saturation was observed only at high V_{ds} end. At high V_g (-24V and -30V), I_{ds} vs. V_{ds} becomes superlinear but does not follow the square law as the space-charge-limited-current (SCLC) theory predicts. Also SCLC, if applicable, will be preferable to occur at low gate biases instead of high gate biases. The superlinear characteristics at high V_g end are probably due to the possibility that channel resistance becomes small enough at high gate biases so that contact resistance plays a role.

3.4.2 Injection barrier formed by interface dipole

The measured devices can be broadly classified into two groups. One group typically shows the behavior similar to Fig. 3.3(a), with fairly good gate modulation, manifesting linear and saturation behavior upon increasing longitudinal field. The other group exhibits a different kind of characteristic, comprising much less gate modulation and always superlinear behavior of the drain current versus V_{ds}, as shown in Fig. 3.3(b) for a 19 nm channel device. These devices also demonstrated lower currents for the same gate/drain voltages, indicating that the contact is inferior to those in the first group. In these devices there is an additional barrier to be overcome before charges are injected into the channel from the source.

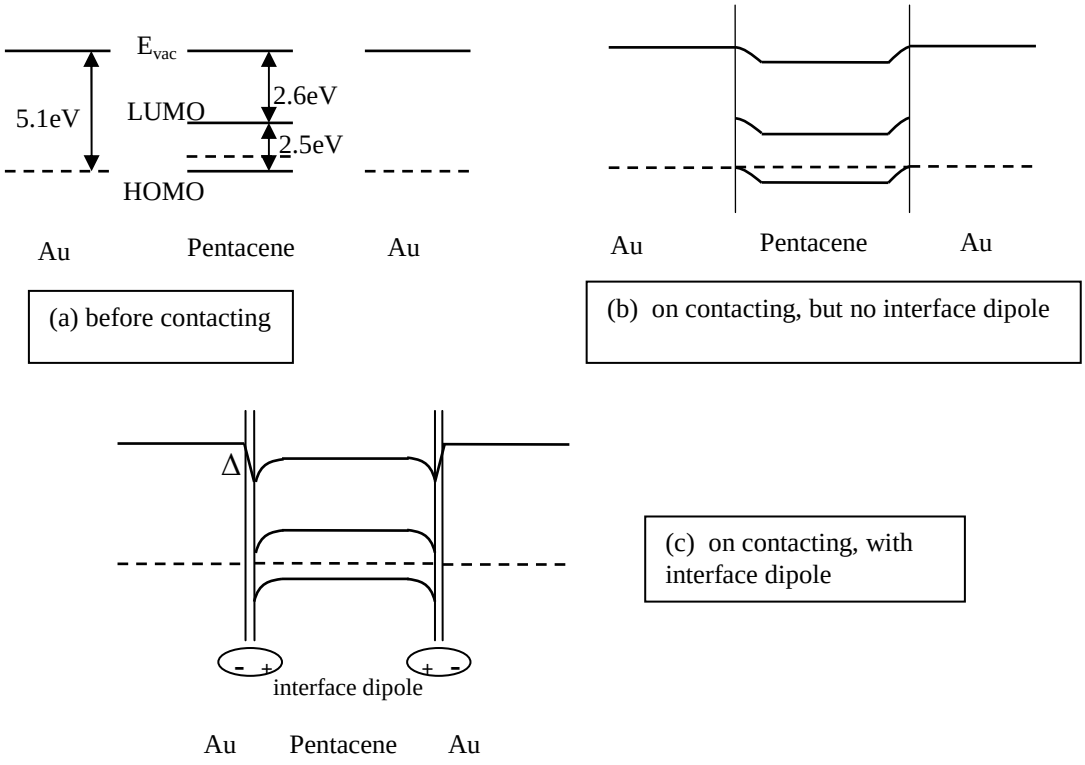


Fig. 3.5 The diagram for the formation of injection barrier at contacts between Au and pentacene, due to the existence of interface dipoles.

The injection barrier at contacts between Au and pentacene is attributed to the existence of interface dipoles. As Fig. 3.5 (a) shows, due to the work function of Au (5.1eV) and electron affinity (2.6eV) / energy gap (2.5eV) of pentacene, the Fermi level of Au meets with the HOMO level of pentacene [10,11]. Therefore on contacting each other, no injection barrier is expected between Au and pentacene, as shown in Fig. 3.5(b). However, due to the accumulation of holes at the pentacene side of the contact, these positive charges and their image charges (negative) at Au side of contact form a type of interface dipole, and the interface dipoles shift the vacuum level at the Au side of the

contact by an amount of Δ [12,13]. This shift on vacuum level changes the band bending situation at the contact and forms a barrier when holes being injected from Au into pentacene, as shown in Fig. 3.5(c).

3.4.3 Fowler-Nordheim tunneling in nanoscale OTFT

The above mentioned injection barrier at metal-organic semiconductor contacts influences the shape of the current-voltage curves. These results are similar to those by Collet ***et al.,*** who reported superlinear currents in α-6T transistors with 30 nm channel length which they attributed to Fowler-Nordheim tunneling through the metal/organic semiconductor interfacial barrier [3]. When the injection barrier is high, the current I_{ds} is not determined by the conduction in the semiconductor channel, but is limited by the injection properties of the contact. The hole injection barrier has been reported to be 0.5~0.85 eV in the presence of surface-dipole contribution (determined from photoemission spectroscopy experiments for large area pentacene thin film deposited atop Au at room temperature) [14-16]. Tunneling through the source/pentacene barrier is preferable only when the longitudinal field is high enough to reduce the width of the barrier. To investigate the relation between the conductivity and the longitudinal field, we rescaled Fig. 3.3(a) and Fig. 3.3(b) into plots of $\ln(I_{ds}/V_{ds})$ vs. $1/|V_{ds}|$ as shown in Fig. 3.3(c) and Fig. 3.3(d) respectively, utilizing the same markers for corresponding V_g values. Both figures show nearly constant conductivities at small V_{ds}. In Fig. 3.3(d), at large V_{ds}, $\ln(I_{ds}/V_{ds})$ vs. $1/|V_{ds}|$ follows the Fowler-Nordheim tunneling model where its

slope decreases with V_g, corresponding to the gate-lowered tunnel barrier. Assuming a triangular potential barrier as a first order approximation, we have [17]

$$\boldsymbol{I_{ds}} \propto \boldsymbol{F} \cdot \boldsymbol{e}^{-\boldsymbol{F}_0/\boldsymbol{F}}, \quad \boldsymbol{F} = |V_{ds}/\boldsymbol{L}|, \quad F_0 = \frac{4\sqrt{2\boldsymbol{m}^*}}{3\boldsymbol{e}\hbar}(\phi_{\boldsymbol{B}})^{3/2} \quad ,$$

where the tunnel barrier height ϕ_B(derived from the slope) is 0.13eV to 0.034eV at V_g = 0V to -30V (taking effective mass m* as 1.7 times free-electron mass [18,19]). Here the pre-factor in the above equation is F instead of F^2, the usual expression for Fowler-Nordheim tunneling, because the tunneling occurs through the pentacene channel which is semiconducting with charges induced from gate control. In usual cases, Fowler-Nordheim tunneling happens through a barrier which is made of insulator, and therefore the charges contributing to current are solely injected from electrodes, which is similar to space-charge limited current (SCLC) and follows the same square law versus source-drain voltage. Here, SCLC is impossible for the devices which exhibit injection limited transport, and even for the devices without injection limitation, the I-V does not follow the SCLC equation. In these devices shown as Fig. 3.3(d), the charges constituting the drain current are induced in the channel by applying gate bias, and thereby the pre-factor of this tunneling current is a linear term. The onset field (V_{ds}/L) of tunneling slightly increases with V_g, probably due to the fact that the ability of the drain bias to make the barrier thinner is screened by the gate-induced charge. On the other hand, in Fig. 3.3(c), at large V_{ds} the slope increases with V_g, which indicates that in this case the transport mechanism is not tunneling through the contact barrier but rather determined by the

intrinsic properties of pentacene. This suggests that in the devices of the first group the metal electrode and organic semiconductor forms good contacts.

3.4.4 The effect of morphology on transport behavior

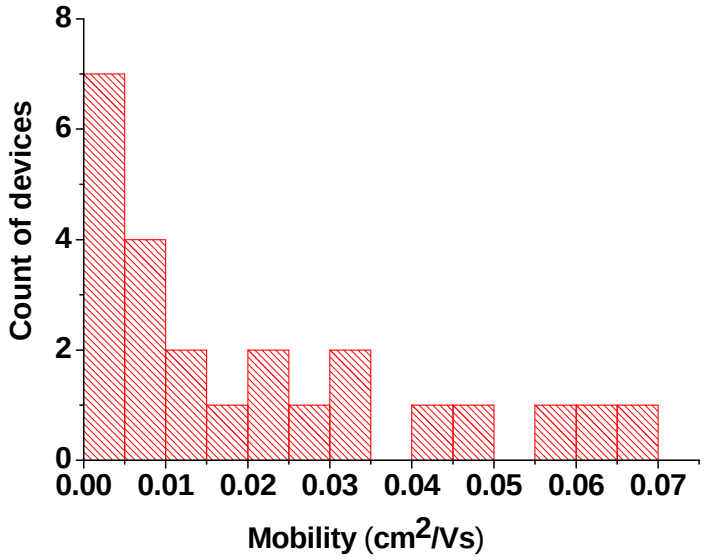


Fig. 3.6 Statistics on the mobility of the measured devices (L=8-35 nm). Reprinted with permission from Liang Wang, Daniel Fine, Taeho Jung, Debarshi Basu, Heinz von Seggern, Ananth Dodabalapur, Appl. Phys. Lett., 85 (10), 1772 (2004). Copyright 2004, American Institute of Physics.

For nanoscale pentacene transistors with non-ideal contacts, the overall transport is limited by the gate-modulated metal/organic semiconductor barrier, as described in Fig. 3.3(b) and Fig. 3.3(d). If the contacts are good, transport is not injection-limited [Fig. 3.3(a) and Fig. 3.3(c)]. In long-channel polycrystalline organic transistors, the overall transport is limited by the transport through grain boundaries rather than that through the bulk of the grains [20,21]. On the other hand, when channel lengths are less than the

average grain size, transport through a single grain may become important; however, the injection properties of the contact (which is possibly affected by the local morphology of the pentacene grain) is the most important factor that influences the electrical response. The grain sizes of the pentacene layer were found to be from 40 nm up to 200 nm, much larger than the channel lengths of the measured devices (from 8 nm to 35 nm). Therefore for these devices the number of grain boundaries inside a channel is significantly reduced, i.e., a channel is composed of only a few grains or has only a single grain boundary inside. For these nanoscale transistors (channel length from 8 nm to 35 nm) with small W/L ratios, field-effect mobility calculated for each of the measured devices was found to have no significant correlation to the channel length. The histogram in Fig. 3.6 gives a distribution of mobility by statistical counts of the number of devices in every mobility interval. Nearly 50% of the measured devices performed with a mobility higher than $0.01 cm^2/Vs$. The wide-range distribution of mobility is attributed to the variability of the semiconductor-electrode interface nature and the local morphology of pentacene coverage on the channel. For such small channel length devices it may be necessary to apply suitable surface treatments such as that proposed by Jackson ***et al*** [22] to improve contact quality.

3.5 Conclusion

In summary, bottom-contact pentacene thin film transistors with channel lengths ranging from sub 10 nm to 40 nm were successfully fabricated and characterized. For devices with small W/L ratios, the direct source-to-drain current was measured at the drain with the side-guards to collect spreading current. The responses of these nanoscale transistors exhibit good gate modulation. The electrical performance of these devices is overwhelmingly influenced by the nature of the metal-organic semiconductor contact and the local morphology of semiconductor coverage on the channel.

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Chapter 4

The transport behavior of nanoscale polymeric field-effect transistors at room temperature

This chapter describes regioregular polythiophene that has been successfully used in large-area FET's on account of its excellent self-assembly properties. We examined the characteristics of regioregular polythiophene FET's with various geometry configurations and channel lengths down to sub 10 nm. The effects of shrinking channel length were investigated for 100nm and 40nm channel length FET's with source and drain patterned by a special design of large W/L ratio. Nanometer scale gaps down to 4nm were formed by electrostatic trapping followed by electromigration processes. The impact of gap geometry was discussed. To suppress the spreading current effects, we employed a pair of guarding electrodes near the two sides of the channel which were kept at the same potential as the drain. The true responses of these nanometer scale FET's exhibit pronounced short-channel effects due to the thick gate insulator used (100 nm) relative to the channel lengths. Our home-developed numerical model simulated the behavior of a 5nm channel FET and reasonable agreement with the experimental data was obtained.

4.1 Introduction

It is of great industrial interest for impact on manufacturing cost to utilize soluble organic semiconductors, both polymers and oligomers, in association with large-area ink-jet printing, stamping, and imprint techniques that could eliminate costly and timely fabrication methods such as lithography and vacuum deposition. Driven mainly by this motivation, conjugated polymers have received great interest from scientific and technological communities [1]. Among conjugated polymers, regioregular poly(3-hexylthiophene) is one of the highest reported as the semiconductor material used in thin film transistors. Due to its self-assembly properties, the field effect mobility can be as high as 0.1 cm^2/Vs, depending on the preparation conditions [2,3,4]. However, the electrical transport properties of regioregular polythiophene have not been studied in transistors on the scale of a few nanometers which is comparable to or less than the conjugation length of the polymer.

Interchain transport in regioregular polythiophene is superior compared to regiorandom polythiophene [2-6]. Regioregular poly(3-alkylthiophene) (>99% head to tail linkage) is found to self-organize and form nanocrystalline domains with sizes of ~15nm [5,6]. We assume that the transport mechanism will be different when the channel length of a transistor shrinks to sub 10 nm, since the grain boundary density becomes lower and the source-drain current would be dominated by the transport within grains (and perhaps across single macromolecules) instead of that through grain boundaries.

Therefore it is interesting to study the characteristics of regioregular poly(3-hexylthiophene) thin film transistors with various channel lengths from 100nm down to sub 5nm.

4.2 The synthesis and characterization of regioregular poly(3-hexylthiophene)

Polythiophene has been employed as one of the candidates for low-cost semiconductor layer of a field-effect transistor since 1980s [7,8]. The conducting/semiconducting properties of polythiophene result from the π electron (in most cases in the form of polaron) on the conjugated single/double bonds along the backbone of the polymer chain. To fulfill the solution-processable requirement for low-cost fabrication, alkyl side chains have been incorporated onto the backbone of polythiophene chain for their solubility in organic solvents. Although these insulating alkyl side chains are not detrimental to the electronic properties of polythiophene, by comparison study it was found that the field-effect mobility of a polythiophene transistor decreases with increasing side chain length from butyl to decyl. High mobility values have been achieved in transistors with thin-film poly(3-hexylthiophene) in a regioregular form.

There are two types of linkage arrangements for the 3-alkyl substituents to be incorporated into the polymer: head to tail (HT), and head to head (HH) or tail to tail (TT) [6], as shown in Fig. 4.1. If poly(3-alkylthiophene) is composed of only one type (>80%

same type of linkage) of arrangement, then it is regioregular; while it is regiorandom if composed of both HH/TT and HT 3-alkylthiophene moieties [5, 6, 9], as Fig. 4.1 shows.

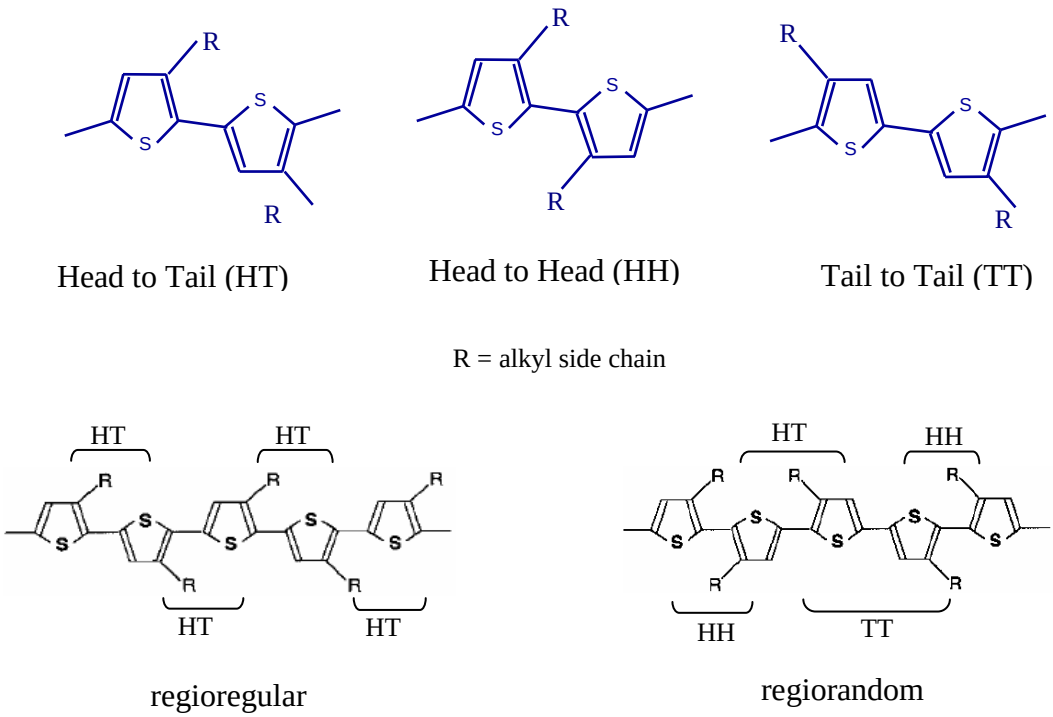

Fig. 4.1 The arrangement of side-chain in polymer with different regioregularity.

The HT regiospecificity (how much percentage of HT linkage in the polymer chain) plays the key role to improve the desired physical properties of the regioregular polymer such as electroconductivity and optical nonlinearity versus the regiorandom polymer, because HH or TT linkage is more sterically hindered and causes defects in the polymer chain [6]. The morphology of regiorandom and regioregular films is quite different and it has strong influence on the mobility of the transistors with these films as the semiconductor layer. Regiorandom film usually exhibits an amorphous morphology.

Spin-coated or solution-cast regioregular film both can self-assemble into well-ordered lamellar structure, while the self-orientation depends on the process conditions. When cast from solution, the regioregular poly(3-hexylthiophene) self-assembles into a layered structure with an edge-on orientation (the assembled polymer chain planes are perpendicular to the substrate), as shown in the left of Fig. 4.2. When spun onto the substrate, highly regioregular film of poly(3-hexylthiophene) (>91% HT linkage) forms lamellae with an edge-on orientation where the π-π stacking direction (the normal direction between planes of assembled thiophene rings) lies in the plane of substrate [4]. On the other hand, the spun film with low regioregularity (81% HT linkage) is composed of lamellae with face-on orientation (the assembled polymer chain planes are parallel to the substrate) which demonstrated a field-effect mobility two orders of magnitude lower than that of edge-on orientation due to the different π-π stacking direction relative to the substrate [4]. Interestingly in contrast, solution-cast 81% regioregular film features an edge-on orientation with an order-of-magnitude higher mobility [4]. In summary, the field-effect mobility of transistors with conjugated polymers as the semiconductor layer depends on not only the degree of order (regioregularity) of the polymer film, but also the orientation of the π-π stacking direction with respect to the substrate.

The complete description of the synthesis of regioregular poly(3-hexylthiophene) is not the emphasis of this work, and it has been well addressed in the literature, known as Rieke method [6]. Here important steps are highlighted from this paper with emphasis on the realization of high regioregularity. The two key steps to fulfill regiospecific

polymerization are: first converting non-polymerizable monomers into polymerizable intermediates by the direct oxidative addition from Rieke zinc with high chemoselectivity; second polymerizing these intermediates with catalyst whose structure can control the regioregularity of the synthesized polymer chain. During the first step, Rieke zinc undergoes direct oxidative addition to 2,5-dibromo-3-alkylthiophe, regioselectively at the C-Br bond of the 5-position (predominant) or the 2-position (minor) and results in the regioisomers as 2-bromo-5-(bromozincio)-3-alkylthiophe (predominant regioisomer) and 5-bromo-2-(bromozincio)-3-alkylthiophene (minor regioisomer). The regioselectivity of the oxidative addition is higher at lower temperature. The polymerizations are then performed in a simple one-pot reaction, i.e., the intermediate regioisomers are treated in situ with catalyst. The turnover number of the catalysts was quite high, namely, only a very small amount (0.2 mol %) of catalyst was needed for high yield of product achieved in these polymerizations. The reactions involve Ni- or Pd-catalyzed cross-coupling polymerizations of regiospecific thiophene organozinc reagents (i.e., these intermediate regioisomers). The regioregularity of the final product can be controlled by the selection of the structure of catalyst. Ni(DPPE)Cl_2 ([1,2-bis-(diphenylphosphino)ethane]nickel(II) chloride) leads to almost complete regioregular poly(3-alkylthiophene) with HT linkages greater than 98.5%, while only 70% linkages of HT versus HH are obtained with Pd(DPPE)Cl_2 with a larger size atom Pd. When switching the ligand of the catalyst from DPPE to a more liable ligand PPh_3 (triphenyl-phosphino), the regioregularity is reduced. Ni(PPh_3)$_4$ and Pd(PPh_3)$_4$ result in 65% and 50% (completely regiorandom) HT linkages respectively. Characterization studies such as electronic absorption, X-ray diffraction,

and crossed polarizing micrograph showed that the regioregular poly(3-alkylthiophene) are self-organized and crystalline whereas the regiorandom ones are amorphous. Also the high regioregularity gives a small bandgap (1.7 eV) which is 0.4 eV lower than that of regiorandom ones (2.1 eV).

Before depositing onto the substrate to form a real field-effect transistor, the synthesized regioregular (>98.5% HT linkages) poly(3-hexylthiophene) can be purified for better performance of the device [10]. The regioregular polymer was dissolved in toluene and precipitated from acetone. This procedure can be repeated multiple cycles and the polymer is then extracted with boiling acetone for elongated time up to 72 hours. In addition to regioregularity of the semiconducting polymer, some extrinsic experimental factors have to be carefully controlled in order to fabricate a polymer trasnsistor with high performance. The field-effect mobility measured in poly(3-hexylthiophene) transistors vary significantly with the choice of the solvent to dissolve the polymer [2]. This is possibly due to the difference in the film forming quality, namely, the polymer thin film might exhibit different degrees of discontinuity dependent on the solubility of the polymer and the nature of the solvent [2]. When THF (Tetrahydrofuran) was employed as the solvent, the polymer precipitates out during the solvent evaporation, resulting in non-uniformity and further phase separation. The deposition methods also have influence on the device performance. Compared to spin-coating, solution-casting takes longer time to evaporate solvent which enables longer time for the self-ordering of the polymer chain and thereby leads to a higher mobility. However solution-casting

usually generates a film thicker than spin-coating, which causes a higher off-current [2]. Several methods have been reported to enhance the on/off ratio, which means to lower the off-current while keeping the mobility nearly unchanged [2, 9]. The polymer film was treated with ammonia by bubbling nitrogen through ammonium hydroxide aqueous solution, which applied the reduction property of ammonia to the residual hole-dopant in polymer. Also thermal treatment (under nitrogen ambient at 100 °C for 5 min) was introduced to lower the off-current by healing the morphological defects in polymer film.

4.3 Experimental

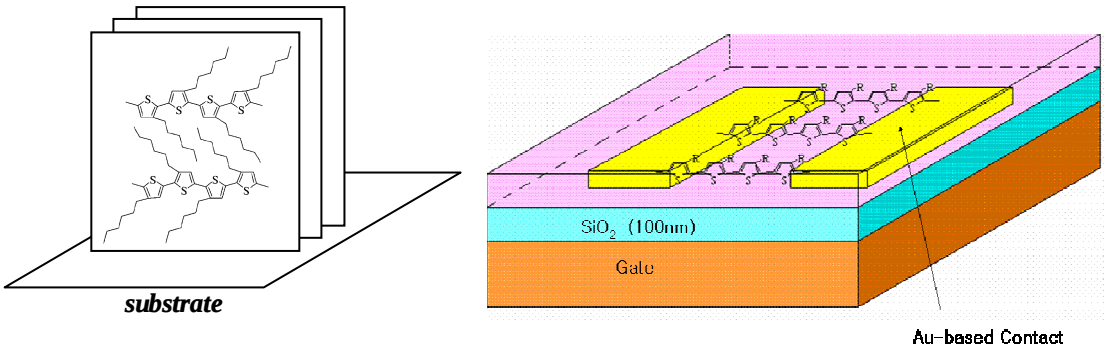

Fig. 4.2 The orientation of regioregualr poly(3-hexylthiphene) planes and the structure of bottom contact thin film transistor. Reprinted with permission from Liang Wang; Taeho Jung; Fine, D.; Khondaker, S.I.; Zhen Yao; von Seggern, H.; Dodabalapur, A., IEEE-NANO 2003, volume 2, Page 577- 580. © 2003 IEEE.

The transistor device structure is shown in Fig. 4.2. Heavily doped n-type silicon substrates with 100nm thermally grown SiO_2 were used as the gate and gate dielectric layers. 3nmTi/50nmAu was deposited by e-beam evaporation onto the wafer after e-beam lithography. With lift-off, electrode patterns of channel lengths down to 40nm were obtained. Sub 10nm channels were made by the bridge & break technique composed of

AC field trapping and DC field electromigration steps [11], starting from the prefabricated patterns with 40-100nm initial separations. Regioregular poly(3-hexylthiophene) (P3HT) was synthesized as described by Bao et al. [2]. The P3HT was dissolved in $CHCl_3$ at a concentration ratio of 0.5mg P3HT to 1ml $CHCl_3$. Solutions were filtered through 0.2μm pore size PTFE membrane syringe filters. Bottom contact devices were completed by solution-casting with a custom ink-jet type deposition apparatus to inject the solution onto electrode patterns and limit the coverage area to within 0.2 mm for low gate leakage. Devices were then immediately transferred into a vacuum oven to evaporate the solvent at 40 ºC for 36-48 hours.

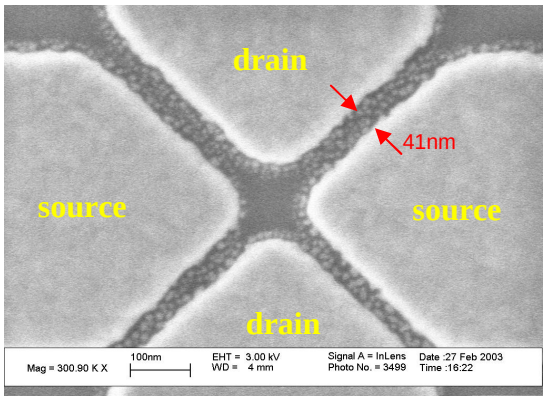

Fig. 4.3 The SEM image of 40nm channel length with extended channel width design (100nm channel has similar image). The left is its source/drain arrangement. Reprinted with permission from Liang Wang; Taeho Jung; Fine, D.; Khondaker, S.I.; Zhen Yao; von Seggern, H.; Dodabalapur, A., IEEE-NANO 2003, volume 2, Page 577- 580. © 2003 IEEE.

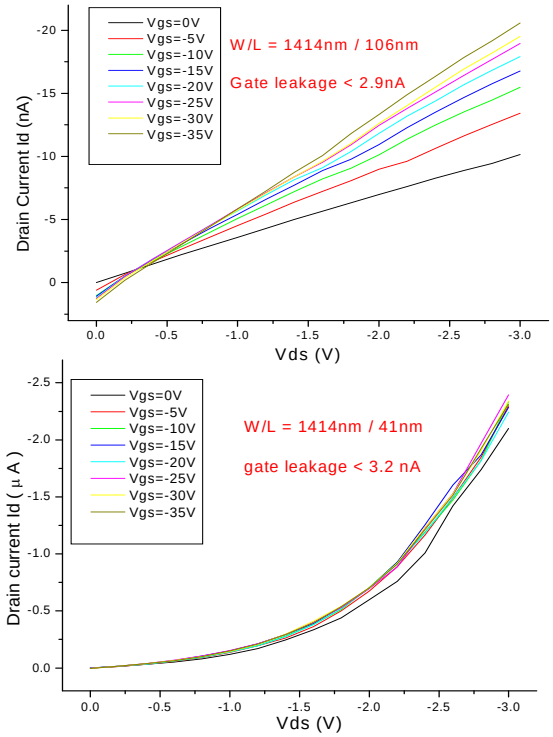

Fig. 4.4 Characteristics of 100nm(upper) and 40nm(lower) channels. Channel width=1.4μm.
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HP 4145B was used to measure the DC electrical characteristics. Transistors with channel lengths of 100nm and 40nm were made with design of tetra-extended channel width as shown in Fig. 4.3. The source-drain current of the 100nm channel still exhibits gate modulation, whereas the 40nm channel demonstrates short-channel like characteristics with reduced gate modulation and higher off-current as shown in Fig. 4.4. Short channel effects are expected when the longitudinal field increases and competes with the transverse (gate) field so that the gradual channel approximation loses validity and the electric field distribution in the channel becomes two-dimensional, which tends to happen in cases where channel length is smaller than the gate dielectric thickness [12]. Since the active semiconductor is not patterned on the scale of the channel length, spreading currents which travel in the large area outside the defined nanoscale channel may become significant. When the channel width/length ratio is not large, the spreading currents must be considered, since they follow pathways significantly longer than the defined channel length. For channel lengths down to 40 nm, we employed a technique of arranging source/drain electrodes to increase the channel width/length ratio so that the spreading current can be ignored, as shown in Fig. 4.3. This method becomes not feasible for channel lengths less than 30 nm since there is an increasing chance for electrodes from this design of extended channel width to be shorted to each other. To suppress spreading current effects, we employed a separated pair of guarding electrodes near the two sides of the channel kept at the same potential as the drain. By this design, the measured drain current was close to the direct source-to-drain current which truly

travels over a nanoscale distance, since the side-guarding electrodes collected the spreading currents and there was no current between the side and drain electrodes due to their equal potentials.

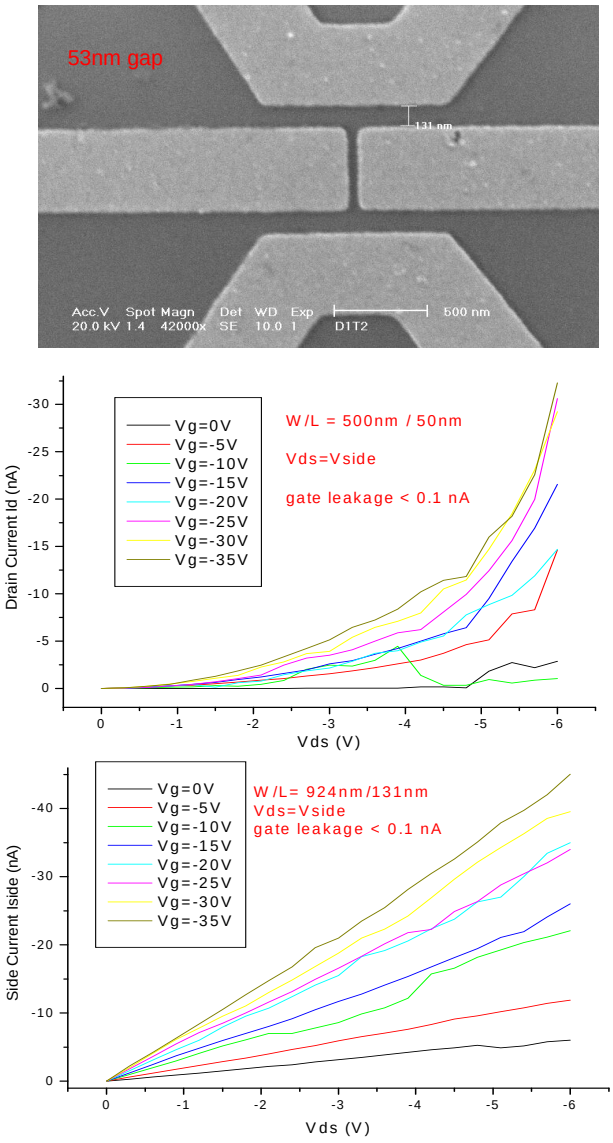

Fig. 4.5 53nm channel SEM image and its drain(upper) and side(lower) currents when kept at same potential.
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Fig. 4.5 shows the SEM image of a 53nm channel with side electrodes and its I-V characteristics. The source-drain current behaves short-channel like while the side current appears less severe. The side current's magnitude is slightly higher than the drain current although its channel width/length ratio is lower (considering that only the source has current flowing to the side electrodes) because of all the fringe current pathways between the source and side electrodes.

4.4 Nanoparticle bridge and break junction to form nanoscale gap

To make a gap of sub 10nm, we applied an AC field between the prefabricated source and drain electrodes to trap Au nanoparticles and form a shorted bridge [11]. Then a slowly ramping DC bias was carefully imposed on the source and drain electrodes, to break the bridge into a sub 5 nm gap via the electromigration in the Au bridge [11, 13]. The entire process was shown as Fig. 4.6, an example to obtain a 3 nm gap. During the AC bridge step, a drop of commercially available Au nanoparticles (5 or 10nm in diameter) solution in water was placed over the channel area, and then an AC (sine or cosine wave) bias of 1MHz (peak to peak < 3V) was applied between source and drain using a wave form generator. The nanoparticles were then attracted to the pre-fabricated gap under the dielectrophoretic force due to the field gradient. Since the dielectrophoretic force exerts nanoparticles to find where the field is the greatest, the aggregation of nanoparticles around the electrode tips can grow continuously until the two growing parts meet and form a bridge.

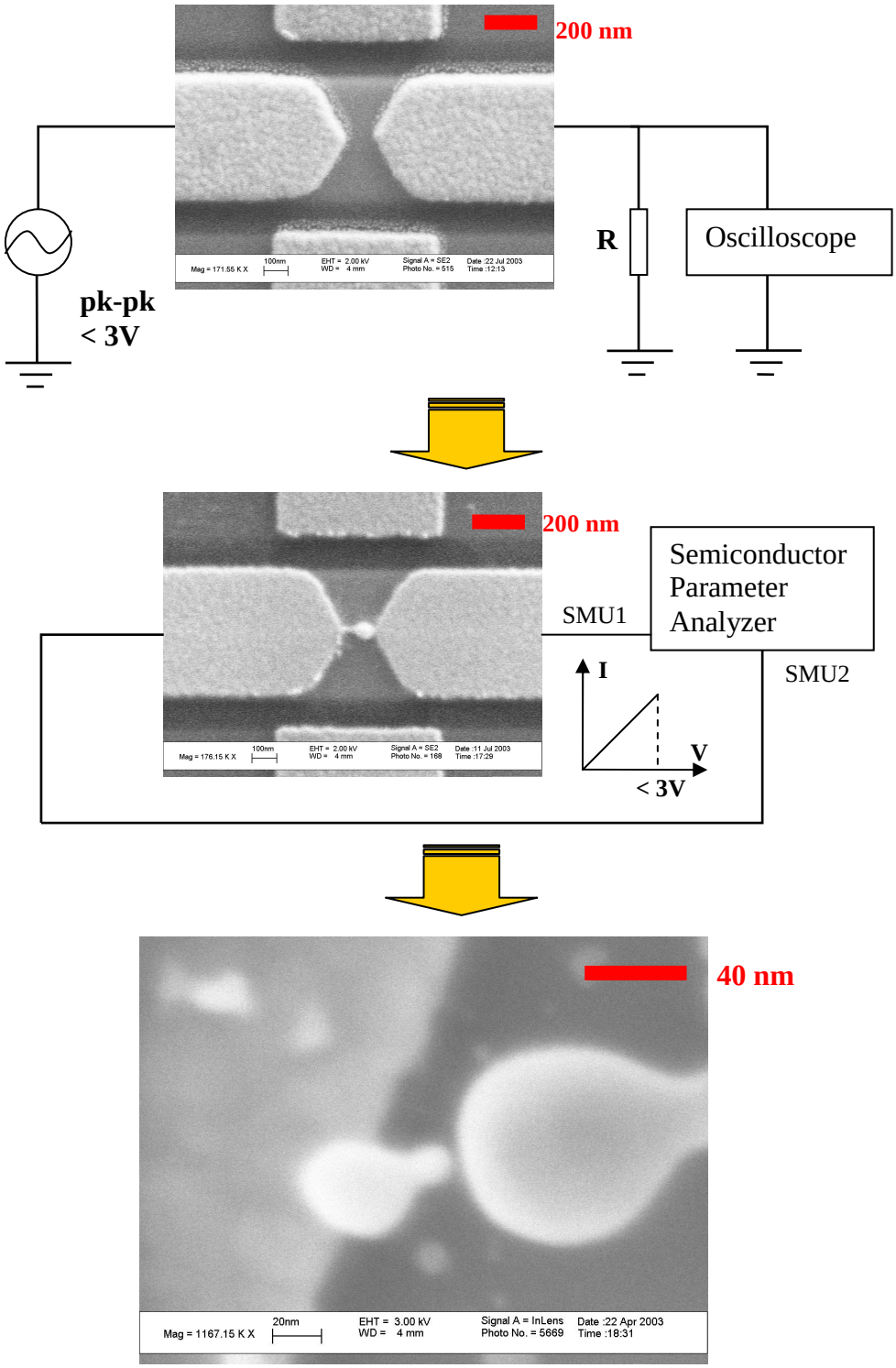

Fig. 4.6 The full process of AC bridge and DC break to form a sub 5 nm gap. Each image was the typical one of that step and was taken by SEM.

The value of the balance resistor R in Fig. 4.6 has to be chosen carefully. The R value should be much smaller than the impedance (~10 M Ω at 1MHz) of the drop before bridge forms so that most of the AC bias was imposed onto the drop to initiate the bridge process. Meanwhile the R value should be much larger than the resistance of the formed bridge (100-300 Ω) so that enough contrast could be observed on the oscilloscope before/after bridge forms, and most importantly, most of AC bias was off the bridge once it forms in order to avoid the damage to the very delicate bridge. Very slowly ramping (~3mV per sec) DC bias was carefully applied to break the bridge into a tiny gap. To obtain a sub 5 nm gap, the DC bias has to be stopped as soon as the breaking signal was observed on the Semiconductor Parameter Analyzer. Also it is possible to obtain smaller gap operating at low temperature (77K). Most bridges were broken below 3 volts. Fig. 4.6 presents the SEM image of one typical gap broken at 1.5 volts. The gap size is about the resolution limit (~3nm) of our field-emission SEM (LEO1530). Most of the gaps we obtained by this way show similar images of less than 5nm in gap size, although some gaps are 8 to 10nm.

Another important point during the operation of DC break junction process is that the substrate has to be directly grounded into the earth or a very large metal (large capacitance), in order to dissipate the static charges. Fig. 4.7 gives an example of the resulting damage to electrodes if this requirement is not fulfilled.

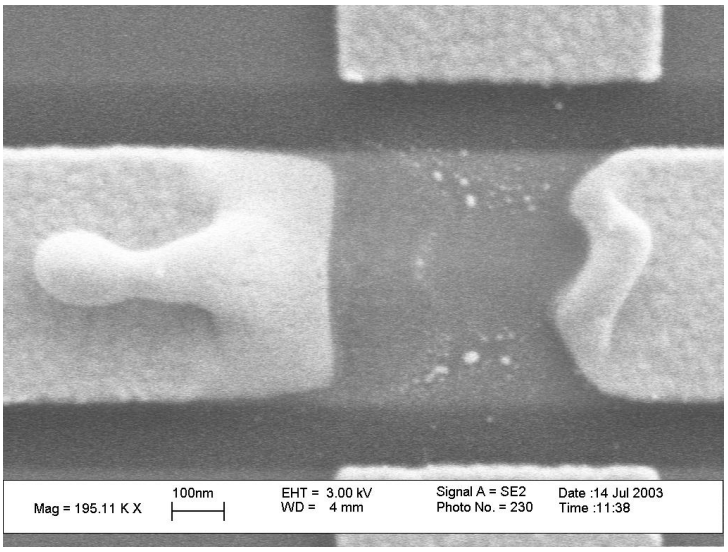

Fig. 4.7 Damage caused by static charges during DC break junction process. This could be avoided by directly grounding the substrate to the earth.

Fig. 4.8(a) shows the characteristic of a device with a 5nm gap that demonstrated a pronounced short channel behavior with side guards functionalized. Similar features were observed for all measured polythiophene devices of sub 10nm channels. It was known for long channel devices that the overall mobility in polycrystalline semiconductors is limited by the transport through grain boundaries rather than that in the higher conductivity grains, and increases with gate voltage. These phenomena are due to the localized trap states distributed in energy gap which originate mainly from grain boundaries [3, 4, 14]. On the other hand, when channel lengths are less than the average grain size of P3HT (15nm) [5, 6], the transport within single grains become dominant compared to that through grain boundaries. Although the side guarding electrodes are designed to be 130nm away from the channel, the current collected from side guards is still short-channel like [Fig. 4.8(b)], possibly because of the extra gold particles of small

curvature attached to the electrode edges during the bridge process which leads to locally intense field. The drain current with side electrodes floating [Fig. 4.8(c)] is also short channel like in spite of the existence of spreading currents. We owe this to the sharp curvature of the two electrode ends forming the sub 10nm gap, which enhances the local electric field there and leads to much higher current density in the gap than elsewhere. Therefore even with the spreading currents, the current directly through the gap still gives a reasonable contribution to the overall source-drain current.

4.5 Transport behavior through nanoscale gap and simulation

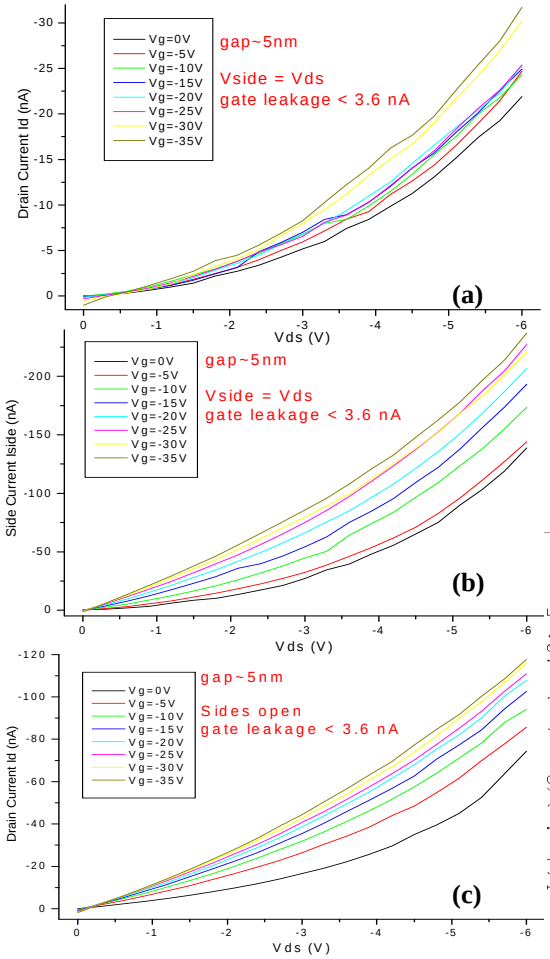

Fig. 4.8 Characteristics of polythiophene transistor with 5nm gap: (a), (b) are the drain, side currents when kept at same potential, (c) is the drain current with side open. Reprinted with permission from Liang Wang; Taeho Jung; Fine, D.; Khondaker, S.I.; Zhen Yao; von Seggern, H.; Dodabalapur, A., IEEE-NANO 2003, volume 2, Page 577- 580. © 2003 IEEE.

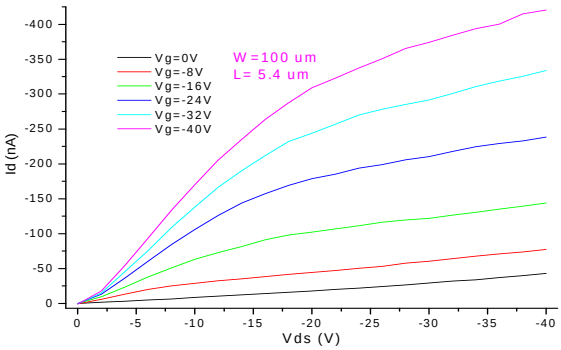

Fig. 4.9 Characteristic of long channel polythiophene transistor. W=100µm, L=5.4µm. Reprinted with permission from Liang Wang; Taeho Jung; Fine, D.; Khondaker, S.I.; Zhen Yao; von Seggern, H.; Dodabalapur, A., IEEE-NANO 2003, volume 2, Page 577- 580. © 2003 IEEE.

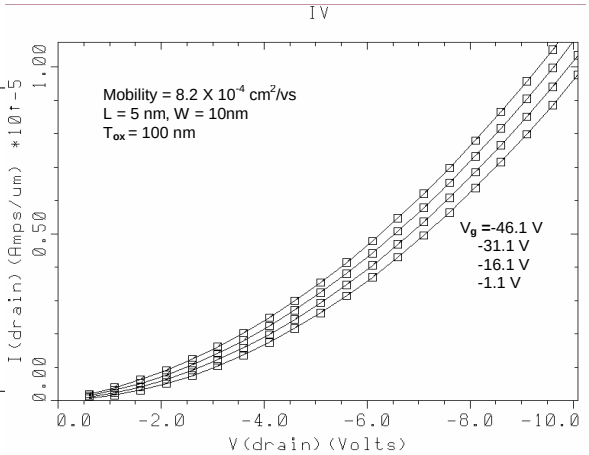

Fig. 4.10 Simulation of 5nm channel polythiophene transistor. Reprinted with permission from Liang Wang; Taeho Jung; Fine, D.; Khondaker, S.I.; Zhen Yao; von Seggern, H.; Dodabalapur, A., IEEE-NANO 2003, volume 2, Page 577- 580. © 2003 IEEE.

Because no saturation regions were approached in characteristic data for all the devices with channel lengths below 100nm, to derive the mobility of the P3HT we prepared the solution in the same batch and followed the same solution-casting procedure

to make bottom contact devices with channels of 100 μm width and 5.4 μm length with the solution. The long channel devices' characteristics featured well defined saturation regions, as Fig. 4.9 indicates, where the mobility was derived to be 0.00082 cm^2/Vs. This mobility's magnitude is one order lower than those reported from others [2, 3, 4]. The P3HT film's conductivity at zero gate voltage is 2.7 X 10^{-4} S/cm, relatively high compared to the data reported [2]. After staying in vacuum to evaporate out the solvent, our devices were measured in the air (in Ref. 2 and 3 the preparation and measurements were implemented in dry N_2 or vacuum). This might cause the high off-current via oxygen doping [15].

To model the sub 10nm channel devices, a commercial MEDICI simulation tool was utilized. A two-dimensional Poisson equation, current continuity and Boltzmann distribution were involved. In this simulation we simply applied the mobility value derived from long channel devices' data and took the diameter of the trapped Au nanoparticles (10nm) as the channel width. Modeling displayed similar behaviors as the experimental data, as shown in Fig. 4.10 and Fig. 4.8(a) for 5nm channel length.

4.6 Conclusion

The field effects of regioregular poly(3-hexylthiophene) were studied by bottom contact thin film transistors with various channel lengths. When channel length shrinks below the gate dielectric thickness, the transverse electric field (controlled by the gate) becomes comparable to the longitudinal one (controlled by the drain), and the gradual channel approximation is no longer valid. Transistors with sub 10nm gaps as channels exhibit pronounced short-channel like behaviors which may arise from space charge limited currents. High k dielectric materials can be used to attain more effective gate control and approach saturation regions in I_D-V_{DS} characteristics, which is ongoing in our lab. We are also engaged to investigate the temperature dependence of the mobility in sub 10nm channel devices to figure out their transport mechanism.

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Chapter 5

Investigation on transport mechanisms in OTFTs by characterization at low temperatures

5.1 Introduction

In the previous chapters, we discussed the characterization of nanoscale organic and polymeric field-effect transistors at room temperature, and proposed several factors which play important roles in the electrical transport of devices with channel lengths from submicron down to sub 10 nm. Although there have been reports of transport characteristics at room temperature for OTFTs with nanoscale channel lengths [1-4], no experimental study has been conducted systematically for these devices with such small dimensions at different temperatures down to 4.2K. On the other hand, there have been many reports on the transport of various organic semiconductor materials in single crystal large channel length transistors at low temperatures with different measurement techniques such as Kelvin probe [5-9]. To investigate the possible transport mechanisms which become dominant when scaling down the device size from micron-scale down to nanoscale, we systematically fabricated thin-film field-effect transistors of a series of channel lengths from 5 μm down to 80 nm, with pentacene as the active organic semiconductor layer in bottom contact structure, and DC I-V characteristics were measured from room temperature down to liquid helium temperatures for these devices.

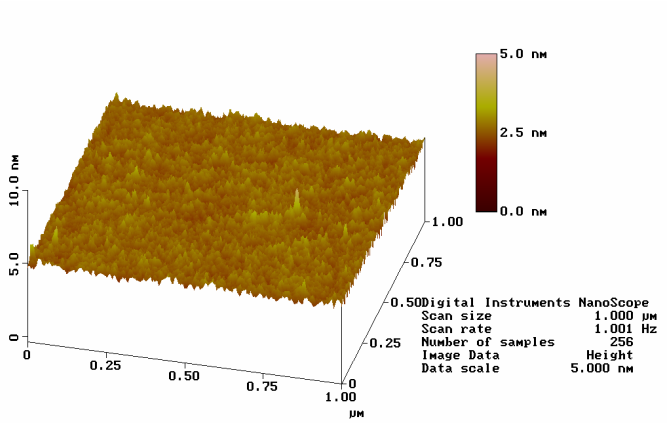
5.2 The fabrication of smooth and flat electrodes for nanoscale channels

Heavily doped n-type silicon wafer serves as the mechanical substrate and the gate. After double Pirhana clean (hydrogen peroxide : sulfuric acid = 1:2 in volume), 1000 Å SiO_2 as a gate dielectric layer was thermally grown from the silicon substrate. Then the source, drain and side-guard electrodes were defined by e-beam lithography on a JEOL JBX-5DII. After developing e-beam resist (ZEP520A), the wafer was immediately transferred into the e-beam evaporator chamber. 20 Å Ti was deposited first as the adhesive layer and 200 Å alloy $Au_{0.6}Pd_{0.4}$ (in weight ratio) followed by 100 Å Au was then deposited.

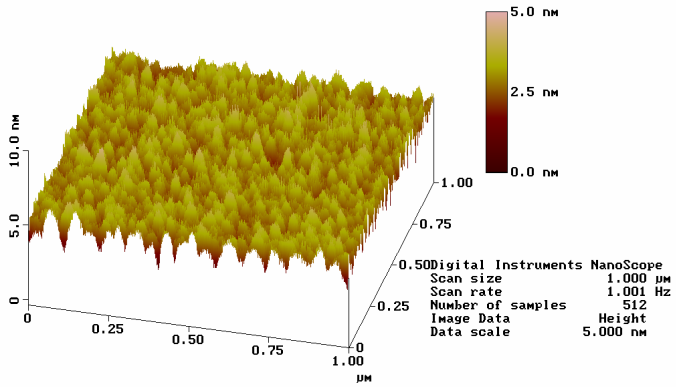
The metal materials and their thicknesses were carefully chosen to optimize the device performance. $Au_{0.6}Pd_{0.4}$ or Au does not adhere well to SiO_2, therefore Ti was used to serve as an adhesive layer. Ti rather than Cr was chosen, because the native oxide of Ti is thinner and denser than that of Cr. Because the adhesive layer material does not make good contacts with the organic semiconductor, if the adhesive layer is thicker than the accumulation layer of organic semiconductor, then carrier injection is limited at the contact which gives rise to high series resistance. If the Ti layer is thinner than the accumulation channel depth, then carriers are injected directly from the high work function metal layer atop Ti layer, which remarkably reduces the series resistance [10]. Therefore Ti layer was chosen to be 1~3 nm thick.

$Au_{0.6}Pd_{0.4}$ and Au was chosen as the electrode material due to their high work functions which allows for easy hole-injection into pentacene layer. The work function of polycrystalline form of Au and Pd is 5.1 eV and 5.16 eV respectively [11]. Vacuum deposited Pd usually forms a polycrystalline layer with very small grain size (< 10nm). This is ideal for nanoscale devices since finer grains of electrode material are necessary to give sharp enough contrast on electrode edges when the channel length is smaller than 1 micron. The alloy of Au and Pd is a good candidate to fulfill this requirement. If the alloy does not contain enough Pd, then the grains of alloy are not fine enough, whereas the alloy's electrical conductivity and chemical resistance will not be good if there is too much Pd in the alloy. $Au_{0.6}Pd_{0.4}$ by weight was chosen as optimal for this purpose [12]. To ensure the chemical resistance of electrodes, a thin layer of Au was deposited on top of $Au_{0.6}Pd_{0.4}$ layer, to take advantage of its chemical inertness. We found that a thin layer (< 200 Å) of Au which is thinner than its average grain size (~30nm), grown at a slow rate (< 0.5 Å/sec in a base vacuum better than 2 μTorr) will still maintain the smooth morphology with very fine grains following the underlying $Au_{0.6}Pd_{0.4}$ layer. All metal layers were deposited at once (no exposure to air) by e-beam evaporation at room temperature. The total thickness of metal electrodes was controlled to be as thin as 350 Å providing a relatively flat topology for ease of pentacene deposition with a good coverage of the pentacene layer on top of nanoscale channels.

(a)



(b)



(c)

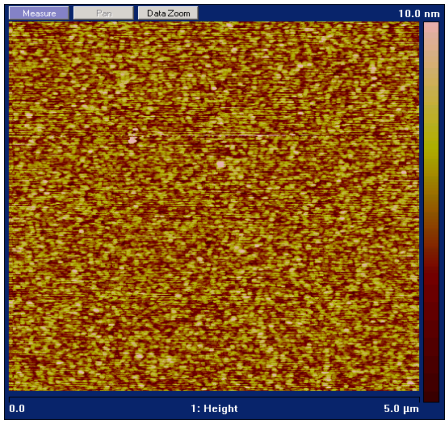


Fig. 5.1 The Atomic Force Microscopy (AFM) images of deposited electrodes. (a) 500Å $Au_{0.6}Pd_{0.4}$ (in weight), (b) 500Å Au, (c) 100Å Au grown (with very slow rate) atop 400Å $Au_{0.6}Pd_{0.4}$, deposited by e-beam evaporator at room temperature in vacuum better than ~2 µTorr.

Fig. 5.1(a) and Fig. 5.1(b) are the Atomic Force Microscopy (AFM) images of the surface of $Au_{0.6}Pd_{0.4}$ and Au in the same scale respectively. It is obvious that the surface of $Au_{0.6}Pd_{0.4}$ is smoother and features finer grains. Fig. 5.1(c) is the AFM image of a thin layer (100 Å) of Au on top of $Au_{0.6}Pd_{0.4}$. The surface of this kind of heterostructure remains smooth and shows fine grains as $Au_{0.6}Pd_{0.4}$, while it is more chemically inert than sole $Au_{0.6}Pd_{0.4}$. A Root-Mean-Square (RMS) roughness of ~ 1 nm was achieved by the above-described fabrication methods.

After the evaporation of metal layers and the lift-off of e-beam resist, very gentle oxygen plasma clean was performed to remove all the resist residues without damaging the electrode surface. The quartz chamber of "March Plasmod" was first vacuumed until < 200 mTorr and then pure oxygen was introduced into the chamber. After the chamber's pressure was steady at 600 mTorr, a RF power of ~25 Watts after optimizing the efficiency was applied onto a total area of ~ 16 $in.^2$ for 40 sec.

5.3 The surface treatment of pentacene layer for low-temperature measurements

To improve the molecular ordering of the pentacene layer on SiO_2 and form a good contact between pentacene and electrodes, the wafer was then immediately coated with HMDS (Hexamethyldisilazane) followed by 4-nitrobenzenethiol. Pure HMDS was spin-coated onto the wafer in air at room temperature at a speed of 4000 rpm for 5sec, followed by a degas step in a 112 °C oven for 3-5 min. The wafer was then soaked in a 5-

10 mM 4-nitrobenzenethiol solution (dissolved in acetonitrile) at room temperature for 2-3 hours and rinsed by acetonitrile and dried with nitrogen.

The silane coupling agent HMDS will form a self-assembled monolayer (SAM) on SiO_2 [13], which will improve the molecular ordering of pentacene layer and reduce the trapped charges at the dielectric-semiconductor interface. This will enhance the field-effect mobility and improve the sub-threshold slope [13-14]. Within the other SAM agent molecule 4-nitrobenzenethiol, its surface active head group (thiol) can anchor to the electrodes through a dative bond between the sulfur atom and the metals such as Au, Pd, Pt and Ag. This treatment can significantly reduce the contact resistance by a factor of 10 at room temperature and even more at low temperatures [14], which is important to the low-temperature measurements described here. Ideally, HMDS only forms a monolayer on SiO_2, without chemisorption onto electrodes, and 4-nitrobenzenethiol only adsorbs onto electrodes. This ideally gives an orthogonal self-assembly without interaction between dielectric treatment and contact treatment [13].

After all the above-mentioned treatments, bottom contact devices were formed by subliming pentacene at room temperature in a base vacuum better than 5×10^{-7} Torr. Pentacene was purchased from Sigma-Aldrich and then purified in a temperature gradient under vacuum. To create a well ordered pentacene layer on SiO_2 surface and to achieve a good contact between pentacene and metal electrodes, the sublimation rate was carefully controlled. A very slow rate (0.3 Å/sec) was applied for the first 100 Å of pentacene layer

to form a well ordered layer with large and flat grains. Since the conduction channel only occurs within the first one or two monolayers of the organic semiconductor [15], it is safe to grow pentacene with a faster rate (1.5 Å/sec) for the rest of the pentacene growth. Faster evaporation rate is preferable to form a good contact because at slow rates the large pentacene grains will leave a void at the region near electrodes while at faster rates the small grains of pentacene will then fill those voids to form a good contact. Usually 300-350 Å is the minimal thickness for the organic semiconductor to uniformly cover the channel region, whereas too thick an organic layer will not increase the gate-induced channel conduction (channel is only one or two monolayer deep) but increase the non-gate-induced bulk conduction and therefore reduce the on/off current ratio of the field-effect transistor. For these reasons the total thickness of pentacene was controlled at 475Å.

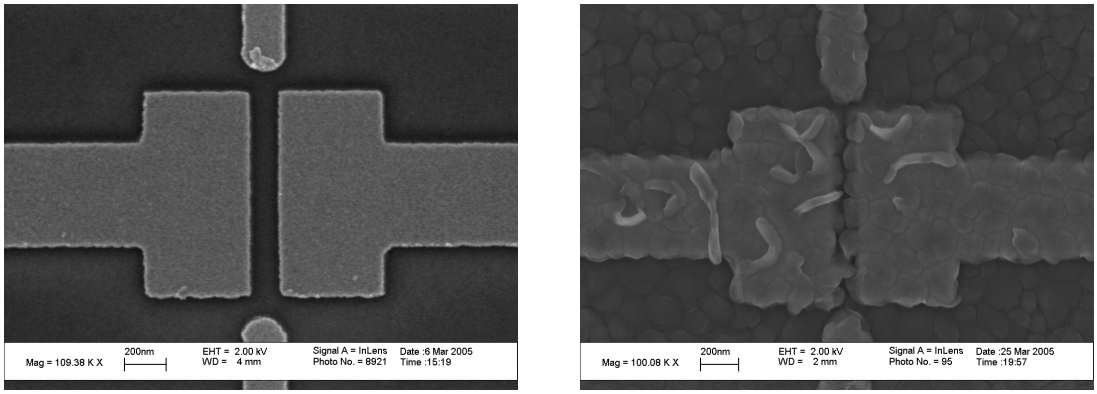


Fig. 5.2 The SEM images of the same channel with L=130 nm and W/L=10, before (as the left) and after (as the right) depositing pentacene layer.

Fig. 5.2 shows the Scanning Electron Microscopy (SEM) images of a 130 nm channel with W/L=10, before and after the deposition of pentacene layer. Since the average grain size of pentacene layer is 100-150 nm at the above-mentioned growth condition, very few grain boundaries are located inside the channel, which makes the devices of this size very interesting for studies on electrical transport and applications as chemical sensors.

5.4 Experimental considerations for low temperature measurements

The doping concentration of n-type silicon substrate has to be carefully chosen in order to validly function as the gate. Below 100K, dopants in silicon are not fully ionized, and the charge carrier concentration changes with temperature linearly on an Arrehnius plot [16]. Based on this fact, the charge carrier concentration will be reduced by 10^3 at 77.2K. Therefore within this scenario, it would be impossible for a silicon substrate to serve as a gate at temperature lower than liquid nitrogen temperature. However it has been known that at low temperatures single crystal silicon or germanium will experience a semiconducting-to-metallic transition upon increasing dopant concentration [17]. Therefore to correctly function as a conducting gate for measurements at low temperatures, the n-type silicon wafer is required to possess a doping concentration higher than 3.74 X 10^{18} /cm^3 for phosphorous dopant or 8.5 X 10^{18} /cm^3 for arsenic dopant [17]. This leads to a requirement on resistivity to be lower than 0.01 ohm·cm for phosphorous or 0.006 ohm·cm for arsenic as dopant [18].

To investigate transport mechanisms in these nanoscale organic thin-film field-effect transistors (TFTs), devices of different channel lengths (from 5μm down to 80 nm) but the same W/L=10 were examined under temperatures from 290K down to 4.4K. A Table Top Manipulated Probe System from Desert Cryogenics was employed for these measurements. Liquid helium was supplied as the heat transfer medium. A Model 331S Temperature Controller from Lake Shore Cryotronics was used to control and display the temperature. An Agilent 4155C Semiconductor Parameter Analyzer was used to supply the assigned voltages to gate, source, drain and side-guard electrodes and measure the currents. In all the DC characteristics, the currents were collected at the drain while the currents from the side-guard electrodes were collected separately. Side guard currents, therefore, do not interfere with the measured drain current. The drain current then represents the charge transport truly through the defined nanoscale channel rather than the large area surrounding the nanoscale channel.

To ensure the good thermal contact between the wafer and the wafer-chuck, a Cryogenic Thermal Contact Grease (Apiezon® N) was applied on the back of the wafer before residing on chuck. This grease offers superior heat transfer properties as compared to indium under high vacuum and at liquid helium temperatures.

In order to cool the temperature down in the absence of moisture to prevent condensation, the chamber was initially pumped down to 1-2 mTorr by a turbo-pump before liquid helium was transferred from a dewar into the enclosed space underneath the

wafer-chuck. The transfer rate of liquid helium should be optimized, because although at high transfer rates it takes relatively less time for the wafer chuck to cool down to 4.4K (less than two hours), the entire system including the wafer chamber and the probe-arm space takes much longer time to approach equilibrium.

After the temperature sensor underneath the wafer reads 4.4K, we usually let the system stay at the medium transfer rate of liquid helium for enough time (~ two hours) until the temperature sensor at the end of the probe-arm (about 10 inches away from the wafer chuck) reads 28.5K. According to the statement from the manufacturer, the system reaches a stable state after the temperature at the end of probe-arm reaches 28.5K. To further ensure that the reading from the temperature controller is really the temperature of the wafer, we usually let the system stay for at least 30 min after temperature reading meets the set-point so that the system can reach a thermal equilibrium before taking data from the wafer. There are two mechanisms simultaneously changing the temperature, namely, the heater underneath the wafer chuck and the transfer rate of liquid helium. High powers generated with the heater will probably degas the thermal grease and disturb the electrical signal in/out of wafer. Therefore we adjust the transfer rate so that the set-point temperature value could be maintained with a 15-30% ratio in the medium range of heater power. Transfer rate below this threshold would only need low range of heater power but due to the lack of enough cooling rate the temperature will deviate to be higher than the set-point before finishing the data retrieval (~30 min for DC characteristics of nine devices at one temperature).

Temperature set-points were chosen so that they are distributed uniformly on an Arrhenius plot, namely, forming uniform intervals in 1/T scale. Totally 18 set-points were chosen between 4.4K and 290K. Therefore one entire measurement takes about 24 hours. It is also possible to choose the temperature set-points as a uniform distribution in logT scale.

5.5 Measurements in air and vacuum:

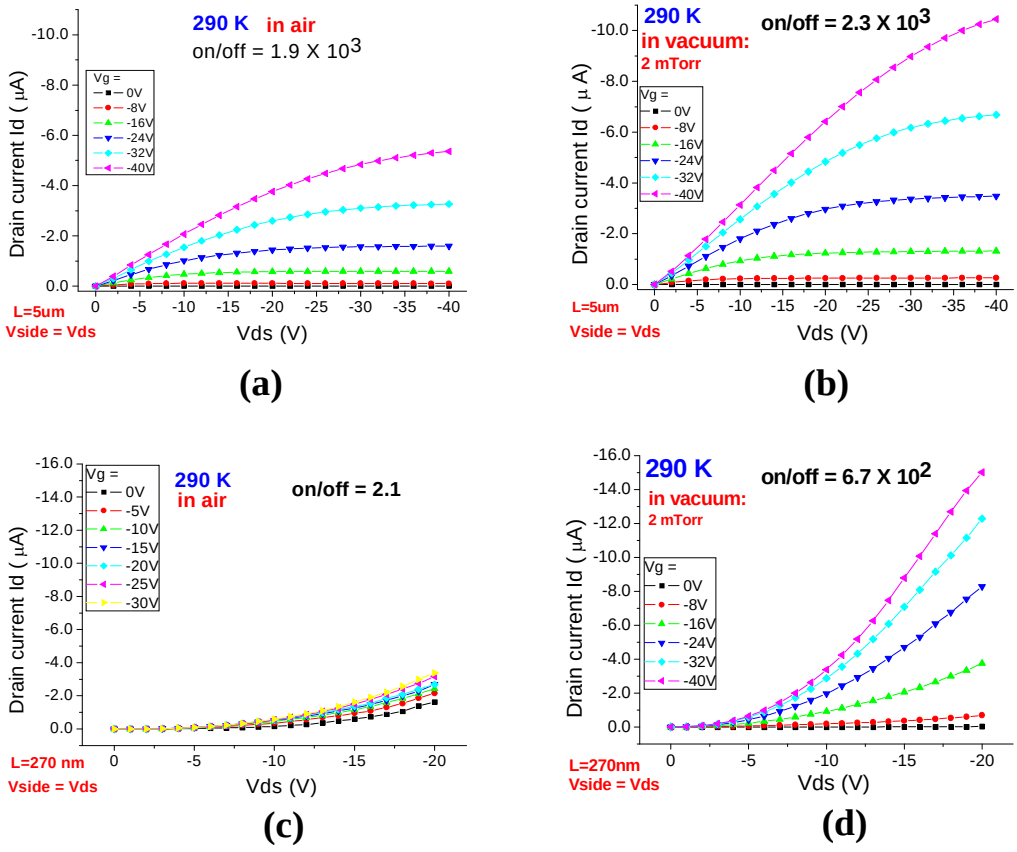


Fig. 5.3 The effect of air ambient on DC characteristics of OTFT. (a) and (b) are the characteristics of a 5 um channel measured in air and vacuum respectively; (c) and (d) are that of a 270 nm channel measured in air and vacuum respectively.

The OTFTs with different channel lengths were examined at room temperature in air and in a vacuum of 2 mTorr to investigate the effect of the presence of air. All the channels have the same W/L (width/length) ratio = 10.

At room temperature, as shown in Fig. 5.3, devices of long channel lengths show saturation region at high V_{ds} end, whereas short channels (L < 500 nm) exhibit super-linear features starting from low V_{ds} end. This is probably due to poor contacts. When the channel length is shorter, the channel resistance is smaller and becomes comparable to the contact resistance so that the Schottky barrier at metal-organic contact limits the current and exhibits a super-linear behavior.

As shown in Fig. 5.3(a) and 5.3(b), compared to the data taken in air, the characteristic of a long channel taken in vacuum shows a higher mobility while on/off ratio remains roughly the same. However, for channels shorter than 500 nm, as shown in Fig. 5.3(c) and 5.3(d), the presence of air as opposed to vacuum greatly reduces the mobility and on/off ratio of the devices.

5.6 The DC characteristics of OTFTs at low temperatures

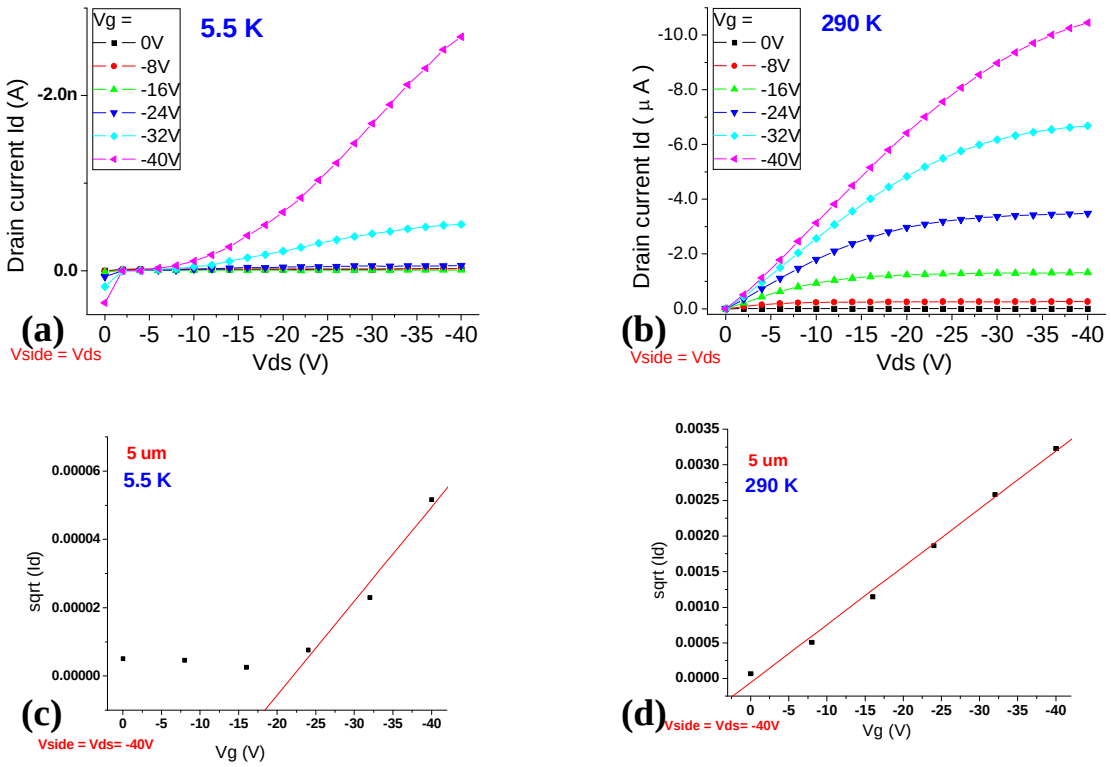


Fig. 5.4(a) and (b): The DC characteristics of a 5 μm channel OTFT at 5.5 K and 290 K respectively. (c) and (d) are the square-root plot of drain current versus gate voltage to show the threshold voltages.

Fig. 5.4 (a) and (b) shows the DC characteristics of a 5 μm channel OTFT at 5.5 K and 290 K respectively. As the temperature decreases to 5.5 K, the Ids-Vds curve becomes super-linear, while the mobility greatly reduces and the threshold voltage shifts by about 20V. This trend with temperature change applies for all the channel lengths (5 μm down to 80 nm).

For OTFTs with channel lengths larger than and including 1 μm, the change in DC characteristics with temperature can be well described by the effective mobility changing with temperature in an Arrhenius plot, as shown in Fig. 5.5(a) and (b) for 5 μm and 2 μm channels respectively.

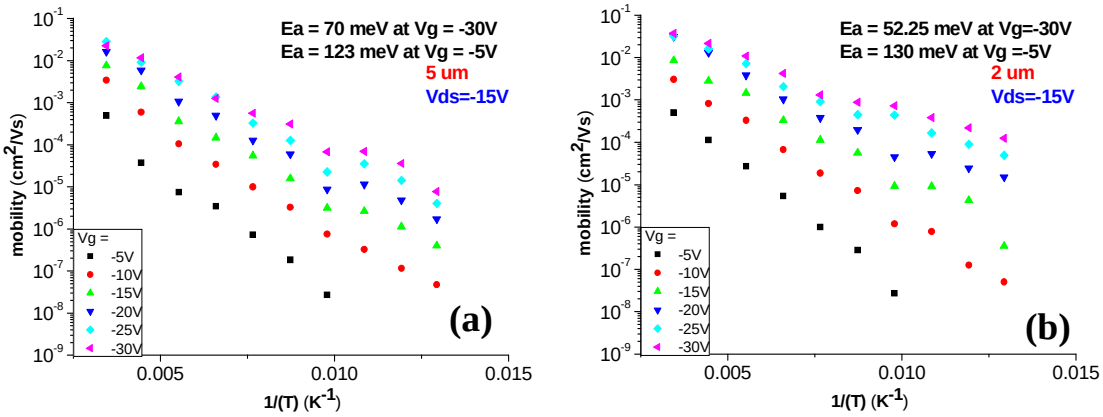


Fig. 5.5 (a) and (b): the Arrhenius plot for 5 μm and 2 μm channel transistors to show the activation energy at different gate bias. The mobility was calculated by the transconductance at a certain Vds (-15V).

According to the Multiple Trapping and Release model [19], the gate-induced charges in an OTFT are composed of two parts: the free (mobile) charges in channel which contribute to the channel conductance; and the trapped charges on trapped levels within the energy gap which do not contribute to the channel conductance. The channel conductivity is a product of free charge density and free charge mobility. There is another way (which is the convention in this area) to view the channel conductivity, namely, it

could also be considered as a product of total gate-induced charge density (including both free charges and trapped charges) and effective mobility. Therefore the value of effective mobility is determined by the ratio of free charge versus the overall summation of free and trapped charges, as the following equation [19-21]:

$$\frac{\mu_{\text{eff}}(T)}{\mu_0} = \frac{N_F}{N_F + N_T} = \frac{1}{1 + \frac{N_T}{N_V}\left(\exp\left(\frac{E_{A,T}}{k_b T}\right)\right)}$$

where the activation energy $E_{A,T}$ is the difference between the Fermi level and the HOMO (for p-type organic semiconductor) level. Usually for room temperature and lower, $E_{A,T}$ is higher than k_bT, so that the effective mobility could be rewritten as [20-21]:

$$\mu_{\text{eff}}(T) \propto \exp\left(\frac{-E_{A,T}}{k_b T}\right)$$

Therefore, in an Arrhenius plot, the slope of effective mobility versus 1/ k_bT yields the activation energy of the multiple trapping and release process. In Fig. 5.5(a) and (b) where an effective mobility was calculated from the transconductance at a certain Vds (-15V), the activation energy ranges from ~50 meV at high gate bias to ~130 meV at low gate bias. The effective mobility in these OTFTs increases with increasing gate bias Vg and becomes saturated at high Vg end, attributed to lifting of the Fermi level by gate bias and filling of the tail states of the density of states (DOS). Also as Fig. 5.5 represents, the gate dependence of effective mobility is stronger at lower temperatures. These phenomena were well-known for disordered organic field-effect transistors where the band tail of localized states has a much wider distribution at grain boundaries than within each grain, due to the increased disorder at grain boundaries [19, 22].

5.7 The scaling behavior of electrical transport in OTFTs

5.7.1 Geometry relation of channel length versus grain sizes

The trap levels within the energy gap of organic semiconductors are the localized states which originate from disorder. For a polycrystalline thin film layer of an organic semiconductor such as pentacene thermally sublimed in vacuum, most of the disorder is located at grain boundaries. Therefore for the OTFTs with channel lengths of 1 μm and longer which is much larger than the average grain size (100-150 nm) of pentacene deposited under the condition above-described, the electrical transport data could be explained by the multiple trapping and release model, as shown in Fig. 5.5. However, when the channel length scales down to 500 nm and smaller which is comparable to the grain sizes of organic semiconductor layer, the average number of grains within one channel reduces as shown in Fig. 5.6 so that the dominant electrical transport mechanism becomes different from large scale devices. For polycrystalline organic thin-film transistors, field-dependent mobility, space-charge limited current and limited injection through Schottky barrier at metal-organic semiconductor contacts play important roles as the device geometry scales down to nanoscale dimensions, and the transport through a single grain body is masked by these effects and could not be observed or distinguished in the experiments conducted to date for this work.

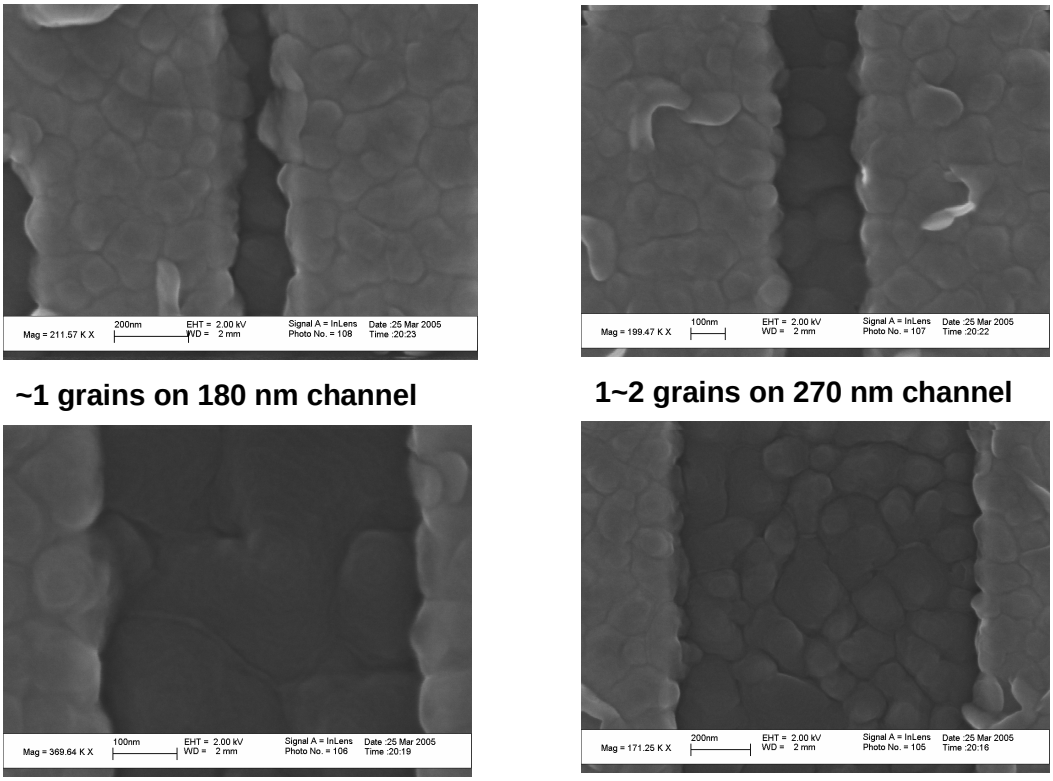


Fig. 5.6 The size of grains of the pentacene layer relative to channel geometry. There are roughly 6-7 grains within a 1μm channel whereas only 1-2 grains within a 270 nm channel.

5.7.2 Field-dependent mobility

When transistor device geometry (channel length L) is scaled down, the longitudinal electrical field along the channel direction becomes stronger, simply because most of the applied source-drain voltage Vds except the contact potential drops is imposed on the channel with a length of L.

For OTFTs with channel lengths of 1 μm or longer, the DC characteristics show normal behavior, i.e., the drain current is in a linear relation to source-drain voltage at low Vds bias while the drain current saturates at high Vds. Therefore we are able to extract the two mobility values for these large scale devices in linear region and saturation region by plotting the transconductance according to the equations [23]

$$\boldsymbol{I_D} = \frac{\boldsymbol{W}}{\boldsymbol{L}} \mu \boldsymbol{C_{ox}} (\boldsymbol{V_G} - \boldsymbol{V_T}) \boldsymbol{V_D} \quad \text{for } V_D << (V_G - V_T) \text{ ----------(I)} \quad \text{and}$$

$$\boldsymbol{I_D} = \frac{1}{2} \frac{\boldsymbol{W}}{\boldsymbol{L}} \mu \boldsymbol{C_{ox}} (\boldsymbol{V_G} - \boldsymbol{V_T})^2 \quad \text{for } V_D > (V_G - V_T) \text{ ----------(II)}$$

respectively.

However for OTFTs with channel lengths of 2 um or shorter, the DC characteristics exhibit super-linear behavior, as shown in Fig. 5.3(d) for a 270 nm and Fig. 5.7(b) for a 80 nm measured at room temperature. In these devices with a wide range of channel lengths, an important transport behavior was observed, namely, the mobility is not a constant any more but it changes with the longitudinal field. Therefore it is impossible to extract just the two values of mobility in the linear region and the saturation region. Instead, we plotted mobility as the function of longitundinal field in full logarithmic scale, as shown in Fig. 5.8.

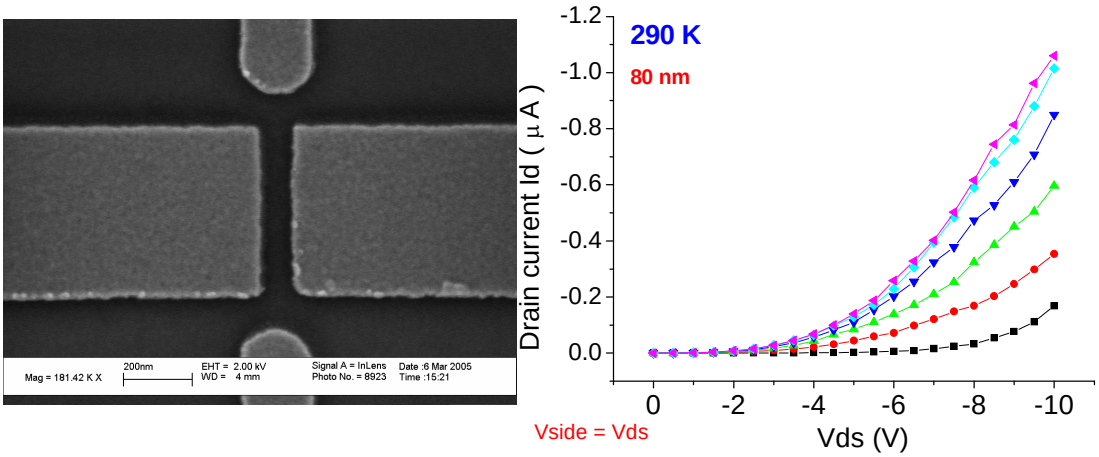


Fig. 5.7 (a) and (b): the SEM image and DC characteristic with super-linear behavior of an 80 nm channel.

To explain the super-linear behavior in nanoscale OTFTs, we propose a field-dependent mobility which superimposes onto the classical picture (as described in equation I and II). In Fig. 5.7(b) it is still possible to extract a mobility value for each Vds by plotting the transconductance according to equation I for linear region operation. By calculating the linear region mobility versus longitudinal field (Vds/L) for different channel lengths over the whole range of temperatures, it was discovered that the mobility of a 2 μm channel or shorter is not a constant any more, instead, it increases with the longitudinal field, as shown in Fig. 5.8 for various channel lengths at four different temperatures.

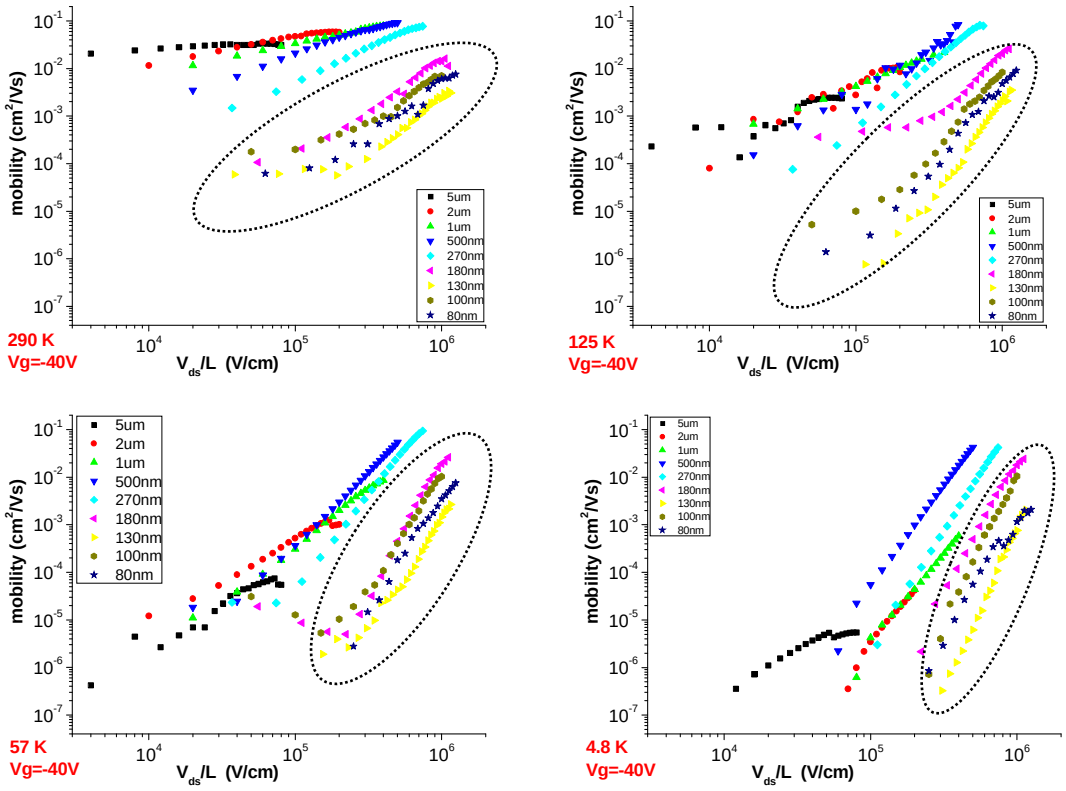


Fig. 5.8 The mobility versus longitudinal field for various channel lengths at different temperatures. The mobility was calculated for each longitudinal filed value via the transconductance in the linear region operation.
All the four figures are exactly on the same scale for the purpose of comparison.

The four parts in Fig. 5.8 representing four different temperatures were plotted exactly on the same scale (full logarithmic scale) for the purpose of comparison. The mobility was calculated for each longitudinal field value via the transconductance in the linear region operation based on equation I. Since in transconductance method, the mobility was calculated via the slope of current versus the gate bias, the threshold voltage V_t in equation I does not take place in the calculation. Therefore although the threshold voltage increases at lower temperature as shown in Fig. 5.4, the calculation performed

here is still valid. In organic semiconductors, the mobility increases with the charge density modulated by gate bias and then saturates at high gate bias end. Here, when we calculated the mobility values in Fig. 5.8, only the top three gate bias (-24V, -32V, -40V) were involved in order to obtain a slope by linear fitting, and we assume at these high gate biases, the mobility almost saturates and does not change with gate bias significantly. At room temperature, the mobility of a 5 μm channel is nearly a constant under longitudinal field over the range below 10^5 V/cm. When the longitudinal field exceeds 10^5 V/cm, for all the channel length under investigation, the mobility becomes dependent on the longitudinal field, namely, increasing with the field. This effect is more apparently indicated in the curves for shorter channels, simply because higher longitudinal fields were built along the shorter channels by the applied source-drain voltages. For the different channel lengths smaller than 200nm, the logarithmic mobility-field curves are roughly parallel to each other. This is attributed to the smaller disorder-induced energy distribution in nanoscale channels and the effect at contacts, and will be discussed later in this chapter. When temperature cools down, the field-dependence of mobility becomes stronger, namely, the slope of the logarithmic mobility-field curve is steeper at lower temperature for the same channel length at the same longitudinal field.

Field-dependent mobility in organics has been studied for decades [24-26]. In disordered organic semiconductor system, charge transport occurs mainly by hopping between adjacent or nearby localized states, and the barrier for hopping is the energy difference between the localized states on these different spatial sites. The physical effect

of longitudinal electrical field is then to bring energy levels of localized states into closer coincidence, and thereby reduce the hopping energy barrier. The imposition of electrical field $\boldsymbol{E}$ onto the two spatial sites with a distance $\boldsymbol{a}$ apart shifts the energy level into closer coincidence by amount of $\boldsymbol{eEa}$ where $\boldsymbol{e}$ is the electron charge, which decreases the hopping activation energy by amount of $\boldsymbol{eEa}$ [25]. Therefore hopping probability and thereby the mobility will demonstrate a dependence on electrical field as $\mu \sim \exp(\boldsymbol{eEa}/kT)$, where k is the Boltzmann's constant and T is the temperature. This expression is known as Poole's law.

One important modification to the initial expression of field-dependent mobility is related to the spatial shape of the hopping barrier. The Poole's law $\mu \sim \exp(\boldsymbol{eEa}/kT)$ is based on the assumption of square well potential where the equilibrium distance $\boldsymbol{a}$ is irrelevant to the electrical field $\boldsymbol{E}$. If a Coulomb potential is assumed so that the hopping barrier under an electrical field is expressed as $U = -\boldsymbol{e}^2/4\pi\varepsilon\boldsymbol{a} - \boldsymbol{eEa}$, then the equilibrium distance between adjacent sites $\boldsymbol{a}$ is determined by the criterion $dU/d\boldsymbol{a} = 0$, which gives a field-dependent equilibrium distance $\boldsymbol{a} = (\boldsymbol{e}/4\pi\varepsilon\boldsymbol{E})^{1/2}$. Therefore the field-dependent mobility for Coulomb potential reads as $\mu \sim \exp(\boldsymbol{E}/E_0)^{1/2}$, which is known as Poole-Frenkel law [24]. Here E_0 is determined by the energy-distribution width and T^2, in case of energy-distributed system as to be discussed below.

If the channel material of an OTFT has some degree of disorder, the energy levels are distributed. The energy required for each hop is no longer a constant. The electrical

field will shift the energy levels in the distribution to which the charge carrier will hop to [25]. Amorphous organic semiconductors usually fall into this category. Bassler et al. [27-28] studied this kind of system with computer simulations and analytical modeling, which led to a similar result as $\mu \sim \exp(\boldsymbol{E}/E_0)^{1/2}$, where E_0 is a constant dependent on the width of energy distribution and proportional to T^2. Monte Carlo simulations for charge carriers hopping between sites that are subject to positional and energetic disorder agree with the above-mentioned field dependence of mobility over a limited field range [29]. This valid range may be wider by considering spatial correlations in the energetic disorder [30-31]. In these theoretical regimes, charge transport occurs by hopping through a manifold of localized states with superimposed energetic or positional disorder. The energy width of the hopping site manifold is comprised of a dipolar component and a Van der Waals component [32]. It was suggested that the Van der Waals component is largely of positional or geometrical origin [33].

Further theoretical modification to the expression of field-dependent mobility included the consideration of hopping directions (forward and backward), the presence of Coulomb traps, asymmetric hopping barrier, and other spatial shapes of hopping barriers [34-36]. There were also some empirical modifications to represent the experimental findings with their physical origin still remaining unclear [37-39]. One of the important empirical parameters introduced is T_0 which represents a field-dependence being temperature independent. Experiments showed that beyond T_0 the field-dependence began to vanish [40]. All these modifications still keep the basic feature as $\mu \sim \exp(\boldsymbol{E})^{1/2}$.

The picture described above can qualitatively explain the transport behavior in Fig. 5.8 for OTFTs with various channel lengths from micron scale to nanoscale at a range of temperatures. As concluded by Poole-Frenkel and Bassler et al., the mobility in organic semiconductors relates to longitudinal field $\boldsymbol{E}$ as $\mu \sim \exp(\boldsymbol{E}/E_0)^{1/2}$, where E_0 is a constant dependent on the width of energy distribution arising from disorder and proportional to T^2. When temperature decreases, E_0 decreases and the field-dependence of mobility becomes stronger, which is consistent with the experimental data of steeper slope at lower temperatures as shown in Fig. 5.8. When the channel length reduces, the number of grain boundaries within a channel becomes less. Because the disorder in organic semiconductor layer is mainly from grain boundaries, for shorter channels the width of energy distribution due to disorder is smaller so that E_0 is smaller. This leads to a steeper slope for a shorter channel at the same temperature in Fig. 5.8, since in the field dependence of mobility $\mu \sim \exp(\boldsymbol{E}/E_0)^{1/2}$, E_0 depends on the width of energy distribution. When the channel length is comparable to the average grain size of pentacene layer, the number of grain boundaries becomes minimal so that this effect reaches its limit. Due to this reason, the channels shorter than 200 nm in Fig. 5.8 exhibit the roughly same slope of mobility-field plots. The contact effects can also contribute to this behavior. Addistionally in Fig. 5.8, with respect to longer channels, the curves of shorter channels (marked by the oval) shift downwards and towards higher longitudinal field. During the fabrication step of pentacene deposition, if the channel length is comparable to the average grain size, grains can lie between the source/drain electrodes because of their

same height, but grains cannot lie on the edges at the ends of channel width due to the severe variation in height there, and thereby grains will not fully cover the channel width. This fact causes the actual W/L ratio to be much smaller than the value we used in Fig. 5.8 to calculate mobility of channels shorter than 200 nm. Therefore the mobility values for these channels were underestimated in Fig. 5.8, which leads to the downward shift. The shift towards higher longitudinal field is due to the injection-limited transport at metal-organic semiconductor contacts and it will be discussed in subsection 5.7.4. In short channel transistors, a significant portion of the applied source-drain voltage will drop at the metal-organic semiconductor contacts. This will lead to an underestimate of mobility and the corresponding shift of longitudinal fileld based on the calculation of linear mobility extracted from the transconductance of I-V curves.

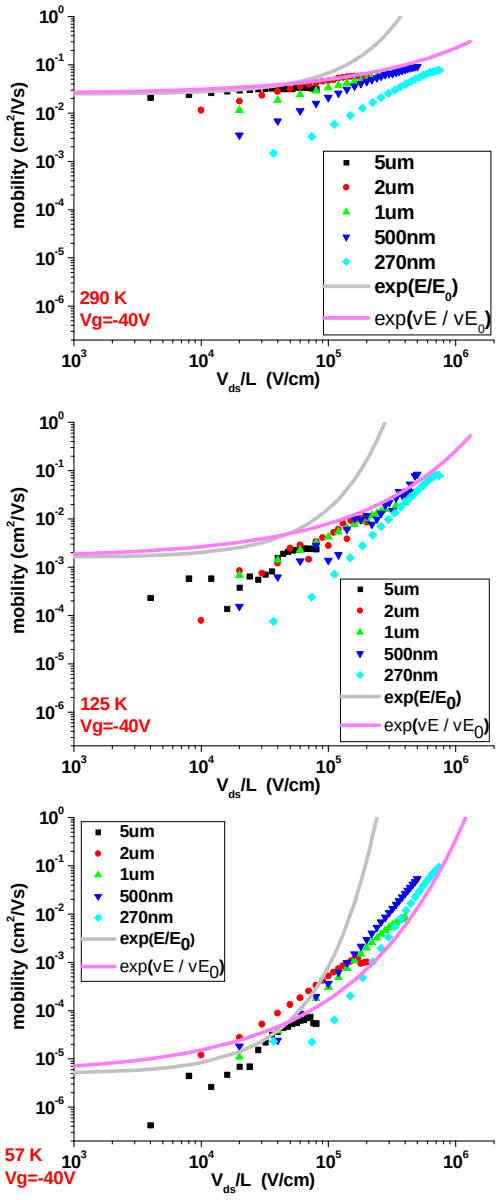


Fig. 5.9 The field-dependent mobility experimental data fitting the Poole-Frenkel model. The mobility was calculated for each longitudinal filed value via the transconductance in the linear region operation.
All the four figures are exactly on the same scale for the purpose of comparison. The best fitting line (in color of magenta) represents the Frenkel model of field-dependent mobility which considers the Coulomb potential in electron's Hamiltonian; while the fitting line (in grey color) deviating the experiments represents the Poole model which considers a much simpler squre-well potential.

Previous reports [41-42] proposed an empirical expression in power law relation of $\mu \sim \mu_0 (E/E_0)^m$ to fit the field-dependent mobility data. However this empirical model does not originate from a clear physical basis. On the other hand, Poole-Frenkel model for field-dependent mobility relies on a simple but effective physical concept (electrical field bringing hopping energy levels into closer coincidence). Therefore we still try to investigate the validity of Poole-Frenkel model as the transport mechanism in nanoscale OTFTs, within the regime where the injection-limited transport is not dominating. Fig. 5.9 shows the experimental data of field-dependent mobility fitting Poole-Frenkel model at different temperatures. In the model considering square well potential in electron's Hamiltonian, the field-dependent mobility reads $\mu = \mu_0 \exp(\boldsymbol{E}/\boldsymbol{E_0})$, where μ_0 is the mobility at zero field (most subject to hopping barrier), $\boldsymbol{E}$ is the longitudinal field, and $\boldsymbol{E_0}$ (which is proportional to kT) is the threshold field value for field-dependence to become severe (below $\boldsymbol{E_0}$, mobility is almost constant). In the model considering Coulomb potential in electron's Hamiltonian, the field-dependent mobility reads $\mu = \mu_0 \exp(\sqrt{\boldsymbol{E}} / \sqrt{\boldsymbol{E_0}})$, where $\sqrt{\boldsymbol{E_0}}$ is proportional to kT. It is important to note that μ_0 in both cases is temperature dependent, reading as $\mu_0 = \mu_{in} \exp(-\Delta / kT)$ where μ_{in} is the intrinsic mobility without suffering hopping barrier and Δ is the hopping barrier height at zero field [25]. In the fitting procedure for both models, μ_0 was taken as the mobility value measured in large scale device (5 um channel) where the channel resistance is much larger than contact resistance and there is no field-dependence of mobility under its operative longitudinal field, and $\boldsymbol{E_0}$ or $\sqrt{\boldsymbol{E_0}}$ in different models were extracted from

experimental data at 290K and then calculated for lower temperatures since $\boldsymbol{E_0}$ or $\sqrt{\boldsymbol{E_0}}$ is proportional to kT in these two models respectively. Interestingly this fitting procedure was able to distinguish the square well potential and the Coulomb potential models with the experimental data. The square well potential model where $\mu = \mu_0 \exp(\boldsymbol{E}/\boldsymbol{E_0})$ possesses too strong field-dependence and deviate far from experimental data. On the other hand, the model which considers Coulomb potential in electron's Hamiltonian fits the experimental data quite well within the regime where injection-limited transport is not dominating. In Fig. 5.9 for each curve of a certain channel length, the "bottom part" of the curve (at relatively lower longitudinal field) is subject to injection-limited transport, while the "top part" of the curve is not dominated by injection-limited transport. Therefore the experimental data neglecting the injection-limitation are the line which draws along the envelope combining all the "top parts" of each curve. As shown in Fig. 5.9, this envelope does fit the field-dependent mobility model assuming Coulomb potential. For temperatures below 45K, the model begins to deviate from the experimental data, probably due to the self-heating effect (Joule heat generated by the imposed voltage and supplied current) which is severe at these low temperatures and makes the actual temperature on devices higher than what is displayed on temperature controller.

Although the experimental data fit the Frenkel model quite well at temperatures higher than 45K, the real situation might not be completely described by the picture of electrical field bringing hopping energy levels into closer coincidence. Other physical

mechanisms for the electrical field to influence the mobility may be functional. The model proposed by Bassler assumes that the disorder in material, results in the Gaussian distribution of charge carrier energy, and the standard deviation of Gaussian distribution increases with the disorder [29, 43-44]. The Gaussian distribution of carrier energy is based on the assumption that the material is amorphous, namely, in a state of completely random disorder. However, this assumption is not likely to be fulfilled in polycrystalline materials such as the vacuum-deposited pentacene layer in the present work. In polycrystalline systems, the disorder region is confined to the grain boundaries, which makes a fully Gaussian Density of States (DOS) less probable than in amorphous materials. It was proposed that in polycrystalline materials the states of charge carriers are mobile states within the crystallites and the trapped states in the disordered grain boundary regions, and the charge transport in this system at time scales longer than 1 μsec is dominated by the thermal excitation from trapped states to mobile states [45]. Based on this concept, the DOS in polycrystalline system was described by bands with tails which extend into the band gap. Inside the band the DOS varies slowly with energy while it decays exponentially into band gap as

$$D_{\exp} = \frac{N_{tot}}{E_b} e^{-E/E_b} \quad \text{---------- (III)},$$

where the N_{tot} is the total concentration of tail states and E_b is the width of the exponential tail [45]. Including this picture for polycrystalline system instead of Bassler model of Gaussian distribution for amorphous system might give a more accurate fitting to Frenkel law for the experimental data of field-dependent mobility in the present work.

Other than the above-mentioned intrinsic mechanism, here, we suggest to consider more extrinsic factors to interpret the experimental data beyond the scope of field-dependent mobility, such as the possibility of space charge limited current and contact limited injection of current, which also become important at nanoscale dimensions.

5.7.3 Justification on the presence of space charge limited current

For OTFTs with nanoscale channel lengths where the longitudinal electrical field is stronger than long channel devices, at zero or low gate bias, the longitudinal field (along the channel direction, imposed by source-drain bias) might become comparable or even stronger than the transverse electrical field (perpendicular to the channel, imposed by gate bias). In this case, the gradual-channel approximation does not hold any more, and the distributions of electrical field, potential and charge density really become two-dimensional. Therefore, the charge density in the channel is not mainly controlled by the gate any more, instead, the charges in the channel are injected from source electrodes and the local charge density at equilibrium is determined by the spatial gradient of the longitudinal field [46]. The current transporting through channel under this condition is the so called space-charge-limited-current (SCLC), and the SCLC has a quadratic dependence versus souce-drain bias V_{ds} as

$$I_d = (9/8)\, \varepsilon\, A \cdot \mu \cdot (V_{ds})^2 / L^3 \quad , \quad \text{---------- (IV)}$$

where ε and A are the permittivity of the organic semiconductor and the injection area of electrodes respectively [46].

In an ideal organic transistors with no or very small injection barrier (< 0.2V) [47], there exist two regimes of charge transport, namely, channel transport (one-dimensional) and SCLC transport (two-dimensional), and the overall current is the combination of these two competing currents. At low Vds bias, the SCLC is small so that the overall transport is mainly determined by the motion of free charge carriers that are present in the organic semiconductor such as the residual doping charges in bulk and the gate-induced charges in channel. The current in this regime follows Ohm's law as

$I_d = A \boldsymbol{e} N \cdot \mu \cdot V_{ds}/L$, ---------- (V)

where N is the free charge density and A is the injection area. The injection area A is different for the residual doping charges at zero Vg (A = W ▪ electrode thickness) and the gate-induced charges at non-zero Vg (A = W ▪ monolayer thickness of organic semiconductor).

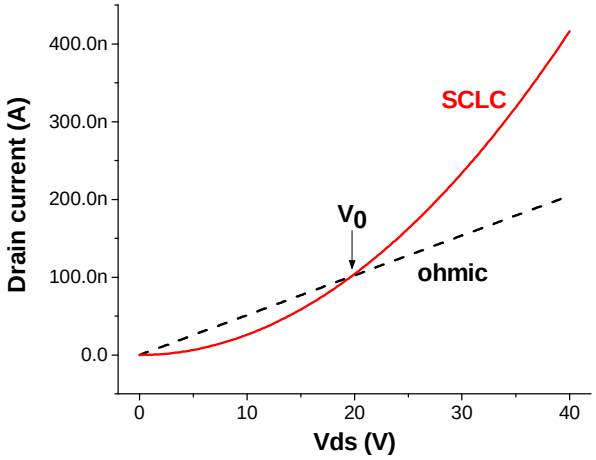


Fig. 5.10 A demonstration that the SCLC outnumbers the ohmic current beyond the transition voltage V_0. Curves were calculated theoretically.

When Vds bias increases, the injected charges begin to outnumber those initially present inside the organic semiconductor. Beyond a certain Vds bias (transition voltage V_0), the current turns from ohmic to SCLC regime [48]. Fig. 5.10 demonstrates a transition from ohmic regime to SCLC regime. For trap-free organic semiconductors, the current in SCLC regime follows a quadratic law as in equation IV. However, for the organic semiconductor layer with disordered regions, an I-V dependence stronger than quadratic law occurs beyond the transition voltage V_0, which is the so called trap-filled limited (TFL) regime [47-48]. If the trap level is located at a single energy, then at the transition voltage V_0, there appears an abrupt increase of the current beyond which the current directly switches to SCLC regime. If the trap levels are distributed exponentially, then the current at $Vds > V_0$ will exhibit a power law relation which reads stronger than quadratic as [47]

$$I \propto \frac{V^{r+1}}{L^{2r+1}}, \quad \text{---------- (VI)}$$

where index r = E_b / kT and E_b is the width of exponential energy distribution of trap states. At high enough fields, the traps are all filled, and the I-V dependence will become quadratic. Therefore the entire bulk transport I-V characteristic can read as ohmic, TFL and trap-free SCLC regimes sequentially with increasing Vds bias.

It was claimed by other groups that there occurs SCLC in nanoscale polymer thin-film transistors fabricated by nanoimprint lithography [49]. However, we think that SCLC is not the dominant transport mechanism for most channel lengths of the OTFTs fabricated in the present work under most operative gate bias. Fig. 5.11 calculates the transition field $F_0 = V_0 / L$ beyond which the two-dimensional bulk transport current (SCLC) will outnumber the one-dimensional channel transport current (by motion of gate-induced charges), based on equation IV and I. The injection area A for SCLC is equal to W▪ t where t is the electrode thickness (32 nm), and the geometry ratio W/L is the same (=10) for all the devices. From Fig. 5.11, it is apparent that the SCLC is not the dominant transport mechanism for channels longer than 100 nm under gate bias higher than 10V across 1000 Å SiO_2, considering that the applied longitudinal field is lower than 2 MV/cm.

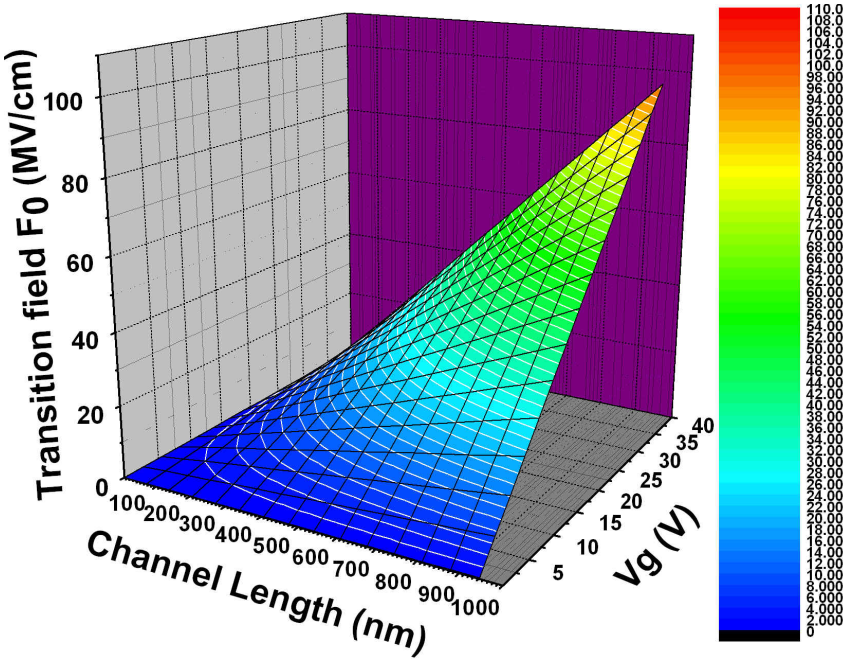


Fig. 5.11 The calculation of transition field $F_0 = V_0/L$ beyond which the quadratic space charge limited current will be higher than the linear channel current by motion of gate-induced charges. The results hold for every temperature.

It is important to note that the result shown in Fig. 5.11 is valid for every temperature since the temperature-dependent mobility appears equivalently as a pre-factor in equation IV and I. Also, it is not trivial to note that the transition field will become higher by considering trap-filled limited (TFL) current instead of SCLC, simply because the TFL current is at a lower value than the SCLC under the same geometry and bias due to less charges involved in transport (injected charges are partially trapped onto localized states) within TFL regime. Therefore, for the devices with channel lengths longer than 100 nm under gate bias higher than 10V, TFL current does not dominate the transport through the channel.

Another possible argument is that the super-linear behavior in OTFTs of small channel lengths as shown in Fig. 5.7 and 5.8 is due to the SCLC but with limitation by the injection barrier at non-ideal metal-organic semiconductor contacts. As we can see in subsection 5.7.4, there is a contact injection barrier in these devices. However such a contact injection of low efficiency can not sustain the high current required in SCLC regime.

In conclusion, the super-linear behavior in OTFTs of small channel lengths as shown in Fig. 5.7 and 5.8 is not mainly due to the SCLC or TFT current. Instead, the super-linear behavior can be attributed to the combination of field-dependent mobility and contact-injection limited transport.

5.7.4 Injection limited transport regime and field-dependent mobility regime

The quadratic SCLC and the linear current by motion of residual doped charges at zero gate bias could be used as a criterion for the judgement on contact-injection limited transport. If a measured current is inferior to the combination of calculated SCLC and bulk current by motion of residual doped charges as reference line, then the transport in this device is subject to the limitation by contact injection-barrier. Furthermore, because SCLC is not the dominant transport mechanism for channels longer than 100 nm under most operative gate biases, for each of the non-zero gate biases, by drawing the

corresponding calculated field-effect channel current as the reference line next to the measured data, we could investigate the issues of contact-injection limited transport and field-dependent mobility behavior by a more conceptual way. The mobility values used to calculate the reference line, are extracted from the experimental data taken at the corresponding temperature for the long channel (>= 5um) devices where the channel resistance is much larger than contact resistance and there is no field-dependent mobility under its operative longitudinal field. The following paragraphs under this subsection are dedicated to the application of these analytical methods to explain the super-linear behavior of nanoscale OTFTs at different temperatures.

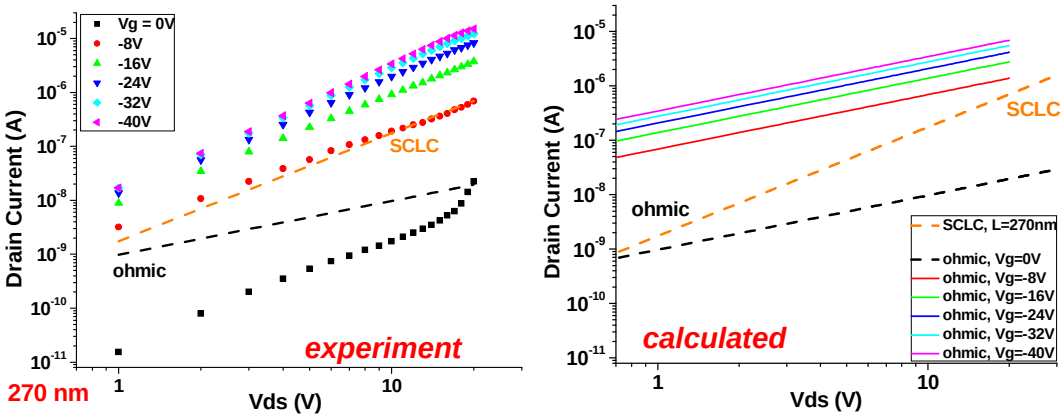


Fig. 5.12 The DC I-V characteristic of a 270 nm channel on logarithmic scale under different gate bias. The plot on the left shows the experimental data measured at room temperature; the plot on the right shows the calculated results. The experimental and calculated plots are exactly on the same scale.

Fig. 5.12 is an example of the methodology above-mentioned, where the DC I-V characteristic of a 270 nm channel under different gate bias is shown on logarithmic scale. The left is the experimental data measured at room temperature and the right is the calculated results. The experimental and calculated plots are exactly on the same scale for comparison. The SCLC and bulk ohmic reference lines were calculated based on equation IV and V, and the ohmic channel transport currents at different gate biases were calculated based on equation I. The residual doping of the organic semiconductor was estimated as 1.9 X $10^{15}/cm^3$, as measured in the pentacene layer fabricated under the same conditions [50]. The mobility value for the calculation in Fig. 5.12 was taken as the mobility measured in large devices shown in Fig. 5.5.

As shown in the right part of Fig. 5.12, transition voltage V_0 of this device is quite small, while the SCLC is below the ohmic channel transport currents at gate voltage higher than 5V. Therefore the device at Vg=0V is in SCLC regime, whereas at non-zero gate bias the SCLC is not the main transport mechanism, which is also obvious from the fact that in Fig. 5.12(left) the calculated SCLC is below all the measured currents under non-zero gate bias. In conclusion, the dominating transport mechanism at non-zero gate bias is the field-effect channel transport. Consequently, in order to discuss the injection-limited transport and field-dependent mobility behavior in the experimental data at zero and non-zero gate bias, we can utilize the calculated SCLC line and the calculated ohmic lines at non-zero Vg respectively as the references. It is non-trivial to note that this conclusion is also valid at temperatures other than 290K, since the temperature-dependent

mobility appears equivalently as a pre-factor in all the equations and thereby has no effects on the relation between different regimes of transport. At Vg=0V, since the SCLC is beyond the experimental off-current, the device is subject to injection limited transport. When gate bias increases, at low Vds the transport is limited by the injection barrier since at these low fields the measured currents are lower than the calculated ohmic channel current. At high Vds the measured current meets and even exceeds the calculated one, which indicates that at these high longitudinal fields the transport is not limited by injection any more. At a higher gate bias, within a wider range of Vds the transport is not limited by injection.

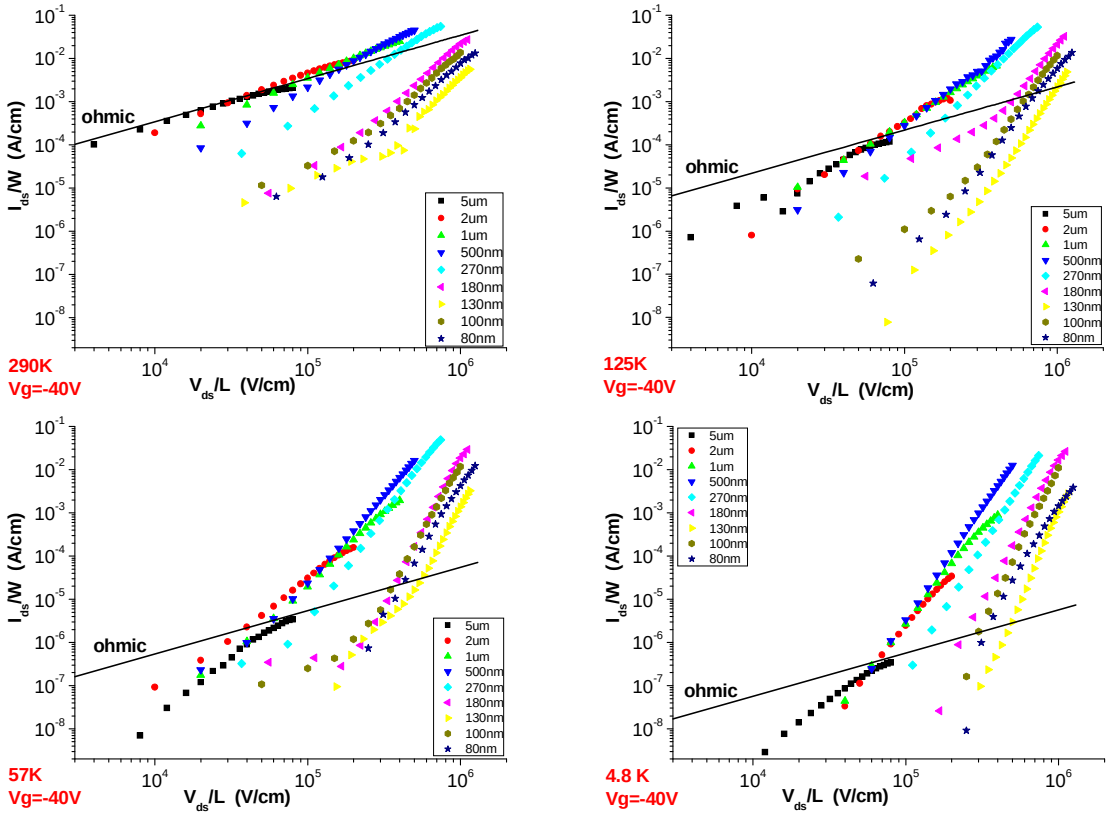


Fig. 5.13 The current density versus longitudinal field plots for various channel lengths at four different temperatures. The solid lines in these plots are the ohmic channel transport currents calculated based on the mobility extracted from long channel (5um) devices. These lines serve as the references to investigate the issues of contact-injection limited transport and field-dependent mobility. All the four figures are exactly on the same scale for the purpose of comparison.

Fig. 5.13 shows the current density versus longitudinal field plots for various channel lengths at four different temperatures under a certain high gate bias (-40V). The solid lines in these plots are the ohmic channel transport currents at Vg=-40V calculated through equation I based on the mobility values extracted from the measurement data taken at the corresponding temperature on the long channel (5um) devices where field-

dependence of mobility is not significant at its operative longidinal field and the channel resistance is much larger than contact resistance. One reason to present the data on current density-field plot is that for all the devices with different channel lengths, their calculated ohmic channel transport follows the same single curve on current density-field plot. As discussed above, at medium and high gate biases, the transport is not dominated by SCLC, therefore these lines of calculated ohmic channel currents are the correct references to investigate the issues of contact-injection limited transport and field-dependent mobility. All the current-field curves in full logarithmic scale measured for different channel lengths shift downward when temperature decreases, simply due to the thermally activated zero-field mobility in channel transport (without considering injection limitation at contacts), represented by the downward shifts of the ohmic reference lines with lowering temperature.

At room temperature, only channels longer than 200 nm exhibit transport exceeding the injection limit at high longitudinal fields, while those channels shorter than 200 nm are subject to the injection-limited transport throughout the entire range of applied longitudinal field (up to 1.25 MV/cm). However, when lowering the temperature to 125K, the situation of injection limited transport is not as severe as that at room temperature, and all channel lengths show transport without injection limiting, smaller channel showing non-limiting transport at higher fields. At high longitudinal fields, the transport is not injection limited, and the current changes with field by a superlinear relation which is steeper than the ohmic (linear) law. High longitudinal field reduces the

contact resistance by thinning the injection-barrier and lowering its height so that the limitation of charge injection reduces. Taking Fig. 5.13 as an example, for the investigation of transport behavior of OTFTs, in current density-field plots for each channel length we name the regimes below and beyond the ohmic channel transport reference line as the injection-limited transport regime and the field-dependent mobility regime respectively. The current-field dependence becomes even stronger at lower temperatures. This fact is the typical features of field-dependent mobility where the field-dependence in Frenkel law increases when temperature decreases. In addition, the field-dependent mobility regime (beyond the injection-limited transport regime) falls in a wider range of longitudinal field at a lower temperature for the same channel length, which is associated with the fact that field-dependence of mobility increases when temperature decreases.

From Fig. 5.13 we can observe that the transport in OTFTs becomes less contact injection-limited at lower temperatures, which is counterintuitive at the first glance. Similar results were reported [55] in the electrostatic potential study by non-contact potentiometry method in scanning Kelvin probe mode. It was suggested that given the stronger temperature-dependence of mobility, the temperature-dependence of contact resistance is then relatively weaker than that of channel resistance, and therefore at lower temperatures the channel resistance becomes a larger portion of the overall resistance as opposed to the contact resistance.

Based on equation I, the plot of current density versus longitudinal field for different channel lengths should overlap onto a single curve. However in Fig. 5.13 it is observed that the curves of shorter channels shift towards higher fields. This is attributed to the existence of extra potential drop on contacts. The applied source-drain voltage Vds will not completely impose onto the gate-modulated channel, instead, part of the Vds drops across the contact region at the source or drain, cited as $V_{contact}$. The actual longitudinal field imposed onto the gate-modulated channel is then equal to (Vds - $V_{contact}$)/L. Therefore, the measured current-field curve for each channel length L will shift towards higher longitudinal field by an amount of $V_{contact}$/L, with respect to the ideal-contact case. Because $V_{contact}$ is not directly dependent on L, the current-field curve for the shorter channel will shift more than that of the longer channel and consequently in the fully logarithmic current-field plot, the shorter channel curve shifts towards high longitudinal field with respect to the longer channel curve.

In conclusion, for the channel longer than 100nm at medium and high gate biases, SCLC is not comparable to the channel current. High longitudinal field will reduce the width and height of the injection barrier at contacts so that the transport is not injection limited, and within this regime the measured current is higher than the calculated ohmic channel current and depends on source-drain voltage in a superlinear way, which can only be explained by the field-dependent mobility behavior. In the regime of high gate bias and high longitudinal field, the dominating transport mechanism is gate-modulated channel transport with field-dependent mobility.

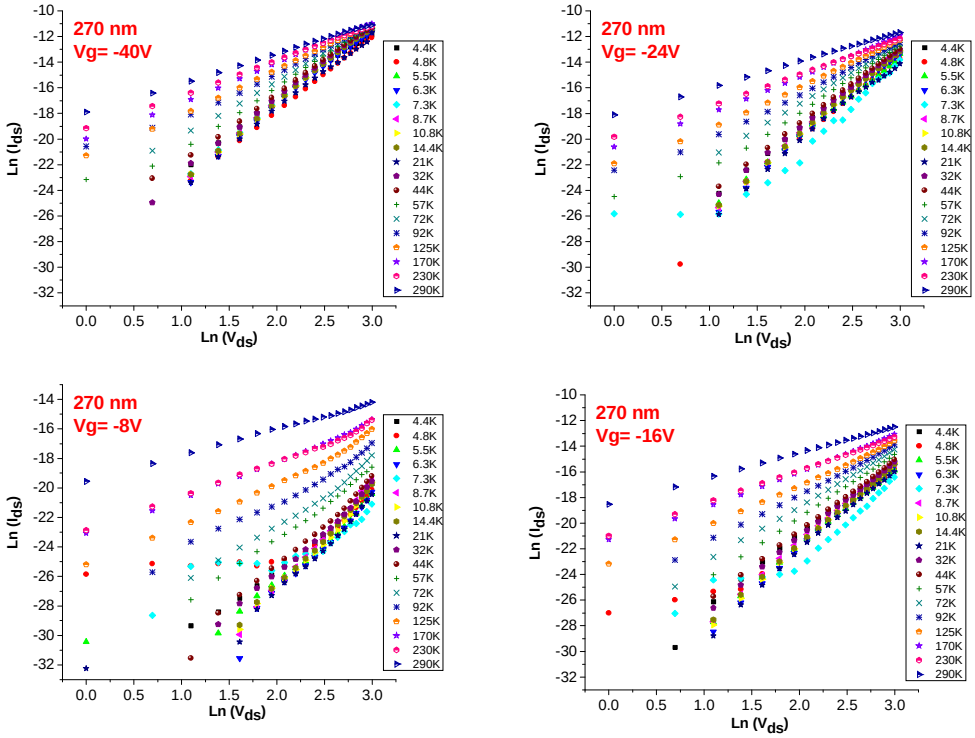


Fig. 5.14 The measured I-V curves in logarithmic scale at a certain gate bias for the entire range of temperatures from 290K down to 4.4K. The four plots show the results at four gate biases. All the four plots are on the exactly same scale for comparison.

There are interesting features to be discussed for the transport behavior of the nanoscale OTFTs measured at different temperatures. As seen from Fig. 5.14, the DC LnI-LnV characteristic of an OTFT with 270 nm channel length shows evident field-dependent mobility behavior. For the same channel length, the LnI-LnV curve at a lower temperature shifts downward relative to that at a higher temperature, simply due to the thermally activated zero-field mobility in channel transport (without considering injection limitation at contacts). Due to the fact that the field-dependence of mobility becomes

stronger at lower temperature as predicted by Poole-Frenkel and Bassler et al., the LnI-LnV curves at different temperatures tend to be closer to each other and even bundle at higher longitudinal fields, which was found previously in a Monte Carlo simulation with drift-diffusion modeling for OTFTs of ideal contact injection [46]. Furthermore, this kind of grouping behavior is more severe at higher gate bias. We attribute this gate-dependence to gate-reduced injection barrier height. As we will discuss in subsection 5.7.5, higher gate bias shifts the Fermi level relative to the bending band which forms an injection barrier so that it reduces the barrier height and improves the injection efficiency at metal-organic semiconductor contact. Injection limitation tends to shift the LnI-LnV curve downward by an extra amount in addition to the downward shift due to thermally activated zero-field mobility, which makes curves at different temperatures farther away from each other and counteracts their grouping behavior since the downward shift is larger at lower temperatures. At lower gate bias, the injection barrier is higher and the downward shift the LnI-LnV curve at each temperature is bigger, which increases the "distance" between curves at different temperatures so that their grouping behavior cannot be observed in the same longitudinal field range (it can only occur at higher Vds). At high gate bias, the injection barrier height is reduced so that the "distance" between curves at different temperatures is smaller with respect to the low gate bias case, and we can observe the grouping behavior. Fig. 5.14 is just an example, and the trends shown in Fig. 5.14 were observed in other sub-micron channels.

5.7.5 Injection barrier at metal-organic semiconductor contacts

It is then important to study the mechanism for injection barrier to limit the transport in an OTFT. Within the theories and models established to study the injection problems in organic devices, there are basically two types of transport behaviors through an injection barrier at metal-organic semiconductor contacts [51], namely, thermionic emission [42, 51-52] and Fowler-Nordheim tunneling [53, 54]. In an OTFT, based on these two models, gate bias and source-drain bias both have an influence on the contact barrier. With increasing gate bias, at the metal-organic semiconductor (p-type) contacts, the Fermi level shifts with respect to the bending HOMO level on the semiconductor side which constitutes the injection barrier, reducing the height of injection barrier (the difference between Fermi level and the HOMO level which contacts the metal side). With increasing longitudinal field, the injection barrier becomes thinner [54] so that the tunneling probability rises; and meanwhile the injection barrier height reduces [54] and the thermionic emission is enhanced, due to the evolution of the curvature of bending HOMO level on semiconductor side (similar to DIBL—Drain Induced Barrier Lowering). There have also been reports showing a model at contacts different from the above mentioned [55], where it was proposed that commonly assumed (diffusion-limited) thermionic-emission models do not adequately describe the charge injection process in bottom-contact polymer transistors, and the resistance due to bulk transport through a depletion region contributes to the drain contact resistance.

Both of the standard models (thermionic emission and Fowler-Nordheim tunneling) for injection behavior through metal-organic semiconductor contacts predict that gate bias and longitudinal field improve the injection efficiency and reduce the contact resistance, which is consistent with the experimental findings as shown in Fig. 5.12 and 5.13. However, the real case of metal-organic semiconductor contacts is very complicated. In reality, the situation of the injection barrier for thermionic emission and Fowler-Nordheim tunneling not only depends on the work function and band structures of the two contacting materials to determine band-alignment and band-bending, but also relates to many inevitable experimental factors such as interface dipoles, residual doping in organic semiconductors (affected by ambient air), the thickness of adhesive metal layer, the chemical resistance of metal material (e.g., native oxide), the reaction between the metal and organic layer, the purity of the organic layer, delamination of the metal layer, and the morphological coverage of organic semiconductor onto the metal electrode sidewall (dependent on the deposition conditions).

Although there are many real factors affecting the contact resistance and even some contact sensitive conditions which are not well controllable or predictable, we can still empirically characterize contact resistance and study its influence on the performance of an OTFT [10, 48, 55-63]. All these reports have shown that the contact resistance in most cases is not ohmic/linear. Different methods were proposed to extract the actual performance parameters (especially mobility) excluding the contact influence out of the experimental data. Scanning Kelvin probe [48, 55] and simulations [56] proved

to be powerful tools to investigate the contact effects giving deep insights into the physical nature at metal-organic semiconductor contacts. It was found that the applied source-drain voltage Vds will not completely impose onto the gate-modulated channel, instead, part of Vds drops across the contact region at the source or drain. The potential drop at the source contact is usually larger than that at the drain contact, and this asymmetry could be reduced by applying high gate bias on the OTFT. Beyond this basic picture for contact effects, there were reports about the charge injection behavior which is related to not only metal-semiconductor contacts, but also the gate dielectric layer. It was suggested that in addition to the determination by electrode-semiconductor interface, the charge injection barriers may also depend on the interactions at the dielectric/electrode interface, the semiconductor/dielectric interface, and even the complex triple interface [63].

5.8 Conclusion

The bulk transport at zero gate control in OTFTs can read as ohmic, TFL and trap-free SCLC regimes sequentially. For the channel longer than 100nm at medium and high gate biases, bulk transport is not comparable to the gate-modulated channel transport. At high longitudinal fields, transport is not limited by the injection barrier. We propose that in real nanoscale OTFTs with a reasonable gate control, the field-effect channel transport exhibits dominating transport-mechanisms in the injection-limited regime and the field-dependent mobility regime sequentially with increasing longitudinal field.

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Chapter 6

Scaling effect on sensing behavior of organic and polymeric FETs

6.1 Introduction

6.1.1 Field-effect transistors as chemical sensors

In recent years chemical sensing has become increasingly important not only from an industrial standpoint but also from a homeland security perspective. Sensors with the ability to detect chemicals, such as volatile organic compounds (VOC), and biological species, including DNA and proteins, have been given more and more attention by the scientific and industrial communities. This is due to their great potential in an array of applications comprising manufacturing, transportation, environmental monitoring, process control, drug delivery, homeland security and national defense [1-5]. However most of the commercial products available at present are bulky, costly and require long time periods for sampling and analyzing data. A novel scheme which employs portable and inexpensive devices with the advantage of fast retrieval is desired. Miniaturization is demanded for all types of sensors because of the needs of better portability, higher sensitivity, lower power dissipation and better device integration [6,7]. There have been many types of sensors evaluated for this purpose, utilizing various techniques of transduction such as acoustic wave devices [8,9], electrochemical resistive sensors [10,11]

and field-effect transistors with a chemically sensing gate (CHEMFETs) [12,13]. Among these sensing schemes, field-effect transistors have attracted more and more interest due to their ability to amplify in-situ, gate modulate channel conductance, and allow for compatibility with well-developed microelectronic fabrication techniques which enable miniaturization. A simple resistive sensor only probes the change on bulk conduction and simple capacitive sensor only probe the change on permittivity. Since the drain current in an FET reflects the transport through the two-dimensional electron gas (2DEG) at the semiconductor-dielectric interface, instead of the conduction through the bulk, an FET sensor would directly detect the effects on 2DEG transport caused by the analyte through the change on drain current. An FET sensor has higher sensitivity due to its gain and provides gate-modulation as one more degree of freedom for pattern recognition.

6.1.2 Organic thin-film transistors as chemical sensors

In this chapter we will first introduce polycrystalline organic and polymeric thin-film field-effect transistors and then cover such topics as the proper detection of sensing signals truly from nanoscale active area, the geometry (for device and material) dependence of the sensing behavior, and discussions for the sensing mechanisms in these sensors. We will also address several aspects of the interactions which produce sensing effects in electronic devices, and the trend towards better device performances and further commercialization. Finally other emerging nanoscale sensors will also be

summarized such as nanocrystal, carbon nanotube and nanowire sensors for electrical detection of biological events.

The chemical sensors made of organic or conjugated polymeric transistors are operated at room temperature, which gives an advantage compared to inorganic MOSFET sensors. Upside-down (see chapter 1) organic thin-film transistor (TFTs) sensors use the organic semiconductor active layer as the transducer which interacts with airborne chemical species referred to as analytes. This kind of structure provides analytes a direct access to the active semiconducting layer and enables to investigate how the sensing behaviors depend on its morphology and interface properties. The interaction given by analytes directly affects the conductive channel unlike the sensors made of inorganic MOSFETs [14-17] or the insulated gate FETs (IGFETs use the polymer layer as the gate for a silicon FET [6]) where the sensing events occur at the gate or gate/insulator boundary and indirectly modulates the drain current through capacitive coupling. This means conductivity in the upside-down structure can be affected by changes in mobility (as well as changes in charge density) which is not possible in the other sensor configurations. These upside-down organic and polymer sensors can be refreshed by reverse biasing the gate (a high positive voltage for p-channel, a high negative voltage for n-channel) to remove the trapped charges which result from the semiconductor/analyte interaction.

The Organic Thin-Film Transistor (OTFT) is a promising sensor device for an electronic olfaction platform that possesses all the required features (sensitivity, reliability and reproducibility) at low cost. Compared to CHEMFETs or chemiresistor sensors, an OTFT sensor can provide more information from changes in multiple parameters upon exposure to analyte, namely the bulk conductivity of the organic thin film, the field-induced conductivity, the transistor threshold voltage and the field effect mobility [18]. Organic and polymeric field-effect transistors employing different active layers are able to detect a variety of analyte molecules with good stability and significant sensitivity [19]. Chemical detection is possible through direct semiconductor-analyte interactions and specific receptor molecules percolated in the semiconductor layer for selective analytes, as well as varying the end/side groups of the semiconductor material, and controlling the thin-film morphology of the semiconductor layer. Compared to inorganic transistor sensors, organic/polymeric transistors possess the advantages of specific functional groups on the semiconductor molecules/backbones able to selectively bind the analyte and the compatibility to incorporate small receptor molecules for better sensitivity and selectivity. These advantages of OTFT offer a basis to construct combinatorial arrays of sensors with different responses to the components of an odor mixture. Furthermore, gas-sensing complementary circuits and logic gates with OTFTs have been demonstrated [20]. These advances, with additional circuitry for pattern recognition, could lead to an electronic nose.

6.1.3 Justification for nanoscale OTFT chemical sensors

There have been reports exploring the chemical sensing effects of organic and conjugated polymer transistors [19-20, 21-23]. It has been shown that on large scale devices (L > 1 μm), alkyl chain alcohol analytes interact with polythiophene thin-films at grain boundaries and at the dielectric interface rather than the bulk of the films [24]. Recently, there have been reports on the role of the side-chain in chemical sensing of polymer/oligomer based field-effect transistors [23, 25]. Other articles have delved into the sensing effects dependent on the channel length to grain size relationship in large scale organic transistors [26, 27]. There is also an increasing need to develop sensors with very small active areas, not only for lower power requirement, but also for the possibility of higher sensitivity [28]. However according to our experimental findings and analysis, scaling down the geometry of an Organic Field-Effect Transistor (OFET) device is not a simple way as expected to enhance the sensitivity. Instead, the sensing mechanism of where and how analyte molecules affect the electrical transport in an organic transistor might be quite different for devices at nanoscale dimensions. The main reason is that unlike the classic MOSFET with crystalline silicon channel, the electrical transport and chemical sensing behaviors of a polycrystalline OFET heavily depend on the morphology structure of the channel material and the properties of interfaces. For large scale OFET devices, grain boundaries play the dominant role for both electrical transport and chemical sensing behaviors. For smaller channel lengths, the number of grain boundaries within a channel decreases so that the weight of influence of grain

boundaries on electrical transport and chemical sensing reduces and other factors become more important. At smaller channel dimensions, especially when the channel length is comparable to or smaller than the grain size of polycrystalline organic molecules or conjugated polymers, we might possibly observe the electrical transport and chemical sensing behaviors within the body of grains which may exhibit a mechanism different from that in large scale devices where grain boundaries dominate. In addition, contact barrier at the interface between electrode and semiconductor will also play an important role upon scaling since the resistance through the semiconductor channel becomes smaller. We believe it is the injection of current at the source/drain contacts that gets modulated by the analyte molecules [29]. Thus the behavior of nanoscale OFET sensors is markedly different from larger channel length devices.

The use of nanoscale device dimensions in organic transistor sensors provides a drastically different sensor mechanism compared to micron sized devices with the same semiconductor-analyte combination. This is because in a large scale device (channel length much larger than the grain size of active semiconductor layer), the sensing mechanism is analyte-induced charge trapping, which generally leads to a decrease in device current upon exposure to the analyte. In nanoscale devices, the analyte molecules modulate the charge carrier injection at the source and drain contacts. This can lead to drastic increases in device current which implies that such sensors are more sensitive. It is known that the electrical transport in very short channel length organic transistors is contact limited and we believe that the analyte molecules diffuse near the source/drain

contacts through the porous semiconductor layer. Thus the analyte molecules are able to influence the behavior of the contact [29]. The smaller the channel length, the stronger this effect is. As documented by the experimental evidences [29], nanoscale OTFT sensors exhibit a remarkably different behavior from the micro-scale counterparts. In OTFTs of such small dimensions, the drain current increases typically by a factor of > 2 in response to the analyte (>5 for some devices). This provides a strong argument to employing nanoscale channel length devices for chemical sensing.

6.1.4 Previous work for micro-sized OTFT vapor sensing and its correlation to thin film morphology

The vapor sensing behavior of nanoscale organic transistors is different from large-scale devices due to the fact that electrical transport in an OTFT depends on its morphological structure and interface properties and thereby analyte molecules are able to interact with different parts of a device and correspondingly modulate the overall conductance of the device. In previous work for micro-sized OTFTs made of a variety of active semiconductor layers [19, 30], Crone and Torsi ***et al.*** have investigated the relation of vapor sensing to thin film morphology upon exposure to different analyte molecules. A correlation of the vapor response characteristics to the length of end groups (flexibility at the molecular level) and grain size (porosity at the morphological level) of the semiconductor was demonstrated by observing the transient source-drain current under

vapor flow and performing transmission electron microscopy (TEM) for morphological characterization.

These experiments have demonstrated that the sensing response of OTFT channels to analytes of moderate dipole moments (e.g. alcohol) is enhanced with decreased grain size and looser molecular packing of the organic semiconductor layer. Smaller grains yield more grain boundaries which provide more interaction sites for sensing events. The response also increases with increasing film thickness, again due to the increased number of grain boundaries (the surface morphology becomes more structured as the films grow thicker from the flat and featureless ultra-thin film). Analytes binding to the disordered and thinner grain boundaries are closer to the channel than those on the top surfaces of the grains and thus exert greater influence on the charge transport in channel.

It was also found that the degree of sensing response increased as the length of the organic semiconductor's hydrocarbon end group increased. This is due to the elongated lamellar morphology and looser molecular packing which allow greater access of analyte vapor and increased surface area, as well as change the electronic or spatial barriers between grains. Therefore the alkyl chains facilitate the adsorption of the analyte molecules by the sensing film. This adsorption mechanism could be a combination of hydrophobic interactions, intercalation to fill defect vacancies and simple surface binding. All of these processes are favored at grain boundaries.

The interaction between organic semiconductor and analyte molecules is still not yet completely understood. The adsorbed polar analyte could influence the charge transport in the channel by trapping some charges and consequently decrease the mobility of other mobile charges in channel. However the major effect of the trapped or otherwise immobile charges at the dielectric interface is to induce a shift of threshold voltage in the transistor characteristics. For alcohol sensing, a constant threshold shift was observed at low gate voltages, which became a gate voltage-dependent mobility change at high gate voltages. It was also observed that a reverse gate bias can facilitate the restoration of drain current to near its original value.

The interaction between the alcohol and the organic semiconductor film in OTFT does not involve the bulk of the crystalline grains of the film since no change in refractive index and thickness of the film was observed with a single wavelength ellipsometer during the exposure of the film to the analyte vapor. It was suggested that the sensing interaction is a surface type interaction involving grain boundaries.

6.2 Experimental

6.2.1 Experimental considerations for fabricating organic/polymeric TFTs as sensors

With the four terminal methodology (see chapter 3), we fabricated transistors with organic molecules (pentacene) and conjugated polymers [regioregular poly(3-hexylthiophene), P3HT] which included a range of channel lengths from a few hundred microns down to sub 10 nm. The field-effect characteristics of the organic semiconductors as the channel layer, as well as their responses to analytes as the sensing layer, were characterized in order to systematically investigate the relationship between sensing behaviors and geometry factors of the channel. The grain size of the organic semiconductor was also varied to investigate the role of scale in organic transistor sensing behaviors. Pentacene was chosen as the active layer due to its relatively high mobility and wide use in organic electronics and sensors [31, 32]. P3HT is a soluble conjugated polymer with relatively high mobility and thus has a great potential to be manufactured into chemical sensors with low-cost techniques such as ink-jet printing [33-35]. The analytes we employ to test nanoscale devices are 1-pentanol and vanillin. Various types of analytes have been applied to investigate the chemical sensing responses of long channel devices, and we have found that 1-Pentanol is a prototypical alcohol analyte to represent their sensing behaviors. Vanillin is widely used in pharmaceuticals, perfumes and flavors.

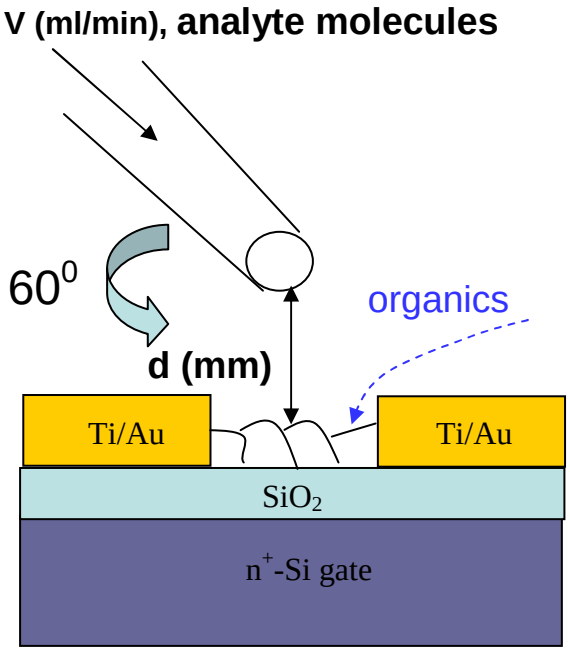

Fig. 6.1 The schematic structure of a bottom contact organic thin film transistor used as chemical sensor. Its organic semiconductor channel, which serves as the sensing layer, is exposed to the analyte vapor delivered with a controlled flux through a carefully positioned syringe. Reprinted from Liang Wang, Daniel Fine, Deepak Sharma, Luisa Torsi and Ananth Dodabalapur, Analytical and Bioanalytical Chemistry, Vol. 383, No. 7, Dec. 2005, with kind permission of Springer Science and Business Media.

The transistor device structure (bottom-contact devices) is shown in Fig. 6.1. This device configuration allows the organic semiconductor to be operated simultaneously as both the transistor channel and the sensing layer which the analyte molecules can directly access. A heavily doped n-type silicon substrate serves as the gate. Transistors of channel length greater than 1μm utilize a 100 nm thermally grown SiO_2 layer as the gate dielectric, whereas for nanoscale transistors, a 5 nm SiO_2 layer as the gate dielectric was grown by rapid thermal annealing in dry oxygen. 3nmTi/45nmAu was deposited by e-beam evaporation onto the wafer after e-beam lithography (for submicron channel

lengths) or photolithography (for micron channel lengths). With lift-off, electrode patterns of channel lengths down to 15 nm were obtained. Sub 10 nm channels were created by electrophoresis trapping bridge and break junction techniques [36, 37]. Electrode patterns of channel lengths > 100 μm were realized directly by metal evaporation through shadow masks. 300-600 Å of pentacene (purchased from Aldrich) were thermally evaporated in a base vacuum of about 3 x 10^{-7} Torr at different growth rates and different substrate temperatures for different grain sizes. For channel lengths greater than a micron, an elevated substrate temperature (80 ºC) and medium growth rate (1.9 Å/sec) resulted in large pentacene grains with an average size of 1 μm. Nanoscale channels comprising of medium pentacene grains, with an average size of 250 nm, were achieved by slow growth rate (0.5 Å/sec) at room temperature. High growth rates (4.4-7.1 Å/sec) at room temperature during thermal evaporation gave a pentacene layer of small grains with an average size of 80-140nm. Regioregular P3HT was synthesized as described by Bao ***et al.*** [38]. The P3HT was dissolved in chloroform with the ratio of about 0.1% by weight. Solutions were filtered with 0.2μm pore size PTFE membrane syringe filters. Bottom contact devices were completed by solution-casting with a custom ink-jet type deposition apparatus to inject the solution and limit the coverage area to within 200 μm to lower the leakage through gate dielectric. The devices were finalized by immediately transferring into a vacuum oven to evaporate the solvent for 36 to 48 hours.

6.2.2 Characterization measurements and sensing experiments

The DC electrical characteristics of the transistors were measured with semiconductor parameter analyzer Agilent 4155C. The transient variation of drain current I_{ds} was then examined under fixed gate (V_g) and source-drain voltage (V_{ds}) in air at room temperature. A peristaltic pump was employed to drive air through a transfer line (TYGON tube) into a monojet syringe to deliver the saturation vapor there to sensing devices. To provide the saturated analyte vapor, the syringe contained a piece of analyte-soaked filter paper and was fixed onto a 3-dimensional micromanipulator to ensure proper alignment of the vapor outlet to the transistor channel. A solenoid valve was placed in the middle of the transfer line to switch the analyte delivery. The analyte flux (v) and the syringe nozzle-device distance (d) were varied to examine the influence of analyte delivery on the sensing responses. Currents were measured throughout the entire measurement period while the analyte was only delivered for a certain period of duration, in order to facilitate a comparison of the drain current behavior before, during, and after the exposure to the analyte.

Before every sensing measurement, each device was tested with pure air (the carrier to deliver various analytes) and no sensing or kinetic effect on drain current was detected. The currents in the absence of analyte continuously decrease over time due to bias stress effect. This is a well-known effect in organic field-effect transistors in which the current slowly decreases with time at a fixed bias because the field-induced carriers

(holes) fall into deep trap states where they are less mobile, which results in a reduction of drain current [39, 40]. The sensor response is superposed on this background. After each sensing measurement, the device characteristics were recovered by using a reverse bias configuration (high positive gate voltage with a small drain current flowing for 1min). The measured leakage currents through the gate dielectric were negligible compared to the drain currents. After the measurements, all the devices were examined by a field-emission SEM and no deterioration in morphology was found.

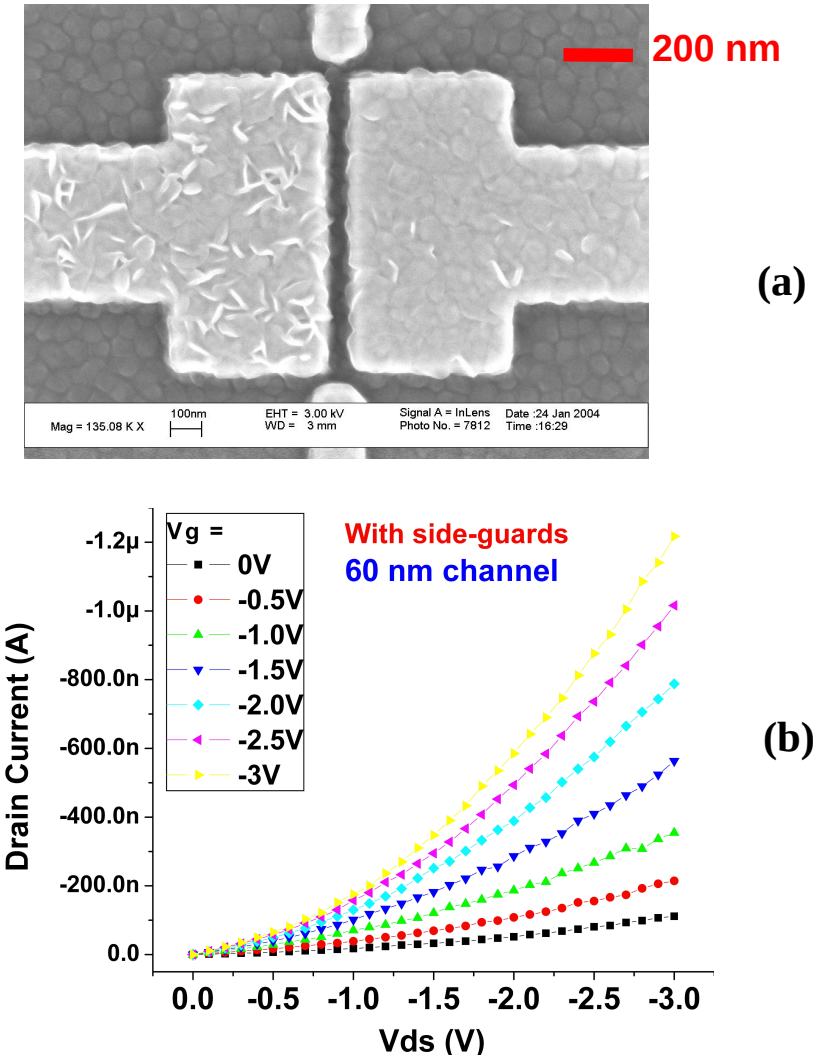

Fig. 6.2 Post-measurement SEM image (a) and Characterization (b) of a pentacene transistor of 60 nm channel (W/L=10) for sensing measurements, measured in 2.4 mTorr vacuum, calculated mobility=0.021 cm^2/Vs. Reprinted with permission from Liang Wang, Daniel Fine, and Ananth Dodabalapur, Applied Physics Letters, 85, 6386 (2004). Copyright 2004, American Institute of Physics.

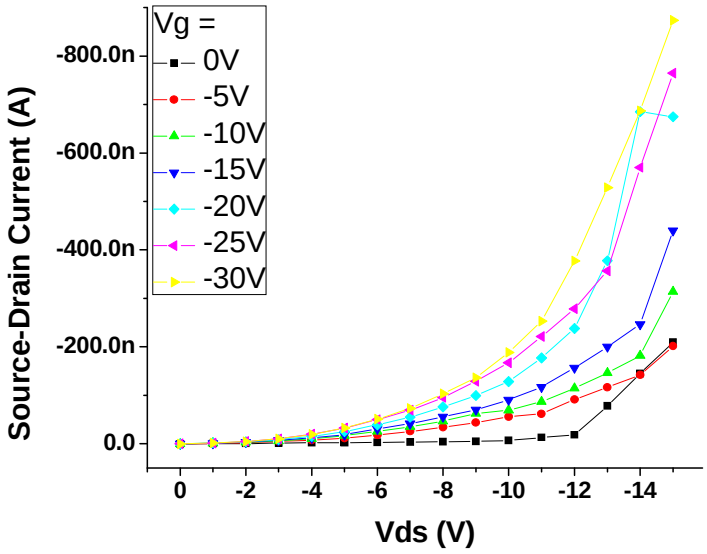

Fig. 6.3 The DC characteristics of a 125 nm channel (W = 275 nm) P3HT transistor in air at room temperature. The mobility is 1.2 X 10^{-2} cm^2/Vs in the linear region of operation. Reprinted from Sensors and Actuators B (in press), Liang Wang, Daniel Fine, Saiful I Khondaker, Taeho Jung, Ananth Dodabalapur, Sub 10 nm conjugated polymer transistors for chemical sensing, Copyright (2005), with permission from Elsevier.

The mobilities of the pentacene transistors were of the order of 10^{-2} cm^2/Vs, with a highest value of 0.045 cm^2/Vs observed in air for the transistors with pentacene grain size of 1 µm and channel length of 36 µm. Fig. 6.2(a) shows the SEM image taken after the sensing measurement of a 60 nm channel (W/L=10) with pentacene grain size of 80 nm. Fig. 6.2(b) is its characterization measured in vacuum. Its mobility was calculated to be 0.021 cm^2/Vs. The mobilities of most P3HT transistors measured in air at room temperature were in the order of 10^{-3} cm^2/Vs, while only a small number of devices exhibited a mobility approaching 10^{-2} cm^2/Vs. Fig. 6.3 shows the characteristics of a P3HT transistor with a channel length of 125 nm and channel width of 275 nm,

corresponding to a mobility of 1.2 X 10^{-2} cm^2/Vs in the linear region of operation. In spite of the relatively high off-current, these plots show a reasonable gate modulation. The super-linear feature in these devices is due to the contact barrier between the conjugated polymer and gold electrodes. In the devices where the mobility of the organic semiconductors is relatively high, the contact barrier becomes the bottleneck of transport which can be seen as the super-linear feature in the characteristics. Variation of mobilities from device to device was observed in these polymer devices, which is attributed to the difference in the semiconductor's local order and coverage on channel.

6.3 The function of guarding electrodes in chemical sensing

With the design of side-guard electrodes, we can investigate the transport behavior of OTFT in truly nanoscale dimensions excluding the spreading currents in large area, without the difficulty to pattern the semiconductor layer into such small size as the channel length. More importantly, with these devices as chemical sensors, the side-guarding function ensures that the active sensing area is truly nansocale. This novel four-terminal geometry design provides a powerful capability to investigate the sensing behavior within the nanoscale active area through the defined channel without any undesirable background from large-scale parasitic conduction pathways around the channel.

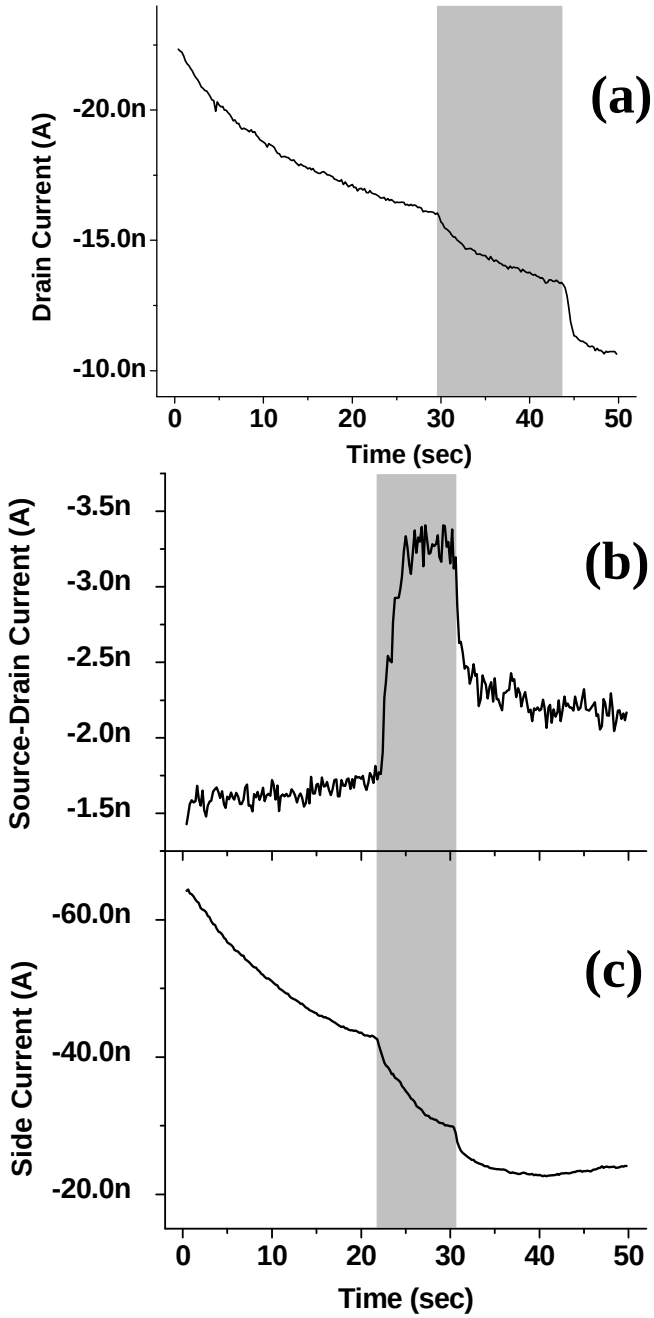

Fig. 6.4 The sensing effects of a 7 nm channel P3HT transistors upon exposure to the saturated 1-pentanol vapor. (a) The sensing response at V_g= -20 V and V_{ds}= -1.5 V, without applying side guarding electrodes. (b) and (c) are the sensing responses of currents simultaneously collected at the drain and side electrodes respectively, with side guarding electrodes at the same potential as the drain to collect spreading current, at V_g= -20 V and V_{ds}= V_{side}= -1.5 V. Reprinted from Sensors and Actuators B (in press), Liang Wang, Daniel Fine, Saiful I Khondaker, Taeho Jung, Ananth Dodabalapur, Sub 10 nm conjugated polymer transistors for chemical sensing, Copyright (2005), with permission from Elsevier.

A transistor with a 7 nm channel was made by trapping bridge and break junction technique [36, 37]. To investigate the sensing response from the sensor active area in truly nanoscale geometries and the role of the side guarding electrodes in the sensing measurement, we recorded the drain current transients upon exposure to 1-pentanol without and with applying side guarding function, as shown in Fig. 6.4(a) and (b) respectively. Surprisingly, Fig. 6.4(a) and (b) manifested opposite sensing response directions. Without the side guarding function, the transient shown in Fig. 6.4(a) represents the sensing behavior of the large area around the channel, which is a decrease in drain current by 20-25%. With the side guarding function to eliminate most of the spreading current (two side guarding electrodes biased at the same potential as the drain), the transient in the drain current [Fig. 6.4(b)] represents the true sensing behavior of the nanoscale active area, which is an increase in drain current by approximately a factor of 2. Fig. 6.4(c) exhibits the variation of the side current (collected at side guarding electrodes) corresponding to that of the drain current [Fig. 6.4(b)], which were measured simultaneously with Fig. 6.4(c). The side current response to the analyte is markedly different compared to the drain current in Fig. 6.4(b), namely, the side current shows a decrease in response to the analyte whereas the drain current simultaneously shows an increase upon exposure to the analyte. Since Fig. 6.4(b) and (c) were recorded simultaneously and showed different kinds of sensing behavior, it is evident that the side current is the spreading current traveling outside the defined channel and the current collected simultaneously at the drain is the direct current through the nanoscale channel.

Therefore utilizing the side guarding function we can eliminate most of the contribution from the spreading current and detect the true sensing response of a nanoscale channel. The experimental findings obtained with this unique side-guard function are presented below for the chemical sensing responses dependent on the scaling geometry, analyte delivery and gate modulation, as well as different type of analytes.

6.4 Experimental results on scaling behavior of sensing responses:

6.4.1 Dependence of sensing responses on channel lengths and grain sizes

We investigated the response of I_{ds} (operated in saturation region) upon exposure to the saturated vapor of 1-pentanol, with a series of channel length and varied grain sizes of pentacene under the same experimental conditions. As shown in Fig. 6.5(a), while the long channel length devices all exhibited a decrease in drain current upon delivery of the analyte, the small channel length devices showed an increase, sometimes by a factor of >5. There are two mechanisms influencing sensor behavior: one causing a decrease in current (dominant in large L devices) and the other causing an increase (dominant in small L devices). There is a crossover between these two types of response behaviors which depends on grain size, occurring in the interval of channel length between 150-450 nm for ~80nm grain size. Under the same condition, when the average grain size of pentacene is increased to 250 nm, the sensors exhibits the crossover behaviors at larger channel lengths (from 450 nm to 1 μm), as shown in Fig. 6.5(b). Fig. 6.6 shows the SEM

image (after measurements) for geometric relation of the same channel length (150nm) with different grain sizes of pentacene layer.

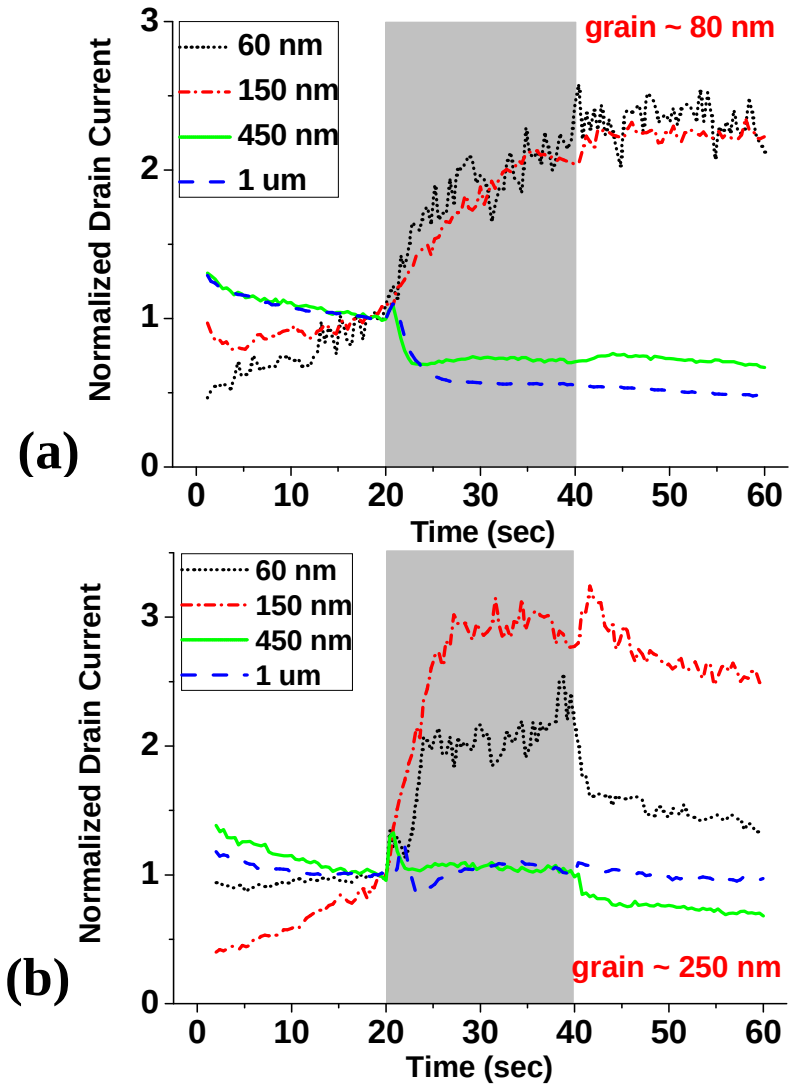

Fig. 6.5 The sensing effects of nanoscale pentacene transistors upon exposure to 1-pentanol. (a) Sensing data of I_{ds} (normalized to that measured just before the analyte took effect) for 80 nm pentacene grain size and different nanoscale channel lengths (same W/L=10), measured at $V_g=V_{ds}=V_{side}$=-2.5 V (two side guards were kept at the same potential as the drain), v (analyte flux)=45 ml/min, d (distance from syringe nozzle to device)=2 mm. (b) Sensing data of normalized I_{ds} for 250 nm pentacene grain size, measured at the same conditions as (a).
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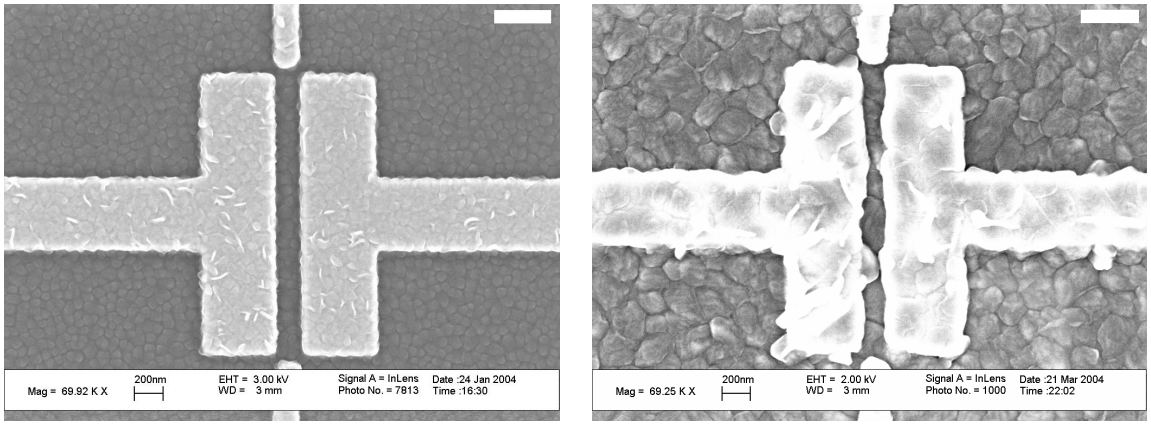

(a) **(b)**

Fig. 6.6 SEM image taken after sensing measurements of a 150 nm channel with different average pentacene grain sizes of 80nm (a) and 250 nm (b), scale bar=400 nm. The grains appearing in the figure are pentacene. Reprinted with permission from Liang Wang, Daniel Fine, and Ananth Dodabalapur, Applied Physics Letters, 85, 6386 (2004). Copyright 2004, American Institute of Physics.

Fig. 6.7(a) and (b) are the sensing responses of long channel devices with pentacene grain size of 140nm and 1 μm respectively. For all devices with channel lengths of 2 μm or greater, I_{ds} manifested decreasing responses upon analyte delivery. The amplitudes of decreasing signal for 2 μm channels were smaller than those of longer channels. This effect is stronger with larger pentacene grains [Fig. 6.7(b)]. These results are consistent with the reported work for sensing effects dependent on organic grain sizes and channel lengths in large scale [30, 41]. The sensing responses shown in Fig. 6.5 and 6.7 are reproducible for different devices with the same channel lengths and grain sizes, concluding that the response of pentacene transistors to the 1-pentanol vapor changes from decreasing I_{ds} to increasing I_{ds}, when the channel length shrinks from micron to 100 nm scale, with a crossover happening in a transition interval of channel length which is related to the grain sizes of pentacene.

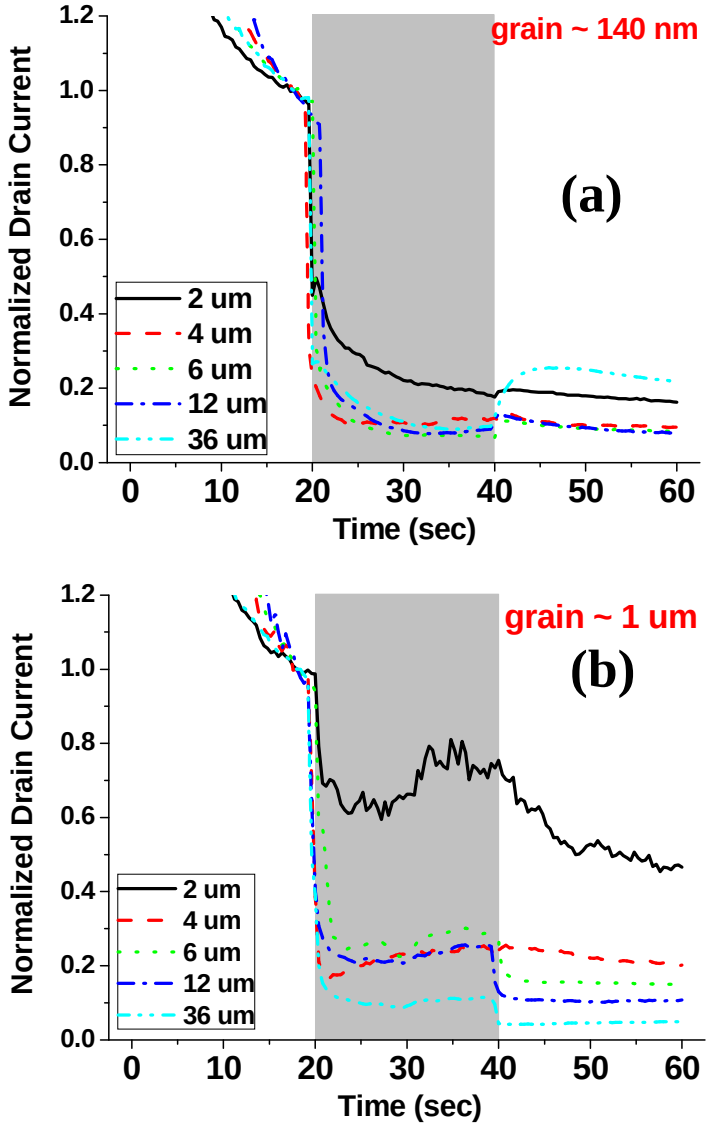

Fig. 6.7 Sensing data of large scale pentacene transistors upon exposure to 1-pentanol: normalized I_{ds} under the condition of $V_g=V_{ds}=-25$ V, v=45 ml/min and d=2 mm for different microscale channel lengths, with average pentacene grain size of 140 nm and 1 μm in (a) and (b) respectively. Reprinted with permission from Liang Wang, Daniel Fine, and Ananth Dodabalapur, Applied Physics Letters, 85, 6386 (2004). Copyright 2004, American Institute of Physics.

6.4.2 Influence of analyte delivery

To examine the influence of analyte delivery on the sensing responses, we adjust the analyte flux (v) and the syringe nozzle-device distance (d). It turns out that for all the channel lengths and grain sizes, increasing v and decreasing d have similar influences, i.e., to increase the amplitude of the sensing signal. Also it was found that the sensing behavior was similar when operated in saturation region or linear region. Fig. 6.8(a) gives an example of this sensing test on a 22 nm channel with an average grain size of 80 nm, measured under operation in the linear region. Fig. 6.8(b) shows the SEM image of this device taken after sensing measurements.

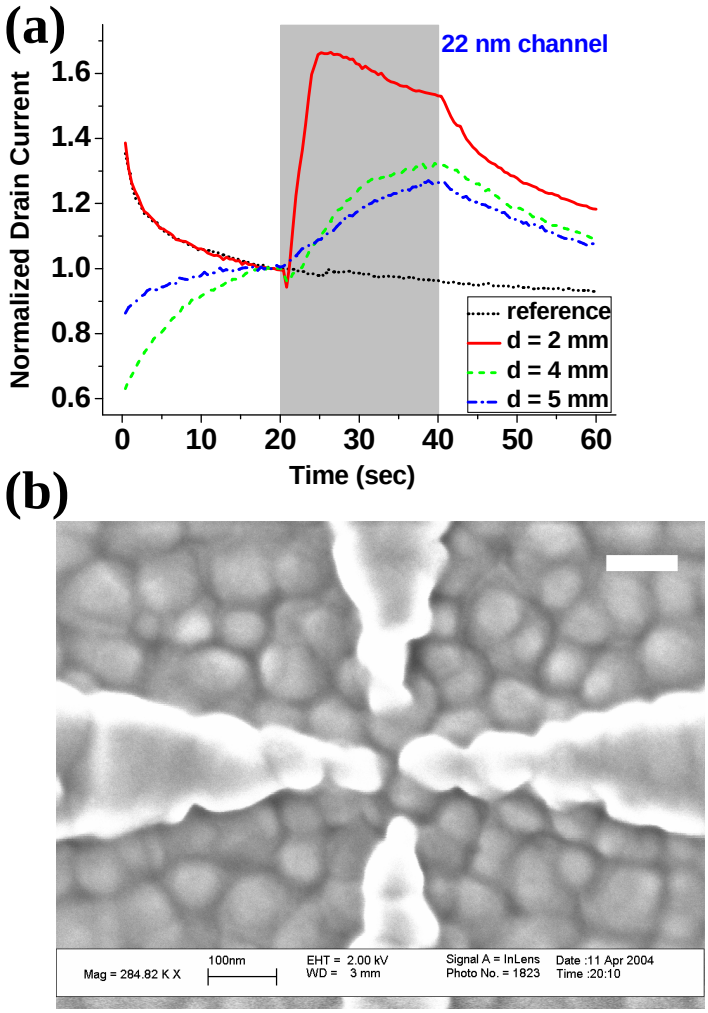

Fig. 6.8 (a) Sensing data of a pentacene transistor of 22 nm channel in response to 1-pentanol, with V_g=-2 V, V_{ds}=V_{side}=-0.4 V and v=45 ml/min for different d (nozzle-device distance), "reference"=absence of analyte.
(b) SEM image of the device in (a) taken after measurements, grain~80 nm, scale bar=100 nm. The appearing grains are pentacene.
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6.4.3 Gate-voltage dependence of sensing responses

For micron scale or larger channel lengths, the drain currents of pentacene or P3HT transistors decreased in response to the analyte 1-pentanol, whereas an increase in current was observed for nanoscale channel lengths. Fig. 6.9(a) and (b) show the two opposite responses at different gate voltages in P3HT transistors of a 25 μm and a 15 nm channel length device respectively. The drain currents are normalized to the pre-exposed base current measured just before the analyte was delivered. As seen from these figures, the gate modulation of the sensing effect is obvious in micron scale channels. In nanoscale channels, the gate bias has less effect on the sensor response, possibly attributed to excess charges given by the analyte-semiconductor interaction which augment the gate-modulated charges, or a reduction in the injection barrier from the contacts to the semiconductor due to some kind of electrostatic analyte interaction at the contact surface. In addition, the dc I-V characteristics of micron scale channels were recovered after reverse bias for 1 minute, while in nanoscale devices recovering was not complete, i.e. off-current increased and on/off ratio degraded after sensing measurement even with reverse bias treatment. Fig. 6.10 shows the SEM image of the 15 nm channel in Fig. 6.9(b) taken before depositing P3HT.

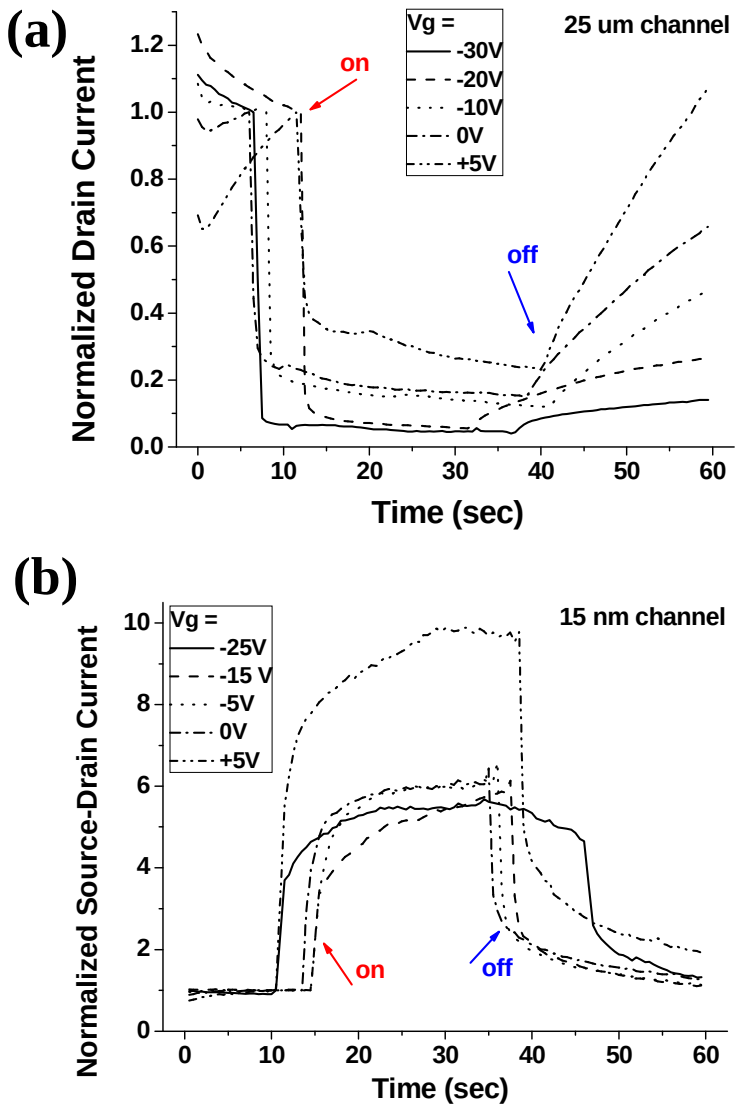

Fig. 6.9 The gate-modulation of sensing effects of micron and nanoscale P3HT transistors upon exposure to 1-pentanol.
(a) Sensing data of top-contact 25 μm channel (W= 500 μm) at different V_g, with V_{ds}= -30 V. The drain current is normalized to that measured just before the analyte was delivered. "on" and "off" indicates the switch of analyte delivery.
(b) Sensing data of 15 nm channel at different V_g, with V_{ds}= V_{side}= -3 V (two side guards were kept at the same potential as the drain)
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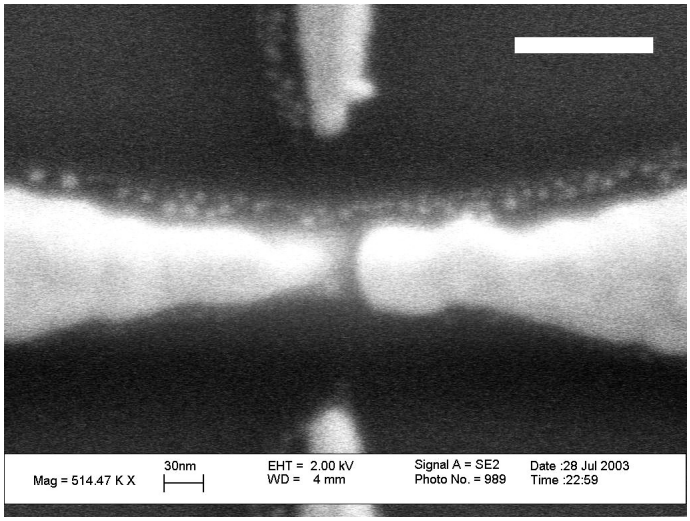

Fig. 6.10 SEM image of the device in Fig. 6.9(b), taken before depositing P3HT, scale bar = 100 nm. Reprinted from Sensors and Actuators B (in press), Liang Wang, Daniel Fine, Saiful I Khondaker, Taeho Jung, Ananth Dodabalapur, Sub 10 nm conjugated polymer transistors for chemical sensing, Copyright (2005), with permission from Elsevier.

6.4.4 Reproducibility of the OTFT chemical sensors

One of the important evaluation on a sensor performance is its reproducibility, namely, how many times the sensor can iteratively demonstrate the same electrical and sensing characteristics before it tends to degrade. For large scale devices, the vapor sensors based on organic field-effect transistors exhibit a reproducibility which reads the same drain current after at least 70 cycles of sensing experiments [19]. However for OTFT sensors at small dimensions, because a different part in the transistor plays the role in sensing event, the reproducibility is not the case in large scale devices.

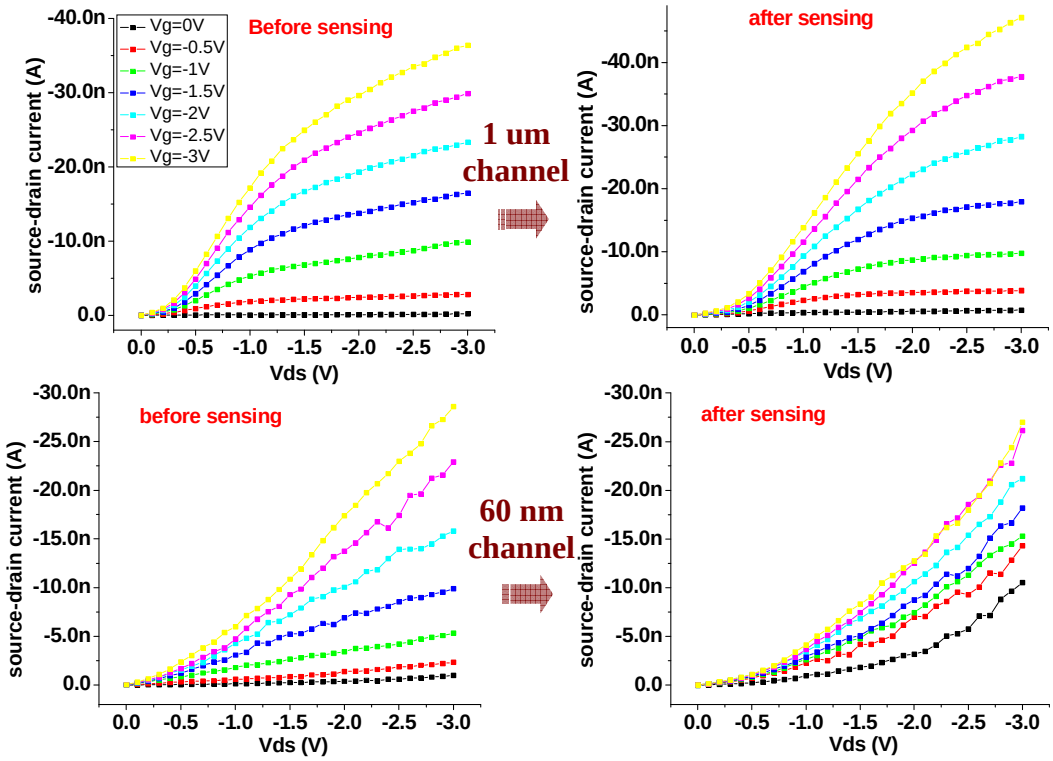

Fig. 6.11 The reproducibility of pentacene TFT sensors. The top and bottom part shows the DC characteristic before and after sensing measurement of devices, with channel length of 1 um and 60 nm respecitively, using the same labels for different gate bias Vg.

Fig. 6.11 shows the DC characteristic before and after sensing measurement of devices with channel length of 1 um and 60 nm. For the channel of L = 1 um, with the aid of reverse bias after each sensing experiment, its DC characteristic measured after the sensing cycles at all the gate biases can still recover to the level before all the sensing measurements. However for the channel shorter than 1 um, especially for nanoscale channel lengths, the drain current can not fully recover to the original level, and more

importantly, the off-current increases significantly after exposure to analytes and thereby the DC characteristic exhibits a different behavior, as shown in Fig. 6.11.

In an OTFT with nanoscale channel length, the analyte-induced modulation on injection barrier at metal-organic semiconductor contacts plays an important role in sensing response, which indicates a different sensing location and sensing mechanism compared to the case in large scale devices. Analyte molecules in volatile vapor form land on and then leave off the grain boundaries in the large scale OTFT sensors, which leads to a reversible change in the device output. However in nanoscale devices the analyte interacts with contacts and causes an irreversible change, and thereby the recover of the transistor performance is limited.

6.4.5 Different type of analyte molecule

P3HT transistors with a series of channel lengths in the sub-micron range were employed to examine the sensing responses of the conjugated polymer upon exposure to another type of analyte--vanillin. As shown in Fig. 6.12(a) for sub micron channels, the 215 nm or larger channels exhibited a decreasing response in drain current upon delivery of vanillin, whereas the 125 nm or smaller channels behaved in the opposite direction, i.e., an increase in current as the sensing response. The crossover of response behavior exists in the interval of channel length 125-215 nm. Fig. 6.12(b) shows the SEM image of a 75 nm channel taken before depositing P3HT. Based on the results for the sensing

measurements of various channel lengths to analyte 1-pentanol and vanillin, there are two mechanisms influencing sensor behavior: one causing a decrease in current (dominant in large L devices) and the other causing an increase (dominant in small L devices).

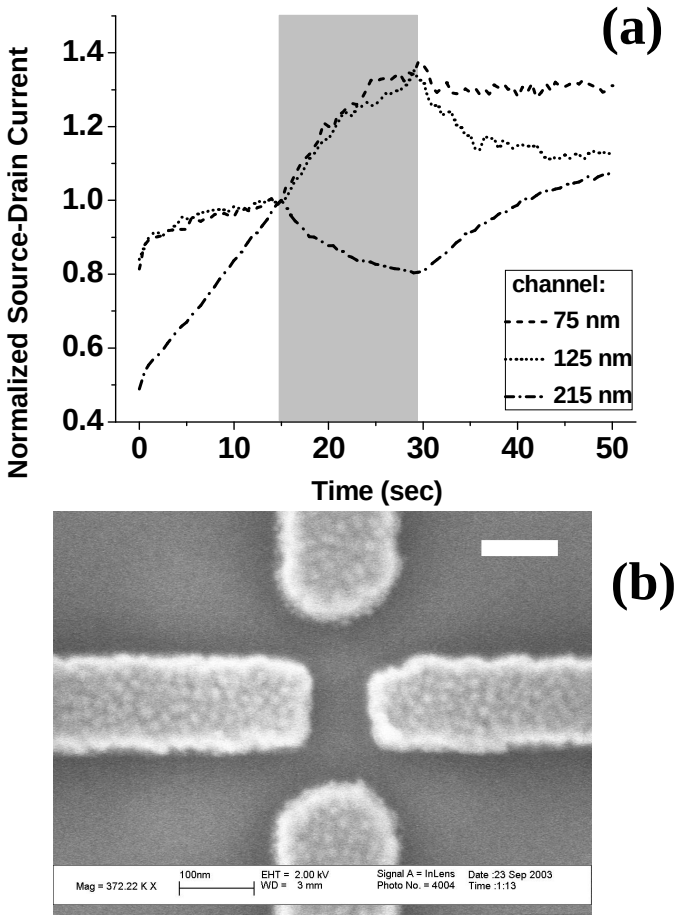

Fig. 6.12 The sensing effects of P3HT transistors upon exposure to vanillin.
(a) Sensing data with V_g= -25 V, V_{ds}= V_{side}= -10 V and -15V for L<100 nm and L>100 nm respectively (two side guards were kept at the same potential as the drain), with different channel lengths and the same W/L of 3.
(b) SEM image of a 75 nm channel taken before depositing P3HT, scale bar = 100 nm.
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6.5 Discussions for the scaling behavior of sensing response:

We discovered that by scaling down the device geometry into nanoscale, the sensing behavior is remarkably different from that of larger devices composed of the same materials for the same analyte. The direction and amplitude of sensing responses were found to be correlated to the channel length and the grain sizes of the organic semiconductor as sensing layer. These results follow the same trend as the reported work for sensing effects dependent on channel lengths relative to grain sizes in large scale organic transistors [30, 41]. These organic and conjugated polymer thin-film field-effect transistors have some features of similarity with polycrystalline oxide semiconductor sensors. In both, grain boundaries play a key role in large scale devices and the analyte influence the electrical transport through grain boundaries and thereby modulates the channel conductivity. According to the mobility study under low temperatures down to 77K, the transistors presented in this work exhibited a transport mechanism of thermally activated hopping, which is mainly attributed to hopping at grain boundaries. Fig. 6.13 shows an Arrhenius plot of temperature-dependent mobility under different gate bias for a pentacene transistor with 2 um channel length. The plot follows the relation for thermally activated hopping: $\mu \sim \exp(- E_a / kT)$. The activation energy E_a (energy barrier at a grain boundary) is 130 meV under -5V gate bias, and reduces to 52 meV under -30V gate bias. The mobility in the OTFTs presented in this work increases with increasing gate bias, as seen in Fig. 6.13, which is attributed to filling of the tail states of the density of states (DOS). Also as Fig. 6.13 represents, the gate dependence is stronger

at lower temperatures. These phenomena are well-known for disordered organic field-effect transistors where the band tail of localized states has a much wider distribution at grain boundaries than within each grain body, due to the increased disorder at grain boundaries [42-43]. It would be meaningful to investigate the influence of sensing action on the distribution of tail states through the combination of sensing experiments and temperature-dependent charge transport measurements. However this is practically difficult at this stage. Most volatile organic compounds (VOC) possess a high vapor pressure so that the analytes will not remain at the sensing sites of device for long enough time. Therefore the comparison of temperature dependence of transistors before and after sensing might not give an accurate view for what happened during the sensing action. Furthermore to perform temperature-dependence experiments in presence of analyte molecules is not feasible due to the condensation effect of VOC at low temperatures.

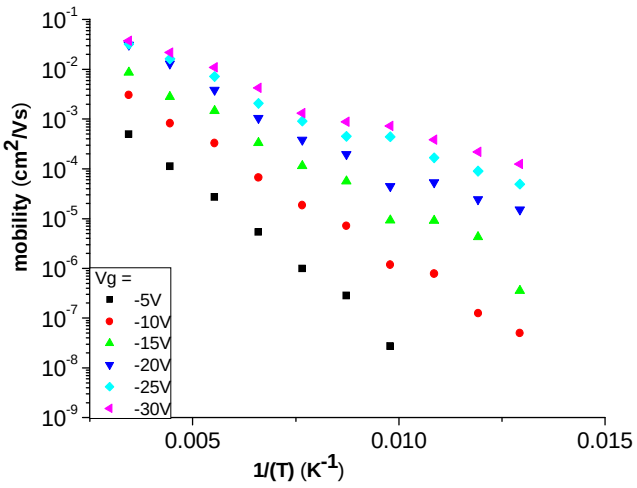

Fig. 6.13 An arrhenius plot of temperature-dependent mobility under different gate bias for a pentacene transistor with 2 um channel length. Mobility values were calculated in linear region of operation.

For large scale transistors, in which a number of grain boundaries are located within a channel, the analyte molecules at grain boundaries play a dominant role in the sensing response, where they trap the mobile charge carriers in active channel and mainly result in a threshold voltage shift of transistor, which leads to a decrease in drain current [19]. For devices with smaller dimensions, there are fewer number of grain boundaries per channel so that the effect of decrease in drain current reduces. When the channel length is close to or smaller than the average grain size, the dominant factor is then a reduction of the contact injection barrier by the interaction from analyte, which leads to an increase in drain current. This is supported by the sensing experiments conducted in our group for the same channel material with contact metals of different work functions [29]. Another possible cause for the increase of drain current as a sensing response observed in nanoscale OTFTs is a doping-like effect which could be the excess charges given from the interaction between semiconductor grains and the analyte molecules. The overall sensing response is the result of a combination of these competing effects from different mechanisms: one causes a decrease in drain current and the other causes an increase, dominating at different length scales. It is indicative of scale being a very key element in the sensing process with organic transistor sensors.

6.6 Discussion on further research and potential applications

6.6.1 For sensing detection by DC I-V or transient measurements

Organic/polymeric transistors and sensors have the flexibility to be improved for better performance and wider applications. Small receptor molecules could be easily incorporated into the semiconductor layer for higher selectivity and sensitivity [44-46]. Co-evaporating organic molecules and blending polymers can be employed to make composite films for a larger variety of detectable analytes. Most importantly, by combining the novel technologies such as soft lithography/nanoimprint [47, 48-53] and ink-jet printing [34, 54-57], we might be able to fabricate chemical sensors based on nanoscale conjugated polymer transistors at fairly low cost. These sensors are also compatible with emerging low-cost organic electronic fabrication processes and can be integrated to processing/display electronics also at low-cost.

One of the most attractive practical applications for organic and polymeric field-effect transistors is to make chemical sensors of high sensitivity and low cost. For this purpose, the following is important but remains to be accomplished: 1) To understand the interaction between analyte molecules and organic semiconductor layers. This will aid the efforts to use experimental parameters to characterize the sensing events for pattern recognition of analytes. 2) By chemical and physical methods, to incorporate small receptor molecules into the organic semiconductor layer to enhance the sensitivity and

selectivity of the nanoscale sensors. However, it is important to remember that there is a trade-off between the sensitivity and reversibility with respect to the binding strength of any type of analyte-sensing layer combinations. Careful study is necessary to find an optimal condition for different needs in different environments. 3) To investigate sensing responses for different analyte-semiconductor combinations in order to find an optimal material for a particular group of analytes. This will enable the building of a database of responses for a sensor array in the purpose of on-line analysis of the composition and concentration of a gas mixture, namely an electronic nose. 4) To investigate the effects of nanoscale morphology of the organic semiconductor layer on sensing behavior, to find an optimal semiconductor morphology and device geometry for high sensitivity. 5) To improve the stability of the organic semiconductor in air. Many reports recounted the influence of humidity on sensing performance and the sensor drift caused by the oxidation of organic materials over time. Therefore, material science and encapsulation/package techniques are needed to overcome these problems.

6.6.2 Proposal of frequency dependent sensing for pattern recognition

The final goal of research in OTFT sensors is to utilize the existing technologies to provide a feasible solution for detecting the composition of a mixture, and evaluating the concentration of each component, namely the electronic nose. By analyzing the response of nanoscale organic transistors to individual analytes in both time and frequency domain, we would be able to identify the distinct signature of individual

analytes and build an integrated chip to analyze the composition and concentration of a mixture of interesting gases.

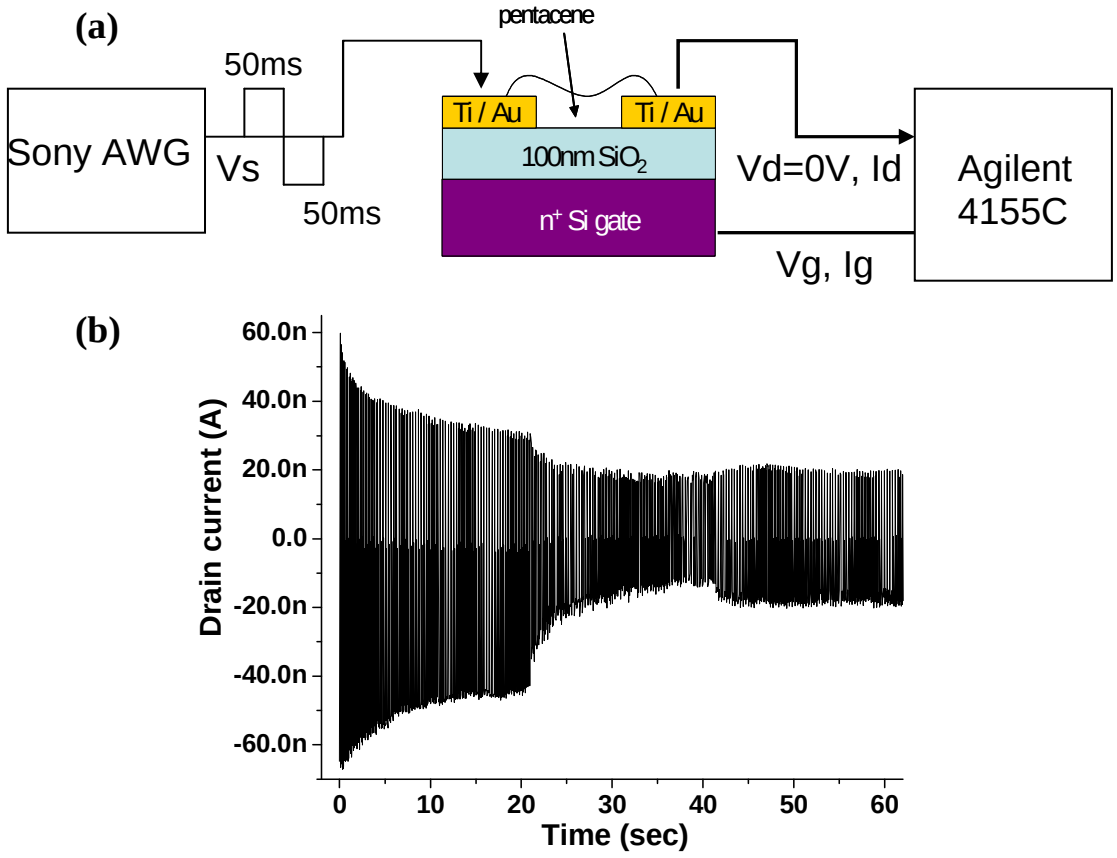

Fig. 6.14 The AC mode of chemical sensing measurements on organic transistors. (a) The experimental set-up. AC signal (Vs as source voltage) oscillating from +6V to -6V within 100 msec are supplied from a Sony AWG; DC bias Vd (=0V) and Vg (= -25V) are supplied from Agilent 4155C; Drain current with variation corresponding to Vs was measured from Agilent 4155C.
(b) The result for a 4 μm long channel to detect the saturated 1-pentanol vapor in AC mode, the envelope of which is similar to sensing signal by DC measurents.

Some preliminary result showed that with AC measurements organic transistors do give the sensing responses in drain current similar to DC measurements. Fig. 6.14(a) shows the experimental set-up for sensing experiments in AC modes. Fig. 6.14(b) is the result taken from a large scale (4 μm channel) pentacene TFT sensor to detect the saturated vapor of 1-pentanol, where the envelope of the AC variation exhibits a similar shape to the sensing curve measured at a DC bias as shown in Fig. 6.7. Therefore the AC variation is able to perform the same function of sensing response as a DC transient measurement does. However AC method has other functions which DC measurements cannot achieve.

DC measurements on transistor can only provide the amplitude of change in drain current. However, even with high sensitivity, this method is inefficient to identify the analyte triggering the sensing event. This is because an analyte with weak interaction to the organic semiconductor layer, in high concentration, can change the current as much as an analyte with strong interaction in mild concentration. This makes pattern recognition by DC method difficult and requires large array of individual sensors. In AC sensing measurement of organic transistors, the output signals are not only amplitudes, but also phases of the response in drain currents, dependent on frequency and gate voltages. By observing this kind of multi-dimensional (amplitude, phase, frequency, gate-voltage) spectrum, we will be able to use the same organic transistor to pattern-recognize the various analytes present in a mixture [58-59].

6.6.3 Other types of nanoscale chemical and biological sensors

The inorganic material LaFeO3 has been made into a nanocrystalline thin-film sensing layer, which acts as the gate of an ordinary n-channel Metal Oxide Semiconductor Field Effect Transistor, to detect alcohol type analytes with good sensitivity and selectivity [60]. This type of sensor utilizes the wealth of grain boundaries and high surface area in the film to enhance the sensitivity. Also, nanocrystals and metal nanoparticles have been used with optical methods to detect biological binding events [61]. However, due to the advantage of miniaturization and integration, electrical detection techniques have become increasingly in demand. Functionalized carbon nanotubes and semiconductor nanowires have been utilized to electrically detect chemical interactions and biological binding events [62-64]. Due to their quasi-one dimensional nature, nanotube and nanowire devices are very sensitive to small perturbations such as a change in conformation or charge state along the tube/wire[61]. With their small diameters and high surface-to-volume ratios, nanowire and nanotube devices have the potential to build sensors of small sizes, low power dissipation levels and high sensitivity. In particular, a nanoelectrode array based on vertically aligned multi-walled carbon nanotubes has been developed recently to offer enough stability and repeatability to deliver real commercialization [65]. Recently silicon nanowire field-effect transistors have been employed to selectively detect the binding and unbinding event of a single virus to an antibody-modified nanowire by the conductance change of the device [66].

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