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Impact of Interconnect Scaling on Electromigration and Stress Migration Reliability

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Impact of Interconnect Scaling on Electromigration and Stress Migration Reliability

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Dedication

To my family

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Impact of Interconnect Scaling on Electromigration and Stress Migration Reliability

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Interconnect scaling has given rise to serious reliability concerns under the impact of low k integration, new processes, and shrinking dimensions. This dissertation attempts to explore the scaling effects on the two main reliability issues in Cu metallization: electromigration (EM) and stress migration. The EM lifetime characteristics were studied on dual damascene Cu/low k interconnect structures for different low k dielectrics with scaling of the metal line width and barrier thickness. A Monte Carlo simulation was used to deduce the statistical parameters for intrinsic EM failures and extrinsic early failures. It was found that line width scaling, when accompanied by corresponding via size scaling, caused an almost linear decrease in the intrinsic EM lifetime, indicating the presence of a critical failure void volume, which depends on line geometry of the cathode end. FIB/SEM and TEM analyses revealed that copper out-diffusion due to defective barrier coverage caused lifetime degradation and line shorting. The threshold current density-length $(jL)_c$ product was also studied on test structures with three different barrier

thicknesses, in both electron flow directions, and processed with different processes. A 3-D Finite Element Analysis (FEA) was employed to investigate the confinement effect through examining the effective bulk modulus B. The change from oxide to low k dielectrics considerably reduced B as well as the $(jL)_c$ values. However, unlike the effective bulk modulus B, which scaled with the barrier thickness, the $(jL)_c$ product did not demonstrate a clear trend. This can be attributed to the decreasing experimental accuracy with a much reduced $(jL)_c$ value and the small difference in the actual confinement due to the barrier thickness variation. Any process-related void formation at an unfavorable location can also significantly reduce the critical failure void volume and the $(jL)_c$ values. Stress migration measurement was performed on Kelvin structures with different underlying metal-1 layer thicknesses and different Cu electroplating chemistries. A lower impurity level or a thinner metal layer thickness was found to degrade the stress migration performance. Microstructural characterization, thermal stress measurement, and 3-D FEA modeling were performed to interpret the observed stress migration results. And a possible failure mechanism was proposed.

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Chapter 1: Introduction

The interconnect signal delay, otherwise known as the resistance-capacitance (RC) delay, represents a major performance bottleneck in the semiconductor industry's relentless quest for an increasingly fast chip speed. This problem was first reviewed in Bohr's paper in 1995 [1]. Ever since then, copper metallization has been accepted over aluminum-based metallization as the most effective means to overcome such signal latency. Besides, new interlayer dielectric (ILD) materials have also been implemented with a dielectric constant much lower than that of silicon dioxide used conventionally (Figure 1.1). This has enabled further reduction of the RC delay and cross talk in the interconnects. The adoption of Cu as the new conducting material and the gradual integration of low dielectric constant (low k) materials are well documented in the various editions, revisions, and updates of the international technology roadmap for semiconductors (ITRS) [2].

However, Cu/low k integration has brought severe yield and reliability concerns. Among these concerns, some are natural for a new integration scheme still on its learning curve in dealing with new materials, new processes, and rapidly shrinking dimensions. Over time, researchers and engineers may come up with better solutions. Some other concerns are inherently more difficult to deal with, such as the weak mechanical properties of low dielectric constant materials and the scaling effect of the ever-shrinking dimensions. Therefore, the primary task for research and development efforts in back-end-of-line (BEOL) is to work out a reliable integration scheme with better performance. Up until now, reliability has seldom been given such attention in all the BEOL areas, from design considerations, process development, to materials selection. As we move

from one technology node to the next, the reliability of the integration schemes has to be carefully examined and constantly re-evaluated.

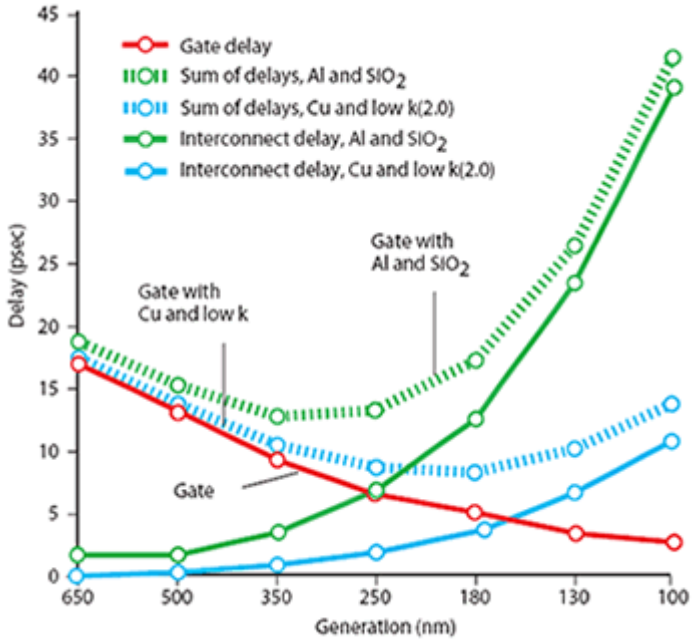


Figure 1.1: RC delays caused by the gate and the interconnects as a function of feature size. Both Al/SiO_2 and Cu/low k interconnects are presented. Courtesy of Laura Peters, Semiconductor International, 1998.

Among many reliability concerns in Cu/low k integration, electromigration (EM) and stress migration (SM) represent two key issues concerning the conducting Cu wires [3-7]. EM failures are circuit opens or shorts caused by Cu mass transport induced by the momentum transfer to metal ions from electrons carrying an electric current [8-9]. Stress migration failures are circuit opens caused by Cu mass transport induced in a stress relaxation process [10-11]. These two reliability issues in Cu metallization will be investigated in this study.

1.01 REVIEW OF ELECTROMIGRATION IN CU METALLIZATION

Electromigration was first observed in molten alloys of lead-tin and mercury-sodium by Geradin in 1861 [8]. It is a diffusion-controlled mass transport phenomenon in metallic materials under the influence of an applied electric field. The moving metal ions are subjected to two forces: the direct force from the external electric field, and the electron wind force as a result of the momentum exchange from collisions with electrons [12]. Since the electron wind force usually plays a more dominant role, the metal ions in effect travel in the direction of the electron flow (Figure 1.2).

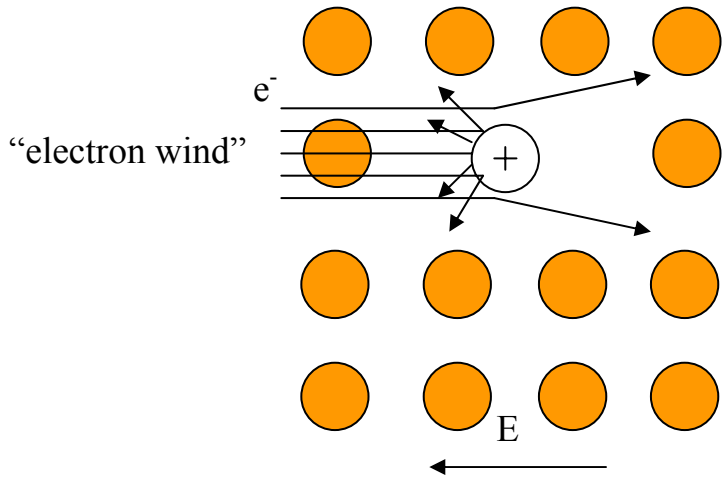


Figure 1.2: The driving forces for electromigration: the direct force from the external electric field and the electron wind force from the momentum exchange from collisions between metal ions and electrons.

The atomic flux J and drift velocity v_d of the moving ions in a metal line can be expressed as

$$J = nv_d \tag{1.1}$$

and

$$v_d = \left(\frac{D_{eff}}{kT} \right) Z^*_{eff} e \rho j \tag{1.2}$$

where n is the atomic density, D_{eff} is the effective diffusivity which represents a weighted sum of the atomic diffusivities of all the diffusion pathways, k is the Boltzmann constant, T is the absolute temperature, Z^*_{eff} is the effective charge number, which is neither a charge nor a valence number but rather a description of the momentum transfer rate, e is the electronic charge, ρ is the resistivity, and j is the current density. It is worth noting that $Z^*_{eff} e \rho j$ represents the electron wind driving force.

In the case of a confined metal line, as in the interconnect structures, the metal atoms diffuse from the cathode end to the anode end, resulting in a tensile stress at the cathode end and a compressive stress at the anode end, and eventually generating a backflow stress gradient. This backflow stress gradient provides a passive resistance against the diffusion driven by the electron flow [13]. Thus, combining both the EM driving force and the backflow stress effects, we have a net drift velocity v_d

$$v_d = \left(\frac{D_{eff}}{kT} \right) \left(Z^*_{eff} e \rho j - \Omega \frac{\partial \sigma}{\partial x} \right) \tag{1.3}$$

where Ω is the atomic volume, $\partial\sigma/\partial x$ is the stress gradient buildup along the line, and $\Omega(\partial\sigma/\partial x)$ is the compensating backflow stress gradient resulting from the mass accumulation at the anode end. The effective diffusivity D_{eff} for an interconnect line with a width w and a thickness h is given by [14]:

$$D_{eff} = D_b + \sum_j^n D_{gb,j}\left(\frac{\delta_{gb,j}}{d}\right) + D_i\left[2\delta_i\left(\frac{1}{w}+\frac{1}{h}\right)\right] + D_p\rho_{disl}d^2 \qquad (1.4)$$

where D_b, D_{gb}, $D_{i,}$ and D_p are the diffusion coefficients of the bulk, grain boundary, interface, and dislocation, respectively, d is the average or median grain size, δ_{gb} and δ_i are the effective thicknesses of the grain boundaries and the interfaces, and ρ_{disl} is the dislocation density. At device operation temperatures, the diffusion contributions from the bulk and the pipe can be assumed to be negligible. The main contributions are primarily from the interfaces and the grain boundaries.

The EM-induced atomic flux by itself does not necessarily create voids or extrusions in the interconnect lines as long as a region with depleting out-diffusion of metal atoms is constantly replenished with atoms coming from the upstream. EM damages only occur at sites of flux divergence, where the local net flux of atoms is not zero. Unfortunately, the multilevel metallization scheme in the ultra-large-scale-integrated circuits (ULSI) has provided abundant locations of flux divergence, e.g. the triple points of grain boundaries and the interfaces between dissimilar materials, as can be seen schematically in Figure 1.3 for Al- and Cu-based interconnect structures.

The presence of EM as a major interconnect reliability concern was first noticed by the semiconductor industry in 1966 when it was identified as the root cause for the failures in Al interconnects [15]. The threat posed by EM reliability to chip performance stimulated enormous interest in understanding the reliability physics involved and exploring solutions to control the EM failures. It was soon discovered that the grain boundaries abundantly present in the polycrystalline Al lines provided the fastest diffusion pathway. In the early 1970's, three main approaches started to be adopted for reliability enhancement against EM in Al lines [16-18]. These approaches included the

optimization of the microstructures to form a bamboo structure to reduce mass transport through grain boundaries in the current direction, the introduction of Al alloys with a small amount of Cu (~0.5 at. %) to slow down the diffusion of Al along the grain boundaries, and the incorporation of refractory overlayer and underlayer which sandwich the Al wires and act as shunting layers to carry the current when the Al metal is depleted (Figure 1.3 (a)). All these improvements helped reduce EM failures in Al-based interconnects, and longer lifetimes were achieved.

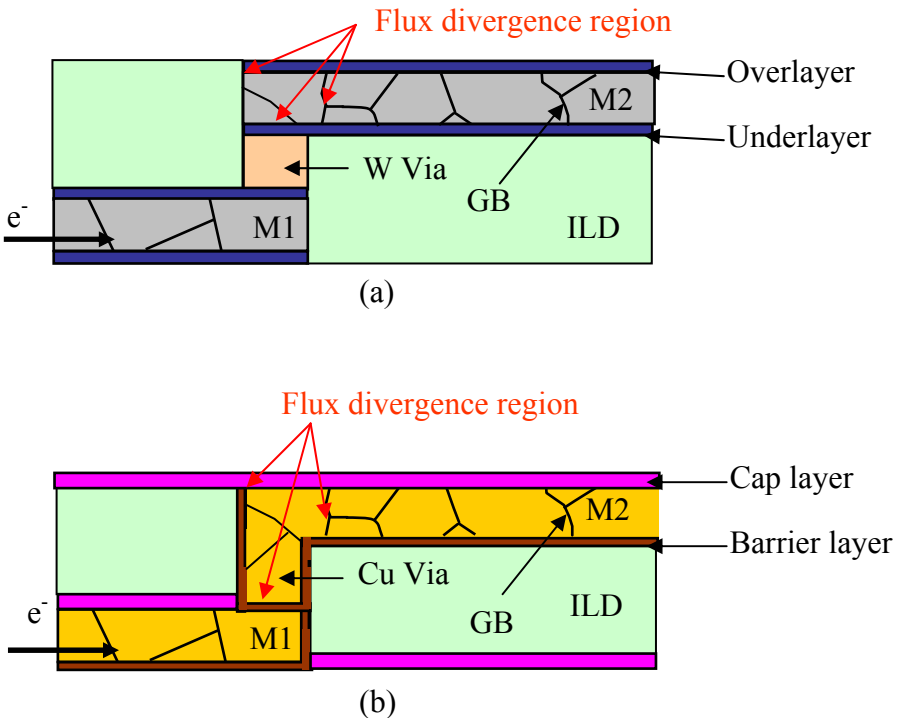


Figure 1.3: Schematic of (a) Al-based interconnects vs. (b) Cu dual damascene interconnects.

However, the continual increase in the maximum current density J_{max} as required for better chip performance and the resulting increase in RC delay eventually justified the introduction of the more expensive Cu as a better conductor, and initiated the revolutionary move to Cu/low k interconnect structures in the industry.

The shift from Al to Cu immediately brought major performance enhancement. As indicated by its higher melting point of 1083°C than that of Al (660°C) [19-20], Cu demonstrated lower diffusivities than Al through lattice, grain boundaries, and interfaces at the same operation temperature (~100°C). Consequently, Cu wires offered an appreciably higher EM resistance than Al.

Unfortunately, new reliability complications were observed in Cu metallization as a result of the introduction of new patterning processes and new surrounding materials. First, Cu lines cannot be patterned with the conventional subtractive patterning approach used for Al, since reactive ion etch (RIE) is not practical due to the lack of volatile Cu compounds at low temperatures [21]. Besides, unlike Al, which has a very dense and stable Al_2O_3 layer that can provide self-passivation and prevent Al from diffusing into the dielectric, Cu oxidizes easily and its loose oxide layer has little passivation effect. Moreover, Cu diffuses easily into SiO_2 dielectric as well as the silicon substrate, leading to device degradation. As a result, Cu wires have to be encapsulated completely with barrier materials and to be insulated from the surrounding dielectric materials. To address these problems, a damascene or gap-filling patterning process has been developed [22-24].

The damascene process is characterized by a processing flow sequence that starts with the deposition of the dielectric stack (Figure 1.4). Via holes and/or trench structures are then opened in the dielectric stack. Next, a conductive diffusion barrier (Ta or TaN) and a Cu seed layer are deposited with a physical vapor deposition (PVD) process. The

trenches and the vias are then filled from bottom up with Cu using an electroplating (EP) or electrochemical deposition (ECD) technique. After the post-Cu-deposition anneal to stabilize the microstructure, a chemical mechanical polishing (CMP) is performed to remove the Cu overburden and the excess barrier layer at the top surface, followed by a dielectric cap layer deposition (SiN_x or SiC_yN_x) so that the subsequent interconnect layers can be built afterwards.

There are two variations of this process: the single damascene (Figure 1.4(a)) and the dual damascene (Figure 1.4(b)). In a single damascene process, the trench and the via are patterned in separate steps; while in a dual damascene process, the trench and the via are filled in one single metal deposition step.

With new interfaces with encapsulating barrier materials, Cu diffusion pathways in the damascene structure now include the bulk, the metal/barrier layer interface, the metal/cap layer interface, and the grain boundaries (Figure 1.3(b)). Because of the weak bonding between the CMP-polished Cu surface and the capping dielectric layer, the Cu/cap layer interface typically provides a faster diffusion pathway than any other component. Extensive studies in the industry and academia have also identified the Cu/cap interface diffusion as the dominant diffusion mechanism affecting EM mass transport [25-28]. Recently, a novel electroless plating of a thin metal overcoating, such as CoWP, Ta, and Al(Cu) alloy, on CMP-polished Cu prior to the deposition of the dielectric cap was proposed as an effective method to strengthen the Cu/cap interface. It was reported that the EM lifetime for Cu interconnects with such strengthened cap interfaces was extended 10-100 times [29-34].

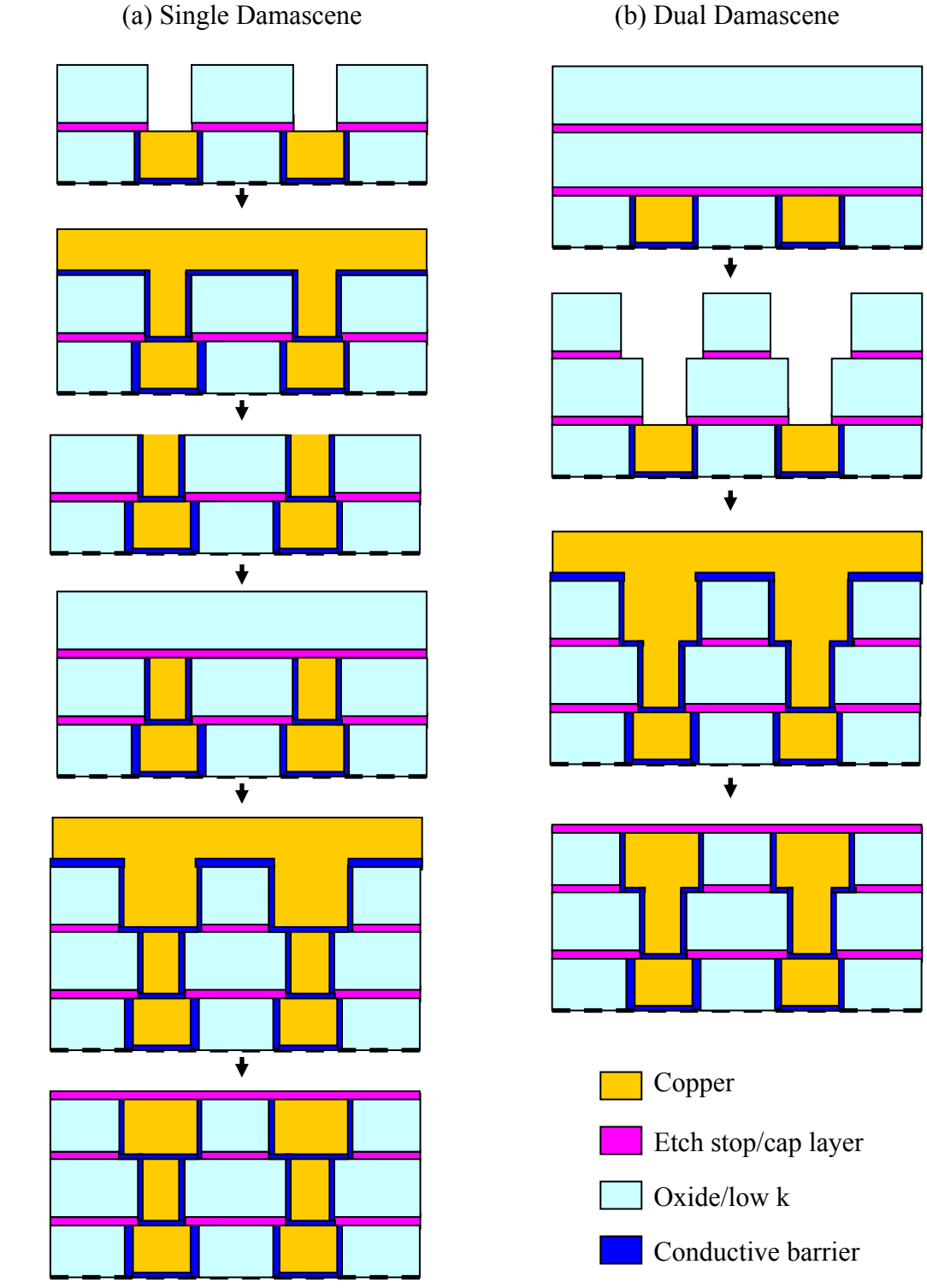


Figure 1.4: Basic process flows for Cu damascene interconnects.

As a more economical patterning process, the dual damascene process produces interconnect structures with continuous trench and via metal material at each metal level, which gives rise to a new EM sensitivity to the via process. Since the Cu via is part of a continuous body of Cu metal without any boundary to the upper level trench metal, EM-induced voiding can start from the via bottom and/or the cathode end trench edge, both of which are flux divergence sites for the mass transport. Sometimes EM-induced extrusions can occur at the anode sites where there is a net accumulation of atoms [35]. Further, difficulties in the via profile control and the barrier deposition processes may create severe barrier integrity issues, especially when porous low k dielectrics are integrated. Defective barrier coverage at the via bottom may provide void nucleation sites as a result of EM mass transport, and reduce the EM lifetime. Such an extrinsic failure mechanism induced by process-related defects represents an early failure mode. A multimodal failure distribution of the Cu EM characteristics is therefore expected, as shown in Figure 1.5 [36-39].

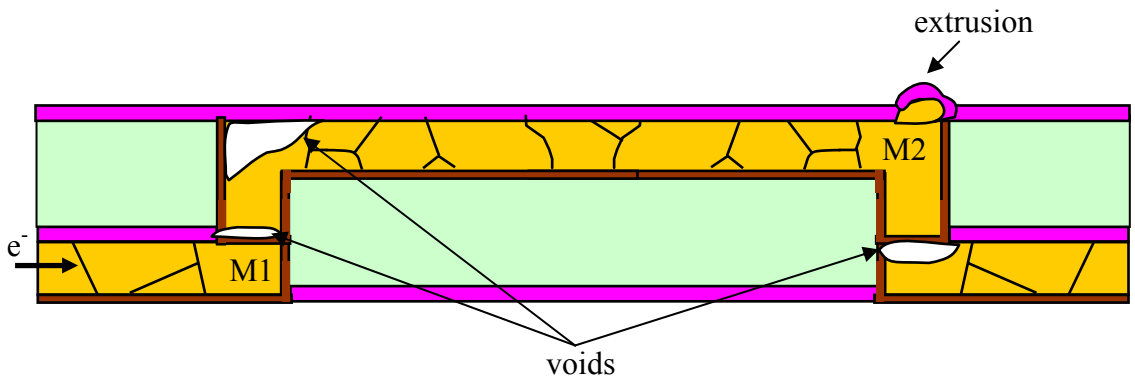


Figure 1.5: Damage formation in Cu dual damascene interconnects.

Apart from the lifetime statistics, another EM reliability parameter, the threshold current density-line length product $(jL)_c$, has also attracted much attention [40-43]. This threshold value is related to the maximum current density allowed in an interconnect structure, J_{max}, which can be used as a design guideline. For a given current density j, the $(jL)_c$ value manifests itself in the presence of a critical length effect, i.e. the Blech length effect [13]. Specifically, as Cu atoms deplete from the cathode end and accumulate at the anode end, the backflow stress gradient in the lines shorter than a critical length may be sufficient to resist EM mass transport. Under such circumstances, voids reach a state of saturation and do not grow any more. An empirical expression can be deduced from Eq. 1.3

$$(jL)_c = \frac{\Omega \cdot \Delta\sigma}{Z^*_{eff} e \rho} \tag{1.5}$$

where $\Delta\sigma$ is the maximum stress difference in a metal line when failure occurs according to a given failure criterion. The maximum tolerable backflow stress depends on the mechanical strength of the conducting metal, the surrounding barriers, and dielectrics in confining the mass accumulation at the anode end [6]. Assuming that there is an identical amount of mass transport and that the surrounding interfaces remain intact, the higher mechanical strength of Cu intrinsically can tolerate higher stress than that of Al, resulting in a greater $(jL)_c$ value. Nevertheless, the fact that the thin barrier layer in Cu interconnects cannot serve as a reliable current shunting layer makes the Cu lines less tolerant against Cu depletion, and the situation becomes worse with the continual scaling of the barrier thickness. Consequently, a small amount of Cu mass transport can easily fail a line before the void growth reaches a saturation point. Process-related barrier defects and interface imperfections at the anode end may introduce further uncertainties

by inducing anode end ruptures. Even without any defective interfaces, the maximum stress that can build up at the anode end is still affected by the confinement of the barriers and the ILD materials. This confinement effect has stimulated considerable interest in studying the role of the Cu barriers in strengthening the Cu/low k interconnect structures [44-45].

1.02 REVIEW OF STRESS MIGRATION IN CU METALLIZATION

Stress migration, otherwise known as stress-induced voiding, is also an important reliability issue in Cu metallization. It is caused by vacancy diffusion and subsequent void formation driven by the residual thermal stress gradient in the interconnect structure. The stress and its gradient are induced as a result of the mismatch of thermal expansion coefficients (CTE) of the metal, the barrier layer, the cap layer, and the surrounding dielectric materials. Various processing steps and the different processing temperatures can also induce a thermal stress/stress gradient in the interconnects [3, 5]. When a void reaches a critical failure volume, the interconnect line fails because of either an unacceptably high resistance or an open circuit. An example of void formation under stress migration is shown in Figure 1.5 with a small via placed over a wider metal lead [10]. Unlike EM, stress migration does not have a constant driving force. Therefore, it is more of an early lifetime reliability concern rather than a steady state or wear-out reliability issue.

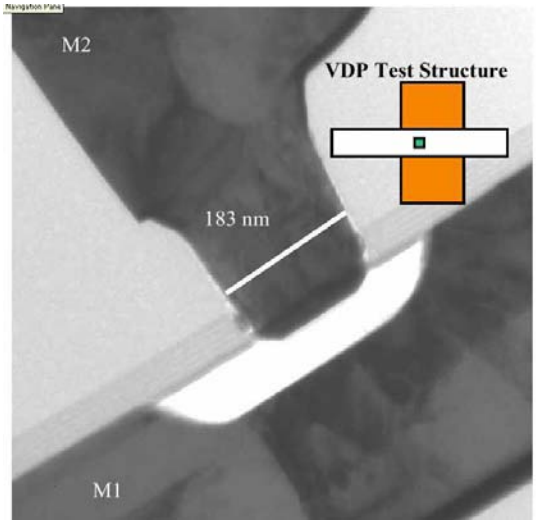


Figure 1.6: Void-formation under a small via placed over a wide Cu metal lead. The M1 lead is about 3μm wide. The void was formed after baking for over 100h at 150°C.

In general, stress migration is caused by the interactions between the thermomechanical stress in the interconnect systems and the diffusion of vacancies. The presence of these two factors gives stress migration an interesting dependence on temperature. Unlike EM, which deteriorates monotonically with the increase of temperature, the temperature dependence curve for stress migration is bell-shaped, peaking at an intermediate temperature range. This can be explained by the fact that the residual tensile stress in the interconnect structure decreases almost linearly with the temperature, and that the vacancy diffusion has an Arrhenius temperature dependence, increasing exponentially with the temperature. McPherson and Dunn [11] have developed an empirical model of stress migration kinetics as follows:

$$R = C(T_0 - T)^N \exp\left(\frac{-Q}{k_B T}\right) \tag{1.6}$$

where R is the creep rate, T_0 is the stress-free temperature where the stress changes from tensile to compressive, T is the testing temperature, N is the creep exponent, Q is the activation energy, k_B is the Boltzman constant, and C is a constant. A plot obtained from Eq. 1.6 is presented in Figure 1.7 [10]. These data were derived from a series of bake tests performed on a single via dual damascene Cu test structure with a fluorinated silicate glass (FSG) low k dielectric. The stress voiding data are then fitted using the following parameters: $N \cong 3.2$, $Q \cong 0.74$eV, and $T_0 \cong 270^{o}$C. The maximum creep/void growth rate is found at an intermediate temperature ~200°C.

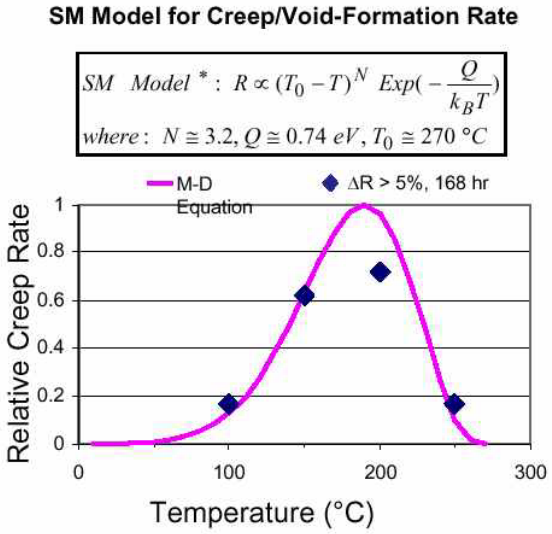


Figure 1.7: McPherson and Dunn's creep rate model for stress migration.

Stress migration in Cu interconnects did not receive adequate attention at first because Cu has some desirable properties to reduce stress-induced voiding, such as lower mobility and similar intrinsic stress compared with Al [10]. However, studies later showed that the problem of stress migration in Cu interconnects is more complicated than expected because it is highly structure- and process-dependent.

The sensitivity of the stress migration to the geometric design can be represented based on the concept of the active diffusion volume as proposed by Ogawa et al. [10]. This volume is a region where the interconnect volume, the diffusion mechanism volume, and the stress gradient region coexist. The interconnect volume is defined by the physical dimensions of the structure within which voiding occurs; the diffusion volume is the area that supplies vacancies for voiding; and the stress gradient region is the area where there is sufficient driving force compelling the vacancies toward a voiding site. Only those vacancies within this volume can contribute to the voiding process. This concept can be used to explain the observations that the structures most sensitive to stress migration are those where single vias are connected to wide metal lines. This is because wide lines provide sufficient sources for vacancies and such a via-to-line layout lends itself to large stress gradients. In contrast, the scaling of the line width for the contact metal line does not lead to increased stress migration vulnerability due to the small interconnect volume and the lack of a large stress gradient. The observations mentioned above are also supported by some studies [46-47] using a wide range of interconnect geometries.

While geometric designs may make some structures more prone to the impact of stress migration, processing conditions can be optimized to control the vacancy levels and stress gradients to reduce the susceptibility to stress migration. Ogawa et al. [10] reported that the stress migration failure rate can be reduced drastically with post-plating annealing due to increasing grain growth to reduce the vacancy concentration in the annealed Cu structure. Oshima et al. [48] demonstrated improved stress migration performance with the optimization of the pre-barrier clean process and the via profile. Alers et al. [49] discovered that resputtering Cu on via sidewalls due to sputter preclean is avoidable with a novel barrier-first via process. Such a change has considerably improved the via stress migration performance. Von Glasow et al. [50] studied the correlation

between the stress migration behavior and the SiN_x cap layer deposition process. They found that pretreatment of Cu with high plasma intensity, although providing good interface adhesion, does damage to the bulk Cu material. Such damage leads to crystal defects that facilitate vacancy generation, and the stress migration performance is compromised accordingly. To conclude, process optimization should remain a top priority in order to minimize available vacancies, reduce the driving force (the stress gradient), or both.

1.03 RELIABILITY CHALLENGES RAISED BY INTERCONNECT SCALING

The past few years has witnessed the semiconductor industry advance from the sub-micron to the sub-100nm technology. The 65nm technology has already been moved from research to development (Figure 1.8), and the 45nm technology and beyond are being studied enthusiastically. To meet the requirements for constant device scaling, new materials, processes, and integration schemes are continually under development. These changes have also introduced a variety of reliability concerns that need to be addressed in the meantime.

As the metal line width and the barrier thickness decrease aggressively (Figure 1.9), the required current density J_{max} increases considerably (Figure 1.10). Further, with more metal levels designed for each technology node (Figure 1.11), a lower failure rate per metal line is necessary in order to maintain a constant chip-level failure rate at a tolerance level. Such a challenge is further complicated with the introduction of new materials and new processes and the limitation imposed by the economical considerations. Consequently, the reliability targets for Cu/low k interconnects are becoming more and more difficult to achieve.

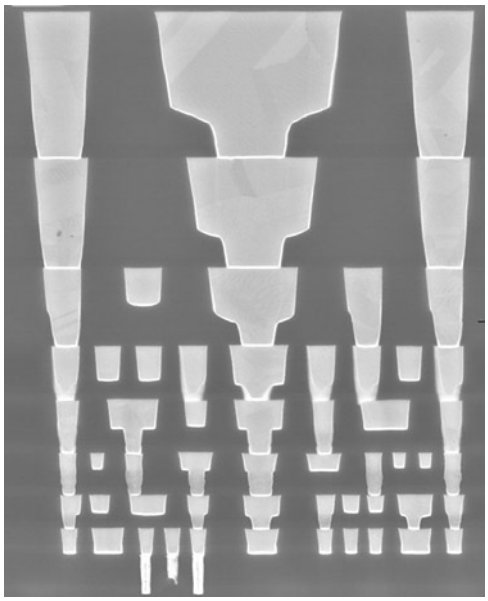


Figure 1.8: Fully integrated 8-level dual-damascene Cu/low k interconnects (k = 2.9) for 65nm technology node (IEDM 2004 Intel [51]).

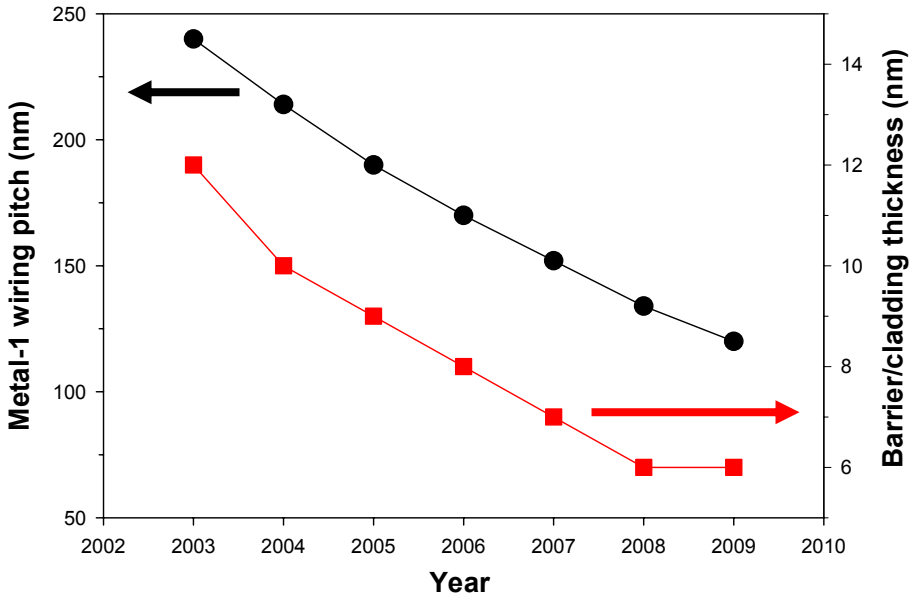


Figure 1.9: Scaling requirements for metal-1 pitch size and barrier thickness as depicted by the International Technology Roadmap for Semiconductors, 2004 update [2].

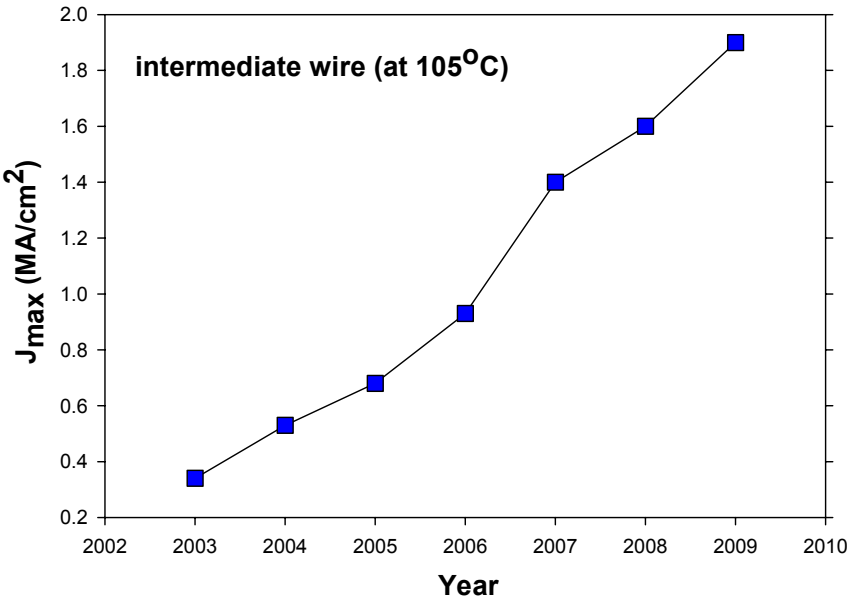


Figure 1.10: The required current density at operation conditions continues to increase as depicted by the International Technology Roadmap for Semiconductors, 2004 update [2].

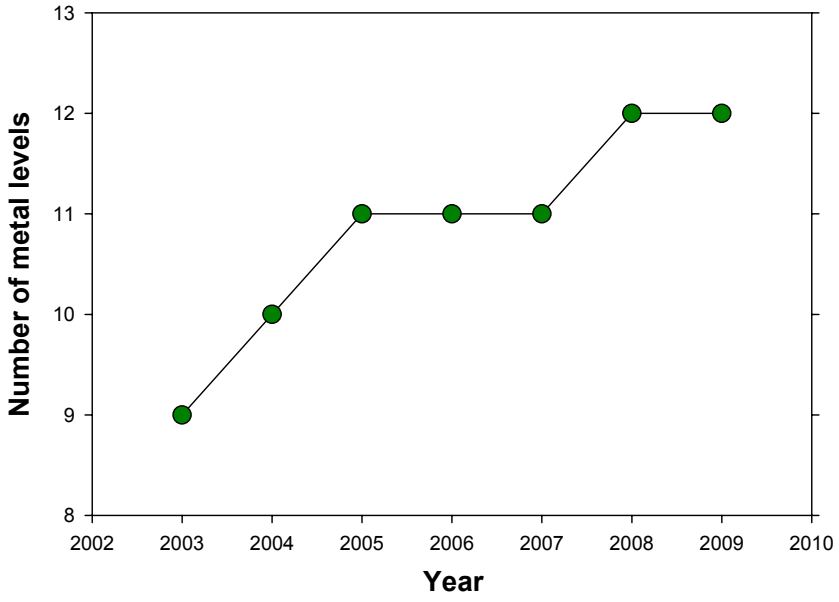


Figure 1.11: The number of metal levels for each technology node as depicted by the International Technology Roadmap for Semiconductors, 2004 update [2].

A comprehensive understanding of the impact of low k and ultra low k integration on the EM and SM reliability is very important for the lifetime distribution prediction for the future technology nodes. The dielectric constant k value is usually lowered through 1) the introduction of chemical bonds such as the Si-C and C-H bonds that have lower polarizability than the Si-O bonds of the traditionally used SiO_2-based ILD material, and 2) the reduction of the bond density through the introduction of porosity or certain molecular reorganization to generate free volume [52-53]. However, both approaches degrade the thermal and mechanical properties of the materials as the less polarizable bonds are generally weaker in bond strength. Low k materials typically have a much lower mechanical hardness, elastic modulus, and thermal conductivity compared with oxide. Moreover, they adhere poorly to the adjacent metal barriers and the etch stop layers. Therefore, the integration of low k materials is a difficult task and its reliability remains a serious concern.

Electrically, with the adoption of low k materials, especially porous low k materials, time-dependent dielectric breakdown and line-to-line leakage have become an increasingly important issue [54]. This is because low k materials typically have weaker dielectric strength compared with oxide. In addition, process-related defects or contamination of the dielectric surface can considerably lower the breakdown field. Furthermore, the difficulty to deposit a thin yet high-quality barrier layer on the porous low k materials can lead to poor barrier coverage, which may in turn cause Cu out-diffusion and line-to-line leakage.

Mechanically, the low k and porous low k dielectrics are soft and weak. Such properties make them highly susceptible to CMP and plasma damages, which may cause feature distortion, interface defects, and even delamination and cracking. Additionally, it is very difficult to achieve good etch profile control and conformal metal coverage on

these dielectric materials. Process-related defects therefore are readily introduced, especially on the sidewall and at the via bottom. As a result, electromigration and stress migration become major reliability concerns. For example, degradation of the lifetime statistics, much reduced critical length, and large scatter in the lifetime distribution have been observed in Cu interconnect structures with various porous low k dielectrics [55-57].

1.04 SCOPE OF WORK

The scaling effect on EM lifetime statistics in Cu dual damascene interconnect structures is the main focus of this study. The influence of the different scaling geometries, low k dielectric materials, and process flows is to be examined. The intrinsic reliability behaviors need to be distinguished from the process-induced extrinsic effects, and the underlying reliability physics that governs the presence and/or absence of the scaling trends in their corresponding lifetime statistics is to be studied.

The impact of scaling on the EM threshold, or the critical current density-length *(jL)c* product, represents another major point of interest. In Cu interconnects, voids typically nucleate readily at the Cu/cap layer interface. Besides, unlike Al-based interconnects, the thin barrier layers usually cannot serve as stable shunting layers in case of voiding. Moreover, with the introduction of the low k materials, the backflow stress is further reduced. All these differences make the impact of scaling on the EM threshold a rather complicated issue. In this study, the EM threshold is to be examined in terms of barrier thickness scaling, various structures, and different processes of Cu/low k interconnect structures, with a view to a better understanding on the nature of this threshold and its controlling parameters.

Another issue examined in this work is stress migration. Alterations in materials, structures, or processes involved in scaling may lead to the increase of the vacancy density and/or stress gradient and in turn degrade the stress migration performance of the interconnect structures. A good understanding of Cu stress migration reliability issues cannot be achieved without a careful analysis of the residual stress. In this study, the impact of Cu electroplating process and interconnect geometry on stress migration is to be investigated. And the results are to be interpreted with the help of a 3-D stress simulation.

This dissertation is arranged as follows.

Chapter 2 describes the experimental setup, test structures, data analysis approaches, and failure analysis methodologies.

Chapter 3 focuses on the scaling effects on the EM lifetime characteristics. There were two sets of test structures examined. The first set consisted of structures with a dense Methylsilsesquioxane (MSQ) low k material and three different metal line widths, 0.5μm, 0.25μm, and 0.175μm. And the second set consisted of structures with a porous MSQ low k material and three different nominal barrier thicknesses, 175Å, 100Å, and 75Å. Two electron flow directions were studied as well. Based on the experimental results, a Monte Carlo Simulation was used to deduce the statistical parameters for intrinsic EM failures and extrinsic early failures. Focused Ion Beam (FIB)/Scanning Electron Microscope (SEM) and Transmission Electron Microscope (TEM) were employed to locate the failure sites and further clarify the failure mechanisms.

Chapter 4 examines another important characteristic parameter for EM reliability, the threshold current density-length $(jL)_c$ product. Void formation in structures with different barrier thicknesses, different electron flow directions, and different processes was examined using FIB microprobe. The threshold value was related to a maximum

backflow stress gradient established in the Cu wires as a result of the EM mass transport. Evaluation of the maximum backflow stress gradient was made by applying the concept of an effective bulk modulus B to describe the confinement effect of Cu wires by the surrounding materials. A 3-D Finite Element Analysis (FEA) was then employed to calculate the modulus B. The discrepancy between the theoretical prediction and the experimental observation was discussed for a better understanding of the confinement effect from the ILD materials and the barrier layers.

Chapter 5 addresses how the structural scaling and the modification of material properties associated with new processes may affect stress migration behavior. Stress migration measurement was performed on structures with three different metal 1 layer thicknesses and with three different Cu electroplating chemistries. Microstructural characterization, thermal stress measurement, and 3-D FEA modeling were performed to interpret the observed stress migration results.

And finally, Chapter 6 presents a summary of the study and proposes some new directions for future work.

Chapter 2: Electromigration Experimental Procedure and Data Analysis

2.01 OVERVIEW

It is impractical to assess the EM reliability under normal operation conditions (i.e. 100°C) due to the extremely long time that such tests would typically take. Therefore, a more realistic accelerated lifetime testing is usually conducted at a high temperature under a high current density. The testing results can then be extrapolated back to the normal operation conditions. The basis for such extrapolation is Black's empirical equation, which is used to calculate the median time to failure, or the 50th percentile failure time of a failure population, t_{50} [58]

$$t_{50} = Aj^{-n} \exp\left(\frac{Q}{kT}\right) \tag{2.1}$$

where A is an empirically determined constant, j is the current density, n is the current density exponent, typically ranging between 1 and 2, and Q is the activation energy. The Q value is indicative of the dominant mass transport diffusion path. Specifically, in Cu-based interconnects, Q usually ranges between 0.7 and 1.0 eV for the interface diffusion, is about 1.2 eV for the grain boundary diffusion, and is 2.3 eV for the bulk Cu lattice diffusion [9].

The EM testing method that was adopted in this study is a conventional package-level test. When a DC current is applied to an interconnect structure, the resistance changes (ΔR) are measured as a function of time. And the failure lifetime distribution

curve is determined based on a certain failure criterion using an ensemble of nominally identical test structures.

In order to study the EM failure statistics and the $(jL)_c$ product, two types of statistical multi-link line/via test structures are employed. Such structures not only enable us to identify the multimodal EM failures with a specially-designed test ensemble, but also save considerable testing time as compared with the traditional single-link EM test structures.

In this chapter, a general EM testing procedure is first provided, from the test structure design to the physical failure analysis. Next, the EM testing system and the system configurations are described in detail. A description of the statistical test structures is then provided, followed by the corresponding data analysis approaches along with their statistical background. The resistance characteristics are then presented for two basic EM-induced damage modes: voiding and open circuit, and extrusion and short circuit. Finally, the failure analysis methodology with dual beam FIB/SEM and the various EM failure sites are provided.

Figure 2.1 illustrates the process flow for the EM studies.

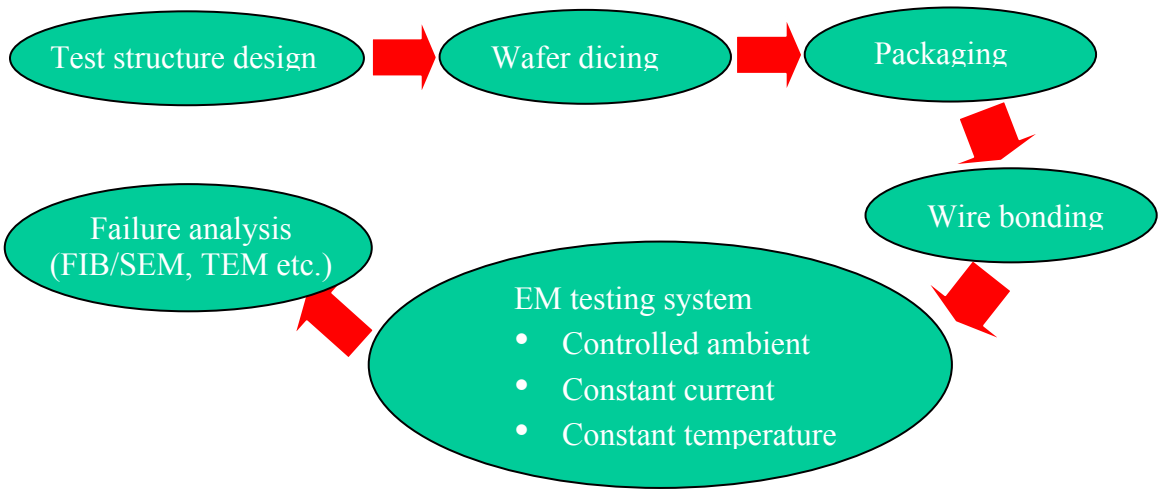


Figure 2.1: A flow chart of a typical EM experiment.

2.02 EM EXPERIMENTAL PROCEDURES

All the Cu/low k EM test structures used in this study were designed at UT-Austin and fabricated at LSI Logic and Sematech, and all the Cu/oxide test structures used in this study were obtained from Novellus Systems.

Upon receiving the test chips, they were diced with a Kulicke and Soffa model 982-10 Precision Dicing System. The selected test structures were packaged in a 16-pin dual-in-line ceramic package (DIP) with a QMI 3555 Ag/Glass die-attach paste, and then cured in a vacuumed oven at 350°C for 45 minutes. Next they were wire-bonded to the ceramic package with a Kulicke and Soffa model 4123 Wedge Bonder. After that, the pin-to-pin resistance of all the structures was measured, and they were inspected under the optical microscope to ensure that the wire bonding was properly performed. The structures were then loaded into the EM testing chamber and a small amount of current ($<10^{-5}$A) was applied to each test structure. Both the passing current and the resultant voltage were measured for individual test structures to make sure that all the test channels were properly functioning. After that, the chamber was placed under vacuum (<10 mTorr) using a mechanical pump and then backfilled with 20 torr nitrogen or forming gas. This controlled testing ambient was used to prevent possible oxidation and low k degradation.

The next step was the temperature ramping to the target testing temperature. During this process, the temperature coefficient of resistivity (TCR) was measured by applying a low current ($<10^{-5}$A) to the test structures. The temperature ramping was performed in steps of 50°C at a rate of 2°C/min, and the resistance of each test structure was recorded at each temperature step. The relationship between the resistance and the temperature was given by the following linear approximation [59]:

$$R \cong R_0\left[1+\alpha\left(T-T_0\right)\right] \tag{2.1}$$

where α is the TCR, R is the resistance at the testing temperature T, and R_0 is the resistance at a reference temperature T_0 (usually taken at room temperature). It was found that α was in the range of 0.0032/^{o}C to 0.0034/^{o}C for Cu/low k interconnect structures used in this study, slightly lower than the TCR of bulk Cu, which is 0.0039/^{o}C. The difference can be possibly attributed to the different microstructural properties in the confined interconnect lines.

Next, joule heating was measured to ensure that the actual temperature did not considerably exceed the target testing temperature and that no severe joule heating occurred during the EM test. At the target testing temperature T, the testing current was gradually ramped to the target current in steps. At each step, the resistance of each structure was recorded. The temperature change ΔT due to joule heating can be calculated by

$$\Delta T = \frac{R\left(T,i\right)-R\left(T,0\right)}{R\left(T,0\right)\alpha} \tag{2.3}$$

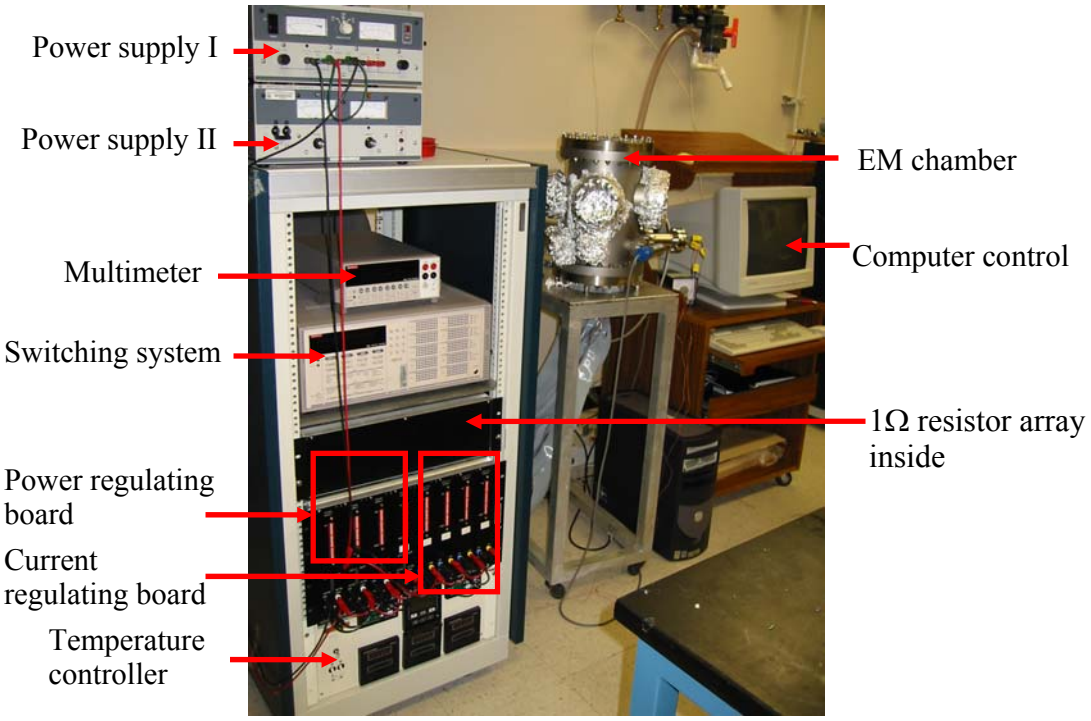
where *R(T, i)* is the actual resistance of each structure at current *i*, *R(T, 0)* is the baseline resistance at a very low current, and α is the measured TCR in the previous step. The average temperature increase due to joule heating was found to be less than 2°C in this study (normally the current density used $\leq$ 1MA/cm^2), so the temperature was not particularly corrected for. It is worth noting that although the measured average temperature increase was limited, local joule heating could be much higher once voids formed, which could potentially lead to severe damage and complicate the subsequent failure analysis.

The actual EM lifetime testing started when both the target testing temperature and current density were reached. The resistance traces and the failure times were automatically recorded. The EM experiment was terminated upon the failures of all the test structures.

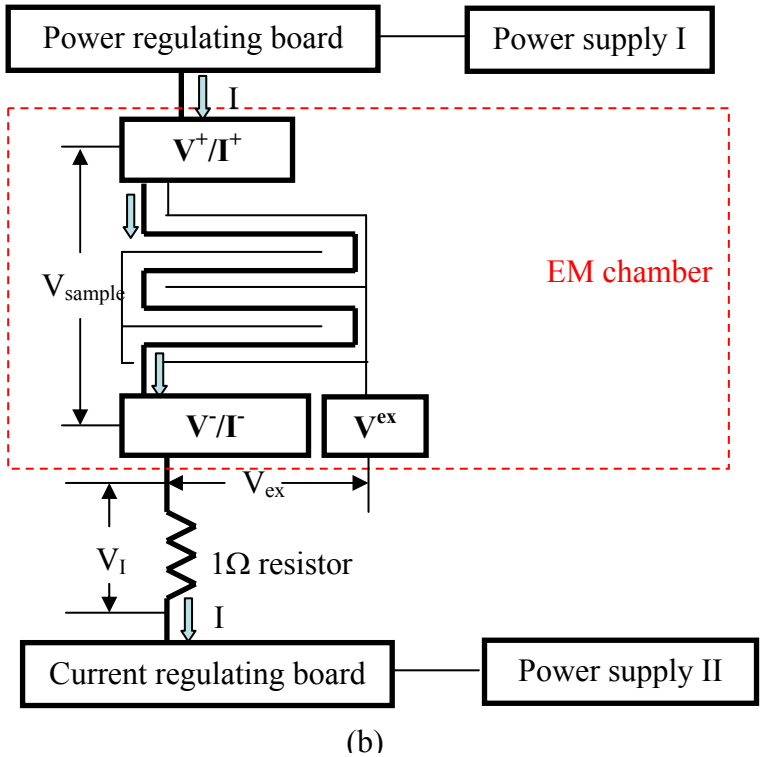
Some selected structures with distinct resistance traces and/or failure times were then analyzed using the FEI Strata™ DB235 dual beam FIB/SEM system, which simultaneously allows both the nanoscale cutting of the structures with FIB and the monitoring of the cutting progress with high resolution SEM imaging. The failure analysis can correlate the changes in resistance with the physical failure mechanisms in the interconnect lines.

2.03 CONFIGURATION OF THE EM TESTING SYSTEM

The basic setup of the EM testing system is shown in Figure 2.2. As part of the testing system, a high-vacuum EM test chamber that can host as many as 76 test structures simultaneously is used. A Keithley 7002 switching system is employed to switch between test structures, and a Keithley 2000 multimeter is used to measure the individual voltage drops across each test structure. The system compliance, ranging up to 80 V and 10 mA (power supplies I and II), was specially designed for testing highly resistive multi-link interconnect structures. The testing temperature ranges up to 450°C. The whole EM testing process is controlled through a computer with a LABVIEW program developed in our laboratory [60].



(a)



(b)

Figure 2.2: Experimental setup for EM testing.

For a given EM test structure, there are typically five terminals for current and voltage measurement (V^+, V^-, I^+, and I^- for the test lines and V^{ex} for the extrusion monitor lines adjacent to the test lines). During the course of testing, a constant current I is maintained through the test structure and the resultant voltage V_{sample} is continuously measured using a four-point probing method. The current in the circuit can be measured through the voltage drop across the 1Ω resistor since $I = V_I/R = V_I/1 = V_I$. Therefore, the resistance of the test structure can be calculated by

$$R_{sample} = V_{sample} / I = V_{sample} / V_I \tag{2.4}$$

In addition, any possible short circuit can be detected through measuring the voltage drop between the V^- and the V^{ex} channels. The V^{ex} is connected to the V^+ channel so that the maximum strength of the electric field between the test line and the extrusion monitor line is limited.

During the EM testing, there are two parameters that need to be precisely controlled: the testing temperature and the current density. Such control is necessary for EM lifetime extrapolation from the experiment conditions to the regular operation conditions.

In order to achieve adequate temperature control in the experiment, heating wires are deployed at the top and the bottom as well as the sidewalls of the chamber. Two sets of calibrated thermocouples are placed at both the center and the perimeter of the chamber to measure the ambient temperature and to provide feedback to the temperature controller.

The constant current condition is adjusted and maintained by a current regulating board, designed in our laboratory for this specific purpose. This board allows adjustment

and maintenance of current densities on an individual test structure basis; and there is minimal interference between the current channels for different test structures in the experiment.

As a result, our EM testing system offers effective regulation of both the experiment temperatures and the current densities. In effect, the maximum current fluctuation is limited to about 0.2%, and the temperature variation is within 1°C.

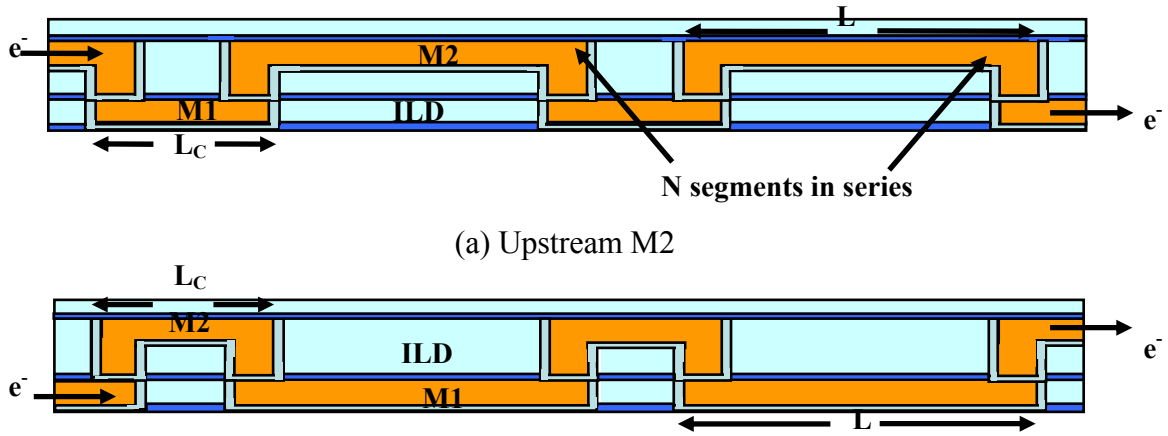
2.04 TEST STRUCTURE

2.04.1 Basic types

Figure 2.3 is a schematic diagram of the statistical multi-link line/via structures used in this study. In the upstream M2 structures (Figure 2.3(a)), the Cu test lines are on the M2 level, and the connecting lines on the M1 level are designed to be shorter than 5μm but very wide in order for the EM failures to occur only within the M2 test lines. Under this circumstance, the EM-induced damage occurs within either the via or the M2 trench at the cathode end. The downstream M1 structures (Figure 2.3(b)) are identical to the upstream M2 structures except that the narrow and long test lines terminating at dual damascene vias are on the M1 level. In this case, the cathode end of the M1 trench is the typical EM failure location. Therefore, a careful examination of both of these structures helps provide a good understanding on the EM damage formation process due to different geometrical designs.

To address different issues of EM reliability, such as the critical length effect, early failures, etc, variations of the two above-mentioned test structure types with different combinations of the test line lengths L and the test line segments N have been

designed. A brief description of different structures will be provided in the following sections.



(a) Upstream M2

(b) Downstream M1

Figure 2.3: Schematic diagram of two-level dual-damascene interconnect structures for EM testing: (a) Upstream M2-type test structure and (b) Downstream M1-type test structure.

2.04.2 Critical length (LC) structures

2.04.2.1 Test structure description

Under a given current density, because the backflow stress may suppress further EM mass transport, EM failures may only occur in lines longer than a certain threshold length. In other words, below a critical length, EM failures do not take place. Such a phenomenon is known as the critical length effect.

The critical length (LC) structure, whose schematic overview is provided in Figure 2.4, is specifically designed to investigate the critical length effect. It contains six identical sets of test lines, with each set comprising 14 test lines of different lengths (10,

15, 20, 25, 30, 35, 40, 45, 50, 75, 100, 150, 200, and 300μm). As a result, a total of 84 interconnects are serially connected with each other in one test structure. This structure enables us to directly observe the length-dependent EM damage formation, from which the critical length can be deduced.

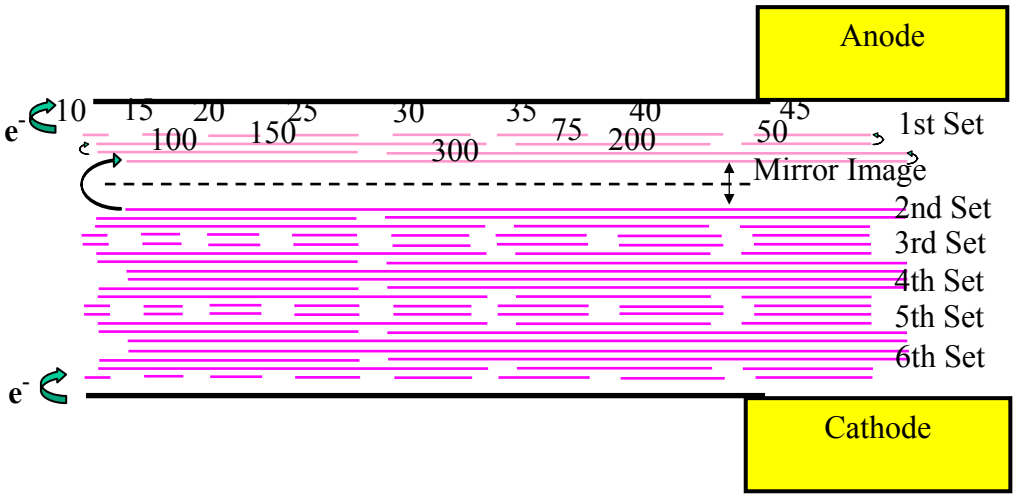


Figure 2.4: Schematic diagram of the LC module [60]. Six identical sets of test lines with various lengths are serially connected with one another. Both the upstream M2 and downstream M1 test structures are available for testing.

2.04.2.2 Length-dependent failure distribution

Based on the LC structure, a statistical approach is used to determine the critical length for a given current density [61]. As indicated by the 1-D drift equation (Eq. 1.3), for a given amount of testing time, the links of different lengths L in the LC structure experience a different amount of Cu ion drift, which is related to the strength of the backflow stress, which is in turn proportional to the reciprocal of the length $1/L$. The amount of drift is also related to the amount of EM damage formation. Consequently, the

EM failure probability $P(j, L_i)$ for a given line length L_i and current density j can be assumed to be proportional to its average drift rate $v_d(j, L_i)$ normalized to the drift rate $v_d(j, L_M)$ of the longest interconnect line L_M (300μm):

$$\frac{P(j,L_i)}{C_N} = \frac{v_d(j,L_i)}{v_d(j,L_M)} = \frac{1-L_c/L_i}{1-L_c/L_M}, \quad \text{for } L_i \geq L_c \qquad (2.5)$$

$$= 0, \qquad \text{for } L_i < L_c$$

where L_c is the critical length for EM failure, and C_N is a normalization constant. As an example, Figure 2.5 provides the regression fit based on the statistical approach analysis for the 0.5μm wide Cu/oxide dual damascene interconnects. There is a dramatic decrease in the failure probability at a certain cut-off point, where in this case the $(jL)_c$ product is roughly 3700A/cm. There is no distinct temperature dependence of the $(jL)_c$ product observed within the testing temperature range of 340°C to 400°C [62].

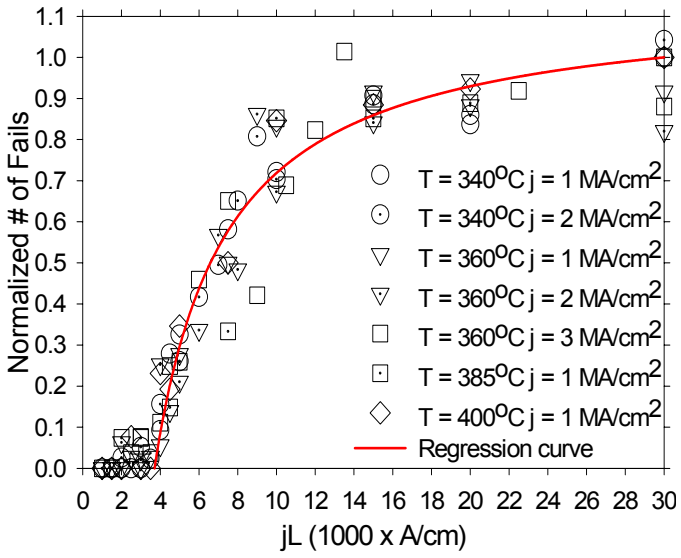


Figure 2.5: EM damage distribution as a function of test line length and current density product (jL) for the 0.5μm Cu/oxide interconnect structures. The $(jL)_c$ product was found to be about 3700A/cm [62].

2.04.3 Early failure (EF) structures

Early failures are a very important issue for EM reliability. They are defined as those failures that occur at a time earlier than that predicted by a single failure mode distribution. Thus, early failures are considered extrinsic in nature, and they seriously affect the extrapolation lifetime for the use conditions. However, due to the rare occurrence of early failures and the difficulties in testing a sufficiently large sample population, early failure detection has always been a difficult issue in EM reliability assessment. The issue of early failures in Al-based interconnects has been addressed in [63-65].

In this section, a brief introduction to the basic EM failure statistics is provided, followed by a description of the statistical early failure test structures used in this study for early failure detection. After that, the corresponding data analysis approach is explained.

2.04.3.1 Statistical background

(A) EM failure statistics for single-link interconnect

Traditionally, lognormal failure distributions, where the natural logarithms of the failure times are normally distributed, have been used to describe the EM failures [58]. This distribution is characterized by a median time to failure t_{50} and the lognormal standard deviation σ. The probability density function *pdf* in time t can be expressed as

$$pdf(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left(-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2} \right), \tag{2.6}$$

The cumulative distribution function *cdf*, or $F(t)$, is the integral of *pdf(t)* from 0 to time t:

$$F(t) = \int_0^t pdf(u)du = \int_{-\infty}^{z} \frac{1}{\sqrt{2\pi}} \exp(-v^2/2)dv, \tag{2.7}$$

where $z = \dfrac{\ln(t) - \ln(t_{50})}{\sigma}$ and $t > 0$.

For single-link interconnect structures, Figure 2.6 illustrates the PDF plot and its corresponding CDF plot for a monomodal EM failure distribution. In comparison, a bimodal EM failure distribution, where two mechanisms are competing against each other to cause failures, is shown in Figure 2.7 [63]. The superscript *in* represents an intrinsic failure mechanism and *ex* represents an extrinsic one. Compared with the almost straight-line CDF plot for a monomodal (intrinsic) failure mechanism, bimodal failures manifest themselves in the branching CDF plot. This is because both the intrinsic (strong) mode with a high t_{50} and the extrinsic (weak) mode with a low t_{50} contribute to the CDF plot. The location of the branching point reveals the proportion of the intrinsic strong mode and the extrinsic weak mode early failures. For example, in Figure 2.7(b), the branching point is roughly located at the 10% cumulative failure distribution, indicating that among all the failures, about 10% are extrinsic early failures.

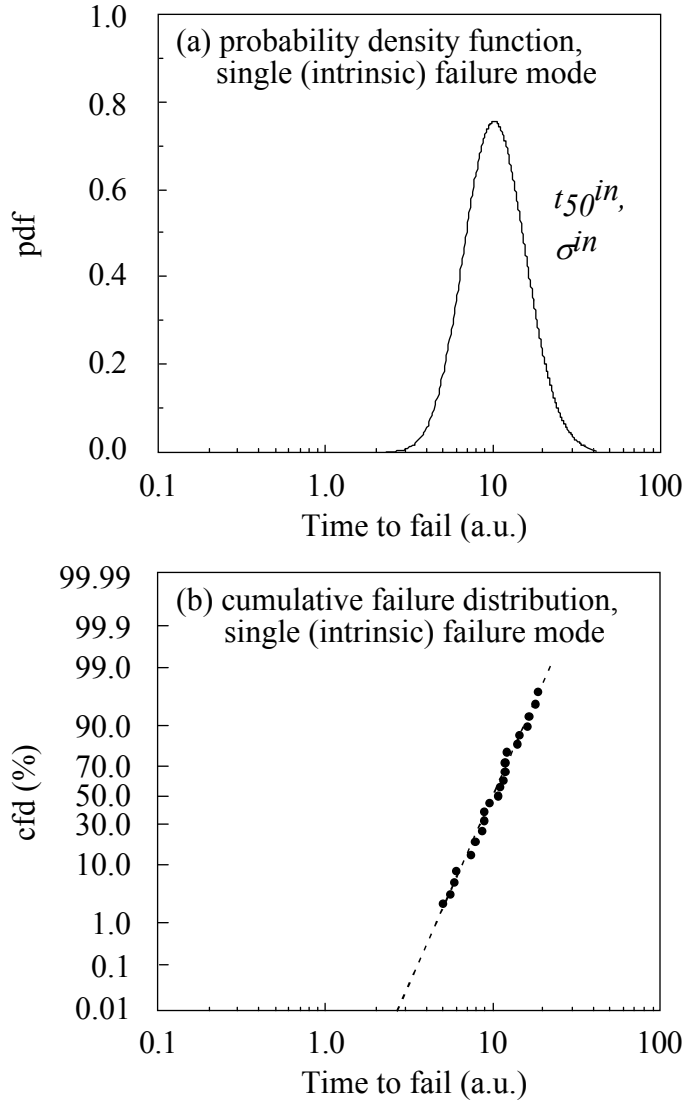


Figure 2.6: Probability density function *pdf* and its corresponding cumulative distribution function *cdf* for a monomodal (intrinsic) EM failure distribution. The distribution is characterized by an intrinsic median time to failure t_{50}^{in} and standard deviation σ^{in} [63].

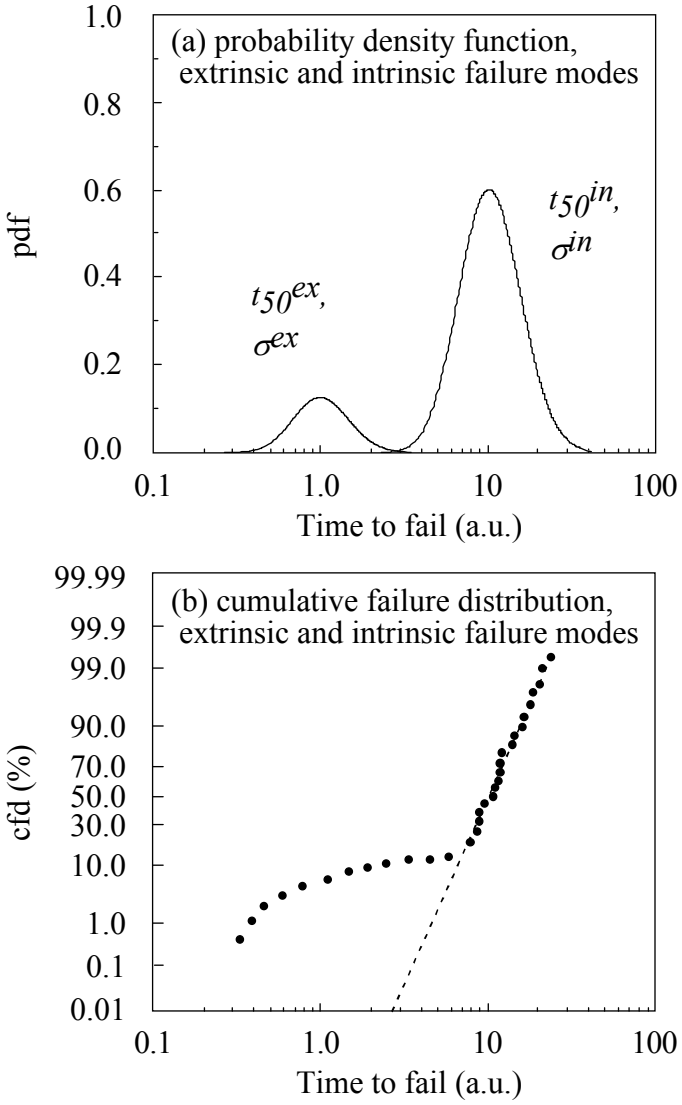


Figure 2.7: Probability density function *pdf* and its corresponding cumulative distribution function *cdf* for a bimodal EM failure distribution, showing both extrinsic (t_{50}^{ex}, σ^{ex}) and intrinsic failures (t_{50}^{in}, σ^{in}) [63].

(B) EM failure statistics for multi-link interconnects

In practice, investigation of early failures normally entails a large number of single-link test structures. To overcome this difficulty, a set of multi-link test structures has been employed to facilitate the estimation of the early failure statistics.

Unfortunately, the lognormal distribution used for the single-link interconnect cannot be extended to the complex multi-link interconnects. In other words, even if each single link follows a lognormal failure distribution, the failure distribution of the whole structure with multi-link interconnects is not lognormal. To solve this problem, a different approach needs to be adopted. It has been shown theoretically that an alternative weakest link failure statistics can be used to explore EM failures under such circumstances [66-67]. Basically, it is assumed that each link is statistically independent, and the whole multi-link structure will fail upon the failure of the weakest link. Statistically, the reliability of the whole structure is the product of the reliability of each single link, which can be expressed by the following equation

$$R(t,N) = R_1(t) \text{ x } R_2(t) \text{ x } R_3(t) \text{ x.....x } R_N(t) \tag{2.8}$$

where $R_i(t)$, $i=1,2 \ldots N$ is the reliability of the ith link at a certain time t, and N is the total number of links within the structure. The failure possibility for the whole structure, therefore, can be described as follows:

$$1\text{-}F(t,N) = (1\text{-}F_1(t)) \text{ x } (1\text{-}F_2(t)) \text{ x } (1\text{-}F_3(t)) \text{ x.....x } (1\text{-}F_N(t)) \tag{2.9}$$

where $F_i(t)$ and $F(t,N)$ are the cumulative failure distribution functions of the ith link and the whole structure, respectively. If $F_i(t)$s are assumed to be identical, then Eq. 2.9 can be simplified as

$$F(t,N) = 1-(1-F_i(t))^N \tag{2.10}$$

Eq. 2.10 is also known as the weakest link approximation (WLA) [68]. Figure 2.8 presents a general trend of the WLA for N-link interconnects, $F(t,N)$ [37]. It is assumed that a single-link structure strictly follows a lognormal distribution, with median time to failure t_{50} = 100 hrs and the standard deviation σ = 0.5. Based on Eq 2.10, the failure probabilities for a multi-link structure with N = 10, 100, 1000, or 10000 are deduced and plotted accordingly. There are two main features observed from the figure: (1) As the number of links N increases, both t_{50} and σ decrease. (2) All the values of the other $F(t,N)$s can be statistically deduced as long as one value of $F(t,N)$ is known for a particular N. Consequently, the failure parameters for single-link interconnects, t_{50} and σ, can be obtained through the testing of the multi-link structures so that the experimental time can be considerably reduced.

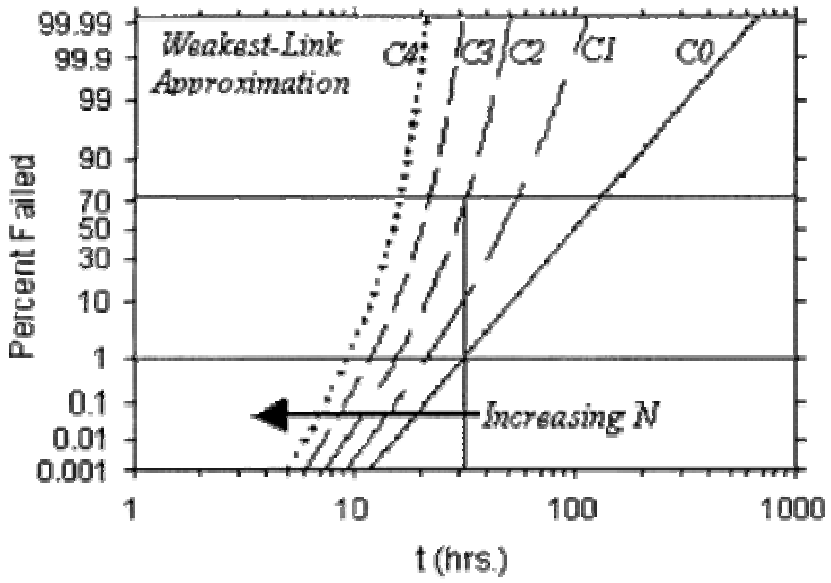


Figure 2.8: General trends of the WLA for *N*-link interconnects, *F(t,N)*. Curves C0, C1, C2, C3 and C4 are obtained using Eq. 2.10 with $N = 1$, 10, 100, 1000 and 10000 respectively. It was assumed that $F_1(t)$ follows a lognormal distribution, with $t_{50} = 100$ hrs and $\sigma = 0.5$ [37].

2.04.3.2 Test structure description

The design of the early failure (EF) test structures is based on the statistical theories discussed above for the investigation of the early failure statistics. With a fixed length (e.g. 150μm), the test lines are either used as single-link structures or connected in series with one anther to form multi-link structures. It should be noted that There are three different types of structures, with $N = 1$, 10, or 100 links, respectively. Figure 2.9 shows a schematic diagram of an M2- type structure with $N = 10$.

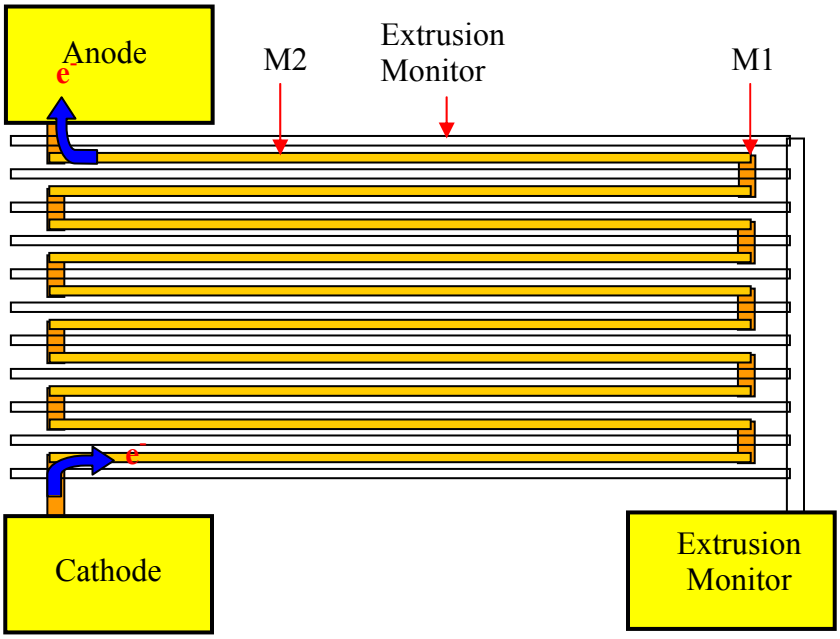


Figure 2.9: Schematic diagram of the M2-type EF module with $N = 10$ [60]. The whole structure fails upon the failure of the weakest link.

2.04.3.3 Monte Carlo simulation for early failure detection

In an EM experiment, typically 12 to 15 samples of each type of test structure (N = 1, 10, or 100) are tested simultaneously to acquire a lifetime failure distribution for each link. The experimental CDF plots for test structures with N = 1, 10, and 100 are obtained accordingly.

Next, based on the WLA approximation, a Monte Carlo simulation [60] is employed to reconstruct the CDF plots for the same structures with the estimated statistical parameters acquired from the experiment, e.g., t_{50} and σ.

Specifically, for the monomodal failure distribution, we start with the examination of the single-link structures (N = 1) whose failures follow a lognormal distribution. The CDF plot for such structures is reconstructed with a set of random lifetimes which can be

generated through the Monte Carlo simulation from the inverse of the CDF plot with the estimated experimental parameters of single links, t_{50} and σ:

$$t = F^{-1}(\text{rand}(\,), t_{50}, \text{and } \sigma) \tag{2.11}$$

where t is the random lifetime generated by the simulation, and F^{-1} is the inverse of the CDF of the lognormal distribution as in Eq. 2.7.

For the reconstruction of the CDF plot for multi-link structures, the shortest of the N lifetimes randomly generated from the single-link structure is used as the one random lifetime for N-link structures based on the WLA approximation. For example, with a 10-link structure, the one random lifetime utilized for the CDF plot is the shortest one among the 10 randomly generated numbers:

$$t(10) = min(t_i), \qquad i = 1, 2, 3, \ldots, 10 \tag{2.12}$$

where t_i is the lifetime of the ith link. A simulated CDF plot for $N = 10$ or 100 can then be created from a large number of $t(10)$ or $t(100)$.

For the bimodal failure distribution, where the early failures are present, we have already defined the strong mode as the failure mode with a longer lifetime, and the weak mode as the failure mode with a shorter lifetime. Based on the experiment, an estimate of the early failure percentage can be acquired. This percentage is used in the Monte Carlo simulation for CDF plot reconstruction. Specifically, random lifetimes for single-link structures are taken from the lognormal distributions for strong mode and weak mode failures according to the estimated early failure percentage. That is,

$$t = \text{IF}((\text{rand}(\,) > \text{P}, F^{-1}(\text{rand}(\,), t_{50s}, \text{and } \sigma_s), F^{-1}(\text{rand}(\,), t_{50w}, \text{and } \sigma_w)) \qquad (2.13)$$

where P is the early failure probability, the subscript *w* represents the weak mode, and the subscript *s* represents the strong mode.

The lifetime of multi-link structures for the bimodal distribution can then be obtained in the same manner as it is for the monomodal distribution. The shortest among the *N* randomly generated lifetimes is chosen for the *N*-link structures, and the CDF plot is created after the acquisition of a large number of the lifetimes.

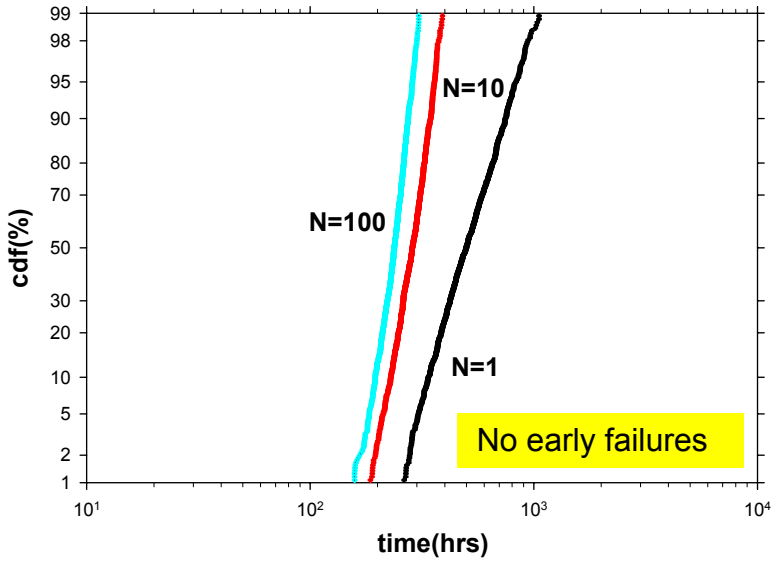
Data fitting is then conducted through the comparison of the CDF plots obtained from the experiment and from the simulation. Because such data fitting is carried out on the N = 1, 10, and 100 links simultaneously, whose CDF plots are statistically correlated with each other, it will generate a more refined set of statistical parameters for subsequent data analyses.

Figure 2.10 shows how the proportion of the weak mode failures can affect the CDF plots of test ensembles with *N* equal to 1, 10, and 100 using the Monte Carlo simulation. In this example, it is assumed that t_{50} = 500 hrs., σ = 0.3 for strong mode failures and t_{50} = 50 hrs., σ = 0.3 for weak mode early failures.

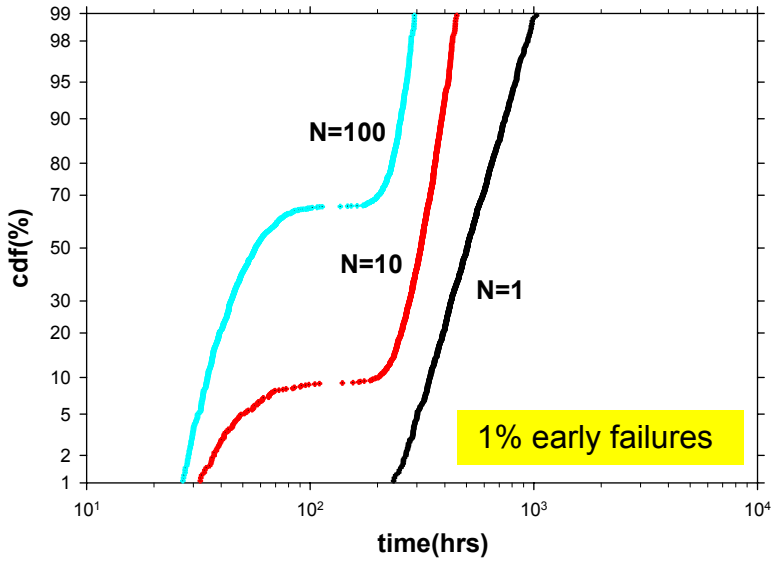
If almost straight-line CDF plots can be observed for *N* = 1, 10, and 100, then the failures are monomodal (Figure 2.10(a)); on the other hand, if branching CDF plots are observed, then the failures are bimodal (Figure 2.10(b)-(d), for weak mode percentage 1%, 10%, and 50%, respectively). As the percentage of the weak mode failures continues to decrease from 50% to 10% to 1%, a well-defined branching point shifts gradually from the *N* = 1 link to the *N* = 10 link, and then to the *N* = 100 link. As shown in Figure 2.10(b), when the weak mode failure percentage is reduced to 1%, a clear branching point is no longer observed in the CDF plots for the single link ensemble (*N* = 1) any more.

Unless an extremely large ensemble is tested, no information about the early failure parameters can be obtained exclusively from testing single-link test structures alone. As N increases to 10, the weak mode failures contribute more to the CDF plot, causing it to shift away from the strong mode line to become a weak mode line roughly for the first 10% cumulative failures. For N =100, we can see that the weak-mode early failures already account for almost 70% of the total failures.

The simulation results demonstrate that early failures of a very low percentage can still be easily detected in medium-sized multi-link ensembles. This statistical approach can be very useful in obtaining good estimates of lifetime statistics (t_{50} and σ) when the resources for testing extremely large sets of single element structures are not available.

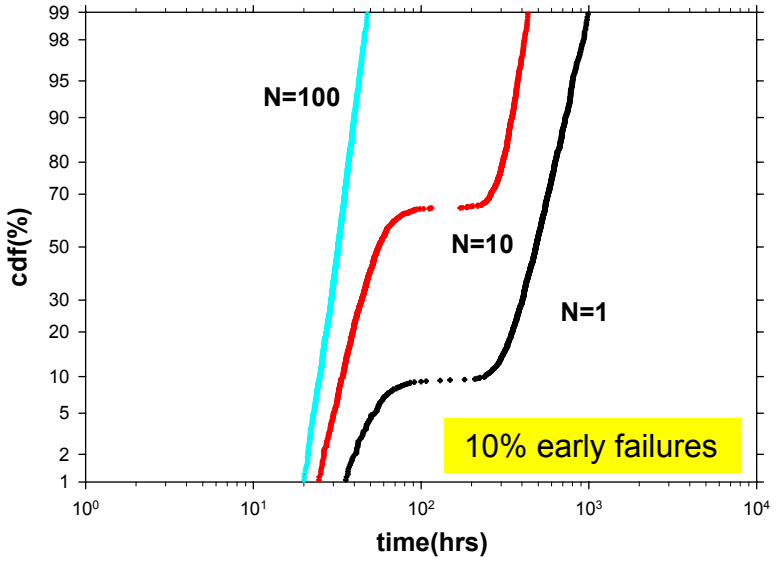


(a)

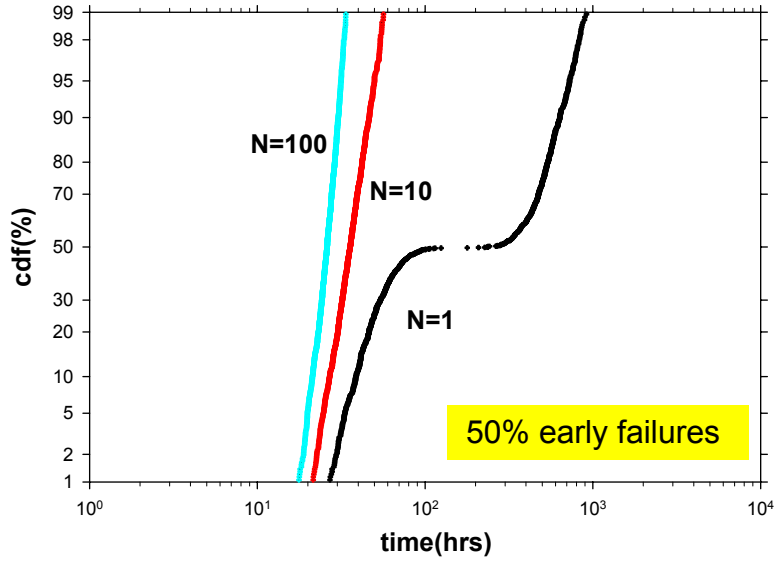


(b)

Figure 2.10: Early failures change the statistical distribution. A Monte Carlo simulation based on the WLA is used to deduce failure mode parameters when there are (a) no early failures, and (b) 1% early failures, assuming t_{50} = 500 hrs., σ = 0.3 for strong mode failures and t_{50} = 50 hrs., σ = 0.3 for weak mode early failures.



(c)



(d)

Figure 2.10: Cont. (c) 10% early failures, and (d) 50% early failures, assuming t_{50} = 500 hrs., σ = 0.3 for strong mode failures and t_{50} = 50 hrs., σ = 0.3 for weak mode early failures.

2.05 TYPICAL RESISTANCE TRACES

EM takes place when a DC current is applied to the interconnect line, eventually resulting in the depletion and accumulation of metal atoms at the locations where there is an imbalance of atomic fluxes, e.g. the cathode and anode ends of the line. Over time, the net atom flux will cause voiding and extrusion in the line, which will ultimately lead to major resistance changes.

In order to better understand the typical resistance changes observed during the EM testing, it is necessary to describe the connections between the test structures and the external circuit. As mentioned in Section 2.03, with a constant current applied to the test structure in the experiment, the voltage across the structure is continuously measured with the wire bonds connected to the V^+ and V^- terminals. In addition, the extrusion monitor lines next to the test lines are employed to detect the occurrence of short circuits in the experiment. And the V^{ex} terminal is connected to the V^+ terminal so that the maximum strength of the electric field between the extrusion monitor line and the test line is limited.

For a typical EM failure due to voiding at the cathode end, the resistance change is almost negligible initially when Cu first starts to be depleted from the cathode end. When Cu is almost depleted of a whole cross-section of the interconnect line, the current is forced to flow through the highly resistive Ta/TaN barrier layer, causing an appreciable resistance increase. Such an increase may eventually lead to a resistance level that is intolerably high, and thus bring about a structural failure. Figure 2.11 provides the resultant resistance trace under such circumstances along with an illustration of the external circuit.

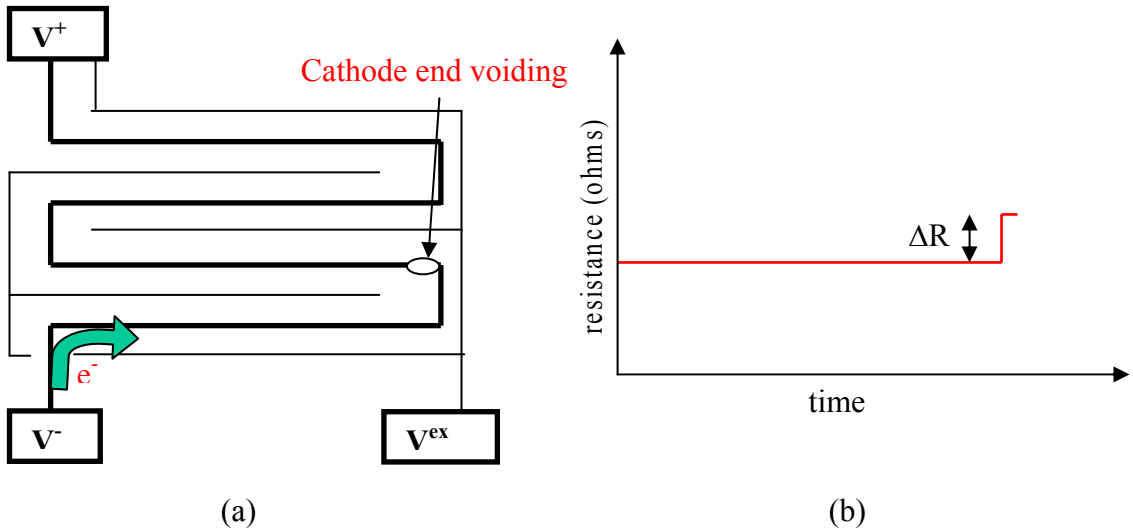


Figure 2.11: Schematic diagrams of (a) an external circuit when there is a cathode end voiding and (b) a resistance increase in a typical EM failure.

A different resistance trace is identified (Figure 2.12) when there is a short circuit between the interconnect line and the extrusion monitor line. With the accumulation of Cu atoms at the anode end, lateral extrusion from the weak interface may occur and the extruded Cu may touch the adjacent extrusion monitor lines. Under such circumstances, some of the current will take a shortcut through the extrusion monitor lines. Compared with the test line, the resistance of the extrusion line typically is lower; as a result there is a major voltage drop measured across the V^+ and V^- channels of the test structure, indicating a resistance drop. The magnitude of the resistance drop is indicative of the location of the extrusion, and thus that of the short circuit. For example, in a multi-link structure, a larger resistance drop suggests that the short circuit takes place in the interconnect line close to the V^- terminal; and a smaller resistance drop suggests that it occurs in the interconnect line close to the V^+ terminal.

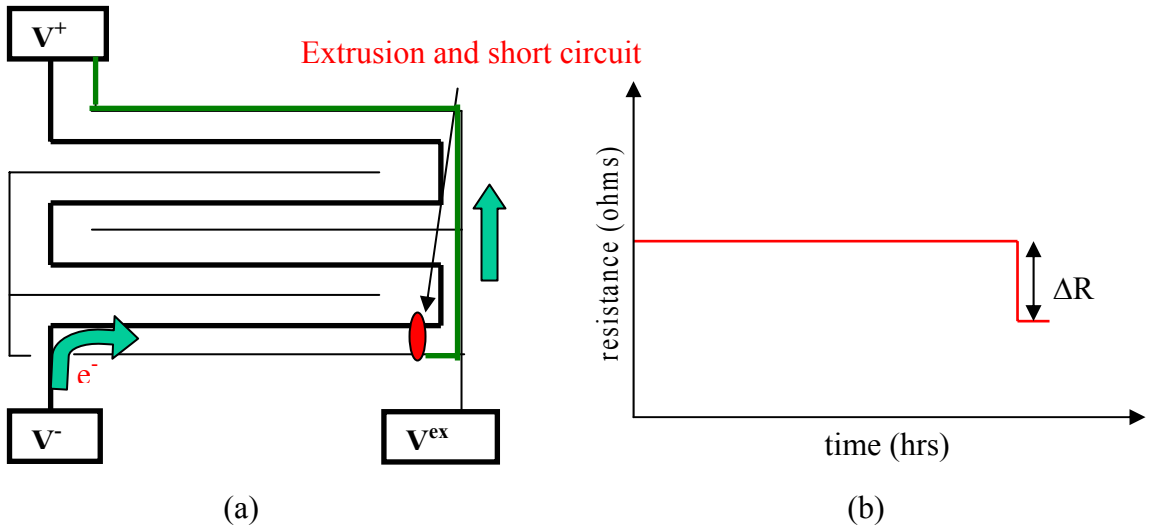


Figure 2.12: Schematic diagram of (a) lateral extrusion at the anode end and a short circuit between the interconnect line and the extrusion monitor line, and (b) a resistance drop. The magnitude of the resistance drop ΔR indicates the location of the short circuit.

2.06 FAILURE ANALYSIS

After the experiment, failure analysis was conducted with the FEI Strata™ DB235 dual beam FIB/SEM system (Figure 2.13). First, a finely focused ion beam normal to the sample surface is used to mill away precisely a certain amount of material from the sample near the region of interest. The volume to be milled away is determined by the size of the mill box and the cut depth. During this milling process, the region of interest, i.e. the sidewall of the M2 lines, or the embedded via and the M1 lines, is gradually exposed. As a result, the SEM images which are taken next at an angle of 52° represent a precise cross-section of the region of interest. The major advantage of this

system is that it allows simultaneous cutting and imaging of the test structures, enabling us to identify the failure locations with ease.

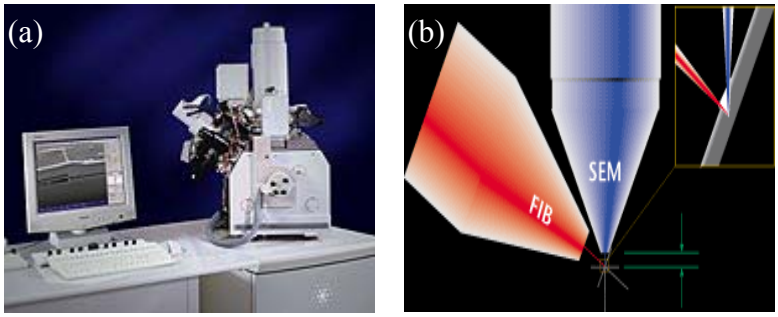


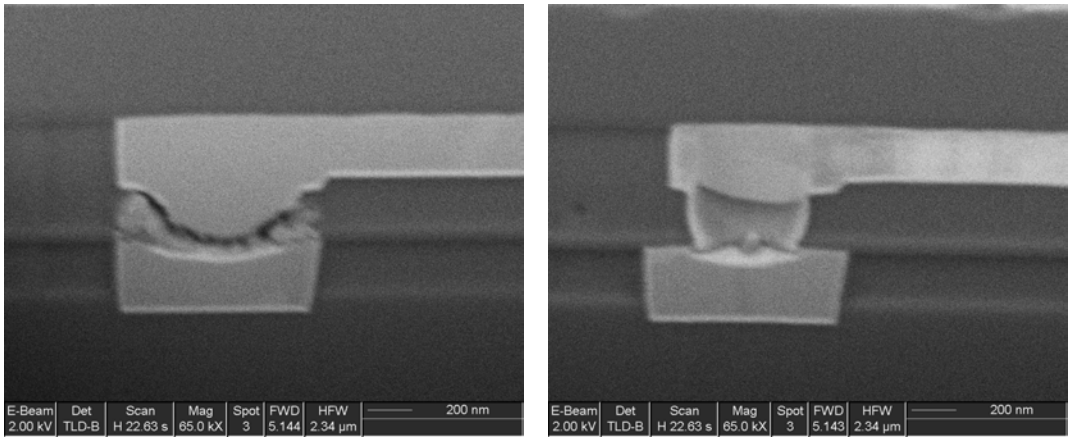
Figure 2.13: (a) The FEI Strata™ DB235 dual beam FIB/SEM system and (b) the schematic of the two beams (~52° in between).

In the following section we will provide some examples of FIB/SEM images obtained from a number of test structures with various EM damage sites.

In the dual-damascene Cu interconnects, the void formation as well as its subsequent growth is a very complicated process, since both process-related defects and geometric features can give rise to voiding at different locations.

Typically, early failures are via-related, because vias are particularly prone to process-related problems, such as a poor via etch or an inadequate cleaning process, which may lead to micro-roughness or interfacial defects at the via bottom and turn it into a potential void nucleation site [69]. In case of a void nucleating at the via bottom, when it will eventually lead to a resistance increase and an EM failure is largely dependent on the quality of the barrier layer. Specifically, with a poor barrier layer, when the Cu is fully depleted at the via bottom, the barrier layer can be blown apart due to a high current density, resulting in an open circuit failure (Figure 2.14(a)). However, with a good and

robust barrier layer, the void can grow along the via sidewall instead of blowing apart immediately. Under such circumstances, a relatively large void is needed to fail the interconnect line. (Figure 2.14(b)).



(a) (b)

Figure 2.14: The quality of the barrier layer is a major determinant in the critical void size. (a) With a poor barrier layer void grows along the via bottom and the barrier layer can blow to cause an open circuit. (b) A larger void is needed to fail the circuit in case of a robust barrier layer.

As mentioned before, the CMP-produced interface between the cap layer and Cu serves as the built-in fast diffusion path for EM. If void nucleates at this interface, then a fairly large void size in the trench is needed to cause an appreciable resistance increase and an EM failure, as can be seen in Figure 2.15.

Occasionally a competing process of the trench failure and the via failure can be found, as shown in Figure 2.16. This process is characterized by the simultaneous void formation and growth at two different sites. The trench void usually grows faster yet may require more material depletion. And the via void normally grows slower because the

Cu/barrier diffusion is slower than the Cu/cap layer diffusion; however, it may require less material depletion to cause a resistance increase [37].

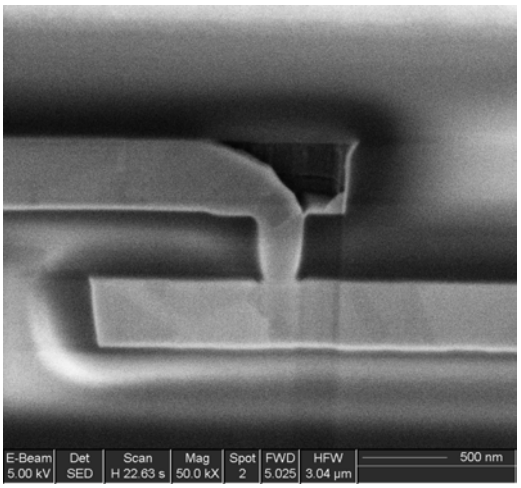


Figure 2.15: Strong mode void formation at the cathode end of the line on the Cu/cap layer interface.

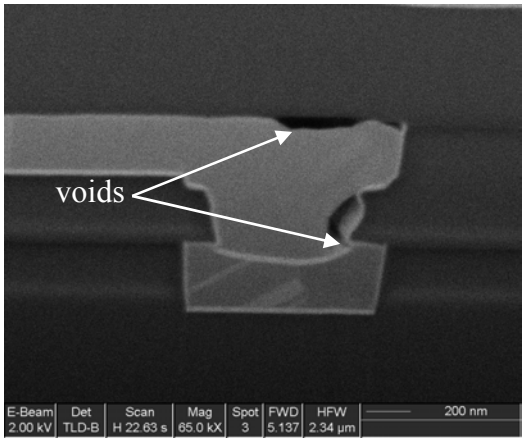


Figure 2.16: A mixture of void formation is present, indicating a competing process of trench failure and via failure.

Figure 2.17 is an example of a Cu extrusion and shorting failure. The Cu at the anode end laterally extrudes to touch the extrusion monitor line. As a result, an electric short leads to the failure of the interconnect line. This failure mode was observed more frequently in the early versions of the Cu/low k structures. It was due to the smaller confinement from the surrounding low k materials and weaker interfaces as a result of less-than-optimal process control. Under such circumstances, the local build-up of compressive stress at the anode end under EM reaches a critical value, and hence readily leads to lateral extrusions.

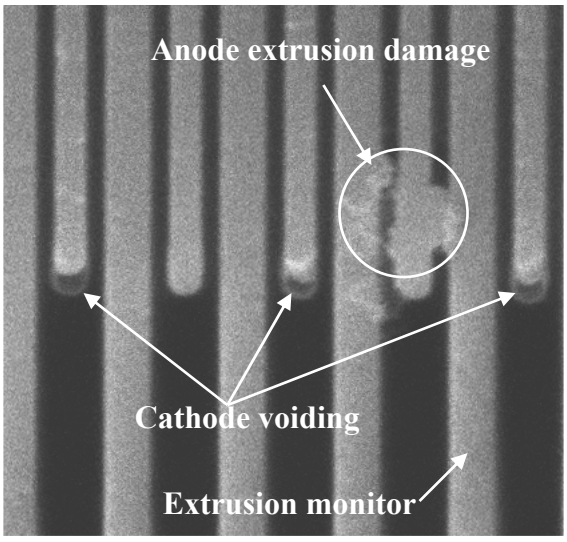


Figure 2.17: Anode extrusion damage is found besides void growth at the cathode end due to a weak interface, which can lead to a shorting failure.

Chapter 3: Impact of Electromigration Lifetime Characteristics

3.01 OVERVIEW

To improve the device density and performance, the interconnect dimensions, e.g., metal line width, via size, and barrier thickness, continue to be scaled down aggressively. This trend necessitates the implementation of new materials and more complex and challenging integration schemes. However, the introduction of new materials and integration schemes has given rise to significant EM reliability concerns.

In this chapter, a statistical approach is adopted to examine the EM lifetime characteristics arising from the interconnect dimensional scaling, the introduction of low k dielectric materials, and the application of the distinct Cu dual-damascene interconnect structures. Specifically, interconnects of three different metal line widths, 0.5μm, 0.25μm, and 0.175μm, and three different barrier thicknesses, 175Å, 100Å, and 75Å, will be studied in terms of their effects on EM lifetime characteristics. Two low k dielectric materials, a dense MSQ low k material and a porous MSQ low k material will be used. Two electron flow directions, upstream M2 and downstream M1, will be explored as well in an effort to examine the EM-induced damage as a result of different geometrical design features. Later, a Monte Carlo simulation is employed to deduce the statistical parameters for both the intrinsic EM failures and the process defect-related extrinsic early failures. Next, in the failure analyses, both FIB and TEM are used to identify the physical locations of the EM failures. It is revealed in the study that there is an intrinsic scaling effect for the strong mode EM statistics. However, process-related issues may lead to lifetime degradation and weak mode failures in structures with a smaller line width/barrier thickness.

3.02 CRITICAL FAILURE VOID VOLUME

EM failures are characterized as either voiding or extrusion. This chapter only focuses on failures resulting from voiding. First of all, a concept of the critical failure void volume will be introduced, followed by a brief discussion of the failure criterion used in this study.

Under EM, void formation in interconnect lines may cause an increase in line resistance. Such an increase, however, is hardly appreciable till a void grows large enough to cut the current flow in the Cu line and all the current is then forced to go through the more resistive thin Ta barrier. Thus, a critical failure void volume can be defined as the volume needed to pinch off the current flow in the Cu line and in turn to cause the first resistance surge.

In Cu dual damascene interconnects, the critical failure void volume is largely dependent on both the void morphology and the local geometry near the via region, and it varies from line to line. For example, it is typically small if a void forms right underneath or above the via; and tends to be large if a void forms somewhat off the via in the line trench [70-71]. Figure 3.1, for example, illustrates the critical failure void volume for an M2 interconnect line.

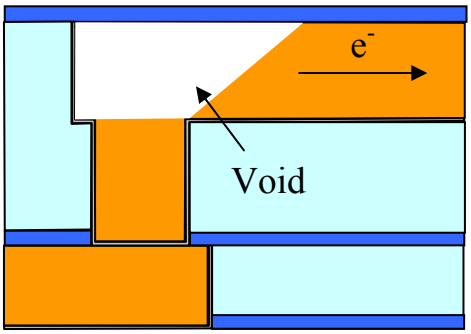


Figure 3.1: Critical failure void volume for an M2-type dual damascene interconnect line: the void has to grow substantially across the line segment over the via.

In this study, the first resistance surge, which is contingent on the critical failure void volume, is employed as the failure criterion to examine the EM lifetime characteristics. This criterion is different from the traditional percentage-based failure criterion, $\Delta R/R_0$, where R_0 is the baseline resistance for an interconnect structure before the EM experiment, and ΔR is the resistance change due to EM. Specifically, with a percentage-based criterion, a failure can be identified as a certain amount of resistance increase, for example, a 5%, 10%, 20%, or 100% increase. This traditional percentage-based criterion has been widely used to define the time to fail an interconnect structure [72-74].

With a poor barrier layer, the choice of the failure criterion makes little difference in that the EM failure lifetime is independent of such a choice. When the critical failure volume is reached, significant joule heating in the thin barrier will instantly lead to an open-circuit, that is, an infinite surge of resistance.

With a good barrier layer that can act as a reliable shunting layer, a fixed percentage-based failure criterion becomes problematic. This is because various test structures are compared, e.g. structures with different line dimensions or line links, which may give rise to a different baseline resistance R_0. Therefore, with a fixed percentage-based failure criterion, we may actually be comparing voids of different developmental stages for different test structures. Such comparisons are not very meaningful.

The first resistance surge criterion, in contrast, addresses the physical process more properly in the sense that a more reasonable comparison is conducted across different structures, since such comparison is independent of the initial line resistance and the barrier layer quality.

Now that the failure criterion to be used in this study is selected, we will proceed to examine the impact of dimensional scaling on EM lifetime characteristics in Cu dual

damascene interconnects, including the scaling of metal line width, via size, and barrier thickness in the following sections.

3.03 METAL LINE WIDTH AND VIA SIZE SCALING

3.03.1 Review of scaling rule in single-damascene interconnects

Figure 3.2 shows a schematic of a single damascene M2 Cu line with a W via connecting the M2 Cu line to the underlying M1 W line. One of the major characteristics that differentiates it from a dual-damascene Cu line is that there is a Ta/TaN barrier layer on top of the via. As a consequence, the explicit EM divergence for a single damascene structure is located over the top of the cathode end W via.

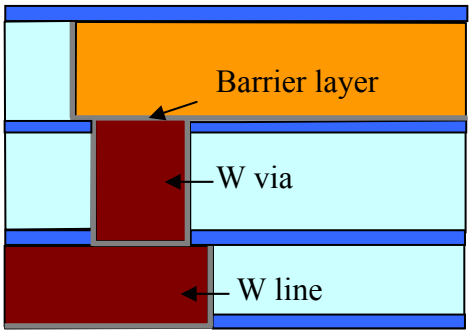


Figure 3.2: Schematic of a single damascene Cu line with a W via and an underlying W M1 line.

A resistance surge can be observed when a void grows past the W via and the current has to go through the thin Ta barrier which connects the remaining Cu line and the W via. Therefore, the critical failure volume $V_{crit,\,fail}$ can be estimated as $\Delta L_{cr} \times A$, where ΔL_{cr}, the critical void length to cause a line failure at the lifetime τ, equals the

overlapping region between the line and the W via, and A is the cross-sectional area of the interconnect line. For long test lines under a high current density, the effect of EM induced backflow stress on the drift velocity of Cu at the cathode end of the line can be ignored in Eq. 1.3. The drift velocity of Cu can thus be expressed as

$$v_d = \Delta L_{cr} / \tau = \frac{D_{eff} Z^*_{eff} e \rho j}{kT} \tag{3.1}$$

The critical failure void volume $V_{crit,\,fail}$ is then given by

$$V_{crit,fail} = A v_d \tau = \frac{A D_{eff} Z^*_{eff} e \rho j}{kT} \tau \tag{3.2}$$

If the interface between Cu and the top cap layer, e.g. SiN_x or $SiC_xN_yH_z$, is the dominant EM diffusion path [25-28], then the EM mass transport is restricted to the top interface, specifically, in an area of $\delta_{Cu/c}\, w$, where $\delta_{Cu/c}$ is the effective thickness of the Cu/caper layer interface and w is the metal line width.

From Eq. 1.4, we can deduce that

$$D_{eff} = \frac{D_{Cu/c} \delta_{Cu/c}}{h} \tag{3.3}$$

where h is the thickness of the metal line. Therefore, Eq. 3.1 can be transformed to the following scaling rule for a single damascene interconnect:

$$\tau = \frac{kT \Delta L_{cr} h}{Z^*_{eff} e \rho j D_{Cu/c} \delta_{Cu/c}} \tag{3.4}$$

It is clear that the lifetime drops as the interconnect dimension ($\Delta L_{cr} \times h$) scales down. This scaling rule for single damascene structure was first reported by Hu et al.[75]. In their study, they also plotted the normalized median lifetime vs. $\Delta L_{cr} \times h$ for various Cu interconnect generations from 90nm technology to 1μm technology, as shown in Figure 3.3. The experimental data that they obtained agree very well with the theoretical curve predicted by Eq. 3.4.

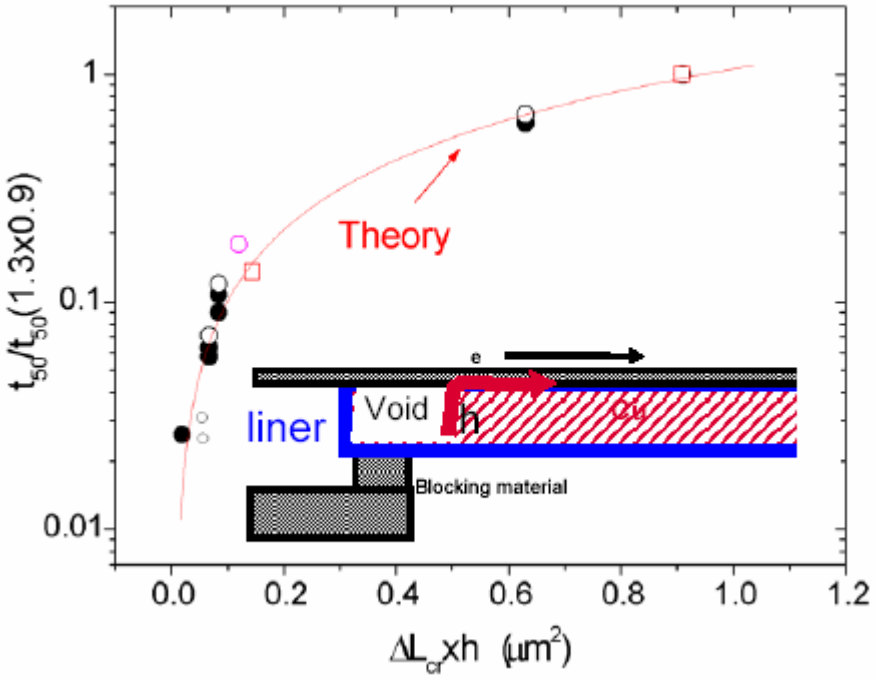


Figure 3.3: Normalized median lifetime vs. $\Delta L_{cr} \times h$ for various Cu single damascene interconnect generations from 90nm technology to 1μm technology [75].

3.03.2 Scaling effects in dual-damascene interconnects

For the dual-damascene Cu interconnects, a more sophisticated integration scheme is expected. Unlike the single-damascene interconnects, the metal trench and the via are formed simultaneously, with no barrier layer on top of the via. Such a difference leads to different EM damage formation mechanisms.

Within the M2 interconnects, for example, due to the presence of the barrier layer at the via bottom which eliminates the Cu atomic fluxes from the underlying M1 layer, the Cu damascene vias represent a local flux divergence site. The upper corner of the cathode end M2 trench is another potential flux divergence site. As a result, the distinct geometric design features of the dual damascene structure can readily give rise to EM failures from complicated void formations.

This study was designed to explore the scaling effects on dual-damascene structures. EM experiments were performed on EF test structures under a current density of 1.0 MA/cm^2 at 300°C, 325°C, and 350°C, respectively. Three different structures were examined, with their line width equal to their via size at 0.5, 0.25, and 0.175μm, respectively. The thickness of all the structures was fixed at 0.32μm and the line length at 300μm. A dense CVD MSQ material with an effective permittivity k of 2.7 was used as the ILD material. Both the upstream M2 structures and the downstream M1 structures were studied.

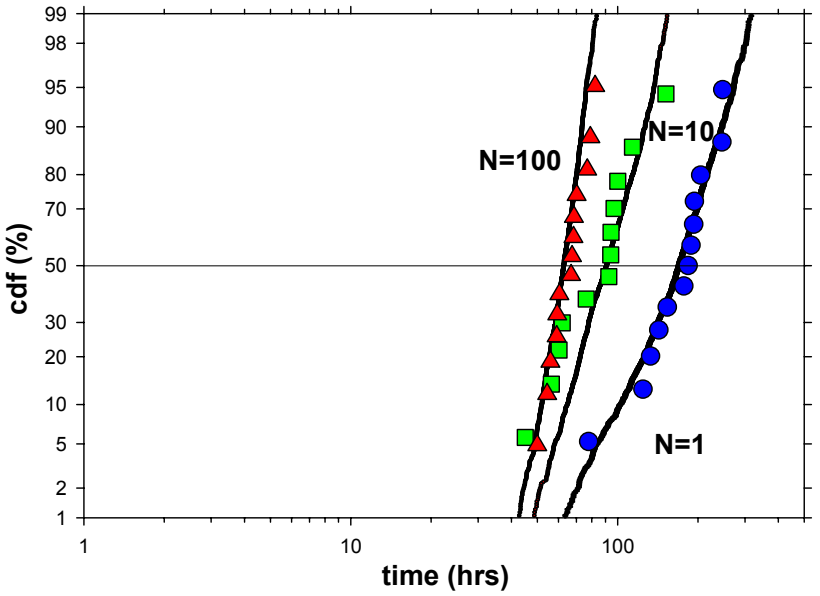
3.03.2.1 Experimental results for upstream EM (M2)

The CDF plots of EF test structures from the experiment and the subsequent WLA Monte Carlo simulation are presented in Figure 3.4 as a function of line width for the upstream M2 electron flows. Solid symbols are the real lifetime data from the experiments and the lines with small dots represent data generated by the simulation. As

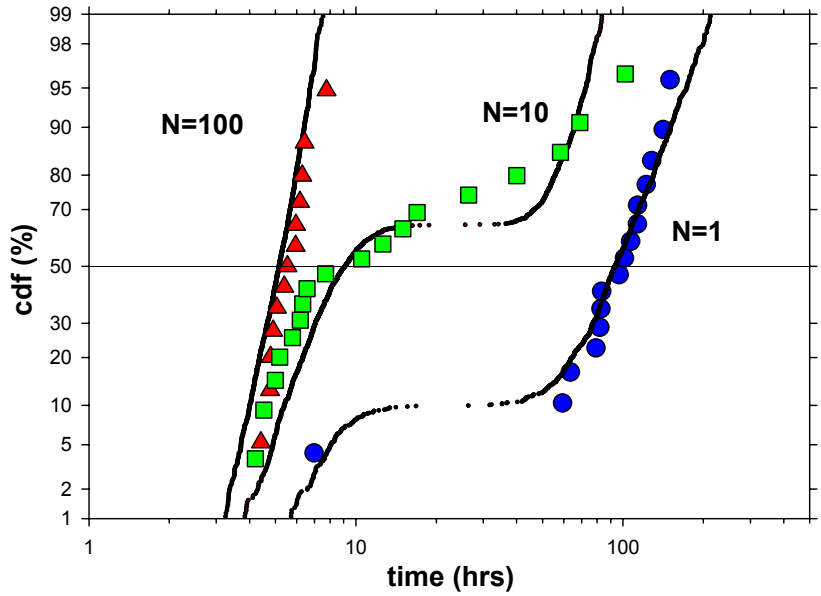
can be seen, the branching due to the bimodal failure mechanism is very obvious for both the 0.25 and the 0.175μm structures. With the Monte Carlo simulation for the best fitting curves, even the 0.5μm structures were revealed with both the strong failure and the weak failure modes. The simulation results on the average lifetime t_{50}, standard deviation σ, and the failure population for the strong and the weak modes are listed in Table 3.1.

Physical failure analyses of the stressed test structures with FIB/SEM enable us to not only pinpoint the failure sites but also establish the correspondence between the resistance trace patterns and the failure modes. For illustration, Figures 3.5 and 3.6 provide some typical examples of line resistance traces and corresponding cross-sectional FIB images for the strong mode and the weak mode failures, respectively.

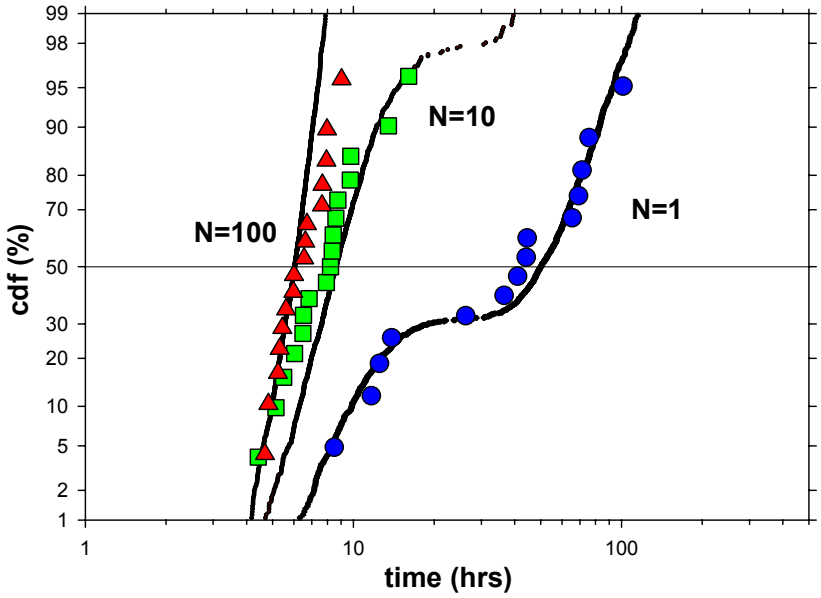
From these two Figures, we can see the resistance surge to infinity corresponding to a void growth completely across the line to cause an open circuit, which is the intrinsic strong mode failure (Figures 3.5(a) and 3.6(a)). In contrast, the small increase in resistance followed by resistance recovery and fluctuation corresponding to void formation at the via bottom represents a typical weak mode failure (Figures 3.5(b) and 3.6(b)). A possible explanation for such recovery and fluctuation is that as the void grows, the density of the current passing through the Ta barrier and via bottom continues to increase. However, sufficient local joule heating will soon induce Cu diffusion to heal the via open. It was also reported that the remaining Cu filament at the via bottom may melt due to local joule heating, leading to the formation of some amorphous and unidentifiable phases, which later may re-connect and heal the Cu line [76]. Such a mechanism can be used to explain the resistance fluctuation following an appreciable increase.



(a) 0.50μm



(b) 0.25μm

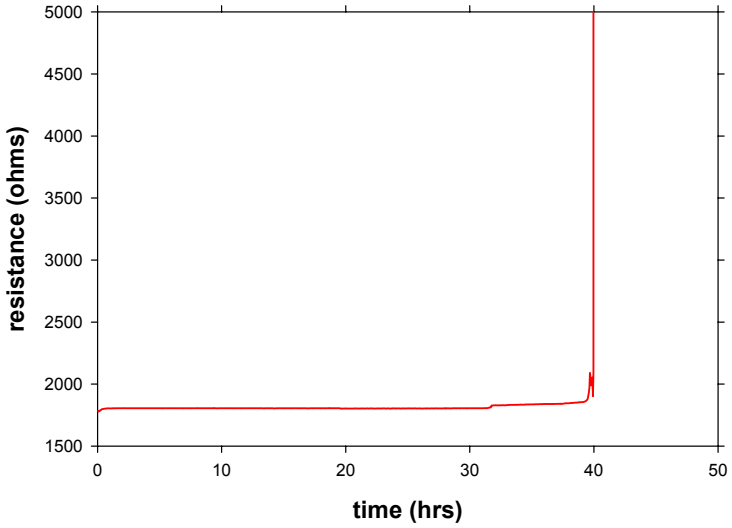


(c) 0.175μm

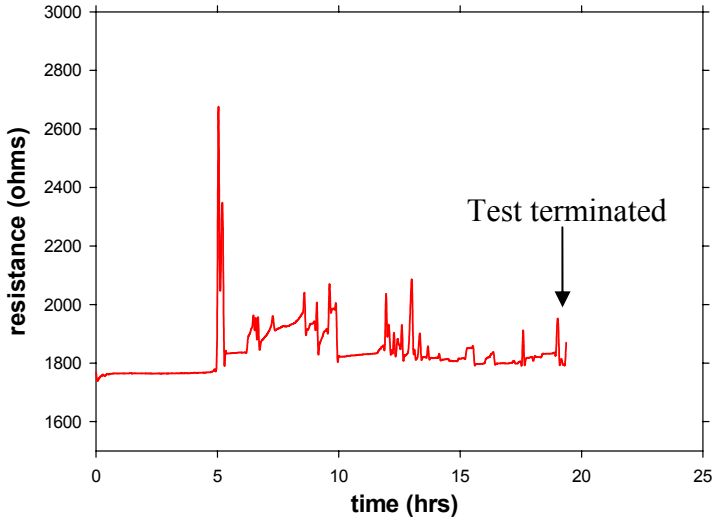
Figure 3.4: CDF plots of EF structures as a function of the line width of (a) 0.5μm, (b) 0.25μm, and (c) 0.175μm for upstream M2 electron flows. Solid symbols were the real lifetime data and small dotted lines were generated by WLA Monte Carlo simulation.

Table 3.1: Summary of EM lifetime data for upstream M2 electron flows. EM tests were performed at $T = 325\ ^{o}C$ and $j = 1.0\ MA/cm^2$.

	Line Width	0.5μm	0.25μm	0.175μm
Upstream M2	% of Weak Mode	15%	10%	30%
	t_{50} of Weak Mode	90 hrs	8 hrs	11 hrs
	σ of Weak Mode	0.25	0.3	0.3
	t_{50} of Strong Mode	180 hrs	100 hrs	60 hrs
	σ of Strong Mode	0.25	0.35	0.3

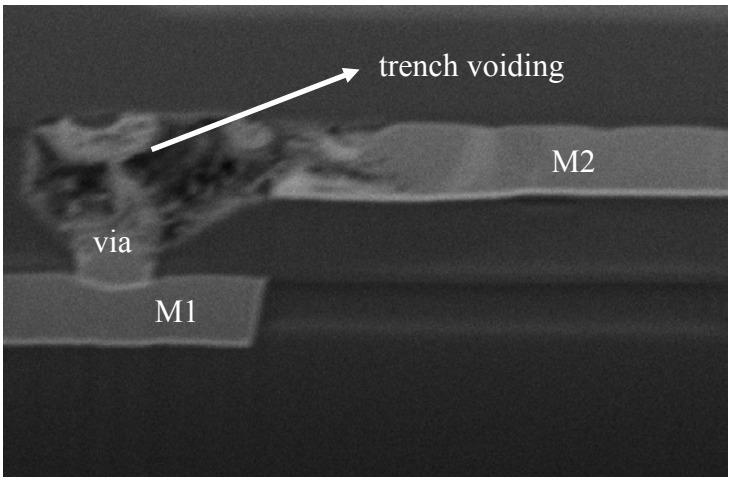


(a)

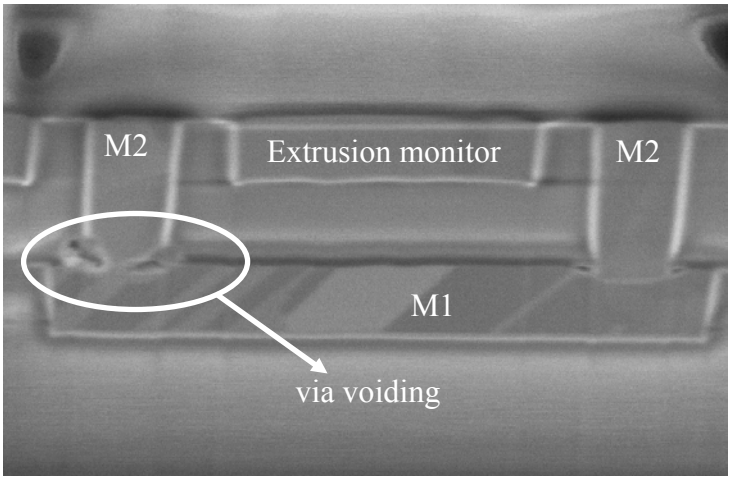


(b)

Figure 3.5: Typical examples of resistance traces for interconnect lines 0.25μm wide failed by (a) a resistance surge to infinity (strong mode failure); and (b) an increase in resistance followed by resistance recovery and fluctuation indicating both a voiding and a healing process (weak mode failure). EM experiments were conducted at $T = 325^{o}$C and $j = 1.0$ MA/cm^2.



(a)



(b)

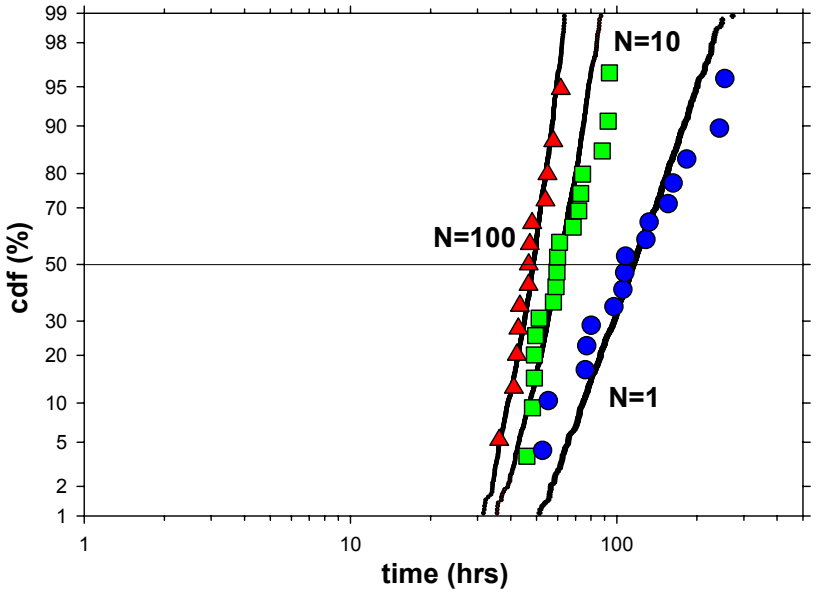
Figure 3.6: Corresponding FIB images for Figure 3.5: (a) a strong mode failure where void grows along the Cu/cap layer interface, and (b) a weak mode failure where void grows at the via bottom.

3.03.2.2 Experimental results for downstream EM (M1)

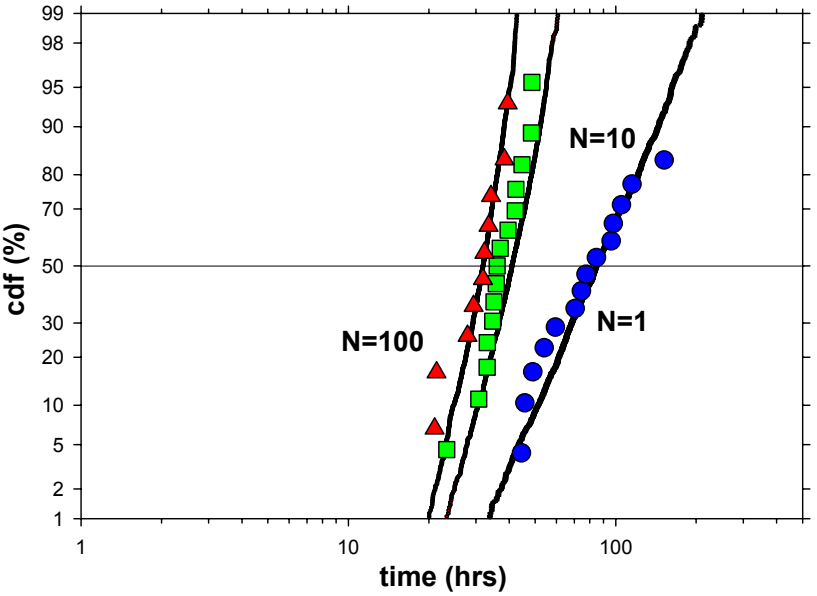
Figure 3.7 shows the CDF plots for the downstream M1 electron flows as a function of the line width. Unlike the upstream M2 structures, merely one set of parameters can be found to fit the overall failure statistics for $N = 1$, 10, and 100 links for all line widths for the downstream M1 structures, suggesting a monomodal failure distribution. Therefore, the lifetime data from the experiment were analyzed using a Monte Carlo simulation based on the monomodal statistics accordingly, and the simulation results are listed in Table 3.2.

It was revealed through the failure analyses that there are actually two types of void locations within the monomodal failure population. Some voids nucleated in M1 underneath the via (Figure 3.8(a)), thereby directly blocking the current path between the via and the line below, and causing an open circuit. In contrast, others nucleated in the M1 trench away from the via. In the latter case, the current will have to pass through the barrier layer along the trench bottom and sidewalls due to the presence of a fully spanned void that cuts the current path in the Cu. A relatively large void is typically needed to fail the line accordingly (Figure 3.8 (b)).

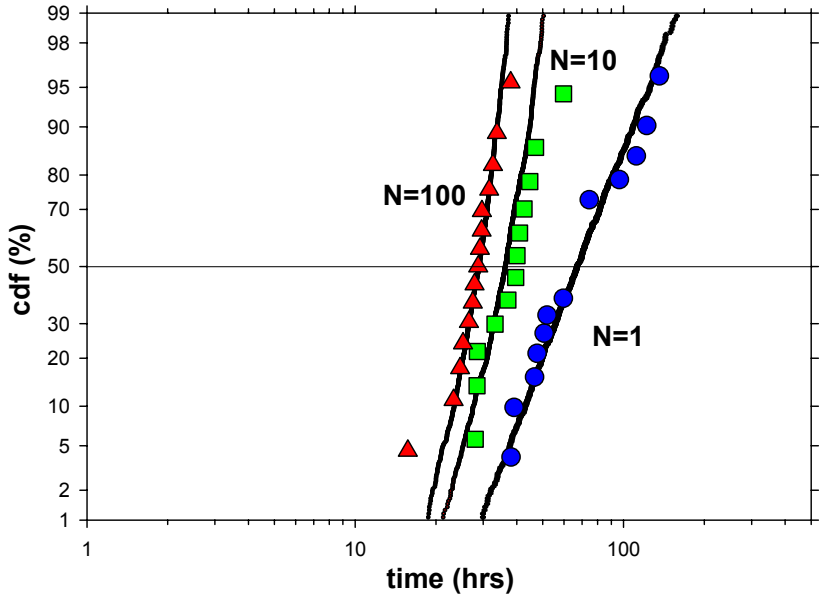
Figure 3.9 presents three types of resistance increase patterns. As mentioned earlier, in all cases, initially the current still goes through the Cu line in spite of some void growth; consequently there is a period of time when little resistance change is detected. When Cu is depleted across a certain line segment, that is, when there is a full-span void, the current is then forced to pass through the thin barrier layer, which results in a surge of resistance. After that, the differences in the stability and integrity of the barrier layers may lead to quite different resistance behavior.



(a) 0.50μm



(b) 0.25μm

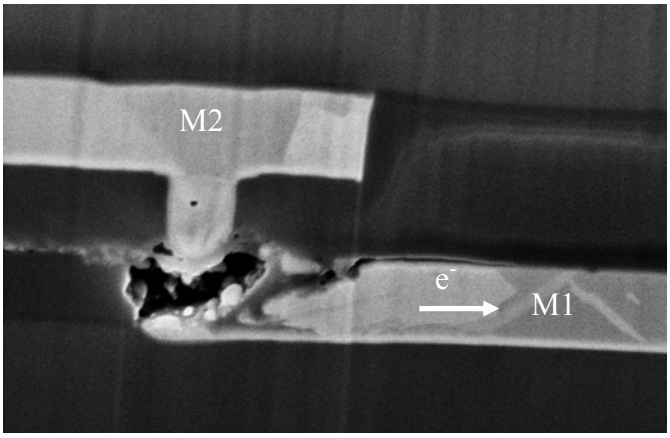


(c) 0.175μm

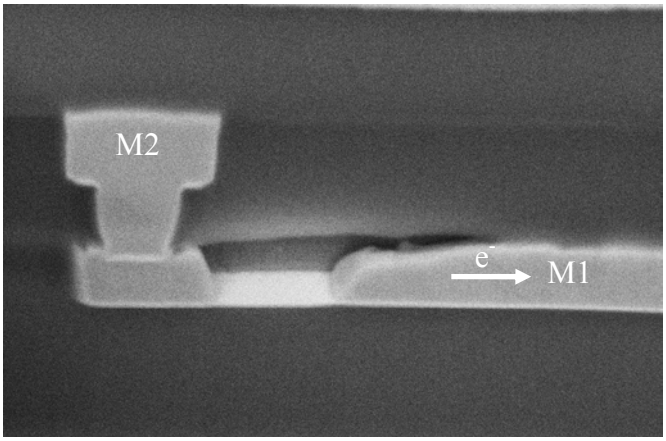
Figure 3.7: CDF plots of EF structures as a function of the line width for downstream M1 electron flows. EM tests were conducted at $T = 325^{o}C$ and $j = 1.0$ MA/cm^2. Solid symbols were the real lifetime data and small dotted lines were generated by WLA Monte Carlo simulation. Data seem to suggest a monomodal distribution.

Table 3.2: Summary of EM lifetime data for downstream M1 electron flows. EM experiments were conducted at $T = 325\ ^{o}C$ and $j = 1.0$ MA/cm^2.

	Line Width	0.5μm	0.25μm	0.175μm
Downstream M1	t_{50}	115 hrs	75 hrs	65 hrs
	σ	0.36	0.38	0.35



(a)

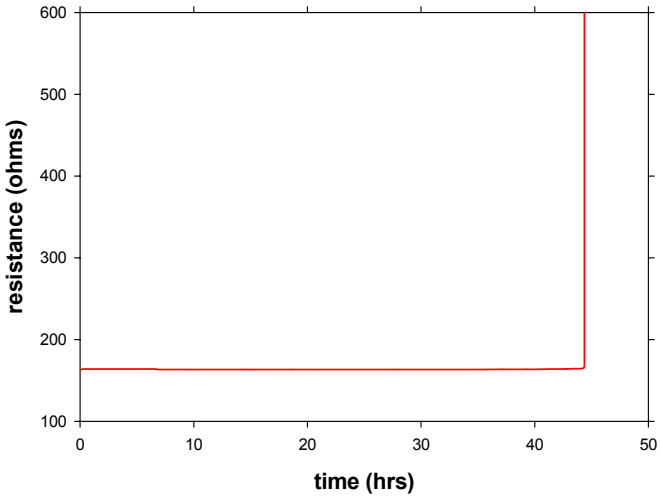


(b)

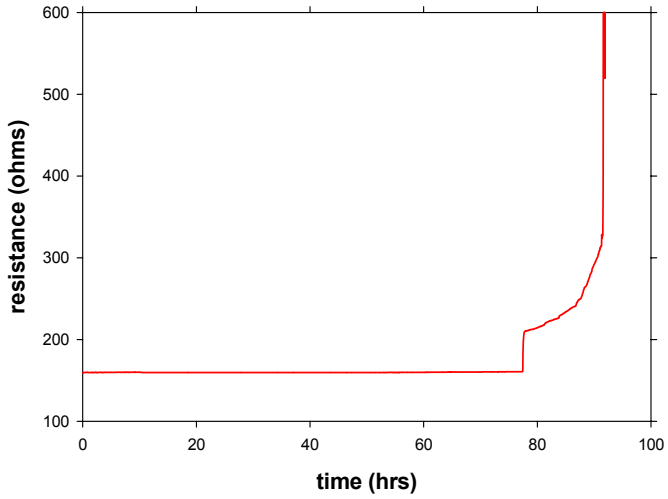
Figure 3.8: FIB images revealed that EM failures were caused by (a) voiding either in M1 under the via, or (b) voiding away from the via in the M1 trench.

In Figure 3.9(a), a plateau is followed by an abrupt resistance surge to infinity because the barrier layer is not able to sustain the applied current. In Figure 3.9(b), a step-like jump is followed by a steady resistance increase, indicating that the thin barrier layer is acting as a shunting layer. In this case, the resistance continues to increase gradually

until the barrier cannot hold the current any more. When this happens, the resistance will increase dramatically and the line will end in an open failure. In Figure 3.9(c), a step-like jump is followed by some resistance fluctuations. This is possibly a result of a less stable barrier layer and local temperature fluctuations. These observed resistance behaviors have also been reported in [73].



(a)



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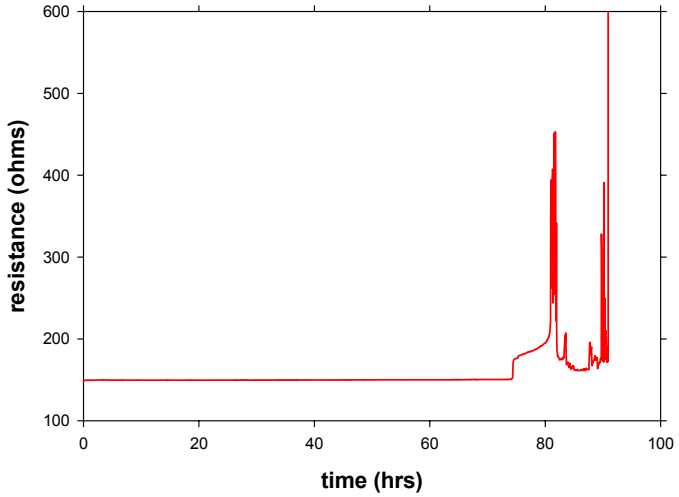
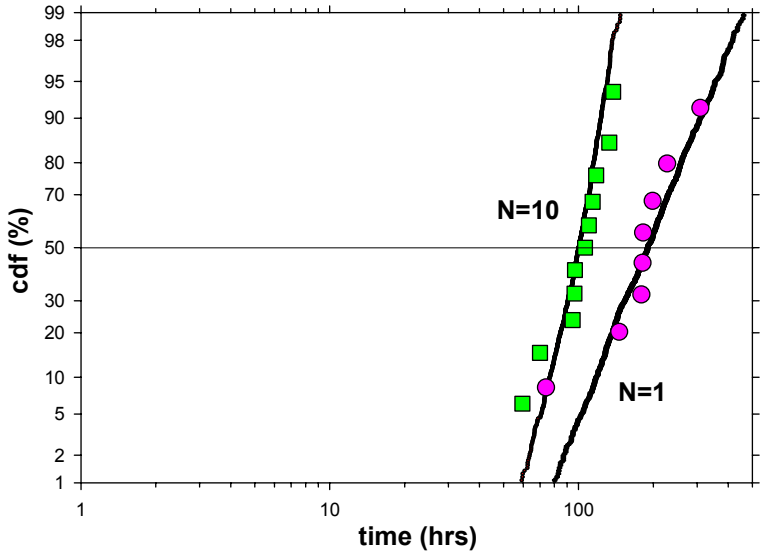
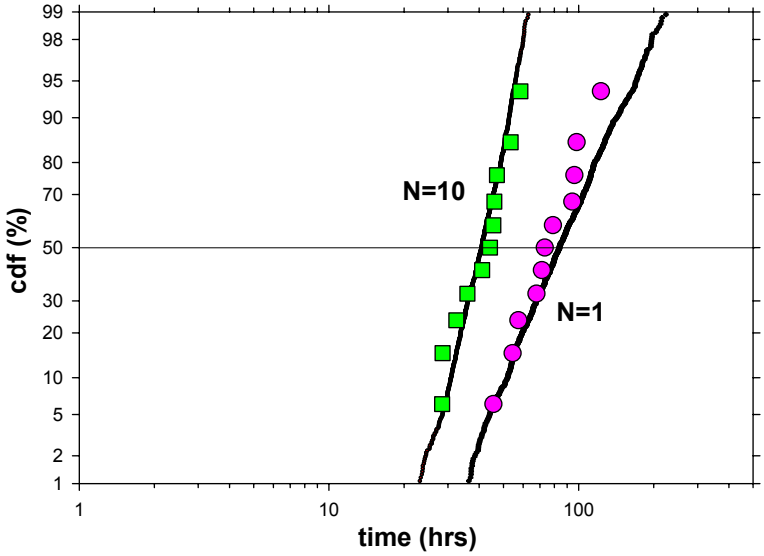


Figure 3.9: Three types of resistance traces were found for downstream M1 electron flows: (a) an abrupt resistance increase to infinity, (b) a step-like jump followed by a slowly increasing resistance, and (c) a step-like jump followed by resistance fluctuations. Such variations in the resistance behavior can be explained by the differences in the stability and integrity of barrier layers.

The temperature dependence of the median lifetime t_{50} for the 0.25μm downstream M1 EF test structures was also studied. The CDF plots for structures tested at 300°C, 325 °C and 350°C are shown in Figure 3.10(a)-(c), respectively. The failure data were simulated based on monomodal statistics. Figure 3.10(d) shows an Arrhenius plot of t_{50} vs. $1/kT$ obtained at 1.0MA/cm^2. In order to identify the dominant diffusion mechanism, the activation energy, Q, was determined from the slope of the best-fit line through the data using the Black's equation (Eq. 2.1). It was found that Q was around 1.0 eV, suggesting that mass transport responsible for EM failure in this particular Cu/dense CVD low k structure is dominated by interfacial diffusion at the Cu/SiCN cap layer interface. This agrees well with studies in [56, 75, 77-79].


99
98
95
90
80
70
50
30
20
10
5
2
1
cdf (%)
N=10
N=1
1
10
100
time (hrs)

(a) 300°C


99
98
95
90
80
70
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30
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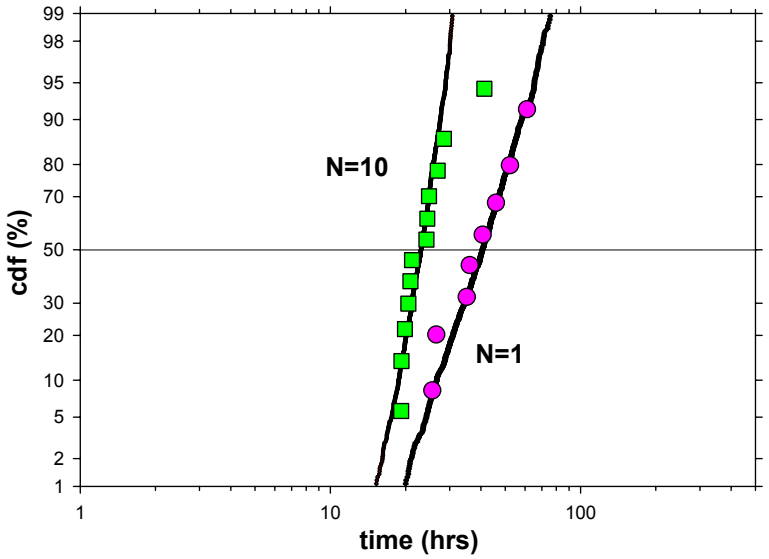
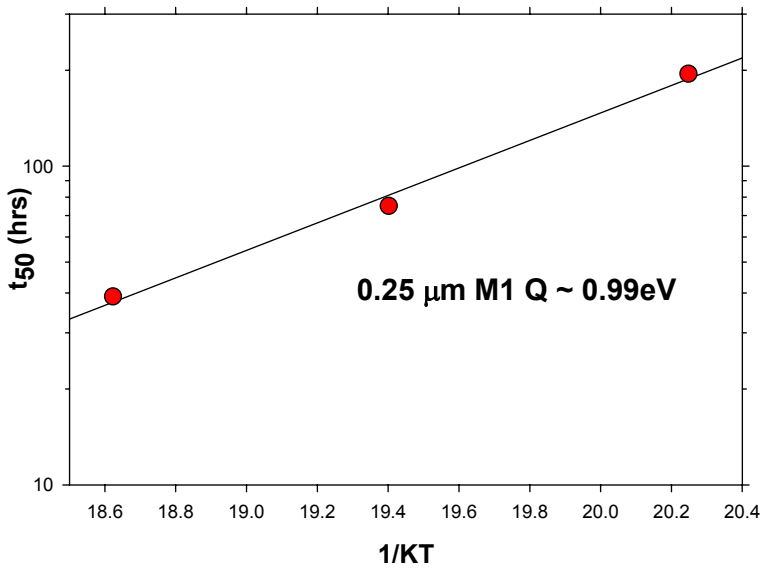
2
1
cdf (%)
N=10
N=1
1
10
100
time (hrs)

(b) 325°C



(c) 350°C



(d)

Figure 3.10: CDF plots of EM lifetime statistics for 0.25μm-wide M1 test structures at three different temperatures (a)-(c), where the solid symbols are the real lifetime data of $N = 1$ and 10 links and the small dotted line is generated by a WLA Monte Carlo simulation. Corresponding Arrhenius plot is shown in (d).

3.03.2.3 Discussion

In our experiment, intrinsic strong mode lifetime showed a systematic linear decrease with the line width scaling for both electron flow directions, i.e., upstream M2 and downstream M1, as shown in Figure 3.11.

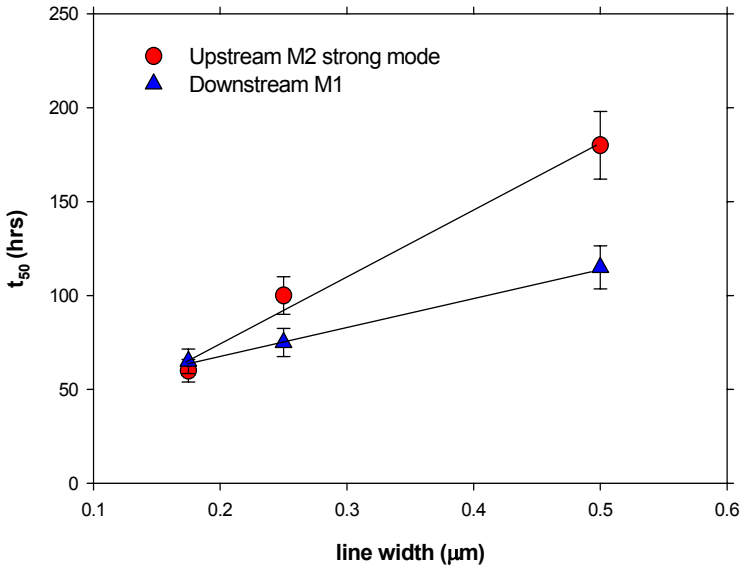


Figure 3.11: Plot of median lifetime t_{50} vs. line width for both electron flow directions. EM tests were conducted at T = 325 ^{o}C and j = 1.0 MA/cm^2. Only the strong mode failures were plotted for upstream M2 cases.

For the upstream M2 cases, it can be reasonably assumed that, with respect to the strong mode EM failures, their critical failure void volumes are very similar to those for the single damascene structures (Figure 3.1). This assumption is mainly based on the fact that the strong mode EM failures in these two cases are fairly similar: they are all trench voiding-related. The only structural difference between the single and the dual damascene structures lies in the presence or absence of a diffusion barrier layer between the trench

and the via. Specifically, in the dual damascene structure, such a layer is absent in integration. Therefore, a major variation for the upstream M2 cases is that occasionally a void growth may cut deep into the via. However, such a variation does not make much difference as it tends to be averaged out in the median time to failure t_{50} determination in this study. Another justification for such an assumption consists in the similarity of the dominant diffusion path. That is, the dominant void formation and mass transport process takes place along the M2 trench/cap layer interface, similar to that in a single damascene structure. Therefore, Eq. 3.4, which is valid for single damascene structures, can also be employed to provide a rough estimation of the strong mode EM lifetime τ in the M2 dual damascene Cu structure

$$\tau = \frac{kT\Delta L_{cr} h}{Z^* e \rho j D_{Cu/c} \delta_{Cu/c}} \tag{3.4}$$

where ΔL_{cr} is the critical depletion length to reach an observable resistance increase. From the equation, the EM life time for the strong mode is not directly related to the line width; rather, it is only related to the product of the critical depletion length ΔL_{cr} and the thickness h, provided that all the other parameters are kept constant. Therefore, any change in either the critical length or the thickness or both in the test structure will change the EM lifetime accordingly.

In this experiment, the thickness of the test structures remained constant for all different line widths. The EM lifetime therefore is only related to the critical length as the line width scales down in this case. Nevertheless, it should be noted that in a typical design, the critical depletion length ΔL_{cr} is almost linearly related to the via size, which usually decreases along with the line width. As a result, the observed EM lifetime in effect scales down almost linearly with the line width.

Weak mode via-related failures were identified for the upstream M2 cases. But such failures were not sensitive to the change of the line width, as they are more closely related to extrinsic process-related problems. For example, in our studies, it was found that such failures were related to a poor barrier open etch process. During this process, the recess of SiCN cap layer at the via bottom may become a potential void nucleation site. Voids growing at this site may eventually lead to via open failures during EM testing, as shown in Figure 3.12. A good process will considerably lower the probability of this type of failures. Unfortunately, as line width scales down, process control necessarily becomes more difficult. As a result, there is a possible indirect consequence of line width scaling: the increase of the weak mode failure rate. Our studies have revealed that the failure percentage for the smallest line width (0.175μm) reached 30%, much higher than the percentage for the other two line widths (0.25μm and 0.5μm) (Ref. Table 3.1).

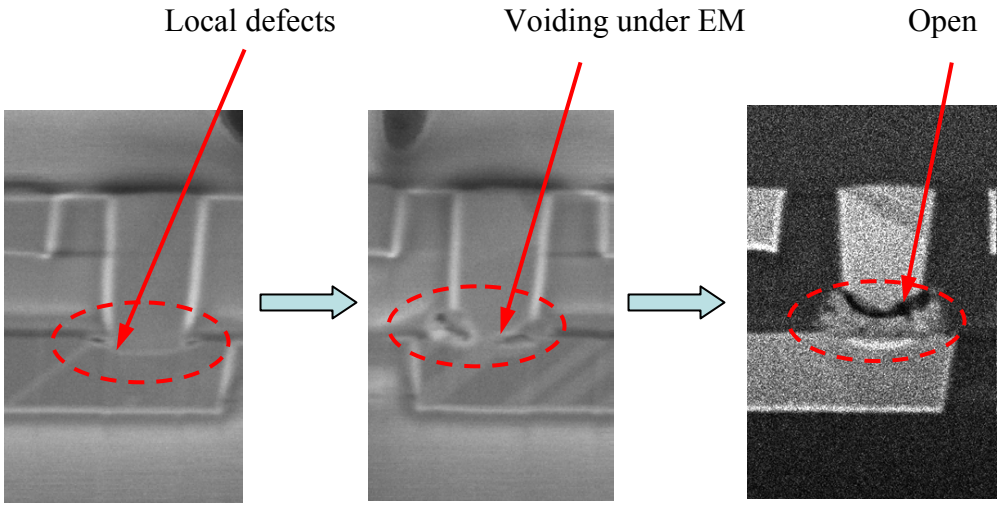


Figure 3.12: FIB image indicating that a bad via etch process can impact EM reliability through providing potential void nucleation sites.

For the downstream M1 cases, although failure distributions are statistically monomodal for all line widths, the situation in reality is more complicated. For example, different void locations can induce vastly different critical failure void volumes, as can be seen in Figure 3.13. If a void nucleates under the via, then the line width basically plays a similar role that it does in the upstream M2 cases. That is, the effects of the line width on the EM lifetime are mediated through the scaling of the via size. On the other hand, if a void starts to nucleate in the M1 trench away from the via, the scaling effects of the line width on the EM lifetime are less predictable, because potentially many other factors, such as the local microstructure and the grain orientation, may be related to the growth of the void and in turn the critical depletion length ΔL_{cr} and the EM lifetime. Therefore, much weaker line width dependence is observed due to a statistical distribution of the failure locations.

From the above discussion on the upstream M2 and downstream M1 cases, we can see that line width scaling per se does not automatically result in a shortened EM intrinsic lifetime. It only indirectly impacts the EM lifetime through the introduction of certain changes on some parameters that have a direct effect. Typically, as line width scaling involves the reduction of the line thickness and/or the via size, it may lead to the increase of the ratio of Cu/cap layer interface to the total line volume or the decrease of the critical depletion length, thereby lowering the EM lifetime.

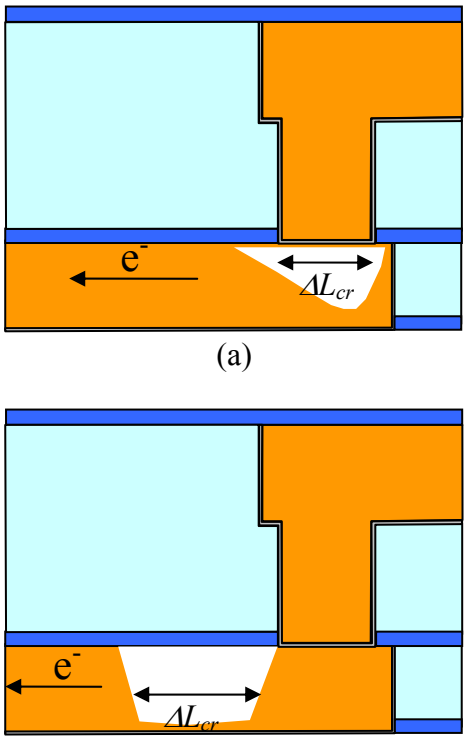


Figure 3.13: Critical failure void volume for the downstream M1 case: (a) the void grows directly underneath the via, or (b) the void grows away from the via in the M1 trench and a comparably larger void is required to cause a failure.

There are a number of possibilities for improvement on EM lifetime characteristics with line width scaling. One possibility involves the modification of the current interconnect structure design. For instance, since the reduction of the via size may directly lead to a shortened EM lifetime, we can consider the use of either a large via size or multiple vias, which in turn will increase ΔL_{cr}. As a result, a larger void will be needed to fail the Cu line and the EM lifetime will be increased accordingly. Nonetheless, this approach is not free from problems in that a large via size design essentially conflicts

with the scaling requirements: dimensional scaling almost invariably calls for the reduction of the via size.

Another method is the employment of a permeable barrier layer at the Cu line/via interface. Hu et al. [80-82] demonstrated that by thinning the barrier coverage at the via bottom, it is possible to achieve a continuous flow of Cu atoms across the Cu line/via interface, so that the voided region under EM can be constantly replenished with a large reservoir of supply. This may prevent a fatal void formation and thus extend the EM lifetime. However, mass transport under EM sooner or later will lead to the formation of some voids; and since the blocking barrier at the via bottom has been deliberately diminished, the control over the location of void formation is compromised accordingly. Thus, the location of the void becomes more unpredictable.

In this study, we define the interconnect failure as the first resistance surge. However, in practice, a total interconnect failure does not occur till there is an intolerable resistance increase or an open circuit resulting from void growth. The quality of the barrier layer plays an important role in determining the resistance traces after the first surge. Therefore, the barrier property is another issue that should be taken into consideration to improve EM lifetime. If we use thick stable barriers for the trench sidewall, the via bottom, and the via sidewall, then the barrier layers become more robust. Under such circumstances, in spite of some void formation, the current can still be forced through the barrier layer, which now effectively serves as a shunting layer. At the same time, a thickened and robust barrier layer may also prevent Cu diffusion along the Cu/barrier interface. But this approach has a major tradeoff as well: the increase of resistance for the whole structure essentially runs against the interconnect performance requirements.

Again, from the above discussion, we have already noticed that EM lifetime can be improved through modification of the interconnect structure design. On the other hand, dimensional scaling has also considerably increased the ratio of the Cu/cap layer interface to the total Cu volume in the interconnect lines. As the Cu/cap layer interface is the dominant diffusion path for EM mass transport in Cu interconnects, the relative significance of the interfacial diffusion becomes even more obvious. Therefore, another possible approach to improving the EM lifetime performance is through the reduction of the diffusivity along the Cu/cap layer interface. It was reported [77, 83] that improving the adhesion at the Cu/cap layer interface could extend the EM lifetime by suppressing interface diffusion and reducing the void growth rate. In addition, a number of modifications of the Cu properties through either alloying or metal overcoating [29-34, 55, 75, 79] have been reported.

Many different types of alloy interconnects have already been investigated, such as Cu(Mg), Cu(Ti), Cu(Sn), Cu(Zr), Cu(In), and Cu(Al). One major drawback of this method is that there is a considerable increase in Cu line resistivity, which conflicts with the electrical performance requirements [55].

Recently there has also been much interest in the development of selective metal overcoating, such as CoWP and Ta, to reduce interfacial diffusion and improve EM reliability. The activation energy for Cu capped with CoWP, Ta/TaN, SiN_x, and $SiC_xH_yN_z$ has been found to be 2.4 eV, 1.4 eV, 1.0 eV and 1.0 eV, respectively [75, 79]. It should be noted that 2.4 eV obtained for samples with CoWP cap is already very close to the value of Cu bulk self-diffusion. One of the challenges of this approach is that the CoWP or Ta overcoating should be, on the one hand, kept as thin as possible, and on the other hand, thick enough to effectively reduce the mass transport along the interface.

Besides, the added complexity of processing should be justified by the potential gains from the alterations of the Cu surface.

3.04 BARRIER THICKNESS SCALING

Generally, a robust Ta-based barrier layer is essential in that as an integrated part of the damascene structure, it not only prevents Cu diffusion into the surrounding dielectric but also positively contributes to the thermomechanical confinement to limit the EM mass transport. In addition, it also serves as a base layer for subsequent Cu seed deposition and electroplating, where processing defects in the barrier can easily lead to early failures to degrade EM reliability [3].

Dimensional scaling requires that the barrier thickness be reduced due to resistivity concerns. At the same time, the integration of low k materials is inevitable and the k value becomes increasingly small. In order to achieve smaller and smaller k values, porous low k materials have been introduced. It was reported [84-86] that deposition of a fully dense yet ultra thin barrier layers on the porous dielectric surface is extremely challenging. Under these circumstances, the thin barrier coverage and integrity becomes problematic and therefore its impact on EM lifetime characteristics has emerged as a serious reliability concern.

In our studies of the barrier thickness scaling effects, the test structures had a fixed Ta barrier thickness at the M1 level (175Å), but three different Ta barrier thicknesses at the M2 level (75Å, 100Å, or 175Å). And a porous MSQ low k material with an effective permittivity k of 2.3 was used as the interlayer dielectric.

In the following sections, both the intrinsic and the extrinsic effects of the barrier thickness scaling and the porous low k implementation on EM lifetime characteristics will be addressed. The study of the intrinsic effects will be focused on the median time to

failure t_{50} and the activation energy Q, and the study of the extrinsic effects will be focused on the early failure statistics and the degradation mechanism.

3.04.1 Intrinsic lifetime characteristics

The effect of barrier thickness scaling was measured using the LC test structures with upstream M2 electron flows. The CDF plot provided in Figure 3.14 indicates that the strong mode EM lifetime which was above 15% seemed to be relatively independent of the Ta barrier thickness. The observed slight increase in lifetime for the thinner Ta barrier samples can be attributed to a slightly lower current density due to a larger Cu cross-sectional area. In contrast, the early failures below 15% were found to spread toward shorter lifetimes with decreasing barrier thickness, which suggested an increase in defect-induced early failures with decreasing barrier thickness.

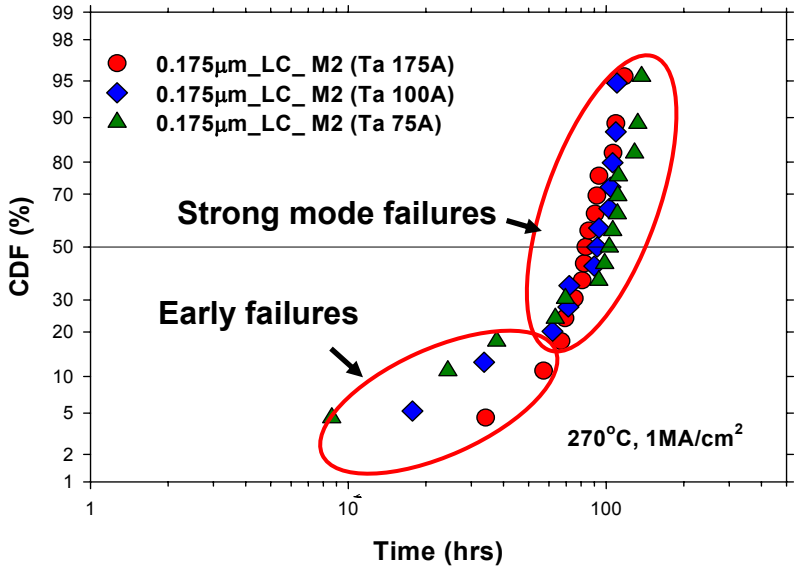


Figure 3.14: CDF plots of the LC structures with different barrier thicknesses for upstream M2 electron flows.

The t_{50} for the samples with different barrier thicknesses as a function of $1/T$ is plotted in Figure 3.15. The activation energy was found to be between 0.9 and 1.0 eV, and was independent of the Ta barrier thickness scaling.

The similarities in the intrinsic EM lifetime and the activation energy among the test structures with various barrier layer thicknesses indicate that Cu diffusion along the Cu/barrier layer interface was minimized and the interfacial diffusion at the Cu/cap layer interface remained the dominant mechanism of mass transport. This also agrees well with studies in [56, 75, 77-79].

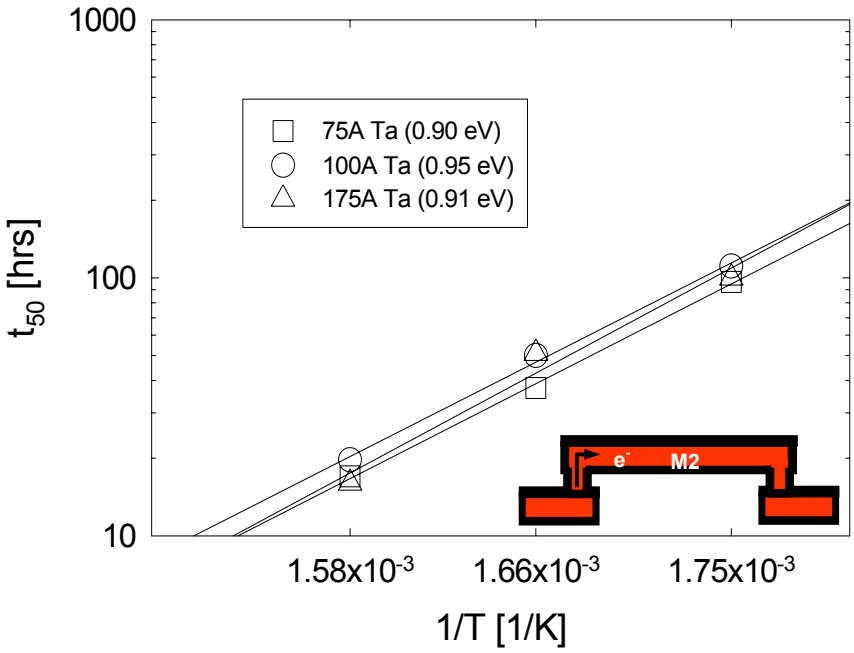
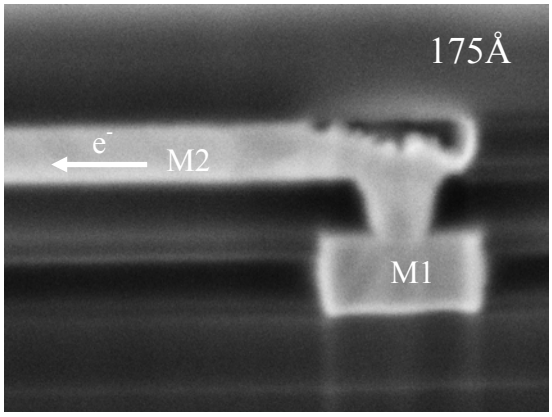
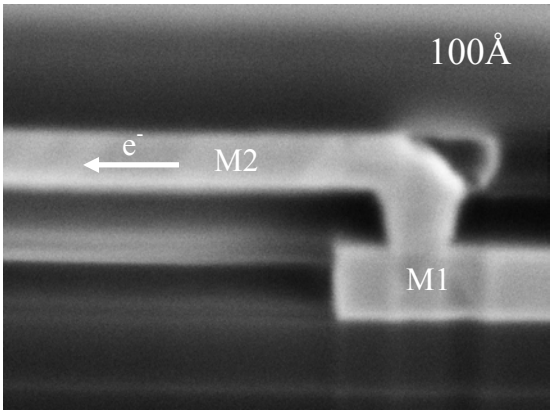


Figure 3.15: Median time to failure t_{50} as a function of testing temperature for structures with three different barrier thicknesses. EM testing was conducted at T = 330°C and j = 1.0 MA/cm^2 [87].

The FIB analyses on the test lines that failed above 15% revealed similar failure modes for all samples with different barrier thicknesses. Failures appeared to be related to trench voiding initiated at the Cu/SiCN cap layer interface (Fig. 3.16), where Cu mass transport determined the growth rate of the void and thus the EM lifetime. Once the void reached a critical size, regardless of the barrier thickness, most of the current would be shunted through the barrier, causing an appreciable resistance increase.



(a)



(b)

Figure 3.16: Failure analyses on structures with Ta barrier thicknesses of (a) 175Å and (b) 100Å. Both samples showed a similar void formation mechanism.

3.04.2 Extrinsic failures and degradation mechanism

To further investigate the EM early failure statistics, experiments were conducted on the EF test structures at 300°C with a current density of 1.0 MA/cm^{2}. The CDF plots of samples with a Ta thickness of 175Å and 100Å are shown in Figure 3.17(a) and (b), respectively.

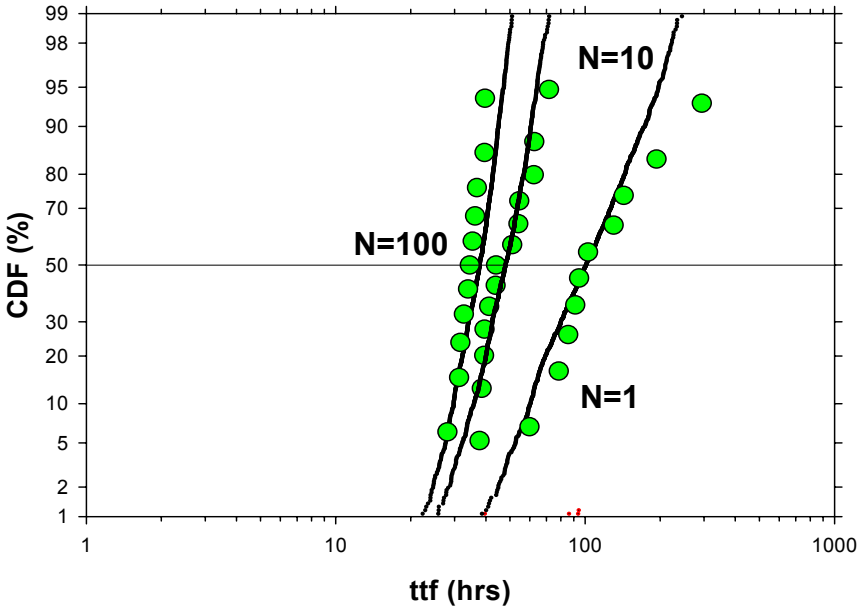
In Figure 3.17(a), approximately linear behavior is identified for multi-link structures with N equal to 1, 10, and 100, suggesting a monomodal failure distribution for samples with a Ta barrier thickness of 175Å. As N increases, the CDF plot shifts toward a shorter lifetime, corresponding to a higher probability of failure within a shorter time. This suggests that only strong mode void formation is responsible for the failures. In contrast, for samples with a Ta barrier thickness of 100Å, a bimodal failure distribution is present, as can be seen from the branching in Figure 3.17(b). The weak mode seems to dominate the early failure statistics for the N = 100 links.

It is worth noting, however, that the failure statistics for N = 1 and N = 10 links are similar for both samples with a Ta barrier thickness of 100 and 175Å, indicating that the strong mode statistics are not affected by the change of the barrier thickness. From a Monte Carlo simulation based on a bimodal failure distribution, the early failure percentage can be deduced to be around 0.6%. Results from the EF structures with a Ta barrier thickness of 75Å also indicate a bimodal failure distribution, with early failures dominating the N = 100 links, which is similar to the statistics of the test structures with a Ta barrier thickness of 100Å.

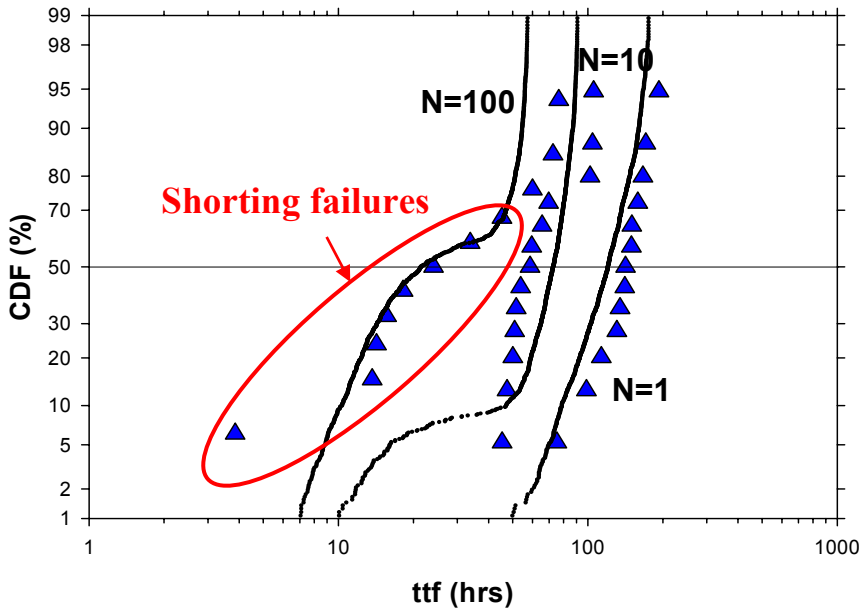
To investigate the weak mode early failure mechanism, the resistance traces of the early failure samples (circle-marked samples in Figure 3.17b) were further examined. It was found that all these structures, except one, failed due to shorting with the adjacent extrusion monitor line. Figure 3.18 plotted the resistance traces for the test structures of N

= 100 links with a Ta barrier thickness of 100Å. A small number of these links failed by a resistance increase, which represents the strong mode voiding-related failure (Figure 3.18(a)). In contrast, the majority of the N = 100 links failed because of a step-like resistance drop (Figure 3.18(b)). This resistance drop is believed to be associated with the current shunting through the wide extrusion monitor line due to a shorting failure.

Test structures failed by early shorting failures were examined using FIB and TEM. From the cross-sectional FIB image shown in Figure 3.19, it appeared that Cu diffused through the thin barrier into the porous low k ILD and touched the adjacent extrusion monitor line, causing a shorting failure in the test structures with a Ta barrier thickness of 100Å. Again, the TEM image of another structure with a similar barrier thickness revealed a dark outer metal layer adjacent to a voided Cu line, as shown in Figure 3.20. The formation of this outer metal layer is probably due to the Cu out-diffusion through some weak spots, such as pinholes, in a thin Ta barrier. Such a failure had been previously reported for ultra low k materials [88], and we believe that it is caused by poor structural integrity of thin barriers under a large electrical field. This type of early failure mechanism is expected to occur more frequently as the electrical field increases with further scaling of the line spacing and the barrier thickness unless the barrier integrity is well maintained.

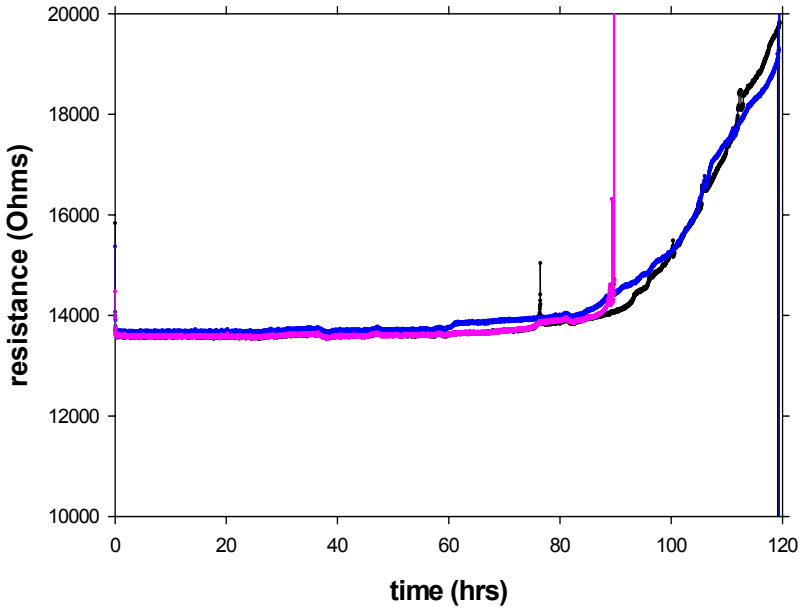


(a) Ta 175Å

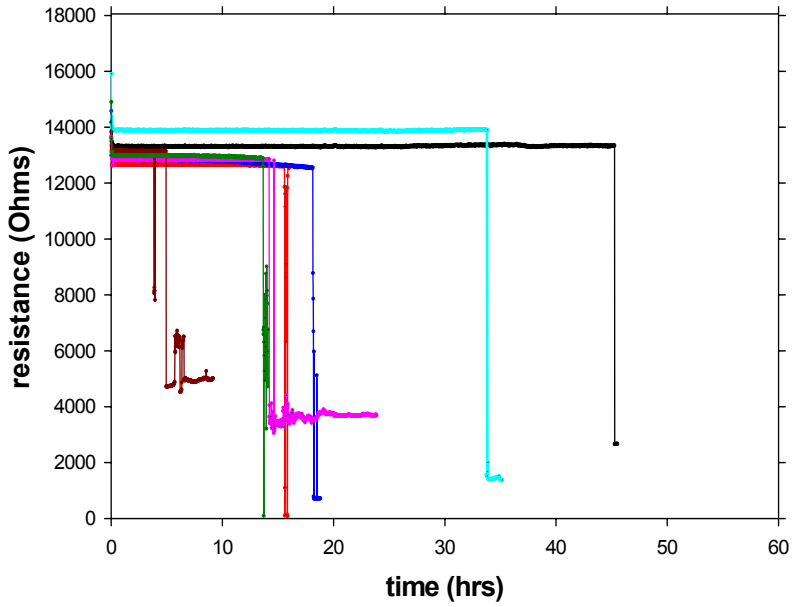


(b) Ta 100Å

Figure 3.17: CDF plots of EF structures with Ta barrier thicknesses of (a) 175Å and (b) 100Å for upstream M2 electron flows. EM testing was conducted at $T = 300$ ^{o}C and $j = 1.0$ MA/cm^2.



(a)



(b)

Figure 3.18: Resistance traces indicated that (a) some of the $N = 100$ links failed by cathode voiding and a resistance increase, and (b) most of the $N = 100$ links failed by shorting with adjacent extrusion monitor lines and a resistance drop.

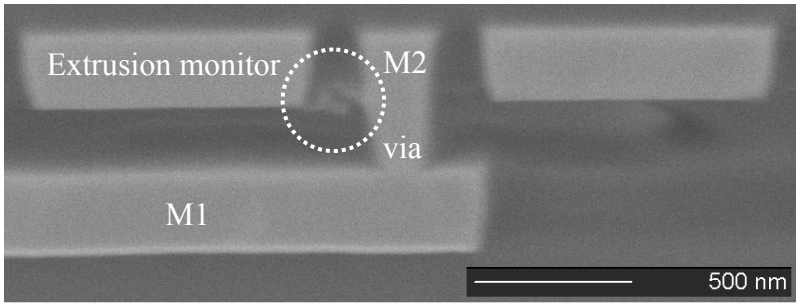


Figure 3.19: FIB image showed Cu diffused out from the thin barrier and touched the adjacent extrusion monitor line, causing a shorting early failure in test structures with a Ta barrier thickness of 100Å [44].

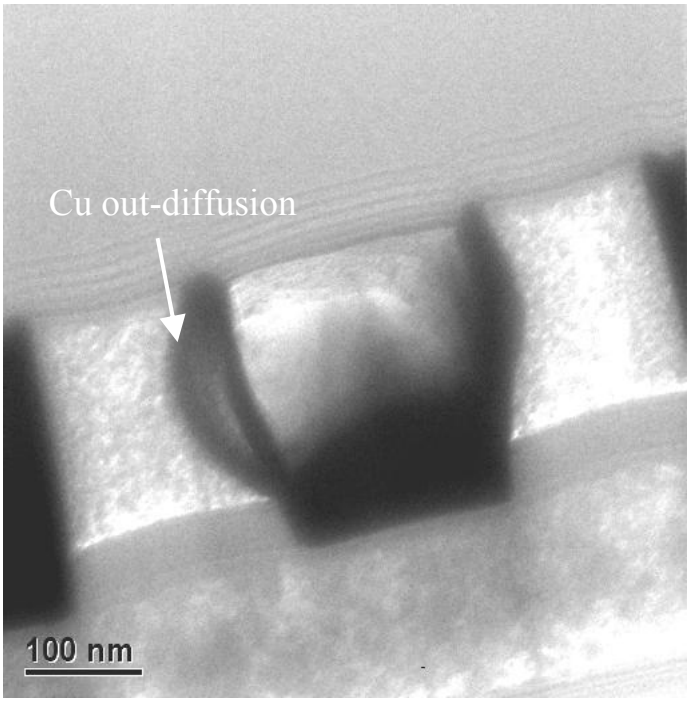


Figure 3.20: TEM image revealed a dark outer metal layer adjacent to the voided Cu line, indicating Cu out-diffusion through the thin Ta barrier. The test structure has a Ta barrier thickness of 100Å [44].

In summary, barrier thickness scaling does not have a major impact on intrinsic EM failure characteristics (median time to failure t_{50} and activation energy Q) as long as the integrity of the barrier is not compromised. Unfortunately, with the adoption of porous low k materials and increasingly thinner barriers, it is becoming ever more challenging to maintain the barrier integrity. Indeed, the observation that early failures spread toward shorter lifetimes with thinner barriers suggests that there is an increase in defect-induced early failures among the samples with thin barriers. And subsequent FIB and TEM analyses have also identified defects related to Cu out-diffusion, which caused line shorting and lifetime degradation.

3.05 ELECTROMIGRATION AND PROCESS

So far we have studied the impact of dimensional scaling on EM reliability with only one process taken into consideration. Nonetheless, with dimensional scaling, various new processes will have to be introduced. Changes in a process may cause changes in the properties of the copper, the cap layer, or the barrier layer, or lead to alterations of the via-to-line profile. Such changes can readily influence the EM lifetime characteristics [3]. Accordingly, while scaling effects deserve much attention in our studies, it is also necessary to study the influence of different processes on EM reliability.

3.05.1 Improvement of via process for upstream M2 cases

In the traditional preclean-first via process for the M2 structures, after a via has been opened and the lower metal layer has been exposed, there is a preclean step followed by the barrier and Cu seed deposition. This preclean step is adopted to ensure a better barrier/Cu interface through the removal of the etch residues as well as the Cu

oxide from the via bottom. As a result, the Ar preclean tends to sputter Cu from the via bottom onto the sidewalls, which can degrade the barrier/ILD interface at the lower sidewalls, and create a weak spot for void nucleation to induce EM early failures (Figure 3.21).

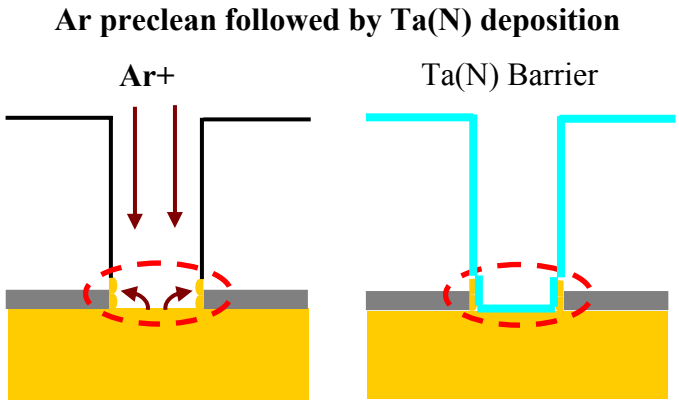


Figure 3.21: A schematic diagram of an aggressive Ar^+ preclean sputtering Cu from the via bottom onto the lower sidewalls.

A barrier-first via process, on the other hand, does not have such a problem. Figure 3.22 presents a flow chart of this process [49]. Specifically, after degassing, a Ta/TaN barrier is deposited first to prevent via sidewall contamination, followed by RF resputtering of the deposited barrier film in order to remove Ta as well as the oxide and etch residues from the via bottom. After that, Ta barrier deposition is applied for a second round, and finally, Cu electroplating is carried out. Using this approach, via sidewall Cu sputtering is effectively avoided. A clean barrier/ILD interface and a clean barrier/Cu interface are obtained accordingly.

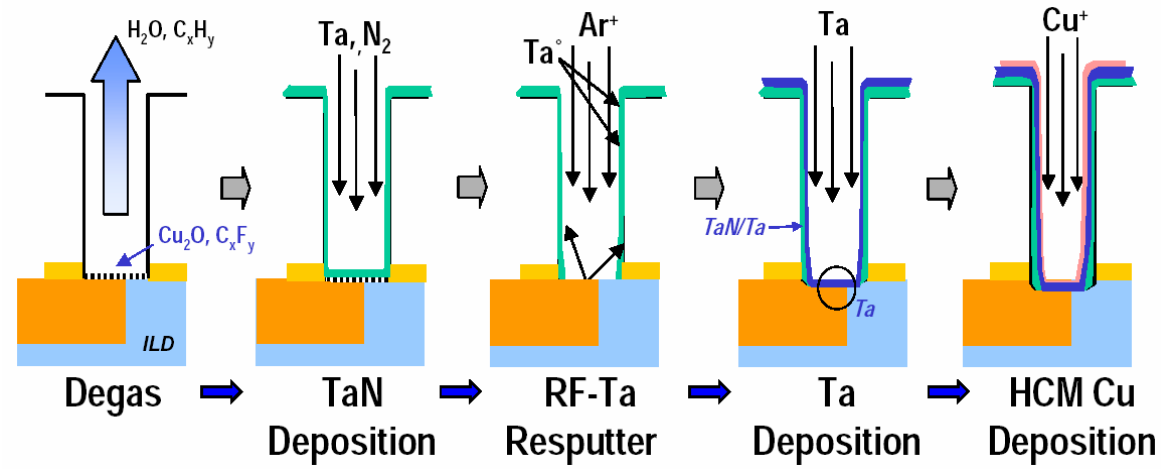


Figure 3.22: Barrier-first via process [49].

To study the impact of these two processes on EM reliability, multi-link M2 structures with N = 200 links were used because of their sensitivity to via-related early failure detection. Different test structures were fabricated with either a barrier-first via process or a preclean-first via process. With each process, there are two electroplating chemistry splits available. In this case, the test line width was 0.3μm, and SiO_2 was the ILD material. The EM testing was conducted at $T = 350^{o}C$ and j = 1.0 MA/cm^2.

The CDF plots obtained for samples fabricated with different processes are presented in Figure 3.23. It was found that the barrier-first via process increased the EM lifetime by an order of magnitude when compared with the preclean-first via process. However, the variation in the electroplating chemistry did not affect the early failure statistics.

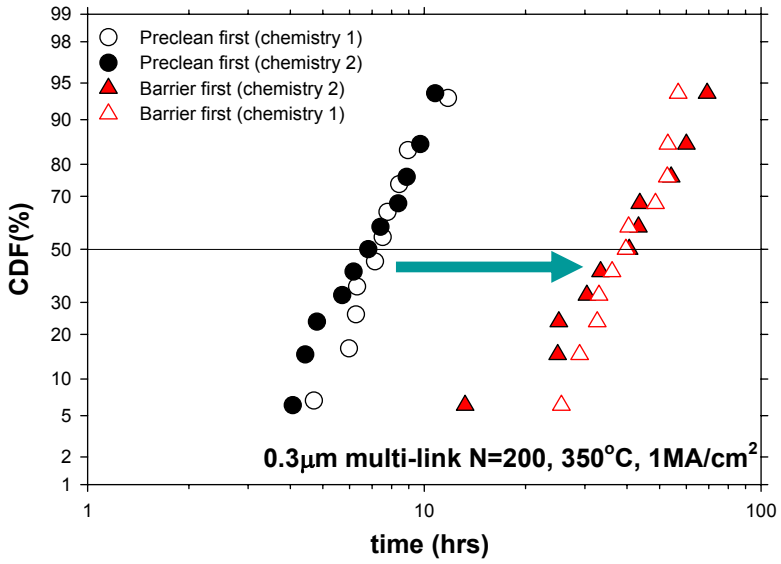
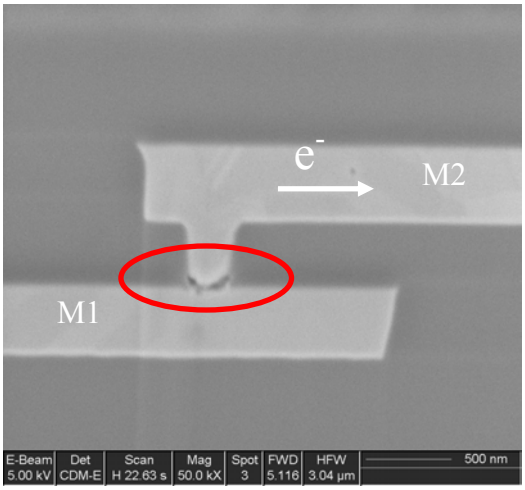


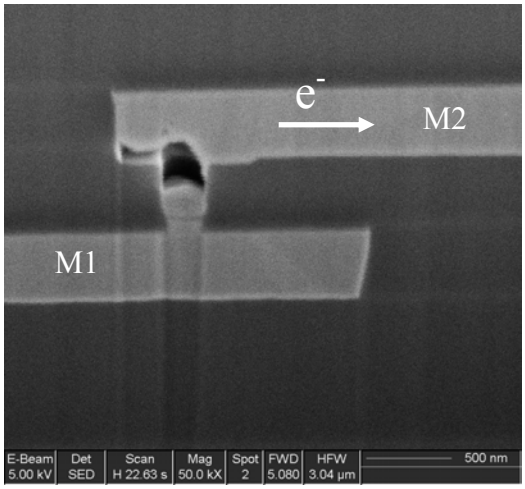
Figure 3.23: CDF plots of multi-link structures with preclean-first via process vs. barrier-first via process for upstream M2 electron flows. EM testing was conducted at $T = 350^{o}$C and $j = 1.0$ MA/cm^2, with SiO_2 used as the ILD material.

From the FIB failure analyses, it was found that for the preclean-first process, samples with different electroplating chemistries were both failed by via bottom early failures, as can be seen from Figure 3.24(a). In contrast, for the barrier-first process as shown in Figure 3.24(b), the early failures due to sputtered Cu onto the sidewalls were eliminated, and the via bottom was intact. Nevertheless, this process is not yet fully optimized, as there are still some via-related failures at the via-to-line connections.

In some other unpublished studies, we have also found that, with a fully optimized barrier-first process, even the via-related failures could be totally eliminated, and that as a result all the failures resulted exclusively from the trench voiding along the Cu/cap layer interface.



(a)



(b)

Figure 3.24: Failure analyses on (a) structures with a preclean-first via process where early failures can be attributed to Cu sputtered onto lower barrier sidewalls; and (b) structures with a barrier-first via process, which demonstrated no via bottom related failures.

3.05.2 Improvement of via process for downstream M1 cases

The application of a new barrier resputtering process has also been investigated for the M1 structures using the LC test structures with a test line width of 0.175μm and a porous MSQ low k material as the ILD material. They were fabricated with one of the two different barrier deposition processes, DEP1 and DEP2. Unlike DEP1, which represents a conventional PVD barrier deposition process, a resputtering step is introduced in DEP2 to improve the bottom via coverage. Specifically, after the deposition of the barrier layer, this resputtering step is taken with the bias power turned on to redistribute the barrier layer more evenly at the sidewall of the via bottom. The bottom via coverage is improved in this way accordingly.

The CDF plots obtained for the LC structures tested at 270ºC under 1MA/cm^2 are given in Figure 3.25 with a downstream M1 electron flow. As can be seen, the samples processed using DEP2 showed a more than two-fold improvement of lifetime over those processed using DEP1.

FIB failure analyses revealed two distinct types of void locations and degradation mechanisms for the two different processes. In the case of DEP1, the dominant mechanism was that voids first nucleated at the Cu/cap interface in the vicinity of the via and then continued to grow under the via. When the Cu underneath the via was depleted, the current path was thus broken, resulting in an open circuit. Figure 3.26(a) is an illustration of such a failure. It is clear that there is a very thin slit-like void at the via/M1 interface, which only requires a small amount of metal depletion and thus a short time to fail. It should be noted that the time needed for this type of failure can vary considerably, depending on the void shape and size at that location. For example, a relatively long failure time may also be possible for a void with morphology shown in Figure 3.8(a). The

failed samples show a fairly large void in the M1 volume underneath the via, resulting a relatively long time to fail.

The dominant void formation mechanism with DEP2 was rather different. In this case, voids nucleate either near the trench edge (Figure 3.26(b)), or away from the via in the M1 trench (Figure 3.26(c)). Under such circumstances, a relatively large void is needed in order to completely remove the Cu across the line to cause a resistance surge. Therefore, the EM failure time tends to be fairly long.

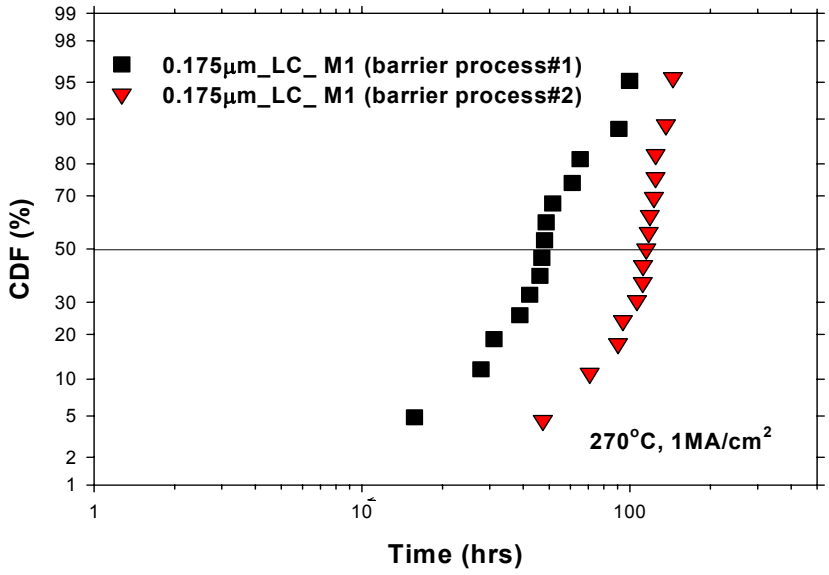


Figure 3.25: CDF plots of the LC structures with different barrier deposition processes for downstream M1 electron flows of a fixed Ta barrier thickness of 175Å. EM testing was conducted at $T = 270^{o}C$ under $j = 1.0$ MA/cm^2. In this case, the testing line width was 0.175µm, and a porous MSQ low k material was used as the ILD material.

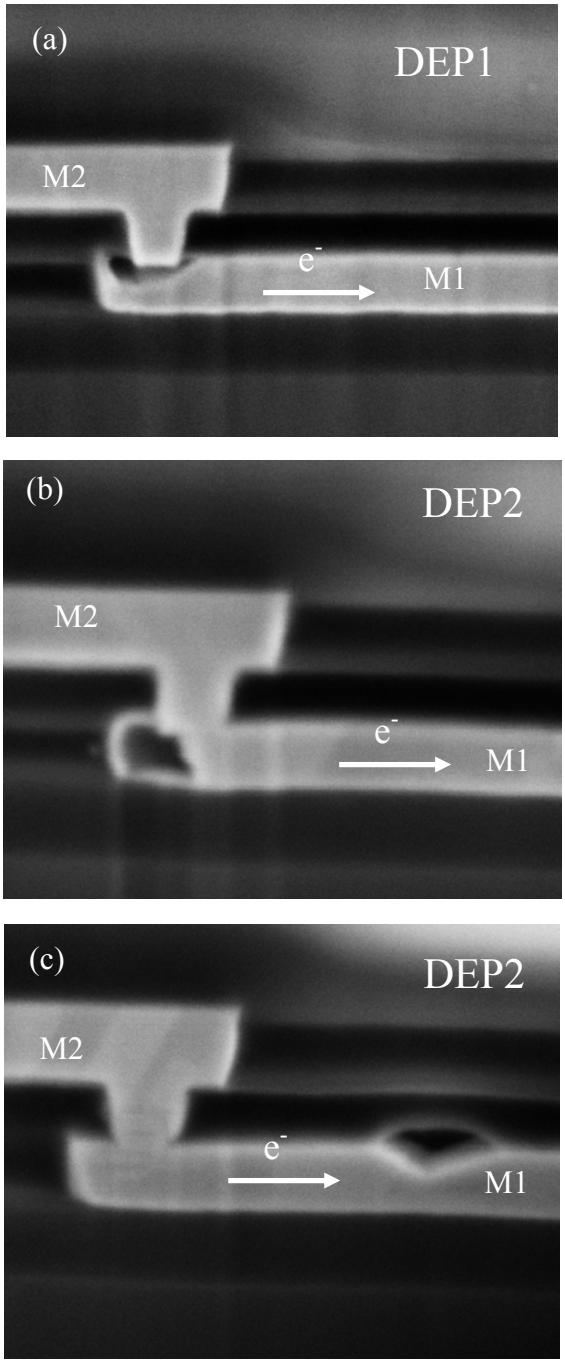


Figure 3.26: FIB images revealed EM void formations at various sites: (a) a slit-like void underneath the via for DEP1, (b) voiding at the trench edge, or (c) voiding away from the via in the M1 trench.

3.06 SUMMARY

In this chapter, the impact of scaling on EM lifetime characteristics was investigated. In terms of interconnect dimensional scaling, we examined the metal line width/via size scaling (0.5μm, 0.25μm, and 0.175μm) and barrier thickness scaling (175Å, 100Å, and 75Å). The implications of adopting low k materials and new processes involved in the scaling have been discussed as well.

For the upstream M2 cases, the EM lifetime scaled linearly down with line width for the intrinsic strong mode failures, and the weak mode failures were independent of the line width and tended to be process-related. For the downstream M1 cases, a weak line width dependence was identified due to mixed void locations. It is concluded that line width scaling does not automatically lead to reduced EM intrinsic lifetime by itself. Instead, its impact is manifested indirectly through changes of some parameters, $\Delta L_{cr} \times h$, for example, that have a direct effect on the EM lifetime. In general, however, as line width scaling involves the reduction of the line thickness or the via size, it will increase the ratio of Cu/cap layer interface to the total line volume and decrease the critical depletion length. Both changes will reduce the EM lifetime.

Barrier thickness scaling does not have a major impact on intrinsic EM failure characteristics (t_{50}, and Q) as long as the integrity of the barrier is intact. In reality, nevertheless, with the implementation of porous low k materials and increasingly thin barriers, maintaining barrier integrity is becoming a difficult task. EM results showed that early failures shifted toward shorter lifetimes for samples with thinner barriers, suggesting that there is an increase in defect-induced early failures in these samples. Further, Cu out-diffusion-related defects have been identified through FIB and TEM analyses, leading to lifetime degradation and line shorting.

To meet the scaling requirements, improvement on integration process should remain one of the top priorities. Our studies have found that process-induced via-related defects have a significant impact on both the upstream M2 and the downstream M1 EM reliability. Without a good process control, interconnect scaling will become very difficult.

Chapter 4: Impact of Scaling on Electromigration Threshold

4.01 INTRODUCTION

The idea of the "critical length effect" or the "Blech length effect" was first introduced by Blech, who proposed the concept of stress-induced backflow [15]. Blech reported that with a diffusion barrier, the accumulation of Al atoms at the anode end of the metal lines generates a stress gradient which opposes the EM driving force. This stress gradient produces a backflow atomic drift. According, the net drift velocity, v_d, is given by

$$v_d = v_e - v_b = \frac{D_{eff}}{kT}\left(Z^* e\rho j - \Omega \frac{\Delta\sigma}{L} \right) \tag{4.1}$$

where v_e is the atomic drift velocity due to EM, v_b is the backflow atomic drift velocity, Ω is the atomic volume, L is the metal length, and $\Delta\sigma/L$ is the backflow stress gradient along the line length. Blech pointed out, by observing the void motion in unpassivated Al lines, that v_d became zero at a particular product of current density and metal length, $(jL)_c$. This product was referred to as the threshold or critical product for EM. Defining in this way, there is no EM damage below the critical $(jL)_c$ product. The importance of this idea for circuit design has long been widely recognized, and a number of studies have been performed to investigate the critical length effects in Al(Cu) and Cu interconnects [40-43, 61-62, 89-91].

With Al-based interconnects, understanding of the critical length is largely based on the discussion of the resistance saturation. In case of voiding, the stable overlayer and underlayer in the interconnect structure may still serve as an alternative current path,

thereby allowing the void to continue to grow. The resistance saturation is reached when there is a balance between the EM driving force and the backflow stress. Any line that is longer than the critical length is bound to fail before the resistance saturation can ever be reached. With Cu interconnects, however, there are a number of distinct characteristics. First, voids can readily nucleate at the Cu/cap layer interface, so if the thin barrier layers cannot reliably serve as the shunting layers, the interconnect lines can fail when voids reach a critical size. Second, with the introduction of the low k materials that are more compliant compared with the oxide-based materials, the backflow stress is considerably reduced. As a consequence of these factors, the critical length effect becomes a more complicated issue in Cu interconnects.

In this chapter, some basic understanding on the critical length effect in Cu damascene interconnects will first be provided. Then the impact of scaling on the threshold $(jL)_c$ product will be studied in Cu/porous low k interconnects using a statistical approach. Specifically, the effects of barrier thickness scaling and the barrier process alterations will be examined. To analyze the observed experimental results, we consider the dielectric confinement effect in terms of two parameters: the critical failure void volume and the effective bulk modulus B. And 3-D FEA modeling was used to evaluate the parameter B.

4.02 UNDERSTANDING OF CRITICAL LENGTH EFFECT IN COPPER INTERCONNECTS

The critical length effect needs to be discussed together with the kinetics of stress buildup and void formation process in Cu interconnects.

Under EM, atoms move from some sections of the line to others, with the total number of atoms unchanged. Consequently, some locations have a net accumulation of atoms whereas others have a net depletion of atoms. In the former case, the local stress

becomes more compressive, while in the latter case, the local stress becomes more tensile (Figure 4.1).

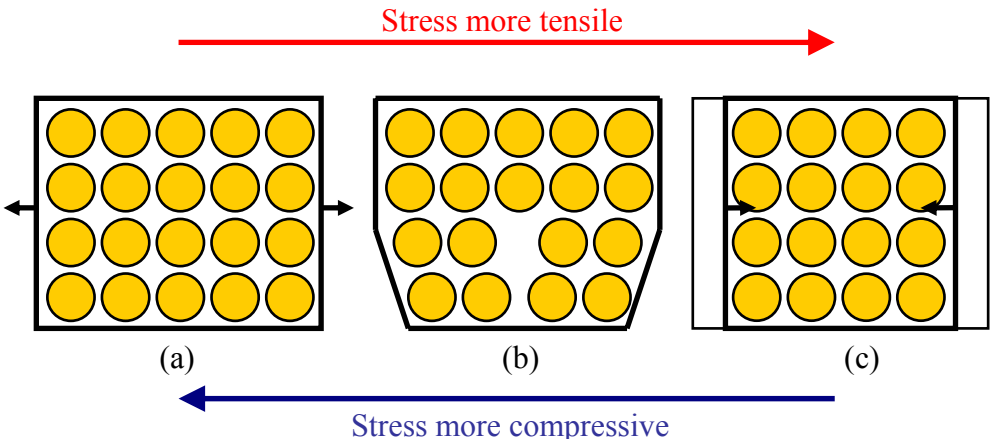


Figure 4.1: Stress buildup due to EM in a confined interconnect line. At sites where there is a net depletion of atoms, the local stress becomes increasingly tensile; and at sites where there is a net accumulation of atoms, the local stress becomes increasingly compressive [92].

The relative change in the concentration of the atomic lattice sites dC/C corresponds to the change of the hydrostatic stress $d\sigma$. This can define an effective bulk modulus B as [93]

$$\frac{dC}{C} = \frac{-d\sigma}{B} \tag{4.2}$$

where B is a function of the surrounding ILD material, interconnect geometry, and metallization.

In practice, there are two situations where a Cu interconnect line does not fail: either there is no void nucleation, or a nucleated void may grow to a saturation size and no further EM damage follows.

4.02.1 Criteria for no void nucleation

In Figure 4.2, the initial state of Cu line with a uniform thermal stress σ_0 is given at time t_0. Under EM mass transport, a small tensile stress builds up at the cathode end at t_1, with a corresponding compressive stress at the anode end. In the case when void nucleation does not occur, the stress will continue to develop until it reaches a steady state t_3 when there is finally a uniform stress gradient along the length of the line. Under such circumstances, the maximum tensile stress σ in the line is less than a certain critical level $\sigma_{crit,nuc}$. This condition can be expressed alternatively by a critical product $(jL)_{crit,nuc}$, below which void formation does not occur. This $(jL)_{crit,nuc}$ can be obtained by solving Eq. 4.1 with $v_d = 0$, that is, when the drift velocity is zero and the forward and the backward flows are canceled out against each other. Therefore

$$\left(jL\right)_{crit,nuc} = \frac{\Omega \Delta\sigma_{crit,nuc}}{Z^* e\rho} \tag{4.3}$$

where $\Delta\sigma_{crit,nuc} = 2\left(\sigma_{crit,nuc} - \sigma_0\right)$.

For Cu interconnects, the critical stress difference for void nucleation, $\Delta\sigma_{crit,nuc}$, is typically very small, and voids nucleate readily at the Cu /cap layer interfaces. Compared with the $\Delta\sigma_{crit,nuc}$ of 600 MPa observed for Al-based interconnects, the $\Delta\sigma_{crit,nuc}$ was found to be less than 41 MPa for SiO_2-based Cu interconnects and even lower for low k

materials [40, 42-43, 94]. From Eq. 4.3, it can be seen that the $(jL)_{crit,nuc}$ found in this way in turn tends to be too small to be practically useful for IC design.

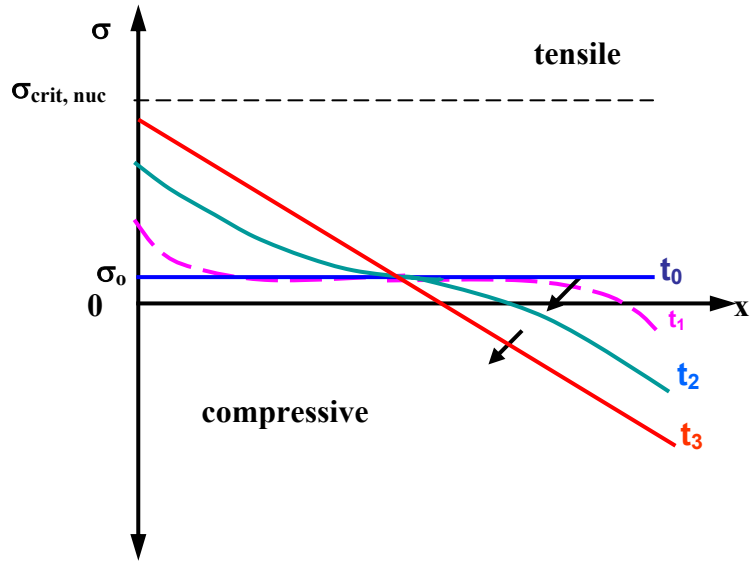


Figure 4.2: Stress evolution in confined Cu line under EM as a function of time. σ_0 is the initial thermal stress. The stress stays below the critical stress for void nucleation $\sigma_{crit,nuc}$, and voids do not nucleate.

4.02.2 Criteria for void growth saturation

Figure 4.3 provides a description of the stress buildup process in the case of void growth saturation. The initial state of Cu line with a uniform thermal stress σ_0 is again given at time t_0. A small tensile stress develops at the cathode end at t_1, while a corresponding compressive stress builds up at the anode end under EM. With continuing EM mass transport to t_2, the tensile stress at the cathode end exceeds a critical value for void nucleation, or the product of the current density and the line length (jL) exceeds the critical (jL) product, then void nucleation results. Once a void is formed, the local stress at the void surface drops to zero, and the stress in the Cu nearby quickly decreases as the

void grows while the compressive stress in the Cu line away from the void continues to increase as shown at t_3 and finally reaches a steady state at t_4.

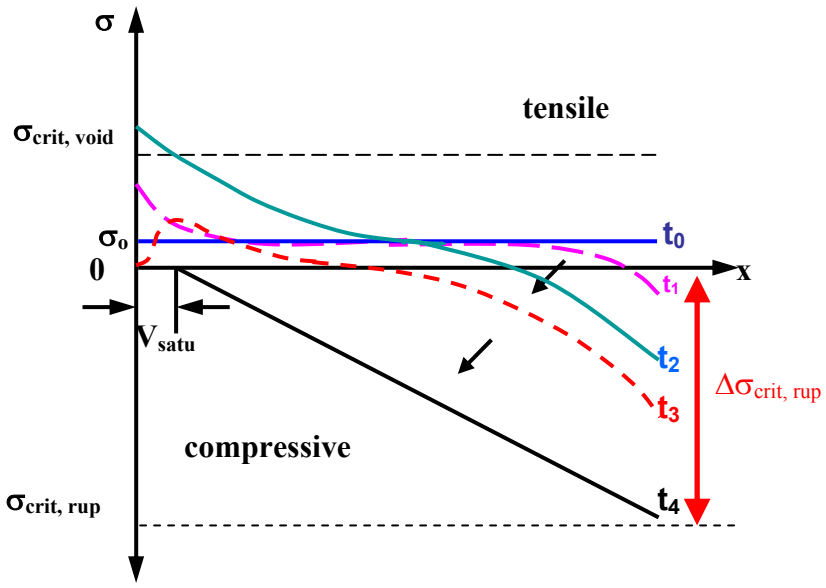


Figure 4.3: Stress evolution in confined Cu line under EM as a function of time. σ_0 is the initial thermal stress. When the tensile stress exceeds the critical stress for void nucleation $\sigma_{crit,nuc}$, a void nucleates. Eventually, the EM driving force is balanced by the backstress force, the void growth saturates.

The saturation void volume is defined as the volume of a void when the stress of the interconnect line reaches a steady state, where the backflow stress can fully compensate the EM mass transport driving force and no further void growth occurs. Based on the void growth kinetics, the saturation void volume for an interconnect line with a given length L_i in the steady state can be estimated as [70-71]

$$V_{satu,i} = \frac{AZ^* e\rho j L_i^2}{2\Omega B} \tag{4.4}$$

The equation shows that the saturation void volume becomes larger as the interconnect line length increases, and that any given interconnect line length has a specific saturation void volume at a given current density.

Under such a circumstance, an interconnect line that does not fail needs to simultaneously satisfy two conditions: (a) its maximum compressive stress at the anode end does not exceed the critical yield or the rupture stress of the surrounding dielectric material; and (b) its saturation void volume at the cathode end is less than the critical failure void volume, i.e. the threshold void volume when EM failure takes place as mentioned in Chapter 3. If either of these two conditions is not met, the interconnect line is bound to fail.

Provided that the interconnect line is failed by the anode extrusion before the void grows to its critical failure volume at the cathode end, the critical $(jL)_c$ product is calculated by

$$\left(jL\right)_{crit,rup} = \frac{\Omega\sigma_{crit,rup}}{Z^* e\rho} \tag{4.5}$$

where $\sigma_{crit,rup}$ is the critical yield or rupture stress of the surrounding dielectric material. It should be noted that once a void is formed at the cathode end, the maximum compressive stress at the anode end is more than doubled compared with the case of no void nucleation. Such a change in the compressive stress leads to a substantial increase in the possibility of anode extrusions.

Assuming that there is no extrusion failure at the anode end, from the second condition, it is clear that the interconnect line will never fail if its saturation volume is smaller than the critical failure void volume. On the other hand, if the saturation void volume is greater than the critical failure void volume, then its corresponding

interconnect line will fail before the void can ever reach its saturation point. The critical line length L_c in this case is the length at which the saturation void volume equals the critical failure void volume (Figure 4.4),

$$V_{satu,i} = V_{crit,void} \tag{4.6}$$

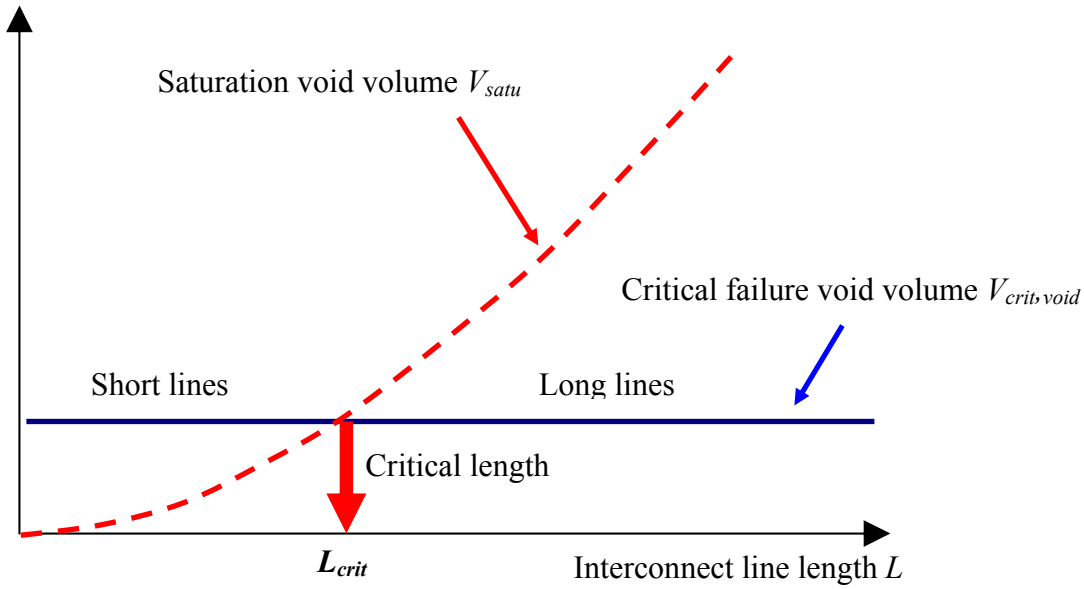


Figure 4.4: Saturation void volume V_{satu} and critical failure volume $V_{crit,void}$ as a function of interconnect line length L, with the assumption that $V_{crit,void}$ is independent of L, and only dependent on the line geometry of the cathode end.

In this case, there are two determining factors for the critical $(jL)_{crit,void}$ product: the critical failure void volume $V_{crit,void}$, and the effective bulk modulus B.

From the discussion above, we can see that a number of criterion can be used for the critical $(jL)_c$ determination: no void nucleation, no anode end extrusion or voiding saturation. However, since voids readily form at the Cu/cap interface and anode extrusions do not occur frequently, we consider voiding saturation as the main criterion for determining the critical $(jL)_c$ in our studies.

4.03 EXPERIMENTAL RESULTS FOR CRITICAL $(JL)_C$ DETERMINATION

In this section, we will examine the impact of the barrier thickness scaling and the barrier process changes on the critical $(jL)_c$ product in Cu dual damascene interconnects.

In these experiments, the ILD was a porous MSQ material with an effective permittivity k of 2.3. Ta barriers of three different thicknesses, 75 Å, 100 Å, and 175 Å, were integrated at the M2 level. In addition, two barrier deposition processes, DEP1 and DEP2, were used for the samples with a Ta barrier of 175 Å. The results reported here were all obtained on the LC test structures with a line width of 0.175μm.

The EM testing was conducted at 270°C under 1MA/cm^2. As discussed in the previous chapter, the time at which the first abrupt resistance change occurs was taken to be the EM lifetime.

Typically, the first step toward the critical length determination is to inspect the EM-induced damages for different line lengths within the LC test structures after extended EM stressing.

In our previous studies with Cu/oxide interconnects, inspection on the length-dependent EM-induced damages in a given LC test structure was conducted with an optical microscope. However, with a reduced line width, the damage sites were too small to be detected using an optical microscope; therefore, an FIB-induced contrast (FIBIC) imaging technique was employed [95] for a better resolution in the investigation of the

interconnect lines. The basis for the FIBIC technique is that in Cu/oxide interconnects, voiding at the cathode end of the line typically accompanies extrusion at the corresponding anode end. Therefore, counting the voids at the cathode end is equal to counting the number of extrusions at the anode end. Extrusions are generally found to protrude upwards through the top passivation, and therefore can be identified using FIBIC. This technique first involves using a Gallium ion beam to drill a small and deep hole in the bond pad region through the silicon to the sample holder, so that the bond pad is grounded. When a bias is applied to the LC structure, the interconnect lines, under various potentials, become slightly brighter. As a rule, the extruding regions appear as much brighter spots which can be easily identified (Figure 4.5) [60]. Such a phenomenon makes counting a relatively simple task.

Unfortunately, with dimensional scaling, it is no longer possible to detect EM cathode end voids under the optical microscope, let alone the voids in the embedded M1 structures. Furthermore, in Cu/low k structures, there are only limited lateral extrusions and no top extrusions. As a result, the FIBIC technique cannot be applied either. A different technique, therefore, needs to be considered for our study.

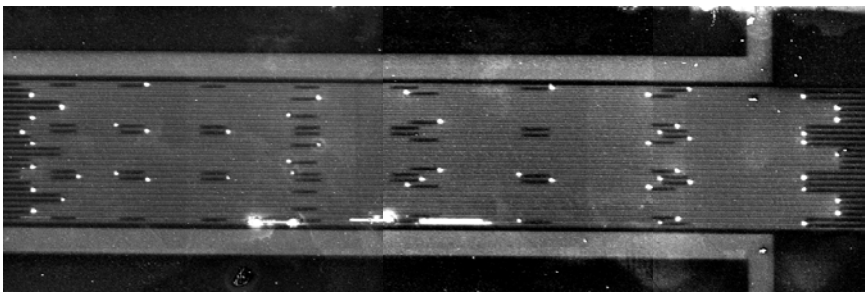


Figure 4.5: An FIBIC image of Cu/oxide structure showing bright spots at the anode end of the interconnect lines, indicating extrusions protruding through the top passivation layer [60].

To solve this problem, both the FIB cutting and the SEM imaging were used to examine EM-induced voids for the individual lines in the LC structure (84 lines in total with various line lengths). A complete experiment involves cutting of each line along the line length by FIB, immediately followed by the SEM imaging of the cross-section and void counting after each cut. Compared with other techniques used in our previous studies as mentioned above, the major tradeoff of this technique is that much more analysis time is needed because of the line-by-line cutting. However, the combination of FIB and SEM allows the counting of very small voids, even when they are deeply hidden in the embedded M1 structures.

As an example, Figure 4.6 illustrates the cathode void formation in the test lines of various lengths for Cu/porous low k samples with a Ta barrier thickness of 175Å. Void formation is observed in all except the 10μm lines, and there is no extrusion observed at the anode end.

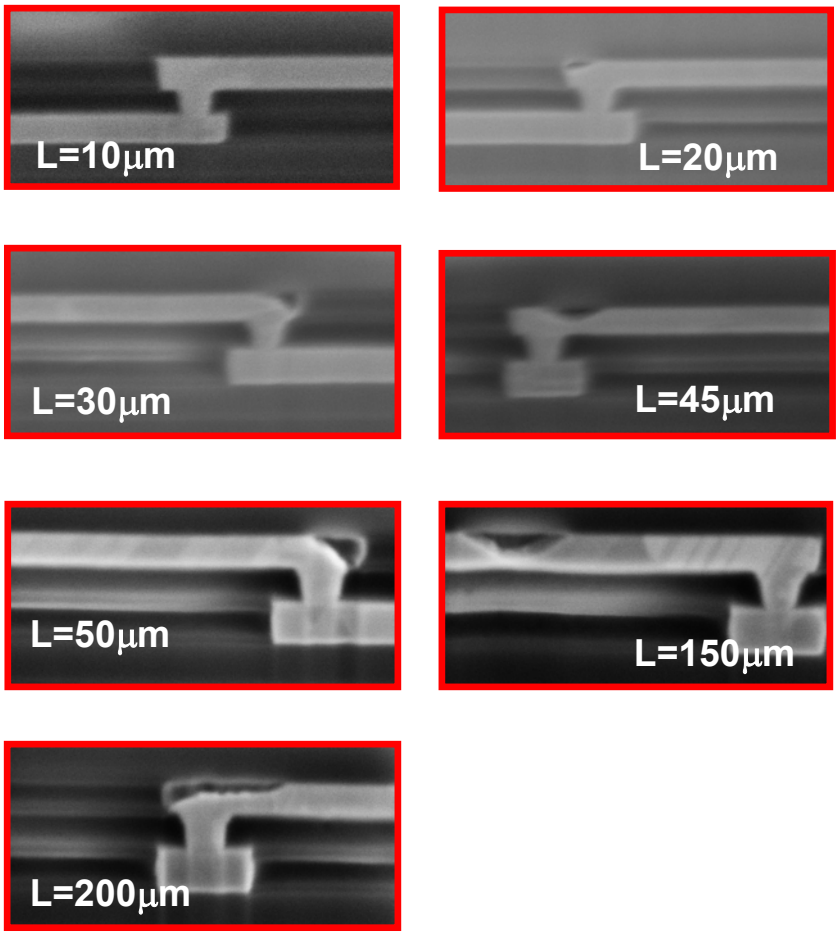


Figure 4.6: Cathode void formation for lines of various lengths in Cu/low k structures. No void is present for lines of 10μm in length; in contrast, void formation is observed in all the other lines.

With the number of voids counted for each test line, the failure statistics as a function of test line length can be determined. The critical length or the critical $(jL)_c$ product can be obtained statistically using the approach mentioned in Chapter 2. Specifically, the normalized failure probability is first plotted versus the line length. Then, the critical length L_c for a given testing current density j can be estimated from the intercept of the regression curve by assuming that the failure probability is proportional to

the net drift velocity and in turn the test line length [29] . The critical length of the case given in Figure 4.6, for instance, was estimated to be 18μm and the $(jL)_c$ to be 1800 A/cm accordingly (Figure 4.7).

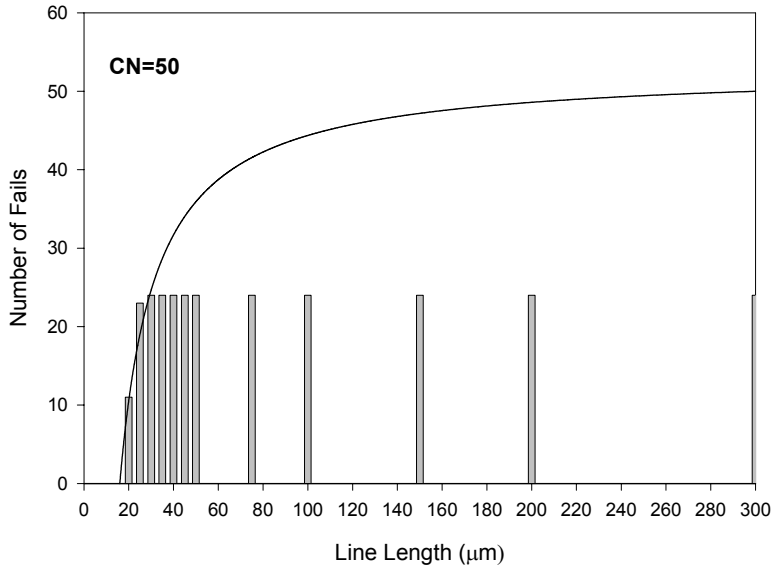


Figure 4.7: Normalized failure probabilities vs. test line length. Testing current density j = 1MA/cm^2. With the regression curve, the critical length L_c is estimated to be 18μm, giving an $(jL)_c$ value of 1800 A/cm .

The results of the $(jL)_c$ product measured for the M2-type LC test structures with different Ta barrier thicknesses are presented in Figure 4.8. The $(jL)_c$ products were found to be 1850, 1750, and 1900 A/cm, respectively, with an error limit of ± 250 A/cm for samples with a Ta barrier thickness of 175Å, 100Å and 75Å, respectively. It appears that the $(jL)_c$ product appeared to be insensitive to the barrier thickness, although a higher $(jL)_c$ value is expected for samples with a thicker Ta barrier due to a stronger confinement effect.

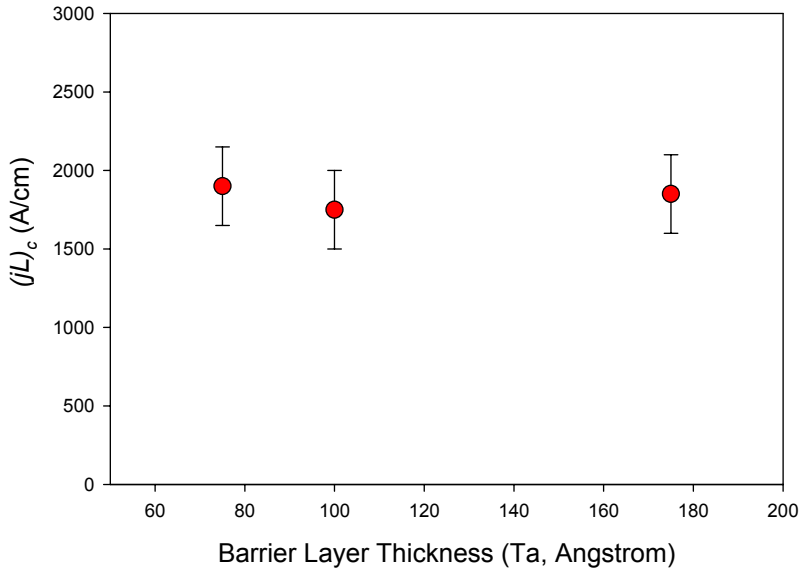


Figure 4.8: Critical $(jL)_c$ product as a function of the Ta barrier layer thickness for the upstream M2 cases. The $(jL)_c$ product seems to be insensitive to changes in the Ta barrier thickness.

The $(jL)_c$ product was also compared between the M1-type structures and the M2-type structures. For the M1 structures, as shown in Figure 4.9, those fabricated with the Ta barrier resputtering process (DEP2) showed a slightly lower $(jL)_c$ value of 1700 A/cm in comparison to that of 1850 A/cm for the M2 structures which were subjected to an identical process. The M1 structures with a more conventional DEP1 process showed a further decreased $(jL)_c$ value of 1350 A/cm.

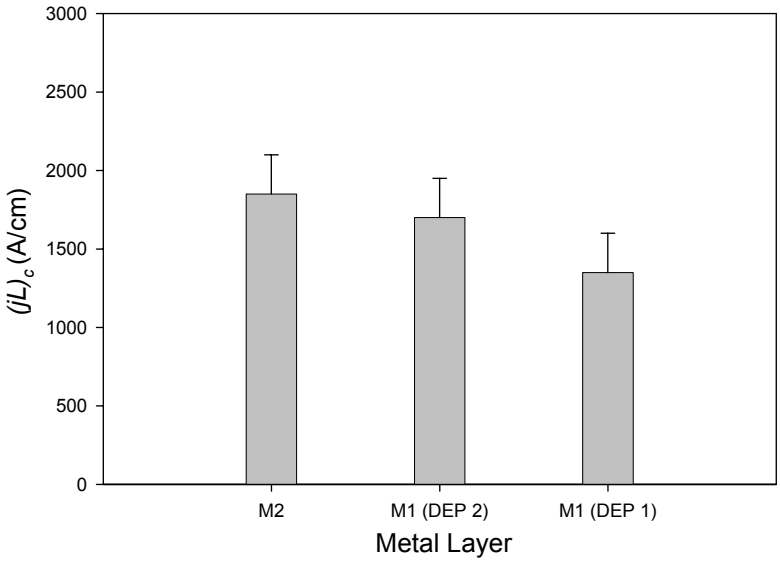


Figure 4.9: Critical $(jL)_c$ product: M1 structures versus M2 structures. DEP1 is a conventional Ta barrier deposition process and DEP 2 is a Ta barrier resputtering process.

4.04 SIMULATION OF EFFECTIVE BULK MODULUS B

To analyze the confinement effect to explain the observed critical $(jL)_c$ results, we evaluated the values of the effective bulk modulus B for different test structures. The effective bulk modulus B is one of the two important parameters in the determination of the critical length (Eq. 4.8).

As mentioned in the previous section, Korhonen et al. [93] formulated an analytical solution to describe the generic behavior of stress buildup in Cu lines under EM. In their solution, the effective bulk modulus B was first proposed to reflect the effects of the mechanical confinement of Cu under the stress generated by the EM mass transport on the EM lifetime and the $(jL)_c$ product. From Eq. 4.2

$$\frac{dC}{C} = \frac{-d\sigma}{B}$$

where dC/C is the volumetric strain induced by EM, and $d\sigma$ is the corresponding amount of hydrostatic stress generated in the interconnect structure. The effective bulk modulus B depends on the elastic properties and the geometry of the metal line and surrounding materials. The larger the B value, the higher the confinement effect from the surrounding materials to allow a larger stress buildup with the same amount of mass transport under EM.

The effective bulk modulus B was evaluated with three-dimensional FEA, which was based on the extension of a two-dimensional model developed by Hau-Riege et al. [96-97]. In our simulation, a real interconnect test structure was considered, consisting of a 0.175μm-wide single-link test line embedded in the dielectric with a 0.85μm-wide adjacent extrusion monitor line. There were also thick SiN and SiO_2 passivation layers on top in the structure. Figure 4.10 represents a cross-sectional overview of this structure, and the extrusion monitor line parallel to the test line can be seen in Figure 4.11.

In this model, X coordinate is parallel to the interconnect line; Y coordinate is perpendicular to the interconnect line; and Z coordinate is perpendicular to the wafer surface. Only half of the interconnect line is modeled due to the structural symmetry along X and Y coordinates. The thickness for both metal 1 and metal 2 was 0.24μm, that of SiCN cap layer was 0.05 μm, and that of the SiN and SiO_2 passivation layers was 0.5μm. The thickness of the thermal oxide was 2μm and that of the silicon substrate was 5μm.

To calculate B, we assumed that there is a set of stress-free homogeneous dilational strains of the interconnect, ε_x^T, ε_y^T, and ε_z^T. The total applied strain Δ can be calculated by

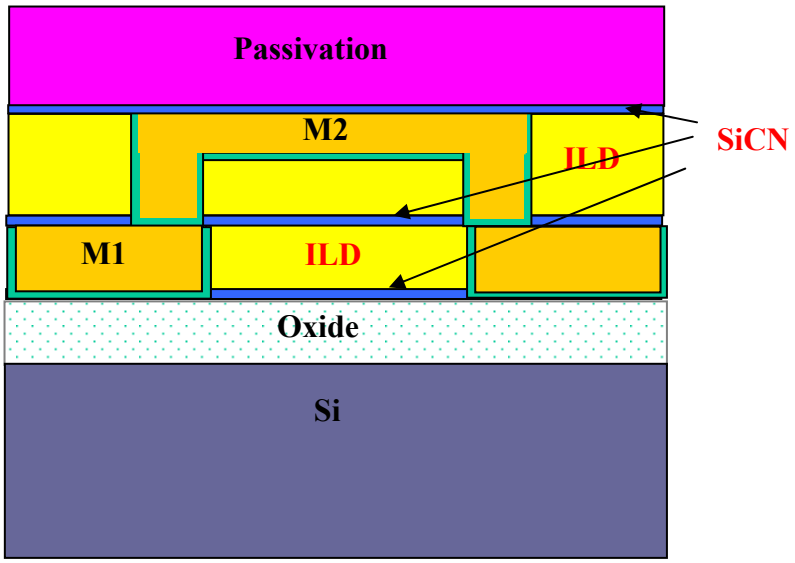
$$\Delta = \varepsilon_x^T + \varepsilon_y^T + \varepsilon_z^T = \frac{dC}{C} \tag{4.7}$$

The corresponding hydrostatic stress can be calculated through FEA next. With the total strain calculated and the hydrostatic stress simulated, the effective bulk modulus B can be calculated accordingly.

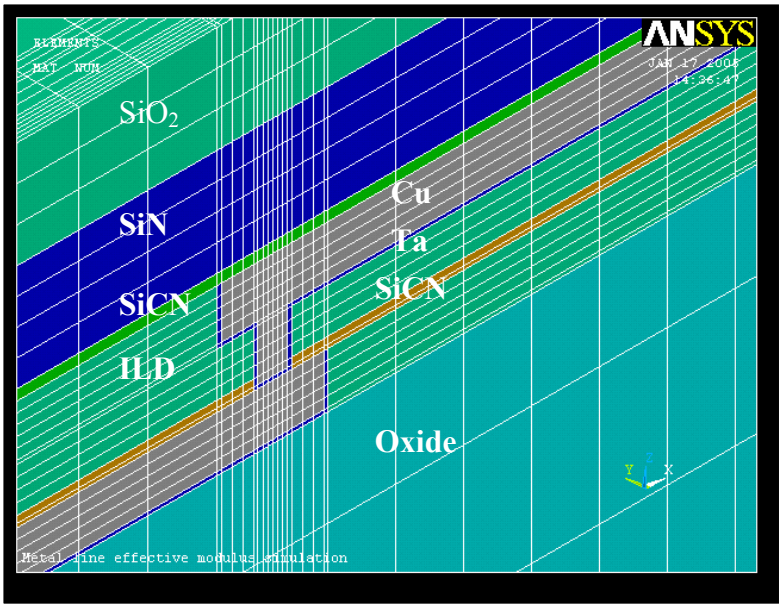
In calculating the total strain, the mass transport mechanism or the primary diffusion pathway under EM needs to be considered. In Al-based interconnects, the grain boundaries serve as the primary diffusion paths; therefore, the mass distribution can be assumed to be isotropic, and $\varepsilon_x^T = \varepsilon_y^T = \varepsilon_z^T$. In contrast, for Cu interconnects, the interfacial diffusion along the Cu/cap layer interface represents the dominant diffusion mechanism. Therefore, the mass distribution can be assumed to be anisotropic, primarily along Z direction, and $\varepsilon_x^T = \varepsilon_y^T = 0$.

In the simulation, the test structures were modeled with three different barrier layer thicknesses, 75Å, 100Å, and 175Å, and with four ILD materials, oxide, dense CVD MSQ, porous MSQ, and organic polymer. Both the upstream M2 and the downstream M1 structures were examined (Figure 4.11).

Some of the material properties used in the simulation are listed in Table 4.1. All the materials were assumed to be isotropic and linear elastic. The adhesion of Cu to the barrier, ILD, and the cap layer was also assumed to be perfect.

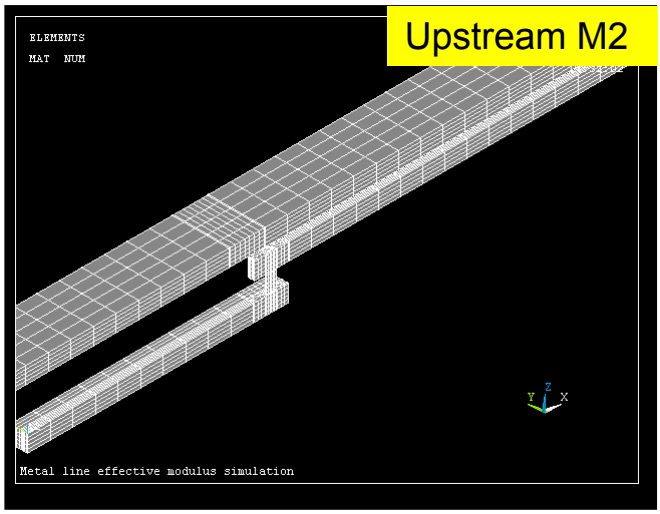


(a)

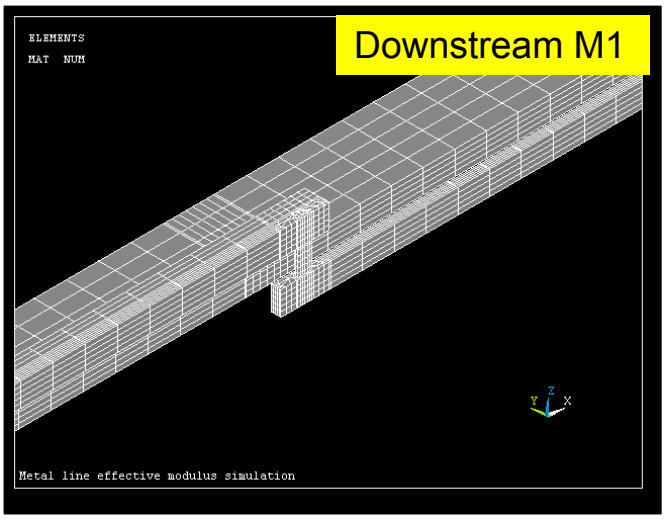


(b)

Figure 4.10: A cross-sectional overview of a two-level Cu dual-damascene interconnect structure: (a) geometry and (b) finite element meshing. The extrusion monitor line parallel to the test line is not visible.



(a)



(b)

Figure 4.11: FEA models: (a) upstream M2, and (b) downstream M1.

Table 4.1: Mechanical properties of the materials used in the FEA simulation.

Material	Young's modulus (GPa)
Cu	122
Ta	185
Silicon	163
SiO_2	66
Dense CVD MSQ	7
Porous MSQ	3.6
Organic polymer	2.5
Hardmask	310

The effective bulk modulus B as a function of the Ta barrier layer thickness is shown in Figure 4.12 for three different ILD materials: oxide, CVD MSQ, and porous MSQ material. For each material, the change of the barrier thickness had only a limited effect on B. In contrast, B had a stronger dependence with the choice of ILD materials. For example, the B values for TEOS were almost twice as large as those for the low k materials under a given barrier thickness, although they are about the same for the three low k materials. Figure 4.13 summarizes the B values for different metallization schemes: M2-type structures vs. M1-type structures. For Cu low k systems, the B values for the M1 structures were only marginally higher than those of the M2 structures. This is possibly due to a slightly stronger substrate confinement in the M1 structures.

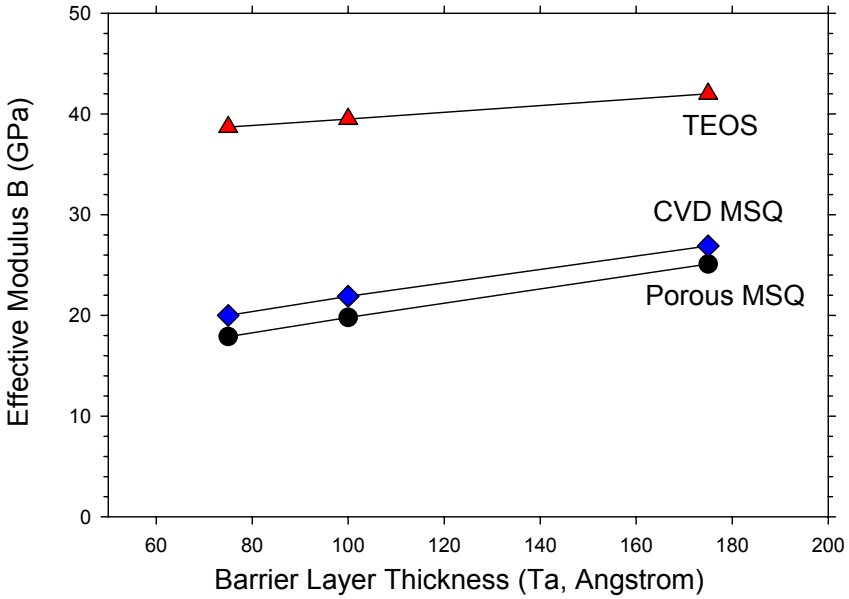


Figure 4.12: The effective bulk modulus B as a function of Ta barrier layer thickness for different ILD materials.

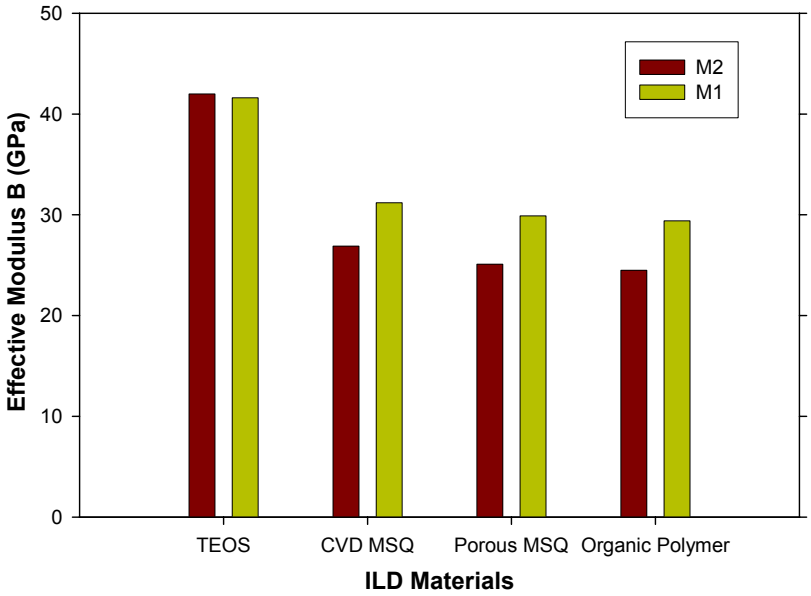


Figure 4.13: The effective bulk modulus B for both M2 and M1 structures with different ILD materials.

4.05 DISCUSSION

In order to examine the EM threshold, below which there are no EM-induced failures, two situations should be considered. Either there is no void nucleation or voids, once nucleated, should be able to reach a point of saturation with no further growth. In reality, with the particularly readily void nucleation at the Cu/cap layer interface in Cu interconnects, the requirements for the latter are less stringent and therefore more practical in IC designs.

In the case where a void will eventually reach a point of saturation, there are two important parameters in determining the critical $(jL)_c$ product: the critical failure void volume $V_{crit,void}$ and the effective bulk modulus B, as mentioned in Section 4.02. Therefore, examining the impact of scaling on the critical length involves studying the impact of scaling on these two controlling parameters.

Scaling by itself is a multi-faceted concept. It comprises dimensional scaling; namely, line width scaling, via size scaling, and barrier thickness scaling, etc. Along with dimensional scaling, there have been many necessary changes in the materials, the structure, and processes; for example, the introduction of Cu dual damascene structures, the implementation of low k materials, and the development of new barrier deposition processes. Therefore, in order to study the impact of the scaling on the critical $(jL)_c$ product, it is essential to examine the impact of the above mentioned factors on the critical failure void volume $V_{crit,void}$ and the effective bulk modulus B.

In our studies of the barrier thickness scaling, with a Ta barrier thickness of 175Å, 100Å, and 75Å, the $(jL)_c$ products were found to be within the range of 1750 and 1900 A/cm. There is no clear trend identified with the barrier thickness scaling.

The critical failure void volume, defined as the void volume at the first appreciable resistance surge, is closely related to a critical depletion length above the Cu

damascene via as well as the line height, and is almost independent of the barrier thickness. Therefore, this parameter remains almost the same, independent of the barrier thickness. On the other hand, according to the simulation results, the effective modulus B decreased by about 25% as the barrier thickness reduced from 175Å to 75Å for the samples with a porous low k ILD (Figure 4.12). However, such difference in the B values from the confinement effect due to different barrier thicknesses was not reflected in the $(jL)_c$ products obtained in our experiments. This can be attributed to two factors. First, the experimental error limits are about ±2.5μm for the critical L_c, which translates into ±250 A/cm (about 10-15% inaccuracy) for the critical $(jL)_c$ determination. Second, the nominal barrier thicknesses were provided for the B simulation, which are the barrier thicknesses measured from the field. However, from a real PVD barrier deposition profile, the thicknesses of the trench bottom and the sidewalls are different to a certain extent. Moreover, the thickness on the sidewalls is not uniform either. Consequently, the actual barrier thickness differences among the different structures might be less than the nominal differences. Therefore, the differences in the actual confinement are smaller. Overall, due to the non-uniformity of the deposited barrier profile, it is very difficult to correct for such differences in the simulation (Figure 4.14).

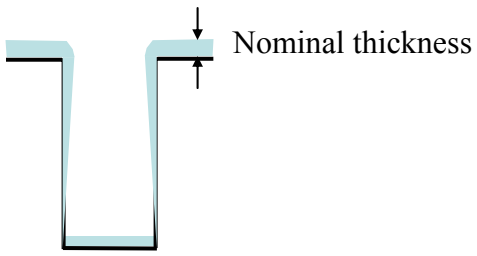


Figure 4.14: Schematic of a deposited barrier profile. The nominal thickness refers to the barrier deposited in the field.

It is noteworthy, however, that although no obvious trend was found in this study for the $(jL)_c$ product in relation to the barrier thickness scaling, there was some major difference in the $(jL)_c$ values when the ILD materials changed from oxide to low k materials. For comparison, we also plotted the results of the $(jL)_c$ product in the M2-type Cu interconnects obtained from several different studies in recent years (Figure 4.15). Over all, the $(jL)_c$ values of low k materials are considerably lower than those of the oxide materials. The lower $(jL)_c$ values for Cu/low structures can be largely attributed to the weaker confinement of the low k materials and in turn the much reduced effective bulk modulus B values (Figure 4.12).

The $(jL)_c$ differences between the M1-type and the M2-type structures also need to be reviewed. If the voiding processes in M1 and M2 are the same, then the critical failure volumes should be fairly similar. As for the influence of the effective bulk modulus B, it only made a minor difference between the M1 and the M2 structures for Cu low k systems. Consequently, we can expect very similar $(jL)_c$ values for both electron flow directions. This conclusion can be drawn from Figure 4.16 for the M2 structures and one type of M1 structures with the DEP2 process, where also presented are the FIB images from these two structures showing similar void formation mechanisms.

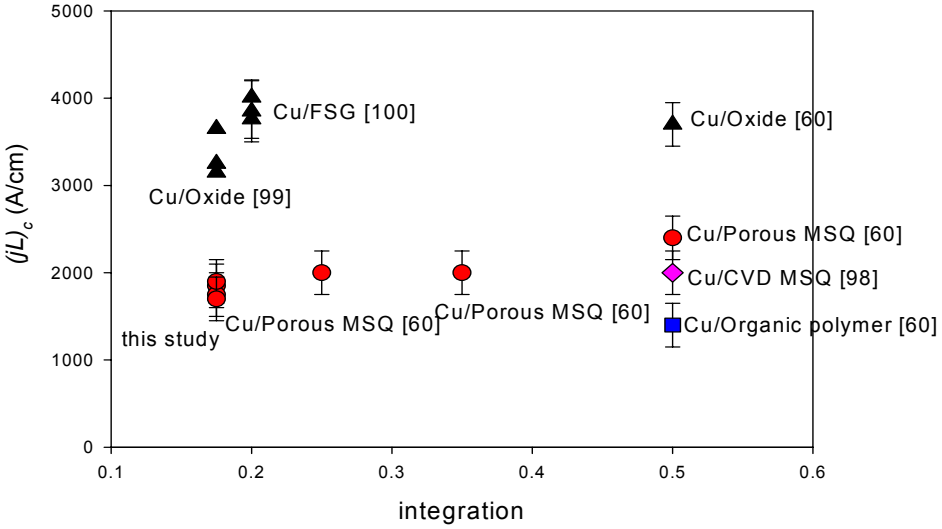


Figure 4.15: Summary of the critical $(jL)_c$ product for various Cu integrations.

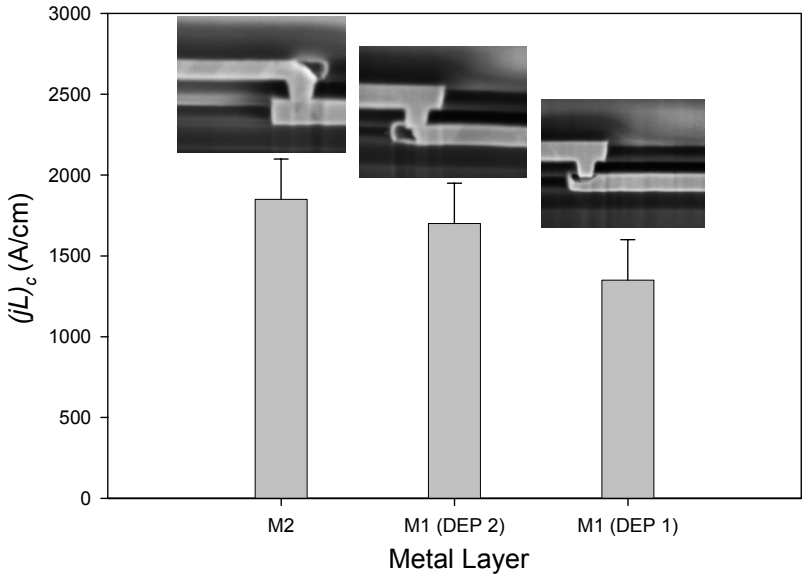


Figure 4.16: The critical $(jL)_c$ product for M1 versus M2 structures, with the void formation mechanisms included.

For the same structures, different processes may result in different $(jL)_c$ values. For example, when compared with the M1 structures processed with DEP2 where there is a barrier resputtering step, those processed with the conventional DEP1 had an appreciably smaller $(jL)_c$ value. This is because different processes can give rise to significantly different critical failure void volumes. In case of a process-induced void formation at an unfavorable location, e.g., if it is directly under the via, then the critical failure volume and the $(jL)_c$ value will be greatly reduced. As can be seen from Figure 4.16, a substantially smaller critical failure void volume and $(jL)_c$ value are identified for the M1 structures with the DEP 1 process.

As discussed above, the EM threshold depends primarily on two parameters. One is the effective bulk modulus B, which is used to measure the mechanical confinement by the surroundings materials (e.g. rigid oxide vs. compliant low k materials or different barrier layers, etc.). As we have consistently seen a lower $(jL)_c$ value for downstream M1 than upstream M2, we've demonstrated that this confinement effect is only one of the intrinsic factors that determines the $(jL)_c$ value. The other parameter is the critical failure void volume, which not only is sensitive to the selected failure criterion (e.g. first appreciable resistance increase or the maximum acceptable resistance increase level ΔR_{crit}^{max}), but also can be largely influenced by extrinsic process related issues. Since the critical volume in downstream EM can be easily affected by process-induced defects, care much be taken in determining the EM threshold for a certain interconnect system. A more detailed and complete study is still needed in the future.

Last but not least, the statistical LC structures used in the study allow not only the simultaneous testing of various line lengths but also direct observation of the critical line length. They can be effectively employed to differentiate the Cu/oxide and Cu/low k materials in terms of the $(jL)_c$ product. Nonetheless, they may not be adequate when the

differences in the $(jL)_c$ product are fairly small. So some improvement is needed in the future test structure design. For example, the longest lines in the current structures, e.g., 300 and 200μm, can be eliminated so that the testing time may be extended. Longer testing times will allow a larger void size in the shorter lines for easier inspection. Additionally, the current design is characterized by an interval of 5μm between 5 and 50μm in line length, with an error limit of ±2.5μm. Such an error limit can be effectively reduced through the introduction of smaller intervals.

4.06 SUMMARY

In this chapter, we have examined the impact of scaling on the critical length and the critical $(jL)_c$ product. There are several different aspects to scaling. It not only includes dimensional scaling, but also involves the changes in processes and structures and the introduction of new materials. There are two controlling parameters for the critical $(jL)_c$ product: the critical failure void volume $V_{crit,void}$ and the effective bulk modulus B. Any effect is actually mediated through these two parameters. Therefore, to study the impact of scaling on the critical $(jL)_c$ product is essentially to examine the effect of various aspects of the scaling on these two parameters.

Our experiments and modeling showed that, unlike the effective modulus B which scaled with the barrier thickness, the $(jL)_c$ product did not demonstrate a clear trend. This can be attributed to the decreasing experimental accuracy with a much reduced $(jL)_c$ value, the barrier thickness variation and the degree of thickness control and calibration. However, we also found that as the ILD material changed from oxide to low k dielectrics, a significant decrease was observed in both the effective bulk modulus B and the $(jL)_c$ value.

Provided that the void formation processes are sufficiently similar, the distinctions in the directions of the electron flows (either the M1 or the M2 structures) were observed to have little influence on the critical $(jL)_c$ product. But since M1 structures tend to be more sensitive to changes in process, process-induced void formation at an unfavorable location can significantly reduce their $(jL)_c$ values by dramatically reducing their critical failure volume.

Chapter 5: Impact of Electroplating Chemistries and Metal Layer Thicknesses on Stress Migration

5.01 OVERVIEW

Stress migration has been a serious reliability challenge for Cu metallization in that it can lead to an unacceptably high resistance or an open circuit. It is typically associated with void nucleation and growth, and is mainly driven by the stress gradient in the interconnects.

In contrast to EM, there is much left to be investigated for stress migration despite numerous research efforts in the past two decades. This is partly because stress migration is highly sensitive to both structure and process. A mature and comprehensive failure model has yet to emerge. The most widely accepted model so far is the vacancy condensation model proposed by Ogawa et al. [10]. According to their study, a large number of vacancies result from the grain growth when Cu is not fully annealed before it is constrained in the dielectric. Such vacancies may lead to void formation as they diffuse through Cu grain boundaries and/or Cu/SiN interface towards the region of the lowest stress, such as the via bottoms, and then accumulate to release the stress gradient.

There are two controlling factors in the study of stress migration: the level of vacancy density and the magnitude of the stress gradient. This chapter addresses how the structural scaling and the modifications of the material properties associated with new processes affect these two factors and in turn the stress migration behavior. Specifically, the implications of different Cu electroplating chemistries and metal layer thickness scaling on the stress migration reliability were examined. The SM experiments were conducted on single vias that were connected to a large Cu pad above and below (M1-via-M2). Microstructural characterization, thermal stress measurement, and 3-D FEA

modeling were performed to interpret the observed SM results, and a possible SM mechanism was proposed accordingly.

5.02 EXPERIMENTAL DETAILS

Both patterned and blanket wafers were used in the study, with SiO_2 as the ILD material.

On the patterned wafers, test structures were fabricated with a standard via-first Cu dual damascene process. Two groups of samples were prepared (Table 5.1). One group was processed with three different chemistries for Cu electroplating, where the impurity concentration level varied from low, medium, to high. The other group was characterized by four different M1 metal layer thicknesses: 90, 150, 250, and 500 nm. All samples had gone through a post-plating anneal of 150°C for one hour to stabilize the Cu microstructure.

Table 5.1: Electroplating chemistries and the M1 metal layer thickness range for stress migration study.

Sample Group A	**Cu impurity concentration**
A-1	low
A-2	medium
A-3	high
Sample Group B	**M1 Cu pad thickness (nm)**
B-1	90
B-2	150
B-3	250
B-4	500

In Chapter 3, we discussed two barrier deposition processes. In the conventional preclean-first process, there is an aggressive Ar sputter preclean step, which can sputter Cu from the via bottom onto the sidewalls, thereby degrading both barrier/Cu and barrier/dielectric interfaces. In contrast, in the novel barrier-first process, which deposits the TaN barrier first and then performs the sputter cleaning, the possibility of resputtering Cu onto the sidewall is successfully eliminated. And it has been reported that the stress migration performance is considerably improved with the adoption of this barrier-first process [49].

In this study, we chose to use the conventional Ar preclean barrier process instead of the improved barrier first process. Such a choice is justified since in the conventional process, the effects of the chemistries for Cu electroplating and the changes of the M1 metal layer thicknesses on stress migration are more magnified, and therefore easier to observe.

Figure 5.1 provides a schematic overview of the Kelvin via test structures used in the stress migration experiments. The Cu contact pads above and below the Kelvin via were 12μm wide. As mentioned earlier, this type of test structure is known to be very sensitive to stress migration due to its large metal reservoir and high stress gradient in the via region. Via stress migration behavior was monitored on the wafer level by measuring the resistance of 120 isolated Kelvin vias with a diameter of 0.25μm across the wafer before and after a thermal treatment. A Keithley Instruments S600 series parametric tester and a fully automatic prober were used for the resistance measurement.

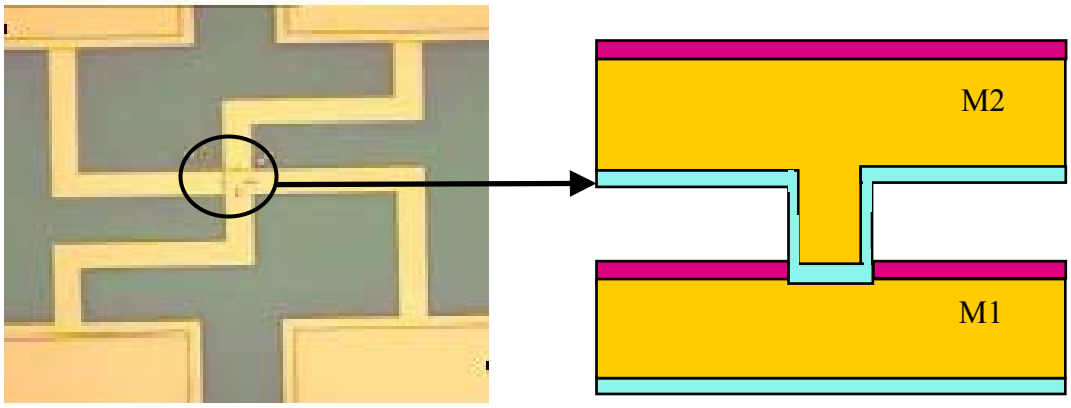


Figure 5.1: (a) Optical micrograph and (b) schematic cross-section of a Kelvin via test structure for via stress migration study.

The conventional stress migration test with a single testing temperature tends to be rather time-consuming, usually varying from 168 to 500 hrs at a fixed temperature between 150°C and 300°C. In contrast, a new stress migration testing approach was employed to induce resistance shifts in Kelvin via structures. It involves continuous thermal cycling within the critical stress migration temperature range of 150°C to 250°C over a period of 12 hours (Figure 5.2) [101]. This cyclic anneal technique considerably shortens the testing time. Besides, it is also independent of the thermal history of the Cu, due to its full coverage of the temperature range for the high voiding rate. The procedure can be used to screen a number of different processes within a relatively short period of time. However, as a result of the varying testing temperatures, lifetime extrapolation to a normal operation condition is not possible.

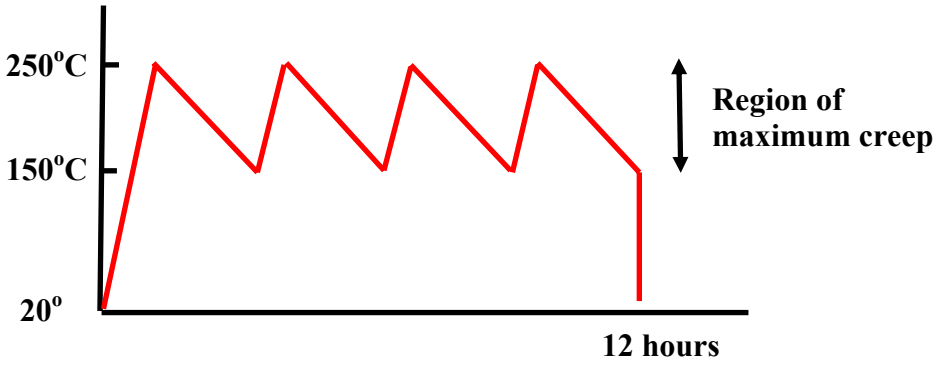


Figure 5.2: A continuous thermal cycling in the critical stress migration temperature range of 150°C to 250°C over a 12-hour period.

To simplify the study of the thermomechanical properties of the large Cu pad in the Kelvin structures, a series of blanket Cu film samples were employed, as they were assumed to be fairly similar to each other in such properties. The blanket Cu film samples were prepared with an identical electroplating chemistry as the patterned wafers. They were 0.8μm thick as deposited, with a 250Å Ta(N) barrier and a 1000Å Cu seed layer film. Next they were annealed at 150°C for one hour for grain growth, and then subjected to CMP. The blanket wafers, now with 0.7μm thick Cu, were subsequently passivated at 400°C with a 700Å SiN, followed by a 1.0μm TEOS.

The thermomechanical behavior of each film is characterized using a bending beam technique [102]. Specifically, samples were subjected to thermal cycling between room temperature and 430°C at a heating and cooling rate of 4°C/min. The stresses in the Cu films were directly calculated from the changes in the sample curvature. Since the microstructure was not adequately stabilized in the first cycle, only the stress-temperature curve in the second cycle was analyzed.

5.03 EXPERIMENTAL RESULTS FOR STRESS MIGRATION

In order to improve the gap fill capability, different additives are usually introduced in the electroplating chemistries [103]. However, this causes the impurity level to increase in the bulk Cu. In this study, the stress migration performances of three chemistries with different impurity levels were examined, and different resistance shifts were observed (Figure 5.3). In our experiment, a decreasing impurity level was associated with an increasing resistance shift, indicating degradation in the via stress migration performance.

The stress migration performance of samples with different M1 Cu thicknesses was also evaluated. The results showed that as the thickness continually dropped from 0.5 to 0.09μm, a significant shift in the via resistance was clearly identified (Figure 5.4). Therefore, the scaling of the thickness of M1 Cu pads degraded the stress migration performance.

FIB failure analyses revealed that all the voids appeared to have initiated at the bottom corners of the via, independent of both the impurity level of the Cu and the M1 metal layer thickness. For illustration, an FIB image of a Kelvin structure with an M1 metal layer of 0.25μm thick is presented in Figure 5.5, which revealed that voids initiated at the via bottom corner and then propagated to the vicinity underneath the via. This phenomenon suggests that the aggressive Ar sputter preclean process introduces a weak spot for possible void formation because it degrades the adhesion between the barrier and the ILD at the lower corner of the via. Although these structures shared a similar void nucleation site, the subsequent void growth and the resultant resistance shift were formed to vary dramatically, depending on the electroplating chemistries for electroplating as well as the M1 metal layer thicknesses (Figures 5.3 and 5.4).

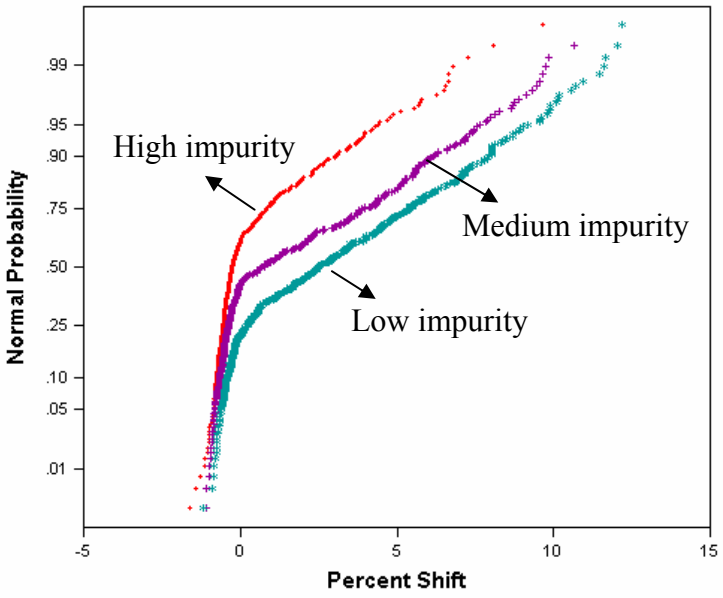


Figure 5.3: Resistance shift of Kelvin via test structures with three different chemistries for Cu electroplating. Via stress migration performance degraded with decreasing impurity level.

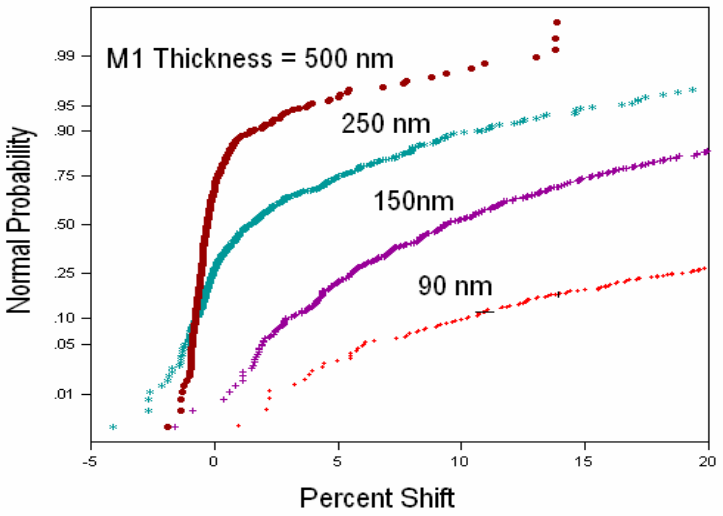


Figure 5.4: Resistance shift of Kelvin via test structures with four different M1 metal layer thicknesses. Via stress migration performance degraded with decreasing M1 metal layer thickness.

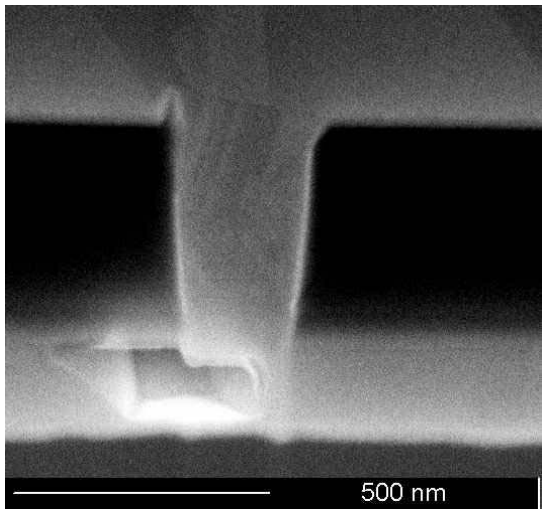


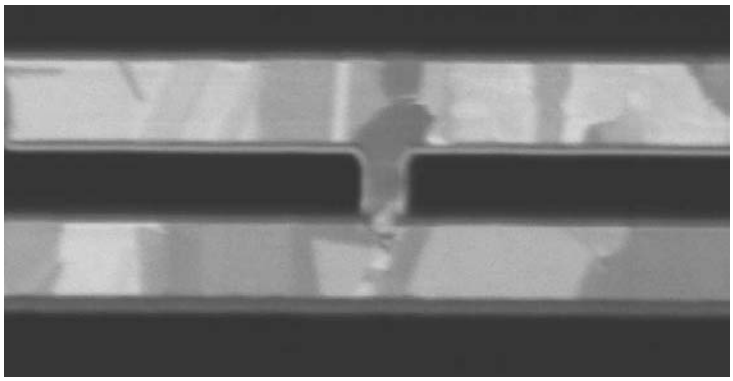
Figure 5.5: FIB image of a Kelvin test structure with an M1 metal layer of 0.25 μm thick revealed that voids initiated at the via bottom corner and propagated to the vicinity region underneath the via.

5.04 DISCUSSION

According to the vacancy condensation mechanism for stress migration proposed by Ogawa et al. [10], the stress migration failure rate depends on the active diffusion volume, within which vacancies are gathered together to form voids. This mechanism also suggests that under a similar stress gradient, a greater number of available vacancies typically lead to larger via stress migration resistance shifts, thereby compromising stress migration performance.

In our previous work [105], the effects of the impurity concentrations in the bulk Cu on the microstructure were examined with FIB/SEM analyses. It was found that in both the blanket film samples and the Kelvin via structures, those with a high impurity level tended to have a smaller grain size than those with a low impurity level (Figures 5.6 and 5.7). And the grain size was similar for samples with a low and with a medium

impurity level. The implication of a smaller grain size was that there would be more grain boundaries, which would give rise to a higher vacancy density. Therefore, a higher impurity level is essentially associated with a higher vacancy density and in turn degraded stress migration performance.



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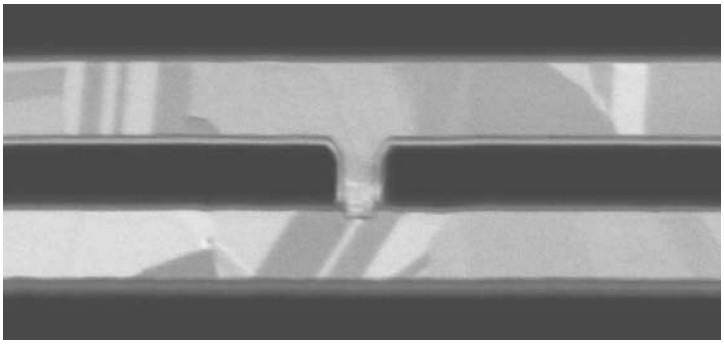
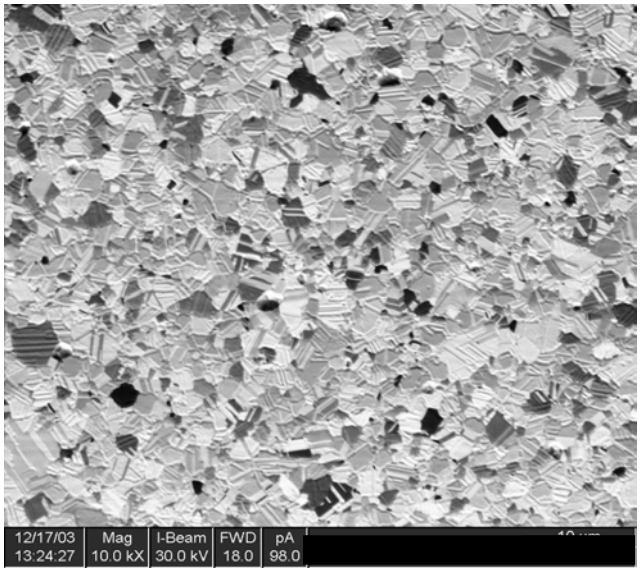


(b)

Figure 5.6: Grain microstructure for Kelvin via test structures with (a) a high impurity level, and (b) a low impurity level.



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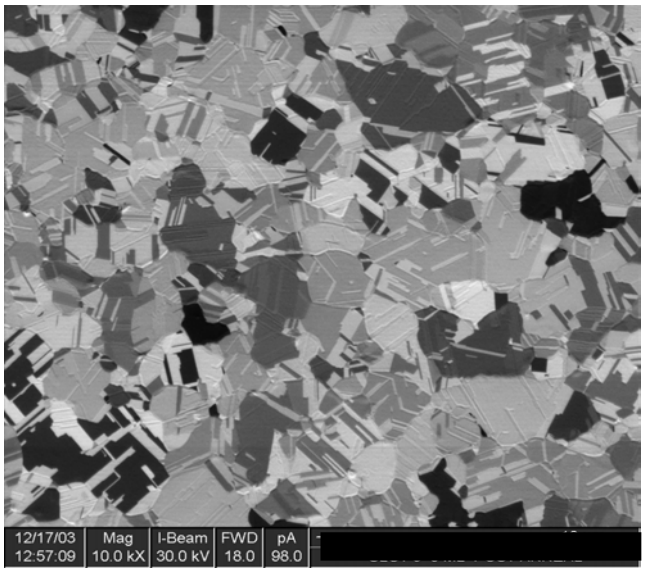


(b)

Figure 5.7: Grain microstructure for blanket Cu films with (a) a high impurity level and (b) a low impurity level, under the same magnification.

On the other hand, compared with a thin Cu pad, a thick pad has a larger volume and thus tends to have a larger total supply of vacancies for voiding for the same bake period. Consequently, thicker M1 Cu pads are expected to demonstrate worse via stress migration performance.

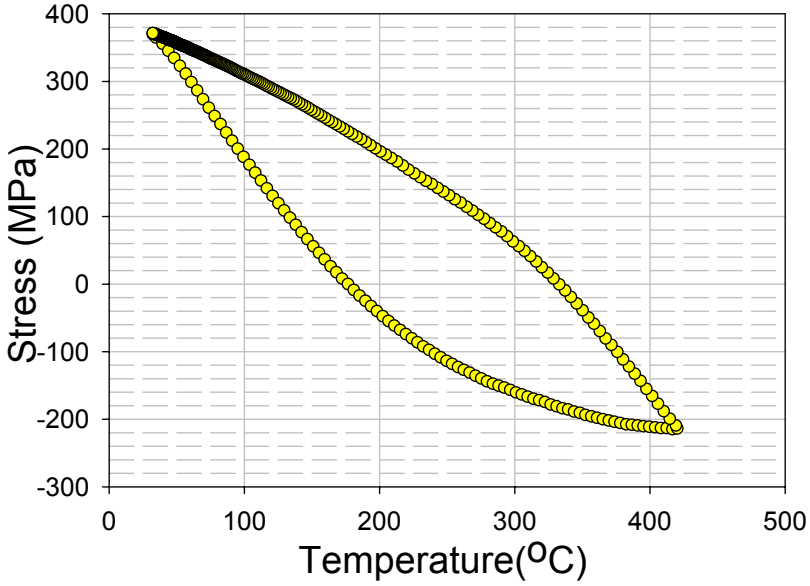
However, this prediction is contrary to our observations that samples with a lower impurity level or with a thick Cu pad in effect had a better via stress migration resistance. The explanation for such a contradiction may be related to the stress gradients in the Cu. That is, the stress gradients are influenced by the change of the chemistry for Cu electroplating and the M1 metal layer thickness. Rather than the absolute number of vacancies, it is probably the stress gradients that dominate the stress migration performance in this study.

In order to explore the differences in the stress gradients, we first examined the thermomechanical stress behaviors in the blanket film samples with different electrofill chemistries. The thermal stress behaviors of the blanket Cu films during thermal cycling are presented in Figure 5.8 for three different impurity levels: low, medium, and high. Samples with a low impurity level exhibited the typical stress behavior for the passivated Cu film as a function of the temperature (Figure 5.8 (a)). At room temperatures, the Cu film is under a tensile stress. Upon heating, the tensile stress starts to be relieved due to a larger thermal expansion coefficient of Cu than that of Si. The tensile stress tapers off to zero at about 175°C, and the compressive stress starts to develop as the temperature continues to rise. At high temperatures, plastic deformation, instead of elastic deformation, becomes dominant and the stress does not build up as fast. Upon cooling down from a high temperature, the stress becomes increasingly tensile. After the stress exceeds the yield point, plastic deformation starts to manifest itself and the stress change rate drops. With an increasing impurity level, as shown in Figure 5.8 (b) and (c), the

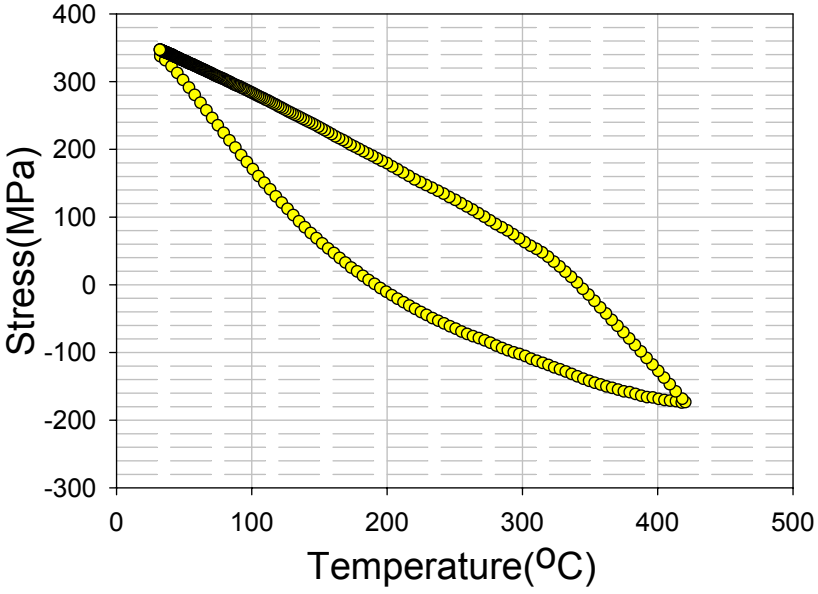
thermal stress behavior deviates gradually and exhibits a lower yield stress, as indicated by a smaller hysteresis loop and a faster plastic flow.

For thin Cu films, we found that they had a higher post-anneal stress. As shown in Figure 5.9, the measured stress in a Cu film after a 350°C anneal increased quickly as the film thickness decreased from 1.7 to 0.3μm. Notably, several researchers reported that for thin Cu films, the measured yield stress appeared to be linearly related to the inverse of the Cu film thickness [106-107]. Therefore, the observed increase of the post-anneal stress with a decreasing film thickness can be attributed to the increasing yield strength.

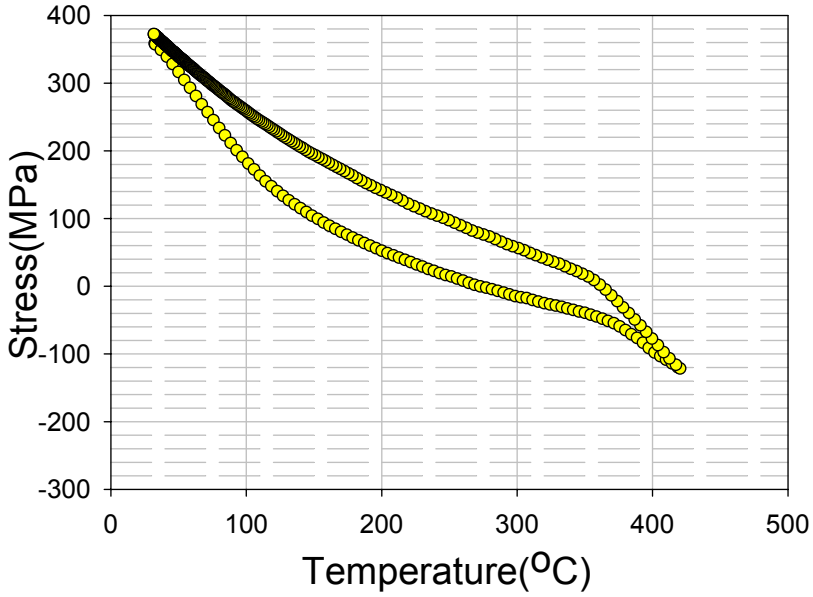
The above observations of the stress migration performance as well as the mechanical properties for samples with different Cu electroplating chemistries and underlying M1 metal layer thicknesses suggest the existence of a correlation between the Cu yield properties and the stress migration. Cu with a lower yield stress tends to have a better stress migration performance, and an increase in the yield stress typically results in degraded stress migration performance.



(a) Low impurity



(b) Medium impurity



(c) High impurity

Figure 5.8: Stress-temperature curves for three different electroplating chemistries with (a) a high impurity level, (b) a medium impurity level, and (c) a low impurity level.

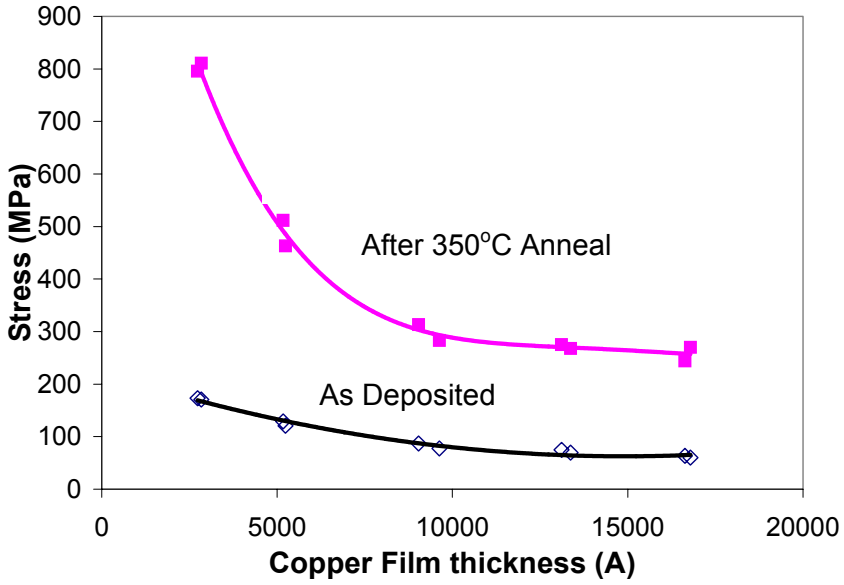


Figure 5.9: Cu stress as a function of blanket film thickness.

To better understand how yield stress affects via stress migration, a 3-D process-oriented thermal stress modeling was performed to simulate the stress distribution in the Kelvin via structures after different wafer processing steps and/or further thermal loading, such as temperature cycling for stress migration measurement.

Two examples were considered in the simulation: a structure with an M1 metal layer thickness of 0.5μm and a yield stress of 383 MPa, and a structure with an M1 metal layer thickness of 0.1μm and a yield stress of 916 MPa. For both cases, the M2 metal layer thickness was 0.5μm, the via diameter was 0.25μm, and the via height was 0.5μm. The geometrical FEA model and the detailed boundary conditions are presented in Figure 5.10. More details about the Kelvin test structure are provided in Figure 5.11. In order to save the computational time, only one quarter of the test structure was modeled, with symmetric boundary conditions at X = 0 and Y = 0 surfaces. The displacement of the XMAX and YMAX surfaces were set to be that of the silicon substrate because of its strong confinement. The Z-displacement at the bottom of the silicon substrate (Z = 0) was set to be zero. For simplicity, Cu was treated as an elastic-plastic material, and its young modulus and yield stress were parameterized for several different temperatures. Other materials were treated as elastic. Some of the materials properties are listed in Table 5.2.

Table 5.2: Some of the materials properties used in the simulation.

Materials	Si	Cu	Ta	TEOS	Hardmask
Young's Modulus (GPa)	162.7	-	185	66	309
Possion ratio υ	0.28	-	0.34	0.18	0.27
CTE ($\times 10^{-6}$)	2.6	17.0	6.5	0.57	2.9

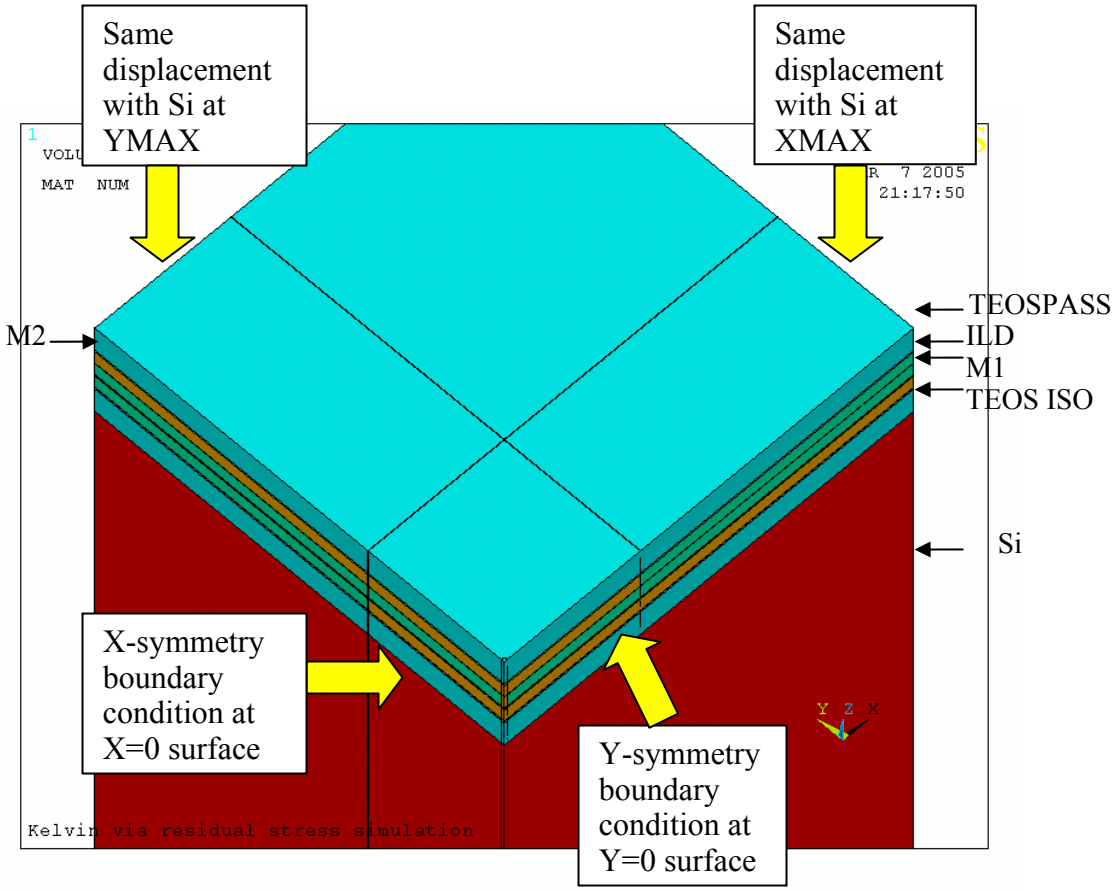


Figure 5.10: Kelvin via structure FEA model.

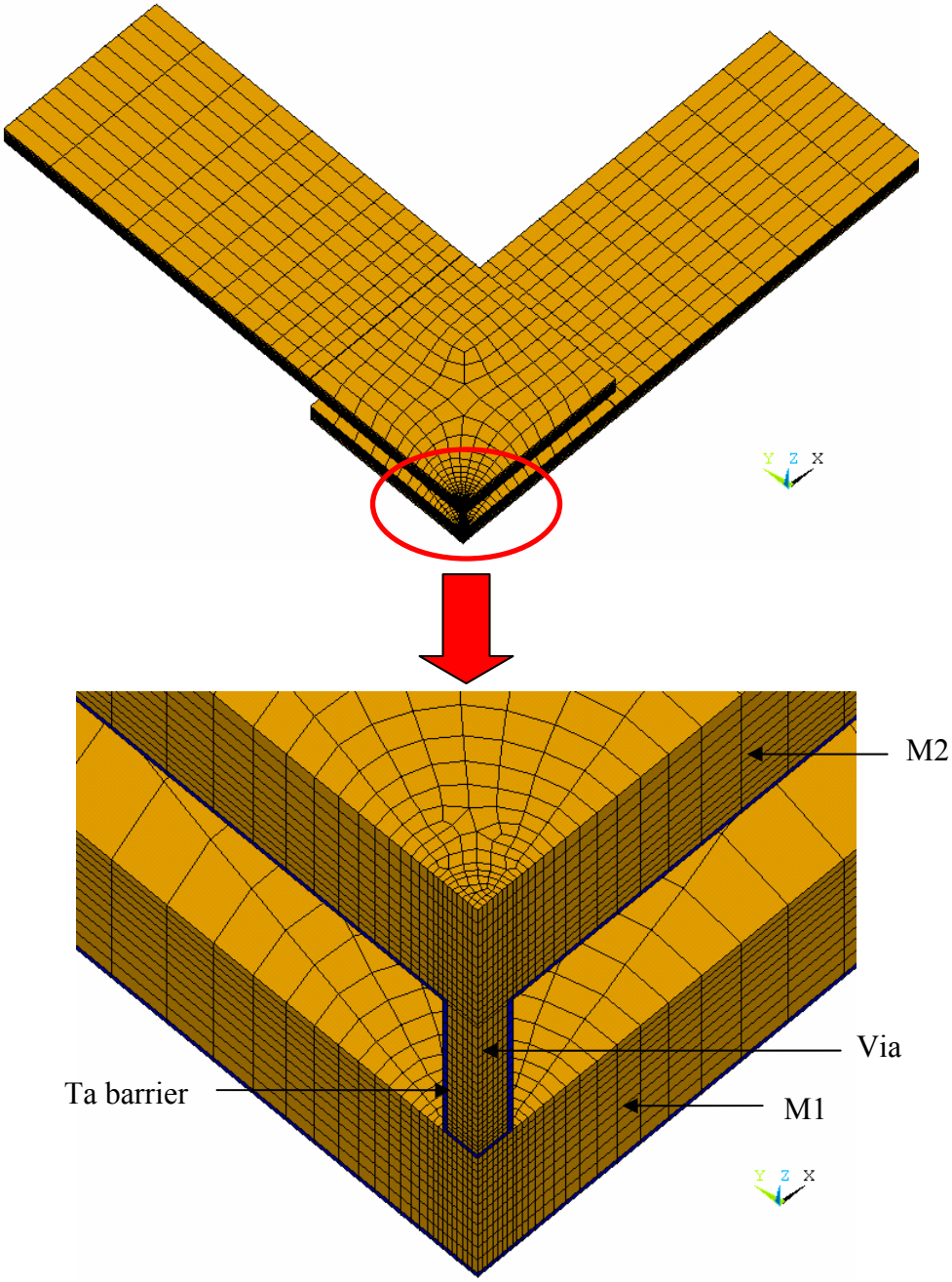


Figure 5.11: Details of the Kelvin via structures (FEA).

Although the wafer processing procedure used in the simulation (Figure 5.12) was a simplified version of the actual procedure, it already offered sufficient sophistication. As provided in [108] with more details, this procedure includes the major processing steps as well as the temperature profile during each processing step. The element birth and death feature was used in the simulation to replicate the material deposition and removal in the actual process. During each of the post-plating annealing processing step, the thermal stress in Cu was assumed to be completely released after a 150 ^{o}C anneal for one hour.

Figure 5.13 shows the contour plots of the hydrostatic stress distribution at 200°C cooling from 400°C after wafer processing for Kelvin structures with an M1 metal layer thickness of 0.5μm and 0.1μm, respectively. It was observed that the structure with an M1 thickness of 0.5μm had a lower global hydrostatic stress in the M1 Cu pad than the structure with an M1 thickness of 0.1μm (~36% lower). This result indicated that a lower yield stress was typically associated with a lower global hydrostatic stress level in the M1 metal layer after the wafer processing. In addition, for both structures the maximum tensile stress occurred at the via bottom corner and along the via/Cu pad interface. Based on such observation, we may propose a possible stress migration mechanism.

Generally, void nucleation is expected when the tensile stress exceeds a threshold stress. The threshold, unfortunately, is easily lowered by some process-induced via defects, for example, a poor diffusion barrier layer coverage at the via bottom sidewall. A weak spot for voiding is therefore introduced accordingly. At the same time, a large tensile stress is developed during the wafer processing at the very location, which further facilitates void nucleation.

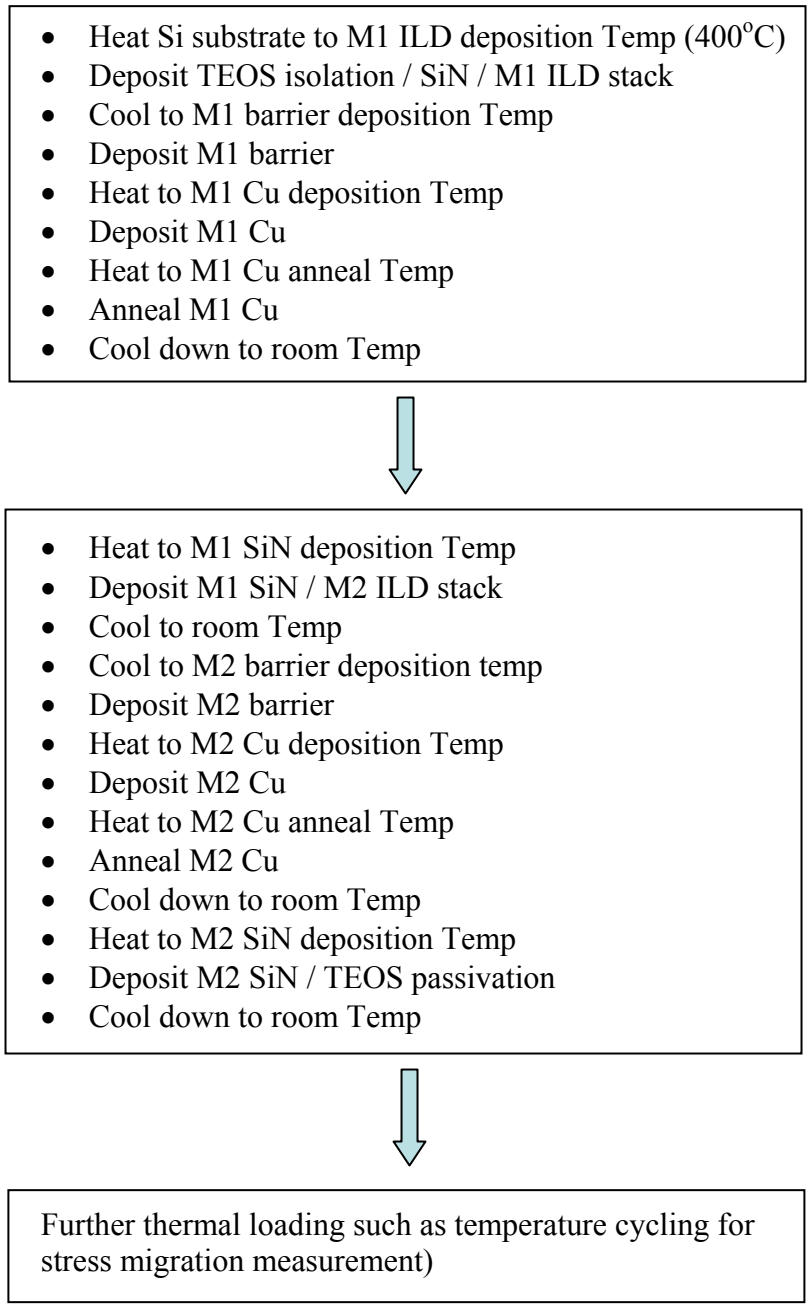
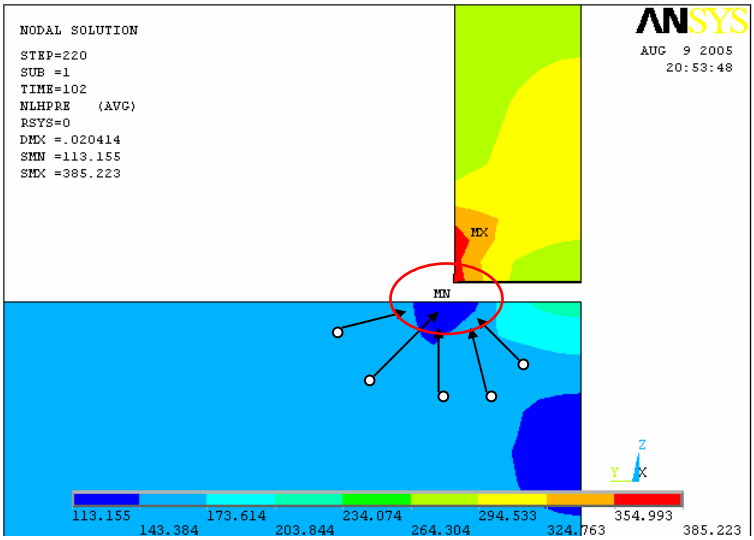
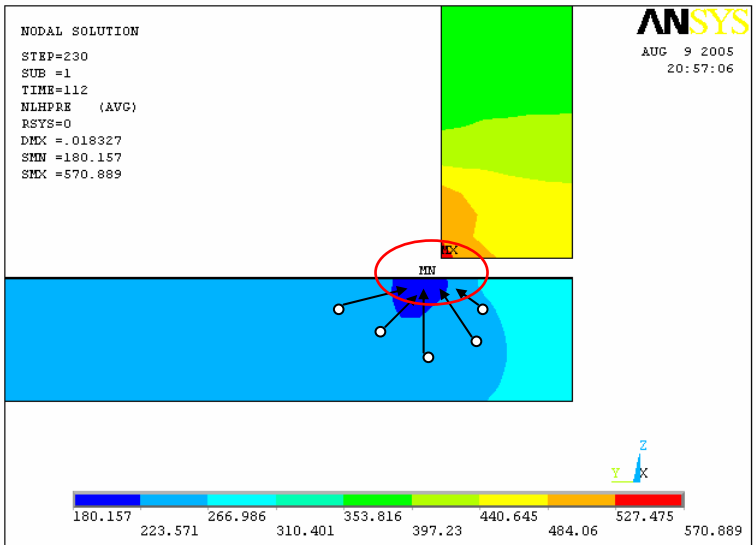


Figure 5.12: Detailed simulation steps for process-oriented thermal stress FEA modeling.



(a)



(b)

Figure 5.13: Hydrostatic stress distribution at 200°C for Kelvin structures with an M1 metal layer thickness of (a) 0.5µm, and (b) 0.1µm.

Once a void is initiated, the large tensile stress is immediately released, and a local minimum hydrostatic stress region will form near the void, resulting in a large stress gradient. This stress gradient will serve as the dominant driving force for vacancy accumulation. The void growth and the final void formed can be thought of as resulting from the vacancies in the M1 metal layer diffusing to the via bottom corner under such stress gradient. At high stressing temperatures, void growth over time will lead to a large resistance shift and eventually an open circuit.

Samples with a thin Cu pad or a low impurity level have a high yield stress and a correspondingly high residual hydrostatic stress level. Therefore, they tend to have a high stress gradient between the void nucleation site and its surrounding areas upon void nucleation. Consequently, a larger final void size can be expected under a large stress gradient for vacancy accumulation, resulting in a large resistance shift and a poor stress migration performance.

As we can see, the stress migration phenomenon is associated with the processing issues as well as the mechanical properties of Cu. In order to improve the stress migration performance, a number of strategies may be adopted. A low threshold for void nucleation represents a major threat in terms of stress migration; so the improvement of the barrier deposition process will be an effective approach to enhancing stress migration performance through the elimination of potential weak spots at the via bottom corner for voiding. Another possible strategy is to avoid single vias touching large metal reservoirs and to deploy multiple vias that are connected to a large Cu pad. Under such a circumstance, the stress migration failure rate may be significantly reduced.

5.05 SUMMARY

Stress migration describes the void formation due to the vacancies driven to accumulate at a low hydrostatic stress region under the stress gradient. There are two determining factors: the vacancy density and the stress gradient. Any process variation and geometric design that may have an impact on either factor will influence the stress migration performance of an interconnect structure.

In this chapter, we have investigated the impact of the chemistries for Cu electroplating and the scaling of the M1 metal layer thicknesses on the via stress migration. Those samples with a lower impurity level or a thinner M1 metal layer thickness were found to have degraded stress migration performance. Such an observation was explained by main driving force due to the stress gradient instead of the vacancy concentration.

Moreover, the stress measurement and 3-D FEA modeling suggested that a low impurity level or a thin Cu pad was linked to a high yield stress, which is in turn related to a high residual hydrostatic stress level.

Based on the experimental data and the simulation results, a stress migration mechanism is proposed accordingly. Void nucleation occurs when threshold stress for void nucleation becomes reduced due to the presence of process-induced via defects and the high tensile stress concentration generated at the via bottom corner during wafer processing. Once a void is nucleated, vacancy diffusion under sufficient stress gradient will cause the void to grow. With sufficient vacancy sources, void growth and the final void size are determined by the magnitude of the stress gradient driving force. Samples with a low impurity level or a thin M1 metal layer thickness tend to have a high residual hydrostatic stress level/high yield stress, which may lead to a high stress gradient, thereby

providing a great driving force, a large resistance shift, and a degraded stress migration performance.

Chapter 6: Summary and Future Work

6.01 SUMMARY

Aggressive scaling, motivated by the need for a higher packing density and better chip performance, has been an essential part of the interconnect technology development in recent years. As a multi-faceted concept, it not only comprises dimensional scaling, but also involves the implementation of new materials and new processes. Nevertheless, scaling has given rise to many technical challenges and in turn some serious reliability concerns.

This dissertation primarily deals with some aspects of the scaling effect on electromigration reliability. Specifically, the impact of interconnect scaling on electromigration lifetime characteristics and the critical current density length product $(jL)_c$ have been examined, and a number of important scaling parameters have been identified. Besides, some effects of different processes as well as geometry designs on stress migration reliability have also been investigated.

In terms of the electromigration lifetime characteristics, both the impact of metal line width scaling (0.5, 0.25, and 0.175μm), via size scaling (0.5, 0.25, and 0.175μm), and barrier thickness scaling (175Å, 100Å, and 75Å), and the implications of the introduction of low k materials and new processes have been explored. The upstream M2 cases indicated that EM lifetime scales down linearly with line width for the intrinsic strong mode failures, and that the weak mode failures, which are typically related to the process, are independent of the line width. The downstream M1 cases suggested a weak lifetime dependence on line width due to mixed void locations. It was concluded that line width scaling itself is not directly associated with the decrease of EM intrinsic lifetime; rather, it induced certain changes on some parameters that have a direct effect on the EM

lifetime, for example, the critical depletion length ΔL_{cr} and the metal line thickness h. Also, the intrinsic electromigration failure characteristics (t_{50} and Q) are almost independent of barrier thickness scaling per se. With the introduction of porous low k materials on thin barriers, it is becoming increasingly difficult to ensure the barrier integrity. The fact that early failures shift toward shorter lifetimes for samples with thinner barriers suggests that there is an increase in defect-induced early failures in such samples. FIB and TEM analyses have revealed that defect-induced Cu out-diffusion leads to lifetime degradation and line shorting. The optimization of the process is always of vital importance in scaling. Our studies have also found that different via-related processes have a significant impact on both the upstream M2 and the downstream M1 electromigration reliability.

The impact of scaling on the $(jL)_c$ product for electromigration was also studied. The critical failure void volume $V_{crit,void}$ and the effective bulk modulus B have been identified as the two controlling parameters. Experimental data and subsequent FEA modeling have showed that, unlike the effective modulus B which scaled with the barrier thickness, the $(jL)_c$ product did not demonstrate a clear trend. This can be attributed to the decreasing experimental accuracy with a much reduced $(jL)_c$ value, the barrier thickness variation and the degree of thickness control and calibration. However, we also found that as the ILD material changed from oxide to low k dielectrics, a significant decrease was observed in both the effective bulk modulus B and the $(jL)_c$ value. With a similar void formation mechanism, the difference in the direction of the electron flows (either M1 or M2 structures) may have minimal impact on the critical $(jL)_c$ product. Nonetheless, with M1 structures being more sensitive to changes in the process, any process-related void formation at an unfavorable location can significantly reduce the critical failure volume and in turn the $(jL)_c$ values.

As far as stress migration is concerned, there are two important factors: the vacancy density and the stress gradient. Process variations and geometric designs may change the stress migration performance by influencing either or both of the two factors. In this study, the impact of both the different chemistries for Cu electroplating and the scaling of the M1 metal layer thickness was investigated. It was found that a lower impurity level or a smaller metal layer thickness was associated with a worse stress migration performance. The stress measurement indicated that a low impurity level and a thin Cu pad are linked to a high yield stress, and the FEA modeling suggested that a high yield stress is related to a high residual hydrostatic stress level after wafer processing. Once a void initiates at the via bottom corner, samples with a low impurity level or a thin M1 metal layer thickness tend to have a high residual hydrostatic stress because of their high yield stress and in turn a high stress gradient for void growth. Consequently, these samples were observed to have a larger resistance shift and worse stress migration performance.

6.02 FUTURE WORK

Interconnect scaling has been a major development trend within the semiconductor industry and its impact on the electromigration lifetime merits continuous research. In our studies, the smallest line width and via size examined are 0.175μm, and the smallest barrier thickness examined is 75Å. Further scaling is bound to introduce more reliability problems. In terms of the scaling effects on intrinsic properties, we need to find out if such effects can be extended to even smaller dimensions. In terms of the scaling effects on extrinsic properties, the nature of the early failures needs to be constantly examined and the impact of the process on early failures should be studied.

For example, the deposition of a further scaled down barrier layer more porous materials may with a lower k give rise to some early failures of quite a different nature.

Also, a more comprehensive study is needed for the critical $(jL)_c$ product. Two controlling parameters have been identified in this study, but our examination only represents a simplification of the real situations, where there are other factors that should be taken into consideration. Since voids nucleate readily in the Cu interconnects, a void growth saturation model was employed in this study. It would be very interesting to consider a good quality cap layer, e.g., CoWP coating, which will increase the void nucleation threshold, and to examine to what extent it will impact the critical $(jL)_c$ product.

As we know, the phenomenon of the stress migration is both highly structure- and process-dependent. In order to get a whole picture of the stress migration mechanism, it is necessary to evaluate a variety of processes and different structural layouts. Also, more efficient modeling and simulation of the stress distribution should be employed in future research.

References

1. M. T. Bohr, IEEE IEDM Technical Digest, 10.1.1 (1995).
2. International technology roadmap for semiconductors, 2004 update.
3. B. Li, T. D. Sullivan, T. C. Lee and D. Badami, Microelectronics reliability, 44 (2004) 365-380.
4. C. Bruynseraede, Zs. Tokei, F. Lacopi, G. P. Beyer, J. Michelon, and K. Maex, IEEE 43rd Annual International Reliability Physics Symposium Proceedings (2005).
5. D. Cheryl, E. T. Ogawa, Y. -J. Park, and T. -C. Chiu, IEEE Trans. On Device and Materials Reliability, vol. 4, pp129-141 (2004).
6. P. S. Ho, K. -D. Lee, S. Yoon, X. Lu, and E. T. Ogawa, Materials Science in Semiconductor Processing 7 (2004) 157-163.
7. R. Rosenberg, D. C. Edelstein, C.-K. Hu, and K. P. Rodbell, Annu. Review Mater. Sci., vol. 30, pp.229-262, 2000
8. P. S. Ho and T. Kwok, Rep. Prog. Phys. 52, 301 (1989).
9. J. R. Lloyd, J. Phys. D: Appl. Phys. 32 (1999) R 109-R118.
10. E. T. Ogawa, J. W. McPherson, J. A. Rosal, K. J. Dickerson, T. -C. Chiu, L. Y. Tsung, M. K. Jain, T. D. Bonifield, J. C. Ondrusek, and W. R. McKee, IEEE International Reliability Physics Symposium 40th Annual, 2002, pp. 312-321.
11. J. W. McPherson and C. F. Dunn, J. Vac. Sci. & Tech, B5(5), 1987, pp. 1321-1325.
12. H. B. Huntington and A. R. Grone, J. Phys. Chem. Solids 23, 123 (1962).
13. I. A. Blech, and C. Herring, Appl. Phys. Lett. 29, 131 (1976).
14. C. -K. Hu, K. P. Rodbell, T. D. Sullivan, K. Y. Lee, and D. P. Bouldin, IBM Journal of Research and Development 39, 465 (1995)
15. I. A. Blech, J. Appl. Phys. 47, 1203 (1976).
16. Ames, F. M. d'Heurle, and R. Horstman, IBM J. Res. Dev. 4, 461 (1970).
17. C. -K. Hu, and J. M. E. Harper, Materials Chemistry and Physics 52 (1998) 5-16.

18. S. Vaidya and A. K. Sinka, Thin Solid Films 75, 253 (1981).

19. J. R. Lloyd, J. Clemens, and R. Snede, Microelectronics Reliability 39 (1999) 1595-1602.

20. K. N Tu, J. Appl. Phys. 94, 5451 (2003).

21. S. P. Murarka and S. W. Hymes, Critical Reviews in Solid State and Materials Science, 20(2):87-124 (1995).

22. Stanley Wolf, Silicon Processing for the VLSI era: Vol. 4-deep submicron process technology, pp 640.

23. R. H. Havemann and J. A. Hutchby, proceedings of the IEEE, Vol. 89, No. 5, May 2001, pp 586-601.

24. D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevittt, W. Motsifft, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz , L. Su, S. Lucet, and J. Slattery, IEDM 31.3.1 (1997)

25. C. -K. Hu, R. Rosenberg, K. Y. Lee, Appl. Phys. Lett. 74, 2945 (1999).

26. C. -K. Hu, K. Y. Lee, L. Giganc, and R. Carruthers, Thin Solid Films 1997; 443: 308-309.

27. L. Arnaud, G. Tartavel, T. Berger, D. Mariolle, Y. Gobil, I. Touet, IEEE 39th Annual Int'l Reliability Phys Symp, 1999. p. 263.

28. C. Ryu, K. -W. Kwon, ALS Loke, H. Lee, T. Nogami, V. M. Dubin, et al. IEEE T-ED 1999; 46:1113

29. C. -K Hu, L. Gignac, R. Rosenberg, J. Rubino, C. Sambucetti, A. K. Stamper, US Patent No. 6, 342, 722, 2002

30. H. Kondo, Y. Nakao, T. Suzuki, H. Sakai, and M. Shimizu, Proceeding of the IITC Conference (IEEE, Piscataway, NJ, 2002), p. 292.

31. M. A. Meyer, M. Grafe, H. J. Engelmanan and E. Zschech, Materials for Advanced Metallization Conf., Brussels, 2004.

32. C. -K. Hu, L. Gignac, E. Liniger, B. Herbst, D. L. Rath, S. T. Chen, S. Kaldor, A. Simon, and W. -T. Tseng, Appl. Phys. Lett. 83, 869 (2003).

33. C. -K. Hu, L. Gignac, R. Rosenberg, E. Liniger, J. Rubino, C. Sambucetti, A. Domenicucci, X. Chen, and A. K. Stamper, Appl. Phys. Lett. 81, 1782 (2002).

34. C. -K. Hu, L. Gignac, R. Rosenberg, E. Liniger, J. Rubino, C. Sambucetti, A. K. Stamper, A. Domenicucci, and X. Chen, Microelectron. Eng. 70, 406 (2003).

35. G. B. Alers, IEEE 41th Annual Int'l Reliability Phys Symp Tutorial Notes, 2003. p. 231.

36. J. Gill, T. Sullivan, S. Yankee, H. Barth, and A. von Glasow, IEEE 40th Annual Int'l Reliability Phys Symp, 2002. p. 298.

37. E. T. Ogawa, K. -D. Lee, V. A. Blaschke and P. S. Ho, IEEE transactions on Reliability, 51, 403 (2002).

38. K.-D. Lee, and P. S. Ho, IEEE Transactions on Device and Materials Reliability, 4, 237 (2004).

39. K. -D. Lee, X. Lu, E. T. Ogawa, H. Matsuhashi, V. A. Blaschke, R. Augur, and P. S. Ho, IEEE 40th Annual Int'l Reliability Phys Symp, 2002. pp. 322-326.

40. S. P. Hau-Riege, J. Appl. Phys. 91, 2014 (2002).

41. K.-D. Lee, E. T. Ogawa, S. Yoon, X. Lu and P. S. Ho, IEEE IITC (2003).

42. C. S. Hau-Riege, A. P. Marathe, V. Pham, 2003 IEEE International Reliability Physics Symposium Proceedings.

43. C. S. Hau-Riege, S. P. Hau-Riege, and A. P. Marathe, J. Appl. Phys. 96, 5792 (2004).

44. J. W. Pyun, X. Lu, J. Chung, S. Yoon, P. S. Ho, N. Henis, K. Neuman, L.Smith, and K. Pfeifer, Appl. Phys. Lett. **87**, 061907 (2005)

45. X. Lu, J. W. Pyun, B. Li, N. Henis, K. Neuman, K. Pfeifer, and P. S. Ho, IEEE IITC (2005).pp 33-35.

46. A. von Glasow, A. H. Fisher, M. Hierlemann, S. Penka, and F. Ungar. Advanced Metallization conference (AMC), October 2002, San Diego, CA.

47. K. Y. Y. Doong, R. C. J. Wang. S. C. Lin, L. J. Hung, S. Y. Lee, C. C. Chiu, D. Su, K. Wu, K. L. Young, and Y. K. Peng. Annual IEEE Internl. Relia. Phys. Symp. (IRPS) Proc., 2003. p. 156-60.

48. T. Oshima, K. Hinode, H. Yamaguchi, H. Aoki, K. Torii, T. Saito, K. Ishikawa, J. Noguchi, M. Fukui, T. Nakamura, S. Uno, K. Tsugane, J. Murata, K. Kikushima, H. Sekisaka, E. Murakami, K. Okuyama, T. Iwasaki, IEEE IEDM Technical Digest, pp.757-760 (2002).

49. G. B. Alers, R. T. Rozbicki, G. J. Harm, S. K. Kailasam, G. W. Ray, M. Danek, International Interconnect Technology Conference, (2003).

50. A. von Glasow, A. H. Fischer, D. Bunel, G. Friese, A. Hausmann, O. Heitzsch, M. Hommel, J. Kriz, S. Penka, P. Raffin, C. Robin, H. -P. Sperlich, F. Ungar, A. E. Zitzelsberger, IEEE International Reliability Physics Symposium 41st Annual, 2003, pp. 146-150.

51. P. Bai, C. Auth, S. Balakrishnan, M. Bost, R. Brain, V. Chikarmane, R. Heussner, M. Hussein, J. Hwang, D. Ingerly, R. James, J. Jeong, C. Kenyon, E. Lee, S-H. Lee, M. Liu, Z. Ma, T. Marieb, A. Murthy, R. Nagisetty, S. Natarajan, J. Neirynck, A. Ott, C. Parker, J. Sebastian, R. Shaheed, S. Sivakumar, J. Steigerwald, S. Tyagi, P.-H. Wang, C. Weber, B. Woolery, A., Yeoh, K. Zhang and M. Bohr, 28.2, IEDM (2004).

52. K. Maex, M. R. Baklanov, D. Shamiryan, F. Lacopi, S. H. Brongersma and Z. S. Yanovitskaya, J. Appl. Phys. 93 (11), 2003, pp. 8793-8841

53. M. Morgen, E. T. Ryan, J. -H. Zhao, C. Hu, T Cho and P S. Ho, Annual Review of Materials Science, Vol. 30, 2000, pp. 645.

54. E. T. Ogawa, J. Kim, G. S. Hasse, H. C. Mogul, and J. W. McPherson, IEEE International Reliability Physics Symposium 41st Annual (2003).

55. C. S. Hau-Riege, Microelectronic Reliability 44 (2004) 195-205.

56. K. -D. Lee, E. T. Ogawa, S. Yoon, X. Lu, and P. S. Ho, Appl. Phys. Lett. **82**, 2032 (2003).

57. J. R. Lloyd, M. R. Lane, X. -H. Liu, E. Liniger, T. M. Shaw, C. -K. Hu, and R. Rosenberg, Microelectronics Reliability 44 (2004) 1835-1841.

58. J. R. Black, Proc. IEEE 6th. Ann. Int. Reliability Phys. Symp. 1967, p148.

59. D. P. Seraphim, R. C. Lasky, and Che-Yu Li, *Principles of Electronic Packaging*, pp.296 (1989)

60. Ki-don Lee, Ph. D Dissertation, University of Texas at Austin, (2003).

61. E. T. Ogawa, A. J. Bierwag, K.-D. Lee, H. Matsuhashi, P. R. Justison, A. N. Ramamurthi, and P. S. Ho, Appl. Phys. Lett. 78, 2652 (2001).

62. K.-D. Lee, E. T. Ogawa, H. Matsuhashi, P. R. Justison, K.-Soo Ko, and P. S. Ho Appl. Phys. Lett. 79, 3236 (2001).

63. M. Gall, Ph. D dissertation, University of Texas at Austin, (1999)

64. M. Gall, C. Capasso, D. Jawarani, R. Hernandez, H. Kawasaki and P. S. Ho, Appl. Phys. Lett. 76, 843 (2000).

65. M. Gall, C. Capasso, D. Jawarani, R. Hernandez, H. Kawasaki and P. S. Ho, J. Appl. Phys. 90, 732 (2001).

66. L. P. Murray, L. C. Rathbun, and E. D. Wolf, Appl. Phys. Lett. 53, 1414 (1988).

67. J. R. Lloyd, and J. Kitchin, J. Appl. Phys. 69, 2117 (1991).

68. W. Nelson, Accelerated Testing: Statistical Models, Test plans, and Data Analyses: John Wiley and Sons, 1990, ch.7, pp. 377-387

69. A. H. Fischer, A. von Glasow, S. Penka and F. Ungar, Proceedings of the IEEE 2003 International Interconnect Technology Conference, 2003. pp. 253-255.

70. J. He and Z. Suo, 7th international workshop on stress-induced phenomena in metallization (2004) 15-26.

71. J. He, Z. Suo, T. N. Marieb, and J. A. Maiz, Appl. Phys. Lett. 85, 4639 (2004).

72. H. Kawasaki ADMET (2002).

73. R. F. Liu, C. -K. Hu, L. Ginac, J. M. E. Harper, J. Lioyd, and X. -H. Liu, J. Appl. Phys. 95, 3737 (2004).

74. M. Hauschildt, M. Gall, S. Thrasher, P. Justison, L. Michaelson, R. Hernandez, H. Kawasaki, and P. S. Ho, 7th international workshop on stress-induced phenomena in metallization (2004) 112-123.

75. C. -K. Hu et al. IEEE International Reliability Physics Symposium 42th Annual. (2004).

76. D. -Y. Kim, and S. S. Wong, Proceedings of the IEEE 2003 International Interconnect Technology Conference. Piscataway, NJ, USA: p. 265-7.

77. J. R. Lloyd, M. W. Lane, E. G. Liniger, C. -K. Hu, T. M. Show, and R. Rosenberg, IEEE Transactions on Device and Materials Reliability, 5, 113 (2005).

78. E. G. Liniger, L. Gignac, C. -K. Hu, and S. Kaldor, J. Appl. Phys. 92, 1803 (2002).

79. C. -K. Hu, L. M. Gignac, R. Rosenberg, B. Herbst, S. Smith, J. Rubino, D. Canaperi, S. T. Chen, S. C. Seo, and D. Restaino, Appl. Phys. Lett. 84, 4986 (2004).

80. C-K. Hu, L. Gignac, S. G. Malhotra, and R. Rosenberg, Appl. Phys. Lett. 78, 904 (2001).

81. C-K. Hu, L. Gignac, E. Liniger, and R. Rosenberg, Journal of the electrochemical Society, 149 (7) G408-G415 (2002).

82. E. G. Liniger, C-K. Hu, L. M. Gignac, J. Appl. Phys. 93, 9576 (2003).

83. M. W. Lane, E. G. Liniger, and J. R. Lloyd, J. Appl. Phys. 93, 1417 (2003).

84. J. -N. Sun, D. W. Gidley, T. L. Dull, W. E. Frieze, A. F. Yee, E. Todd Ryan, S. Lin, and J. Wetzel, J. Appl. Phys. 89, 5138 (2001).

85. R. Caluwaerts et al. Proc. IITC 2003 pp. 242-244.

86. Zs. Tőkei, F. Iacopi, O. Richard, J. Waeterloos, S. Rozeveld, E. Beach, B. Mebarki, T. Mandrekar, S. Guggilla and K. Maex , Microelectronic Engineering, 70, 352 (2003).

87. J. W. Pyun, X. Lu, S. Yoon, N. Henis, K. Neuman, K. Pfeifer, and P. S. Ho, 2005 IEEE International Reliability Physics Symposium. Proceedings 43rd p. 191-4.

88. M. L. Michael, C.-U. Kim, P. Gillespie and R. Augur, Appl. Phys. Lett. 83, 1959, (2003).

89. R. G. Filippi, P. -C. Wang, R. A. Wachnik, D. Chidambarrao, M. A. Korhonen, T. M. Show, R. Rosenberg, and T. D. Sullivan, 6th international workshop on stress-induced phenomena in metallization (2002) 33-48.

90. R. G. Filippi, R. A. Wachnik, H. Aochi, J. R. Lloyd and M. A. Korhonen, Appl. Phys. Lett. 69, 2350 (1996).

91. R. G. Filippi, R. A. Wachnik, C. -P. Eng, D. Chidambarrao, P. -C. Wang, J. F. White, M. A. Korhonen, T. M. Show, R. Rosenberg and T. D. Sullivan, J. Appl. Phys. 47, 5787 (2002).

92. P. S. Ho, IEEE Int Reliability Phys. Symp tutorial (2005).

93. M. A. Korhonen, P. Borgesen, K. N. Tu and C. –Y. Li, J. Appl. Phys. 73, 3790 (1993).

94. C. S. Hau-Riege, and C. V. Thompson, J. Appl. Phys. 87, 8467 (2000).

95. A. J. Bierwag, Master's Thesis, University of Texas at Austin, (1999).

96. S. P. Hau-Riege and C. V. Thompson, J. Mater. Res., 15, 1797 (2000).

97. S. P. Hau-Riege and C. V. Thompson, Mat. Res. Soc. Symp. Proc., 612, D10.2.1 (2000).

98. X. Lu, K.-D. Lee, H. Matsuhashi, and P. S. Ho, Mat. Res. Society Symp. Proc. (April, 2003).

99. S. Thrasher, M. Gall, C. Capasso, P. Justison, R. Hernandez, T. Nguyen, and H. Kawasaki, 7th international workshop on stress-induced phenomena in metallization (2004) 165-172.

100. D. Ney, X. Federspiel, V. Girault, O. Thomas, and P. Gergaud, IITC 105-107 (2005).

101. G. B. Alers, J. J. Kuo, G. Harm, S. R. Weinzierl, and G. W. Gay, Adv. Met. Conf., (2003).

102. Yong Du, Ph. D. Dissertation, University of Texas at Austin (2002).

103. P. C. Andricacos, et al, IBM J. Res. Dev., 42, 567 (1998).

104. M. Kawano, T. Fukase, Y. Yamamoto, T. Ito, S. Yokogawa, H. Tsuda, Y. Kunimune, T. Saitoh, K. Ueno, and M. Sekine, International Interconnect Technology Conference, (2003).

105. G. B. Alers, X. Lu, J. H. Sukamto, S. K. Kailasam, J. Reid, and G. Harm, IEEE IITC (2004).

106. C. V. Thompson, J. Mater. Res. 8, 237 (1993).

107. M. Lane and R. H. Dauskardt, J. Mater. Res.,15, 2758 (2000).

108. Guotao Wang, Ph. D Dissertation, University of Texas at Austin, (2004).

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