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A Novel High-K SONOS Type Non-volatile Memory and NMOS HfO_2 V_{th} Instability Studies for Gate Electrode and Interface Treatment Effects

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A Novel High-K SONOS Type Non-volatile Memory and NMOS HfO_2 V_{th} Instability Studies for Gate Electrode and Interface Treatment Effects

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Dedication

To my parents and my wife

Acknowledgement

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A Novel High-K SONOS Type Non-volatile Memory and NMOS HfO_2 V_{th} Instability Studies for Gate Electrode and Interface Treatment Effects

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According to the 2004 International Technology Roadmaps for Semiconductors (ITRS), one of the most important challenges in the semiconductor flash memory industry is the continuously scaling of the tunneling oxide thickness. As the tunneling oxide is thinner than 100Å, it becomes a formidable challenge to obtain a fast programming and a 10-year long retention simultaneously. In this work, novel Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) type non-volatile memories using high-K dielectric materials are proposed to tackle this problem. Thanks to its lower carrier injection barrier, HfO_2 is found beneficial to improve the programming efficiency even with a physically thicker tunneling oxide as compared to equivalent SiO_2. This thicker tunneling oxide together with a much deeper trap level of the Ta_2O_5 ensures a better retention as compared to thinner SiO_2 tunneling layer and the

Si_3N_4 trapping layer. Therefore, a better trade-off between the faster programming and longer retention is obtained in such high-K SONOS memories. Two structures, the TaN-HfO_2-Ta_2O_5-HfO_2-Si (MHTHS) and the TaN-Al_2O_3-Ta_2O_5-HfO_2-Si (MATHS) are compared and MATHS is found to have better charge blocking due to the higher barrier of Al_2O_3 as the top oxide. The fabricated devices demonstrate fast programming, excellent retention, endurance, and read disturbance as compared to state-of-the-art SONOS devices.

The impacts of the top gate electrodes and bottom interface treatments on the NMOS HfO_2 V_{th} instability are also studied. This knowledge is very important not only to the memory but also to the logic device applications. Both DC and AC stresses are used. The O_3 treated interface is found to lead to worse V_{th} instability due to the enhanced valance band electrons injection as compared to NH_3 treated interface. While a top interfacial layer formed in the poly-Si gated samples is found to introduce more charges trapping under DC stresses than the TiN metal gated samples. But this top layer only plays a minor effect once the stress frequency increases under AC stress conditions.

Table of Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 Background

The non-volatile semiconductor memory industry has seen a significant growth during the last several decades due to the unique mix of the functionality and the cost of the flash memory technology. It has been projected that the flash memory revenue will rise to $17.5 billion in year 2005 and it will continue to expand at a Compound Annual Growth Rate (CAGR) of 14% from 2003 to 2008 according to the semiconductor research company iSuppli. The basic idea of a non-volatile semiconductor flash memory behind such a huge industry is actually fairly simple and is firstly proposed in 1967 [1]. As shown in Fig. 1.1, a continuous floating gate is embedded inside a conventional MOS transistor gate stack. Electrons can be injected and stored in this floating gate by the hot carrier injection. The stored electrons can be erased either by a reversed electric field or by shining an UV light onto the device. The information of "1" or "0" can be found through different threshold voltages introduced with or without the extra electrons in the floating gate as shown in Fig. 1.2. Following the silicon process-scaling rule, flash memory cost per bit has been dramatically reduced and the memory density has increased millions fold from 64Kb to 8Gb to date. However, as the industry continuously scales down the device, it becomes more and more difficult to maintain a fast programming and

10-year data retention simultaneously as the tunnel oxide becomes thinner and thinner. As the tunneling oxide is scaled below 10nm, the stress-induced-leakage-current (SILC) becomes such a severe problem that even one defect can drain the stored electrons out of the floating gate. In the 2004 international technology road-map for semiconductors (ITRS) update [2], the industry has already had a great challenge to scale the tunnel oxide thickness for the NOR type flash to 8-9nm at 65nm and for the NAND type flash to 6-7nm at 45nm generation. A brief summary for these ITRS requirements is shown in Table 1.1. Therefore, in the next 5 years some major breakthroughs may be required either in the process integration or in the device structure so that the scaling trend can be maintained to meet the market's cost per bit and functionality requirements.

In this work, a novel silicon-oxide-nitride-oxide-silicon (SONOS) type non-volatile memory using high-K dielectrics for faster programming and longer data retention is proposed and demonstrated. Such memory structure may also have potential for non-volatile memory applications beyond the 45nm generation. In the following sections the motivations for developing such memory will be discussed. In addition, the impact of different gate electrodes and different interface treatment techniques on high-K NMOS HfO_2 V_{th} instability will also be compared. Such knowledge can provide insight into HfO_2 charge trapping behavior, which is important not only to memory but also to the logic applications.

1.2 Motivations for development of the high-K SONOS memory

1.2.1 Advantages of charge trapping memory vs. floating gate flash memory

One solution to solve the problem of the tunnel oxide scaling in floating gate memory devices is the use of charge trapping memory. A schematic comparison between floating gate and charge trapping memory devices is shown in Fig. 1.3. Compared to the floating gate device, a discrete charge trapping layer is used to replace the continuous floating gate. This charge trapping layer can be either a nitride layer (SONOS) [3] or a Si nanocrystal layer (Si-NC) [4]. As charges are injected into the trapping layer, they are stored inside the nitride traps or Si nano-crystals and are isolated from each other with no lateral charges movement. As a result, such charge trapping memory is more robust to the SILC as the gate stack is continuously scaled down because each defect will only drain charges close to it, instead of all charges in the floating gate. The nitride based non-volatile memory was invented at about the same time as the floating gate memory technology [3]. Because of issues such as high temperature retention, technology complexity, and development entry cost, it has not proven to be as popular as the floating gate technology in the industry. Currently, SONOS technology is only used in a very small market mainly for military and space applications, which require high resistance to radiation.

1.2.2 Recent progress on the SONOS memory development

Very recently, SONOS memory has again received considerable interest. This is mainly due to the discrete charge trapping nature of SONOS, which offers better scalability of the tunneling oxide and/or blocking oxide, and to the two bit per cell storage capability of SONOS, which provides better cost per bit reduction as the industry moves beyond the 45nm generation. Much of the recent work done on SONOS based devices can be divided into two categories: the development of novel programming methods, and the development of novel process and/or structure.

Various programming methods have been proposed for SONOS memories. Conventional SONOS flash memory uses modified F-N electron tunneling to program the cell and direct hole tunneling to erase the cell. A novel NROM structure using SONOS stack with channel hot-electron injection (CHI) for programming and band-to-band tunneling enhanced hot hole injection for erasing has been proposed [5]. By using a reverse read, such a cell can achieve two bits per cell storage with small cell area ($2.5F^2$/bit), which translates to a larger cell density. The CHI programming and the uniform tunnel erase combination have also been proposed for 90nm SONOS flash [6]. The CHI programming can achieve faster programming while the uniform tunnel erase can reduce residue electrons build up. It can also suppress the hot hole damage during erasing. Combination of band-to-band hot hole and electron F-N tunneling is also demonstrated in PHINES devices, which is used to reduce the high power consumption introduced by the CHI programming [7]. Among all these programming schemes, it is hard to tell which one is the best. It will

be strongly related to the specific process and the targeting market requirement. However, no matter which combination is chosen, the ultimate goal is to achieve lower cost per bit while maintaining a scaling trend. If the conventional SONOS technology is used, these different programming schemes might only provide a short term solution. For instance, the CHI programming enables a 2 bits storage operation, which doubles the bit density without pushing the scaling of the cell size. Therefore, a thicker tunneling oxide can be used for a better retention while a faster write can be maintained. But the well-known hot carrier damage to the interface during write/erase will inevitably degrade the device endurance performance. If no hot carriers are used, a thinner oxide is required for fast programming. But this will make it hard to keep 10-year retention as the tunneling oxide becomes thinner for each new generation. Therefore, novel process technology and/or novel material must be needed to compromise the disadvantages of these programming schemes.

The conventional SONOS process optimization is very important but much of the reported findings are mainly from novel material integration into the SONOS structure, which is also the direction this work will follow. For process optimization, CVD grown oxide has been reported to replace the conventional thermally grown oxide for the top blocking layer to achieve a top barrier with better retention [8]. A p^+ poly gate is also reported to suppress the top gate electrode injection current [9]. High temperature deuterium annealing is used to replace hydrogen annealing for better endurance and data retention [10]. The band-gap engineering approach has also been used to modify the SiN band to achieve better charge retention [11]. State-

of-the-art vertical transistor structures have also been applied into SONOS memories for fast operation and to evaluate the possibility of two bits operation [12;13]. Novel material integration can be divided into three categories, corresponding to the top blocking layer, the charge trapping layer, and the bottom tunneling layer. The major function of the top blocking layer is to block the carrier transport either from the gate injection to the trapping layer or from the trapping layer escaping to the gate. Because of its much higher barrier height, Al_2O_3 has been used by several different groups as a top blocking layer for both poly and metal gates [14-16]. For the charge trapping layer, Al_2O_3, HfAlO and HfO_2 have been demonstrated to improve the band offsets for reduced charge leakage [14;17;18]. Little work has been done on the tunneling layer. Recently, a novel SiO_2/Si nano-crystal/ SiO_2 tunneling oxide exploits the coulomb blockade effect to provide improved charge retention [19].

These reported studies have contributed to a better understanding of SONOS device operation and have provided ways for the continuous scaling of SONOS devices. Using these approaches, the tunneling oxide thicknesses have already reached close to 20Å. Below this thickness direct tunneling becomes a huge obstacle to meeting the 10-year retention time requirement. As a result, scaling the tunnel oxide beyond the 45nm node is a huge obstacle for SiO_2 tunneling oxides. Novel materials may need to be introduced for a better trade-off between the faster programming and the longer retention for the flash memory technology beyond the 45nm generation.

1.2.3 Recent progress on high-K dielectric materials

Gate oxide scaling for the microprocessor/ASIC applications has proven to be a significant challenge in the semiconductor industry. In such devices, the gate oxide thickness is scaled more aggressively than the memory applications, and it has been projected a less than 10Å oxide must be used very soon [2]. However, for such a thin SiO_2 gate oxide, the direct tunneling current will lead to excessive gate leakage when the transistor is turned on. As a result, the power consumption and the heat dissipation will become severe problems using SiO_2 as the gate dielectric for future generations.

One of the most promising solutions for continuously scaling the gate oxide EOT below 10Å is the adoption of the high dielectric constant (high-K) materials to replace the silicon oxide. By using high-K gate dielectrics, the capacitive coupling to the channel remains large enough to achieve high drive current, while the increased gate oxide physical thickness can be several times larger than the equivalent silicon oxide thickness (EOT),, significantly suppressing the direct tunneling current. Various high-k materials have been extensively studied, such as Al_2O_3, ZrO_2, Ta_2O_5, and HfO_2. A review on the material considerations of high-K material development for gate dielectrics can be found in [20]. Among all these materials, HfO_2 and Hf based silicate or nitride have been considered the leading candidates due to various attractive features. These include good thermal stability in contact with the Si substrate, compatibility with both poly-Si and metal gates, good band alignments to Si, and excellent TDDB reliability. High performance PMOS and NMOS transistors

using HfO_2 as the gate dielectric with less than 10Å EOT and several orders of magnitude gate leakage current reduction have been reported [21]. The leakage currents at 1V beyond the flat-band voltage for various Hf based high-K dielectrics are compared with the state of the art SiON data as shown in Fig. 1.4 [21-28].

In this work, HfO_2, Ta_2O_5 and Al_2O_3 will be used in the SONOS memory structure for different layers and their advantages for replacing conventional SONOS stacks will be discussed in the following chapters. High quality HfO_2 high-K dielectrics made with CVD have been successfully developed in our facility using both poly-Si and TaN metal gates [29;30]. Such films demonstrqate reduction of the leakage current at an EOT less than 10Å and it also has excellent TDDB reliability. The HfO_2 films used in this work follow the procedures developed in previous work. This work uses the TaN metal gate electrode, since it is a mid-gap metal gate and thus has a large gate electron barrier to prevent back electron injection.

1.3 Motivations for HfO_2 V_{th} instability studies

Although high performance HfO_2 MOS transistors have been demonstrated with EOT less than 10Å and low leakage, long term V_{th} instability under stressing has remained a major challenge for its final integration into next generation microprocessor/ASIC processes. Compared to SiO_2 gate dielectrics more intrinsic bulk traps have been observed in HfO_2 [31]. The physical origin of these traps is not yet fully understood yet and research is still under way to determine the causes. However, one possible reason is that HfO_2 becomes poly-crystalline at thermal treatments exceeding 600°C. In this case, the poly-crystal grain boundary may introduce additional traps.

Contrary to the SiO_2 MOSFET, in which PMOS NBTI is the major reliability concern due to the V_{th} shift, the HfO_2 MOSFET life time is limited by the NMOS PBTI [32]. Models based on traditional charge trapping theory have also reported for predicting the HfO_2 MOSFET life time [33;34]. The interfacial oxide (SiO_2) thickness effect on the V_{th} instability has also been reported [35]. There are few works studying the top and bottom interface impacts on the V_{th} instability due to different gate electrodes or interface treatment techniques. Most of the work up to now is based on poly-Si gated HfO_2 devices and only one work using W gate is reported recently [36]. Therefore, studies of top gate electrode and bottom interface treatment effects on the V_{th} instability is an important issue.

1.4 Outlines

In previous sections, the basic concepts of flash memory and the motivations for developing high-K SONOS memories have been discussed in detail. In the following chapters major achievements of this work on high-K SONOS memory development and V_{th} instability will be presented.

A novel TaN-HfO_2-Ta_2O_5-HfO_2-Si (MHTHS) device will be proposed and demonstrated in Chapter 2. In this chapter, band engineering analysis will be used to compare the advantages of the proposed MHTHS device over the conventional SONOS device. Following band analysis, the device fabrication flow will be illustrated. The memory characteristics will then be presented and discussed.

Though the MHTHS devices show advantages over SONOS devices, the obtained memory window is not large enough for a practical nonvolatile memory application. Therefore, in Chapter 3 a better high-K SONOS structure using a TaN-Al_2O_3-Ta_2O_5-HfO_2-Si (MATHS) stack is demonstrated. A theoretical comparison of the MHTHS and the MATHS structure is shown to demonstrate the advantages of using Al_2O_3 as the top blocking oxide to replace HfO_2. A calculation is also made to determine the Al_2O_3 thickness for comparison with previously made MHTHS devices. The device fabrication flow is then presented, along with Al_2O_3 recipe development. The improved memory characteristics are then compared to the MHTHS and with the state-of-the-art SONOS devices.

In Chapter 4, the impact of different gate electrodes and different interface treatment techniques on the NMOS HfO_2 V_{th} instability both at DC and AC stress conditions is presented. For the gate electrode effect, TiN and the poly-Si gates will be compared. For the interface treatments, the O_3 and the NH_3 treatments are compared. Models will then be proposed to explain the observed results.

In Chapter 5, conclusions will be made to summarize the important results obtained from this work and also to discuss future research topics indicated by this work.

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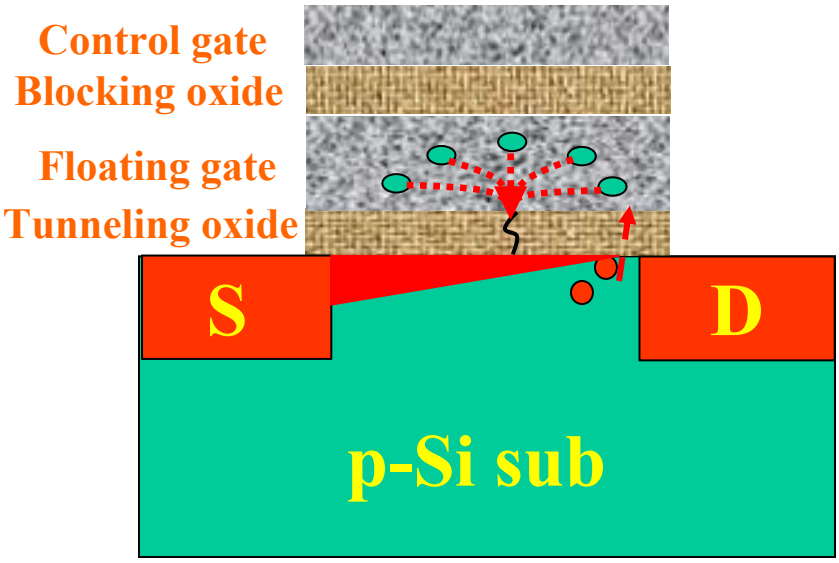

Fig. 1.1 The schematic of the NMOS floating gate memory. The electrons are injected into the floating gate through the hot carrier injection near the drain region when high gate and drain biases are applied. One single defect inside the tunneling oxide may drain all the stored charges.

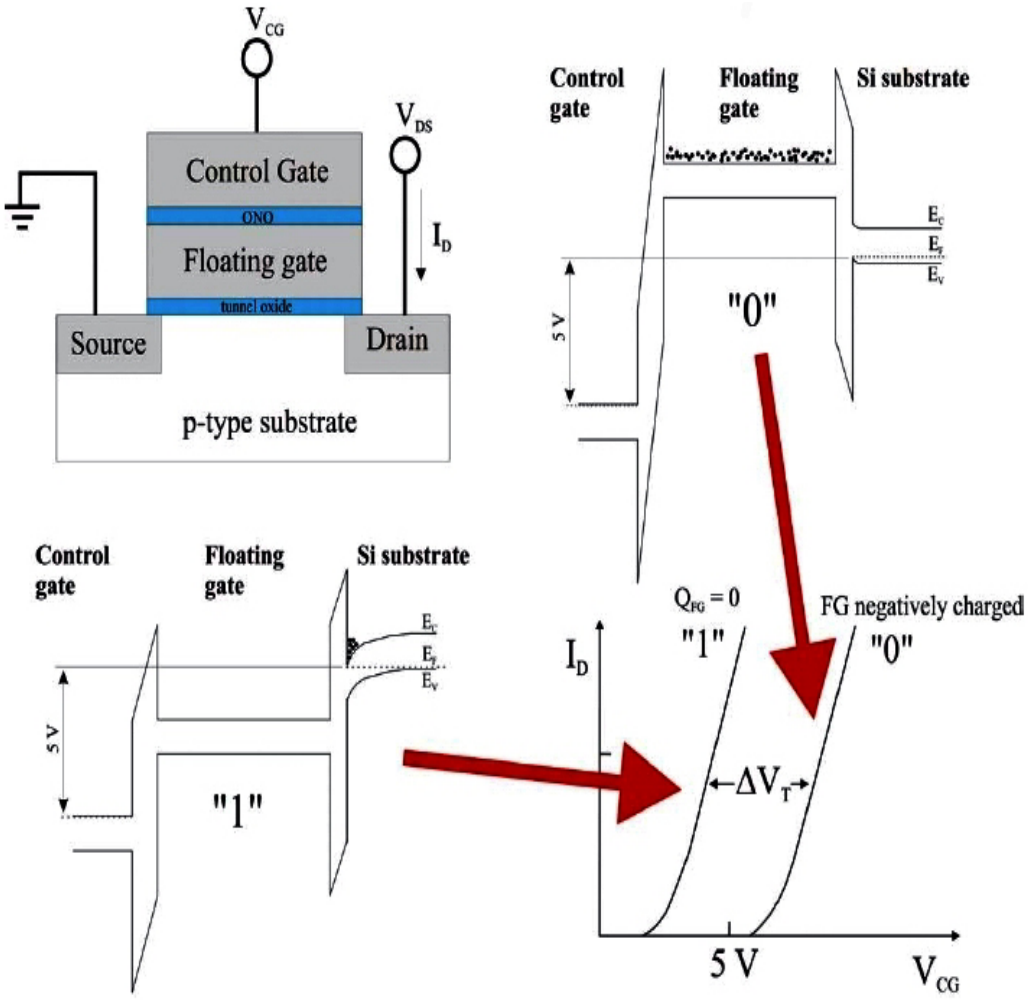

Fig. 1.2 The schematics show the band diagram differences between two devices with and without programmed charge in the floating gate. The resulting Id-Vg curves show different thresholds. Information is read using a "sense" voltage between two thresholds.

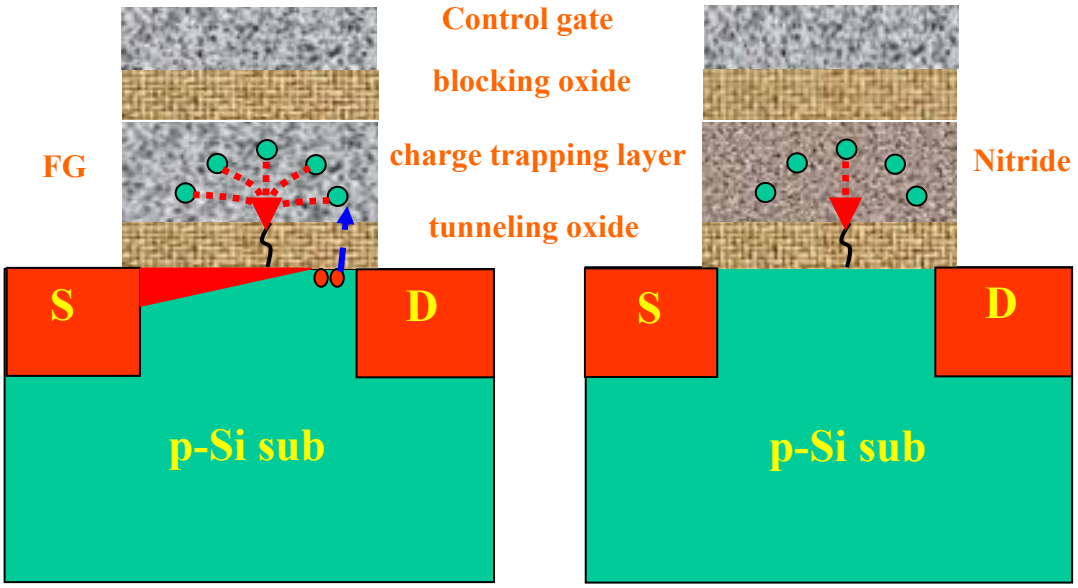

Fig. 1.3 The schematics comparison between a continuous floating gate and a SONOS memory structure. The main difference is the charge trapping layer. In SONOS memories charges are stored in discrete nitride traps. One single defect in such SONOS memory can only drain the charge closest to this defect.

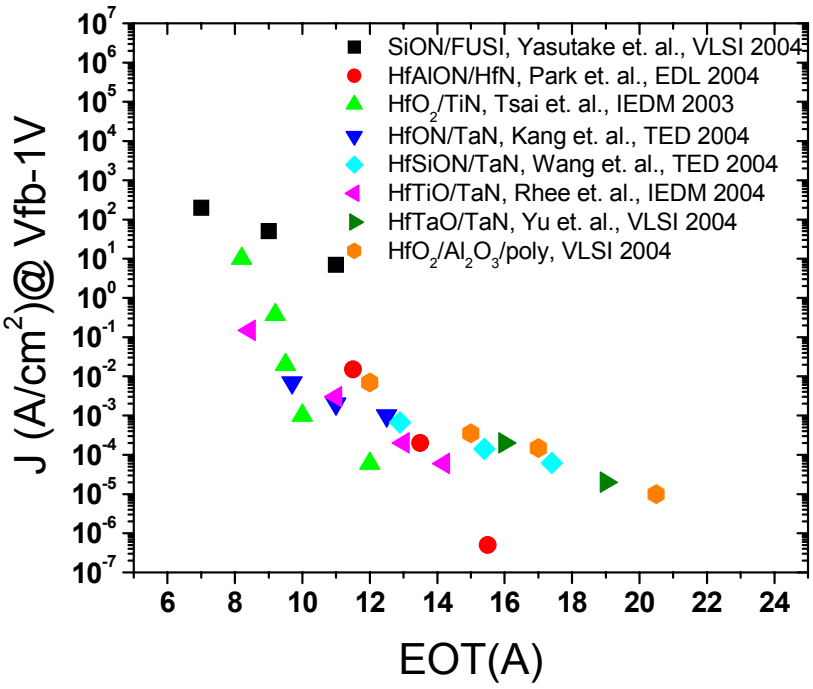

Fig. 1.4 The leakage currents at 1V beyond the flat-band voltage at different EOTs for state-of-the-art Hf based dielectrics and the most recent advanced SiON dielectrics.

Years of production	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013
Flash Technology Node	90	80	70	65	57	50	45	40	35	32
Flash NOR tunnel oxide thickness (nm)	8.5-9.5	8.5-9.5	8-9	8-9	8-9	8-9	8-9	8-9	8-9	8
Flash NAND tunnel oxide thickness (nm)	7-8	7-8	6-7	6-7	6-7	6-7	6-7	6-7	6-7	6-7
SONOS/NROM tunnel oxide thickness (nm)	5	4.5	4	3.5	3.5	3.5	3	3	3	2.5
SONOS/NROM nitride dielectric thickness (nm)	5	5	4.5	4	4	4	4	4	4	4
SONOS/NROM blocking oxide thickness (nm)	5	4.5	4.5	4	4	4	4	4	4	4

Table 1.1 The scaling requirements for the conventional flash and SONOS memory devices predicted in the ITRS 2004. The yellow color represents known solutions under investigation and the red color represents solution is not known.

Chapter 2 Novel MHTHS Nonvolatile Memory

2.1 Introduction

In this chapter, a novel TaN-HfO_2-Ta_2O_5-HfO_2-Si (MHTHS) nonvolatile memory device will be presented. By using HfO_2 as the bottom tunnel oxide and top blocking layer, and Ta_2O_5 as the charge trapping layer, faster programming and a longer data retention can be obtained as compared to conventional SONOS devices.

A band engineering analysis comparing the MHTHS and the SONOS devices at Write, Retention and Erase modes is demonstrated first. Due to lower electron and hole injection barriers, F-N tunneling programming in the HfO_2 tunneling layer is greatly enhanced. As a result, physically thicker films can be used for the tunnel oxide while preservig programming efficiency. Due to deep trap levels in the Ta_2O_5 trapping layer and to larger band offset with the HfO_2 tunneling layer, the retention of this device can also be improved.

The detailed device fabrication flow will follow the band engineering analysis. A two mask process using a ring shaped transistor structure is also introduced. This can significantly reduce the process flow and improve research productivity.

The basic electrical data for the gate stack material, HfO_2 and Ta_2O_5, will be shown first. Detailed memory characteristics: the memory window, the programming

transient, the charge retention, the data endurance and the read disturbance will next be demonstrated and discussed in detail. These devices are shown to have very fast write and erase speed, and close to 3 times improvement in the data retention as compared to SONOS devices. This is achieved at a tunneling oxide thickness of 9.5Å equivalent oxide thickness (EOT).

To conclude, the advantages and disadvantages of this MHTHS device will be summarized. An improvement in device structure by introducing other high-k material is briefly discussed.

2.2 Band engineering analysis

2.2.1 Write

The energy diagrams of the traditional SONOS device and the proposed Metal-HfO_2-Ta_2O_5-HfO_2-Si (MHTHS) device at Write mode are illustrated in Fig. 2.1. In the SONOS devices (Fig. 2.1a), electrons must tunnel through both the tunneling oxide and part of the nitride layer by modified F-N tunneling [3] because of the 3.2eV high barrier. But for the MHTHS device, the barrier height for the electron injection is only 1.5eV (Fig. 2.1b). Such a low electron barrier improves the programming in two ways as shown by the conventional F-N tunneling equations in equations 2.1-2-3:

$$J = \alpha E_{inj}^2 \exp[\frac{-E_c}{E_{inj}}] \qquad 2.1.$$

$$\alpha = \frac{q^3}{8\pi h \varphi_b} \frac{m}{m^*} \qquad 2.2.$$

$$E_c = 4\sqrt{2m^*} \frac{\varphi_b^{3/2}}{3\hbar q} \qquad 2.3.$$

where h = Planck's constant

φ_b = the energy barrier at the injection interface

E_{inj}= the electric field at the injection interface

q = the charge of a single electron

m = the mass of a free electron

m^* = the effective mass of an electron in the band gap

The E_c term, is proportional to the electron barrier by a power law factor of 1.5, while the injection current is exponentially dependent on E_c. Therefore, a lower injection barrier significantly improves the injection current. F-N tunneling due to the injection field (E_{inj}) term starts to occur when a tri-angular energy barrier forms as the band bending in the tunneling layer is lower than the Si substrate conduction band edge. Due to a lower electron injection barrier in HfO_2, the voltage needed to start F-N tunneling in the HfO_2 tunneling layer will be smaller than that in the SiO_2 tunneling layer. Therefore, for a fixed thickness of tunneling layer, a smaller voltage can be used for the HfO_2 device to start the F-N tunneling. In other words, if the same programming voltage is used, a thicker HfO_2 can be used to achieve the same programming current. A thicker tunneling oxide is very important since it can greatly improve the device retention. In conclusion, this low barrier allows the HfO_2 tunneling layer to have a larger physical thickness with the same EOT while still retaining a high F-N current for faster programming.

2.2.2 Retention

In the data retention mode as shown in Fig. 2.2, there are two possible charge loss mechanisms, as shown by dashed lines. The first one is the direct back tunneling with a barrier height determined by both the conduction band offset ΔE_c and the trap energy level E_{tr}. The second one is the thermally assisted electron detrapping and subsequently tunneling back to the substrate through a barrier height of ΔE_c. Therefore, for better retention deeper trap levels and band offsets are desired. It has been known that the trap level in Si_3N_4 is about 1eV below the conduction band and that the conduction band offset for nitride to oxide is about 1.05V (Fig. 2.2a). For Ta_2O_5, a 2.7eV deep trap energy level has been reported [4] (Fig.2.2b), which is much deeper than that of the Si_3N_4 trap level. The 1.2eV band offset of Ta_2O_5 to HfO_2 is also favorable with respect to the 1.05eV band offset in the SONOS device to prevent the back tunneling. Another important factor to suppress the back tunneling current is the tunneling oxide thickness. As in the discussion for the "Write" mode in the precious section, a physically thicker HfO_2 tunneling layer can be used due to its lower electron barrier. Therefore, these parameters are effectively optimized in MHTHS devices with respect to SONOS devices for better retention, making them ideal for the future scaling.

2.2.3 Erase

For the Erase mode as shown in Fig. 2.3, similar arguments apply. During erase, holes will be injected to compensate for the stored electrons. For HfO_2 the hole injection barrier is 3.4eV, which is about 1eV lower than that of the SiO_2 injection barrier. Erase is achieved by direct hole tunneling, therefore a thick high-K barrier may not be desirable for erase speed since direct tunneling is thickness dependent. As will be shown in the experimental data, this is true if low bias (<6V) is used. But if the erase bias is increased beyond -8V, a very fast erase time is observed, even faster than the writing speed. This is due to the unique trap nature of Ta_2O_5, whose trap levels enable a direct band to trap tunneling from the Si substrate to the traps. This will be discussed in detail with the experimental data.

Another advantage of this MHTHS device during erase is that gate electron injection can be suppressed. Because the TaN metal gate work-function is about the mid-bandgap of the Si, the electron back tunneling barrier is increased by about 0.5eV as compared to the poly-Si gate.

2.3 Device fabrication

2.3.1 HfO_2 films deposition

High quality MOCVD HfO_2 films have been reported by our group with excellent leakage reduction and TDDB reliability [5]. HfO_2 used in this work will follow the same recipe.

A P-type Si (100) substrate is used for NMOSFET transistors fabrication. Wafers are first cleaned in Pirannah solutions for 8mins and then dipped in a 40:1 diluted HF solution to remove the native oxide. After cleaning, the wafers are immediately transferred to the high vacuum MOCVD chamber with a back pressure of 1E-6 Torr. This MOCVD chamber uses RTP deposition method. A 700°C, 10s NH_3 treatment is first done to improve the interface quality. Immediately following the interface treatment the HfO_2 tunneling oxide layer is formed by using Hafnium t-butoxide ($Hf(OC_4H_9)_4$) RTP processing at 500°C for about 3 minutes. The mass flow controller setting during the deposition is carrying Ar 15%, O_2 100%, diluted Ar 8%. The reaction chamber pressure is stabilized at 2.6~3Torr. A 700°C, 30s post deposition annealing is done after the HfO_2 deposition to improve the films quality. The resulting HfO_2 thickness can be measured with an ellipsometer and has thickness of about 50Å, which translates to a 16.7Å/min deposition rate.

2.3.2 Ta_2O_5 film deposition

After HfO_2 formation, the wafer is immediately transferred to an ultra-high vacuum sputtering chamber with a base pressure of 5E-7Torr. A 6 inch pure Ta target is used for the DC sputtering process. Before the film deposition, a 3min, 600W pre-sputtering in Ar ambient is done to clean the target. The gas setting for the sputtering is 10% and the reaction pressure is set at 30mTorr. The power for the sputtering can be controlled in either "power constant" or "current constant" mode. If constant power control mode is used, the minimum power is 100W and the Ta deposition rate is so rapid that the film thickness is difficult to controll. Therefore, the current control mode is used and the current is set at 0.35A. This corresponds to a power of 70~80W and the voltage applied is about 220V.

After PVD sputtering, the wafer is annealed in a RTP chamber at 550°C, 5mins in a N_2 atmosphere. However, small traces of O existing during this annealing so that the Ta won't be over oxidized. After oxidation, the final Ta_2O_5 thickness is measured using the ellipsometer. The final Ta_2O_5 thickness is determined by the sputtering deposition time giving deposition rate for the Ta_2O_5 is about 61Å/min. It should be noted that the total (HfO_2 + Ta_2O_5) stack thickness can still be measured using the ellipsometer due to the similar refractive indexes of HfO_2 and Ta_2O_5, which is about 2.1,.

2.3.3 Transistor fabrication and two mask process

After Ta_2O_5 deposition, the wafers are transferred back to the RTP MOCVD chamber for deposition of the top blocking HfO_2 layer using the recipe described in Section 2.3.1. The metal TaN gate is deposited using the PVD DC sputtering tool. The gas setting for Ar is 20% and for N_2 is 4%. The reaction pressure is kept at 10mTorr. The power for the sputtering is 700W. For a 5min sputtering, the TaN thickness is about 2000Å and the sheet resistance is around 30Ω/□. Thus the TaN deposition rate is approximately 400Å per minute.

For device pattering, a two mask process is used to create the ring transistor structure shown in Fig. 2.4a. Such a process has no need to use field oxide. The first mask is used to define the gate and channel, while the second mask is used to define the source/drain contact. The whole transistor is en-circuled by a rectangular metal isolation ring. The source also surrounds the transistor channel. It should be noted that for such structure the effective channel width is not that labeled in Fig. 2.4b. A transfer equation is shown in eqn 2.4:

$$W_{eff} = \frac{8L}{\ln(1+2L/W)} \qquad 2.4.$$

Various sizes used in the mask are summarized in Table. 2.1.

After gate pattering, reactive ion etching (RIE) using CF_4 is used to etch away both the TaN and the gate dielectrics at the source/drain. The power is 150W and the gas setting is 50%. Then the source/drain is implanted with P^{31} with ion

energy of 50KeV and dosage of 5E15/cm^2. Source/drain activation is done at 700°C for 2mins. For actioation anneal temperatures beyond this point, the memory window will be significantly reduced. It is found that Ta_2O_5 becomes very leaky when heated above this temperature and shows decreased charge trapping. The process is completed with source/drain metallization using Al sputtering.

To confirm the Ta_2O_5 charge trapping, a control sample without the Ta_2O_5 charge trapping layer is also fabricated using a process identical to the other memory wafers except for Ta_2O_5 deposition.

The final transistor devices used for characterization have a stack structure of Si-HfO_2(48Å)-Ta_2O_5(64Å)-HfO_2(100Å)-TaN. The EOT of the 48Å HfO_2 tunnel oxide is determined to be 9.5Å from the C-V measurement.

2.4 Basic electrical data

2.4.1 HfO_2

HfO_2 only stacks with different thicknesses were tested to verify the HfO_2 film quality. A typical capacitor C-V curve is shown in Fig. 2.5. The experimental data has an excellent fit to the simulated C-V, including the quantum mechanical effect [6]. This indicates an excellent interface in contact with the Si substrate. The leakage currents at one volt beyond the flat band voltage for different equivalent oxide thicknesses are shown in Fig. 2.6. The SiO_2 data are also shown in the same figure for the comparison. Form Fig. 2.6, It is clear that these HfO_2 can significantly reduce the leakage current by several orders of magnitude.

2.4.2 Ta_2O_5

The Ta_2O_5 only C-V curve is shown in Fig. 2.7. By sweeping the bias from -SV to SV and back to -SV, a hysteresis window as large as 0.85V is obtained. This hysteresis window is consistent with electron charge trapping as discussed in section 2.2. In Fig. 2.8, the HfO_2-HfO_2 only stack and the HfO_2-Ta_2O_5-HfO_2 stack are compared. It is clearly shown that the hysteresis is negligible without Ta_2O_5, while introduction of the Ta_2O_5 significantly increases the memory window. This indicates that Ta_2O_5 introduces the memory effect into this stack configuration.

2.5 Memory characteristics

2.5.1 Memory window

The MHTHS N-MOS transistor Ids-Vds curves are shown in Fig. 2.9. This device is then programmed and erased using ±8V, 1ms gate pulse with source, drain and substrate grounded. C-V hysteresis indicates a 0.8V memory window as shown in Fig. 2.10. The Ids-Vgs shown in Fig. 2.11 also show the 0.8V memory window, which is consistent with the C-V result. The EOT of the HTH stack is determined by C-V curves to be 42Å.

Compared to state-of-the-art SONOS memories [7-11], a 0.8mm memory window is not as large and not very practical for the real memory applications. As will be shown in the next section, this small memory window is not due to the Ta_2O_5 trapping capability but arises from poor top blocking.

2.5.2 Programming and Erase Characteristics

Programming speeds at various gate voltages are shown in Fig. 2.12 and 2.13. The "threshold shift" is defined as the threshold change between a written/erased device and a virgin device if not otherwise specified. When the device is biased at 4V as shown in Fig. 2.12, the programming voltage is not large enough to start the F-N programming. The memory window starts to open from 0.1ms under writing and 1ms under erasing. When the device is biased at 6 and 7 volts, the threshold voltage starts to shift from 10μs writing and 1ms erasing in the same figure. But at higher biases such as 8 and 10 volts, the threshold voltage shift can start from 1μs under writing and an extremely fast 10ns erasing speed is observed in Fig. 2.13. The programming current vs. the programming voltage curve is shown in Fig. 2.14. The insert in Fig. 2.14 shows the F-N plot and the excellent linear relation confirms that F-N tunneling is the dominant mechanism at the "Write" mode starting from 6.5V. The extracted barrier height from the F-N plot is about 1.4eV, which matches well with published data used in Fig. 2.1 [1].

The conduction mechanism responsible for the ultra fast 10 ns erasing speed in the "Erase" mode is not fully understood in the literature. I propose enhanced band to trap hole tunneling to explain enhanced erase speeds. The erase configuration is drawn in Fig. 2.2 showing the Ta_2O_5 trap level to be 1.3eV below the Si valence band edge E_v at zero bias. Note that this level is below E_v at low erasing bias. However, when erasing bias is increased to the point that the Ta_2O_5 trap levels are

aligned with or above E_v, these trap states are energetically favorable for direct tunnelling of holes in the valance band to them. In this bias configuration, injected holes can be captured directly by electrons already trapped in the Ta_2O_5 layer as shown in Fig. 2.3, resulting in greatly enhanced hole capture efficiency and hence larger hole current. Under such bias conditions, the erase speed could be even faster than the write speed, as seen in the data of Fig. 2.13, since the “Write” mode speed is not enhanced, since electron capture is not as efficient as in the high bias “Erase” mode. Since electrons in the "write" mode always need to tunnel to the Ta_2O_5 conduction band first and be subsequently captured as illustrated in Fig. 2.1. The capture of back tunneling electrons from the top electrode during erase is also not as efficient as hole injection at this bias condition. Therefore, the erase saturation as shown in Fig. 2.12 cannot be observed in Fig. 2.13.

Fig. 2.13 shows a saturation of the program V_t for program beyond 8V. It also should be noted that the memory window will go to a faster saturation even at the Write mode. The erase saturation due to the back gate electron injection to compensate for the injected holes has long been understood. Such fast write saturation indicates the writing is not very efficient in this novel MHTHS device. The detailed explanation and the solution to this problem will be discussed in the next chapter. The programming speed between this work and some most recent SONOS work are compared in Table 2.2 to demonstrate the superiority of the MHTHS device.

2.5.3 Data retention

The data retention characteristics of the MHTHS device at both room temperature and 85°C are shown in Fig. 2.15. In the first 1000s of data storage, the program V_t has minimal degradation; after 1000s the program V_t starts to degrade at an accelerated decay rate of about 50mV/dec. Such program V_t degradation has been reported and explained in SONOS devices [12]. As shown in Fig. 2.16, once the electrons are injected into the charge trapping layer, a built in electric field exists in the retention mode. Under the influence of the built in field, trapped charges can drift to the top and the bottom of the charge trapping layer. The drift time period corresponds to the slow degradation in program V_t seen for t<1000s in fig. 2.15. Once the electrons approach the interface, they start to escape from the trapping layer and therefore lead to a program V_t degradation at an accelerated rate. Compared to recently published SONOS device data [9;10;13;14] in Table 2.2 , the MHTHS program V_t decay rate is improved by a factor more than three over contemporary SONOS device. Since the starting memory window of the MHTHS device is smaller than the compared SONOS devices, a normalized parameter, time for a 20% charge loss is used to evaluate the data retention performance. As shown in Table 2.2, the MHTHS device has better data retention than SONOS type devices. The extrapolated memory window for 10 years retention is 0.64V at room temperature and 0.42V at 85°C.

2.5.4 Write/Erase Endurance

The write/erase endurance of the MHTHS device is shown in Fig. 2.17. No degradation is observed up to 10^4 write/erase cycles using ±8V 1ms stress. The excellent endurance of the MHTHS arises from the fact that the write/erase electric field in the MHTHS devices is smaller than that in SONOS devices due to the lower electron and hole barrier height. As shown in Fig. 2.14, F-N programming for the MHTHS device can start at fields as low as 3MV/cm. This is well below the field necessary for SONOS device programming, which normally exceeds 7MV/cm. The smaller programming field in the MHTHS is desirable for better endurance because stress-induced degradations in the NVM devices are normally related to interface traps generated at the tunnel oxide-Si substrate interface. The interface state generation rate is proportional to the applied electric field across the tunneling oxide layer. The interface traps density before and after the endurance was measured for the MHTHS device and is shown in Fig. 2.18. Only slight increase of the interface trap density at mid band-gap is observed, indicating that the MHTHS device has excellent immunity to stress induced trapping.

2.5.5 Read disturb

Read disturb is a reliability issue for both SONOS and MHTHS memory. The read distub stress is illustrated in Fig. 2.19. In a memory array, the cell is read by applying a small sensing bias on the selected cell word line and the current is sensed by applying the drain voltage to the bit line. For cells on the same word line, the read bias may provide a low-voltage since the drain, source and substrate are all grounded. If the read disturb cell is erased, the low voltage write can change the cell state to written state and lead to an error. Such read disturb can be characterized by using erased memory cells. The change in erased device threshold voltage due to read disturb for this MHTHS device is shown in Fig. 2.20. At Vgs=1.5V read bias, the MHTHS device has negligible threshold shift up to 5000s and only 30mV shift is observed at 10000s read disturb. After ±8V, 1ms stress for 10000 cycles, the maximum threshold shift is 0.11V at 10000s, comparable to that of the state-of-the-art SONOS device [13]. The band diagrams in the Fig. 2.20 insert is used to illustrate the reason for enhanced read disturb performance in MHTHS devices. At low reading bias the MHTHS device works in the direct tunneling regime to the bottom tunneling layer. Compared to equivalent SONOS devices, the much larger physical thickness used in the MHTHS high-k HfO_2 tunneling layer compensates for its electron barrier lowing and effectively suppresses the read disturb current. At high write bias, the electrical thickness for electrons tunneling into the oxide conduction band decreases due to the switch from direct band to band tunneling to F-N tunneling.

Therefore, fast programming and small read disturbance are also optimized in this MHTHS device structure.

Other disturb mechanisms include gate and drain disturb. These are disturbs taking place during the write operation for unselected cells on the same word lines or bit lines. Gate disturb is for the same work line as another cell being programmed. These disturb effects can be suppressed by using the bias splitting technique. Instead of using 8V on the gate and 0V on the substrate, a +4V gate bias and -4V substrate bias can be used for programming. From Fig. 2.12, when the programming time is less than 1ms, the -4V substrate bias applied on an unselected bit has negligible effect in changing its state. Therefore, gate and drain disturb can be minimized using bias splitting.

2.6 Summary

In this chapter, significant advantages of the newly proposed MHTHS nonvolatile memory over traditional SONOS devices are analyzed and demonstrated. Through band engineering analysis, the superiorities of the MHTHS device in obtaining faster programming and longer retention than the SONOS device is demonstrated. Fabricated MHTHS devices show fast write speed in the 10μs range and an ultra fast 10ns erase speed is observed for the first time. Excellent retention, endurance and read disturbance are also achieved for the MHTHS device and discussed. These results show that the MHTHS HfO_2-Ta_2O_5-HfO_2 stack has a high potential to replace ONO stack for improving the data retention and programming speed simultaneously.

Though the MHTHS devices show fast programming, long retention and good endurance, the MHTHS memory window is relatively small for a practical memory application. The programming transient data shows very fast program saturation, demonstating low programming efficiency even after increasing the program voltage, which suggests an intrinsic limitation for the MHTHS device structure. In the next chapter, an optimized high-K SONOS structure will be demonstrated which improves the memory window without sacrificing programming speed and data retention.

2.7 References

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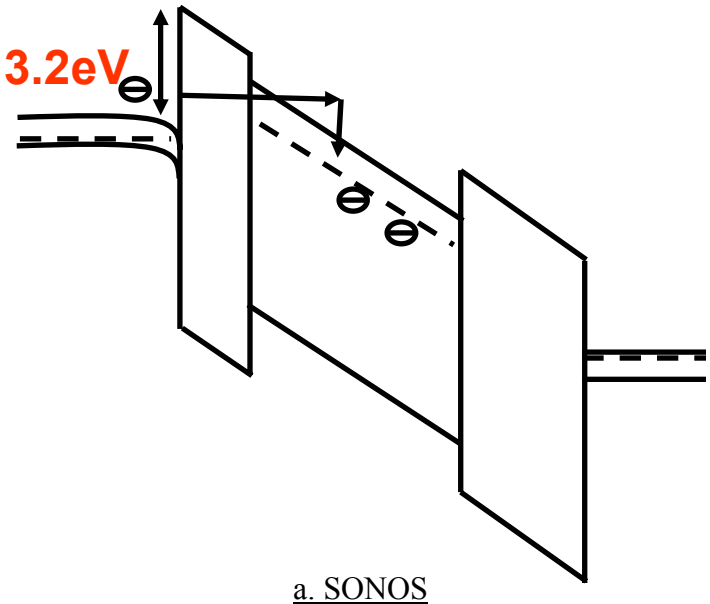
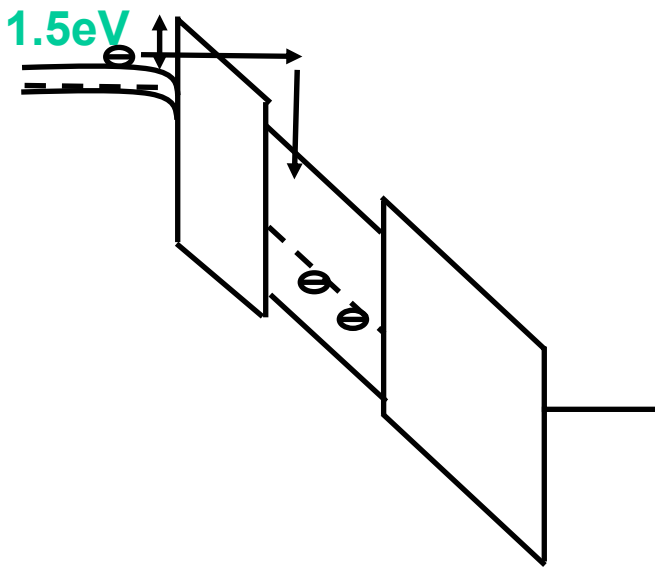
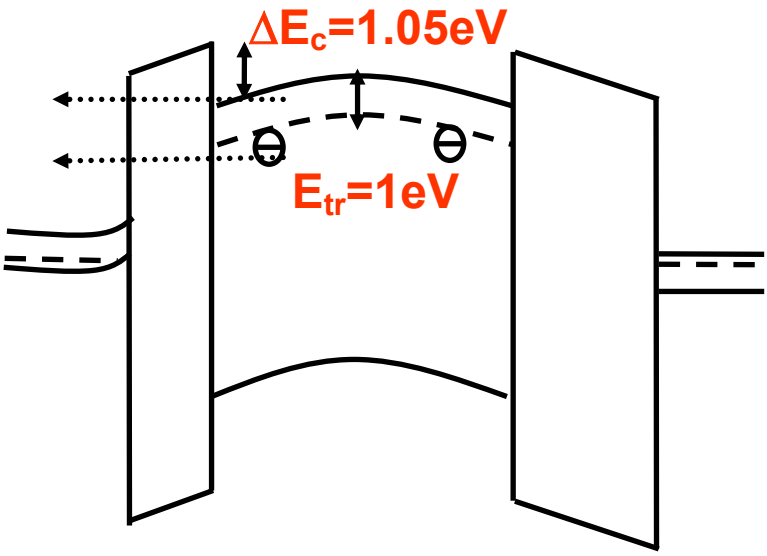


a. SONOS

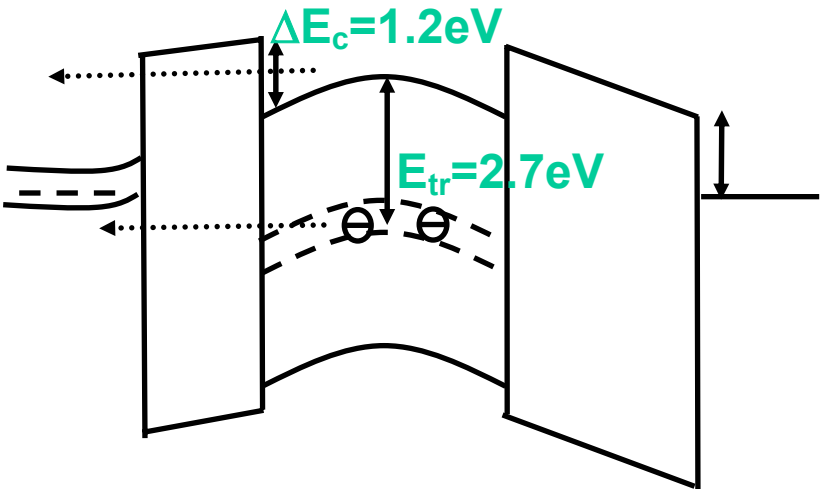


b. MHTHS

Fig. 2.1 The energy band diagrams for the a) SONOS and b) MHTHS devices at the Write mode. The lower electron barrier for the HfO2 (b) than the SiO2 (a) improves the F-N tunneling efficiency even when a physically thicker layer is used.



a. SONOS



b. MHTHS

Fig. 2.2 The energy band diagrams for the a) SONOS and b) MHTHS devices at the Retention mode. The deeper trap level and the larger band offset of the Ta_2O_5 trapping layer to the HfO_2 tunneling layer is more desirable to keep a better retention than the SONOS devices.

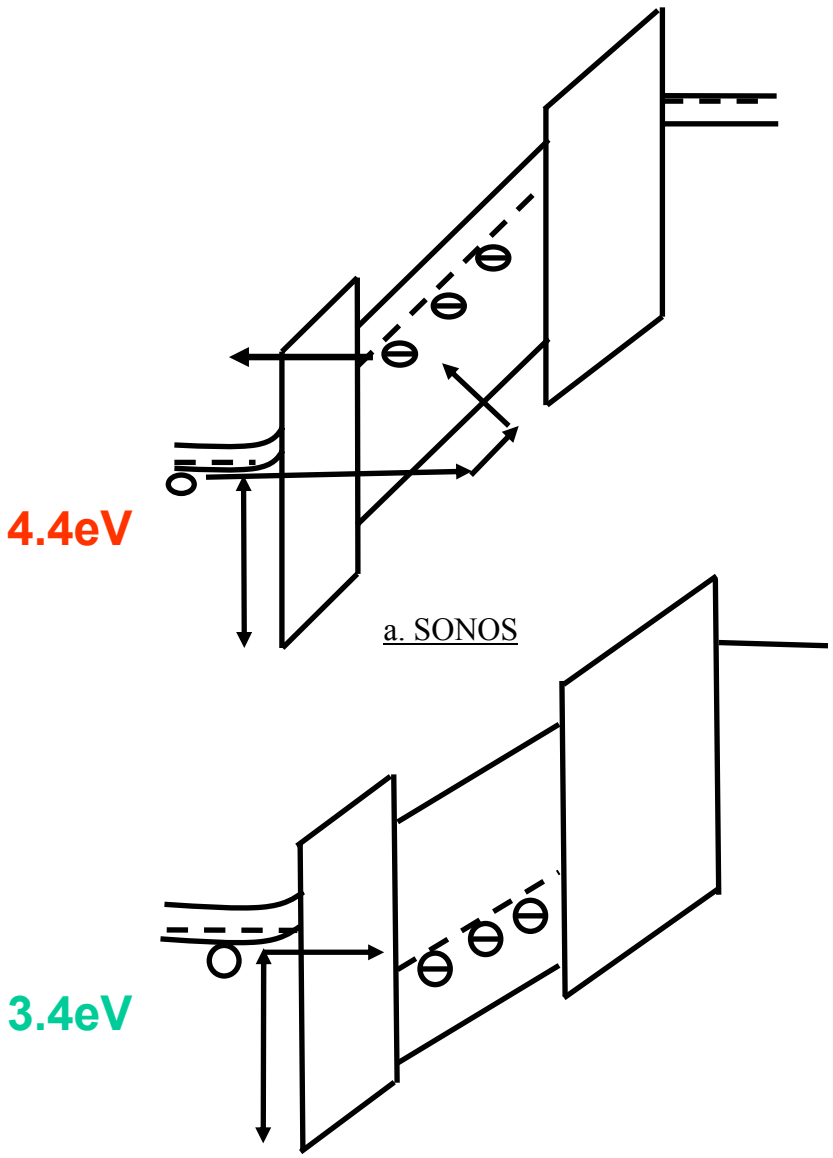
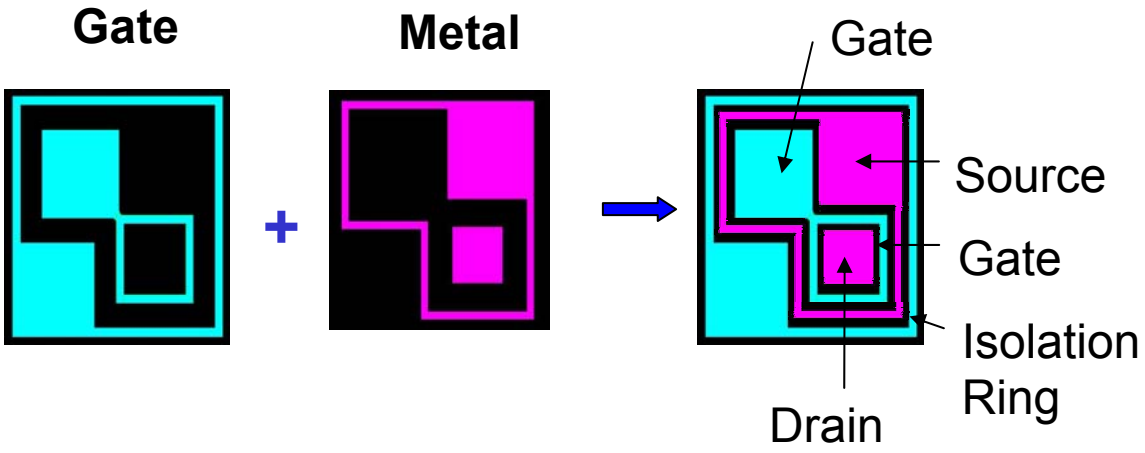
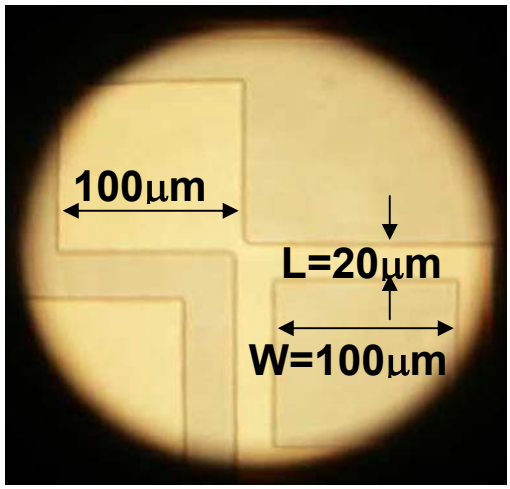


Fig. 2.3 The energy band diagrams for the a) SONOS and b) MHTHS devices at the Erase mode. The hole barrier in the MHTHS device is also lower than that of the SONOS device. A direct band to trap hole tunneling may enhance the erasing efficiency to improve the erasing speed.



(a)



(b)

Fig. 2.4 (a) Schematic diagrams of the two masks used for the MHTHS transistors and (b) the dimension used for the effective channel width calculation as shown in equation 2.4.

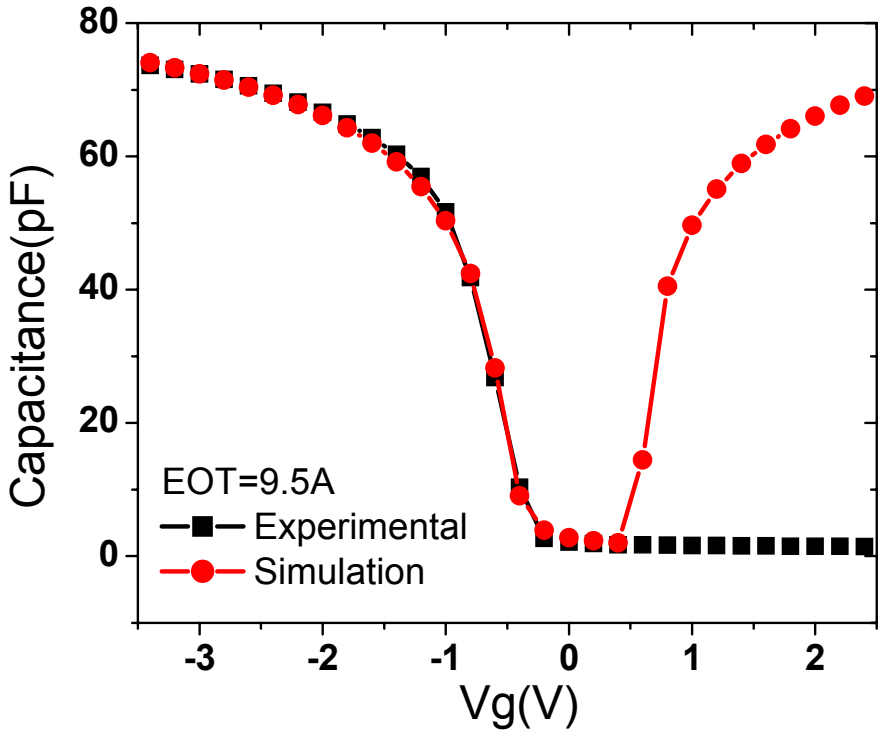


Fig. 2.5 The excellent fit of the experimental HfO_2 only CV data to the theoretical simulation curves show a good interface in between the Si substrate and the HfO_2 film.

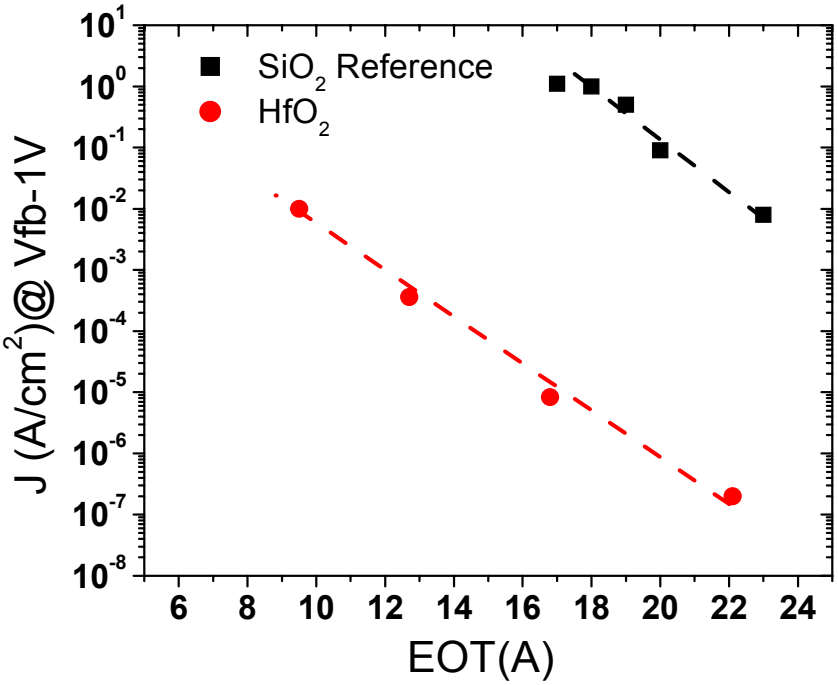


Fig. 2.6 Gate leakage current at 1V beyond the flat band voltage for HfO_2 films at different thicknesses. SiO_2 data is also plotted as a reference. It is clearly shown that the leakage current can be significantly reduced using HfO_2 for the gate dielectric.

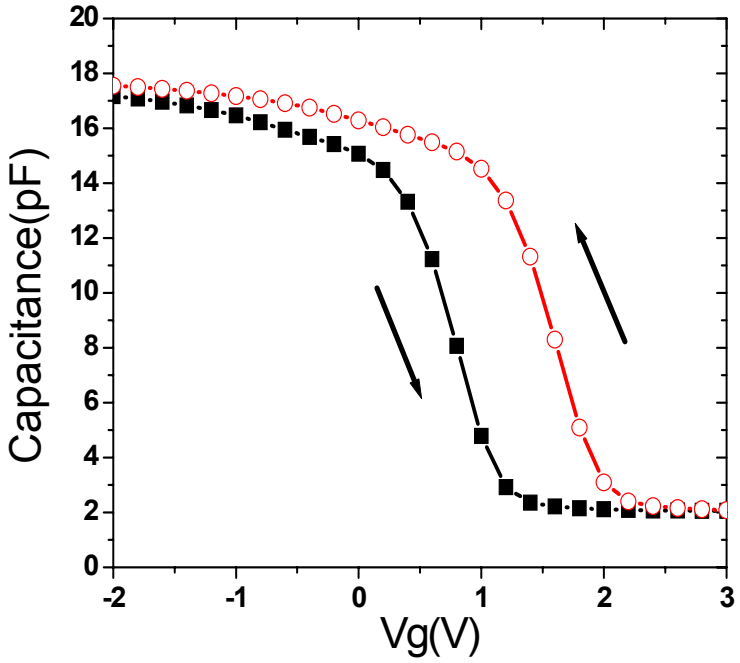


Fig. 2.7 C-V hysteresis for Ta_2O_5 only stacks swept from -5V to 5V and back to -5V. A 0.85V memory window is observed due to the Ta_2O_5 charges trapping.

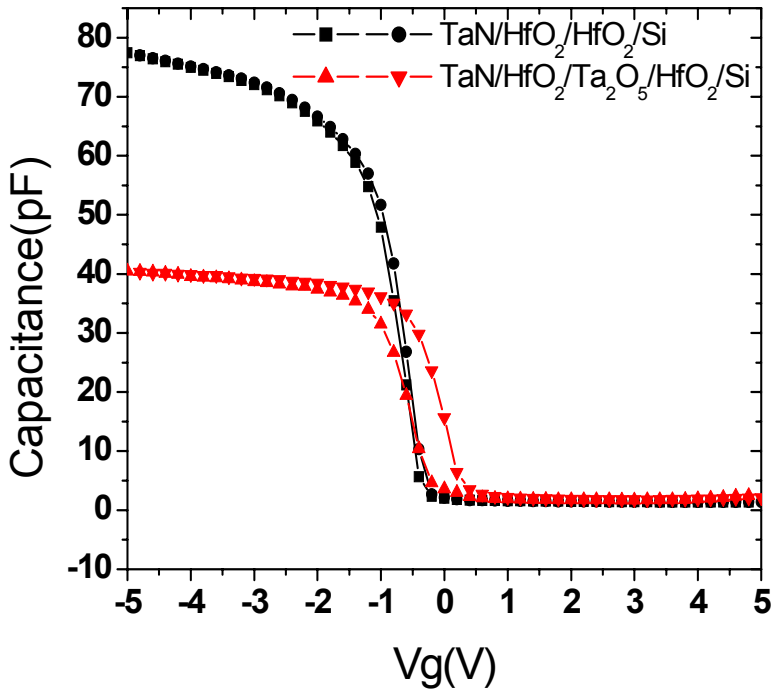


Fig. 2.8 Normalized C-V hysteresis curves for HfO_2 only stack and the stack with Ta_2O_5 charge trapping layer. Negligible hysteresis is observed in the HfO_2 only stack while large hysteresis is found in the Ta_2O_5 added stacks.

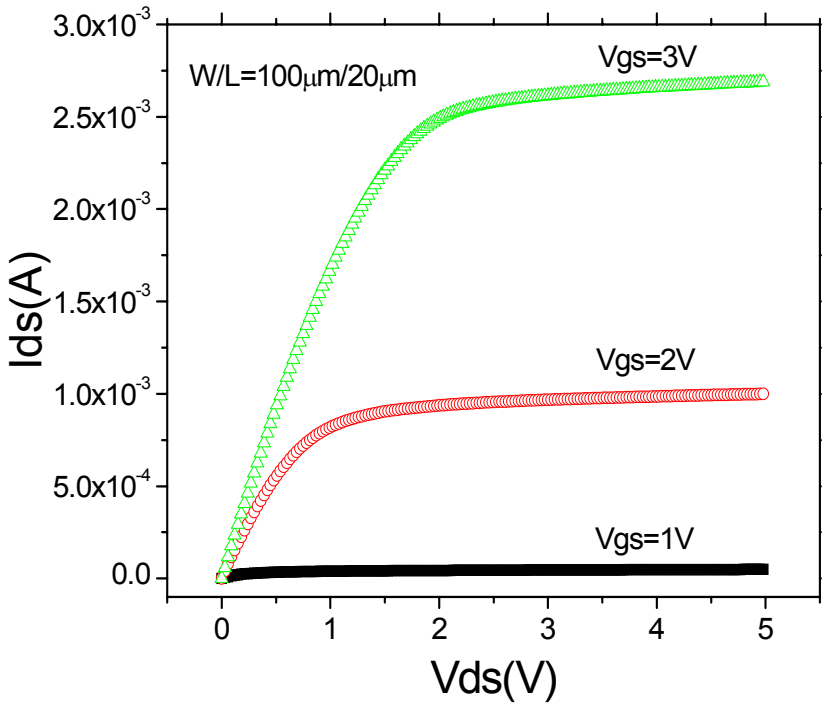


Fig. 2.9 The well behaved Ids-Vds curves of the MHTHS devices.

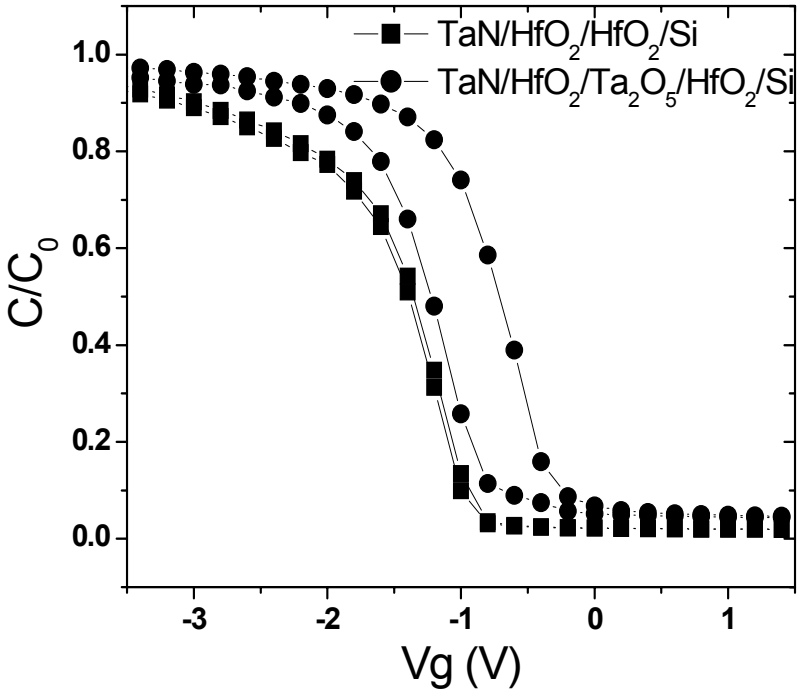


Fig. 2.10 Transistor C-V hysteresis shows the memory window of the MHTHS devices. Little hysteresis is found in the stack without the Ta_2O_5 stacks.

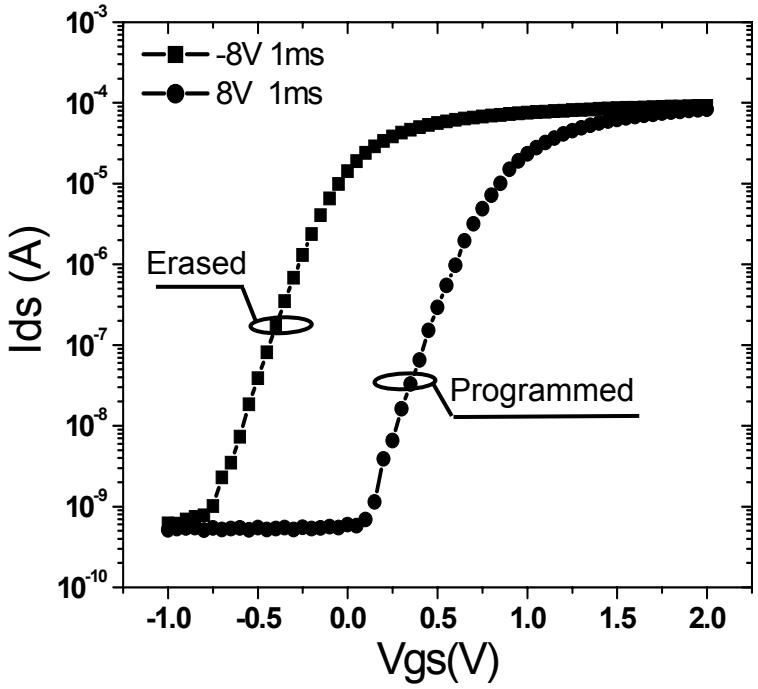


Fig. 2.11 The transistor Ids-Vgs hysteresis show a 0.8V memory window after the MHTHS device is programmed under ±8V, 1ms.

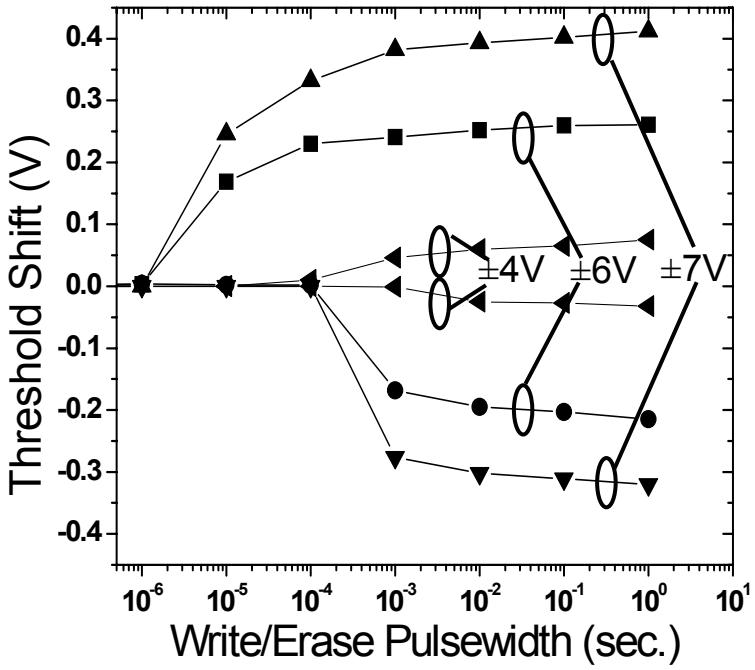


Fig. 2.12 MHTHS programming transients under 8V programming. Memory window starts to open from 10μs and being erased from 1ms when programming voltage is larger than 6V. At 4V programming, the memory window starts to open at 1ms for both writing and erasing.

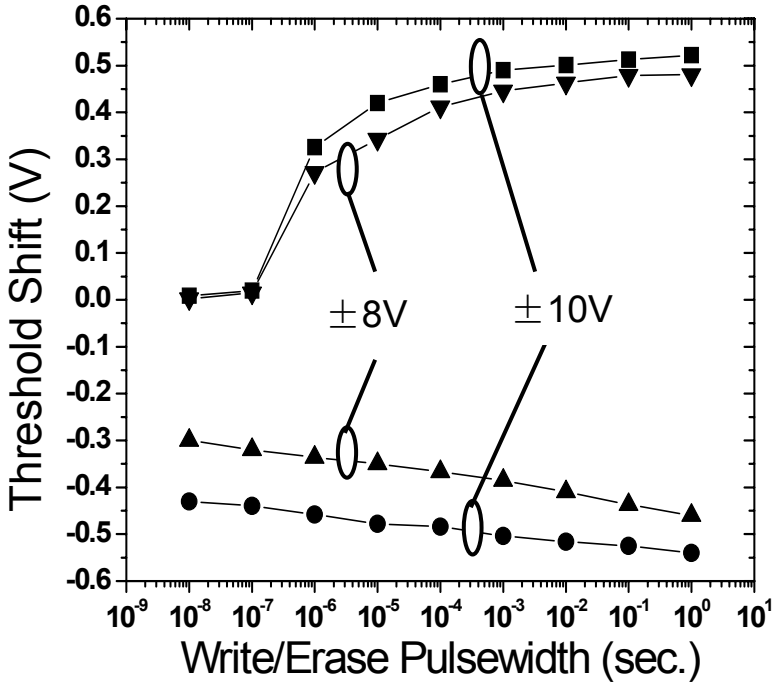


Fig. 2.13 MHTHS Programming transients beyond 8V programming. Note that Memory window starts to open from 1μs and being erased from 10ns. But memory windows saturate very fast and do not increase much as the programming voltage increases.

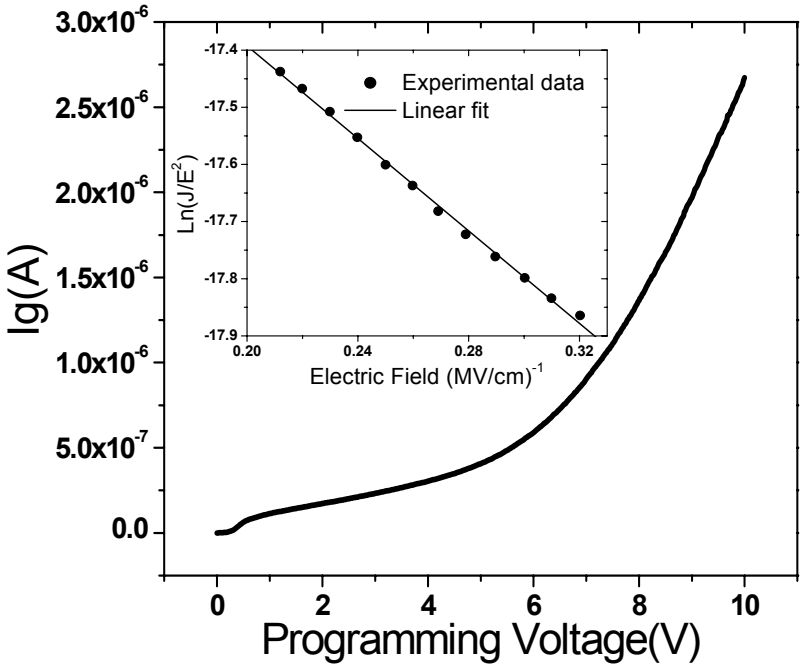


Fig. 2.14 Program Voltage vs. Current. Note that the programming current has a F-N characteristic (insert) once programming voltages exceedes 6.5V.

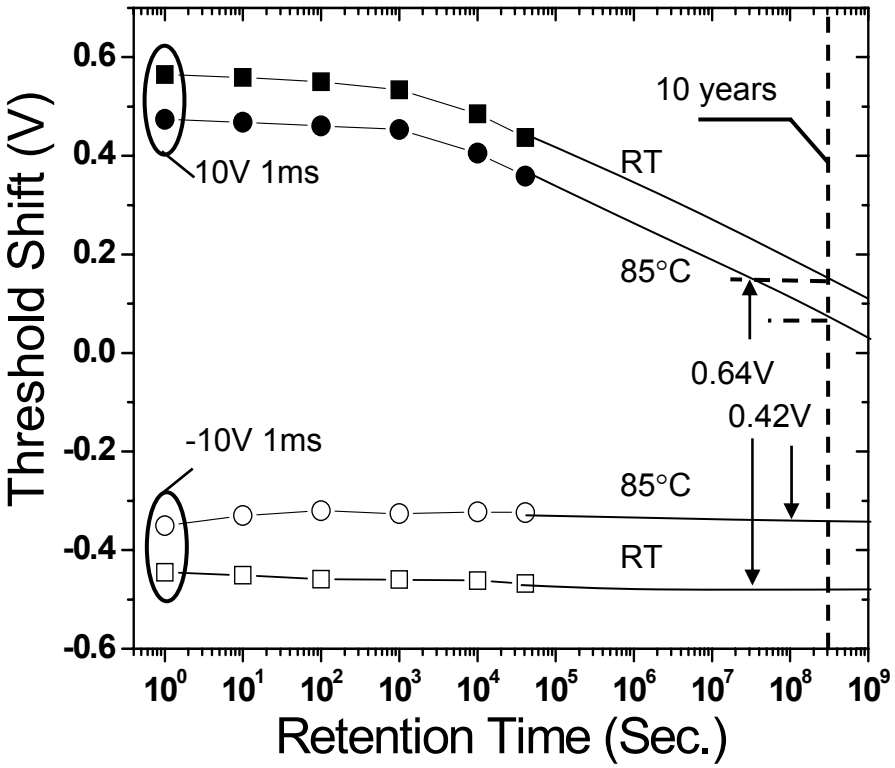


Fig. 2.15 MHTHS data retention characteristics at both room temperature (RT) and 85°C. Devices first have slow degradation and beyond 1000s the degradation rate becomes faster. At 10-year life time, the memory window is 0.64V and 0.42V for the RT and 85°C respectively.

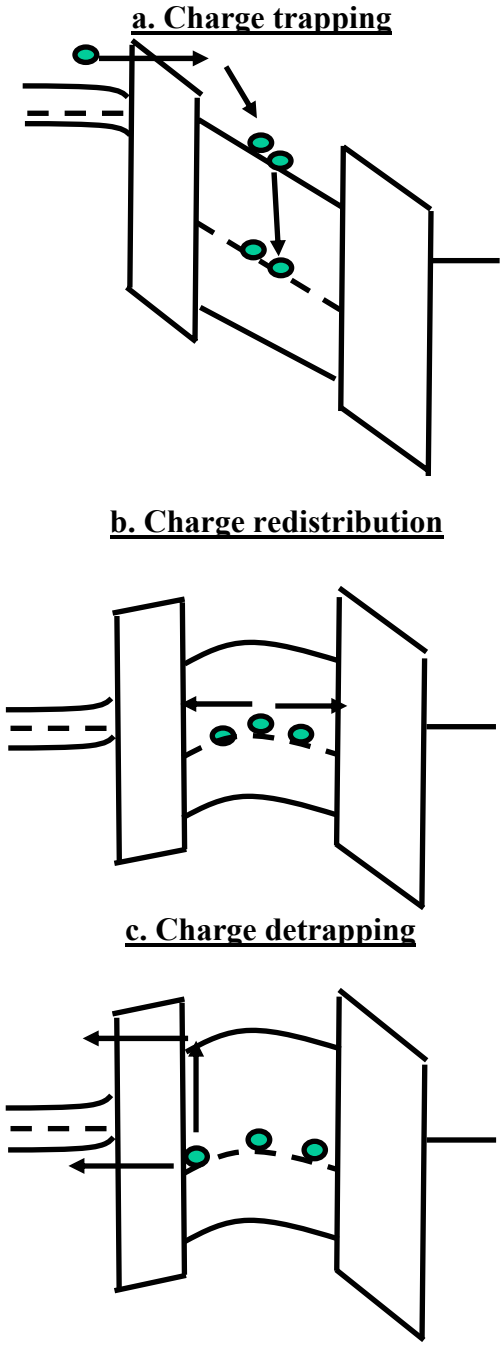


Fig. 2.16 Schematic illustration of the retention degradation stages a) charge trapping, b) charge redistribution and c) charge detrapping [12].

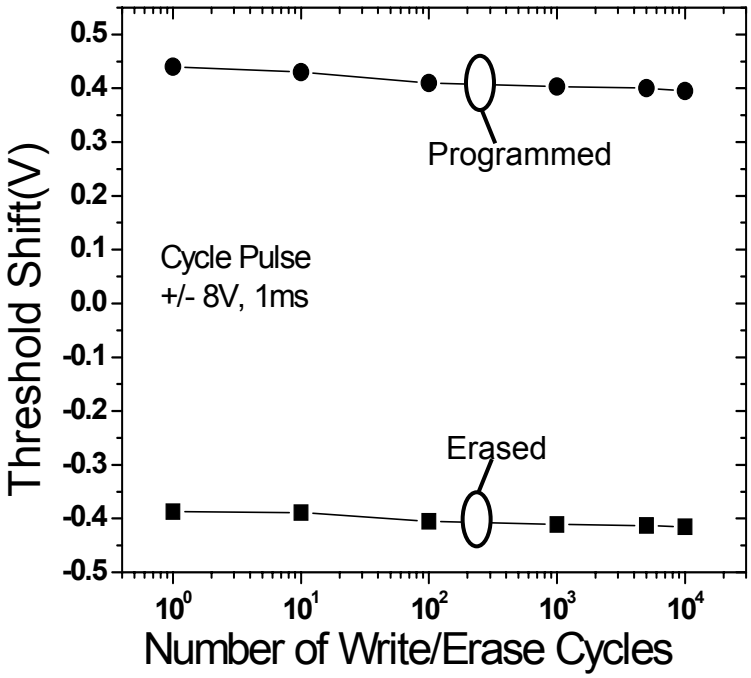


Fig. 2.17 MHTHS write/erase endurance. This data shows the MHTHS devices have negligible degradation under ±8V, 1ms programming up to 10000 cycles.

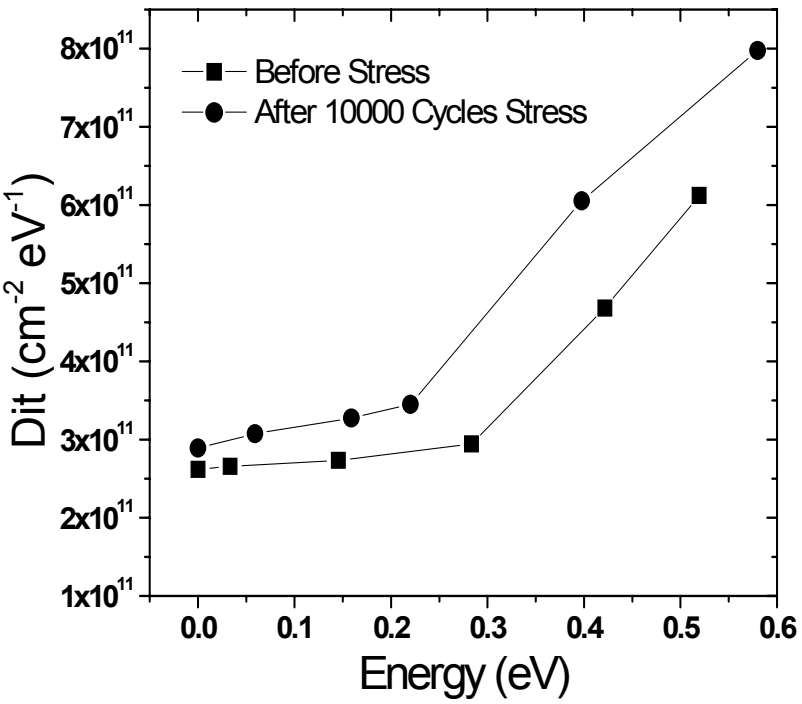


Fig. 2.18 Interface states densities for the MHTHS devices before and after the stress show that only small amounts of interface states are generated during write/erase cycling.

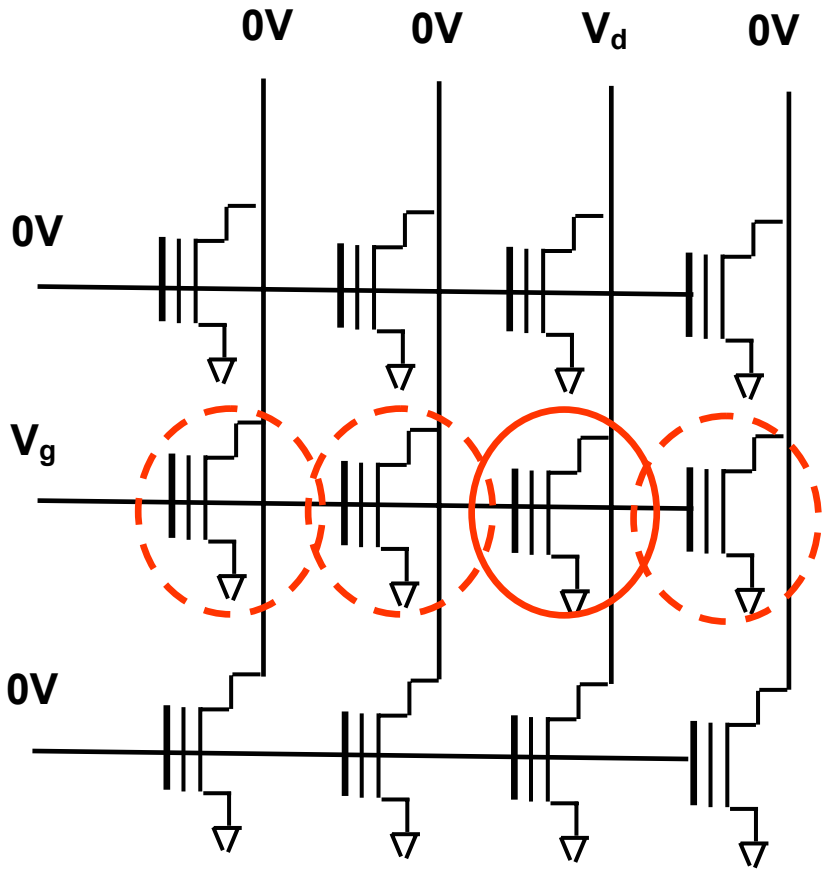


Fig. 2.19 Read disturb configuration in a memory array. The solid circled cell is selected reading causing the dash line circled cells on the same word line to be read disturbed by the small gate bias applied during read.

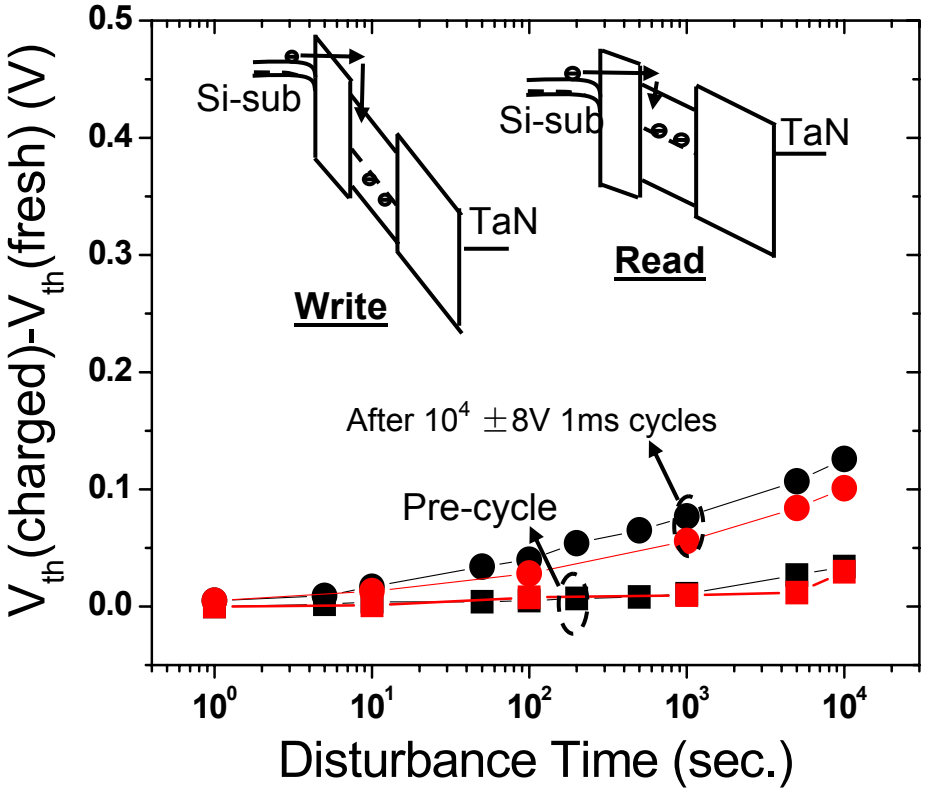


Fig. 2.20 MHTHS threshold shift at 1.5V gate disturb bias. Fresh MHTHS device show small changes while only 0.1V shift is found even when device has been stressed by ±8V, 10000 cycles.

W(μm)	L(μm)	Effective W(μm)	Area(cm^2)
200	20	877.5703916	0.000275514
100	20	475.5221459	0.000195104
80	20	394.608554	0.000178922
200	10	839.364695	0.000183936
100	10	438.7851958	0.000143879
80	10	358.5136094	0.000135851

Table 2.1 Transistor sizes for the two mask process used for the MHTHS devices.

	Decay Rate	20% charge loss	Write/Erase speed
This Work	50mV/dec	2.6×10^4s	1μs
Ref [9]	400mV/dec	N/A	10μs
Ref [10]	200mV/dec	7×10^4s	20μs
Ref [12]	500mV/dec	5×10^3s	100μs
Ref [13]	150mV/dec	10^3s	2.5ms

Table 2.2 Comparisons between MHTHS and SONOS devices, showing the improved programming and retention characteristics of MHTHS devices.

Chapter 3 Novel MATHS Nonvolatile Memory

3.1 Introduction

In this chapter, a novel high-K SONOS type memory using a TaN-Al_2O_3-Ta_2O_5-HfO_2-Si (MATHS) stack structure will be demonstrated. Compared to the MHTHS device discussed in the last chapter, this new structure can provide better charge blocking efficiency by replacing the top HfO_2 blocking layer with an Al_2O_3 blocking layer, while the advantages of faster programming speed and longer retention time of high-K SONOS memory can be preserved.

As discussed in Chapter 2, one major problem for the MHTHS device is that the memory window is not large enough for a practical memory application. To solve this problem, band engineering analysis will be introduced to analyze the origin of this problem and then a solution will be proposed. Several different high-K material choices will be discussed. Next, calculation results for choosing the right Al_2O_3 thickness to compare with the equivalent HfO_2 blocking layer will be presented.

A stack with this MATHS device structure will be fabricated to the calculated dimensions. Al_2O_3 is deposited with a reactive sputtering method, while the HfO_2 and Ta_2O_5 still use the same process as shown in the last chapter.

The electrical data for the fabricated Al_2O_3 will then be illustrated together with the fabricated transistor basic characteristics. The memory characteristics: the memory window, the programming transient, the data retention, the data endurance, and the read disturbance will then be compared with equivalent MHTHS devices. The fabricated MATHS devices show greatly improved memory window due to better charge blocking efficiency. The Write speed is improved significantly and excellent retention is also achieved.

Finally the major advantages of these novel MATHS devices will be summarized.

3.2 Theoretical Analysis

3.2.1 Band engineering analysis

As was discussed in Chapter 2, the 1.5eV low electron barrier of the MHTHS tunneling HfO_2 is desirable for improving the charge injection as compared to the 3.2eV high electron barrier of the SiO_2 tunneling layer. Because the HfO_2 tunneling layer is physically thicker, and because of the Ta_2O_5 deep trap level, the direct back tunneling current through the HfO_2 tunneling layer is suppressed as compared to the SiO_2 tunneling layer at the same EOT, hence a better trade-off for longer retention and faster programming.

HfO_2 is not energetically favorable as the top blocking oxide as shown in Fig. 3.1. Because the electric fields across the top and the bottom HfO_2 layers are about the same during programming, the F-N tunneling through the top HfO_2 layer is in competition with that of lower barrier. Therefore, there is a high probability for injected charges to escape through the top HfO_2 layer, rather than being trapped in the Ta_2O_5 charge trapping layer. To solve this problem, a gate dielectric which forms a higher charge blocking barrier will be ideal for this purpose. The band offsets of various gate dielectrics relative to the Si band are shown in Fig. 3.2 [1]. It is seen that only SiO_2, Si_3N_4 and Al_2O_3 have higher band offsets than HfO_2 for electrons. However, it should be noted a high-K material is preferred for the top blocking layer because a larger portion of the applied programming voltage will be dropped onto the top layer if a lower K material is used for the bottom high-K material, hence

increasing the programming voltage for the same injection currents. Therefore, SiO_2 can be excluded. Comparing Si_3N_4 and Al_2O_3, the hole barrier for the Si_3N_4 is even lower than that of HfO_2. As a result, Al_2O_3 is the right choice for the top blocking layer.

The energy band diagrams at Write and Erase modes for MATHS and MHTHS devices are compared in Fig. 3.3 to show the advantages of using Al_2O_3 to replace HfO_2 as the top oxide. All band offset data are from published literature [1]. For the top layer, both Al_2O_3 and HfO_2 are drawn in the same figure. The top blocking barrier is increased from 1.2eV to 2.5eV for HfO_2 and Al_2O_3 top blocking layer respectively. Since F-N tunneling is exponentially proportional to the barrier height, the top electron leakage currents can be significantly reduced by using a proper thickness of Al_2O_3 to replace HfO_2 (Fig. 3.3a). The same argument is also true for holes in the Erase mode as shown in Fig. 3.3b, where the top barrier is increased from 0.4eV to 1.9eV. One additional advantage in the Erase mode is that unwanted backward gate electron injection is suppressed due to the larger gate electron injection barrier of Al_2O_3, which is (2.8eV vs. 1.5eV for HfO_2).

3.2.2 Calculation of the top Al_2O_3 thickness

Since Al_2O_3 has a smaller dielectric constant than HfO_2 and Ta_2O_5, it may share a larger portion of the applied programming voltage, which results in a reduced bottom injection current. Therefore, the top Al_2O_3 thickness must be carefully chosen so that bottom injection won't be sacrificed while reducing the top leakage. For this purpose, a calculation is done to compare the top oxide leakage and the bottom oxide injection currents in stacks of different Al_2O_3 layer thickness with a 100Å HfO_2 top oxide stack. The results are shown in Fig. 3.4 and Fig. 3.5 for top leakage and bottom injection currents respectively. The current is calculated using conventional F-N and direct tunneling (D-T) theory [2]. The tunneling HfO_2 and trapping Ta_2O_5 thicknesses are fixed at 48Å and 64Å respectively. The effective electron mass is taken from [3] and the dielectric constants used are 10 and 19.5 for Al_2O_3 and HfO_2 respectively, measured from the fabricated films.

As shown in Fig. 3.4, using a 100Å HfO_2 blocking oxide, an Al_2O_3 layer thicker than 40Å can reduce the top leakage current by more than one order of magnitude. Fig. 3.5 shows the 40Å Al_2O_3 layer can also induce a larger injection current. Therefore, replacing 100Å HfO_2 with 40Å Al_2O_3 for the top layer could drastically increase the charge trapping efficiency while improving the programming speed. The memory window can therefore be increased while maintaining the unique features of high-K SONOS memory for faster programming and the longer retention. At low programming voltages, the electric field is not large for F-N tunneling and it

is direct tunneling that dominates within this region. The kinks at low voltages in both figures are where D-T currents dominate over F-N tunneling currents. The proposed MATHS structure is illustrated together with SONOS and MHTHS devices in Fig. 3.6, showing the actual device thickness for comparison.

For hole erase currents, no calculation result is available since the hole effective mass is not known for the HfO_2 and because the tunneling mechanism is prohibitively complex. For instance, the known erasing mechanism is direct hole tunneling for conventional SONOS devices. But enhanced band to trap tunneling may exist as we have discussed in the last chapter, which significantly improve the erasing speed. The calculation of such currents is beyond the scope of this project.

3.3 Device fabrication

3.3.1 Al_2O_3 deposition

High quality Al_2O_3 has been extensively studied in the literature. Various methods have been reported for Al_2O_3 deposition [4;5] and it has been used in the SONOS memory structure [6-8]. In this work the reactive DC sputtering method is used for Al_2O_3 deposition.

The back pressure for Al_2O_3 sputtering is 5E-7Torr. Since the Al deposition rate is very fast, the current control mode is used for low power to control the thin Al_2O_3 deposition. Before film deposition, a 300W, 5min pre-sputtering was done to clean the Al target surface of any oxidized Al. Failure to clean the target may result in an Al_2O_3 deposition rate which is inconsistant due to the reduced sputtering rate of the Al_2O_3 layer. The current used is 0.35A and the corresponding power is 110W with a DC bias of 325V. The gas setting for Ar is 20% and for O_2 is 0.5%. The reaction pressure during the sputtering is 10mTorr. After sputtering, the sample is immediately transferred to an oxidation chamber for annealing at 400°C for 5 minutes in a N_2 ambient with small traces of O present. This oxidation temperature is critical since the Al diffusivity will become much larger at higher temperature and the stack will become very leaky. After oxidation, the Al_2O_3 is annealed in a RTP chamber at 700°C for 2 minutes. The deposition rate for this Al_2O_3 is 36Å/min, which is measured by ellipsometer.

3.3.2 Whole process flow

NMOS transistors using the two masks process discussed in the last chapter were formed in the MATHS configuration. The HfO_2 and Ta_2O_5 are deposited using the same process discussed in Chapter 2 and controlled to be the same thickness as the MHTHS devices for comparison. After Ta_2O_5 deposition the Al_2O_3 is directly deposited onto the Ta_2O_5 layer using the process discussed in the last section. A 2000Å TaN gate is used for the top electrode. The Al_2O_3 layer is etched with the CF_4 RIE dry etch. For the source/drain activation, a 700°C, 2mins annealing is used.

3.4 Basic electrical data

In Fig. 3.7, a typical Al_2O_3 C-V curve is shown. The device is first stressed by a ±6V, 1ms stress at the start of forward and reverse sweeping. There is negligible hysteresis, indicating this is a high quality trap free film. The dielectric constant derived from the C-V curve is about 10. The leakage currents at 1V beyond the flat-band voltages for different EOTs are shown in Fig. 3.8. Compared to SiO_2, Al_2O_3 can significantly reduce the leakage currents. Well behaved Ids-Vds transistor curves are shown in Fig. 3.9.

3.5 Memory characteristics

3.5.1 Memory window

Transistor C-Vs of MATHS and MHTHS are compared with HfO_2 and Al_2O_3 only stacks in Fig. 3.10. Under ±6V, 1ms stress, the MATHS device shows nearly two times larger hysteresis window than that of the MHTHS device, while stacks with only HfO_2 and Al_2O_3 show no hysteresis. The EOTs extracted from C-V measurements are 41.9Å and 37.5Å for MHTHS and MATHS devices respectively with a tunneling oxide of only 9.5Å EOT, the thinnest so far for a SONOS memory to our knowledge. The Ids-Vgs memory windows after ±8V, 1ms programming for the MATHS and MHTHS devices are also compared in Fig. 3.11. Note that MATHS devices show two times larger memory window as compared to MHTHS devices. These greatly improved memory windows demonstrate that more charges are trapped in the MATHS devices than the MHTHS devices as been predicted in the previous section.

3.5.2 Programming transient

The MATHS programming transients for the write and erase modes are shown in Fig. 3.12. The memory window starts to open as 10ns at Write and less than 1μs at Erase when programming voltage is larger than 8V. For comparison, the programming speeds of state-of-the-art SONOS type devices when memory windows open at 0.5V are shown in Table. 3.1 [9-13]. These high-K MATHS and MHTHS devices show faster speed at the same programming voltage. Improved charge trapping by use of Al_2O_3 top layer is shown in Fig. 3.13 in which trapped charge densities as a function of the write time are compared. Though the same Ta_2O_5 trapping layer is used, more charge is trapped in the MATHS device than in the MHTHS device. Another interesting feature is that the MHTHS device shows lower faster saturation. Once memory window starts to open, the memory window doesn't increase much even as the programming voltage increases from 8V to 10V. This is mainly due to the quicker balance between the bottom injection and the top leakage as discussed in Fig. 3.1. But for the MATHS device, there is no such write saturation within the measurement time scale and increasing the programming voltage will increase the memory window. If not using the programming voltage but rather the bottom oxide field for comparison, the MATHS devices with E_{tox} of 4.21MV/cm still shows a larger memory window than the MHTHS devices with E_{tox} of 4.72MV/cm, indicating that more electrons are blocked and trapped by the introduction of Al_2O_3 to replace HfO_2 as the top blocking layer.

It should also be noticed that the Write speed is improved from 1μs to 10ns at the MATHS bottom injection fields, another advantage of using Al_2O_3 as the top blocking oxide.

3.5.3 Data Retention

Room temperature data retention for MATHS and MHTHS devices are compared in Fig. 3.14. At 10-year life time the MATHS device has a 1.86V memory window, close to three times improvement over the 0.64V memory window of the MHTHS device. In this same figure, the retention of the MATHS device after a 10^5 ±10V, 1ms cycling is also shown. Though the device degrades faster after stressing, the memory window at 10 years is still close to 1.5V. In Fig. 3.15, the retention at 85°C baking for both devices is shown. Although the memory window shrinks due to the thermally assisted de-trapping, a reasonable 1.4V memory window still exists for MATHS devices, as opposed to MHTHS devices this is less than 0.5V. By using this novel MATHS device the memory window has been greatly improved to meet the 10-year life time requirement. As was shown in the last section, this increased memory window is obtained together with a fast programming.

The worst case decay rates for both devices are compared with the state-of-the-art SONOS type devices shown in Table 3.1. These high-K SONOS memories show much slower decay rate mainly due to its thicker tunneling oxide thickness (48Å vs. ~20Å in other devices) and its deeper Ta_2O_5 trap level. Since different works have different memory windows, a normalized parameter, 20% charge loss is also used for the retention comparison. The MATHS devices show about 27% better retention time than MHTHS devices and this is also comparable with the other SONOS devices. However, it must be noted that such retention is achieved with a

48Å tunnel oxide, which makes it possible for further scaling in this structure. For other SONOS type devices, the bottom layer has already reached to about 20Å, which makes further scaling very difficult.

It should be interesting to note that MATHS and MHTHS demonstrate totally different erased retention behavior. For the MHTHS devices, almost no retention degradation is observed. But for the MATHS devices, the devices start to degrade quickly after 100s. For the MHTHS devices, the excellent erased state retention actually indicates that the device is very close to the equilibrium state. Therefore, this suggests that the erased trap level states are almost aligned with the Fermi level of the top and bottom gate electrode. While for the MATHS devices, the degradation of the erased memory window indicates electrons injection even at zero bias, which suggests that the erased trap levels may be lower than the top and bottom gate electrode Fermi levels. Therefore, the trap levels in these two memory devices actually are different. But considering the same bulk Ta_2O_5 films are used in both devices, the difference in the trap levels are most probably due to the interface traps between the top blocking oxide and the trapping layers.

3.5.4 Data Endurance

The endurance characteristics of MATHS and MHTHS devices under ±10V 1ms stress are shown in Fig. 3.16. Negligible degradation is observed for MHTHS devices but slight degradation is found in MATHS devices at 10^5 write/erase cycles. This difference could be due to the slightly larger bottom oxide field applied on the MATHS devices as shown in Fig. 3.13. It can be seen that the electric fields needed for programming these devices are 3 ~ 5MV/cm due to the much lower HfO_2 electron barrier, which is smaller than that needed for traditional SONOS devices programming. As has been discussed in the previous sections, reduced programming electric field is the main reason for increase data endurance since the interface will not be stressed as hard as in the conventional SONOS devices.

3.5.5 Read disturb

The changes in the erased device threshold voltage due to read disturb for both devices is compared in Fig. 3.17. Without stressing, both devices show less than 50mV threshold shift up to 10^4 seconds. If devices are stressed by a ±8V, 1ms voltage for 10000 cycles, the threshold shift will increase faster but is still less than 150mV at 10^4 seconds. The large threshold shift observed in the MATHS devices doesn't mean it is more vulnerable to read disturbance than the MHTHS device. This could most probably because a larger voltage is applied across the bottom layer if the same read disturb voltage is used as evidenced in Fig. 3.13. And again this read disturb result is comparable with the state of the art SONOS devices.

3.6 Summary

In this chapter, significant advantages of a novel high-K MATHS memory over MHTHS devices are analyzed and presented. By using Al_2O_3 to replace HfO_2 as the top blocking layer, the memory window and the programming speed are greatly improved through the much higher carrier barrier of Al_2O_3 as compared to HfO_2. By carefully choosing the top blocking Al_2O_3 thickness, not only is the memory window improved but also the writing speed becomes faster. Excellent data retention and endurance are also obtained in this device at a less than 10Å EOT tunneling oxide, which indicates that such device is a very promising candidate for flash memory applications beyond the 45nm node.

3.7 References

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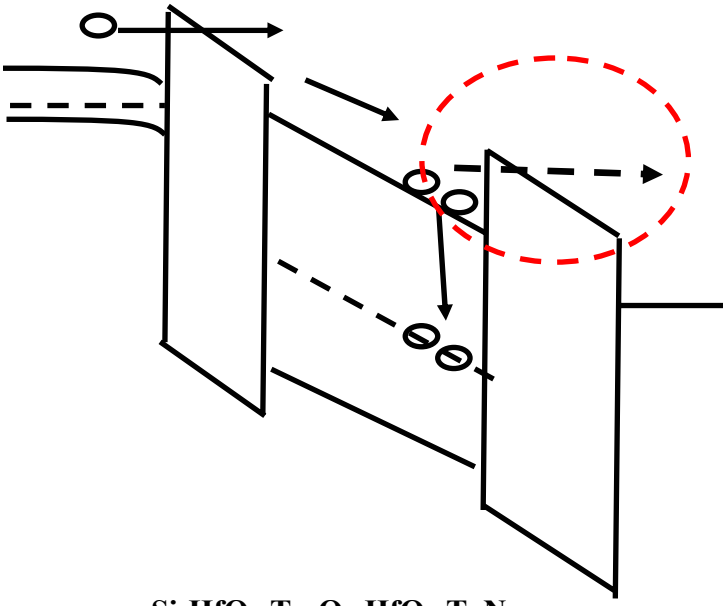


Fig. 3.1 The band diagram of a MHTHS device in Write mode shows both charge trapping and charge escape in competition with each other. Due to the low electron barrier of HfO_2, there is a large probability for injected electrons to escape from the top of the Ta_2O_5 charge trapping layer into the gate electrode.

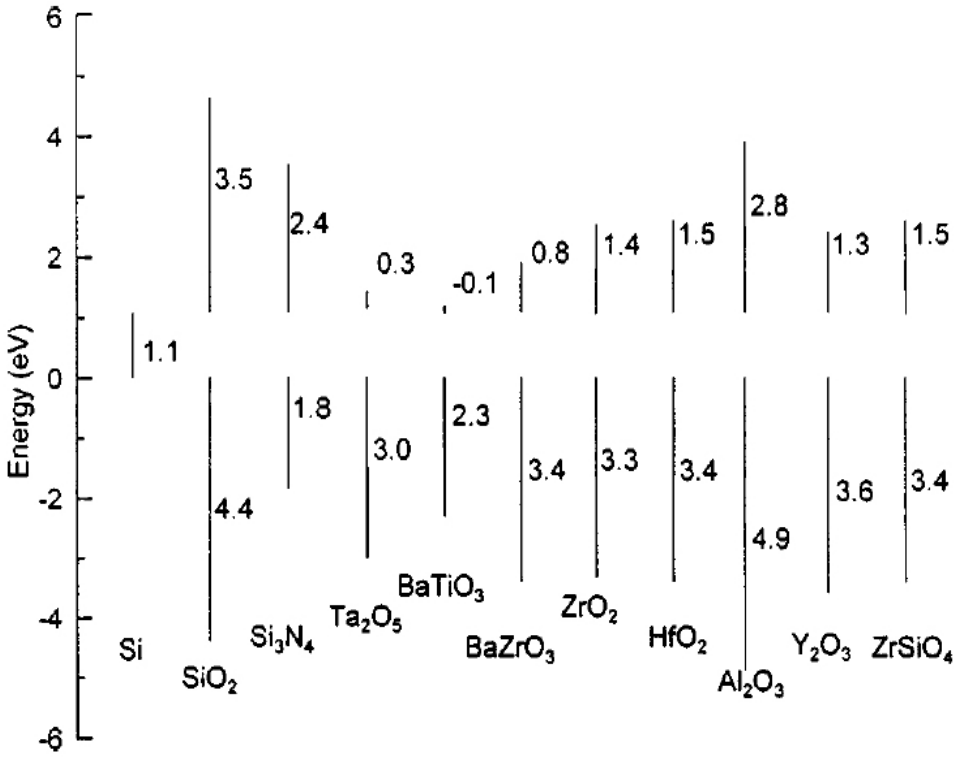


Fig. 3.2 Band offsets of various dielectric materials on Si [1].

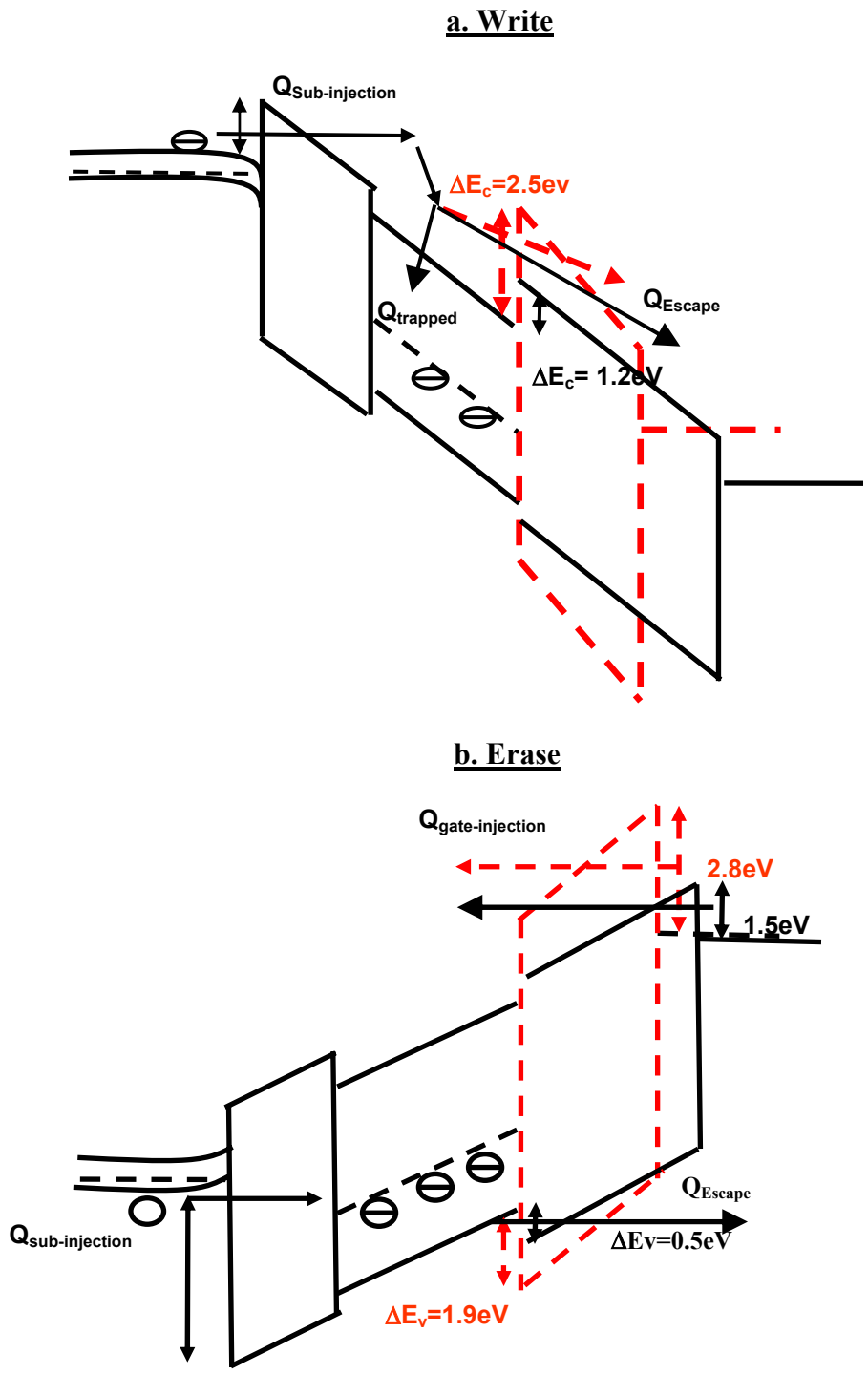


Fig. 3.3 Band diagrams of MATHS (dashed line) and MHTHS (solid line) devices at a) Write and b) Erase modes show the improvement of charge blocking using MATHS.

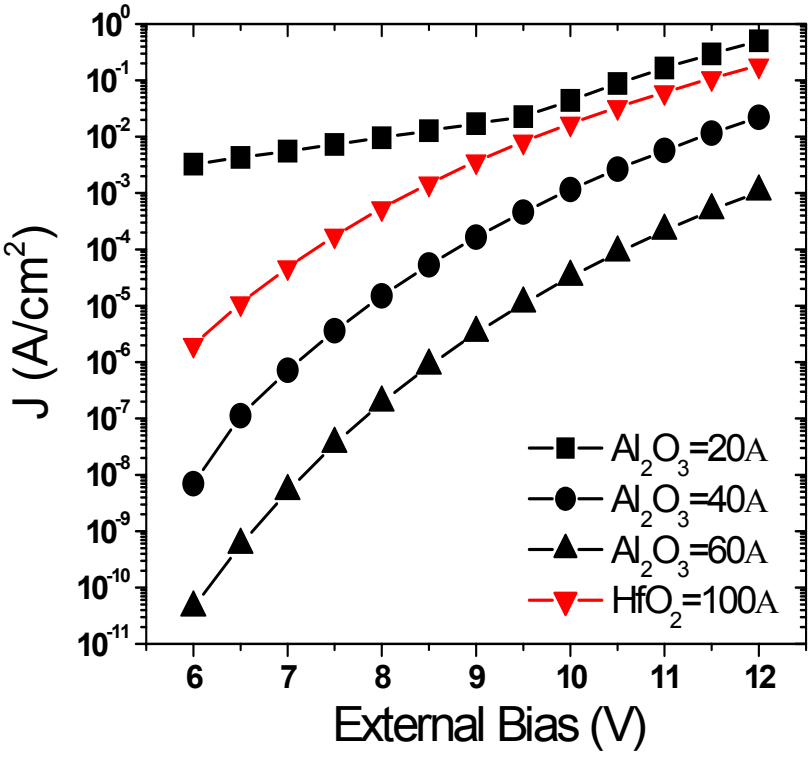


Fig. 3.4 Calculated leakage currents in the top blocking layer for various top Al_2O_3 thicknesses are compared with 100Å HfO_2 top blocking layer. When the Al_2O_3 thickness is larger than 40Å, the leakage current is reduced.

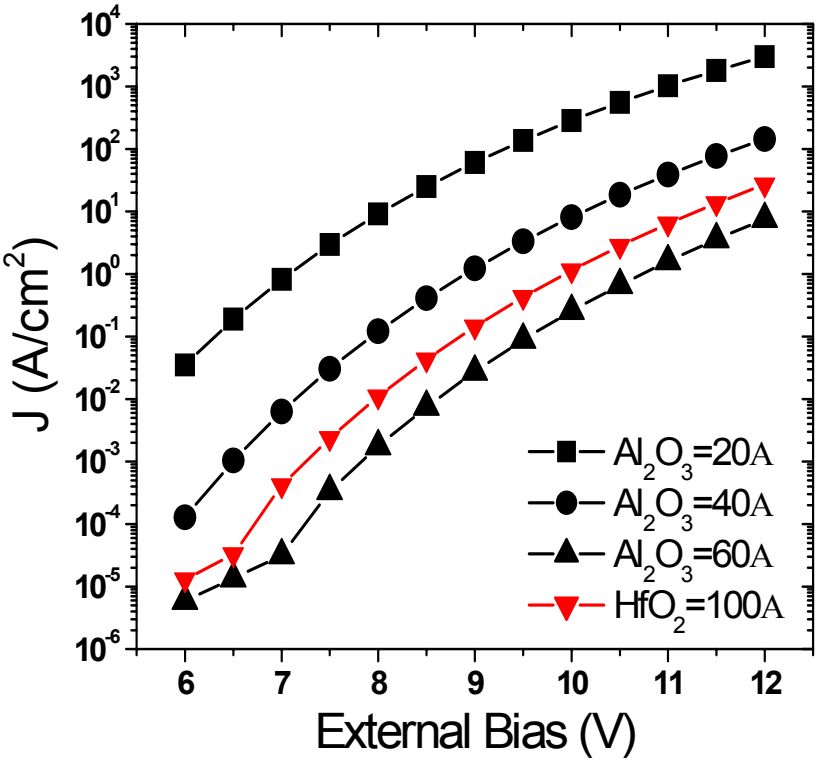


Fig. 3.5 Calculated injection currents in the bottom tunneling layer for various top Al_2O_3 thicknesses are compared with 100Å HfO_2 top blocking layer. When the Al_2O_3 thickness is thinner than 40Å, the injection current is increased.

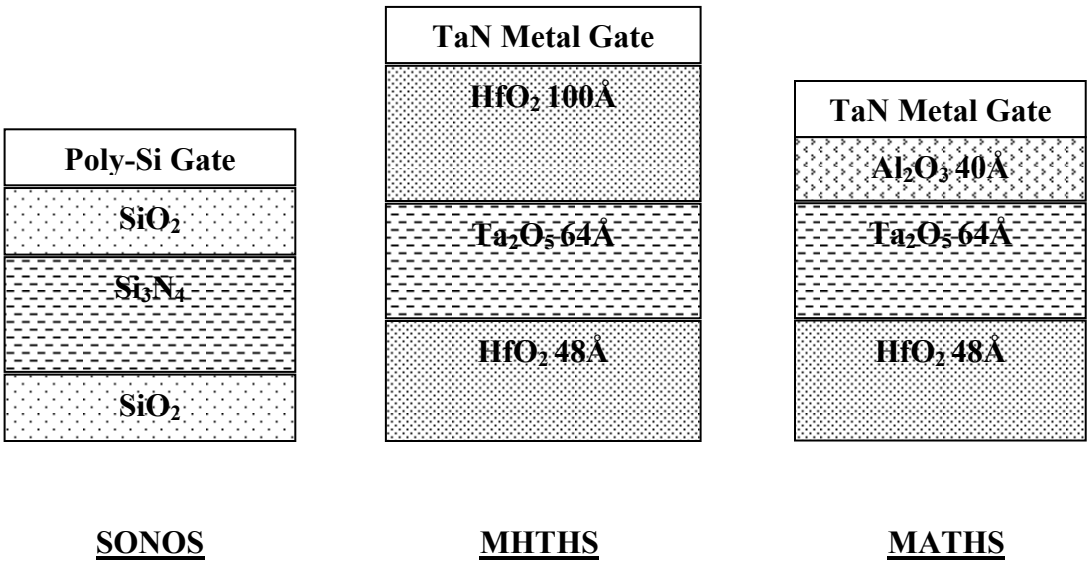


Fig. 3.6 Schematics of SONOS, MHTHS and MATHS device gate stack structures. The numbers labeled in the MHTHS and MATHS devices are the layer thickness used.

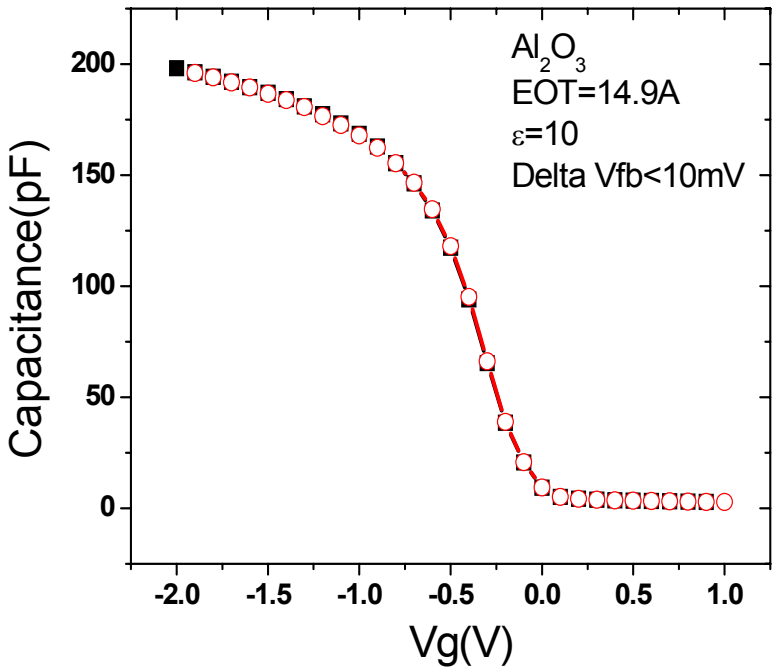


Fig. 3.7 C-V hysteresis of fabricated Al_2O_3 thin film under a ±6V, 1ms stress before each sweeping starts. There is little hysteresis, which indicates few traps exist in this film.

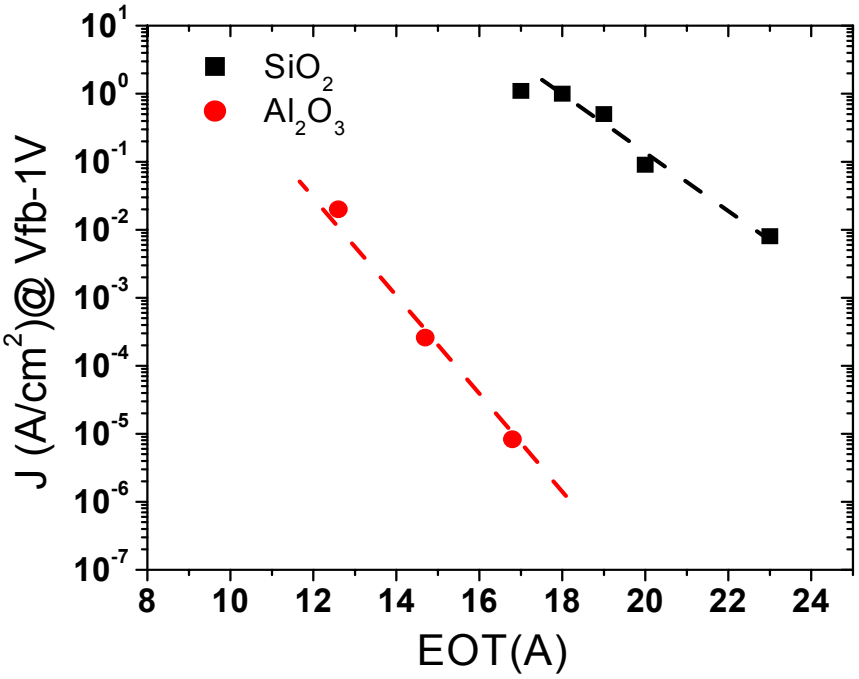


Fig. 3.8 Leakage currents of Al_2O_3 thin film at 1V beyond the flat band voltage vs. the equivalent oxide thickness. As compared to SiO_2, this Al_2O_3 has excellent current reduction.

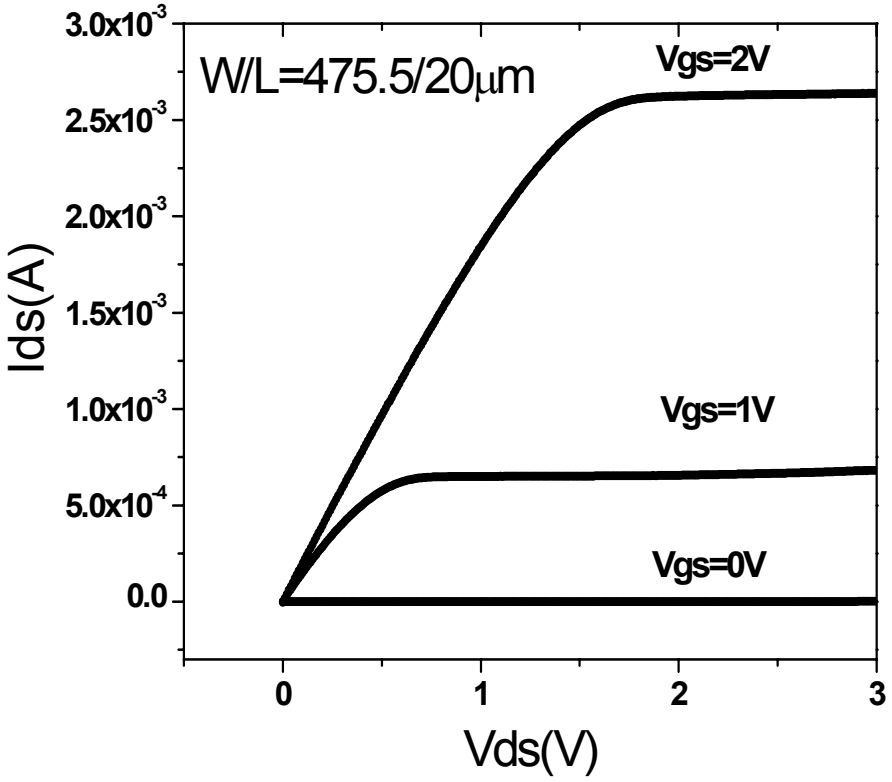


Fig. 3.9 Ids-Vds curves for fabricated MATHS transistor devices.

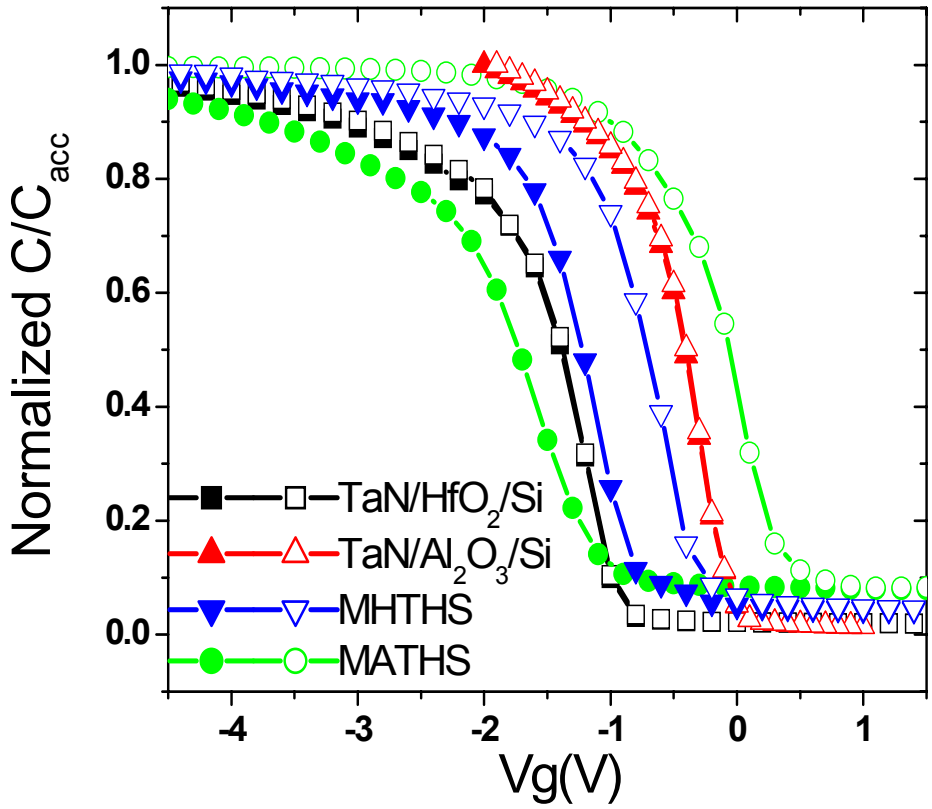


Fig. 3.10 Normalized C-Vs of Al_2O_3 only, HfO_2 only, MHTHS and MATHS gate stacks after programming illustrate the Ta_2O_5 trapping effect. All hysteresis curves are in counter-clock wise direction.

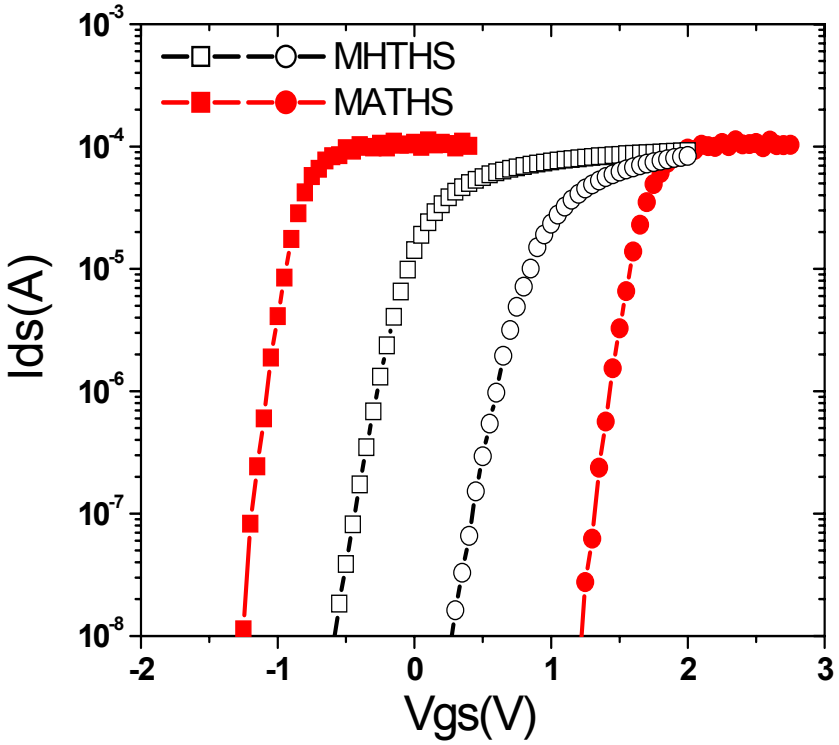
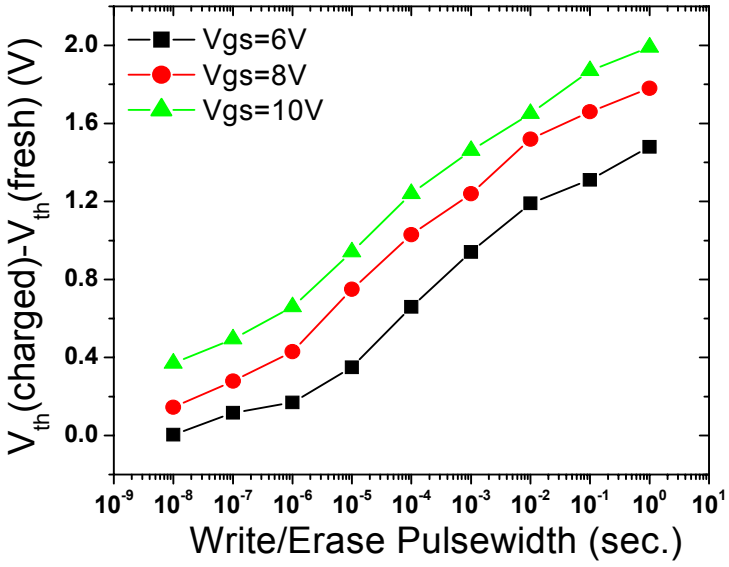
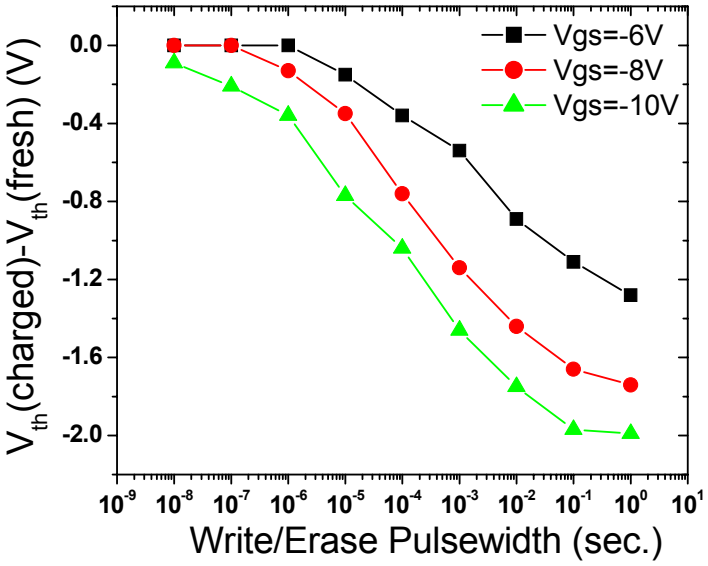


Fig. 3.11 I_{ds}-V_{gs} curves after ±8V, 1ms programming show the MATHS memory has two times larger memory window than the MHTHS devices.



a. Write



b. Erase

Fig. 3.12 MATHS (a) Write and (b) Erase transient curves at different programming voltages show fast write speed from 10ns and erase speed from 100ns to open the memory window.

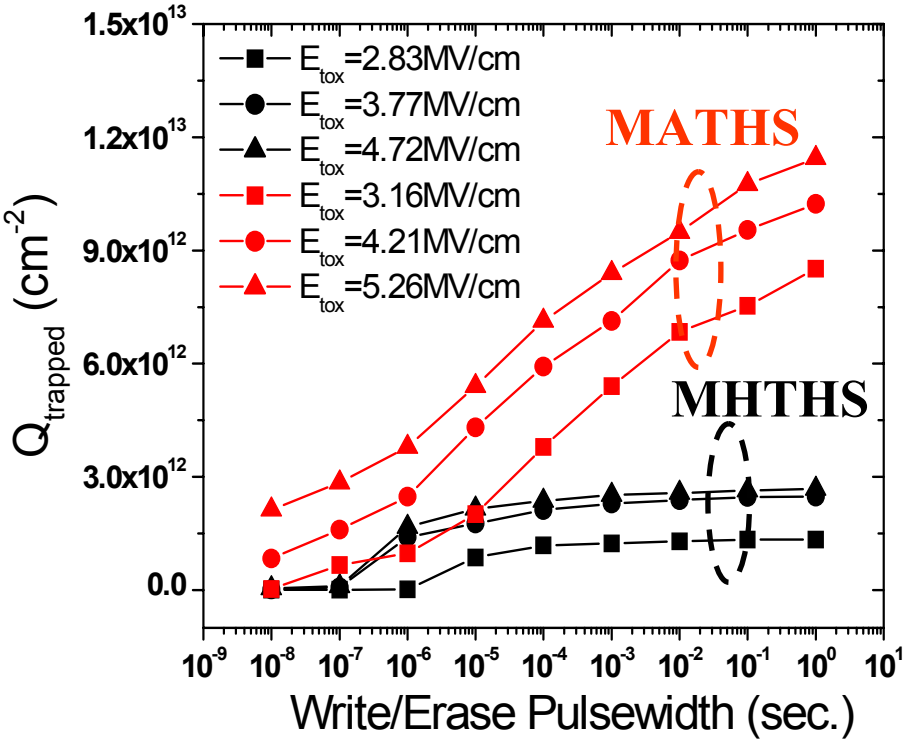


Fig. 3.13 Trapped charge density comparisons at Vgs=6, 8 and 10V for both devices show that MATHS device has much better charge trapping. The electric fields across the tunneling oxides at these programming voltages are also illustrated.

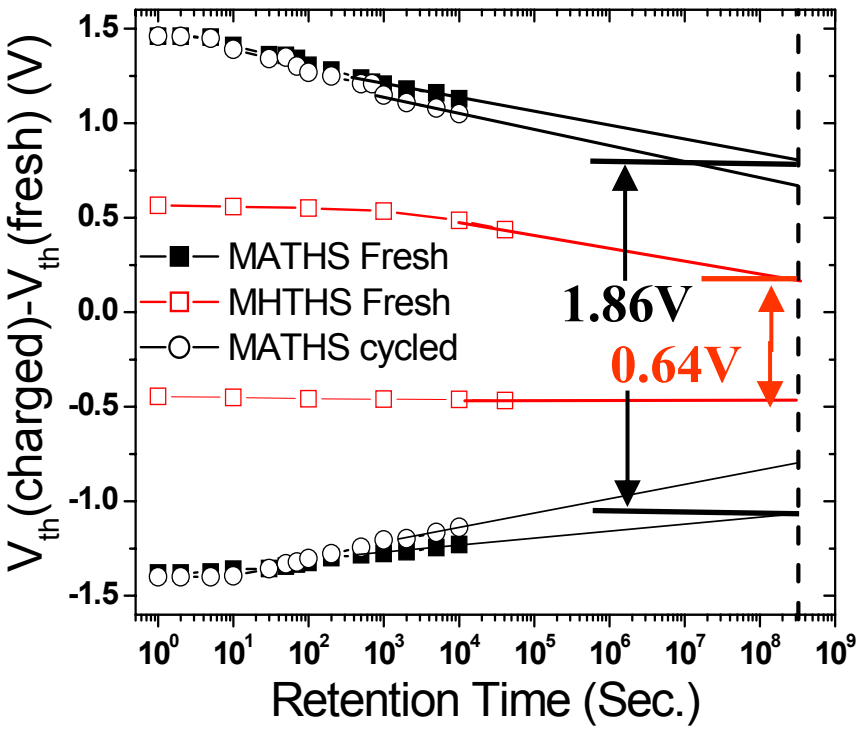


Fig. 3.14 Data retention comparison between MATHS and MHTHS at RT when both devices are programmed at ±10V,1ms. The MATHS device shows close to three times improvement at 10-year lifetime as compared to the MHTHS device. The 10^5 cycled MATHS data retention curve is also shown.

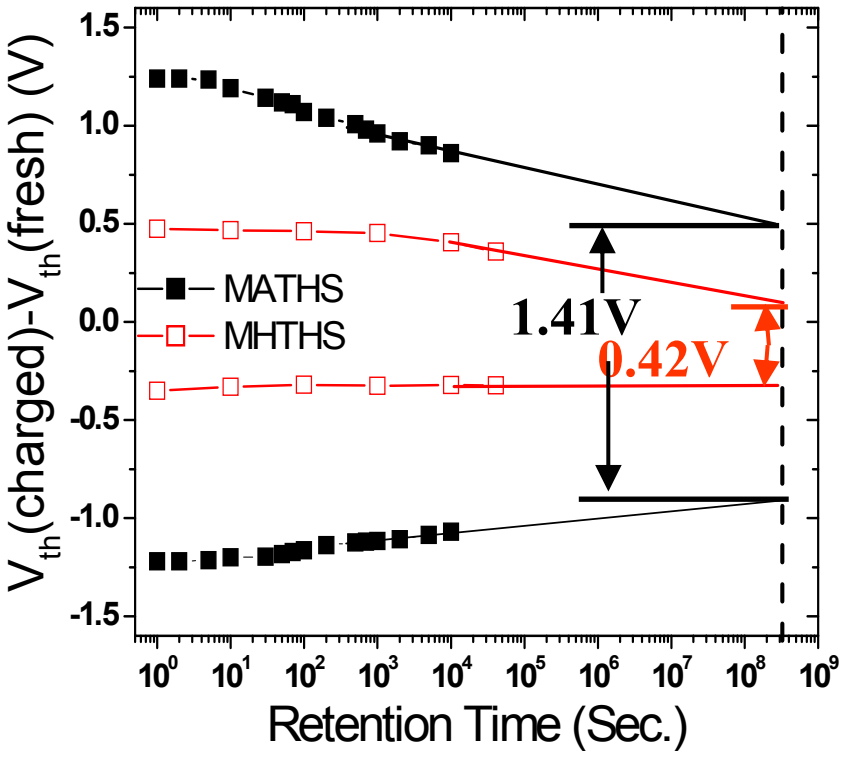


Fig. 3.15 85°C bake data retention comparison between MATHS and MHTHS when both devices are programmed at ±10V, 1ms. At 10-year lifetime larger than 1V memory window has been achieved.

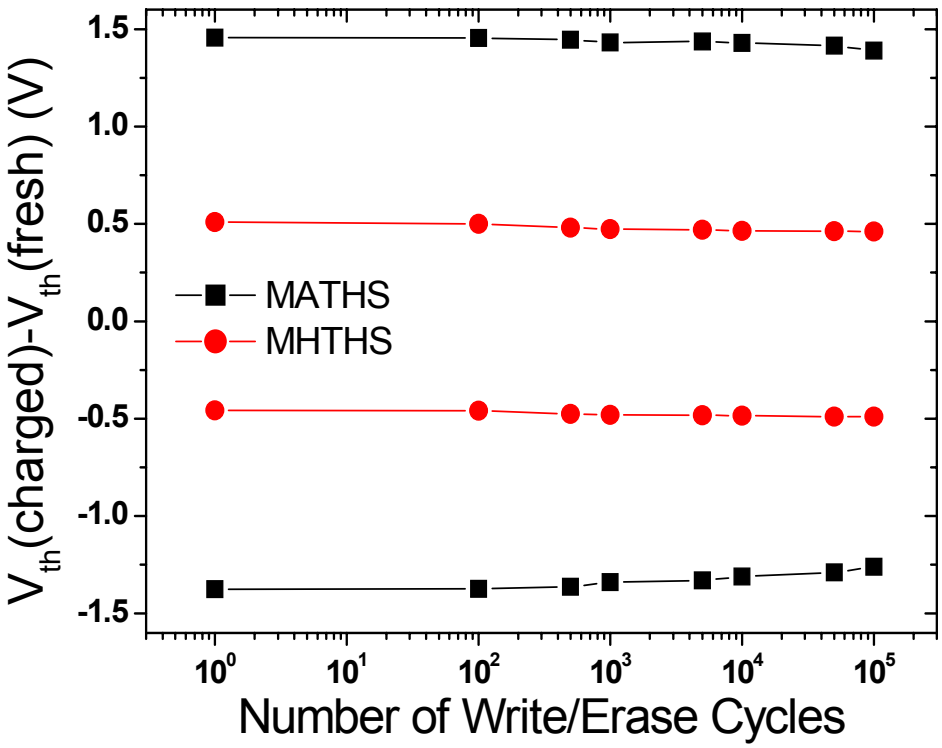


Fig. 3.16 Write/Erase endurance data show both devices can be programmed up to 10^5 cycles without much degradation.

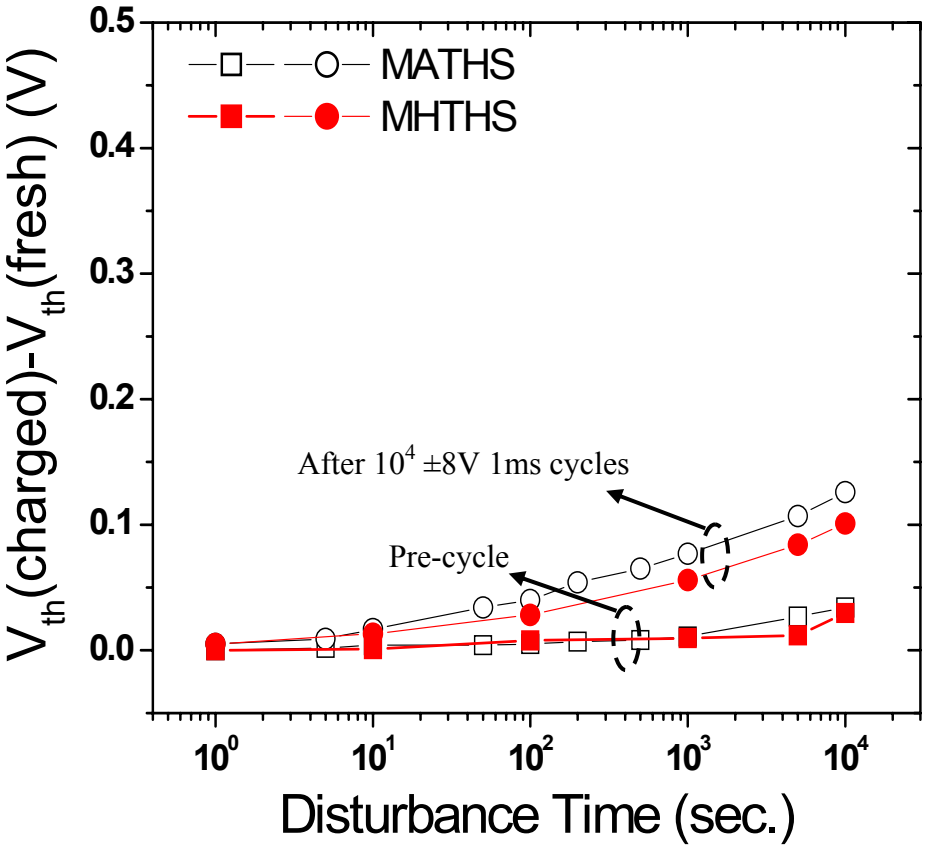


Fig. 3.17 Read disturb curves for MATHS and MHTHS devices before and after cycling stress show small disturbance up to 10^4s.

	Structure	Speed (ΔVth>0.5V)	Decay rate (mv/dec.)	20% charge loss (s)	Tunnel oxide EOT
This work	$HfO_2/Ta_2O_5/Al_2O_3$	100ns@10V	75	3.3×10^4	9.5Å
MHTHS	$HfO_2/Ta_2O_5/HfO_2$	1μs@10V	50	2.6×10^4	9.5Å
2004 IEDM	SiO_2/SiNC/SiO_2/SiN/ SiO_2	< 10μs@10V	250	3×10^2	10Å+20ÅSiNC+10Å
2004 IEDM	FinFET SONOS	1μs@10V	187.5	3.5×10^4	23Å
2004 IEDM	SiO_2/HfAlO/SiO_2	200μs@6V	118	3×10^4	26Å
2003 Enro SSDRC	$SiO_2/SiN/Al_2O_3$	n/a	233	7×10^5	23Å

Table. 3.1 Speed and retention comparison of MATHS, MHTHS and state-of-the-art SONOS devices. (NC: nano-crystal)

Chapter 4 Vth Instability in HfO2 NMOS: Gate Electrodes and Interface Treatments Effects

4.1 Introduction

In previous chapters, novel SONOS type memories using high-K dielectrics have been demonstrated. It is clear that the high quality HfO_2 tunneling oxide is one of the keys for the successful integration of this new device. As was discussed in the first chapter, significant progress has been achieved by both academic and industry to make high quality HfO_2 thin films. But there are still several issues needed to be solved before HfO_2's integration to replace SiO_2 in the semiconductor industry. Among these, the threshold V_{th} instability is one of the major concerns. An understanding of the V_{th} instability is very important, especially for the logic circuits applications for the following reasons: 1. The HfO_2 material is targeted for EOT less than 10Å, where the electric field is large and a large charge injection may exist; 2. Large amounts of intrinsic traps exist inside the HfO_2 films [1] as compared to SiO_2, which is almost trap free; 3. Vdd will approach 1V at the time when HfO_2 needs to be introduced. The reduced noise margin will require a higher standard on the tolerance of the V_{th} shift. This knowledge is also very important for improving high-K SONOS memories proposed in previous chapters. Because of charge trapping inside the HfO_2, the tunneling layer may introduce data retention degradation by trap

assisted back tunneling [2]. Therefore, a HfO_2 V_{th} instability study will be very important for both logic and memory applications.

In Table 4.1 a brief comparison between HfO_2 and SiO_2 V_{th} instability behaviors are illustrated. The most important difference between HfO_2 and SiO_2 is the origin of the V_{th} instability. For SiO_2 the fabricated film is almost trap free and it is the stress electric field that introduces either the interface traps N_{it} or the bulk traps N_{ot}. But for HfO_2 there are intrinsic traps existing before the device is stressed. Also for the SiO_2, Gm degradation rather than V_{th} instability is normally the dominant lifetime limitation factor. While for HfO_2 the V_{th} instability is a more serious concern [3;4].

The V_{th} shift is normally measured by interrupting a DC stress and measuring the Id-Vg curves of the transistor devices. However, it has been reported that both fast and slow traps components existing in the HfO_2 stacks [1]. As a result the conventional Id-Vg measurement is not fast enough to capture all the traps since fast traps will detrap during measurement and the V_{th} instability may be underestimated. Therefore, a fast pulsed Id-Vg measurement may be needed for the V_{th} measurement. Recently, the physics nature of such HfO_2 fast and slow traps have been studied using this fast measurement and a negative U trap model has been proposed [5].

Besides the DC stress measurement, dynamic AC stress measurement has received considerable interest recently [5-8]. The stress set-up for such dynamic stress is shown in Fig. 4.1. During the stress, the source and the substrate are grounded. Two exactly inverted pulse chains are applied to the gate and the drain

respectively. This configuration simulates transistor operation in an inverter, i.e, when the gate is high, the drain is low and vice versa. By using such dynamic circuits, both charge trapping and detrapping can be evaluated and the extrapolated device lifetime is more precise.

In this chapter, the impact of top gate electrodes and bottom interface treatment techniques on the NMOS HfO_2 will be studied. For the gate electrode, the poly-Si gate and the TiN metal gate will be compared. Two popular interface treatment techniques: NH_3 and O_3 treatment will be compared for the interface treatments. Both DC and dynamic stress will be used to characterize devices. In this work, only slow traps performances are compared as the measurement set-up resolution is limited to larger than 100ms.

4.2 Device fabrication

N-MOSFETs with different interface treatments and gate electrodes were fabricated using the conventional CMOS flow. After pre-cleaning, the Si surface was thermally treated in NH_3 and O_3, followed by 30Å ALD HfO_2 deposition. All stacks were subjected to a 600°C, 60s post deposition annealing (PDA) in N_2 prior to gate deposition The poly-Si gate electrode was deposited over the HfO_2 layer. For the TiN electrode, 100Å of TiN was deposited using CVD, followed by a RPCVD poly-silicon layer. Source/drain activation was done at 1000°C for all samples. The transistors were fabricated in the SEMATECH facility and the transistor samples discussed in the following sections are all W/L=20/0.13μm devices if not otherwise specified.

4.3 Basic electrical data

4.3.1 The C-V and the I-V data

The experimental and simulated C-V curves are shown in Fig. 4.2 and Fig. 4.3 for NH_3 and O_3 treated samples respectively. EOTs are extracted from these C-Vs taking into account of the quantum-mechanical effect [9]. All the experimental curves show excellent fit to the simulation curves, indicating excellent interface state densities exist in all stacks.

The Jg-Vg curves are shown in Fig. 4.4 and Fig. 4.5 for the NH_3 and O_3 treated samples respectively. The leakage currents at 1V beyond the flat-band voltage are comparable with the state-of-the-art HfO_2 devices [10]. The electron mobility at 1MV/cm is measured with standard split C-V method. The flat-band voltages are also obtained from the C-V measurements. The threshold voltages are read at an Ids current equal to 1E-6A. All these data are summarized in Table 4.2. A computer controlled system is used to coordinate the stress and the V_{th} measurement so that the V_{th} evolution as a function of time during stressing will be recorded automatically.

4.3.2 V_{th} shift and sub-threshold slope degradation

The transistor Id-Vg curves have different behaviors if different polarity stresses are applied. If a positive gate to substrate bias is applied, the curve will shift to the positive bias region as shown in Fig. 4.6, suggesting electron trapping. It should also be noted that the sub-threshold slope has negligible change, an indication of negligable interface state generation during stressing. The charged electrons can be discharged by using a reverse bias also shown in Fig. 4.6. A smaller reverse bias and a shorter bias period can totally recover the device to its original threshold. Therefore, the trapped charges can be easily de-trapped in these HfO_2 films and it is important to include both the charge trapping and the charge de-trapping effect for a correct evaluation of the device lifetime as discussed before.

If a negative gate to substrate bias is applied, the transistor threshold will shift to the negative direction, indicating hole trapping as shown in Fig. 4.7. Another important feature is that the sub-threshold slope (SS) increases, suggesting new interface state generation. This is very similar to what has been known in the SiO_2 NBTI failure, where hole injection will lead to the interfaces generation and device threshold shift.

Fig. 4.6 and 4.7 are from the TiN gate and NH_3 treated samples only. But the other samples also exhibit similar performances.

4.4 Interface treatment effects

4.4.1 DC stress results

Transistor Id-Vg curves are measured for ΔV_{th} during a positive constant voltage stress (CVS) at different stressing times. In order to minimize the fast unstable charge de-trapping effect, care has been taken to ensure the Id-Vg measurement time between two consecutive stresses is minimized to about 100ms. Stress time as long as 4000s has been used and the data show a linear correlation between ΔV_{th} and log*t* (Fig.4.8). This has been attributed to electrons trapping in bulk traps uniformly distributed inside the high-k layer [4]. V_{th} shifts under different biases for samples with different interfaces are compared in Fig. 4.9. TiN gated samples are shown in Fig. 4.9a and the poly-Si gated samples are shown in Fig. 4.9b. It is clear that for the same stress voltage the O_3 treated samples always show larger ΔV_{th} than the NH_3 treated samples, regardless of the gate electrode used. The dashed lines in Fig. 4.9 represent linear extrapolations to obtain the time-to-failure where 50mV ΔV_{th} is used as the failure criterion. Operating voltages at 10-year lifetime are obtained from Fig. 4.10. Gm degradations are also compared but are found not as severe as the V_{th} shift to limit the device lifetime. This is understandable since the SS during stressing shows little change as shown in Fig. 4.11, indicating few interface states generation, while Gm degradation is normally correlated to poor interface states.

4.4.2 The valance band electron injection model

Enhanced electron trapping observed in O_3 treated samples can be explained by an enhanced valance band electron injection model, as shown in Fig. 4.12 band diagrams. In Fig. 4. 12(a), the pre-existing bulk trap band reported by Kerber et. al. in the HfO_2/IL dual layer stack is illustrated at the flat band condition [1]. The center of the band to the Si substrate valance band edge is offset by ΔE. The band diagrams of the stacks with O_3 and NH_3 treated interfaces at positive gate to substrate biases are shown in Fig. 4. 12(b) and 12(c). As the gate bias increases, the band bending of the interface layer (IL) will reduce the conduction band offset so that electrons in the substrate can be injected and trapped in the bulk traps. At the same gate bias, larger voltage is therefore dropped across the SiO_2 layer than the SiON layer since the dielectric constant of the O_3 treated interface (SiO_2) is smaller than that of the NH_3 treated interface (SiON), while the interfacial layer thickness estimated from the EOT results are nearly equal. As a result, the IL band bending is larger in the HfO_2/SiO_2 (O_3) stack (Fig. 4. 12b) than in the HfO_2/SiON (NH_3) stack (Fig. 4. 12c). When bulk traps offset ΔE is reduced so that part of the trap band drops below the Si valance band edge, the traps start to align with the valance band, and direct valance band to trap tunneling is energetically favorable and greatly enhances the trapping efficiency. On the other hand, for the same bias, the HfO_2 trap levels in the HfO_2/SiON (NH_3) stack can still be above the valance band edge and the probability for valance band electron injection is much smaller. In this case, only conduction

band electrons are trapped, which are not as efficient as combined conduction and valance band electrons injection seen in the O_3 treated samples.

The contribution of the conduction and the valance band electrons to the gate current can be separated as the substrate current J_{sub} and the source current J_{source} as shown in Fig. 4. 12 [11]. The gate current is the sum of these two currents contributions. The conduction band electrons mainly contribute to the source current and the valance band electrons mainly contribute to the substrate current.

4.4.3 Carrier separation results

The gate, the substrate and the source currents are monitored at the same time. The proposed enhanced valance band electrons injection model is supported by such carrier separation measurement as shown in Fig. 4. 13(a) and 13(b). At low gate biases, the gate current is mainly due to the source current from conduction band electrons in both stacks. At higher gate biases, however, contribution from the substrate current increases dramatically in the O_3 treated samples, indicating significant valance band electrons injection taking place. On the contrary, for the same high biases, the substrate current in the NH_3 treated samples is still three orders of magnitude smaller than the source current, noticing that the source current is about the same at our CVS voltage used in Fig. 4.9 (even a little bit larger). Therefore, only small amount of valance band electrons injection occur in the NH_3 treated sample and the charge trapping is not as efficient as in the O_3 treated samples. It is interesting to see that the gate current in O_3 treated stack also starts to "saturate" as the substrate current increases, which should also be an indication of the enhanced charge trapping. The enhanced valance band electrons trapping is therefore verified by this carrier separation experiment.

4.4.4 Dynamic stress results

An HP 8116A pulse generator is used for the dynamic stress measurement as shown in Fig. 4.1. A computer is used to coordinate the HP4155B semiconductor parameter analyzer and the pulse generator for stress and V_{th} measurement. The ΔV_{th} evolution during a dynamic stressing is shown in Fig. 4.14 under a very slow stress frequency. A positive gate to substrate bias is applied first and it is clear that ΔV_{th} increases due to charges trapping. When the applied bias is reversed, the ΔV_{th} decreases due to charges de-trapping. No matter which gate is used, the O_3 treated samples always have larger ΔV_{th} in both trapping and de-trapping stages than the NH_3 treated samples. This better de-trapping in NH_3 treated samples is understandable because the SiO_2 conduction band edge offset to the Si substrate is larger than that of the SiON. Therefore, the electron de-trapping barrier is lower for SiON IL than for SiO_2 IL stacks. As a result, the electrons are more easily de-trapped in NH_3 treated stacks than that in the O_3 treated stacks, contributing to its improved dynamic V_{th} instability. It should also be noted that for the TiN gated samples the V_{th} shift recovers more during de-trapping than the poly-Si gated samples. The V_{th} can even recover to its initial value (ΔV_{th}<5mV) for the NH_3 treated samples. This will be discussed in the next section on the different gate electrode effects.

4.5 Gate electrode effects

4.5.1 DC stress results

In Fig. 4.9 and Fig. 4.10, the DC stress data have already shown that the O_3 treated samples have worse V_{th} stability than the NH_3 treated samples no matter TiN metal gate or the poly-Si gate is used. Therefore, only the NH_3 treated sample will be used for different gate electrodes effects discussion. The ΔV_{th} vs. DC stress time at varying stress voltages are shown in Fig. 4.15. Even though stress fields in the TiN electrode gated stacks exceed that of the poly-Si gate electrode, it is clear that for the same stress voltage (V_g-V_{fb}) the poly-Si gated samples always show larger ΔV_{th} than the TiN gated samples. The extracted operation voltage for 10-year lifetime projection is 1.8V for TiN gated samples and only 0.8V for poly-Si gated samples. Because the bulk HfO_2 traps density should be the same for both stacks, this significantly degraded V_{th} stability in poly-Si gated devices indicates that additional traps may be introduced at the top poly-Si/high-K interface as compared to the metal TiN gate. The origin of these traps most probably arises from the poly-Si/high-K interface reaction as shown by the XTEM in Fig. 4.16 [12], where a sharp TiN/high-K interface is shown but an interfacial layer is formed at the poly-Si and the HfO_2 interface.

4.5.2 Dynamic stress results

The existence of such top interface traps can also be observed through AC dynamic stress measurement. Since the top interface traps are farther away from the Si substrate surface, they can be expected to have a longer characteristic charging time as compared to the HfO_2 bulk traps. This is shown in Fig. 4.17 when V_{th} shift of these two devices are compared under an AC stressing at a very low frequency. It is clear there are four trapping and de-trapping stages during one stress cycle as labeled in Fig. 4.17(a). At stage (i) from time zero to five seconds stress, the ΔV_{th} increases very quickly for both devices. After that the ΔV_{th} increases slowly at stage (ii) and the poly-Si gated device shows a faster increase than the TiN gated devices. At stage (iii) both devices have a fast recovery due to charge detrapping, but poly-Si gated devices show a larger residual ΔV_{th}. In stage (iv), TiN gated devices almost completely recover to the initial V_{th}, but poly-Si gated devices recover to the initial V_{th} at a much slower rate. Log-log plots for the de-trapping stages for Fig. 4.17(a) are redrawn in Fig. 4.17(b) for better illustrating of the different discharging phases. Such phenomena can be qualitatively understood through the band diagram as shown in Fig.4.18. In addition to the bulk trap band reported for the SiO_2/HfO_2 gate stack, the top IL for the poly-Si gated devices introduces more trap states. At stage (i), only fast traps close to the bottom IL are charged and they are the same for both devices so they exhibit a similar charging behavior. As top IL starts to charge at stage (ii), the top IL traps have a slower charging time constant and also introduce a larger shift

in poly-Si gated devices. When devices start to de-trap at stage (iii) those trapped charges close to the bottom IL will discharge first but more residual charges exist in the poly-Si gated devices, resulting in a slow recovery of the ΔV_{th}. Finally, at stage (iv) trapped charges close to the top IL start to discharge but poly-Si gated devices show a much slower discharge time constant. Such AC stress results clearly demonstrate that the traps have a different physical nature at the top electrode/high-K interface for two different gated devices.

Though poly-Si gated devices exhibit significantly degraded DC V_{th} stability. The frequency dependence results under AC stress demonstrate that the top IL in the poly-Si gate electrode has less impact during a practical CMOS operation. Figure 4.19 shows the ΔV_{th} after 1000s stress at various frequencies. At very low frequency, poly-Si gated devices show degraded ΔV_{th}, however, as stress frequency increases, the ΔV_{th} for both stacks decreases and the difference between two devices converges, indicating that the charge trapping time is not long enough for top interface traps to be charged. At high enough frequency (>10Hz), there is negligible difference between the two stacks because only the traps close to the Si substrate surface are charged, a region which is similar for both stacks.

Both HfO_2 stacks in this work show negligible G_m degradation, while the ΔV_{th} acts as the lifetime limiter. This is probably due to interface states passivation effects as shown in Fig. 4.20. During gate stress the SS has negligible change indicating little interface state generation. While during drain stress SS starts to

increase since hole injection starts to occur and leads to interface states generation. However, these generated interface states can again be recovered during the following “drain stress” as shown by the SS decrease. Such electrical passivation effect has been observed and explained by an H^+ diffuse-drift model reported for ultra thin SiO_2 stacks [7] but is first time reported for HfO_2 based devices. In Fig. 4.21, the mechanism for such diffuse-drift model is illustrated.

4.6 Summary

In this chapter the impact of the top gate electrodes and the bottom interface treatments on the HfO_2 NMOS V_{th} instabilities are systematically studied. Ultra thin high quality HfO_2 thin films were fabricated with excellent leakage current reduction.

Two popular interface treatment techniques NH_3 and O_3 are compared. No matter what gate is used the O_3 treated samples always demonstrate a worse V_{th} stability than the NH_3 treated samples under DC stressing. This is explained by an enhanced valance band electrons injection model. This model is successfully supported by carrier separation measurement results. Under AC dynamic stresses, the NH_3 treated samples also exhibit better recovery of the V_{th} shift. Therefore, NH_3 treatment is a better choice on the interface treatment for the HfO_2 NMOS devices.

Poly-Si and TiN metal gate electrodes are compared for the gate electrodes effect. Under DC bias stresses even with a higher stress field, the TiN gated samples show a better V_{th} stability than the poly-Si gated samples. The XTEM pictures demonstrate a top interface layer existing in the poly-Si gated samples while a sharp interface existing in the TiN gates samples. This top interfacial layer introduces additional traps to the devices. The AC dynamic stress demonstrates two different kinds of traps existing in these stacks with different characteristic charging time constants. However, as the stress frequencies increases, the V_{th} shifts differences between two samples become smaller and finally diminishes. This indicates that the top interfacial layer may only play a minor effect in affecting the V_{th} reliability as the

operating frequency increases. Consistent with previous reports, the G_m degradation is found not as severe in the HfO_2 high-K gate stacks as the V_{th} instability to be the device lifetime limitation factor. Although the interface states can be generated during the hole injection stages, these generated interface states can be passivated during the following reverse stress bias. Therefore, dynamic stress is a key for the correct evaluation of the HfO_2 BTI reliability performances.

4.7 References

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"Subnanometer Scaling of HfO_2/Metal Electrode Gate Stacks," *Electrochemical and Solid-State Letters*, vol. 17, no. 8, pp. G164-G167, 2004.

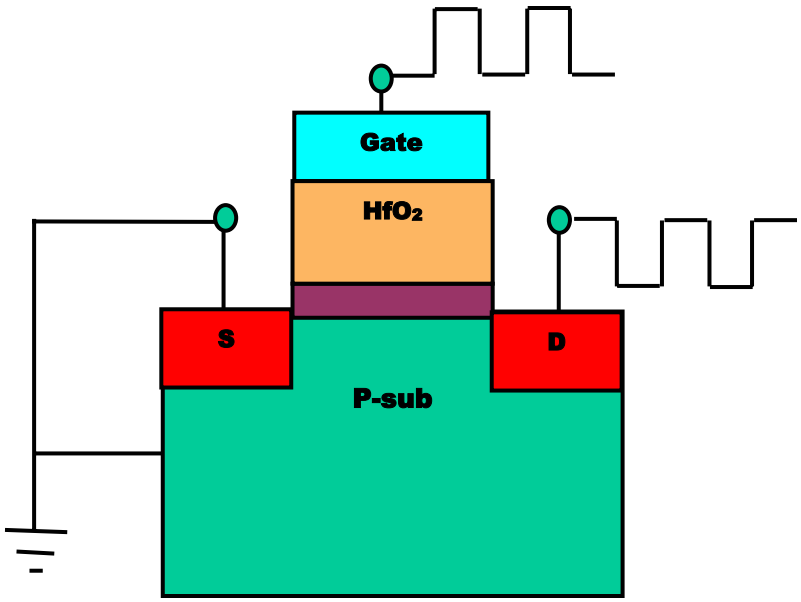


Fig. 4.1 Dynamic AC stress setup. Two inverted stress signals are applied on the drain and the gate at the same time.

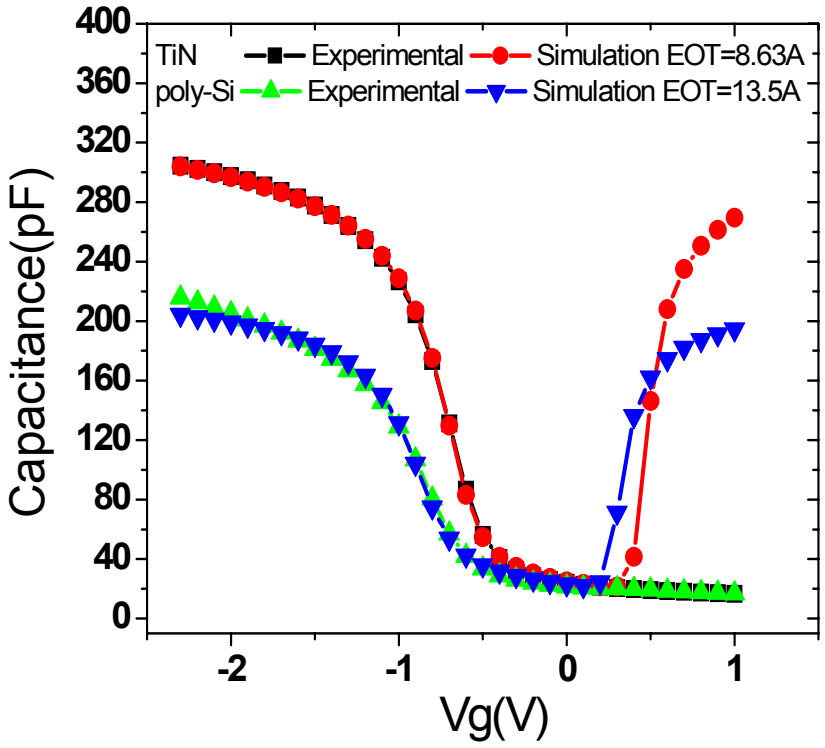


Fig. 4.2 Experimental and simulated C-V curves for NH_3 treated samples with different gate electrodes.

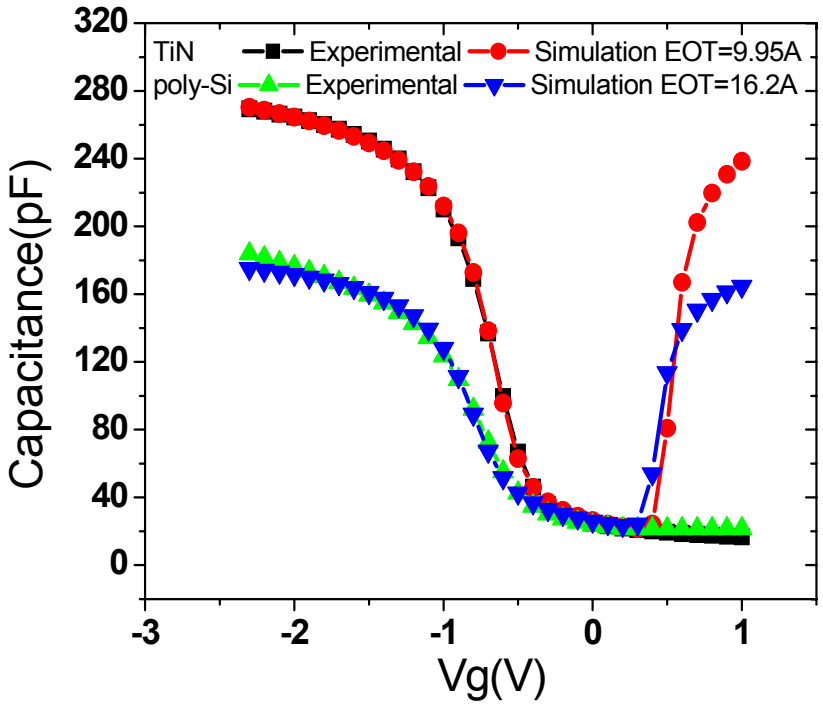


Fig. 4.3 Experimental and simulated C-V curves for the O_3 treated samples with different gate electrodes.

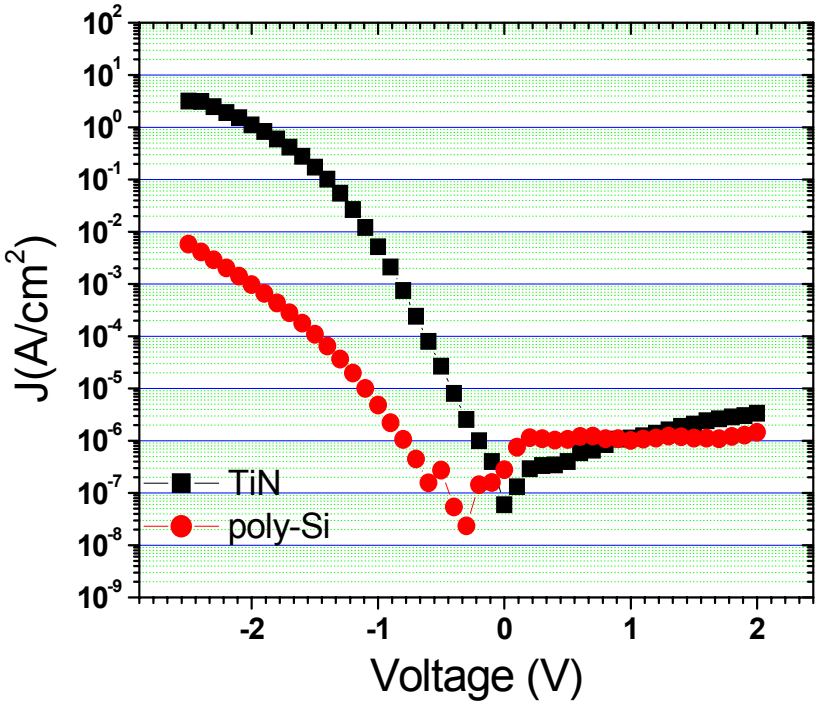


Fig. 4.4 Jg vs.Vg curves for NH_3 treated samples with different gate electrodes.

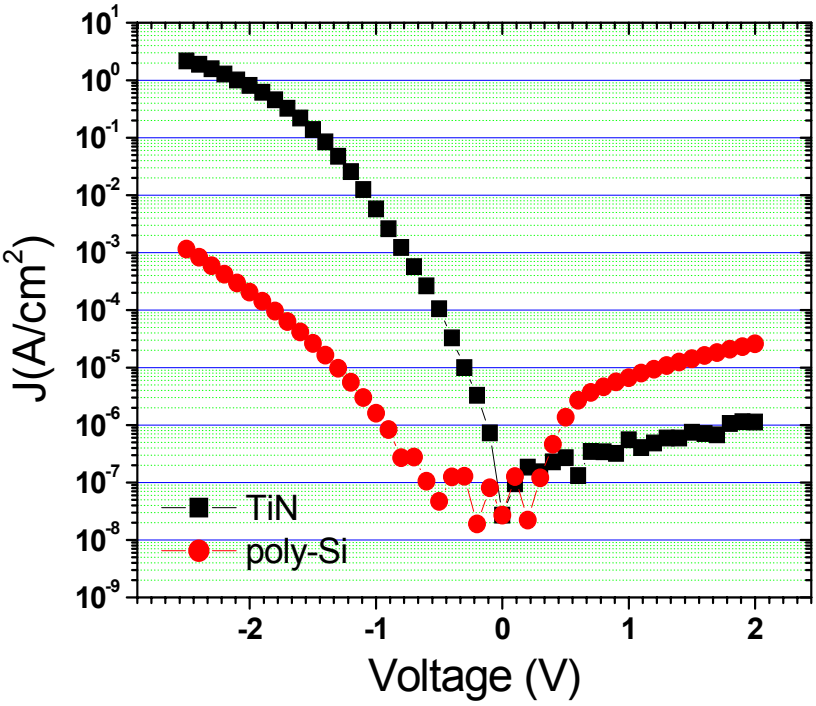


Fig. 4.5 Jg vs. V curves for O_3 treated samples with different gate electrodes.

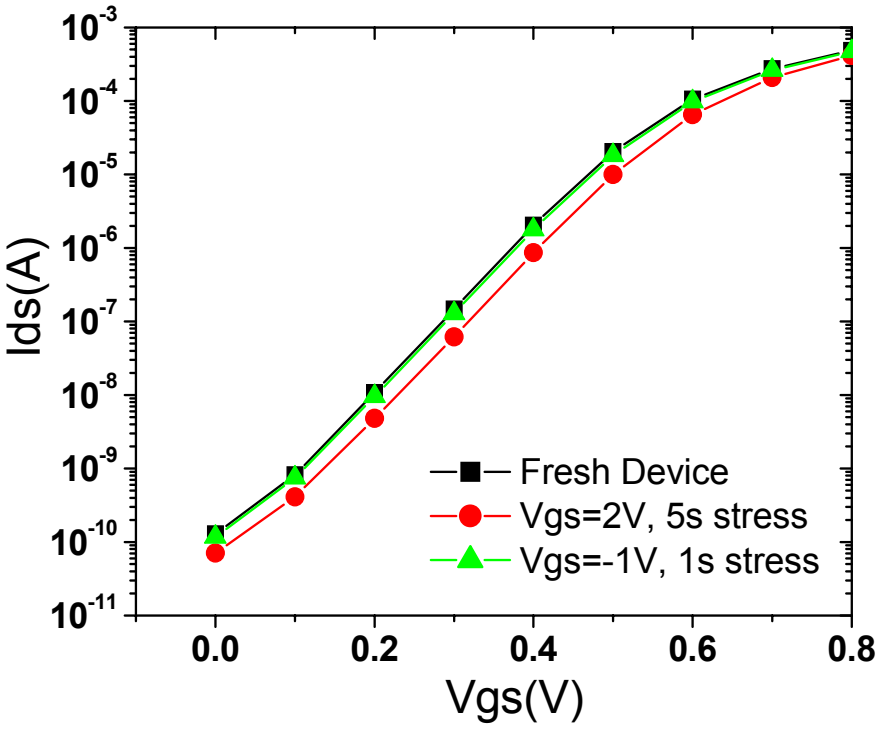


Fig. 4.6 Id vs. Vg shift for TiN gated NH_3 treated samples under a DC positive stress followed by a negative stress show that the V_{th} can be fully recovered and that sub-threshold slopes have negligible changes.

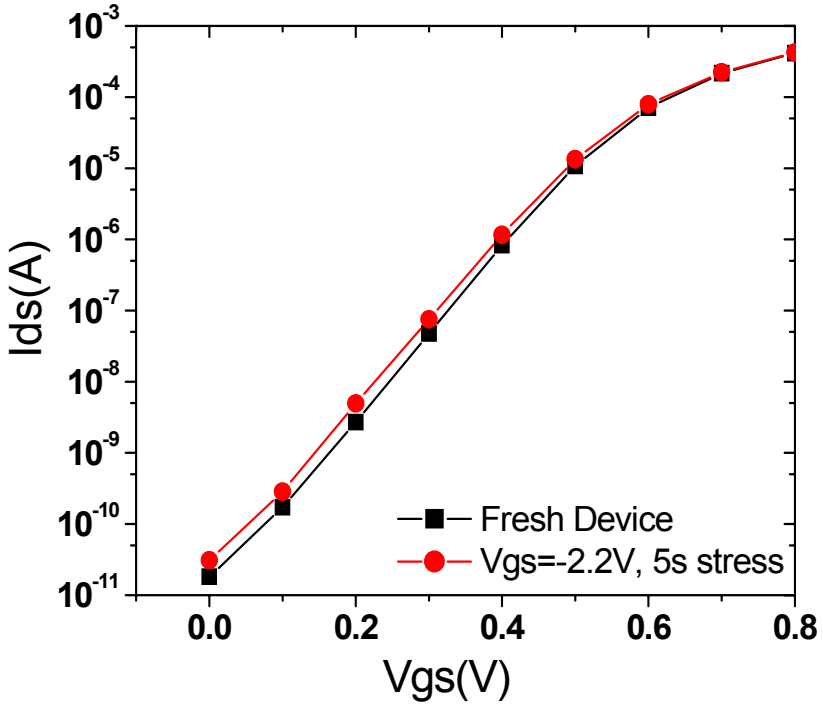


Fig. 4.7 Id vs. Vg shift for TiN gated NH_3 treated sample under a DC negative stress showing V_{th} shifts to the negative direction and the sub-threshold slopes increases.

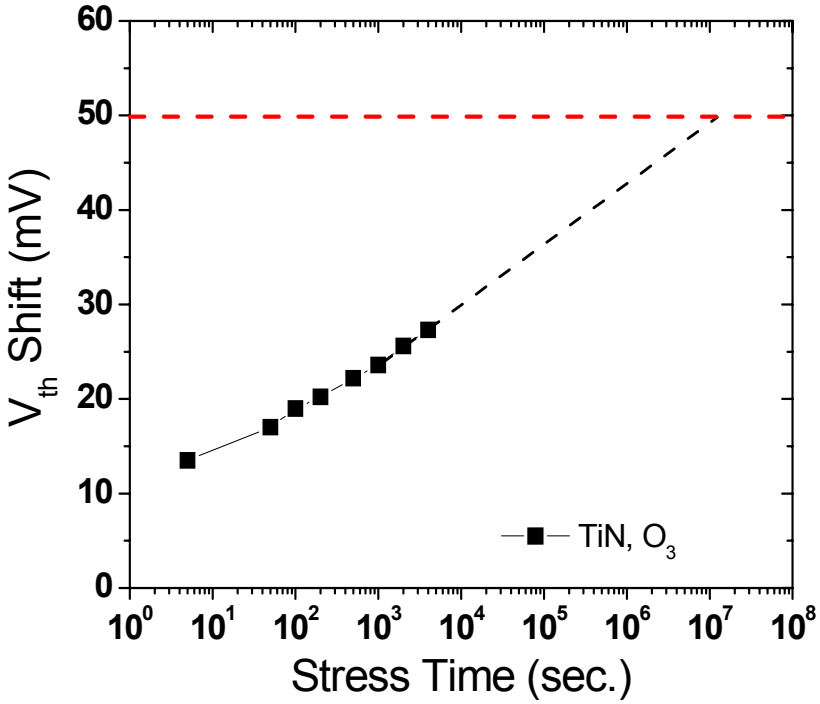
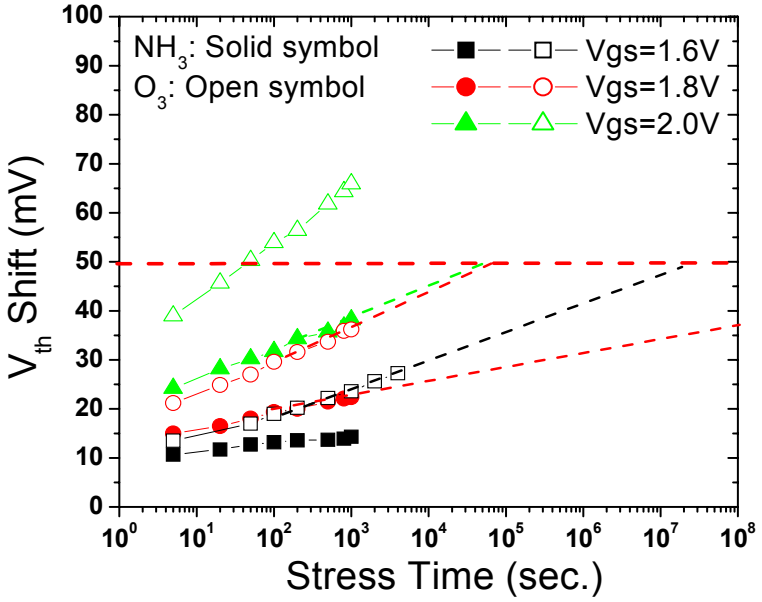
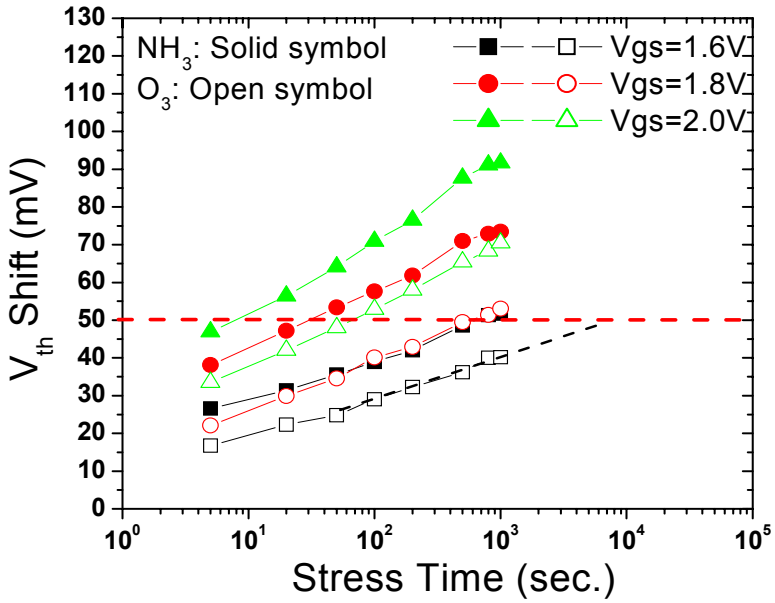


Fig. 4.8 V_{th} shift vs. CVS stress time for a TiN gated O_3 treated samples show a nice *log*t dependence up to 4000s.



(a)



(b)

Fig. 4.9 V_{th} shift under DC stress for (a) TiN gated and (b) poly-Si gated samples show O_3 treated samples have worse V_{th} stability.

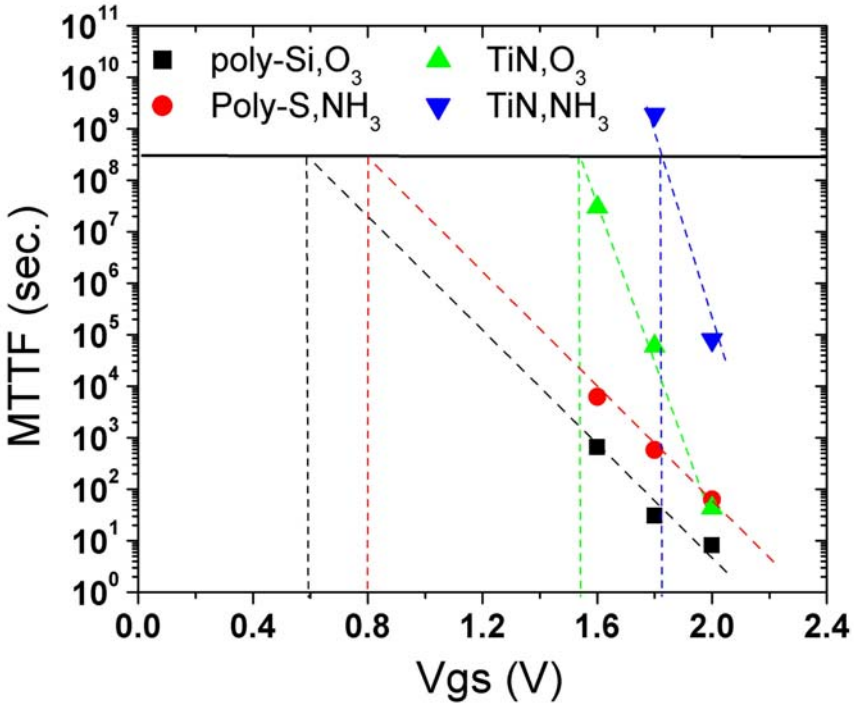


Fig. 4.10 CVS 10-year lifetime and operation voltage extrapolation for all four stacks.

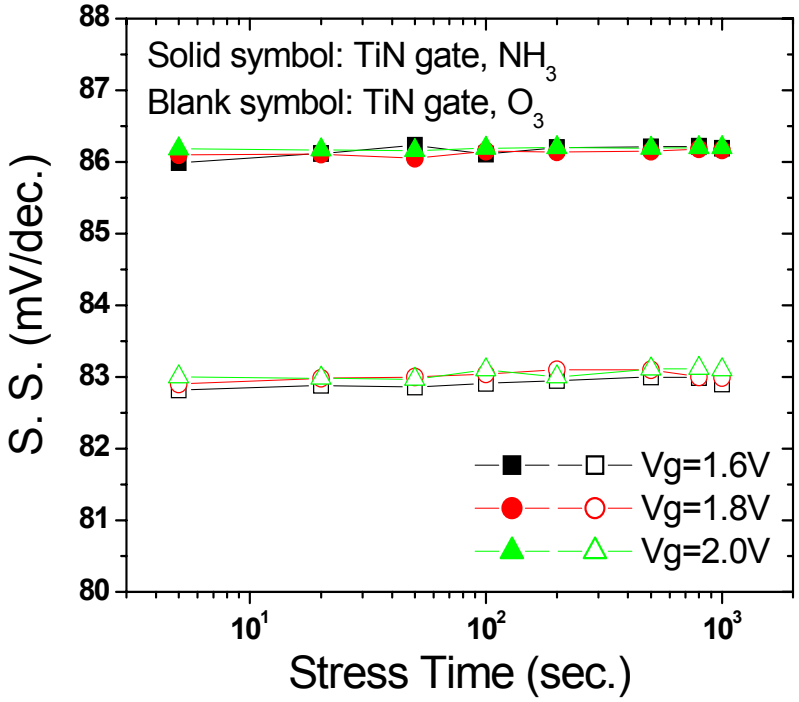
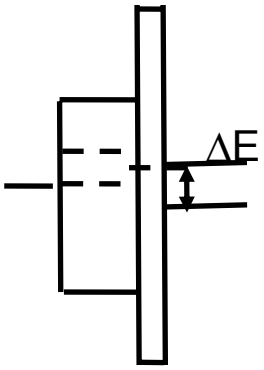
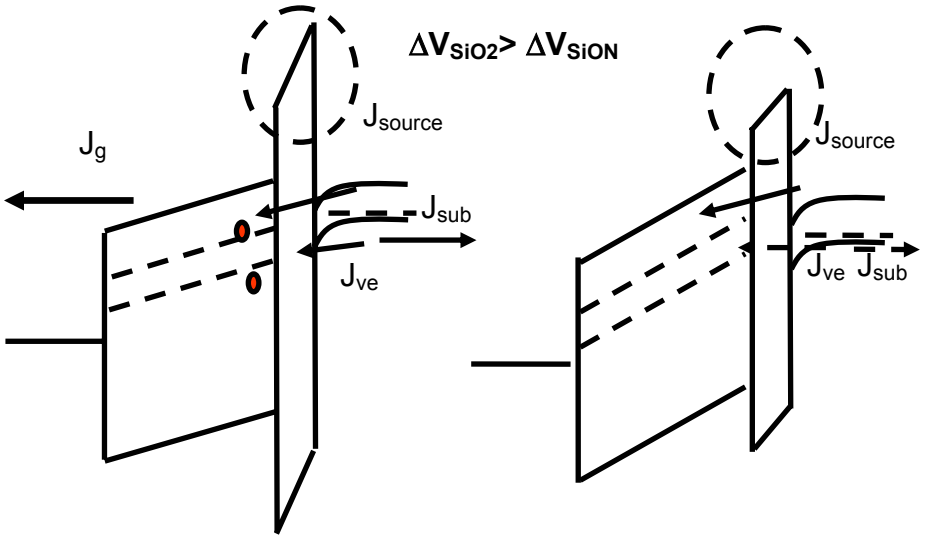


Fig. 4.11 Sub-threshold slope changes during a DC bias stressing.

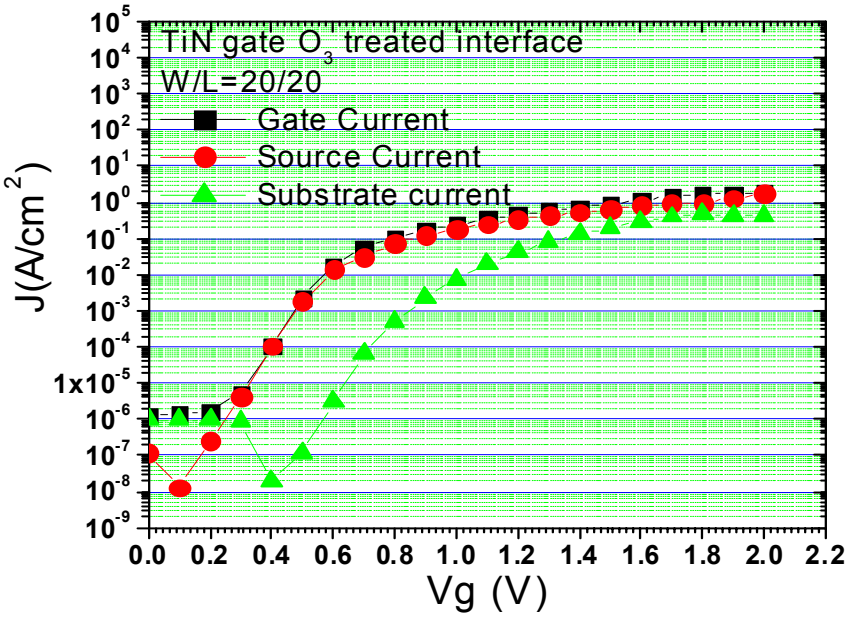


(a) TiN/HfO_2/IL/Si

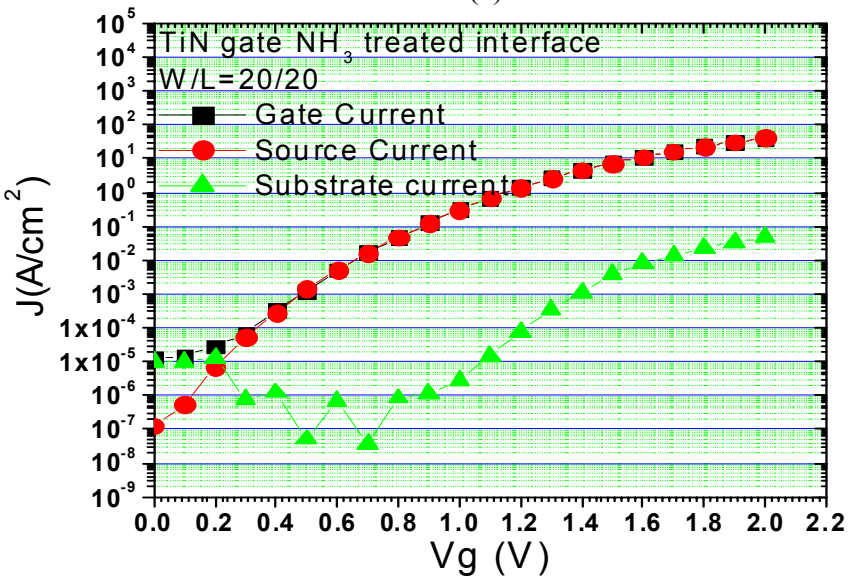


(b) TiN/HfO_2/SiO_2/Si (c) TiN/HfO_2/SiON/Si

Fig. 4.12 Band diagrams of the (a) high-K/IL stack at flat-band condition, (b) the O_3 treated and (c) the NH_3 treated samples. Enhanced valance band electron injection exists in the O_3 treated samples.

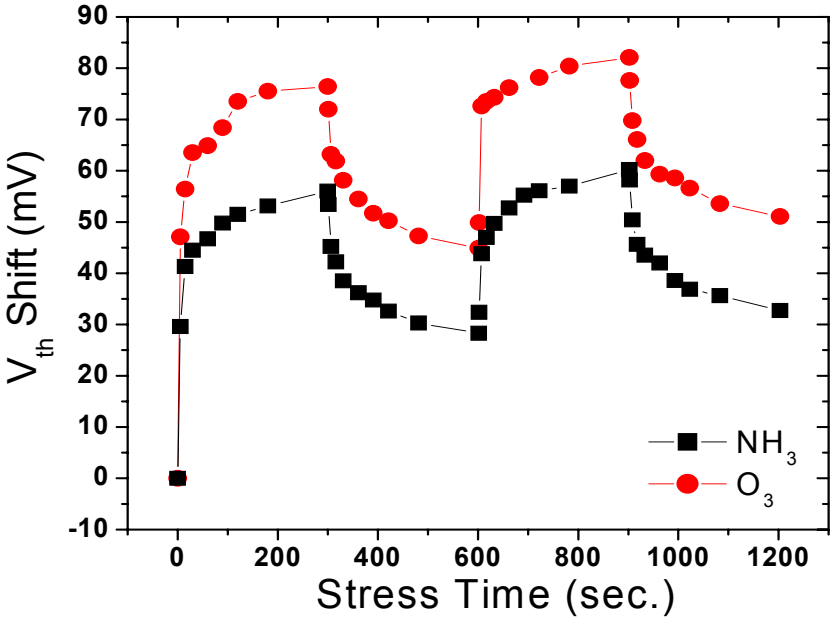


(a)

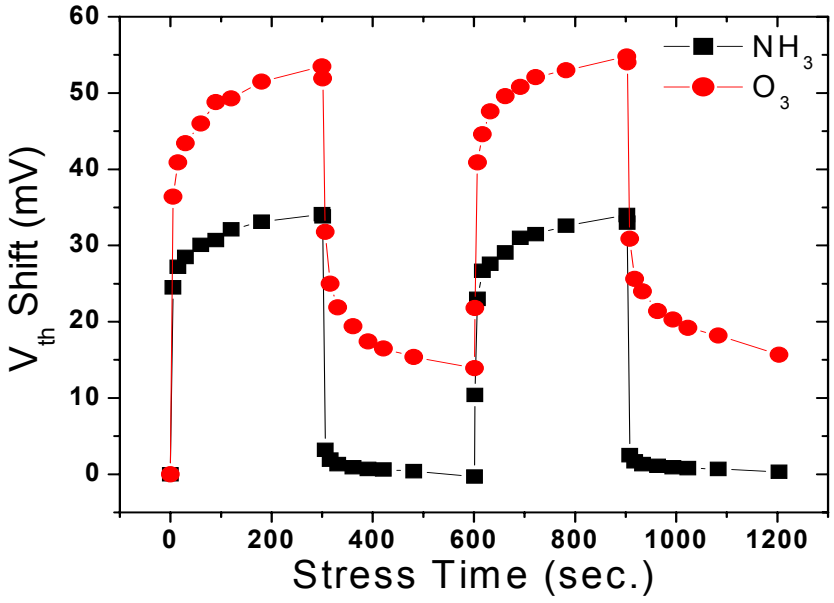


(b)

Fig. 4.13 Carrier separation results confirm that significant amount of valance band electrons injection exist in the O_3 treated samples as shown by J_{sub} in (a), while this is negligible in NH_3 treated samples (b).



(a) poly-Si gate



(b) TiN gate

Fig. 4.14 V_{th} shifts under a dynamic stress for (a) the poly-Si gated samples and (b) TiN gated samples with different interfaces.

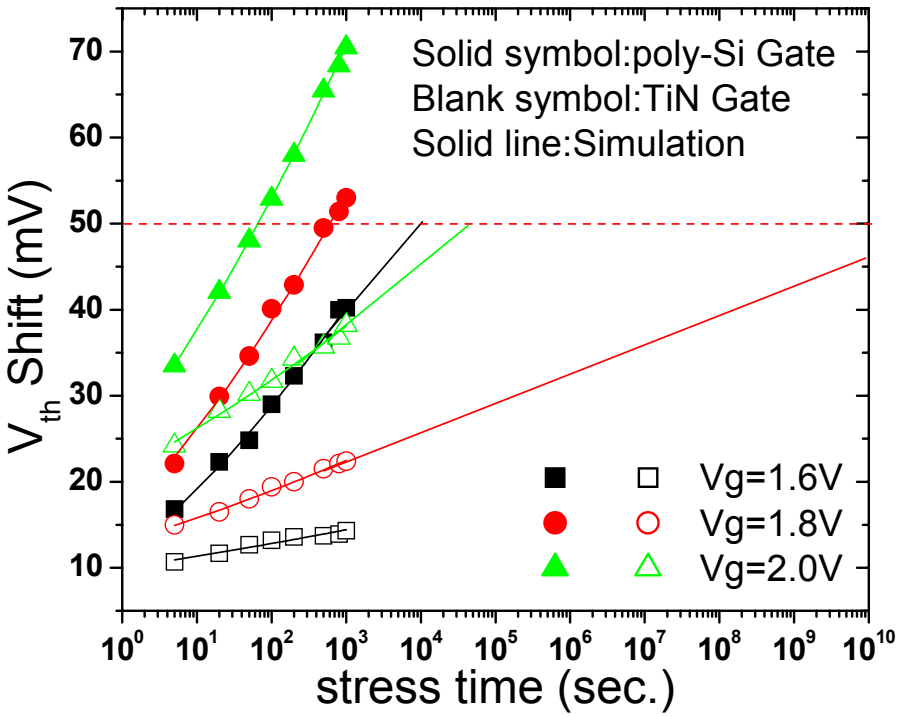
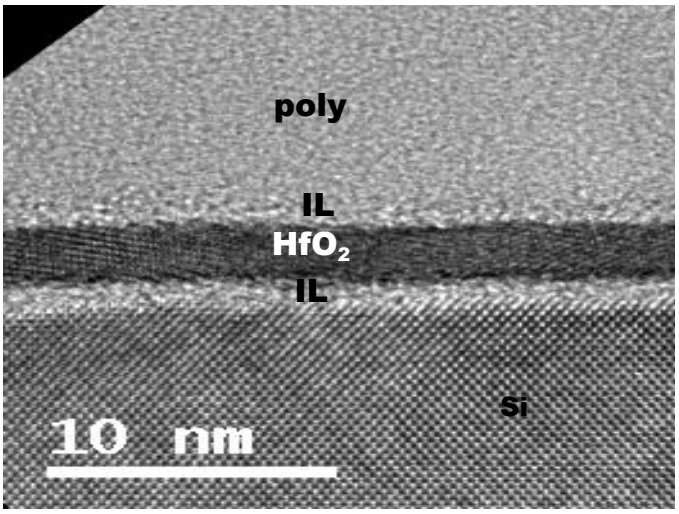
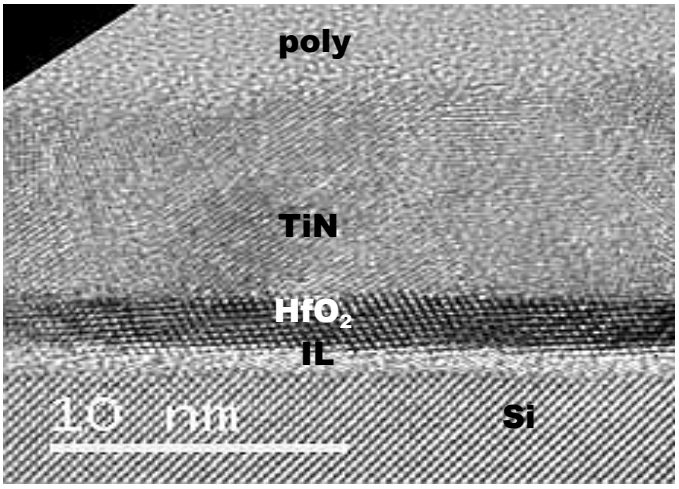


Fig. 4.15 Voltage threshold shifts ΔV_{th} vs. CVS stress time at varying gate stress voltages show a log*t* dependence on the stress time. Poly-Si gated devices show a larger ΔV_{th} at the same stress (V_g-V_{fb}) vs. TiN gated devices.



(a) poly-Si gate



(b) TiN gate

Fig. 4.16 XTEM of the two devices show a sharp interface between TiN and HfO_2 but an interfacial layer (IL) is formed between poly-Si and HfO_2.

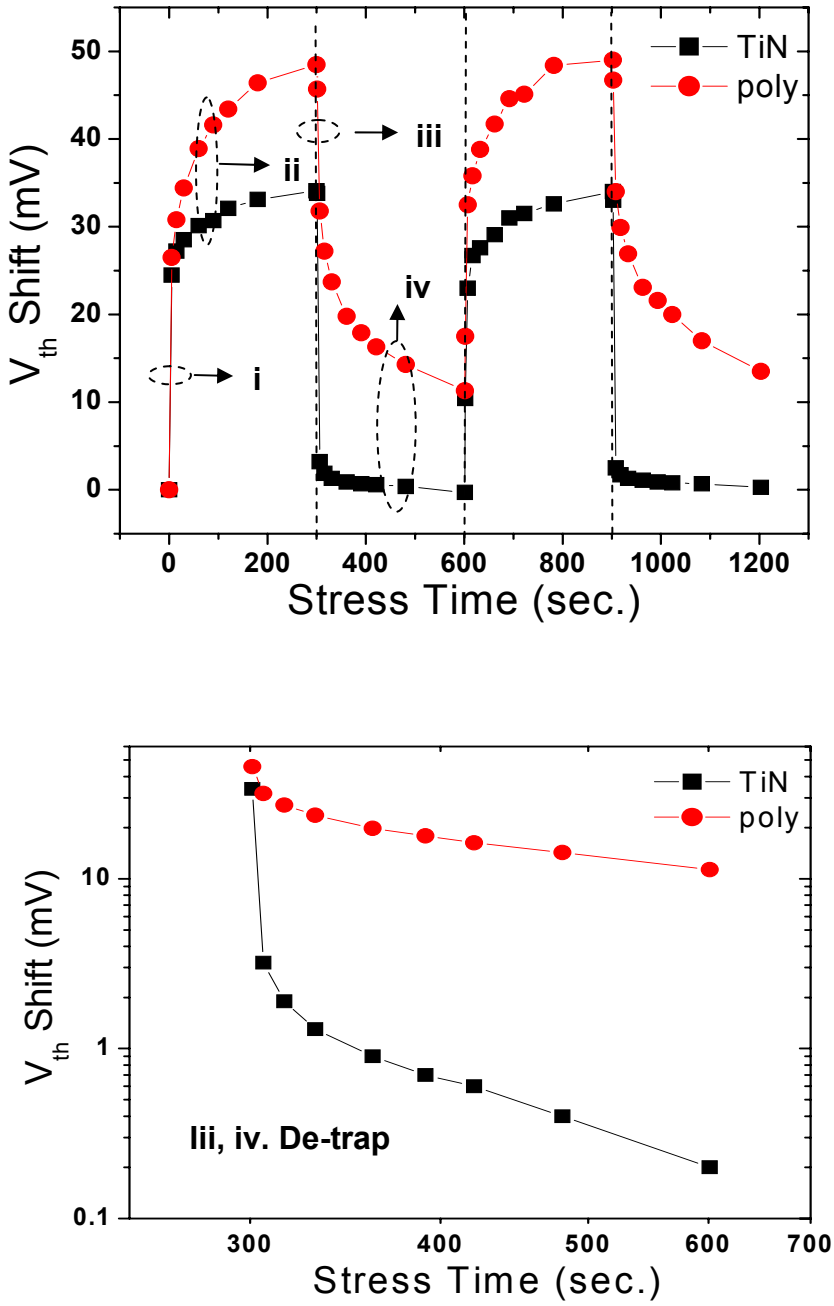


Fig. 4.17 (a) Low frequency AC stress result demonstrates four different stages existing during charges trapping and de-trapping. (b) The *log-log* plot for the detrapping stage is redrawn. (gate stress: V_g-V_{fb}=2.65V, V_d=V_s=V_{sub}=0; drain stress: V_d-V_{fb}=1.35V, V_g=V_s=V_{sub}=0.)

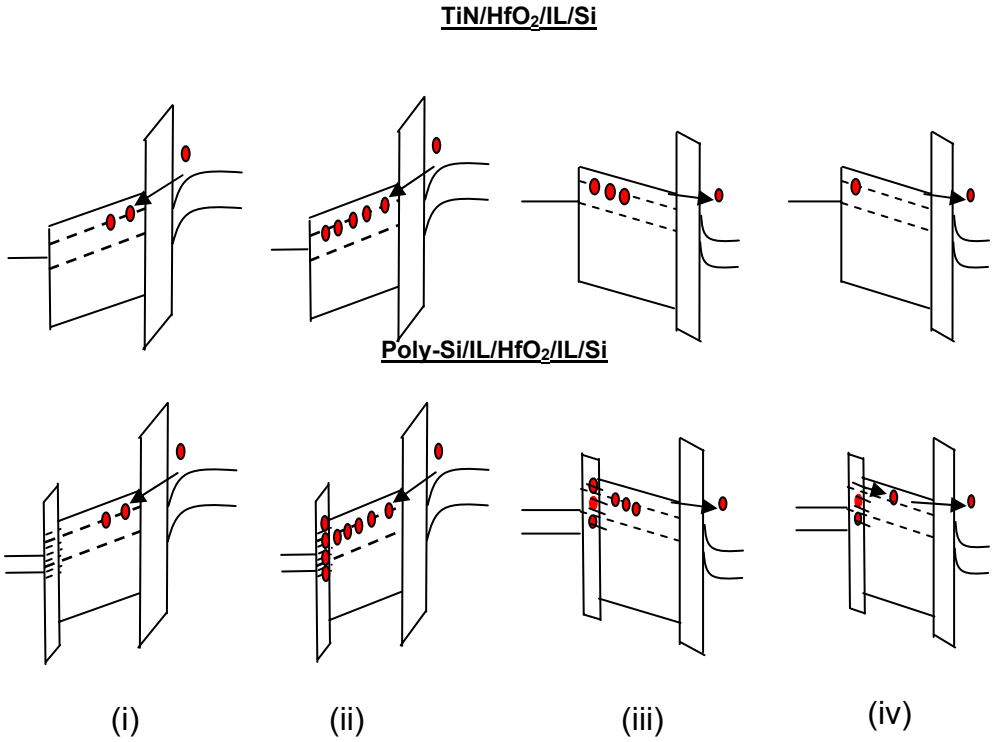


Fig. 4.18 Energy band diagrams at four stages to illustrate how charge trapping/de-trapping behaves differently due to the additional top IL traps in poly-Si gated devices for understanding curves in Fig. 4.17.

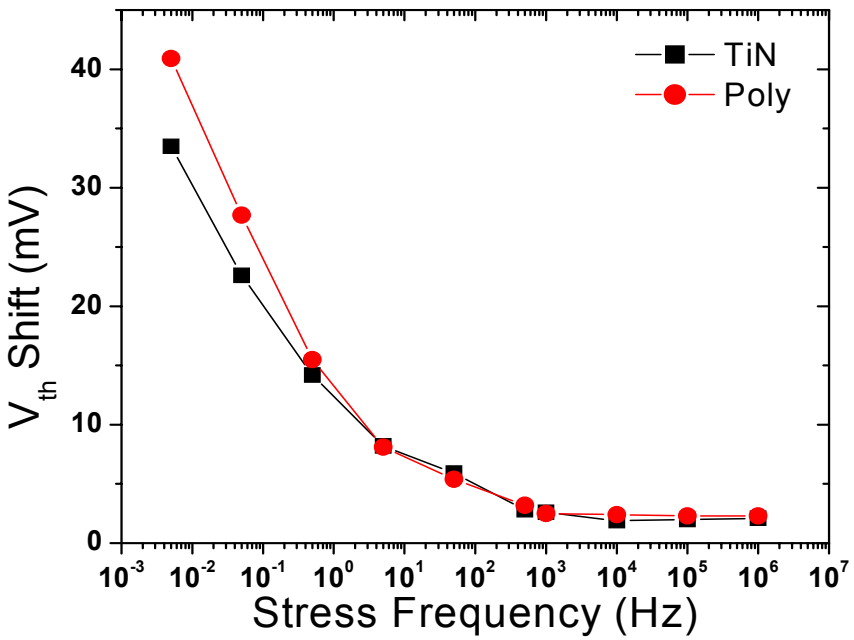


Fig. 4.19 ΔV_{th} after 1000s stress at various stress frequencies demonstrates that ΔV_{th} difference between two stacks decreases as frequency increases, indicating the top gate induced traps only affect Vth stability at very low frequency.

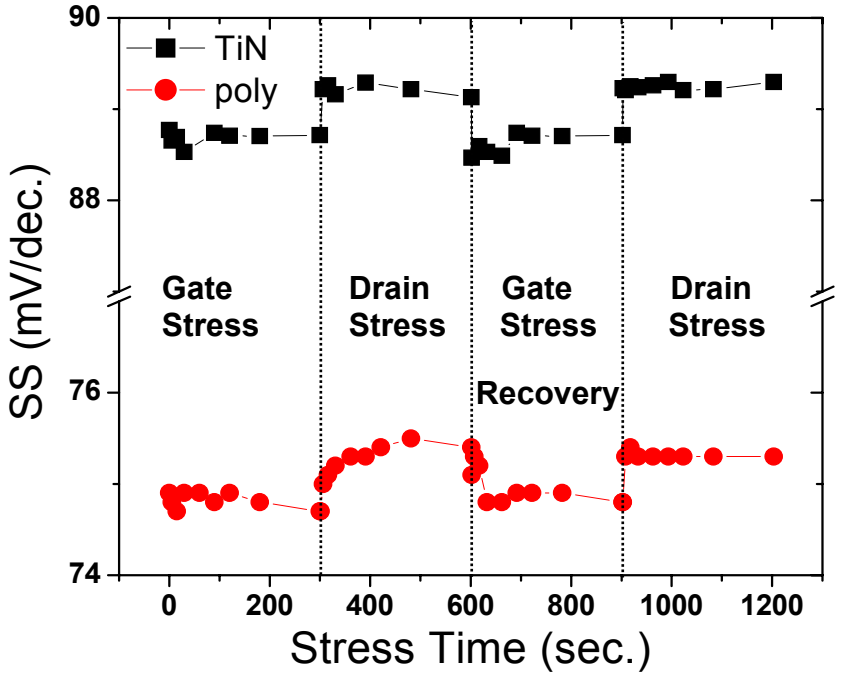
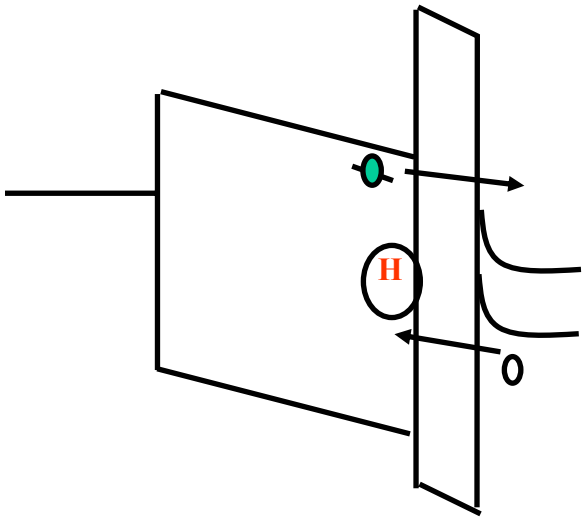
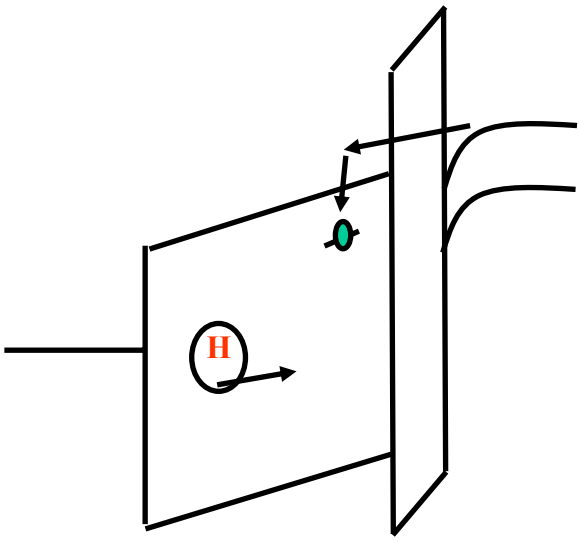


Fig. 4.20 The SS during the dynamic stress show negligible change under first gate stress followed by an increase during first drain stress. But this increased SS recovers to its initial value during the following gate stress indicating the passivation of the generated interface states.



(a) Drain stress



(b) Gate stress

Fig. 4.21 H release during (a) drain stress and recovers during (b) gate stress for the interface states generation and passivation [7].

	SiO_2	HfO_2
Life time limitation factor	**NBTI**	**PBTI (Onishi, TED, 2003)**
Mechanism	**New Nit and Not generation**	**Preexisting trap charging (Kerber, IRPS, 2003)**
Characterization	**DC Id-Vg**	**Dynamic Id-Vg (Kerber, IRPS, 2003)**
Dynamic stress response	**Frequency independent (Alam, IEDM, 2003)**	**Slow traps and fast traps different (Shen, IEDM, 2004)**

Table. 4.1 Comparison between SiO_2 and HfO_2 V_{th} instability behaviors according to published results.

Wfr ID	20	11	17	14
Interface	NH_3	NH_3	O_3	O_3
Electrode	Poly	TiN	Poly	TiN
EOT(Å)	13.4	8.63	16.2	9.95
Vfb(V)	-0.87	-0.65	-0.81	-0.62
Vth(V)	0.23	0.51	0.39	0.57
Jg@Vfb-1(A/cm^2)	4.30E-04	2.66E-01	1.45E-04	2.44E-01
E-high Mobility (cm^2/Vs)	149.8	125.1	150.2	123.7

Table. 4.2 Electrical data for all four stacks.

Chapter 5 Conclusions and Future Studies

5.1 Conclusions

In this work, SONOS type non-volatile memory using high-K gate dielectrics are proposed and demonstrated for the first time. The impacts of the top gate electrodes and the bottom interface treatment techniques on the NMOS HfO_2 transistors V_{tb} instability reliability are also studied.

Two novel high-K SONOS structures, the TaN-HfO_2-Ta_2O_5-HfO_2-Si (MHTHS) and the TaN-Al_2O_3-Ta_2O_5-HfO_2-Si (MATHS) are demonstrated. By using HfO_2 to replace the SiO_2 for the bottom tunneling layer, a physically thicker tunneling oxide can be used. Because the electron/hole injection barrier of the HfO_2 is lower than that of the SiO_2, improved programming current even with thicker bottom layers can be achieved. This thicker bottom layer is also beneficial for longer data retention. Another factor to improve the data retention is the introduction of the Ta_2O_5 for the charge trapping layer. Compared to Si_3N_4, the trap level in the Ta_2O_5 is much deeper and its conduction band-edge offset to the HfO_2 tunneling layer is also larger than that of the Si_3N_4 to the SiO_2 layer. These all contribute to better data retention performance. Therefore, longer retention and faster programming than the conventional SONOS memories can be achieved simultaneously in MATHS and MHTHS structures. The fabricated MHTHS devices exhibit an ultra-fast

programming speed, excellent retention, superior endurance and good resistance to read disturb. However, the memory window of this MHTHS device is not large enough for a practical memory application. For this reason, the MATHS device is proposed and fabricated.

Though the lower barrier of the HfO_2 is ideal as the bottom tunneling layer for better programming, it is not favorable as the top blocking layer. F-N tunneling in the top blocking layer is also large during the programming due to the low charge blocking barrier. As a result, much of the injected charge will escape from the top layer. To improve the top blocking efficiency, Al_2O_3 is used to replace HfO_2 as the top blocking layer due to its much higher barrier. After carefully selecting the top Al_2O_3 thickness, a MATHS and a MHTHS device are compared. The measurement results demonstrate that MATHS devices have a much better charge trapping capability than MHTHS, hence a larger memory window at both room temperature and elevated temperatures. The advantages of faster programming and longer retention of the high-K SONOS memory is still kept in this structure. Compared to the state-of-the-art SONOS memory, the MATHS device can be written at a faster speed of 100ns, erased at μs, and has excellent data retention. This is achieved at an EOT less than 10Å, which can never be achieved in conventional SONOS memories. Therefore, such memory has a high potential to extend the scaling trend for the next generation of non-volatile flash memory.

NMOS HfO_2 transistors with NH_3 and O_3 interface treatments were also compared. Under DC stress, NH_3 treated samples are found to suppress the V_{th} shift

versus O_3 treated samples. More charges trapping in the O_3 treated interfaces was explained by an enhanced valance band electron injection model. Such a model was verified through a carrier separation test, which shows a significant amount of valance band electron current in the O_3 treated sample but not in the NH_3 treated samples. A dynamic stress measurement on these samples also shows that the NH_3 treated samples have better charge detrapping capability, which suggests the NH_3 interface treatment technique is better than the O_3 treatment in terms of V_{th} instability.

In terms of gate electrode effects, the poly-Si and the TiN metal gate were compared. The DC stress results show that the TiN gated samples have better V_{th} stability than the poly-Si gated samples even under a higher stress electric field. This is attributed to additional top interfacial traps formed at the poly-Si/HfO_2 interface and is supported from the XTEM and dynamic stress measurement results. However, when stress frequencies increase both devices show similar smaller V_{th} shift, indicating the top interface plays a minor role at higher operation frequencies. The interface states are found to be passivated during the dynamic stress and are not of major concern as compared to the V_{th} instability reliability.

5.2 Future Studies

The high-K SONOS memory results demonstrate it is a promising candidate for the next generation of non-volatile memory. However, some additional work may need to be addressed before its successful integration. For instance, currently the device activation temperature must be under 700°C. If higher temperature is used, the memory window will be closed. The mechanism for such phenomenon is not clear and it may be due to the different stacks interaction at higher temperature annealing. Therefore, detailed physical characterization of the high-K SONOS structure during different stages of fabrication is necessary. By correlating this information with the electrical data, a solution may be found to improve the thermal budget for such memories.

Due to the measurement setup resolution limit, the compared V_{th} instability results for the NMOS HfO_2 stacks are only valid for the slow traps inside the HfO_2 films. A fast pulsed Id-Vg measurement may be needed to include also the fast traps trapping and detrapping effects for these different gate electrodes and/or interface treatments.

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