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Methods for High Volume Mixed Signal Circuit Testing in the Presence of Resource Constraints

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Methods for High Volume Mixed Signal Circuit Testing in the Presence of Resource Constraints

by

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To Baba, the inspiration to start this effort.

And to Ira, the motivation to complete it.

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My father, a.k.a. Baba, has been the silent inspiration behind my drive to pursue this degree and I am grateful for the support and motivation received from both my parents. They have always been present as a safety net throughout my childhood, and I am thankful to them for giving me the freedom to follow my interests while also being protected.

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This Ph.D. is a culmination of my interest in science and technology that began at a very young age. However, I recall that as a child, I was not particularly thrilled with the idea of spending my days at school and had even openly expressed my protests. So I most definitely would like to thank my caring kindergarten teacher Mrs. Vrundatai Sule, for ensuring that I actually made it to the first grade in school to begin with.

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I understand that it almost takes a village to raise a child, specially when the child is planning to do a Ph.D., part time. My extended family, friends, teachers over the years, colleagues who may not have been mentioned here, deserve a note of gratitude from my side and I would like to sincerely thank each and every one of them.

Methods for High Volume Mixed Signal Circuit Testing in the Presence of Resource Constraints

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Analog and mixed signal device testing is resource intensive due to the spectral and temporal specifications of the input/output interface signals. These devices and circuits are commonly validated by parametric specification tests to ensure compliance with the required performance criteria. Analog signal complexity increases resource requirements for the Automatic Test Equipment (ATE) systems used for commercial testing, making mixed signal testing resource inefficient as compared to digital structural testing. This dissertation proposes and implements a test ecosystem to address these constraints where Built In Self Test (BIST) modules are designed for internal stimulus generation. Data learning and processing algorithms are developed for output response shaping. This modified output response is then compared against the established performance matrices to maintain test quality with low cost receiver hardware. BIST modules reduce dependence on ATE resources for stimulus and output observation while improving capability to test

multiple devices in parallel. Data analysis algorithms are used to predict specification parameters based on learning methods applied to measurable device parameters. Active hardware resources can be used in conjunction with post processing resources to implement complex specification based tests within the hardware limitations. This dissertation reviews the results obtained with the consolidated approach of using BIST, output response analysis and active hardware resources to reduce test cost while maintaining test quality.

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Chapter 1

Introduction

Mixed signal modules consist of digital and analog blocks and interfaces with vastly different test requirements and specifications for individual components. Testing and validation of mixed signal blocks typically includes stimulus generation and response observation in both analog and digital domains. Analog stimulus and response signals have stringent temporal and spectral requirements that are dictated by the final application of the analog IP. Complex test hardware is required to meet these requirements; the higher cost of this hardware results in a higher test cost for mixed signal modules.

Minimizing test cost can be achieved by various approaches, such as:

- **Multi-Site Testing:** Parallel testing for multiple Devices Under Test (DUT) results in test cost reduction. Pin resource limitations and DUT power requirements are major constraints which limit multi-site configurations. Limiting the use of ATE resources with BIST schemes may enable further scaling of multi-site capabilities.

- **Test Parallelization:** Parallel testing attempts to independently test various blocks in DUT with mutually-exclusive internal and ATE resources. Due to ATE resource sharing limitations, this approach can

saturate for conventional testing methods. BIST schemes and output analysis methods may aid parallel testing of various blocks if the dependency on ATE stimulus and response capture resources can be reduced.

- **Lower Cost Test Hardware:** A low cost test solution can be provided by reducing the ATE system capabilities. The number of power supplies/signal pins/power specifications may be lowered as compared to a full-capacity ATE to reduce cost. Use of innovative methods for stimulus generation and response analysis is needed to maintain test quality with limited resources available.

ATE used in digital domain address cost concerns by lowering timing/power or tester channel requirements. Very-Low-Cost (VLC) ATE systems are devised by optimizing the available ATE resources for performing basic structural testing. Low pin speeds, reduced ATE channel resources, minimal analog test hardware and reduced set of ATE power supplies may be enforced in order to drive down the VLC-ATE cost. Although VLC-ATE are capable of performing digital structural testing with available resources, they have limited analog test capabilities. Adding analog stimulus generation and response observation capabilities to VLC-ATE results in a overall test cost increase.

Various practical factors in modern semiconductor manufacturing demand high test coverage and test quality at minimal test cost [1]. Innovative techniques are required to enable this optimization with approaches involving

BIST, output analysis methods and active test hardware.

Conventional VLC-ATE approaches typically use reduced resources at the cost of lower test coverage. Only a limited set of selective IP may be tested at wafer-sort stage if the entire DUT will be retested after packaging. Low-speed ATE capabilities at probe environment due to hardware limitations drive this constraint. Packaging costs and emergence of System in a Package (SiP) systems make this approach impractical for some applications.

Modern System on a Chip (SoC) may use SiP, flip-chip or stacked die packages which can cost a significant fraction of silicon fabrication. An escaped defect at wafer-sort, when screened at package test, results in added cost when the packaged part is discarded. SiP modules typically use a Known Good Die (KGD) approach [1]. If VLC-ATE test done at wafer-sort for one of the n die results in a test escape, the entire package with $n-1$ good die is discarded, with great cost implications.

BIST mechanisms to enable self-test involve an area overhead, resulting in additional silicon fabrication cost. Modern sub-100nm fabrication nodes have enabled progressively larger component densities, reducing silicon area per component and thus effectively reducing the fabrication cost per component. An approximate cost/transistor reduction of 29% is projected between successive techonology nodes [2], while the ATE test cost is expected to increase linearly per decade [1], independent of the process nodes being tested. This trend supports aggresive use of BIST schemes where the test resources can be lowered while marginally adding silicon area.

Functional testing is typically used to ensure test quality for mixed-signal modules. The stimulus and output observation requirements for such testing may not be provided by VLC-ATE. Design for Test (DFT) techniques further reduce test development time and cost, reducing the engineering overhead.

Semiconductor production test strategies need to optimize the test coverage and quality to align with the outgoing device quality requirements and cost constraints. This balance is further complicated for VLC-ATE, as the resources available to enable tests are limited in nature. The aim of this work is to achieve high test coverage and test quality while using VLC-ATE. Novel BIST methods combined with active test hardware and response shaping provide a converging ecosystem towards meeting this challenge. The multi-pronged approach is reviewed in detail in the following sections of this dissertation.

Figure 1.1 represents the high level summary of the approach towards providing a low-cost high-quality test solution for mixed signal devices.

BIST approaches involve fabricating stimulus generation and analysis capability on-chip. BIST reduces reliance on the ATE resources and can enable application specific stimulus generation. BIST modules may also be developed to selectively observe internal nodes of mixed signal circuits in order to infer the performance of the Circuit Under Test (CUT). On-chip stimulus generation schemes for ramp generation, quiescent current testing and internal circuit node access are discussed in the following sections.

BIST modules can also be combined with response shaping methods where the output response can be translated into a form compatible with VLC-ATE. Response shaping and post-processing reduce the output observation and analysis requirements for the VLC-ATE, enabling implementation of complex test algorithms. Stimulus conditioning methods are used to enable low cost signal generator modules for precision specification testing. Real time testing of Analog to Digital Converters (ADC), curve fitting algorithms and alternate test approaches for parametric analysis are proposed to reduce ATE response observation capabilities.

Test resource reduction can also be performed by loopback methods where DUT modules are combined to enable mutual test. Active loopback methods presented in this work enable discrimination of spectral artifacts in loopback environments.

This dissertation reviews the work towards enabling high quality/ low cost testing of mixed signal devices. Following sections cover individual methods in detail. Prior work and solutions are described for each of the methods, comparing the effectiveness of the methods described in this dissertation. Existing standard practices are described in detail with prevalent data to highlight the improvement seen with our methodology.

Our work is geared towards enabling a global test resource optimization over the current practices. While the innovative methods included approach testing differently, fundamental test quality matrices remain unchanged. Each of the BIST schemes are geared towards screening for random and systematic

defects. The coverage matrices provided in the later sections for each of the schemes include defects of any origin – the methods are designed to screen systematic failures introduced by design or process issues as well as statistically expected random defects.

The ADC BIST methology offers a solution to optimize the outgoing defects while using on-chip BIST – if no optimization is possible on a non-mature design or process, the reduced coverage can be disabled to perform a full ramp test on every device. While this does not use the complete optimization potential offered by the BIST, it still provides a significant improvement over a conventional ATE-ramp driven ADC test as no ATE resources are used for stimulus generation.

Vector based testing of ADC provides relaxed response storage and analysis criteria based on a functional vector formulated with the expected error. A functional vector with zero tolerance for DNL can be easily formulated if required by the ADC end application. As the complete ADC response is analyzed in the method, any random or systematic errors, including artifacts introduced by the ATE may be screened with this approach.

The PLL BIST methodolgy is an alternative approach to the existing PLL lock test that provides additional parametric coverage. The test quality matrix is improved by the virtue of this additional coverage and hence it includes a consistent quality improvement over the existing methods.

Post processing and input stimulus conditioning methods included in

this dissertation have a similar approach where the methodlogy provides a blanket coverage for random or systematic defects. While the input fidelity requirements are relaxed, output test quality remains consistent.

Fault models considered for the simulations included introduction of a single fault into the netlist, which is a superset of multi-fault models. Monte Carlo simulations performed with the single fault introduction are more aggressive w.r.t. multi-fault models and define the bounds for the multi-fault models. This provides additional confidence in the effectiveness of the results presented as any open loop system with multiple defects is easier to detect as compared to a single fault when similar test cases and conditions are used.

Semiconductor quality matrices define the defectivity at the time of test as well as through field use of the SoC. Semiconductor test needs to be geared towards ensuring continued circuit functionality and performance through the device life period. High Temperature Operating Life (HTOL) experiments are performed during silicon characterization where accelerated stress is applied on the DUT by operating the circuits at elevated voltage and temperature conditions. Parametric performance of the DUT is characterized prior to applying this HTOL stress and again redone after the stress duration. Any device that meets the performance criteria (operating voltage, specification frequency, jitter, signal-to-noise ration etc.) at the end of this experimental stress duration is deemed to be functional at the end of its field operating life. As some performance measurements may show degradation with HTOL, additional test margin may need to be added when the DUT is intially tested, so that the

degraded performance at the end of life cycle still meets or exceeds the criteria.

Covnentional tests may be used in order to characterize the DUT prior to and after applying HTOL stress. As the proposed schemes provides alternate and improved methods to test mixed signal modules, they can be easily used as a replacement to conventional methods for reliability validation. The characterization data obtained out of these schemes prior to HTOL stress will be guard-banded based on the parametric shifts seen, and final production criteria is finalized while accounting for the required specifications and this guardband. The methods and procedures include in the dissertation are interchangable with the conventional methods with improvements as the basic performance validation steps done on the ATE are comparable between the two approaches.

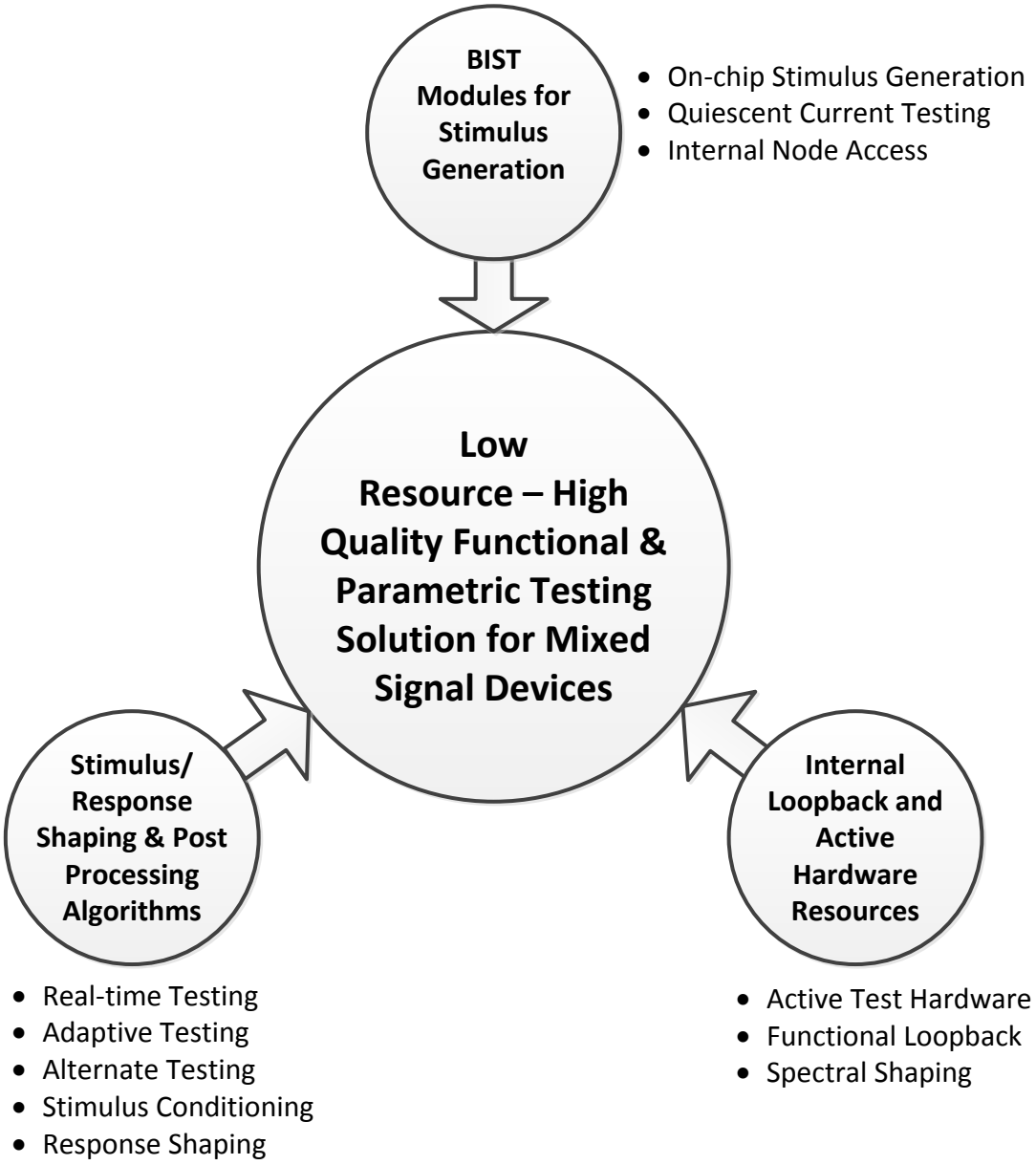

Figure 1.1: Converging Approaches to Enable Low Cost, High Quality Mixed Signal Production Testing

Chapter 2

On-Chip Stimulus Generation

Analog stimulus generation and response observation constraints in VLC-ATE limit their application for mixed signal testing. Mixed signal functional testing requires stimulus with precise temporal and/or spectral components which drives the requirements for precision hardware. On-chip sources need to comply with the stimulus specifications and need to be carefully designed to be accurate across a variety of operating and testing conditions.

Built-in ramp and triangle wave generator circuits have been a subject of research and a large number of solutions have been proposed [3, 4, 5, 6, 7, 8, 9]. While silicon area minimization is a typical concern with BIST modules, designing a BIST module for VLC-ATE requires careful consideration of voltage and clocking limitations of the test system. The stimulus generator is clocked with 50% duty cycle to reuse any Phase Locked Loop (PLL) or ATE clocks that may be available. A hybrid scheme is used to enable at-speed testing of output pads and paths. A full-scan enabled sceheme requires all the overhead bits to be shifted serially, increasing design timing closure and ATE observation frequency requirements. Figure 2.1 represents the approach where on-chip stimulus generation capability is used to reduce ATE dependence.

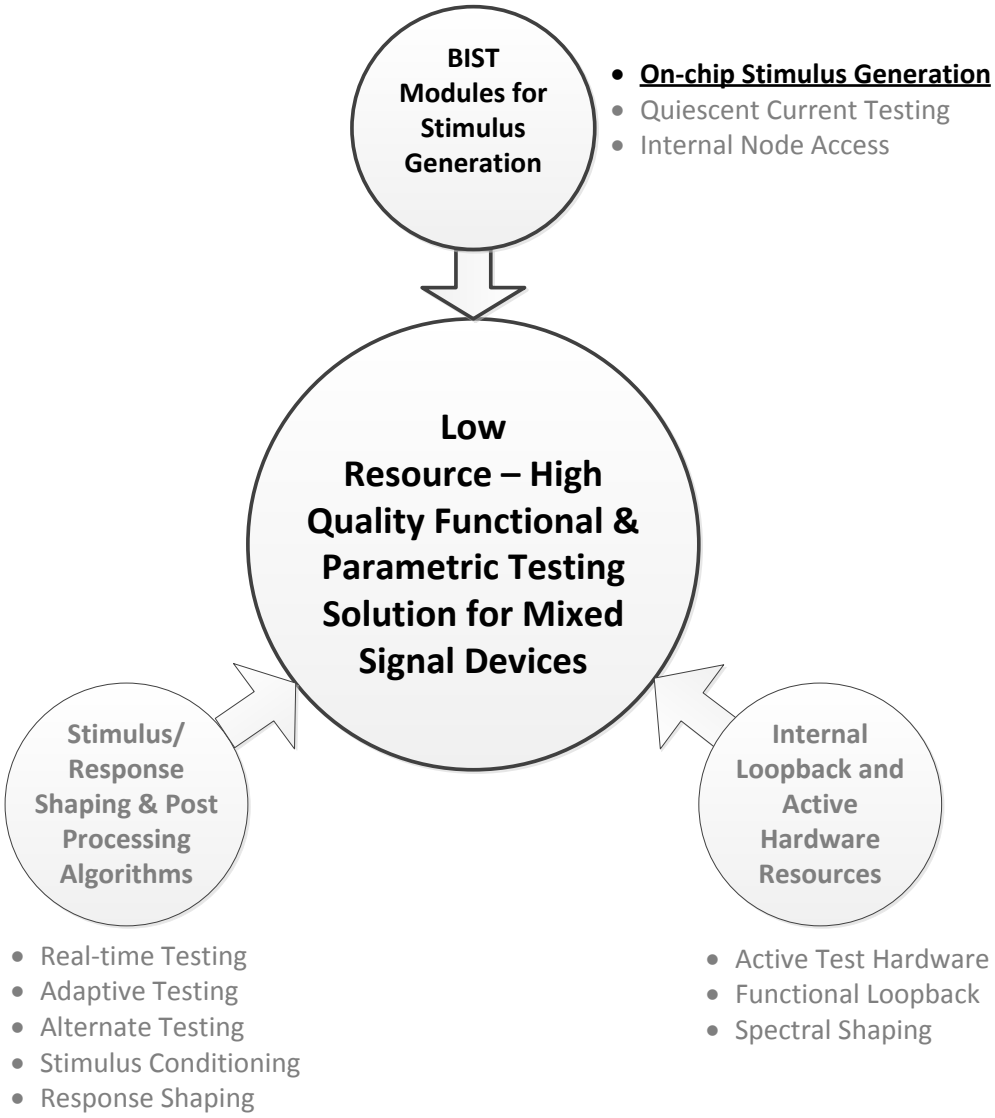

Figure 2.1: BIST with On-Chip Stimulus Generation

2.1 On-Chip Stimulus Generator

A ramp input with a well characterized linear slope can be used effectively for production testing of an ADC with either a histogram or the real-time

code analysis method discussed later in this dissertation. Multiple ramp generation schemes have been proposed in the past [3, 5, 9] with corresponding trade-offs. Robustness to process variation is a crucial factor addressed in this work which is necessary to make the BIST scheme manufacturable. External resource requirements for the BIST module also needs to be minimized to ensure compatibility with VLC-ATE.

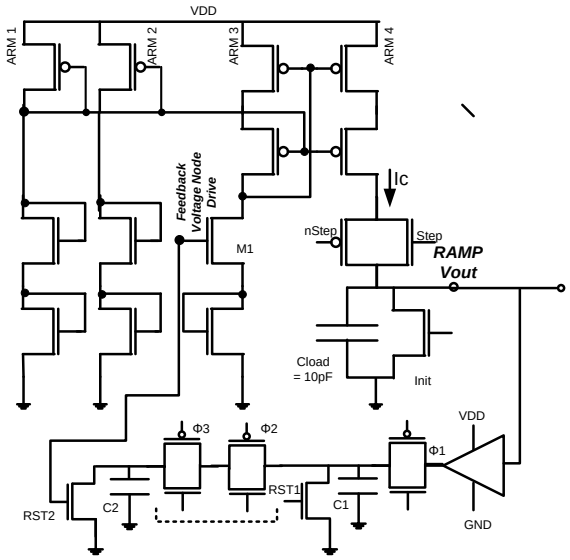

Figure 2.2: Constant Current Source with Feedback Mechanism for Constant Current Capacitor Charging

2.1.1 Effect of Process Variation

The basic ramp generator involves an ideal constant current source feeding an ideal capacitor in series. An exact charging current i_{charge} and load capacitance value would be required to ensure a constant-slope, constant-period ramp out of this topology. If 0 V to VDD is the input swing spec for the ADC, the input ramp should reach VDD at an exact time period t' for each cycle with a linear slope in the entire duration. Process variation affects the ramp slope and linearity, making this basic stimulus generator of very limited use for mass production testing.

Constant current charging of a capacitor C linearly increases the voltage across the plates – any process variation causing a change in capacitance inversely affects the ramp voltage slope. Similarly, any variation in the current drive of the charging circuit affects the charging time.

$$C = \frac{Q}{V} \tag{2.1}$$

$$\Rightarrow V_{cap} \alpha \frac{1}{C} \tag{2.2}$$

hence,

$$\delta V_{Cap} \alpha \frac{1}{\delta C} \tag{2.3}$$

Monte Carlo simulations across process corners clearly indicate that a very precise process target is required to maintain required ramp slope for a basic ramp generator. A feedback scheme is required for controllability of the ramp. A variable feedback which can maintain a constant voltage ramp slope

for any process variation in the capacitor or the current source is required to enable compatibility with process variation. The feedback is required to be dynamic to ensure linear operation in the presence of any load or line variations.

Multiple schemes have been proposed for feedback [7, 9] which use a feedback path to control bias current depending on mid-cycle samples from the ramp voltage. Limited duty cycle latches are used in [7] to control charging and discharging of a capacitor. The feedback scheme used in the implementation is included in the Figure 2.2. Advantages of the topology used are covered later in this section.

2.1.2 Feedback Mechanism for Process Independence

A clocked comparator is used to compare the ramp output with $\frac{VDD}{2}$ at $\frac{T_{per}}{2}$ where T_{per} is the ramp period. Transistor M_1 in Figure 2.2 is used to reset capacitor C_1. C_1 is used as per-cycle-charge-storage for the comparator output. Charging conditions for the capacitor C_1 are defined as –

$$If\ V_{ramp} < \frac{VDD}{2} \text{ at } \frac{T_{per}}{2},$$
$$V_{C1} = VDD \text{ else } V_{C1} = 0V$$

Latches L_2 and L_3 are toggled by an offset clock to limit the conductive phase of the combination latch –

$$\Phi_3 = \Phi_1 \cap \Phi_2 \tag{2.4}$$

This offset phase Φ_3 is generated out of an oversized gate delay and no additional clocking source is required. When L_2 and L_3 conduct, capacitors C_1 and C_2 in Figure 2.2 are connected in parallel and a charge sharing current flows to equalize the voltage across each capacitor.

$$I_{charge-sharing} = \frac{d}{dt}\left[\frac{v1 - v2}{c1 + c2}\right] \tag{2.5}$$

Voltage across capacitor C_2 is used to change the bias current in the constant current source – if the $V_{ramp} < V_{ref}$ at $\frac{Tper}{2}$, C_1 will charge C_2 to a higher voltage value while for $V_{ramp} > V_{ref}$ at $\frac{Tper}{2}$, C_1 being at $0V$, will partially discharge C_2, lowering the effective voltage across C_2. A reduction in voltage across C_2 results in a lower gate bias for the current mirror, reducing load charging current. Settling time for the ramp generator needs to be optimized as ADC test can not begin until a consistent ramp slope is obtained. Using wide transistors for latches L_2 and L_3 enables rapid charge sharing between C_1 and C_2 due to increased conductivity. It would also result in V_{ramp} overshoot and undershoot as excessive correction bias may be applied to the constant current source. Transistor widths for L_2 and L_3 are thus optimized to stabilize V_{ramp} in approximately 6-7 cycles.

The current mirror circuit is implemented using semi-telescopic topology and a capacitive load C_1 is charged linearly using this current source. Feedback circuit adjusts the gate bias for transistor M_1 per cycle to ensure that V_{out} reaches $\frac{VDD}{2}$ value at time $\frac{Tper}{2}$. The feedback scheme ensures a dynamic process-corner-independent stable operation providing positive or negative feedback which is determined by the results from the previous cycle.

2.2 Scanable Interval Counter

A digital counter that shares synchronous clocking with the ramp generator is used as an interval counter in the BIST scheme. The interval counter acts as an accurate approximation of the ramp stimulus as clocking resources are synchronous. It provides a timing reference and the code-width is optimized to provide adequate resolution without excessive silicon or timing overhead.

A scan enabled 4-bit counter effectively provides one timing anchor for each 2^8-bits of ADC output. Increasing the counter width provides additional timing anchors, effectively resulting in more accurate Differential Non Linearity (DNL) calculations at the cost of area overhead. A higher counter width also increases silicon area and timing scan overhead; therefore counter width needs to be optimized.

2.3 Hybrid BIST Scheme

The ADC output is routed to the output pads and observed using a functional pattern. A full scannable scheme for ADC test requires the entire code width to be output and scanned out at-speed, which may not be feasible for a typical low cost ATE. For an n-bit code width ADC rated at $f_{operational}$, the required synchronous data transfer rate is represented as –

$$R_{sync} = f_{opr} \times W_{code} + f_{opr} \times W_{int-counter} + T_{overhead} \tag{2.6}$$

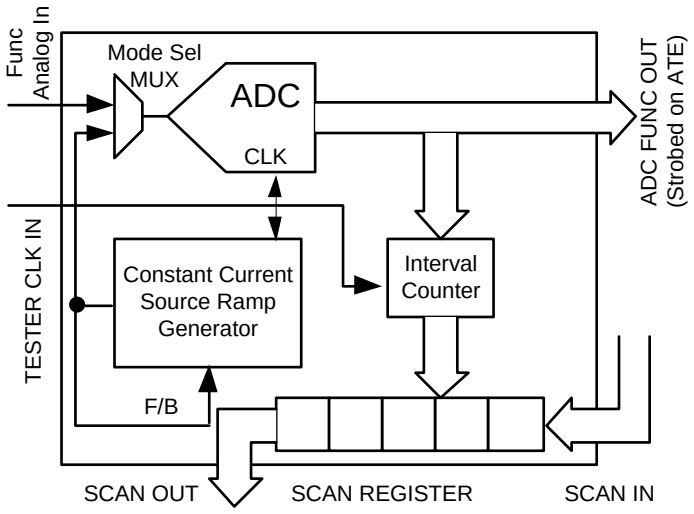

Figure 2.3: System Level Schematic for Hybrid BIST Scheme

A typical 12-bit ADC with sampling at 25MHz with a 4-bit interval counter would result in a synchronous scan requirement of 400MHz, significantly higher than the 25MHz scan limit. Such a high frequency requirement in the digital block may also cause strict timing closure constraints. Running the ADC slower than the rated speed would compromise test quality while it may limit the data scan rates to fit within the ATE data rate.

The hybrid scheme is shown in Figure 2.3. This may be applicable to SoC or SiP systems where the ADC output is accessible either as dedicated outputs or muxed in a test mode. The overall error factor due to added noise

is represented as follows –

$$\epsilon_{total} = \epsilon_{ADC-inherent} + \epsilon_{ramp-stimulus} + \epsilon_{system} \tag{2.7}$$

The inherent ADC errors are not analyzed in detail as their intrinsic values and probabilities can be assumed to be unchanged in the BIST scheme. Providing an internal stimulus and observing digital output nodes ensures that the $\epsilon_{ADC-inherent}$ estimate is very close to the ADC intrinsic error. Factors $\epsilon_{ramp-stimulus}$ and ϵ_{system} may encounter catastrophic errors in the presence of fabrication defects but any errors which cause $\epsilon_{ramp-stimulus}$ and ϵ_{system} to be equal to 1 are very easily detected by observing the ADC outputs with a functional pattern. The additional circuitry including the interval counter and scan register is digital in nature and is not be affected by noise as long as clean clocks are used to drive the blocks and setup/hold constraints are met. Therefore, $\epsilon_{ramp-stimulus}$ is the dominant component of the injected noise. The ramp generator error can be further classified into two components – waveform inherent errors in form of Integral Non Linearity (INL) and DNL and noise added due to feedback mechanism. Switching noise added by the voltage feedback scheme is added to the ramp voltage peak noise. Feedback transmission gate width is optimized to ensure that the ramp peak noise present is within acceptable limits.

$$N_{total} = \int_0^T [N_{INL} + N_{DNL} + N_{Ramp-Slope}] \tag{2.8}$$

where,

$$N_{Ramp-Slope} = f[fab - corner, XstorW/L, C_{out}] \tag{2.9}$$

The ADC testing is performed in a specialized test mode which can run concurrently along with other tests due to its resource independence in production test. An initialization signal is provided to the ramp generator by the test mode controller and the functional clocks are gated to the ADC, ramp generator and interval-counter. A functional pattern is designed to observe the ADC and interval counter outputs in test mode. The functional pattern observing these nodes is designed to enable data capture for performing Bit Error Rate (BER) calculations to observe INL and DNL errors.

The hybrid BIST scheme is implemented using a $90nm$ CMOS library. Multiple iterations of SPICE simulations were performed to minimize the capacitor values in the ramp generator feedback path to reduce the area overhead. A smaller feedback capacitor requires a smaller trickle charge current and would reduce the fabrication area at the cost of a marginally larger output V_{max} variation. A smaller capacitive load also enables smaller $\frac{W}{L}$ ratios for the charging circuit. Table 2.1 contains the result summary for Monte Carlo simulations performed at the three process corners. The tight distributions for ramp voltage values and CpK (Process Capability) numbers indicate robustness to process variations.

This BIST scheme enables use of VLC-ATE while adding a moderate area overhead. Hybrid nature of the methodology enables at-speed testing using built-in stimulus while using low-end external test resources. The interval

Table 2.1: System Level Post Layout Simulation Results

Time	**Bin.Code**	**Ramp Voltage**(Med.)	**Std Dev**	**CpK**
0	0000	0.003 V	0.22mV	12.24
$\frac{1}{4} \times T_{per}$	0100	0.2764 V	0.16mV	8.45
$\frac{1}{2} \times T_{per}$	1000	0.5513 V	0.09mV	7.45
$\frac{3}{4} \times T_{per}$	1100	0.8248 V	0.12mV	9.32
T_{per}	1111	1.0996 V	0.04mV	21.78

counter along with sequential analysis method can provide data required to completely characterize the ADC.

2.4 Improvements Over Existing Work

Built-in ramp and triangle wave generator circuits have been a subject of research for last few decades and a large number of solutions have been proposed [3, 4, 5, 6, 7, 8, 9]. The stimulus generation scheme is directed at optimizing silicon overhead as well as considering the voltage and clocking limitations of low cost ATE. Ramp generation scheme proposed in [9] is robust for process variation but requires a negative voltage supply available on the DUT which is very rare for modern System on a Chip (SoC) and System in a Package (SiP) systems. A single positive supply is used for all components with a total of two differential clocks - a 50 percent duty cycle PLL-generated clock may be produced on most low-cost ATE at the required high frequencies. Using phase-shifted limited duty cycle clocks may require greater system resources and may not be within the capabilities of a typical low cost ATE. Use

of real-time code analysis method is a notable improvement for reducing test time window and system memory requirements over the existing methods used. The interval-counter which can be shifted out of a scanable register and is used for the characterization calculations, which an improvement over the currently used methologies. This counter indicates the estimated instantaneous input stimulus value which is essential to perform accurate INL/DNL calculations on ATE with limited computing resources. A hybrid scheme is used as against a fully-scanable scheme as explained in [9] to enable at-speed testing of output pads and paths. This enables at-speed functional testing which may not be feasible for a full-scan scheme while adding topology limitations. A full-scan scheme requires all the data and the overhead bits to be shifted serially, increasing the frequency requirements of the ATE. A Digital Signal Processor (DSP) based approach is not considered unlike earlier work [9], as an on-chip DSP is less likely to be available for most of the modern DUTs. Analog blocks are increasingly common on digital Application Specific Integrated Circuits (ASICs) and SiP where access to DSP cores may not be available.

This approach gives versatility to the BiST scheme, making it portable for a range of ADC IP as well as VLC-ATE configurations. The low-coverage spot check testing, which involves providing a DC input to the ADC to check its instantaneous output can provide cost savings for testing multiple types of ADCs but is not compatible with delta-sigma ADCs where a monotonic input signal rising to any predetermined level is required.

Chapter 3

Vector Based Sequential ADC Testing

While intput stimulus requirements for ADC test can be met by the BIST stimulus generator discussed in the previous section, conventional output response analysis methods are commonly used for ADC testing. These legacy methods, such as the histrogram method [5, 6, 9, 10, 11, 12] provide required test coverage at the cost of additional test time and processing resources. The histogram test metholodology for ADC testing involves applying a slow ramp stimulus to the ADC input for multiple ramp cycles and recording the output response which is then represented as a histogram for analysis. Various linearity test parameters are calculated from the histrogram representation and are used as the screening criteria. Histogram analysis method requires ATE memory and computational resources to calculate the INL and DNL values from the measured ADC output data. The measured output codes are stored in the memory while the data collection for the repeated ramp signal is completed. This stored data is processed to extract the parametric specification values.

The real-time-code-analysis method discussed in this section observes ADC response using a functional vector which is formulated using the ADC

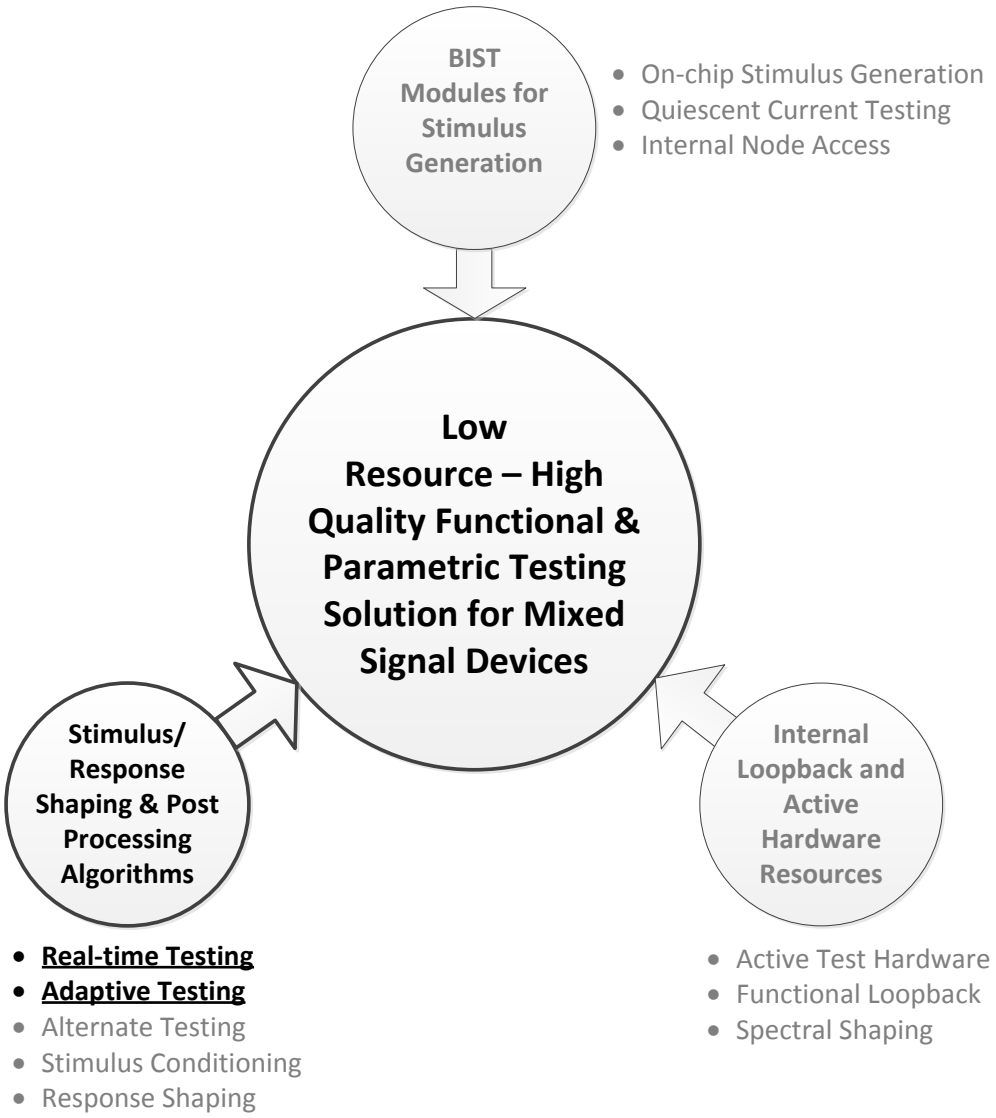

Figure 3.1: Vector Based Real Time Response Analysis

parametric linearity test criteria. The vector based approach reduces memory and processing constraints for the ATE while providing an output test quality

identical to the conventional histogram method. The approach is represented in Figure 3.1 where real time and adaptive testing principles are applied to enable vector based testing with existing ATE resources.

Use of VLC-ATE requires novel approaches for DUT response capture and analysis to minimize resource requirements while maintaining the same coverage and quality of conventional high-resource methodologies. The vector based ADC sequential test methodology is directed at using lower computational and memory resources of the ATE. The approach enables the use of VLC-ATE for response capture and enables test decision making by real-time output observation with an ATE functional pattern. The sequential test methodology offers lower test time as well as relaxed memory and processing requirements for the ATE.

The various parameters used to characterize ADC performance can be translated in terms of a digital functional pattern and the analysis is covered later in this section.

This scheme is compatible with ADC configuration where n-bit ADC outputs may or may not have external access. If the ADC nodes are not externally accessible, a scan enabled scheme can be implemented to scan out the ADC output – this serial data stream can be observed and compared against the functional pattern constraints.

3.1 Functional Testing and Analysis of ADC

ADC linearity response is characterized by parameters such as INL, DNL, voltage offset and gain. Signicant test resources are used for measuring these parameters during ADC test and therefore efficient capture methods have been a topic of research [12, 13, 14, 15]. Efficient methods to calculate these with minimal BIST area overhead and test time have been proposed [13], almost all relying on the histogram method. A histogram test method involves providing a characterized input signal *(ramp, sinusoid etc.)* with data padding provided at the V_{min} and V_{max} range extremes of the ADC. Multiple repeated instances of the input waveform are applied to the DUT and the resulting output measurements are represented as a histogram for further analysis. Histogram method of ADC analysis uses ATE memory to store the output code samples collected from the DUT and the ATE computing resources are used to perform analysis. This requires adequate storage memory and computing power in the ATE to minimize test time overheads.

Complete characterization of an ADC typically involves computing the following parameters by post processing the output data represented as a histogram. An ideal ADC transfer function contains a uniform distribution of histogram bins for a linear input signal provided. The distribution contains regularity defects in case of a practical ADC causing a non-uniform histogram.

If $H(i)$ represents the i^{th} output code of the ADC, the following expressions are used for calculating linearity test parameters –

DNL: DNL is defined as the relative difference between the observed and ideal code counts [15, 16]:

$$DNL(i) = \frac{H(i) - H_(ideal)}{H_{ideal}} \tag{3.1}$$

When observed in terms of the ADC output response to a linear ramp input, it can be defined as the difference between the actual step width and the value of 1 Least Significant Bit (LSB). A DNL error specification is typically defined to be $\leq$1 LSB to ensure a monotonic transfer function with no missing codes. The ADC output should increase or remain constant for an increasing input signal.

INL: INL is represented as the cumulative sum of the DNL values processed for all preceding output codes [16]:

$$INL(i) = \sum_{j=1}^{i} DNL(j) \tag{3.2}$$

The INL value is used as a measure of ADC response linearity. It is the deviation of the output code from the ideal code value in terms of LSB or Full Scale Range (FSR). The ideal ADC transfer function is linear with axial intercepts at $(0, 0)$ and (max_code, max_in) corners, any deviation of these transfer function end points results in an offset at intermediate codes, captured by INL calculation.

Offset: Offset represents the deviation of the ADC response curve from the ideal response in terms of the LSB count of the ADC [15, 16]:

$$Offset = \frac{H(2^n) - H(1)}{2 \times H_{ideal}} \tag{3.3}$$

Gain: Gain is the ratio between measurement count of any non-extreme (min or max on full scale input) code $H(i)$ and the ideal code count of H_{ideal}. The extreme codes are not considered, as typically additional input points are provided at the extreme ends of the range to ensure complete input range sweep.

$$Gain = \frac{H_{ideal}}{H(i)} \tag{3.4}$$

As mentioned earlier, regularity defects affect output code distributions and therefore a cumulative $Gain$ is computed for n points around the center code [15, 16] –

$$Gain^{-1} = \frac{\sum_{i=N1}^{N2} H(i)}{n.H_{ideal}} \tag{3.5}$$

The following terms are used with reference to ADC test methods:

Sampling Frequency (f_s): It is the clock frequency provided to the ADC. An output code is generated every $\frac{1}{f_s}$ seconds by the ADC.

Hits Per Code: Hits per code (HPC) is the number of outputs generated for each output code level in the test window. If test stimulus is a linear ramp signal, an n-bit ADC test with $HPC = k$ will have input stimulus adjusted to transit from code [0...0] to [1...1] in $\frac{k}{f_s} \times 2^n$ seconds.

3.2 Translating ADC Output Codes to Parameters

Digital vectors are widely used for structural and functional testing of digital devices. These vectors typically contain the driven input data as well as checks for observing the circuit output response. The edge timing information for driving and receiving data is defined separately and the vector can be programmed to observe an output node in a specified time window.

Consider an n-bit ADC operating at a sampling frequency of f_{opr}. The ADC sampling frequency corresponds to the ADC clocking frequency. An n-bit digital output code is converted every $\frac{1}{f_{opr}}$ seconds. If $HPC = 1$ for the input ramp stimulus, the ideal response distribution is shown in Figure 3.2–(a), where the ramp input is superimposed on the output step waveform. The sampling instance falls at the exact center of the output step in the ideal case. For an ideal ADC, each output code has a cardinal relationship with a specific point on the input ramp which is repeatable in nature. For a practical and functional ADC with $HPC = 1$, the code-center distribution can be assumed to be Gaussian in nature as seen in Figure 3.2. Case (a) in the Figure 3.2 represents an error-free DUT response distribution where the code center has a tight distribution ($CpK \geq 1.3$) and case (b) where the outlier points in the code distribution, shaded in Figure, fall under adjacent bins, resulting in a non-zero DNL error.

The Gaussian distribution shown in Figure 3.2 can be represented in terms of DNL if the timing variation for the code center is characterized.

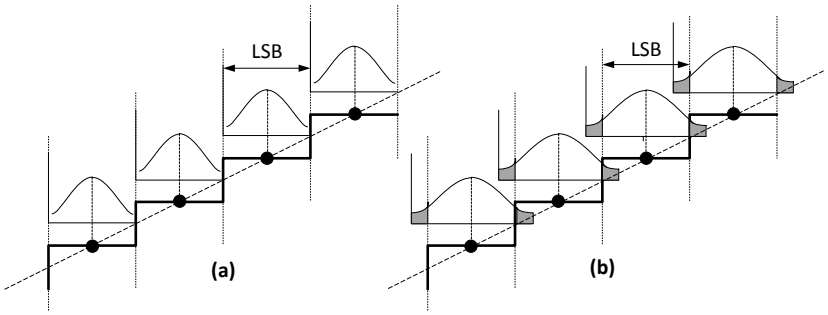

Figure 3.2: $HPC = 1$ Test Case with Ideal and Erroneous Code Center Distributions

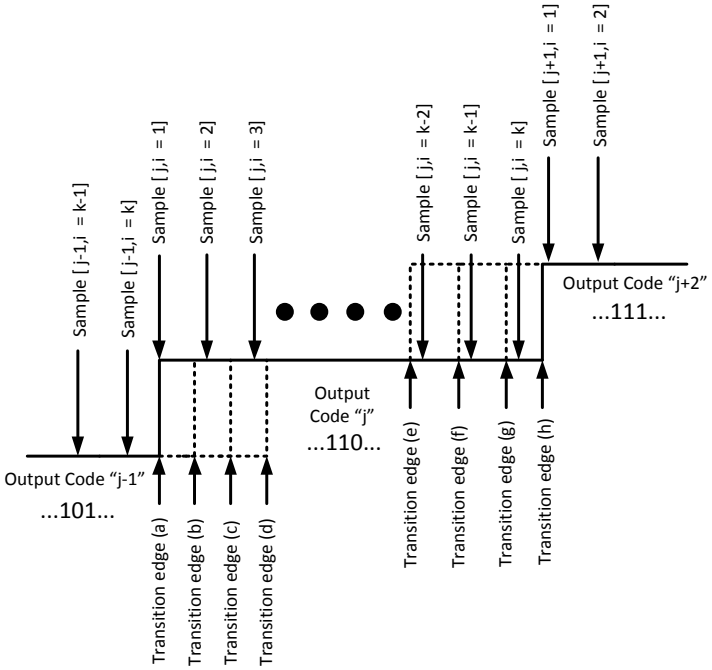

Figure 3.3: ADC Output Step Transition with $HPC = k$

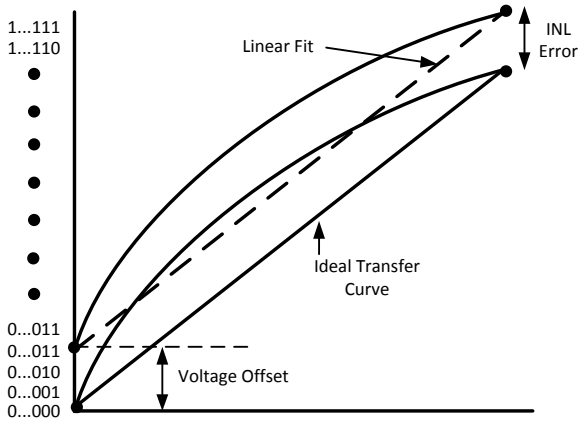

Figure 3.4: ADC Output Step Transition with $HPC = k$

All practical ADC tests involve HPC values which are greater than 1, $HPC = k$ results in k output codes generated per output level, each separated by $\frac{1}{f_s \times k}$ in time.

For an ADC clocked at a frequency f_s with $HPC = k$, the *one-to-many* relationship between the output codes and the corresponding instantaneous input ramp values can be represented as –

$$Ramp[i] \leftrightarrow ADC_{out}[j] \tag{3.6}$$

for $i = t'$ to $t' + \frac{1}{f_s} \times k$

Figure 3.3 shows three successive output levels $j-1$, j and $j+1$ observed. The ideal code duration per ADC output step is $\frac{1}{k \times f_s}$, as discussed earlier. The edge transitions between output levels at ideal and non-ideal in-

Table 3.1: Test Case for Ideal ADC Response for Steps in Figure 3.3

Digital Compare Vector									
Sample $[j-1, i=1]$:	.	.	.	1	0	1	.	.	.
Repeated k times total									
Sample $[j-1, i=k]$:	.	.	.	1	0	1	.	.	.
Sample $[j, i=1]$:	.	.	.	1	1	0	.	.	.
Repeated k times total									
Sample $[j, i=k]$:	.	.	.	1	1	0	.	.	.
Sample $[j+1, i=1]$:	.	.	.	1	1	1	.	.	.
Repeated k times total									
Sample $[j+1, i=k]$:	.	.	.	1	1	1	.	.	.

stances are noted by transition edges (a,...,h). Samples ($i = 1, ..., k$) denotes the k hits per code.

3.2.1 Translating DNL Errors to a Functional Vector

For an ideal ADC with 0 LSB DNL error, the probability of error function for any recorded sample is –

$$P_\epsilon[l, m, 0/1] = 0 \tag{3.7}$$

where,

$l = 0$ to 2^n,

$m = 0$ to n,

$0 \rightarrow$ Error when ideal bit value is 0,

$1 \rightarrow$ Error when ideal bit value is 1.

Table 3.2: DNL Errors Corresponding to DNL Transitions

Transition Edges	**Effective DNL Value**
$(a), (h)$	$0 \times LSB$
$(b), (h)$	$\frac{1}{k} \times LSB$
$(c), (h)$	$\frac{2}{k} \times LSB$
$(a), (e)$	$\frac{2}{k} \times LSB$
$(b), (e)$	$\frac{3+1}{k} \times LSB$
$(c), (e)$	$\frac{2+3}{k} \times LSB$

For the ideal case mentioned above, a functional pattern used to observe the ideal $3 \times k$ output samples for codes [...101..., ...110..., ...111...] is represented in Table 3.1, where 0→(Expecting digit 0) and 1→(Expecting digit 1).

The ideal step transition would result in transition edge (a) for [...101...→...110...] and transition edge (h) for [...110...→...111...], with $DNL = 0$.

A practical ADC test situation involves a non-zero DNL and a maximum limit is allowed for the measured DNL value if the DUT is to be categorized as acceptable.

If the [...101...→...110...] transition follows the edge (b), the sampled output $[j, i = 1]$ reads a [...101...] instead of the expected ideal [...110...]. The sampled output $[j, i = 2]$ still represents the ideal expected code output value [...110...].

The DNL error observed in this case is $\frac{1}{f_s \times k}$ seconds, or $\frac{1}{k} \times LSB$.

The DNL errors corresponding to some of the transition edge combinations are represented in Table 3.2

If the DNL value of $\frac{1}{k} \times LSB$ is accepted as the error allowance, the functional test pattern can be modified to accommodate *"don't care" or "X"* symbols where the observed output bit is discarded and not used for decision making.

The vector line corresponding to sample $[j, i = 1]$ is therefore changed from [...110...] to $[...1XX...]$; DNL errors thus can be translated into the compare bits in functional patterns. The changes in the bit compare values are represented in Table 3.3 as compared to Table 3.1.

3.2.2 Translating INL Errors to a Functional Vector

INL errors are ADC response linearity errors, either with or without an initial voltage offset, as seen in Figure 3.4. The functional vector discussed earlier covers detection of INL errors as any non-linear transfer curve shift results in an adjacent code being erroneously generated at the ADC output and depending on the $l \times LSB$ error margin limit added while generating the vector, a device with excessive INL error can be screened.

The predetermined INL spec is thus coded into the test vector allowing an error margin to comply with the specification requirements.

Table 3.3: Test Case for Practical ADC Response with $\frac{2}{k} \times LSB$ DNL Allowance

Digital Compare Vector									
Sample $[j-1, i=1]$:	.	.	.	1	0	X	.	.	.
Sample $[j-1, i=2]$:	.	.	.	1	0	1	.	.	.
Repeated k times total									
Sample $[j-1, i=k-1]$:	.	.	.	1	0	1	.	.	.
Sample $[j-1, i=k]$:	.	.	.	1	X	X	.	.	.
Sample $[j, i=1]$:	.	.	.	1	X	X	.	.	.
Sample $[j, i=2]$:	.	.	.	1	1	0	.	.	.
Repeated k times total									
Sample $[j, i=k-1]$:	.	.	.	1	1	0	.	.	.
Sample $[j, i=k]$:	.	.	.	1	X	X	.	.	.
Sample $[j+1, i=1]$:	.	.	.	1	X	X	.	.	.
Sample $[j+1, i=2]$:	.	.	.	1	1	1	.	.	.
Repeated k times total									
Sample $[j+1, i=k]$:	.	.	.	1	1	1	.	.	.

3.2.3 Translating Voltage Offset Errors

Similar screening can be done for the voltage offset. If a 1-bit LSB offset is permitted by the specification, the first ADC output vector can be compared against $[...000X]$, where 'X' denotes a *"don't care"* compare operation. Similar offset can be screened at V_{max}, where the ADC output code is expected to be $[1...1]$ but can be checked against $[1...1X]$.

3.3 Correlation with Experimental Results

The validity and fault coverage for this vector based approach is verified on a practical production test program used to test a 90nm ASIC on a *HP-93000* ATE. The production test program uses a conventional histogram method for analyzing the ADC response. A slow input voltage ramp, generated by the ATE is fed to the ADC input. The input ramp goes 6% above and below the ADC supply rail value to ensure all the output combinations are covered by the input ramp range.

The overshoot and undershoot section of the input ramp waveform tests the ADC performance to ensure that no glitches occur if the input exceeds the rail-to-rail voltage range. The ADC output does not maintain cardinality for out-of-range input ramp values; these values are lumped into codes corresponding to 0 and V_{max}.

$$\Psi_{Undershoot} = \{n | n \in 0\} \tag{3.8}$$

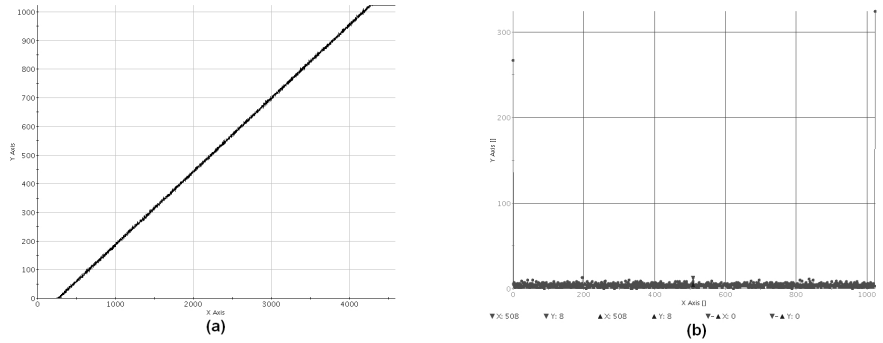

Figure 3.5: ATE Results: ADC Output Step Transition with $HPC = 16$

for the inductive set 0.

$$\Psi_{Overshoot} = \{n | n \in Code_{max}\} \tag{3.9}$$

for the inductive set $Code_{max}$.

The DUT is operated in 10-bit mode and is tested for full resolution. HPC value is set 16 while sampling frequency for the ADC is set at $48kHz$.

The input signal ramp supplied and the resulting observed histogram is included in Figure 3.5. Figure 3.5–(a) represents the input ramp signal provided while Figure 3.5–(b) represents the calculated histogram on the ATE. ADC output data stream is collected for a passing as well as a marginal failing device to observe the bit locations that cause the failure. The motivation for selecting a marginal failure over a catastrophic failure (causing either a output stuck-at fault or a dead output response) was that a marginal failure may not significantly affect the nature of the histogram, minimally affecting the DNL

and is more difficult to screen out as compared to a catastrophic failure.

The measured parameter values for the marginal part are presented in Table 3.4. Typically average values are considered for HPC/DNL/INL screen in the histogram method and the use of average value may be mask localized marginalities – as the parameters are averaged for the entire code width, a single marginal measurement may get averaged and become non-distinguishable.

The recorded data stream is processed with a script to emulate the use of a functional pattern. The error margin in the functional pattern is based on the use of *"don't care"* compare operations to not compare the leading and trailing samples per bit for the specific bit transition associated with the vector. By setting the HPC_{lower} limit at 15, the marginal DUT could be screened with the functional pattern.

Vector based ADC testing can be a feasible alternative to the conventional histogram method to reduce ATE memory and data processing requirements. As the vector based approach screens for output data marginalities per cycle, no averaging artifacts which may cause error masking are present. The specification values for various ADC parameters are coded into the functional vector during the vector-generation phase. This also demonstrates the compatibility of the functional test vector approach to ADC test with the ATE results obtained for a conventional histogram test. The scheme can also be used with any deterministic non-linear inputs such as a sine wave wtih reformulation of the functional vectors.

Table 3.4: Calculated Parameters for Marginal DUT

Parameter	**Calculated Value**
INL	$-2.941(Min), 2.172(Max)$
DNL	$-1.00(Min), 1.81(Max)$
Gain	2.20
Offset	-2.875
Avg. HPC	14.9138

3.4 Improvements Over Existing Work

Histogram method to capture and analyze ADC output is the most commonly used procedure to characterize linearity parameters of an ADC. While a lot of research has been done in the area of generating stimuli on-chip, most of the methods proposed and validated in [10, 5, 6, 9, 11, 12] use variants of this method.

Method proposed in [10] reviews the code density analysis of the histogram test methodology where a variety of input stimulii are reviewed. It decomposes the temporal and spectral components for analysis and analyzes them to come up with application specific test solutions. Results presented are limited to successive approximation ADC's and while test time reduction is estimated, this represents a marginal improvement over the existing code density/histogram method.

Work in [11] proposes a consolidated spectral and histogram test methodolgy where matrix manipulation is performed as post-processing on the cap-

tured data. While this adds additional coverage for spectral performance, the linearity/temporal test coverage and complexity remains unchanged.

The work reviewed in this sections provides significant improvements over the histogram method by enabling real-time testing of ADCs using functional patterns. This reduces overall test time window and system memory/processing requirements, supporting use of VLC-ATE resources for performing temporal testing of ADCs.

Chapter 4

Real-Time Dynamic Hybrid BIST

Comprehensive functional tests to find all detectable faults require a long test time which results in a prohibitive cost. Real time data analysis methods are used in digital testing and are combined with statistical tools, to optimize the test cost and Defective Parts Per Million (DPPM) by real-time analysis. BIST scheme reviewed in this section is compatible with adaptive methods to optimize test time in production environments while controlling the outgoing defective devices. The hybrid BIST scheme enables complete ramp testing and reduced coverage testing with VLC-ATE with a BIST mode. Figure 4.1 represents the components of this scheme where on-chip stimulus generation schemes are combined with statistical calculation resources on ATE in order to create a dynamic test scheme.

Dynamic test flows are increasingly used in digital semiconductor production testing to optimize the test costs and DPPM requirements for the target application [17, 18]. This approach includes testing the overall population with a reduced-coverage test with lower test time while a pre-determined number of samples of DUT are tested with the full-coverage test with high test time. Statistics are collected on those sampled DUTs and real time deci-

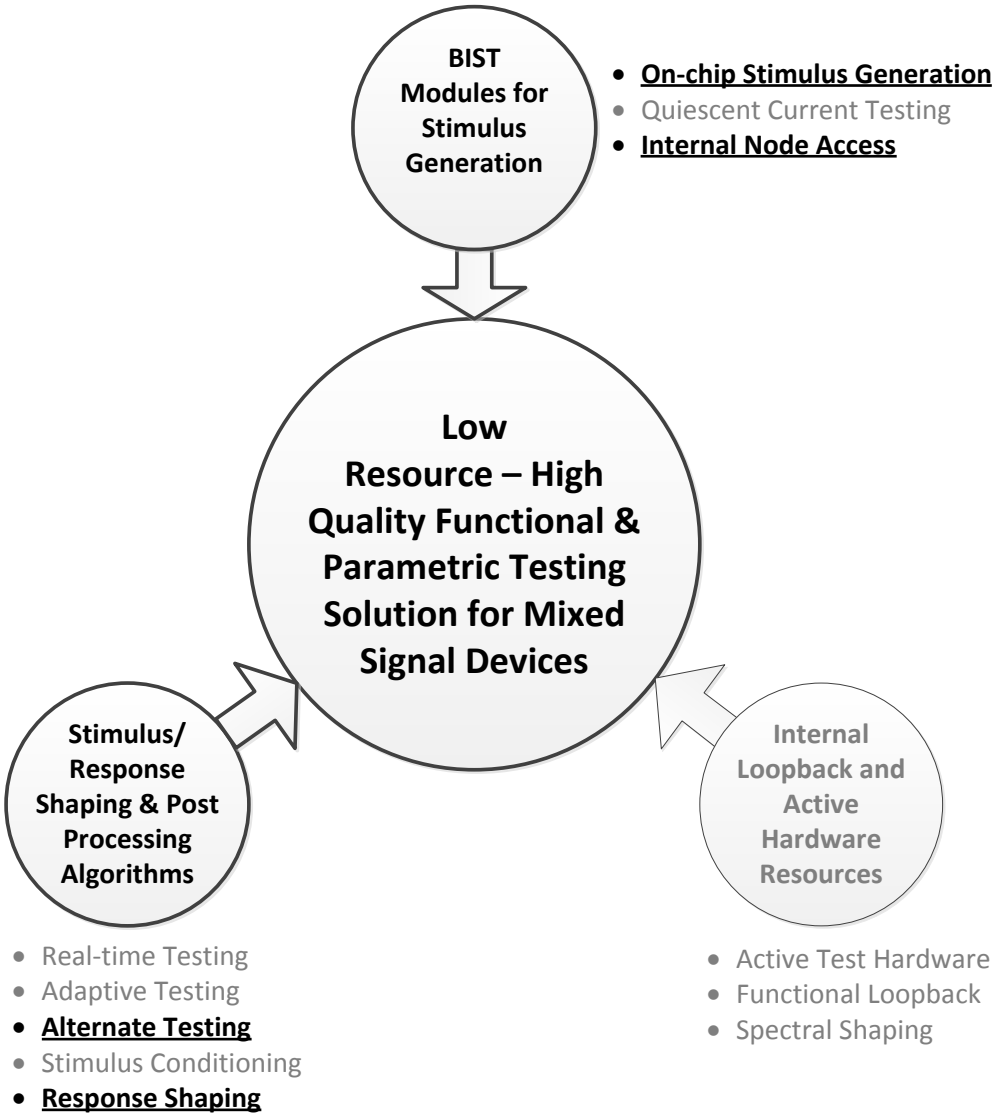

Figure 4.1: Adaptive BIST Schedule with Compatibility with Real Time Testing

sions are taken by the tools to run the full coverage test if the DPPM value is beyond the acceptable range. In case of digital patterns, the DPPM value is considered, while for analog tests where parametric measurements are required, measurement distributions may be observed by this external tool. This approach can be easily applied when mixed signal circuits are tested using a regular full-functionality tester, as a variety of stimuli can be programmed on the ATE. Ability to support high and low coverage stimuli gives versatility to the BIST scheme, making it portable for a range of ADC IP across VLC-ATE configurations.

A gross fabrication defect present in the ADC module is likely to cause a catastrophic failure of the ADC, affecting multiple output code combinations.

$$f(v1_{analog}) \overset{ADC}{\rightarrow} C[r, n] \tag{4.1}$$

where,

r: Output code range 2^n for an $n - bit$ ADC.

n: Code width in bits.

This cardinal functional relationship between ADC inputs and outputs is violated for multiple output codes in case of a catastrophic failure.

A spot-check or a code-offset test can be used to detect such catastrophic failures. This approach involves applying a fixed DC voltage level to the ADC and observing the ADC output. ADC transfer function is used to

map the applied analog input to the output matrix. Figure 4.2 represents the spot-check method of reduced-coverage functionality testing of ADCs where analog voltages $v1$ or $v2$ are applied to the ADC input – the corresponding output codes, tested by the ATE digital pattern, are obtained by the ADC transfer function –

$$f(v1) \overset{ADC}{\rightarrow} C[v1, K_{i=1}^{n}] \tag{4.2}$$

and,

$$f(v2) \overset{ADC}{\rightarrow} C[v2, K_{i=1}^{n}] \tag{4.3}$$

This methodology optimizes the test time for the DUT at the expense of reducing test coverage. Limited number of output codes are tested on the ADC as against the full scale testing involving 2^n codes.

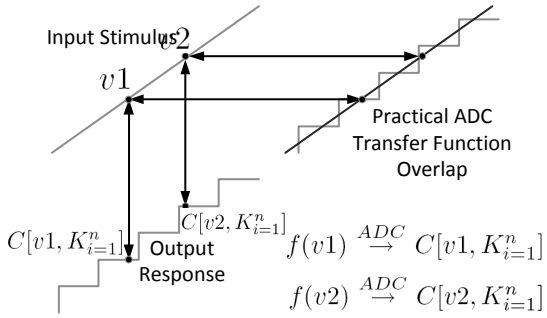

Figure 4.2: Spot-Check Voltage Input and Corresponding Response

When such spot-check methods are used on mixed-signal ATE, the analog voltage values $v1$ or $v2$ are provided by the analog resources of the ATE. Non-availability of such a reliable and consistent analog voltage level

may pose a problem when VLC-ATE are used and hence a band-gap circuit based voltage level generator is incorporated in the BIST scheme. Use of a bandgap circuit [19, 20] provides a process-independent reliable internal voltage reference within the BIST controller, making the BIST scheme compatible with reduced coverage spot-check testing on VLC-ATE. An on-chip bandgap circuit may also be shared with other test/mission mode applications if the provision is available.

4.1 Real-Time Dynamic Production Testing

The BIST scheme thus achieves compatibility with the external tools that can be used to switch between the limited and full coverage tests on successive DUT without using any additional ATE resources. ATE production testing with an option to switch between coverage levels has been a topic of research [18] as it offers a cost optimized test solution. Depending on the DPPM extrapolations performed on the basis of full-coverage test samples, real-time decisions are taken to either resume the low-cost-low-coverage testing or and to enable the full-coverage testing while maintaining an acceptable DPPM. The algorithms are not visited in detail for the purpose of validating the BIST scheme. The various test time vs quality matrices used for such dynamic testing are application and customer specific and are typically determined at product level.

Figure 4.3 represents the dynamic test flow used in a typical test setup. If a limited-coverage spot-test check is enabled, the short test is performed on

the DUT. If the setup is programmed to run the full coverage test suite on every n^{th} unit, the pass/fail value for the full coverage test on the unit is used to extrapolate a DPPM value from the total number of units tested till that instant. A decision is made to switch to full coverage if DPPM $>$ *Spec_Limit*, otherwise the reduced-coverage test with n^{th}-unit-full-test sampling is reverted back.

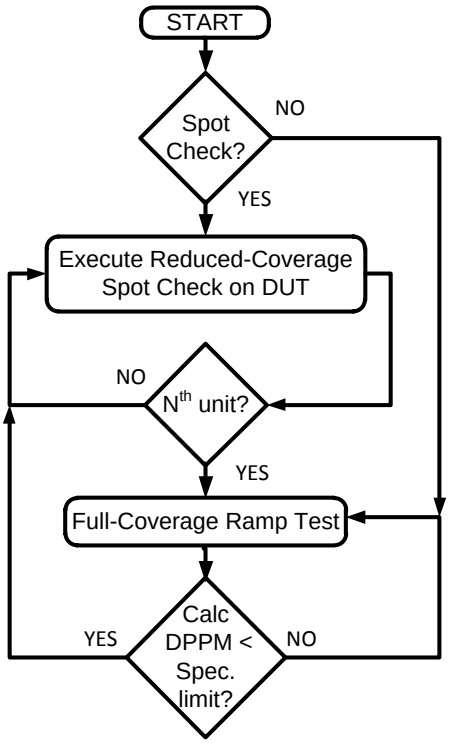

Figure 4.3: Dynamic Test Flow per Unit in Production Test

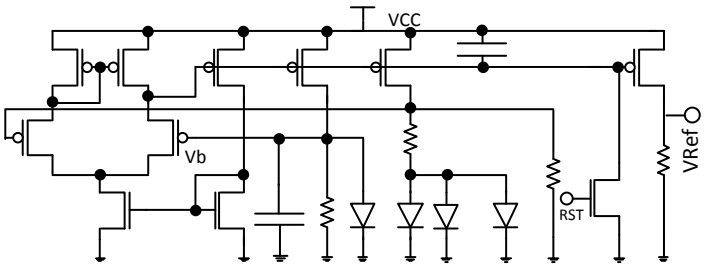

Figure 4.4: Bandgap Reference Circuit Used

4.2 On-Chip Stimulus Generator

Availability of an on-chip stimulus generator is crucial to eliminate the need of expensive analog testers. The process-compensated ramp generator described in the prior sections is used for ADC linearity testing. Code-offset testing of ADCs requires a DC stimulus which is generated on chip by using a bandgap reference circuit.

Bandgap reference circuits have been developed [19, 20] in order to provide a reliable, process-independent and consistent DC voltage reference on chips. Availability of such a voltage reference eliminates the need to have an ATE-supplied DC voltage for ADC spot-check test. A sub-$1V$ bandgap circuit [20] is used over a typical $1.25V$ circuit to provide an approximately $\frac{VDD}{2}$ analog voltage to the ADC when the BIST controller enables the reduced-coverage spot-test.

The bandgap circuit in Figure 4.4 is designed to provide a voltage reference value of $518mV$ with an observed standard deviation of $5mV$, as

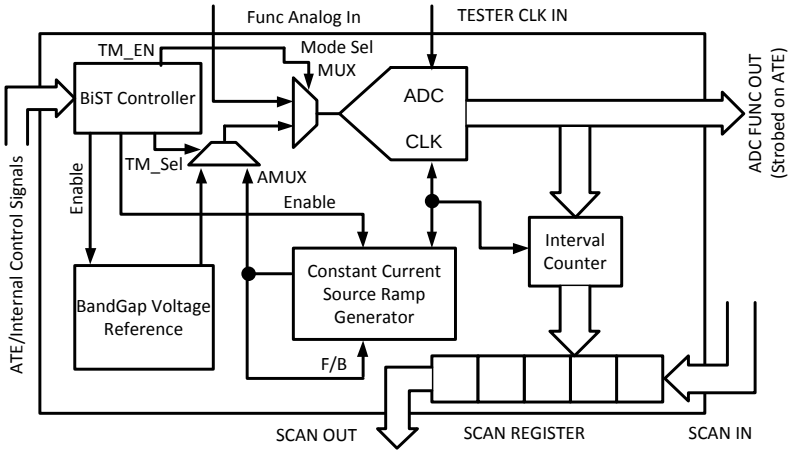

Figure 4.5: System Level Schematic for Hybrid Dynamic BIST Scheme

shown in [20].

When the module is programmed for the spot-check BIST test, the V_{ref} value is applied internally to the ADC input through an analog multiplexer. Selecting full-coverage ramp test enables the rampout signal node connected to the same multiplexer.

4.3 Hybrid BIST Controller and the BIST Scheme

The system level hybrid BIST scheme is shown in Figure 4.5. Any loading of ADC inputs is limited to ensure that mission mode performance is not impacted due to the BIST scheme. A single mode-select multiplexer is used to toggle between test mode and functional mode, the functional analog input is provided by the mission-mode source. Use of a single analog multi-

plexer makes the ADC input immune to additional loading due to other BIST components. The various important functional blocks of the BIST scheme are as follows:

- **BIST Controller:** This control module interacts with the DUT for mode selection. Either a direct ATE interface using shared IO resources or a register read operation can be used for this purpose. The DUT/ATE programs the control module in TEST mode while specifying the use of either full-coverage test or the limited coverage spot-check test. The controller then provides a select signal to the mode-select multiplexer and the analog multiplexer accordingly enables the corresponding BIST stimulus generator module.

- **BandGap Voltage Source:** A process-independent DC voltage reference is included and is fed to the ADC during spot-check mode.

- **Ramp Generator Module:** The ramp generator module includes the constant current source with feedback mechanism required to provide process independence. The ramp generator output is routed to the feedback module and the analog multiplexer which is used to select between the ramp generator and the constant voltage source.

- **Interval Counter:** The counter output is scan-enabled and can be shifted out of a scan register included in the BIST scheme.

- **ADC:** This is the 12-bit ADC IP present in the DUT. The ADC output nodes are connected directly to the ATE channel resources and this

scheme can be used for any ADC which has test accessibility to its output buffers.

Concurrent execution of ADC test can be enabled along with other blocks due to independent resources used. An initialization signal is provided to the ramp generator by the test mode control block and the functional clocks are gated to the ADC, the ramp generator and interval-counter blocks. A functional pattern designed to screen for INL, DNL, offset and gain is used for observing the interval counter and ADC outputs.

4.4 BIST Scheme Circuit Implementation

The system level topology used for simulation includes a tracking ADC along with the ramp and constant voltage generator for the spot-check scheme. A tracking ADC configuration is chosen for the BIST scheme to capture the mixed nature of the ADC characteristics. Unlike a flash ADC, a tracking ADC does not initialize to represent its analog input correctly. A *'catch up'* is required for the internal up-down counter to provide enough pulses so that the output can track and reach the same digital voltage level as the input signal. This tracking delay is a typical characteristic of multiple types of ADCs and checking the performance of the two BIST methods with this design makes it more universally acceptable.

The tracking time τ for the ADC to reach a voltage level V_i from initialization can be well characterized in simulation for various process corners.

The constant input needed for the limited-coverage spot test can be applied for the duration $\tau + \delta\tau$ to provide adequate settling time. This time duration can be controlled by the ATE interface signals provided to the BIST controller and is an added feature to test such tracking ADC configurations, which are not typically tested with spot-check methods.

The hybrid BIST scheme is implemented using a 90nm CMOS library. Post layout simulations were performed for ramp generator in the BIST scheme across process corners to confirm the SPICE simulation results. A 12-bit ADC configuration was used in the simulation which closely matches a typical general-purpose on-chip ADC. Post layout simulations for the spot-check stimulus generation circuit across process corners confirm the findings in [19]. Table 4.1 summarizes the results for the three process corners, the standard deviation point lies within the $3 \times$ LSB of the ADC, demonstrating the stimulus process-independence and stability.

Area overhead of a BIST scheme is a measure of merit as it directly translates to the die-area and the die repeatability on a production wafer. The silicon area of the individual blocks of the BIST scheme is presented in Table 4.1. The overall area overhead of the BIST scheme is $867.5\mu m^2$, which translates to an area overhead of 5.84%. A 12-bit ADC module of area $0.014mm^2$ is used for simulations.

The ADC BIST enables linearity testing with VLC-ATE while adding a moderate area overhead. Hybrid nature of the methodology enables at-speed testing using built-in stimulus while using low-end external test resources.

Table 4.1: System Level Post Layout Simulation Results for Spot-Check Test: Bandgap Circuit Output

Process	**Output (Mean)**	**Output (12-bit)**	**Std Dev**	**Std Dev (LSB)**
Slow	$519mV$	0..11000001	$6.1mV$	2.26
Nom	$529mV$	0..11000101	$7.3mV$	2.71
Fast	$534mV$	0..11000111	$6.8mV$	2.52

The interval counter along with sequential analysis method can provide data required to completely characterize the ADC.

Availability of spot-check or reduced coverage testing provides compatibility with innovative dynamic testing tools. Basic low-cost-testing can be performed on VLC-ATE, with an option of full coverage to align with the established DPPM quality matrices.

The fault coverage matrix for the DUT remains unchanged in this BIST scheme as the BIST mechanism replicates the analog functional testing done in a non-BIST environment. This ensures that the ADC output data can be processed by conventional analysis methods and no engineering overhead would be needed to apply established quality metrics to the observed data.

4.5 Improvements Over Existing Work

Existing schemes and proposals for adaptive test methodlogies concentrate on digital circuits where non-parametric testing is performed to determine circuit functionality. Use of adaptive test methods can help optimize test cost while maintaining acceptable defectivity as represented in [17, 18]. The proposed BIST scheme provides compatibility with the existing software resources that support adaptive testing which is a novel approach for low-resource mixed signal testing.

Chapter 5

Quiescent Current Measurement with a Built-In Current Sensor

Parametric defects are of increasing concern in the sub-65nm process technologies due to fabrication imperfections. While catastrophic faults result in non-functional devices, parameteric faults may result in performance degradation. CMOS circuits require voltage biasing for operation and draw finite current. This voltage/current (VI) behavior is well defined in quiescent as well as active states. Device state and process parameters govern the VI characteristics, and catastrophic as well as parametric defects present in CUT may result in deviation from the ideal VI characteristics. DC testing of circuits is therefore an established semiconductor production test practice to screen defective devices.

Modern SoC designs combine diverse functionality on a chip, which results in the presence of a variety of modules on the same silicon die. Multiple blocks operating at the same voltage may share power planes in the design in order to reduce metal-level layout complexity. CUT-level measurement resolution is restricted with shared power supplies, since variation in one block may be masked by other current components. Subsequent stages in multi-

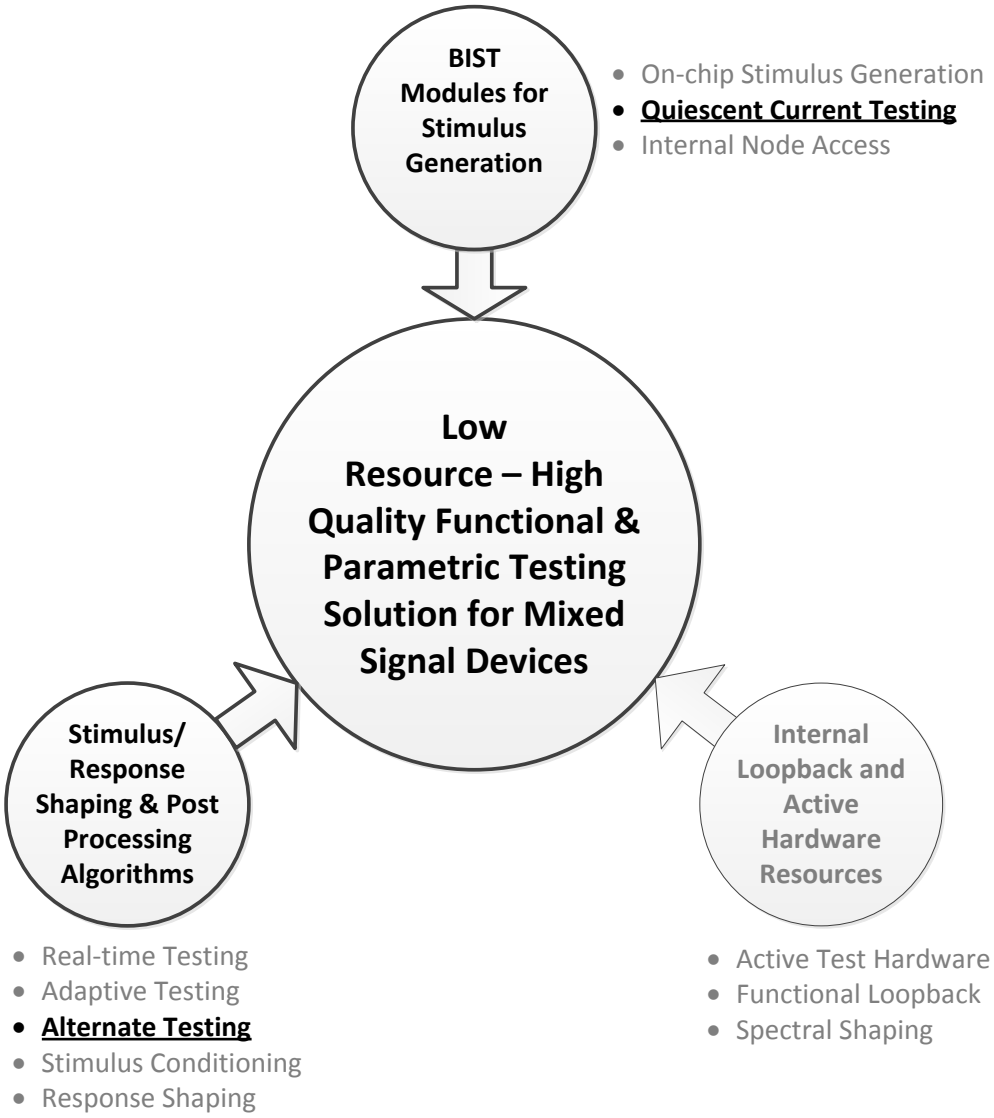

Figure 5.1: BIST Scheme to Enable Module Level Quiescent Current Testing

stage systems may compensate for parametric faults of previous stages, making detection difficult. Feedback systems may adjust themselves due to closed-loop

transfer functions and mask parametric faults in individual blocks.

The Built in Current Sensor (BICS) proposal to enable sub-system/circuit level current monitoring is described in this section. The BICS provides accessibility to internal blocks and enables isolated parametric testing. Calibration routine enables process independence and provides robustness and thus the BICS can be used for detailed parametric testing in the production environment. Figure 5.1 represents the BICS and data analysis approach used. A BICS/BIST module is used along with an alternate testing approach in order to reduce the frequency requirements of the self test scheme. The BICS scheme may be applied to a circuit, block or sub-block to enable measurement at the required hierarchical level. As process parameters strongly affect the quiescent current, calibration is enabled in the BICS. The BIST proposal is compatible with VLC-ATE systems to enable high-volume, low-cost high-test coverage for bias current testing. The current signature is converted to a voltage signal that can be read out by using the Per Pin Measurement Unit (PPMU) on VLC-ATE. A process-reference voltage is generated in the calibration stage and is used for test limit determination.

While a majority of prior proposals include provisions for linearity across a wide current measurement range and efforts to minimize interference to CUT functionality, practical manufacturing concerns are not addressed. Mission mode circuit performance may also be affected due to any additional load introduced while forming a sensor. Work in [23, 25, 26] does not go into any analysis on the effect of BIST on mission mode performance, limiting its

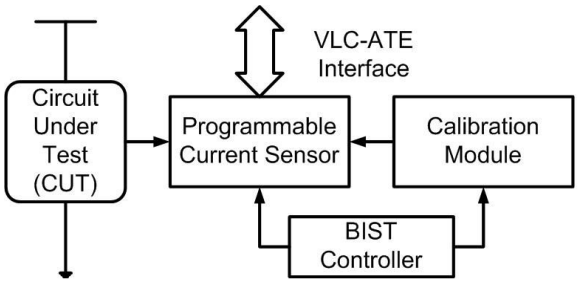

Figure 5.2: System Representation of the BICS Scheme

applications. This topology has minimal impact on the mission mode CUT topology as no bias current paths are shared or loads introduced, and hence is an improvement over the previous work. Fabrication imperfections may vary the sheet resistance value affecting the power sensor load. Measurement variability due to process variation may not be separated from variation caused due to CUT defects. These concerns need to be addressed as they limit the scope of applications for the BICS scheme.

A calibrated current-to-voltage converter is used in order to obtain a voltage output representing the CUT current measurement. Ramp generator circuits can be used for this application as the final ramp output value is a function of the charging current. Various ramp generator proposals have been published in the past [7, 8, 28]. The BICS is based on the process compensated proposal from [28] to ensure usability across process corners.

5.1 BICS Scheme Topology and Operation

The system level representation shown in Figure 5.2 includes a programmable current sensor, which is used to estimate the CUT supply current value. A current reference is deduced by the sensor module by a current-strap connection with the DUT [29]. The PMOS transistor included in Figure 5.3 is a part of the CUT and the circuit performance remains unaffected due to the addition of this BICS. The sensor thus uses a current reference from the DUT as against using an IR drop value in the power-plane connection similar to some of the previous BIST proposals. The effective enable signal that is used to program the CUT is translated into a single-bit control signal to enable the BICS current mirror.

A current mirror circuit is connected in parallel with a load transistor which drives the CUT; the mirror circuit is designed such that it can independently source a current i_{src} when the $Test_{EN}$ signal is not asserted.

Semiconductor process variations can cause deviations in the transistor and the load from the target. A clocked comparator is used to compare the ramp output with $\frac{VDD}{2}$ at the end of test duration τ_{test}. The test clock used during calibration and BIST test mode is provided by the ATE and the duration τ_{test} is based on characterization performed using Monte Carlo simulations.

C_1 is used as per-cycle-charge-storage for the comparator output. Charging conditions for the capacitor C_1 are defined as follows. If $V_{ramp} < \frac{VDD}{2}$ at

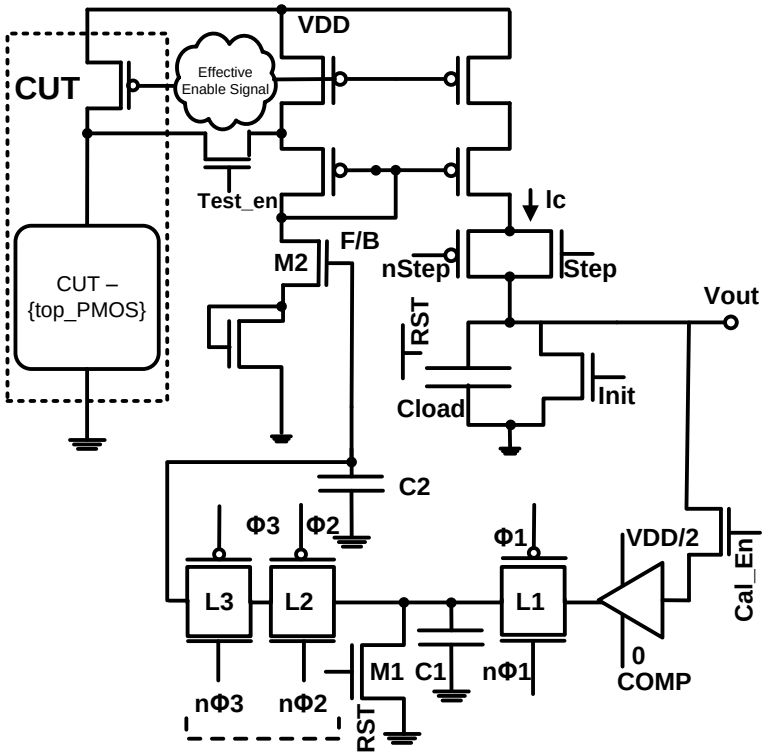

Figure 5.3: Programmable Current Sensor Circuit with Calibration

$\frac{T_{per}}{2}$, $V_{C1} = VDD$ else $V_{C1} = 0V$. Latches L_2 and L_3 are toggled by an offset clock to limit the conductive phase of the combination latch.

The voltage across capacitor C_2 is used to change the bias current in the constant current source; if the $V_{ramp} < V_{ref}$ at $\frac{T_{per}}{2}$, C_1 charges C_2 to a higher voltage value while for $V_{ramp} > V_{ref}$ at $\frac{T_{per}}{2}$, C_1 being at $0V$, partially discharges C_2, lowering the effective voltage across C_2. A reduction in voltage across $C2$ results in a lower gate bias for the current mirror, reducing the load charging current. Detailed analysis for this calibration process is covered in prior sections where a process compensated current source is used for ADC self-test.

The feedback signal voltage node can be sampled at this instant for self testing the BICS. This analog voltage may be output on a DUT pin and may be measured with an VLC-ATE PPMU.

The BICS scheme proposal uses the analog output voltage value across the load as the parametric representation of the CUT supply current. For reliable use of this V_{load} value as a measurement parameter, the two matrices should have a bijective relationship denoted by –

$$P[V_{load}] \leftrightarrow P[i_{CUT}] \tag{5.1}$$

where,

$P[V_{load}]$: Linear vector containing the range of V_{load} values.

$P[i_{CUT}]$: Linear vector containing the range of CUT supply current values.

A cardinality between these two vectors is thus essential for accurate prediction of CUT supply current. The BIST output vector is a function of both the CUT supply current and process conditions in the current sensor circuit [30].

$$P[V_{load}] \leftrightarrow f[i_{CUT}, BIST_{proc}] \tag{5.2}$$

Monte Carlo simulations were designed to estimate the effect of process variations. Absence of calibration for process variations limits production usability of the BICS scheme, as output variations due to CUT supply cannot be separated from variations due to process spread in the current sensor module.

The BIST proposal is designed to be compatible with the commercial VLC-ATE which optimize the available system resources to limit cost by optimizing power and clocking requirements. The large scale cost reduction enabled by VLC-ATE makes the use of compatible BICS schemes attractive where optimization between test quality and cost can be achieved.

The BICS was simulated using a 90nm CMOS library. A programmable constant current source is used to simulate the effect of the CUT. A $\pm 10\%$ variation in supply current is simulated in order to mimic the effect of process corners [31] by varying dopant implantation and sheet resistance by $\pm 10\%$ in the SPICE models.

The BICS uses the same supply grid as the CUT and any IR-drop/voltage droop affects both circuits equally. As the calibration scheme ensures a $\frac{VDD}{2}$ crossover at t_{per}, the feedback voltage node value automatically adjusts to

compensate for supply voltage variation impacting the BICS. Any drop in the CUT current due to IR-drop/voltage droop is a change to the BICS and is accurately measured.

Results from Monte Carlo analysis are included in Table 5.1. A range of constant CUT currents is used for these simulations and the required capacitor values with programmed test duration are used for the setup. The BIST output voltage and the corresponding measured CUT current value is obtained from the BIST characterization simulation data. While maintaining CUT current constant, the process and voltage corners are varied around the nominal medians for a 3σ value corresponding to 10% of the nominal. Temperature is switched between 0 °C, 25 °C and 95 °C for simulation. Results show a tight centering due to the closed loop feedback loop used in the calibration circuit during initialization. The measurement envelopes achieved with the BIST circuit using the test duration variation is included in Table 5.1. The results are indicative of the repeatability and robustness of the the BICS proposal. Silicon area constraints limit the capacitance value that can be included on-chip – if a higher range current measurement is required, an off-chip capacitor scheme may be used. While the versatility of the scheme can be demonstrated with these results, DUT currents in the nA range can be measured with an on chip capacitance value of a few pF.

Table 5.1: Monte Carlo Results for PVT Variation

CUT Current (μA)	**Cap Load** (nF)	**BIST Measurement**	
		Lower (μA)	**Higher** (μA)
1	10	0.982	0.021
10	25	1.034	0.037
50	100	50.256	0.438
100	250	100.648	0.636
500	500	503.133	1.394

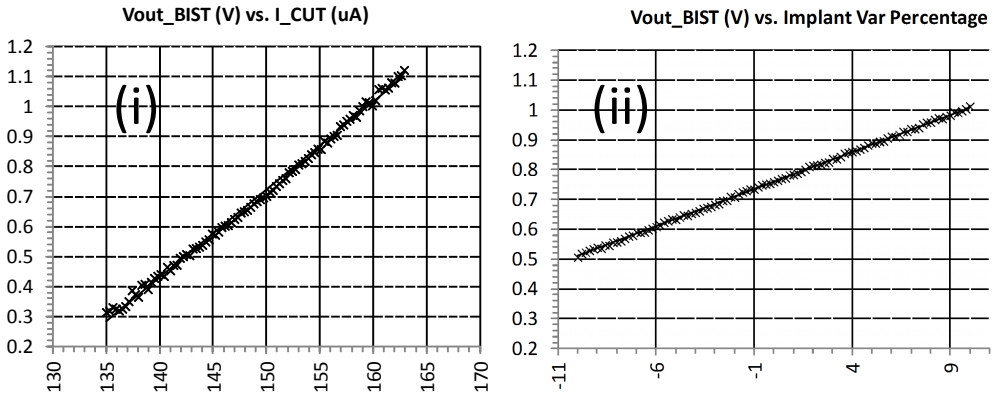

Figure 5.4: Impact of process variation: (i) Variation in V_{out} as a function on i_{CUT} with no process variation and (ii) V_{out} distribution vs. process variation with a constant i_{CUT}

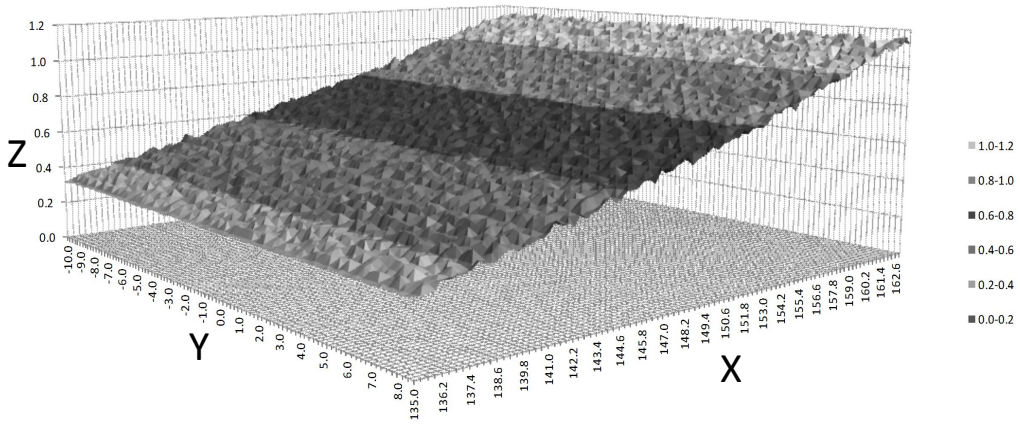

Figure 5.5: Multi-variable simulation with BIST output V_{out} variation (Z-axis) plotted against CUT current variation (X-axis) and process variation in SPICE models (Y-axis)

Table 5.2: Measurement Range with Capacitor Bank and τ Variation

Mode	**Load Capacitance**	τ **= 1mS**	τ **= 100mS**
C_1	$10nF$	$0.7\mu A$	$7nA$
C_2	$1uF$	$1.1mA$	$11\mu A$

5.1.1 Impact of Process Calibration

Lack of process calibration results in violation of the bijective relationship between i_{CUT} and V_{load}. Figure 5.4 demonstrates the variability in the analog output voltage in absence of process compensation. Figure 5.4–(i) represents the ideal simulation case with a valid relationship between i_{CUT} and V_{load} with nominal process, where a 10% i_{CUT} variation around a $150\mu A$ median value is plotted against the corresponding i_{CUT} simulation values.

The BIST output voltage can also be varied by changing the process

Table 5.3: Dynamic Statistical Limits Supported by Feedback Node Voltage

			Statistical Limit (μA)	
	Parts	**Median** (μA)	**Lower** (μA)	**Higher** (μA)
(i)	Slow	27.75	21.25	33
	Fast	31.75	26	36.75
(ii)	Typical	29	21.75	34.5

implant levels for the current sensor circuit. A ±10% variation in the SPICE model parametrics and the corresponding variation in the BIST output V_{load} is plotted in Figure 5.4–(ii). Thus this bijective relationship is maintained across process variation.

Tri-variable simulation results are presented in Figure 5.5 where the process implant value follows a Gaussian normal distribution around the targets in SPICE models, the CUT current i_{CUT} is varied linearly by ±10%. The plane corresponding to V_{out} has a globally monotonic one-dimensional slope as a function of i_{CUT} indicating independence from process implant variations when process calibration is performed.

5.2 Programmable Range and Dynamic Limits

Programmability to the BICS scheme to cover a wider current range improves usability for testing multiple on-chip modules which can be interfaced with the BICS in their respective test modes.

Test duration τ is controlled by the VLC-ATE through the controller.

The relationship between the BICS output and the test duration τ is linear in nature for an ideal BIST model. For a given value of C_{load}, τ can be adjusted to measure a range of i_{CUT} values. A capacitor bank consisting of a range of values may also be used with a selection mechanism in order to extend the BIST measurement range. A combination of load selection and test duration is used to achieve this goal. CUT current value range and the corresponding τ values are presented in Table 5.2.

While the BIST circuit is compensated for process variations, process variations in the CUT would result in a change in i_{CUT}. Defects that result in δi_{CUT} variation may be difficult to differentiate from the process dominated current variation. Figure 5.6–(i) presents SPICE simulation leakage data collected across fast and slow process corners for for a 12-bit ADC IP. The two distributions overlap due to the standard deviation around the process target and the median values are $27.5\mu A$ and $32\mu A$, respectively. Figure 5.6–(ii) includes results when faults causing opens and shorts are injected and the current drawn by a typical functional sample and non-functional failures drawing zero current and marginal short parametric failures drawing a higher current value are plotted in histogram form. Outliers present in Figure 5.6–(ii) are deviant from the population trend and required to be screened out. The outliers are marked as (a) and (b) in the Figure 5.6; the population (a) corresponds to potentially non-functional parts while the population (b) corresponds to parametric failures that draw a higher supply current.

Typical static limits used for DC testing do not provide flexibility where

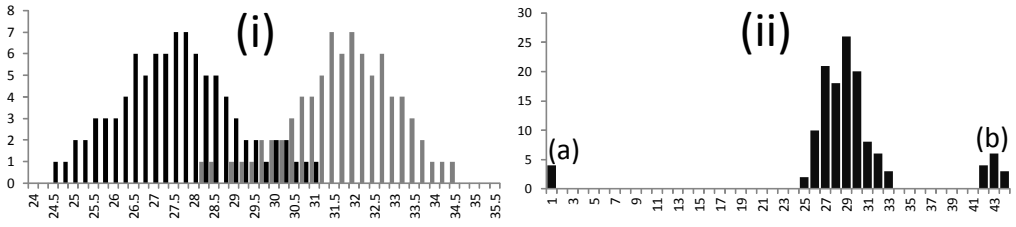

Figure 5.6: Need for dynamic limits: (i) Measurement variation seen between fast and slow process corners, (ii) Non-functional parts with no current drawn (a) and statistical outliers (b). Current measurement in μA on X-axis, bin count on Y-axis

the outlier parts in Figure 5.6–(ii) are required to be screened while the higher measurements in Figure 5.6–(i) can still be a part of the passing distribution. Dynamic limits, which can be adjusted to the distribution median, can allow this flexibility. The feedback node output from the BICS scheme is representative of the process corner as discussed earlier. This value may be used to process dynamic limits in order to screen out the outlier parts while faster or slower process material that follows the statistical trend is not rejected.

Table 5.3 includes the statistics for Figure 5.6–(i)/(ii). The median values of the distribution are used to determine the seed for the dynamic limit. An arbitrary $\pm$ 3σ limit around the calculated median may be used to screen out device groups (a) and (b) from Figure 5.6–(ii).

5.3 Layout and Area Overhead

The the hybrid BICS scheme was implemented using a 90nm CMOS library. Monte Carlo simulations were performed to validate process indepen-

dent performance while optimizing the load capacitor values. A programmable load consisting of selectable capacitor values is included in order to improve the measurement range for the current sensor BIST scheme. The BICS scheme area is approximately $450\mu m^2$ with the variable load capacitors included. Additional capacitive elements can be included at the expense of silicon area based on the requirements. Multiple blocks can share the BICS to reduce overhead impact. Scalability of this scheme makes it attractive and feasible for commercial implementation.

5.4 Improvements Over Existing Work

Current testing is an established industry practice and fault models/fault detection [21] have been a research focus. Singh [22] proposes a differential current sensor for high speed current sensing applications where results are presented for fault detection, while programmability features are absent in the proposal.

The built-in current sensor in [23] makes use of the parasitic resistance attached to an interconnect layer. Maidon [24] supports the simulation findings with silicon results and dynamic performance of the system is analyzed in presence of CUT faults. While detailed circuit results are presented, application as a volume manufactured BICS is limited due to fixed measurement range and sensitivity to any variation in the sensor.

Vahedi et. al. [25] uses a current mirror with a compensating circuit and a dynamic control loop to ensure linearity. While this provides linearity

improvement, distinguishing process-corner driven current variation vs. defect driven defect variation is not feasible with the scheme in [25].

A sensor load may used for measurements which results in a deterministic voltage drop in mission mode. [26] uses a similar approach of mirroring current using a parasitic load in the interconnect layer and active amplifiers are used in order to obtain a measurable signal. Process sensitive analog circuits are used in the active amplifiers to improve the measurement range which may not be reliable in a production process window. The assumption of 1Ω resistance of the current sense element is not reliable for volume stastics, limiting the usablility of this scheme. No mechanism is present to augment the measurement range of $10mA$ to $50mA$ which has been used for simulation and this dissertation provides a significant improvement in terms of current measurement programmability.

Proposals in [27] include BICS schemes to monitor the voltage drop on supply lines due to quiescent current drop. The resolution of $10\mu A$ is achieved with the [27] scheme with SCAN enabled output. Use of the circuit path to provide an IR-drop can limit the application of the scheme in modern sub-$45-nm$ circuit technologies where the Back End of the Line (BEOL) process steps and metal layers dominate the parametric faults in volume manufacturing. The calibration process is limited to enable 0-input calibration where a null signal may be generated with no current flowing. BEOL and Front End of the Line (FEOL) variation in the CUT or the stochastic sensor can proceed undetected in this limited calibration process while impacting the final current

readout due to fabrication variation. The scheme prosposed in this dissertation overcomes this shortfall by enabling a full process-sensitivity calibration for the BICS.

Chapter 6

Phase Locked Loop BIST with Internal Node Access

PLLs need to meet analog performance matrices such as lock time, phase error and jitter in addition to the frequency lock test in commercial semiconductor testing. Parametric testing of PLLs is resource intensive and requires high precision hardware on the ATE. A BIST scheme for performing functional and parametric tests is reviewed in this section. The scheme enables indirect access to internal nodes of the PLL and uses a low resource stimulus generator in order to test the PLL in closed loop mode using internal loopback for this 'opened closed loop' system as depicted in Figure 6.1. The BIST controller is independent of the PLL frequency and can be used effectively in multi-PLL SoC modules. The BIST scheme is designed to minimize impact to mission mode performance by not perturbing analog nodes and the phase sensitive feedback loop. The test methodology enables parametric testing for process variation and specification compliance while using minimal external test resources.

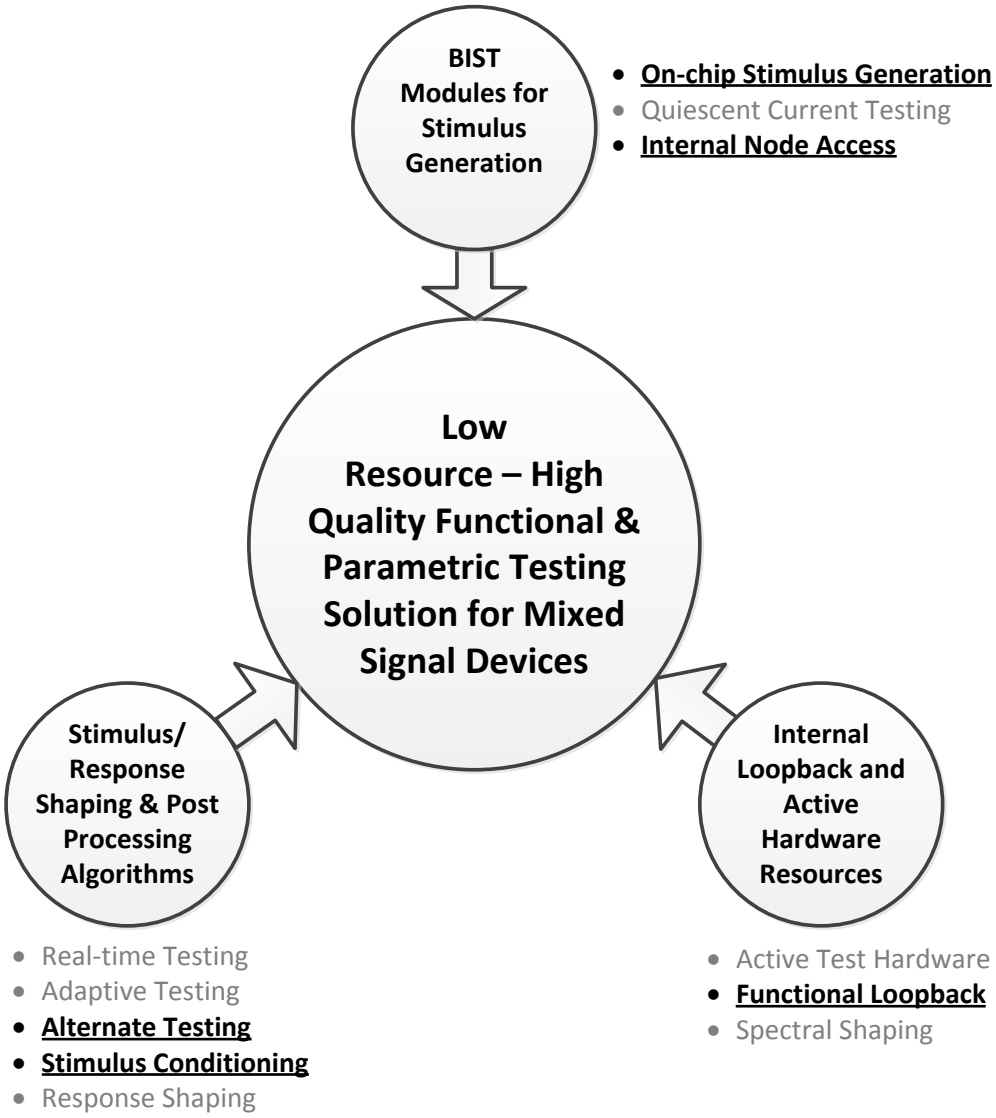

Figure 6.1: PLL BIST with Internal Node Access

6.1 PLL Self Test

PLLs are used as clock generators in SoC and parametric compliance of PLL output can therefore impact SoC function. Parameters such as jitter, set-

tling time, lock time and frequency drift etc. need to be met to ensure expected performance. SoC testing strategies are complicated by PLL test requirements as the digital blocks may be tested with minimal ATE resources [32]. Basic PLL lock test requires high speed hardware while the parametric tests require precision timing equipment, making the test cost prohibitively high in semiconductor production. PLL lock test is used as the typical test gate for PLLs and it does not provide coverage for functional or fabrication parametric faults. Limited coverage offered by the economical lock test may compromise quality required for certain PLL applications.

A PLL BIST needs to ensure that the sensitive analog nodes in the PLL (shown in Figure 6.2) interfacing with Charge Pump (CP), Loop Filter (LF) and Voltage Controller Oscillator (VCO) are not disturbed as it impacts mission mode performance [33, 34, 35]. The feedback loop is phase sensitive and any additional components added impact the phase of the loopback signal. Any noise added due this impacts the mission mode phase performance of the PLL and is not desirable. Use of the feedback loop also limits BIST application to a particular frequency range, limiting reuse. A closed loop test solution adds effectiveness as self-test is enabled within the PLL. This also enables mission mode test of internal blocks to screen for any parametric faults.

The BIST scheme presented uses non sensitive internal digital nodes to implement self test capabilities with baseband/low frequency signals. The solution is frequency independent and therefore scalable across a wide range of PLL frequencies.

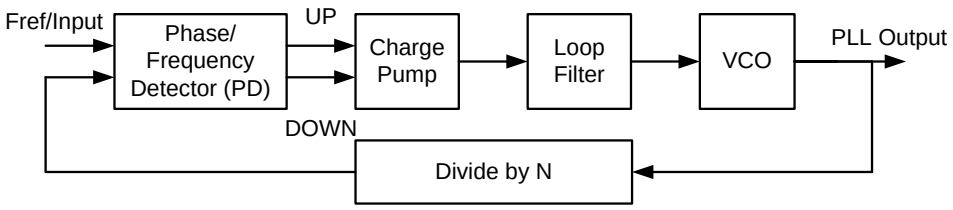

Figure 6.2: Top Level Schematic of a PLL

The BIST controller has a baseband interface with the ATE and thus uses minimal resources. Compatibility with a basic digital ATE system is critical to lower test cost and is of particular concern. The scheme is thus able provide a high test quality, at-speed, closed loop, scalable solution while minimizing test resource requirements.

A variety of BIST approaches have been proposed in the past – [36] proposes an all digital BIST scheme for testing catastrophic faults in PLLs with no parametric coverage. [37] digitally programs the CP and observes the loop filter output – the scheme does not sample the VCO input as the additional load may affect VCO characteristics. Adding duplicate modules or providing internal node access is explored in [38], while not enabling a complete closed loop test solution without external stimulus. Open loop solution that drive selective blocks within the PLL [39] reduce test coverage. [40] proposes a BIST mechanism with a test mode that can select between PLL output fed to the Phase Detector (PD) as against added line delay. The work presented in [42] attempts to perform parametric testing apart from simple catastrophic failure

testing proposed in many other schemes. All the three schemes presented in [42] use additional circuits in the feedback loop and would result in a phase shift and frequency dependence on the PLL operating frequency.

6.2 Applying Alternate Test Methodology to a PLL

Alternate Testing principles can be applied to a mixed signal circuit with multiple internal nodes, where the nodes and output are inter-dependent. Parametric relations between various internal nodes and the functional output can be explained as follows – when an input frequency signal at frequency f_{opr} is applied to a PLL with a loop multiplier of n, the PLL attempts to latch to a frequency equal to $n \times f_{opr}$ the input frequency and phase within the time interval t_{latch}. The phase detector signal is instantaneously proportional to the phase and frequency difference between f_{opr} and the PLL output signal at the measurement instant t'. This dependence can be represented as:

$$P[f_{opr}, f_{PLL}, t'] \leftrightarrow P[PD_{out}, t'] \tag{6.1}$$

where,

$P[p1] \rightarrow$ is the parametric space matrix for parameter $p1$.

The parametric set $P[PD_{out}, t']$ is finitely bound and can be well characterized using SPICE simulations for the independent variables. The set of $[PD_{out}]$ is a bijective function of $[f_{opr}, t']$ with a finite deterministic statistical confidence for a stable and functional PLL during lock-mode [30]. The value

of $[PD_{out}]$ can be predicted with certain statistical confidence at an instant t' if the variables f_{opr} and f_{PLL} can be measured.

Similar relationships exist between the remaining internal system nodes. The CP_{out} signal is a function of the PD output and when considered over an interval $[0, t']$, it is a bijective relation represented by –

$$P[PD_{out}, 0, t'] \leftrightarrow P[CP_{out}] \tag{6.2}$$

The LF and VCO have similar bijective relations –

$$P[CP_{out}, 0, t'] \leftrightarrow P[LF_{out}, 0, t'] \tag{6.3}$$

The bijective relationship between CP and LF can be established over a specified time interval $[0, t']$ as the node voltages are analog in nature and are a function of the measurement window during PLL lock process.

The bijective relationship between LF and VCO can be established instantaneously and represents the relationship between the voltage node and the effective frequency output.

The BIST uses the bijective relationship between PD and CP to perform parametric testing of the PLL. While accessing the common node between PD and CP, remaining PLL is treated as a closed loop with successive bijection-related sub-blocks. An input vector $i[CP_{in}]$, which is a subset of the vector set $P[CP_{in}]$, is applied to the CP block using an external driver and the corresponding output vector from PD block $i[PD_{out}]$ is recorded by using the BIST scheme. The vector $i[PD_{out}]$ is integrated over a time interval $[0, t']$

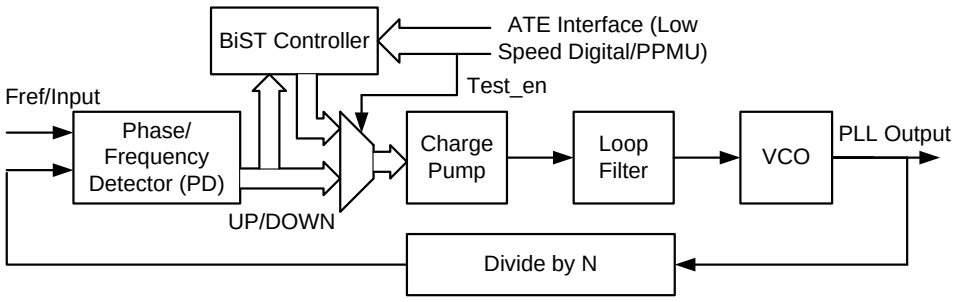

Figure 6.3: BIST Schematic: BIST Controller added between PD and CP

and compared with simulation data to compare the accumulated voltage value. The bijective relations are valid for this analysis as the CP_{in} vector is injected and the closed loop response on PD_{out} node is observed, isolated in the test mode. By including the tolerance limits for the value of the integrated vector $i[PD_{out}]$, a pass/fail decision can be taken by the ATE.

6.3 Hybrid BIST Scheme Review and Operation

The BIST scheme is presented in Figure 6.3. The BIST controller, which acts as a programmable stimulus generator as well an observation module, is connected between the PD output and the CP input. The digital output of the PD is fanned out to the BIST controller in parallel with the mission mode connection to the CP module. Output from the BIST controller is fed to CP through a multiplexer which is connected to PD during mission mode and to the controller in the test mode. Test enable signal provided by the ATE is used to enable multiplexing. The ATE control/data signals that connect

to the BIST controller are represented by a bus which includes either analog or low frequency digital signals. The input vector applied at CP to perform controlled charging of the VCO input is scanned in serially. The high/low nature of this digital input controls the conduction of the CP switches. The controller also reads in the the PD output for a specified duration after feeding in the CP code and this signal on PD output is fed to a Low Pass Filter (LPF) to generate a DC voltage level internally. A PPMU is then used to measure this DC voltage value. The input pin used to scan in the CP programming code can be designed to be a general purpose IO which is also used for this PPMU measurement.

The internal blocks of the BIST controller are shown in Figure 6.4. The input section of the controller consists of an IO pin of the DUT which is used to scan in digital data onto the CP input. The output of the PD block is fed into the controller and is used to drive a constant current source in test mode. This output is then integrated over the test duration, which can be programmed by the control signals fed in from the ATE. The BIST scheme needs process independence to ensure that the integration process yields identical results in case of multiple process corners. A feedback bias mechanism, similar to the compensated ramp generator in prior sections, is used to calibrate the constant current source for process variation. The calibration routine thus compensates for the process variation and achieves a consistent input to the LPF.

When the test mode input is activated, data pulses are forced into the CP input through the ATE IO interface. The duration of the input pulses is

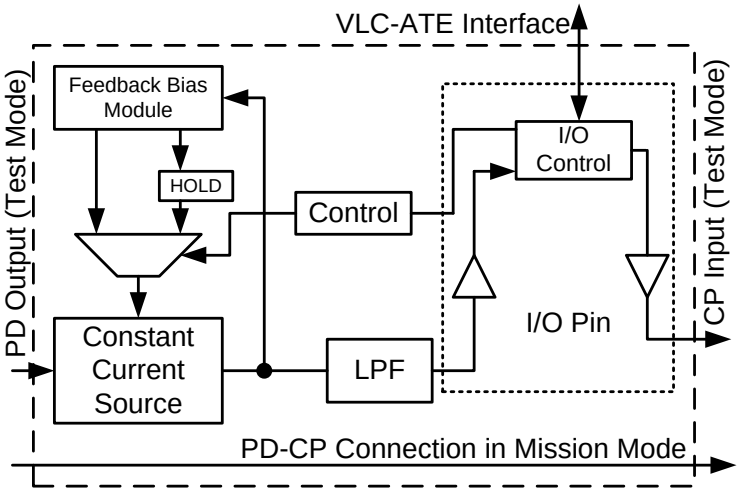

Figure 6.4: BIST Controller Components

controlled by the ATE and can be programmed depending on the DUT specifications and characterization results. A pulse applied on CP input connects the CP output node to VDD or ground depending on the input used; thus providing a charging or a discharging path to the CP load. The conductivity of the transistors used in the CP block as well as the input pulse duration affects the net charge interchange that can occur during test mode. If a pulse of duration τ is applied to CP during test mode during DUT initialization, the loop filter capacitor is charged to a voltage V_{LFout} which can be represented as:

$$V_{LFout} = Q_{LF}/C_{LF} = \int_0^{\tau} I_{LFdrive}/C_{LF} \tag{6.4}$$

In case of catastrophic failures in the CP block, the LF_{out} node would remain at

ground level when the DUT is initialized. Any marginalities/process variation in CP would result in an LF output which is denoted by –

$$V_{LFout} \pm \delta V_{LFout} = \int_0^{\tau} [I_{LFdr} \pm \delta I_{LFdr}]/[C_{LF} \pm \delta C_{LF}] \tag{6.5}$$

The BIST scheme, using a full-self test approach now tests the following blocks with this parametric variation at the VCO input. The VCO output frequency in test mode can be given by –

$$F_{VCO} = f[V_{LFout}] \tag{6.6}$$

Therefore, any variation in the VCO output frequency can be parametrically traced to the LF output variation –

$$F_{VCO-min} = f[V_{LFout-min}] \tag{6.7}$$

and,

$$F_{VCO-max} = f[V_{LFout-max}] \tag{6.8}$$

The sequence of pulses generated by the PD module for this VCO input signal is a function of the frequency and phase difference between the VCO output and the input frequency reference signal. When passed through an LPF or integrated over a specified duration, it represents the exact frequency difference between these two signals, creating a DC representation of the VCO output frequency.

$$\int_0^{t1} V_{PDout} = f[F_{VCO}] \tag{6.9}$$

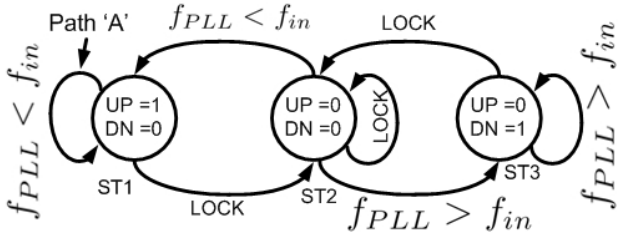

Figure 6.5: PLL Locking Process State Machine – PD_{out}/CP_{in} Represented

Therefore effectively,

$$\int_0^{t1} V_{PDout} = f[F_{PD,VCO,LF,LFdr}] \tag{6.10}$$

A catastrophic failure in any of the sub-blocks is detectable by the above function. Parametric or specification failures in any of the sub-blocks can be identified with the above transfer function.

It is essential to ensure that any of the additional components added in the BIST scheme do not influence this transfer function and therefore a process calibrated current source is used to drive the LPF. Using PD to drive the LPF results in loading of the internal node. The PD output signal is thus used to switch the process-stabilized constant current source and LPF combination, eliminating effects of process variation from the externally added BIST circuits.

The state machine in Figure 6.5 represents the PD_{out}/CP_{in} nodes and the corresponding signal values. A locked PLL requires no additional charging or discharging of the VCO_{in} node and hence this state is represented by $ST2 \leftrightarrow [UP = 0, DN = 0]$. This is the stable and locked state of the PLL. Depending on the PD block design, $ST2$ can be metastable, where succes-

sive charging and discharging cycles are provided to the CP input to maintain a charging neutrality. For example, the PD block may alternate between $[UP = 1, DN = 0]$ and $[UP = 0, DN = 1]$ so that the net effect on the CP input node is equivalent for each UP and DN, effectively conserving the charge at CP_{out} while the PLL remains in the lock state. The net PD_{out} signal in this case is $[UP = \frac{1}{2}, DN = \frac{1}{2}]$, when averaged over two successive cycles, identical in effect to the $[UP = 0, DN = 0]$ condition required for lock stability.

Any charging/discharging required for the VCO input node to increment/decrement the VCO frequency is represented by the states $ST1 \leftrightarrow [UP = 1, DN = 0]$ and $ST3 \leftrightarrow [UP = 0, DN = 1]$ respectively.

The BIST scheme forces the CP_{in} along 'Path A', as marked in Figure 6.5 when in test mode. This path is forced externally, and the corrective signal produced by the comparison between f_{PLL} and f_{in} does not affect the CP block in test mode.

This state-machine-control is only limited to test mode operation and the PLL can translate between the three states during mission mode, depending on the concerning circuit conditions.

6.3.1 Characterization of the Hybrid BIST Scheme

Monte Carlo simulation results are presented in Figure 6.6 where the impact of PLL parametrics and process variation on the BIST output is seen. The acceptable BIST output range is calibrated based on the simulation results to establish test screening limits to discard devices beyond the tolerance range.

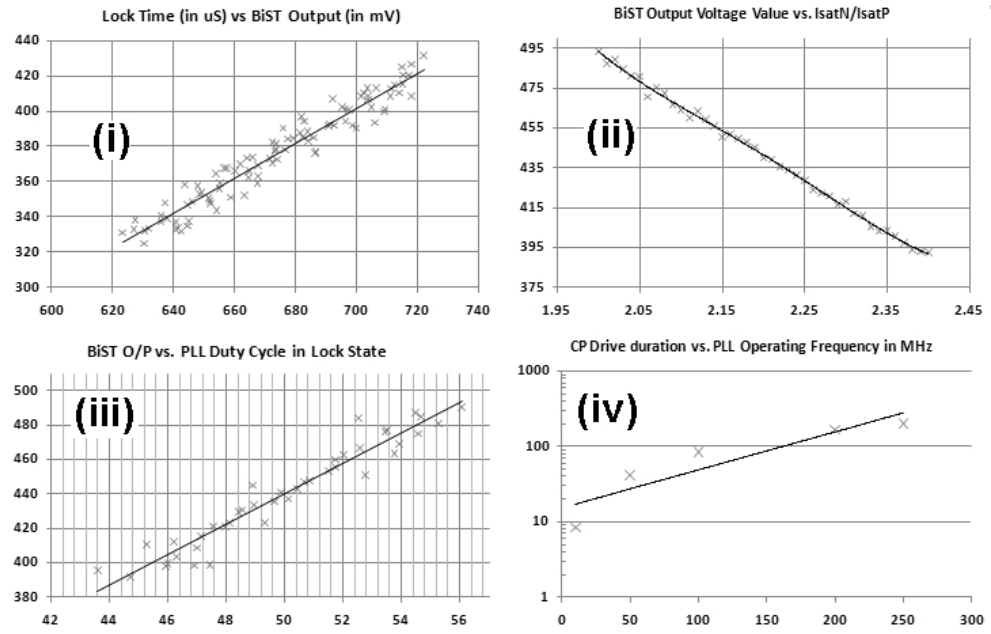

Figure 6.6: Monte Carlo simulation results: (i) Lock time to BIST output correlation, (ii) BIST output variation w.r.t. process spread, (iii) BIST output variation w.r.t. PLL duty cycle variation and (iv) CP drive duration required for the corresponding PLL frequencies

Frequency independence is crucial to reusing BIST module across multiple PLLs within the SoC. The BIST stimulus as well as observed PD output is baseband in nature, making it possible to program the scheme for multiple operating frequencies. VCO output frequency is a direct function of the input reference voltage applied and by changing the pulse width of the ATE stimulus applied, a different LF_{out} voltage can be programmed into the DUT. Design simulations can determine the CP charging duration that needs to be provided by the ATE and thus frequency independence is achieved.

Table 6.1 presents the SPICE simulation results when a varying CP

Table 6.1: BIST Scheme Performance for Input Frequency Range

PLL Freq.(MHz)	**CP Drive Duration** (μS)	**Meas at PD o/p** mV
10	8.4	684
50	42	662
100	84	687
200	168	654
250	200	664

stimulus duration is applied to account for different input frequency signals. The observation node voltage (PD_{out} with process stabilized LPF) measured for each of the cases is included. It can be clearly seen that by programming the input pulse duration, consistent results can be obtained with the BIST scheme, confirming the frequency independence. Digital CMOS transistor models used for SPICE simulations were frequency limited and hence data up to $250MHz$ is presented.

This BIST scheme can be easily configured in case of a multi-frequency PLL/multiple PLLs. Individual connections from PD_{out} nodes in each of the blocks under test can be connected to the BIST controller through a multiplexing scheme. Similarly ,a multiplexer activated in test mode for the specific block can be used to route the test stimulus to CP_{in} node.

At-speed testing of PLLs is required to ensure test quality as speed sensitive failure mechanisms may not manifest at lower frequencies. An ATE resource used for receiving PLL output in the conventional lock test needs to operate *at-speed*. This precision hardware effectively increases the test cost.

The proposed BIST uses looped-self-testing for all the high-speed nodes and modules and only a DC baseband signal representing the self-test operation is used for decision making. This eliminates any high-speed requirements from ATE pins interfacing with the DUT. PPMU units are extremely common on all ATE channels/pins on the lowest resource ATE as they used in basic continuity measurements during production testing. Use of basic PPMU pins for BIST output measurement thus simplifies the ATE measurement and decision making of the PLL test and a simple criteria, very similar to typical pin continuity tests can be used on the ATE. The upper and lower measurement limits are determined by the process-split characterization work done during product bring-up phase.

6.3.2 Fault Coverage Analysis

The BIST scheme enables testing of catastrophic, marginal as well as parametric failures in the PLL. A majority of work in the past such as [36, 40] consider fault coverage only for catastrophic failures in the internal digital and mixed signal blocks as parametric test capability does not exist for such schemes. The two fault domains are separately discussed in order to highlight confirmation with the typical coverage as well as additional parametric coverage.

A closed-loop frequency latch test is used in order to observe the fault coverage over the entire circuit. This basic test involves applying the CP input in test mode using short data bursts. The PD output is integrated over

Table 6.2: Catastrophic Fault Coverage Analysis Results

Sub-Block	**Total Faults**	**Faults Detected in Simulation**	**Coverage Percentage**
VCO	156	146	93.58
CP+LF	108	103	95.37
BIST Module	226	222	98.23
PD	780	754	96.67
Total	1270	1225	96.45

a time interval $[0, t'']$ and observed using the PPMU. Successively stable and consistent measurements on the LPF indicate the locked state of the PLL. This method is used in the BIST scheme to avoid using an ATE frequency measurement resource on the PLL output pin.

Stuck-at fault model is considered for PD while a catastrophic fault model is considered for the internal mixed signal blocks. The fault catastrophic detection results are presented in Table 6.2, results are based on SPICE simulation performed under a Perl wrapper injecting faults within the PLL.

Parametric faults are likely to be caused by fabrication marginalities as discussed earlier and the series/shunt path resistances would between the ideal and the catastrophic values in the previous subsection.

Parametric fault coverage can be represented either in terms of passing range of the observed parameters ($USL > PPMU\_out > LSL$) or statistically in the form of repeated convolutions to represent interdependency of the

Table 6.3: Parametric Fault Coverage Analysis Results

Sub-Block	**Total Faults**	**Faults Detected in Simulation**	**Coverage Percentage**
VCO	156	136	87.17
CP+LF	108	97	89.81
BIST Module	226	214	94.69
PD	780	729	93.46
Total	1270	1176	92.59

closed loop system. Due to the closed-loop nature of the individual blocks, the observed integrated PD output can be represented as a sum of convolutions of successive parameters –

$$M[PD_{out}] = \sum_{m=min}^{max} Module_i[m].Module_{i+1}[n-m] \tag{6.11}$$

for $Module_i$: i^{th} module in the closed loop.

Various specification based tests can be used for parametric testing, increasing overall fault coverage for marginalities and reliability hazards. Some faults, such as an open in one of the telescopic arms of the current mirror used in the CP module, may still allow the VCO to be driven to a level where the PLL can be locked. The remaining functional branches may carry additional or uneven current causing electromigration risk during field use of the DUT. This fault may be difficult to screen during a typical lock test but an intermediate value of the PD_{out} can be characterized on various process corners to identify

such moderate low-slope charging devices. Similar characterization can be performed on the measured node to screen out marginal short connections.

Conventional PLL testing in production is limited to testing the PLL locking mechanism and passing the DUT if the PLL locks to the input frequency within t_{lock}. A gross fabrication fault in the PLL would disable the DUT from frequency-locking while a fabrication marginality can cause an abnormality in the lock time. Most of the PLL tests are directed at ensuring $t_{lock} < t_{limit}$ as a rejection criteria while typically no test targets a lower limit on t_{lock}.

Results for SPICE simulation where parametric faults are injected in the same fault model are included in Table 6.3. As the fault model is shared between the two analyses, the overall number of fault locations remain unchanged. Overall, 92.6% parametric fault coverage is provided the BIST scheme, which is satisfactory for a commercial low-cost test.

Parametric testing can provide a screen for marginal parts with marginal shorts as their manifestation into internal parameters is more likely to be detected than the overall system output. A closed loop system may be able to compensate for such marginalities, effectively masking the faults during testing. Driving an input signal at an internal node during test mode and observing the corresponding driver node in a 'opened-close-loop' system provides the ability to perform numerical limit based testing for the internal parameter observed. Test specification can be applied to the PD_{out} signal within the test window to screen out devices where marginal shorts are present within blocks.

6.3.3 Area Overhead and Layout

Layout was implemented using a $90nm$ library where the BIST scheme was included along with a digital programmable PLL supporting 200MHz to 250MHz of operation. The BIST area overhead is $456\mu m^2$, which constitutes 12% overhead for this basic PLL. When combined and shared between with multi-frequency programmable D-PLLs, the overhead drops below 2% [33]. The parametric coverage, scalability, process indepence and the low test resource requirements make this an attractive BIST solution for practical applications.

6.4 All-Digital BIST Solution with Area Optimization

While the hybrid BIST scheme is effective at providing a frequency independent parametric test solution, further use of digital blocks enables reduction in silicon overhead. Absense of analog components also makes it more efficient to implement and integrate into designs. Improvements to the hybrid scheme are shown in Figure 6.7. The input section of the controller consists of an IO pin of the DUT which is used to scan in digital data routed onto the CP input via the test controller. In test mode, the UP/DOWN outputs of the PD block are fed into the controller and are used to drive a programmable counter. The two counters can be output on an ATE IO pin using a FIFO (First In First Out) register for further analysis and comparison. The PD output accumulation is performed over the test duration, which can be programmed by the control signals fed in from the ATE. The PD output signature pulse

counting method is robust and repeatable across process corners, results for which are provided in the later sections. Reliance on a programmable digital BIST controller provides process independence where no analog measurements are required for signature observation and analysis.

When the test mode input is activated, data pulses are forced into the CP input through the ATE IO interface. The test duration of the pulses is maintained constant at 50% duty cycle, operating at the BIST frequency and the count is controlled by the ATE and can be programmed depending on the DUT specifications and characterization results. A pulse applied on CP input connects the CP output node to VDD or ground depending on the input used thus providing a charging or a discharging path to the CP load. The conductivity of the transistors used in the CP block as well as the input pulse duration affects the net charge interchange that can occur during test mode.

6.4.1 Internal Node Access Simulation Results

Monte Carlo simulation results are presented in Figure 6.8 where the impact of PLL lock time and frequency variation on the BIST output is seen.

Figure 6.8–(i) represents the BIST counter simulation results for Monte Carlo simulations corresponding to PLL lock time. Lock state is defined when the PLL output frequency tracks the input within 0.1% accuracy. The counter output value closely tracks the measured lock time with a co-efficient of determination (R^2) value of 0.96. The distribution shows a variance of $\pm 3\%$ around the fit curve, reflecting the close correlation. The counter output, therefore,

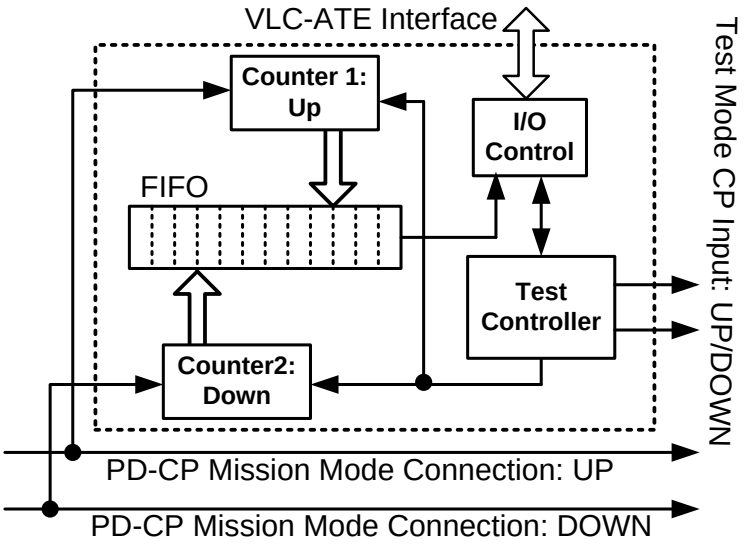

Figure 6.7: BIST Schematic: Digital BIST Controller added between PD and CP

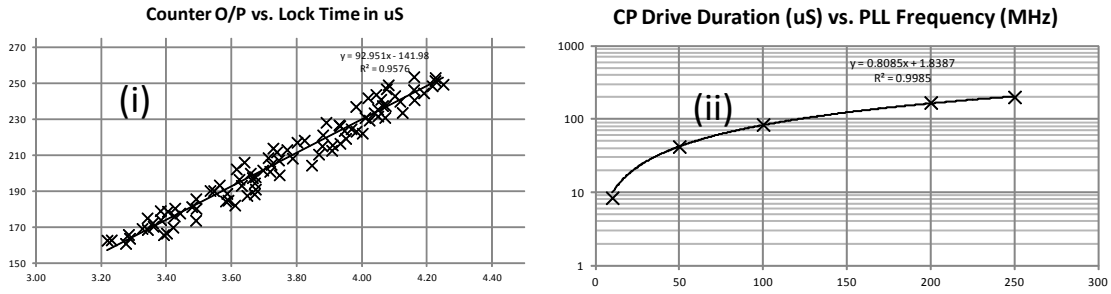

Figure 6.8: Monte Carlo simulation results – (i) Lock time to BIST output counter correlation and (ii) CP drive duration required for the corresponding PLL frequencies

can be used to determine the lock state of the PLL when compared against statistical limits. The counter may be read out in a volume production test environment in order to screen defective PLL modules with lock time outside the acceptance bound.

Statistical correlation between the input CP drive duration and the corresponding PLL frequency is covered in Figure 6.8–(ii). A very high co-efficient of determination (R^2) value of 0.99 indicates close correlation indicating predictable behavior of the BIST module across the input frequency range of interest.

6.4.2 Fault Coverage Analysis and Area Overhead

Similar fault models are used to simulate both BIST schemes and the fault coverage matrix is identical. Layout was implemented using a $90nm$ library where the BIST scheme was included along with a digital programmable

PLL supporting 10MHz to 200MHz of operation. The BIST area overhead is $132\mu m^2$, which constitutes 3.47% overhead for this basic PLL. When combined and shared between with multi-frequency programmable D-PLLs, the overhead drops below 0.5% [33]. The parametric coverage, scalability, process indepence and the low test resource requirements make this an attractive BIST solution for practical applications.

6.5 Improvements Over Existing Work

Multiple approaches towards self testing of PLLs have been proposed in the past with trade off between benefits and BIST overheads. [36] proposes an all digital BIST scheme for testing catastrophic faults in PLLs – though the ATE resources required are limited, this provides a non-parametric gross failure test method. The proposal in [37] digitally programs the CP and observes the loop filter output – we refrain from sampling the VCO input node as a parasitic capacitance added at that node may affect the settling time characteristics. This approach also does not allow a complete self-test of the DUT.

Some of approaches involve addition of duplicate modules or using ATE to provide internal node voltages [38] – this does not completely enable self-test as the stimuli are provided externally. Additional testing may be required for blocks that are not covered with the primary stimulus. As a PLL is a closed loop system, self-testing of the internal modules is optimum as it reduces external resource requirements and is likely to have the minimal test time

overhead. A test controller module is used in [39] can be used to control the CP input in test mode. The PD within the PLL does not drive the CP and hence it is not tested in the loop. [40] proposes a BIST mechanism with a test mode that can select between PLL output fed to the PD as against added line delay. The work presented in [42] attempts to perform parametric testing in addition to simple catastrophic failure testing proposed in many other schemes. All the three schemes presented in this prior work use additional circuits in the feedback loop and would result in a phase shift as well as frequency dependence on the input signal as the at-speed signal in the feedback loop is captured and used. This paper includes a significant improvement over the process compensated scheme in [41] as a completely digital system is used in the BIST controller in order reduce the design and layout complexity.

Chapter 7

PLL Jitter Measurement with BIST Resources

Signal jitter is caused by a variety of sources and may be present in multiple forms. Timing jitter, which corresponds to edge timing uncertainty, is of particular concern as it may cause soft errors in communication systems. Jitter in clock signals affects critical timing edges and resulting errors can be propagated through the circuit. Jitter in data signals reduces the detection opening in signal eye-diagrams, making detection more prone to soft errors in receiver circuits. For video sub circuits, a sub carrier frequency shift would result in incorrect color information being transmitted.

Jitter can be classified as deterministic and random, the deterministic component being predictable as its sources are known and characterized [43, 44]. A voltage supply drop due to supply current may change the conduction cycle of a circuit and effectively add a duty cycle variation which is the added timing jitter. This component is predictable and hence deterministic. Various other factors such as process non-uniformity, specific data patterns etc. can contribute to this type of jitter. Random jitter is caused due to non-deterministic phenomena and can only be characterized statistically. It is usually modeled as a single or multimode Gaussian distribution, indepen-

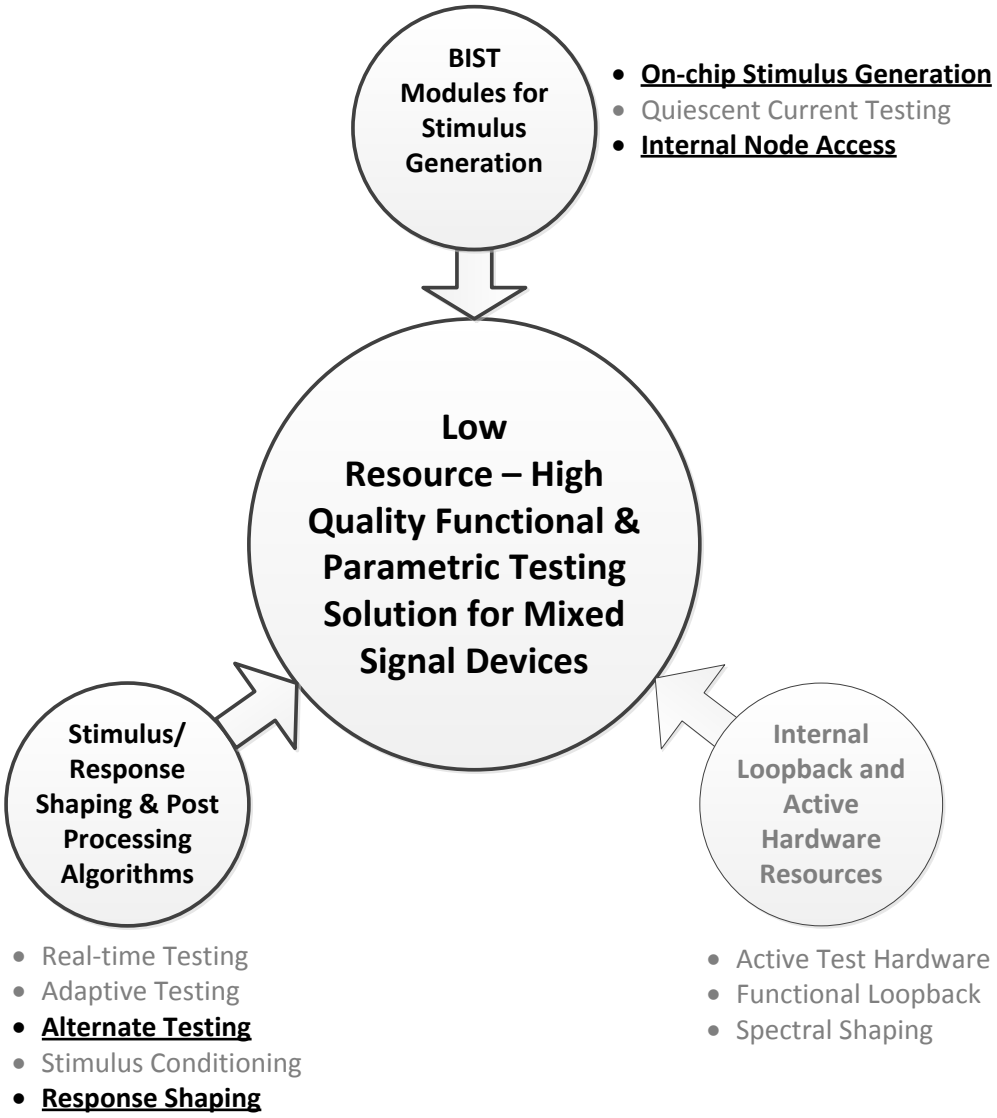

Figure 7.1: BIST Based Scheme for PLL Output Jitter Measurement

dent of any other deterministic factors and is unbounded for a large number of sample points.

Jitter measurement on clock/data signals is a resource-intensive operation as the timing variation introduced due to jitter is typically of the scale of a few pico seconds. A typical low cost ATE does not include the timing sense hardware required for this measurement in production test. The BIST scheme presented in this section generates a voltage representation of this signal. An on-chip housekeeping ADC, typically present on a large percentage of SoC/SiP modules general operations is used to provide a fully digital output to the BIST scheme. An interval-sampling scheme is proposed for high data rates that an on-chip ADC cannot handle. The statistical parameters of a Gaussian distribution are verified using regular at-speed sampling and interval-sampling to ensure that no information is lost and no artifacts are created using this method.

The BIST-supported scheme to enable jitter measurement with minimal ATE resources is represented in Figure 7.1. A combination of on chip measurement modules is used to convert the jitter data in voltage domain and output response shaping methods are used in combination with alternate testing to analyze this response.

Jitter and its effects are a serious concern due to the limited timing margins available in high-speed designs. High speed data communication is severely sensitive to timing edges. Multiple novel methods have been discussed in previous work [45, 46, 47] which involve methods to measure jitter with external hardware. Work has also been done in the area of designing on-chip circuits and developing algorithms to perform some level of jitter measure-

ment on the DUT [48, 49, 50, 51, 52, 53]. A phase frequency detector circuit is used in [48] and jitter measurements are performed without a reference clock. A similar scheme with a reference clock in [49] gives out digitized measured signals. Jitter spectral extraction techniques are discussed in [52] with MATLAB results. A time-to-voltage conversion approach followed in [46, 53] attempts to generate a voltage signal to represent the timing variation.

The scheme is geared towards optimizing the silicon overhead while providing independence from process variation. Compatibility with VLC-ATE and reuse of existing on-chip hardware capabilities is considered in order to maintain the test cost low.

7.1 Jitter Measurement Scheme Overview

Timing variation in a clock or data signal is typically of the order of a few pico seconds and hence a very small fraction of the actual period of the affected signal. Due to this nature of period jitter, high precision timing measurement hardware is required to accurately measure and characterize signal jitter. Typical timing generation/measurement circuitry present on premium ATE typically cannot perform these measurements, which requires additional precision timing hardware, increasing the ATE cost. While pico-second-scale timing measurements require precision circuitry, the voltage generation and measurement systems provided on typical ATE can measure signals of the order of a few nano volts. A scheme is hence used to represent the jitter timing variation in terms of a voltage signal, where the voltage is a function of the

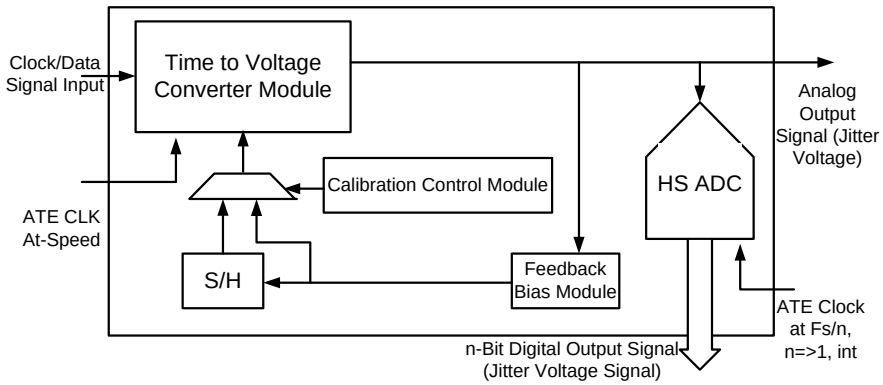

Figure 7.2: System Level Schematic for BIST Jitter Measurement Scheme

timing variation. Since the jitter timing variation is a small fraction of the signal frequency, adequate voltage resolution is provided by using reference voltages derived from SPICE simulations. A band-gap voltage source can also be used for internal voltage reference if the process technology used allows the dynamic voltage value.

Figure 7.2 represents the top level schematic of the BIST scheme; details for the building blocks are covered later in this section. The input signal/clock is fed to the time-to-voltage converter module which generates a voltage signal proportional to the timing jitter present in the input. The Gaussian nature of jitter in the input signal would be maintained as the time-to-voltage converter has a linear response to the input timing variation. The slope of this transformation is a function of the resolution of the converter and process variations, as it may affect the current drive of the constant current source used inside

the converter.

A reference voltage is provided to the converter based on the process corner analysis done in SPICE simulations, which improves resolution, and the dynamic range can be made to cover the entire supply-to-ground rail voltage range available. Programmable constant current source described prior in this dissertation is used in the Time to Voltage Converter (TTVC) module to provide a process stabilized current source.

The calibration control module provides the control signals required to perform process-independence calibration and then switches over to mission mode when the actual time-to-voltage conversions for the input clock begin. The control module thus switches over to the sample-and-hold (S/H) circuit to provide the set bias voltage once the calibration process is complete. The jitter measurement circuit is then put into mission mode where an analog voltage, proportional to the timing jitter value present in each cycle of the input signal, is produced at the output of the TTVC. As the duty cycle of the input signal is used as a charging switch to the capacitor, any jitter present in the signal affects the charging duration of the capacitor. It is expected that this δT_{charge} value would be a fraction of the overall time period, producing a small δV_{cap} across the capacitor. To ensure that an adequate resolution is available for this δV_{cap}, a reference voltage is used to bias the ADC V_{low} node based on the process variation results obtained in SPICE simulations.

An on-chip flash ADC is used to perform digital conversion of this signal so that a digital output representing the input jitter can be obtained

on-chip. Flash ADCs are not commonly used for low-speed operations due to the area overheads, and the Successive Approximation ADCs (SA-ADC) used typically have sampling rates which may be below the requirements for high speed clock/data signals. If a slower housekeeping ADC such as SA-ADC is available on the SoC/SiP, an interval-sampling scheme can be used. If the data/clock signal being processed is at the frequency of F_{signal}, the ADC sampling frequency is set to F_{ADC} where F_{signal} is an integral multiple of F_{ADC}, both signals being synchronous in the time domain. For example, for measuring a 200MHz signal, an ADC clocked at $\frac{200}{n}$MHz synchronous clock is used. Thus a lower sampling rate is used, which results in discarding of some of the samples without the loss of information about the distribution. This marginally increases the test time as a longer jitter-voltage-string has to be captured for the same confidence level in measurements, but use of significantly lower cost ATE compensates for the added test time.

If an on-board ADC is not present on the DUT, the analog output of the time-to-voltage converter can be measured using the analog instrumentation of the ATE. Depending on the data rate of the input signal, either the PPMU or analog measurement resources can be used for higher speeds. Though not as cost-effective as using a digital low cost ATE, this has a significantly lower cost than conventional jitter measurement systems, as it eliminates the high cost of the precision timing circuitry needed for jitter measurement.

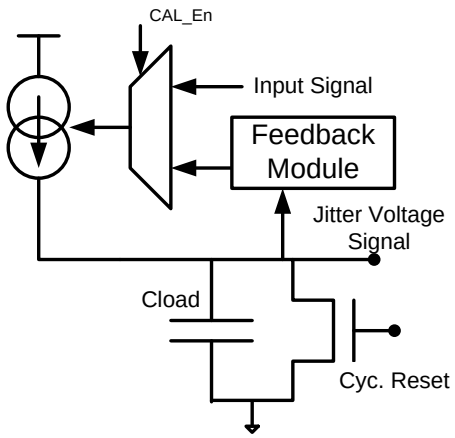

Figure 7.3: Time to Voltage Converter Module with Feedback for Process Independence

7.2 Time-to-Voltage Converter Module

The time-to-voltage converter can be represented at the system level as shown in Figure 7.3. When the input signal jitter is required to be measured in mission mode, the input is used to drive/control a constant current source which charges a capacitor. As the input signal phase drives the transmission gate which acts as a switch to the capacitor, the charge stored on the capacitor is proportional to the duty cycle of the signal. A reset signal is applied to the capacitor to discharge it between two successive cycles. Functionally, a ramp generator, with its ramp amplitude controlled by the input signal, is used to generate the voltage representation of the jitter signal. Figure 7.4 includes SPICE simulation results for the TTVC-plot (a) represents the TTVC

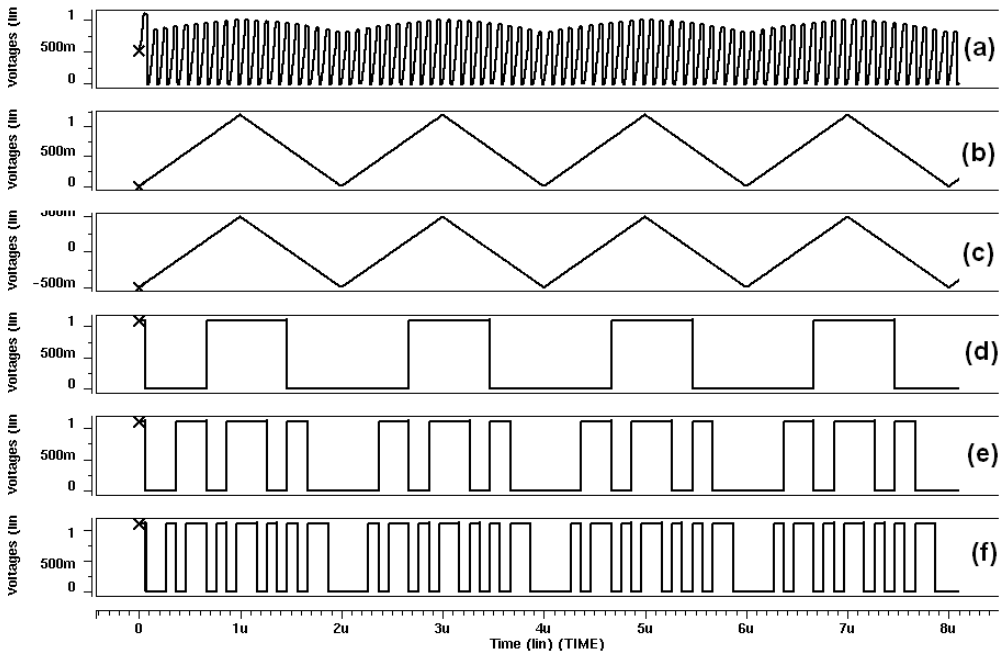

Figure 7.4: Analog and Digital waveforms of the Time-to-Voltage Converter. a) TTVC output for ideal waveform modulated with ramp jitter. b) Jitter waveform converted to 0 to Vdd format. c) Actual jitter waveform output by TTVC. d/e/f) ADC output representing per cycle jitter.

input signal with an ideal waveform modulated with a ramp jitter signal. (b)/(c) represent the added jitter and the zero-centered version of it which is used to generate the simulated input. Plots (d)/(e)/(f) represent the 3-bit TTVC output signal where the input jitter signal is converted to its binary representation.

7.3 Undersampling/Interval-Sampling

When data is collected sequentially and processed without any sorting, the random nature of the data is preserved. The Gaussian nature of the jitter samples collected and its statistical parameters remain constant if a subset of data is obtained by undersampling the parent data-set. A large sample size and random nature of recorded data is required to validate this assumption. This is verified in simulation by generating a string of 1 million data points of Gaussian-random nature in Matlab which is then sampled at $\frac{R_{data}}{100}$ and the graphical representation as well as statistical parameters are compared. Figure 7.5 contains the graphical distributions while Table 7.1 contains the statistical parameters.

The TTVC module is capable of handling high data rates for jitter waveform generation. The circuit was simulated for frequencies up to $1GHz$ by changing current bias and load capacitor values. On-chip ADCs present on most of the SoC/SiP modules cannot operate at such high speeds and a compromise can be reached where the ADC is clocked at a frequency which is $\frac{1}{n}$ times the data rate where n is an integer. Though this results in an increase in test time as more signal cycles need to be captured, it does not result in data distortion or data loss artifacts as seen in the Gaussian-random distribution statistics above.

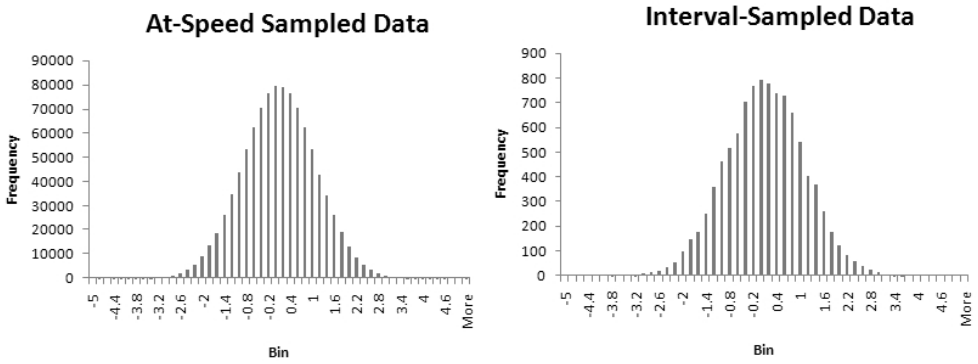

Figure 7.5: Histograms for At-speed and Interval Sampled Gaussian Dataset

Table 7.1: Statistical Comparison of At-speed and Under-sampling Methods

Parameter	**At-Speed Sampled**	**Under-sampled**
$Std.Dev.$	0.9992	0.9998
$Mean$	-0.00232	-0.00265
$Median$	0.00292	0.00345
$Min.$	-4.9983	-4.9985
$Max.$	4.9989	4.9987

7.4 Simulation Results

The jitter measurement BIST scheme is tested as depicted in Figure 7.2 with an ideal clock signal injected with a linearly varying jitter. The time period T_{per} of the input signal varies linearly between $T_{per} - \delta$ to $T_{per} + \delta$, and vice versa, repeatedly and waveforms captured for four such cycles are represented in Figure 7.4 with a 3-bit on-board ADC. The TTVC output ramp is modulated by the input signal jitter as can be seen in the first plot. The variation in input signal period provides different charging durations for the load capacitor. The ADC reference voltages are provided by V_{ref} values obtained from SPICE simulations for all three process corners.

The circuit is also characterized across a range of input frequencies and corresponding percentage jitter signals are added. An SoC/SiP may have either multiple PLLs or a single programmable PLL operating at multiple frequencies that need to be characterized and having the ability to perform accurate jitter measurements for multiple frequencies with a single BIST IP may be crucial for the BIST scheme. Gate widths in the current source in the TTVC as well as the load capacitance used for converting period variations into a voltage signal greatly affect the bandwidth of the input signal that can be accurately measured for jitter. If the current source and load capacitance are designed for a frequency F_{nom}, the feedback network needs to adjust the value of the current through the charging circuit to maintain constant ramp slope at the end of calibration period. For a frequency $F_{nom} - \delta$, where δ is a very large number, the feedback voltage may need to trim the current excessively

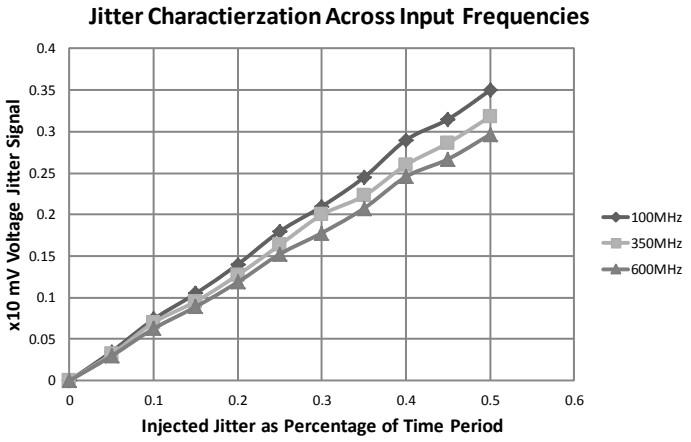

Figure 7.6: Jitter Voltage Generated by TTVC for Different Percentage Jitter for Three Input Frequencies

and can drive the gating transistor into cut-off, disabling the current charging process. Similarly, it may not be possible to limit the current to maintain the constant slope for a frequency $F_{nom} - \delta$ if the transistor is saturated before the feedback circuit negative correction can be applied.

Figure 7.6 represents the voltage jitter signals measured across a frequency range for varied percentages of jitter induced in the corresponding signal. The current source and capacitor values were designed for the median frequency of interest and the marginal variation between the three plots, even after using the hybrid feedback, can be seen in the plots. The slope differences cannot be ignored when the frequencies are higher orders of magnitude of each other, and some other form of programmability may be needed with a potential capacitor bank where the load could be selected depending on the

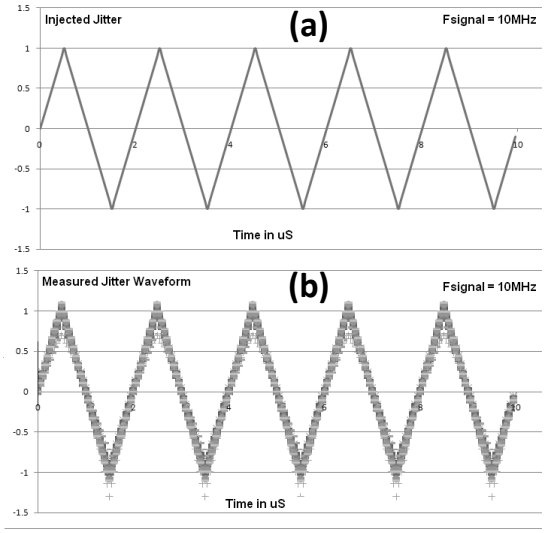

Figure 7.7: Voltage Representation of Injected Jitter in Figure (a), Measured Output Jitter Voltage Signal over Multiple Cycles (b). Measurements performed at 10MHz

input frequency using some type of logic selection. Current source drive can be similarly programmed if a wider range of frequencies is targeted.

The BIST scheme has a repeatable response with minimal hysteresis as seen in Figure 7.7, where multiple measurements of the output jitter voltage signal are plotted against time. Figure 7.7–(a) representes the inserted jitter and Figure 7.7–(b) represents the output response with variation from the triangular input waveform.

7.5 Jitter Testing in Production Environment

Histogram methods are commonly used in production jitter testing where jitter timing variation on a predetermined number of signal cycles is measured and analyzed. Various criteria may be applied in order to screen out potentially problematic parts. Some of the jitter test methods have absolute limits defined where any jitter measurement exceeding the limit value results in rejection of the part. Outlier screening methods may also be utilized where apart from the absolute limit, a percentage limit is defined dynamically from the measured values and any measurement which falls outside a 6σ result in rejection of the part. The outlier method is more commonly used in communication circuits as any data loop has a tolerance limit specified in terms of BER which can be reliably defined by using outlier methods of jitter measurement and sorting. The scheme proposed in this paper is compatible with outlier analysis as it captures an array of jitter voltage measurements on successive cycles and this data can be analyzed using the computing resources of the ATE without any significant overheads.

The BIST scheme can be used for performing jitter measurements over a a range of input frequencies. The use of on board ADC can enable complete production quality testing of signal jitter using purely digital ATE, as the ADC outputs can be observed on external pins. In case an ADC is not available, the alternative scheme provided in this paper can be used, where PMU/ analog measurement resources on the ATE are utilized to record the analog jitter voltage signal, and it can be processed by using the computing capability

available in the ATE. This BIST solution therefore provides a low-cost ATE alternative to a typically resource intensive test.

Chapter 8

Arbitrary Waveform Generator Response Shaping Method

Mixed signal parametric testing is resource intensive and requires high-precision sources. Precision requirements for test instrumentation are driven by the CUT specifications and are required to ensure minimal test escapes or excessive fallout due to source generated artifacts. Stringent accuracy requirements for the arbitrary waveform generator (AWG) modules on ATE drive the high hardware costs. A linearity correction methodology is presented in this chapter to compensate for linearity distortion present in the analog source generator to eliminate the resulting artifacts that can cause false test results. This method can be used to reduce the linearity specifications for AWGs present in the VLC-ATE systems.

Mixed signal circuits are tested against parametric performance criteria which may be resource intensive. The performance criteria are application specific and involve linearity as well spectral specifications. Stimulus generation resources need to be vastly superior to the CUT (perfectly linear in the required voltage range and free of spurious tones in the required frequency range) to ensure that the CUT does not fail due to artifacts produced by

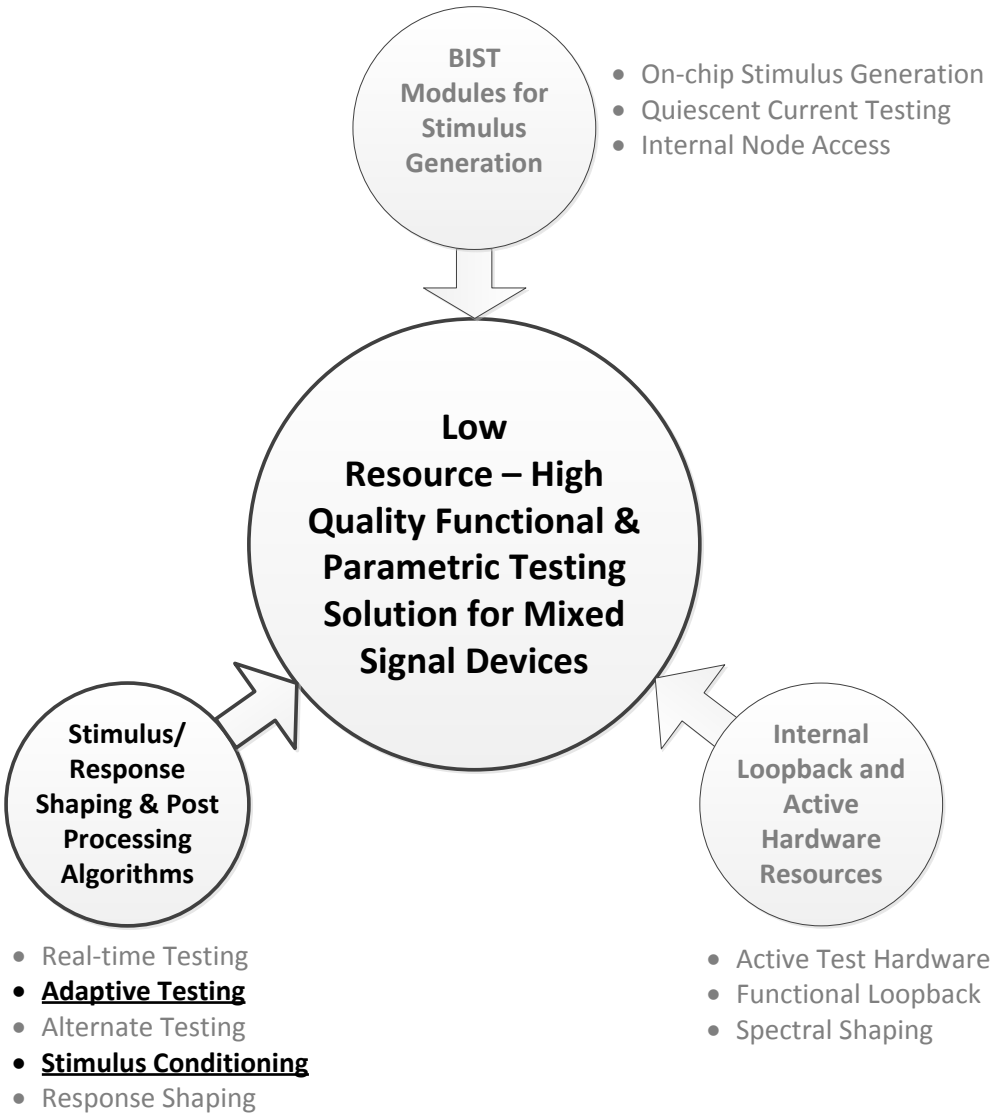

Figure 8.1: AWG Compensation Scheme to Enable ADC Testing with Low Cost Resources

non-ideal test stimulus.

AWG modules are programmable and are available on ATE to generate a variety of analog stimuli for ADC testing, while DSP modules are used for response analysis [54]. Linearity and spectral characteristics of AWGs are critical as any inherent imperfections in the ADC input stimulus result in artifacts in the ADC output. While the output is affected due to non-idealities in the input stimulus, the effect is deterministic. The scheme introduces a calibration based correction factor that is applied to the response analysis to compensate for AWG linearity and spectral imperfections. AWG modules on VLC-ATE thus can be chosen with a relaxed linearity and spectral purity criteria which effectively results in a lower cost. The method is made suitable for mass production environments by reducing the calibration requirements. The correction factor calculation is performed in a calibration routine at the beginning of a production run and the values can be retained over a volume of DUT. This overhead is typically acceptable and similar to the existing calibration routines that are used in manufacturing environments.

The scheme to enable production quality ADC testing using practical noisy AWG modules is represented in Figure 8.1 – stimulus conditioning methods are used to enable adaptive testing using low cost ATE instrumentation.

AWG modules require complex topologies of Digital to Analog Converters (DACs) which can be digitally programmed by the ATE to generate the required analog signal. The digital interface is required to implement complex DSP algorithms in analog domains. The DAC module suffers from inherent

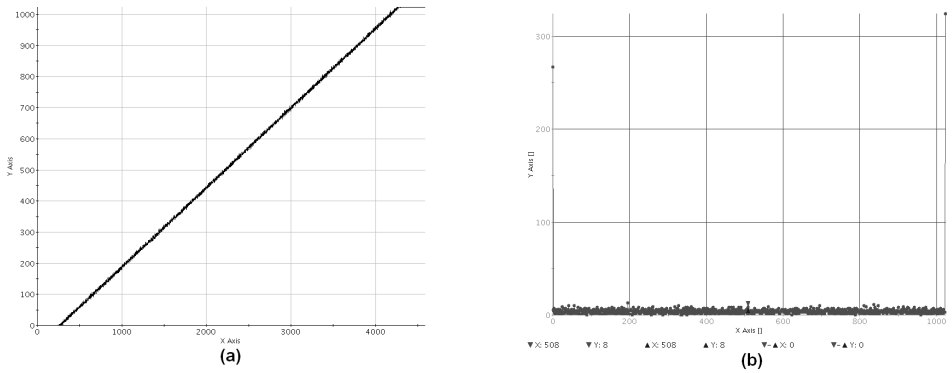

Figure 8.2: ADC Ramp Input [Figure (a)] and Histogram Analysis for Output Response [Figure (b)]

limitations; linearity/spectral performance may be impacted as a result. [55] proposes a compensation scheme for AWG DAC non-linearities with hardware modifications involved, limiting application for existing VLC-ATE.

Methods to discriminate between error sources have been considered in [56, 57]. While [56] method has limited applications due to the application to specific ADC types, [57] attempts to enable discrimination by effectively analyzing a differential response. While effective at discriminating errors, it does not offer a generalized solution for production environments. A 2-ADC configuration may not always be present in a test topology, limiting its applications.

Kerzerho [58] presents experimental results for a method to estimate AWG spectral components using a 2-ADC method. While this technique is effective in spectral noise prediction of the AWG, use of a 2-ADC configuration may limit its practical applications, similar to [56, 57].

8.1 Linearity Testing of ADCs

Histogram method is most commonly used for production linearity testing of ADCs [5, 6, 59] while other efficient methods have been proposed [60]. Histogram analysis method provides a linear ramp signal to the CUT and records an output vector in the ATE memory which is then processed to calculate the INL and DNL values. Any inherent non-linearities in the ramp source impact the histogram distribution, resulting in erroneous INL/DNL measurements.

Histogram analysis uses the bin frequencies for each voltage step to determine the INL/DNL values. For an n-bit ADC, the maximum output code corresponds to the rail voltage with 2^n steps. Each *'voltage step'* corresponds to $\frac{1}{2^n}$ of the rail voltage and is the smallest measurable unit considering during test. For a bin i, the number of ADC measurements corresponding to the particular voltage test bin can be denoted as $H_c[i]$. A sample ramp signal applied by the ADC and the corresponding captured histogram and are shown in Figure 8.2. While a DC signal is applied for a finite duration causing $H_c[0]$ and $H_c[2^n]$ to be higher than the remaining, remaining bins should have a measurement count which equals the hits per code (HPC) setting of the input ramp signal.

$$H_c[i] = HPC, \tag{8.1}$$

for $0 < i < 2^n$ This ideal output vector can be represented as –

$$[H_c[0], H_c[1], H_c[2], ..., H_c[n-2], H_c[n-1], H_c[n]] \tag{8.2}$$

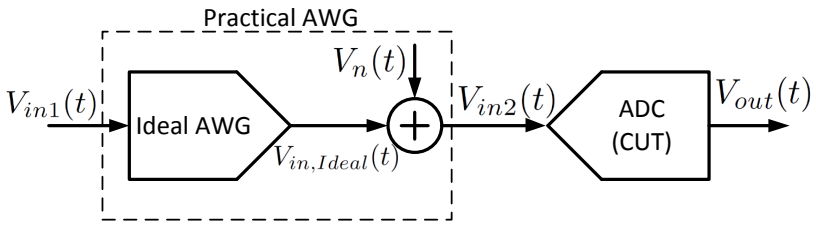

Figure 8.3: ADC Test Scheme with Ideal and Practical AWG

Practical AWG can be modeled as the topology in Figure 8.3 where a perfectly linear source $V_{in,Ideal}(t)$ is injected with a time domain noise signal $V_n(t)$ producing an effective stimulus signal $V_{in2}(t)$ which is fed to ADC. Non-ideal AWG modules available on VLC-ATE can be modeled as Figure 8.3 where noise components impact linearity of the stimulus. The non-linear AWG output $V_{in2}(t)$ can be decomposed into the linear ramp and the noise –

$$V_{in2}t = V_{in1}(t) + V_n(t) \tag{8.3}$$

The noise signal $V_n(t)$ can be modeled to represent non-ideal behavior which can manifest itself as INL, DNL, offset or gain errors. This results in an error $P_{\epsilon i}$ in the bin count $H_c[i]$ for the i_{th} bin of the histogram. The bin frequency error can be represented as a vector given by,

$$[P_{\epsilon 0}, P_{\epsilon 1}, P_{\epsilon 2}, ..., P_{\epsilon n-2}, P_{\epsilon n-1}, P_{\epsilon n}] \tag{8.4}$$

This error matrix generated is due to variation in the transition levels as the ideal ramp and the noise signals contribute to this variation. In absence

of the noise signal $V_n(t)$, the code transition levels are given by,

$$T_(r - ideal, k) = \frac{\sum_{j=0}^{k-1} C_j}{\sum_{j=0}^{N-1} C_j} \tag{8.5}$$

for an n-bit AWG. The noise signal imparts a transition error with the effective transition levels represented as,

$$T_(r - Noisy, k) = \frac{\sum_{j=0}^{k-1} C_j}{\sum_{j=0}^{N-1} C_j} + \epsilon_k \tag{8.6}$$

Characteristics of the error signal ϵ_k are driven by $V_n(t)$ and not analyzed in depth in this work. Impact of linearity errors in AWG can be analyzed by considering the waveform in Figure 8.4, where the AWG step size is enlarged to show details. Ideal AWG step signal is shown along with the noisy AWG signal $V_{in2}(t)$. Ideal level transition between steps j and $j+1$ is represented by the distance $[V_{in1}[j+1] - V_{in1}[j]]$ while the AWG response results in step size of $[V_{in2}[j+1] - V_{in2}[j]]$. The area contained between the two plots is responsible for the noise components added.

Figure 8.4(a) shows AWG response that results in a marginal DNL error contribution while each deviation from the ideal curve contributes to INL, therefore resulting in a large INL error. The error matrix calculated for this AWG behavior accounts for the individual step contribution to INL by assigning a sign as a function of leading or trailing nature of the AWG response. If V_{step} is the voltage step size, the INL contribution by the step transition from j to $j+1$ is given by,

$$A_{j,j+1} = V_{step} \times [V_{in2}(j+1) - V_j(j)] \tag{8.7}$$

Considering the impact of a total of m steps that lead the idea response, if $f(n)$ represents the AWG response curve,

$$A_{j,j+1} = \int_{V_{in2}[j]}^{V_{in2}[j+m]} f(x) \times dx \times [(j+1) - (j)] \tag{8.8}$$

$$A_{j,j+1} = f(\overline{x}) \times [V_{in2}(j+1) - V_j(j)] \tag{8.9}$$

As it can be seen from the nature of the waveform, the impact to INL is accumulative and such lead-only or lag-only trend results in a high INL while testing the DUT. Error matrix generated for behavior similar to Figure 8.4(a) contain all-positive or all-negative elements.

In Figure 8.4(b), the AWG response partially leads and lags the ideal curve and the overall area of overlap is represented the equation where the contributions due to lead and lag are assigned a sign,

$$A_{0,N} = \int_{V_{in2}[j]}^{V_{in2}[j+m]} f(x).dx \times [(j+m) - (j)] \tag{8.10}$$

$$- \int_{V_{in2}[j]}^{V_{in2}[j+m']} f(x).dx \times [(j+m') - (j)] \tag{8.11}$$

The area of overlap between the two curves thus defines the overall linearity impact; while the integral over a quantization step represents individual error matrix contents.

The error vector is calculated during the pre-production calibration process where the AWG is characterized to define the corresponding error vector which is stored in the ATE. This calibration process is similar to the existing production practices where analog source/receive modules are characterized

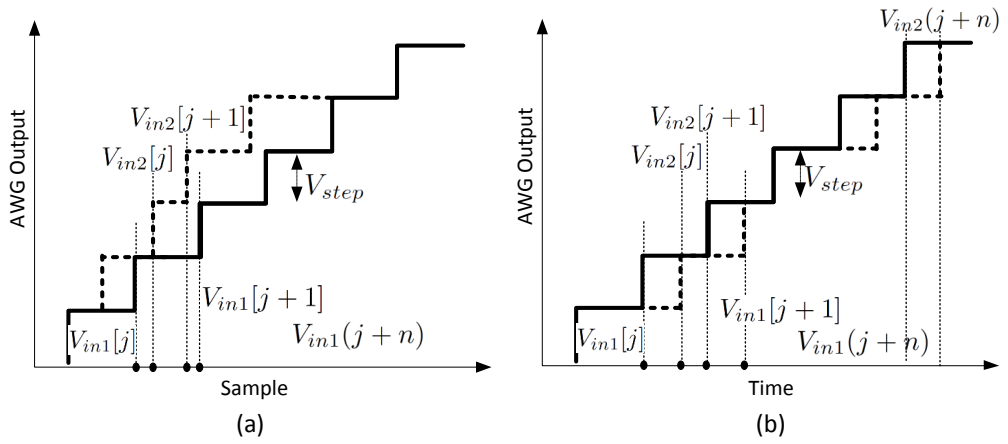

Figure 8.4: Ideal AWG Step vs. Noisy Ramp

and calibrated with a finite recurrence prior to production testing of DUT. For an n-bit ADC that is being tested by a m-bit AWG DAC, minimum HPC count is $(m-n)^2$ for an ideal AWG due to the quantization error. The AWG resolution requirement is driven by the DNL tolerance as the quantization voltage step $1/(m-n)^2$ results in a measurement error.

If C_i is the HPC count for the ideal test environment, the error vector in equation 8.4 has an upper bound that is defined as –

$$P_{\epsilon i} \leq \eta \tag{8.12}$$

where, $\eta \leq (m-n)^2$, for all $i = 0, ...n$.

This matrix operation represents the error signal $V_n(t)$, which can also be calculated on the basis of the spatial differences when the two signals are plotted.

The proposed method pre calculates this error matrix and a correction factor is applied to the output matrix before calculating the linearity parameters.

$$\left(H_{DUT}\right) = \begin{pmatrix} H_c[0] \\ H_c[1] \\ .. \\ .. \\ H_c[n-1] \\ H_c[n] \end{pmatrix} + \begin{pmatrix} P_{\epsilon 0} \\ P_{\epsilon 1} \\ .. \\ .. \\ P_{\epsilon n-1} \\ P_{\epsilon n} \end{pmatrix} \tag{8.13}$$

The learning and production flow for the AWG Response Shaping (ARS) is shown in Figure 8.5. Error vector is generated in the AWG calibration phase where the data is stored in the ATE memory in order to shape DUT response. The volume production run uses this stored data. The production test can be made compatible with adaptive test techniques where systematic linearity fails seen across successive devices can be used as a flag to re-iterate the pre-production calibration stage.

8.2 Simulation Results

A 16-bit DAC model is used as the AWG and a 12-bit ADC is used as the DUT to evaluate the proposed scheme, the ramp generator is first characterized using the plan of record (POR) AWG resolution. Linearity measurements obtained for the ADC under test with the POR AWG are recorded as the benchmark. The DUT linearity performance is reflected by the measurements in the 'Ideal AWG' column in Table 8.1. When a noisy AWG signal with 4-bit lower resolution than ideal is applied to the ADC, effective INL/gain/offset and

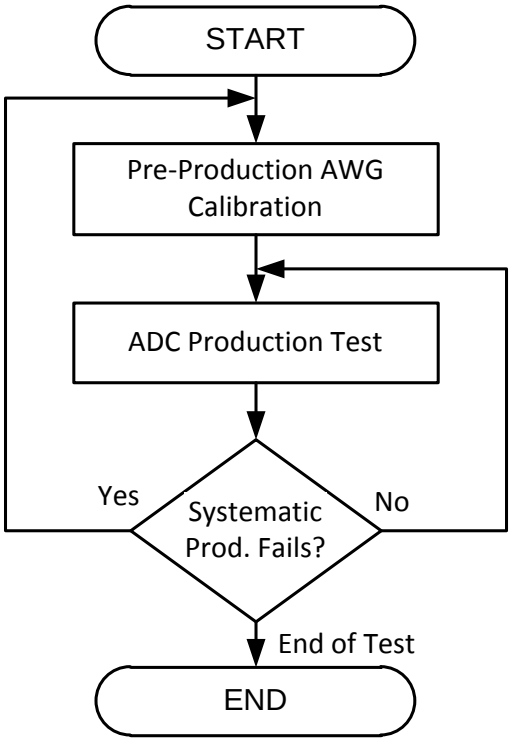

Figure 8.5: AWG Calibration and Production Flow

HPC measurements are largely unaffected. The DNL error maximum value reported is inflated due to the additional quantization noise with the reported error at 3.47. On applying the correction factors with the ARS method, the calculated DNL is reduced to 1.75, which is approximately 3% of the ideal measurement. Similarly, a noisy AWG signal with an inherent offset error is applied to the ADC to compare the ARS performance. AWG offset error results in an INL failure for the ADC as the marginally higher DNL is accumulated over the entire ramp stimulus range. The excessive INL error is adjusted by applying ARS as seen in Tables 8.1 and 8.2.

Results for Monte Carlo analysis are show in Figure 8.6 with the following variables included:

1. **DUT:** 12-bit ADC model where parameters are skewed to cause 20% variation from median

2. **AWG source:** 16-bit DAC where dither is added to introduce noise. AWG linearity is modified for up to +/- 4-LSB DNL error and +/- 16-LSB INL error.

ADC linearity is measured under two conditions: the first case where the AWG does not include the injected non-linearities and the second case with the non-linearity inject while enabling the ARS scheme compensation. Identical ADC model corner is used for the corresponding measurements. The ADC linearity performance is seen in the scatter plots with the trend included

Table 8.1: ADC Linearity Test simulation results – 4-bit AWG Quantization Error

Parameter	**Ideal AWG**	**Practical AWG - Without ARS**	**Practical AWG - With ARS**
INL	2.14	2.32	2.21
DNL	1.81	3.47	1.75
Gain	2.20	2.37	2.31
Offset	−2.875	−2.798	−2.806
HPC	14.91	15.08	14.98

for reference. The Monte Carlo results are thus used to validate the ARS scheme across ADC model variation.

The results for AWG waveform characterization and the Monte Carlo simulation with ARS system in Figure 8.6 indicate that the proposed compensation scheme is effective at eliminating the output artifacts resulted due to AWG source non-linearity. This procedure may be used for ADC testing in production environments where a non-ideal AWG can be used to reduce test resource cost.

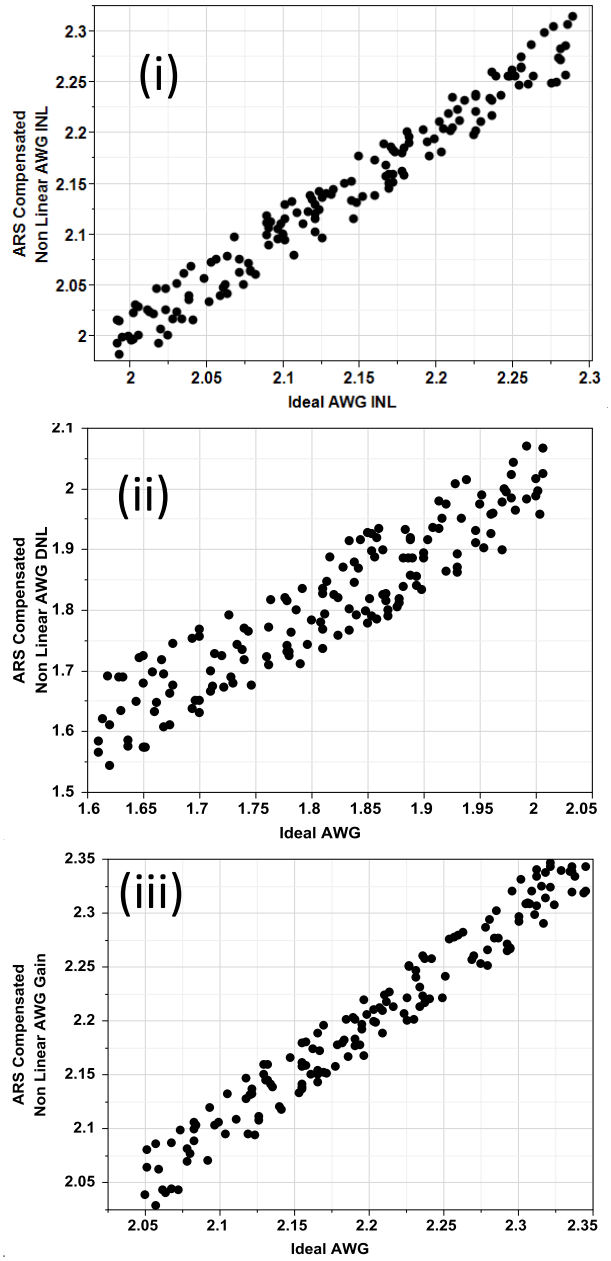

Figure 8.6: Monte Carlo Results with ADC response to ideal AWG plotted on Y-axis, response to ARS compensated noisy AWG. Figure(i) includes DNL performance, Figure(ii) includes INL performance and Figure(iii) includes offset performance

Table 8.2: ADC Linearity Test simulation results – 4-bit AWG Offset Error

Parameter	**Ideal AWG**	**Practical AWG - Without ARS**	**Practical AWG - With ARS**
INL	2.14	19.63	2.23
DNL	1.81	4.38	1.92
Gain	2.20	2.09	2.27
Offset	-2.875	-7.10	-2.837
HPC	14.91	14.87	15.02

Chapter 9

Conclusions and Closing Remarks

Modern commercial semicondutor testing requires balance between cost and quality, which can be in conflict with each other. Modern processors running at multi-GHz processors may require high speed functional tests that push the speed requirements for ATE resources. Modern communication standards pose specific temporal and spectral criteria that need to be met by mixed signal modules, which drives ATE resource complexity and cost. Silicon fabrication cost per device has been reducing progressively with the modern deep sub-micron while the test equipment cost has increased linearly.

The low resource semiconductor test solutions were developed bottom-up where the constraints of lower cost testing are addressed while utilizing the benefits of lower cost fabrication and digital signal processing capabilities. A variety of complimenting methods and modules is used to achieve optimization between cost and quality. Resources such as silicon overheads for BIST modules or data post processing algorithms are utilized to compensate for the high cost test hardware.

Importance of developing process-compensated BIST schemes needs to be reiterated at this point – a BIST scheme needs to operate across the produc-

tion process and temperature window to be effective in volume semicondutor testing. Feedback based self-calibrating systems were designed with this critical requirement in mind and Monte Carlo simulations were extensively used in order validate this behavior.

Methods for low-cost high-quality testing proposed in this dissertation have been extenstively simulated using Monte Carlo simulations and regression analysis. Experimental silicon data collected using *HP-93000* ATE system and NI ELVIS bench has been presented to support the algorithms proposed. I believe that this dissertation provides novel and effective methods that can be implemented to enable low resource testing while maintaining high test quality for commercial semiconductor devices.

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Vita

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